PSOC™ Control C3 MCU registers

Reference manual

About this document

Scope and purpose

This reference manual lists all the registers in the mapping tables of the PSOC™ Control C3 MCU in address order. For architecture details, see PSOC™ Control C3 MCU architecture reference manual.

Intended audience

This reference manual is intended for the embedded hardware engineers, software developers, and system architects who want to understand the register details of the Infineon PSOC™ Control C3 series of microcontrollers.

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Register mapping

The register mapping section discusses the registers of the PSOC™ Control C3 MCU registers device. This document should be used in conjunction with PSOC™ Control C3 MCU architecture reference manual. The register mapping section lists all the registers in mapping tables, in address order.

Register general conventions

The register conventions specific to this section and the Register Reference chapter are listed in this table.

Convention	Description	Explanation
'x' in a register name	ACBxxCR1	multiple instances/address ranges of the same register
R	R: 00	read register or bit(s)
W	W: 00	write register or bit(s)
W1C	W1C:0	write one to clear
W0C	W0C:0	write zero to clear
W1S	W1S:0	write one to set
RC	RC:0	read to clear
WC	WC:0	write to clear
NA	NA:000	reserved
U	R:U	undefined
00	RW: 00	Reset value is 0x00
XX	RW: XX	Reset is not reset

Acronyms

This table lists the acronyms used in this reference manual.

Table 1 Acronyms

Symbol	Unit of measure
AES	advanced encryption standard
AMUX	analog multiplexer
BLDC	brushless direct current
BOD	brownout detect
CAN	controller area network
CORDIC	coordinate rotation digital computer
CSV	clock supervision
DAC	digital to analog converter
DFU	device firmware upgrade
DSI	digital signal interconnect
DSP	digital signal processor
DMA	direct memory access
ECC	error correcting code

Acronyms

Table 1 Acronyms

Symbol	Unit of measure
ECO	external crystal oscillators
ETB	embedded trace buffer
ETM	embedded trace macrocell
FET	field effect transistor
FIFO	first in, first out
FOC	field-oriented control
FPU	floating point unit
GPIO	general-purpose input/output
HPPASS	high-performance programmable analog subsystem
HRPWM	high-resolution pulse width modulator
HSIOM	high-speed I/O matrix
I-cache	instruction-cache
I2C	inter-integrated circuit
IHO	internal high-speed oscillator
ILO	low-speed oscillator
IMO	internal main oscillator
IPC	inter-processor communication
IRQ	IRQ interrupt request
ISR	interrupt service routine
LPCOMP	low-power comparator
LUT	lookup table
LVD	low-voltage detection
LVTTL	low-voltage transistor-transistor logic
MCWDT	multi-counter watchdog timer
MPU	memory protection unit
NVIC	nested vectored interrupt controller
PAL	programmable array logic
PLD	programmable logic device
PLL	phase-locked loops
POR	power-on reset
ROM	read-only memory
RSA	rivest-shamir-adleman, a public-key cryptography algorithm
RTC	real-time clock
RWW	read-while-write
S/H	sample/hold
SAR	successive approximation register
SAU	secure attribution unit
SCB	serial communication blocks

Acronyms

Table 1 Acronyms

Symbol	Unit of measure
SHA	secure hash algorithm
SPI	serial peripheral interface
SRAM	static random access memory
SRSS	system resources subsystem
TCPWM	timer/counter pulse-width modulator
TRNG	true random number generator
UART	universal asynchronous transmitter receiver
WCO	watch crystal oscillator
WIC	wakeup interrupt controller

1 CPU Subsystem (CPUSS) registers

This section discusses the CPUSS registers. It lists all the registers in mapping tables, in address order.

1.1 Register details

Register	Address	Description
RAMC_PPU0_PWPR	0x42100000	Power Policy Register
RAMC_PPU0_PMER	0x42100004	Power Mode Emulation Register
RAMC_PPU0_PWSR	0x42100008	Power Status Register
RAMC_PPU0_DISR	0x42100010	Device Interface Input Current Status Register
RAMC_PPU0_MISR	0x42100014	Miscellaneous Input Current Status Register
RAMC_PPU0_STSR	0x42100018	Stored Status Register
RAMC_PPU0_UNLK	0x4210001C	Unlock register
RAMC_PPU0_PWCR	0x42100020	Power Configuration Register
RAMC_PPU0_PTCR	0x42100024	Power Mode Transition Configuration Register
RAMC_PPU0_IMR	0x42100030	Interrupt Mask Register
RAMC_PPU0_AIMR	0x42100034	Additional Interrupt Mask Register
RAMC_PPU0_ISR	0x42100038	Interrupt Status Register
RAMC_PPU0_AISR	0x4210003C	Additional Interrupt Status Register
RAMC_PPU0_IESR	0x42100040	Input Edge Sensitivity Register
RAMC_PPU0_OPSR	0x42100044	Operating Mode Active Edge Sensitivity Register
RAMC_PPU0_FUNRR	0x42100050	Functional Retention RAM Configuration Register
RAMC_PPU0_FULRR	0x42100054	Full Retention RAM Configuration Register
RAMC_PPU0_MEMRR	0x42100058	Memory Retention RAM Configuration Register
RAMC_PPU0_EDTR0	0x42100160	Power Mode Entry Delay Register 0
RAMC_PPU0_EDTR1	0x42100164	Power Mode Entry Delay Register 1
RAMC_PPU0_DCDR0	0x42100170	Device Control Delay Configuration Register 0
RAMC_PPU0_DCDR1	0x42100174	Device Control Delay Configuration Register 1
RAMC_PPU0_IDR0	0x42100FB0	PPU Identification Register 0
RAMC_PPU0_IDR1	0x42100FB4	PPU Identification Register 1
RAMC_PPU0_IIDR	0x42100FC8	Implementation Identification Register
RAMC_PPU0_AIDR	0x42100FCC	Architecture Identification Register
RAMC_PPU0_PID4	0x42100FD0	Implementation Defined Identification Register (PID4)
RAMC_PPU0_PID0	0x42100FE0	Implementation Defined Identification Register (PID0)
RAMC_PPU0_PID1	0x42100FE4	Implementation Defined Identification Register (PID1)
RAMC_PPU0_PID2	0x42100FE8	Implementation Defined Identification Register (PID2)

CPU Subsystem (CPUSS) registers

Register	Address	Description
RAMC_PPU0_PID3	0x42100FEC	Implementation Defined Identification Register (PID3)
RAMC_PPU0_ID0	0x42100FF0	Implementation Defined Identification Register (ID0)
RAMC_PPU0_ID1	0x42100FF4	Implementation Defined Identification Register (ID1)
RAMC_PPU0_ID2	0x42100FF8	Implementation Defined Identification Register (ID2)
RAMC_PPU0_ID3	0x42100FFC	Implementation Defined Identification Register (ID3)
ICACHE0_CTL	0x42103000	Cache control
ICACHE0_CMD	0x42103008	Cache command
ICACHE0_STATUS0	0x42103080	Cache status 0
ICACHE0_STATUS1	0x42103084	Cache status 1
ICACHE0_STATUS2	0x42103088	Cache status 2
CPUSS_PPU_PWPR	0x42105000	Power Policy Register
CPUSS_PPU_PMER	0x42105004	Power Mode Emulation Register
CPUSS_PPU_PWSR	0x42105008	Power Status Register
CPUSS_PPU_DISR	0x42105010	Device Interface Input Current Status Register
CPUSS_PPU_MISR	0x42105014	Miscellaneous Input Current Status Register
CPUSS_PPU_STSR	0x42105018	Stored Status Register
CPUSS_PPU_UNLK	0x4210501C	Unlock register
CPUSS_PPU_PWCR	0x42105020	Power Configuration Register
CPUSS_PPU_PTCR	0x42105024	Power Mode Transition Configuration Register
CPUSS_PPU_IMR	0x42105030	Interrupt Mask Register
CPUSS_PPU_AIMR	0x42105034	Additional Interrupt Mask Register
CPUSS_PPU_ISR	0x42105038	Interrupt Status Register
CPUSS_PPU_AISR	0x4210503C	Additional Interrupt Status Register
CPUSS_PPU_IESR	0x42105040	Input Edge Sensitivity Register
CPUSS_PPU_OPSR	0x42105044	Operating Mode Active Edge Sensitivity Register
CPUSS_PPU_FUNRR	0x42105050	Functional Retention RAM Configuration Register
CPUSS_PPU_FULRR	0x42105054	Full Retention RAM Configuration Register
CPUSS_PPU_MEMRR	0x42105058	Memory Retention RAM Configuration Register
CPUSS_PPU_EDTR0	0x42105160	Power Mode Entry Delay Register 0
CPUSS_PPU_EDTR1	0x42105164	Power Mode Entry Delay Register 1
CPUSS_PPU_DCDR0	0x42105170	Device Control Delay Configuration Register 0
CPUSS_PPU_DCDR1	0x42105174	Device Control Delay Configuration Register 1
CPUSS_PPU_IDR0	0x42105FB0	PPU Identification Register 0
CPUSS_PPU_IDR1	0x42105FB4	PPU Identification Register 1
CPUSS_PPU_IIDR	0x42105FC8	Implementation Identification Register
CPUSS_PPU_AIDR	0x42105FCC	Architecture Identification Register
CPUSS_PPU_PID4	0x42105FD0	Implementation Defined Identification Register (PID4)

CPU Subsystem (CPUSS) registers

Register	Address	Description
CPUSS_PPU_PID0	0x42105FE0	Implementation Defined Identification Register (PID0)
CPUSS_PPU_PID1	0x42105FE4	Implementation Defined Identification Register (PID1)
CPUSS_PPU_PID2	0x42105FE8	Implementation Defined Identification Register (PID2)
CPUSS_PPU_PID3	0x42105FEC	Implementation Defined Identification Register (PID3)
CPUSS_PPU_ID0	0x42105FF0	Implementation Defined Identification Register (ID0)
CPUSS_PPU_ID1	0x42105FF4	Implementation Defined Identification Register (ID1)
CPUSS_PPU_ID2	0x42105FF8	Implementation Defined Identification Register (ID2)
CPUSS_PPU_ID3	0x42105FFC	Implementation Defined Identification Register (ID3)
MXCM33_CM33_CTL	0x42160000	Control
MXCM33_CM33_CMD	0x42160004	Command
MXCM33_CM33_STATUS	0x42160008	Status
MXCM33_CM33_NMI_CTL0	0x42160080	CM33 NMI control
MXCM33_CM33_NMI_CTL1	0x42160084	CM33 NMI control. See MXCM33_CM33_NMI_CTL0 for the details of bit fields.
MXCM33_CM33_NMI_CTL2	0x42160088	CM33 NMI control. See MXCM33_CM33_NMI_CTL0 for the details of bit fields.
MXCM33_CM33_NMI_CTL3	0x4216008C	CM33 NMI control. See MXCM33_CM33_NMI_CTL0 for the details of bit fields.
MXCM33_CM33_EVENT_CTL	0x421600C0	CM33 event control
MXCM33_CM33_S_VECTOR_TABLE_BASE	0x42161000	CM33 secure vector table base
MXCM33_CM33_NS_VECTOR_TABLE_BASE	0x42161004	CM33 non-secure vector table base
MXCM33_CM33_PC_CTL	0x42162000	CM33 protection context control
MXCM33_CM33_PC0_HANDLER	0x42162040	CM33 protection context 0 handler
MXCM33_CM33_PC1_HANDLER	0x42162100	CM33 protection context 1 handler
MXCM33_CM33_PC2_HANDLER	0x42162140	CM33 protection context 2 handler
MXCM33_CM33_PC3_HANDLER	0x42162180	CM33 protection context 3 handler
CPUSS_IDENTITY	0x421C0000	Identity
CPUSS_PRODUCT_ID	0x421C0010	Product identifier and version (same as CoreSight RomTables)
CPUSS_DP_STATUS	0x421C0020	Debug port status
CPUSS_BUFF_CTL	0x421C0030	Buffer control
CPUSS_CAL_SUP_SET	0x421C0040	Calibration support set and read
CPUSS_CAL_SUP_CLR	0x421C0044	Calibration support clear and reset
CPUSS_INFRA_CTL	0x421C0050	Infrastructure Control
CPUSS_SYSTICK_S_CTL	0x421C0100	Secure SysTick timer control

CPU Subsystem (CPUSS) registers

Register	Address	Description
CPUSS_SYSTICK_NS_CTL	0x421C0120	Non Secure SysTick timer control
CPUSS_INTR_MSC	0x421C0200	Master security controller Interrupt
CPUSS_INTR_MASK_MSC	0x421C0208	Master security controller Interrupt mask
CPUSS_INTR_MASKED_MSC	0x421C020C	Master security controller Interrupt masked
CPUSS_AP_CTL	0x421C1000	Access port control
CPUSS_PROTECTION	0x421C2004	Protection status
MS0_CTL	0x421C4000	Master 'x' protection context control
MS4_CTL	0x421C4040	Master 'x' protection context control. See MS0_CTL for the details of bit fields.
MS5_CTL	0x421C4050	Master 'x' protection context control. See MS0_CTL for the details of bit fields.
MS7_CTL	0x421C4070	Master 'x' protection context control. See MS0_CTL for the details of bit fields.
MS31_CTL	0x421C41F0	Master 'x' protection context control
MS_PC0_PC	0x421C5000	Master 'x' protection context value
MS_PC0_PC_READ_MIR	0x421C5004	Master 'x' protection context value read mirror register
MS_PC31_PC	0x421C51F0	Master 'x' protection context value
MS_PC31_PC_READ_MIR	0x421C51F4	Master 'x' protection context value read mirror register
SYS_MS0_MSC_ACG_CTL	0x421C6010	SYS_MS0 master security Controller & ACG configuration
EXP_MS_MSC_ACG_CTL	0x421C6020	EXP_MS master security Controller & ACG configuration
CPUSS_SL_CTL_SL_CTL	0x421C8000	Slave control (Clock enables)
CPUSS_SL_CTL_SL_CTL2	0x421C8004	Slave control2 (Reset enables)
CM33_SCS_ICTR	0xE000E004	Interrupt Controller Type Register
CM33_SCS_ACTLR	0xE000E008	Auxiliary Control Register
CM33_SCS_SYST_CSR	0xE000E010	SysTick Control and Status Register
CM33_SCS_SYST_RVR	0xE000E014	SysTick Reload Value Register
CM33_SCS_SYST_CVR	0xE000E018	SysTick Current Value Register
CM33_SCS_SYST_CALIB	0xE000E01C	SysTick Calibration value Register
CM33_SCS_NVIC_ISER0	0xE000E100	Interrupt Set-Enable Registers
CM33_SCS_NVIC_ISER1	0xE000E104	Interrupt Set-Enable Registers. See CM33_SCS_NVIC_ISER0 for the details of bit fields.
CM33_SCS_NVIC_ISER2	0xE000E108	Interrupt Set-Enable Registers. See CM33_SCS_NVIC_ISER0 for the details of bit fields.
CM33_SCS_NVIC_ISER3	0xE000E10C	Interrupt Set-Enable Registers. See CM33_SCS_NVIC_ISER0 for the details of bit fields.
CM33_SCS_NVIC_ISER4	0xE000E110	Interrupt Set-Enable Registers. See CM33_SCS_NVIC_ISER0 for the details of bit fields.

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Register	Address	Description
CM33_SCS_NVIC_ISER5	0xE000E114	Interrupt Set-Enable Registers. See CM33_SCS_NVIC_ISER0 for the details of bit fields.
CM33_SCS_NVIC_ISER6	0xE000E118	Interrupt Set-Enable Registers. See CM33_SCS_NVIC_ISER0 for the details of bit fields.
CM33_SCS_NVIC_ISER7	0xE000E11C	Interrupt Set-Enable Registers. See CM33_SCS_NVIC_ISER0 for the details of bit fields.
CM33_SCS_NVIC_ISER8	0xE000E120	Interrupt Set-Enable Registers. See CM33_SCS_NVIC_ISER0 for the details of bit fields.
CM33_SCS_NVIC_ISER9	0xE000E124	Interrupt Set-Enable Registers. See CM33_SCS_NVIC_ISER0 for the details of bit fields.
CM33_SCS_NVIC_ISER10	0xE000E128	Interrupt Set-Enable Registers. See CM33_SCS_NVIC_ISER0 for the details of bit fields.
CM33_SCS_NVIC_ISER11	0xE000E12C	Interrupt Set-Enable Registers. See CM33_SCS_NVIC_ISER0 for the details of bit fields.
CM33_SCS_NVIC_ISER12	0xE000E130	Interrupt Set-Enable Registers. See CM33_SCS_NVIC_ISER0 for the details of bit fields.
CM33_SCS_NVIC_ISER13	0xE000E134	Interrupt Set-Enable Registers. See CM33_SCS_NVIC_ISER0 for the details of bit fields.
CM33_SCS_NVIC_ISER14	0xE000E138	Interrupt Set-Enable Registers. See CM33_SCS_NVIC_ISER0 for the details of bit fields.
CM33_SCS_NVIC_ISER15	0xE000E13C	Interrupt Set-Enable Registers. See CM33_SCS_NVIC_ISER0 for the details of bit fields.
CM33_SCS_NVIC_ICER0	0xE000E180	Interrupt Clear-Enable Registers
CM33_SCS_NVIC_ICER1	0xE000E184	Interrupt Clear-Enable Registers. See CM33_SCS_NVIC_ICER0 for the details of bit fields.
CM33_SCS_NVIC_ICER2	0xE000E188	Interrupt Clear-Enable Registers. See CM33_SCS_NVIC_ICER0 for the details of bit fields.
CM33_SCS_NVIC_ICER3	0xE000E18C	Interrupt Clear-Enable Registers. See CM33_SCS_NVIC_ICER0 for the details of bit fields.
CM33_SCS_NVIC_ICER4	0xE000E190	Interrupt Clear-Enable Registers. See CM33_SCS_NVIC_ICER0 for the details of bit fields.
CM33_SCS_NVIC_ICER5	0xE000E194	Interrupt Clear-Enable Registers. See CM33_SCS_NVIC_ICER0 for the details of bit fields.
CM33_SCS_NVIC_ICER6	0xE000E198	Interrupt Clear-Enable Registers. See CM33_SCS_NVIC_ICER0 for the details of bit fields.
CM33_SCS_NVIC_ICER7	0xE000E19C	Interrupt Clear-Enable Registers. See CM33_SCS_NVIC_ICER0 for the details of bit fields.
CM33_SCS_NVIC_ICER8	0xE000E1A0	Interrupt Clear-Enable Registers. See CM33_SCS_NVIC_ICER0 for the details of bit fields.
CM33_SCS_NVIC_ICER9	0xE000E1A4	Interrupt Clear-Enable Registers. See CM33_SCS_NVIC_ICER0 for the details of bit fields.
CM33_SCS_NVIC_ICER10	0xE000E1A8	Interrupt Clear-Enable Registers. See CM33_SCS_NVIC_ICER0 for the details of bit fields.

CPU Subsystem (CPUSS) registers

Register	Address	Description
CM33_SCS_NVIC_ICER11	0xE000E1AC	Interrupt Clear-Enable Registers. See CM33_SCS_NVIC_ICER0 for the details of bit fields.
CM33_SCS_NVIC_ICER12	0xE000E1B0	Interrupt Clear-Enable Registers. See CM33_SCS_NVIC_ICER0 for the details of bit fields.
CM33_SCS_NVIC_ICER13	0xE000E1B4	Interrupt Clear-Enable Registers. See CM33_SCS_NVIC_ICER0 for the details of bit fields.
CM33_SCS_NVIC_ICER14	0xE000E1B8	Interrupt Clear-Enable Registers. See CM33_SCS_NVIC_ICER0 for the details of bit fields.
CM33_SCS_NVIC_ICER15	0xE000E1BC	Interrupt Clear-Enable Registers. See CM33_SCS_NVIC_ICER0 for the details of bit fields.
CM33_SCS_NVIC_ISPR0	0xE000E200	Interrupt Set-Pending Registers
CM33_SCS_NVIC_ISPR1	0xE000E204	Interrupt Set-Pending Registers. See CM33_SCS_NVIC_ISPR0 for the details of bit fields.
CM33_SCS_NVIC_ISPR2	0xE000E208	Interrupt Set-Pending Registers. See CM33_SCS_NVIC_ISPR0 for the details of bit fields.
CM33_SCS_NVIC_ISPR3	0xE000E20C	Interrupt Set-Pending Registers. See CM33_SCS_NVIC_ISPR0 for the details of bit fields.
CM33_SCS_NVIC_ISPR4	0xE000E210	Interrupt Set-Pending Registers. See CM33_SCS_NVIC_ISPR0 for the details of bit fields.
CM33_SCS_NVIC_ISPR5	0xE000E214	Interrupt Set-Pending Registers. See CM33_SCS_NVIC_ISPR0 for the details of bit fields.
CM33_SCS_NVIC_ISPR6	0xE000E218	Interrupt Set-Pending Registers. See CM33_SCS_NVIC_ISPR0 for the details of bit fields.
CM33_SCS_NVIC_ISPR7	0xE000E21C	Interrupt Set-Pending Registers. See CM33_SCS_NVIC_ISPR0 for the details of bit fields.
CM33_SCS_NVIC_ISPR8	0xE000E220	Interrupt Set-Pending Registers. See CM33_SCS_NVIC_ISPR0 for the details of bit fields.
CM33_SCS_NVIC_ISPR9	0xE000E224	Interrupt Set-Pending Registers. See CM33_SCS_NVIC_ISPR0 for the details of bit fields.
CM33_SCS_NVIC_ISPR10	0xE000E228	Interrupt Set-Pending Registers. See CM33_SCS_NVIC_ISPR0 for the details of bit fields.
CM33_SCS_NVIC_ISPR11	0xE000E22C	Interrupt Set-Pending Registers. See CM33_SCS_NVIC_ISPR0 for the details of bit fields.
CM33_SCS_NVIC_ISPR12	0xE000E230	Interrupt Set-Pending Registers. See CM33_SCS_NVIC_ISPR0 for the details of bit fields.
CM33_SCS_NVIC_ISPR13	0xE000E234	Interrupt Set-Pending Registers. See CM33_SCS_NVIC_ISPR0 for the details of bit fields.
CM33_SCS_NVIC_ISPR14	0xE000E238	Interrupt Set-Pending Registers. See CM33_SCS_NVIC_ISPR0 for the details of bit fields.
CM33_SCS_NVIC_ISPR15	0xE000E23C	Interrupt Set-Pending Registers. See CM33_SCS_NVIC_ISPR0 for the details of bit fields.
CM33_SCS_NVIC_ICPR0	0xE000E280	Interrupt Clear-Pending Registers

CPU Subsystem (CPUSS) registers

Register	Address	Description
CM33_SCS_NVIC_ICPR1	0xE000E284	Interrupt Clear-Pending Registers. See CM33_SCS_NVIC_ICPR0 for the details of bit fields.
CM33_SCS_NVIC_ICPR2	0xE000E288	Interrupt Clear-Pending Registers. See CM33_SCS_NVIC_ICPR0 for the details of bit fields.
CM33_SCS_NVIC_ICPR3	0xE000E28C	Interrupt Clear-Pending Registers. See CM33_SCS_NVIC_ICPR0 for the details of bit fields.
CM33_SCS_NVIC_ICPR4	0xE000E290	Interrupt Clear-Pending Registers. See CM33_SCS_NVIC_ICPR0 for the details of bit fields.
CM33_SCS_NVIC_ICPR5	0xE000E294	Interrupt Clear-Pending Registers. See CM33_SCS_NVIC_ICPR0 for the details of bit fields.
CM33_SCS_NVIC_ICPR6	0xE000E298	Interrupt Clear-Pending Registers. See CM33_SCS_NVIC_ICPR0 for the details of bit fields.
CM33_SCS_NVIC_ICPR7	0xE000E29C	Interrupt Clear-Pending Registers. See CM33_SCS_NVIC_ICPR0 for the details of bit fields.
CM33_SCS_NVIC_ICPR8	0xE000E2A0	Interrupt Clear-Pending Registers. See CM33_SCS_NVIC_ICPR0 for the details of bit fields.
CM33_SCS_NVIC_ICPR9	0xE000E2A4	Interrupt Clear-Pending Registers. See CM33_SCS_NVIC_ICPR0 for the details of bit fields.
CM33_SCS_NVIC_ICPR10	0xE000E2A8	Interrupt Clear-Pending Registers. See CM33_SCS_NVIC_ICPR0 for the details of bit fields.
CM33_SCS_NVIC_ICPR11	0xE000E2AC	Interrupt Clear-Pending Registers. See CM33_SCS_NVIC_ICPR0 for the details of bit fields.
CM33_SCS_NVIC_ICPR12	0xE000E2B0	Interrupt Clear-Pending Registers. See CM33_SCS_NVIC_ICPR0 for the details of bit fields.
CM33_SCS_NVIC_ICPR13	0xE000E2B4	Interrupt Clear-Pending Registers. See CM33_SCS_NVIC_ICPR0 for the details of bit fields.
CM33_SCS_NVIC_ICPR14	0xE000E2B8	Interrupt Clear-Pending Registers. See CM33_SCS_NVIC_ICPR0 for the details of bit fields.
CM33_SCS_NVIC_ICPR15	0xE000E2BC	Interrupt Clear-Pending Registers. See CM33_SCS_NVIC_ICPR0 for the details of bit fields.
CM33_SCS_NVIC_IABR0	0xE000E300	Interrupt Active Bit Registers
CM33_SCS_NVIC_IABR1	0xE000E304	Interrupt Active Bit Registers. See CM33_SCS_NVIC_IABR0 for the details of bit fields.
CM33_SCS_NVIC_IABR2	0xE000E308	Interrupt Active Bit Registers. See CM33_SCS_NVIC_IABR0 for the details of bit fields.
CM33_SCS_NVIC_IABR3	0xE000E30C	Interrupt Active Bit Registers. See CM33_SCS_NVIC_IABR0 for the details of bit fields.
CM33_SCS_NVIC_IABR4	0xE000E310	Interrupt Active Bit Registers. See CM33_SCS_NVIC_IABR0 for the details of bit fields.
CM33_SCS_NVIC_IABR5	0xE000E314	Interrupt Active Bit Registers. See CM33_SCS_NVIC_IABR0 for the details of bit fields.
CM33_SCS_NVIC_IABR6	0xE000E318	Interrupt Active Bit Registers. See CM33_SCS_NVIC_IABR0 for the details of bit fields.

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Register	Address	Description
CM33_SCS_NVIC_IABR7	0xE000E31C	Interrupt Active Bit Registers. See CM33_SCS_NVIC_IABR0 for the details of bit fields.
CM33_SCS_NVIC_IABR8	0xE000E320	Interrupt Active Bit Registers. See CM33_SCS_NVIC_IABR0 for the details of bit fields.
CM33_SCS_NVIC_IABR9	0xE000E324	Interrupt Active Bit Registers. See CM33_SCS_NVIC_IABR0 for the details of bit fields.
CM33_SCS_NVIC_IABR10	0xE000E328	Interrupt Active Bit Registers. See CM33_SCS_NVIC_IABR0 for the details of bit fields.
CM33_SCS_NVIC_IABR11	0xE000E32C	Interrupt Active Bit Registers. See CM33_SCS_NVIC_IABR0 for the details of bit fields.
CM33_SCS_NVIC_IABR12	0xE000E330	Interrupt Active Bit Registers. See CM33_SCS_NVIC_IABR0 for the details of bit fields.
CM33_SCS_NVIC_IABR13	0xE000E334	Interrupt Active Bit Registers. See CM33_SCS_NVIC_IABR0 for the details of bit fields.
CM33_SCS_NVIC_IABR14	0xE000E338	Interrupt Active Bit Registers. See CM33_SCS_NVIC_IABR0 for the details of bit fields.
CM33_SCS_NVIC_IABR15	0xE000E33C	Interrupt Active Bit Registers. See CM33_SCS_NVIC_IABR0 for the details of bit fields.
CM33_SCS_NVIC_ITNS0	0xE000E380	Interrupt Target Non-secure Registers
CM33_SCS_NVIC_ITNS1	0xE000E384	Interrupt Target Non-secure Registers. See CM33_SCS_NVIC_ITNS0 for the details of bit fields.
CM33_SCS_NVIC_ITNS2	0xE000E388	Interrupt Target Non-secure Registers. See CM33_SCS_NVIC_ITNS0 for the details of bit fields.
CM33_SCS_NVIC_ITNS3	0xE000E38C	Interrupt Target Non-secure Registers. See CM33_SCS_NVIC_ITNS0 for the details of bit fields.
CM33_SCS_NVIC_ITNS4	0xE000E390	Interrupt Target Non-secure Registers. See CM33_SCS_NVIC_ITNS0 for the details of bit fields.
CM33_SCS_NVIC_ITNS5	0xE000E394	Interrupt Target Non-secure Registers. See CM33_SCS_NVIC_ITNS0 for the details of bit fields.
CM33_SCS_NVIC_ITNS6	0xE000E398	Interrupt Target Non-secure Registers. See CM33_SCS_NVIC_ITNS0 for the details of bit fields.
CM33_SCS_NVIC_ITNS7	0xE000E39C	Interrupt Target Non-secure Registers. See CM33_SCS_NVIC_ITNS0 for the details of bit fields.
CM33_SCS_NVIC_ITNS8	0xE000E3A0	Interrupt Target Non-secure Registers. See CM33_SCS_NVIC_ITNS0 for the details of bit fields.
CM33_SCS_NVIC_ITNS9	0xE000E3A4	Interrupt Target Non-secure Registers. See CM33_SCS_NVIC_ITNS0 for the details of bit fields.
CM33_SCS_NVIC_ITNS10	0xE000E3A8	Interrupt Target Non-secure Registers. See CM33_SCS_NVIC_ITNS0 for the details of bit fields.
CM33_SCS_NVIC_ITNS11	0xE000E3AC	Interrupt Target Non-secure Registers. See CM33_SCS_NVIC_ITNS0 for the details of bit fields.
CM33_SCS_NVIC_ITNS12	0xE000E3B0	Interrupt Target Non-secure Registers. See CM33_SCS_NVIC_ITNS0 for the details of bit fields.

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Register	Address	Description
CM33_SCS_NVIC_ITNS13	0xE000E3B4	Interrupt Target Non-secure Registers. See CM33_SCS_NVIC_ITNS0 for the details of bit fields.
CM33_SCS_NVIC_ITNS14	0xE000E3B8	Interrupt Target Non-secure Registers. See CM33_SCS_NVIC_ITNS0 for the details of bit fields.
CM33_SCS_NVIC_ITNS15	0xE000E3BC	Interrupt Target Non-secure Registers. See CM33_SCS_NVIC_ITNS0 for the details of bit fields.
CM33_SCS_NVIC_IPR0	0xE000E400	Interrupt Priority Registers. This is the starting address of a register bank containing 120 registers (CM33_SCS_NVIC_IPR0 to CM33_SCS_NVIC_IPR119).
CM33_SCS_CPUID	0xE000ED00	CPUID Base Register
CM33_SCS_VTOR	0xE000ED08	Vector Table Offset Register
CM33_SCS_AIRCR	0xE000ED0C	Application Interrupt and Reset Control Register
CM33_SCS_SCR	0xE000ED10	System Control Register
CM33_SCS_CCR	0xE000ED14	Configuration and Control Register
CM33_SCS_DFSR	0xE000ED30	Debug Fault Status Register
CM33_SCS_ID_PFR0	0xE000ED40	Processor Feature Register 0
CM33_SCS_ID_PFR1	0xE000ED44	Processor Feature Register 1
CM33_SCS_ID_DFR0	0xE000ED48	Debug Feature Register 0
CM33_SCS_ID_AFR0	0xE000ED4C	Auxiliary Feature Register 0
CM33_SCS_ID_MMFR0	0xE000ED50	Memory Model Feature Register 0
CM33_SCS_ID_MMFR1	0xE000ED54	Memory Model Feature Register 1
CM33_SCS_ID_MMFR2	0xE000ED58	Memory Model Feature Register 2
CM33_SCS_ID_MMFR3	0xE000ED5C	Memory Model Feature Register 3
CM33_SCS_ID_ISAR0	0xE000ED60	Instruction Set Attributes Register 0
CM33_SCS_ID_ISAR1	0xE000ED64	Instruction Set Attributes Register 1
CM33_SCS_ID_ISAR2	0xE000ED68	Instruction Set Attributes Register 2
CM33_SCS_ID_ISAR3	0xE000ED6C	Instruction Set Attributes Register 3
CM33_SCS_ID_ISAR4	0xE000ED70	Instruction Set Attributes Register 4
CM33_SCS_CLIDR	0xE000ED78	Cache Level ID Register
CM33_SCS_CTR	0xE000ED7C	Cache Type Register
CM33_SCS_CPACR	0xE000ED88	Coprocessor Access Control Register
CM33_SCS_NSACR	0xE000ED8C	Non-secure Access Control Register
CM33_SCS_MPU_TYPE	0xE000ED90	MPU Type Register
CM33_SCS_MPU_CTRL	0xE000ED94	MPU Control Register
CM33_SCS_MPU_RNR	0xE000ED98	MPU Region Number Register
CM33_SCS_MPU_RBAR	0xE000ED9C	MPU Region Base Address Register
CM33_SCS_MPU_RLAR	0xE000EDA0	MPU Region Limit Address Register
CM33_SCS_MPU_RBAR_A1	0xE000EDA4	MPU alias registers
CM33_SCS_MPU_RLAR_A1	0xE000EDA8	MPU alias registers
CM33_SCS_MPU_RBAR_A2	0xE000EDAC	MPU alias registers

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Register	Address	Description
CM33_SCS_MPU_RLAR_A2	0xE000EDB0	MPU alias registers
CM33_SCS_MPU_RBAR_A3	0xE000EDB4	MPU alias registers
CM33_SCS_MPU_RLAR_A3	0xE000EDB8	MPU alias registers
CM33_SCS_MPU_MAIR0	0xE000EDC0	MPU Memory Attribute Indirection Register 0
CM33_SCS_MPU_MAIR1	0xE000EDC4	MPU Memory Attribute Indirection Register 1
CM33_SCS_SAU_CTRL	0xE000EDD0	SAU Control Register
CM33_SCS_SAU_TYPE	0xE000EDD4	SAU Type Register
CM33_SCS_SAU_RNR	0xE000EDD8	SAU Region Number Register
CM33_SCS_SAU_RBAR	0xE000EDDC	SAU Region Base Address Register
CM33_SCS_SAU_RLAR	0xE000EDE0	SAU Region Limit Address Register
CM33_SCS_DHCSR	0xE000EDF0	Debug Halting Control and Status Register
CM33_SCS_DCRSR	0xE000EDF4	Debug Core Register Selector Register
CM33_SCS_DCRDR	0xE000EDF8	Debug Core Register Data Register
CM33_SCS_DEMCR	0xE000EDFC	Debug Exception and Monitor Control Register
CM33_SCS_DAUTHCTRL	0xE000EE04	Debug Authentication Control Register
CM33_SCS_DSCSR	0xE000EE08	Debug Security Control and Status Register
CM33_SCS_FPCCR	0xE000EF34	FP Context Control Register
CM33_SCS_FPCAR	0xE000EF38	FP Context Control Register
CM33_SCS_FPDSCR	0xE000EF3C	FP Context Control Register
CM33_SCS_MVFR0	0xE000EF40	Media and VFP Feature Register 0
CM33_SCS_MVFR1	0xE000EF44	Media and VFP Feature Register 1
CM33_SCS_MVFR2	0xE000EF48	Media and VFP Feature Register 2
CM33_SCS_DAUTHSTATUS	0xE000EFB8	Debug Authentication Status Register
CM33_SCS_DEVARCH	0xE000EFBC	CoreSight Device Architecture Register
CM33_SCS_PIDR4	0xE000EFD0	Peripheral Identification Register 4
CM33_SCS_PIDR5	0xE000EFD4	Peripheral Identification Register 5
CM33_SCS_PIDR6	0xE000EFD8	Peripheral Identification Register 6
CM33_SCS_PIDR7	0xE000EFDC	Peripheral Identification Register 7
CM33_SCS_PIDR0	0xE000EFE0	Peripheral Identification Register 0
CM33_SCS_PIDR1	0xE000EFE4	Peripheral Identification Register 1
CM33_SCS_PIDR2	0xE000EFE8	Peripheral Identification Register 2
CM33_SCS_PIDR3	0xE000EFEC	Peripheral Identification Register 3
CM33_SCS_CIDR0	0xE000EFF0	Component Identification Register 0
CM33_SCS_CIDR1	0xE000EFF4	Component Identification Register 1
CM33_SCS_CIDR2	0xE000EFF8	Component Identification Register 2
CM33_SCS_CIDR3	0xE000EFFC	Component Identification Register 3
CM33_CM33CTI_CTICONTROL	0xE0042000	CTI Control Register
CM33_CM33CTI_CTIINTACK	0xE0042010	CTI Interrupt Acknowledge Register
CM33_CM33CTI_CTIAPPSET	0xE0042014	CTI Application Trigger Set Register

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Register	Address	Description
CM33_CM33CTI_CTIAPPCLEAR	0xE0042018	CTI Application Trigger Clear Register
CM33_CM33CTI_CTIAPPPULSE	0xE004201C	CTI Application Pulse Register
CM33_CM33CTI_CTIINEN0	0xE0042020	CTI Trigger to Channel Enable Registers
CM33_CM33CTI_CTIINEN1	0xE0042024	CTI Trigger to Channel Enable Registers. See CM33_CM33CTI_CTIINEN0 for the details of bit fields.
CM33_CM33CTI_CTIINEN2	0xE0042028	CTI Trigger to Channel Enable Registers. See CM33_CM33CTI_CTIINEN0 for the details of bit fields.
CM33_CM33CTI_CTIINEN3	0xE004202C	CTI Trigger to Channel Enable Registers. See CM33_CM33CTI_CTIINEN0 for the details of bit fields.
CM33_CM33CTI_CTIINEN4	0xE0042030	CTI Trigger to Channel Enable Registers. See CM33_CM33CTI_CTIINEN0 for the details of bit fields.
CM33_CM33CTI_CTIINEN5	0xE0042034	CTI Trigger to Channel Enable Registers. See CM33_CM33CTI_CTIINEN0 for the details of bit fields.
CM33_CM33CTI_CTIINEN6	0xE0042038	CTI Trigger to Channel Enable Registers. See CM33_CM33CTI_CTIINEN0 for the details of bit fields.
CM33_CM33CTI_CTIINEN7	0xE004203C	CTI Trigger to Channel Enable Registers. See CM33_CM33CTI_CTIINEN0 for the details of bit fields.
CM33_CM33CTI_CTIOUTEN0	0xE00420A0	CTI Channel to Trigger Enable Registers
CM33_CM33CTI_CTIOUTEN1	0xE00420A4	CTI Channel to Trigger Enable Registers. See CM33_CM33CTI_CTIOUTEN0 for the details of bit fields.
CM33_CM33CTI_CTIOUTEN2	0xE00420A8	CTI Channel to Trigger Enable Registers. See CM33_CM33CTI_CTIOUTEN0 for the details of bit fields.
CM33_CM33CTI_CTIOUTEN3	0xE00420AC	CTI Channel to Trigger Enable Registers. See CM33_CM33CTI_CTIOUTEN0 for the details of bit fields.
CM33_CM33CTI_CTIOUTEN4	0xE00420B0	CTI Channel to Trigger Enable Registers. See CM33_CM33CTI_CTIOUTEN0 for the details of bit fields.
CM33_CM33CTI_CTIOUTEN5	0xE00420B4	CTI Channel to Trigger Enable Registers. See CM33_CM33CTI_CTIOUTEN0 for the details of bit fields.
CM33_CM33CTI_CTIOUTEN6	0xE00420B8	CTI Channel to Trigger Enable Registers. See CM33_CM33CTI_CTIOUTEN0 for the details of bit fields.
CM33_CM33CTI_CTIOUTEN7	0xE00420BC	CTI Channel to Trigger Enable Registers. See CM33_CM33CTI_CTIOUTEN0 for the details of bit fields.
CM33_CM33CTI_CTITRIGINSTATUS	0xE0042130	CTI Trigger In Status Register
CM33_CM33CTI_CTITRIGOUTSTATUS	0xE0042134	CTI Trigger Out Status Register
CM33_CM33CTI_CTICHINSTATUS	0xE0042138	CTI Channel In Status Register
CM33_CM33CTI_CTIGATE	0xE0042140	Enable CTI Channel Gate Register

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Register	Address	Description
CM33_CM33CTI_ASICCTL	0xE0042144	External Multiplexor Control Register
CM33_CM33CTI_ITCHOUT	0xE0042EE4	ITCHOUT Register
CM33_CM33CTI_ITTRIGOUT	0xE0042EE8	ITTRIGOUT Register
CM33_CM33CTI_ITCHIN	0xE0042EF4	ITCHIN Register
CM33_CM33CTI_ITCTRL	0xE0042F00	Integration Mode Control Register
CM33_CM33CTI_DEVARCH	0xE0042FBC	Device Architecture register
CM33_CM33CTI_DEVID	0xE0042FC8	Device Configuration Register
CM33_CM33CTI_DEVTYPE	0xE0042FCC	Device Type Identifier Register
CM33_CM33CTI_PIDR4	0xE0042FD0	Peripheral Identification Register 4
CM33_CM33CTI_PIDR5	0xE0042FD4	Peripheral Identification Register 5
CM33_CM33CTI_PIDR6	0xE0042FD8	Peripheral Identification Register 6
CM33_CM33CTI_PIDR7	0xE0042FDC	Peripheral Identification Register 7
CM33_CM33CTI_PIDR0	0xE0042FE0	Peripheral Identification Register 0
CM33_CM33CTI_PIDR1	0xE0042FE4	Peripheral Identification Register 1
CM33_CM33CTI_PIDR2	0xE0042FE8	Peripheral Identification Register 2
CM33_CM33CTI_PIDR3	0xE0042FEC	Peripheral Identification Register 3
CM33_CM33CTI_CIDR0	0xE0042FF0	Component Identification Register 0
CM33_CM33CTI_CIDR1	0xE0042FF4	Component Identification Register 1
CM33_CM33CTI_CIDR2	0xE0042FF8	Component Identification Register 2
CM33_CM33CTI_CIDR3	0xE0042FFC	Component Identification Register 3
CM33_TRC_CTI_CTICONTROL	0xE0080000	CTI Control Register
CM33_TRC_CTI_CTIINTACK	0xE0080010	CTI Interrupt Acknowledge Register
CM33_TRC_CTI_CTIAPPSET	0xE0080014	CTI Application Trigger Set Register
CM33_TRC_CTI_CTIAPPCLEAR	0xE0080018	CTI Application Trigger Clear Register
CM33_TRC_CTI_CTIAPPPULSE	0xE008001C	CTI Application Pulse Register
CM33_TRC_CTI_CTIINEN0	0xE0080020	CTI Trigger to Channel Enable Registers. This is the starting address of a register bank containing 32 registers (CM33_TRC_CTI_CTIINEN0 to CM33_TRC_CTI_CTIINEN31).
CM33_TRC_CTI_CTIOUTEN0	0xE00800A0	CTI Channel to Trigger Enable Registers. This is the starting address of a register bank containing 32 registers (CM33_TRC_CTI_CTIOUTEN0 to CM33_TRC_CTI_CTIOUTEN31).
CM33_TRC_CTI_CTITRIGINSTATUS	0xE0080130	CTI Trigger In Status Register
CM33_TRC_CTI_CTITRIGOUTSTATUS	0xE0080134	CTI Trigger Out Status Register
CM33_TRC_CTI_CTICHINSTATUS	0xE0080138	CTI Channel In Status Register
CM33_TRC_CTI_CTICHOUTSTATUS	0xE008013C	CTI Channel Out Status Register
CM33_TRC_CTI_CTIGATE	0xE0080140	Enable CTI Channel Gate Register
CM33_TRC_CTI_ASICCTL	0xE0080144	External Multiplexor Control Register
CM33_TRC_CTI_ITCHINACK	0xE0080EDC	ITCHINACK Register

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Register	Address	Description
CM33_TRC_CTI_ITTRIGINACK	0xE0080EE0	ITTRIGINACK Register
CM33_TRC_CTI_ITCHOUT	0xE0080EE4	ITCHOUT Register
CM33_TRC_CTI_ITTRIGOUT	0xE0080EE8	ITTRIGOUT Register
CM33_TRC_CTI_ITCHOUTACK	0xE0080EEC	ITCHOUTACK Register
CM33_TRC_CTI_ITTRIGOUTACK	0xE0080EF0	ITTRIGOUTACK Register
CM33_TRC_CTI_ITCHIN	0xE0080EF4	ITCHIN Register
CM33_TRC_CTI_ITTRIGIN	0xE0080EF8	ITTRIGIN Register
CM33_TRC_CTI_ITCTRL	0xE0080F00	Integration Mode Control Register
CM33_TRC_CTI_CLAIMSET	0xE0080FA0	Claim Tag Set Register
CM33_TRC_CTI_CLAIMCLR	0xE0080FA4	Claim Tag Clear Register
CM33_TRC_CTI_DEVAFF0	0xE0080FA8	Device Affinity Register 0
CM33_TRC_CTI_DEVAFF1	0xE0080FAC	Device Affinity Register 1
CM33_TRC_CTI_LAR	0xE0080FB0	Lock Access Register
CM33_TRC_CTI_LSR	0xE0080FB4	Lock Status Register
CM33_TRC_CTI_AUTHSTATUS	0xE0080FB8	Authentication Status Register
CM33_TRC_CTI_DEVARCH	0xE0080FBC	Device Architecture Register
CM33_TRC_CTI_DEVID	0xE0080FC8	Device Configuration Register
CM33_TRC_CTI_DEVTYPE	0xE0080FCC	Device Type Identifier Register
CM33_TRC_CTI_PIDR4	0xE0080FD0	Peripheral Identification Register 4
CM33_TRC_CTI_PIDR5	0xE0080FD4	Peripheral Identification Register 5
CM33_TRC_CTI_PIDR6	0xE0080FD8	Peripheral Identification Register 6
CM33_TRC_CTI_PIDR7	0xE0080FDC	Peripheral Identification Register 7
CM33_TRC_CTI_PIDR0	0xE0080FE0	Peripheral Identification Register 0
CM33_TRC_CTI_PIDR1	0xE0080FE4	Peripheral Identification Register 1
CM33_TRC_CTI_PIDR2	0xE0080FE8	Peripheral Identification Register 2
CM33_TRC_CTI_PIDR3	0xE0080FEC	Peripheral Identification Register 3
CM33_TRC_CTI_CIDR0	0xE0080FF0	Component Identification Register 0
CM33_TRC_CTI_CIDR1	0xE0080FF4	Component Identification Register 1
CM33_TRC_CTI_CIDR2	0xE0080FF8	Component Identification Register 2
CM33_TRC_CTI_CIDR3	0xE0080FFC	Component Identification Register 3
CM33_CSTF_FUNNELCONTROL	0xE0088000	Funnel Control Register
CM33_CSTF_PRIORITYCONTROL	0xE0088004	Priority Control Register
CM33_CSTF_ITATBDATA0	0xE0088EEC	Integration Register
CM33_CSTF_ITATBCTR3	0xE0088EF0	Integration Register
CM33_CSTF_ITATBCTR2	0xE0088EF4	Integration Register
CM33_CSTF_ITATBCTR1	0xE0088EF8	Integration Register
CM33_CSTF_ITATBCTR0	0xE0088EFC	Integration Register
CM33_CSTF_ITCTRL	0xE0088F00	Integration Mode Control Register
CM33_CSTF_CLAIMSET	0xE0088FA0	Claim Tag Set Register

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Register	Address	Description
CM33_CSTF_CLAIMCLR	0xE0088FA4	Claim Tag Clear Register
CM33_CSTF_DEVAFF0	0xE0088FB0	Device Affinity Register0
CM33_CSTF_DEVAFF1	0xE0088FB4	Device Affinity Register1
CM33_CSTF_AUTHSTATUS	0xE0088FB8	Authentication Status Register
CM33_CSTF_DEVARCH	0xE0088FBC	Device Architecture Register
CM33_CSTF_DEVID2	0xE0088FC0	Device Configuration Register 2
CM33_CSTF_DEVID1	0xE0088FC4	Device Configuration Register 1
CM33_CSTF_DEVID	0xE0088FC8	Device Configuration Register
CM33_CSTF_DEVTYPE	0xE0088FCC	Device Type Identifier Register
CM33_CSTF_PIDR4	0xE0088FD0	Peripheral Identification Register 4
CM33_CSTF_PIDR5	0xE0088FD4	Peripheral Identification Register 5
CM33_CSTF_PIDR6	0xE0088FD8	Peripheral Identification Register 6
CM33_CSTF_PIDR7	0xE0088FDC	Peripheral Identification Register 7
CM33_CSTF_PIDR0	0xE0088FE0	Peripheral Identification Register 0
CM33_CSTF_PIDR1	0xE0088FE4	Peripheral Identification Register 1
CM33_CSTF_PIDR2	0xE0088FE8	Peripheral Identification Register 2
CM33_CSTF_PIDR3	0xE0088FEC	Peripheral Identification Register 3
CM33_CSTF_CIDR1	0xE0088FF4	Component Identification Register 1
CM33_CSTF_CIDR2	0xE0088FF8	Component Identification Register 2
CM33_CSTF_CIDR3	0xE0088FFC	Component Identification Register 3
CM33_ETF_RSZ	0xE008D004	RAM Size register
CM33_ETF_STS	0xE008D00C	Status Register
CM33_ETF_RRD	0xE008D010	RAM Read Data Register
CM33_ETF_RRP	0xE008D014	RAM Read Pointer Register
CM33_ETF_RWP	0xE008D018	RAM Write Pointer Register
CM33_ETF_TRG	0xE008D01C	Trigger Counter Register
CM33_ETF_CTL	0xE008D020	Control Register
CM33_ETF_RWD	0xE008D024	RAM Write Data Register
CM33_ETF_MODE	0xE008D028	Mode Register
CM33_ETF_LBUFLEVEL	0xE008D02C	Latched Buffer Fill Level
CM33_ETF_CBUFLEVEL	0xE008D030	Current Buffer Fill Level
CM33_ETF_BUFWM	0xE008D034	Buffer Level Water Mark
CM33_ETF_FFSR	0xE008D300	formatter and Flush Status Register
CM33_ETF_FFCR	0xE008D304	formatter and Flush Control Register
CM33_ETF_PSCR	0xE008D308	Periodic Synchronization Counter Register
CM33_ETF_ITATBMDATA0	0xE008DED0	Integration Test ATB Master Data 0 Register
CM33_ETF_ITATBMCTR2	0xE008DED4	Integration Test ATB Master Interface Control 2 Register

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Register	Address	Description
CM33_ETF_ITATBMCTR1	0xE008DED8	Integration Test ATB Master Interface Control 1 Register
CM33_ETF_ITATBMCTR0	0xE008DEDC	Integration Test ATB Master Interface Control 0 Register
CM33_ETF_ITEVTINTR	0xE008DEE0	Integration Test Event & Interrupt Status Register
CM33_ETF_ITTRFLIN	0xE008DEE8	Integration Test Trigger In and Flush In Register
CM33_ETF_ITATBDATA0	0xE008DEEC	Integration Test ATB Data 0 Register
CM33_ETF_ITATBCTR2	0xE008DEF0	Integration Test ATB Control 2 Register
CM33_ETF_ITATBCTR1	0xE008DEF4	Integration Test ATB Control 1 Register
CM33_ETF_ITATBCTR0	0xE008DEF8	Integration Test ATB Control 0 Register
CM33_ETF_ITCTRL	0xE008DF00	Integration Mode Control Register
CM33_ETF_CLAIMSET	0xE008DFA0	Claim Tag Set Register
CM33_ETF_CLAIMCLR	0xE008DFA4	Claim Tag Clear Register
CM33_ETF_AUTHSTATUS	0xE008DFB8	Authentication Status Register
CM33_ETF_DEVID1	0xE008DFC4	Device Configuration Register 1
CM33_ETF_DEVID	0xE008DFC8	Device Configuration Register
CM33_ETF_DEVTYPE	0xE008DFCC	Device Type Identifier Register
CM33_ETF_PIDR4	0xE008DFD0	Peripheral Identification Register 4
CM33_ETF_PIDR5	0xE008DFD4	Peripheral Identification Register 5
CM33_ETF_PIDR6	0xE008DFD8	Peripheral Identification Register 6
CM33_ETF_PIDR7	0xE008DFDC	Peripheral Identification Register 7
CM33_ETF_PIDR0	0xE008DFE0	Peripheral Identification Register 0
CM33_ETF_PIDR1	0xE008DFE4	Peripheral Identification Register 1
CM33_ETF_PIDR2	0xE008DFE8	Peripheral Identification Register 2
CM33_ETF_PIDR3	0xE008DFEC	Peripheral Identification Register 3
CM33_ETF_CIDR0	0xE008DFF0	Component Identification Register 0
CM33_ETF_CIDR1	0xE008DFF4	Component Identification Register 1
CM33_ETF_CIDR2	0xE008DFF8	Component Identification Register 2
CM33_ETF_CIDR3	0xE008DFFC	Component Identification Register 3
CM33_CSS600_TPIU_TPIU_SSPSR	0xE008E000	Supported Parallel Port Size Register
CM33_CSS600_TPIU_TPIU_CSPSR	0xE008E004	Current Parallel Port Size Register
CM33_CSS600_TPIU_TPIU_STMR	0xE008E100	Supported Trigger Model Register
CM33_CSS600_TPIU_TPIU_TCVR	0xE008E104	Trigger Counter Value Register
CM33_CSS600_TPIU_TPIU_TCMR	0xE008E108	Trigger Counter Multiplier Register
CM33_CSS600_TPIU_TPIU_STPMR	0xE008E200	Supported Test Patterns Modes Register
CM33_CSS600_TPIU_TPIU_CTPMR	0xE008E204	Current Test Patterns Modes Register
CM33_CSS600_TPIU_TPIU_TPRCR	0xE008E208	Test Pattern Repeat Counter Register
CM33_CSS600_TPIU_TPIU_FFSR	0xE008E300	formatter and Flush Status Register
CM33_CSS600_TPIU_TPIU_FFCR	0xE008E304	formatter and Flush Control Register

CPU Subsystem (CPUSS) registers

Register	Address	Description
CM33_CSS600_TPIU_TPIU_FSCR	0xE008E308	formatter Synchronization Count Register
CM33_CSS600_TPIU_TPIU_EXTCTLIN	0xE008E400	External Control Port In Register
CM33_CSS600_TPIU_TPIU_EXTCTLOUT	0xE008E404	External Control Port Out Register
CM33_CSS600_TPIU_ITTRFLIN	0xE008EEE8	Integration Test Trigger In Flush In Register
CM33_CSS600_TPIU_ITATBDATA0	0xE008EEEC	Integration Test ATB Data Register0
CM33_CSS600_TPIU_ITATBCTR2	0xE008EEF0	Integration Test ATB Control Register 2
CM33_CSS600_TPIU_ITATBCTR1	0xE008EEF4	Integration Test ATB Control Register 1
CM33_CSS600_TPIU_ITATBCTR0	0xE008EEF8	Integration Test ATB Control Register 0
CM33_CSS600_TPIU_ITOUTCTR	0xE008EEFC	Integration Test Output Control Register
CM33_CSS600_TPIU_ITCTRL	0xE008EF00	Integration Mode Control Register
CM33_CSS600_TPIU_CLAIMSET	0xE008EFA0	Claim Tag Set Register
CM33_CSS600_TPIU_CLAIMCLR	0xE008EFA4	Claim Tag Clear Register
CM33_CSS600_TPIU_AUTHSTATUS	0xE008EFB8	Authentication Status Register
CM33_CSS600_TPIU_DEVARCH	0xE008EFBC	Device Architecture Register
CM33_CSS600_TPIU_DEVID	0xE008EFC8	Device ID
CM33_CSS600_TPIU_DEVTYPE	0xE008EFCC	Device Type Identifier Register
CM33_CSS600_TPIU_PIDR4	0xE008EFD0	Peripheral Identification Register 4
CM33_CSS600_TPIU_PIDR5	0xE008EFD4	Peripheral Identification Register 5
CM33_CSS600_TPIU_PIDR6	0xE008EFD8	Peripheral Identification Register 6
CM33_CSS600_TPIU_PIDR7	0xE008EFDC	Peripheral Identification Register 7
CM33_CSS600_TPIU_PIDR0	0xE008EFE0	Peripheral Identification Register 0
CM33_CSS600_TPIU_PIDR1	0xE008EFE4	Peripheral Identification Register 1
CM33_CSS600_TPIU_PIDR2	0xE008EFE8	Peripheral Identification Register 2
CM33_CSS600_TPIU_PIDR3	0xE008EFEC	Peripheral Identification Register 3
CM33_CSS600_TPIU_CIDR0	0xE008EFF0	Component Identification Register 0
CM33_CSS600_TPIU_CIDR1	0xE008EFF4	Component Identification Register 1
CM33_CSS600_TPIU_CIDR2	0xE008EFF8	Component Identification Register 2
CM33_CSS600_TPIU_CIDR3	0xE008EFFC	Component Identification Register 3
SYSAP_ROMTABLE_DID	0xE00BEFCC	Device Type Identifier register.
SYSAP_ROMTABLE_PID4	0xE00BEFD0	Peripheral Identification Register 4.
SYSAP_ROMTABLE_PID5	0xE00BEFD4	Peripheral Identification Register 5.
SYSAP_ROMTABLE_PID6	0xE00BEFD8	Peripheral Identification Register 6.
SYSAP_ROMTABLE_PID7	0xE00BEFDC	Peripheral Identification Register 7.
SYSAP_ROMTABLE_PID0	0xE00BEFE0	Peripheral Identification Register 0.
SYSAP_ROMTABLE_PID1	0xE00BEFE4	Peripheral Identification Register 1.
SYSAP_ROMTABLE_PID2	0xE00BEFE8	Peripheral Identification Register 2.
SYSAP_ROMTABLE_PID3	0xE00BEFEC	Peripheral Identification Register 3.
SYSAP_ROMTABLE_CID0	0xE00BEFF0	Component Identification Register 0.
SYSAP_ROMTABLE_CID1	0xE00BEFF4	Component Identification Register 1.

CPU Subsystem (CPUSS) registers

Register	Address	Description
SYSAP_ROMTABLE_CID2	0xE00BEFF8	Component Identification Register 2.
SYSAP_ROMTABLE_CID3	0xE00BEFFC	Component Identification Register 3.
CM33_ROMTABLE_TRC_CTI	0xE00BF000	CM33 CoreSight ROM Table Peripheral #0
CM33_ROMTABLE_TRC_TPIU	0xE00BF004	CM33 CoreSight ROM Table Peripheral #3
CM33_ROMTABLE_TRC_CSS600_ATBFUNNEL_CSTF	0xE00BF008	CM33 CoreSight ROM Table Peripheral #5
CM33_ROMTABLE_TRC_ETF	0xE00BF00C	CM33 CoreSight ROM Table Peripheral #2
CM33_ROMTABLE_CM33	0xE00BF010	CM33 CoreSight ROM Table Peripheral #6
CM33_ROMTABLE_CSMT	0xE00BFFCC	CM33 CoreSight ROM Table Memory Type
CM33_ROMTABLE_PID4	0xE00BFFD0	CM33 CoreSight ROM Table Peripheral ID #4
CM33_ROMTABLE_PID0	0xE00BFFE0	CM33 CoreSight ROM Table Peripheral ID #0
CM33_ROMTABLE_PID1	0xE00BFFE4	CM33 CoreSight ROM Table Peripheral ID #1
CM33_ROMTABLE_PID2	0xE00BFFE8	CM33 CoreSight ROM Table Peripheral ID #2
CM33_ROMTABLE_PID3	0xE00BFFEC	CM33 CoreSight ROM Table Peripheral ID #3
CM33_ROMTABLE_CID0	0xE00BFFF0	CM33 CoreSight ROM Table Component ID #0
CM33_ROMTABLE_CID1	0xE00BFFF4	CM33 CoreSight ROM Table Component ID #1
CM33_ROMTABLE_CID2	0xE00BFFF8	CM33 CoreSight ROM Table Component ID #2
CM33_ROMTABLE_CID3	0xE00BFFFC	CM33 CoreSight ROM Table Component ID #3
CM33_ROM_SCS	0xE00FF000	CM33 CoreSight ROM Table Peripheral #0
CM33_ROM_DWT	0xE00FF004	CM33 CoreSight ROM Table Peripheral #1
CM33_ROM_FPB	0xE00FF008	CM33 CoreSight ROM Table Peripheral #2
CM33_ROM_ITM	0xE00FF00C	CM33 CoreSight ROM Table Peripheral #3
CM33_ROM_ETM	0xE00FF014	CM33 CoreSight ROM Table Peripheral #4
CM33_ROM_CTI	0xE00FF018	CM33 CoreSight ROM Table Peripheral #5
CM33_ROM_MTB	0xE00FF01C	CM33 CoreSight ROM Table Peripheral #6
CM33_ROM_CSMT	0xE00FFFCC	CM33 CoreSight ROM Table Memory Type
CM33_ROM_PID4	0xE00FFFD0	CM33 CoreSight ROM Table Peripheral ID #4
CM33_ROM_PID0	0xE00FFFE0	CM33 CoreSight ROM Table Peripheral ID #0
CM33_ROM_PID1	0xE00FFFE4	CM33 CoreSight ROM Table Peripheral ID #1
CM33_ROM_PID2	0xE00FFFE8	CM33 CoreSight ROM Table Peripheral ID #2
CM33_ROM_PID3	0xE00FFFEC	CM33 CoreSight ROM Table Peripheral ID #3
CM33_ROM_CID0	0xE00FFFF0	CM33 CoreSight ROM Table Component ID #0
CM33_ROM_CID1	0xE00FFFF4	CM33 CoreSight ROM Table Component ID #1
CM33_ROM_CID2	0xE00FFFF8	CM33 CoreSight ROM Table Component ID #2
CM33_ROM_CID3	0xE00FFFFC	CM33 CoreSight ROM Table Component ID #3

1.1.1 RAMC_PPU0_PWPR

Power Policy Register

Address: 0x42100000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				PWR_POLICY [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None			RW
HW Access	None			R	None			R
Name	None [15:13]			LOCK_EN	None [11:9]			PWR_DY-N_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				OP_POLICY [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							OP_DY-N_EN

Bits	Name	Description
24	OP_DYN_EN	Reserved Default Value: 0x0
19 : 16	OP_POLICY	Reserved Default Value: 0x0
12	LOCK_EN	Reserved Default Value: 0x0
8	PWR_DYN_EN	Power mode dynamic transition enable. When this bit is set to 1 dynamic transitions are enabled for power modes, allowing transitions to be initiated by changes on power mode DEVACTIVE inputs. Default Value: 0x1
3 : 0	PWR_POLICY	Power mode policy. When static power mode transitions are enabled, PWR_DYN_EN is set to 0, this is the target power mode for the PPU. When dynamic power mode transitions are enabled, PWR_DYN_EN is set to 1, this is the minimum power mode for the PPU. This PPU supports the following modes: OFF(0), MEM_RET(2), ON(8). Do not use WARM_RST(9) or other unsupported modes. Default Value: 0x8

1.1.2 RAMC_PPU0_PMER

Power Mode Emulation Register

Address: 0x42100004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							EMU_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	EMU_EN	Reserved Default Value: 0x0

1.1.3 RAMC_PPU0_PWSR

Power Status Register

Address: 0x42100008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				RW			
Name	None [7:4]				PWR_STATUS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None			R	None			R
HW Access	None			RW	None			RW
Name	None [15:13]			LOCK_STATUS	None [11:9]			PWR_DYN_STATUS

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				RW			
Name	None [23:20]				OP_STATUS [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							RW
Name	None [31:25]							OP_DYN_STATUS

Bits	Name	Description
24	OP_DYN_STATUS	Reserved Default Value: 0x0
19 : 16	OP_STATUS	Reserved Default Value: 0x0
12	LOCK_STATUS	Reserved Default Value: 0x0
8	PWR_DYN_STATUS	Power mode dynamic transition status. When set to 1 power mode dynamic transitions are enabled. There might be a delay in dynamic transitions becoming active or inactive if the PPU is transitioning when PWR_DYN_EN is programmed. Default Value: 0x0
3 : 0	PWR_STATUS	Power mode status. These bits reflect the current power mode of the PPU. See PPU_PWPR.PWR_POLICY for power mode enumeration. Default Value: 0x0

1.1.4 RAMC_PPU0_DISR

Device Interface Input Current Status Register

Address: 0x42100010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	PWR_DEVACTIVE_STATUS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None					R		
HW Access	None					RW		
Name	None [15:11]					PWR_DEVACTIVE_STATUS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	OP_DEVACTIVE_STATUS [31:24]							

Bits	Name	Description
31 : 24	OP_DEVACTIVE_STATUS	Reserved Default Value: 0x0
10 : 0	PWR_DEVACTIVE_STATUS	Status of the power mode DEVACTIVE inputs. There is one bit for each device interface Q-Channel DEVQACTIVE. For example, bit 0 is for Q-channel device 0 DEVQACTIVE. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x0

1.1.5 RAMC_PPU0_MISR

Miscellaneous Input Current Status Register

Address: 0x42100014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							PCSMPACCEPT_STATUS

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	DEVACCEPT_STATUS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	DEVDENY_STATUS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	DEVDENY_STATUS	Status of the device interface DEVDENY inputs. There is one bit for each device interface DEVQDENY. For example, bit 16 is for Q-Channel 0 DEVQDENY, and bit 17 for Q-Channel 1 DEVQDENY. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x0
15 : 8	DEVACCEPT_STATUS	Status of the device interface DEVACCEPT inputs. There is one bit for each device interface DEVQACCEPTn. For example, bit 8 is for Q-Channel 0 DEVQACCEPTn and bit 9 for Q-Channel 1 DEVQACCEPTn. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x0
0	PCSMPACCEPT_STATUS	The status of the PCSMPACCEPT input. Default Value: 0x0

1.1.6 RAMC_PPU0_STSR

Stored Status Register

Address: 0x42100018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	STORED_DEVDENY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	STORED_DEVDENY	Reserved (this PPU has a single Q-channel) Default Value: 0x0

1.1.7 RAMC_PPU0_UNLK

Unlock register

Address: 0x4210001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							UNLOCK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	UNLOCK	Reserved Default Value: 0x0

1.1.8 RAMC_PPU0_PWCR

Power Configuration Register

Address: 0x42100020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DEVREQEN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PWR_DEVACTIVEEN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					R		
Name	None [23:19]					PWR_DEVACTIVEEN [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	OP_DEVACTIVEEN [31:24]							

Bits	Name	Description
31 : 24	OP_DEVACTIVEEN	Reserved Default Value: 0x0
18 : 8	PWR_DEVACTIVEEN	These bits enable the power mode DEVACTIVE inputs. When a bit is to 1 the related DEVACTIVE input is enabled, when set to 0 it is disabled. All available bits are reset to 1. There is one bit for each device interface Q-Channel DEVQACTIVE. For example, bit 8 is for the Q-Channel 0 DEVQACTIVE, and bit 9 for the Q-Channel 1 DEVQACTIVE. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x001
7 : 0	DEVREQEN	When set to 1 enables the device interface handshake for transitions. All available bits are reset to 1. There is one bit for each device interface channel. For example, bit 0 is for Q-Channel 0, and bit 1 is for Q-Channel 1. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x01

1.1.9 RAMC_PPU0_PTCR

Power Mode Transition Configuration Register

Address: 0x42100024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						DBG_RE-COV_POR ST_EN	WARM_RS T_DEVREQ EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	DBG_RE-COV_PORST_EN	Reserved Default Value: 0x0
0	WARM_RST_DEVREQEN	Transition behavior between ON and WARM_RST. This bit should not be modified when the PPU is in WARM_RST, or if the PPU is performing a transition, otherwise PPU behavior is UN-PREDICTABLE. 0: The PPU does not perform a device interface handshake when transitioning between ON and WARM_RST. 1: The PPU performs a device interface handshake when transitioning between ON and WARM_RST. This disables all Q-Channels for this transition. Default Value: 0x0

1.1.10 RAMC_PPU0_IMR

Interrupt Mask Register

Address: 0x42100030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		LOCKED_IRQ_MASK	EMU_DENY_IRQ_MASK	EMU_ACCEPT_IRQ_MASK	STA_DENY_IRQ_MASK	STA_ACCEPT_IRQ_MASK	STA_POLICY_TRN_IRQ_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	LOCKED_IRQ_MASK	Reserved Default Value: 0x1
4	EMU_DENY_IRQ_MASK	Reserved Default Value: 0x1
3	EMU_ACCEPT_IRQ_MASK	Reserved Default Value: 0x1
2	STA_DENY_IRQ_MASK	Static transition denial event mask. Default Value: 0x0
1	STA_ACCEPT_IRQ_MASK	Static transition acceptance event mask. Default Value: 0x1
0	STA_POLICY_TRN_IRQ_MASK	Static full policy transition completion event mask. Default Value: 0x0

1.1.11 RAMC_PPU0_AIMR

Additional Interrupt Mask Register

Address: 0x42100034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			STA_POLICY_OP_IRQ_MASK	STA_POLICY_PWR_IRQ_MASK	DYN_DENY_IRQ_MASK	DYN_ACCEPT_IRQ_MASK	UNSPT_POLICY_IRQ_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	STA_POLICY_OP_IRQ_MASK	Reserved Default Value: 0x1
3	STA_POLICY_PWR_IRQ_MASK	Reserved Default Value: 0x1
2	DYN_DENY_IRQ_MASK	Dynamic transition denial event mask. Default Value: 0x1
1	DYN_ACCEPT_IRQ_MASK	Dynamic transition acceptance event mask. Default Value: 0x1
0	UNSPT_POLICY_IRQ_MASK	Unsupported Policy event mask. Default Value: 0x0

1.1.12 RAMC_PPU0_ISR

Interrupt Status Register

Address: 0x42100038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	None	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	None	R	R	R	R	R	R
Name	OTH-ER_IRQ	None	LOCKED_IRQ	EMU_DE-NY_IRQ	EMU_AC-CEPT_IRQ	STA_DE-NY_IRQ	STA_AC-CEPT_IRQ	STA_POLI-CY_TRN_IRQ

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	R							
Name	PWR_ACTIVE_EDGE_IRQ [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW1C		
HW Access	None					R		
Name	None [23:19]					PWR_ACTIVE_EDGE_IRQ [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	R							
Name	OP_ACTIVE_EDGE_IRQ [31:24]							

Bits	Name	Description
31 : 24	OP_ACTIVE_EDGE_IRQ	Indicates which operating mode DEVPACTIVE inputs caused the input edge event. When operating modes are not supported this field is reserved. Default Value: 0x0
18 : 8	PWR_ACTIVE_EDGE_IRQ	Indicates which power mode DEVACTIVE inputs caused the input edge event. Bits for unused channels are the MSBs and are reserved. There is one bit for each device Q-Channel DEVQACTIVE. For example, bit 8 is for the Q-Channel 0 DEVQACTIVE. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x00
7	OTHER_IRQ	Indicates there is an interrupt event pending in the Additional Interrupt Status Register (PPU_AISR). Default Value: 0x0
5	LOCKED_IRQ	Reserved Default Value: 0x0
4	EMU_DENY_IRQ	Reserved Default Value: 0x0
3	EMU_ACCEPT_IRQ	Reserved Default Value: 0x0
2	STA_DENY_IRQ	Static transition denial event status. Default Value: 0x0
1	STA_ACCEPT_IRQ	Static transition acceptance event status. Default Value: 0x0

1.1.12 RAMC_PPU0_ISR (continued)

0	STA_POLICY_TRN_IRQ	Static full policy transition completion event status. Default Value: 0x0

1.1.13 RAMC_PPU0_AISR

Additional Interrupt Status Register

Address: 0x4210003C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None			R	R	R	R	R
Name	None [7:5]			STA_POLICY_OP_IRQ	STA_POLICY_PWR_IRQ	DYN_DENY_IRQ	DYN_ACCEPT_IRQ	UNSPT_POLICY_IRQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	STA_POLICY_OP_IRQ	Reserved Default Value: 0x0
3	STA_POLICY_PWR_IRQ	Reserved Default Value: 0x0
2	DYN_DENY_IRQ	Dynamic transition denial event status. Default Value: 0x0
1	DYN_ACCEPT_IRQ	Dynamic transition acceptance event status. Default Value: 0x0
0	UNSPT_POLICY_IRQ	Unsupported Policy event status. Default Value: 0x0

1.1.14 RAMC_PPU0_IESR

Input Edge Sensitivity Register

Address: 0x42100040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE03_EDGE [7:6]		DEVACTIVE02_EDGE [5:4]		DEVACTIVE01_EDGE [3:2]		DEVACTIVE00_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE07_EDGE [15:14]		DEVACTIVE06_EDGE [13:12]		DEVACTIVE05_EDGE [11:10]		DEVACTIVE04_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [23:22]		DEVACTIVE10_EDGE [21:20]		DEVACTIVE09_EDGE [19:18]		DEVACTIVE08_EDGE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21 : 20	DEVACTIVE10_EDGE	Reserved Default Value: 0x0
19 : 18	DEVACTIVE09_EDGE	Reserved Default Value: 0x0
17 : 16	DEVACTIVE08_EDGE	Reserved Default Value: 0x0
15 : 14	DEVACTIVE07_EDGE	Reserved Default Value: 0x0
13 : 12	DEVACTIVE06_EDGE	Reserved Default Value: 0x0
11 : 10	DEVACTIVE05_EDGE	Reserved Default Value: 0x0
9 : 8	DEVACTIVE04_EDGE	Reserved Default Value: 0x0
7 : 6	DEVACTIVE03_EDGE	Reserved Default Value: 0x0
5 : 4	DEVACTIVE02_EDGE	Reserved Default Value: 0x0
3 : 2	DEVACTIVE01_EDGE	Reserved Default Value: 0x0

1.1.14 RAMC_PPU0_IESR (continued)

1 : 0	DEVACTIVE00_EDGE	DEVACTIVE 0 edge sensitivity. Default Value: 0x0

1.1.15 RAMC_PPU0_OPSR

Operating Mode Active Edge Sensitivity Register

Address: 0x42100044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE19_EDGE [7:6]		DEVACTIVE18_EDGE [5:4]		DEVACTIVE17_EDGE [3:2]		DEVACTIVE16_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE23_EDGE [15:14]		DEVACTIVE22_EDGE [13:12]		DEVACTIVE21_EDGE [11:10]		DEVACTIVE20_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 14	DEVACTIVE23_EDGE	Reserved Default Value: 0x0
13 : 12	DEVACTIVE22_EDGE	Reserved Default Value: 0x0
11 : 10	DEVACTIVE21_EDGE	Reserved Default Value: 0x0
9 : 8	DEVACTIVE20_EDGE	Reserved Default Value: 0x0
7 : 6	DEVACTIVE19_EDGE	Reserved Default Value: 0x0
5 : 4	DEVACTIVE18_EDGE	Reserved Default Value: 0x0
3 : 2	DEVACTIVE17_EDGE	Reserved Default Value: 0x0
1 : 0	DEVACTIVE16_EDGE	Reserved Default Value: 0x0

1.1.16 RAMC_PPU0_FUNRR

Functional Retention RAM Configuration Register

Address: 0x42100050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FUNC_RET_RAM_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	FUNC_RET_RAM_CFG	Reserved Default Value: 0x0

1.1.17 RAMC_PPU0_FULRR

Full Retention RAM Configuration Register

Address: 0x42100054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FULL_RET_RAM_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	FULL_RET_RAM_CFG	Reserved Default Value: 0x0

1.1.18 RAMC_PPU0_MEMRR

Memory Retention RAM Configuration Register

Address: 0x42100058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MEM_RET_RAM_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	MEM_RET_RAM_CFG	Reserved Default Value: 0x0

1.1.19 RAMC_PPU0_EDTR0

Power Mode Entry Delay Register 0

Address: 0x42100160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	OFF_DEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MEM_RET_DEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	LOGIC_RET_DEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	FULL_RET_DEL [31:24]							

Bits	Name	Description
31 : 24	FULL_RET_DEL	Reserved Default Value: 0x00
23 : 16	LOGIC_RET_DEL	Reserved Default Value: 0x00
15 : 8	MEM_RET_DEL	Reserved Default Value: 0x00
7 : 0	OFF_DEL	Reserved Default Value: 0x00

1.1.20 RAMC_PPU0_EDTR1

Power Mode Entry Delay Register 1

Address: 0x42100164

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MEM_OFF_DEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	FUNC_RET_DEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	FUNC_RET_DEL	Reserved Default Value: 0x00
7 : 0	MEM_OFF_DEL	Reserved Default Value: 0x00

1.1.21 RAMC_PPU0_DCDR0

Device Control Delay Configuration Register 0

Address: 0x42100170

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CLKEN_RST_DLY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	ISO_CLKEN_DLY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	RST_HWSTAT_DLY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	RST_HWSTAT_DLY	Reserved Default Value: 0x0
15 : 8	ISO_CLKEN_DLY	Reserved Default Value: 0x0
7 : 0	CLKEN_RST_DLY	Reserved Default Value: 0x0

1.1.22 RAMC_PPU0_DCDR1

Device Control Delay Configuration Register 1

Address: 0x42100174

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ISO_RST_DLY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CLKEN_ISO_DLY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	CLKEN_ISO_DLY	Reserved Default Value: 0x0
7 : 0	ISO_RST_DLY	Reserved Default Value: 0x0

1.1.23 RAMC_PPU0_IDR0

PPU Identification Register 0

Address: 0x42100FB0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	NUM_OPMODE [7:4]				DEVCHAN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	STA_-FUNC_RET_SPT	STA_-FULL_RET_SPT	STA_MEM_OFF_SPT	STA_LG-C_RET_SPT	STA_MEM_RET_EMU_SPT	STA_MEM_RET_SPT	STA_OFF_EMU_SPT	STA_OFF_SPT

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	None	R	R	R
HW Access	RW	RW	RW	RW	None	RW	RW	RW
Name	DY-N_MEM_RET_EMU_SPT	DY-N_MEM_RET_SPT	DY-N_OFF_EMU_SPT	DY-N_OFF_SPT	None	STA_DB-G_RE-COV_SPT	STA_WRM_RST_SPT	STA_ON_SPT

Bits	31	30	29	28	27	26	25	24
SW Access	None		R	R	R	R	R	R
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [31:30]		DY-N_WRM_RST_SPT	DY-N_ON_SPT	DYN_-FUNC_RET_SPT	DYN_-FULL_RET_SPT	DY-N_MEM_OFF_SPT	DYN_LG-C_RET_SPT

Bits	Name	Description
29	DYN_WRM_RST_SPT	Dynamic WARM_RST support. Default Value: 0x0
28	DYN_ON_SPT	Dynamic ON support. Default Value: 0x1
27	DYN_FUNC_RET_SPT	Dynamic FUNC_RET support. Default Value: 0x0
26	DYN_FULL_RET_SPT	Dynamic FULL_RET support. Default Value: 0x0
25	DYN_MEM_OFF_SPT	Dynamic MEM_OFF support. Default Value: 0x0
24	DYN_LGC_RET_SPT	Dynamic LOGIC_RET support. Default Value: 0x0
23	DY-N_MEM_RET_EMU_SPT	Dynamic MEM_RET_EMU support Default Value: 0x0
22	DYN_MEM_RET_SPT	Dynamic MEM_RET support. Default Value: 0x1

1.1.23 RAMC_PPU0_IDR0 (continued)

21	DYN_OFF_EMU_SPT	Dynamic OFF_EMU support. Default Value: 0x0
20	DYN_OFF_SPT	Dynamic OFF support. Default Value: 0x1
18	STA_DBG_RECOV_SPT	DBG_RECOV support. Default Value: 0x0
17	STA_WRM_RST_SPT	WARM_RST support. Ignore this bit. Do not use WARM_RST. Default Value: 0x1
16	STA_ON_SPT	ON support. Default Value: 0x1
15	STA_FUNC_RET_SPT	FUNC_RET support. Default Value: 0x0
14	STA_FULL_RET_SPT	FULL_RET support. Default Value: 0x0
13	STA_MEM_OFF_SPT	MEM_OFF support. Default Value: 0x0
12	STA_LGC_RET_SPT	LOGIC_RET support. Default Value: 0x0
11	STA_MEM_RET_EMU_SPT	MEM_RET_EMU support. Default Value: 0x0
10	STA_MEM_RET_SPT	MEM_RET support. Default Value: 0x1
9	STA_OFF_EMU_SPT	OFF_EMU support. Default Value: 0x0
8	STA_OFF_SPT	OFF support. Default Value: 0x1
7 : 4	NUM_OPMODE	No. of operating modes supported is NUM_OPMODE + 1. Default Value: 0x0
3 : 0	DEVCHAN	No. of Device Interface Channels. The device enumeration is: Device 0: PDCM Default Value: 1

1.1.24 RAMC_PPU0_IDR1

PPU Identification Register 1

Address: 0x42100FB4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R	R	R	None	R	R	R
HW Access	None	RW	RW	RW	None	RW	RW	RW
Name	None	FUNC_RET_RAM_REG	FULL_RET_RAM_REG	MEM_RET_RAM_REG	None	LOCK_SPT	SW_DEV_DEL_SPT	PWR_MODE_ENTRY_DEL_SPT

Bits	15	14	13	12	11	10	9	8
SW Access	None			R	None	R	R	R
HW Access	None			RW	None	RW	RW	RW
Name	None [15:13]			OFF_MEM_RET_TRANS	None	OP_ACTIVE	STA_POLICY_OP_IRQ_SPT	STA_POLICY_PWR_IRQ_SPT

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	OFF_MEM_RET_TRANS	OFF to MEM_RET direct transition. Indicates if direct transitions from OFF to MEM_RET and from OFF_EMU to MEM_RET_EMU are supported. Default Value: 0x0
10	OP_ACTIVE	Reserved Default Value: 0x0
9	STA_POLICY_OP_IRQ_SPT	Operating policy transition completion event status. Default Value: 0x0
8	STA_POLICY_PWR_IRQ_SPT	Power policy transition completion event status. Default Value: 0x0
6	FUNC_RET_RAM_REG	Indicates if the PPU_FUNRR register is present or reserved. 0: Reserved. 1: Present. Default Value: 0x0
5	FULL_RET_RAM_REG	Indicates if the PPU_FULRR register is present or reserved. 0: Reserved. 1: Present. Default Value: 0x0
4	MEM_RET_RAM_REG	Indicates if the PPU_MEMRR register is present or reserved. 0: Reserved. 1: Present. Default Value: 0x1
2	LOCK_SPT	Lock and the lock interrupt event are supported. Default Value: 0x0

1.1.24 RAMC_PPU0_IDR1 (continued)

1	SW_DEV_DEL_SPT	Software device delay control configuration support. Default Value: 0x0
0	PWR_MODE_EN- TRY_DEL_SPT	Power mode entry delay support. Default Value: 0x0

1.1.25 RAMC_PPU0_IIDR

Implementation Identification Register

Address: 0x42100FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	IMPLEMENTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R				R			
HW Access	RW				RW			
Name	REVISION [15:12]				IMPLEMENTER [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access	RW				RW			
Name	PRODUCT_ID [23:20]				VARIANT [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	PRODUCT_ID [31:24]							

Bits	Name	Description
31 : 20	PRODUCT_ID	PPU part identification. Default Value: 0x0B5
19 : 16	VARIANT	Major revision of the product. Default Value: 0
15 : 12	REVISION	Minor revision of the product. Default Value: 0
11 : 0	IMPLEMENTER	Implementer identification. [11:8] The JEP106 continuation code of the implementer. [7] Always 0. [6:0] The JEP106 identity code of the implementer. For an Arm implementation, bits [11:0] are 0x43B. Default Value: 0x43B

1.1.26 RAMC_PPU0_AIDR

Architecture Identification Register

Address: 0x42100FCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	ARCH_REV_MAJOR [7:4]				ARCH_REV_MINOR [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	ARCH_REV_MAJOR	0x1 - PPU architecture major revision 1. Other Values - Reserved. Default Value: 0x1
3 : 0	ARCH_REV_MINOR	0x1 - PPU Architecture minor revision 1. Other Values - Reserved. Default Value: 0x1

1.1.27 RAMC_PPU0_PID4

Implementation Defined Identification Register (PID4)

Address: 0x42100FD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				RW			
Name	None [7:4]				IMPLEMENTER_11_8 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	IMPLEMENTER_11_8	The JEP106 continuation code of the implementer, which is 0x4 hardcoded value. Default Value: 0x4

1.1.28 RAMC_PPU0_PID0

Implementation Defined Identification Register (PID0)

Address: 0x42100FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	PRODUCT_ID_7_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	PRODUCT_ID_7_0	PPU part identification bits [7:0]. Default Value: 0xB5

1.1.29 RAMC_PPU0_PID1

Implementation Defined Identification Register (PID1)

Address: 0x42100FE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	IMPLEMENTER_3_0 [7:4]				PRODUCT_ID_11_8 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	IMPLEMENTER_3_0	JEP106_ID bits [3:0] Default Value: 0xB
3 : 0	PRODUCT_ID_11_8	PPU part identification bits [11:8] Default Value: 0x0

1.1.30 RAMC_PPU0_PID2

Implementation Defined Identification Register (PID2)

Address: 0x42100FE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R	R		
HW Access	RW				RW	RW		
Name	REV_CONST [7:4]				CON-ST_HIGH	IMPLEMENTER_6_4 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	REV_CONST	Constant LOW Revision (4 bits) Default Value: 0x0
3	CONST_HIGH	Constant HIGH Default Value: 0x1
2 : 0	IMPLEMENTER_6_4	JEP106_ID bits [6:4] Default Value: 0x3

1.1.31 RAMC_PPU0_PID3

Implementation Defined Identification Register (PID3)

Address: 0x42100FEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	PID3_REVISION [7:4]				PID3_REV_CONST [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	PID3_REVISION	Minor revision of the product. Default Value: 0x0
3 : 0	PID3_REV_CONST	Constant LOW (4 bits) Default Value: 0x0

1.1.32 RAMC_PPU0_ID0

Implementation Defined Identification Register (ID0)

Address: 0x42100FF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ID0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	ID0	ID0 hard coded value Default Value: 0x0D

1.1.33 RAMC_PPU0_ID1

Implementation Defined Identification Register (ID1)

Address: 0x42100FF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ID1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	ID1	ID1 hardcoded value Default Value: 0xF0

1.1.34 RAMC_PPU0_ID2

Implementation Defined Identification Register (ID2)

Address: 0x42100FF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ID2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	ID2	ID2 hardcoded value Default Value: 0x05

1.1.35 RAMC_PPU0_ID3

Implementation Defined Identification Register (ID3)

Address: 0x42100FFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ID3 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	ID3	ID3 hardcoded value Default Value: 0xB1

1.1.36 ICACHE0_CTL

Cache control

Address: 0x42103000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						WAY [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None	RW				
HW Access	R	R	None	R				
Name	CA_EN	PREF_EN	None	SET_ADDR [28:24]				

Bits	Name	Description
31	CA_EN	Cache enable: 0: Disabled. The cache tag valid bits are reset to "0"s and the cache LRU information is set to "1"s (making way 0 the LRU way and way 3 the MRU way). 1: Enabled. Default Value: 1
30	PREF_EN	Prefetch enable: 0: Disabled. 1: Enabled. Prefetching requires the cache to be enabled; i.e. ENABLED is "1". Default Value: 1
28 : 24	SET_ADDR	Specifies the cache set for which cache information is provided in STATUS0/1/2. Default Value: 0
17 : 16	WAY	Specifies the cache way for which cache information is provided in STATUS0/1/2. Default Value: 0

1.1.37 ICACHE0_CMD

Cache command

Address: 0x42103008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						RW1C	RW1C
Name	None [7:2]						BUFF_INV	INV

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	BUFF_INV	Invalidation of buffers (does not invalidate the caches). SW writes a "1" to clear the buffers. HW sets this field to "0" when the operation is completed. Default Value: 0
0	INV	Invalidation of cahce and buffer. SW writes a "1" to clear the caches. HW sets this field to "0" when the operation is completed. The caches' LRU structures are also reset to their default state. Default Value: 0

1.1.38 ICACHE0_STATUS0

Cache status 0

Address: 0x42103080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VALID32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	VALID32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	VALID32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	VALID32 [31:24]							

Bits	Name	Description
31 : 0	VALID32	Sixteen valid bits of the cache line specified by CTL.WAY and CTL.SET_ADDR. Default Value: 0

1.1.39 ICACHE0_STATUS1

Cache status 1

Address: 0x42103084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	TAG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	TAG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	TAG [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	TAG [31:24]							

Bits	Name	Description
31 : 0	TAG	Cache line address of the cache line specified by CTL.WAY and CTL.SET_ADDR. Default Value: Undefined

1.1.40 ICACHE0_STATUS2

Cache status 2

Address: 0x42103088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R					
HW Access	None		W					
Name	None [7:6]		LRU [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	LRU	Six bit LRU representation of the cache set specified by CTL.SET_ADDR. The encoding of the field is as follows ("X_LRU_Y" indicates that way X is Less Recently Used than way Y): Bit 5: 0_LRU_1: way 0 less recently used than way 1. Bit 4: 0_LRU_2. Bit 3: 0_LRU_3. Bit 2: 1_LRU_2. Bit 1: 1_LRU_3. Bit 0: 2_LRU_3. Default Value: 0x3F

1.1.41 CPUSS_PPU_PWPR

Power Policy Register

Address: 0x42105000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				PWR_POLICY [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None			RW
HW Access	None			R	None			R
Name	None [15:13]			LOCK_EN	None [11:9]			PWR_DYN_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				OP_POLICY [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							OP_DYN_EN

Bits	Name	Description
24	OP_DYN_EN	Reserved Default Value: 0x0
19 : 16	OP_POLICY	Reserved Default Value: 0x0
12	LOCK_EN	Reserved Default Value: 0x0
8	PWR_DYN_EN	Power mode dynamic transition enable. When this bit is set to 1 dynamic transitions are enabled for power modes, allowing transitions to be initiated by changes on power mode DEVACTIVE inputs. Default Value: 0x1
3 : 0	PWR_POLICY	Power mode policy. When static power mode transitions are enabled, PWR_DYN_EN is set to 0, this is the target power mode for the PPU. When dynamic power mode transitions are enabled, PWR_DYN_EN is set to 1, this is the minimum power mode for the PPU. This PPU supports the following modes: OFF(0), FULL_RET(5), ON(8). Do not use WARM_RST(9) or other unsupported modes. Default Value: 0x8

1.1.42 CPUSS_PPU_PMER

Power Mode Emulation Register

Address: 0x42105004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							EMU_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	EMU_EN	Reserved Default Value: 0x0

1.1.43 CPUSS_PPU_PWSR

Power Status Register

Address: 0x42105008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				RW			
Name	None [7:4]				PWR_STATUS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None			R	None			R
HW Access	None			RW	None			RW
Name	None [15:13]			LOCK_STA-TUS	None [11:9]			PWR_DY-N_STATUS

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				RW			
Name	None [23:20]				OP_STATUS [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							RW
Name	None [31:25]							OP_DY-N_STATUS

Bits	Name	Description
24	OP_DYN_STATUS	Reserved Default Value: 0x0
19 : 16	OP_STATUS	Reserved Default Value: 0x0
12	LOCK_STATUS	Reserved Default Value: 0x0
8	PWR_DYN_STATUS	Power mode dynamic transition status. When set to 1 power mode dynamic transitions are enabled. There might be a delay in dynamic transitions becoming active or inactive if the PPU is transitioning when PWR_DYN_EN is programmed. Default Value: 0x0
3 : 0	PWR_STATUS	Power mode status. These bits reflect the current power mode of the PPU. See PPU_PWPR.PWR_POLICY for power mode enumeration. Default Value: 0x0

1.1.44 CPUSS_PPU_DISR

Device Interface Input Current Status Register

Address: 0x42105010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	PWR_DEVACTIVE_STATUS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None					R		
HW Access	None					RW		
Name	None [15:11]					PWR_DEVACTIVE_STATUS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	OP_DEVACTIVE_STATUS [31:24]							

Bits	Name	Description
31 : 24	OP_DEVACTIVE_STATUS	Reserved Default Value: 0x0
10 : 0	PWR_DEVACTIVE_STATUS	Status of the power mode DEVACTIVE inputs. There is one bit for each device interface Q-Channel DEVQACTIVE. For example, bit 0 is for Q-channel device 0 DEVQACTIVE. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x0

1.1.45 CPUSS_PPU_MISR

Miscellaneous Input Current Status Register

Address: 0x42105014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							PCSMPAC-CEPT_STA-TUS

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	DEVACCEPT_STATUS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	DEVDENY_STATUS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	DEVDENY_STATUS	Status of the device interface DEVDENY inputs. There is one bit for each device interface DEVQDENY. For example, bit 16 is for Q-Channel 0 DEVQDENY, and bit 17 for Q-Channel 1 DEVQDENY. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x0
15 : 8	DEVACCEPT_STATUS	Status of the device interface DEVACCEPT inputs. There is one bit for each device interface DEVQACCEPTn. For example, bit 8 is for Q-Channel 0 DEVQACCEPTn and bit 9 for Q-Channel 1 DEVQACCEPTn. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x0
0	PCSMPACCEPT_STA-TUS	The status of the PCSMPACCEPT input. Default Value: 0x0

1.1.46 CPUSS_PPU_STSR

Stored Status Register

Address: 0x42105018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	STORED_DEVDENY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	STORED_DEVDENY	Status of the DEVDENY signals from the last device interface Q-Channel transition. For Q-Channel: There is one bit for each device interface DEVQDENY. For example, bit 0 is for Q-Channel 0 DEVQDENY, and bit 1 for Q-Channel 1 DEVQDENY. Refer to PPU_DISR.PWR_DEVACTIVE_STATUS for device enumeration. Default Value: 0x0

1.1.47 CPUSS_PPU_UNLK

Unlock register

Address: 0x4210501C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							UNLOCK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	UNLOCK	Reserved Default Value: 0x0

1.1.48 CPUSS_PPU_PWCR

Power Configuration Register

Address: 0x42105020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DEVREQEN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PWR_DEVACTIVEEN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					R		
Name	None [23:19]					PWR_DEVACTIVEEN [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	OP_DEVACTIVEEN [31:24]							

Bits	Name	Description
31 : 24	OP_DEVACTIVEEN	Reserved Default Value: 0x00
18 : 8	PWR_DEVACTIVEEN	These bits enable the power mode DEVACTIVE inputs. When a bit is to 1 the related DEVACTIVE input is enabled, when set to 0 it is disabled. All available bits are reset to 1. There is one bit for each device interface Q-Channel DEVQACTIVE. For example, bit 8 is for the Q-Channel 0 DEVQACTIVE, and bit 9 for the Q-Channel 1 DEVQACTIVE. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x03
7 : 0	DEVREQEN	When set to 1 enables the device interface handshake for transitions. All available bits are reset to 1. There is one bit for each device interface channel. For example, bit 0 is for Q-Channel 0, and bit 1 is for Q-Channel 1. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x03

1.1.49 CPUSS_PPU_PTCR

Power Mode Transition Configuration Register

Address: 0x42105024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						DBG_RE-COV_POR ST_EN	WARM_RS T_DEVREQ EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	DBG_RE-COV_PORST_EN	Reserved Default Value: 0x0
0	WARM_RST_DEVREQEN	Transition behavior between ON and WARM_RST. This bit should not be modified when the PPU is in WARM_RST, or if the PPU is performing a transition, otherwise PPU behavior is UN-PREDICTABLE. 0: The PPU does not perform a device interface handshake when transitioning between ON and WARM_RST. 1: The PPU performs a device interface handshake when transitioning between ON and WARM_RST. This disables all Q-Channels for this transition. Default Value: 0x0

1.1.50 CPUSS_PPU_IMR

Interrupt Mask Register

Address: 0x42105030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		LOCKED_IRQ_MASK	EMU_DENY_IRQ_MASK	EMU_ACCEPT_IRQ_MASK	STA_DENY_IRQ_MASK	STA_ACCEPT_IRQ_MASK	STA_POLICY_TRN_IRQ_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	LOCKED_IRQ_MASK	Reserved Default Value: 0x0
4	EMU_DENY_IRQ_MASK	Reserved Default Value: 0x0
3	EMU_ACCEPT_IRQ_MASK	Reserved Default Value: 0x0
2	STA_DENY_IRQ_MASK	Static transition denial event mask. Default Value: 0x0
1	STA_ACCEPT_IRQ_MASK	Static transition acceptance event mask. Default Value: 0x1
0	STA_POLICY_TRN_IRQ_MASK	Static full policy transition completion event mask. Default Value: 0x0

1.1.51 CPUSS_PPU_AIMR

Additional Interrupt Mask Register

Address: 0x42105034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			STA_POLICY_OP_IRQ_MASK	STA_POLICY_PWR_IRQ_MASK	DYN_DENY_IRQ_MASK	DYN_ACCEPT_IRQ_MASK	UNSPT_POLICY_IRQ_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	STA_POLICY_OP_IRQ_MASK	Reserved Default Value: 0x0
3	STA_POLICY_PWR_IRQ_MASK	Reserved Default Value: 0x0
2	DYN_DENY_IRQ_MASK	Dynamic transition denial event mask. Default Value: 0x1
1	DYN_ACCEPT_IRQ_MASK	Dynamic transition acceptance event mask. Default Value: 0x1
0	UNSPT_POLICY_IRQ_MASK	Unsupported Policy event mask. Default Value: 0x0

1.1.52 CPUSS_PPU_ISR

Interrupt Status Register

Address: 0x42105038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	None	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	None	R	R	R	R	R	R
Name	OTH-ER_IRQ	None	LOCKED_IRQ	EMU_DE-NY_IRQ	EMU_AC-CEPT_IRQ	STA_DE-NY_IRQ	STA_AC-CEPT_IRQ	STA_POLI-CY_TRN_IRQ

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	R							
Name	PWR_ACTIVE_EDGE_IRQ [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW1C		
HW Access	None					R		
Name	None [23:19]					PWR_ACTIVE_EDGE_IRQ [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	R							
Name	OP_ACTIVE_EDGE_IRQ [31:24]							

Bits	Name	Description
31 : 24	OP_ACTIVE_EDGE_IRQ	Indicates which operating mode DEVPACTIVE inputs caused the input edge event. When operating modes are not supported this field is reserved. Default Value: 0x0
18 : 8	PWR_ACTIVE_EDGE_IRQ	Indicates which power mode DEVACTIVE inputs caused the input edge event. Bits for unused channels are the MSBs and are reserved. There is one bit for each device Q-Channel DEVQACTIVE. For example, bit 8 is for the Q-Channel 0 DEVQACTIVE. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x00
7	OTHER_IRQ	Indicates there is an interrupt event pending in the Additional Interrupt Status Register (PPU_AISR). Default Value: 0x0
5	LOCKED_IRQ	Reserved Default Value: 0x0
4	EMU_DENY_IRQ	Reserved Default Value: 0x0
3	EMU_ACCEPT_IRQ	Reserved Default Value: 0x0
2	STA_DENY_IRQ	Static transition denial event status. Default Value: 0x0
1	STA_ACCEPT_IRQ	Static transition acceptance event status. Default Value: 0x0

1.1.52 CPUSS_PPU_ISR (continued)

0	STA_POLICY_TRN_IRQ	Static full policy transition completion event status. Default Value: 0x0

1.1.53 CPUSS_PPU_AISR

Additional Interrupt Status Register

Address: 0x4210503C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None			R	R	R	R	R
Name	None [7:5]			STA_POLICY_OP_IRQ	STA_POLICY_PWR_IRQ	DYN_DENY_IRQ	DYN_ACCEPT_IRQ	UNSPT_POLICY_IRQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	STA_POLICY_OP_IRQ	Reserved Default Value: 0x0
3	STA_POLICY_PWR_IRQ	Reserved Default Value: 0x0
2	DYN_DENY_IRQ	Dynamic transition denial event status. Default Value: 0x0
1	DYN_ACCEPT_IRQ	Dynamic transition acceptance event status. Default Value: 0x0
0	UNSPT_POLICY_IRQ	Unsupported Policy event status. Default Value: 0x0

1.1.54 CPUSS_PPU_IESR

Input Edge Sensitivity Register

Address: 0x42105040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE03_EDGE [7:6]		DEVACTIVE02_EDGE [5:4]		DEVACTIVE01_EDGE [3:2]		DEVACTIVE00_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE07_EDGE [15:14]		DEVACTIVE06_EDGE [13:12]		DEVACTIVE05_EDGE [11:10]		DEVACTIVE04_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [23:22]		DEVACTIVE10_EDGE [21:20]		DEVACTIVE09_EDGE [19:18]		DEVACTIVE08_EDGE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21 : 20	DEVACTIVE10_EDGE	Reserved Default Value: 0x0
19 : 18	DEVACTIVE09_EDGE	Reserved Default Value: 0x0
17 : 16	DEVACTIVE08_EDGE	Reserved Default Value: 0x0
15 : 14	DEVACTIVE07_EDGE	Reserved Default Value: 0x0
13 : 12	DEVACTIVE06_EDGE	Reserved Default Value: 0x0
11 : 10	DEVACTIVE05_EDGE	Reserved Default Value: 0x0
9 : 8	DEVACTIVE04_EDGE	Reserved Default Value: 0x0
7 : 6	DEVACTIVE03_EDGE	Reserved Default Value: 0x0
5 : 4	DEVACTIVE02_EDGE	DEVACTIVE 2 edge sensitivity. Default Value: 0x0
3 : 2	DEVACTIVE01_EDGE	DEVACTIVE 1 edge sensitivity. Default Value: 0x0

1.1.54 CPUSS_PPU_IESR (continued)

1 : 0	DEVACTIVE00_EDGE	DEVACTIVE 0 edge sensitivity. Default Value: 0x0

1.1.55 CPUSS_PPU_OPSR

Operating Mode Active Edge Sensitivity Register

Address: 0x42105044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE19_EDGE [7:6]		DEVACTIVE18_EDGE [5:4]		DEVACTIVE17_EDGE [3:2]		DEVACTIVE16_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE23_EDGE [15:14]		DEVACTIVE22_EDGE [13:12]		DEVACTIVE21_EDGE [11:10]		DEVACTIVE20_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 14	DEVACTIVE23_EDGE	Reserved Default Value: 0x0
13 : 12	DEVACTIVE22_EDGE	Reserved Default Value: 0x0
11 : 10	DEVACTIVE21_EDGE	Reserved Default Value: 0x0
9 : 8	DEVACTIVE20_EDGE	Reserved Default Value: 0x0
7 : 6	DEVACTIVE19_EDGE	Reserved Default Value: 0x0
5 : 4	DEVACTIVE18_EDGE	Reserved Default Value: 0x0
3 : 2	DEVACTIVE17_EDGE	Reserved Default Value: 0x0
1 : 0	DEVACTIVE16_EDGE	Reserved Default Value: 0x0

1.1.56 CPUSS_PPU_FUNRR

Functional Retention RAM Configuration Register

Address: 0x42105050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FUNC_RET_RAM_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	FUNC_RET_RAM_CFG	Reserved Default Value: 0x0

1.1.57 CPUSS_PPU_FULRR

Full Retention RAM Configuration Register

Address: 0x42105054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FULL_RET_RAM_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	FULL_RET_RAM_CFG	Reserved Default Value: 0x0

1.1.58 CPUSS_PPU_MEMRR

Memory Retention RAM Configuration Register

Address: 0x42105058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MEM_RET_RAM_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	MEM_RET_RAM_CFG	Reserved Default Value: 0x0

1.1.59 CPUSS_PPU_EDTR0

Power Mode Entry Delay Register 0

Address: 0x42105160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	OFF_DEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MEM_RET_DEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	LOGIC_RET_DEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	FULL_RET_DEL [31:24]							

Bits	Name	Description
31 : 24	FULL_RET_DEL	Reserved Default Value: 0x00
23 : 16	LOGIC_RET_DEL	Reserved Default Value: 0x00
15 : 8	MEM_RET_DEL	Reserved Default Value: 0x00
7 : 0	OFF_DEL	Reserved Default Value: 0x00

1.1.60 CPUSS_PPU_EDTR1

Power Mode Entry Delay Register 1

Address: 0x42105164

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MEM_OFF_DEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	FUNC_RET_DEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	FUNC_RET_DEL	Reserved Default Value: 0x00
7 : 0	MEM_OFF_DEL	Reserved Default Value: 0x00

1.1.61 CPUSS_PPU_DCDR0

Device Control Delay Configuration Register 0

Address: 0x42105170

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CLKEN_RST_DLY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	ISO_CLKEN_DLY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	RST_HWSTAT_DLY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	RST_HWSTAT_DLY	Reserved Default Value: 0x0
15 : 8	ISO_CLKEN_DLY	Reserved Default Value: 0x0
7 : 0	CLKEN_RST_DLY	Reserved Default Value: 0x0

1.1.62 CPUSS_PPU_DCDR1

Device Control Delay Configuration Register 1

Address: 0x42105174

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ISO_RST_DLY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CLKEN_ISO_DLY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	CLKEN_ISO_DLY	Reserved Default Value: 0x0
7 : 0	ISO_RST_DLY	Reserved Default Value: 0x0

1.1.63 CPUSS_PPU_IDR0

PPU Identification Register 0

Address: 0x42105FB0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	NUM_OPMODE [7:4]				DEVCHAN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	STA_-FUNC_RET_SPT	STA_-FULL_RET_SPT	STA_MEM_OFF_SPT	STA_LG-C_RET_SPT	STA_MEM_RET_EMU_SPT	STA_MEM_RET_SPT	STA_OFF_EMU_SPT	STA_OFF_SPT

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	None	R	R	R
HW Access	RW	RW	RW	RW	None	RW	RW	RW
Name	DY-N_MEM_RET_EMU_SPT	DY-N_MEM_RET_SPT	DY-N_OFF_EMU_SPT	DY-N_OFF_SPT	None	STA_DB-G_RE-COV_SPT	STA_WRM_RST_SPT	STA_ON_SPT

Bits	31	30	29	28	27	26	25	24
SW Access	None		R	R	R	R	R	R
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [31:30]		DY-N_WRM_RST_SPT	DY-N_ON_SPT	DYN_-FUNC_RET_SPT	DYN_-FULL_RET_SPT	DY-N_MEM_OFF_SPT	DYN_LG-C_RET_SPT

Bits	Name	Description
29	DYN_WRM_RST_SPT	Dynamic WARM_RST support. Default Value: 0x0
28	DYN_ON_SPT	Dynamic ON support. Default Value: 0x1
27	DYN_FUNC_RET_SPT	Dynamic FUNC_RET support. Default Value: 0x0
26	DYN_FULL_RET_SPT	Dynamic FULL_RET support. Default Value: 0x1
25	DYN_MEM_OFF_SPT	Dynamic MEM_OFF support. Default Value: 0x0
24	DYN_LGC_RET_SPT	Dynamic LOGIC_RET support. Default Value: 0x0
23	DY-N_MEM_RET_EMU_SPT	Dynamic MEM_RET_EMU support Default Value: 0x0
22	DYN_MEM_RET_SPT	Dynamic MEM_RET support. Default Value: 0x0

1.1.63 CPUSS_PPU_IDR0 (continued)

21	DYN_OFF_EMU_SPT	Dynamic OFF_EMU support. Default Value: 0x0
20	DYN_OFF_SPT	Dynamic OFF support. Default Value: 0x1
18	STA_DBG_RECOV_SPT	DBG_RECOV support. Default Value: 0x0
17	STA_WRM_RST_SPT	WARM_RST support. Ignore this bit. Do not use WARM_RST. Default Value: 0x1
16	STA_ON_SPT	ON support. Default Value: 0x1
15	STA_FUNC_RET_SPT	FUNC_RET support. Default Value: 0x0
14	STA_FULL_RET_SPT	FULL_RET support. Default Value: 0x1
13	STA_MEM_OFF_SPT	MEM_OFF support. Default Value: 0x0
12	STA_LGC_RET_SPT	LOGIC_RET support. Default Value: 0x0
11	STA_MEM_RET_EMU_SPT	MEM_RET_EMU support. Default Value: 0x0
10	STA_MEM_RET_SPT	MEM_RET support. Default Value: 0x0
9	STA_OFF_EMU_SPT	OFF_EMU support. Default Value: 0x0
8	STA_OFF_SPT	OFF support. Default Value: 0x1
7 : 4	NUM_OPMODE	No. of operating modes supported is NUM_OPMODE + 1. Default Value: 0x0
3 : 0	DEVCHAN	No. of Device Interface Channels. 0: This is a P-Channel PPU. Refer to PPU_IDR1.OP_ACTIVE for the number of DEVPACTIVE inputs and their meaning. non-zero: The value is the number of Q-Channels. The device enumeration is: Device 0: SRSS PDCM, Device 1: CPUSS SEQ between SS level LPD500 EXP & PERI Q-Channel Default Value: 0x2

1.1.64 CPUSS_PPU_IDR1

PPU Identification Register 1

Address: 0x42105FB4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R	R	R	None	R	R	R
HW Access	None	RW	RW	RW	None	RW	RW	RW
Name	None	FUNC_RET_RAM_REG	FULL_RET_RAM_REG	MEM_RET_RAM_REG	None	LOCK_SPT	SW_DEV_DEL_SPT	PWR_MODE_ENTRY_DEL_SPT

Bits	15	14	13	12	11	10	9	8
SW Access	None			R	None	R	R	R
HW Access	None			RW	None	RW	RW	RW
Name	None [15:13]			OFF_MEM_RET_TRANS	None	OP_ACTIVE	STA_POLICY_OP_IRQ_SPT	STA_POLICY_PWR_IRQ_SPT

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	OFF_MEM_RET_TRANS	OFF to MEM_RET direct transition. Indicates if direct transitions from OFF to MEM_RET and from OFF_EMU to MEM_RET_EMU are supported. Default Value: 0x0
10	OP_ACTIVE	Operating mode use model for dynamic transitions. 0: Ladder use model. 1: Independent use model. When operating modes are not supported (PPU_IDR0.NUM_OPMODE==0), this field is reserved. Default Value: 0x0
9	STA_POLICY_OP_IRQ_SPT	Operating policy transition completion event status. Default Value: 0x0
8	STA_POLICY_PWR_IRQ_SPT	Power policy transition completion event status. Default Value: 0x0
6	FUNC_RET_RAM_REG	Indicates if the PPU_FUNRR register is present or reserved. 0: Reserved. 1: Present. Default Value: 0x0
5	FULL_RET_RAM_REG	Indicates if the PPU_FULRR register is present or reserved. 0: Reserved. 1: Present. Default Value: 0x0
4	MEM_RET_RAM_REG	Indicates if the PPU_MEMRR register is present or reserved. 0: Reserved. 1: Present. Default Value: 0x0

1.1.64 CPUSS_PPU_IDR1 (continued)

2	LOCK_SPT	Lock and the lock interrupt event are supported. Default Value: 0x0
1	SW_DEV_DEL_SPT	Software device delay control configuration support. Default Value: 0x0
0	PWR_MODE_EN- TRY_DEL_SPT	Power mode entry delay support. Default Value: 0x0

1.1.65 CPUSS_PPU_IIDR

Implementation Identification Register

Address: 0x42105FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	IMPLEMENTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R				R			
HW Access	RW				RW			
Name	REVISION [15:12]				IMPLEMENTER [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access	RW				RW			
Name	PRODUCT_ID [23:20]				VARIANT [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	PRODUCT_ID [31:24]							

Bits	Name	Description
31 : 20	PRODUCT_ID	PPU part identification. Default Value: 0x0B5
19 : 16	VARIANT	Major revision of the product. Default Value: 0
15 : 12	REVISION	Minor revision of the product. Default Value: 0
11 : 0	IMPLEMENTER	Implementer identification. [11:8] The JEP106 continuation code of the implementer. [7] Always 0. [6:0] The JEP106 identity code of the implementer. For an Arm implementation, bits [11:0] are 0x43B. Default Value: 0x43B

1.1.66 CPUSS_PPU_AIDR

Architecture Identification Register

Address: 0x42105FCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	ARCH_REV_MAJOR [7:4]				ARCH_REV_MINOR [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	ARCH_REV_MAJOR	0x1 - PPU architecture major revision 1. Other Values - Reserved. Default Value: 0x1
3 : 0	ARCH_REV_MINOR	0x1 - PPU Architecture minor revision 1. Other Values - Reserved. Default Value: 0x1

1.1.67 CPUSS_PPU_PID4

Implementation Defined Identification Register (PID4)

Address: 0x42105FD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				RW			
Name	None [7:4]				IMPLEMENTER_11_8 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	IMPLEMENTER_11_8	The JEP106 continuation code of the implementer, which is 0x4 hardcoded value. Default Value: 0x4

1.1.68 CPUSS_PPU_PID0

Implementation Defined Identification Register (PID0)

Address: 0x42105FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	PRODUCT_ID_7_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	PRODUCT_ID_7_0	PPU part identification bits [7:0]. Default Value: 0xB5

1.1.69 CPUSS_PPU_PID1

Implementation Defined Identification Register (PID1)

Address: 0x42105FE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	IMPLEMENTER_3_0 [7:4]				PRODUCT_ID_11_8 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	IMPLEMENTER_3_0	JEP106_ID bits [3:0] Default Value: 0xB
3 : 0	PRODUCT_ID_11_8	PPU part identification bits [11:8] Default Value: 0x0

1.1.70 CPUSS_PPU_PID2

Implementation Defined Identification Register (PID2)

Address: 0x42105FE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R	R		
HW Access	RW				RW	RW		
Name	REV_CONST [7:4]				CON-ST_HIGH	IMPLEMENTER_6_4 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	REV_CONST	Constant LOW Revision (4 bits) Default Value: 0x0
3	CONST_HIGH	Constant HIGH Default Value: 0x1
2 : 0	IMPLEMENTER_6_4	JEP106_ID bits [6:4] Default Value: 0x3

1.1.71 CPUSS_PPU_PID3

Implementation Defined Identification Register (PID3)

Address: 0x42105FEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	PID3_REVISION [7:4]				PID3_REV_CONST [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	PID3_REVISION	Minor revision of the product. Default Value: 0x0
3 : 0	PID3_REV_CONST	Constant LOW (4 bits) Default Value: 0x0

1.1.72 CPUSS_PPU_ID0

Implementation Defined Identification Register (ID0)

Address: 0x42105FF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ID0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	ID0	ID0 hard coded value Default Value: 0x0D

1.1.73 CPUSS_PPU_ID1

Implementation Defined Identification Register (ID1)

Address: 0x42105FF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ID1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	ID1	ID1 hardcoded value Default Value: 0xF0

1.1.74 CPUSS_PPU_ID2

Implementation Defined Identification Register (ID2)

Address: 0x42105FF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ID2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	ID2	ID2 hardcoded value Default Value: 0x05

1.1.75 CPUSS_PPU_ID3

Implementation Defined Identification Register (ID3)

Address: 0x42105FFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ID3 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	ID3	ID3 hardcoded value Default Value: 0xB1

1.1.76 MXCM33_CM33_CTL

Control

Address: 0x42160000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None			
HW Access	None			R	None			
Name	None [7:5]			CPU_WAIT	None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [15:13]			LOCKSAU	LOCKNSM-PU	LOCKSM-PU	LOCKSVTAIRCR	LOCKNS-VTOR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None		RW	RW	RW	RW	RW
HW Access	R	None		R	R	R	R	R
Name	IDC_MASK	None [30:29]		IXC_MASK	UFC_MASK	OFC_MASK	DZC_MASK	IOC_MASK

Bits	Name	Description
31	IDC_MASK	CPU FPU exception mask for the CPU's FPCSR.IDC "input denormalized" exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. Note: if the CPU FPCSR.FZ field is set to '1', denormalized inputs are "flushed to zero". Dependent on the FPU algorithm, this may or may not occur frequently. To prevent frequent CPU FPU interrupts as a result of denormalized inputs, this field may be set to '0'. Default Value: 0
28	IXC_MASK	CPU FPU exception mask for the CPU's FPCSR.IXC "inexact" exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. Note: the "inexact" condition is set as a result of rounding. Rounding may occur frequently and is typically not an error condition. To prevent frequent CPU FPU interrupts as a result of rounding, this field is typically set to '0'. Default Value: 0
27	UFC_MASK	CPU FPU exception mask for the CPU's FPCSR.UFC "underflow" exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. Default Value: 0
26	OFC_MASK	CPU FPU exception mask for the CPU's FPCSR.OFC "overflow" exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. Default Value: 0

1.1.76 MXCM33_CM33_CTL (continued)

25	DZC_MASK	CPU FPU exception mask for the CPU's FPCSR.DZC "divide by zero" exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. Default Value: 0
24	IOC_MASK	CPU floating point unit (FPU) exception mask for the CPU's FPCSR.IOC "invalid operation" exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. Note: the ARM architecture does NOT support FPU exceptions; i.e. there is no precise FPU exception handler. Instead, FPU conditions are captured in the CPU's FPCSR register and the conditions are provided as CPU interface signals. The interface signals are "masked" with the fields provided by this register (CM33_CTL). The "masked" signals are reduced/OR-ed into a single CPU floating point interrupt signal. The associated CPU interrupt handler allows for imprecise handling of FPU exception conditions. Note: the CPU's FPCSR exception conditions are "sticky". Typically, the CPU FPU interrupt handler will clear the exception condition(s) to '0'. Note: by default, the FPU exception masks are '0'. Therefore, FPU exception conditions will NOT activate the CPU's floating point interrupt. Default Value: 0
12	LOCKSAU	Asserting this bit prevents changes to Secure SAU memory regions already programmed. All writes to the registers are ignored. '1': Disables writes to the SAU_CTRL, SAU_RNR, SAU_RBAR and SAU_RLAR registers from software or from a debug agent connected to the processor. '0': Unlocks these registers. This signal has no affect if the Cortex-M33 processor has not been configured with support for the Armv8-M Security Extension, or if no SAU regions have been configured. Default Value: 0
11	LOCKNSMPU	Asserting this bit prevents changes to Nonsecure MPU memory regions already programmed. All writes to the registers are ignored. '1': Disables writes to the MPU_CTRL_NS, MPU_RNR_NS, MPU_RBAR_NS, MPU_RLAR_NS, MPU_RBAR_A_NSn and MPU_RLAR_A_NSn from software or from a debug agent connected to the processor. '0': Unlocks these registers. This signal has no affect if the Cortex-M33 processor has been configured without any Nonsecure MPU regions. Default Value: 0
10	LOCKSMPU	Asserting this bit prevents changes to programmed Secure MPU memory regions and all writes to the registers are ignored. '1': Disables writes to the MPU_CTRL, MPU_RNR, MPU_RBAR, MPU_RLAR, MPU_RBAR_An and MPU_RLAR_An from software or from a debug agent connected to the processor in Secure state. '0': Unlocks these registers. This bit has no affect if the Cortex-M33 processor has not been configured with support for the Armv8-M Security Extension, or if no Secure MPU regions have been configured. Default Value: 0
9	LOCKSVTAIRCR	Asserting this bit prevents changes to: - The Secure vector table base address. - Handling of Secure interrupt priority. - BusFault, HardFault, and NMI security target settings in the processor. '1': Disables writes to the VTOR_S,AIRCR.PRIS, and AIRCR.BFHFNMINS registers. '0': Unlocks these registers. Default Value: 0
8	LOCKNSVTOR	Asserting this bit prevents changes to the Non-secure vector table base address. '1': Disables writes to the VTOR_NS register. '0': Unlocks this register. Default Value: 0
4	CPU_WAIT	When this signal is '1' out of reset, it forces the CPU into a quiescent state that delays its boot-up sequence and instruction execution until this signal is driven '0'. Default Value: 0

1.1.77 MXCM33_CM33_CMD

Command

Address: 0x42160004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	None
HW Access	None						RW1S	None
Name	None [7:2]						ENABLED	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VECTKEYSTAT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VECTKEYSTAT [31:24]							

Bits	Name	Description
31 : 16	VECTKEYSTAT	Register key (to prevent accidental writes). - Should be written with a 0x05fa key value for the write to take effect. - Always reads as 0xfa05. Default Value: 0xFA05
1	ENABLED	Processor enable: '0': Disabled. Processor clock is turned off and reset is activated. After SW clears this field to '0', HW automatically sets this field to '1'. This effectively results in a CM33 reset, followed by a CM33 warm boot. '1': Enabled. Note: The intent is that this bit is modified only through an external probe or by the other CM33 while this CM33 is in Sleep or DeepSleep power mode. If this field is cleared to '0' by this CM33 itself, it should be done under controlled conditions (such that undesirable side effects can be prevented). Note: The CM33 CPU has a AIRCR.SYSRESETREQ register field that allows the CM33 to reset the complete device (ENABLED only disables/enables the CM33), resulting in a warm boot. This CPU register field has similar "built-in protection" as this register to prevent accidental system writes (the upper 16-bits of the register need to be written with a 0x05fa key value; see CPU user manual for more details). Default Value: 1

1.1.78 MXCM33_CM33_STATUS

Status

Address: 0x42160008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						SLEEP-DEEP	SLEEPING

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	SLEEPDEEP	Specifies if the CPU is in Sleep or DeepSleep power mode. See SLEEPING field. Default Value: 0
0	SLEEPING	Specifies if the CPU is in Active, Sleep or DeepSleep power mode: - Active power mode: SLEEPING is '0'. - Sleep power mode: SLEEPING is '1' and SLEEPDEEP is '0'. - DeepSleep power mode: SLEEPING is '1' and SLEEPDEEP is '1'. Default Value: 0

1.1.79 MXCM33_CM33_NMI_CTL0

CM33 NMI control

Address: 0x42160080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SYSTEM_INT_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SYSTEM_INT_IDX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	SYSTEM_INT_IDX	System interrupt select for CPU NMI. The reset value ("1023") ensures that the CPU NMI is NOT connected to any system interrupt after DeepSleep reset. Default Value: 1023

1.1.80 MXCM33_CM33_EVENT_CTL

CM33 event control

Address: 0x421600C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			MASK [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	MASK	One mask bit for each CPU (other than itself). 0: Mask is not set. 1: RX event from the corresponding CPU is masked. Bit 0: Other CM33 CPU event Bit 1: CM55_0 CPU event Bit 2: CM55_1 CPU event Bit 3: CM55_2 CPU event Bit 4: CM55_3 CPU event Default Value: 0

1.1.81 MXCM33_CM33_S_VECTOR_TABLE_BASE

CM33 secure vector table base

Address: 0x42161000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	None						
HW Access	R	None						
Name	ADDR25	None [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR25 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR25 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR25 [31:24]							

Bits	Name	Description
31 : 7	ADDR25	Address of CM33 secure vector table to be used at reset. Default value: ADDR25: 0x0200000 if PROM is present (points to Secure ROM start address i.e. 0x1000_0000). ADDR25: 0x0680000 if PROM is not present (points to Secure RAMC0 start address i.e. 0x3400_0000). Default Value: 2162688

1.1.82 MXCM33_CM33_NS_VECTOR_TABLE_BASE

CM33 non-secure vector table base

Address: 0x42161004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	None						
HW Access	R	None						
Name	ADDR25	None [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR25 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR25 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR25 [31:24]							

Bits	Name	Description
31 : 7	ADDR25	Address of CM33 non-secure vector table to be used at reset. Default value: ADDR25: 0x0000000 if PROM is present (points to Non-Secure ROM start address i.e. 0x0000_0000). ADDR25: 0x0480000 if PROM is not present (points to Non-Secure RAMC0 start address i.e. 0x2400_0000). Default Value: 65536

1.1.83 MXCM33_CM33_PC_CTL

CM33 protection context control

Address: 0x42162000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				VALID [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	VALID	Valid fields for the protection context handler CM33_PCi_HANDLER registers: Bit 0: Valid field for CM33_PC0_HANDLER. Bit 1: Valid field for CM33_PC1_HANDLER. Bit 2: Valid field for CM33_PC2_HANDLER. Bit 3: Valid field for CM33_PC3_HANDLER. Default Value: 0

1.1.84 MXCM33_CM33_PC0_HANDLER

CM33 protection context 0 handler

Address: 0x42162040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Address of the protection context 0 handler. This field is used to detect entry to Cypress "trusted" code through an exception/interrupt. Default Value: 0

1.1.85 MXCM33_CM33_PC1_HANDLER

CM33 protection context 1 handler

Address: 0x42162100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Address of the protection context 1 handler. Default Value: 0

1.1.86 MXCM33_CM33_PC2_HANDLER

CM33 protection context 2 handler

Address: 0x42162140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR [31:24]							

Bits	Name	Description
31	ENABLED	- 0: AREF disabled - 1: AREF enabled Default Value: 0
21 : 20	VREF_SEL	bandgap voltage select control Default Value: 0 **0x0: RESERVED :** Reserved, for normal operation, set to '1' selection (LOCAL) **0x1: LOCAL :** Use locally generated Vref
16	IZTAT_SEL	iztat current select control Default Value: 0 **0x0: RESERVED :** Reserved, for normal operation, set to '1' selection (LOCAL) **0x1: LOCAL :** Use locally generated 250nA

1.1.86 MXCM33_CM33_PC2_HANDLER (continued)

15 : 8	CTB_IPTAT_REDIRECT	RESERVED - all bits must be set to 0 Default Value: 0
7	CTB_IPTAT_SCALE	RESERVED - set this bit to 0 Default Value: 0
6 : 4	AREF_RMB	RESERVED - all bits must be set to 0 Default Value: 0
3 : 2	AREF_BIAS_SCALE	RESERVED - This field must be set to b01 Default Value: 0
0	AREF_MODE	RESERVED - This bit must be set to 0 Default Value: 0

1.1.87 MXCM33_CM33_PC3_HANDLER

CM33 protection context 3 handler

Address: 0x42162180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Address of the protection context 3 handler. Default Value: 0

1.1.88 CPUSS_IDENTITY

Identity

Address: 0x421C0000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None		R	R
HW Access	W				None		W	W
Name	PC [7:4]				None [3:2]		NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	None		R					
HW Access	None		W					
Name	None [15:14]		MS [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13 : 8	MS	This field specifies the bus master identifier of the transfer that reads the register. Default Value: Undefined
7 : 4	PC	This field specifies the protection context of the transfer that reads the register. Default Value: Undefined
1	NS	This field specifies the security setting ('0': secure mode; '1': non-secure mode) of the transfer that reads the register. Default Value: Undefined
0	P	This field specifies the privileged setting ('0': user mode; '1': privileged mode) of the transfer that reads the register. Default Value: Undefined

1.1.89 CPUSS_PRODUCT_ID

Product identifier and version (same as CoreSight RomTables)

Address: 0x421C0010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	FAMILY_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				FAMILY_ID [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access	W				W			
Name	MINOR_REV [23:20]				MAJOR_REV [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 20	MINOR_REV	Minor Revision, starts with 1, increments with metal layer only tape-out (implemented with metal ECO-able tie-off) Default Value: Undefined
19 : 16	MAJOR_REV	Major Revision, starts with 1, increments with all layer tape-out (implemented with metal ECO-able tie-off) Default Value: Undefined
11 : 0	FAMILY_ID	Family ID. Common ID (Partnumber a.k.a. Silicon ID) for a product family. Default Value: 280

1.1.90 CPUSS_DP_STATUS

Debug port status

Address: 0x421C0020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				SWJ_SWD_SEL	SWJ_JTAG_SEL	SWJ_DEBUG_EN	SWJ_CONNECTED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	SWJ_SWD_SEL	Specifies if the SWD interface is selected. '0': SWD not selected. '1': SWD selected. Default Value: 0
2	SWJ_JTAG_SEL	Specifies if the JTAG interface is selected. '0': JTAG not selected. '1': JTAG selected. Default Value: 0
1	SWJ_DEBUG_EN	Specifies if SWJ debug is enabled, i.e. CDBGPWRUPACK is '1' and thus debug clocks are on: '0': Disabled. '1': Enabled. Default Value: 0
0	SWJ_CONNECTED	Specifies if the SWJ debug port is connected; i.e. debug host interface is active: '0': Not connected/not active. '1': Connected/active. Default Value: 0

1.1.91 CPUSS_BUFF_CTL

Buffer control

Address: 0x421C0030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							WRITE_BUFF

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	WRITE_BUFF	Specifies if write transfer can be buffered in the bus infrastructure bridges: '0': Write transfers are not buffered, independent of the transfer's bufferable attribute. '1': Write transfers can be buffered, if the transfer's bufferable attribute indicates that the transfer is a bufferable/posted write. This bit controls buffering only for subsystems that interfaced using the AHB2AHB bridge, not for components utilised from the ARM SIE200, such as the 32-bit SYS interconnect in SYSCPUSS, Peripheral Group0, MSC etc. Default Value: 1

1.1.92 CPUSS_CAL_SUP_SET

Calibration support set and read

Address: 0x421C0040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Read without side effect, write 1 to set Default Value: 0

1.1.93 CPUSS_CAL_SUP_CLR

Calibration support clear and reset

Address: 0x421C0044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	A							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	A							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	A							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Read side effect: when read all bits are cleared, write 1 to clear a specific bit Note: no exception for the debug host, it also causes the read side effect Default Value: 0

1.1.94 CPUSS_INFRA_CTL

Infrastructure Control

Address: 0x421C0050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							CLOCK_-FORCE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CLOCK_FORCE	Force Infrastructure clock gating to be always ON. 0: Disabled 1: Enabled Default Value: 0

1.1.95 CPUSS_SYSTICK_S_CTL

Secure SysTick timer control

Address: 0x421C0100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TENMS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TENMS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	TENMS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None				RW	
HW Access	R	R	None				R	
Name	NOREF	SKEW	None [29:26]				CLOCK_SOURCE [25:24]	

Bits	Name	Description
31	NOREF	Specifies if an external clock source is provided: '0': An external clock source is provided. '1': An external clock source is NOT provided and only the CPU internal clock can be used as SysTick timer clock source. Default Value: 0
30	SKEW	Specifies the precision of the clock source and if the TENMS field represents exactly 10 ms (clock source frequency is a multiple of 100 Hz). This affects the suitability of the SysTick timer as a SW real-time clock: '0': Precise. '1': Imprecise. Default Value: 1
25 : 24	CLOCK_SOURCE	Specifies an external clock source: "0": The low frequency clock "clk_lf" is selected. The precision of this clock depends on whether the low frequency clock source is a SRSS internal RC oscillator (imprecise) or a device external crystal oscillator (precise). "1": The internal main oscillator (IMO) clock "clk_imo" is selected. o "2": The external crystal oscillator (ECO) clock "clk_eco" is selected. "3": The SRSS "clk_timer" is selected ("clk_timer" is a divided/gated version of "clk_hf" or "clk_imo"). Note: If NOREF is '1', the CLOCK_SOURCE value is NOT used. Note: It is SW's responsibility to provide the correct NOREF, SKEW and TENMS field values for the selected clock source. Default Value: 0
23 : 0	TENMS	Specifies the number of clock source cycles (minus 1) that make up 10 ms. E.g., for a 32,768 Hz reference clock, TENMS is 328 - 1 = 327. Default Value: 327

1.1.96 CPUSS_SYSTICK_NS_CTL

Non Secure SysTick timer control

Address: 0x421C0120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TENMS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TENMS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	TENMS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None				RW	
HW Access	R	R	None				R	
Name	NOREF	SKEW	None [29:26]				CLOCK_SOURCE [25:24]	

Bits	Name	Description
31	NOREF	Specifies if an external clock source is provided: '0': An external clock source is provided. '1': An external clock source is NOT provided and only the CPU internal clock can be used as SysTick timer clock source. Default Value: 0
30	SKEW	Specifies the precision of the clock source and if the TENMS field represents exactly 10 ms (clock source frequency is a multiple of 100 Hz). This affects the suitability of the SysTick timer as a SW real-time clock: '0': Precise. '1': Imprecise. Default Value: 1
25 : 24	CLOCK_SOURCE	Specifies an external clock source: "0": The low frequency clock "clk_lf" is selected. The precision of this clock depends on whether the low frequency clock source is a SRSS internal RC oscillator (imprecise) or a device external crystal oscillator (precise). "1": The internal main oscillator (IMO) clock "clk_imo" is selected. o "2": The external crystal oscillator (ECO) clock "clk_eco" is selected. "3": The SRSS "clk_timer" is selected ("clk_timer" is a divided/gated version of "clk_hf" or "clk_imo"). Note: If NOREF is '1', the CLOCK_SOURCE value is NOT used. Note: It is SW's responsibility to provide the correct NOREF, SKEW and TENMS field values for the selected clock source. Default Value: 0
23 : 0	TENMS	Specifies the number of clock source cycles (minus 1) that make up 10 ms. E.g., for a 32,768 Hz reference clock, TENMS is 328 - 1 = 327. Default Value: 327

1.1.97 CPUSS_INTR_MSC

Master security controller Interrupt

Address: 0x421C0200

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	None	RW1C	None
HW Access	None				A	None	A	None
Name	None [7:4]				EXP_MS_MSC	None	SYS_MS0_MSC	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EXP_MS_MSC	This interrupt cause field is activated (HW sets the field to '1') when there is a security violation on SYSCPUSS external EXP AHB5 bus master interfaces. SW writes a '1' to this field to clear the interrupt cause to '0'. The HW captures a new MSC interrupt only after clearing the interrupt cause. Default Value: 0
1	SYS_MS0_MSC	This interrupt cause field is activated (HW sets the field to '1') when there is a security violation on SYSCPUSS external SYS AHB5 bus master interface 0. SW writes a '1' to this field to clear the interrupt cause to '0'. The HW captures a new MSC interrupt only after clearing the interrupt cause. Default Value: 0

1.1.98 CPUSS_INTR_MASK_MSC

Master security controller Interrupt mask

Address: 0x421C0208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	None	RW	None
HW Access	None				R	None	R	None
Name	None [7:4]				EXP_MS_MSC	None	SYS_MS0_MSC	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EXP_MS_MSC	Mask bit for the corresponding field in the SYSCPUSS_INTR_MSC register. Default Value: 0
1	SYS_MS0_MSC	Mask bit for the corresponding field in the SYSCPUSS_INTR_MSC register. Default Value: 0

1.1.99 CPUSS_INTR_MASKED_MSC

Master security controller Interrupt masked

Address: 0x421C020C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	None	R	None
HW Access	None				W	None	W	None
Name	None [7:4]				EX-P_MS_MSC	None	SYS-_MS0_MSC	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EXP_MS_MSC	Logical AND of corresponding SYSCPUSS_INTR_MSC and SYSCPUSS_INTR_MASK_MSC bit fields. Default Value: 0
1	SYS_MS0_MSC	Logical AND of corresponding SYSCPUSS_INTR_MSC and SYSCPUSS_INTR_MASK_MSC bit fields. Default Value: 0

1.1.100 CPUSS_AP_CTL

Access port control

Address: 0x421C1000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None	RW	RW	RW
HW Access	R	R	R	R	None	R	R	R
Name	CM33_0_SPNID_ENABLE	CM33_0_SPID_ENABLE	CM33_0_NID_ENABLE	CM33_0_DBG_ENABLE	None	SYS_ENABLE	CM33_1_ENABLE	CM33_0_ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW	None	RW	None		RW	RW
HW Access	None	R	None	R	None		R	R
Name	None	SYS_SECURE_ENABLE	None	CM33_0_SECURE_ENABLE	None [11:10]		CM33_1_NID_ENABLE	CM33_1_DBG_ENABLE

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S	RW1S	RW1S	RW1S	None	RW1S	RW1S	RW1S
HW Access	R	R	R	R	None	R	R	R
Name	CM33_0_SPNID_DISABLE	CM33_0_SPID_DISABLE	CM33_0_NID_DISABLE	CM33_0_DBG_DISABLE	None	SYS_DISABLE	CM33_1_DISABLE	CM33_0_DISABLE

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW1S	None	RW1S	None		RW1S	RW1S
HW Access	None	R	None	R	None		R	R
Name	None	SYS_SECURE_DISABLE	None	CM33_0_SECURE_DISABLE	None [27:26]		CM33_1_NID_DISABLE	CM33_1_DBG_DISABLE

Bits	Name	Description
30	SYS_SECURE_DISABLE	Disables the system secure AP interface: '0': Enabled. '1': Disabled. Typically, this field is set by the Infineon boot code with information from OTP memory. The access port is only enabled when SYS_SECURE_DISABLE is '0' and SYS_SECURE_ENABLE is '1'. Default Value: 0
28	CM33_0_SECURE_DISABLE	Disables the CM33_0 secure AP interface: '0': Enabled. '1': Disabled. Typically, this field is set by the Infineon boot code with information from OTP memory. The access port is only enabled when CM33_0_DISABLE is '0' and CM33_0_ENABLE is '1'. Default Value: 0

1.1.100 CPUSS_AP_CTL (continued)

25	CM33_1_NID_DISABLE	Disable Non-invasive debug for CM33_1. '1': Disables all trace and non-invasive debug features. '0': Enables all trace and non-invasive debug features. Typically, this field is set by the Infineon boot code with information from OTP memory. The non-invasive debug is only enabled when CM33_1_NID_DISABLE is '0' and CM33_1_NID_ENABLE is '1'. Default Value: 0
24	CM33_1_DBG_DISABLE	Disable Invasive debug for CM33_1. '1': Disables all halt-mode and invasive debug features. '0': Enables invasive debug features. Typically, this field is set by the Infineon boot code with information from OTP memory. The invasive debug is only enabled when CM33_1_DBG_DISABLE is '0' and CM33_1_DBG_ENABLE is '1'. Default Value: 0
23	CM33_0_SPNID_DISABLE	Secure non-invasive debug disable for CM33_0. '1': Disables non-invasive debug features when the processor is in Secure state. '0': Enables non-invasive debug features when the processor is in Secure state. Typically, this field is set by the Infineon boot code with information from OTP memory. The non-invasive debug in secure state is only enabled when CM33_0_SPNID_DISABLE is '0' and CM33_0_SPNID_ENABLE is '1'. Default Value: 0
22	CM33_0_SPID_DISABLE	Secure invasive debug disable for CM33_0. '1': disables all halt mode and invasive debug features when the processor is in Secure state. '0': Enables all halt mode and invasive debug features when the processor is in Secure state. Typically, this field is set by the Infineon boot code with information from OTP memory. The invasive debug in secure state is only enabled when CM33_0_SPID_DISABLE is '0' and CM33_0_SPID_ENABLE is '1'. Default Value: 0
21	CM33_0_NID_DISABLE	Disable Non-invasive debug for CM33_0. '1': Disables all trace and non-invasive debug features. '0': Enables all trace and non-invasive debug features. Typically, this field is set by the Infineon boot code with information from OTP memory. The non-invasive debug is only enabled when CM33_0_NID_DISABLE is '0' and CM33_0_NID_ENABLE is '1'. Default Value: 0
20	CM33_0_DBG_DISABLE	Disable Invasive debug for CM33_0. '1': Disables all halt-mode and invasive debug features. '0': Enables invasive debug features. Typically, this field is set by the Infineon boot code with information from OTP memory. The invasive debug is only enabled when CM33_0_DBG_DISABLE is '0' and CM33_0_DBG_ENABLE is '1'. Default Value: 0
18	SYS_DISABLE	Disables the system AP interface: '0': Enabled. '1': Disabled. Typically, this field is set by the Infineon boot code with information from OTP memory. The access port is only enabled when SYS_DISABLE is '0' and SYS_ENABLE is '1'. Default Value: 0
17	CM33_1_DISABLE	Disables the CM33_1 AP interface: '0': Enabled. '1': Disabled. Typically, this field is set by the Infineon boot code with information from OTP memory. The access port is only enabled when CM33_1_DISABLE is '0' and CM33_1_ENABLE is '1'. Default Value: 0
16	CM33_0_DISABLE	Disables the CM33_0 AP interface: '0': Enabled. '1': Disabled. Typically, this field is set by the Infineon boot code with information from OTP memory. The access port is only enabled when CM33_0_DISABLE is '0' and CM33_0_ENABLE is '1'. Default Value: 0

1.1.100 CPUSS_AP_CTL (continued)

14	SYS_SECURE_ENABLE	Enables the system secure AP interface: '0': Disabled. '1': Enabled. Default Value: 0
12	CM33_0_SECURE_ENABLE	Enables the CM33_0 secure AP interface: '0': Disabled. '1': Enabled. Default Value: 0
9	CM33_1_NID_ENABLE	Non-invasive debug enable for CM33_1. '0': Disables all trace and non-invasive debug features. '1': Enables all trace and non-invasive debug features. Default Value: 0
8	CM33_1_DBG_ENABLE	Invasive debug enable for CM33_1. '0': Disables all halt-mode and invasive debug features. '1': Enables invasive debug features. Default Value: 0
7	CM33_0_SPNID_ENABLE	Secure non-invasive debug enable for CM33_0. '0': Disables non-invasive debug features when the processor is in Secure state. '1': Enables non-invasive debug features when the processor is in Secure state. Default Value: 0
6	CM33_0_SPID_ENABLE	Secure invasive debug enable for CM33_0. '0': disables all halt mode and invasive debug features when the processor is in Secure state. '1': Enables all halt mode and invasive debug features when the processor is in Secure state. Default Value: 0
5	CM33_0_NID_ENABLE	Non-invasive debug enable for CM33_0. '0': Disables all trace and non-invasive debug features. '1': Enables all trace and non-invasive debug features. Default Value: 0
4	CM33_0_DBG_ENABLE	Invasive debug enable for CM33_0. '0': Disables all halt-mode and invasive debug features. '1': Enables invasive debug features. Default Value: 1
2	SYS_ENABLE	Enables the system AP interface: '0': Disabled. '1': Enabled. Default Value: 0
1	CM33_1_ENABLE	Enables the CM33_1 AP interface: '0': Disabled. '1': Enabled. Default Value: 0
0	CM33_0_ENABLE	Enables the CM33_0 AP interface: '0': Disabled. '1': Enabled. Default Value: 0

1.1.101 CPUSS_PROTECTION

Protection status

Address: 0x421C2004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	STATE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	STATE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	STATE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	STATE [31:24]							

Bits	Name	Description
31 : 0	STATE	Protection state: PROTECTION is "0x5B719A4F": UNKNOWN state. PROTECTION is "0x5D48F714": VIRGIN state. PROTECTION is "0xC39D5455": OPEN state PROTECTION is "0x652372F7": NORMAL state. PROTECTION is "0x8DF117A1": SECURE state. PROTECTION is "0xFBF6D1B6": RMA state PROTECTION is "0x2E94B3DD": DEAD state. PROTECTION is "0x3A5BC6F1": CORRUPTED state. PROTECTION is "0x3F80442F": TESTMODE state. The following state transitions are allowed (and enforced by HW): - UNKNOWN => VIRGIN/RMA/OPEN/NORMAL/SECURE/DEAD/CORRUPTED - RMA/OPEN/NORMAL/SECURE => DEAD - RMA/OPEN/NORMAL/SECURE => TESTMODE - RMA/OPEN/NORMAL/SECURE => CORRUPTED An attempt to make a NOT allowed state transition will NOT affect this register field. Default Value: 0x5B719A4F **0x5b719a4f: UNKNOWN** **0x5d48f714: VIRGIN** **0xc39d5455: OPEN** **0x652372f7: NORMAL**

1.1.101 CPUSS_PROTECTION (continued)

0x8df117a1: SECURE

0xfbf6d1b6: RMA

0x2e94b3dd: DEAD

0x3a5bc6f1: CORRUPTED

0x3f80442f: TESTMODE

1.1.102 MS0_CTL

Master 'x' protection context control

Address: 0x421C4000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	PC_MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	PC_MASK	Protection context mask for protection contexts "15" down to "0". Bit PC_MASK[i] indicates if the MS_PC_STRUCT[x].PC[3:0] protection context field can be set to the value "i": - PC_MASK[i] is '0': MS_PC_STRUCT[x].PC[3:0] can NOT be set to "i"; and PC[3:0] is not changed. - PC_MASK[i] is '1': MS_PC_STRUCT[x].PC[3:0] can be set to "i". Note: When CM33_0 CM33_PC_CTL.VALID[i] is '1' (the associated protection context handler is valid), write transfers to PC_MASK[i] always write '0', regardless of data written. This ensures that when valid protection context handlers are used to enter protection contexts 0, 1, 2 or 3 through HW (HW modifies MS_PC_STRUCT[x].PC[3:0] on entry of the handler), it is NOT possible for SW to enter those protection contexts. Default Value: 0

1.1.103 MS31_CTL

Master 'x' protection context control

Address: 0x421C41F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							P

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	PC_MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	PC_MASK	Protection context mask for protection contexts "15" down to "0". Bit PC_MASK[i] indicates if the MS_PC_STRUCT[x].PC[3:0] protection context field can be set to the value "i": - PC_MASK[i] is '0': MS_PC_STRUCT[x].PC[3:0] can NOT be set to "i"; and PC[3:0] is not changed. - PC_MASK[i] is '1': MS_PC_STRUCT[x].PC[3:0] can be set to "i". Note: When CM33_0 CM33_PC_CTL.VALID[i] is '1' (the associated protection context handler is valid), write transfers to PC_MASK[i] always write '0', regardless of data written. This ensures that when valid protection context handlers are used to enter protection contexts 0, 1, 2 or 3 through HW (HW modifies MS_PC_STRUCT[x].PC[3:0] on entry of the handler), it is NOT possible for SW to enter those protection contexts. Default Value: 0
0	P	Privileged setting ('0': user mode; '1': privileged mode). Notes: This field is ONLY used for masters that do NOT provide their own user/privileged access control attribute. The default/reset field value provides privileged mode access capabilities. Default Value: 1

1.1.104 MS_PC0_PC

Master 'x' protection context value

Address: 0x421C5000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				RW			
Name	None [7:4]				PC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				RW			
Name	None [23:20]				PC_SAVED [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	PC_SAVED	Saved protection context. Modifications to this field are constrained by the associated MS_CTL_STRUCT[x].CTL.PC_MASK. Note: this field is ONLY used by the CM33_0. Default Value: 0

3 : 0	PC	Active protection context (PC). Modifications to this field are constrained by the associated MS_CTL_STRUCT[x].CTL.PC_MASK value. PC[3:0] can be set to "i" only if the corresponding mask bit (PC_MASK[i]) is '1'.
		The CM33_0 PC register is special: the PC field is modifiable by BOTH HW and SW (for all other masters, the PC field is modifiable by SW ONLY. For CM33_0 PC field HW modifications, the following holds:
		* On entry of a CM33_PC0/1/2/3_HANDLER exception/interrupt handler:
		IF (the new PC is the same as MS_PC_STRUCT[0].PC)
		PC is not affected; PC_SAVED is not affected.
		ELSE IF (CM33_PC_CTL.VALID[MS_PC_STRUCT[0].PC])
		An AHB5 bus error is generated for the exception handler fetch;
		PC is not affected; PC_SAVED is not affected.
		ELSE
		PC = "new PC"; PC_SAVED = PC (push operation).
		* On entry of any other exception/interrupt handler:
		PC = PC_SAVED; PC_SAVED is not affected (pop operation).
		
		Note: this field is NOT used by the DW controllers, DMA controllers as they inherit the protection context from master that configures the corresponding channel.
		Default Value: 0

1.1.105 MS_PC0_PC_READ_MIR

Master 'x' protection context value read mirror register

Address: 0x421C5004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				PC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				PC_SAVED [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	PC_SAVED	Read-only mirror of PC.PC_SAVED Default Value: 0
3 : 0	PC	Read-only mirror of PC.PC Default Value: 0

1.1.106 MS_PC31_PC

Master 'x' protection context value

Address: 0x421C51F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				RW			
Name	None [7:4]				PC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description

3 : 0	PC	Active protection context (PC). Modifications to this field are constrained by the associated MS_CTL_STRUCT[x].CTL.PC_MASK value. PC[3:0] can be set to "i" only if the corresponding mask bit (PC_MASK[i]) is '1'.
		The CM33_0 PC register is special: the PC field is modifiable by BOTH HW and SW (for all other masters, the PC field is modifiable by SW ONLY. For CM33_0 PC field HW modifications, the following holds:
		* On entry of a CM33_PC0/1/2/3_HANDLER exception/interrupt handler:
		IF (the new PC is the same as MS_PC_STRUCT[0].PC)
		PC is not affected; PC_SAVED is not affected.
		ELSE IF (CM33_PC_CTL.VALID[MS_PC_STRUCT[0].PC])
		An AHB5 bus error is generated for the exception handler fetch;
		PC is not affected; PC_SAVED is not affected.
		ELSE
		PC = "new PC"; PC_SAVED = PC (push operation).
		* On entry of any other exception/interrupt handler:
		PC = PC_SAVED; PC_SAVED is not affected (pop operation).
		
		Note: this field is NOT used by the DW controllers, DMA controllers as they inherit the protection context from master that configures the corresponding channel.
		Default Value: 0

1.1.107 MS_PC31_PC_READ_MIR

Master 'x' protection context value read mirror register

Address: 0x421C51F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				PC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	PC	Read-only mirror of PC.PC Default Value: 0

1.1.108 SYS_MS0_MSC_ACG_CTL

SYS_MS0 master security Controller & ACG configuration

Address: 0x421C6010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						SEC_RESP	CFG_GATE_RESP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	SEC_RESP	Reseponse type when transfers are not allowed by MSC. 0: Read as zero, write ignore. 1: Error response. Default Value: 1
0	CFG_GATE_RESP	Response type when the ACG is blocking the incoming transfers: 0: Waited transfer 1: Error response Default Value: 0

1.1.109 EXP_MS_MSC_ACG_CTL

EXP_MS master security Controller & ACG configuration

Address: 0x421C6020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						SEC_RESP	CFG_GATE_RESP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	SEC_RESP	Reseponse type when transfers are not allowed by MSC. 0: Read as zero, write ignore. 1: Error response. Default Value: 1
0	CFG_GATE_RESP	Response type when the ACG is blocking the incoming transfers: 0: Waited transfer 1: Error response Default Value: 0

1.1.110 CPUSS_SL_CTL_SL_CTL

Slave control (Clock enables)

Address: 0x421C8000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	None		RW	RW	None	RW
HW Access	R	R	None		R	R	None	R
Name	DW1_ENABLED	DW0_ENABLED	None [5:4]		RAMC0_ENABLED	FLASHC_ENABLED	None	PROMC_ENABLED

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	None	
HW Access	None				R	R	None	
Name	None [15:12]				FAULT_ENABLED	IPC_ENABLED	None [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	FAULT_ENABLED	Default Value: 1
10	IPC_ENABLED	Default Value: 1
7	DW1_ENABLED	Default Value: 1
6	DW0_ENABLED	Default Value: 1
3	RAMC0_ENABLED	Default Value: 1
2	FLASHC_ENABLED	Default Value: 1
0	PROMC_ENABLED	Slave enable controls. Each bit indicates whether the respective slave is enabled or not. 0: Disabled 1: Enabled If the slave is disabled, its clock is gated off (constant "0"). Any access (MMIO AHB access or ROM/System SRAM memory access) to slave when disabled result in AHB error response. Default Value: 1

1.1.111 CPUSS_SL_CTL_SL_CTL2

Slave control2 (Reset enables)

Address: 0x421C8004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	None		RW	RW	None	RW
HW Access	R	R	None		R	R	None	R
Name	DW1_RST	DW0_RST	None [5:4]		RAMC0_RST	FLASH-C_RST	None	PROMC_RST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	None	
HW Access	None				R	R	None	
Name	None [15:12]				FAULT_RST	IPC_RST	None [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	FAULT_RST	Default Value: 0
10	IPC_RST	Default Value: 0
7	DW1_RST	Default Value: 0
6	DW0_RST	Default Value: 0
3	RAMC0_RST	Default Value: 0
2	FLASHC_RST	Default Value: 0
0	PROMC_RST	Slave reset controls. Each bit indicates whether the respective slave reset is enabled or not. 0: Disabled 1: Enabled If the slave is under reset enabled state, its clock is gated off (constant "0") and its resets are in activated state (rst_n = 0) Any access (MMIO AHB access or ROM/System SRAM memory access) to slave when disabled result in AHB error response. Default Value: 0

1.1.112 CM33_SCS_ICTR

Interrupt Controller Type Register

Address: 0xE000E004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Shows the number of interrupt lines that the NVIC supports Total number of interrupt lines in groups of 32: 0b0000 = 1...32 0b0001 = 33...64 0b0010 = 65...96 0b0011 = 97...128 0b0100 = 129...160 0b0101 = 161...192 0b0110 = 193...224 0b0111 = 225...256 0b1000 = 257...288 0b1001 = 289...320 0b1010 = 321...352 0b1011 = 353...384 0b1100 = 385...416 0b1101 = 417...448 0b1110 = 449...480 Default Value: 0x0000000X

1.1.113 CM33_SCS_ACTLR

Auxiliary Control Register

Address: 0xE000E008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer the following ARM documents for details about CPU register descriptions: ARMv8-M : https://developer.arm.com/documentation/ddi0553/latest/ CM33 TRM - ACTLR : https://developer.arm.com/documentation/100230/0100/System-Control/Auxiliary-Control-Register Default Value: 0

1.1.114 CM33_SCS_SYST_CSR

SysTick Control and Status Register

Address: 0xE000E010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.189 SYST_CSR, SysTick Control and Status Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

1.1.115 CM33_SCS_SYST_RVR

SysTick Reload Value Register

Address: 0xE000E014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.191 SYST_RVR, SysTick Reload Value Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

1.1.116 CM33_SCS_SYST_CVR

SysTick Current Value Register

Address: 0xE000E018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.190 SYST_CVR, SysTick Current Value Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

1.1.117 CM33_SCS_SYST_CALIB

SysTick Calibration value Register

Address: 0xE000E01C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.188 SYST_CALIB, SysTick Calibration Value Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

1.1.118 CM33_SCS_NVIC_ISER0

Interrupt Set-Enable Registers

Address: 0xE000E100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.165 NVIC_ISER, Interrupt Set Enable Register, n = 0 - 15" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

1.1.119 CM33_SCS_NVIC_ICER0

Interrupt Clear-Enable Registers

Address: 0xE000E180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.162 NVIC_ICER, Interrupt Clear Enable Register, n = 0 - 15" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

1.1.120 CM33_SCS_NVIC_ISPR0

Interrupt Set-Pending Registers

Address: 0xE000E200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.166 NVIC_ISPR, Interrupt Set Pending Register, n = 0 - 15" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

1.1.121 CM33_SCS_NVIC_ICPR0

Interrupt Clear-Pending Registers

Address: 0xE000E280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.163 NVIC_ICPR, Interrupt Clear Pending Register, n = 0 - 15" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

1.1.122 CM33_SCS_NVIC_IABR0

Interrupt Active Bit Registers

Address: 0xE000E300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.161 NVIC_IABR, Interrupt Active Bit Register, n = 0 - 15" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

1.1.123 CM33_SCS_NVIC_ITNS0

Interrupt Target Non-secure Registers

Address: 0xE000E380

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.167 NVIC_ITNS, Interrupt Target Non-secure Register, n = 0 - 15" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

1.1.124 CM33_SCS_NVIC_IPR0

Interrupt Priority Registers

Address: 0xE000E400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.164 NVIC_IPR, Interrupt Priority Register, n = 0 - 123" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

1.1.125 CM33_SCS_CPUID

CPUID Base Register

Address: 0xE000ED00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer CM33 TRM - CPUID: https://developer.arm.com/documentation/100230/0100/System-Control/CPUID-Base-Register Default Value: 0x410FD214

1.1.126 CM33_SCS_VTOR

Vector Table Offset Register

Address: 0xE000ED08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Table offset. Bits [31:7] of the vector table address for the selected Security state. It is IMPLEMENTATION DEFINED whether any of the TBLOFF bits are WI. This field resets to an IMPLEMENTATION DEFINED value on a Warm reset. Default Value: 0

1.1.127 CM33_SCS_AIRCR

Application Interrupt and Reset Control Register

Address: 0xE000ED0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.3 AIRCR, Application Interrupt and Reset Control Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

1.1.128 CM33_SCS_SCR

System Control Register

Address: 0xE000ED10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.178 SCR, System Control Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

1.1.129 CM33_SCS_CCR

Configuration and Control Register

Address: 0xE000ED14

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.9 CCR, Configuration and Control Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

1.1.130 CM33_SCS_DFSR

Debug Fault Status Register

Address: 0xE000ED30

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.37 DFSR, Debug Fault Status Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

1.1.131 CM33_SCS_ID_PFR0

Processor Feature Register 0

Address: 0xE000ED40

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.120 ID_PFR0, Processor Feature Register 0" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00000030

1.1.132 CM33_SCS_ID_PFR1

Processor Feature Register 1

Address: 0xE000ED44

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.121 ID_PFR1, Processor Feature Register 1" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x000002X0

1.1.133 CM33_SCS_ID_DFR0

Debug Feature Register 0

Address: 0xE000ED48

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.109 ID_DFR0, Debug Feature Register 0" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00200000

1.1.134 CM33_SCS_ID_AFR0

Auxiliary Feature Register 0

Address: 0xE000ED4C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.108 ID_AFR0, Auxiliary Feature Register 0" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

1.1.135 CM33_SCS_ID_MMFR0

Memory Model Feature Register 0

Address: 0xE000ED50

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.116 ID_MMFR0, Memory Model Feature Register 0" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00101F40

1.1.136 CM33_SCS_ID_MMFR1

Memory Model Feature Register 1

Address: 0xE000ED54

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.117 ID_MMFR1, Memory Model Feature Register 1" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

1.1.137 CM33_SCS_ID_MMFR2

Memory Model Feature Register 2

Address: 0xE000ED58

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.118 ID_MMFR2, Memory Model Feature Register 2" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x01000000

1.1.138 CM33_SCS_ID_MMFR3

Memory Model Feature Register 3

Address: 0xE000ED5C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.119 ID_MMFR3, Memory Model Feature Register 3" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

1.1.139 CM33_SCS_ID_ISAR0

Instruction Set Attributes Register 0

Address: 0xE000ED60

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.110 ID_ISAR0, Instruction Set Attribute Register 0" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x011X1110

1.1.140 CM33_SCS_ID_ISAR1

Instruction Set Attributes Register 1

Address: 0xE000ED64

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.111 ID_ISAR1, Instruction Set Attribute Register 1" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x0221X000

1.1.141 CM33_SCS_ID_ISAR2

Instruction Set Attributes Register 2

Address: 0xE000ED68

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.112 ID_ISAR2, Instruction Set Attribute Register 2" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x20XX2232

1.1.142 CM33_SCS_ID_ISAR3

Instruction Set Attributes Register 3

Address: 0xE000ED6C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.113 ID_ISAR3, Instruction Set Attribute Register 3" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x011111XX

1.1.143 CM33_SCS_ID_ISAR4

Instruction Set Attributes Register 4

Address: 0xE000ED70

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.114 ID_ISAR4, Instruction Set Attribute Register 4" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x01310132

1.1.144 CM33_SCS_CLIDR

Cache Level ID Register

Address: 0xE000ED78

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.12 CLIDR, Cache Level ID Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

1.1.145 CM33_SCS_CTR

Cache Type Register

Address: 0xE000ED7C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.18 CTR, Cache Type Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x8000C000

1.1.146 CM33_SCS_CPACR

Coprocessor Access Control Register

Address: 0xE000ED88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.14 CPACR, Coprocessor Access Control Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

1.1.147 CM33_SCS_NSACR

Non-secure Access Control Register

Address: 0xE000ED8C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.160 NSACR, Non-secure Access Control Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

1.1.148 CM33_SCS_MPU_TYPE

MPU Type Register

Address: 0xE000ED90

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.155 MPU_TYPE, MPU Type Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x0000XX00

1.1.149 CM33_SCS_MPU_CTRL

MPU Control Register

Address: 0xE000ED94

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.147 MPU_CTRL, MPU Control Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

1.1.150 CM33_SCS_MPU_RNR

MPU Region Number Register

Address: 0xE000ED98

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.154 MPU_RNR, MPU Region Number Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

1.1.151 CM33_SCS_MPU_RBAR

MPU Region Base Address Register

Address: 0xE000ED9C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.150 MPU_RBAR, MPU Region Base Address Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

1.1.152 CM33_SCS_MPU_RLAR

MPU Region Limit Address Register

Address: 0xE000EDA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.152 MPU_RLAR, MPU Region Limit Address Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

1.1.153 CM33_SCS_MPU_RBAR_A1

MPU alias registers

Address: 0xE000EDA4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.151 MPU_RBAR_A, MPU Region Base Address Register Alias, n = 1" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

1.1.154 CM33_SCS_MPU_RLAR_A1

MPU alias registers

Address: 0xE000EDA8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.153 MPU_RLAR_A, MPU Region Limit Address Register Alias, n = 1" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

1.1.155 CM33_SCS_MPU_RBAR_A2

MPU alias registers

Address: 0xE000EDAC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.151 MPU_RBAR_A, MPU Region Base Address Register Alias, n = 2" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

1.1.156 CM33_SCS_MPU_RLAR_A2

MPU alias registers

Address: 0xE000EDB0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.153 MPU_RLAR_A, MPU Region Limit Address Register Alias, n = 2" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

1.1.157 CM33_SCS_MPU_RBAR_A3

MPU alias registers

Address: 0xE000EDB4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.151 MPU_RBAR_A, MPU Region Base Address Register Alias, n = 3" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

1.1.158 CM33_SCS_MPU_RLAR_A3

MPU alias registers

Address: 0xE000EDB8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.153 MPU_RLAR_A, MPU Region Limit Address Register Alias, n = 3" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

1.1.159 CM33_SCS_MPU_MAIR0

MPU Memory Attribute Indirection Register 0

Address: 0xE000EDC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.148 MPU_MAIR0, MPU Memory Attribute Indirection Register 0" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

1.1.160 CM33_SCS_MPU_MAIR1

MPU Memory Attribute Indirection Register 1

Address: 0xE000EDC4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.149 MPU_MAIR1, MPU Memory Attribute Indirection Register 1" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

1.1.161 CM33_SCS_SAU_CTRL

SAU Control Register

Address: 0xE000EDD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.173 SAU_CTRL, SAU Control Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

1.1.162 CM33_SCS_SAU_TYPE

SAU Type Register

Address: 0xE000EDD4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.177 SAU_TYPE, SAU Type Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00000008

1.1.163 CM33_SCS_SAU_RNR

SAU Region Number Register

Address: 0xE000EDD8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.176 SAU_RNR, SAU Region Number Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

1.1.164 CM33_SCS_SAU_RBAR

SAU Region Base Address Register

Address: 0xE000EDDC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.174 SAU_RBAR, SAU Region Base Address Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

1.1.165 CM33_SCS_SAU_RLAR

SAU Region Limit Address Register

Address: 0xE000EDE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.175 SAU_RLAR, SAU Region Limit Address Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

1.1.166 CM33_SCS_DHCSR

Debug Halting Control and Status Register

Address: 0xE000EDF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.38 DHCSR, Debug Halting Control and Status Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

1.1.167 CM33_SCS_DCRSR

Debug Core Register Selector Register

Address: 0xE000EDF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.33 DCRSR, Debug Core Register Select Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

1.1.168 CM33_SCS_DCRDR

Debug Core Register Data Register

Address: 0xE000EDF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.32 DCRDR, Debug Core Register Data Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

1.1.169 CM33_SCS_DEMCR

Debug Exception and Monitor Control Register

Address: 0xE000EDFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.36 DEMCR, Debug Exception and Monitor Control Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

1.1.170 CM33_SCS_DAUTHCTRL

Debug Authentication Control Register

Address: 0xE000EE04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.19 DAUTHCTRL, Debug Authentication Control Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

1.1.171 CM33_SCS_DSCSR

Debug Security Control and Status Register

Address: 0xE000EE08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.49 DSCSR, Debug Security Control and Status Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

1.1.172 CM33_SCS_FPCCR

FP Context Control Register

Address: 0xE000EF34

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.81 FPCCR, Floating-Point Context Control Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0xC0000004

1.1.173 CM33_SCS_FPCAR

FP Context Control Register

Address: 0xE000EF38

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.80 FPCAR, Floating-Point Context Address Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

1.1.174 CM33_SCS_FPDSCR

FP Context Control Register

Address: 0xE000EF3C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.82 FPDSCR, Floating-Point Default Status Control Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

1.1.175 CM33_SCS_MVFR0

Media and VFP Feature Register 0

Address: 0xE000EF40

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.157 MVFR0, Media and VFP Feature Register 0" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x10110021

1.1.176 CM33_SCS_MVFR1

Media and VFP Feature Register 1

Address: 0xE000EF44

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.158 MVFR1, Media and VFP Feature Register 1" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x11000011

1.1.177 CM33_SCS_MVFR2

Media and VFP Feature Register 2

Address: 0xE000EF48

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.159 MVFR2, Media and VFP Feature Register 2" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00000040

1.1.178 CM33_SCS_DAUTHSTATUS

Debug Authentication Status Register

Address: 0xE000EFB8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.20 DAUTHSTATUS, Debug Authentication Status Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: Undefined

1.1.179 CM33_SCS_DEVARCH

CoreSight Device Architecture Register

Address: 0xE000EFBC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.34 DDEVARCH, SCS Device Architecture Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x47702A04

1.1.180 CM33_SCS_PIDR4

Peripheral Identification Register 4

Address: 0xE000EFD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.45 DPIDR4, SCS Peripheral Identification Register 4" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00000004

1.1.181 CM33_SCS_PIDR5

Peripheral Identification Register 5

Address: 0xE000EFD4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.46 DPIDR5, SCS Peripheral Identification Register 5" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

1.1.182 CM33_SCS_PIDR6

Peripheral Identification Register 6

Address: 0xE000EFD8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.47 DPIDR5, SCS Peripheral Identification Register 6" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

1.1.183 CM33_SCS_PIDR7

Peripheral Identification Register 7

Address: 0xE000EFDC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.48 DPIDR7, SCS Peripheral Identification Register 7" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

1.1.184 CM33_SCS_PIDR0

Peripheral Identification Register 0

Address: 0xE000EFE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.41 DPIDR0, SCS Peripheral Identification Register 0" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00000021

1.1.185 CM33_SCS_PIDR1

Peripheral Identification Register 1

Address: 0xE000EFE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.42 DPIDR1, SCS Peripheral Identification Register 1" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x000000BD

1.1.186 CM33_SCS_PIDR2

Peripheral Identification Register 2

Address: 0xE000EFE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.43 DPIDR2, SCS Peripheral Identification Register 2" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x0000000B

1.1.187 CM33_SCS_PIDR3

Peripheral Identification Register 3

Address: 0xE000EFEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.44 DPIDR3, SCS Peripheral Identification Register 3" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0

1.1.188 CM33_SCS_CIDR0

Component Identification Register 0

Address: 0xE000EFF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.26 DCIDR0, SCS Component Identification Register 0" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x0000000D

1.1.189 CM33_SCS_CIDR1

Component Identification Register 1

Address: 0xE000EFF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.27 DCIDR1, SCS Component Identification Register 1" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00000090

1.1.190 CM33_SCS_CIDR2

Component Identification Register 2

Address: 0xE000EFF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.28 DCIDR2, SCS Component Identification Register 2" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00000005

1.1.191 CM33_SCS_CIDR3

Component Identification Register 3

Address: 0xE000EFFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.29 DCIDR3, SCS Component Identification Register 3" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x000000B1

1.1.192 CM33_CM33CTI_CTICONTROL

CTI Control Register

Address: 0xE0042000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

1.1.193 CM33_CM33CTI_CTIINTACK

CTI Interrupt Acknowledge Register

Address: 0xE0042010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: X

1.1.194 CM33_CM33CTI_CTIAPPSET

CTI Application Trigger Set Register

Address: 0xE0042014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

1.1.195 CM33_CM33CTI_CTIAPPCLEAR

CTI Application Trigger Clear Register

Address: 0xE0042018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

1.1.196 CM33_CM33CTI_CTIAPPPULSE

CTI Application Pulse Register

Address: 0xE004201C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: X

1.1.197 CM33_CM33CTI_CTIINEN0

CTI Trigger to Channel Enable Registers

Address: 0xE0042020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

1.1.198 CM33_CM33CTI_CTIOUTEN0

CTI Channel to Trigger Enable Registers

Address: 0xE00420A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

1.1.199 CM33_CM33CTI_CTITRIGINSTATUS

CTI Trigger In Status Register

Address: 0xE0042130

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

1.1.200 CM33_CM33CTI_CTITRIGOUTSTATUS

CTI Trigger Out Status Register

Address: 0xE0042134

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

1.1.201 CM33_CM33CTI_CTICHINSTATUS

CTI Channel In Status Register

Address: 0xE0042138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

1.1.202 CM33_CM33CTI_CTIGATE

Enable CTI Channel Gate Register

Address: 0xE0042140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x0000000F

1.1.203 CM33_CM33CTI_ASICCTL

External Multiplexor Control Register

Address: 0xE0042144

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

1.1.204 CM33_CM33CTI_ITCHOUT

ITCHOUT Register

Address: 0xE0042EE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: X

1.1.205 CM33_CM33CTI_ITTRIGOUT

ITTRIGOUT Register

Address: 0xE0042EE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: X

1.1.206 CM33_CM33CTI_ITCHIN

ITCHIN Register

Address: 0xE0042EF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

1.1.207 CM33_CM33CTI_ITCTRL

Integration Mode Control Register

Address: 0xE0042F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

1.1.208 CM33_CM33CTI_DEVARCH

Device Architecture register

Address: 0xE0042FBC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x47701A14

1.1.209 CM33_CM33CTI_DEVID

Device Configuration Register

Address: 0xE0042FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00040800

1.1.210 CM33_CM33CTI_DEVTYPE

Device Type Identifier Register

Address: 0xE0042FCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000014

1.1.211 CM33_CM33CTI_PIDR4

Peripheral Identification Register 4

Address: 0xE0042FD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000004

1.1.212 CM33_CM33CTI_PIDR5

Peripheral Identification Register 5

Address: 0xE0042FD4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

1.1.213 CM33_CM33CTI_PIDR6

Peripheral Identification Register 6

Address: 0xE0042FD8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

1.1.214 CM33_CM33CTI_PIDR7

Peripheral Identification Register 7

Address: 0xE0042FDC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

1.1.215 CM33_CM33CTI_PIDR0

Peripheral Identification Register 0

Address: 0xE0042FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000021

1.1.216 CM33_CM33CTI_PIDR1

Peripheral Identification Register 1

Address: 0xE0042FE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x000000BD

1.1.217 CM33_CM33CTI_PIDR2

Peripheral Identification Register 2

Address: 0xE0042FE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x0000000B

1.1.218 CM33_CM33CTI_PIDR3

Peripheral Identification Register 3

Address: 0xE0042FEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

1.1.219 CM33_CM33CTI_CIDR0

Component Identification Register 0

Address: 0xE0042FF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x0000000D

1.1.220 CM33_CM33CTI_CIDR1

Component Identification Register 1

Address: 0xE0042FF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000090

1.1.221 CM33_CM33CTI_CIDR2

Component Identification Register 2

Address: 0xE0042FF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000005

1.1.222 CM33_CM33CTI_CIDR3

Component Identification Register 3

Address: 0xE0042FFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x000000B1

1.1.223 CM33_TRC_CTI_CTICONTROL

CTI Control Register

Address: 0xE0080000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							GLBEN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	GLBEN	Enables or disables the ECT: 0 = disabled (reset) 1 = enabled. When disabled, all cross triggering mapping logic functionality is disabled for this processor. Default Value: 0

1.1.224 CM33_TRC_CTI_CTIINTACK

CTI Interrupt Acknowledge Register

Address: 0xE0080010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	INTACK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	INTACK	Acknowledges the corresponding CTITRIGOUT output: 1 = CTITRIGOUT is acknowledged and is cleared when MAPTRIGOUT is LOW. 0 = no effect. There is one bit of the register for each CTITRIGOUT output. Default Value: 0

1.1.225 CM33_TRC_CTI_CTIAPPSET

CTI Application Trigger Set Register

Address: 0xE0080014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				APPSET [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	APPSET	Setting a bit HIGH generates a channel event for the selected channel. Read: 0 = application trigger inactive (reset) 1 = application trigger active. Write: 0 = no effect 1 = generate channel event. There is one bit of the register for each channel. Default Value: 0

1.1.226 CM33_TRC_CTI_CTIAPPCLEAR

CTI Application Trigger Clear Register

Address: 0xE0080018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				W			
HW Access	None				R			
Name	None [7:4]				APPCLEAR [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	APPCLEAR	Clears corresponding bits in the CTIAPPSET register. 1 = application trigger disabled in the CTIAPPSET register 0 = no effect. There is one bit of the register for each channel. Default Value: 0

1.1.227 CM33_TRC_CTI_CTIAPPPULSE

CTI Application Pulse Register

Address: 0xE008001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				W			
HW Access	None				R			
Name	None [7:4]				APPULSE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	APPULSE	Setting a bit HIGH generates a channel event pulse for the selected channel. Write: 1 = channel event pulse generated for one CTICLK period 0 = no effect. There is one bit of the register for each channel. Default Value: 0

1.1.228 CM33_TRC_CTI_CTIINEN0

CTI Trigger to Channel Enable Registers

Address: 0xE0080020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGINEN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	TRIGINEN	Enables a cross trigger event to the corresponding channel when an CTITRIGIN is activated. 1 = enables the CTITRIGIN signal to generate an event on the respective channel of the CTM. There is one bit of the register for each of the four channels. For example in register CTIINEN0, TRIGINEN[0] set to 1 enables CTITRIGIN onto channel 0. 0 = disables the CTITRIGIN signal from generating an event on the respective channel of the CTM. Default Value: 0

1.1.229 CM33_TRC_CTI_CTIOUTEN0

CTI Channel to Trigger Enable Registers

Address: 0xE00800A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGOUTEN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	TRIGOUTEN	Changing the value of this bit from a 0 to a 1 enables a channel event for the corresponding channel to generate an CTITRIGOUT output: 0 = the channel input (CTICHIN) from the CTM is not routed to the CTITRIGOUT output 1 = the channel input (CTICHIN) from the CTM is routed to the CTITRIGOUT output. There is one bit for each of the four channels. For example in register CTIOUTEN0, enabling bit 0 enables CTICHIN[0] to cause a trigger event on the CTITRIGOUT[0] output. Default Value: 0

1.1.230 CM33_TRC_CTI_CTITRIGINSTATUS

CTI Trigger In Status Register

Address: 0xE0080130

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TRIGINSTATUS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	TRIGINSTATUS	Shows the status of the CTITRIGIN inputs: 1 = CTITRIGIN is active 0 = CTITRIGIN is inactive. Because the register provides a view of the raw CTITRIGIN inputs, the reset value is unknown. There is one bit of the register for each trigger input. Default Value: 0

1.1.231 CM33_TRC_CTI_CTITRIGOUTSTATUS

CTI Trigger Out Status Register

Address: 0xE0080134

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TRIGOUTSTATUS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	TRIGOUTSTATUS	Shows the status of the CTITRIGOUT outputs. 1 = CTITRIGOUT is active 0 = CTITRIGOUT is inactive (reset). There is one bit of the register for each trigger output. Default Value: 0

1.1.232 CM33_TRC_CTI_CTICHINSTATUS

CTI Channel In Status Register

Address: 0xE0080138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				RW			
Name	None [7:4]				CTICHINSTATUS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	CTICHINSTATUS	Shows the status of the CTICHIN inputs: 1 = CTICHIN is active 0 = CTICHIN is inactive. Because the register provides a view of the raw CTICHIN inputs from the CTM, the reset value is unknown. There is one bit of the register for each channel input. Default Value: 0

1.1.233 CM33_TRC_CTI_CTICHOUTSTATUS

CTI Channel Out Status Register

Address: 0xE008013C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				RW			
Name	None [7:4]				CTICHOUTSTATUS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	CTICHOUTSTATUS	Shows the status of the CTICHOUT outputs. 1 = CTICHOUT is active 0 = CTICHOUT is inactive (reset). There is one bit of the register for each channel output. Default Value: 0

1.1.234 CM33_TRC_CTI_CTIGATE

Enable CTI Channel Gate Register

Address: 0xE0080140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				CTIGA-TEEN3	CTIGA-TEEN2	CTIGA-TEEN1	CTIGA-TEEN0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	CTIGATEEN3	Enable CTICHOUT3. Set to 0 to disable channel propagation. Default Value: 1
2	CTIGATEEN2	Enable CTICHOUT2. Set to 0 to disable channel propagation. Default Value: 1
1	CTIGATEEN1	Enable CTICHOUT1. Set to 0 to disable channel propagation. Default Value: 1
0	CTIGATEEN0	Enable CTICHOUT0. Set to 0 to disable channel propagation. Default Value: 1

1.1.235 CM33_TRC_CTI_ASICCTL

External Multiplexor Control Register

Address: 0xE0080144

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ASICCTL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	ASICCTL	Implementation-defined ASIC control, value written to the register is output on ASICCTL[7:0]. If external multiplexing of trigger signals is implemented then the number of multiplexed signals on each trigger must be reflected within the Device ID Register. This is done within a Verilog define EXTMUXNUM. See ECT CoreSight defined registers on page 4-28. Default Value: 0

1.1.236 CM33_TRC_CTI_ITCHINACK

ITCHINACK Register

Address: 0xE0080EDC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				W			
HW Access	None				R			
Name	None [7:4]				CTCHINACK [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	CTCHINACK	Set the value of the CTCHINACK outputs Default Value: 0

1.1.237 CM33_TRC_CTI_ITTRIGINACK

ITTRIGINACK Register

Address: 0xE0080EE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	CTTRIGINACK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CTTRIGINACK	Set the value of the CTTRIGINACK outputs Default Value: 0

1.1.238 CM33_TRC_CTI_ITCHOUT

ITCHOUT Register

Address: 0xE0080EE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				W			
HW Access	None				R			
Name	None [7:4]				CTCHOUT [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	CTCHOUT	Set the value of the CTCHOUT outputs Default Value: 0

1.1.239 CM33_TRC_CTI_ITTRIGOUT

ITTRIGOUT Register

Address: 0xE0080EE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	CTTRIGOUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CTTRIGOUT	Set the value of the CTTRIGOUT outputs Default Value: 0

1.1.240 CM33_TRC_CTI_ITCHOUTACK

ITCHOUTACK Register

Address: 0xE0080EEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				CTCHOUTACK [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	CTCHOUTACK	Read the values of the CTCHOUTACK inputs Default Value: 0

1.1.241 CM33_TRC_CTI_ITTRIGOUTACK

ITTRIGOUTACK Register

Address: 0xE0080EF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CTTRIGOUTACK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CTTRIGOUTACK	Read the values of the CTTRIGOUTACK inputs Default Value: 0

1.1.242 CM33_TRC_CTI_ITCHIN

ITCHIN Register

Address: 0xE0080EF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				CTCHIN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	CTCHIN	Read the values of the CTCHIN inputs Default Value: 0

1.1.243 CM33_TRC_CTI_ITTRIGIN

ITTRIGIN Register

Address: 0xE0080EF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CTTRIGIN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CTTRIGIN	Read the values of the CTTRIGIN inputs Default Value: 0

1.1.244 CM33_TRC_CTI_ITCTRL

Integration Mode Control Register

Address: 0xE0080F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							MODE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	MODE	When set, the component enters integration mode, enabling topology detection or integration testing to be performed. At reset the component must enter functional mode. If no integration functionality is implemented, this register must read as zero. Default Value: 0

1.1.245 CM33_TRC_CTI_CLAIMSET

Claim Tag Set Register

Address: 0xE0080FA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S			
HW Access	None				R			
Name	None [7:4]				TAG [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	TAG	A bit programmable register bank which sets the Claim Tag Value. A read will return a logic 1 for all implemented locations. Default Value: 0xF

1.1.246 CM33_TRC_CTI_CLAIMCLR

Claim Tag Clear Register

Address: 0xE0080FA4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C			
HW Access	None				R			
Name	None [7:4]				TAG [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	TAG	A bit programmable register bank that is zero at reset. Default Value: 0

1.1.247 CM33_TRC_CTI_DEVAFF0

Device Affinity Register 0

Address: 0xE0080FA8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DEVAFF0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DEVAFF0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DEVAFF0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DEVAFF0 [31:24]							

Bits	Name	Description
31 : 0	DEVAFF0	Lower 32-bits of DEVAFF. The value is set by the devaff[31:0] tie-off inputs. Default Value: 0

1.1.248 CM33_TRC_CTI_DEVAFF1

Device Affinity Register 1

Address: 0xE0080FAC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DEVAFF0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DEVAFF0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DEVAFF0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DEVAFF0 [31:24]							

Bits	Name	Description
31 : 0	DEVAFF0	Upper 32-bits of DEVAFF. The value is set by the devaff[63:32] tie-off inputs. Default Value: 0

1.1.249 CM33_TRC_CTI_LAR

Lock Access Register

Address: 0xE0080FB0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	KEY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	KEY [31:24]							

Bits	Name	Description
31 : 0	KEY	Write Access Code. A write of 0xC5ACCE55 enables further write access to this device. An invalid write will have the affect of removing write access. If LSR[2] is set, then only bits [7:0] of this register are implemented and lock access is obtained by consecutively writing 0xC5, 0xAC, 0xCE, 0x55. Bits [31:8] are unused and any writes to them ignored. Default Value: 0

1.1.250 CM33_TRC_CTI_LSR

Lock Status Register

Address: 0xE0080FB4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [7:3]					nTT	SLK	SLI

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	nTT	This component implements an 32-bit Lock Access Register. Default Value: 0
1	SLK	The values of this bit mean: 0 = Access permitted. 1 = Write access to the component is blocked. All writes to control registers are ignored. Reads are permitted Default Value: 1
0	SLI	Indicates that a lock control mechanism exists for this device Default Value: 1

1.1.251 CM33_TRC_CTI_AUTHSTATUS

Authentication Status Register

Address: 0xE0080FB8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		R		R		R	
HW Access	W		W		W		W	
Name	SNIDBG [7:6]		SIDBG [5:4]		NSNIDBG [3:2]		NSIDBG [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SNIDBG	Secure Non-Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 0
5 : 4	SIDBG	Secure Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 0
3 : 2	NSNIDBG	Non-Secure Non-Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 0
1 : 0	NSIDBG	Non-Secure Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 0

1.1.252 CM33_TRC_CTI_DEVARCH

Device Architecture Register

Address: 0xE0080FBC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	.R							
HW Access	R							
Name	ARCHID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	.R							
HW Access	R							
Name	ARCHID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	.R			.R	.R			
HW Access	R			R	R			
Name	ARCHITECT [23:21]			PRESENT	REVISION [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	.R							
HW Access	R							
Name	ARCHITECT [31:24]							

Bits	Name	Description
31 : 21	ARCHITECT	Returns 0x23B, denoting Arm as architect of the component. Default Value: 0x023B
20	PRESENT	Returns 1, indicating that the DEVARCH register is present. Default Value: 1
19 : 16	REVISION	Architecture revision. Returns the revision of the architecture that the ARCHID field specifies. Default Value: 0x0000
15 : 0	ARCHID	Architecture ID. Returns 0x1A14, identifying Cross Trigger Interface architecture v2. Default Value: 0x1A14

1.1.253 CM33_TRC_CTI_DEVID

Device Configuration Register

Address: 0xE0080FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			R				
Name	None [7:5]			EXTMUXNUM [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	NUMTRIG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				R			
Name	None [23:20]				NUMCH [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	NUMCH	Number of ECT channels available. Default Value: 4
15 : 8	NUMTRIG	Number of ECT triggers available. Default Value: 8
4 : 0	EXTMUXNUM	Indicates the number of multiplexing available on Trigger Inputs and Trigger Outputs using ASICCTL. Default value of 5'b00000 indicating no multiplexing present. Reflects the value of the Verilog `define EXTMUXNUM that you must alter accordingly. Default Value: 0

1.1.254 CM33_TRC_CTI_DEVTYPE

Device Type Identifier Register

Address: 0xE0080FCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	SUB_TYPE [7:4]				CLASS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	SUB_TYPE	cross trigger Default Value: 0x1
3 : 0	CLASS	debug control logic component Default Value: 0x4

1.1.255 CM33_TRC_CTI_PIDR4

Peripheral Identification Register 4

Address: 0xE0080FD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	N/A Default Value: 0x00000004

1.1.256 CM33_TRC_CTI_PIDR5

Peripheral Identification Register 5

Address: 0xE0080FD4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	N/A Default Value: 0x00000000

1.1.257 CM33_TRC_CTI_PIDR6

Peripheral Identification Register 6

Address: 0xE0080FD8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	N/A Default Value: 0x00000000

1.1.258 CM33_TRC_CTI_PIDR7

Peripheral Identification Register 7

Address: 0xE0080FDC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	N/A Default Value: 0x00000000

1.1.259 CM33_TRC_CTI_PIDR0

Peripheral Identification Register 0

Address: 0xE0080FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	N/A Default Value: 0x00000006

1.1.260 CM33_TRC_CTI_PIDR1

Peripheral Identification Register 1

Address: 0xE0080FE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	N/A Default Value: 0x000000B9

1.1.261 CM33_TRC_CTI_PIDR2

Peripheral Identification Register 2

Address: 0xE0080FE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	N/A Default Value: 0x0000005B

1.1.262 CM33_TRC_CTI_PIDR3

Peripheral Identification Register 3

Address: 0xE0080FEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None			
HW Access	R				None			
Name	ECOREVNUM [7:4]				None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	ECOREVNUM	ECO revision for MTB Default Value: 0x0

1.1.263 CM33_TRC_CTI_CIDR0

Component Identification Register 0

Address: 0xE0080FF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	N/A Default Value: 0x0000000D

1.1.264 CM33_TRC_CTI_CIDR1

Component Identification Register 1

Address: 0xE0080FF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	N/A Default Value: 0x00000090

1.1.265 CM33_TRC_CTI_CIDR2

Component Identification Register 2

Address: 0xE0080FF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	N/A Default Value: 0x00000005

1.1.266 CM33_TRC_CTI_CIDR3

Component Identification Register 3

Address: 0xE0080FFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	N/A Default Value: 0x000000B1

1.1.267 CM33_CSTF_FUNNELCONTROL

Funnel Control Register

Address: 0xE0088000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.1 css600_atbfunnel Funnel Control register, FUNNELCONTROL" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x00000300

1.1.268 CM33_CSTF_PRIORITYCONTROL

Priority Control Register

Address: 0xE0088004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.2 css600_atbfunnel Priority Control register, PRIORITYCONTROL" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0

1.1.269 CM33_CSTF_ITATBDATA0

Integration Register

Address: 0xE0088EEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.3 css600_atbfunnel Integration test data register, ITATBDATA0" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0

1.1.270 CM33_CSTF_ITATBCTR3

Integration Register

Address: 0xE0088EF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.4 css600_atbfunnel Integration test control register 3, ITATBCTR3" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0

1.1.271 CM33_CSTF_ITATBCTR2

Integration Register

Address: 0xE0088EF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.5 css600_atbfunnel Integration test control register 2, ITATBCTR2" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0

1.1.272 CM33_CSTF_ITATBCTR1

Integration Register

Address: 0xE0088EF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.6 css600_atbfunnel Integration test control register 1, ITATBCTR1" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0

1.1.273 CM33_CSTF_ITATBCTR0

Integration Register

Address: 0xE0088EFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.7 css600_atbfunnel Integration test control register 0, ITATBCTR0" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0

1.1.274 CM33_CSTF_ITCTRL

Integration Mode Control Register

Address: 0xE0088F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.8 css600_atbfunnel Integration Mode Control Register, ITCTRL" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0

1.1.275 CM33_CSTF_CLAIMSET

Claim Tag Set Register

Address: 0xE0088FA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.9 css600_atbfunnel Claim Tag Set Register, CLAIMSET" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0xF

1.1.276 CM33_CSTF_CLAIMCLR

Claim Tag Clear Register

Address: 0xE0088FA4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.10 css600_atbfunnel Claim Tag Clear Register, CLAIMCLR" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0

1.1.277 CM33_CSTF_DEVAFF0

Device Affinity Register0

Address: 0xE0088FB0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.11 css600_atbfunnel Device Affinity register 0, DEVAFF0" in ARM Core-Sight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0

1.1.278 CM33_CSTF_DEVAFF1

Device Affinity Register1

Address: 0xE0088FB4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.12 css600_atbfunnel Device Affinity register 1, DEVAFF1" in ARM Core-Sight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x3

1.1.279 CM33_CSTF_AUTHSTATUS

Authentication Status Register

Address: 0xE0088FB8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.13 css600_atbfunnel Authentication Status Register, AUTHSTATUS" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0

1.1.280 CM33_CSTF_DEVARCH

Device Architecture Register

Address: 0xE0088FBC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.14 css600_atbfunnel Device Architecture Register, DEVARCH" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0

1.1.281 CM33_CSTF_DEVID2

Device Configuration Register 2

Address: 0xE0088FC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.15 css600_atbfunnel Device Configuration Register 2, DEVID2" in ARM Core-Sight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x00000000

1.1.282 CM33_CSTF_DEVID1

Device Configuration Register 1

Address: 0xE0088FC4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.16 css600_atbfunnel Device Configuration Register 1, DEVID1" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x00000000

1.1.283 CM33_CSTF_DEVID

Device Configuration Register

Address: 0xE0088FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.17 css600_atbfunnel Device Configuration Register, DEVID" in ARM Core-Sight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x0000003X

1.1.284 CM33_CSTF_DEVTYPE

Device Type Identifier Register

Address: 0xE0088FCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.18 css600_atbfunnel Device Type Identifier Register, DEVTYPE" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x00000012

1.1.285 CM33_CSTF_PIDR4

Peripheral Identification Register 4

Address: 0xE0088FD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.19 css600_atbfunnel Peripheral Identification Register 4, PIDR4" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x00000004

1.1.286 CM33_CSTF_PIDR5

Peripheral Identification Register 5

Address: 0xE0088FD4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.20 css600_atbfunnel Peripheral Identification Register 5, PIDR5" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x00000000

1.1.287 CM33_CSTF_PIDR6

Peripheral Identification Register 6

Address: 0xE0088FD8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.21 css600_atbfunnel Peripheral Identification Register 6, PIDR6" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x00000000

1.1.288 CM33_CSTF_PIDR7

Peripheral Identification Register 7

Address: 0xE0088FDC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.22 css600_atbfunnel Peripheral Identification Register 7, PIDR7" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x00000000

1.1.289 CM33_CSTF_PIDR0

Peripheral Identification Register 0

Address: 0xE0088FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.23 css600_atbfunnel Peripheral Identification Register 0, PIDR0" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x000000EB

1.1.290 CM33_CSTF_PIDR1

Peripheral Identification Register 1

Address: 0xE0088FE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.24 css600_atbfunnel Peripheral Identification Register 1, PIDR1" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x000000B9

1.1.291 CM33_CSTF_PIDR2

Peripheral Identification Register 2

Address: 0xE0088FE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.25 css600_atbfunnel Peripheral Identification Register 2, PIDR2" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x0000002B

1.1.292 CM33_CSTF_PIDR3

Peripheral Identification Register 3

Address: 0xE0088FEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None			
HW Access	R				None			
Name	ECOREVNUM [7:4]				None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	ECOREVNUM	Refer "10.11.2.26 css600_atbfunnel Peripheral Identification Register 3, PIDR3" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x0

1.1.293 CM33_CSTF_CIDR1

Component Identification Register 1

Address: 0xE0088FF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.28 css600_atbfunnel Component Identification Register 1, CIDR1" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x00000090

1.1.294 CM33_CSTF_CIDR2

Component Identification Register 2

Address: 0xE0088FF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.29 css600_atbfunnel Component Identification Register 2, CIDR2" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x00000005

1.1.295 CM33_CSTF_CIDR3

Component Identification Register 3

Address: 0xE0088FFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "10.11.2.30 css600_atbfunnel Component Identification Register 3, CIDR3" in ARM CoreSight(TM) System-on-Chip SoC-600 TRM: https://developer.ARMcom/documentation/100806/0402/?lang=en Default Value: 0x000000B1

1.1.296 CM33_ETF_RSZ

RAM Size register

Address: 0xE008D004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VALUE0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	VALUE0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	VALUE0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	VALUE0 [31:24]							

Bits	Name	Description
31 : 0	VALUE0	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

1.1.297 CM33_ETF_STS

Status Register

Address: 0xE008D00C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VALUE1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	VALUE1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	VALUE1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	VALUE1 [31:24]							

Bits	Name	Description
31 : 0	VALUE1	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

1.1.298 CM33_ETF_RRD

RAM Read Data Register

Address: 0xE008D010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VALUE2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	VALUE2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	VALUE2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	VALUE2 [31:24]							

Bits	Name	Description
31 : 0	VALUE2	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

1.1.299 CM33_ETF_RRP

RAM Read Pointer Register

Address: 0xE008D014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE3 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE3 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE3 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE3 [31:24]							

Bits	Name	Description
31 : 0	VALUE3	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

1.1.300 CM33_ETF_RWP

RAM Write Pointer Register

Address: 0xE008D018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE4 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE4 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE4 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE4 [31:24]							

Bits	Name	Description
31 : 0	VALUE4	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

1.1.301 CM33_ETF_TRG

Trigger Counter Register

Address: 0xE008D01C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE5 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE5 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE5 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE5 [31:24]							

Bits	Name	Description
31 : 0	VALUE5	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

1.1.302 CM33_ETF_CTL

Control Register

Address: 0xE008D020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE6 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE6 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE6 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE6 [31:24]							

Bits	Name	Description
31 : 0	VALUE6	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

1.1.303 CM33_ETF_RWD

RAM Write Data Register

Address: 0xE008D024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	VALUE7 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	VALUE7 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	VALUE7 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	VALUE7 [31:24]							

Bits	Name	Description
31 : 0	VALUE7	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

1.1.304 CM33_ETF_MODE

Mode Register

Address: 0xE008D028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE8 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE8 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE8 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE8 [31:24]							

Bits	Name	Description
31 : 0	VALUE8	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

1.1.305 CM33_ETF_LBUFLEVEL

Latched Buffer Fill Level

Address: 0xE008D02C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE9 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE9 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE9 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE9 [31:24]							

Bits	Name	Description
31 : 0	VALUE9	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

1.1.306 CM33_ETF_CBUFLEVEL

Current Buffer Fill Level

Address: 0xE008D030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE10 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE10 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE10 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE10 [31:24]							

Bits	Name	Description
31 : 0	VALUE10	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

1.1.307 CM33_ETF_BUFWM

Buffer Level Water Mark

Address: 0xE008D034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE11 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE11 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE11 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE11 [31:24]							

Bits	Name	Description
31 : 0	VALUE11	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

1.1.308 CM33_ETF_FFSR

Formatter and Flush Status Register

Address: 0xE008D300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE12 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE12 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE12 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE12 [31:24]							

Bits	Name	Description
31 : 0	VALUE12	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

1.1.309 CM33_ETF_FFCR

Formatter and Flush Control Register

Address: 0xE008D304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE13 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE13 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE13 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE13 [31:24]							

Bits	Name	Description
31 : 0	VALUE13	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

1.1.310 CM33_ETF_PSCR

Periodic Synchronization Counter Register

Address: 0xE008D308

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE14 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE14 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE14 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE14 [31:24]							

Bits	Name	Description
31 : 0	VALUE14	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0x0000000A

1.1.311 CM33_ETF_ITATBMDATA0

Integration Test ATB Master Data 0 Register

Address: 0xE008DED0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	VALUE15 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	VALUE15 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	VALUE15 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	VALUE15 [31:24]							

Bits	Name	Description
31 : 0	VALUE15	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

1.1.312 CM33_ETF_ITATBMCTR2

Integration Test ATB Master Interface Control 2 Register

Address: 0xE008DED4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE16 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE16 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE16 [31:24]							

Bits	Name	Description
31 : 0	VALUE16	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

1.1.313 CM33_ETF_ITATBMCTR1

Integration Test ATB Master Interface Control 1 Register

Address: 0xE008DED8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	VALUE17 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	VALUE17 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	VALUE17 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	VALUE17 [31:24]							

Bits	Name	Description
31 : 0	VALUE17	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

1.1.314 CM33_ETF_ITATBMCTR0

Integration Test ATB Master Interface Control 0 Registe

Address: 0xE008DEDC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	VALUE18 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	VALUE18 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	VALUE18 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	VALUE18 [31:24]							

Bits	Name	Description
31 : 0	VALUE18	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

1.1.315 CM33_ETF_ITEVTINTR

Integration Test Event & Interrupt Status Register

Address: 0xE008DEE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	VALUE19 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	VALUE19 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	VALUE19 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	VALUE19 [31:24]							

Bits	Name	Description
31 : 0	VALUE19	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

1.1.316 CM33_ETF_ITTRFLIN

Integration Test Trigger In and Flush In Register

Address: 0xE008DEE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE20 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE20 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE20 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE20 [31:24]							

Bits	Name	Description
31 : 0	VALUE20	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

1.1.317 CM33_ETF_ITATBDATA0

Integration Test ATB Data 0 Register

Address: 0xE008DEEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE21 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE21 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE21 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE21 [31:24]							

Bits	Name	Description
31 : 0	VALUE21	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

1.1.318 CM33_ETF_ITATBCTR2

Integration Test ATB Control 2 Register

Address: 0xE008DEF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	VALUE22 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	VALUE22 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	VALUE22 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	VALUE22 [31:24]							

Bits	Name	Description
31 : 0	VALUE22	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

1.1.319 CM33_ETF_ITATBCTR1

Integration Test ATB Control 1 Register

Address: 0xE008DEF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE23 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE23 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE23 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE23 [31:24]							

Bits	Name	Description
31 : 0	VALUE23	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

1.1.320 CM33_ETF_ITATBCTR0

Integration Test ATB Control 0 Register

Address: 0xE008DEF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE24 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE24 [31:24]							

Bits	Name	Description
31 : 0	VALUE24	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

1.1.321 CM33_ETF_ITCTRL

Integration Mode Control Register

Address: 0xE008DF00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE25 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE25 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE25 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE25 [31:24]							

Bits	Name	Description
31 : 0	VALUE25	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

1.1.322 CM33_ETF_CLAIMSET

Claim Tag Set Register

Address: 0xE008DFA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RAZWI				RW1S			
HW Access	R				R			
Name	VALUE26 [7:4]				TAG [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RAZWI							
HW Access	R							
Name	VALUE26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RAZWI							
HW Access	R							
Name	VALUE26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RAZWI							
HW Access	R							
Name	VALUE26 [31:24]							

Bits	Name	Description
31 : 4	VALUE26	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0
3 : 0	TAG	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0xF

1.1.323 CM33_ETF_CLAIMCLR

Claim Tag Clear Register

Address: 0xE008DFA4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RAZWI				RW1C			
HW Access	R				R			
Name	VALUE27 [7:4]				TAG [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RAZWI							
HW Access	R							
Name	VALUE27 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RAZWI							
HW Access	R							
Name	VALUE27 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RAZWI							
HW Access	R							
Name	VALUE27 [31:24]							

Bits	Name	Description
31 : 4	VALUE27	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0
3 : 0	TAG	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0

1.1.324 CM33_ETF_AUTHSTATUS

Authentication Status Register

Address: 0xE008DFB8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		R		R		R	
HW Access	W		W		W		W	
Name	SNIDBG [7:6]		SIDBG [5:4]		NSNIDBG [3:2]		NSIDBG [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R				R		R	
HW Access	R				W		W	
Name	RES0_1 [15:12]				HNIDBG [11:10]		HIDBG [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	RES0_1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	RES0_1 [31:24]							

Bits	Name	Description
31 : 12	RES0_1	RESERVED Default Value: 0
11 : 10	HNIDBG	Hypervisor non-invasive debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 0
9 : 8	HIDBG	Hypervisor invasive debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 0
7 : 6	SNIDBG	Secure Non-Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 0
5 : 4	SIDBG	Secure Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 0

1.1.324 CM33_ETF_AUTHSTATUS (continued)

3 : 2	NSNIDBG	Non-Secure Non-Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 0
1 : 0	NSIDBG	Non-Secure Invasive Debug 0: Functionality not implemented or controlled elsewhere 1: Functionality disabled 2: Reserved 3: Functionality enabled Default Value: 0

1.1.325 CM33_ETF_DEVID1

Device Configuration Register 1

Address: 0xE008DFC4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							R
HW Access	R							R
Name	RES0_2 [7:1]							RMC

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	RES0_2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	RES0_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	RES0_2 [31:24]							

Bits	Name	Description
31 : 1	RES0_2	RESERVED Default Value: 0
0	RMC	Registr Management mode Default Value: 1

1.1.326 CM33_ETF_DEVID

Device Configuration Register

Address: 0xE008DFC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		R	R				
HW Access	R		R	R				
Name	CONFIGTYPE [7:6]		CLKSCHEME	ATBINPORTCOUNT [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	R					R		
HW Access	R					R		
Name	RES0_3 [15:11]					MEMWIDTH [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	RES0_3 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	RES0_3 [31:24]							

Bits	Name	Description
31 : 11	RES0_3	RESERVED Default Value: 0
10 : 8	MEMWIDTH	This value is twice ATB_DATA_WIDTH. 0x3 Memory interface databus is 64-bits wide. (ATB_-DATA_WIDTH= 32bit) 0x4 Memory interface databus is 128-bits wide. (ATB_DATA_WIDTH= 64bit) 0x5 Memory interface databus is 256-bits wide. (ATB_DATA_WIDTH= 128bit) Default Value: 0
7 : 6	CONFIGTYPE	Returns 0x2, indicating ETF configuration Default Value: 0x2
5	CLKSCHEME	RAM Clocking Scheme. This value indicates the TMC RAM clocking scheme used, that is, whether the TMC RAM operates synchronously or asynchronously to the TMC clock. Fixed to 0 indicating that TMC RAM clock is synchronous to the clk input Default Value: 0
4 : 0	ATBINPORTCOUNT	Hidden Level of ATB input multiplexing. This value indicates the type/ number of ATB multiplexing present on the input ATB. Fixed to 0x00 indicating that no multiplexing is present. Default Value: 0

1.1.327 CM33_ETF_DEVTYPE

Device Type Identifier Register

Address: 0xE008DFCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	SUB_TYPE [7:4]				MAJOR [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	RES0_4 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	RES0_4 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	RES0_4 [31:24]							

Bits	Name	Description
31 : 8	RES0_4	Reserved Default Value: 0
7 : 4	SUB_TYPE	Minor classification. Returns 0x3, indicating this component is a FIFO Default Value: 0x3
3 : 0	MAJOR	Major classification. Returns 0x2, indicating this component is a Trace Link Default Value: 0x2

1.1.328 CM33_ETF_PIDR4

Peripheral Identification Register 4

Address: 0xE008DFD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE28 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE28 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE28 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE28 [31:24]							

Bits	Name	Description
31 : 0	VALUE28	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0x00000004

1.1.329 CM33_ETF_PIDR5

Peripheral Identification Register 5

Address: 0xE008DFD4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE29 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE29 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE29 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE29 [31:24]							

Bits	Name	Description
31 : 0	VALUE29	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0x00000000

1.1.330 CM33_ETF_PIDR6

Peripheral Identification Register 6

Address: 0xE008DFD8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE30 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE30 [31:24]							

Bits	Name	Description
31 : 0	VALUE30	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0x00000000

1.1.331 CM33_ETF_PIDR7

Peripheral Identification Register 7

Address: 0xE008DFDC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE31 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE31 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE31 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE31 [31:24]							

Bits	Name	Description
31 : 0	VALUE31	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0x00000000

1.1.332 CM33_ETF_PIDR0

Peripheral Identification Register 0

Address: 0xE008DFE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE32 [31:24]							

Bits	Name	Description
31 : 0	VALUE32	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0x000000EA

1.1.333 CM33_ETF_PIDR1

Peripheral Identification Register 1

Address: 0xE008DFE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE33 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE33 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE33 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE33 [31:24]							

Bits	Name	Description
31 : 0	VALUE33	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0x000000B9

1.1.334 CM33_ETF_PIDR2

Peripheral Identification Register 2

Address: 0xE008DFE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE34 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE34 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE34 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE34 [31:24]							

Bits	Name	Description
31 : 0	VALUE34	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0x0000004B

1.1.335 CM33_ETF_PIDR3

Peripheral Identification Register 3

Address: 0xE008DFEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None			
HW Access	R				None			
Name	ECOREVNUM [7:4]				None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	ECOREVNUM	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0x0

1.1.336 CM33_ETF_CIDR0

Component Identification Register 0

Address: 0xE008DFF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE35 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE35 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE35 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE35 [31:24]							

Bits	Name	Description
31 : 0	VALUE35	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0x000000D

1.1.337 CM33_ETF_CIDR1

Component Identification Register 1

Address: 0xE008DFF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE36 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE36 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE36 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE36 [31:24]							

Bits	Name	Description
31 : 0	VALUE36	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0x00000090

1.1.338 CM33_ETF_CIDR2

Component Identification Register 2

Address: 0xE008DFF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE37 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE37 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE37 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE37 [31:24]							

Bits	Name	Description
31 : 0	VALUE37	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0x00000005

1.1.339 CM33_ETF_CIDR3

Component Identification Register 3

Address: 0xE008DFFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE38 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE38 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE38 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE38 [31:24]							

Bits	Name	Description
31 : 0	VALUE38	Refer CoreSight TRM for details of register description https://developer.arm.com/documentation/100806/0401/Programmers-model/css600-tmc-etf-introduction/Register-descriptions Default Value: 0x000000B1

1.1.340 CM33_CSS600_TPIU_TPIU_SSPSR

Supported Parallel Port Size Register

Address: 0xE008E000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.213 TPIU_SSPSR, TPIU Supported Parallel Port Sizes Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: X

1.1.341 CM33_CSS600_TPIU_TPIU_CSPSR

Current Parallel Port Size Register

Address: 0xE008E004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.197 TPIU_CSPSR, TPIU Current Parallel Port Sizes Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x1

1.1.342 CM33_CSS600_TPIU_TPIU_STMR

Supported Trigger Model Register

Address: 0xE008E100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	0: MULT2 1: MULT4 2: MULT6 3: MULT256 4: MULT64K 7:5 : RES0 8: TCOUNT8 15:9: RES0 16: TRIGGERED 17: TrgRun 31:18: RES0 Default Value: 0x0000011F

1.1.343 CM33_CSS600_TPIU_TPIU_TCVR

Trigger Counter Value Register

Address: 0xE008E104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	7:0 : TrigCount 31:8 : RES0 Default Value: 0x00000000

1.1.344 CM33_CSS600_TPIU_TPIU_TCMR

Trigger Counter Multiplier Register

Address: 0xE008E108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	7:0 : TrigCount 31:8 : RES0 Default Value: 0x00000000

1.1.345 CM33_CSS600_TPIU_TPIU_STPMR

Supported Test Patterns Modes Register

Address: 0xE008E200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	0 : MULT2 1 : MULT4 2 : MULT16 3 : MULT256 4 : MULT64K 31:5 : RES0 Default Value: 0x00000000

1.1.346 CM33_CSS600_TPIU_TPIU_CTPMR

Current Test Patterns Modes Register

Address: 0xE008E204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	0 : PATW1 1 : PATW0 2 : PATA5 3 : PATAF0 15:4 :RES0 16 : PTIMEEN 17 : PCONTEN 31:18 : RES0 Default Value: 0x00000000

1.1.347 CM33_CSS600_TPIU_TPIU_TPRCR

Test Pattern Repeat Counter Register

Address: 0xE008E208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

1.1.348 CM33_CSS600_TPIU_TPIU_FFSR

Formatter and Flush Status Register

Address: 0xE008E300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.200 TPIU_FFSR, TPIU Formatter and Flush Status Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: X

1.1.349 CM33_CSS600_TPIU_TPIU_FFCR

Formatter and Flush Control Register

Address: 0xE008E304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.199 TPIU_FFCR, TPIU Formatter and Flush Control Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00001000

1.1.350 CM33_CSS600_TPIU_TPIU_FSCR

Formatter Synchronization Count Register

Address: 0xE008E308

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.211 TPIU_PSCR, TPIU Periodic Synchronization Control Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00000040

1.1.351 CM33_CSS600_TPIU_TPIU_EXTCTLIN

External Control Port In Register

Address: 0xE008E400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x000000XX

1.1.352 CM33_CSS600_TPIU_TPIU_EXTCTLOUT

External Control Port Out Register

Address: 0xE008E404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

1.1.353 CM33_CSS600_TPIU_ITTRFLIN

Integration Test Trigger In Flush In Register

Address: 0xE008EEE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0

1.1.354 CM33_CSS600_TPIU_ITATBDATA0

Integration Test ATB Data Register0

Address: 0xE008EEEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	VALUE0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	VALUE0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	VALUE0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	VALUE0	Default Value: 0

1.1.355 CM33_CSS600_TPIU_ITATBCTR2

Integration Test ATB Control Register 2

Address: 0xE008EEF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0

1.1.356 CM33_CSS600_TPIU_ITATBCTR1

Integration Test ATB Control Register 1

Address: 0xE008EEF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0

1.1.357 CM33_CSS600_TPIU_ITATBCTR0

Integration Test ATB Control Register 0

Address: 0xE008EEF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0

1.1.358 CM33_CSS600_TPIU_ITOUTCTR

Integration Test Output Control Register

Address: 0xE008EEFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0

1.1.359 CM33_CSS600_TPIU_ITCTRL

Integration Mode Control Register

Address: 0xE008EF00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	MODE	Specifies the current mode for the TPIU: 0b00 Normal mode. 0b01 Integration test mode. 0b10 Integration data test mode. 0b11 Reserved. In integration data test mode, the trace output is disabled, and data can be read directly from each input port using the integration data registers. Default Value: 0

1.1.360 CM33_CSS600_TPIU_CLAIMSET

Claim Tag Set Register

Address: 0xE008EFA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S			
HW Access	None				R			
Name	None [7:4]				TAG [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	TAG	A bit programmable register bank which sets the Claim Tag Value. A read will return a logic 1 for all implemented locations. Default Value: 0xF

1.1.361 CM33_CSS600_TPIU_CLAIMCLR

Claim Tag Clear Register

Address: 0xE008EFA4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C			
HW Access	None				R			
Name	None [7:4]				TAG [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	TAG	A bit programmable register bank that is zero at reset Default Value: 0

1.1.362 CM33_CSS600_TPIU_AUTHSTATUS

Authentication Status Register

Address: 0xE008EFB8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				TAG [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	TAG	Default Value: 0

1.1.363 CM33_CSS600_TPIU_DEVARCH

Device Architecture Register

Address: 0xE008EFBC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				TAG [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	TAG	Default Value: 0

1.1.364 CM33_CSS600_TPIU_DEVID

Device ID

Address: 0xE008EFC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "B.3.10 Device Configuration Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00000020

1.1.365 CM33_CSS600_TPIU_DEVTYPE

Device Type Identifier Register

Address: 0xE008EFCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "B.3.11 Device Type Identifier Register" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x11

1.1.366 CM33_CSS600_TPIU_PIDR4

Peripheral Identification Register 4

Address: 0xE008EFD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.207 TPIU_PIDR4, TPIU Peripheral Identification Register 4" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00000004

1.1.367 CM33_CSS600_TPIU_PIDR5

Peripheral Identification Register 5

Address: 0xE008EFD4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.208 TPIU_PIDR5, TPIU Peripheral Identification Register 5" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00000000

1.1.368 CM33_CSS600_TPIU_PIDR6

Peripheral Identification Register 6

Address: 0xE008EFD8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Default Value: 0x00000000

1.1.369 CM33_CSS600_TPIU_PIDR7

Peripheral Identification Register 7

Address: 0xE008EFDC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.210 TPIU_PIDR7, TPIU Peripheral Identification Register 7" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00000000

1.1.370 CM33_CSS600_TPIU_PIDR0

Peripheral Identification Register 0

Address: 0xE008EFE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.203 TPIU_PIDR0, TPIU Peripheral Identification Register 0" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x000000E7

1.1.371 CM33_CSS600_TPIU_PIDR1

Peripheral Identification Register 1

Address: 0xE008EFE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.204 TPIU_PIDR1, TPIU Peripheral Identification Register 1" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00000089

1.1.372 CM33_CSS600_TPIU_PIDR2

Peripheral Identification Register 2

Address: 0xE008EFE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.205 TPIU_PIDR2, TPIU Peripheral Identification Register 2" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x0000002B

1.1.373 CM33_CSS600_TPIU_PIDR3

Peripheral Identification Register 3

Address: 0xE008EFEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None			
HW Access	R				None			
Name	ECOREVNUM [7:4]				None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	ECOREVNUM	Refer "D2.2.206 TPIU_PIDR3, TPIU Peripheral Identification Register 3" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00000000

1.1.374 CM33_CSS600_TPIU_CIDR0

Component Identification Register 0

Address: 0xE008EFF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.206 TPIU_PIDR3, TPIU Peripheral Identification Register 3" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x0000008D

1.1.375 CM33_CSS600_TPIU_CIDR1

Component Identification Register 1

Address: 0xE008EFF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.206 TPIU_PIDR3, TPIU Peripheral Identification Register 3" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00000090

1.1.376 CM33_CSS600_TPIU_CIDR2

Component Identification Register 2

Address: 0xE008EFF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.195 TPIU_CIDR2, TPIU Component Identification Register 2" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x00000005

1.1.377 CM33_CSS600_TPIU_CIDR3

Component Identification Register 3

Address: 0xE008EFFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Refer "D2.2.196 TPIU_CIDR3, TPIU Component Identification Register 3" in ARMv8-M architecture spec: https://developer.arm.com/documentation/ddi0553/latest/ Default Value: 0x000000B1

1.1.378 SYSAP_ROMTABLE_DID

Device Type Identifier register.

Address: 0xE00BEFCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Identifies the classification of the debug component. Default Value: 0x00000001

1.1.379 SYSAP_ROMTABLE_PID4

Peripheral Identification Register 4.

Address: 0xE00BEFD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	COUNT [7:4]				JEP_CONTINUATION [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	COUNT	Size of ROM Table is 2^COUNT * 4 KByte. Default Value: 0
3 : 0	JEP_CONTINUATION	JEP106 continuation code. This value is product specific and specified as part of the product definition in the CPUSS.JEPCONTINUATION parameter. Default Value: Undefined

1.1.380 SYSAP_ROMTABLE_PID5

Peripheral Identification Register 5.

Address: 0xE00BEFD4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Reserved Default Value: 0

1.1.381 SYSAP_ROMTABLE_PID6

Peripheral Identification Register 6.

Address: 0xE00BEFD8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Reserved Default Value: 0

1.1.382 SYSAP_ROMTABLE_PID7

Peripheral Identification Register 7.

Address: 0xE00BEFDC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Reserved Default Value: 0

1.1.383 SYSAP_ROMTABLE_PID0

Peripheral Identification Register 0.

Address: 0xE00BEFE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	PN_MIN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	PN_MIN	JEP106 part number. 4 lsbs of CPUSS.PARTNUMBER parameter. Default Value: Undefined

1.1.384 SYSAP_ROMTABLE_PID1

Peripheral Identification Register 1.

Address: 0xE00BEFE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	JEPID_MIN [7:4]				PN_MAJ [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	JEPID_MIN	JEP106 vendor id. 4 lsbs of CPUSS.JEPID parameter. Default Value: Undefined
3 : 0	PN_MAJ	JEP106 part number. 4 msbs of CPUSS.PARTNUMBER parameter. Default Value: Undefined

1.1.385 SYSAP_ROMTABLE_PID2

Peripheral Identification Register 2.

Address: 0xE00BEFE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None	R		
HW Access	R				None	R		
Name	REV [7:4]				None	JEPID_MAJ [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	REV	Major REVision number (chip specific). Identifies the design iteration of the component. For first tape out: 0x1. This field is incremented on subsequent tape outs. Default Value: Undefined
2 : 0	JEPID_MAJ	JEP106 vendor id. 4 msbs of CPUSS.JEPID parameter. Default Value: Undefined

1.1.386 SYSAP_ROMTABLE_PID3

Peripheral Identification Register 3.

Address: 0xE00BEFEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	REV_AND [7:4]				CM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	REV_AND	Minor REVision number (chip specific). For first tape out: 0x1. This field is incremented on subsequent tape outs. Default Value: Undefined
3 : 0	CM	Customer modified field. This field is used to track modifications to the original component design as a result of component IP reuse. Default Value: 0

1.1.387 SYSAP_ROMTABLE_CID0

Component Identification Register 0.

Address: 0xE00BEFF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 0 of 4-byte component identification 0xB105:100D. Default Value: 0x0000000D

1.1.388 SYSAP_ROMTABLE_CID1

Component Identification Register 1.

Address: 0xE00BEFF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 1 of 4-byte component identification 0xB105:100D. Component class: "ROM Table". Default Value: 0x00000010

1.1.389 SYSAP_ROMTABLE_CID2

Component Identification Register 2.

Address: 0xE00BEFF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 2 of 4-byte component identification 0xB105:100D. Default Value: 0x00000005

1.1.390 SYSAP_ROMTABLE_CID3

Component Identification Register 3.

Address: 0xE00BEFFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 3 of 4-byte component identification 0xB105:100D. Default Value: 0x000000B1

1.1.391 CM33_ROMTABLE_TRC_CTI

CM33 CoreSight ROM Table Peripheral #0

Address: 0xE00BF000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to TRC_CTI component Default Value: 0xFFFC1003

1.1.392 CM33_ROMTABLE_TRC_TPIU

CM33 CoreSight ROM Table Peripheral #3

Address: 0xE00BF004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to TPIU component. For the products that doesn't have TPIU, this field reads as 0xfffcf002. Default Value: 0xFFFCF003

1.1.393 CM33_ROMTABLE_TRC_CSS600_ATBFUNNEL_CSTF

CM33 CoreSight ROM Table Peripheral #5

Address: 0xE00BF008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to CSS600_ATBFUNNEL_CSTF component Default Value: 0xFFFC9003

1.1.394 CM33_ROMTABLE_TRC_ETF

CM33 CoreSight ROM Table Peripheral #2

Address: 0xE00BF00C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to ETF component. Note that this entry is present only for the products which has ETF. For the products that has no ETF, this field read as 0xfffce002. Default Value: 0xFFFCE003

1.1.395 CM33_ROMTABLE_CM33

CM33 CoreSight ROM Table Peripheral #6

Address: 0xE00BF010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to CM33_0 internal ROM Table (i.e. CM33_ROM) Default Value: 0x00040003

1.1.396 CM33_ROMTABLE_CSMT

CM33 CoreSight ROM Table Memory Type

Address: 0xE00BFFCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Memory Type Default Value: 1

1.1.397 CM33_ROMTABLE_PID4

CM33 CoreSight ROM Table Peripheral ID #4

Address: 0xE00BFFD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 0x00000004

1.1.398 CM33_ROMTABLE_PID0

CM33 CoreSight ROM Table Peripheral ID #0

Address: 0xE00BFFE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 0x000000C0

1.1.399 CM33_ROMTABLE_PID1

CM33 CoreSight ROM Table Peripheral ID #1

Address: 0xE00BFFE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 0x000000B4

1.1.400 CM33_ROMTABLE_PID2

CM33 CoreSight ROM Table Peripheral ID #2

Address: 0xE00BFFE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 0x0000000B

1.1.401 CM33_ROMTABLE_PID3

CM33 CoreSight ROM Table Peripheral ID #3

Address: 0xE00BFFEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0

1.1.402 CM33_ROMTABLE_CID0

CM33 CoreSight ROM Table Component ID #0

Address: 0xE00BFFF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 0x0000000D

1.1.403 CM33_ROMTABLE_CID1

CM33 CoreSight ROM Table Component ID #1

Address: 0xE00BFFF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 0x00000010

1.1.404 CM33_ROMTABLE_CID2

CM33 CoreSight ROM Table Component ID #2

Address: 0xE00BFFF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 0x00000005

1.1.405 CM33_ROMTABLE_CID3

CM33 CoreSight ROM Table Component ID #3

Address: 0xE00BFFFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 0x000000B1

1.1.406 CM33_ROM_SCS

CM33 CoreSight ROM Table Peripheral #0

Address: 0xE00FF000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to SCS ROM Table Default Value: 0xFFF0F003

1.1.407 CM33_ROM_DWT

CM33 CoreSight ROM Table Peripheral #1

Address: 0xE00FF004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to DWT ROM Table. Reads as 0xfff02002 if DWT is not present in system. Default Value: 0xFFF02003

1.1.408 CM33_ROM_FPB

CM33 CoreSight ROM Table Peripheral #2

Address: 0xE00FF008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to BPU ROM Table. Reads as 0xfff03002 if BPU is not present. Default Value: 0xFFF03003

1.1.409 CM33_ROM_ITM

CM33 CoreSight ROM Table Peripheral #3

Address: 0xE00FF00C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to ITM ROM Table. Reads as 0xfff01002 if ITM is not present. Default Value: 0xFFF01003

1.1.410 CM33_ROM_ETM

CM33 CoreSight ROM Table Peripheral #4

Address: 0xE00FF014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to ETM ROM Table. Reads as 0xfff42002 if ETM is not present. Default Value: 0xFFF42003

1.1.411 CM33_ROM_CTI

CM33 CoreSight ROM Table Peripheral #5

Address: 0xE00FF018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to CTI ROM Table. Reads as 0xfff43002 if CTI is not present. Default Value: 0xFFF43003

1.1.412 CM33_ROM_MTB

CM33 CoreSight ROM Table Peripheral #6

Address: 0xE00FF01C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to MTB ROM Table. Reads as 0xfff42002 if MTB is not present. Default Value: 0xFFF44002

1.1.413 CM33_ROM_CSMT

CM33 CoreSight ROM Table Memory Type

Address: 0xE00FFFCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Memory Type Default Value: 1

1.1.414 CM33_ROM_PID4

CM33 CoreSight ROM Table Peripheral ID #4

Address: 0xE00FFFD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 0x00000004

1.1.415 CM33_ROM_PID0

CM33 CoreSight ROM Table Peripheral ID #0

Address: 0xE00FFFE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 0x000000C0

1.1.416 CM33_ROM_PID1

CM33 CoreSight ROM Table Peripheral ID #1

Address: 0xE00FFFE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 0x000000B4

1.1.417 CM33_ROM_PID2

CM33 CoreSight ROM Table Peripheral ID #2

Address: 0xE00FFFE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 0x0000000B

1.1.418 CM33_ROM_PID3

CM33 CoreSight ROM Table Peripheral ID #3

Address: 0xE00FFFEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0

1.1.419 CM33_ROM_CID0

CM33 CoreSight ROM Table Component ID #0

Address: 0xE00FFFF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 0x0000000D

1.1.420 CM33_ROM_CID1

CM33 CoreSight ROM Table Component ID #1

Address: 0xE00FFFF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 0x00000010

1.1.421 CM33_ROM_CID2

CM33 CoreSight ROM Table Component ID #2

Address: 0xE00FFFF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 0x00000005

1.1.422 CM33_ROM_CID3

CM33 CoreSight ROM Table Component ID #3

Address: 0xE00FFFFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 0x000000B1

2 Inter Processor Communication (IPC) registers

This section discusses the IPC registers. It lists all the registers in mapping tables, in address order.

2.1 Register details

Register	Address	Description
IPC_STRUCT0_ACQUIRE	0x421D0000	IPC acquire
IPC_STRUCT0_RELEASE	0x421D0004	IPC release
IPC_STRUCT0_NOTIFY	0x421D0008	IPC notification
IPC_STRUCT0_DATA0	0x421D000C	IPC data 0
IPC_STRUCT0_DATA1	0x421D0010	IPC data 1
IPC_STRUCT0_LOCK_STATUS	0x421D001C	IPC lock status
IPC_STRUCT1_ACQUIRE	0x421D0020	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT1_RELEASE	0x421D0024	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT1_NOTIFY	0x421D0028	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT1_DATA0	0x421D002C	IPC data 0. See IPC_STRUCT0_DATA0 for the details of bit fields.
IPC_STRUCT1_DATA1	0x421D0030	IPC data 1. See IPC_STRUCT0_DATA1 for the details of bit fields.
IPC_STRUCT1_LOCK_STATUS	0x421D003C	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT2_ACQUIRE	0x421D0040	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT2_RELEASE	0x421D0044	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT2_NOTIFY	0x421D0048	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT2_DATA0	0x421D004C	IPC data 0. See IPC_STRUCT0_DATA0 for the details of bit fields.
IPC_STRUCT2_DATA1	0x421D0050	IPC data 1. See IPC_STRUCT0_DATA1 for the details of bit fields.
IPC_STRUCT2_LOCK_STATUS	0x421D005C	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT3_ACQUIRE	0x421D0060	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.

Inter Processor Communication (IPC) registers

Register	Address	Description
IPC_STRUCT3_RELEASE	0x421D0064	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT3_NOTIFY	0x421D0068	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT3_DATA0	0x421D006C	IPC data 0. See IPC_STRUCT0_DATA0 for the details of bit fields.
IPC_STRUCT3_DATA1	0x421D0070	IPC data 1. See IPC_STRUCT0_DATA1 for the details of bit fields.
IPC_STRUCT3_LOCK_STATUS	0x421D007C	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_INTR_STRUCT0_INTR	0x421D1000	Interrupt
IPC_INTR_STRUCT0_INTR_SET	0x421D1004	Interrupt set
IPC_INTR_STRUCT0_INTR_MASK	0x421D1008	Interrupt mask
IPC_INTR_STRUCT0_INTR_MASKED	0x421D100C	Interrupt masked
IPC_INTR_STRUCT1_INTR	0x421D1020	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT1_INTR_SET	0x421D1024	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT1_INTR_MASK	0x421D1028	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT1_INTR_MASKED	0x421D102C	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.

2.1.1 IPC_STRUCT0_ACQUIRE

IPC acquire

Address: 0x421D0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None		R	R
HW Access	W				None		W	W
Name	PC [7:4]				None [3:2]		NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	None		R					
HW Access	None		W					
Name	None [15:14]		MS [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	SUCCESS	None [30:24]						

Bits	Name	Description
31	SUCCESS	Specifies if the lock is successfully acquired or not (reading the ACQUIRE register can have affect on SUCCESS and LOCK_STATUS.ACQUIRED): '0': Not successfully acquired; i.e. the lock was already acquired by another read transaction and not released. The P, NS, PC and MS fields reflect the access attributes of the transaction that previously successfully acuired the lock; the fields are NOT affected by the current access. '1': Successfully acquired. The P, NS, PC and MS fields reflect the access attributes of the current access. Note that this field is NOT SW writable. A lock is released by writing to the associated RELEASE register (irrespective of the write value). Default Value: 0
13 : 8	MS	This field specifies the bus master identifier that successfully acquired the lock. Default Value: Undefined
7 : 4	PC	This field specifies the protection context that successfully acquired the lock. Default Value: Undefined
1	NS	Secure/non-secure access control: '0': secure. '1': non-secure. This field is set with the secure/non-secure access control of the access that successfully acquired the lock. Default Value: Undefined
0	P	User/privileged access control: '0': user mode. '1': privileged mode. This field is set with the user/privileged access control of the access that successfully acquired the lock. Default Value: Undefined

2.1.2 IPC_STRUCT0_RELEASE

IPC release

Address: 0x421D0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						W	
HW Access	None							
Name	None [7:2]						INTR_RELEASE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	INTR_RELEASE	Writing this field releases a lock and allows for the generation of release events to the IPC interrupt structures, but only when the lock is acquired (LOCK_STATUS.ACQUIRED is '1'). The IPC release cause fields associated with this IPC structure are set to '1', but only for those IPC interrupt structures for which the corresponding bit field in INTR_RELEASE[] is set to '1'. SW writes a '1' to the bit fields to generate a release event. Due to the transient nature of this event, SW always reads a '0' from this field. Default Value: 0

2.1.3 IPC_STRUCT0_NOTIFY

IPC notification

Address: 0x421D0008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						W	
HW Access	None							
Name	None [7:2]						INTR_NOTIFY [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	INTR_NOTIFY	This field allows for the generation of notification events to the IPC interrupt structures. The IPC notification cause fields associated with this IPC structure are set to '1', but only for those IPC interrupt structures for which the corresponding bit field in INTR_NOTIFY[] is set to '1'. SW writes a '1' to the bit fields to generate a notify event. Due to the transient nature of this event, SW always reads a '0' from this field. Default Value: 0

2.1.4 IPC_STRUCT0_DATA0

IPC data 0

Address: 0x421D000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	This field holds a 32-bit data element that is associated with the IPC structure. Default Value: Undefined

2.1.5 IPC_STRUCT0_DATA1

IPC data 1

Address: 0x421D0010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	This field holds a 32-bit data element that is associated with the IPC structure. Default Value: Undefined

2.1.6 IPC_STRUCT0_LOCK_STATUS

IPC lock status

Address: 0x421D001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None		R	R
HW Access	W				None		W	W
Name	PC [7:4]				None [3:2]		NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	MS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	ACQUIRED	None [30:24]						

Bits	Name	Description
31	ACQUIRED	Specifies if the lock is acquired. This field is set to '1', if a ACQUIRE read transfer successfully acquires the lock (the ACQUIRE read transfer returns ACQUIRE.SUCCESS as '1'). If zero, P, NS, PC, and MS are not valid. Default Value: 0
15 : 8	MS	This field specifies the bus master identifier that successfully acquired the lock. Default Value: Undefined
7 : 4	PC	This field specifies the protection context that successfully acquired the lock. Default Value: Undefined
1	NS	This field specifies the secure/non-secure access control: '0': secure. '1': non-secure. Default Value: Undefined
0	P	This field specifies the user/privileged access control: '0': user mode. '1': privileged mode. Default Value: Undefined

2.1.7 IPC_INTR_STRUCT0_INTR

Interrupt

Address: 0x421D1000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C			
HW Access	None				RW1S			
Name	None [7:4]				RELEASE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW1C			
HW Access	None				RW1S			
Name	None [23:20]				NOTIFY [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	NOTIFY	These interrupt cause fields are activated (HW sets the field to '1') when a IPC notification event is detected. One bit field for each master. SW writes a '1' to these field to clear the interrupt cause. Default Value: 0
3 : 0	RELEASE	These interrupt cause fields are activated (HW sets the field to '1') when a IPC release event is detected. One bit field for each master. SW writes a '1' to these field to clear the interrupt cause. Default Value: 0

2.1.8 IPC_INTR_STRUCT0_INTR_SET

Interrupt set

Address: 0x421D1004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S			
HW Access	None				A			
Name	None [7:4]				RELEASE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW1S			
HW Access	None				A			
Name	None [23:20]				NOTIFY [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	NOTIFY	SW writes a '1' to this field to set the corresponding field in the INTR register. Default Value: 0
3 : 0	RELEASE	SW writes a '1' to this field to set the corresponding field in the INTR register. Default Value: 0

2.1.9 IPC_INTR_STRUCT0_INTR_MASK

Interrupt mask

Address: 0x421D1008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				RELEASE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				NOTIFY [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	NOTIFY	Mask bit for corresponding field in the INTR register. Default Value: 0
3 : 0	RELEASE	Mask bit for corresponding field in the INTR register. Default Value: 0

2.1.10 IPC_INTR_STRUCT0_INTR_MASKED

Interrupt masked

Address: 0x421D100C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				RELEASE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				NOTIFY [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	NOTIFY	Logical and of corresponding INTR and INTR_MASK fields. Default Value: 0
3 : 0	RELEASE	Logical and of corresponding request and mask bits. Default Value: 0

3 Direct Memory Access (DMA) registers

This section discusses the DMA registers. It lists all the registers in mapping tables, in address order.

3.1 Register details

Register	Address	Description
DW0_CTL	0x42180000	Control
DW0_STATUS	0x42180004	Status
DW0_ACT_DESCR_CTL	0x42180020	Active descriptor control
DW0_ACT_DESCR_SRC	0x42180024	Active descriptor source
DW0_ACT_DESCR_DST	0x42180028	Active descriptor destination
DW0_ACT_DESCR_X_CTL	0x42180030	Active descriptor X loop control
DW0_ACT_DESCR_Y_CTL	0x42180034	Active descriptor Y loop control
DW0_ACT_DESCR_NEXT_PTR	0x42180038	Active descriptor next pointer
DW0_ACT_SRC	0x42180040	Active source
DW0_ACT_DST	0x42180044	Active destination
DW0_CRC_CTL	0x42180100	CRC control
DW0_CRC_DATA_CTL	0x42180110	CRC data control
DW0_CRC_POL_CTL	0x42180120	CRC polynomial control
DW0_CRC_LFSR_CTL	0x42180130	CRC LFSR control
DW0_CRC_REM_CTL	0x42180140	CRC remainder control
DW0_CRC_REM_RESULT	0x42180148	CRC remainder result
DW0_CH_STRUCT0_CH_CTL	0x42188000	Channel control
DW0_CH_STRUCT0_CH_STATUS	0x42188004	Channel status
DW0_CH_STRUCT0_CH_IDX	0x42188008	Channel current indices
DW0_CH_STRUCT0_CH_CURR_PTR	0x4218800C	Channel current descriptor pointer
DW0_CH_STRUCT0_INTR	0x42188010	Interrupt
DW0_CH_STRUCT0_INTR_SET	0x42188014	Interrupt set
DW0_CH_STRUCT0_INTR_MASK	0x42188018	Interrupt mask
DW0_CH_STRUCT0_INTR_MASKED	0x4218801C	Interrupt masked
DW0_CH_STRUCT0_TR_CMD	0x42188028	Channel software trigger
DW0_CH_STRUCT1_CH_CTL	0x42188040	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT1_CH_STATUS	0x42188044	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT1_CH_IDX	0x42188048	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.

Direct Memory Access (DMA) registers

Register	Address	Description
DW0_CH_STRUCT1_CH_CURR_PTR	0x4218804C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT1_INTR	0x42188050	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT1_INTR_SET	0x42188054	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT1_INTR_MASK	0x42188058	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT1_INTR_MASKED	0x4218805C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT1_TR_CMD	0x42188068	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT2_CH_CTL	0x42188080	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT2_CH_STATUS	0x42188084	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT2_CH_IDX	0x42188088	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT2_CH_CURR_PTR	0x4218808C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT2_INTR	0x42188090	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT2_INTR_SET	0x42188094	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT2_INTR_MASK	0x42188098	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT2_INTR_MASKED	0x4218809C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT2_TR_CMD	0x421880A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT3_CH_CTL	0x421880C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT3_CH_STATUS	0x421880C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT3_CH_IDX	0x421880C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.

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Register	Address	Description
DW0_CH_STRUCT3_CH_CURR_PTR	0x421880CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT3_INTR	0x421880D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT3_INTR_SET	0x421880D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT3_INTR_MASK	0x421880D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT3_INTR_MASKED	0x421880DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT3_TR_CMD	0x421880E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT4_CH_CTL	0x42188100	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT4_CH_STATUS	0x42188104	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT4_CH_IDX	0x42188108	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT4_CH_CURR_PTR	0x4218810C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT4_INTR	0x42188110	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT4_INTR_SET	0x42188114	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT4_INTR_MASK	0x42188118	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT4_INTR_MASKED	0x4218811C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT4_TR_CMD	0x42188128	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT5_CH_CTL	0x42188140	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT5_CH_STATUS	0x42188144	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT5_CH_IDX	0x42188148	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.

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Register	Address	Description
DW0_CH_STRUCT5_CH_CURR_PTR	0x4218814C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT5_INTR	0x42188150	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT5_INTR_SET	0x42188154	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT5_INTR_MASK	0x42188158	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT5_INTR_MASKED	0x4218815C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT5_TR_CMD	0x42188168	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT6_CH_CTL	0x42188180	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT6_CH_STATUS	0x42188184	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT6_CH_IDX	0x42188188	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT6_CH_CURR_PTR	0x4218818C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT6_INTR	0x42188190	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT6_INTR_SET	0x42188194	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT6_INTR_MASK	0x42188198	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT6_INTR_MASKED	0x4218819C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT6_TR_CMD	0x421881A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT7_CH_CTL	0x421881C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT7_CH_STATUS	0x421881C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT7_CH_IDX	0x421881C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.

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Register	Address	Description
DW0_CH_STRUCT7_CH_CURR_PTR	0x421881CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT7_INTR	0x421881D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT7_INTR_SET	0x421881D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT7_INTR_MASK	0x421881D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT7_INTR_MASKED	0x421881DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT7_TR_CMD	0x421881E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT8_CH_CTL	0x42188200	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT8_CH_STATUS	0x42188204	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT8_CH_IDX	0x42188208	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT8_CH_CURR_PTR	0x4218820C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT8_INTR	0x42188210	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT8_INTR_SET	0x42188214	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT8_INTR_MASK	0x42188218	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT8_INTR_MASKED	0x4218821C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT8_TR_CMD	0x42188228	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT9_CH_CTL	0x42188240	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT9_CH_STATUS	0x42188244	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT9_CH_IDX	0x42188248	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.

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Register	Address	Description
DW0_CH_STRUCT9_CH_CURR_PTR	0x4218824C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT9_INTR	0x42188250	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT9_INTR_SET	0x42188254	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT9_INTR_MASK	0x42188258	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT9_INTR_MASKED	0x4218825C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT9_TR_CMD	0x42188268	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT10_CH_CTL	0x42188280	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT10_CH_STATUS	0x42188284	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT10_CH_IDX	0x42188288	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT10_CH_CURR_PTR	0x4218828C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT10_INTR	0x42188290	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT10_INTR_SET	0x42188294	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT10_INTR_MASK	0x42188298	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT10_INTR_MASKED	0x4218829C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT10_TR_CMD	0x421882A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT11_CH_CTL	0x421882C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT11_CH_STATUS	0x421882C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT11_CH_IDX	0x421882C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.

Direct Memory Access (DMA) registers

Register	Address	Description
DW0_CH_STRUCT11_CH_CURR_PTR	0x421882CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT11_INTR	0x421882D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT11_INTR_SET	0x421882D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT11_INTR_MASK	0x421882D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT11_INTR_MASKED	0x421882DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT11_TR_CMD	0x421882E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT12_CH_CTL	0x42188300	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT12_CH_STATUS	0x42188304	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT12_CH_IDX	0x42188308	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT12_CH_CURR_PTR	0x4218830C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT12_INTR	0x42188310	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT12_INTR_SET	0x42188314	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT12_INTR_MASK	0x42188318	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT12_INTR_MASKED	0x4218831C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT12_TR_CMD	0x42188328	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT13_CH_CTL	0x42188340	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT13_CH_STATUS	0x42188344	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT13_CH_IDX	0x42188348	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.

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Register	Address	Description
DW0_CH_STRUCT13_CH_CURR_PTR	0x4218834C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT13_INTR	0x42188350	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT13_INTR_SET	0x42188354	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT13_INTR_MASK	0x42188358	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT13_INTR_MASKED	0x4218835C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT13_TR_CMD	0x42188368	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT14_CH_CTL	0x42188380	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT14_CH_STATUS	0x42188384	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT14_CH_IDX	0x42188388	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT14_CH_CURR_PTR	0x4218838C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT14_INTR	0x42188390	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT14_INTR_SET	0x42188394	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT14_INTR_MASK	0x42188398	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT14_INTR_MASKED	0x4218839C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT14_TR_CMD	0x421883A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW0_CH_STRUCT15_CH_CTL	0x421883C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT15_CH_STATUS	0x421883C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT15_CH_IDX	0x421883C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.

Register	Address	Description
DW0_CH_STRUCT15_CH_CURR_PTR	0x421883CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT15_INTR	0x421883D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT15_INTR_SET	0x421883D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT15_INTR_MASK	0x421883D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT15_INTR_MASKED	0x421883DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT15_TR_CMD	0x421883E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CTL	0x42190000	Control. See DW0_CTL for the details of bit fields.
DW1_STATUS	0x42190004	Status. See DW0_STATUS for the details of bit fields.
DW1_ACT_DESCR_CTL	0x42190020	Active descriptor control. See DW0_ACT_DESCR_CTL for the details of bit fields.
DW1_ACT_DESCR_SRC	0x42190024	Active descriptor source. See DW0_ACT_DESCR_SRC for the details of bit fields.
DW1_ACT_DESCR_DST	0x42190028	Active descriptor destination. See DW0_ACT_DESCR_DST for the details of bit fields.
DW1_ACT_DESCR_X_CTL	0x42190030	Active descriptor X loop control. See DW0_ACT_DESCR_X_CTL for the details of bit fields.
DW1_ACT_DESCR_Y_CTL	0x42190034	Active descriptor Y loop control. See DW0_ACT_DESCR_Y_CTL for the details of bit fields.
DW1_ACT_DESCR_NEXT_PTR	0x42190038	Active descriptor next pointer. See DW0_ACT_DESCR_NEXT_PTR for the details of bit fields.
DW1_ACT_SRC	0x42190040	Active source. See DW0_ACT_SRC for the details of bit fields.
DW1_ACT_DST	0x42190044	Active destination. See DW0_ACT_DST for the details of bit fields.
DW1_CRC_CTL	0x42190100	CRC control. See DW0_CRC_CTL for the details of bit fields.
DW1_CRC_DATA_CTL	0x42190110	CRC data control. See DW0_CRC_DATA_CTL for the details of bit fields.
DW1_CRC_POL_CTL	0x42190120	CRC polynomial control. See DW0_CRC_POL_CTL for the details of bit fields.
DW1_CRC_LFSR_CTL	0x42190130	CRC LFSR control. See DW0_CRC_LFSR_CTL for the details of bit fields.

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Register	Address	Description
DW1_CRC_REM_CTL	0x42190140	CRC remainder control. See DW0_CRC_REM_CTL for the details of bit fields.
DW1_CRC_REM_RESULT	0x42190148	CRC remainder result. See DW0_CRC_REM_RESULT for the details of bit fields.
DW1_CH_STRUCT0_CH_CTL	0x42198000	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT0_CH_STATUS	0x42198004	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT0_CH_IDX	0x42198008	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT0_CH_CURR_PTR	0x4219800C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT0_INTR	0x42198010	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT0_INTR_SET	0x42198014	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT0_INTR_MASK	0x42198018	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT0_INTR_MASKED	0x4219801C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT0_TR_CMD	0x42198028	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT1_CH_CTL	0x42198040	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT1_CH_STATUS	0x42198044	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT1_CH_IDX	0x42198048	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT1_CH_CURR_PTR	0x4219804C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT1_INTR	0x42198050	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT1_INTR_SET	0x42198054	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT1_INTR_MASK	0x42198058	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.

Register	Address	Description
DW1_CH_STRUCT1_INTR_MASKED	0x4219805C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT1_TR_CMD	0x42198068	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT2_CH_CTL	0x42198080	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT2_CH_STATUS	0x42198084	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT2_CH_IDX	0x42198088	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT2_CH_CURR_PTR	0x4219808C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT2_INTR	0x42198090	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT2_INTR_SET	0x42198094	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT2_INTR_MASK	0x42198098	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT2_INTR_MASKED	0x4219809C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT2_TR_CMD	0x421980A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT3_CH_CTL	0x421980C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT3_CH_STATUS	0x421980C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT3_CH_IDX	0x421980C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT3_CH_CURR_PTR	0x421980CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT3_INTR	0x421980D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT3_INTR_SET	0x421980D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT3_INTR_MASK	0x421980D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.

Direct Memory Access (DMA) registers

Register	Address	Description
DW1_CH_STRUCT3_INTR_MASKED	0x421980DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT3_TR_CMD	0x421980E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT4_CH_CTL	0x42198100	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT4_CH_STATUS	0x42198104	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT4_CH_IDX	0x42198108	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT4_CH_CURR_PTR	0x4219810C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT4_INTR	0x42198110	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT4_INTR_SET	0x42198114	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT4_INTR_MASK	0x42198118	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT4_INTR_MASKED	0x4219811C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT4_TR_CMD	0x42198128	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT5_CH_CTL	0x42198140	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT5_CH_STATUS	0x42198144	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT5_CH_IDX	0x42198148	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT5_CH_CURR_PTR	0x4219814C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT5_INTR	0x42198150	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT5_INTR_SET	0x42198154	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT5_INTR_MASK	0x42198158	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.

Direct Memory Access (DMA) registers

Register	Address	Description
DW1_CH_STRUCT5_INTR_MASKED	0x4219815C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT5_TR_CMD	0x42198168	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT6_CH_CTL	0x42198180	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT6_CH_STATUS	0x42198184	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT6_CH_IDX	0x42198188	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT6_CH_CURR_PTR	0x4219818C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT6_INTR	0x42198190	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT6_INTR_SET	0x42198194	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT6_INTR_MASK	0x42198198	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT6_INTR_MASKED	0x4219819C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT6_TR_CMD	0x421981A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT7_CH_CTL	0x421981C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT7_CH_STATUS	0x421981C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT7_CH_IDX	0x421981C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT7_CH_CURR_PTR	0x421981CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT7_INTR	0x421981D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT7_INTR_SET	0x421981D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT7_INTR_MASK	0x421981D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.

Direct Memory Access (DMA) registers

Register	Address	Description
DW1_CH_STRUCT7_INTR_MASKED	0x421981DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT7_TR_CMD	0x421981E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT8_CH_CTL	0x42198200	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT8_CH_STATUS	0x42198204	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT8_CH_IDX	0x42198208	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT8_CH_CURR_PTR	0x4219820C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT8_INTR	0x42198210	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT8_INTR_SET	0x42198214	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT8_INTR_MASK	0x42198218	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT8_INTR_MASKED	0x4219821C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT8_TR_CMD	0x42198228	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT9_CH_CTL	0x42198240	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT9_CH_STATUS	0x42198244	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT9_CH_IDX	0x42198248	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT9_CH_CURR_PTR	0x4219824C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT9_INTR	0x42198250	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT9_INTR_SET	0x42198254	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT9_INTR_MASK	0x42198258	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.

Direct Memory Access (DMA) registers

Register	Address	Description
DW1_CH_STRUCT9_INTR_MASKED	0x4219825C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT9_TR_CMD	0x42198268	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT10_CH_CTL	0x42198280	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT10_CH_STATUS	0x42198284	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT10_CH_IDX	0x42198288	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT10_CH_CURR_PTR	0x4219828C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT10_INTR	0x42198290	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT10_INTR_SET	0x42198294	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT10_INTR_MASK	0x42198298	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT10_INTR_MASKED	0x4219829C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT10_TR_CMD	0x421982A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT11_CH_CTL	0x421982C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT11_CH_STATUS	0x421982C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT11_CH_IDX	0x421982C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT11_CH_CURR_PTR	0x421982CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT11_INTR	0x421982D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT11_INTR_SET	0x421982D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT11_INTR_MASK	0x421982D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.

Direct Memory Access (DMA) registers

Register	Address	Description
DW1_CH_STRUCT11_INTR_MASKED	0x421982DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT11_TR_CMD	0x421982E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT12_CH_CTL	0x42198300	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT12_CH_STATUS	0x42198304	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT12_CH_IDX	0x42198308	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT12_CH_CURR_PTR	0x4219830C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT12_INTR	0x42198310	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT12_INTR_SET	0x42198314	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT12_INTR_MASK	0x42198318	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT12_INTR_MASKED	0x4219831C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT12_TR_CMD	0x42198328	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT13_CH_CTL	0x42198340	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT13_CH_STATUS	0x42198344	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT13_CH_IDX	0x42198348	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT13_CH_CURR_PTR	0x4219834C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT13_INTR	0x42198350	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT13_INTR_SET	0x42198354	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT13_INTR_MASK	0x42198358	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.

Direct Memory Access (DMA) registers

Register	Address	Description
DW1_CH_STRUCT13_INTR_MASKED	0x4219835C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT13_TR_CMD	0x42198368	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT14_CH_CTL	0x42198380	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT14_CH_STATUS	0x42198384	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT14_CH_IDX	0x42198388	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT14_CH_CURR_PTR	0x4219838C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT14_INTR	0x42198390	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT14_INTR_SET	0x42198394	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT14_INTR_MASK	0x42198398	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT14_INTR_MASKED	0x4219839C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT14_TR_CMD	0x421983A8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.
DW1_CH_STRUCT15_CH_CTL	0x421983C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT15_CH_STATUS	0x421983C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT15_CH_IDX	0x421983C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT15_CH_CURR_PTR	0x421983CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT15_INTR	0x421983D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT15_INTR_SET	0x421983D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT15_INTR_MASK	0x421983D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.

Direct Memory Access (DMA) registers

Register	Address	Description
DW1_CH_STRUCT15_INTR_MASKED	0x421983DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT15_TR_CMD	0x421983E8	Channel software trigger. See DW0_CH_STRUCT0_TR_CMD for the details of bit fields.

3.1.1 DW0_CTL

Control

Address: 0x42180000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	IP enable: '0': Disabled. Disabling the IP activates the IP's Active logic reset: Active logic and non-retention MMIO registers are reset (retention MMIO registers are not affected). Note that DW SRAM writes/reads are possible when ENABLED=0 also. '1': Enabled. Default Value: 0

3.1.2 DW0_STATUS

Status

Address: 0x42180004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None	R	R	R
HW Access	RW				None	RW	RW	RW
Name	PC [7:4]				None	B	NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	None	R	
HW Access	None				W	None	W	
Name	None [15:12]				PREEMPT-ABLE	None	PRIO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							W
Name	None [23:17]							CH_IDX

Bits	31	30	29	28	27	26	25	24
SW Access	R	R			None			
HW Access	W	W			None			
Name	ACTIVE	STATE [30:28]			None [27:24]			

Bits	Name	Description
31	ACTIVE	Active channel present: '0': No. '1': Yes. Default Value: 0
30 : 28	STATE	State of the DW controller. "0": Default/inactive state. "1": Loading descriptor. "2": Loading data element from source location. "3": Storing data element to destination location. "4": CRC functionality (only used for CRC transfer descriptor type). "5": Update of active control information (e.g. source and destination addresses) and wait for trigger de-activation. "6": Error. Default Value: 0
16	CH_IDX	Active channel index. Default Value: Undefined
11	PREEMPTABLE	Active channel preemptable. Default Value: Undefined
9 : 8	PRIO	Active channel priority. Default Value: Undefined
7 : 4	PC	Active channel protection context. Default Value: Undefined

3.1.2 DW0_STATUS (continued)

2	B	Active channel, non-bufferable/bufferable access control: '0': non-bufferable '1': bufferable. Default Value: Undefined
1	NS	Active channel, secure/non-secure access control: '0': secure. '1': non-secure. Default Value: Undefined
0	P	Active channel, user/privileged access control: '0': user mode. '1': privileged mode. Default Value: Undefined

3.1.3 DW0_ACT_DESCR_CTL

Active descriptor control

Address: 0x42180020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description

3.1.3 DW0_ACT_DESCR_CTL (continued)

31 : 0	DATA	Copy of DESCR_CTL of the currently active descriptor. [1:0] WAIT_FOR_DEACT Specifies whether the controller should wait for the input trigger to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controller with the agent that generated the trigger. This field is ONLY used at the completion of the transfer as specified by TR_IN. E.g., a TX FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the controller AND received by the agent. Furthermore, the agent's trigger may be delayed by a few cycles before it reaches the controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW controller performance. "0": Do not wait for trigger de-activation (for pulse sensitive triggers). "1": Wait for up to 4 cycles. "2": Wait for up to 16 cycles. "3": Wait indefinitely. This option may result in controller lockup if the trigger is not de-activated. [3:2] INTR_TYPE Specifies the input trigger type (not to be confused with the descriptor type): "0": A trigger results in the execution of a single transfer. The descriptor type can be single, 1D or 2D. "1": A trigger results in the execution of a single 1D transfer. - If the descriptor type is "single", the trigger results in the execution of a single transfer. - If the descriptor type is "1D" or "2D", the trigger results in the execution of a 1D transfer. "2": A trigger results in the execution of the current descriptor. "3": A trigger results in the execution of the current descriptor and continues (without requiring another input trigger) with the execution of the next descriptor using the next descriptor's information. [5:4] TR_OUT_TYPE Specifies when an output trigger is generated: "0": An output trigger is generated after a single transfer. "1": An output trigger is generated after a single 1D transfer. - If the descriptor type is "single", the output trigger is generated after a single transfer. - If the descriptor type is "1D", "CRC" or "2D", the output trigger is generated after the execution of a 1D transfer. "2": An output trigger is generated after the execution of the current descriptor. "3": An output trigger is generated after the execution of a descriptor list: after the execution of the current descriptor AND the current descriptor DESCR_NEXT_PTR.ADDR is "0'. [7:6] TR_IN_TYPE Specifies the input trigger type (not to be confused with the descriptor type): "0": A trigger results in the execution of a single transfer. The descriptor type can be single, 1D or 2D. "1": A trigger results in the execution of a single 1D transfer. - If the descriptor type is "single", the trigger results in the execution of a single transfer. - If the descriptor type is "1D" or "2D", the trigger results in the execution of a 1D transfer. "2": A trigger results in the execution of the current descriptor. "3": A trigger results in the execution of the current descriptor and continues (without requiring another input trigger) with the execution of the next descriptor using the next descriptor's information. [24] CH_DISABLE Specifies whether the channel is disabled or not after completion of the current descriptor (independent of the value of the DESCR_NEXT_PTR value): '0': Channel is not disabled. '1': Channel is disabled. Note: a disabled channel will ignore its input trigger. [26] SRC_TRANSFER_SIZE Specifies the bus transfer size to the source location: '0': As specified by DATA_SIZE. '1': Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element. [27] DST_TRANSFER_SIZE Specifies the bus transfer size to the destination location: '0': As specified by DATA_SIZE. '1': Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element. [29:28] DATA_SIZE Specifies the data element size: "0": Byte (8 bits). "1": Halfword (16 bits). "2": Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: - DATA is 8 bit, SRC is 8 bit, DST is 8 bit. - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit. - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made "0"). - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made "0"). - DATA is 16 bit, SRC is 16 bit, DST is 16 bit. - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit. - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made "0"). - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made "0"). - DATA is 32 bit, SRC is 32 bit, DST is 32 bit. [31:30] DESCR_TYPE Specifies the descriptor type (not to be confused with the trigger type): "0": Single transfer. The DESCR_X_CTL and DESCR_Y_CTL registers are not present and DESCR_NEXT_PTR is at offset 0x0c. "1": 1D transfer. The DESCR_X_CTL register is present, the DESCR_Y_CTL is not present and DESCR_NEXT_PTR is at offset 0x10. A 1D transfer consists out of DESCR_X_CTL.X_COUNT single transfers. "2": 2D transfer. The DESCR_X_CTL and DESCR_Y_CTL registers are present and DESCR_NEXT_PTR is at offset 0x14. A 2D transfer consists of DESCR_X_CTL.X_COUNT*DESCR_Y_CTL.Y_COUNT single transfers. "3": CRC transfer. The DESCR_X_CTL register is present, theDESCR_Y_CTL is not present and DESCR_NEXT_PTR is at offset 0x10. A CRC transfer consists out of DESCR_X_CTL.X_COUNT single transfers. After the execution of the current descriptor, the DESCR_NEXT_PTR address is copied to the channel's CH_CURR_PTR address and CH_STATUS.X_IDX and CH_STATUS.Y_IDX are set to "0". Default Value: Undefined

3.1.4 DW0_ACT_DESCR_SRC

Active descriptor source

Address: 0x42180024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Copy of DESCR_SRC of the currently active descriptor. Base address of source location. Default Value: Undefined

3.1.5 DW0_ACT_DESCR_DST

Active descriptor destination

Address: 0x42180028

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Copy of DESCR_DST of the currently active descriptor. Base address of destination location. Note: For a CRC transfer descriptor, this field should be programmed with the address of the CRC_LFSR_CTL register. The calculated CRC LFSR state is written to this address (through the CRYPTO AHB-Lite master interface) when the input trigger is processed. The write transfer will be submitted to the CPUSS and PERI protection schemes. Default Value: Undefined

3.1.6 DW0_ACT_DESCR_X_CTL

Active descriptor X loop control

Address: 0x42180030

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Copy of DESCR_X_CTL of the currently active descriptor. [11:0] SRC_X_INCR Specifies increment of source address for each X loop iteration (in multiples of SRC_TRANSFER_SIZE). This field is a signed number in the range [-2048, 2047]. If this field is "0", the source address is not incremented. This is useful for reading from RX FIFO structures. [23:12] DST_X_INCR Specifies increment of destination address for each X loop iteration (in multiples of DST_TRANSFER_SIZE). This field is a signed number in the range [-2048, 2047]. If this field is "0", the destination address is not incremented. This is useful for writing to TX FIFO structures. Note: this field is not used for CRC transfer descriptors and must be set to "0". [31:24] X_COUNT Number of iterations (minus 1) of the "X loop" (X_COUNT+1 is the number of single transfers in a 1D transfer). This field is an unsigned number in the range [0, 255], representing 1 through 256 iterations. For a single transfer descriptor type, descriptor will not have X_CTL. Default Value: Undefined

3.1.7 DW0_ACT_DESCR_Y_CTL

Active descriptor Y loop control

Address: 0x42180034

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Copy of DESCR_Y_CTL of the currently active descriptor. [11:0] SRC_Y_INCR Specifies increment of source address for each Y loop iteration (in multiples of SRC_TRANSFER_SIZE). This field is a signed number in the range [-2048, 2047]. [23:12] DST_Y_INCR Specifies increment of destination address for each Y loop iteration (in multiples of DST_TRANSFER_SIZE). This field is a signed number in the range [-2048, 2047]. [31:24] Y_COUNT Number of iterations (minus 1) of the "Y loop" (X_COUNT+1)*(Y_COUNT+1) is the number of single transfers in a 2D transfer). This field is an unsigned number in the range [0, 255], representing 1 through 256 iterations. For single, 1D and CRC transfer descriptor types, descriptor will not have Y_CTL. Default Value: Undefined

3.1.8 DW0_ACT_DESCR_NEXT_PTR

Active descriptor next pointer

Address: 0x42180038

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 2	ADDR	Copy of DESCR_NEXT_PTR of the currently active descriptor. [31:2] ADDR Address of next descriptor in descriptor list. When this field is "0", this is the last descriptor in the descriptor list. Default Value: Undefined

3.1.9 DW0_ACT_SRC

Active source

Address: 0x42180040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SRC_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SRC_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	SRC_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	SRC_ADDR [31:24]							

Bits	Name	Description
31 : 0	SRC_ADDR	Current address of source location. Default Value: Undefined

3.1.10 DW0_ACT_DST

Active destination

Address: 0x42180044

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DST_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DST_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DST_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DST_ADDR [31:24]							

Bits	Name	Description
31 : 0	DST_ADDR	Current address of destination location. Default Value: Undefined

3.1.11 DW0_CRC_CTL

CRC control

Address: 0x42180100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							DATA_REVERSE

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							REM_REVERSE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	REM_REVERSE	Specifies whether the remainder is bit reversed (reversal is performed after XORing): '0': No. '1': Yes. Default Value: 0
0	DATA_REVERSE	Specifies the bit order in which a data Byte is processed (reversal is performed after XORing): '0': Most significant bit (bit 1) first. '1': Least significant bit (bit 0) first. Default Value: 0

3.1.12 DW0_CRC_DATA_CTL

CRC data control

Address: 0x42180110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA_XOR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA_XOR	Specifies a byte mask with which each data byte is XOR'd. The XOR is performed before data reversal. Default Value: 0

3.1.13 DW0_CRC_POL_CTL

CRC polynomial control

Address: 0x42180120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [31:24]							

Bits	Name	Description
31 : 0	POLYNOMIAL	CRC polynomial. The polynomial is represented WITHOUT the high order bit (this bit is always assumed '1'). The polynomial should be aligned/shifted such that the more significant bits (bit 31 and down) contain the polynomial and the less significant bits (bit 0 and up) contain padding '0's. Some frequently used polynomials: - CRC32: POLYNOMIAL is 0x04c11db7 (x^32 + x^26 + x^23 + x^22 + x^16 + x^12 + x^11 + x^10 + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1). - CRC16: POLYNOMIAL is 0x80050000 (x^16 + x^15 + x^2 + 1, shifted by 16 bit positions). - CRC16 CCITT: POLYNOMIAL is 0x10210000 (x^16 + x^12 + x^5 + 1, shifted by 16 bit positions). Default Value: 0

3.1.14 DW0_CRC_LFSR_CTL

CRC LFSR control

Address: 0x42180130

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	LFSR32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	LFSR32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	LFSR32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	LFSR32 [31:24]							

Bits	Name	Description
31 : 0	LFSR32	State of a 32-bit Linear Feedback Shift Registers (LFSR) that is used to implement CRC. This register needs to be initialized by SW to provide the CRC seed value. The seed value should be aligned such that the more significant bits (bit 31 and down) contain the seed value and the less significant bits (bit 0 and up) contain padding '0's. Note that SW can write this field. This functionality can be used prevent information leakage (through either CRC_LFSR_CTL or CRC_REM_RESULT). Default Value: 0

3.1.15 DW0_CRC_REM_CTL

CRC remainder control

Address: 0x42180140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	REM_XOR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	REM_XOR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	REM_XOR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	REM_XOR [31:24]							

Bits	Name	Description
31 : 0	REM_XOR	Specifies a mask with which the CRC_LFSR_CTL.LFSR32 register is XOR'd to produce a remainder. The XOR is performed before remainder reversal. Default Value: 0

3.1.16 DW0_CRC_REM_RESULT

CRC remainder result

Address: 0x42180148

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	REM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	REM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	REM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	REM [31:24]							

Bits	Name	Description
31 : 0	REM	Remainder value. The alignment of the remainder depends on CRC_REM_CTL0.REM_REVERSE: '0': the more significant bits (bit 31 and down) contain the remainder. '1': the less significant bits (bit 0 and up) contain the remainder. Note: This field is combinatorially derived from CRC_LFSR_CTL.LFSR32, CRC_CTL.REM_REVERSE and CRC_REM_CTL.REM_XOR. Default Value: 0

3.1.17 DW0_CH_STRUCT0_CH_CTL

Channel control

Address: 0x42188000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				None	RW	RW	RW
HW Access	R				None	R	R	R
Name	PC [7:4]				None	B	NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	None	RW	
HW Access	None				R	None	R	
Name	None [15:12]				PREEMPT-ABLE	None	PRIO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW1C	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	Channel enable: '0': Disabled. The channel's trigger is ignored and the channel cannot be made pending and therefore cannot be made active. If a pending channel is disabled, the channel is made non pending. If the activate channel is disabled, the channel is de-activated (bus transactions are completed). '1': Enabled. SW sets this field to '1' to enable a specific channel. HW sets this field to '0' on an error interrupt cause (the specific error is specified by CH_STATUS.INTR_CAUSE). Default Value: 0
11	PREEMPTABLE	Specifies if the channel is preemptable. '0': Not preemptable. '1': Preemptable. This field allows higher priority pending channels (from a higher priority group; i.e. an active channel can NOT be preempted by a pending channel in the same priority group) to preempt the active channel in between "single transfers" (a 1D transfer consists out of X_COUNT single transfers; a 2D transfer consists out of X_COUNT*Y_COUNT single transfers). Preemption will NOT affect the pending status of channel. As a result, after completion of a higher priority activated channel, the current channel may be reactivated. Default Value: Undefined

3.1.17 DW0_CH_STRUCT0_CH_CTL (continued)

9 : 8	PRIO	Channel priority: "0": highest priority. "1" "2" "3": lowest priority. Channels with the same priority constitute a priority group. Priority decoding determines the highest priority pending channel. This channel is determined as follows. First, the highest priority group with pending channels is identified. Second, within this priority group, round robin arbitration is applied. Round robin arbitration (within a priority group) gives the highest priority to the lower channel indices (within the priority group). Default Value: 0
7 : 4	PC	Protection context. This field is set with the protection context of the transaction that writes this register; i.e. the 'write data' is ignored and instead the context is inherited from the write transaction (note the field attributes should be HW:RW, SW:R). All transactions for this channel uses the PC field for the protection context. Note: protection context (PC) is routed on "hauser" bus of the AHB5 bus. Default Value: Undefined
2	B	Non-bufferable/bufferable access control: '0': non-bufferable. '1': bufferable. This field is used to indicate to an AMBA bridge that a write transaction can complete without waiting for the destination to accept the write transaction data. All transactions for this channel uses the B field for the non-bufferable/bufferable access control ("hprot[2]"). Default Value: Undefined
1	NS	Secure/on-secure access control: '0': secure. '1': non-secure. This field is set with the secure/non-secure access control of the transaction that writes this register; i.e. the 'write data' is ignored and instead the access control is inherited from the write transaction (note the field attributes should be HW:RW, SW:R). All transactions for this channel use the NS field for the secure/non-secure access control ("hnonsec"). Default Value: Undefined
0	P	User/privileged access control: '0': user mode. '1': privileged mode. This field is set with the user/privileged access control of the transaction that writes this register; i.e. the 'write data' is ignored and instead the access control is inherited from the write transaction (note the field attributes should be HW:RW, SW:R). All transactions for this channel use the P field for the user/privileged access control ("hprot[1]"). Default Value: Undefined

3.1.18 DW0_CH_STRUCT0_CH_STATUS

Channel status

Address: 0x42188004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				INTR_CAUSE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	PENDING	None [30:24]						

Bits	Name	Description
31	PENDING	Specifies pending DW channels; i.e. enabled channels whose trigger got activated. This field includes all channels that are in the pending state (not scheduled) or active state (scheduled and performing data transfer(s)). Default Value: 0
3 : 0	INTR_CAUSE	Specifies the source of the interrupt cause: "0": NO_INTR "1": COMPLETION "2": SRC_BUS_ERROR "3": DST_BUS_ERROR "4": SRC_MISAL "5": DST_MISAL "6": CURR_PTR_NULL "7": ACTIVE_CH_DISABLED "8": DESCR_BUS_ERROR "9"-"15": Not used. For error related interrupt causes (INTR_CAUSE is "2", "3", ..., "8"), the channel is disabled (HW sets CH_CTL.ENABLED to '0'). Default Value: Undefined

3.1.19 DW0_CH_STRUCT0_CH_IDX

Channel current indices

Address: 0x42188008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	X_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	Y_IDX [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	Y_IDX	Specifies the Y loop index, with X_COUNT taken from the current descriptor. Note: HW sets this field to "0" when it updates the current descriptor pointer CH_CURR_PTR with DESCR_NEXT_PTR after execution of the current descriptor. Note: SW should set this field to "0" when it updates CH_CURR_PTR. Default Value: Undefined
7 : 0	X_IDX	Specifies the X loop index. In the range of [0, X_COUNT], with X_COUNT taken from the current descriptor. Note: HW sets this field to "0" when it updates the current descriptor pointer CH_CURR_PTR with DESCR_NEXT_PTR after execution of the current descriptor. Note: SW should set this field to "0" when it updates CH_CURR_PTR. Default Value: Undefined

3.1.20 DW0_CH_STRUCT0_CH_CURR_PTR

Channel current descriptor pointer

Address: 0x4218800C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	RW						None	
Name	ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 2	ADDR	Address of current descriptor. When this field is "0", there is no valid descriptor. Note: HW updates the current descriptor pointer CH_CURR_PTR with DESCR_NEXT_PTR after execution of the current descriptor. Note: Typically, when SW updates the current descriptor pointer CH_CURR_PTR, it also sets CH_IDX.X_IDX and CH_IDX.Y_IDX to "0". Default Value: Undefined

3.1.21 DW0_CH_STRUCT0_INTR

Interrupt

Address: 0x42188010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [7:1]							CH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CH	Set to '1', when event (as specified by CH_STATUS.INTR_CAUSE) is detected. Write INTR.CH field with '1', to clear bit. Write INTR_SET.CH field with '1', to set bit. Default Value: 0

3.1.22 DW0_CH_STRUCT0_INTR_SET

Interrupt set

Address: 0x42188014

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							A
Name	None [7:1]							CH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CH	Write INTR_SET field with '1' to set corresponding INTR.CH field (a write of '0' has no effect). Default Value: 0

3.1.23 DW0_CH_STRUCT0_INTR_MASK

Interrupt mask

Address: 0x42188018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							CH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CH	Mask for corresponding field in INTR register. Default Value: 0

3.1.24 DW0_CH_STRUCT0_INTR_MASKED

Interrupt masked

Address: 0x4218801C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							CH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CH	Logical and of corresponding INTR and INTR_MASK fields. Default Value: 0

3.1.25 DW0_CH_STRUCT0_TR_CMD

Channel software trigger

Address: 0x42188028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							A
Name	None [7:1]							ACTIVATE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	ACTIVATE	Software trigger. When written with '1', a trigger is generated which sets 'trigger pending' (only if the channel is enabled). A read always returns a 0. Default Value: 0

4 FLASH registers

This section discusses the FLASH registers. It lists all the registers in mapping tables, in address order.

4.1 Register details

Register	Address	Description
FLASHC_FLASH_CTL	0x42150000	Flash control
FLASHC_FLASH_SECTOR_M	0x42150104	Number of sectors of a FM
FLASHC_FLASH_MAIN_N	0x42150108	Size of MAIN in 8 KB block for each pair of sectors
FLASHC_FLASH_WORK_Z	0x4215010C	Size of WORK in 8 KB block for each pair of sectors
FLASHC_FLASH_SFLASH_Y	0x42150110	Size of SLFASH in 8KB block in Sector 1
FLASHC_FLASH_REFRESH_ROW	0x42150114	Size of refresh rows for each sector
FLASHC_FLASH_CMD	0x42150200	Command
FLASHC_FLASH_LOCK	0x42150204	Flash Controller Lock Register
FLASHC_FLASH_PWR_CTL	0x42150208	Flash power control
FLASHC_ENFORCE_PC_LOCK_SHADOW	0x4215020C	Shadow bit of FLASH_CTL.ENFORCE_PC_LOCK
FLASHC_ECC_INJ_EN	0x42150800	ECC injection enable on read
FLASHC_ECC_INJ_CTL	0x42150804	ECC injection control
FLASHC_ECC_LOGIR	0x42150808	Interrupt threshold for number of ECC correctable error
FLASHC_MPC0_CFG	0x42151000	Config register with error response, RegionID PPC_MPC_MAIN is the security owner PC. The error response configuration is located in CFG.RESPONSE, only one such configuration exists applying to all protection contexts in the system.
FLASHC_MPC0_CTRL	0x42151100	Control register with lock bit and auto-increment only (Separate CTRL for each PC depends on access_pc)
FLASHC_MPC0_BLK_MAX	0x42151104	Max value of block-based index register
FLASHC_MPC0_BLK_CFG	0x42151108	Block size & initialization in progress
FLASHC_MPC0_BLK_IDX	0x4215110C	Index of 32-block group accessed through BLK_LUT (Separate IDX for each PC depending on access_pc)
FLASHC_MPC0_BLK_LUT	0x42151110	NS status for 32 blocks at BLK_IDX with PC=<access_pc>
FLASHC_MPC0_ROT_CTRL	0x42151200	Control register with lock bit and auto-increment only
FLASHC_MPC0_ROT_BLK_MAX	0x42151208	Max value of block-based index register for ROT
FLASHC_MPC0_ROT_BLK_CFG	0x4215120C	Same as BLK_CFG
FLASHC_MPC0_ROT_BLK_IDX	0x42151210	Index of 8-block group accessed through ROT_BLK_LUT_*
FLASHC_MPC0_ROT_BLK_PC	0x42151214	Protection context of 8-block group accesses through ROT_BLK_LUT

FLASH registers

Register	Address	Description
FLASHC_MPC0_ROT_BLK_LUT	0x42151218	(R,W,NS) bits for 8 blocks at ROT_BLK_IDX for PC=ROT_BKL_PC
FLASHC_FM_CTL_RED_CTL01	0x42152040	Redundancy Control normal sectors 0,1
FLASHC_FM_CTL_RED_CTL23	0x42152044	Redundancy Control normal sectors 2,3
FLASHC_FM_CTL_FM_PL_DATA0	0x42152800	Flash macro Page Latches data. This is the starting address of a register bank containing 132 registers (FLASHC_FM_CTL_FM_PL_DATA0 to FLASHC_FM_CTL_FM_PL_DATA131).
FLASHC_FM_CTL_FLASH_MACRO_CTL	0x42152A10	Flash macro control
FLASHC_FM_CTL_STATUS	0x42152A14	Status
FLASHC_FM_CTL_FM_ADDR	0x42152A18	Flash macro address
FLASHC_FM_CTL_BOOKMARK	0x42152A1C	Bookmark register - keeps the current FW HV seq
FLASHC_FM_CTL_GEOMETRY	0x42152A20	Regular flash geometry
FLASHC_FM_CTL_GEOMETRY_SUPERVISORY	0x42152A24	Supervisory flash geometry
FLASHC_FM_CTL_ANA_CTL0	0x42152A28	Analog control 0
FLASHC_FM_CTL_ANA_CTL1	0x42152A2C	Analog control 1
FLASHC_FM_CTL_FM_PL_WRDATA_ALL	0x42152A30	Flash macro write page latches all
FLASHC_FM_CTL_FM_REFRESH_ADDR	0x42152A34	Address bit to point to scratch area
FLASHC_FM_CTL_RGRANT_DELAY_ERS	0x42152A38	R-grant delay for erase
FLASHC_FM_CTL_RGRANT_SCALE_ERS	0x42152A3C	R-grant delay scale for erase
FLASHC_FM_CTL_PW_SEQ23	0x42152A40	HV Pulse Delay for seq2 post & seq3
FLASHC_FM_CTL_PW_SEQ12	0x42152A44	HV Pulse Delay for seq 1&2 pre
FLASHC_FM_CTL_WAIT_CTL	0x42152A48	Wait State control
FLASHC_FM_CTL_RGRANT_DELAY_PRG	0x42152A4C	R-grant delay for program
FLASHC_FM_CTL_TIMER_CLK_CTL	0x42152A50	Timer prescaler (clk_t to timer clock frequency divider)
FLASHC_FM_CTL_TIMER_CTL	0x42152A54	Timer control
FLASHC_FM_CTL_ACLK_CTL	0x42152A58	MPCON clock
FLASHC_FM_CTL_INTR	0x42152A5C	Interrupt
FLASHC_FM_CTL_INTR_SET	0x42152A60	Interrupt set
FLASHC_FM_CTL_INTR_MASK	0x42152A64	Interrupt mask
FLASHC_FM_CTL_INTR_MASKED	0x42152A68	Interrupt masked
FLASHC_FM_CTL_CAL_CTL0	0x42152A6C	Cal control - VCT, VBG, CDAC, IPREF
FLASHC_FM_CTL_CAL_CTL1	0x42152A70	Cal control - ICREF, IPREF
FLASHC_FM_CTL_CAL_CTL2	0x42152A74	Cal control - IDAC, IBS_CTL, LAT_DIS
FLASHC_FM_CTL_CAL_CTL3	0x42152A78	Cal control - OSC trims, FDIV, REG_ACT, TURBO, LP_ULP_SW
FLASHC_FM_CTL_CAL_CTL4	0x42152A7C	Cal control - VLIM, IDAC, SDAC, ITIM ULP trims
FLASHC_FM_CTL_CAL_CTL5	0x42152A80	Cal control - VLIM, IDAC, SDAC, ITIM LP trims

FLASH registers

Register	Address	Description
FLASHC_FM_CTL_CAL_CTL6	0x42152A84	Cal control - SA CTL LP/ULP trims
FLASHC_FM_CTL_CAL_CTL7	0x42152A88	Cal control - ERSX8_CLK_SEL, FM_ACTIVE, TURBO_EXT
FLASHC_FM_CTL_FM_PL_ECC0	0x42152B00	Flash macro Page Latches ECC. This is the starting address of a register bank containing 33 registers (FLASHC_FM_CTL_FM_PL_ECC0 to FLASHC_FM_CTL_FM_PL_ECC32).
FLASHC_FM_CTL_FM_MEM_DATA0	0x42152C00	Flash macro memory sense amplifier data. This is the starting address of a register bank containing 132 registers (FLASHC_FM_CTL_FM_MEM_DATA0 to FLASHC_FM_CTL_FM_MEM_DATA131).
FLASHC_FM_CTL_FM_MEM_ECC0	0x42152F00	Flash macro memory sense amplifier ECC. This is the starting address of a register bank containing 33 registers (FLASHC_FM_CTL_FM_MEM_ECC0 to FLASHC_FM_CTL_FM_MEM_ECC32).
FLASHC_FM_CTL_FM_ECC_CTL_ADDR	0x42152FEC	Internal ECC signal - unused
FLASHC_FM_CTL_FM_RED_CTL_SM01_ADDR	0x42152FF0	Internal register
FLASHC_FM_CTL_FM_RED_CTL67_ADDR	0x42152FF4	Internal register
FLASHC_FM_CTL_FM_RED_CTL45_ADDR	0x42152FF8	Internal register
FLASHC_FM_CTL_FM_CAL_CTL8_ADDR	0x42152FFC	Internal register

4.1.1 FLASHC_FLASH_CTL

Flash control

Address: 0x42150000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				RBUS_WS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [15:13]			BANK_-MODE	None [11:10]		BANK_MAPPING [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW	None	RW
HW Access	None					R	None	R
Name	None [23:19]					RBUS_ER-R_SILENT	None	ECC_EN

Bits	31	30	29	28	27	26	25	24
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				R	R	R	R
Name	None [31:28]				BLOCK_BULK_OPER-ATIONS	BLOCK_-SUBSEC-TOR_OPERATIONS	BLOCK_-SEC-TOR_OPERATIONS	EN-FORCE_P-C_LOCK

Bits	Name	Description
27	BLOCK_BULK_OPERA-TIONS	This bit can be set once and not cleared thereafter. When set it is no longer possible to perform bulk erase or bulk DFT operations. The flash controller will block any write operations to the FM_CTL register pertaining to such operations. Default Value: 0
26	BLOCK_SUBSEC-TOR_OPERATIONS	This bit can be set once and not cleared thereafter. When set it is no longer possible to perform subsector erase or subsector DFT operations. The flash controller will block any write operations to the FM_CTL register pertaining to such operations. Default Value: 0
25	BLOCK_SECTOR_OPER-ATIONS	This bit can be set once and not cleared thereafter. When set it is no longer possible to perform sector erase or sector DFT operations. The flash controller will block any write operations to the FM_CTL register pertaining to such operations. Default Value: 0
24	ENFORCE_PC_LOCK	This bit can be set once and not cleared thereafter. When set the PC inheritiance and locking mechanism described with the FLASH_LOCK register is enabled. When cleared, access to the flash controller and flash macro is possible from any protection context with appropriate PPC permissions. Default Value: 0

4.1.1 FLASHC_FLASH_CTL (continued)

18	RBUS_ERR_SILENT	Please note that it is SW's responsibility that I$ of M33 must be disabled before setting RBUS_ERR_SILENT HIGH. Otherwise, the erroneous goes to I$ which is NOT desired. Specifies bus transfer behavior for a non-recoverable error on the FLASH macro main interface (either a non-correctable ECC error, a FLASH macro main interface internal error, a FLASH macro main interface memory hole access): 0: Bus transfer has a bus error. 1: Bus transfer does NOT have a bus error; i.e. the error is "silent" In either case, the erroneous FLASH macro data is returned to CPU since I$ is disabled. This field is ONLY used by CPU bus transfers. Non-CPU bus transfers always have a bus transfer with a bus error and fault/interrupt, in case of a non-recoverable error. Note: All CPU bus masters have dedicated status registers (CM33 to register the occurrence of FLASH macro main interface (R-bus) internal errors. Note: fault reporting can be used to identify the error that occurred: - FLASH macro main interface internal error. - FLASH macro main interface non-recoverable ECC error. - FLASH macro main interface recoverable ECC error (over its threshold). - FLASH macro main interface memory hole error. Default Value: 0
16	ECC_EN	Enable ECC checking for FLASH main (R-bus) interface: 0: Disabled. ECC checking/reporting on FLASH main interface is disabled. No correctable or non-correctable faults are reported. 1: Enabled. Default Value: 1
12	BANK_MODE	Specifies bank mode of FLASH macro main array. 0: Single bank mode. 1: Dual bank mode. Default Value: 0
9 : 8	BANK_MAPPING	Specifies mapping of FLASH macro main subregion. 00: MAIN (Mapping A), WORK (Mapping A). 01: MAIN (Mapping B), WORK (Mapping A). 10: MAIN (Mapping A), WORK (Mapping B). 11: MAIN (Mapping B), WORK (Mapping B). This field is only used when MAIN_BANK_MODE is "1" (dual bank mode). Default Value: 0
3 : 0	RBUS_WS	FLASH macro main interface (R-bus) wait states: "0": 0 wait states. ... "15": 15 wait states Default Value: 0

4.1.2 FLASHC_FLASH_SECTOR_M

of sector of a FM

Address: 0x42150104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	SECTOR_M [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	SECTOR_M [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	SECTOR_M [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	SECTOR_M [31:24]							

Bits	Name	Description
31 : 0	SECTOR_M	# of sectors of a FM, must be an even number, same value as RTL parameter SECTOR_M. Default Value: 2

4.1.3 FLASHC_FLASH_MAIN_N

Size of MAIN in 8KB block for each pair of sectors

Address: 0x42150108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	MAIN_N [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	MAIN_N [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	MAIN_N [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	MAIN_N [31:24]							

Bits	Name	Description
31 : 0	MAIN_N	Size of MAIN_NVM in 8KB blocks for each pair of sectors, same value as RTL parameter MAIN_N. Default Value: 32

4.1.4 FLASHC_FLASH_WORK_Z

Size of WORK in 8KB block for each pair of sectors

Address: 0x4215010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK_Z [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK_Z [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	WORK_Z [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	WORK_Z [31:24]							

Bits	Name	Description
31 : 0	WORK_Z	Size of WORK_NVM in 8KB blocks for each pair of sectors, same value as RTL parameter WORK_Z, the value WORK_Z can be zero. Default Value: 0

4.1.5 FLASHC_FLASH_SFLASH_Y

Size of SLFASH in 8KB block in Sector 1

Address: 0x42150110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	SFLASH_Y [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	SFLASH_SECNUM	None [30:24]						

Bits	Name	Description
31	SFLASH_SECNUM	0: Not allowed 1: SM only in Sector 1 Default Value: 1
7 : 0	SFLASH_Y	Size of SFLASH_NVM in 8KB blocks in Sector 1, same value as RTL parameter SFLASH_Y. Default Value: 4

4.1.6 FLASHC_FLASH_REFRESH_ROW

Size of refresh rows for each sector

Address: 0x42150114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	REFRESH_ROW [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	REFRESH_ROW [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	REFRESH_ROW [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	REFRESH_ROW [31:24]							

Bits	Name	Description
31 : 0	REFRESH_ROW	Size of refresh rows for each sector, same value as RTL parameter REFRESH_ROW All sectors of a FM must have the same refresh rows It is 4 per sector for s40flash.3 FM. Default Value: 4

4.1.7 FLASHC_FLASH_CMD

Command

Address: 0x42150200

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	None
HW Access	None						RW1C	None
Name	None [7:2]						BUFF_INV	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	BUFF_INV	Invalidation of ALL buffers. SW writes a "1" to clear the buffers. HW sets this field to "0" when the operation is completed. The operation takes a maximum of three clock cycles. Default Value: 0

4.1.8 FLASHC_FLASH_LOCK

Flash Controller Lock Register

Address: 0x42150204

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				RW			
Name	None [7:4]				PC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	LOCKED	None [30:24]						

Bits	Name	Description
31	LOCKED	Software writes this register bit to 1 to 'lock' the flash controller to its own protection context (after setting the protection context by writing to a flash memory location). Once set, any subsequent (AHB) writes result in bus error and operation ignored. Software (FLASH.PC) reads back this field to check whether the lock succeeded. Software (FLASH_LOCK.PC) clears this field when it has completed a program/erase operation. To avoid deadlock and for management purpose, HW entitles PC0 the omnipotent capability to read FLASH_LOCK.PC and to release FLASH_LOCK.LOCKED no matter which PC acquires it. All PCs allowed by PPC can access FLASH_LOCK when its LOCKED bit is LOW (not locked). Default Value: 0
3 : 0	PC	When FLASH_LOCK is acquired, even PPC allows, further MMIO access is possible only to this FLASH_LOCK.PC (& same HMASTER_ID) irrespective of corresponding PPC attributes. Other PCs or the same PC but different HMASTER_ID violation results in bus error & operation ignored. There is no further interrupt/fault triggered for this violation. Default Value: 0

4.1.9 FLASHC_FLASH_PWR_CTL

Flash power control

Address: 0x42150208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						EN-ABLE_HV	ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	ENABLE_HV	Controls "enable_hv" pin of the Flash memory. Default Value: 1
0	ENABLE	Controls "enable" pin of the Flash memory. Default Value: 1

4.1.10 FLASHC_ENFORCE_PC_LOCK_SHADOW

Shadow bit of FLASH_CTL.ENFORCE_PC_LOCK

Address: 0x4215020C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							PC_LOCK_SHADOW

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	PC_LOCK_SHADOW	Shadow register of FLASH_CTL.ENFORCE_PC_LOCK. Read only irrespective of PPC's configuration. Default Value: 0

4.1.11 FLASHC_ECC_INJ_EN

ECC injection enable on read

Address: 0x42150800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							ECC_IN-J_ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							RW
Name	None [15:9]							ECC_ER-ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R				None			
HW Access	RW				None			
Name	ECC_INJ_PC [31:28]				None [27:24]			

Bits	Name	Description
31 : 28	ECC_INJ_PC	The PC is inherited from the master who enabled ECC_INJ_ENABLE (while ECC_INJ_ENABLE is low) Default Value: 0
8	ECC_ERROR	1'b0: If the injected ECC does not trigger any non-recoverable error (ECC errors <= 1). 1'b1: If the injected ECC triggers non-recoverable error (ECC errors >= 2). The AHB read transaction results in bus error. There is no additional fault/interrupt trigged. Default Value: 0
0	ECC_INJ_ENABLE	Enable ECC error injection for FLASH R-bus interface (while FLASH_CTL.ECC_EN enabled) . 1'b0: ECC_INJ_EN is disabled. 1'b1: ECC_INJ_EN is enabled. Only the PC specified by ECC_INJ_PC can access (read/write) ECC_INJ_ENABLE and ECC_ERROR when ECC_INJ_ENABLE is high excpet PC0 which can access it at any time to break the potential deadlock of ECC_INJ_EN. Default Value: 0

4.1.12 FLASHC_ECC_INJ_CTL

ECC injection control

Address: 0x42150804

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	WORD_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	WORD_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW						
HW Access	RW	RW						
Name	PARITY	WORD_ADDR [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	PARITY [31:24]							

Bits	Name	Description
31 : 23	PARITY	ECC parity to use for ECC error injection at address WORD_ADDR. The 9-bit ECC PARITY[8:0] is for a 128bit long word. Default Value: 0
22 : 0	WORD_ADDR	Specifies the word address where an error will be injected. The word address WORD_ADDR[22:0] is FM column address (module-internal offset), including cxa, bax, axa, sector, row/page definitions. On a FLASH R-bus read and when ECC_INJ_EN bit is "1", and when ECC_INJ_EN.ECC_INJ_PC value matches, the parity (PARITY[8:0]) replaces the FM parity. When ECC_INJ_ENABLE is 1'b1, only PC specified by ECC_INJ_EN.ECC_INJ_PC can access (read/write) WORD_ADDR and PARITY. Default Value: 0

4.1.13 FLASHC_ECC_LOGIR

Interrupt threshold for number of ECC correctable error

Address: 0x42150808

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ECCTHRESHOLD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ECCTHRESHOLD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	ECC1CNT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	ECC1CNT [31:24]							

Bits	Name	Description
31 : 16	ECC1CNT	Number of ECC single-bit failures detected and corrected during the memory read operations SW writes to register ECC_LOGIR.ECC1CNT are ignored if SW writes any number other than the real RTL counter. But write value of 16'b0 is allowed to clear ECC_LOGIR.ECC1CNT (when the number of ECC single-bit failures detected and corrected reaches threshold value). By design, ECC_LOGIR.ECC1CNT will be saturated at ECC_LOGIR.ECCTHRESHOLD and will not overru. It is recommended that ECCTHRESHOLD is at least 8'b1. Default Value: 0
15 : 0	ECCTHRESHOLD	Interrupt/fault threshold for number of ECC single-bit failures detected and corrected indicated in bit[31:16]. The # of failures must be one larger than ECCTHRESHOLD to trigger interrupt/fault." For example, while ECCTHRESHOLD is 0xFF, only upon the 256th failures, the ECC Fault information will be reported on flashc_main_c_ecc_mmio_fault_* output pins (fault will be triggered). After the 256th failures, ECC_LOGIR.ECC1CNT will stay saturated at 0xFF and will not overrun. Default Value: 0xFF

4.1.14 FLASHC_MPC0_CFG

Config register with error response, RegionID PPC_MPC_MAIN is the security owner PC. The error response configuration is located in CFG.RESPONSE, only one such configuration exists applying to all protection contexts in the system.

Address: 0x42151000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None			
HW Access	None			R	None			
Name	None [7:5]			RE-SPONSE	None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	RESPONSE	Response Configuration for Security and PC violations 0: Read-Zero Write Ignore (RAZ/WI) 1: Bus Error Default Value: 0

4.1.15 FLASHC_MPC0_CTRL

Control register with lock bit and auto-increment only (Separate CTRL for each PC depends on access_pc)

Address: 0x42151100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							AUTO_INC

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	None						
HW Access	R	None						
Name	LOCK	None [30:24]						

Bits	Name	Description
31	LOCK	Security lockdown for this protection context. Software can set this bit but not clear it once set. When set, write operations to BLK_LUT are not possible from this protection context. Setting LOCK also blocks writes to CTRL itself (for that PC copy). All writes are ignored. Default Value: 0
8	AUTO_INC	Auto-increment BLK_IDX by 1 for this protection context as a side effect of each read/write access to BLK_LUT Default Value: 1

4.1.16 FLASHC_MPC0_BLK_MAX

Max value of block-based index register

Address: 0x42151104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R		
HW Access	None					R		
Name	None [7:3]					VALUE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	VALUE	Maximum value of block-based index register. The number and size blocks in an MPC is design time configurable and for embedded memories defaults to covering the entire memory using 4kB blocks; See product datasheet for details on protection of external memories. Default Value: 7

4.1.17 FLASHC_MPC0_BLK_CFG

Block size & initialization in progress

Address: 0x42151108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				R			
Name	None [7:4]				BLOCK_SIZE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	INIT_IN_PROGRESS	None [30:24]						

Bits	Name	Description
31	INIT_IN_PROGRESS	During initialization INIT_IN_PROGRESS is '1' and MMIO register accesses to BLK_LUT is blocked (BLK_IDX increment is also ignored). The block attributes are retained in DeepSleep (and obviously Active) power mode. Initialization is only required from a power mode in which the block attributes are not retained. E.g., initialization is required for a cold boot (after a Power-on-Reset). HW initializes the block attributes: the NS attributes are set to '0' (secure), the R attributes are set to '1' (read access allowed) and the W attributes are set to '1' (write access allowed). During initialization, the MPC supports memory accesses (memory accesses are NOT blocked) with the initialization block attribute values as mentioned above. This e.g. allows MPC initialization to proceed in parallel with boot program memory accesses (as opposed to serializing the two), improving device boot time. Default Value: 1
3 : 0	BLOCK_SIZE	Block size of individually protected blocks (0: 32B, 1: 64B, ... up to 15: 1MB) Block size= (1<<(BLOCK_SIZE+5)) The number and size blocks in an MPC is design time configurable and for embedded memories defaults to covering the entire memory using 4kB blocks; see product datasheet for details on protection of external memories. Default Value: 6

4.1.18 FLASHC_MPC0_BLK_IDX

Index of 32-block group accessed through BLK_LUT (Separate IDX for each PC depending on access_pc)

Address: 0x4215110C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					RW		
Name	None [7:3]					VALUE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	VALUE	Index value for accessing block-based lookup table using BLK_LUT. Programming out of LUT range is an user error and it loops back to "0" once overflow occurs. Default Value: 0

4.1.19 FLASHC_MPC0_BLK_LUT

NS status for 32 blocks at BLK_IDX with PC=_pc>

Address: 0x42151110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	ATTR_NS7	ATTR_NS6	ATTR_NS5	ATTR_NS4	ATTR_NS3	ATTR_NS2	ATTR_NS1	ATTR_NS0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	ATTR_NS15	ATTR_NS14	ATTR_NS13	ATTR_NS12	ATTR_NS11	ATTR_NS10	ATTR_NS9	ATTR_NS8

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	ATTR_NS23	ATTR_NS22	ATTR_NS21	ATTR_NS20	ATTR_NS19	ATTR_NS18	ATTR_NS17	ATTR_NS16

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	ATTR_NS31	ATTR_NS30	ATTR_NS29	ATTR_NS28	ATTR_NS27	ATTR_NS26	ATTR_NS25	ATTR_NS24

Bits	Name	Description
31	ATTR_NS31	NS bit for block 31 based on BLK_IDX Default Value: 0
30	ATTR_NS30	NS bit for block 30 based on BLK_IDX Default Value: 0
29	ATTR_NS29	NS bit for block 29 based on BLK_IDX Default Value: 0
28	ATTR_NS28	NS bit for block 28 based on BLK_IDX Default Value: 0
27	ATTR_NS27	NS bit for block 27 based on BLK_IDX Default Value: 0
26	ATTR_NS26	NS bit for block 26 based on BLK_IDX Default Value: 0
25	ATTR_NS25	NS bit for block 25 based on BLK_IDX Default Value: 0
24	ATTR_NS24	NS bit for block 24 based on BLK_IDX Default Value: 0
23	ATTR_NS23	NS bit for block 23 based on BLK_IDX Default Value: 0
22	ATTR_NS22	NS bit for block 22 based on BLK_IDX Default Value: 0

4.1.19 FLASHC_MPC0_BLK_LUT (continued)

21	ATTR_NS21	NS bit for block 21 based on BLK_IDX Default Value: 0
20	ATTR_NS20	NS bit for block 20 based on BLK_IDX Default Value: 0
19	ATTR_NS19	NS bit for block 19 based on BLK_IDX Default Value: 0
18	ATTR_NS18	NS bit for block 18 based on BLK_IDX Default Value: 0
17	ATTR_NS17	NS bit for block 17 based on BLK_IDX Default Value: 0
16	ATTR_NS16	NS bit for block 16 based on BLK_IDX Default Value: 0
15	ATTR_NS15	NS bit for block 15 based on BLK_IDX Default Value: 0
14	ATTR_NS14	NS bit for block 14 based on BLK_IDX Default Value: 0
13	ATTR_NS13	NS bit for block 13 based on BLK_IDX Default Value: 0
12	ATTR_NS12	NS bit for block 12 based on BLK_IDX Default Value: 0
11	ATTR_NS11	NS bit for block 11 based on BLK_IDX Default Value: 0
10	ATTR_NS10	NS bit for block 10 based on BLK_IDX Default Value: 0
9	ATTR_NS9	NS bit for block 9 based on BLK_IDX Default Value: 0
8	ATTR_NS8	NS bit for block 8 based on BLK_IDX Default Value: 0
7	ATTR_NS7	NS bit for block 7 based on BLK_IDX Default Value: 0
6	ATTR_NS6	NS bit for block 6 based on BLK_IDX Default Value: 0
5	ATTR_NS5	NS bit for block 5 based on BLK_IDX Default Value: 0
4	ATTR_NS4	NS bit for block 4 based on BLK_IDX Default Value: 0
3	ATTR_NS3	NS bit for block 3 based on BLK_IDX Default Value: 0
2	ATTR_NS2	NS bit for block 2 based on BLK_IDX Default Value: 0
1	ATTR_NS1	NS bit for block 1 based on BLK_IDX Default Value: 0
0	ATTR_NS0	NS bit for block 0 based on BLK_IDX Default Value: 0

4.1.20 FLASHC_MPC0_ROT_CTRL

Control register with lock bit and auto-increment only

Address: 0x42151200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							AUTO_INC

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	None						
HW Access	R	None						
Name	LOCK	None [30:24]						

Bits	Name	Description
31	LOCK	Security lockdown for the root-of-trust configuration registers. Software can set this bit but not clear it once set. When set, write operations to ROT_BLK_LUT are not possible. Write is ignored. Default Value: 0
8	AUTO_INC	Auto-increment BLK_IDX by 1 for each read/write of ROT_BLK_LUT Default Value: 1

4.1.21 FLASHC_MPC0_ROT_BLK_MAX

Max value of block-based index register for ROT

Address: 0x42151208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			R				
Name	None [7:5]			VALUE [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	VALUE	Maximum value of block-based index register. The number and size blocks in an MPC is design time configurable and for embedded memories defaults to covering the entire memory using 4kB blocks; see product datasheet for details on protection of external memories. Default Value: 31

4.1.22 FLASHC_MPC0_ROT_BLK_CFG

Same as BLK_CFG

Address: 0x4215120C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				R			
Name	None [7:4]				BLOCK_SIZE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	INIT_IN_PROGRESS	None [30:24]						

Bits	Name	Description
31	INIT_IN_PROGRESS	During initialization INIT_IN_PROGRESS is '1' and MMIO register accesses to ROT_BLK_LUT is RAZWI. The block attributes are retained in DeepSleep (and obviously Active) power mode. Initialization is only required from a power mode in which the block attributes are not retained. E.g., initialization is required for a cold boot (after a Power-on-Reset). HW initializes the block attributes: the NS attributes are set to '0' (secure), the R attributes are set to '1' (read access allowed) and the W attributes are set to '1' (write access allowed). During initialization, the MPC supports memory accesses (memory accesses are NOT blocked) with the initialization block attribute values as mentioned above. This e.g. allows MPC initialization to proceed in parallel with boot program memory accesses (as opposed to serializing the two), improving device boot time. Default Value: 1
3 : 0	BLOCK_SIZE	Block size of individually protected blocks (0: 32B, 1: 64B, ...up to 15:1MB) Block size= (1<<(BLOCK_SIZE+5)) The number and size blocks in an MPC is design time configurable and for embedded memories defaults to covering the entire memory using 4kB blocks; see product datasheet for details on protection of external memories. Default Value: 6

4.1.23 FLASHC_MPC0_ROT_BLK_IDX

Index of 8-block group accessed through ROT_BLK_LUT_*

Address: 0x42151210

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			RW				
Name	None [7:5]			VALUE [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	VALUE	Index value for accessing block-based lookup table using ROT_BLK_LUT. Programming out of LUT range is an user error and it loops back to "0" once overflow occurs. Default Value: 0

4.1.24 FLASHC_MPC0_ROT_BLK_PC

Protection context of 8-block group accesses through ROT_BLK_LUT

Address: 0x42151214

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				PC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	PC	Specify PC values for ROT_BLK_IDX and ROT_BLK_LUT Default Value: 0

4.1.25 FLASHC_MPC0_ROT_BLK_LUT

(R,W,NS) bits for 8 blocks at ROT_BLK_IDX for PC=ROT_BKL_PC

Address: 0x42151218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	RW			None	RW		
Name	None	ATTR1 [6:4]			None	ATTR0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW			None	RW		
HW Access	None	RW			None	RW		
Name	None	ATTR3 [14:12]			None	ATTR2 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW			None	RW		
HW Access	None	RW			None	RW		
Name	None	ATTR5 [22:20]			None	ATTR4 [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW			None	RW		
HW Access	None	RW			None	RW		
Name	None	ATTR7 [30:28]			None	ATTR6 [26:24]		

Bits	Name	Description
30 : 28	ATTR7	W/R/NS bits for block 7 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
26 : 24	ATTR6	W/R/NS bits for block 6 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
22 : 20	ATTR5	W/R/NS bits for block 5 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
18 : 16	ATTR4	W/R/NS bits for block 4 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
14 : 12	ATTR3	W/R/NS bits for block 3 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
10 : 8	ATTR2	W/R/NS bits for block 2 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
6 : 4	ATTR1	W/R/NS bits for block 1 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
2 : 0	ATTR0	W/R/NS bits for block 0 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0

4.1.26 FLASHC_FM_CTL_RED_CTL01

Redundancy Control normal sectors 0,1

Address: 0x42152040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RED_ADDR_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RED_EN_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RED_ADDR_1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						RED_AXA	RED_EN_1

Bits	Name	Description
25	RED_AXA	'1': Redundancy Enable for SM Rows in Sector 1; Uses RED_ADDR_1 bits for Bad Row Pair Address Default Value: 0
24	RED_EN_1	'1': Redundancy Enable for Sector 1 Default Value: 0
23 : 16	RED_ADDR_1	Bad Row Pair Address for Sector 1 Default Value: 0
8	RED_EN_0	'1': Redundancy Enable for Sector 0 Default Value: 0
7 : 0	RED_ADDR_0	Bad Row Pair Address for Sector 0 Default Value: 0

4.1.27 FLASHC_FM_CTL_RED_CTL23

Redundancy Control normal sectors 2,3

Address: 0x42152044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RED_ADDR_2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RED_EN_2

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RED_ADDR_3 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							RED_EN_3

Bits	Name	Description
24	RED_EN_3	1': Redundancy Enable for Sector 3 Default Value: 0
23 : 16	RED_ADDR_3	Bad Row Pair Address for Sector 3 Default Value: 0
8	RED_EN_2	1': Redundancy Enable for Sector 2 Default Value: 0
7 : 0	RED_ADDR_2	Bad Row Pair Address for Sector 2 Default Value: 0

4.1.28 FLASHC_FM_CTL_FM_PL_DATA0

Flash macro Page Latches data

Address: 0x42152800

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Normal PL data read: four page latch Bytes When reading the page latches it requires FM_CTL.IF_SEL to be '1' Note: the high Voltage page latches are readable for test mode functionality. Default Value: 0

4.1.29 FLASHC_FM_CTL_FLASH_MACRO_CTL

Flash macro control

Address: 0x42152A10

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				FM_MODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						FM_SEQ [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DAA_MUX_SEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						WR_EN	IF_SEL

Bits	Name	Description
25	WR_EN	0: normal mode 1: Fm Write Enable Note: IF_SEL and WR_EN cannot be changed at the same time Default Value: 0
24	IF_SEL	Interface selection. Specifies the interface that is used for flash memory read operations: 0: R interface is used (default value). In this case, the flash memory address is provided as part of the R signal interface. 1: C interface is used. In this case, the flash memory address is provided by FM_MEM_ADDR (the page address) and by the C interface access offset in the FM_MEM_DATA structure. Note: IF_SEL and WR_EN cannot be changed at the same time Default Value: 0
23 : 16	DAA_MUX_SEL	Direct memory cell access address. Default Value: 0
9 : 8	FM_SEQ	Requires (IF_SEL|WR_EN)=1 Flash macro sequence selection Default Value: 0
3 : 0	FM_MODE	Requires (IF_SEL|WR_EN)=1 Flash macro mode selection Default Value: 0

4.1.30 FLASHC_FM_CTL_STATUS

Status

Address: 0x42152A14

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	R_GRANT_DE-LAY_STA-TUS	TIM-ER_PE_SY NC	IF-_SEL_MON	WR_EN_M ON	TURBO_N	ILLE-GAL_HVOP	HV_REGS_ ISOLATED	TIM-ER_STA-TUS

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	RE-SET_MM	SEC-TOR1_SR	ECC_CFG	RWW	NEG_PUM P_VHI	POS_PUM P_VLO	FM_READY	FM_BUSY

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	RQ_ER-ROR	CBUS_RED _ROW_EN	CBUS_RA_ MATCH	HVO-P_BULK_A LL	HVOP_-SECTOR	HVOP_-SUB_SEC-TOR_N	ROW_EVE N	ROW_ODD

Bits	31	30	29	28	27	26	25	24
SW Access	R				R			
HW Access	W				W			
Name	PUMP_NDAC [31:28]				PUMP_PDAC [27:24]			

Bits	Name	Description
31 : 28	PUMP_NDAC	Test_only, internal node: regif ndac outputs to pos pump Default Value: 0
27 : 24	PUMP_PDAC	Test_only, internal node: regif pdac outputs to pos pump Default Value: 0
23	RQ_ERROR	Test_only, internal node: rq_error sync-de in clk_c domain Default Value: 0
22	CBUS_RED_ROW_EN	Test_only, internal node: mpcon red_row_en Default Value: 0
21	CBUS_RA_MATCH	Test_only, internal node: mpcon ra match Default Value: 0
20	HVOP_BULK_ALL	Test_only, internal node: mpcon bk_all Default Value: 0
19	HVOP_SECTOR	Test_only, internal node: mpcon bk_sec Default Value: 0
18	HVOP_SUB_SECTOR_N	Test_only, internal node: mpcon bk_subb Default Value: 0

4.1.30 FLASHC_FM_CTL_STATUS (continued)

17	ROW_EVEN	Test_only, internal node: mpcon row_even Default Value: 0
16	ROW_ODD	Test_only, internal node: mpcon row_odd Default Value: 0
15	RESET_MM	Test_only, internal node: mpcon reset_mm Default Value: 0
14	SECTOR1_SR	0: Sector 1 does not contain special rows. The special rows are located in separate special sectors. 1: Sector 1 contains special rows Default Value: 0
13	ECC_CFG	Geometry ECC configuration: 0: FM with No ECC 1: FM with ECC Default Value: 0
12	RWW	FM Type (Read While Write or Not Read While Write): 0: Non RWW FM Type 1: RWW FM Type Default Value: 1
11	NEG_PUMP_VHI	NEG pump VHI Default Value: 1
10	POS_PUMP_VLO	POS pump VLO Default Value: 0
9	FM_READY	0: FM not ready 1: FM ready Default Value: 0
8	FM_BUSY	0': FM not busy 1: FM BUSY : R_GRANT is 0 as result of a busy request from FM ready, or from HV operations. Default Value: 0
7	R_GRANT_DELAY_STATUS	0: R_GRANT_DELAY timer is not running 1: R_GRANT_DELAY timer is running Default Value: 0
6	TIMER_PE_SYNC	The actual timer state sync-ed in clk_c domain: 0: timer is not running: 1: timer is running; Default Value: 0
5	IF_SEL_MON	FM_CTL.IF_SEL bit after being synchronized in clk_r domain Default Value: 0
4	WR_EN_MON	FM_CTL.WR_EN bit after being synchronized in clk_r domain Default Value: 0
3	TURBO_N	After FM power up indicates the analog blocks currents are boosted to faster reach their functional state.. Used in the testchip boot only as an "FM READY" flag. 0: turbo mode 1: normal mode Default Value: 0
2	ILLEGAL_HVOP	Indicates a bulk,sector erase, program has been requested when axa=1 0: no error 1: illegal HV operation error Default Value: 0
1	HV_REGS_ISOLATED	Indicates the isolation status at HV trim and redundancy registers inputs 0: Not isolated, writing permitted 1: isolated writing disabled Default Value: 0

4.1.30 FLASHC_FM_CTL_STATUS (continued)

0	TIMER_STATUS	This is the timer_en bit set by writing a "1" in the TIMER_CTL bit 31. It is reset by HW when the timer expires 0: timer not running 1: Timer is enabled and not expired yet Default Value: 0

4.1.31 FLASHC_FM_CTL_FM_ADDR

Flash macro address

Address: 0x42152A18

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	BA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							AXA

Bits	Name	Description
24	AXA	Auxiliairy address field: 0: regular flash memory. 1: supervisory flash memory. Default Value: 0
23 : 16	BA	Bank address. Default Value: 0
15 : 0	RA	Row address. Default Value: 0

4.1.32 FLASHC_FM_CTL_BOOKMARK

Bookmark register - keeps the current FW HV seq

Address: 0x42152A1C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BOOKMARK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	BOOKMARK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	BOOKMARK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	BOOKMARK [31:24]							

Bits	Name	Description
31 : 0	BOOKMARK	Used by FW. Keeps the Current HV cycle sequence Default Value: 0

4.1.33 FLASHC_FM_CTL_GEOMETRY

Regular flash geometry

Address: 0x42152A20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ROW_COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ROW_COUNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BANK_COUNT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R				R			
HW Access	W				W			
Name	PAGE_SIZE_LOG2 [31:28]				WORD_SIZE_LOG2 [27:24]			

Bits	Name	Description
31 : 28	PAGE_SIZE_LOG2	Number of Bytes per page (log 2): 0: 1 Byte 1: 2 Bytes 2: 4 Bytes ... 15: 32768 Bytes Default Value: 0x9 (512 bytes)
27 : 24	WORD_SIZE_LOG2	Number of Bytes per word (log 2). A word is defined as the data that is read from the flash macro over the R interface with a single read access: 0: 1 Byte 1: 2 Bytes 2: 4 Bytes ... 3: 128 Bytes Default Value: 0x4 (16 bytes)
23 : 16	BANK_COUNT	Number of banks (minus 1): 0: 1 bank 1: 2 banks ... "255": 256 banks Default Value: 0x01 (2 banks)

4.1.33 FLASHC_FM_CTL_GEOMETRY (continued)

15 : 0	ROW_COUNT	Number of rows (minus 1): 0: 1 row 1: 2 rows 2: 3 rows ... "65535": 65536 rows Default Value: 0x00FF (256 rows)

4.1.34 FLASHC_FM_CTL_GEOMETRY_SUPERVISORY

Supervisory flash geometry

Address: 0x42152A24

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ROW_COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ROW_COUNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BANK_COUNT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R				R			
HW Access	W				W			
Name	PAGE_SIZE_LOG2 [31:28]				WORD_SIZE_LOG2 [27:24]			

Bits	Name	Description
31 : 28	PAGE_SIZE_LOG2	Number of Bytes per page (log 2). See GEOMETRY.PAGE_SIZE_LOG2. Typically, PAGE_-SIZE_LOG2 equals GEOMETRY.PAGE_SIZE_LOG2. Default Value: 0x9
27 : 24	WORD_SIZE_LOG2	Number of Bytes per word (log 2). See GEOMETRY.WORD_SIZE_LOG2. Typically, WORD_-SIZE_LOG2 equals GEOMETRY.WORD_SIZE_LOG2. Default Value: 0x4
23 : 16	BANK_COUNT	Number of banks (minus 1). BANK_COUNT is less or equal to GEOMETRY.BANK_COUNT. Default Value: 0
15 : 0	ROW_COUNT	Number of rows (minus 1). ROW_COUNT is typically less than GEOMETRY.ROW_COUNT Default Value: 0x003F

4.1.35 FLASHC_FM_CTL_ANA_CTL0

Analog control 0

Address: 0x42152A28

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW						
HW Access	R	R						
Name	SPARE_ANA_CTL0	MDAC [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW	RW	R	RW
HW Access	R				R	RW	R	R
Name	NDAC_MIN [15:12]				FLIP_AMUXBUS_AB	RST_SFT_HVPL	DNU_2_TM_ECC_DIS	ECC_ENC_DIS

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW		RW			
HW Access	R		R		R			
Name	SCALE_PRG_SEQ12 [23:22]		SCALE_PRG_SEQ01 [21:20]		PDAC_MIN [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	SCALE_PRG_PEOFF [31:30]		SCALE_PRG_PEON [29:28]		SCALE_SEQ30 [27:26]		SCALE_PRG_SEQ23 [25:24]	

Bits	Name	Description
31 : 30	SCALE_PRG_PEOFF	PROG_PROG: Scale for R_GRANT_DELAY on PE OFF transition: 00: 0.125uS 01: 1uS 10: 10uS 11: 100uS Default Value: 0
29 : 28	SCALE_PRG_PEON	PROG_PROG: Scale for R_GRANT_DELAY on PE On transition: 00: 0.125uS 01: 1uS 10: 10uS 11: 100uS Default Value: 0
27 : 26	SCALE_SEQ30	PROG_PROG& ERASE: Scale for R_GRANT_DELAY on seq3-seq0 transition: 00: 0.125uS 01: 1uS 10: 10uS 11: 100uS Default Value: 0

4.1.35 FLASHC_FM_CTL_ANA_CTL0 (continued)

25 : 24	SCALE_PRG_SEQ23	PROG_PROG: Scale for R_GRANT_DELAY on seq2-seq3 transition: 00: 0.125uS 01: 1uS 10: 10uS 11: 100uS Default Value: 0
23 : 22	SCALE_PRG_SEQ12	PROG_PROG: Scale for R_GRANT_DELAY on seq1-seq2 transition: 00: 0.125uS 01: 1uS 10: 10uS 11: 100uS Default Value: 0
21 : 20	SCALE_PRG_SEQ01	PROG_PROG: Scale for R_GRANT_DELAY on seq0-seq1 transition: 00: 0.125uS 01: 1uS 10: 10uS 11: 100uS Default Value: 0
19 : 16	PDAC_MIN	PDAC staircase min value Default Value: 0x0
15 : 12	NDAC_MIN	NDAC staircase min value Default Value: 0x0
11	FLIP_AMUXBUS_AB	Flips amuxbusa and amuxbusb 0: amuxbusa, amuxbusb 1: amuxbusb, amuxbusb Default Value: 0
10	RST_SFT_HVPL	1: Page Latches Soft Reset Default Value: 0
9	DNU_2_TM_ECC_DIS	Do Not Use this bit as it is for test Mode use only. Write only to 0 in normal mode (tm_ecc_dis in RTL) Default Value: 0
8	ECC_ENC_DIS	0': ECC encoder is enabled for the FM with ECC feature. The PL ECC bits are loaded automatically '1': ECC encoder disabled. - The Macro needs to be in C-BUS mode - IF_SEL=1 to write and keep this bit at 1 Default Value: 0
7	SPARE_ANA_CTL0	Spare bit Default Value: 0
6 : 0	MDAC	Trimming of the output margin Voltage as a function of Vpos and Vneg. Default Value: 0

4.1.36 FLASHC_FM_CTL_ANA_CTL1

Analog control 1

Address: 0x42152A2C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	NDAC_STEP [7:4]				NDAC_MAX [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	PDAC_STEP [15:12]				PDAC_MAX [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	NPDAC_STEP_TIME [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	NPDAC_ZERO_TIME [31:24]							

Bits	Name	Description
31 : 24	NPDAC_ZERO_TIME	Ndac/Pdac LO duration: (1uS .. 255uS) * 8 When 0, N/PDAC don't return to 0 Default Value: 0x0D
23 : 16	NPDAC_STEP_TIME	Ndac/Pdac step duration: (1uS .. 255uS) * 8 When = 0 N/PDAC_MAX control the pumps Default Value: 0x32
15 : 12	PDAC_STEP	Pdac step increment Default Value: 0xF
11 : 8	PDAC_MAX	Pdac Max Value.Trimming of positive pump output Voltage: Default Value: 0xA
7 : 4	NDAC_STEP	Ndac step increment Default Value: 0xF
3 : 0	NDAC_MAX	Ndac Max Value.Trimming of negative pump output Voltage. Default Value: 0xA

4.1.37 FLASHC_FM_CTL_FM_PL_WRDATA_ALL

Flash macro write page latches all

Address: 0x42152A30

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Write all high Voltage page latches with the same 32-bit data in a single write cycle. In order to also write same lower 8bit from 32-bit data to all the ECC bits in the page latches, set ANA_CTL0.ECC_ENC_DIS=1. Read always returns 0. Used for test mode and sims only Default Value: 0

4.1.38 FLASHC_FM_CTL_FM_REFRESH_ADDR

Address bit to point to scratch area

Address: 0x42152A34

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None			RW
HW Access	None			R	None			R
Name	None [7:5]			FM_CXA	None [3:1]			FM_BXA

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	FM_CXA	Address bit to point to Column 33 0: Point to normal columns in sector 1: Point to Column 33 used for BL Disturb Counter. For engineering use only. Default Value: 0
0	FM_BXA	Address bit to point to scratch area 0: Point to normal rows in sector 1: Point to scratch rows in sector. For engineering use only. Default Value: 0

4.1.39 FLASHC_FM_CTL_RGRANT_DELAY_ERS

R-grant delay for erase

Address: 0x42152A38

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RGRANT_DELAY_ERS_SEQ01 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RGRANT_DELAY_ERS_SEQ12 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RGRANT_DELAY_ERS_SEQ23 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	RGRANT_DELAY_ERS_SEQ23	ERASE: R-grant blocking delay on seq2-seq3 transition. Scale = ANA_CTL0.SCALE_SEQ23 When = 0 R_GRANT_DELAY control is disabled when IF_SEL=1 R_GRANT_DELAY control is disabled Default Value: 0
15 : 8	RGRANT_DELAY_ERS_SEQ12	ERASE: R-grant blocking delay on seq1-seq2 transition. Scale = ANA_CTL0.SCALE_SEQ12 When = 0 R_GRANT_DELAY control is disabled when IF_SEL=1 R_GRANT_DELAY control is disabled Default Value: 0
7 : 0	RGRANT_DELAY_ERS_SEQ01	ERASE: R-grant blocking delay on seq0-seq1 transition. Scale = ANA_CTL0.SCALE_SEQ01 When = 0 R_GRANT_DELAY control is disabled when IF_SEL=1 R_GRANT_DELAY control is disabled Default Value: 0

4.1.40 FLASHC_FM_CTL_RGRANT_SCALE_ERS

R-grant delay scale for erase

Address: 0x42152A3C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	SCALE_ERS_PEON [7:6]		SCALE_ERS_SEQ23 [5:4]		SCALE_ERS_SEQ12 [3:2]		SCALE_ERS_SEQ01 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SCALE_ERS_PEOFF [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RGRANT_DELAY_ERS_PEON [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	RGRANT_DELAY_ERS_PEOFF [31:24]							

Bits	Name	Description
31 : 24	RGRANT_DELAY_ERS_PEOFF	ERASE: R-grant blocking delay on PE OFF. Scale = ANA_CTL0.SCALE_PEOFF When = 0 R_GRANT_DELAY control is disabled when IF_SEL=1 R_GRANT_DELAY control is disabled Default Value: 0
23 : 16	RGRANT_DELAY_ERS_PEON	ERASE: R-grant blocking delay on PE ON. Scale = ANA_CTL0.SCALE_PEON When = 0 R_GRANT_DELAY control is disabled when IF_SEL=1 R_GRANT_DELAY control is disabled Default Value: 0
9 : 8	SCALE_ERS_PEOFF	ERASE: Scale for R_GRANT_DELAY on PE OFF transition: '00': 0.125uS '01': 1uS '10': 10uS '11': 100uS Default Value: 0
7 : 6	SCALE_ERS_PEON	ERASE: Scale for R_GRANT_DELAY on PE On transition: '00': 0.125uS '01': 1uS '10': 10uS '11': 100uS Default Value: 0
5 : 4	SCALE_ERS_SEQ23	ERASE: Scale for R_GRANT_DELAY on seq2-seq3 transition: '00': 0.125uS '01': 1uS '10': 10uS '11': 100uS Default Value: 0

4.1.40 FLASHC_FM_CTL_RGRANT_SCALE_ERS (continued)

3 : 2	SCALE_ERS_SEQ12	ERASE: Scale for R_GRANT_DELAY on seq1-seq2 transition: '00': 0.125uS '01': 1uS '10': 10uS '11': 100uS Default Value: 0
1 : 0	SCALE_ERS_SEQ01	ERASE: Scale for R_GRANT_DELAY on seq0-seq1 transition: '00': 0.125uS '01': 1uS '10': 10uS '11': 100uS Default Value: 0

4.1.41 FLASHC_FM_CTL_PW_SEQ23

HV Pulse Delay for seq2 post & seq3

Address: 0x42152A40

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PW_SEQ2_POST [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PW_SEQ2_POST [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	PW_SEQ3 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	PW_SEQ3 [31:24]							

Bits	Name	Description
31 : 16	PW_SEQ3	Seq3 delay Default Value: 0
15 : 0	PW_SEQ2_POST	Seq2 post delay Default Value: 0

4.1.42 FLASHC_FM_CTL_PW_SEQ12

HV Pulse Delay for seq 1&2 pre

Address: 0x42152A44

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PW_SEQ1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PW_SEQ1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	PW_SEQ2_PRE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	PW_SEQ2_PRE [31:24]							

Bits	Name	Description
31 : 16	PW_SEQ2_PRE	Seq2 pre delay Default Value: 0
15 : 0	PW_SEQ1	Seq1 delay Default Value: 0

4.1.43 FLASHC_FM_CTL_WAIT_CTL

Wait State control

Address: 0x42152A48

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				WAIT_FM_MEM_RD [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				WAIT_FM_HV_RD [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					R		
Name	None [23:19]					WAIT_FM_HV_WR [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW	None		RW	RW	
HW Access	None		R	None		R	R	
Name	None [31:30]		PL_SOFT-_SET_EN	None [28:27]		LV_SPARE_1	FM_RWW_MODE [25:24]	

Bits	Name	Description
29	PL_SOFT_SET_EN	Page latch soft set enable, 0 = disabled, 1 = enabled (at end of seq_2), taken care in API Default Value: 0
26	LV_SPARE_1	Spare register Default Value: 0
25 : 24	FM_RWW_MODE	2'b00: Full CBUS MODE 2'b01: RWW 2'b10: RWW. R_GRANT is stalling r_bus for the whole program/erase duration Default Value: 0
18 : 16	WAIT_FM_HV_WR	Number of C interface wait cycles (on "clk_c") for a write to the Page Latches. Default Value: 3
11 : 8	WAIT_FM_HV_RD	Number of C interface wait cycles (on "clk_c") for a read from the Page Latches. Common for reading HV Page Latches and the DATA_COMP_RESULT bit Default Value: 11
3 : 0	WAIT_FM_MEM_RD	Number of C interface wait cycles (on "clk_c") for a read from the memory Default Value: 9

4.1.44 FLASHC_FM_CTL_RGRANT_DELAY_PRG

R-grant delay for program

Address: 0x42152A4C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RGRANT_DELAY_PRG_SEQ12 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RGRANT_DELAY_PRG_SEQ23 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RGRANT_DELAY_SEQ30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None			RW			
HW Access	R	None			R			
Name	HV_PARAMS_LOADED	None [30:28]			RGRANT_DELAY_CLK [27:24]			

Bits	Name	Description
31	HV_PARAMS_LOADED	0': HV Pulse common params not loaded '1': HV Pulse common params loaded: r-grant delays, r-grant scale, prescaler, timer values for seq1,seq2_pre, seq2_post, seq3 Default Value: 0
27 : 24	RGRANT_DELAY_CLK	Frequency divider from clk_t to create the 8MHz reference clock for R_grant delay. The value of 0 is equivalent with 1. If the clock clk_t = 8MHz the value needs to be 1 The value of this field is the integer result of "clk_t frequency / 8". Example: for clk_t=100 this field is INT(100/8) =12. This field is updated at runtime with the "SW_RGRANT_DELAY_CLK " value from the HV parameters table Default Value: 0
23 : 16	RGRANT_DELAY_SEQ30	PROG_PROG & ERASE: R-grant blocking delay on seq3-seq0 transition. Scale = ANA_CTL0.SCALE_SEQ30 When = 0 R_GRANT_DELAY control is disabled when IF_SEL=1 R_GRANT_DELAY control is disabled Default Value: 0
15 : 8	RGRANT_DELAY_PRG_SEQ23	PROG_PROG: R-grant blocking delay on seq2-seq3 transition. Scale = ANA_CTL0.SCALE_SEQ23 When = 0 R_GRANT_DELAY control is disabled when IF_SEL=1 R_GRANT_DELAY control is disabled Default Value: 0

4.1.44 FLASHC_FM_CTL_RGRANT_DELAY_PRG (continued)

7 : 0	RGRANT_DE-LAY_PRG_SEQ12	PROG_PROG: R-grant blocking delay on seq1-seq2 transition. Scale = ANA_CTL0.SCALE_SEQ12 When = 0 R_GRANT_DELAY control is disabled when IF_SEL=1 R_GRANT_DELAY control is disabled Default Value: 0

4.1.45 FLASHC_FM_CTL_TIMER_CLK_CTL

Timer prescaler (clk_t to timer clock frequency divider)

Address: 0x42152A50

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TIMER_CLOCK_FREQ [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RGRANT_DELAY_PRG_PEON [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RGRANT_DELAY_PRG_PEOFF [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	RGRANT_DELAY_PRG_SEQ01 [31:24]							

Bits	Name	Description
31 : 24	RGRANT_DELAY_PRG_SEQ01	PROG_PROG: R-grant blocking delay on seq0-seq1 transition. Scale = ANA_CTL0.SCALE_SEQ01 When = 0 R_GRANT_DELAY control is disabled when IF_SEL=1 R_GRANT_DELAY control is disabled Default Value: 0
23 : 16	RGRANT_DELAY_PRG_PEOFF	PROG_PROG: R-grant blocking delay on PE OFF. Scale = ANA_CTL0.SCALE_PEOFF When = 0 R_GRANT_DELAY control is disabled when IF_SEL=1 R_GRANT_DELAY control is disabled Default Value: 0
15 : 8	RGRANT_DELAY_PRG_PEON	PROG_PROG: R-grant blocking delay on PE ON. Scale = ANA_CTL0.SCALE_PEON When = 0 R_GRANT_DELAY control is disabled when IF_SEL=1 R_GRANT_DELAY control is disabled Default Value: 0
7 : 0	TIMER_CLOCK_FREQ	Clk_t frequency divider to provide the 1MHz reference clock for the Regif Timer. Equal to the frequency in MHz of the timer clock "clk_t". Example: if "clk_t" has a frequency of 4 MHz then this field value is "4" Max clk_t frequency = 100MHz. This field is updated at runtime with the "SW_TIMER_CLOCK_FREQ " value from the HV parameters table Default Value: 0x08

4.1.46 FLASHC_FM_CTL_TIMER_CTL

Timer control

Address: 0x42152A54

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW						
HW Access	R	R						
Name	SCALE	PERIOD [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	None		RW	RW	RW
HW Access	RW0C	RW0C	RW0C	None		R	R	RW
Name	TIMER_EN	ACLK_EN	PUMP_EN	None [28:27]		PRE_PROG_CSL	PRE_PROG	AUTO_SEQUENCE

Bits	Name	Description
31	TIMER_EN	Timer enable: 0: disabled 1: enabled. SW sets this field to "1" to start the timer. HW sets this field to "0" when the timer is expired. Default Value: 0
30	ACLK_EN	ACLK enable (generates a single cycle pulse for the FM): 0: disabled 1: enabled. SW set this field to "1" to generate a single cycle pulse. HW sets this field to "0" when the pulse is generated. Default Value: 0
29	PUMP_EN	Pump enable: 0: disabled 1: enabled (also requires FM_CTL.IF_SEL to be"1", this additional restriction is required to prevent non intentional clearing of the FM). SW sets this field to "1" to generate a single PE pulse. HW clears this field when timer is expired. Default Value: 0
26	PRE_PROG_CSL	0: CSL lines driven by MDAC 1: CSL lines driven by VNEG_G Default Value: 1
25	PRE_PROG	1 during pre-program operation Default Value: 0

4.1.46 FLASHC_FM_CTL_TIMER_CTL (continued)

24	AUTO_SEQUENCE	1': Starts1 the HV automatic sequencing Cleared by HW Default Value: 0
15	SCALE	Timer tick scale: 0: 1 microsecond. 1: 100 microseconds. Default Value: 0
14 : 0	PERIOD	Timer period in either microseconds (SCALE is '0') or 100's of microseconds (SCALE is '1') multiples. Default Value: 1

4.1.47 FLASHC_FM_CTL_ACLK_CTL

MPCON clock

Address: 0x42152A58

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							W
HW Access	None							R
Name	None [7:1]							ACLK_GEN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	ACLK_GEN	Write '1b1' to generate one clock pulse for HV control registers (mpcon outputs) Default Value: 0x0

4.1.48 FLASHC_FM_CTL_INTR

Interrupt

Address: 0x42152A5C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [7:1]							TIMER_EXPIRED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER_EXPIRED	Set to '1', when event is detected. Write INTR field with '1', to clear bit. Write INTR_SET field with '1', to set bit. Default Value: 0

4.1.49 FLASHC_FM_CTL_INTR_SET

Interrupt set

Address: 0x42152A60

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							A
Name	None [7:1]							TIMER_EXPIRED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER_EXPIRED	Write INTR_SET field with "1" to set corresponding INTR field (a write of "0" has no effect). Default Value: 0

4.1.50 FLASHC_FM_CTL_INTR_MASK

Interrupt mask

Address: 0x42152A64

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TIMER_EXPIRED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER_EXPIRED	Mask for corresponding field in INTR register. Default Value: 0

4.1.51 FLASHC_FM_CTL_INTR_MASKED

Interrupt masked

Address: 0x42152A68

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							TIMER_EXPIRED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER_EXPIRED	Logical and of corresponding request and mask fields. Default Value: 0

4.1.52 FLASHC_FM_CTL_CAL_CTL0

Cal control - VCT, VBG, CDAC, IPREF

Address: 0x42152A6C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				
HW Access	R			R				
Name	CDAC_HV [7:5]			VCT_TRIM_HV [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW					
HW Access	R		R					
Name	VBG_TC_TRIM_HV [15:14]		VBG_TRIM_HV [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW	RW	RW	
HW Access	None				R	R	R	
Name	None [23:20]				SPARE_CTL0_HV	IPREF_TRIMA_HV	VBG_TC_TRIM_HV [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19	SPARE_CTL0_HV	Spare trim bits, DNU Default Value: 0x0
18	IPREF_TRIMA_HV	Adds 100-150nA boost on IPREF Default Value: 0x0
17 : 14	VBG_TC_TRIM_HV	Bandgap Voltage Temperature Compensation trim control Default Value: 0x5
13 : 8	VBG_TRIM_HV	Bandgap Voltage trim control. Default Value: 0x2D
7 : 5	CDAC_HV	Temperature compensated trim DAC. To control Vctat slope for VNEG. Default Value: 0x4
4 : 0	VCT_TRIM_HV	Bandgap Voltage Temperature Compensation trim control. Default Value: 0x16

4.1.53 FLASHC_FM_CTL_CAL_CTL1

Cal control - ICREF, IPREF

Address: 0x42152A70

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW					
HW Access	R		R					
Name	ICREF_TC_TRIM_HV [7:6]		ICREF_TRIM_HV [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW					RW	
HW Access	R	R					R	
Name	IP-REF_TC_HV	IPREF_TRIM_HV [14:10]					ICREF_TC_TRIM_HV [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW	RW		
HW Access	None				R	R		
Name	None [23:20]				SPARE_CTL1_HV	IPREF_TC_HV [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19	SPARE_CTL1_HV	Spare trim bit, DNU Default Value: 0x0
18 : 15	IPREF_TC_HV	IPREF Slope Control Default Value: 0x8
14 : 10	IPREF_TRIM_HV	Bandgap IPTAT trim control. Default Value: 0xF
9 : 6	ICREF_TC_TRIM_HV	Bandgap Current Temperature Compensation trim control Default Value: 0x3
5 : 0	ICREF_TRIM_HV	Bandgap Current trim control. Default Value: 0x27

4.1.54 FLASHC_FM_CTL_CAL_CTL2

Cal control - IDAC, IBS_CTL, LAT_DIS

Address: 0x42152A74

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	IDAC_ULP_HV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW						RW	RW
HW Access	R						R	R
Name	IDAC_LP_HV [15:10]						VREF_SEL_ULP_HV	SPARE_ULP_CTL2_HV

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW	RW	RW	
HW Access	None				R	R	R	
Name	None [23:20]				VREF_SEL_LP_HV	SPARE_LP_CTL2_HV	IDAC_LP_HV [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19	VREF_SEL_LP_HV	0: Uses VBG as reference for VLIM - LP Mode 1: Uses VCTAT as reference for VLIM - LP mode Default Value: 0x0
18	SPARE_LP_CTL2_HV	Spare bit to be used in LP configuration Default Value: 0x0
17 : 10	IDAC_LP_HV	Sets the sense current reference offset value. Refer to trim tables for details. Default Value: 0x28
9	VREF_SEL_ULP_HV	0: Uses VBG as reference for VLIM - ULP Mode 1: Uses VCTAT as reference for VLIM - ULP mode Default Value: 0x0
8	SPARE_ULP_CTL2_HV	Spare bit to be used in ULP configuration Default Value: 0x0
7 : 0	IDAC_ULP_HV	Sets the sense current reference offset value. Refer to trim tables for details. Default Value: 0x28

4.1.55 FLASHC_FM_CTL_CAL_CTL3

Cal control - OSC trims, FDIV, REG_ACT, TURBO, LP_ULP_SW

Address: 0x42152A78

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW			
HW Access	R	R	R	R	R			
Name	LAT_DIS3_HV	OSC_-TEMP-CO_HV	VPROT_ACT_HV	OS-C_RANGE_TRIM_HV	OSC_TRIM_HV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW		RW	RW		RW	RW
HW Access	R	R		R	R		R	R
Name	IOSC_TRIM_HV	TURBO_PULSEW_HV [14:13]		VDDHI_HV	FDIV_TRIM_HV [11:10]		REG_ACT_HV	PM_EN_HV

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [23:20]				LP_ULP_SW_HV	R_GRANT_EN_HV	CL_ISO_DIS_HV	IOSC_TRIM_HV

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19	LP_ULP_SW_HV	LP<-->ULP switch for trim signals: 0: LP 1: ULP Default Value: 0x0
18	R_GRANT_EN_HV	0: r_grant handshake disabled, r_grant always 1. 1: r_grant handshake enabled Default Value: 0x0
17	CL_ISO_DIS_HV	0: The internal logic controlls the CL isolation 1: Forces CL bypass Default Value: 0x0
16 : 15	IOSC_TRIM_HV	Oscillator Bias Current Trim during Standby 0.33 uA -- 1.65 uA Default Value: 0x0
14 : 13	TURBO_PULSEW_HV	Turbo pulse width trim (Typical) 00: 40 us 01: 20 us 10: 15 us 11: 8 us Default Value: 0x1

4.1.55 FLASHC_FM_CTL_CAL_CTL3 (continued)

12	VDDHI_HV	0: vdd < 2.3V 1: vdd >= 2.3V '0' setting can used for vdd > 2.3V also, but with a current penalty. Default Value: 0x0
11 : 10	FDIV_TRIM_HV	FDIV_TRIM_HV[1:0]: Assuming oscillator frequency of 8MHz in standby. Following are the clock frequencies seen by doubler 00: F = 0.5MHz 01: F = 1MHz 10: F = 2MHz 11: F = 4MHz Default Value: 0x1
9	REG_ACT_HV	0: VBST regulator will operate in active/standby mode based on control signal. 1: Forces the VBST regulator in active mode all the time Default Value: 0x1
8	PM_EN_HV	0: Sense Amp bias similar to _ver2 1: pbias enabled in Sense Amp for Better Margin Default Value: 0x1
7	LAT_DIS3_HV	0: Enable saen3 control for data out latches 1: Disable saen3 control for data out latches Default Value: 0x1
6	OSC_TEMPCO_HV	0: Uses VBG as reference 1: Uses VCTAT as reference Default Value: 0x0
5	VPROT_ACT_HV	Forces VPROT in active mode all the time Default Value: 0x0
4	OSC_RANGE_TRIM_HV	0: Oscillator Low Frequency range 1: Oscillator High Frequency Range Default Value: 0x1
3 : 0	OSC_TRIM_HV	Flash macro pump clock trim control. Default Value: 0x4

4.1.56 FLASHC_FM_CTL_CAL_CTL4

Cal control - VLIM, IDAC, SDAC, ITIM ULP trims

Address: 0x42152A7C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW		RW			RW	
HW Access	R	R		R			R	
Name	ITIM_ULP_HV	SDAC_ULP_HV [6:5]		SPARE_CTL4_ULP_HV [4:2]			VLIM_TRIM_ULP_HV [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW		RW				
HW Access	R	R		R				
Name	SA_CTL_TRIM_T8_ULP_HV	FM_READY_DEL_ULP_HV [14:13]		ITIM_ULP_HV [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [23:20]				UGB_EN_HV	AUTO_HVPULSE_HV	VBST_S_DIS_HV	READY_RESTART_N_HV

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19	UGB_EN_HV	UGB enable in TM control Default Value: 0x0
18	AUTO_HVPULSE_HV	0: HV Pulse controlled by FW 1: HV Pulse controlled by Hardware Default Value: 0x0
17	VBST_S_DIS_HV	0: VBST_S voltage for each sector to allow VBST level to be dropped to VCC during Erase in the selected sector, reducing coupling to GBL. 1: VBST_S voltage for each sector stays at VBST level during Erase in the selected sector. Default Value: 0x0
16	READY_RESTART_N_HV	Toggle: 1-->0, ready goes low, ready will remain low as long as the bit is low. Toggle the bit back to 1 to activate the ready logic. To be used by API only. Default Value: 0x1
15	SA_CTL_TRIM_T8_ULP_HV	saen3 pulse width trim (Current trim) Default Value: 0x1
14 : 13	FM_READY_DEL_ULP_HV	00: Default : delay 1ns 01: Delayed by 1.5us 10: Delayed by 2.0us 11: Delayed by 2.5us Default Value: 0x0

4.1.56 FLASHC_FM_CTL_CAL_CTL4 (continued)

12 : 7	ITIM_ULP_HV	Trimming of timing current Default Value: 0x1E
6 : 5	SDAC_ULP_HV	Sets the sense current reference temp slope. Refer to trim tables for details. Default Value: 0x1
4 : 2	SPARE_CTL4_ULP_HV	Default Value: 0x0
1 : 0	VLIM_TRIM_ULP_HV	VLIM_TRIM[1:0]: 00: V2 = 650mV 01: V2 = 700mV 10: V2 = 750mV - Default 11: V2 = 800mV Default Value: 0x2

4.1.57 FLASHC_FM_CTL_CAL_CTL5

Cal control - VLIM, IDAC, SDAC, ITIM LP trims

Address: 0x42152A80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW		RW			RW	
HW Access	R	R		R			R	
Name	ITIM_LP_HV	SDAC_LP_HV [6:5]		SPARE_CTL5_LP_HV [4:2]			VLIM_TRIM_LP_HV [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW		RW				
HW Access	R	R		R				
Name	SA_CTL_TRIM_T8_LP_HV	FM_READY_DEL_LP_HV [14:13]		ITIM_LP_HV [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [23:20]				AMUX_SEL_HV [19:18]		SPARE2_CTL5_LP_HV [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 18	AMUX_SEL_HV	Amux Select in AMUX_UGB 00: Bypass UGB for both amuxbusa and amuxbusb 01: Bypass UGB for amuxbusb while passing amuxbusa through UGB. 10: Bypass UGB for amuxbusa while passing amuxbusb through UGB. 11: UGB Calibrate mode Default Value: 0x0
17 : 16	SPARE2_CTL5_LP_HV	Spare Bit, not used Default Value: 0x0
15	SA_CTL_TRIM_T8_LP_HV	saen3 pulse width trim (Current trim) Default Value: 0x0
14 : 13	FM_READY_DEL_LP_HV	00: Delayed by 1us 01: Delayed by 1.5us 10: Delayed by 2.0us 11: Delayed by 2.5us Default Value: 0x0
12 : 7	ITIM_LP_HV	Trimming of timing current Default Value: 0x28
6 : 5	SDAC_LP_HV	Sets the sense current reference temp slope. Refer to trim tables for details. Default Value: 0x1
4 : 2	SPARE_CTL5_LP_HV	Spare Bit, not used Default Value: 0x0

4.1.57 FLASHC_FM_CTL_CAL_CTL5 (continued)

1 : 0	VLIM_TRIM_LP_HV	VLIM_TRIM[1:0]: 00: V2 = 650mV 01: V2 = 700mV 10: V2 = 750mV - Default 11: V2 = 800mV Default Value: 0x2

4.1.58 FLASHC_FM_CTL_CAL_CTL6

Cal control - SA CTL LP/ULP trims

Address: 0x42152A84

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	SA_CTL_TRIM_T5_ULP_HV [7:5]			SA_CTL_TRIM_T4_ULP_HV [4:2]			SA_CT-L_TRIM_T1_ULP_HV [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW		RW	
HW Access	R	R			R		R	
Name	SA_CT-L_TRIM_T5_LP_HV	SA_CTL_TRIM_T4_LP_HV [14:12]			SA_CT-L_TRIM_T1_LP_HV [11:10]		SA_CT-L_TRIM_T6_ULP_HV [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [23:20]				SA_CT-L_TRIM_T6_LP_HV [19:18]		SA_CT-L_TRIM_T5_LP_HV [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 18	SA_CT-L_TRIM_T6_LP_HV	SA_CTL_TRIM_T6_LP_HV<1>= eni (enable current trim) SA_CTL_TRIM_T6_LP_HV<0> = ecn (enable cap trim) Default Value: 0x1
17 : 15	SA_CT-L_TRIM_T5_LP_HV	SA_CTL_TRIM_T5_LP_HV<2>= evi (integration current trim) SA_CTL_TRIM_T5_LP_HV<1:0> = evc (integration cap trim) Default Value: 0x5
14 : 12	SA_CT-L_TRIM_T4_LP_HV	SA_CTL_TRIM_T4_LP_HV<2>= eqi (eq current trim) SA_CTL_TRIM_T4_LP_HV<1:0> = eqc (eq cap trim) Default Value: 0x4
11 : 10	SA_CT-L_TRIM_T1_LP_HV	clk_trk delay Default Value: 0x2
9 : 8	SA_CT-L_TRIM_T6_ULP_HV	SA_CTL_TRIM_T6_ULP_HV<1>= eni (enable current trim) SA_CTL_TRIM_T6_ULP_HV<0> = ecn (enable cap trim) Default Value: 0x2
7 : 5	SA_CT-L_TRIM_T5_ULP_HV	SA_CTL_TRIM_T5_ULP_HV<2>= evi (integration current trim) SA_CTL_TRIM_T5_ULP_HV<1:0> = evc (integration cap trim) Default Value: 0x6
4 : 2	SA_CT-L_TRIM_T4_ULP_HV	SA_CTL_TRIM_T4_ULP_HV<2>= eqi (eq current trim) SA_CTL_TRIM_T4_ULP_HV<1:0> = eqc (eq cap trim) Default Value: 0x5

4.1.58 FLASHC_FM_CTL_CAL_CTL6 (continued)

1 : 0	SA_CT- L_TRIM_T1_ULP_HV	clk_trk delay Default Value: 0x3

4.1.59 FLASHC_FM_CTL_CAL_CTL7

Cal control - ERSX8_CLK_SEL, FM_ACTIVE, TURBO_EXT

Address: 0x42152A88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	
HW Access	R	R	R	R	R	R	R	
Name	READY_DEL_HV	ERSX-8_EN_ALL_HV	FM_READY_DIS_HV	NP-DAC_HWCTL_DIS_HV	TUR-BO_EX-T_HV	FM_AC-TIVE_HV	ERSX8_CLK_SEL_HV [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW		RW	
HW Access	R	R			R		R	
Name	PTRIM_LP_HV	SPARE2_CTL7_ULP_HV [14:12]			PTRIM_ULP_HV [11:10]		SPARE_CTL7_HV [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			RW
HW Access	None				R			R
Name	None [23:20]				SPARE3_CTL7_LP_HV [19:17]			PTRIM_LP_HV

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 17	SPARE3_CTL7_LP_HV	Default Value: 0x0
16 : 15	PTRIM_LP_HV	SA PBIAS Trim for LP Operation Default Value: 0x3
14 : 12	SPARE2_CTL7_ULP_HV	Default Value: 0x0
11 : 10	PTRIM_ULP_HV	SA PBIAS Trim for ULP Operation Default Value: 0x3
9 : 8	SPARE_CTL7_HV	Default Value: 0x0
7	READY_DEL_HV	0: Ready Delay trim. 1: Ready Delay trim. Default Value: 0x0
6	ERSX8_EN_ALL_HV	0': Staggered turn on/off of GWL 1: GWL are turned on/off at the same time (old FM legacy) Default Value: 0x0
5	FM_READY_DIS_HV	0': fm ready is enabled 1: fm ready is disabled (fm_ready is always "1") Default Value: 0x0
4	NPDAC_HWCTL_DIS_HV	0': ndac, pdac staircase hardware controlled 1: ndac, pdac staircase disabled. Enables FW control. Default Value: 0x0

4.1.59 FLASHC_FM_CTL_CAL_CTL7 (continued)

3	TURBO_EXT_HV	0: Normal operation 1: Uses external turbo pulse Default Value: 0x0
2	FM_ACTIVE_HV	0: Normal operation 1: Forces FM SYS in active mode Default Value: 0x0
1 : 0	ERSX8_CLK_SEL_HV	Clock frequency into the ersx8 shift register block 00: Oscillator clock 01: Oscillator clock / 2 10: Oscillator clock / 4 11: Oscillator clock / 8 Default Value: 0x0

4.1.60 FLASHC_FM_CTL_FM_PL_ECC0

Flash macro Page Latches ECC

Address: 0x42152B00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA9 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							DATA9

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	DATA9_1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							R
Name	None [31:25]							DATA9_1

Bits	Name	Description
24 : 16	DATA9_1	ECC encoder output. Can be read any time at address 0xa00 Default Value: 0
8 : 0	DATA9	if_sel must be 1 Normal PL ECC data read: one page latch Byte When reading the page latches it requires FM_CTL.IF_SEL to be '1' Note: the high Voltage page latches are readable for test mode functionality. Only even addresses, address step =8. Default Value: 0

4.1.61 FLASHC_FM_CTL_FM_MEM_DATA0

Flash macro memory sense amplifier data

Address: 0x42152C00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Sense amplifier and column multiplexer structure Bytes. The read data is dependent on FM_CTL.IF_SEL - IF_SEL is 0: data as specified by the R interface address; If accessed when IF_SEL=0, the data read is not valid. - IF_SEL is 1: data as specified by FM_MEM_ADDR and the offset of the accessed FM_MEM_-DATA register. Four FM data out Bytes. Each access is a full FM core read through C-BUS. The row address is given by the FM_ADDRESS register, the word and column addresses are driven by c_addr bus. Default Value: 0

4.1.62 FLASHC_FM_CTL_FM_MEM_ECC0

Flash macro memory sense amplifier ECC.

Address: 0x42152F00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ECC_PARITY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							ECC_PARI-TY

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8 : 0	ECC_PARITY	Sense amplifier ECC Bits. FM_CTL.IF_SEL must be 1. FM ECC data. Each access is a full FM core read through C-BUS. The row address is given by the FM_ADDRESS register, the word and column addresses are driven by c_addr bus. Default Value: 0

4.1.63 FLASHC_FM_CTL_FM_ECC_CTL_ADDR

Internal ECC signal - unused

Address: 0x42152FEC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							R
Name	None [7:1]							ECC_CT-L_ADDR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	ECC_CTL_ADDR	Internal Register - Spare for future use - Read Undefined, Write Ignore Default Value: 0

4.1.64 FLASHC_FM_CTL_FM_RED_CTL_SM01_ADDR

Internal register

Address: 0x42152FF0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	FM_RED_CTL_SM01_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	FM_RED_CTL_SM01_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	FM_RED_CTL_SM01_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	FM_RED_CTL_SM01_ADDR [31:24]							

Bits	Name	Description
31 : 0	FM_RED_CT-L_SM01_ADDR	Internal Register - Spare for future use - Read Undefined, Write Ignore Default Value: 0

4.1.65 FLASHC_FM_CTL_FM_RED_CTL67_ADDR

Internal register

Address: 0x42152FF4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	FM_RED_CTL67_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	FM_RED_CTL67_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	FM_RED_CTL67_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	FM_RED_CTL67_ADDR [31:24]							

Bits	Name	Description
31 : 0	FM_RED_CTL67_ADDR	Internal Register - Spare for future use - Read Undefined, Write Ignore Default Value: 0

4.1.66 FLASHC_FM_CTL_FM_RED_CTL45_ADDR

Internal register

Address: 0x42152FF8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	FM_RED_CTL45_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	FM_RED_CTL45_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	FM_RED_CTL45_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	FM_RED_CTL45_ADDR [31:24]							

Bits	Name	Description
31 : 0	FM_RED_CTL45_ADDR	Internal Register - Spare for future use - Read Undefined, Write Ignore Default Value: 0

4.1.67 FLASHC_FM_CTL_FM_CAL_CTL8_ADDR

Internal register

Address: 0x42152FFC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	FM_CAL_CTL8_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	FM_CAL_CTL8_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	FM_CAL_CTL8_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	FM_CAL_CTL8_ADDR [31:24]							

Bits	Name	Description
31 : 0	FM_CAL_CTL8_ADDR	Internal Register - Spare for future use - Read Undefined, Write Ignore Default Value: 0

5 Supervisory Flash (SFLASH) registers

This section discusses the SFLASH registers. It lists all the registers in mapping tables, in address order.

5.1 Register details

Register	Address	Description
SFLASH_SI_REVISION_ID	0x03400001	Indicates Silicon Revision ID of the device
SFLASH_SILICON_ID	0x03400002	Indicates Silicon ID of the device
SFLASH_FAMILY_ID	0x03400004	Indicates Family ID of the device
SFLASH_SFLASH_SVN	0x03400018	SFLASH Subversion
SFLASH_DIE_LOT0	0x03400600	Lot Number (3 bytes)
SFLASH_DIE_LOT1	0x03400601	Lot Number (3 bytes). See SFLASH_DIE_LOT0 for the details of bit fields.
SFLASH_DIE_LOT2	0x03400602	Lot Number (3 bytes). See SFLASH_DIE_LOT0 for the details of bit fields.
SFLASH_DIE_WAFER	0x03400603	Wafer Number
SFLASH_DIE_X	0x03400604	X Position on Wafer, CRI Pass/Fail Bin
SFLASH_DIE_Y	0x03400605	Y Position on Wafer, CHI Pass/Fail Bin
SFLASH_DIE_SORT	0x03400606	Sort1/2/3 Pass/Fail Bin
SFLASH_DIE_MINOR	0x03400607	Minor Revision Number
SFLASH_DIE_DAY	0x03400608	Day number
SFLASH_DIE_MONTH	0x03400609	Month number
SFLASH_DIE_YEAR	0x0340060A	Year number
SFLASH_CSP_PANEL_ID	0x0340060C	CSP Panel Id to record panel ID of CSP die
SFLASH_SAR_CALOFFST_0_25C	0x03400630	SAR Calibration Offset for sampler 0 at 25C measured after packaging. This value is copied to the CALOFFST register in the SAR during the init function. Each of these 4 registers contains the offset cal for 4 successive samplers, where N is the iteration of each of the 4 registers. for example CALOFFST_0 contains the offset cal for samplers 0-3, CAOFFST_1 contains the offset cal for samplers 4-7, etc
SFLASH_SAR_CALOFFST_1_25C	0x03400634	SAR Calibration Offset for sampler 0 at 25C measured after packaging. This value is copied to the CALOFFST register in the SAR during the init function. Each of these 4 registers contains the offset cal for 4 successive samplers, where N is the iteration of each of the 4 registers. for example CALOFFST_0 contains the offset cal for samplers 0-3, CAOFFST_1 contains the offset cal for samplers 4-7, etc. See SFLASH_SAR_CALOFFST_0_25C for the details of bit fields.

Supervisory Flash (SFLASH) registers

Register	Address	Description
SFLASH_SAR_CALOFFST_2_25C	0x03400638	SAR Calibration Offset for sampler 0 at 25C measured after packaging. This value is copied to the CALOFFST register in the SAR during the init function. Each of these 4 registers contains the offset cal for 4 successive samplers, where N is the iteration of each of the 4 registers. for example CALOFFST_0 contains the offset cal for samplers 0-3, CAOFFST_1 contains the offset cal for samplers 4-7, etc. See SFLASH_SAR_CALOFFST_0_25C for the details of bit fields.
SFLASH_SAR_CALOFFST_3_25C	0x0340063C	SAR Calibration Offset for sampler 0 at 25C measured after packaging. This value is copied to the CALOFFST register in the SAR during the init function. Each of these 4 registers contains the offset cal for 4 successive samplers, where N is the iteration of each of the 4 registers. for example CALOFFST_0 contains the offset cal for samplers 0-3, CAOFFST_1 contains the offset cal for samplers 4-7, etc. See SFLASH_SAR_CALOFFST_0_25C for the details of bit fields.
SFLASH_SAR_CALREFPT	0x03400640	SAR Calibration Reference Point (Voltage) AKA VAREF_PROD
SFLASH_SAR_TEMP_COEF_A	0x03400644	Factors used in temperature calculation formula Temperature = a * ratio^3 + b * ratio^2 + c * ratio^1 + d
SFLASH_SAR_TEMP_COEF_B	0x03400648	Factors used in temperature calculation formula Temperature = a * ratio^3 + b * ratio^2 + c * ratio^1 + d. See SFLASH_SAR_TEMP_COEF_A for the details of bit fields.
SFLASH_SAR_TEMP_COEF_C	0x0340064C	Factors used in temperature calculation formula Temperature = a * ratio^3 + b * ratio^2 + c * ratio^1 + d. See SFLASH_SAR_TEMP_COEF_A for the details of bit fields.
SFLASH_SAR_TEMP_COEF_D	0x03400650	Factors used in temperature calculation formula Temperature = a * ratio^3 + b * ratio^2 + c * ratio^1 + d. See SFLASH_SAR_TEMP_COEF_A for the details of bit fields.
SFLASH_SAR_CAL_LIN_TABLE0	0x03400654	Table of values that are loaded in the HPPASS_SARADC_CALLIN0 - 15 registers by the init function. Each value contains 4x 7 bit calibration values. See the Registers Technical Reference Manual for the details of these calibration registers.

Supervisory Flash (SFLASH) registers

Register	Address	Description
SFLASH_SAR_CAL_LIN_TABLE1	0x03400658	Table of values that are loaded in the HPPASS_SARADC_CALLIN0 - 15 registers by the init function. Each value contains 4x 7 bit calibration values. See the Registers Technical Reference Manual for the details of these calibration registers. See SFLASH_SAR_CAL_LIN_TABLE0 for the details of bit fields.
SFLASH_SAR_CAL_LIN_TABLE2	0x0340065C	Table of values that are loaded in the HPPASS_SARADC_CALLIN0 - 15 registers by the init function. Each value contains 4x 7 bit calibration values. See the Registers Technical Reference Manual for the details of these calibration registers. See SFLASH_SAR_CAL_LIN_TABLE0 for the details of bit fields.
SFLASH_SAR_CAL_LIN_TABLE3	0x03400660	Table of values that are loaded in the HPPASS_SARADC_CALLIN0 - 15 registers by the init function. Each value contains 4x 7 bit calibration values. See the Registers Technical Reference Manual for the details of these calibration registers. See SFLASH_SAR_CAL_LIN_TABLE0 for the details of bit fields.
SFLASH_SAR_CAL_LIN_TABLE4	0x03400664	Table of values that are loaded in the HPPASS_SARADC_CALLIN0 - 15 registers by the init function. Each value contains 4x 7 bit calibration values. See the Registers Technical Reference Manual for the details of these calibration registers. See SFLASH_SAR_CAL_LIN_TABLE0 for the details of bit fields.
SFLASH_SAR_CAL_LIN_TABLE5	0x03400668	Table of values that are loaded in the HPPASS_SARADC_CALLIN0 - 15 registers by the init function. Each value contains 4x 7 bit calibration values. See the Registers Technical Reference Manual for the details of these calibration registers. See SFLASH_SAR_CAL_LIN_TABLE0 for the details of bit fields.
SFLASH_SAR_CAL_LIN_TABLE6	0x0340066C	Table of values that are loaded in the HPPASS_SARADC_CALLIN0 - 15 registers by the init function. Each value contains 4x 7 bit calibration values. See the Registers Technical Reference Manual for the details of these calibration registers. See SFLASH_SAR_CAL_LIN_TABLE0 for the details of bit fields.

Supervisory Flash (SFLASH) registers

Register	Address	Description
SFLASH_SAR_CAL_LIN_TABLE7	0x03400670	Table of values that are loaded in the HPPASS_SARADC_CALLIN0 - 15 registers by the init function. Each value contains 4x 7 bit calibration values. See the Registers Technical Reference Manual for the details of these calibration registers. See SFLASH_SAR_CAL_LIN_TABLE0 for the details of bit fields.
SFLASH_SAR_CAL_LIN_TABLE8	0x03400674	Table of values that are loaded in the HPPASS_SARADC_CALLIN0 - 15 registers by the init function. Each value contains 4x 7 bit calibration values. See the Registers Technical Reference Manual for the details of these calibration registers. See SFLASH_SAR_CAL_LIN_TABLE0f or the details of bit fields.
SFLASH_SAR_CAL_LIN_TABLE9	0x03400678	Table of values that are loaded in the HPPASS_SARADC_CALLIN0 - 15 registers by the init function. Each value contains 4x 7 bit calibration values. See the Registers Technical Reference Manual for the details of these calibration registers. See SFLASH_SAR_CAL_LIN_TABLE0 for the details of bit fields.
SFLASH_SAR_CAL_LIN_TABLE10	0x0340067C	Table of values that are loaded in the HPPASS_SARADC_CALLIN0 - 15 registers by the init function. Each value contains 4x 7 bit calibration values. See the Registers Technical Reference Manual for the details of these calibration registers. See SFLASH_SAR_CAL_LIN_TABLE0 for the details of bit fields.
SFLASH_SAR_CAL_LIN_TABLE11	0x03400680	Table of values that are loaded in the HPPASS_SARADC_CALLIN0 - 15 registers by the init function. Each value contains 4x 7 bit calibration values. See the Registers Technical Reference Manual for the details of these calibration registers. See SFLASH_SAR_CAL_LIN_TABLE0 for the details of bit fields.
SFLASH_SAR_CAL_LIN_TABLE12	0x03400684	Table of values that are loaded in the HPPASS_SARADC_CALLIN0 - 15 registers by the init function. Each value contains 4x 7 bit calibration values. See the Registers Technical Reference Manual for the details of these calibration registers. See SFLASH_SAR_CAL_LIN_TABLE0 for the details of bit fields.

Supervisory Flash (SFLASH) registers

Register	Address	Description
SFLASH_SAR_CAL_LIN_TABLE13	0x03400688	Table of values that are loaded in the HPPASS_SARADC_CALLIN0 - 15 registers by the init function. Each value contains 4x 7 bit calibration values. See the Registers Technical Reference Manual for the details of these calibration registers. See SFLASH_SAR_CAL_LIN_TABLE0 for the details of bit fields.
SFLASH_SAR_CAL_LIN_TABLE14	0x0340068C	Table of values that are loaded in the HPPASS_SARADC_CALLIN0 - 15 registers by the init function. Each value contains 4x 7 bit calibration values. See the Registers Technical Reference Manual for the details of these calibration registers. See SFLASH_SAR_CAL_LIN_TABLE0 for the details of bit fields.
SFLASH_SAR_CAL_LIN_TABLE15	0x03400690	Table of values that are loaded in the HPPASS_SARADC_CALLIN0 - 15 registers by the init function. Each value contains 4x 7 bit calibration values. See the Registers Technical Reference Manual for the details of these calibration registers. See SFLASH_SAR_CAL_LIN_TABLE0 for the details of bit fields.
SFLASH_SAR_CALGAINC	0x03400694	SARADC Coarse-grained Gain Calibration Values - Load to CALGAINC register
SFLASH_SAR_CALGAINF	0x03400698	SARADC Fine-grained Gain Calibration Values - Load to CALGAINF register
SFLASH_SAR_INFRA_TRIM_TABLE0	0x0340069C	Table of trim values loaded to SAR by the hppass init function. The table format is as follows: [32-bits] n_trim_pairs [32-bits list] (mmio_addr, mmio_value) x (n_trim_pairs)
SFLASH_SAR_INFRA_TRIM_TABLE1	0x034006A0	Table of trim values loaded to SAR by the hppass init function. The table format is as follows: [32-bits] n_trim_pairs [32-bits list] (mmio_addr, mmio_value) x (n_trim_pairs). See SFLASH_SAR_INFRA_TRIM_TABLE0 for the details of bit fields.
SFLASH_SAR_INFRA_TRIM_TABLE2	0x034006A4	Table of trim values loaded to SAR by the hppass init function. The table format is as follows: [32-bits] n_trim_pairs [32-bits list] (mmio_addr, mmio_value) x (n_trim_pairs). See SFLASH_SAR_INFRA_TRIM_TABLE0 for the details of bit fields.

Supervisory Flash (SFLASH) registers

Register	Address	Description
SFLASH_SAR_INFRA_TRIM_TABLE3	0x034006A8	Table of trim values loaded to SAR by the hppass init function. The table format is as follows: [32-bits] n_trim_pairs [32-bits list] (mmio_addr, mmio_value) x (n_trim_pairs). See SFLASH_SAR_INFRA_TRIM_TABLE0 for the details of bit fields.
SFLASH_SAR_INFRA_TRIM_TABLE4	0x034006AC	Table of trim values loaded to SAR by the hppass init function. The table format is as follows: [32-bits] n_trim_pairs [32-bits list] (mmio_addr, mmio_value) x (n_trim_pairs). See SFLASH_SAR_INFRA_TRIM_TABLE0 for the details of bit fields.
SFLASH_SAR_INFRA_TRIM_TABLE5	0x034006B0	Table of trim values loaded to SAR by the hppass init function. The table format is as follows: [32-bits] n_trim_pairs [32-bits list] (mmio_addr, mmio_value) x (n_trim_pairs). See SFLASH_SAR_INFRA_TRIM_TABLE0 for the details of bit fields.
SFLASH_SAR_INFRA_TRIM_TABLE6	0x034006B4	Table of trim values loaded to SAR by the hppass init function. The table format is as follows: [32-bits] n_trim_pairs [32-bits list] (mmio_addr, mmio_value) x (n_trim_pairs). See SFLASH_SAR_INFRA_TRIM_TABLE0 for the details of bit fields.
SFLASH_SAR_INFRA_TRIM_TABLE7	0x034006B8	Table of trim values loaded to SAR by the hppass init function. The table format is as follows: [32-bits] n_trim_pairs [32-bits list] (mmio_addr, mmio_value) x (n_trim_pairs). See SFLASH_SAR_INFRA_TRIM_TABLE0 for the details of bit fields.
SFLASH_SAR_INFRA_TRIM_TABLE8	0x034006BC	Table of trim values loaded to SAR by the hppass init function. The table format is as follows: [32-bits] n_trim_pairs [32-bits list] (mmio_addr, mmio_value) x (n_trim_pairs). See SFLASH_SAR_INFRA_TRIM_TABLE0 for the details of bit fields.

Supervisory Flash (SFLASH) registers

Register	Address	Description
SFLASH_SAR_INFRA_TRIM_TABLE9	0x034006C0	Table of trim values loaded to SAR by the hppass init function. The table format is as follows: [32-bits] n_trim_pairs [32-bits list] (mmio_addr, mmio_value) x (n_trim_pairs). See SFLASH_SAR_INFRA_TRIM_TABLE0 for the details of bit fields.
SFLASH_SAR_INFRA_TRIM_TABLE10	0x034006C4	Table of trim values loaded to SAR by the hppass init function. The table format is as follows: [32-bits] n_trim_pairs [32-bits list] (mmio_addr, mmio_value) x (n_trim_pairs). See SFLASH_SAR_INFRA_TRIM_TABLE0 for the details of bit fields.
SFLASH_SAR_INFRA_TRIM_TABLE11	0x034006C8	Table of trim values loaded to SAR by the hppass init function. The table format is as follows: [32-bits] n_trim_pairs [32-bits list] (mmio_addr, mmio_value) x (n_trim_pairs). See SFLASH_SAR_INFRA_TRIM_TABLE0 for the details of bit fields.
SFLASH_SAR_INFRA_TRIM_TABLE12	0x034006CC	Table of trim values loaded to SAR by the hppass init function. The table format is as follows: [32-bits] n_trim_pairs [32-bits list] (mmio_addr, mmio_value) x (n_trim_pairs). See SFLASH_SAR_INFRA_TRIM_TABLE0 for the details of bit fields.
SFLASH_SAR_INFRA_TRIM_TABLE13	0x034006D0	Table of trim values loaded to SAR by the hppass init function. The table format is as follows: [32-bits] n_trim_pairs [32-bits list] (mmio_addr, mmio_value) x (n_trim_pairs). See SFLASH_SAR_INFRA_TRIM_TABLE0 for the details of bit fields.
SFLASH_SAR_INFRA_TRIM_TABLE14	0x034006D4	Table of trim values loaded to SAR by the hppass init function. The table format is as follows: [32-bits] n_trim_pairs [32-bits list] (mmio_addr, mmio_value) x (n_trim_pairs). See SFLASH_SAR_INFRA_TRIM_TABLE0 for the details of bit fields.

Supervisory Flash (SFLASH) registers

Register	Address	Description
SFLASH_SAR_INFRA_TRIM_TABLE15	0x034006D8	Table of trim values loaded to SAR by the hppass init function. The table format is as follows: [32-bits] n_trim_pairs [32-bits list] (mmio_addr, mmio_value) x (n_trim_pairs). See SFLASH_SAR_INFRA_TRIM_TABLE0 for the details of bit fields.
SFLASH_LDO_0P9V_TRIM	0x034006DC	LDO trim value for 0.9V. Loaded to the SRSS_PWR_TRIM_PWRSYS_CTL register when changing LDO regulator settings.
SFLASH_LDO_1P0V_TRIM	0x034006E0	LDO trim value for 1.0V. Loaded to the SRSS_PWR_TRIM_PWRSYS_CTL register when changing LDO regulator settings.
SFLASH_LDO_1P1V_TRIM	0x034006E4	LDO trim value for 1.1V. Loaded to the SRSS_PWR_TRIM_PWRSYS_CTL register when changing LDO regulator settings.
SFLASH_LDO_1P2V_TRIM	0x034006E8	LDO trim value for 1.2V. Loaded to the SRSS_PWR_TRIM_PWRSYS_CTL register when changing LDO regulator settings.
SFLASH_PWR_TRIM_WAKE_CTL	0x034006FC	Wakeup delay values for ULP, LP, MF and OD modes (4 values) loaded to the PWR_TRIM_WAKE_CTL register
SFLASH_CPUSS_TRIM_ROM_CTL_ULP	0x03400700	CPUSS TRIM ROM CTL ULP value
SFLASH_CPUSS_TRIM_ROM_CTL_LP	0x03400704	CPUSS TRIM ROM CTL LP value
SFLASH_CPUSS_TRIM_ROM_CTL_MF	0x03400708	CPUSS TRIM ROM CTL MF value
SFLASH_CPUSS_TRIM_ROM_CTL_OD	0x0340070C	CPUSS TRIM ROM CTL OD value
SFLASH_CPUSS_TRIM_RAM_CTL_ULP	0x03400710	CPUSS TRIM RAM CTL ULP value
SFLASH_CPUSS_TRIM_RAM_CTL_LP	0x03400714	CPUSS TRIM RAM CTL LP value
SFLASH_CPUSS_TRIM_RAM_CTL_MF	0x03400718	CPUSS TRIM RAM CTL MF value
SFLASH_CPUSS_TRIM_RAM_CTL_OD	0x0340071C	CPUSS TRIM RAM CTL OD value
SFLASH_CPUSS_TRIM_ROM_CTL_HALF_ULP	0x03400720	CPUSS TRIM ROM CTL HALF ULP value
SFLASH_CPUSS_TRIM_ROM_CTL_HALF_LP	0x03400724	CPUSS TRIM ROM CTL HALF LP value
SFLASH_CPUSS_TRIM_ROM_CTL_HALF_MF	0x03400728	CPUSS TRIM ROM CTL HALF MF value
SFLASH_CPUSS_TRIM_ROM_CTL_HALF_OD	0x0340072C	CPUSS TRIM ROM CTL HALF OD value
SFLASH_CPUSS_TRIM_RAM_CTL_HALF_ULP	0x03400730	CPUSS TRIM RAM CTL HALF ULP value
SFLASH_CPUSS_TRIM_RAM_CTL_HALF_LP	0x03400734	CPUSS TRIM RAM CTL HALF LP value

Supervisory Flash (SFLASH) registers

Register	Address	Description
SFLASH_CPUSS_TRIM_RAM_CTL_HALF_MF	0x03400738	CPUSS TRIM RAM CTL HALF MF value
SFLASH_CPUSS_TRIM_RAM_CTL_HALF_OD	0x0340073C	CPUSS TRIM RAM CTL HALF OD value

5.1.1 SFLASH_SI_REVISION_ID

Indicates Silicon Revision ID of the device

Address: 0x03400001

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	SI_REVISION_ID [7:0]							

Bits	Name	Description
7 : 0	SI_REVISION_ID	Silicon Revision ID Default Value: 0x11

5.1.2 SFLASH_SILICON_ID

Indicates Silicon ID of the device

Address: 0x03400002

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	ID [15:8]							

Bits	Name	Description
15 : 0	ID	Silicon ID Default Value: 0xEE40

5.1.3 SFLASH_FAMILY_ID

Indicates Family ID of the device

Address: 0x03400004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	FAMILY_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	FAMILY_ID [15:8]							

Bits	Name	Description
15 : 0	FAMILY_ID	Indicates Family ID of the device Default Value: 0x0118

5.1.4 SFLASH_SFLASH_SVN

SFLASH Subversion

Address: 0x03400018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	SFLASH Subversion Default Value: 0

5.1.5 SFLASH_DIE_LOT0

Lot Number (3 bytes)

Address: 0x03400600

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	LOT [7:0]							

Bits	Name	Description
7 : 0	LOT	Lot Number Byte Default Value: X

5.1.6 SFLASH_DIE_WAFER

Wafer Number

Address: 0x03400603

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	WAFER [7:0]							

Bits	Name	Description
7 : 0	WAFER	Wafer Number Default Value: X

5.1.7 SFLASH_DIE_X

X Position on Wafer, CRI Pass/Fail Bin

Address: 0x03400604

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	X [7:0]							

Bits	Name	Description
7 : 0	X	X Position Default Value: X

5.1.8 SFLASH_DIE_Y

Y Position on Wafer, CHI Pass/Fail Bin

Address: 0x03400605

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	Y [7:0]							

Bits	Name	Description
7 : 0	Y	Y Position Default Value: X

5.1.9 SFLASH_DIE_SORT

Sort1/2/3 Pass/Fail Bin

Address: 0x03400606

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None							
Name	None [7:6]		ENG_PASS	CHI_PASS	CRI_PASS	S3_PASS	S2_PASS	S1_PASS

Bits	Name	Description
5	ENG_PASS	ENG Pass Bin Default Value: X
4	CHI_PASS	CHI Pass Bin (1) or 0 (Fail Bin) Default Value: X
3	CRI_PASS	CRI Pass Bin (1) or 0 (Fail Bin) Default Value: X
2	S3_PASS	SORT3 Pass Bin (1) or 0 (Fail Bin) Default Value: X
1	S2_PASS	SORT2 Pass Bin (1) or 0 (Fail Bin) Default Value: X
0	S1_PASS	SORT1 Pass Bin (1) or 0 (Fail Bin) Default Value: X

5.1.10 SFLASH_DIE_MINOR

Minor Revision Number

Address: 0x03400607

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	MINOR [7:0]							

Bits	Name	Description
7 : 0	MINOR	Minor revision number Default Value: X

5.1.11 SFLASH_DIE_DAY

Day number

Address: 0x03400608

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	MINOR [7:0]							

Bits	Name	Description
7 : 0	MINOR	Day number Default Value: X

5.1.12 SFLASH_DIE_MONTH

Month number

Address: 0x03400609

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	MINOR [7:0]							

Bits	Name	Description
7 : 0	MINOR	Month number Default Value: X

5.1.13 SFLASH_DIE_YEAR

Year number

Address: 0x0340060A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	MINOR [7:0]							

Bits	Name	Description
7 : 0	MINOR	Year number Default Value: X

5.1.14 SFLASH_CSP_PANEL_ID

CSP Panel Id to record panel ID of CSP die

Address: 0x0340060C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

5.1.15 SFLASH_SAR_CALOFFST_0_25C

SAR Calibration Offset for sampler 0 at 25C measured after packaging. This value is copied to the CALOFFST register in the SAR during the init function. Each of these 4 registers contains the offset cal for 4 succesive samplers, where N is the iteration of each of the 4 registers. For example CALOFFST_0 contains the offset cal for samplers 0-3, CAOFFST_1 contains the offset cal for samplers 4-7, etc

Address: 0x03400630

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None							
Name	None	OFFSET_4N_0 [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW						
HW Access	None							
Name	None	OFFSET_4N_1 [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None							
Name	None	OFFSET_4N_2 [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW						
HW Access	None							
Name	None	OFFSET_4N_3 [30:24]						

Bits	Name	Description
30 : 24	OFFSET_4N_3	Default Value: X
22 : 16	OFFSET_4N_2	Default Value: X
14 : 8	OFFSET_4N_1	Default Value: X
6 : 0	OFFSET_4N_0	Default Value: X

5.1.16 SFLASH_SAR_CALREFPT

SAR Calibration Reference Point (Voltage) AKA VAREF_PROD

Address: 0x03400640

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

5.1.17 SFLASH_SAR_TEMP_COEF_A

Factors used in temperature calculation formula Temperature = a * ratio^3 + b * ratio^2 + c * ratio^1 + d

Address: 0x03400644

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

5.1.18 SFLASH_SAR_CAL_LIN_TABLE0

Table of values that are loaded in the HPPASS_SARADC_CALLIN0 - 15 registers by the init function. Each value contains 4x 7 bit calibration values. See the Registers Technical Reference Manual for the details of these calibration registers.

Address: 0x03400654

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

5.1.19 SFLASH_SAR_CALGAINC

SARADC Coarse-grained Gain Calibration Values - Load to CALGAINC register

Address: 0x03400694

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

5.1.20 SFLASH_SAR_CALGAINF

SARADC Fine-grained Gain Calibration Values - Load to CALGAINF register

Address: 0x03400698

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

5.1.21 SFLASH_SAR_INFRA_TRIM_TABLE0

Table of trim values loaded to SAR by the hppass init function. The table format is as follows: [32-bits] n_trim_pairs [32-bits list] (mmio_addr, mmio_value) x (n_trim_pairs)

Address: 0x0340069C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

5.1.22 SFLASH_LDO_0P9V_TRIM

LDO trim value for 0.9V. Loaded to the SRSS_PWR_TRIM_PWRSYS_CTL register when changing LDO regulator settings.

Address: 0x034006DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

5.1.23 SFLASH_LDO_1P0V_TRIM

LDO trim value for 1.0V. Loaded to the SRSS_PWR_TRIM_PWRSYS_CTL register when changing LDO regulator settings.

Address: 0x034006E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

5.1.24 SFLASH_LDO_1P1V_TRIM

LDO trim value for 1.1V. Loaded to the SRSS_PWR_TRIM_PWRSYS_CTL register when changing LDO regulator settings.

Address: 0x034006E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

5.1.25 SFLASH_LDO_1P2V_TRIM

LDO trim value for 1.2V. Loaded to the SRSS_PWR_TRIM_PWRSYS_CTL register when changing LDO regulator settings.

Address: 0x034006E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

5.1.26 SFLASH_PWR_TRIM_WAKE_CTL

Wakeup delay values for ULP, LP, MF and OD modes (4 values) loaded to the PWR_TRIM_WAKE_CTL register

Address: 0x034006FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	WAKE_DELAY_0P9V [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	WAKE_DELAY_1P0V [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	WAKE_DELAY_1P1V [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	WAKE_DELAY_1P2V [31:24]							

Bits	Name	Description
31 : 24	WAKE_DELAY_1P2V	When changing power modes, thie appropriate byte within this structure needs to be copied into SRSS.PWR_TRIM_WAKE_CTL.WAKE_DELAY.CDT 290172 Default Value: X
23 : 16	WAKE_DELAY_1P1V	When changing power modes, thie appropriate byte within this structure needs to be copied into SRSS.PWR_TRIM_WAKE_CTL.WAKE_DELAY.CDT 290172 Default Value: X
15 : 8	WAKE_DELAY_1P0V	When changing power modes, thie appropriate byte within this structure needs to be copied into SRSS.PWR_TRIM_WAKE_CTL.WAKE_DELAY.CDT 290172 Default Value: X
7 : 0	WAKE_DELAY_0P9V	When changing power modes, thie appropriate byte within this structure needs to be copied into SRSS.PWR_TRIM_WAKE_CTL.WAKE_DELAY.CDT 290172 Default Value: X

5.1.27 SFLASH_CPUSS_TRIM_ROM_CTL_ULP

CPUSS TRIM ROM CTL ULP value

Address: 0x03400700

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

5.1.28 SFLASH_CPUSS_TRIM_ROM_CTL_LP

CPUSS TRIM ROM CTL LP value

Address: 0x03400704

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

5.1.29 SFLASH_CPUSS_TRIM_ROM_CTL_MF

CPUSS TRIM ROM CTL MF value

Address: 0x03400708

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

5.1.30 SFLASH_CPUSS_TRIM_ROM_CTL_OD

CPUSS TRIM ROM CTL OD value

Address: 0x0340070C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

5.1.31 SFLASH_CPUSS_TRIM_RAM_CTL_ULP

CPUSS TRIM RAM CTL ULP value

Address: 0x03400710

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

5.1.32 SFLASH_CPUSS_TRIM_RAM_CTL_LP

CPUSS TRIM RAM CTL LP value

Address: 0x03400714

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

5.1.33 SFLASH_CPUSS_TRIM_RAM_CTL_MF

CPUSS TRIM RAM CTL MF value

Address: 0x03400718

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

5.1.34 SFLASH_CPUSS_TRIM_RAM_CTL_OD

CPUSS TRIM RAM CTL OD value

Address: 0x0340071C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

5.1.35 SFLASH_CPUSS_TRIM_ROM_CTL_HALF_ULP

CPUSS TRIM ROM CTL HALF ULP value

Address: 0x03400720

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

5.1.36 SFLASH_CPUSS_TRIM_ROM_CTL_HALF_LP

CPUSS TRIM ROM CTL HALF LP value

Address: 0x03400724

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

5.1.37 SFLASH_CPUSS_TRIM_ROM_CTL_HALF_MF

CPUSS TRIM ROM CTL HALF MF value

Address: 0x03400728

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

5.1.38 SFLASH_CPUSS_TRIM_ROM_CTL_HALF_OD

CPUSS TRIM ROM CTL HALF OD value

Address: 0x0340072C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

5.1.39 SFLASH_CPUSS_TRIM_RAM_CTL_HALF_ULP

CPUSS TRIM RAM CTL HALF ULP value

Address: 0x03400730

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

5.1.40 SFLASH_CPUSS_TRIM_RAM_CTL_HALF_LP

CPUSS TRIM RAM CTL HALF LP value

Address: 0x03400734

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

5.1.41 SFLASH_CPUSS_TRIM_RAM_CTL_HALF_MF

CPUSS TRIM RAM CTL HALF MF value

Address: 0x03400738

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

5.1.42 SFLASH_CPUSS_TRIM_RAM_CTL_HALF_OD

CPUSS TRIM RAM CTL HALF OD value

Address: 0x0340073C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: X

6 SRAM Controller Registers

This section discusses the SRAM Controller registers. It lists all the registers in mapping tables, in address order.

6.1 Register details

Register	Address	Description
RAMC0_CTL	0x42110000	Control
RAMC0_STATUS	0x42110008	Status
RAMC0_ECC_CTL	0x42110020	ECC control
RAMC0_ECC_STATUS0	0x42110024	ECC status 0
RAMC0_ECC_STATUS1	0x42110028	ECC status 1
RAMC0_ECC_MATCH	0x42110104	ECC match
RAMC0_PWR_MACRO_CTL	0x42110200	SRAM power partition power control
RAMC0_PWR_MACRO_CTL_LOCK	0x42110240	SRAM power partition power control Lock
RAMC0_PWR_DELAY_CTL	0x42110280	SRAM power switch power up & sequence delay
RAMC0_MPC0_CFG	0x42114000	Config register with error response, RegionID PPC_MPC_MAIN is the security owner PC. The error response configuration is located in CFG.RESPONSE, only one such configuration exists applying to all protection contexts in the system.
RAMC0_MPC0_CTRL	0x42114100	Control register with lock bit and auto-increment only (Separate CTRL for each PC depends on access_pc)
RAMC0_MPC0_BLK_MAX	0x42114104	Max value of block-based index register
RAMC0_MPC0_BLK_CFG	0x42114108	Block size & initialization in progress
RAMC0_MPC0_BLK_IDX	0x4211410C	Index of 32-block group accessed through BLK_LUT (Separate IDX for each PC depending on access_pc)
RAMC0_MPC0_BLK_LUT	0x42114110	NS status for 32 blocks at BLK_IDX with PC=<access_pc>
RAMC0_MPC0_ROT_CTRL	0x42114200	Control register with lock bit and auto-increment only
RAMC0_MPC0_ROT_BLK_MAX	0x42114208	Max value of block-based index register for ROT
RAMC0_MPC0_ROT_BLK_CFG	0x4211420C	Same as BLK_CFG
RAMC0_MPC0_ROT_BLK_IDX	0x42114210	Index of 8-block group accessed through ROT_BLK_LUT_*
RAMC0_MPC0_ROT_BLK_PC	0x42114214	Protection context of 8-block group accesses through ROT_BLK_LUT
RAMC0_MPC0_ROT_BLK_LUT	0x42114218	(R,W,NS) bits for 8 blocks at ROT_BLK_IDX for PC=ROT_BKL_PC

6.1.1 RAMC0_CTL

Control

Address: 0x42110000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						SRAM_WS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							CLOCK_-FORCE

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	CLOCK_FORCE	Force EAM clock gating to be always ON. 0: Disabled 1: Enabled This bit provides fail safe mechanism for dynamic clock gating added on EAM block. Default Value: 0
1 : 0	SRAM_WS	Wait states. Default Value: 0 **0x0: WS_0** **0x1: WS_1** **0x2: WS_2** **0x3: WS_3**

6.1.2 RAMC0_STATUS

Status

Address: 0x42110008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	None			R
HW Access	None			W	None			W
Name	None [7:5]			PWR_-DONE	None [3:1]			WB_EMP-TY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	PWR_DONE	After a PWR_MACRO_CTL.OFF change this flag indicates if the new power mode has taken effect or not. 1: Indicates change is effective; 0: Indicates change is in progress; Default Value: 1
0	WB_EMPTY	Write buffer empty. This information is used when entering DeepSleep power mode: WB_EMP-TY must be '1' before a transition to system DeepSleep power mode. '0': Write buffer NOT empty. '1': Write buffer empty. Note: the SRAM controller write buffer is only used when ECC checking is enabled. (RAMi_CTL.ECC_EN is '1'). Default Value: 1

6.1.3 RAMC0_ECC_CTL

ECC control

Address: 0x42110020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				CHECK_EN	INJ_EN	AU-TO_COR-RECT	EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	PARITY [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
22 : 16	PARITY	Injected parity. Default Value: 0
3	CHECK_EN	ECC checking enable: '0': Disabled. No ECC checking and associated bus errors. No fault reporting. Intended for SRAM initialization. '1': Enabled. Note: This field is ignored when EN is '0'. Default Value: 0
2	INJ_EN	ECC parity injection: '0': Disabled. '1': Enabled. Instead of calculating the parity from the transfer's write data, the parity is taken from PARITY upon a match of the transfer's write address with ECC_MATCH.WORD_ADDR (no match is performed on the transfer's write strobes/mask). Note: Parity injection invalidates the write buffer for this word address. If only a part of 64-bit data word is written AND consistency should be maintained, STATUS.ALL_WB_EMPTY is '1' should be checked before. Note: This field is ignored when EN is '0'. Default Value: 0

6.1.3 RAMC0_ECC_CTL (continued)

1	AUTO_CORRECT	ECC auto correction: '0': Disabled. Corrected ECC errors are ONLY HW corrected "on-the-fly" (not corrected in the SRAM). Fault reporting is enabled. '1': Enabled. Correctable ECC errors are HW corrected "on-the-fly" and in the SRAM, without CPU intervention. Fault reporting is enabled. Note: This field is ignored when EN is '0' or when CHECK_EN is '0'. Default Value: 1
0	EN	ECC enable: '0': Disabled. '1': Enabled. Default Value: 1 **0x0: ECC_DISABLED** **0x1: ECC_ENABLED**

6.1.4 RAMC0_ECC_STATUS0

ECC status 0

Address: 0x42110024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	ECC error address. This register captures the address location when ECC error happens. Default Value: Undefined

6.1.5 RAMC0_ECC_STATUS1

ECC status 1

Address: 0x42110028

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R						
HW Access	None	W						
Name	None	SYNDROME [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 0	SYNDROME	This register captures the ECC syndrome when ECC error happens. Default Value: Undefined

6.1.6 RAMC0_ECC_MATCH

ECC match

Address: 0x42110104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WORD_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	WORD_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	WORD_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							WORD_ADDR

Bits	Name	Description
24 : 0	WORD_ADDR	Specifies the word address where an error will be injected. - On a write transfer to this SRAM address and when the ECC_CTL.INJ_EN bit is '1', the parity (ECC_CTL.PARITY) is injected. Default Value: 0

6.1.7 RAMC0_PWR_MACRO_CTL

SRAM power partition power control

Address: 0x42110200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							OFF

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	OFF	Each bit represent the individual RAM power partition power state. One bit for each macro of RAM controller when all 32 bits are populated as 32 independent power partitions. 0: Macros in power partion is to be powered-ON 1: Macros in power partion is to be powered-OFF Note 1: it is not allowed to disable a macro during access to its address range. Note 2: it is not allowed to disable few macros while enable others in the same AHB write transaction. It is mandatory to check for STATUS.PWR_DONE to become 1 once this PWR_MACRO_DTL register contents are changed to ensure SRAM mode transition is completed successfully. Default Value: 0

6.1.8 RAMC0_PWR_MACRO_CTL_LOCK

SRAM power partition power control Lock

Address: 0x42110240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						A	
Name	None [7:2]						PWR_MACRO_CT-L_LOCK [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	PWR_MACRO_CT-L_LOCK	Prohibits Read/Write access to PWR_MACRO_CTL register when this field is not equal to 0. Requires at least two different writes to unlock. Note that this field is 2 bits to force multiple writes only. By default AHB reads/writes to PWR_MACRO_CTL register are locked. Default Value: 3 **0x0: NO_CHG :** No effect **0x1: CLR0 :** Clears bit 0 **0x2: CLR1 :** Clears bit 1 **0x3: SET01 :** Sets both bits 0 and 1

6.1.9 RAMC0_PWR_DELAY_CTL

SRAM power switch power up & sequence delay

Address: 0x42110280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	UP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						UP [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SEQ0_DELAY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	SEQ1_DELAY [31:24]							

Bits	Name	Description
31 : 24	SEQ1_DELAY	Number of IMO clock cycles delay needed for sequence-1 of SRAM power transition Default Value: 0x9
23 : 16	SEQ0_DELAY	Number of IMO clock cycles delay needed for sequence-0 of SRAM power transition Default Value: 0x2
9 : 0	UP	Number of IMO clock cycles delay needed after power domain power up Default Value: 0x9

6.1.10 RAMC0_MPC0_CFG

Config register with error response, RegionID PPC_MPC_MAIN is the security owner PC. The error response configuration is located in CFG.RESPONSE, only one such configuration exists applying to all protection contexts in the system.

Address: 0x42114000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None			
HW Access	None			R	None			
Name	None [7:5]			RE-SPONSE	None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	RESPONSE	Response Configuration for Security and PC violations 0: Read-Zero Write Ignore (RAZ/WI) 1: Bus Error Default Value: 0

6.1.11 RAMC0_MPC0_CTRL

Control register with lock bit and auto-increment only (Separate CTRL for each PC depends on access_pc)

Address: 0x42114100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							AUTO_INC

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	None						
HW Access	R	None						
Name	LOCK	None [30:24]						

Bits	Name	Description
31	LOCK	Security lockdown for this protection context. Software can set this bit but not clear it once set. When set, write operations to BLK_LUT are not possible from this protection context. Setting LOCK also blocks writes to CTRL itself (for that PC copy). All writes are ignored. Default Value: 0
8	AUTO_INC	Auto-increment BLK_IDX by 1 for this protection context as a side effect of each read/write access to BLK_LUT Default Value: 1

6.1.12 RAMC0_MPC0_BLK_MAX

Max value of block-based index register

Address: 0x42114104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							R
Name	None [7:1]							VALUE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	VALUE	Maximum value of block-based index register. The number and size blocks in an MPC is design time configurable and for embedded memories defaults to covering the entire memory using 4kB blocks; See product datasheet for details on protection of external memories. Default Value: 0

6.1.13 RAMC0_MPC0_BLK_CFG

Block size & initialization in progress

Address: 0x42114108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				R			
Name	None [7:4]				BLOCK_SIZE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	INIT_IN_PROGRESS	None [30:24]						

Bits	Name	Description
31	INIT_IN_PROGRESS	During initialization INIT_IN_PROGRESS is '1' and MMIO register accesses to BLK_LUT is blocked (BLK_IDX increment is also ignored). The block attributes are retained in DeepSleep (and obviously Active) power mode. Initialization is only required from a power mode in which the block attributes are not retained. E.g., initialization is required for a cold boot (after a Power-on-Reset). HW initializes the block attributes: the NS attributes are set to '0' (secure), the R attributes are set to '1' (read access allowed) and the W attributes are set to '1' (write access allowed). During initialization, the MPC supports memory accesses (memory accesses are NOT blocked) with the initialization block attribute values as mentioned above. This e.g. allows MPC initialization to proceed in parallel with boot program memory accesses (as opposed to serializing the two), improving device boot time. Default Value: 1
3 : 0	BLOCK_SIZE	Block size of individually protected blocks (0: 32B, 1: 64B, ... up to 15: 1MB) Block size= (1<<(BLOCK_SIZE+5)) The number and size blocks in an MPC is design time configurable and for embedded memories defaults to covering the entire memory using 4kB blocks; see product datasheet for details on protection of external memories. Default Value: 6

6.1.14 RAMC0_MPC0_BLK_IDX

Index of 32-block group accessed through BLK_LUT (Separate IDX for each PC depending on access_pc)

Address: 0x4211410C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							RW
Name	None [7:1]							VALUE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	VALUE	Index value for accessing block-based lookup table using BLK_LUT. Programming out of LUT range is an user error and it loops back to "0" once overflow occurs. Default Value: 0

6.1.15 RAMC0_MPC0_BLK_LUT

NS status for 32 blocks at BLK_IDX with PC=_pc>

Address: 0x42114110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	ATTR_NS7	ATTR_NS6	ATTR_NS5	ATTR_NS4	ATTR_NS3	ATTR_NS2	ATTR_NS1	ATTR_NS0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	AT-TR_NS15	AT-TR_NS14	AT-TR_NS13	AT-TR_NS12	ATTR_NS11	AT-TR_NS10	ATTR_NS9	ATTR_NS8

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	AT-TR_NS23	AT-TR_NS22	AT-TR_NS21	AT-TR_NS20	AT-TR_NS19	AT-TR_NS18	AT-TR_NS17	AT-TR_NS16

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	AT-TR_NS31	AT-TR_NS30	AT-TR_NS29	AT-TR_NS28	AT-TR_NS27	AT-TR_NS26	AT-TR_NS25	AT-TR_NS24

Bits	Name	Description
31	ATTR_NS31	NS bit for block 31 based on BLK_IDX Default Value: 0
30	ATTR_NS30	NS bit for block 30 based on BLK_IDX Default Value: 0
29	ATTR_NS29	NS bit for block 29 based on BLK_IDX Default Value: 0
28	ATTR_NS28	NS bit for block 28 based on BLK_IDX Default Value: 0
27	ATTR_NS27	NS bit for block 27 based on BLK_IDX Default Value: 0
26	ATTR_NS26	NS bit for block 26 based on BLK_IDX Default Value: 0
25	ATTR_NS25	NS bit for block 25 based on BLK_IDX Default Value: 0
24	ATTR_NS24	NS bit for block 24 based on BLK_IDX Default Value: 0
23	ATTR_NS23	NS bit for block 23 based on BLK_IDX Default Value: 0
22	ATTR_NS22	NS bit for block 22 based on BLK_IDX Default Value: 0

6.1.15 RAMC0_MPC0_BLK_LUT (continued)

21	ATTR_NS21	NS bit for block 21 based on BLK_IDX Default Value: 0
20	ATTR_NS20	NS bit for block 20 based on BLK_IDX Default Value: 0
19	ATTR_NS19	NS bit for block 19 based on BLK_IDX Default Value: 0
18	ATTR_NS18	NS bit for block 18 based on BLK_IDX Default Value: 0
17	ATTR_NS17	NS bit for block 17 based on BLK_IDX Default Value: 0
16	ATTR_NS16	NS bit for block 16 based on BLK_IDX Default Value: 0
15	ATTR_NS15	NS bit for block 15 based on BLK_IDX Default Value: 0
14	ATTR_NS14	NS bit for block 14 based on BLK_IDX Default Value: 0
13	ATTR_NS13	NS bit for block 13 based on BLK_IDX Default Value: 0
12	ATTR_NS12	NS bit for block 12 based on BLK_IDX Default Value: 0
11	ATTR_NS11	NS bit for block 11 based on BLK_IDX Default Value: 0
10	ATTR_NS10	NS bit for block 10 based on BLK_IDX Default Value: 0
9	ATTR_NS9	NS bit for block 9 based on BLK_IDX Default Value: 0
8	ATTR_NS8	NS bit for block 8 based on BLK_IDX Default Value: 0
7	ATTR_NS7	NS bit for block 7 based on BLK_IDX Default Value: 0
6	ATTR_NS6	NS bit for block 6 based on BLK_IDX Default Value: 0
5	ATTR_NS5	NS bit for block 5 based on BLK_IDX Default Value: 0
4	ATTR_NS4	NS bit for block 4 based on BLK_IDX Default Value: 0
3	ATTR_NS3	NS bit for block 3 based on BLK_IDX Default Value: 0
2	ATTR_NS2	NS bit for block 2 based on BLK_IDX Default Value: 0
1	ATTR_NS1	NS bit for block 1 based on BLK_IDX Default Value: 0
0	ATTR_NS0	NS bit for block 0 based on BLK_IDX Default Value: 0

6.1.16 RAMC0_MPC0_ROT_CTRL

Control register with lock bit and auto-increment only

Address: 0x42114200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							AUTO_INC

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	None						
HW Access	R	None						
Name	LOCK	None [30:24]						

Bits	Name	Description
31	LOCK	Security lockdown for the root-of-trust configuration registers. Software can set this bit but not clear it once set. When set, write operations to ROT_BLK_LUT are not possible. Write is ignored. Default Value: 0
8	AUTO_INC	Auto-increment BLK_IDX by 1 for each read/write of ROT_BLK_LUT Default Value: 1

6.1.17 RAMC0_MPC0_ROT_BLK_MAX

Max value of block-based index register for ROT

Address: 0x42114208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R		
HW Access	None					R		
Name	None [7:3]					VALUE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	VALUE	Maximum value of block-based index register. The number and size blocks in an MPC is design time configurable and for embedded memories defaults to covering the entire memory using 4kB blocks; see product datasheet for details on protection of external memories. Default Value: 3

6.1.18 RAMC0_MPC0_ROT_BLK_CFG

Same as BLK_CFG

Address: 0x4211420C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				R			
Name	None [7:4]				BLOCK_SIZE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	INIT_IN_PROGRESS	None [30:24]						

Bits	Name	Description
31	INIT_IN_PROGRESS	During initialization INIT_IN_PROGRESS is '1' and MMIO register accesses to ROT_BLK_LUT is RAZWI. The block attributes are retained in DeepSleep (and obviously Active) power mode. Initialization is only required from a power mode in which the block attributes are not retained. E.g., initialization is required for a cold boot (after a Power-on-Reset). HW initializes the block attributes: the NS attributes are set to '0' (secure), the R attributes are set to '1' (read access allowed) and the W attributes are set to '1' (write access allowed). During initialization, the MPC supports memory accesses (memory accesses are NOT blocked) with the initialization block attribute values as mentioned above. This e.g. allows MPC initialization to proceed in parallel with boot program memory accesses (as opposed to serializing the two), improving device boot time. Default Value: 1
3 : 0	BLOCK_SIZE	Block size of individually protected blocks (0: 32B, 1: 64B, ...up to 15:1MB) Block size= (1<<(BLOCK_SIZE+5)) The number and size blocks in an MPC is design time configurable and for embedded memories defaults to covering the entire memory using 4kB blocks; see product datasheet for details on protection of external memories. Default Value: 6

6.1.19 RAMC0_MPC0_ROT_BLK_IDX

Index of 8-block group accessed through ROT_BLK_LUT_*

Address: 0x42114210

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					RW		
Name	None [7:3]					VALUE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	VALUE	Index value for accessing block-based lookup table using ROT_BLK_LUT. Programming out of LUT range is an user error and it loops back to "0" once overflow occurs. Default Value: 0

6.1.20 RAMC0_MPC0_ROT_BLK_PC

Protection context of 8-block group accesses through ROT_BLK_LUT

Address: 0x42114214

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				PC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	PC	Specify PC values for ROT_BLK_IDX and ROT_BLK_LUT Default Value: 0

6.1.21 RAMC0_MPC0_ROT_BLK_LUT

(R,W,NS) bits for 8 blocks at ROT_BLK_IDX for PC=ROT_BKL_PC

Address: 0x42114218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	RW			None	RW		
Name	None	ATTR1 [6:4]			None	ATTR0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW			None	RW		
HW Access	None	RW			None	RW		
Name	None	ATTR3 [14:12]			None	ATTR2 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW			None	RW		
HW Access	None	RW			None	RW		
Name	None	ATTR5 [22:20]			None	ATTR4 [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW			None	RW		
HW Access	None	RW			None	RW		
Name	None	ATTR7 [30:28]			None	ATTR6 [26:24]		

Bits	Name	Description
30 : 28	ATTR7	W/R/NS bits for block 7 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
26 : 24	ATTR6	W/R/NS bits for block 6 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
22 : 20	ATTR5	W/R/NS bits for block 5 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
18 : 16	ATTR4	W/R/NS bits for block 4 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
14 : 12	ATTR3	W/R/NS bits for block 3 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
10 : 8	ATTR2	W/R/NS bits for block 2 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
6 : 4	ATTR1	W/R/NS bits for block 1 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0
2 : 0	ATTR0	W/R/NS bits for block 0 indicated by ROT_BLK_IDX for ROT_BLK_PC PC Default Value: 0

7 Fault Monitoring registers

This section discusses the Fault Monitoring registers. It lists all the registers in mapping tables, in address order.

7.1 Register details

Register	Address	Description
FAULT_STRUCT0_CTL	0x421E0000	Fault control
FAULT_STRUCT0_STATUS	0x421E000C	Fault status
FAULT_STRUCT0_DATA0	0x421E0010	Fault data
FAULT_STRUCT0_DATA1	0x421E0014	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT0_DATA2	0x421E0018	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT0_DATA3	0x421E001C	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT0_PENDING0	0x421E0040	Fault pending 0
FAULT_STRUCT0_PENDING1	0x421E0044	Fault pending 1
FAULT_STRUCT0_PENDING2	0x421E0048	Fault pending 2
FAULT_STRUCT0_MASK0	0x421E0050	Fault mask 0
FAULT_STRUCT0_INTR	0x421E00C0	Interrupt
FAULT_STRUCT0_INTR_SET	0x421E00C4	Interrupt set
FAULT_STRUCT0_INTR_MASK	0x421E00C8	Interrupt mask
FAULT_STRUCT0_INTR_MASKED	0x421E00CC	Interrupt masked

7.1.1 FAULT_STRUCT0_CTL

Fault control

Address: 0x421E0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					RESET_REQ_EN	OUT_EN	TR_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	RESET_REQ_EN	Reset request enable: '0': Disabled. '1': Enabled. The output reset request signal "fault_reset_req" reflects STATUS.VALID. This reset causes a warm/soft/core reset. This warm/soft/core reset does not affect the fault logic STATUS, DATA0, ..., DATA3 registers (allowing for post soft reset failure analysis). The "fault_reset_req" signals of the individual fault report structures are combined (logically OR'd) into a single SRSS "fault_reset_req" signal. Default Value: 0
1	OUT_EN	IO output signal enable: '0': Disabled. The IO output signal "fault_out" is '0'. The IO output enable signal "fault_out_en" is '0'. '1': Enabled. The IO output signal "fault_out" reflects STATUS.VALID. The IO output enable signal "fault_out_en" is '1'. Default Value: 0
0	TR_EN	Trigger output enable: '0': Disabled. The trigger output "tr_fault" is '0'. '1': Enabled. The trigger output "tr_fault" reflects STATUS.VALID. The trigger can be used to initiate a Datawire transfer of the FAULT data (FAULT_DATA0 through FAULT_DATA3). Default Value: 0

7.1.2 FAULT_STRUCT0_STATUS

Fault status

Address: 0x421E000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	W						
Name	None	IDX [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW1S	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	Valid indication: '0': Invalid. '1': Valid. STATUS.IDX, DATA0, ..., DATA3 specify the fault. Note: Typically, HW sets this field to '1' (on an activated HW fault source that is "enabled" by the MASK registers) and SW clears this field to '0' (typically by boot code SW (after a warm system reset, when the fault is handled). In this typical use case scenario, the HW source fault data is simultaneously captured into DATA0, ..., DATA3 when the VALID field is set to '1'. An exceptional SW use case scenario is identified as well. In this scenario, SW sets this field to '1' with a fault source index different to one of the defined HW fault sources. SW update is not restricted by the MASK registers). In both use case scenarios, the following holds: - STATUS.IDX, DATA0, ..., DATA3 can only be written when STATUS.VALID is '0'; the fault structure is not in use yet. Writing STATUS.VALID to '1' effectively locks the fault structure (until SW clears STATUS.VALID to '0'). This restriction requires a SW update to sequentially update the DATA registers followed by an update of the STATUS register. Note: For the exceptional SW use case, sequential updates to the DATA and STATUS registers may be "interrupted" by a HW fault capture. In this case, the SW DATA register updates are over-written by the HW update (and the STATUS.IDX field will reflect the HW capture) Default Value: 0
6 : 0	IDX	The fault source index for which fault information is captured in DATA0 through DATA3. The fault information is fault source specific and described below. Note: this register field (and associated fault source data in DATA0 through DATA3) should only be considered valid, when VALID is '1'. The description of the encoded meaning of this field is comes from the Fault assignment in the Product TRM. Default Value: Undefined

7.1.3 FAULT_STRUCT0_DATA0

Fault data

Address: 0x421E0010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Captured fault source data. Note: the DATA registers can only be written when STATUS.VALID is '0'. Note: the fault source index STATUS.IDX specifies the format of the DATA registers. Default Value: Undefined

7.1.4 FAULT_STRUCT0_PENDING0

Fault pending 0

Address: 0x421E0040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SOURCE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SOURCE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	SOURCE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	SOURCE [31:24]							

Bits	Name	Description
31 : 0	SOURCE	This field specifies the fault source. The list of fault sources is in the PSOC™ Control C3 architecture reference manual 8.3 Fault Sources. Default Value: Undefined

7.1.5 FAULT_STRUCT0_PENDING1

Fault pending 1

Address: 0x421E0044

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SOURCE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SOURCE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	SOURCE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	SOURCE [31:24]							

Bits	Name	Description
31 : 0	SOURCE	This field specifies the following sources: Bit 0: Peripheral group 0 PPU. Bit 1: Peripheral group 1 PPU. Bit 2: Peripheral group 2 PPU. Bit 3: Peripheral group 3 PPU. Bit 4: Peripheral group 4 PPU. Bit 5: Peripheral group 5 PPU. Bit 6: Peripheral group 6 PPU. Bit 7: Peripheral group 7 PPU. ... Bit 15: Peripheral group 15 PPU. Bit 16 - 31: See STATUS register. Default Value: Undefined

7.1.6 FAULT_STRUCT0_PENDING2

Fault pending 2

Address: 0x421E0048

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SOURCE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SOURCE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	SOURCE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	SOURCE [31:24]							

Bits	Name	Description
31 : 0	SOURCE	This field specifies the following sources: Bit 0 - 31: See STATUS register. Default Value: Undefined

7.1.7 FAULT_STRUCT0_MASK0

Fault mask 0

Address: 0x421E0050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SOURCE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SOURCE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SOURCE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	SOURCE [31:24]							

Bits	Name	Description
31 : 0	SOURCE	Fault source enables: Bits 31-0: Fault sources 31 to 0. Default Value: 0

7.1.8 FAULT_STRUCT0_INTR

Interrupt

Address: 0x421E00C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [7:1]							FAULT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	FAULT	This interrupt cause field is activated (HW sets the field to '1') when an enabled (MASK0/MASK1/MASK2) pending fault source is captured: - STATUS.VALID is set to '1'. - STATUS.IDX specifies the fault source index. - DATA0 through DATA3 captures the fault source data. SW writes a '1' to this field to clear the interrupt cause to '0'. SW clear STATUS.VALID to '0' to enable capture of the next fault. Note that when there is an enabled pending fault source, the pending fault source is captured immediately and INTR.FAULT is immediately activated (set to '1'). Default Value: 0

7.1.9 FAULT_STRUCT0_INTR_SET

Interrupt set

Address: 0x421E00C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							A
Name	None [7:1]							FAULT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	FAULT	SW writes a '1' to this field to set the corresponding field in the INTR register. Default Value: 0

7.1.10 FAULT_STRUCT0_INTR_MASK

Interrupt mask

Address: 0x421E00C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							FAULT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	FAULT	Mask bit for corresponding field in the INTR register. Default Value: 0

7.1.11 FAULT_STRUCT0_INTR_MASKED

Interrupt masked

Address: 0x421E00CC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							FAULT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	FAULT	Logical and of corresponding INTR and INTR_MASK fields. Default Value: 0

8 Program and Debug Interface registers

This section discusses the Program and Debug Interface registers. It lists all the registers in mapping tables, in address order.

8.1 Register details

Register	Address	Description
DEBUG600_VERSION	0x42250000	IP Version Information

8.1.1 DEBUG600_VERSION

IP Version Information

Address: 0x42250000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	MINOR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	MAJOR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	MAJOR	IP Major Revision Number Default Value: Undefined
7 : 0	MINOR	IP Minor Revision Number Default Value: Undefined

9 Protection Unit registers

This section discusses the Protection Unit registers. It lists all the registers in mapping tables, in address order.

9.1 Register details

Register	Address	Description
PPC0_PPC_CTL	0x42020000	PPC Control Registers
PPC0_PPC_LOCK_MASK	0x4202000C	Locked Mask
PPC0_PPC_PC_MASK0	0x42021000	Protection Context Mask. This is the starting address of a register bank containing 222 registers (PPC0_PPC_PC_MASK0 to PPC0_PPC_PC_MASK221).
PPC0_PPC_NS_ATT0	0x42022000	Non-secure attribute
PPC0_PPC_NS_ATT1	0x42022004	Non-secure attribute. See PPC0_PPC_NS_ATT0 for the details of bit fields.
PPC0_PPC_NS_ATT2	0x42022008	Non-secure attribute. See PPC0_PPC_NS_ATT0 for the details of bit fields.
PPC0_PPC_NS_ATT3	0x4202200C	Non-secure attribute. See PPC0_PPC_NS_ATT0 for the details of bit fields.
PPC0_PPC_NS_ATT4	0x42022010	Non-secure attribute. See PPC0_PPC_NS_ATT0 for the details of bit fields.
PPC0_PPC_NS_ATT5	0x42022014	Non-secure attribute. See PPC0_PPC_NS_ATT0 for the details of bit fields.
PPC0_PPC_NS_ATT6	0x42022018	Non-secure attribute. See PPC0_PPC_NS_ATT0 for the details of bit fields.
PPC0_PPC_S_P_ATT0	0x42022400	Secure Privilege Attribute
PPC0_PPC_S_P_ATT1	0x42022404	Secure Privilege Attribute. See PPC0_PPC_S_P_ATT0 for the details of bit fields.
PPC0_PPC_S_P_ATT2	0x42022408	Secure Privilege Attribute. See PPC0_PPC_S_P_ATT0 for the details of bit fields.
PPC0_PPC_S_P_ATT3	0x4202240C	Secure Privilege Attribute. See PPC0_PPC_S_P_ATT0 for the details of bit fields.
PPC0_PPC_S_P_ATT4	0x42022410	Secure Privilege Attribute. See PPC0_PPC_S_P_ATT0 for the details of bit fields.
PPC0_PPC_S_P_ATT5	0x42022414	Secure Privilege Attribute. See PPC0_PPC_S_P_ATT0 for the details of bit fields.
PPC0_PPC_S_P_ATT6	0x42022418	Secure Privilege Attribute. See PPC0_PPC_S_P_ATT0 for the details of bit fields.
PPC0_PPC_NS_P_ATT0	0x42024000	Non-secure Privilege Attribute

Protection Unit registers

Register	Address	Description
PPC0_PPC_NS_P_ATT1	0x42024004	Non-secure Privilege Attribute. See PPC0_PPC_NS_P_ATT0 for the details of bit fields.
PPC0_PPC_NS_P_ATT2	0x42024008	Non-secure Privilege Attribute. See PPC0_PPC_NS_P_ATT0 for the details of bit fields.
PPC0_PPC_NS_P_ATT3	0x4202400C	Non-secure Privilege Attribute. See PPC0_PPC_NS_P_ATT0 for the details of bit fields.
PPC0_PPC_NS_P_ATT4	0x42024010	Non-secure Privilege Attribute. See PPC0_PPC_NS_P_ATT0 for the details of bit fields.
PPC0_PPC_NS_P_ATT5	0x42024014	Non-secure Privilege Attribute. See PPC0_PPC_NS_P_ATT0 for the details of bit fields.
PPC0_PPC_NS_P_ATT6	0x42024018	Non-secure Privilege Attribute. See PPC0_PPC_NS_P_ATT0 for the details of bit fields.
PPC0_PPC_R_ADDR0	0x42025000	Region Address
PPC0_PPC_R_ADDR1	0x42025004	Region Address
PPC0_PPC_R_ADDR2	0x42025008	Region Address
PPC0_PPC_R_ADDR3	0x4202500C	Region Address
PPC0_PPC_R_ADDR4	0x42025010	Region Address
PPC0_PPC_R_ADDR5	0x42025014	Region Address
PPC0_PPC_R_ADDR6	0x42025018	Region Address
PPC0_PPC_R_ADDR7	0x4202501C	Region Address
PPC0_PPC_R_ADDR8	0x42025020	Region Address
PPC0_PPC_R_ADDR9	0x42025024	Region Address
PPC0_PPC_R_ADDR10	0x42025028	Region Address
PPC0_PPC_R_ADDR11	0x4202502C	Region Address
PPC0_PPC_R_ADDR12	0x42025030	Region Address
PPC0_PPC_R_ADDR13	0x42025034	Region Address
PPC0_PPC_R_ADDR14	0x42025038	Region Address
PPC0_PPC_R_ADDR15	0x4202503C	Region Address
PPC0_PPC_R_ADDR16	0x42025040	Region Address
PPC0_PPC_R_ADDR17	0x42025044	Region Address
PPC0_PPC_R_ADDR18	0x42025048	Region Address
PPC0_PPC_R_ADDR19	0x4202504C	Region Address
PPC0_PPC_R_ADDR20	0x42025050	Region Address
PPC0_PPC_R_ADDR21	0x42025054	Region Address
PPC0_PPC_R_ADDR22	0x42025058	Region Address
PPC0_PPC_R_ADDR23	0x4202505C	Region Address

Protection Unit registers

Register	Address	Description
PPC0_PPC_R_ADDR24	0x42025060	Region Address
PPC0_PPC_R_ADDR25	0x42025064	Region Address
PPC0_PPC_R_ADDR26	0x42025068	Region Address
PPC0_PPC_R_ADDR27	0x4202506C	Region Address
PPC0_PPC_R_ADDR28	0x42025070	Region Address
PPC0_PPC_R_ADDR29	0x42025074	Region Address
PPC0_PPC_R_ADDR30	0x42025078	Region Address
PPC0_PPC_R_ADDR31	0x4202507C	Region Address
PPC0_PPC_R_ADDR32	0x42025080	Region Address
PPC0_PPC_R_ADDR33	0x42025084	Region Address
PPC0_PPC_R_ADDR34	0x42025088	Region Address
PPC0_PPC_R_ADDR35	0x4202508C	Region Address
PPC0_PPC_R_ADDR36	0x42025090	Region Address
PPC0_PPC_R_ADDR37	0x42025094	Region Address
PPC0_PPC_R_ADDR38	0x42025098	Region Address
PPC0_PPC_R_ADDR39	0x4202509C	Region Address
PPC0_PPC_R_ADDR40	0x420250A0	Region Address
PPC0_PPC_R_ADDR41	0x420250A4	Region Address
PPC0_PPC_R_ADDR42	0x420250A8	Region Address
PPC0_PPC_R_ADDR43	0x420250AC	Region Address
PPC0_PPC_R_ADDR44	0x420250B0	Region Address
PPC0_PPC_R_ADDR45	0x420250B4	Region Address
PPC0_PPC_R_ADDR46	0x420250B8	Region Address
PPC0_PPC_R_ADDR47	0x420250BC	Region Address
PPC0_PPC_R_ADDR48	0x420250C0	Region Address
PPC0_PPC_R_ADDR49	0x420250C4	Region Address
PPC0_PPC_R_ADDR50	0x420250C8	Region Address
PPC0_PPC_R_ADDR51	0x420250CC	Region Address
PPC0_PPC_R_ADDR52	0x420250D0	Region Address
PPC0_PPC_R_ADDR53	0x420250D4	Region Address
PPC0_PPC_R_ADDR54	0x420250D8	Region Address
PPC0_PPC_R_ADDR55	0x420250DC	Region Address
PPC0_PPC_R_ADDR56	0x420250E0	Region Address
PPC0_PPC_R_ADDR57	0x420250E4	Region Address
PPC0_PPC_R_ADDR58	0x420250E8	Region Address
PPC0_PPC_R_ADDR59	0x420250EC	Region Address

Protection Unit registers

Register	Address	Description
PPC0_PPC_R_ADDR60	0x420250F0	Region Address
PPC0_PPC_R_ADDR61	0x420250F4	Region Address
PPC0_PPC_R_ADDR62	0x420250F8	Region Address
PPC0_PPC_R_ADDR63	0x420250FC	Region Address
PPC0_PPC_R_ADDR64	0x42025100	Region Address
PPC0_PPC_R_ADDR65	0x42025104	Region Address
PPC0_PPC_R_ADDR66	0x42025108	Region Address
PPC0_PPC_R_ADDR67	0x4202510C	Region Address
PPC0_PPC_R_ADDR68	0x42025110	Region Address
PPC0_PPC_R_ADDR69	0x42025114	Region Address
PPC0_PPC_R_ADDR70	0x42025118	Region Address
PPC0_PPC_R_ADDR71	0x4202511C	Region Address
PPC0_PPC_R_ADDR72	0x42025120	Region Address
PPC0_PPC_R_ADDR73	0x42025124	Region Address
PPC0_PPC_R_ADDR74	0x42025128	Region Address
PPC0_PPC_R_ADDR75	0x4202512C	Region Address
PPC0_PPC_R_ADDR76	0x42025130	Region Address
PPC0_PPC_R_ADDR77	0x42025134	Region Address
PPC0_PPC_R_ADDR78	0x42025138	Region Address
PPC0_PPC_R_ADDR79	0x4202513C	Region Address
PPC0_PPC_R_ADDR80	0x42025140	Region Address
PPC0_PPC_R_ADDR81	0x42025144	Region Address
PPC0_PPC_R_ADDR82	0x42025148	Region Address
PPC0_PPC_R_ADDR83	0x4202514C	Region Address
PPC0_PPC_R_ADDR84	0x42025150	Region Address
PPC0_PPC_R_ADDR85	0x42025154	Region Address
PPC0_PPC_R_ADDR86	0x42025158	Region Address
PPC0_PPC_R_ADDR87	0x4202515C	Region Address
PPC0_PPC_R_ADDR88	0x42025160	Region Address
PPC0_PPC_R_ADDR89	0x42025164	Region Address
PPC0_PPC_R_ADDR90	0x42025168	Region Address
PPC0_PPC_R_ADDR91	0x4202516C	Region Address
PPC0_PPC_R_ADDR92	0x42025170	Region Address
PPC0_PPC_R_ADDR93	0x42025174	Region Address
PPC0_PPC_R_ADDR94	0x42025178	Region Address
PPC0_PPC_R_ADDR95	0x4202517C	Region Address

Protection Unit registers

Register	Address	Description
PPC0_PPC_R_ADDR96	0x42025180	Region Address
PPC0_PPC_R_ADDR97	0x42025184	Region Address
PPC0_PPC_R_ADDR98	0x42025188	Region Address
PPC0_PPC_R_ADDR99	0x4202518C	Region Address
PPC0_PPC_R_ADDR100	0x42025190	Region Address
PPC0_PPC_R_ADDR101	0x42025194	Region Address
PPC0_PPC_R_ADDR102	0x42025198	Region Address
PPC0_PPC_R_ADDR103	0x4202519C	Region Address
PPC0_PPC_R_ADDR104	0x420251A0	Region Address
PPC0_PPC_R_ADDR105	0x420251A4	Region Address
PPC0_PPC_R_ADDR106	0x420251A8	Region Address
PPC0_PPC_R_ADDR107	0x420251AC	Region Address
PPC0_PPC_R_ADDR108	0x420251B0	Region Address
PPC0_PPC_R_ADDR109	0x420251B4	Region Address
PPC0_PPC_R_ADDR110	0x420251B8	Region Address
PPC0_PPC_R_ADDR111	0x420251BC	Region Address
PPC0_PPC_R_ADDR112	0x420251C0	Region Address
PPC0_PPC_R_ADDR113	0x420251C4	Region Address
PPC0_PPC_R_ADDR114	0x420251C8	Region Address
PPC0_PPC_R_ADDR115	0x420251CC	Region Address
PPC0_PPC_R_ADDR116	0x420251D0	Region Address
PPC0_PPC_R_ADDR117	0x420251D4	Region Address
PPC0_PPC_R_ADDR118	0x420251D8	Region Address
PPC0_PPC_R_ADDR119	0x420251DC	Region Address
PPC0_PPC_R_ADDR120	0x420251E0	Region Address
PPC0_PPC_R_ADDR121	0x420251E4	Region Address
PPC0_PPC_R_ADDR122	0x420251E8	Region Address
PPC0_PPC_R_ADDR123	0x420251EC	Region Address
PPC0_PPC_R_ADDR124	0x420251F0	Region Address
PPC0_PPC_R_ADDR125	0x420251F4	Region Address
PPC0_PPC_R_ADDR126	0x420251F8	Region Address
PPC0_PPC_R_ADDR127	0x420251FC	Region Address
PPC0_PPC_R_ADDR128	0x42025200	Region Address
PPC0_PPC_R_ADDR129	0x42025204	Region Address
PPC0_PPC_R_ADDR130	0x42025208	Region Address
PPC0_PPC_R_ADDR131	0x4202520C	Region Address

Protection Unit registers

Register	Address	Description
PPC0_PPC_R_ADDR132	0x42025210	Region Address
PPC0_PPC_R_ADDR133	0x42025214	Region Address
PPC0_PPC_R_ADDR134	0x42025218	Region Address
PPC0_PPC_R_ADDR135	0x4202521C	Region Address
PPC0_PPC_R_ADDR136	0x42025220	Region Address
PPC0_PPC_R_ADDR137	0x42025224	Region Address
PPC0_PPC_R_ADDR138	0x42025228	Region Address
PPC0_PPC_R_ADDR139	0x4202522C	Region Address
PPC0_PPC_R_ADDR140	0x42025230	Region Address
PPC0_PPC_R_ADDR141	0x42025234	Region Address
PPC0_PPC_R_ADDR142	0x42025238	Region Address
PPC0_PPC_R_ADDR143	0x4202523C	Region Address
PPC0_PPC_R_ADDR144	0x42025240	Region Address
PPC0_PPC_R_ADDR145	0x42025244	Region Address
PPC0_PPC_R_ADDR146	0x42025248	Region Address
PPC0_PPC_R_ADDR147	0x4202524C	Region Address
PPC0_PPC_R_ADDR148	0x42025250	Region Address
PPC0_PPC_R_ADDR149	0x42025254	Region Address
PPC0_PPC_R_ADDR150	0x42025258	Region Address
PPC0_PPC_R_ADDR151	0x4202525C	Region Address
PPC0_PPC_R_ADDR152	0x42025260	Region Address
PPC0_PPC_R_ADDR153	0x42025264	Region Address
PPC0_PPC_R_ADDR154	0x42025268	Region Address
PPC0_PPC_R_ADDR155	0x4202526C	Region Address
PPC0_PPC_R_ADDR156	0x42025270	Region Address
PPC0_PPC_R_ADDR157	0x42025274	Region Address
PPC0_PPC_R_ADDR158	0x42025278	Region Address
PPC0_PPC_R_ADDR159	0x4202527C	Region Address
PPC0_PPC_R_ADDR160	0x42025280	Region Address
PPC0_PPC_R_ADDR161	0x42025284	Region Address
PPC0_PPC_R_ADDR162	0x42025288	Region Address
PPC0_PPC_R_ADDR163	0x4202528C	Region Address
PPC0_PPC_R_ADDR164	0x42025290	Region Address
PPC0_PPC_R_ADDR165	0x42025294	Region Address
PPC0_PPC_R_ADDR166	0x42025298	Region Address
PPC0_PPC_R_ADDR167	0x4202529C	Region Address

Protection Unit registers

Register	Address	Description
PPC0_PPC_R_ADDR168	0x420252A0	Region Address
PPC0_PPC_R_ADDR169	0x420252A4	Region Address
PPC0_PPC_R_ADDR170	0x420252A8	Region Address
PPC0_PPC_R_ADDR171	0x420252AC	Region Address
PPC0_PPC_R_ADDR172	0x420252B0	Region Address
PPC0_PPC_R_ADDR173	0x420252B4	Region Address
PPC0_PPC_R_ADDR174	0x420252B8	Region Address
PPC0_PPC_R_ADDR175	0x420252BC	Region Address
PPC0_PPC_R_ADDR176	0x420252C0	Region Address
PPC0_PPC_R_ADDR177	0x420252C4	Region Address
PPC0_PPC_R_ADDR178	0x420252C8	Region Address
PPC0_PPC_R_ADDR179	0x420252CC	Region Address
PPC0_PPC_R_ADDR180	0x420252D0	Region Address
PPC0_PPC_R_ADDR181	0x420252D4	Region Address
PPC0_PPC_R_ADDR182	0x420252D8	Region Address
PPC0_PPC_R_ADDR183	0x420252DC	Region Address
PPC0_PPC_R_ADDR184	0x420252E0	Region Address
PPC0_PPC_R_ADDR185	0x420252E4	Region Address
PPC0_PPC_R_ADDR186	0x420252E8	Region Address
PPC0_PPC_R_ADDR187	0x420252EC	Region Address
PPC0_PPC_R_ADDR188	0x420252F0	Region Address
PPC0_PPC_R_ADDR189	0x420252F4	Region Address
PPC0_PPC_R_ADDR190	0x420252F8	Region Address
PPC0_PPC_R_ADDR191	0x420252FC	Region Address
PPC0_PPC_R_ADDR192	0x42025300	Region Address
PPC0_PPC_R_ADDR193	0x42025304	Region Address
PPC0_PPC_R_ADDR194	0x42025308	Region Address
PPC0_PPC_R_ADDR195	0x4202530C	Region Address
PPC0_PPC_R_ADDR196	0x42025310	Region Address
PPC0_PPC_R_ADDR197	0x42025314	Region Address
PPC0_PPC_R_ADDR198	0x42025318	Region Address
PPC0_PPC_R_ADDR199	0x4202531C	Region Address
PPC0_PPC_R_ADDR200	0x42025320	Region Address
PPC0_PPC_R_ADDR201	0x42025324	Region Address
PPC0_PPC_R_ADDR202	0x42025328	Region Address
PPC0_PPC_R_ADDR203	0x4202532C	Region Address

Protection Unit registers

Register	Address	Description
PPC0_PPC_R_ADDR204	0x42025330	Region Address
PPC0_PPC_R_ADDR205	0x42025334	Region Address
PPC0_PPC_R_ADDR206	0x42025338	Region Address
PPC0_PPC_R_ADDR207	0x4202533C	Region Address
PPC0_PPC_R_ADDR208	0x42025340	Region Address
PPC0_PPC_R_ADDR209	0x42025344	Region Address
PPC0_PPC_R_ADDR210	0x42025348	Region Address
PPC0_PPC_R_ADDR211	0x4202534C	Region Address
PPC0_PPC_R_ADDR212	0x42025350	Region Address
PPC0_PPC_R_ADDR213	0x42025354	Region Address
PPC0_PPC_R_ADDR214	0x42025358	Region Address
PPC0_PPC_R_ADDR215	0x4202535C	Region Address
PPC0_PPC_R_ADDR216	0x42025360	Region Address
PPC0_PPC_R_ADDR217	0x42025364	Region Address
PPC0_PPC_R_ADDR218	0x42025368	Region Address
PPC0_PPC_R_ADDR219	0x4202536C	Region Address
PPC0_PPC_R_ADDR220	0x42025370	Region Address
PPC0_PPC_R_ADDR221	0x42025374	Region Address
PPC0_PPC_R_ATT0	0x42026000	Region Attribute
PPC0_PPC_R_ATT1	0x42026004	Region Attribute
PPC0_PPC_R_ATT2	0x42026008	Region Attribute
PPC0_PPC_R_ATT3	0x4202600C	Region Attribute. See PPC0_PPC_R_ATT2 for the details of bit fields.
PPC0_PPC_R_ATT4	0x42026010	Region Attribute. See PPC0_PPC_R_ATT2 for the details of bit fields.
PPC0_PPC_R_ATT5	0x42026014	Region Attribute. See PPC0_PPC_R_ATT2 for the details of bit fields.
PPC0_PPC_R_ATT6	0x42026018	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT7	0x4202601C	Region Attribute. This is the starting address of a register bank containing 47 registers (PPC0_PPC_R_ATT7 to PPC0_PPC_R_ATT219).
PPC0_PPC_R_ATT13	0x42026034	Region Attribute
PPC0_PPC_R_ATT14	0x42026038	Region Attribute. See PPC0_PPC_R_ATT0 for the details of bit fields.
PPC0_PPC_R_ATT13	0x4202603C	Region Attribute. See PPC0_PPC_R_ATT0 for the details of bit fields.
PPC0_PPC_R_ATT16	0x42026040	Region Attribute
PPC0_PPC_R_ATT17	0x42026044	Region Attribute. See PPC0_PPC_R_ATT16 for the details of bit fields.
PPC0_PPC_R_ATT18	0x42026048	Region Attribute. This is the starting address of a register bank containing 61 registers (PPC0_PPC_R_ATT18 to PPC0_PPC_R_ATT217).
PPC0_PPC_R_ATT19	0x4202604C	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.

Protection Unit registers

Register	Address	Description
PPC0_PPC_R_ATT20	0x42026050	Region Attribute. This is the starting address of a register bank containing 33 registers (PPC0_PPC_R_ATT20 to PPC0_PPC_R_ATT216).
PPC0_PPC_R_ATT22	0x42026058	Region Attribute. See PPC0_PPC_R_ATT2 for the details of bit fields.
PPC0_PPC_R_ATT23	0x4202605C	Region Attribute. See PPC0_PPC_R_ATT2 for the details of bit fields.
PPC0_PPC_R_ATT26	0x42026068	Region Attribute. See PPC0_PPC_R_ATT2 for the details of bit fields.
PPC0_PPC_R_ATT27	0x4202606C	Region Attribute. See PPC0_PPC_R_ATT2 for the details of bit fields.
PPC0_PPC_R_ATT28	0x42026070	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT29	0x42026074	Region Attribute. See PPC0_PPC_R_ATT2 for the details of bit fields.
PPC0_PPC_R_ATT30	0x42026078	Region Attribute
PPC0_PPC_R_ATT31	0x4202607C	Region Attribute
PPC0_PPC_R_ATT32	0x42026080	Region Attribute. See PPC0_PPC_R_ATT30 for the details of bit fields.
PPC0_PPC_R_ATT34	0x42026088	Region Attribute. See PPC0_PPC_R_ATT2 for the details of bit fields.
PPC0_PPC_R_ATT35	0x4202608C	Region Attribute. See PPC0_PPC_R_ATT2 for the details of bit fields.
PPC0_PPC_R_ATT37	0x42026094	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT38	0x42026098	Region Attribute
PPC0_PPC_R_ATT42	0x420260A8	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC0_PPC_R_ATT47	0x420260BC	Region Attribute
PPC0_PPC_R_ATT48	0x420260C0	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC0_PPC_R_ATT49	0x420260C4	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC0_PPC_R_ATT50	0x420260C8	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC0_PPC_R_ATT51	0x420260CC	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC0_PPC_R_ATT84	0x42026150	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC0_PPC_R_ATT88	0x42026160	Region Attribute. See PPC0_PPC_R_ATT30 for the details of bit fields.
PPC0_PPC_R_ATT90	0x42026168	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT101	0x42026194	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT102	0x42026198	Region Attribute. See PPC0_PPC_R_ATT2 for the details of bit fields.
PPC0_PPC_R_ATT103	0x4202619C	Region Attribute. See PPC0_PPC_R_ATT2 for the details of bit fields.
PPC0_PPC_R_ATT104	0x420261A0	Region Attribute. See PPC0_PPC_R_ATT2 for the details of bit fields.
PPC0_PPC_R_ATT105	0x420261A4	Region Attribute. See PPC0_PPC_R_ATT2 for the details of bit fields.
PPC0_PPC_R_ATT106	0x420261A8	Region Attribute. See PPC0_PPC_R_ATT30 for the details of bit fields.
PPC0_PPC_R_ATT107	0x420261AC	Region Attribute. See PPC0_PPC_R_ATT30 for the details of bit fields.
PPC0_PPC_R_ATT109	0x420261B4	Region Attribute. See PPC0_PPC_R_ATT47 for the details of bit fields.
PPC0_PPC_R_ATT111	0x420261BC	Region Attribute. See PPC0_PPC_R_ATT30 for the details of bit fields.
PPC0_PPC_R_ATT112	0x420261C0	Region Attribute
PPC0_PPC_R_ATT113	0x420261C4	Region Attribute

Protection Unit registers

Register	Address	Description
PPC0_PPC_R_ATT114	0x420261C8	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT116	0x420261D0	Region Attribute. See PPC0_PPC_R_ATT30 for the details of bit fields.
PPC0_PPC_R_ATT118	0x420261D8	Region Attribute. See PPC0_PPC_R_ATT0 for the details of bit fields.
PPC0_PPC_R_ATT120	0x420261E0	Region Attribute. See PPC0_PPC_R_ATT30 for the details of bit fields.
PPC0_PPC_R_ATT121	0x420261E4	Region Attribute. See PPC0_PPC_R_ATT30 for the details of bit fields.
PPC0_PPC_R_ATT122	0x420261E8	Region Attribute. See PPC0_PPC_R_ATT2 for the details of bit fields.
PPC0_PPC_R_ATT127	0x420261FC	Region Attribute. See PPC0_PPC_R_ATT16 for the details of bit fields.
PPC0_PPC_R_ATT129	0x42026204	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT130	0x42026208	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT131	0x4202620C	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT132	0x42026210	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT133	0x42026214	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT134	0x42026218	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT135	0x4202621C	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT136	0x42026220	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT137	0x42026224	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT138	0x42026228	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT149	0x42026254	Region Attribute. See PPC0_PPC_R_ATT30 for the details of bit fields.
PPC0_PPC_R_ATT150	0x42026258	Region Attribute. See PPC0_PPC_R_ATT30 for the details of bit fields.
PPC0_PPC_R_ATT173	0x420262B4	Region Attribute. See PPC0_PPC_R_ATT1 for the details of bit fields.
PPC0_PPC_R_ATT181	0x420262D4	Region Attribute. See PPC0_PPC_R_ATT16 for the details of bit fields.
PPC0_PPC_R_ATT182	0x420262D8	Region Attribute. See PPC0_PPC_R_ATT112 for the details of bit fields.
PPC0_PPC_R_ATT184	0x420262E0	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC0_PPC_R_ATT186	0x420262E8	Region Attribute. See PPC0_PPC_R_ATT31 for the details of bit fields.
PPC0_PPC_R_ATT187	0x420262EC	Region Attribute
PPC0_PPC_R_ATT188	0x420262F0	Region Attribute. See PPC0_PPC_R_ATT187 for the details of bit fields.
PPC0_PPC_R_ATT190	0x420262F8	Region Attribute. See PPC0_PPC_R_ATT16 for the details of bit fields.
PPC0_PPC_R_ATT191	0x420262FC	Region Attribute. See PPC0_PPC_R_ATT16 for the details of bit fields.
PPC0_PPC_R_ATT192	0x42026300	Region Attribute. See PPC0_PPC_R_ATT16 for the details of bit fields.
PPC0_PPC_R_ATT193	0x42026304	Region Attribute. See PPC0_PPC_R_ATT16 for the details of bit fields.
PPC0_PPC_R_ATT194	0x42026308	Region Attribute. See PPC0_PPC_R_ATT16 for the details of bit fields.
PPC0_PPC_R_ATT195	0x4202630C	Region Attribute. See PPC0_PPC_R_ATT16 for the details of bit fields.
PPC0_PPC_R_ATT196	0x42026310	Region Attribute. See PPC0_PPC_R_ATT16 for the details of bit fields.

Protection Unit registers

Register	Address	Description
PPC0_PPC_R_ATT120	0x42026370	Region Attribute. See PPC0_PPC_R_ATT187 for the details of bit fields.
PPC0_PPC_R_ATT221	0x42026374	Region Attribute

9.1.1 PPC0_PPC_CTL

PPC Control Registers

Address: 0x42020000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							RESP_CFG

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	RESP_CFG	Response Configuration. This field configures the security violation response. 0 - Read-Zero Write Ignore (RZWI) 1 - Bus Error Default Value: 0

9.1.2 PPC0_PPC_LOCK_MASK

Locked Mask

Address: 0x4202000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	R							
Name	LOCK_MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	LOCK_MASK	A mask that indicates which protection contexts are 'locked'. Once locked, a protection context cannot be unlocked until the next reset or power cycle. Bit i specifies the locked status for protection context i. 0: The protection context is unlocked. 1: The protection context is locked. When a PC is locked, the PPC_PC_MASK, PPC_NS_ATT and PPC_S_P_ATT register bits for peripheral regions to which this PC has access can no longer be modified (PPC_NS_P_ATT is not subject to these restrictions). The one exception to this is that PPC_PC_MASK bits associated with other protection contexts that are not themselves locked can still be cleared (but not set). Default Value: 0

9.1.3 PPC0_PPC_PC_MASK0

Protection Context Mask

Address: 0x42021000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PC_MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	PC_MASK	A mask that indicates which protection contexts have access to a peripheral region. Bit i specifies the access for protection context i. 0: The protection context has no access to this region. 1: The protection context has access to this region, subject to secure and privilege attribute constraints setup in PPC_NS_ATT, PPC_S_P_ATT, PPC_NS_P_ATT registers) Default Value: 255

9.1.4 PPC0_PPC_NS_ATT0

Non-secure attribute

Address: 0x42022000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	NS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	NS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	NS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	NS [31:24]							

Bits	Name	Description
31 : 0	NS	Non-Secure. Each bit indicates whether access to a peripheral region must be secure or non-secure: IF SECURITY_AWARE=0 0 - allow only secure access to respective peripheral region. 1 - allow only non-secure access to respective peripheral region. IF SECURITY_AWARE=1 0 - allow only secure access to respective peripheral region. 1 - allows both secure and non-secure access to respective peripheral region. (Note that, depending on this setting the privilege access requirement for this region is specified in the corresponding PPC_S_P_ATT or PPC_NS_P_ATT register) Default Value: 0

9.1.5 PPC0_PPC_S_P_ATT0

Secure Privilege Attribute

Address: 0x42022400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	S_P [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	S_P [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	S_P [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	S_P [31:24]							

Bits	Name	Description
31 : 0	S_P	Secure Privilege. Each bit indicates whether access to a secure peripheral region requires privilege: 0 - allow only secure privileged access to respective peripheral region. 1 - allow only secure unprivileged or privileged access to respective peripheral region. Default Value: 0

9.1.6 PPC0_PPC_NS_P_ATT0

Non-secure Privilege Attribute

Address: 0x42024000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	NS_P [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	NS_P [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	NS_P [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	NS_P [31:24]							

Bits	Name	Description
31 : 0	NS_P	Non-Secure Privilege. Each bit indicates whether access to a non-secure peripheral region requires privilege: 0 - allow only non-secure privileged access to respective peripheral region. 1 - allow only non-secure unprivileged or privileged access to respective peripheral region. Default Value: 0

9.1.7 PPC0_PPC_R_ADDR0

Region Address

Address: 0x42025000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 276824064

9.1.8 PPC0_PPC_R_ADDR1

Region Address

Address: 0x42025004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 276828164

9.1.9 PPC0_PPC_R_ADDR2

Region Address

Address: 0x42025008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 276828176

9.1.10 PPC0_PPC_R_ADDR3

Region Address

Address: 0x4202500C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 276828192

9.1.11 PPC0_PPC_R_ADDR4

Region Address

Address: 0x42025010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 276828208

9.1.12 PPC0_PPC_R_ADDR5

Region Address

Address: 0x42025014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 276828224

9.1.13 PPC0_PPC_R_ADDR6

Region Address

Address: 0x42025018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 276828244

9.1.14 PPC0_PPC_R_ADDR7

Region Address

Address: 0x4202501C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 276828168

9.1.15 PPC0_PPC_R_ADDR8

Region Address

Address: 0x42025020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 276828184

9.1.16 PPC0_PPC_R_ADDR9

Region Address

Address: 0x42025024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 276828200

9.1.17 PPC0_PPC_R_ADDR10

Region Address

Address: 0x42025028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 276828216

9.1.18 PPC0_PPC_R_ADDR11

Region Address

Address: 0x4202502C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 276828232

9.1.19 PPC0_PPC_R_ADDR12

Region Address

Address: 0x42025030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 276828248

9.1.20 PPC0_PPC_R_ADDR13

Region Address

Address: 0x42025034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 276832256

9.1.21 PPC0_PPC_R_ADDR14

Region Address

Address: 0x42025038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 276856832

9.1.22 PPC0_PPC_R_ADDR15

Region Address

Address: 0x4202503C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 276860928

9.1.23 PPC0_PPC_R_ADDR16

Region Address

Address: 0x42025040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 276889600

9.1.24 PPC0_PPC_R_ADDR17

Region Address

Address: 0x42025044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277086208

9.1.25 PPC0_PPC_R_ADDR18

Region Address

Address: 0x42025048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277102592

9.1.26 PPC0_PPC_R_ADDR19

Region Address

Address: 0x4202504C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277102656

9.1.27 PPC0_PPC_R_ADDR20

Region Address

Address: 0x42025050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277102720

9.1.28 PPC0_PPC_R_ADDR21

Region Address

Address: 0x42025054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277106688

9.1.29 PPC0_PPC_R_ADDR22

Region Address

Address: 0x42025058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277106752

9.1.30 PPC0_PPC_R_ADDR23

Region Address

Address: 0x4202505C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277106816

9.1.31 PPC0_PPC_R_ADDR24

Region Address

Address: 0x42025060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277151744

9.1.32 PPC0_PPC_R_ADDR25

Region Address

Address: 0x42025064

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277152768

9.1.33 PPC0_PPC_R_ADDR26

Region Address

Address: 0x42025068

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277152832

9.1.34 PPC0_PPC_R_ADDR27

Region Address

Address: 0x4202506C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277152896

9.1.35 PPC0_PPC_R_ADDR28

Region Address

Address: 0x42025070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277168128

9.1.36 PPC0_PPC_R_ADDR29

Region Address

Address: 0x42025074

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277168192

9.1.37 PPC0_PPC_R_ADDR30

Region Address

Address: 0x42025078

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277168256

9.1.38 PPC0_PPC_R_ADDR31

Region Address

Address: 0x4202507C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277168384

9.1.39 PPC0_PPC_R_ADDR32

Region Address

Address: 0x42025080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277168640

9.1.40 PPC0_PPC_R_ADDR33

Region Address

Address: 0x42025084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277169152

9.1.41 PPC0_PPC_R_ADDR34

Region Address

Address: 0x42025088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277169216

9.1.42 PPC0_PPC_R_ADDR35

Region Address

Address: 0x4202508C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277169280

9.1.43 PPC0_PPC_R_ADDR36

Region Address

Address: 0x42025090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277170176

9.1.44 PPC0_PPC_R_ADDR37

Region Address

Address: 0x42025094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277170192

9.1.45 PPC0_PPC_R_ADDR38

Region Address

Address: 0x42025098

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277170688

9.1.46 PPC0_PPC_R_ADDR39

Region Address

Address: 0x4202509C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277184512

9.1.47 PPC0_PPC_R_ADDR40

Region Address

Address: 0x420250A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277185536

9.1.48 PPC0_PPC_R_ADDR41

Region Address

Address: 0x420250A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277185537

9.1.49 PPC0_PPC_R_ADDR42

Region Address

Address: 0x420250A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277186560

9.1.50 PPC0_PPC_R_ADDR43

Region Address

Address: 0x420250AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277186624

9.1.51 PPC0_PPC_R_ADDR44

Region Address

Address: 0x420250B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277186640

9.1.52 PPC0_PPC_R_ADDR45

Region Address

Address: 0x420250B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277186656

9.1.53 PPC0_PPC_R_ADDR46

Region Address

Address: 0x420250B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277186672

9.1.54 PPC0_PPC_R_ADDR47

Region Address

Address: 0x420250BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277192704

9.1.55 PPC0_PPC_R_ADDR48

Region Address

Address: 0x420250C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277217280

9.1.56 PPC0_PPC_R_ADDR49

Region Address

Address: 0x420250C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277233664

9.1.57 PPC0_PPC_R_ADDR50

Region Address

Address: 0x420250C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277217344

9.1.58 PPC0_PPC_R_ADDR51

Region Address

Address: 0x420250CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277233728

9.1.59 PPC0_PPC_R_ADDR52

Region Address

Address: 0x420250D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277225472

9.1.60 PPC0_PPC_R_ADDR53

Region Address

Address: 0x420250D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277225488

9.1.61 PPC0_PPC_R_ADDR54

Region Address

Address: 0x420250D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277225504

9.1.62 PPC0_PPC_R_ADDR55

Region Address

Address: 0x420250DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277225520

9.1.63 PPC0_PPC_R_ADDR56

Region Address

Address: 0x420250E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277225536

9.1.64 PPC0_PPC_R_ADDR57

Region Address

Address: 0x420250E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277225552

9.1.65 PPC0_PPC_R_ADDR58

Region Address

Address: 0x420250E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277225568

9.1.66 PPC0_PPC_R_ADDR59

Region Address

Address: 0x420250EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277225584

9.1.67 PPC0_PPC_R_ADDR60

Region Address

Address: 0x420250F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277225600

9.1.68 PPC0_PPC_R_ADDR61

Region Address

Address: 0x420250F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277225616

9.1.69 PPC0_PPC_R_ADDR62

Region Address

Address: 0x420250F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277225632

9.1.70 PPC0_PPC_R_ADDR63

Region Address

Address: 0x420250FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277225648

9.1.71 PPC0_PPC_R_ADDR64

Region Address

Address: 0x42025100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277225664

9.1.72 PPC0_PPC_R_ADDR65

Region Address

Address: 0x42025104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277225680

9.1.73 PPC0_PPC_R_ADDR66

Region Address

Address: 0x42025108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277225696

9.1.74 PPC0_PPC_R_ADDR67

Region Address

Address: 0x4202510C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277225712

9.1.75 PPC0_PPC_R_ADDR68

Region Address

Address: 0x42025110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277241856

9.1.76 PPC0_PPC_R_ADDR69

Region Address

Address: 0x42025114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277241872

9.1.77 PPC0_PPC_R_ADDR70

Region Address

Address: 0x42025118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277241888

9.1.78 PPC0_PPC_R_ADDR71

Region Address

Address: 0x4202511C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277241904

9.1.79 PPC0_PPC_R_ADDR72

Region Address

Address: 0x42025120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277241920

9.1.80 PPC0_PPC_R_ADDR73

Region Address

Address: 0x42025124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277241936

9.1.81 PPC0_PPC_R_ADDR74

Region Address

Address: 0x42025128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277241952

9.1.82 PPC0_PPC_R_ADDR75

Region Address

Address: 0x4202512C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277241968

9.1.83 PPC0_PPC_R_ADDR76

Region Address

Address: 0x42025130

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277241984

9.1.84 PPC0_PPC_R_ADDR77

Region Address

Address: 0x42025134

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277242000

9.1.85 PPC0_PPC_R_ADDR78

Region Address

Address: 0x42025138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277242016

9.1.86 PPC0_PPC_R_ADDR79

Region Address

Address: 0x4202513C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277242032

9.1.87 PPC0_PPC_R_ADDR80

Region Address

Address: 0x42025140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277242048

9.1.88 PPC0_PPC_R_ADDR81

Region Address

Address: 0x42025144

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277242064

9.1.89 PPC0_PPC_R_ADDR82

Region Address

Address: 0x42025148

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277242080

9.1.90 PPC0_PPC_R_ADDR83

Region Address

Address: 0x4202514C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277242096

9.1.91 PPC0_PPC_R_ADDR84

Region Address

Address: 0x42025150

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277282816

9.1.92 PPC0_PPC_R_ADDR85

Region Address

Address: 0x42025154

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277282848

9.1.93 PPC0_PPC_R_ADDR86

Region Address

Address: 0x42025158

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277282880

9.1.94 PPC0_PPC_R_ADDR87

Region Address

Address: 0x4202515C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277282888

9.1.95 PPC0_PPC_R_ADDR88

Region Address

Address: 0x42025160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277282944

9.1.96 PPC0_PPC_R_ADDR89

Region Address

Address: 0x42025164

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277283840

9.1.97 PPC0_PPC_R_ADDR90

Region Address

Address: 0x42025168

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277284864

9.1.98 PPC0_PPC_R_ADDR91

Region Address

Address: 0x4202516C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277286912

9.1.99 PPC0_PPC_R_ADDR92

Region Address

Address: 0x42025170

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277286928

9.1.100 PPC0_PPC_R_ADDR93

Region Address

Address: 0x42025174

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277286932

9.1.101 PPC0_PPC_R_ADDR94

Region Address

Address: 0x42025178

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277286940

9.1.102 PPC0_PPC_R_ADDR95

Region Address

Address: 0x4202517C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277287036

9.1.103 PPC0_PPC_R_ADDR96

Region Address

Address: 0x42025180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277287936

9.1.104 PPC0_PPC_R_ADDR97

Region Address

Address: 0x42025184

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277288060

9.1.105 PPC0_PPC_R_ADDR98

Region Address

Address: 0x42025188

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277287937

9.1.106 PPC0_PPC_R_ADDR99

Region Address

Address: 0x4202518C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277288061

9.1.107 PPC0_PPC_R_ADDR100

Region Address

Address: 0x42025190

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277288960

9.1.108 PPC0_PPC_R_ADDR101

Region Address

Address: 0x42025194

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277291008

9.1.109 PPC0_PPC_R_ADDR102

Region Address

Address: 0x42025198

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277299200

9.1.110 PPC0_PPC_R_ADDR103

Region Address

Address: 0x4202519C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277299208

9.1.111 PPC0_PPC_R_ADDR104

Region Address

Address: 0x420251A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277299216

9.1.112 PPC0_PPC_R_ADDR105

Region Address

Address: 0x420251A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277299224

9.1.113 PPC0_PPC_R_ADDR106

Region Address

Address: 0x420251A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277300224

9.1.114 PPC0_PPC_R_ADDR107

Region Address

Address: 0x420251AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277300232

9.1.115 PPC0_PPC_R_ADDR108

Region Address

Address: 0x420251B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277315584

9.1.116 PPC0_PPC_R_ADDR109

Region Address

Address: 0x420251B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277348352

9.1.117 PPC0_PPC_R_ADDR110

Region Address

Address: 0x420251B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277348608

9.1.118 PPC0_PPC_R_ADDR111

Region Address

Address: 0x420251BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277348904

9.1.119 PPC0_PPC_R_ADDR112

Region Address

Address: 0x420251C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277349376

9.1.120 PPC0_PPC_R_ADDR113

Region Address

Address: 0x420251C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277350400

9.1.121 PPC0_PPC_R_ADDR114

Region Address

Address: 0x420251C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277352448

9.1.122 PPC0_PPC_R_ADDR115

Region Address

Address: 0x420251CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277352576

9.1.123 PPC0_PPC_R_ADDR116

Region Address

Address: 0x420251D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277360640

9.1.124 PPC0_PPC_R_ADDR117

Region Address

Address: 0x420251D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277361664

9.1.125 PPC0_PPC_R_ADDR118

Region Address

Address: 0x420251D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277364736

9.1.126 PPC0_PPC_R_ADDR119

Region Address

Address: 0x420251DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277381120

9.1.127 PPC0_PPC_R_ADDR120

Region Address

Address: 0x420251E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277382144

9.1.128 PPC0_PPC_R_ADDR121

Region Address

Address: 0x420251E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277382148

9.1.129 PPC0_PPC_R_ADDR122

Region Address

Address: 0x420251E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277382152

9.1.130 PPC0_PPC_R_ADDR123

Region Address

Address: 0x420251EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277382176

9.1.131 PPC0_PPC_R_ADDR124

Region Address

Address: 0x420251F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277397440

9.1.132 PPC0_PPC_R_ADDR125

Region Address

Address: 0x420251F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277397504

9.1.133 PPC0_PPC_R_ADDR126

Region Address

Address: 0x420251F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277397568

9.1.134 PPC0_PPC_R_ADDR127

Region Address

Address: 0x420251FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277413888

9.1.135 PPC0_PPC_R_ADDR128

Region Address

Address: 0x42025200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277430272

9.1.136 PPC0_PPC_R_ADDR129

Region Address

Address: 0x42025204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277872640

9.1.137 PPC0_PPC_R_ADDR130

Region Address

Address: 0x42025208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277872644

9.1.138 PPC0_PPC_R_ADDR131

Region Address

Address: 0x4202520C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277872648

9.1.139 PPC0_PPC_R_ADDR132

Region Address

Address: 0x42025210

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277872652

9.1.140 PPC0_PPC_R_ADDR133

Region Address

Address: 0x42025214

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277872656

9.1.141 PPC0_PPC_R_ADDR134

Region Address

Address: 0x42025218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277872660

9.1.142 PPC0_PPC_R_ADDR135

Region Address

Address: 0x4202521C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277872664

9.1.143 PPC0_PPC_R_ADDR136

Region Address

Address: 0x42025220

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277872668

9.1.144 PPC0_PPC_R_ADDR137

Region Address

Address: 0x42025224

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277872672

9.1.145 PPC0_PPC_R_ADDR138

Region Address

Address: 0x42025228

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277872676

9.1.146 PPC0_PPC_R_ADDR139

Region Address

Address: 0x4202522C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277873664

9.1.147 PPC0_PPC_R_ADDR140

Region Address

Address: 0x42025230

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277873668

9.1.148 PPC0_PPC_R_ADDR141

Region Address

Address: 0x42025234

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277873672

9.1.149 PPC0_PPC_R_ADDR142

Region Address

Address: 0x42025238

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277873676

9.1.150 PPC0_PPC_R_ADDR143

Region Address

Address: 0x4202523C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277873680

9.1.151 PPC0_PPC_R_ADDR144

Region Address

Address: 0x42025240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277873684

9.1.152 PPC0_PPC_R_ADDR145

Region Address

Address: 0x42025244

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277873688

9.1.153 PPC0_PPC_R_ADDR146

Region Address

Address: 0x42025248

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277873692

9.1.154 PPC0_PPC_R_ADDR147

Region Address

Address: 0x4202524C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277873696

9.1.155 PPC0_PPC_R_ADDR148

Region Address

Address: 0x42025250

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277873700

9.1.156 PPC0_PPC_R_ADDR149

Region Address

Address: 0x42025254

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277874688

9.1.157 PPC0_PPC_R_ADDR150

Region Address

Address: 0x42025258

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277874816

9.1.158 PPC0_PPC_R_ADDR151

Region Address

Address: 0x4202525C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277889024

9.1.159 PPC0_PPC_R_ADDR152

Region Address

Address: 0x42025260

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277889056

9.1.160 PPC0_PPC_R_ADDR153

Region Address

Address: 0x42025264

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277889088

9.1.161 PPC0_PPC_R_ADDR154

Region Address

Address: 0x42025268

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277889120

9.1.162 PPC0_PPC_R_ADDR155

Region Address

Address: 0x4202526C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277889152

9.1.163 PPC0_PPC_R_ADDR156

Region Address

Address: 0x42025270

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277889184

9.1.164 PPC0_PPC_R_ADDR157

Region Address

Address: 0x42025274

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277889216

9.1.165 PPC0_PPC_R_ADDR158

Region Address

Address: 0x42025278

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277889248

9.1.166 PPC0_PPC_R_ADDR159

Region Address

Address: 0x4202527C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277889280

9.1.167 PPC0_PPC_R_ADDR160

Region Address

Address: 0x42025280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277889312

9.1.168 PPC0_PPC_R_ADDR161

Region Address

Address: 0x42025284

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277889040

9.1.169 PPC0_PPC_R_ADDR162

Region Address

Address: 0x42025288

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277889072

9.1.170 PPC0_PPC_R_ADDR163

Region Address

Address: 0x4202528C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277889104

9.1.171 PPC0_PPC_R_ADDR164

Region Address

Address: 0x42025290

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277889136

9.1.172 PPC0_PPC_R_ADDR165

Region Address

Address: 0x42025294

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277889168

9.1.173 PPC0_PPC_R_ADDR166

Region Address

Address: 0x42025298

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277889200

9.1.174 PPC0_PPC_R_ADDR167

Region Address

Address: 0x4202529C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277889232

9.1.175 PPC0_PPC_R_ADDR168

Region Address

Address: 0x420252A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277889264

9.1.176 PPC0_PPC_R_ADDR169

Region Address

Address: 0x420252A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277889296

9.1.177 PPC0_PPC_R_ADDR170

Region Address

Address: 0x420252A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277889328

9.1.178 PPC0_PPC_R_ADDR171

Region Address

Address: 0x420252AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277896192

9.1.179 PPC0_PPC_R_ADDR172

Region Address

Address: 0x420252B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277897216

9.1.180 PPC0_PPC_R_ADDR173

Region Address

Address: 0x420252B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277898240

9.1.181 PPC0_PPC_R_ADDR174

Region Address

Address: 0x420252B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277905408

9.1.182 PPC0_PPC_R_ADDR175

Region Address

Address: 0x420252BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277905472

9.1.183 PPC0_PPC_R_ADDR176

Region Address

Address: 0x420252C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277905536

9.1.184 PPC0_PPC_R_ADDR177

Region Address

Address: 0x420252C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277905600

9.1.185 PPC0_PPC_R_ADDR178

Region Address

Address: 0x420252C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277905728

9.1.186 PPC0_PPC_R_ADDR179

Region Address

Address: 0x420252CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277905792

9.1.187 PPC0_PPC_R_ADDR180

Region Address

Address: 0x420252D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277905984

9.1.188 PPC0_PPC_R_ADDR181

Region Address

Address: 0x420252D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 277921792

9.1.189 PPC0_PPC_R_ADDR182

Region Address

Address: 0x420252D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 278396928

9.1.190 PPC0_PPC_R_ADDR183

Region Address

Address: 0x420252DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 278413312

9.1.191 PPC0_PPC_R_ADDR184

Region Address

Address: 0x420252E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 278413376

9.1.192 PPC0_PPC_R_ADDR185

Region Address

Address: 0x420252E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 278413408

9.1.193 PPC0_PPC_R_ADDR186

Region Address

Address: 0x420252E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 278413824

9.1.194 PPC0_PPC_R_ADDR187

Region Address

Address: 0x420252EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 278921216

9.1.195 PPC0_PPC_R_ADDR188

Region Address

Address: 0x420252F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 278921344

9.1.196 PPC0_PPC_R_ADDR189

Region Address

Address: 0x420252F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 278922240

9.1.197 PPC0_PPC_R_ADDR190

Region Address

Address: 0x420252F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 278937600

9.1.198 PPC0_PPC_R_ADDR191

Region Address

Address: 0x420252FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 278953984

9.1.199 PPC0_PPC_R_ADDR192

Region Address

Address: 0x42025300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 278986752

9.1.200 PPC0_PPC_R_ADDR193

Region Address

Address: 0x42025304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 279003136

9.1.201 PPC0_PPC_R_ADDR194

Region Address

Address: 0x42025308

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 279019520

9.1.202 PPC0_PPC_R_ADDR195

Region Address

Address: 0x4202530C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 279035904

9.1.203 PPC0_PPC_R_ADDR196

Region Address

Address: 0x42025310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 279969792

9.1.204 PPC0_PPC_R_ADDR197

Region Address

Address: 0x42025314

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 279445504

9.1.205 PPC0_PPC_R_ADDR198

Region Address

Address: 0x42025318

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 279445568

9.1.206 PPC0_PPC_R_ADDR199

Region Address

Address: 0x4202531C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 279445632

9.1.207 PPC0_PPC_R_ADDR200

Region Address

Address: 0x42025320

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 279445696

9.1.208 PPC0_PPC_R_ADDR201

Region Address

Address: 0x42025324

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 279461888

9.1.209 PPC0_PPC_R_ADDR202

Region Address

Address: 0x42025328

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 279461952

9.1.210 PPC0_PPC_R_ADDR203

Region Address

Address: 0x4202532C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 279462016

9.1.211 PPC0_PPC_R_ADDR204

Region Address

Address: 0x42025330

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 279462080

9.1.212 PPC0_PPC_R_ADDR205

Region Address

Address: 0x42025334

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 279462144

9.1.213 PPC0_PPC_R_ADDR206

Region Address

Address: 0x42025338

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 279462208

9.1.214 PPC0_PPC_R_ADDR207

Region Address

Address: 0x4202533C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 279462272

9.1.215 PPC0_PPC_R_ADDR208

Region Address

Address: 0x42025340

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 279462336

9.1.216 PPC0_PPC_R_ADDR209

Region Address

Address: 0x42025344

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 279478272

9.1.217 PPC0_PPC_R_ADDR210

Region Address

Address: 0x42025348

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 279478336

9.1.218 PPC0_PPC_R_ADDR211

Region Address

Address: 0x4202534C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 279478400

9.1.219 PPC0_PPC_R_ADDR212

Region Address

Address: 0x42025350

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 279478464

9.1.220 PPC0_PPC_R_ADDR213

Region Address

Address: 0x42025354

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 279478528

9.1.221 PPC0_PPC_R_ADDR214

Region Address

Address: 0x42025358

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 279478592

9.1.222 PPC0_PPC_R_ADDR215

Region Address

Address: 0x4202535C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 279478656

9.1.223 PPC0_PPC_R_ADDR216

Region Address

Address: 0x42025360

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 279478720

9.1.224 PPC0_PPC_R_ADDR217

Region Address

Address: 0x42025364

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 279576576

9.1.225 PPC0_PPC_R_ADDR218

Region Address

Address: 0x42025368

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 279592960

9.1.226 PPC0_PPC_R_ADDR219

Region Address

Address: 0x4202536C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 279593472

9.1.227 PPC0_PPC_R_ADDR220

Region Address

Address: 0x42025370

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 279613440

9.1.228 PPC0_PPC_R_ADDR221

Region Address

Address: 0x42025374

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	R_ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	R_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	R_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	R_ADDR [31:24]							

Bits	Name	Description
31 : 2	R_ADDR	This field specifies the base address of the peripheral region. The region size is defined by R_ATTR.R_SIZE. A region of n Bytes mus be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR must be '0's. E.g., a 64KB address region (R_SIZE is "15") must be 64 KByte aligned, and R_ADDR[13:0] must be '0's. Default Value: 279707648

9.1.229 PPC0_PPC_R_ATT0

Region Attribute

Address: 0x42026000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None			R				
HW Access	None			W				
Name	None [31:29]			R_SIZE [28:24]				

Bits	Name	Description

9.1.229 PPC0_PPC_R_ATT0 (continued)

28 : 24	R_SIZE	This field specifies the size of the peripheral region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 13

9.1.230 PPC0_PPC_R_ATT1

Region Attribute

Address: 0x42026004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None			R				
HW Access	None			W				
Name	None [31:29]			R_SIZE [28:24]				

Bits	Name	Description

9.1.230 PPC0_PPC_R_ATT1 (continued)

28 : 24	R_SIZE	This field specifies the size of the peripheral region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 2

9.1.231 PPC0_PPC_R_ATT2

Region Attribute

Address: 0x42026008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None			R				
HW Access	None			W				
Name	None [31:29]			R_SIZE [28:24]				

Bits	Name	Description

9.1.231 PPC0_PPC_R_ATT2 (continued)

28 : 24	R_SIZE	This field specifies the size of the peripheral region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 4

9.1.232 PPC0_PPC_R_ATT7

Region Attribute

Address: 0x4202601C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None			R				
HW Access	None			W				
Name	None [31:29]			R_SIZE [28:24]				

Bits	Name	Description

9.1.232 PPC0_PPC_R_ATT7 (continued)

28 : 24	R_SIZE	This field specifies the size of the peripheral region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 1

9.1.233 PPC0_PPC_R_ATT13

Region Attribute

Address: 0x42026034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None			R				
HW Access	None			W				
Name	None [31:29]			R_SIZE [28:24]				

Bits	Name	Description

9.1.233 PPC0_PPC_R_ATT13 (continued)

28 : 24	R_SIZE	This field specifies the size of the peripheral region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 14

9.1.234 PPC0_PPC_R_ATT16

Region Attribute

Address: 0x42026040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None			R				
HW Access	None			W				
Name	None [31:29]			R_SIZE [28:24]				

Bits	Name	Description

9.1.234 PPC0_PPC_R_ATT16 (continued)

28 : 24	R_SIZE	This field specifies the size of the peripheral region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 15

9.1.235 PPC0_PPC_R_ATT18

Region Attribute

Address: 0x42026048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None			R				
HW Access	None			W				
Name	None [31:29]			R_SIZE [28:24]				

Bits	Name	Description

9.1.235 PPC0_PPC_R_ATT18 (continued)

28 : 24	R_SIZE	This field specifies the size of the peripheral region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 5

9.1.236 PPC0_PPC_R_ATT20

Region Attribute

Address: 0x42026050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None			R				
HW Access	None			W				
Name	None [31:29]			R_SIZE [28:24]				

Bits	Name	Description

9.1.236 PPC0_PPC_R_ATT20 (continued)

28 : 24	R_SIZE	This field specifies the size of the peripheral region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 7

9.1.237 PPC0_PPC_R_ATT30

Region Attribute

Address: 0x42026078

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None			R				
HW Access	None			W				
Name	None [31:29]			R_SIZE [28:24]				

Bits	Name	Description

9.1.237 PPC0_PPC_R_ATT30 (continued)

28 : 24	R_SIZE	This field specifies the size of the peripheral region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 3

9.1.238 PPC0_PPC_R_ATT31

Region Attribute

Address: 0x4202607C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None			R				
HW Access	None			W				
Name	None [31:29]			R_SIZE [28:24]				

Bits	Name	Description

9.1.238 PPC0_PPC_R_ATT31 (continued)

28 : 24	R_SIZE	This field specifies the size of the peripheral region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 6

9.1.239 PPC0_PPC_R_ATT38

Region Attribute

Address: 0x42026098

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None			R				
HW Access	None			W				
Name	None [31:29]			R_SIZE [28:24]				

Bits	Name	Description

9.1.239 PPC0_PPC_R_ATT38 (continued)

28 : 24	R_SIZE	This field specifies the size of the peripheral region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 10

9.1.240 PPC0_PPC_R_ATT47

Region Attribute

Address: 0x420260BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None			R				
HW Access	None			W				
Name	None [31:29]			R_SIZE [28:24]				

Bits	Name	Description

9.1.240 PPC0_PPC_R_ATT47 (continued)

28 : 24	R_SIZE	This field specifies the size of the peripheral region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 9

9.1.241 PPC0_PPC_R_ATT112

Region Attribute

Address: 0x420261C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None			R				
HW Access	None			W				
Name	None [31:29]			R_SIZE [28:24]				

Bits	Name	Description

9.1.241 PPC0_PPC_R_ATT112 (continued)

28 : 24	R_SIZE	This field specifies the size of the peripheral region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 11

9.1.242 PPC0_PPC_R_ATT113

Region Attribute

Address: 0x420261C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None			R				
HW Access	None			W				
Name	None [31:29]			R_SIZE [28:24]				

Bits	Name	Description

9.1.242 PPC0_PPC_R_ATT113 (continued)

28 : 24	R_SIZE	This field specifies the size of the peripheral region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 12

9.1.243 PPC0_PPC_R_ATT187

Region Attribute

Address: 0x420262EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None			R				
HW Access	None			W				
Name	None [31:29]			R_SIZE [28:24]				

Bits	Name	Description

9.1.243 PPC0_PPC_R_ATT187 (continued)

28 : 24	R_SIZE	This field specifies the size of the peripheral region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 8

9.1.244 PPC0_PPC_R_ATT221

Region Attribute

Address: 0x42026374

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None			R				
HW Access	None			W				
Name	None [31:29]			R_SIZE [28:24]				

Bits	Name	Description

9.1.244 PPC0_PPC_R_ATT221 (continued)

28 : 24	R_SIZE	This field specifies the size of the peripheral region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 19

10 Peripheral registers

This section discusses the Peripheral registers. It lists all the registers in mapping tables, in address order.

10.1 Register details

Register	Address	Description
PERI0_TIMEOUT_CTL	0x42000200	Timeout control
PERI0_TR_CMD	0x42002000	Trigger command
PERI0_INFRA_CLK_FORCE	0x42002004	Infrastructure clock force enable
PERI0_GR0_SL_CTL	0x42004010	Slave control
PERI0_GR0_SL_CTL2	0x42004014	Slave control2
PERI0_GR1_CLOCK_CTL	0x42004040	Clock control
PERI0_GR1_SL_CTL	0x42004050	Slave control
PERI0_GR1_SL_CTL2	0x42004054	Slave control2
PERI0_GR2_CLOCK_CTL	0x42004080	Clock control. See PERI0_GR1_CLOCK_CTL for the details of bit fields.
PERI0_GR2_SL_CTL	0x42004090	Slave control
PERI0_GR2_SL_CTL2	0x42004094	Slave control2
PERI0_GR3_CLOCK_CTL	0x420040C0	Clock control. See PERI0_GR1_CLOCK_CTL for the details of bit fields.
PERI0_GR3_SL_CTL	0x420040D0	Slave control
PERI0_GR3_SL_CTL2	0x420040D4	Slave control2
PERI0_GR4_CLOCK_CTL	0x42004100	Clock control. See PERI0_GR1_CLOCK_CTL for the details of bit fields.
PERI0_GR4_SL_CTL	0x42004110	Slave control. See PERI0_GR2_SL_CTL for the details of bit fields.
PERI0_GR4_SL_CTL2	0x42004114	Slave control2. See PERI0_GR2_SL_CTL2 for the details of bit fields.
PERI0_GR5_SL_CTL	0x42004150	Slave control
PERI0_GR5_SL_CTL2	0x42004154	Slave control2
PERI0_TR_GR0_TR_CTL0	0x42008000	Trigger control register
PERI0_TR_GR0_TR_CTL1	0x42008004	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR0_TR_CTL2	0x42008008	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR0_TR_CTL3	0x4200800C	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR0_TR_CTL4	0x42008010	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR0_TR_CTL5	0x42008014	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.

Peripheral registers

Register	Address	Description
PERI0_TR_GR0_TR_CTL6	0x42008018	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR0_TR_CTL7	0x4200801C	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR0_TR_CTL8	0x42008020	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR0_TR_CTL9	0x42008024	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR0_TR_CTL10	0x42008028	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR0_TR_CTL11	0x4200802C	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR0_TR_CTL12	0x42008030	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR0_TR_CTL13	0x42008034	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR0_TR_CTL14	0x42008038	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR0_TR_CTL15	0x4200803C	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR1_TR_CTL0	0x42008400	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR1_TR_CTL1	0x42008404	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR1_TR_CTL2	0x42008408	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR1_TR_CTL3	0x4200840C	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR1_TR_CTL4	0x42008410	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR1_TR_CTL5	0x42008414	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR1_TR_CTL6	0x42008418	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR1_TR_CTL7	0x4200841C	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR1_TR_CTL8	0x42008420	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR1_TR_CTL9	0x42008424	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR1_TR_CTL10	0x42008428	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.

Peripheral registers

Register	Address	Description
PERI0_TR_GR1_TR_CTL11	0x4200842C	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR1_TR_CTL12	0x42008430	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR1_TR_CTL13	0x42008434	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR1_TR_CTL14	0x42008438	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR1_TR_CTL15	0x4200843C	Trigger control register. See PERI0_TR_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_GR2_TR_CTL0	0x42008800	Trigger control register. This is the starting address of a register bank containing 50 registers (PERI0_TR_GR2_TR_CTL0 to PERI0_TR_GR2_TR_CTL49).
PERI0_TR_GR3_TR_CTL0	0x42008C00	Trigger control register
PERI0_TR_GR3_TR_CTL1	0x42008C04	Trigger control register. See PERI0_TR_GR3_TR_CTL0 for the details of bit fields.
PERI0_TR_GR3_TR_CTL2	0x42008C08	Trigger control register. See PERI0_TR_GR3_TR_CTL0 for the details of bit fields.
PERI0_TR_GR3_TR_CTL3	0x42008C0C	Trigger control register. See PERI0_TR_GR3_TR_CTL0 for the details of bit fields.
PERI0_TR_GR3_TR_CTL4	0x42008C10	Trigger control register. See PERI0_TR_GR3_TR_CTL0 for the details of bit fields.
PERI0_TR_GR3_TR_CTL5	0x42008C14	Trigger control register. See PERI0_TR_GR3_TR_CTL0 for the details of bit fields.
PERI0_TR_GR3_TR_CTL6	0x42008C18	Trigger control register. See PERI0_TR_GR3_TR_CTL0 for the details of bit fields.
PERI0_TR_GR3_TR_CTL7	0x42008C1C	Trigger control register. See PERI0_TR_GR3_TR_CTL0 for the details of bit fields.
PERI0_TR_GR4_TR_CTL0	0x42009000	Trigger control register. See PERI0_TR_GR3_TR_CTL0 for the details of bit fields.
PERI0_TR_GR4_TR_CTL1	0x42009004	Trigger control register. See PERI0_TR_GR3_TR_CTL0 for the details of bit fields.
PERI0_TR_GR4_TR_CTL2	0x42009008	Trigger control register. See PERI0_TR_GR3_TR_CTL0 for the details of bit fields.
PERI0_TR_GR4_TR_CTL3	0x4200900C	Trigger control register. See PERI0_TR_GR3_TR_CTL0 for the details of bit fields.
PERI0_TR_GR4_TR_CTL4	0x42009010	Trigger control register. See PERI0_TR_GR3_TR_CTL0 for the details of bit fields.
PERI0_TR_GR4_TR_CTL5	0x42009014	Trigger control register. See PERI0_TR_GR3_TR_CTL0 for the details of bit fields.
PERI0_TR_GR4_TR_CTL6	0x42009018	Trigger control register. See PERI0_TR_GR3_TR_CTL0 for the details of bit fields.

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Register	Address	Description
PERI0_TR_GR4_TR_CTL7	0x4200901C	Trigger control register. See PERI0_TR_GR3_TR_CTL0 for the details of bit fields.
PERI0_TR_GR5_TR_CTL0	0x42009400	Trigger control register. See PERI0_TR_GR3_TR_CTL0 for the details of bit fields.
PERI0_TR_GR5_TR_CTL1	0x42009404	Trigger control register. See PERI0_TR_GR3_TR_CTL0 for the details of bit fields.
PERI0_TR_GR5_TR_CTL2	0x42009408	Trigger control register. See PERI0_TR_GR3_TR_CTL0 for the details of bit fields.
PERI0_TR_GR5_TR_CTL3	0x4200940C	Trigger control register. See PERI0_TR_GR3_TR_CTL0 for the details of bit fields.
PERI0_TR_GR5_TR_CTL4	0x42009410	Trigger control register. See PERI0_TR_GR3_TR_CTL0 for the details of bit fields.
PERI0_TR_GR5_TR_CTL5	0x42009414	Trigger control register. See PERI0_TR_GR3_TR_CTL0 for the details of bit fields.
PERI0_TR_GR5_TR_CTL6	0x42009418	Trigger control register. See PERI0_TR_GR3_TR_CTL0 for the details of bit fields.
PERI0_TR_GR5_TR_CTL7	0x4200941C	Trigger control register. See PERI0_TR_GR3_TR_CTL0 for the details of bit fields.
PERI0_TR_GR6_TR_CTL0	0x42009800	Trigger control register
PERI0_TR_GR6_TR_CTL1	0x42009804	Trigger control register. See PERI0_TR_GR6_TR_CTL0 for the details of bit fields.
PERI0_TR_GR7_TR_CTL0	0x42009C00	Trigger control register
PERI0_TR_GR7_TR_CTL1	0x42009C04	Trigger control register. See PERI0_TR_GR7_TR_CTL0 for the details of bit fields.
PERI0_TR_GR8_TR_CTL0	0x4200A000	Trigger control register. See PERI0_TR_GR7_TR_CTL0 for the details of bit fields.
PERI0_TR_GR8_TR_CTL1	0x4200A004	Trigger control register. See PERI0_TR_GR7_TR_CTL0 for the details of bit fields.
PERI0_TR_GR9_TR_CTL0	0x4200A400	Trigger control register
PERI0_TR_GR9_TR_CTL1	0x4200A404	Trigger control register. See PERI0_TR_GR9_TR_CTL0 for the details of bit fields.
PERI0_TR_GR9_TR_CTL2	0x4200A408	Trigger control register. See PERI0_TR_GR9_TR_CTL0 for the details of bit fields.
PERI0_TR_GR9_TR_CTL3	0x4200A40C	Trigger control register. See PERI0_TR_GR9_TR_CTL0 for the details of bit fields.
PERI0_TR_GR10_TR_CTL0	0x4200A800	Trigger control register
PERI0_TR_GR10_TR_CTL1	0x4200A804	Trigger control register. See PERI0_TR_GR10_TR_CTL0 for the details of bit fields.
PERI0_TR_GR10_TR_CTL2	0x4200A808	Trigger control register. See PERI0_TR_GR10_TR_CTL0 for the details of bit fields.
PERI0_TR_GR10_TR_CTL3	0x4200A80C	Trigger control register. See PERI0_TR_GR10_TR_CTL0 for the details of bit fields.

Peripheral registers

Register	Address	Description
PERI0_TR_GR10_TR_CTL4	0x4200A810	Trigger control register. See PERI0_TR_GR10_TR_CTL0 for the details of bit fields.
PERI0_TR_GR10_TR_CTL5	0x4200A814	Trigger control register. See PERI0_TR_GR10_TR_CTL0 for the details of bit fields.
PERI0_TR_GR10_TR_CTL6	0x4200A818	Trigger control register. See PERI0_TR_GR10_TR_CTL0 for the details of bit fields.
PERI0_TR_GR10_TR_CTL7	0x4200A81C	Trigger control register. See PERI0_TR_GR10_TR_CTL0 for the details of bit fields.
PERI0_TR_GR10_TR_CTL8	0x4200A820	Trigger control register. See PERI0_TR_GR10_TR_CTL0 for the details of bit fields.
PERI0_TR_GR10_TR_CTL9	0x4200A824	Trigger control register. See PERI0_TR_GR10_TR_CTL0 for the details of bit fields.
PERI0_TR_GR10_TR_CTL10	0x4200A828	Trigger control register. See PERI0_TR_GR10_TR_CTL0 for the details of bit fields.
PERI0_TR_GR10_TR_CTL11	0x4200A82C	Trigger control register. See PERI0_TR_GR10_TR_CTL0 for the details of bit fields.
PERI0_TR_GR11_TR_CTL0	0x4200AC00	Trigger control register
PERI0_TR_GR11_TR_CTL1	0x4200AC04	Trigger control register. See PERI0_TR_GR11_TR_CTL0 for the details of bit fields.
PERI0_TR_GR11_TR_CTL2	0x4200AC08	Trigger control register. See PERI0_TR_GR11_TR_CTL0 for the details of bit fields.
PERI0_TR_GR11_TR_CTL3	0x4200AC0C	Trigger control register. See PERI0_TR_GR11_TR_CTL0 for the details of bit fields.
PERI0_TR_GR11_TR_CTL4	0x4200AC10	Trigger control register. See PERI0_TR_GR11_TR_CTL0 for the details of bit fields.
PERI0_TR_GR11_TR_CTL5	0x4200AC14	Trigger control register. See PERI0_TR_GR11_TR_CTL0 for the details of bit fields.
PERI0_TR_GR11_TR_CTL6	0x4200AC18	Trigger control register. See PERI0_TR_GR11_TR_CTL0 for the details of bit fields.
PERI0_TR_GR11_TR_CTL7	0x4200AC1C	Trigger control register. See PERI0_TR_GR11_TR_CTL0 for the details of bit fields.
PERI0_TR_GR11_TR_CTL8	0x4200AC20	Trigger control register. See PERI0_TR_GR11_TR_CTL0 for the details of bit fields.
PERI0_TR_GR11_TR_CTL9	0x4200AC24	Trigger control register. See PERI0_TR_GR11_TR_CTL0 for the details of bit fields.
PERI0_TR_GR11_TR_CTL10	0x4200AC28	Trigger control register. See PERI0_TR_GR11_TR_CTL0 for the details of bit fields.
PERI0_TR_GR11_TR_CTL11	0x4200AC2C	Trigger control register. See PERI0_TR_GR11_TR_CTL0 for the details of bit fields.
PERI0_TR_GR11_TR_CTL12	0x4200AC30	Trigger control register. See PERI0_TR_GR11_TR_CTL0 for the details of bit fields.
PERI0_TR_GR11_TR_CTL13	0x4200AC34	Trigger control register. See PERI0_TR_GR11_TR_CTL0 for the details of bit fields.

Peripheral registers

Register	Address	Description
PERI0_TR_GR11_TR_CTL14	0x4200AC38	Trigger control register. See PERI0_TR_GR11_TR_CTL0 for the details of bit fields.
PERI0_TR_GR11_TR_CTL15	0x4200AC3C	Trigger control register. See PERI0_TR_GR11_TR_CTL0 for the details of bit fields.
PERI0_TR_GR11_TR_CTL16	0x4200AC40	Trigger control register. See PERI0_TR_GR11_TR_CTL0 for the details of bit fields.
PERI0_TR_GR11_TR_CTL17	0x4200AC44	Trigger control register. See PERI0_TR_GR11_TR_CTL0 for the details of bit fields.
PERI0_TR_GR11_TR_CTL18	0x4200AC48	Trigger control register. See PERI0_TR_GR11_TR_CTL0 for the details of bit fields.
PERI0_TR_GR11_TR_CTL19	0x4200AC4C	Trigger control register. See PERI0_TR_GR11_TR_CTL0 for the details of bit fields.
PERI0_TR_GR12_TR_CTL0	0x4200B000	Trigger control register
PERI0_TR_GR12_TR_CTL1	0x4200B004	Trigger control register. See PERI0_TR_GR12_TR_CTL0 for the details of bit fields.
PERI0_TR_GR12_TR_CTL2	0x4200B008	Trigger control register. See PERI0_TR_GR12_TR_CTL0 for the details of bit fields.
PERI0_TR_GR12_TR_CTL3	0x4200B00C	Trigger control register. See PERI0_TR_GR12_TR_CTL0 for the details of bit fields.
PERI0_TR_GR12_TR_CTL4	0x4200B010	Trigger control register. See PERI0_TR_GR12_TR_CTL0 for the details of bit fields.
PERI0_TR_GR12_TR_CTL5	0x4200B014	Trigger control register. See PERI0_TR_GR12_TR_CTL0 for the details of bit fields.
PERI0_TR_GR12_TR_CTL6	0x4200B018	Trigger control register. See PERI0_TR_GR12_TR_CTL0 for the details of bit fields.
PERI0_TR_GR12_TR_CTL7	0x4200B01C	Trigger control register. See PERI0_TR_GR12_TR_CTL0 for the details of bit fields.
PERI0_TR_GR12_TR_CTL8	0x4200B020	Trigger control register. See PERI0_TR_GR12_TR_CTL0 for the details of bit fields.
PERI0_TR_GR12_TR_CTL9	0x4200B024	Trigger control register. See PERI0_TR_GR12_TR_CTL0 for the details of bit fields.
PERI0_TR_GR12_TR_CTL10	0x4200B028	Trigger control register. See PERI0_TR_GR12_TR_CTL0 for the details of bit fields.
PERI0_TR_GR12_TR_CTL11	0x4200B02C	Trigger control register. See PERI0_TR_GR12_TR_CTL0 for the details of bit fields.
PERI0_TR_GR12_TR_CTL12	0x4200B030	Trigger control register. See PERI0_TR_GR12_TR_CTL0 for the details of bit fields.
PERI0_TR_GR12_TR_CTL13	0x4200B034	Trigger control register. See PERI0_TR_GR12_TR_CTL0 for the details of bit fields.
PERI0_TR_GR12_TR_CTL14	0x4200B038	Trigger control register. See PERI0_TR_GR12_TR_CTL0 for the details of bit fields.
PERI0_TR_GR12_TR_CTL15	0x4200B03C	Trigger control register. See PERI0_TR_GR12_TR_CTL0 for the details of bit fields.

Peripheral registers

Register	Address	Description
PERI0_TR_GR12_TR_CTL16	0x4200B040	Trigger control register. See PERI0_TR_GR12_TR_CTL0 for the details of bit fields.
PERI0_TR_GR12_TR_CTL17	0x4200B044	Trigger control register. See PERI0_TR_GR12_TR_CTL0 for the details of bit fields.
PERI0_TR_GR12_TR_CTL18	0x4200B048	Trigger control register. See PERI0_TR_GR12_TR_CTL0 for the details of bit fields.
PERI0_TR_GR12_TR_CTL19	0x4200B04C	Trigger control register. See PERI0_TR_GR12_TR_CTL0 for the details of bit fields.
PERI0_TR_GR13_TR_CTL0	0x4200B400	Trigger control register
PERI0_TR_GR13_TR_CTL1	0x4200B404	Trigger control register. See PERI0_TR_GR13_TR_CTL0 for the details of bit fields.
PERI0_TR_GR13_TR_CTL2	0x4200B408	Trigger control register. See PERI0_TR_GR13_TR_CTL0 for the details of bit fields.
PERI0_TR_GR13_TR_CTL3	0x4200B40C	Trigger control register. See PERI0_TR_GR13_TR_CTL0 for the details of bit fields.
PERI0_TR_GR13_TR_CTL4	0x4200B410	Trigger control register. See PERI0_TR_GR13_TR_CTL0 for the details of bit fields.
PERI0_TR_GR13_TR_CTL5	0x4200B414	Trigger control register. See PERI0_TR_GR13_TR_CTL0 for the details of bit fields.
PERI0_TR_GR13_TR_CTL6	0x4200B418	Trigger control register. See PERI0_TR_GR13_TR_CTL0 for the details of bit fields.
PERI0_TR_GR13_TR_CTL7	0x4200B41C	Trigger control register. See PERI0_TR_GR13_TR_CTL0 for the details of bit fields.
PERI0_TR_GR14_TR_CTL0	0x4200B800	Trigger control register. See PERI0_TR_GR13_TR_CTL0 for the details of bit fields.
PERI0_TR_GR14_TR_CTL1	0x4200B804	Trigger control register. See PERI0_TR_GR13_TR_CTL0 for the details of bit fields.
PERI0_TR_GR14_TR_CTL2	0x4200B808	Trigger control register. See PERI0_TR_GR13_TR_CTL0 for the details of bit fields.
PERI0_TR_GR14_TR_CTL3	0x4200B80C	Trigger control register. See PERI0_TR_GR13_TR_CTL0 for the details of bit fields.
PERI0_TR_GR14_TR_CTL4	0x4200B810	Trigger control register. See PERI0_TR_GR13_TR_CTL0 for the details of bit fields.
PERI0_TR_GR14_TR_CTL5	0x4200B814	Trigger control register. See PERI0_TR_GR13_TR_CTL0 for the details of bit fields.
PERI0_TR_GR14_TR_CTL6	0x4200B818	Trigger control register. See PERI0_TR_GR13_TR_CTL0 for the details of bit fields.
PERI0_TR_GR14_TR_CTL7	0x4200B81C	Trigger control register. See PERI0_TR_GR13_TR_CTL0 for the details of bit fields.
PERI0_TR_1TO1_GR0_TR_CTL0	0x4200C000	Trigger control register
PERI0_TR_1TO1_GR0_TR_CTL1	0x4200C004	Trigger control register. See PERI0_TR_1TO1_GR0_TR_CTL0 for the details of bit fields.
PERI0_TR_1TO1_GR1_TR_CTL0	0x4200C400	Trigger control register

Peripheral registers

Register	Address	Description
PERI0_TR_1TO1_GR1_TR_CTL1	0x4200C404	Trigger control register. See PERI0_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI0_TR_1TO1_GR1_TR_CTL2	0x4200C408	Trigger control register. See PERI0_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI0_TR_1TO1_GR1_TR_CTL3	0x4200C40C	Trigger control register. See PERI0_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI0_TR_1TO1_GR1_TR_CTL4	0x4200C410	Trigger control register. See PERI0_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI0_TR_1TO1_GR1_TR_CTL5	0x4200C414	Trigger control register. See PERI0_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI0_TR_1TO1_GR1_TR_CTL6	0x4200C418	Trigger control register. See PERI0_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI0_TR_1TO1_GR1_TR_CTL7	0x4200C41C	Trigger control register. See PERI0_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI0_TR_1TO1_GR1_TR_CTL8	0x4200C420	Trigger control register. See PERI0_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI0_TR_1TO1_GR1_TR_CTL9	0x4200C424	Trigger control register. See PERI0_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI0_TR_1TO1_GR1_TR_CTL10	0x4200C428	Trigger control register. See PERI0_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI0_TR_1TO1_GR1_TR_CTL11	0x4200C42C	Trigger control register. See PERI0_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI0_TR_1TO1_GR1_TR_CTL12	0x4200C430	Trigger control register. See PERI0_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI0_TR_1TO1_GR1_TR_CTL13	0x4200C434	Trigger control register. See PERI0_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI0_TR_1TO1_GR1_TR_CTL14	0x4200C438	Trigger control register. See PERI0_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI0_TR_1TO1_GR1_TR_CTL15	0x4200C43C	Trigger control register. See PERI0_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI0_TR_1TO1_GR1_TR_CTL16	0x4200C440	Trigger control register. See PERI0_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI0_TR_1TO1_GR1_TR_CTL17	0x4200C444	Trigger control register. See PERI0_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI0_TR_1TO1_GR1_TR_CTL18	0x4200C448	Trigger control register. See PERI0_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI0_TR_1TO1_GR1_TR_CTL19	0x4200C44C	Trigger control register. See PERI0_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI0_TR_1TO1_GR2_TR_CTL0	0x4200C800	Trigger control register
PERI0_TR_1TO1_GR2_TR_CTL1	0x4200C804	Trigger control register. See PERI0_TR_1TO1_GR2_TR_CTL0 for the details of bit fields.
PERI0_TR_1TO1_GR2_TR_CTL2	0x4200C808	Trigger control register. See PERI0_TR_1TO1_GR2_TR_CTL0 for the details of bit fields.

Peripheral registers

Register	Address	Description
PERI0_TR_1TO1_GR2_TR_CTL3	0x4200C80C	Trigger control register. See PERI0_TR_1TO1_GR2_TR_CTL0 for the details of bit fields.
PERI0_TR_1TO1_GR2_TR_CTL4	0x4200C810	Trigger control register. See PERI0_TR_1TO1_GR2_TR_CTL0 for the details of bit fields.
PERI0_TR_1TO1_GR2_TR_CTL5	0x4200C814	Trigger control register. See PERI0_TR_1TO1_GR2_TR_CTL0 for the details of bit fields.
PERI0_TR_1TO1_GR2_TR_CTL6	0x4200C818	Trigger control register. See PERI0_TR_1TO1_GR2_TR_CTL0 for the details of bit fields.
PERI0_TR_1TO1_GR2_TR_CTL7	0x4200C81C	Trigger control register. See PERI0_TR_1TO1_GR2_TR_CTL0 for the details of bit fields.

10.1.1 PERI0_TIMEOUT_CTL

Timeout control

Address: 0x42000200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TIMEOUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TIMEOUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	HWRST_-DISABLE	None [30:24]						

Bits	Name	Description
31	HWRST_DISABLE	This field provides control for HW to reset the slave that is causing the timeout to occur. 1 - no HW reset during timeout. 0 - HW resets the corresponding slave during timeout. This ensures the AHB bus not to be hung after a timeout has occurred. HW asserts the reset along with fault request (peri_gp'i'_mmio_timeout_vio_req) and holds it until fault acknowledge (mmio_peri_gp'i'_timeout_vio_ack) is received from centralized fault infrastructure. Note, SW needs to take care of the implication when clearing this bit when a HW reset has occurred as clearing this bit will cause HW reset de-assert. Note that peripheral group-0 slaves are excluded from timeout (Refer Timeout section in mxs-peri.1 BROS for more details). Default Value: 0
15 : 0	TIMEOUT	This field specifies a number of peripheral group root undivided (clk_group_root[i]) clock cycles. If an AHB-Lite bus transfer takes more than the specified number of cycles (timeout detection), the bus transfer is terminated with an AHB5 bus error and a timeout status is set. "0x0000"-"0xfffe": Number of peripheral group clock cycles. "0xffff": This value is the default/reset value and specifies that no timeout detection is performed: a bus transfer will never be terminated, and a interrupt will never be generated. Note that TIMEOUT_CTL.TIMEOUT[15:0] in clk_pclk0_root (clk_hf0) is used directly in peripheral group clock domain clk_group_root[i], even if clk_group_root[i] is async to clk_pclk0_root. This is on the assumption that this register is programmed once by SW, remain constant. Following SW programming restrictions apply to TIMEOUT_CTL.TIMEOUT[15:0]. SW should make sure that no other AHB transactions are initiated through PERI before programming this register. SW should make sure that write to TIMEOUT_CTL.TIMEOUT[15:0] is completed by doing a readback. Note that peripheral group-0 slaves are excluded from timeout (Refer Timeout section in mxs-peri.1 BROS for more details). Default Value: 0xFFFF

10.1.2 PERI0_TR_CMD

Trigger command

Address: 0x42002000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TR_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			GROUP_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	None				
HW Access	RW1C	R	R	None				
Name	ACTIVATE	OUT_SEL	TR_EDGE	None [28:24]				

Bits	Name	Description
31	ACTIVATE	SW sets this field to '1' to activate (set to '1') a trigger as identified by TR_SEL, TR_EDGE and OUT_SEL. HW sets this field to '0' for edge sensitive triggers AFTER the selected trigger is activated for two clk_peri cycles. Note: when ACTIVATE is '1', SW should not modify the other register fields. SW MUST NOT set ACTIVATE bit to '1' while updating the other register bits simultaneously. At first the SW MUST update the other register bits as needed, and then set ACTIVATE to '1' with a new register write. Default Value: 0
30	OUT_SEL	Specifies whether trigger activation is for a specific input or output trigger of the trigger multiplexer. Activation of a specific input trigger, will result in activation of all output triggers that have the specific input trigger selected through their TR_CTL.TR_SEL field. Activation of a specific output trigger, will result in activation of the specified TR_SEL output trigger only. '0': TR_SEL selection and trigger activation is for an input trigger to the trigger multiplexer. '1': TR_SEL selection and trigger activation is for an output trigger from the trigger multiplexer. Note: this field is not used for trigger 1-to-1 groups. Default Value: 0
29	TR_EDGE	Specifies if the activated trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. The trigger reflects TR_CMD.ACTIVATE. '1': edge sensitive trigger. The trigger is activated for two clk_peri cycles. Default Value: 0
12 : 8	GROUP_SEL	Specifies the trigger group: "0"-"15": trigger multiplexer groups. "16"-"31": trigger 1-to-1 groups. Default Value: 0

10.1.2 PERI0_TR_CMD (continued)

7 : 0	TR_SEL	Specifies the activated trigger when ACTIVATE is '1'. If the specified trigger is not present, the trigger activation has no effect. Default Value: 0

10.1.3 PERI0_INFRA_CLK_FORCE

Infrastructure clock force enable

Address: 0x42002004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							ENABLED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	ENABLED	Infrastructure clock force enable. 0: Disabled 1: Enabled Default Value: 0

10.1.4 PERI0_GR0_SL_CTL

Slave control

Address: 0x42004010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ENABLED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						ENABLED [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	ENABLED	Slave Enable. Each bit indicates whether the respective slave is enabled. If the slave is disabled, its clock is gated off (constant "0"). Note: For peripheral group 0 slave 0,1, and 2 (the peripheral interconnect MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. The peripheral IP that drives the Q-Channel back to Clock Controllers need to ensure that it has clock (usually driven by Clk_hf1~N that is only available after CPU configures their roots in the SRSS) to provide back the Q-Channel handshake, if not the deadlock situation will procure. To avoid deadlock mentioned above, all IPs in all groups other than group-0 are disabled (SL_CTL.ENABLED is set to '0') by default after POR (cold boot) (i.e. PERI HW hardcodes local parameter SL_CTL_DEFAULT to 32'hFFFFFFFF for group-0 and to 32'h00000000 for other groups (group-1 to group-15)). Once CPU is up and running & Clk_hf1~N configured, CPU can enable them. The SL_CTL.ENABLED are retained during DEEPSLEEP to avoid enabling configuration after wakeup. Default Value: 1023

10.1.5 PERI0_GR0_SL_CTL2

Slave control2

Address: 0x42004014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RST [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						RST [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	RST	Slave reset. Each bit indicates whether the respective slave is enabled. If the slave is under reset, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 slave 0,1, and 2 (the peripheral interconnect MMIO registers), this field is a constant '0' (SW: R): the slave can NOT be in reset. Default Value: 0

10.1.6 PERI0_GR1_CLOCK_CTL

Clock control

Address: 0x42004040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT8_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	INT8_DIV	Specifies a group clock divider (from the peripheral clock "clk_peri" to the group clock "clk_group[1/2/3/4/5/...15]"). Integer division by (1+INT8_DIV). Allows for integer divisions in the range [1, 256]. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0

10.1.7 PERI0_GR1_SL_CTL

Slave control

Address: 0x42004050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				ENABLED [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	ENABLED	Slave Enable. Each bit indicates whether the respective slave is enabled. If the slave is disabled, its clock is gated off (constant "0"). Note: For peripheral group 0 slave 0,1, and 2 (the peripheral interconnect MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. The peripheral IP that drives the Q-Channel back to Clock Controllers need to ensure that it has clock (usually driven by Clk_hf1~N that is only available after CPU configures their roots in the SRSS) to provide back the Q-Channel handshake, if not the deadlock situation will procure. To avoid deadlock mentioned above, all IPs in all groups other than group-0 are disabled (SL_CTL.ENABLED is set to '0') by default after POR (cold boot) (i.e. PERI HW hardcodes local parameter SL_CTL_DEFAULT to 32'hFFFFFFFF for group-0 and to 32'h00000000 for other groups (group-1 to group-15)). Once CPU is up and running & Clk_hf1~N configured, CPU can enable them. The SL_CTL.ENABLED are retained during DEEPSLEEP to avoid enabling configuration after wakeup. Default Value: 0

10.1.8 PERI0_GR1_SL_CTL2

Slave control2

Address: 0x42004054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				RST [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	RST	Slave reset. Each bit indicates whether the respective slave is enabled. If the slave is under reset, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 slave 0,1, and 2 (the peripheral interconnect MMIO registers), this field is a constant '0' (SW: R): the slave can NOT be in reset. Default Value: 0

10.1.9 PERI0_GR2_SL_CTL

Slave control

Address: 0x42004090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						ENABLED [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	ENABLED	Slave Enable. Each bit indicates whether the respective slave is enabled. If the slave is disabled, its clock is gated off (constant "0"). Note: For peripheral group 0 slave 0,1, and 2 (the peripheral interconnect MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. The peripheral IP that drives the Q-Channel back to Clock Controllers need to ensure that it has clock (usually driven by Clk_hf1~N that is only available after CPU configures their roots in the SRSS) to provide back the Q-Channel handshake, if not the deadlock situation will procure. To avoid deadlock mentioned above, all IPs in all groups other than group-0 are disabled (SL_CTL.ENABLED is set to '0') by default after POR (cold boot) (i.e. PERI HW hardcodes local parameter SL_CTL_DEFAULT to 32'hFFFFFFFF for group-0 and to 32'h00000000 for other groups (group-1 to group-15)). Once CPU is up and running & Clk_hf1~N configured, CPU can enable them. The SL_CTL.ENABLED are retained during DEEPSLEEP to avoid enabling configuration after wakeup. Default Value: 0

10.1.10 PERI0_GR2_SL_CTL2

Slave control2

Address: 0x42004094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						RST [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	RST	Slave reset. Each bit indicates whether the respective slave is enabled. If the slave is under reset, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 slave 0,1, and 2 (the peripheral interconnect MMIO registers), this field is a constant '0' (SW: R): the slave can NOT be in reset. Default Value: 0

10.1.11 PERI0_GR3_SL_CTL

Slave control

Address: 0x420040D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		ENABLED [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	ENABLED	Slave Enable. Each bit indicates whether the respective slave is enabled. If the slave is disabled, its clock is gated off (constant "0"). Note: For peripheral group 0 slave 0,1, and 2 (the peripheral interconnect MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. The peripheral IP that drives the Q-Channel back to Clock Controllers need to ensure that it has clock (usually driven by Clk_hf1~N that is only available after CPU configures their roots in the SRSS) to provide back the Q-Channel handshake, if not the deadlock situation will procure. To avoid deadlock mentioned above, all IPs in all groups other than group-0 are disabled (SL_CTL.ENABLED is set to '0') by default after POR (cold boot) (i.e. PERI HW hardcodes local parameter SL_CTL_DEFAULT to 32'hFFFFFFFF for group-0 and to 32'h00000000 for other groups (group-1 to group-15)). Once CPU is up and running & Clk_hf1~N configured, CPU can enable them. The SL_CTL.ENABLED are retained during DEEPSLEEP to avoid enabling configuration after wakeup. Default Value: 0

10.1.12 PERI0_GR3_SL_CTL2

Slave control2

Address: 0x420040D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		RST [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	RST	Slave reset. Each bit indicates whether the respective slave is enabled. If the slave is under reset, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 slave 0,1, and 2 (the peripheral interconnect MMIO registers), this field is a constant '0' (SW: R): the slave can NOT be in reset. Default Value: 0

10.1.13 PERI0_GR5_SL_CTL

Slave control

Address: 0x42004150

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							ENABLED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	ENABLED	Slave Enable. Each bit indicates whether the respective slave is enabled. If the slave is disabled, its clock is gated off (constant "0"). Note: For peripheral group 0 slave 0,1, and 2 (the peripheral interconnect MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. The peripheral IP that drives the Q-Channel back to Clock Controllers need to ensure that it has clock (usually driven by Clk_hf1~N that is only available after CPU configures their roots in the SRSS) to provide back the Q-Channel handshake, if not the deadlock situation will procure. To avoid deadlock mentioned above, all IPs in all groups other than group-0 are disabled (SL_CTL.ENABLED is set to '0') by default after POR (cold boot) (i.e. PERI HW hardcodes local parameter SL_CTL_DEFAULT to 32'hFFFFFFFF for group-0 and to 32'h00000000 for other groups (group-1 to group-15)). Once CPU is up and running & Clk_hf1~N configured, CPU can enable them. The SL_CTL.ENABLED are retained during DEEPSLEEP to avoid enabling configuration after wakeup. Default Value: 0

10.1.14 PERI0_GR5_SL_CTL2

Slave control2

Address: 0x42004154

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							RST

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	RST	Slave reset. Each bit indicates whether the respective slave is enabled. If the slave is under reset, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 slave 0,1, and 2 (the peripheral interconnect MMIO registers), this field is a constant '0' (SW: R): the slave can NOT be in reset. Default Value: 0

10.1.15 PERI0_TR_GR0_TR_CTL0

Trigger control register

Address: 0x42008000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	TR_SEL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_-FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
6 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

10.1.16 PERI0_TR_GR2_TR_CTL0

Trigger control register

Address: 0x42008800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TR_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_-FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
7 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

10.1.17 PERI0_TR_GR3_TR_CTL0

Trigger control register

Address: 0x42008C00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TR_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None			
HW Access	None			R	None			
Name	None [15:13]			DBG_-FREEZE_EN	None [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
3 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

10.1.18 PERI0_TR_GR6_TR_CTL0

Trigger control register

Address: 0x42009800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TR_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_-FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
7 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

10.1.19 PERI0_TR_GR7_TR_CTL0

Trigger control register

Address: 0x42009C00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						TR_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_-FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
1 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

10.1.20 PERI0_TR_GR9_TR_CTL0

Trigger control register

Address: 0x4200A400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			TR_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_-FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
4 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

10.1.21 PERI0_TR_GR10_TR_CTL0

Trigger control register

Address: 0x4200A800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TR_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_-FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
7 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

10.1.22 PERI0_TR_GR11_TR_CTL0

Trigger control register

Address: 0x4200AC00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:6]			TR_SEL [5:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_-FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
5 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

10.1.23 PERI0_TR_GR12_TR_CTL0

Trigger control register

Address: 0x4200B000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			TR_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_-FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
4 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

10.1.24 PERI0_TR_GR13_TR_CTL0

Trigger control register

Address: 0x4200B400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	TR_SEL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_-FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
6 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

10.1.25 PERI0_TR_1TO1_GR0_TR_CTL0

Trigger control register

Address: 0x4200C000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TR_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_-FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
0	TR_SEL	Specifies input trigger: '0'': constant signal level '0'. '1': input trigger. Default Value: 0

10.1.26 PERI0_TR_1TO1_GR1_TR_CTL0

Trigger control register

Address: 0x4200C400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TR_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_-FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
0	TR_SEL	Specifies input trigger: '0'': constant signal level '0'. '1': input trigger. Default Value: 0

10.1.27 PERI0_TR_1TO1_GR2_TR_CTL0

Trigger control register

Address: 0x4200C800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TR_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_-FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
0	TR_SEL	Specifies input trigger: '0'': constant signal level '0'. '1': input trigger. Default Value: 0

11 System Resources and Clocking registers

This section discusses the System Resources and Clocking registers. It lists all the registers in mapping tables, in address order.

11.1 Register details

Register	Address	Description
PERI_PCLK0_GR0_DIV_CMD	0x42040000	Divider command
PERI_PCLK0_GR0_CLOCK_CTL0	0x42040C00	Clock control
PERI_PCLK0_GR0_DIV_24_5_CTL0	0x42041C00	Divider control (for 24.5 divider)
PERI_PCLK0_GR1_DIV_CMD	0x42042000	Divider command. See PERI_PCLK0_GR0_DIV_CMD for the details of bit fields.
PERI_PCLK0_GR1_CLOCK_CTL0	0x42042C00	Clock control
PERI_PCLK0_GR1_CLOCK_CTL1	0x42042C04	Clock control. See PERI_PCLK0_GR1_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR1_CLOCK_CTL2	0x42042C08	Clock control. See PERI_PCLK0_GR1_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR1_CLOCK_CTL3	0x42042C0C	Clock control. See PERI_PCLK0_GR1_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR1_CLOCK_CTL4	0x42042C10	Clock control. See PERI_PCLK0_GR1_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR1_CLOCK_CTL5	0x42042C14	Clock control. See PERI_PCLK0_GR1_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR1_CLOCK_CTL6	0x42042C18	Clock control. See PERI_PCLK0_GR1_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR1_DIV_8_CTL0	0x42043000	Divider control (for 8.0 divider)
PERI_PCLK0_GR4_DIV_CMD	0x42048000	Divider command. See PERI_PCLK0_GR0_DIV_CMD for the details of bit fields.
PERI_PCLK0_GR4_CLOCK_CTL0	0x42048C00	Clock control. See PERI_PCLK0_GR1_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR4_CLOCK_CTL1	0x42048C04	Clock control. See PERI_PCLK0_GR1_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR4_CLOCK_CTL2	0x42048C08	Clock control. See PERI_PCLK0_GR1_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR4_CLOCK_CTL3	0x42048C0C	Clock control. See PERI_PCLK0_GR1_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR4_CLOCK_CTL4	0x42048C10	Clock control. See PERI_PCLK0_GR1_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR4_CLOCK_CTL5	0x42048C14	Clock control. See PERI_PCLK0_GR1_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR4_CLOCK_CTL6	0x42048C18	Clock control. See PERI_PCLK0_GR1_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR4_DIV_8_CTL0	0x42049000	Divider control ((forfor 8.0 divider)

Register	Address	Description
PERI_PCLK0_GR4_DIV_8_CTL1	0x42049004	Divider control (for 8.0 divider). See PERI_PCLK0_GR4_DIV_8_CTL0 for the details of bit fields.
PERI_PCLK0_GR4_DIV_16_CTL0	0x42049400	Divider control (for 16.0 divider)
PERI_PCLK0_GR4_DIV_16_5_CTL0	0x42049800	Divider control (for 16.5 divider)
PERI_PCLK0_GR4_DIV_16_5_CTL1	0x42049804	Divider control (for 16.5 divider). See PERI_PCLK0_GR4_DIV_16_5_CTL0 for the details of bit fields.
PERI_PCLK0_GR4_DIV_16_5_CTL2	0x42049808	Divider control (for 16.5 divider). See PERI_PCLK0_GR4_DIV_16_5_CTL0 for the details of bit fields.
PERI_PCLK0_GR4_DIV_24_5_CTL0	0x42049C00	Divider control (for 24.5 divider). See PERI_PCLK0_GR0_DIV_24_5_CTL0 for the details of bit fields.
PERI_PCLK0_GR5_DIV_CMD	0x4204A000	Divider command. See PERI_PCLK0_GR0_DIV_CMD for the details of bit fields.
PERI_PCLK0_GR5_CLOCK_CTL0	0x4204AC00	Clock control
PERI_PCLK0_GR5_CLOCK_CTL1	0x4204AC04	Clock control. See PERI_PCLK0_GR5_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR5_CLOCK_CTL2	0x4204AC08	Clock control. See PERI_PCLK0_GR5_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR5_CLOCK_CTL3	0x4204AC0C	Clock control. See PERI_PCLK0_GR5_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR5_CLOCK_CTL4	0x4204AC10	Clock control. See PERI_PCLK0_GR5_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR5_CLOCK_CTL5	0x4204AC14	Clock control. See PERI_PCLK0_GR5_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR5_CLOCK_CTL6	0x4204AC18	Clock control. See PERI_PCLK0_GR5_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR5_CLOCK_CTL7	0x4204AC1C	Clock control. See PERI_PCLK0_GR5_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR5_CLOCK_CTL8	0x4204AC20	Clock control. See PERI_PCLK0_GR5_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR5_CLOCK_CTL9	0x4204AC24	Clock control. See PERI_PCLK0_GR5_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR5_CLOCK_CTL10	0x4204AC28	Clock control. See PERI_PCLK0_GR5_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR5_CLOCK_CTL11	0x4204AC2C	Clock control. See PERI_PCLK0_GR5_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR5_CLOCK_CTL12	0x4204AC30	Clock control. See PERI_PCLK0_GR5_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR5_CLOCK_CTL13	0x4204AC34	Clock control. See PERI_PCLK0_GR5_CLOCK_CTL0 for the details of bit fields.

Register	Address	Description
PERI_PCLK0_GR5_CLOCK_CTL14	0x4204AC38	Clock control. See PERI_PCLK0_GR5_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR5_CLOCK_CTL15	0x4204AC3C	Clock control. See PERI_PCLK0_GR5_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR5_CLOCK_CTL16	0x4204AC40	Clock control. See PERI_PCLK0_GR5_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR5_CLOCK_CTL17	0x4204AC44	Clock control. See PERI_PCLK0_GR5_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR5_CLOCK_CTL18	0x4204AC48	Clock control. See PERI_PCLK0_GR5_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR5_CLOCK_CTL19	0x4204AC4C	Clock control. See PERI_PCLK0_GR5_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR5_CLOCK_CTL20	0x4204AC50	Clock control. See PERI_PCLK0_GR5_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR5_CLOCK_CTL21	0x4204AC54	Clock control. See PERI_PCLK0_GR5_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR5_DIV_8_CTL0	0x4204B000	Divider control (for 8.0 divider)
PERI_PCLK0_GR5_DIV_8_CTL1	0x4204B004	Divider control (for 8.0 divider). See PERI_PCLK0_GR5_DIV_8_CTL0 for the details of bit fields.
PERI_PCLK0_GR5_DIV_8_CTL2	0x4204B008	Divider control (for 8.0 divider). See PERI_PCLK0_GR5_DIV_8_CTL0 for the details of bit fields.
PERI_PCLK0_GR5_DIV_8_CTL3	0x4204B00C	Divider control (for 8.0 divider). See PERI_PCLK0_GR5_DIV_8_CTL0 for the details of bit fields.
PERI_PCLK0_GR5_DIV_8_CTL4	0x4204B010	Divider control (for 8.0 divider). See PERI_PCLK0_GR5_DIV_8_CTL0 for the details of bit fields.
PERI_PCLK0_GR5_DIV_8_CTL5	0x4204B014	Divider control (for 8.0 divider). See PERI_PCLK0_GR5_DIV_8_CTL0 for the details of bit fields.
PERI_PCLK0_GR5_DIV_8_CTL6	0x4204B018	Divider control (for 8.0 divider). See PERI_PCLK0_GR5_DIV_8_CTL0 for the details of bit fields.
PERI_PCLK0_GR5_DIV_8_CTL7	0x4204B01C	Divider control (for 8.0 divider). See PERI_PCLK0_GR5_DIV_8_CTL0 for the details of bit fields.
PERI_PCLK0_GR5_DIV_8_CTL8	0x4204B020	Divider control (for 8.0 divider). See PERI_PCLK0_GR5_DIV_8_CTL0 for the details of bit fields.
PERI_PCLK0_GR5_DIV_8_CTL9	0x4204B024	Divider control (for 8.0 divider). See PERI_PCLK0_GR5_DIV_8_CTL0 for the details of bit fields.

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Register	Address	Description
PERI_PCLK0_GR5_DIV_16_CTL0	0x4204B400	Divider control (for 16.0 divider)
PERI_PCLK0_GR5_DIV_16_CTL1	0x4204B404	Divider control (for 16.0 divider). See PERI_PCLK0_GR5_DIV_16_CTL0 for the details of bit fields.
PERI_PCLK0_GR5_DIV_16_CTL2	0x4204B408	Divider control (for 16.0 divider). See PERI_PCLK0_GR5_DIV_16_CTL0 for the details of bit fields.
PERI_PCLK0_GR5_DIV_16_CTL3	0x4204B40C	Divider control (for 16.0 divider). See PERI_PCLK0_GR5_DIV_16_CTL0 for the details of bit fields.
PERI_PCLK0_GR6_DIV_CMD	0x4204C000	Divider command. See PERI_PCLK0_GR0_DIV_CMD for the details of bit fields.
PERI_PCLK0_GR6_CLOCK_CTL0	0x4204CC00	Clock control. See PERI_PCLK0_GR0_CLOCK_CTL0 for the details of bit fields.
PERI_PCLK0_GR6_DIV_16_5_CTL0	0x4204D800	Divider control (for 16.5 divider)
PWR_LVD_STATUS	0x42200040	High Voltage / Low Voltage Detector (HVLVD) Status Register
CLK_DSI_SELECT0	0x42200100	Clock DSI Select Register
CLK_DSI_SELECT1	0x42200104	Clock DSI Select Register. See CLK_DSI_SELECT0 for the details of bit fields.
CLK_DSI_SELECT2	0x42200108	Clock DSI Select Register. See CLK_DSI_SELECT0 for the details of bit fields.
CLK_DSI_SELECT3	0x4220010C	Clock DSI Select Register. See CLK_DSI_SELECT0 for the details of bit fields.
CLK_DSI_SELECT4	0x42200110	Clock DSI Select Register. See CLK_DSI_SELECT0 for the details of bit fields.
CLK_DSI_SELECT5	0x42200114	Clock DSI Select Register. See CLK_DSI_SELECT0 for the details of bit fields.
CLK_DSI_SELECT6	0x42200118	Clock DSI Select Register. See CLK_DSI_SELECT0 for the details of bit fields.
CLK_OUTPUT_FAST	0x42200140	Fast Clock Output Select Register
CLK_OUTPUT_SLOW	0x42200144	Slow Clock Output Select Register
CLK_CAL_CNT1	0x42200148	Clock Calibration Counter 1
CLK_CAL_CNT2	0x4220014C	Clock Calibration Counter 2
SRSS_INTR	0x42200200	SRSS Interrupt Register
SRSS_INTR_SET	0x42200204	SRSS Interrupt Set Register
SRSS_INTR_MASK	0x42200208	SRSS Interrupt Mask Register
SRSS_INTR_MASKED	0x4220020C	SRSS Interrupt Masked Register
SRSS_AINTR	0x42200300	SRSS Additional Interrupt Register
SRSS_AINTR_SET	0x42200304	SRSS Additional Interrupt Set Register
SRSS_AINTR_MASK	0x42200308	SRSS Additional Interrupt Mask Register
SRSS_AINTR_MASKED	0x4220030C	SRSS Additional Interrupt Masked Register

System Resources and Clocking registers

Register	Address	Description
BOOT_DLM_CTL	0x42200404	Debug Control Register
BOOT_DLM_CTL2	0x42200408	Debug Control Register 2
BOOT_DLM_STATUS	0x4220040C	Debug Status Register
RES_SOFT_CTL	0x42200410	Soft Reset Trigger Register
BOOT_STATUS	0x42200418	Boot Execution Status Register
BOOT_ENTRY	0x42200430	Warm Boot Entry Address
PWR_HIB_WAKE_CTL	0x422008A0	Hibernate Wakeup Mask Register
PWR_HIB_WAKE_CTL2	0x422008A4	Hibernate Wakeup Polarity Register
PWR_HIB_WAKE_CAUSE	0x422008AC	Hibernate Wakeup Cause Register
PWR_CTL	0x42201000	Power Mode Control
PWR_CTL2	0x42201004	Power Mode Control 2
PWR_HIBERNATE	0x42201008	HIBERNATE Mode Register
PWR_LVD_CTL	0x42201020	High Voltage / Low Voltage Detector (HVLVD) Configuration Register
CLK_PATH_SELECT0	0x42201200	Clock Path Select Register
CLK_PATH_SELECT1	0x42201204	Clock Path Select Register. See CLK_PATH_SELECT0 for the details of bit fields.
CLK_PATH_SELECT2	0x42201208	Clock Path Select Register. See CLK_PATH_SELECT0 for the details of bit fields.
CLK_PATH_SELECT3	0x4220120C	Clock Path Select Register. See CLK_PATH_SELECT0 for the details of bit fields.
CLK_PATH_SELECT4	0x42201210	Clock Path Select Register. See CLK_PATH_SELECT0 for the details of bit fields.
CLK_PATH_SELECT5	0x42201214	Clock Path Select Register. See CLK_PATH_SELECT0 for the details of bit fields.
CLK_PATH_SELECT6	0x42201218	Clock Path Select Register. See CLK_PATH_SELECT0 for the details of bit fields.
CLK_ROOT_SELECT0	0x42201240	Clock Root Select Register
CLK_ROOT_SELECT1	0x42201244	Clock Root Select Register. See CLK_ROOT_SELECT0 for the details of bit fields.
CLK_ROOT_SELECT2	0x42201248	Clock Root Select Register. See CLK_ROOT_SELECT0 for the details of bit fields.
CLK_ROOT_SELECT3	0x4220124C	Clock Root Select Register. See CLK_ROOT_SELECT0 for the details of bit fields.
CLK_ROOT_SELECT4	0x42201250	Clock Root Select Register. See CLK_ROOT_SELECT0 for the details of bit fields.
CLK_ROOT_SELECT5	0x42201254	Clock Root Select Register. See CLK_ROOT_SELECT0 for the details of bit fields.
CLK_ROOT_SELECT6	0x42201258	Clock Root Select Register. See CLK_ROOT_SELECT0 for the details of bit fields.
CLK_DIRECT_SELECT0	0x42201280	Clock Root Direct Select Register

Register	Address	Description
CLK_DIRECT_SELECT1	0x42201284	Clock Root Direct Select Register. See CLK_DIRECT_SELECT0 for the details of bit fields.
CLK_DIRECT_SELECT2	0x42201288	Clock Root Direct Select Register. See CLK_DIRECT_SELECT0 for the details of bit fields.
CLK_DIRECT_SELECT3	0x4220128C	Clock Root Direct Select Register. See CLK_DIRECT_SELECT0 for the details of bit fields.
CLK_DIRECT_SELECT4	0x42201290	Clock Root Direct Select Register. See CLK_DIRECT_SELECT0 for the details of bit fields.
CLK_DIRECT_SELECT5	0x42201294	Clock Root Direct Select Register. See CLK_DIRECT_SELECT0 for the details of bit fields.
CLK_DIRECT_SELECT6	0x42201298	Clock Root Direct Select Register. See CLK_DIRECT_SELECT0 for the details of bit fields.
CSV_HF_CSV0_REF_CTL	0x42201400	Clock Supervision Reference Control
CSV_HF_CSV0_REF_LIMIT	0x42201404	Clock Supervision Reference Limits
CSV_HF_CSV0_MON_CTL	0x42201408	Clock Supervision Monitor Control
CSV_HF_CSV1_REF_CTL	0x42201410	Clock Supervision Reference Control. See CSV_HF_CSV0_REF_CTL for the details of bit fields.
CSV_HF_CSV1_REF_LIMIT	0x42201414	Clock Supervision Reference Limits. See CSV_HF_CSV0_REF_LIMIT for the details of bit fields.
CSV_HF_CSV1_MON_CTL	0x42201418	Clock Supervision Monitor Control. See CSV_HF_CSV0_MON_CTL for the details of bit fields.
CSV_HF_CSV2_REF_CTL	0x42201420	Clock Supervision Reference Control. See CSV_HF_CSV0_REF_CTL for the details of bit fields.
CSV_HF_CSV2_REF_LIMIT	0x42201424	Clock Supervision Reference Limits. See CSV_HF_CSV0_REF_LIMIT for the details of bit fields.
CSV_HF_CSV2_MON_CTL	0x42201428	Clock Supervision Monitor Control. See CSV_HF_CSV0_MON_CTL for the details of bit fields.
CSV_HF_CSV3_REF_CTL	0x42201430	Clock Supervision Reference Control. See CSV_HF_CSV0_REF_CTL for the details of bit fields.
CSV_HF_CSV3_REF_LIMIT	0x42201434	Clock Supervision Reference Limits. See CSV_HF_CSV0_REF_LIMIT for the details of bit fields.
CSV_HF_CSV3_MON_CTL	0x42201438	Clock Supervision Monitor Control. See CSV_HF_CSV0_MON_CTL for the details of bit fields.
CSV_HF_CSV4_REF_CTL	0x42201440	Clock Supervision Reference Control. See CSV_HF_CSV0_REF_CTL for the details of bit fields.
CSV_HF_CSV4_REF_LIMIT	0x42201444	Clock Supervision Reference Limits. See CSV_HF_CSV0_REF_LIMIT for the details of bit fields.
CSV_HF_CSV4_MON_CTL	0x42201448	Clock Supervision Monitor Control. See CSV_HF_CSV0_MON_CTL for the details of bit fields.
CSV_HF_CSV5_REF_CTL	0x42201450	Clock Supervision Reference Control. See CSV_HF_CSV0_REF_CTL for the details of bit fields.
CSV_HF_CSV5_REF_LIMIT	0x42201454	Clock Supervision Reference Limits. See CSV_HF_CSV0_REF_LIMIT for the details of bit fields.

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Register	Address	Description
CSV_HF_CSV5_MON_CTL	0x42201458	Clock Supervision Monitor Control. See CSV_HF_CSV0_MON_CTL for the details of bit fields.
CSV_HF_CSV6_REF_CTL	0x42201460	Clock Supervision Reference Control. See CSV_HF_CSV0_REF_CTL for the details of bit fields.
CSV_HF_CSV6_REF_LIMIT	0x42201464	Clock Supervision Reference Limits. See CSV_HF_CSV0_REF_LIMIT for the details of bit fields.
CSV_HF_CSV6_MON_CTL	0x42201468	Clock Supervision Monitor Control. See CSV_HF_CSV0_MON_CTL for the details of bit fields.
CLK_SELECT	0x42201500	Clock selection register
CLK_IMO_CONFIG	0x42201518	IMO Configuration
CLK_ECO_CONFIG	0x4220151C	ECO Configuration Register
CLK_ECO_PRESCALE	0x42201520	ECO Prescaler Configuration Register
CLK_ECO_STATUS	0x42201524	ECO Status Register
CLK_FLL_CONFIG	0x42201530	FLL Configuration Register
CLK_FLL_CONFIG2	0x42201534	FLL Configuration Register 2
CLK_FLL_CONFIG3	0x42201538	FLL Configuration Register 3
CLK_FLL_CONFIG4	0x4220153C	FLL Configuration Register 4
CLK_FLL_STATUS	0x42201540	FLL Status Register
CLK_ECO_CONFIG2	0x42201544	ECO Configuration Register 2
CLK_ILO_CONFIG	0x42201548	ILO Configuration
CLK_TRIM_ILO_CTL	0x4220154C	ILO Trim Register
CLK_MF_SELECT	0x42201554	Medium Frequency Clock Select Register
CLK_MFO_CONFIG	0x42201558	MFO Configuration Register
CLK_IHO_CONFIG	0x42201560	IHO Configuration Register
CSV_REF_SEL	0x42201700	Select CSV Reference clock for Active domain
CSV_REF_CSV_REF_CTL	0x42201710	Clock Supervision Reference Control. See CSV_HF_CSV0_REF_CTL for the details of bit fields.
CSV_REF_CSV_REF_LIMIT	0x42201714	Clock Supervision Reference Limits. See CSV_HF_CSV0_REF_LIMIT for the details of bit fields.
CSV_REF_CSV_MON_CTL	0x42201718	Clock Supervision Monitor Control. See CSV_HF_CSV0_MON_CTL for the details of bit fields.
CSV_LF_CSV_REF_CTL	0x42201720	Clock Supervision Reference Control
CSV_LF_CSV_REF_LIMIT	0x42201724	Clock Supervision Reference Limits
CSV_LF_CSV_MON_CTL	0x42201728	Clock Supervision Monitor Control
CSV_ILO_CSV_REF_CTL	0x42201730	Clock Supervision Reference Control. See CSV_LF_CSV_REF_CTL for the details of bit fields.
CSV_ILO_CSV_REF_LIMIT	0x42201734	Clock Supervision Reference Limits. See CSV_LF_CSV_REF_LIMIT for the details of bit fields.
CSV_ILO_CSV_MON_CTL	0x42201738	Clock Supervision Monitor Control. See CSV_LF_CSV_MON_CTL for the details of bit fields.
RES_CAUSE	0x42201800	Reset Cause Observation Register

Register	Address	Description
RES_CAUSE2	0x42201804	Reset Cause Observation Register 2
RES_PXRES_CTL	0x42201814	Programmable XRES Control Register
CLK_DPLL_LP0_CONFIG	0x42201A00	DPLL_LP Configuration Register
CLK_DPLL_LP0_CONFIG2	0x42201A04	DPLL_LP Configuration Register 2
CLK_DPLL_LP0_CONFIG3	0x42201A08	DPLL_LP Configuration Register 3
CLK_DPLL_LP0_CONFIG4	0x42201A0C	DPLL_LP Configuration Register 4
CLK_DPLL_LP0_CONFIG5	0x42201A10	DPLL_LP Configuration Register 5
CLK_DPLL_LP0_CONFIG6	0x42201A14	DPLL_LP Configuration Register 6
CLK_DPLL_LP0_CONFIG7	0x42201A18	DPLL_LP Configuration Register 7
CLK_DPLL_LP0_STATUS	0x42201A1C	DPLL_LP Status Register
CLK_DPLL_LP1_CONFIG	0x42201A20	DPLL_LP Configuration Register. See CLK_DPLL_LP0_CONFIG for the details of bit fields.
CLK_DPLL_LP1_CONFIG2	0x42201A24	DPLL_LP Configuration Register 2. See CLK_DPLL_LP0_CONFIG2 for the details of bit fields.
CLK_DPLL_LP1_CONFIG3	0x42201A28	DPLL_LP Configuration Register 3. See CLK_DPLL_LP0_CONFIG3 for the details of bit fields.
CLK_DPLL_LP1_CONFIG4	0x42201A2C	DPLL_LP Configuration Register 4. See CLK_DPLL_LP0_CONFIG4 for the details of bit fields.
CLK_DPLL_LP1_CONFIG5	0x42201A30	DPLL_LP Configuration Register 5. See CLK_DPLL_LP0_CONFIG5 for the details of bit fields.
CLK_DPLL_LP1_CONFIG6	0x42201A34	DPLL_LP Configuration Register 6. See CLK_DPLL_LP0_CONFIG6 for the details of bit fields.
CLK_DPLL_LP1_CONFIG7	0x42201A38	DPLL_LP Configuration Register 7. See CLK_DPLL_LP0_CONFIG7 for the details of bit fields.
CLK_DPLL_LP1_STATUS	0x42201A3C	DPLL_LP Status Register. See CLK_DPLL_LP0_STATUS for the details of bit fields.
TST_XRES_SECURE	0x42202054	SECURE TEST and FIRMWARE TEST Key control register
PWR_TRIM_PWRSYS_CTL	0x422020E0	Power System Trim Register
PWR_TRIM_PWRSYS_CTL2	0x422020E4	Power System Trim Register 2
CLK_TRIM_ECO_CTL	0x4220301C	ECO Trim Register
RAM_TRIM_TRIM_RAM_CTL	0x42204000	Trim Register for RAM Type 0
RAM_TRIM_TRIM_ROM_CTL	0x42204004	Trim Register for ROM
CLK_TRIM_DPLL_LP0_DPLL_LP_CTL	0x42204200	DPLL LP Trim Register
CLK_TRIM_DPLL_LP0_DPLL_LP_CTL3	0x42204208	DPLL LP Trim Register 3
CLK_TRIM_DPLL_LP0_DPLL_LP_CTL4	0x4220420C	DPLL LP Trim Register 4
CLK_TRIM_DPLL_LP0_DPLL_LP_TEST4	0x4220421C	DPLL LP Test Register 4
CLK_TRIM_DPLL_LP1_DPLL_LP_CTL	0x42204220	DPLL LP Trim Register. See CLK_TRIM_DPLL_LP0_DPLL_LP_CTL for the details of bit fields.

System Resources and Clocking registers

Register	Address	Description
CLK_TRIM_DPLL_LP1_DPLL_LP_CTL3	0x42204228	DPLL LP Trim Register 3. See CLK_TRIM_DPLL_LP0_DPLL_LP_CTL3 for the details of bit fields.
CLK_TRIM_DPLL_LP1_DPLL_LP_CTL4	0x4220422C	DPLL LP Trim Register 4. See CLK_TRIM_DPLL_LP0_DPLL_LP_CTL4 for the details of bit fields.
CLK_TRIM_DPLL_LP1_DPLL_LP_TEST4	0x4220423C	DPLL LP Test Register 4. See CLK_TRIM_DPLL_LP0_DPLL_LP_TEST4 for the details of bit fields.
WDT_CTL	0x4220C000	Watchdog Counter Control Register (Type A)
WDT_CNT	0x4220C004	Watchdog Counter Count Register (Type A)
WDT_MATCH	0x4220C008	Watchdog Counter Match Register (Type A)
WDT_MATCH2	0x4220C00C	Watchdog Counter Match Register 2 (Type A)
MCWDT_CNTLOW0	0x4220D004	Multi-Counter Watchdog Sub-counters 0/1
MCWDT_CNTHIGH0	0x4220D008	Multi-Counter Watchdog Sub-counter 2
MCWDT_MATCH0	0x4220D00C	Multi-Counter Watchdog Counter Match Register
MCWDT_CONFIG0	0x4220D010	Multi-Counter Watchdog Counter Configuration
MCWDT_CTL0	0x4220D014	Multi-Counter Watchdog Counter Control
MCWDT_INTR0	0x4220D018	Multi-Counter Watchdog Counter Interrupt Register
MCWDT_INTR_SET0	0x4220D01C	Multi-Counter Watchdog Counter Interrupt Set Register
MCWDT_INTR_MASK0	0x4220D020	Multi-Counter Watchdog Counter Interrupt Mask Register
MCWDT_INTR_MASKED0	0x4220D024	Multi-Counter Watchdog Counter Interrupt Masked Register
MCWDT_LOCK0	0x4220D028	Multi-Counter Watchdog Counter Lock Register
MCWDT_LOWER_LIMIT0	0x4220D02C	Multi-Counter Watchdog Counter Lower Limit Register

11.1.1 PERI_PCLK0_GR0_DIV_CMD

Divider command

Address: 0x42040000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DIV_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						TYPE_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	PA_DIV_SEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None				RW	
HW Access	RW1C	RW1C	None				R	
Name	ENABLE	DISABLE	None [29:26]				PA_TYPE_SEL [25:24]	

Bits	Name	Description
31	ENABLE	Clock divider enable command (mutually exclusive with DISABLE). Typically, SW sets this field to '1' to enable a divider and HW sets this field to '0' to indicate that divider enabling has completed. When a divider is enabled, its integer and fractional (if present) counters are initialized to "0". If a divider is to be re-enabled using different integer and fractional divider values, the SW should follow these steps: 0: Disable the divider using the DIV_CMD.DISABLE field. 1: Configure the divider's DIV_XXX_CTL register. 2: Enable the divider using the DIV_CMD_ENABLE field. The DIV_SEL and TYPE_SEL fields specify which divider is to be enabled. The enabled divider may be phase aligned to either "clk_pclk_root[i]" (typical usage) or to ANY enabled divider. The PA_DIV_SEL and PA_TYPE_SEL fields specify the reference divider. The HW sets the ENABLE field to '0' when the enabling is performed and the HW set the DIV_XXX_CTL.EN field of the divider to '1' when the enabling is performed. Note that enabling with phase alignment to a low frequency divider takes time. E.g. To align to a divider that generates a clock of "clk_pclk_root[i]"/n (with n being the integer divider value INT_DIV+1), up to n cycles may be required to perform alignment. Phase alignment to "clk_pclk_root[i]" takes affect immediately. SW can set this field to '0' during phase alignment to abort the enabling process. Default Value: 0

11.1.1 PERI_PCLK0_GR0_DIV_CMD (continued)

30	DISABLE	Clock divider disable command (mutually exclusive with ENABLE). SW sets this field to '1' and HW sets this field to '0'. The DIV_SEL and TYPE_SEL fields specify which divider is to be disabled. The HW sets the DISABLE field to '0' immediately and the HW sets the DIV_XXX_CTL.EN field of the divider to '0' immediately. Default Value: 0
25 : 24	PA_TYPE_SEL	Specifies the divider type of the divider to which phase alignment is performed for the clock enable command: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
23 : 16	PA_DIV_SEL	(PA_TYPE_SEL, PA_DIV_SEL) specifies the divider to which phase alignment is performed for the clock enable command. Any enabled divider can be used as reference. This allows all dividers to be aligned with each other, even when they are enabled at different times. If PA_DIV_SEL is "255" and PA_TYPE_SEL is "3", "clk_pclk_root[i]" is used as reference. Default Value: 255
9 : 8	TYPE_SEL	Specifies the divider type of the divider on which the command is performed: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
7 : 0	DIV_SEL	(TYPE_SEL, DIV_SEL) specifies the divider on which the command (DISABLE/ENABLE) is performed. If DIV_SEL is "255" and TYPE_SEL is "3" (default/reset value), no divider is specified and no clock signal(s) are generated. Default Value: 255

11.1.2 PERI_PCLK0_GR0_CLOCK_CTL0

Clock control

Address: 0x42040C00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DIV_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						TYPE_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	TYPE_SEL	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	DIV_SEL	Specifies one of the dividers of the divider type specified by TYPE_SEL. If DIV_SEL is "255" and TYPE_SEL is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out-of-phase dividers, spurious clock control signals may be generated for one "clk_pclk_root[i]" cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (DIV_SEL is "255" and TYPE_SEL is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

11.1.3 PERI_PCLK0_GR0_DIV_24_5_CTL0

Divider control (for 24.5 divider)

Address: 0x42041C00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		R
HW Access	R					None		RW
Name	FRAC5_DIV [7:3]					None [2:1]		EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT24_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT24_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	INT24_DIV [31:24]							

Bits	Name	Description
31 : 8	INT24_DIV	Integer division by (1+INT24_DIV). Allows for integer divisions in the range [1, 16,777,216]. Note: combined with fractional division, this divider type allows for a division in the range [1, 16,777,216 31/32] in 1/32 increments. For the generation of a divided clock, the integer division range is restricted to [2, 16,777,216 31/32]. For the generation of a 50/50% duty cycle divided clock, the division range is restricted to [2, 16,777,216]. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
7 : 3	FRAC5_DIV	Fractional division by (FRAC5_DIV/32). Allows for fractional divisions in the range [0, 31/32]. Note that fractional division results in clock jitter as some clock periods may be 1 "clk_pclk_-root[i]" cycle longer than other clock periods. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

11.1.4 PERI_PCLK0_GR1_CLOCK_CTL0

Clock control

Address: 0x42042C00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DIV_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						TYPE_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	TYPE_SEL	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	DIV_SEL	Specifies one of the dividers of the divider type specified by TYPE_SEL. If DIV_SEL is "255" and TYPE_SEL is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out-of-phase dividers, spurious clock control signals may be generated for one "clk_pclk_root[i]" cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (DIV_SEL is "255" and TYPE_SEL is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

11.1.5 PERI_PCLK0_GR1_DIV_8_CTL0

Divider control (for 8.0 divider)

Address: 0x42043000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT8_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	INT8_DIV	Integer division by (1+INT8_DIV). Allows for integer divisions in the range [1, 256]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 256]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 256]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

11.1.6 PERI_PCLK0_GR4_DIV_8_CTL0

Divider control (for 8.0 divider)

Address: 0x42049000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT8_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	INT8_DIV	Integer division by (1+INT8_DIV). Allows for integer divisions in the range [1, 256]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 256]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 256]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

11.1.7 PERI_PCLK0_GR4_DIV_16_CTL0

Divider control (for 16.0 divider)

Address: 0x42049400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

11.1.8 PERI_PCLK0_GR4_DIV_16_5_CTL0

Divider control (for 16.5 divider)

Address: 0x42049800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		R
HW Access	R					None		RW
Name	FRAC5_DIV [7:3]					None [2:1]		EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: combined with fractional division, this divider type allows for a division in the range [1, 65,536 31/32] in 1/32 increments. For the generation of a divided clock, the division range is restricted to [2, 65,536 31/32]. For the generation of a 50/50% duty cycle divided clock, the division range is restricted to [2, 65,536]. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
7 : 3	FRAC5_DIV	Fractional division by (FRAC5_DIV/32). Allows for fractional divisions in the range [0, 31/32]. Note that fractional division results in clock jitter as some clock periods may be 1 "clk_pclk_-root[i]" cycle longer than other clock periods. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

11.1.9 PERI_PCLK0_GR5_CLOCK_CTL0

Clock control

Address: 0x4204AC00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DIV_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						TYPE_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	TYPE_SEL	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	DIV_SEL	Specifies one of the dividers of the divider type specified by TYPE_SEL. If DIV_SEL is "255" and TYPE_SEL is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out-of-phase dividers, spurious clock control signals may be generated for one "clk_pclk_root[i]" cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (DIV_SEL is "255" and TYPE_SEL is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

11.1.10 PERI_PCLK0_GR5_DIV_8_CTL0

Divider control (for 8.0 divider)

Address: 0x4204B000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT8_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	INT8_DIV	Integer division by (1+INT8_DIV). Allows for integer divisions in the range [1, 256]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 256]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 256]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

11.1.11 PERI_PCLK0_GR5_DIV_16_CTL0

Divider control (for 16.0 divider)

Address: 0x4204B400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

11.1.12 PERI_PCLK0_GR6_DIV_16_5_CTL0

Divider control (for 16.5 divider)

Address: 0x4204D800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		R
HW Access	R					None		RW
Name	FRAC5_DIV [7:3]					None [2:1]		EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: combined with fractional division, this divider type allows for a division in the range [1, 65,536 31/32] in 1/32 increments. For the generation of a divided clock, the division range is restricted to [2, 65,536 31/32]. For the generation of a 50/50% duty cycle divided clock, the division range is restricted to [2, 65,536]. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
7 : 3	FRAC5_DIV	Fractional division by (FRAC5_DIV/32). Allows for fractional divisions in the range [0, 31/32]. Note that fractional division results in clock jitter as some clock periods may be 1 "clk_pclk_-root[i]" cycle longer than other clock periods. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

11.1.13 PWR_LVD_STATUS

High Voltage / Low Voltage Detector (HVLVD) Status Register

Address: 0x42200040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							HVL-VD1_OK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	HVLVD1_OK	HVLVD1 output. 0: below voltage threshold 1: above voltage threshold Default Value: 0

11.1.14 CLK_DSI_SELECT0

Clock DSI Select Register

Address: 0x42200100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			DSI_MUX [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	DSI_MUX	Selects a DSI source or low frequency clock for use in a clock path. The output of this mux can be selected for clock PATH *using CLK_SELECT_PATH register. Using the output of this mux as HFCLK source will result in undefined behavior. It can be used to clocks to DSI or as reference inputs for the FLL/PLL, subject to the frequency limits of those circuits. This mux is not glitch free, so do not change the selection while it is an actively selected clock. Default Value: 0* **0x0: DSI_OUT0 :** DSI0 - dsi_out[0] **0x1: DSI_OUT1 :** DSI1 - dsi_out[1] **0x2: DSI_OUT2 :** DSI2 - dsi_out[2] **0x3: DSI_OUT3 :** DSI3 - dsi_out[3] **0x4: DSI_OUT4 :** DSI4 - dsi_out[4]

11.1.14 CLK_DSI_SELECT0 (continued)

0x5: DSI_OUT5 :

DSI5 - dsi_out[5]

0x6: DSI_OUT6 :

DSI6 - dsi_out[6]

0x7: DSI_OUT7 :

DSI7 - dsi_out[7]

0x8: DSI_OUT8 :

DSI8 - dsi_out[8]

0x9: DSI_OUT9 :

DSI9 - dsi_out[9]

0xa: DSI_OUT10 :

DSI10 - dsi_out[10]

0xb: DSI_OUT11 :

DSI11 - dsi_out[11]

0xc: DSI_OUT12 :

DSI12 - dsi_out[12]

0xd: DSI_OUT13 :

DSI13 - dsi_out[13]

0xe: DSI_OUT14 :

DSI14 - dsi_out[14]

0xf: DSI_OUT15 :

DSI15 - dsi_out[15]

0x10: ILO :

ILO - Internal Low-speed Oscillator #0

0x11: WCO :

WCO - Watch-Crystal Oscillator

0x12: ALTLF :

ALTLF - Alternate Low-Frequency Clock

11.1.14 CLK_DSI_SELECT0 (continued)

0x13: PILO :

PILO - Precision Internal Low-speed Oscillator

0x14: ILO1 :

ILO1 - Internal Low-speed Oscillator #1, if present.

11.1.15 CLK_OUTPUT_FAST

Fast Clock Output Select Register

Address: 0x42200140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PATH_SEL0 [7:4]				FAST_SEL0 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				HFCLK_SEL0 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	PATH_SEL1 [23:20]				FAST_SEL1 [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				RW			
HW Access	None				R			
Name	None [31:28]				HFCLK_SEL1 [27:24]			

Bits	Name	Description
27 : 24	HFCLK_SEL1	Selects a HFCLK tree for use in fast clock output #1 logic Default Value: 0
23 : 20	PATH_SEL1	Selects a clock path to use in fast clock output #1 logic. Default Value: 0
19 : 16	FAST_SEL1	Select signal for fast clock output #1 Default Value: 0 **0x0: NC :** Disabled - output is 0. For power savings, clocks are blocked before entering any muxes, including PATH_SEL1 and HFCLK_SEL1. **0x1: ECO :** External Crystal Oscillator (ECO) **0x2: EXTCLK :** External clock input (EXTCLK) **0x3: ALTHF :** Alternate High-Frequency (ALTHF) clock input to SRSS

11.1.15 CLK_OUTPUT_FAST (continued)

		0x4: TIMERCLK : Timer clock. It is grouped with the fast clocks because it may be a gated version of a fast clock, and therefore may have a short high pulse. **0x5: PATH_SEL1 :** Selects the clock path chosen by PATH_SEL1 field **0x6: HFCLK_SEL1 :** Selects the output of the HFCLK_SEL1 mux **0x7: SLOW_SEL1 :** Selects the output of CLK_OUTPUT_SLOW.SLOW_SEL1 **0x8: IHO :** Internal High-speed Oscillator (IHO). **0x9: PWR :** clk_pwr: used for PPU and related components
11 : 8	HFCLK_SEL0	Selects a HFCLK tree for use in fast clock output #0 Default Value: 0
7 : 4	PATH_SEL0	Selects a clock path to use in fast clock output #0 logic. Default Value: 0
3 : 0	FAST_SEL0	Select signal for fast clock output #0 Default Value: 0
		0x0: NC : Disabled - output is 0. For power savings, clocks are blocked before entering any muxes, including PATH_SEL0 and HFCLK_SEL0. **0x1: ECO :** External Crystal Oscillator (ECO) **0x2: EXTCLK :** External clock input (EXTCLK) **0x3: ALTHF :** Alternate High-Frequency (ALTHF) clock input to SRSS **0x4: TIMERCLK :** Timer clock. It is grouped with the fast clocks because it may be a gated version of a fast clock, and therefore may have a short high pulse. **0x5: PATH_SEL0 :** Selects the clock path chosen by PATH_SEL0 field

11.1.15 CLK_OUTPUT_FAST (continued)

0x6: HFCLK_SEL0 :

Selects the output of the HFCLK_SEL0 mux

0x7: SLOW_SEL0 :

Selects the output of CLK_OUTPUT_SLOW.SLOW_SEL0

0x8: IHO :

Internal High-speed Oscillator (IHO).

0x9: PWR :

clk_pwr: used for PPU and related components

11.1.16 CLK_OUTPUT_SLOW

Slow Clock Output Select Register

Address: 0x42200144

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	SLOW_SEL1 [7:4]				SLOW_SEL0 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	SLOW_SEL1	Select signal for slow clock output #1 Default Value: 0 **0x0: NC :** Disabled - output is 0. For power savings, clocks are blocked before entering any muxes. **0x1: ILO :** Internal Low Speed Oscillator (ILO) **0x2: WCO :** Watch-Crystal Oscillator (WCO) **0x3: BAK :** Root of the Backup domain clock tree (BAK) **0x4: ALTLF :** Alternate low-frequency clock input to SRSS (ALTLF)

11.1.16 CLK_OUTPUT_SLOW (continued)

0x5: LFCLK :

Root of the low-speed clock tree (LFCLK)

0x6: IMO :

Internal Main Oscillator (IMO). This is grouped with the slow clocks so it can be observed during DEEPSLEEP entry/exit.

0x7: SLPCTRL :

Sleep Controller clock (SLPCTRL). This is grouped with the slow clocks so it can be observed during DEEPSLEEP entry/exit.

0x8: PILO :

Precision Internal Low Speed Oscillator (PILO)

0x9: ILO1 :

Internal Low Speed Oscillator (ILO1), if present on the product.

0xa: ECO_PRESCALER :

ECO Prescaler (ECO_PRESCALER)

0xb: LPECO :

LPECO

0xc: LPECO_PRESCALER :

LPECO Prescaler (LPECO_PRESCALER)

0xd: MFO :

Medium Frequency Oscillator (MFO)

3 : 0	SLOW_SEL0	Select signal for slow clock output #0 Default Value: 0

0x0: NC :

Disabled - output is 0. For power savings, clocks are blocked before entering any muxes.

0x1: ILO :

Internal Low Speed Oscillator (ILO)

0x2: WCO :

Watch-Crystal Oscillator (WCO)

0x3: BAK :

Root of the Backup domain clock tree (BAK)

11.1.16 CLK_OUTPUT_SLOW (continued)

0x4: ALTLF :

Alternate low-frequency clock input to SRSS (ALTLF)

0x5: LFCLK :

Root of the low-speed clock tree (LFCLK)

0x6: IMO :

Internal Main Oscillator (IMO). This is grouped with the slow clocks so it can be observed during DEEPSLEEP entry/exit.

0x7: SLPCTRL :

Sleep Controller clock (SLPCTRL). This is grouped with the slow clocks so it can be observed during DEEPSLEEP entry/exit.

0x8: PILO :

Precision Internal Low Speed Oscillator (PILO)

0x9: ILO1 :

Internal Low Speed Oscillator (ILO1), if present on the product.

0xa: ECO_PRESCALER :

ECO Prescaler (ECO_PRESCALER)

0xb: LPECO :

LPECO

0xc: LPECO_PRESCALER :

LPECO Prescaler (LPECO_PRESCALER)

0xd: MFO :

Medium Frequency Oscillator (MFO)

11.1.17 CLK_CAL_CNT1

Clock Calibration Counter 1

Address: 0x42200148

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	CAL_COUNTER1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	CAL_COUNTER1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	CAL_COUNTER1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	RW	None				
HW Access	W	W	R	None				
Name	CAL_COUNTER_DONE	CAL_CLK1_PRESENT	CAL_RESET	None [28:24]				

Bits	Name	Description
31	CAL_COUNTER_DONE	Status bit indicating that the internal counter #1 is finished counting and CLK_CAL_CNT2.COUNTER stopped counting up Default Value: 1
30	CAL_CLK1_PRESENT	Status bit indicating that a posedge was detected by counter #1. If this bit never asserts, there is no clock on counter #1 and CAL_COUNTER_DONE will stay low indefinitely. This can be recovered with CAL_RESET. Default Value: 0
29	CAL_RESET	Reset clock calibration logic for window mode. This can be used to recover from unexpected conditions, such as no clock present on counter #1. Set this bit only when CLK_CAL_TEST.CAL_WINDOW_SEL=1 (window mode). It takes 3 clock cycles for reset to propagate. Default Value: 0
23 : 0	CAL_COUNTER1	Down-counter clocked on fast clock output #0 (see CLK_OUTPUT_FAST). This register always reads as zero. Counting starts internally when this register is written with a nonzero value. CAL_COUNTER_DONE goes immediately low to indicate that the counter has started and will be asserted when the counters are done. Do not write this field unless CAL_COUNTER_DONE==1. Both clocks must be running or the measurement will not complete, and this case can be recovered using CAL_RESET. Default Value: 0

11.1.18 CLK_CAL_CNT2

Clock Calibration Counter 2

Address: 0x4220014C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CAL_COUNTER2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CAL_COUNTER2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	CAL_COUNTER2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	CAL_COUNTER2	Up-counter clocked on fast clock output #1 (see CLK_OUTPUT_FAST). When CLK_-CAL_CNT1.CAL_COUNTER_DONE==1, the counter is stopped and can be read by SW. Do not read this value unless CAL_COUNTER_DONE==1. The expected final value is related to the ratio of clock frequencies used for the two counters and the value loaded into counter 1: CLK_-CAL_CNT2.COUNTER=(F_cnt2/F_cnt1)*(CLK_CAL_CNT1.COUNTER) Default Value: 0

11.1.19 SRSS_INTR

SRSS Interrupt Register

Address: 0x42200200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1C	None				RW1C
HW Access	None		A	None				A
Name	None [7:6]		CLK_CAL	None [4:1]				WDT_-MATCH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	AINTR	None [30:24]						

Bits	Name	Description
31	AINTR	See additional interrupts in SRSS_AINTR. Default Value: 0
5	CLK_CAL	Clock calibration counter is done. This field is reset during DEEPSLEEP mode. Default Value: 0
0	WDT_MATCH	WDT Interrupt Request. This bit is set each time WDT_COUNTR==WDT_MATCH. W1C also feeds the watch dog. Missing 2 interrupts in a row will generate a reset. Due to internal synchronization, it takes 2 SYSCLK cycles to update after a W1C. Default Value: 0

11.1.20 SRSS_INTR_SET

SRSS Interrupt Set Register

Address: 0x42200204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1S	None				RW1S
HW Access	None		A	None				A
Name	None [7:6]		CLK_CAL	None [4:1]				WDT_-MATCH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	CLK_CAL	Set interrupt for clock calibration counter done. This field is reset during DEEPSLEEP mode. Default Value: 0
0	WDT_MATCH	Set interrupt for low voltage detector WDT_MATCH Default Value: 0

11.1.21 SRSS_INTR_MASK

SRSS Interrupt Mask Register

Address: 0x42200208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	None				RW
HW Access	None		R	None				R
Name	None [7:6]		CLK_CAL	None [4:1]				WDT_-MATCH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	CLK_CAL	Mask for clock calibration done Default Value: 0
0	WDT_MATCH	Mask for watchdog timer. Clearing this bit will not forward the interrupt to the CPU. It will not, however, disable the WDT reset generation on 2 missed interrupts. When WDT resets the chip, it also internally pends an interrupt that survives the reset. To prevent unintended ISR execution, clear SRSS_INTR.WDT_MATCH before setting this bit. Default Value: 0

11.1.22 SRSS_INTR_MASKED

SRSS Interrupt Masked Register

Address: 0x4220020C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	None				R
HW Access	None		RW	None				RW
Name	None [7:6]		CLK_CAL	None [4:1]				WDT_-MATCH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	AINTR	None [30:24]						

Bits	Name	Description
31	AINTR	See additional MASKED bits in SRSS_AINTR_MASKED.ADDITIONAL Default Value: 0
5	CLK_CAL	Logical and of corresponding request and mask bits. Default Value: 0
0	WDT_MATCH	Logical and of corresponding request and mask bits. Default Value: 0

11.1.23 SRSS_AINTR

SRSS Additional Interrupt Register

Address: 0x42200300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	None
HW Access	None						A	None
Name	None [7:2]						HVLVD1	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	HVLVD1	Interrupt for low voltage detector HVLVD1 Default Value: 0

11.1.24 SRSS_AINTR_SET

SRSS Additional Interrupt Set Register

Address: 0x42200304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	None
HW Access	None						A	None
Name	None [7:2]						HVLVD1	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	HVLVD1	Set interrupt for low voltage detector HVLVD1 Default Value: 0

11.1.25 SRSS_AINTR_MASK

SRSS Additional Interrupt Mask Register

Address: 0x42200308

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	None
HW Access	None						R	None
Name	None [7:2]						HVLVD1	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	HVLVD1	Mask for low voltage detector HVLVD1 Default Value: 0

11.1.26 SRSS_AINTR_MASKED

SRSS Additional Interrupt Masked Register

Address: 0x4220030C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	None
HW Access	None						RW	None
Name	None [7:2]						HVLVD1	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	HVLVD1	Logical and of corresponding request and mask bits. Default Value: 0

11.1.27 BOOT_DLM_CTL

Debug Control Register

Address: 0x42200404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				A			
Name	None [7:4]				REQUEST [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	None				
HW Access	A	A	A	None				
Name	WFA	RESET	IN-PUT_AVAIL	None [28:24]				

Bits	Name	Description
31	WFA	Wait for Action. Set by BootROM when it waits for application or debug certificate to be loaded into the RAM. The bit must be cleared to continue BootROM operation. It is used by the Sys-AP. Default Value: 0
30	RESET	Request the device reset after RAM application complete input parameters processing. This bit is analyzed with APP_INPUT_AVAIL so to take effect write both. 0 - No action, the device waits for input parameters. 1 - Reset the device after input parameters processing complete. Default Value: 0
29	INPUT_AVAIL	Notify RAM application that input parameters are valid for processing: 0 - the input parameters are not available. 1 - the input parameters are available (ready) for processing. Default Value: 0
3 : 0	REQUEST	A request to ROM_BOOT FW to execute particular code. This field survives some resets, including a system reset: * 0 - No request (default). * 1 - ROM_BOOT to wait for DLM app (PC=0). * 2 - ROM_BOOT to wait for an OEM debug token. * 3 - ROM_BOOT to wait for a PROT_FW debug token. * 4, 5 - ignored by ROM_BOOT. * 6 - ROM_BOOT to launch DLM app which has been downloaded by DFU. * 7 - ROM_BOOT to respond to DFU with DLM app status. Other: ignored by ROM_BOOT. Default Value: 0

11.1.28 BOOT_DLM_CTL2

Debug Control Register 2

Address: 0x42200408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	APP_CTL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	APP_CTL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	APP_CTL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	APP_CTL [31:24]							

Bits	Name	Description
31 : 0	APP_CTL	Address of application descriptor or debug certificate depends on DEBUG_TST_CTL.REQUEST. The application descriptor provides info about RAM application and its parameters layout in the staging area to BootROM and RAM application itself Default Value: 0

11.1.29 BOOT_DLM_STATUS

Debug Status Register

Address: 0x4220040C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DEBUG_STATUS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	DEBUG_STATUS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	DEBUG_STATUS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	DEBUG_STATUS [31:24]							

Bits	Name	Description
31 : 0	DEBUG_STATUS	RAM application execution status. This status can be read by the debugger using Sys-AP or user application when RAM application completes with system reset. This field survives some resets, including a system reset. Default Value: 0

11.1.30 RES_SOFT_CTL

Soft Reset Trigger Register

Address: 0x42200410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							R
Name	None [7:1]							TRIGGER_-SOFT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TRIGGER_SOFT	Triggers a soft reset. The reset clears this bit. Default Value: 0

11.1.31 BOOT_STATUS

Boot Execution Status Register

Address: 0x42200418

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DEBUG_STATUS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	DEBUG_STATUS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	DEBUG_STATUS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	DEBUG_STATUS [31:24]							

Bits	Name	Description
31 : 0	DEBUG_STATUS	Boot execution status. This status register can be used for communication between ROM_BOOT and User Application. This status can be read by the debugger using Sys-AP or User Application. This field survives some resets, including a system reset. Default Value: 0

11.1.32 BOOT_ENTRY

Warm Boot Entry Address

Address: 0x42200430

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	WARM_BOOT_ENTRY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	WARM_BOOT_ENTRY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	WARM_BOOT_ENTRY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	WARM_BOOT_ENTRY [31:24]							

Bits	Name	Description
31 : 0	WARM_BOOT_ENTRY	Warm boot entry point. This status register can be used for communication between 2 software application before/after DS-RAM, DS-OFF or soft reset. This field survives low voltage resets, including a system reset. Default Value: 0

11.1.33 PWR_HIB_WAKE_CTL

Hibernate Wakeup Mask Register

Address: 0x422008A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				A			
Name	None [7:4]				HIB_WAKE_SRC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	A	A	None					
Name	HIB_WAKE_WDT	HIB_WAKE_RTC	None [29:24]					

Bits	Name	Description
31	HIB_WAKE_WDT	When set, HIBERNATE will wakeup for a pending WDT interrupt. Default Value: 0
30	HIB_WAKE_RTC	When set, HIBERNATE will wakeup for a pending RTC interrupt. Default Value: 0
3 : 0	HIB_WAKE_SRC	When set, HIBERNATE will wakeup for the assigned source. Default Value: 0

11.1.34 PWR_HIB_WAKE_CTL2

Hibernate Wakeup Polarity Register

Address: 0x422008A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				A			
Name	None [7:4]				HIB_WAKE_SRC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	HIB_WAKE_SRC	Each bit selects the polarity for the corresponding HIBERNATE wakeup source. 0: Wakes when unmasked input is 0. 1: Wakes when unmasked input is 1. Default Value: 0

11.1.35 PWR_HIB_WAKE_CAUSE

Hibernate Wakeup Cause Register

Address: 0x422008AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C			
HW Access	None				A			
Name	None [7:4]				HIB_WAKE_SRC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C	RW1C	None					
HW Access	A	A	None					
Name	HIB_WAKE_WDT	HIB_WAKE_RTC	None [29:24]					

Bits	Name	Description
31	HIB_WAKE_WDT	Indicates WDT wakeup cause. The WDT interrupt must be cleared before this bit can be cleared. Default Value: 0
30	HIB_WAKE_RTC	Indicates RTC wakeup cause. The RTC interrupt must be cleared before this bit can be cleared. Default Value: 0
3 : 0	HIB_WAKE_SRC	Each bit indicates a HIBERNATE wakeup cause. For each bit, writing a 1 clears the cause flag. Default Value: 0

11.1.36 PWR_CTL

Power Mode Control

Address: 0x42201000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	None		R	
HW Access	None		RW	RW	None		RW	
Name	None [7:6]		LP-M_READY	DEBUG_-SESSION	None [3:2]		POWER_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	LPM_READY	Indicates whether certain low power functions are ready. The low current circuits take longer to startup after XRES, HIBERNATE wakeup, or supply supervision reset wakeup than the normal mode circuits. HIBERNATE mode may be entered regardless of this bit. 0: If a low power circuit operation is requested, it will stay in its normal operating mode until it is ready. If DEEPSLEEP is requested by all processors WFI/WFE, the device will instead enter SLEEP. When low power circuits are ready, device will automatically enter the originally requested mode. 1: Normal operation. DEEPSLEEP and low power circuits operate as requested in other registers. Default Value: 0
4	DEBUG_SESSION	Indicates whether a debug session is active (CDBGPWRUPREQ signal is 1) Default Value: 0 **0x0: NO_SESSION :** No debug session active **0x1: SESSION_ACTIVE :** Debug session is active. Power modes behave differently to keep the debug session active, and current consumption may be higher than datasheet specification.
1 : 0	POWER_MODE	Current power mode of the device. Note that this field cannot be read in all power modes. Default Value: 0

11.1.36 PWR_CTL (continued)

0x0: RESET :

System is resetting.

0x1: ACTIVE :

CPU is running.

0x2: SLEEP :

CPUs not running. Peripherals may be running.

0x3: DEEPSLEEP :

Main high-frequency clock is off; low speed clocks are available. Communication interface clocks may be present.

11.1.37 PWR_CTL2

Power Mode Control 2

Address: 0x42201004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	R	RW
HW Access	None			A	None	A	RW	A
Name	None [7:5]			DPS-LP_REG_DIS	None	LIN-REG_LP-MODE	LIN-REG_OK	LIN-REG_DIS

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None			RW
HW Access	None			A	None			A
Name	None [15:13]			NWELL_REG_DIS	None [11:9]			RET_REG_DIS

Bits	23	22	21	20	19	18	17	16
SW Access	None		R	RW	None		R	RW
HW Access	None		RW	A	None		RW	A
Name	None [23:22]		REFVBUF_OK	REFVBUF_DIS	None [19:18]		REFV_OK	REFV_DIS

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW1C	None	RW	RW	RW	None	
HW Access	A	A	None	A	A	A	None	
Name	PLL_LS_BYPASS	FREEZE_DPSLP	None	BGREF_LP MODE	POR-BOD_LP-MODE	REFI_LP-MODE	None [25:24]	

Bits	Name	Description
31	PLL_LS_BYPASS	Bypass level shifter inside the PLL. 0: Do not bypass the level shifter. This setting is ok for all operational modes and vccd target voltage. 1: Bypass the level shifter. This may reduce jitter on the PLL output clock, but can only be used when vccd is targeted to 1.1V nominal. Otherwise, it can result in clock degradation and static current. Default Value: 0
30	FREEZE_DPSLP	Controls whether mode and state of GPIOs and SIOs in the system are frozen. This is intended to be used as part of the DEEPSLEEP-RAM and DEEPSLEEP-OFF entry and exit sequences. It is set by HW while entering DEEPSLEEP-RAM and DEEPSLEEP-OFF modes. Writing a 1 clears freeze and GPIOs and SIOs resume normal operation. Default Value: 0

11.1.37 PWR_CTL2 (continued)

28	BGREF_LPMODE	Control the circuit-level power mode of the Bandgap Reference circuits for higher operating modes than DEEPSLEEP. This selects a second set of bandgap voltage and current generation circuits that are optimized for low current consumption. The low current circuits are automatically used in DEEPSLEEP mode regardless of this bit. The value in this register is ignored and higher-current mode is used until LPM_READY==1. After this bit is set, the Active Reference circuit can be disabled to reduce current (ACT_REF_DIS=0). Firmware is responsible to enable the Active Reference and ensure ACT_REF_OK==1 before changing back to higher current mode. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. 0: Bandgap Reference uses the normal settings. 1: Bandgap Reference uses the low power DeepSleep circuits. Power supply rejection is reduced to save current. Default Value: 0
27	PORBOD_LPMODE	Control the power mode of the POR/BOD circuits. The value in this register is ignored and normal mode is used until LPM_READY==1. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. 0: POR/BOD circuits operate in normal mode. 1: POR/BOD circuits operate in low power mode. Response time is reduced to save current. Default Value: 0
26	REFI_LPMODE	Control the power mode of the reference current generator. The value in this register is ignored and normal mode is used until LPM_READY==1. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. 0: Current reference generator operates in normal mode. 1: Current reference generator operates in low power mode. Response time is reduced to save current. Default Value: 0
21	REFVBUF_OK	Indicates that the voltage reference buffer is ready. Due to synchronization delays, it may take two IMO clock cycles for hardware to clear this bit after asserting REFVBUF_DIS=1. Default Value: 0
20	REFVBUF_DIS	Disable the voltage reference buffer. Firmware should only disable the buffer when there is no connected circuit that is using it. SRSS circuits that require it are the PLL and ECO. Circuits outside the SRSS may use the buffer. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. Default Value: 0
17	REFV_OK	Indicates that the normal mode of the voltage reference is ready. Default Value: 0
16	REFV_DIS	Disables the voltage reference. This disables the Active voltage reference. Firmware must ensure that LPM_READY==1 and BGREF_LPMODE==1 for at least 1us before disabling the Active Reference. When enabling the Active Reference, use REFV_OK indicator to know when it is ready. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. Default Value: 0
12	NWELL_REG_DIS	Explicitly disable the Nwell regulator. This register should normally be zero, except for special sequences provided by Infineon to use a different regulator. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. 0: Nwell Regulator is on. Hardware disables it automatically for internal sequences, including for HIBERNATE and XRES low power modes. Hardware keeps the Nwell Regulator enabled during ACTIVE/SLEEP modes, so it is ready to enter DEEPSLEEP at any time. 1: Nwell Regulator is explicitly disabled. Only use this for special cases when another source supplies vnwell during DEEPSLEEP mode. This setting is only legal when another source supplies vnwell, but there is no special hardware protection for this case. Default Value: 0

11.1.37 PWR_CTL2 (continued)

8	RET_REG_DIS	Explicitly disable the Retention regulator. This field should normally be zero, except for special sequences provided by Infineon to use a different regulator. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. 0: Retention Regulator is not explicitly disabled. Hardware disables it automatically for internal sequences, including for HIBERNATE and XRES low power modes. Hardware keeps the Retention Regulator enabled during ACTIVE/SLEEP modes, so it is ready to enter DEEPSLEEP at any time. 1: Retention Regulator is explicitly disabled. Only use this for special cases when another source supplies vccret during DEEPSLEEP mode. This setting is only legal when another source supplies vccret, but there is no special hardware protection for this case. Default Value: 0
4	DPSLP_REG_DIS	Explicity disable the DeepSleep regulator, including circuits shared with the Active Regulator. This register must not be set except as part of an Infineon-provided sequence or API. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. 0: DeepSleep Regulator is not explicitly disabled. This is the normal setting, and hardware automatically controls the DeepSleep regulator for most sequences, including for HIBERNATE and XRES low power modes. This setting must be used if the Active Linear Regulator is used, because some circuitry is shared. 1: DeepSleep Regulator is explicitly disabled. Only use this for special cases as part of an Infineon-provided handoff to another supply source. For example, this setting may be used when another source supplies vccdpslp during DEEPSLEEP mode and the Active Linear Regulator is not usedfor ACTIVE/SLEEP modes. Default Value: 0
2	LINREG_LPMODE	Control the power mode of the Linear Regulator. The value in this register is ignored and normal mode is used until LPM_READY==1. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. 0: Linear Regulator operates in normal mode. 1: Linear Regulator operates in low power mode. Load current capability is reduced, and firmware must ensure the current is kept within the limit. Default Value: 0
1	LINREG_OK	Status of the linear Core Regulator. Default Value: 0
0	LINREG_DIS	Explicitly disable the linear Core Regulator. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. 0: Linear Core Regulator is not explicitly disabled. Hardware disables it automatically for internal sequences, including for DEEPSLEEP, HIBERNATE, and XRES low power modes. 1: Linear Core Regulator is explicitly disabled. Only use this for special cases when another source supplies vccd during ACTIVE and SLEEP modes. This setting is only legal when another source supplies vccd, but there is no special hardware protection for this case. Default Value: 0

11.1.38 PWR_HIBERNATE

HIBERNATE Mode Register

Address: 0x42201008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	TOKEN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	UNLOCK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW	RW	RW	None
HW Access	A				A	A	A	None
Name	POLARITY_HIBPIN [23:20]				MASK_HIB-WDT	MASK_HI-BALARM	FREEZE	None

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW1S	RW1S	None	RW			
HW Access	A	R	A	None	A			
Name	HIBER-NATE	HIBER-NATE_DIS-ABLE	SENSE_-MODE	None	MASK_HIBPIN [27:24]			

Bits	Name	Description
31	HIBERNATE	Firmware sets this bit to enter HIBERNATE mode. The system will enter HIBERNATE mode immediately after writing to this bit and will wakeup only in response to XRES or WAKEUP. Both UNLOCK and FREEZE must have been set correctly in a previous write operations. Otherwise, it will not enter HIBERNATE. External supplies must have been stable for 250us before entering HIBERNATE mode. Default Value: 0
30	HIBERNATE_DISABLE	Hibernate disable bit. 0: Normal operation, HIBERNATE works as described 1: Further writes to this register are ignored Note: This bit is a write-once bit until the next reset. Avoid changing any other bits in this register while disabling HIBERNATE mode. Also, it is recommended to clear the UNLOCK code, if it was previously written.. Default Value: 0
29	SENSE_MODE	Power mode when wakeups are sensitive. The default of this field is 0 for software compatibility with other products. It is recommended to set this field to 1 for new/updated software. 0: Wakeups are sensitive only during HIBERNATE mode. A wakeup pulse that comes just before HIBERNATE entry may be missed. Backward compatible. 1: Wakeups are sensitive in HIBERNATE and higher modes. Before entering HIBERNATE, software must clear all unmasked, pending wakeups in PWR_HIB_WAKE_CAUSE register. An unmasked, pending wakeup causes HIBERNATE wakeup, even if it was pending from before HIBERNATE entry. This prevents missed wakeups. Default Value: 0

11.1.38 PWR_HIBERNATE (continued)

27 : 24	MASK_HIBPIN	Reserved. Use PWR_HIB_WAKE_CTL.HIB_WAKE_SRC for new designs. Default Value: 0
23 : 20	POLARITY_HIBPIN	Reserved. Use PWR_HIB_WAKE_CTL2.HIB_WAKE_SRC for new designs. Default Value: 0
19	MASK_HIBWDT	Reserved. Use PWR_HIB_WAKE_CTL.HIB_WAKE_WDT for new designs. Default Value: 0
18	MASK_HIBALARM	Reserved. Use PWR_HIB_WAKE_CTL.HIB_WAKE_RTC for new designs. Default Value: 0
17	FREEZE	Controls whether mode and state of GPIOs and SIOs in the system are frozen. This is intended to be used as part of the HIBERNATE entry and exit sequences. When entering HIBERNATE mode, the first write instructs DEEPSLEEP peripherals that they cannot ignore the upcoming freeze command. This occurs even in the illegal condition where UNLOCK is not set. If UNLOCK and HIBERNATE are properly set, the IOs actually freeze on the second write. Supply supervision is disabled during HIBERNATE mode. HIBERNATE peripherals ignore resets (excluding XRES) while FREEZE==1. Default Value: 0
15 : 8	UNLOCK	This byte must be set to 0x3A for FREEZE or HIBERNATE fields to operate. Any other value in this register will cause FREEZE/HIBERNATE to have no effect, except as noted in the FREEZE description. Default Value: 0
7 : 0	TOKEN	Contains a 8-bit token that is retained through a HIBERNATE/WAKEUP sequence that can be used by firmware to differentiate WAKEUP from a general RESET event. Note that waking up from HIBERNATE using XRES will reset this register. Default Value: 0

11.1.39 PWR_LVD_CTL

High Voltage / Low Voltage Detector (HVLVD) Configuration Register

Address: 0x42201020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW			
HW Access	R	R			R			
Name	HVL-VD1_EN	HVLVD1_SRCSEL [6:4]			HVLVD1_TRIPSEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW	RW	
HW Access	None					R	R	
Name	None [23:19]					HVL-VD1_AC-TION	HVLVD1_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
18	HVLVD1_ACTION	Action taken when the threshold is crossed in the programmed directions(s) Default Value: 0 **0x0: INTERRUPT :** Generate an interrupt **0x1: FAULT :** Generate a fault
17 : 16	HVLVD1_EDGE_SEL	Sets which edge(s) will trigger an action when the threshold is crossed. Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge

11.1.39 PWR_LVD_CTL (continued)

		0x2: FALLING : Falling edge **0x3: BOTH :** Both rising and falling edges
7	HVLVD1_EN	Enable HVLVD1 voltage monitor. HVLVD1 does not function during DEEPSLEEP, but it automatically returns to its configured setting after DEEPSLEEP wakeup. Do not change other HVLVD1 settings when enabled. Default Value: 0
6 : 4	HVLVD1_SRCSEL	Source selection for HVLVD1 Default Value: 0 **0x0: VDDD :** Select VDDD **0x1: AMUXBUSA :** Select AMUXBUSA (VDDD branch) **0x2: RESERVED :** Reserved. **0x3: RESERVED :** Reserved. **0x4: AMUXBUSB :** Select AMUXBUSB (VDDD branch)
3 : 0	HVLVD1_TRIPSEL	Threshold selection for HVLVD1. Disable the detector (HVLVD1_EN=0) before changing the threshold. 0: rise=1.225V (nom), fall=1.2V (nom) 1: rise=1.425V (nom), fall=1.4V (nom) 2: rise=1.625V (nom), fall=1.6V (nom) 3: rise=1.825V (nom), fall=1.8V (nom) 4: rise=2.025V (nom), fall=2V (nom) 5: rise=2.125V (nom), fall=2.1V (nom) 6: rise=2.225V (nom), fall=2.2V (nom) 7: rise=2.325V (nom), fall=2.3V (nom) 8: rise=2.425V (nom), fall=2.4V (nom) 9: rise=2.525V (nom), fall=2.5V (nom) 10: rise=2.625V (nom), fall=2.6V (nom) 11: rise=2.725V (nom), fall=2.7V (nom) 12: rise=2.825V (nom), fall=2.8V (nom) 13: rise=2.925V (nom), fall=2.9V (nom) 14: rise=3.025V (nom), fall=3.0V (nom) 15: rise=3.125V (nom), fall=3.1V (nom) Default Value: 0

11.1.40 CLK_PATH_SELECT0

Clock Path Select Register

Address: 0x42201200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					PATH_MUX [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	PATH_MUX	Selects a source for clock PATH. *Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. It takes four cycles of the originally selected clock to switch away from it. Do not disable the original clock during this time. Default Value: 0* **0x0: IMO :** IMO - Internal R/C Oscillator **0x1: EXTCLK :** EXTCLK - External Clock Pin **0x2: ECO :** ECO - External-Crystal Oscillator **0x3: ALTHF :** ALTHF - Alternate High-Frequency clock input (product-specific clock) **0x4: DSI_MUX :** DSI_MUX - Output of DSI mux for this path. Using a DSI source directly as root of HFCLK will result in undefined behavior.

11.1.40 CLK_PATH_SELECT0 (continued)

0x5: LPECO :

LPECO - Low-Power External-Crystal Oscillator

0x6: IHO :

IHO - Internal High-speed Oscillator

11.1.41 CLK_ROOT_SELECT0

Clock Root Select Register

Address: 0x42201240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW			
HW Access	None		R		R			
Name	None [7:6]		ROOT_DIV [5:4]		ROOT_MUX [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				ROOT_DIV_INT [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	A	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	Enable for this clock root. All clock roots default to disabled (ENABLE==0) except HFCLK0, which cannot be disabled. Default Value: 0
11 : 8	ROOT_DIV_INT	Selects predivider value for this clock root and DSI input. This divider is after DIRECT_MUX. For products with DSI, the output of this mux is routed to DSI for use as a signal. For products with clock supervision, the output of this mux is the monitored clock for CSV_HF. Default Value: 0 **0x0: NO_DIV :** Transparent mode, feed through selected clock source w/o dividing. **0x1: DIV_BY_2 :** Divide selected clock source by 2 **0x2: DIV_BY_3 :** Divide selected clock source by 3 **0x3: DIV_BY_4 :** Divide selected clock source by 4

11.1.41 CLK_ROOT_SELECT0 (continued)

		0x4: DIV_BY_5 : Divide selected clock source by 5 **0x5: DIV_BY_6 :** Divide selected clock source by 6 **0x6: DIV_BY_7 :** Divide selected clock source by 7 **0x7: DIV_BY_8 :** Divide selected clock source by 8 **0x8: DIV_BY_9 :** Divide selected clock source by 9 **0x9: DIV_BY_10 :** Divide selected clock source by 10 **0xa: DIV_BY_11 :** Divide selected clock source by 11 **0xb: DIV_BY_12 :** Divide selected clock source by 12 **0xc: DIV_BY_13 :** Divide selected clock source by 13 **0xd: DIV_BY_14 :** Divide selected clock source by 14 **0xe: DIV_BY_15 :** Divide selected clock source by 15 **0xf: DIV_BY_16 :** Divide selected clock source by 16
5 : 4	ROOT_DIV	Obsolete. Do not use in new designs. Default Value: 0

11.1.41 CLK_ROOT_SELECT0 (continued)

3 : 0	ROOT_MUX	Selects a clock path for HFCLK and SRSS DSI input . The output of this mux goes to the direct mux (see CLK_DIRECT_SELECT). Use CLK_SELECT_PATH[i] to configure the desired path. The number of clock paths is product-specific, and selecting an unimplemented path is not supported. Some paths may have FLL or PLL available (product-specific), and the control and bypass mux selections of these are in other registers. Configure the FLL using CLK_FLL_CONFIG register. Configure a PLL using the related CLK_PLL_CONFIG[k] register. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. It takes four cycles of the originally selected clock to switch away from it. Do not disable the original clock during this time. Default Value: 0 **0x0: PATH0 :** Select PATH0 **0x1: PATH1 :** Select PATH1 **0x2: PATH2 :** Select PATH2 **0x3: PATH3 :** Select PATH3 **0x4: PATH4 :** Select PATH4 **0x5: PATH5 :** Select PATH5 **0x6: PATH6 :** Select PATH6 **0x7: PATH7 :** Select PATH7 **0x8: PATH8 :** Select PATH8 **0x9: PATH9 :** Select PATH9 **0xa: PATH10 :** Select PATH10 **0xb: PATH11 :** Select PATH11

11.1.41 CLK_ROOT_SELECT0 (continued)

0xc: PATH12 :

Select PATH12

0xd: PATH13 :

Select PATH13

0xe: PATH14 :

Select PATH14

0xf: PATH15 :

Select PATH15

11.1.42 CLK_DIRECT_SELECT0

Clock Root Direct Select Register

Address: 0x42201280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							A
Name	None [15:9]							DI-RECT_MUX

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	DIRECT_MUX	Direct selection mux that allows IMO to bypass most of the clock mux structure. For products with multiple regulators, this mux can be used to reduce current without requiring significant re-configuration of the clocking network. The default value of HFCLK<0>==ROOT_MUX, and the default value for other clock trees is product-specific. Default Value: 1 **0x0: IMO :** Select IMO **0x1: ROOT_MUX :** Select ROOT_MUX selection

11.1.43 CSV_HF_CSV0_REF_CTL

Clock Supervision Reference Control

Address: 0x42201400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	STARTUP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	STARTUP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	CSV_EN	CSV_ACTION	None [29:24]					

Bits	Name	Description
31	CSV_EN	Enables clock supervision, both frequency and loss. CSV in Active domain: Clock supervision is reset during DeepSleep and Hibernate modes. When enabled it begins operating automatically after a DeepSleep wakeup, but it must be reconfigured after Hibernate wakeup. CSV in DeepSleep domain: Clock supervision is reset during Hibernate mode. It must be reconfigured after Hibernate wakeup. A CSV error detection is reported to the Fault structure, or instead it can generate a power reset. Default Value: 0
30	CSV_ACTION	Specifies the action taken when an anomaly is detected on the monitored clock. CSV in DeepSleep domain always do a Fault report (which also wakes up the system). Default Value: 0 **0x0: FAULT :** Generate a fault **0x1: RESET :** Cause a power reset. This should only be used for clk_hf0.

11.1.43 CSV_HF_CSV0_REF_CTL (continued)

15 : 0	STARTUP	Startup delay time -1 (in reference clock cycles), after enable or DeepSleep wakeup, from reference clock start to monitored clock start. At a minimum (both clocks running): STARTUP >= (PERIOD +3) * FREQ_RATIO - UPPER, with FREQ_RATIO = (Reference frequency / Monitored frequency) On top of that the actual clock startup delay and the margin for accuracy of both clocks must be added. Default Value: 0

11.1.44 CSV_HF_CSV0_REF_LIMIT

Clock Supervision Reference Limits

Address: 0x42201404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LOWER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	LOWER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	UPPER [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	UPPER [31:24]							

Bits	Name	Description
31 : 16	UPPER	Cycle time upper limit. Set the upper limit -1, in reference clock cycles, before (or same time) the next monitored clock event must happen. If a monitored clock event does not happen before this limit is reached, or does not happen at all (clock loss), a CSV error is detected. Default Value: 0
15 : 0	LOWER	Cycle time lower limit. Set the lower limit -1, in reference clock cycles, before the next monitored clock event is allowed to happen. If a monitored clock event happens before this limit is reached a CSV error is detected. LOWER must be at least 1 less than UPPER. In case the clocks are asynchronous LOWER must be at least 3 less than UPPER. Default Value: 0

11.1.45 CSV_HF_CSV0_MON_CTL

Clock Supervision Monitor Control

Address: 0x42201408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period time. Set the Period -1, in monitored clock cycles, before the next monitored clock event happens. PERIOD <= (UPPER+1) / FREQ_RATIO -1, with FREQ_RATIO = (Reference frequency / Monitored frequency) In case the clocks are asynchronous: PERIOD <= UPPER / FREQ_RATIO -1 Additionally margin must be added for accuracy of both clocks. Default Value: 0

11.1.46 CLK_SELECT

Clock selection register

Address: 0x42201500

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					A		
Name	None [7:3]					LFCLK_SEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			
HW Access	R	R			R			
Name	PUMP_ENABLE	PUMP_DIV [14:12]			PUMP_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	PUMP_ENABLE	Enable the pump clock. PUMP_ENABLE and the PUMP_SEL mux are not glitch-free to minimize side-effects, avoid changing the PUMP_SEL and PUMP_DIV while changing PUMP_ENABLE. To change the settings, do the following: 1) If the pump clock is enabled, write PUMP_ENABLE=0 without changing PUMP_SEL and PUMP_DIV. 2) Change PUMP_SEL and PUMP_DIV to desired settings with PUMP_ENABLE=0. 3) Write PUMP_ENABLE=1 without changing PUMP_SEL and PUMP_DIV. Default Value: 0
14 : 12	PUMP_DIV	Division ratio for PUMPCLK. Uses selected PUMP_SEL clock as the source. Default Value: 0 **0x0: NO_DIV :** Transparent mode, feed through selected clock source w/o dividing. **0x1: DIV_BY_2 :** Divide selected clock source by 2 **0x2: DIV_BY_4 :** Divide selected clock source by 4

11.1.46 CLK_SELECT (continued)

		0x3: DIV_BY_8 : Divide selected clock source by 8 **0x4: DIV_BY_16 :** Divide selected clock source by 16
11 : 8	PUMP_SEL	Selects clock PATH, where k=PUMP_SEL. The output of this mux goes to the PUMP_DIV to make PUMPCLK Each product has a specific number of available clock paths. Selecting a path that is not implemented on a product will result in undefined behavior. Note that this is not a glitch free mux. Default Value: 0
2 : 0	LFCLK_SEL	Select source for LFCLK. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. Writes to this field are ignored unless the WDT is unlocked using WDT_LOCK register. It takes four cycles of the originally selected clock to switch away from it. Do not disable the original clock during this time. Default Value: 0 **0x0: ILO :** ILO - Internal Low-speed Oscillator **0x1: WCO :** WCO - Watch-Crystal Oscillator. Requires Backup domain to be present and properly configured (including external watch crystal, if used). **0x2: ALTLF :** ALTLF - Alternate Low-Frequency Clock. Capability is product-specific **0x3: PILO :** PILO - Precision ILO, if present. **0x4: ILO1 :** ILO1 - Internal Low-speed Oscillator #1, if present. **0x5: ECO_PRESCALER :** ECO_PRESCALER - External-Crystal Oscillator after prescaling, if present. Does not work in DEEPSLEEP or HIBERNATE modes. Intended for applications that operate in ACTIVE/SLEEP modes only. This option is only valid when ECO is present in the product. Not compatible with an clk_sys frequency <48MHz. **0x6: LPECO_PRESCALER :** LPECO_PRESCALER - Low-Power External-Crystal Oscillator after prescaling, if present. This choice works in ACTIVE/SLEEP/DEEPSLEEP modes. This option is only valid when LPECO is present in the product.

11.1.47 CLK_IMO_CONFIG

IMO Configuration

Address: 0x42201518

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	ENABLE	DPS-LP_EN-ABLE	None [29:24]					

Bits	Name	Description
31	ENABLE	Master enable for IMO oscillator. This bit must be high at all times for all functions to work properly. Hardware will automatically disable the IMO during HIBERNATE and XRES. It will automatically disable during DEEPSLEEP if DPSLP_ENABLE==0. Default Value: 1
30	DPSLP_ENABLE	Enable for IMO during DEEPSLEEP. This bit configures IMO behavior during DEEPSLEEP: 0: IMO is automatically disabled during DEEPSLEEP and enables upon wakeup; 1: IMO is kept enabled throughout DEEPSLEEP Default Value: 0

11.1.48 CLK_ECO_CONFIG

ECO Configuration Register

Address: 0x4220151C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	None
HW Access	None						R	None
Name	None [7:2]						AGC_EN	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None		RW	RW	None		
HW Access	R	None		RW1C	RW1C	None		
Name	ECO_EN	None [30:29]		ECO_DIV_ENABLE	ECO_DIV_-DISABLE	None [26:24]		

Bits	Name	Description
31	ECO_EN	Master enable for ECO oscillator. Configure the settings in CLK_ECO_CONFIG2 to work with the selected crystal, before enabling ECO. Default Value: 0
28	ECO_DIV_ENABLE	ECO prescaler enable command (mutually exclusive with ECO_DIV_DISABLE). ECO Prescaler only works in ACTIVE and SLEEP modes. SW sets this field to '1' to enable the divider and HW sets this field to '0' to indicate that divider enabling has completed. When the divider is enabled, its integer and fractional counters are initialized to "0". If a divider is to be re-enabled using different integer and fractional divider values, the SW should follow these steps: 0: Disable the divider using the ECO_DIV_DISABLE field. 1: Configure CLK_ECO_PRESCALE registers. 2: Enable the divider using the ECO_DIV_ENABLE field. HW sets the ECO_DIV_ENABLE field to '0' when the enabling is performed and HW set CLK_ECO_PRESCALER.ENABLED to '1' when the enabling is performed. Default Value: 0
27	ECO_DIV_DISABLE	ECO prescaler disable command (mutually exclusive with ECO_DIV_ENABLE). SW sets this field to '1' and HW sets this field to '0'. HW sets ECO_DIV_DISABLE field to '0' immediately and HW sets CLK_ECO_PRESCALE.ECO_DIV_EN field to '0' immediately. Default Value: 0

11.1.48 CLK_ECO_CONFIG (continued)

1	AGC_EN	Automatic Gain Control (AGC) enable. When set, the oscillation amplitude is controlled to the level selected by CLK_ECO_CONFIG2.ATRIM. When low, the amplitude is not explicitly controlled and can be as high as the vddd supply. WARNING: use care when disabling AGC because driving a crystal beyond its rated limit can permanently damage the crystal. Default Value: 1

11.1.49 CLK_ECO_PRESCALE

ECO Prescaler Configuration Register

Address: 0x42201520

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							ECO_DIV_ENABLED

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ECO_FRAC_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ECO_INT_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						ECO_INT_DIV [25:24]	

Bits	Name	Description
25 : 16	ECO_INT_DIV	10-bit integer value allows for ECO frequencies up to 33.55MHz. Subtract one from the desired divide value when writing this field. For example, to divide by 1, write ECO_INT_DIV=0. Do not change this setting when ECO Prescaler is enabled. Default Value: 0
15 : 8	ECO_FRAC_DIV	8-bit fractional value, sufficient to get prescaler output within the +/-65ppm calibration range. Do not change this setting when ECO Prescaler is enabled. Default Value: 0
0	ECO_DIV_ENABLED	ECO prescaler enabled. HW sets this field to '1' as a result of an CLK_ECO_CONFIG.ECO_DIV_ENABLE command. HW sets this field to '0' as a result on a CLK_ECO_CONFIG.ECO_DIV_DISABLE command. ECO prescaler is incompatible with DEEPSLEEP modes, and firmware must disable it before entering DEEPSLEEP. Default Value: 0

11.1.50 CLK_ECO_STATUS

ECO Status Register

Address: 0x42201524

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						ECO_READY	ECO_OK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	ECO_READY	Indicates the ECO internal oscillator circuit has had enough time to fully stabilize. This is the output of a counter since ECO was enabled, and it does not check the ECO output. It is recommended to also confirm ECO_OK==1. Default Value: 0
0	ECO_OK	Indicates the ECO internal oscillator circuit has sufficient amplitude. It may not meet the PPM accuracy or duty cycle spec. Default Value: 0

11.1.51 CLK_FLL_CONFIG

FLL Configuration Register

Address: 0x42201530

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FLL_MULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	FLL_MULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						FLL_MULT [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						RW
HW Access	R	None						R
Name	FLL_ENABLE	None [30:25]						FLL_OUTPUT_DIV

Bits	Name	Description
31	FLL_ENABLE	Master enable for FLL. The FLL requires firmware sequencing when enabling and disabling. Hardware handles sequencing automatically when entering/exiting DEEPSLEEP. To enable the FLL, use the following sequence: 1) Configure FLL and CCO settings. Do not modify CLK_FLL_CONFIG3.BYPASS_SEL (must be AUTO) or CLK_FLL_CONFIG.FLL_ENABLE (must be 0). 2) Enable the CCO by writing CLK_FLL_CONFIG4.CCO_ENABLE=1 3) Wait until CLK_FLL_STATUS.CCO_READY==1. 4) Ensure the reference clock has stabilized. 5) Write FLL_ENABLE=1. 6) Optionally wait until CLK_FLL_STATUS.LOCKED==1. The hardware automatically changes to the FLL output when LOCKED==1. To disable the FLL, use the following sequence: 1) Write CLK_FLL_CONFIG3.BYPASS_SEL=FLL_REF. 2) Read CLK_FLL_CONFIG3.BYPASS_SEL to ensure the write completes (read is not optional). 3) Wait at least ten cycles of either FLL reference clock or FLL output clock, whichever is slower. 4) Disable FLL with FLL_ENABLE=0. 5) Disable the CCO by writing CLK_FLL_CONFIG4.CCO_ENABLE=0. 6) Write CLK_FLL_CONFIG3.BYPASS_SEL=AUTO. 7) Read CLK_FLL_CONFIG3.BYPASS_SEL to ensure the write completes (read is not optional). 8) Wait three cycles of FLL reference clock. 0: Block is powered off 1: Block is powered on Default Value: 0

11.1.51 CLK_FLL_CONFIG (continued)

24	FLL_OUTPUT_DIV	Control bits for Output divider. Set the divide value before enabling the FLL, and do not change it while FLL is enabled. 0: no division 1: divide by 2 Default Value: 1
17 : 0	FLL_MULT	Multiplier to determine CCO frequency in multiples of the frequency of the selected reference clock (Fref). Ffll = (FLL_MULT) * (Fref / REFERENCE_DIV) / (OUTPUT_DIV+1) Default Value: 0

11.1.52 CLK_FLL_CONFIG2

FLL Configuration Register 2

Address: 0x42201534

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FLL_REF_DIV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			FLL_REF_DIV [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	LOCK_TOL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	UPDATE_TOL [31:24]							

Bits	Name	Description
31 : 24	UPDATE_TOL	Update tolerance sets the error threshold for when the FLL will update the CCO frequency settings. The update tolerance is the allowed difference between the count value for the ideal formula and the measured value. UPDATE_TOL should be less than LOCK_TOL. Default Value: 0
23 : 16	LOCK_TOL	Lock tolerance sets the error threshold for when the FLL output is considered locked to the reference input. A high tolerance can be used to lock more quickly or allow less accuracy. The tolerance is the allowed difference between the count value for the ideal formula and the measured value. 0: tolerate error of 1 count value 1: tolerate error of 2 count values ... 255: tolerate error of 256 count values Default Value: 2
12 : 0	FLL_REF_DIV	Control bits for reference divider. Set the divide value before enabling the FLL, and do not change it while FLL is enabled. 0: illegal (undefined behavior) 1: divide by 1 ... 8191: divide by 8191 Default Value: 1

11.1.53 CLK_FLL_CONFIG3

FLL Configuration Register 3

Address: 0x42201538

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	FLL_LF_PGAIN [7:4]				FLL_LF_IGAIN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SETTLING_COUNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			R				
Name	None [23:21]			SETTLING_COUNT [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW		None			
HW Access	None		R		None			
Name	None [31:30]		BYPASS_SEL [29:28]		None [27:24]			

Bits	Name	Description
29 : 28	BYPASS_SEL	Bypass mux located just after FLL output. This register can be written while the FLL is enabled. When changing BYPASS_SEL, do not turn off the reference clock or CCO clock for five cycles (whichever is slower). Whenever BYPASS_SEL is changed, it is required to read CLK_FLL_-CONFIG3 to ensure the change takes effect. Default Value: 0 **0x0: AUTO :** Automatic using lock indicator. When unlocked, automatically selects FLL reference input (bypass mode). When locked, automatically selects FLL output. This can allow some processing to occur while the FLL is locking, such as after DEEPSLEEP wakeup. It is incompatible with clock supervision, because the frequency changes based on the lock signal. **0x1: LOCKED_OR_NOTHING :** Similar to AUTO, except the clock is gated off when unlocked. This is compatible with clock supervision, because the supervisors allow no clock during startup (until a timeout occurs), and the clock targets the proper frequency whenever it is running. **0x2: FLL_REF :** Select FLL reference input (bypass mode). Ignores lock indicator **0x3: FLL_OUT :** Select FLL output. Ignores lock indicator.

11.1.53 CLK_FLL_CONFIG3 (continued)

20 : 8	SETTLING_COUNT	Number of undivided reference clock cycles to wait after changing the CCO trim until the loop measurement restarts. A delay allows the CCO output to settle and gives a more accurate measurement. The default is tuned to an 8MHz reference clock since the IMO is expected to be the most common use case. 0: no settling time 1: wait one reference clock cycle ... 8191: wait 8191 reference clock cycles Default Value: 40
7 : 4	FLL_LF_PGAIN	FLL Loop Filter Gain Setting #2. The proportional gain is the sum of FLL_LF_IGAIN and FLL_LF_PGAIN. 0: 1/256 1: 1/128 2: 1/64 3: 1/32 4: 1/16 5: 1/8 6: 1/4 7: 1/2 8: 1.0 9: 2.0 10: 4.0 11: 8.0 >=12: illegal Default Value: 0
3 : 0	FLL_LF_IGAIN	FLL Loop Filter Gain Setting #1. The proportional gain is the sum of FLL_LF_IGAIN and FLL_LF_PGAIN. 0: 1/256 1: 1/128 2: 1/64 3: 1/32 4: 1/16 5: 1/8 6: 1/4 7: 1/2 8: 1.0 9: 2.0 10: 4.0 11: 8.0 >=12: illegal Default Value: 0

11.1.54 CLK_FLL_CONFIG4

FLL Configuration Register 4

Address: 0x4220153C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CCO_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					R		
Name	None [15:11]					CCO_RANGE [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	CCO_FREQ [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					RW
HW Access	R	R	None					RW
Name	CCO_EN-ABLE	CCO_HW_UP-DATE_DIS	None [29:25]					CCO_-FREQ

Bits	Name	Description
31	CCO_ENABLE	Enable the CCO. It is required to enable the CCO before using the FLL. 0: Block is powered off 1: Block is powered on Default Value: 0
30	CCO_HW_UPDATE_DIS	Disable CCO frequency update by FLL hardware 0: Hardware update of CCO settings is allowed. Use this setting for normal FLL operation. 1: Hardware update of CCO settings is disabled. Use this setting for open-loop FLL operation. Default Value: 0
24 : 16	CCO_FREQ	CCO frequency code. This is updated by HW when the FLL is enabled. It can be manually updated to use the CCO in an open loop configuration. The meaning of each frequency code depends on the range. Default Value: 0
10 : 8	CCO_RANGE	Frequency range of CCO Default Value: 0 **0x0: RANGE0 :** Target frequency is in range [48, 64) MHz **0x1: RANGE1 :** Target frequency is in range [64, 85) MHz

11.1.54 CLK_FLL_CONFIG4 (continued)

		0x2: RANGE2 : Target frequency is in range [85, 113) MHz **0x3: RANGE3 :** Target frequency is in range [113, 150) MHz **0x4: RANGE4 :** Target frequency is in range [150, 200] MHz
7 : 0	CCO_LIMIT	Maximum CCO offset allowed (used to prevent FLL dynamics from selecting an CCO frequency that the logic cannot support) Default Value: 0xFF

11.1.55 CLK_FLL_STATUS

FLL Status Register

Address: 0x42201540

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	RW1C	R
HW Access	None					RW	A	W
Name	None [7:3]					CCO_READY	UNLOCK_OCCURRED	LOCKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CCO_READY	This indicates that the CCO is internally settled and ready to use. Default Value: 0
1	UNLOCK_OCCURRED	This bit sets whenever the FLL is enabled and goes out of lock. This bit stays set until cleared by firmware. Note: When exiting Deep Sleep with FLL enabled, UNLOCK_OCCURRED will set. Therefore, after FLL successfully locks, FW should clear UNLOCK_OCCURRED flag to prevent a false positive that would indicate that FLL erroneously unlocked. Default Value: 0
0	LOCKED	FLL Lock Indicator Default Value: 0

11.1.56 CLK_ECO_CONFIG2

ECO Configuration Register 2

Address: 0x42201544

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				None	RW		
HW Access	R				None	R		
Name	ATRIM [7:4]				None	WDTRIM [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW			RW		RW	
HW Access	None	R			R		R	
Name	None	GTRIM [14:12]			RTRIM [11:10]		FTRIM [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14 : 12	GTRIM	Gain Trim - Startup time. Default Value: 0
11 : 10	RTRIM	Feedback resistor Trim Default Value: 0
9 : 8	FTRIM	Filter Trim - 3rd harmonic oscillation Default Value: 0
7 : 4	ATRIM	Amplitude trim to set the crystal drive level when ECO_CONFIG.AGC_EN=1. WARNING: use care when setting this field because driving a crystal beyond its rated limit can permanently damage the crystal. 0x0 - 150mV 0x1 - 175mV 0x2 - 200mV 0x3 - 225mV 0x4 - 250mV 0x5 - 275mV 0x6 - 300mV 0x7 - 325mV 0x8 - 350mV 0x9 - 375mV 0xA - 400mV 0xB - 425mV 0xC - 450mV 0xD - 475mV 0xE - 500mV 0xF - 525mV Default Value: 0

11.1.56 CLK_ECO_CONFIG2 (continued)

2 : 0	WDTRIM	Watch Dog Trim - Delta voltage below steady state level 0x0 - 50mV 0x1 - 75mV 0x2 - 100mV 0x3 - 125mV 0x4 - 150mV 0x5 - 175mV 0x6 - 200mV 0x7 - 225mV Default Value: 3

11.1.57 CLK_ILO_CONFIG

ILO Configuration

Address: 0x42201548

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							A
Name	None [7:1]							ILO_BACK-UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	A	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	Master enable for ILO. Writes to this field are ignored unless the WDT is unlocked using WDT_LOCK register. After enabling, it takes at most two cycles to reach the accuracy spec. Default Value: 1
0	ILO_BACKUP	If backup domain is present on this product, this register indicates that ILO should stay enabled for use by backup domain during XRES, HIBERNATE mode, and through power-related resets like BOD on VDDD/VCCD. Writes to this field are ignored unless the WDT is unlocked using WDT_LOCK register. 0: ILO turns off at XRES/BOD event or HIBERNATE entry. 1: ILO remains on if backup domain is present and powered even for XRES/BOD or HIBERNATE entry. Default Value: 0

11.1.58 CLK_TRIM_ILO_CTL

ILO Trim Register

Address: 0x4220154C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		A					
Name	None [7:6]		ILO_FTRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	ILO_FTRIM	IL0 frequency trims. LSB step size is 1.5% (typical) of the frequency. Default Value: 0x2C

11.1.59 CLK_MF_SELECT

Medium Frequency Clock Select Register

Address: 0x42201554

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					MFCLK_SEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MFCLK_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	Enable for MFCLK (clk_mf). When disabling clk_mf, do not disable the source until after 5 clk_mf periods. clk_mf continues to operate in DEEPSLEEP for compatible sources. Firmware must disable clk_mf before entering DEEPSLEEP if the source is not compatible with DEEPSLEEP mode. Default Value: 0
15 : 8	MFCLK_DIV	Divide selected clock source by (1+MFCLK_DIV). The output of this divider is MFCLK (clk_mf). Allows for integer divisions in the range [1, 256]. Do not change this setting while ENABLE==1. Default Value: 0
2 : 0	MFCLK_SEL	Select source for MFCLK (clk_mf). Note that not all products support all clock sources. Selecting a clock source that is not supported results in undefined behavior. Default Value: 0 **0x0: MFO :** MFO - Medium Frequency Oscillator. DEEPSLEEP compatibility is product-specific. See CLK_MFO_CONFIG for capability of this product. **0x1: ILO :** ILO - Internal Low-speed Oscillator. **0x2: WCO :** WCO - Watch-Crystal Oscillator, if present.

11.1.59 CLK_MF_SELECT (continued)

0x3: ALTLF :

ALTLF - Alternate Low-Frequency Clock. Capability is product-specific

0x4: PILO :

PILO - Precision ILO, if present.

0x5: ILO1 :

ILO1 - Internal Low-speed Oscillator #1, if present.

0x6: ECO_PRESCALER :

ECO_PRESCALER - External-Crystal Oscillator, if present, after prescaling in CLK_ECO_PRESCALE. Intended for applications that operate in ACTIVE/SLEEP modes only. Does not work in DEEPSLEEP mode.

0x7: LPECO :

LPECO - Low Power External Crystal Oscillator, if present.

11.1.60 CLK_MFO_CONFIG

MFO Configuration Register

Address: 0x42201558

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	ENABLE	DPS-LP_EN-ABLE	None [29:24]					

Bits	Name	Description
31	ENABLE	Enable for Medium Frequency Oscillator (MFO) to generate clk_mf. It is product-specific whether this is a separate component or implemented as a divided version of another clock (eg. IMO). Default Value: 1
30	DPSLP_ENABLE	Enable for MFO during DEEPSLEEP. This bit is ignored when ENABLE==0. When ENABLE==1: 0: MFO is automatically disabled during DEEPSLEEP and enables upon wakeup; 1: MFO is kept enabled throughout DEEPSLEEP Default Value: 0

11.1.61 CLK_IHO_CONFIG

IHO Configuration Register

Address: 0x42201560

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	Enable for Internal High-speed Oscillator (IHO) to generate clk_iho. Default Value: 1

11.1.62 CSV_REF_SEL

Select CSV Reference clock for Active domain

Address: 0x42201700

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					REF_MUX [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	REF_MUX	Selects a source for clock clk_ref_hf. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. It takes four cycles of the originally selected clock to switch away from it. Do not disable the original clock during this time. Default Value: 0 **0x0: IMO :** IMO - Internal R/C Oscillator **0x1: EXTCLK :** EXTCLK - External Clock Pin **0x2: ECO :** ECO - External-Crystal Oscillator **0x3: ALTHF :** ALTHF - Alternate High-Frequency clock input (product-specific clock) **0x4: IHO :** IHO - Internal High-speed Oscillator

11.1.63 CSV_LF_CSV_REF_CTL

Clock Supervision Reference Control

Address: 0x42201720

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	STARTUP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	CSV_EN	None [30:24]						

Bits	Name	Description
31	CSV_EN	Enables clock supervision, both frequency and loss. CSV in Active domain: Clock supervision is reset during DeepSleep and Hibernate modes. When enabled it begins operating automatically after a DeepSleep wakeup, but it must be reconfigured after Hibernate wakeup. CSV in DeepSleep domain: Clock supervision is reset during Hibernate mode. It must be reconfigured after Hibernate wakeup. CSV in Backup domain: Clock supervision operates during Hibernate mode, can be configured to wake from Hibernate, and continues operating during reboot. A CSV error detection is reported to the Fault structure. Default Value: 0
7 : 0	STARTUP	Startup delay time -1 (in reference clock cycles), after enable, from reference clock start to monitored clock start. At a minimum (both clocks running): STARTUP >= (PERIOD +3) * FREQ_RATIO - UPPER, with FREQ_RATIO = (Reference frequency / Monitored frequency) On top of that the actual clock startup delay and the margin for accuracy of both clocks must be added. Default Value: 0

11.1.64 CSV_LF_CSV_REF_LIMIT

Clock Supervision Reference Limits

Address: 0x42201724

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LOWER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	UPPER [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	UPPER	Cycle time upper limit. Set the upper limit -1, in reference clock cycles, before (or same time) the next monitored clock event must happen. If a monitored clock event does not happen before this limit is reached, or does not happen at all (clock loss), a CSV error is detected. Default Value: 0
7 : 0	LOWER	Cycle time lower limit. Set the lower limit -1, in reference clock cycles, before the next monitored clock event is allowed to happen. If a monitored clock event happens before this limit is reached a CSV error is detected. LOWER must be at least 1 less than UPPER. In case the clocks are asynchronous LOWER must be at least 3 less than UPPER. Default Value: 0

11.1.65 CSV_LF_CSV_MON_CTL

Clock Supervision Monitor Control

Address: 0x42201728

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	PERIOD	Period time. Set the Period -1, in monitored clock cycles, before the next monitored clock event happens. PERIOD <= (UPPER+1) / FREQ_RATIO -1, with FREQ_RATIO = (Reference frequency / Monitored frequency) In case the clocks are asynchronous: PERIOD <= UPPER / FREQ_RATIO -1 Additionally margin must be added for accuracy of both clocks. Default Value: 0

11.1.66 RES_CAUSE

Reset Cause Observation Register

Address: 0x42201800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1C	RW1C	RW1C	None	RW1C	RW1C
HW Access	None		A	A	A	None	A	A
Name	None [7:6]		RESET_MCWDT0	RESET_SOFT	RESET_TC_DBGRESET	None	RESET_ACT_FAULT	RESET_WDT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	RESET_MCWDT0	Multi-Counter Watchdog timer reset #0. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). This bit is only valid when parameter NUM_MCWDT>0 Default Value: 0
4	RESET_SOFT	A CPU requested a system reset through it's SYSRESETREQ. This can be done via a debugger probe or in firmware. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). Default Value: 0
3	RESET_TC_DBGRESET	Test controller or debugger asserted reset. Only resets debug domain. This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). Default Value: 0
1	RESET_ACT_FAULT	Fault logging system requested a reset from its Active logic Default Value: 0
0	RESET_WDT	A basic WatchDog Timer (WDT) reset has occurred since last power cycle. ULP products: This is a low-voltage cause bit that hardware clears when the low-voltage supply is initialized (see comments above). For products that support high-voltage cause detection, this bit blocks recording of other high-voltage cause bits, except RESET_PORVDDD. Hardware clears this bit during POR. This bit is not blocked by other HV cause bits. Default Value: 0

11.1.67 RES_CAUSE2

Reset Cause Observation Register 2

Address: 0x42201804

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW1C						
HW Access	None	A						
Name	None	RESET_CSV_HF [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW1C
HW Access	None							A
Name	None [23:17]							RESET_CSV_REF

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	RESET_CSV_REF	Clock supervision logic requested a reset due to loss or frequency violation of the reference clock source that is used to monitor the other HF clock sources. Default Value: 0
6 : 0	RESET_CSV_HF	Clock supervision logic requested a reset due to loss or frequency violation of a high-frequency clock. Each bit index K corresponds to a HFCLK. Default Value: 0

11.1.68 RES_PXRES_CTL

Programmable XRES Control Register

Address: 0x42201814

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							W1S
HW Access	None							R
Name	None [7:1]							PX-RES_TRIG-GER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	PXRES_TRIGGER	Triggers PXRES. This causes a full-scope reset and reboot. Default Value: 0

11.1.69 CLK_DPLL_LP0_CONFIG

DPLL_LP Configuration Register

Address: 0x42201A00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FEEDBACK_DIV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			REFERENCE_DIV [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			R				
Name	None [23:21]			OUTPUT_DIV [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None	RW		RW	None		
HW Access	R	None	R		R	None		
Name	ENABLE	None	BYPASS_SEL [29:28]		PLL_DCO_CODE_MULT	None [26:24]		

Bits	Name	Description
31	ENABLE	Master enable for PLL. Setup FEEDBACK_DIV, REFERENCE_DIV, and OUTPUT_DIV at least one cycle before setting ENABLE=1. fOUT = (FEEDBACK_DIV + FRAC_EN*FRAC_DIV/2^24) * (fREF / REFERENCE_DIV) / (OUTPUT_DIV) 0: Block is disabled. When the PLL disables, hardware controls the bypass mux as described in BYPASS_SEL, before disabling the PLL circuit. 1: Block is enabled Default Value: 0
29 : 28	BYPASS_SEL	Bypass mux located just after PLL output. This selection is glitch-free and can be changed while the PLL is running. When changing BYPASS_SEL, do not turn off the reference clock or PLL clock for five cycles (whichever is slower). Default Value: 0 **0x0: AUTO :** Automatic using lock indicator. When unlocked, automatically selects PLL reference input (bypass mode). When locked, automatically selects PLL output. If ENABLE=0, automatically selects PLL reference input. **0x1: LOCKED_OR_NOTHING :** Similar to AUTO, except the clock is gated off when unlocked. This is compatible with clock supervision, because the supervisors allow no clock during startup (until a timeout occurs), and the clock targets the proper frequency whenever it is running. If ENABLE=0, no clock is output.

11.1.69 CLK_DPLL_LP0_CONFIG (continued)

		0x2: PLL_BYPASS : Select PLL reference input (bypass mode). Ignores lock indicator **0x3: PLL_OUT :** Select PLL output. Ignores lock indicator. If ENABLE=0, no clock is output.
27	PLL_DCO_CODE_MULT	DCO code coefficient during SAR operation; this trim bit is Fpfd frequency dependent 0: multilply by 16, Fpfd <= 8MHZ 1: mulitply by 28, Fpfd > 8MHz Default Value: 0
20 : 16	OUTPUT_DIV	Control bits for Output divider. Set the divide value before enabling the PLL, and do not change it while PLL is enabled. 0: illegal (undefined behavior) 1: divide by 1. Suitable for direct usage as HFCLK source. 2: divide by 2. Suitable for direct usage as HFCLK source. ... 16: divide by 16. Suitable for direct usage as HFCLK source. >16: illegal (undefined behavior) Default Value: 2
12 : 8	REFERENCE_DIV	Control bits for reference divider. Set the divide value before enabling the PLL, and do not change it while PLL is enabled. 0: illegal (undefined behavior) 1: divide by 1 ... 16: divide by 16 others: illegal (undefined behavior) Default Value: 1
7 : 0	FEEDBACK_DIV	Control bits for feedback divider. Set the divide value before enabling the PLL, and do not change it while PLL is enabled. 0-15: illegal (undefined behavior) 16: divide by 16 ... 125: divide by 125 >125: illegal (undefined behavior) Default Value: 22

11.1.70 CLK_DPLL_LP0_CONFIG2

DPLL_LP Configuration Register 2

Address: 0x42201A04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	FRAC_DIV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	FRAC_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	FRAC_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW			None			
HW Access	R	R			None			
Name	FRAC_EN	FRAC_DITHER_EN [30:28]			None [27:24]			

Bits	Name	Description
31	FRAC_EN	Enables fractional division mode. Default Value: 0
30 : 28	FRAC_DITHER_EN	Enables dithering during fractional operation. 3'b000: disables dithering; 3'b001: enables dithering; others: reserved Default Value: 0
23 : 0	FRAC_DIV	Control bits for fractional divider. This value is interpreted as a fraction of the PFD frequency, i.e. fPFD * (FRAC_DIV/2^24). This field can be dynamically updated within the 1000ppm control limit. It takes up to 115 AHB cycles to transfer the setting to the PLL, and writes that occur faster may be silently ignored and require the application to write again after the previous update has finished. Reading the register returns the accepted value. The PLL will start targeting the new value, but it may take significant time (milliseconds) to stabilize at the new average value. Do not change the FRAC_DIV setting while the PLL is initially locking. Default Value: 0

11.1.71 CLK_DPLL_LP0_CONFIG3

DPLL_LP Configuration Register 3

Address: 0x42201A08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SSCG_DEPTH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SSCG_DEPTH [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					R		
Name	None [23:19]					SSCG_RATE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None		RW	None			RW
HW Access	R	None		R	None			R
Name	SSCG_EN	None [30:29]		SSCG_-MODE	None [27:25]			SSC-G_DITH-ER_EN

Bits	Name	Description
31	SSCG_EN	Enables spreading mode. When SSCG mode is enabled, DPLL_LP_TEST4.PLL_DIS_FAST_LOCK should be set to 1 to disable fast re-lock. Default Value: 0
28	SSCG_MODE	Reserved. Write zero always. Default Value: 0
24	SSCG_DITHER_EN	Reserved. Default Value: 0
18 : 16	SSCG_RATE	Control bits for SSCG modulation rate as a factor of fPFD clock frequency. Audio applications should choose a setting that results in a modulation rate that is greater than 20kHz, so fPFD/512 or fPFD/256 is recommended. Note: All modulation rate trims are valid as long as the fPFD/_number> is less than 32KHz, which is the max modulation rate defined at spec. 0: Modulation rate = fPFD/4096, 1: Modulation rate = fPFD/2048, 2: Modulation rate = fPFD/1024, 3: Modulation rate = fPFD/512, 4: Modulation rate = fPFD/256, 5: Modulation rate = pPFD/128, 6: Modulation rate = pPFD/744 others: reserved Default Value: 0

11.1.71 CLK_DPLL_LP0_CONFIG3 (continued)

9 : 0	SSCG_DEPTH	Control bits for SSCG modulation depth as a percentage of the non-modulated clock. The following choices are supported, and all others are reserved: 10'h029: -0.5% (down-spread), 10'h052: -1% (down-spread), 10'h0a4: -2% (down-spread), 10'h0f6: -3% (down-spread) Default Value: 0

11.1.72 CLK_DPLL_LP0_CONFIG4

DPLL_LP Configuration Register 4

Address: 0x42201A0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DCO_CODE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					R		
Name	None [15:11]					DCO_CODE [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [23:22]		PLL_TG [21:20]		TDC_MODE [19:18]		ACC_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							AC-C_CNT_LOCK

Bits	Name	Description
24	ACC_CNT_LOCK	Control signal for switching to stable filter coefficients (PLL_KP_TRIM/PLL_KI_TRIM) 0: PLL_ACC_PHASE_CNT_DONE 1: PLL_LOCK Default Value: 0
21 : 20	PLL_TG	This value is a number of PFD clocks in relation to the DCO count. Can change the number of counts, set by p_div in integer mode, by the values of -1, +1, or +2. 0: 0 1: -1 2: +1 3: +2 In integer and SSCG mode, PLL_TG must be set to 0. If in fractional mode, PLL_TG must be 0 if frac_ratio <= 0.5 (pll_frac <= 2^23), PLL_TG must be 2 if frac_ratio > 0.5 (pll_frac > 2^23). Default Value: 0
19 : 18	TDC_MODE	0: TDC crude mode - Active only TDC MSB 1: TDC accurate mode - Active TDC MSB,LSB 2: Reserved 3: TDC accurate mode - Active TDC MSB,LSB (clip M3,M2) Default Value: 1
17 : 16	ACC_MODE	bit 17: Reserved - always write 0 bit 16: see description of DPLL_LP_TRIM_STRUCT_Regs.DPLL_LP_CTL.PLL_-FRAC_ORDER Default Value: 1

11.1.72 CLK_DPLL_LP0_CONFIG4 (continued)

10 : 0	DCO_CODE	Initial DCO code. It is recommended to leave this at the default setting. This setting only has effect in open loop mode. See DPLL BROS regarding test modes. Default Value: 0xF

11.1.73 CLK_DPLL_LP0_CONFIG5

DPLL_LP Configuration Register 5

Address: 0x42201A10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	KI_INT [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW						
HW Access	None	R						
Name	None	KP_INT [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	KI_ACC_INT [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW						
HW Access	None	R						
Name	None	KP_ACC_INT [30:24]						

Bits	Name	Description
30 : 24	KP_ACC_INT	Gain of P/I loop filter integrator path during cold start for INT operation. Gain coefficient is 2^KP, eg. 0=>1, 15=>32768. Default Value: 0x1A
22 : 16	KI_ACC_INT	Gain of P/I loop filter integrator path during cold start for INT operation. Gain coefficient is 2^KI, eg. 0=>1, 15=>32768. Default Value: 0x23
14 : 8	KP_INT	Gain of P/I loop filter integrator path for INT operation. Gain coefficient is 2^KP, eg. 0=>1, 15=>32768. Default Value: 0x1C
6 : 0	KI_INT	Gain of P/I loop filter integrator path for INT operation. Gain coefficient is 2^KI, eg. 0=>1, 15=>32768. Default Value: 0x24

11.1.74 CLK_DPLL_LP0_CONFIG6

DPLL_LP Configuration Register 6

Address: 0x42201A14

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	KI_FRACT [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW						
HW Access	None	R						
Name	None	KP_FRACT [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	KI_ACC_FRACT [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW						
HW Access	None	R						
Name	None	KP_ACC_FRACT [30:24]						

Bits	Name	Description
30 : 24	KP_ACC_FRACT	Gain of P/I loop filter integrator path during cold start for FRACT operation. Gain coefficient is 2^KP, eg. 0=>1, 15=>32768. Default Value: 0x1A
22 : 16	KI_ACC_FRACT	Gain of P/I loop filter integrator path during cold start for FRACT operation. Gain coefficient is 2^KI, eg. 0=>1, 15=>32768. Default Value: 0x23
14 : 8	KP_FRACT	Gain of P/I loop filter proportional path for FRACT operation. Gain coefficient is 2^KP, eg. 0=>1, 15=>32768. Default Value: 0x20
6 : 0	KI_FRACT	Gain of P/I loop filter proportional path for FRACT operation. Gain coefficient is 2^KI, eg. 0=>1, 15=>32768. Default Value: 0x24

11.1.75 CLK_DPLL_LP0_CONFIG7

DPLL_LP Configuration Register 7

Address: 0x42201A18

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	KI_SSCG [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW						
HW Access	None	R						
Name	None	KP_SSCG [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	KI_ACC_SSCG [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW						
HW Access	None	R						
Name	None	KP_ACC_SSCG [30:24]						

Bits	Name	Description
30 : 24	KP_ACC_SSCG	Gain of P/I loop filter integrator path during cold start for SSCG operation. Gain coefficient is 2^KP, eg. 0=>1, 15=>32768. Default Value: 0x14
22 : 16	KI_ACC_SSCG	Gain of P/I loop filter integrator path during cold start for SSCG operation. Gain coefficient is 2^KI, eg. 0=>1, 15=>32768. Default Value: 0x16
14 : 8	KP_SSCG	Gain of P/I loop filter proportional path for SSCG operation. Gain coefficient is 2^KP, eg. 0=>1, 15=>32768. Default Value: 0x18
6 : 0	KI_SSCG	Gain of P/I loop filter proportional path for SSCG operation. Gain coefficient is 2^KI, eg. 0=>1, 15=>32768. Default Value: 0x18

11.1.76 CLK_DPLL_LP0_STATUS

DPLL_LP Status Register

Address: 0x42201A1C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	R
HW Access	None						A	W
Name	None [7:2]						UN-LOCK_OC-CURRED	LOCKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	UNLOCK_OCCURRED	This bit sets whenever the PLL Lock bit goes low, and stays set until cleared by firmware. Note: When disabling DPLL via register write, UNLOCK_OCCURRED will set. Therefore, after enabling DPLL and DPLL successfully locks, FW should clear UNLOCK_OCCURRED flag to prevent a false positive that would indicate that DPLL erroneously unlocked. Default Value: 0
0	LOCKED	PLL Lock Indicator Default Value: 0

11.1.77 TST_XRES_SECURE

SECURE TEST and FIRMWARE TEST Key control register

Address: 0x42202054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA8 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				FW_WR [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				SECURE_WR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	R	R	None				
HW Access	R	RW	RW	None				
Name	SECURE_-DISABLE	SE-CURE_KEY_OK	FW_KEY_OK	None [28:24]				

Bits	Name	Description
31	SECURE_DISABLE	Disables the SECURE TEST key entry capability until next reset. Must not be set in the same write when any of the above *_WR bits are set or toggling. Default Value: 0
30	SECURE_KEY_OK	Indicates that the 32-bit SECURE TEST key is observing the correct key. Secure key is not reset, but it will establish low after a deep power cycle that causes it to lose its written state. Default Value: 0
29	FW_KEY_OK	Indicates that the 32-bit FIRMWARE TEST key is observing the correct key. Firmware key is re-set by (A)XRES and STRUCT_XRES. Default Value: 0
19 : 16	SECURE_WR	Latch enables for each of the 4 bytes in the 32-bit SECURE TEST key. Must be toggled high and then low while keeping DATA8 to the correct value. Default Value: 0
11 : 8	FW_WR	Latch enables for each of the 4 bytes in the 32-bit FIRMWARE TEST key. Must be toggled high and then low while keeping DATA8 to the correct value. Default Value: 0
7 : 0	DATA8	Data byte to be set into either SECURE TEST or FIRMWARE TEST key. Must not be changed in the same write that is toggling any of the *_WR bits below, Default Value: 0

11.1.78 PWR_TRIM_PWRSYS_CTL

Power System Trim Register

Address: 0x422020E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			A				
Name	None [7:5]			ACT_REG_TRIM [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	A		None					
Name	ACT_REG_BOOST [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	ACT_REG_BOOST	Controls the tradeoff between output current and internal operating current for the Active Regulator. The maximum output current depends on the silicon implementation, but an application may limit its maximum current to less than that. This may allow a reduction in the internal operating current of the regulator. The regulator internal operating current depends on the boost setting: 2'b00: 50uA 2'b01: 100uA 2'b10: 150uA 2'b11: 200uA The allowed setting is a lookup table based on the chip-specific maximum (set in factory) and an application-specific maximum (set by customer). The defaults are set assuming the application consumes the maximum allowed by the chip. 50mA chip: 2'b00 (default); 100mA chip: 2'b00 (default); 150mA chip: 50..100mA app => 2'b00, 150mA app => 2'b01 (default); 200mA chip: 50mA app => 2'b00, 100..150mA app => 2'b01, 200mA app => 2'b10 (default); 250mA chip: 50mA app => 2'b00, 100..150mA app => 2'b01, 200..250mA app => 2'b10 (default); 300mA chip: 50mA app => 2'b00, 100..150mA app => 2'b01, 200..250mA app => 2'b10, 300mA app => 2'b11 (default); This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. Default Value: X

11.1.78 PWR_TRIM_PWRSYS_CTL (continued)

4 : 0	ACT_REG_TRIM	Trim for the Active-Regulator. This sets the output voltage level. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. The nominal output voltage is vccd=850mV + ACT_REG_TRIM*12.5mV. The actual output voltage will vary depending on conditions and load. The following settings are explicitly shown for convenience, and other values may be calculated using the formula: 5'h04: 900mV (nominal) 5'h0C: 1000mV (nominal) 5'h14: 1100mV (nominal) 5'h1C: 1200mV (nominal) Default Value: 0x14

11.1.79 PWR_TRIM_PWRSYS_CTL2

Power System Trim Register 2

Address: 0x422020E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW			None	RW		
HW Access	None	A			None	A		
Name	None	RET_REG_TRIM [14:12]			None	DPSLP_REG_TRIM [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW			None	RW		
HW Access	None	A			None	A		
Name	None	DPSLP_REG_ACT_TRIM [22:20]			None	NWELL_REG_TRIM [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					A		
Name	None [31:27]					RET_REG_ACT_TRIM [26:24]		

Bits	Name	Description
26 : 24	RET_REG_ACT_TRIM	Trim for the Retention-Regulator (if present) applied during (LP)ACTIVE/(LP)SLEEP modes. These are expected to be constant but provided as registers for risk mitigation. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. Default Value: 0x3
22 : 20	DPSLP_REG_ACT_TRIM	Trim for the DeepSleep-Regulator applied during (LP)ACTIVE/(LP)SLEEP modes. These are expected to be constant but provided as registers for risk mitigation. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. Default Value: 0x0
18 : 16	NWELL_REG_TRIM	Trim for the Nwell-Regulator (if present) applied during DEEPSLEEP mode. Nwell trim is always forced to zero during (LP)ACTIVE/(LP)SLEEP modes. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. Default Value: 0x0
14 : 12	RET_REG_TRIM	Trim for the Retention-Regulator (if present) applied during DEEPSLEEP mode. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. Default Value: 0x5
10 : 8	DPSLP_REG_TRIM	Trim for the DeepSleep-Regulator applied during DEEPSLEEP mode. This register is only reset by XRES, HIBERNATE wakeup, or supply supervision reset. 0: 0.825V 1: 0.850V 2: 0.875V 3: 0.900V 4: 0.925V 5: 1.050V 6: 1.100V 7: 1.150V Default Value: 0x2

11.1.80 CLK_TRIM_ECO_CTL

ECO Trim Register

Address: 0x4220301C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW					
HW Access	None		R					
Name	None [23:22]		ITRIM [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21 : 16	ITRIM	Current Trim Default Value: 31

11.1.81 RAM_TRIM_TRIM_RAM_CTL

Trim Register for RAM Type 0

Address: 0x42204000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	TRIM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	TRIM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	TRIM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	TRIM [31:24]							

Bits	Name	Description
31 : 0	TRIM	For Synopsys RAMs the bits are defined as follows: [3:0] Read-Write margin control. This is used for setting the Read-Write margin. It programs the sense amplifier differential setting and allows the trade off between speed and robustness. - RM[1:0] values control access time and cycle time of the memory. RM[1:0] = "0" is the slowest possible mode of operation for the memory. This setting is required for VDDMIN operation. - RM[3:2] are factory pins reserved for debug mode and should be set to "0". [4] RME: Read-Write margin enable control. This selects between the default Read-Write margin setting, and the external RM[3:0] Read-Write margin setting. [7:5] WPULSE: Write Assist Pulse to control pulse width of negative voltage on SRAM bitline. [9:8] RA: Read Assist control for WL under-drive. [14:12] WA: Write assist enable control (Active High). - WA[2:0] Write Assist pins to control negative voltage on SRAM bitline. Recommended default value for LP: WA=4, RA=0, WPULSE=0, RME=1, RM=3 (RAM_TRIM_DEFAULT=0x0000_4013, RAM_TRIM_WIDTH=15) Recommended default value for ULP: WA=6, RA=0, WPULSE=0, RME=1, RM=2 (RAM_TRIM_DEFAULT=0x0000_6012, RAM_TRIM_WIDTH=15) Default Value: 16403

11.1.82 RAM_TRIM_TRIM_ROM_CTL

Trim Register for ROM

Address: 0x42204004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	TRIM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	TRIM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	TRIM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	TRIM [31:24]							

Bits	Name	Description
31 : 0	TRIM	For Synopsys ROMs the bits are defined as follows: [3:0] RM: Read-Write margin control. This is used for setting the Read-Write margin. It programs the sense amplifier differential setting and allows the trade off between speed and robustness. - RM[1:0] values control access time and cycle time of the memory. RM[1:0] = "0" is the slowest possible mode of operation for the memory. This setting is required for VDDMIN operation. - RM[3:2] are factory pins reserved for debug mode and should be set to "0". [4] RME: Read-Write margin enable control. This selects between the default Read-Write margin setting, and the external pin Read-Write margin setting. Recommended default value for ULP: RME=1, RM=2 (ROM_TRIM_DEFAULT=0x0000_0012, ROM_TRIM_WIDTH=5) Recommended default value for LP: RME=1, RM=3 (ROM_TRIM_DEFAULT=0x0000_0013, ROM_TRIM_WIDTH=5) Default Value: 19

11.1.83 CLK_TRIM_DPLL_LP0_DPLL_LP_CTL

DPLL LP Trim Register

Address: 0x42204200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				None			
HW Access	R				None			
Name	SAR_CYCLE_STOP [7:4]				None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW			None		RW	RW
HW Access	None	R			None		R	R
Name	None	LDO_DCO_TRIM [14:12]			None [11:10]		PLL_SAR_FSM_EN	SAR_DIS

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW			None	RW	
HW Access	R	R	R			None	R	
Name	ISOLATE_N	PLL_-FRAC_ORDER	LDO_PERI_TRIM [21:19]			None	PLL_DCO_SD_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None	RW					
HW Access	R	None	R					
Name	EN-ABLE_CNT	None	ISOLATE_CNT [29:24]					

Bits	Name	Description
31	ENABLE_CNT	Enable for the PLL hardware sequencer. 0: Disables the hardware sequencer. Before enabling the DPLL manually make sure to have DPLL_LP_STRUCT_Regs->CONFIG->BYPASS_SEL at default value to avoid unwanted glitch on clock HF root. When disabling the PLL, first deselect it using .BYPASS_SEL=PLL_REF, wait at least six PLL clock cycles, and then disable it with .ENABLE=0. Before entering DEEPSLEEP, firmware must switch to another clock source and disable the PLL. 1: Enables the hardware sequencer. The sequencer handles all PLL enable/disable transitions, including around DEEPSLEEP entry/exit. Default Value: 1
29 : 24	ISOLATE_CNT	Terminal count for the stabilization counter handles PLL_ISOLATE_N Default Value: 0x7
23	ISOLATE_N	Manual isolation control for PLL . This field is ignored when ENABLE_CNT==1. When controlling manually, de-assert >= 3us after ENABLE=1. Assertion can happen in cycle just before EN-ABLE=0. 0: Isolate outputs 1: Do not isolate outputs Default Value: 0

11.1.83 CLK_TRIM_DPLL_LP0_DPLL_LP_CTL (continued)

22	PLL_FRAC_ORDER	Order of the delta-sigma modulator used for fractional mode. If DPLL_LP_STRUCT_Regs.CONFIG4.ACC_MODE = 00b: 0: 4th order 1: 3rd order If DPLL_LP_STRUCT_Regs.CONFIG4.ACC_MODE = 01b: 0: 2nd order 1: 1st order Default Value: 0
21 : 19	LDO_PERI_TRIM	pll ldo peripheri voltage trim (scan mode - can be '0' or '1' - not High Z) Default Value: 0
17 : 16	PLL_DCO_SD_SEL	00': disable, '01' first order SigmaDelta enabled;'10' third order SigmaDelta enabled;'11' RSVD Default Value: 0
14 : 12	LDO_DCO_TRIM	Trim for PLL local regulator for DCO 0 0.906V 1 0.786V 2 0.846V 3 0.876V 4 0.936V 5 0.966V Default Value: 0
9	PLL_SAR_FSM_EN	SAR FSM enable. Always set to 1 for functional mode. This register was kept in the design (and moved to hidden trim register) to increase coverage on the hard IP, and could be removed once the hard IP input is removed. Default Value: 0x1
8	SAR_DIS	Disable Successive Approximation Register during locking. 0: Use SAR. 1: Disable SAR. Default Value: 0
7 : 4	SAR_CYCLE_STOP	Successive Approximation Register (SAR) configuration. Ignored when SAR_DIS==1. 0x1...0xB: Number of cycles until SAR stops. others: illegal Note: For initial lock, default should be left at 0x3. After successful lock with code write = 0, FW should set to 0x1 to improve recovery time for successive locks. Default Value: 0x3

11.1.84 CLK_TRIM_DPLL_LP0_DPLL_LP_CTL3

DPLL LP Trim Register 3

Address: 0x42204208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PHASE_ACC_CNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						PHASE_ACC_CNT [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	PHASE_ACC_CNT_SSCG [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						PHASE_ACC_CNT_SS-CG [25:24]	

Bits	Name	Description
25 : 16	PHASE_ACC_CNT_SS-CG	counter for phase accelerate cycles during PLL wakeup SSCG mode Optimal settings: 4 --> 5 MHz: 127 5-->6 MHz: 157 6-->7 MHz: 187 7-->8 MHz: 217 8-->9 MHz: 255 9-->10 MHz: 286 10-->11 MHz: 317 11-->12 MHz: 348 12-->13 MHz: 379 13-->14 MHz: 410 14-->15 MHz: 441 15-->16 MHz: 472 16 MHz: 511 Default Value: 0x1

11.1.84 CLK_TRIM_DPLL_LP0_DPLL_LP_CTL3 (continued)

9 : 0	PHASE_ACC_CNT	counter for phase accelerate cycles during PLL wakeup for INT and FRAC modes Optimal settings: 4 --> 5 MHz: 127 5-->6 MHz: 157 6-->7 MHz: 187 7-->8 MHz: 217 8-->9 MHz: 255 9-->10 MHz: 286 10-->11 MHz: 317 11-->12 MHz: 348 12-->13 MHz: 379 13-->14 MHz: 410 14-->15 MHz: 441 15-->16 MHz: 472 16 MHz: 511 Default Value: 0x7F

11.1.85 CLK_TRIM_DPLL_LP0_DPLL_LP_CTL4

DPLL LP Trim Register 4

Address: 0x4220420C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				None		RW	
HW Access	R				None		R	
Name	LOCK_WAIT_RISE [7:4]				None [3:2]		LOCK_WAIT_FALL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW					
HW Access	None		R					
Name	None [15:14]		LOCK_WAIT_RISE [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description

11.1.85 CLK_TRIM_DPLL_LP0_DPLL_LP_CTL4 (continued)

13 : 4	LOCK_WAIT_RISE	Wait time from when static phase error is within the lock window until lock signal asserts. 0: Illegal 1: 1 PFD clocks 2: 2 PFD clocks ... 1023: 1023 PFD clocks Optimal settings f, MHz With Code Write Without Code Write --- --- --- 4-->5 6 33 5-->6 6 40 6-->7 6 49 7-->8 8 60 8-->9 8 85 9-->10 11 95 10-->11 12 105 11-->12 14 115 12-->13 15 125 13-->14 17 135 14-->15 18 145 15-->16 20 155 16 21 165 Notes: 1. For initial DPLL locking or when DPLL Fast Lock is disabled (PLL_DIS_FAST_LOCK=1), user must program DPLL_CTL4.LOCK_WAIT_RISE using appropriate value for "Without Code Write" for corresponding frequency range. 2. After initial DPLL locking, when DPLL Fast Lock is enabled (PLL_DIS_FAST_LOCK=0), before DEEPSLEEP entry, FW must poll the DPLL_LP.STATUS.LOCKED bit to acknowledge successful DPLL lock, then must program DPLL_LP_CTL4.LOCK_WAIT_RISE using appropriate value for "With Code Write" for corresponding frequency range. Default Value: 0xA5
1 : 0	LOCK_WAIT_FALL	Wait time from when static phase error is within the lock window until lock signal asserts. 0: 0 PFD clocks 1: 2 PFD clocks 2: 3 PFD clocks 3: 4 PFD clocks Default Value: 0

11.1.86 CLK_TRIM_DPLL_LP0_DPLL_LP_TEST4

DPLL LP Test Register 4

Address: 0x4220421C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	PLL_USER_DCO_CODE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW					
HW Access	A	R	A					
Name	PLL_READ_EN	PLL_DIS_-FAST_LOCK	PLL_USER_DCO_CODE [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW						
HW Access	R	R						
Name	PHASE_ACC_US-ER_WRITE_FRACT	PHASE_ACC_USER_WRITE_INT [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW					
HW Access	None		R					
Name	None [31:30]		PHASE_ACC_USER_WRITE_FRACT [29:24]					

Bits	Name	Description
29 : 23	PHASE_ACC_US-ER_WRITE_FRACT	reduce KI,KP coefficient during PLL deepsleep wakeup fract. Default Value: 0x10
22 : 16	PHASE_ACC_US-ER_WRITE_INT	Reduce KI,KP coefficient during PLL deepsleep wakeup integer. Default Value: 0x10
15	PLL_READ_EN	This bit is a self clear bit. The FW writes 1 to get an updated value in PLL_USER_D-CO_CODE.HW will self clear this bit to indicate that the PLL_USER_DCO_CODE be read. Default Value: 0
14	PLL_DIS_FAST_LOCK	0: Enables DPLL Fast Lock 1: Disables DPLL Fast Lock When PLL_DIS_FAST_LOCK=0, if DPLL successfully locks prior to a DEEPSLEEP entry: - HW will read the DCO code before DEEPSLEEP entry, then write the DCO code upon DEEP-SLEEP exit, to reduce DPLL lock time. - FW must follow the procedure described under DPLL_LP_CTL4.LOCK_WAIT_RISE Notes: 2 Default Value: 0
13 : 0	PLL_USER_DCO_CODE	FW can read the code saved by the DPLL before deepsleep.Use PLL_READ_EN to get updated DCO_CODE from the DPLL: To read properly please refer to PLL_USER_D-CO_CODE_RD_EN/PLL_READ_EN. Before any read, FW should check first that PLL_READ_EN is 0. To account for Clock Domain Crossings, FW should wait at least 3 CLK_IMO cycles (3*125ns=375ns) between SW write and SW read operation. Default Value: 0

11.1.87 WDT_CTL

Watchdog Counter Control Register (Type A)

Address: 0x4220C000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		None			RW
HW Access	None		A		None			A
Name	None [7:6]		WDT_CLK_SEL [5:4]		None [3:1]			WDT_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	A		None					
Name	WDT_LOCK [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	WDT_LOCK	Prohibits writing to WDT_*, CLK_ILO_CONFIG, CLK_SELECT.LFCLK_SEL, and CLK_TRIM_ILO_CTL registers when not equal 0. Requires at least two different writes to unlock. A change in WDT_LOCK takes effect beginning with the next write cycle. Note that this field is 2 bits to force multiple writes only. It represents only a single write protect signal protecting all those registers at the same time. WDT will lock on any reset. This field is not retained during DEEPSLEEP or HIBERNATE mode, so the WDT will be locked after wakeup from these modes. Default Value: 3 **0x0: NO_CHG :** No effect **0x1: CLR0 :** Clears bit 0 **0x2: CLR1 :** Clears bit 1 **0x3: SET01 :** Sets both bits 0 and 1

11.1.87 WDT_CTL (continued)

5 : 4	WDT_CLK_SEL	Select source for WDT. Not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. Writes to this field are ignored unless the WDT is unlock using WDT_LOCK register. It takes four cycles of the originally selected clock to switch away from it. Do not disable the original clock during this time. Default Value: 0 **0x0: ILO :** ILO - Internal Low-speed Oscillator **0x1: PILO :** PILO - Precision ILO. If present, if present **0x2: BAK :** BAK - Selected clk_bak source, if present. See BACKUP_CTL. This choice is not recommended for applications that rely upon the watchdog timer for safety or security, unless the product supports clock supervision of clk_bak (CSV_BAK). Generation of clk_bak is not protected by WDT_LOCK and is in a different memory region with potentially different security attributes.
0	WDT_EN	Enable this watchdog timer. This field is retained during DEEPSLEEP and HIBERNATE modes. Default Value: 1

11.1.88 WDT_CNT

Watchdog Counter Count Register (Type A)

Address: 0x4220C004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	COUNTER [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	COUNTER [31:24]							

Bits	Name	Description
31 : 0	COUNTER	Current value of WDT Counter. The write feature of this register is for engineering use (DfV), have no synchronization, and can only be applied when the WDT is fully off. When writing, the value is updated immediately in the WDT counter, but it will read back as the old value until this register resynchronizes just after the negedge of ILO. Writes will be ignored if they occur when the WDT is enabled. Default Value: 0

11.1.89 WDT_MATCH

Watchdog Counter Match Register (Type A)

Address: 0x4220C008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	MATCH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	MATCH [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	MATCH [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	MATCH [31:24]							

Bits	Name	Description
31 : 0	MATCH	Match value for Watchdog counter. Every time WDT_COUNTER reaches MATCH an interrupt is generated. Two unserviced interrupts will lead to a system reset (i.e. at the third match). Default Value: 4096

11.1.90 WDT_MATCH2

Watchdog Counter Match Register 2 (Type A)

Address: 0x4220C00C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			A				
Name	None [7:5]			IGNORE_BITS_ABOVE [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	IGNORE_BITS_ABOVE	The bit index to be considered the MSB for matching. Bit indices above this setting are NOT checked against MATCH. This value provides control over the time-to-reset of the watchdog (which happens after 3 successive matches). The four LSBs cannot be ignored for matching. Settings <3 behave like a setting of 3. If the setting is higher than the number of bits in the WDT counter, all actual bits in the counter are matched. Default Value: 31

11.1.91 MCWDT_CNTLOW0

Multi-Counter Watchdog Sub-counters 0/1

Address: 0x4220D004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	WDT_CTR0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	WDT_CTR0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	WDT_CTR1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	WDT_CTR1 [31:24]							

Bits	Name	Description
31 : 16	WDT_CTR1	Current value of sub-counter 1 for this MCWDT. Software writes are ignored when the sub-counter is enabled Default Value: 0
15 : 0	WDT_CTR0	Current value of sub-counter 0 for this MCWDT. Software writes are ignored when the sub-counter is enabled. Default Value: 0

11.1.92 MCWDT_CNTHIGH0

Multi-Counter Watchdog Sub-counter 2

Address: 0x4220D008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	WDT_CTR2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	WDT_CTR2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	WDT_CTR2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	WDT_CTR2 [31:24]							

Bits	Name	Description
31 : 0	WDT_CTR2	Current value of sub-counter 2 for this MCWDT. Software writes are ignored when the sub-counter is enabled Default Value: 0

11.1.93 MCWDT_MATCH0

Multi-Counter Watchdog Counter Match Register

Address: 0x4220D00C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WDT_MATCH0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	WDT_MATCH0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	WDT_MATCH1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	WDT_MATCH1 [31:24]							

Bits	Name	Description
31 : 16	WDT_MATCH1	Match value for sub-counter 1 of this MCWDT Default Value: 0
15 : 0	WDT_MATCH0	Match value for sub-counter 0 of this MCWDT Default Value: 0

11.1.94 MCWDT_CONFIG0

Multi-Counter Watchdog Counter Configuration

Address: 0x4220D010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW		RW	RW	RW	
HW Access	R	R	R		R	R	R	
Name	WDT_-MATCH0_1	WDT_CAR-RY0_1	WDT_LOWER_MODE0 [5:4]		WDT_CAS-CADE0_1	WDT_-CLEAR0	WDT_MODE0 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW		RW	RW	RW	
HW Access	R	R	R		R	R	R	
Name	WDT_-MATCH1_2	WDT_CAR-RY1_2	WDT_LOWER_MODE1 [13:12]		WDT_CAS-CADE1_2	WDT_-CLEAR1	WDT_MODE1 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							WDT_-MODE2

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			R				
Name	None [31:29]			WDT_BITS2 [28:24]				

Bits	Name	Description
28 : 24	WDT_BITS2	Bit to observe for WDT_INT2: 0: Assert after bit0 of WDT_CTR2 toggles (one int every tick) ... 31: Assert after bit31 of WDT_CTR2 toggles (one int every 2^31 ticks) Default Value: 0
16	WDT_MODE2	Watchdog Counter 2 Mode. Default Value: 0 **0x0: NOTHING :** Free running counter with no interrupt requests **0x1: INT :** Free running counter with interrupt request that occurs one LFCLK cycle after the specified bit in CTR2 toggles (see WDT_BITS2).
15	WDT_MATCH1_2	Specifies matching behavior when WDT_CASCADE1_2==1. When WDT_CASCADE1_2==0, this bit is not used and match is based on counter 2 alone. 0: Match based on counter 2 alone. 1: Match based on counter 2 and counter 1 matching simultaneously. Default Value: 0

11.1.94 MCWDT_CONFIG0 (continued)

14	WDT_CARRY1_2	Carry out behavior that applies when WDT_CASCADE1_2==1. This bit is not used when WDT_-CASCADE1_2==0. 0: carry out on counter 1 match. 1: carry out on counter 1 roll-over. Default Value: 0
13 : 12	WDT_LOWER_MODE1	Watchdog Counter Action on service before lower limit. Default Value: 0 **0x0: NOTHING :** Do nothing **0x1: INT :** Assert WDT_INTx **0x2: RESET :** Assert WDT Reset
11	WDT_CASCADE1_2	Cascade Watchdog Counters 1,2. Counter 2 increments the cycle after WDT_CTR1=WDT_-MATCH1. It is allowed to cascade all three WDT counters. 0: Independent counters 1: Cascaded counters. When cascading all three counters, WDT_CLEAR1 must be 1. Default Value: 0
10	WDT_CLEAR1	Clear Watchdog Counter when WDT_CTR1==WDT_MATCH1. In other words WDT_CTR1 di-vides LFCLK by (WDT_MATCH1+1). 0: Free running counter 1: Clear on match. In this mode, the minimum legal setting of WDT_MATCH1 is 1. Default Value: 0
9 : 8	WDT_MODE1	Watchdog Counter Action on Match. Action is taken on the next increment after the values match (WDT_CTR1=WDT_MATCH1). Default Value: 0 **0x0: NOTHING :** Do nothing **0x1: INT :** Assert WDT_INTx **0x2: RESET :** Assert WDT Reset **0x3: INT_THEN_RESET :** Assert WDT_INTx, assert WDT Reset after 3rd unhandled interrupt
7	WDT_MATCH0_1	Specifies matching behavior when WDT_CASCADE0_1==1. When WDT_CASCADE0_1==0, this bit is not used and match is based on counter 1 alone. 0: Match based on counter 1 alone. 1: Match based on counter 1 and counter 0 matching simultaneously. Default Value: 0
6	WDT_CARRY0_1	Carry out behavior that applies when WDT_CASCADE0_1==1. This bit is not used when WDT_-CASCADE0_1==0. 0: carry out on counter 0 match. 1: carry out on counter 0 roll-over. Default Value: 0

11.1.94 MCWDT_CONFIG0 (continued)

5 : 4	WDT_LOWER_MODE0	Watchdog Counter Action on service before lower limit. Default Value: 0 **0x0: NOTHING :** Do nothing **0x1: INT :** Assert WDT_INTx **0x2: RESET :** Assert WDT Reset
3	WDT_CASCADE0_1	Cascade Watchdog Counters 0,1. Counter 1 increments the cycle after WDT_CTR0=WDT_-MATCH0. 0: Independent counters 1: Cascaded counters Default Value: 0
2	WDT_CLEAR0	Clear Watchdog Counter when WDT_CTR0=WDT_MATCH0. In other words WDT_CTR0 divides LFCLK by (WDT_MATCH0+1). 0: Free running counter 1: Clear on match. In this mode, the minimum legal setting of WDT_MATCH0 is 1. Default Value: 0
1 : 0	WDT_MODE0	Watchdog Counter Action on Match. Action is taken on the next increment after the values match (WDT_CTR0=WDT_MATCH0). Default Value: 0 **0x0: NOTHING :** Do nothing **0x1: INT :** Assert WDT_INTx **0x2: RESET :** Assert WDT Reset **0x3: INT_THEN_RESET :** Assert WDT_INTx, assert WDT Reset after 3rd unhandled interrupt

11.1.95 MCWDT_CTL0

Multi-Counter Watchdog Counter Control

Address: 0x4220D014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S	None	R	RW
HW Access	None				RW0C	None	RW	R
Name	None [7:4]				WDT_RESET0	None	WDT_ENABLED0	WDT_ENABLE0

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	None	R	RW
HW Access	None				RW0C	None	RW	R
Name	None [15:12]				WDT_RESET1	None	WDT_ENABLED1	WDT_ENABLE1

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW1S	None	R	RW
HW Access	None				RW0C	None	RW	R
Name	None [23:20]				WDT_RESET2	None	WDT_ENABLED2	WDT_ENABLE2

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19	WDT_RESET2	Resets counter 2 back to 0000. Hardware will reset this bit after counter was reset. This will take up to one LFCLK cycle to take effect. Default Value: 0
17	WDT_ENABLED2	Indicates actual state of counter. May lag WDT_ENABLE2 by up to two LFCLK cycles. Default Value: 0
16	WDT_ENABLE2	Enable subcounter 2. May take up to 2 LFCLK cycles to take effect. 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) Default Value: 0
11	WDT_RESET1	Resets counter 1 back to 0000. Hardware will reset this bit after counter was reset. This will take up to one LFCLK cycle to take effect. Default Value: 0
9	WDT_ENABLED1	Indicates actual state of counter. May lag WDT_ENABLE1 by up to two LFCLK cycles. Default Value: 0
8	WDT_ENABLE1	Enable subcounter 1. May take up to 2 LFCLK cycles to take effect. 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) Default Value: 0
3	WDT_RESET0	Resets counter 0 back to 0000. Hardware will reset this bit after counter was reset. This will take up to one LFCLK cycle to take effect. Default Value: 0

11.1.95 MCWDT_CTL0 (continued)

1	WDT_ENABLED0	Indicates actual state of counter. May lag WDT_ENABLE0 by up to two LFCLK cycles. Default Value: 0
0	WDT_ENABLE0	Enable subcounter 0. May take up to 2 LFCLK cycles to take effect. 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) Default Value: 0

11.1.96 MCWDT_INTR0

Multi-Counter Watchdog Counter Interrupt Register

Address: 0x4220D018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					A	A	A
Name	None [7:3]					MCWDT_INT2	MCWDT_INT1	MCWDT_INT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	MCWDT_INT2	MCWDT Interrupt Request for sub-counter 2. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. Clearing this bit also prevents Reset from happening when WDT_MODE2=3. Default Value: 0
1	MCWDT_INT1	MCWDT Interrupt Request for sub-counter 1. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. Clearing this bit also prevents Reset from happening when WDT_MODE1=3. Default Value: 0
0	MCWDT_INT0	MCWDT Interrupt Request for sub-counter 0. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. Clearing this bit also prevents Reset from happening when WDT_MODE0=3. Default Value: 0

11.1.97 MCWDT_INTR_SET0

Multi-Counter Watchdog Counter Interrupt Set Register

Address: 0x4220D01C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [7:3]					MCWDT_INT2	MCWDT_INT1	MCWDT_INT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	MCWDT_INT2	Set interrupt for MCWDT_INT2 Default Value: 0
1	MCWDT_INT1	Set interrupt for MCWDT_INT1 Default Value: 0
0	MCWDT_INT0	Set interrupt for MCWDT_INT0 Default Value: 0

11.1.98 MCWDT_INTR_MASK0

Multi-Counter Watchdog Counter Interrupt Mask Register

Address: 0x4220D020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					MCWDT_INT2	MCWDT_INT1	MCWDT_INT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	MCWDT_INT2	Mask for sub-counter 2. This controls if the interrupt is forwarded to the CPU. 0: Interrupt is masked (not forwarded). 1: Interrupt is forwarded. Default Value: 0
1	MCWDT_INT1	Mask for sub-counter 1. This controls if the interrupt is forwarded to the CPU. 0: Interrupt is masked (not forwarded). 1: Interrupt is forwarded. Default Value: 0
0	MCWDT_INT0	Mask for sub-counter 0. This controls if the interrupt is forwarded to the CPU. 0: Interrupt is masked (not forwarded). 1: Interrupt is forwarded. Default Value: 0

11.1.99 MCWDT_INTR_MASKED0

Multi-Counter Watchdog Counter Interrupt Masked Register

Address: 0x4220D024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					RW	RW	RW
Name	None [7:3]					MCWDT_INT2	MCWDT_INT1	MCWDT_INT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	MCWDT_INT2	Logical and of corresponding request and mask bits. Default Value: 0
1	MCWDT_INT1	Logical and of corresponding request and mask bits. Default Value: 0
0	MCWDT_INT0	Logical and of corresponding request and mask bits. Default Value: 0

11.1.100 MCWDT_LOCK0

Multi-Counter Watchdog Counter Lock Register

Address: 0x4220D028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	A		None					
Name	MCWDT_LOCK [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	MCWDT_LOCK	Prohibits writing control and configuration registers related to this MCWDT when not equal 0 (as specified in the other register descriptions). Requires at least two different writes to unlock. Note that this field is 2 bits to force multiple writes only. Each MCWDT has a separate local lock. LFCLK settings are locked by the global WDT_LOCK register, and this register has no effect on that. Default Value: 0 **0x0: NO_CHG :** No effect **0x1: CLR0 :** Clears bit 0 **0x2: CLR1 :** Clears bit 1 **0x3: SET01 :** Sets both bits 0 and 1

11.1.101 MCWDT_LOWER_LIMIT0

Multi-Counter Watchdog Counter Lower Limit Register

Address: 0x4220D02C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WDT_LOWER_LIMIT0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	WDT_LOWER_LIMIT0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	WDT_LOWER_LIMIT1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	WDT_LOWER_LIMIT1 [31:24]							

Bits	Name	Description
31 : 16	WDT_LOWER_LIMIT1	Lower limit for sub-counter 1 of this MCWDT Default Value: 0
15 : 0	WDT_LOWER_LIMIT0	Lower limit for sub-counter 0 of this MCWDT Default Value: 0

12 Device Power Modes registers

This section discusses the Device Power Modes registers. It lists all the registers in mapping tables, in address order.

12.1 Register details

Register	Address	Description
PWRMODE_PD0_PD_SENSE	0x42210000	Dependency Sense Register
PWRMODE_PD0_PD_SPT	0x42210004	Dependency Support Register
PWRMODE_PD1_PD_SENSE	0x42210010	Dependency Sense Register. See PWRMODE_PD0_PD_SENSE for the details of bit fields.
PWRMODE_PD1_PD_SPT	0x42210014	Dependency Support Register. See PWRMODE_PD0_PD_SPT for the details of bit fields.
PWRMODE_PD2_PD_SENSE	0x42210020	Dependency Sense Register. See PWRMODE_PD0_PD_SENSE for the details of bit fields.
PWRMODE_PD2_PD_SPT	0x42210024	Dependency Support Register. See PWRMODE_PD0_PD_SPT for the details of bit fields.
PWRMODE_PD3_PD_SENSE	0x42210030	Dependency Sense Register. See PWRMODE_PD0_PD_SENSE for the details of bit fields.
PWRMODE_PD3_PD_SPT	0x42210034	Dependency Support Register. See PWRMODE_PD0_PD_SPT for the details of bit fields.
PWRMODE_PD4_PD_SENSE	0x42210040	Dependency Sense Register. See PWRMODE_PD0_PD_SENSE for the details of bit fields.
PWRMODE_PD4_PD_SPT	0x42210044	Dependency Support Register. See PWRMODE_PD0_PD_SPT for the details of bit fields.
PWRMODE_PD5_PD_SENSE	0x42210050	Dependency Sense Register. See PWRMODE_PD0_PD_SENSE for the details of bit fields.
PWRMODE_PD5_PD_SPT	0x42210054	Dependency Support Register. See PWRMODE_PD0_PD_SPT for the details of bit fields.
PWRMODE_PD6_PD_SENSE	0x42210060	Dependency Sense Register. See PWRMODE_PD0_PD_SENSE for the details of bit fields.
PWRMODE_PD6_PD_SPT	0x42210064	Dependency Support Register. See PWRMODE_PD0_PD_SPT for the details of bit fields.
PWRMODE_PD7_PD_SENSE	0x42210070	Dependency Sense Register. See PWRMODE_PD0_PD_SENSE for the details of bit fields.
PWRMODE_PD7_PD_SPT	0x42210074	Dependency Support Register. See PWRMODE_PD0_PD_SPT for the details of bit fields.
PWRMODE_PD8_PD_SENSE	0x42210080	Dependency Sense Register. See PWRMODE_PD0_PD_SENSE for the details of bit fields.
PWRMODE_PD8_PD_SPT	0x42210084	Dependency Support Register. See PWRMODE_PD0_PD_SPT for the details of bit fields.
PWRMODE_PD9_PD_SENSE	0x42210090	Dependency Sense Register. See PWRMODE_PD0_PD_SENSE for the details of bit fields.

Device Power Modes registers

Register	Address	Description
PWRMODE_PD9_PD_SPT	0x42210094	Dependency Support Register. See PWRMODE_PD0_PD_SPT for the details of bit fields.
PWRMODE_PD10_PD_SENSE	0x422100A0	Dependency Sense Register. See PWRMODE_PD0_PD_SENSE for the details of bit fields.
PWRMODE_PD10_PD_SPT	0x422100A4	Dependency Support Register. See PWRMODE_PD0_PD_SPT for the details of bit fields.
PWRMODE_PD11_PD_SENSE	0x422100B0	Dependency Sense Register. See PWRMODE_PD0_PD_SENSE for the details of bit fields.
PWRMODE_PD11_PD_SPT	0x422100B4	Dependency Support Register. See PWRMODE_PD0_PD_SPT for the details of bit fields.
PWRMODE_PD12_PD_SENSE	0x422100C0	Dependency Sense Register. See PWRMODE_PD0_PD_SENSE for the details of bit fields.
PWRMODE_PD12_PD_SPT	0x422100C4	Dependency Support Register. See PWRMODE_PD0_PD_SPT for the details of bit fields.
PWRMODE_PD13_PD_SENSE	0x422100D0	Dependency Sense Register. See PWRMODE_PD0_PD_SENSE for the details of bit fields.
PWRMODE_PD13_PD_SPT	0x422100D4	Dependency Support Register. See PWRMODE_PD0_PD_SPT for the details of bit fields.
PWRMODE_PD14_PD_SENSE	0x422100E0	Dependency Sense Register. See PWRMODE_PD0_PD_SENSE for the details of bit fields.
PWRMODE_PD14_PD_SPT	0x422100E4	Dependency Support Register. See PWRMODE_PD0_PD_SPT for the details of bit fields.
PWRMODE_PD15_PD_SENSE	0x422100F0	Dependency Sense Register. See PWRMODE_PD0_PD_SENSE for the details of bit fields.
PWRMODE_PD15_PD_SPT	0x422100F4	Dependency Support Register. See PWRMODE_PD0_PD_SPT for the details of bit fields.
PWRMODE_PPU_MAIN_PWPR	0x42211000	Power Policy Register
PWRMODE_PPU_MAIN_PMER	0x42211004	Power Mode Emulation Register
PWRMODE_PPU_MAIN_PWSR	0x42211008	Power Status Register
PWRMODE_PPU_MAIN_DISR	0x42211010	Device Interface Input Current Status Register
PWRMODE_PPU_MAIN_MISR	0x42211014	Miscellaneous Input Current Status Register
PWRMODE_PPU_MAIN_STSR	0x42211018	Stored Status Register
PWRMODE_PPU_MAIN_UNLK	0x4221101C	Unlock register
PWRMODE_PPU_MAIN_PWCR	0x42211020	Power Configuration Register
PWRMODE_PPU_MAIN_PTCR	0x42211024	Power Mode Transition Configuration Register
PWRMODE_PPU_MAIN_IMR	0x42211030	Interrupt Mask Register
PWRMODE_PPU_MAIN_AIMR	0x42211034	Additional Interrupt Mask Register
PWRMODE_PPU_MAIN_ISR	0x42211038	Interrupt Status Register
PWRMODE_PPU_MAIN_AISR	0x4221103C	Additional Interrupt Status Register
PWRMODE_PPU_MAIN_IESR	0x42211040	Input Edge Sensitivity Register
PWRMODE_PPU_MAIN_OPSR	0x42211044	Operating Mode Active Edge Sensitivity Register

Device Power Modes registers

Register	Address	Description
PWRMODE_PPU_MAIN_FUNRR	0x42211050	Functional Retention RAM Configuration Register
PWRMODE_PPU_MAIN_FULRR	0x42211054	Full Retention RAM Configuration Register
PWRMODE_PPU_MAIN_MEMRR	0x42211058	Memory Retention RAM Configuration Register
PWRMODE_PPU_MAIN_EDTR0	0x42211160	Power Mode Entry Delay Register 0
PWRMODE_PPU_MAIN_EDTR1	0x42211164	Power Mode Entry Delay Register 1
PWRMODE_PPU_MAIN_DCDR0	0x42211170	Device Control Delay Configuration Register 0
PWRMODE_PPU_MAIN_DCDR1	0x42211174	Device Control Delay Configuration Register 1
PWRMODE_PPU_MAIN_IDR0	0x42211FB0	PPU Identification Register 0
PWRMODE_PPU_MAIN_IDR1	0x42211FB4	PPU Identification Register 1
PWRMODE_PPU_MAIN_IIDR	0x42211FC8	Implementation Identification Register
PWRMODE_PPU_MAIN_AIDR	0x42211FCC	Architecture Identification Register
PWRMODE_CLK_SELECT	0x42212000	Clock Selection for Power Mode Components

12.1.1 PWRMODE_PD0_PD_SENSE

Dependency Sense Register

Address: 0x42210000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	PD_ON [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	PD_ON [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PD_ON	Each bit *indicates whether PD is directly kept on when PD is on. Indirect dependency is still possible if multiple direct dependencies work together to create a transitive relationship. For example, if PD1 depends upon PD2; and PD2 dpends upon PD3; then PD1 indirectly depends upon PD3 regardless of whether there is a direct dependency from PD3 to PD1. Some bits are implemented as constants, and some bits are implemented as user-configurable registers. Refer to PD_SPT register to see how each bit is implemented. Default Value: X*

12.1.2 PWRMODE_PD0_PD_SPT

Dependency Support Register

Address: 0x42210004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	PD_FORCE_ON [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	PD_FORCE_ON [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	PD_CONFIG_ON [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	PD_CONFIG_ON [31:24]							

Bits	Name	Description
31 : 16	PD_CONFIG_ON	Each bit *indicates whether PD can be configured on when PD is on. Default Value: X*
15 : 0	PD_FORCE_ON	Each bit *indicates whether PD is always kept on when PD is on for sense bits that are not configurable. For configurable bits, this indicates the reset value of the configurable bit. Default Value: X*

12.1.3 PWRMODE_PPU_MAIN_PWPR

Power Policy Register

Address: 0x42211000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				PWR_POLICY [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None			RW
HW Access	None			R	None			R
Name	None [15:13]			LOCK_EN	None [11:9]			PWR_DYN_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				OP_POLICY [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							OP_DYN_EN

Bits	Name	Description
24	OP_DYN_EN	Reserved Default Value: 0x0
19 : 16	OP_POLICY	Reserved Default Value: 0x0
12	LOCK_EN	Reserved Default Value: 0x0
8	PWR_DYN_EN	Power mode dynamic transition enable. For main PPU, keep this bit 1. Default Value: 0x1
3 : 0	PWR_POLICY	Power mode policy. When static power mode transitions are enabled, PWR_DYN_EN is set to 0, this is the target power mode for the PPU. When dynamic power mode transitions are enabled, PWR_DYN_EN is set to 1, this is the minimum power mode for the PPU. This PPU supports the following modes: OFF(0), MEM_RET(2), FULL_RET(5), ON(8). Do not use WARM_RST(9) or other unsupported modes. Default Value: 0x8

12.1.4 PWRMODE_PPU_MAIN_PMER

Power Mode Emulation Register

Address: 0x42211004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							EMU_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	EMU_EN	Reserved Default Value: 0x0

12.1.5 PWRMODE_PPU_MAIN_PWSR

Power Status Register

Address: 0x42211008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				RW			
Name	None [7:4]				PWR_STATUS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None			R	None			R
HW Access	None			RW	None			RW
Name	None [15:13]			LOCK_STATUS	None [11:9]			PWR_DYN_STATUS

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				RW			
Name	None [23:20]				OP_STATUS [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							RW
Name	None [31:25]							OP_DYN_STATUS

Bits	Name	Description
24	OP_DYN_STATUS	Reserved Default Value: 0x0
19 : 16	OP_STATUS	Reserved Default Value: 0x0
12	LOCK_STATUS	Reserved Default Value: 0x0
8	PWR_DYN_STATUS	Power mode dynamic transition status. When set to 1 power mode dynamic transitions are enabled. There might be a delay in dynamic transitions becoming active or inactive if the PPU is transitioning when PWR_DYN_EN is programmed. Default Value: 0x0
3 : 0	PWR_STATUS	Power mode status. These bits reflect the current power mode of the PPU. See PPU_PWPR.PWR_POLICY for power mode enumeration. Default Value: 0x0

12.1.6 PWRMODE_PPU_MAIN_DISR

Device Interface Input Current Status Register

Address: 0x42211010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	PWR_DEVACTIVE_STATUS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None					R		
HW Access	None					RW		
Name	None [15:11]					PWR_DEVACTIVE_STATUS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	OP_DEVACTIVE_STATUS [31:24]							

Bits	Name	Description
31 : 24	OP_DEVACTIVE_STATUS	Reserved Default Value: 0x0
10 : 0	PWR_DEVACTIVE_STATUS	Status of the power mode DEVACTIVE inputs. There is one bit for each device interface Q-Channel DEVQACTIVE. For example, bit 0 is for Q-channel device 0 DEVQACTIVE. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x0

12.1.7 PWRMODE_PPU_MAIN_MISR

Miscellaneous Input Current Status Register

Address: 0x42211014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							PCSMPACCEPT_STATUS

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	DEVACCEPT_STATUS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	DEVDENY_STATUS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	DEVDENY_STATUS	Status of the device interface DEVDENY inputs. There is one bit for each device interface DEVQDENY. For example, bit 16 is for Q-Channel 0 DEVQDENY, and bit 17 for Q-Channel 1 DEVQDENY. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x0
15 : 8	DEVACCEPT_STATUS	Status of the device interface DEVACCEPT inputs. There is one bit for each device interface DEVQACCEPTn. For example, bit 8 is for Q-Channel 0 DEVQACCEPTn and bit 9 for Q-Channel 1 DEVQACCEPTn. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x0
0	PCSMPACCEPT_STATUS	The status of the PCSMPACCEPT input. Default Value: 0x0

12.1.8 PWRMODE_PPU_MAIN_STSR

Stored Status Register

Address: 0x42211018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	STORED_DEVDENY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	STORED_DEVDENY	Status of the DEVDENY signals from the last device interface Q-Channel transition. For Q-Channel: There is one bit for each device interface DEVQDENY. For example, bit 0 is for Q-Channel 0 DEVQDENY, and bit 1 for Q-Channel 1 DEVQDENY. Refer to PPU_DISR.PWR_DEVACTIVE_STATUS for device enumeration. Default Value: 0x0

12.1.9 PWRMODE_PPU_MAIN_UNLK

Unlock register

Address: 0x4221101C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							UNLOCK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	UNLOCK	Reserved Default Value: 0x0

12.1.10 PWRMODE_PPU_MAIN_PWCR

Power Configuration Register

Address: 0x42211020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DEVREQEN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PWR_DEVACTIVEEN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					R		
Name	None [23:19]					PWR_DEVACTIVEEN [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	OP_DEVACTIVEEN [31:24]							

Bits	Name	Description
31 : 24	OP_DEVACTIVEEN	Reserved Default Value: 0x00
18 : 8	PWR_DEVACTIVEEN	These bits enable the power mode DEVACTIVE inputs. When a bit is to 1 the related DEVACTIVE input is enabled, when set to 0 it is disabled. All available bits are reset to 1. There is one bit for each device interface Q-Channel DEVQACTIVE. For example, bit 8 is for the Q-Channel 0 DEVQACTIVE, and bit 9 for the Q-Channel 1 DEVQACTIVE. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x001
7 : 0	DEVREQEN	When set to 1 enables the device interface handshake for transitions. All available bits are reset to 1. There is one bit for each device interface channel. For example, bit 0 is for Q-Channel 0, and bit 1 is for Q-Channel 1. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x01

12.1.11 PWRMODE_PPU_MAIN_PTCR

Power Mode Transition Configuration Register

Address: 0x42211024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						DBG_RE-COV_POR ST_EN	WARM_RS T_DEVREQ EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	DBG_RE-COV_PORST_EN	Reserved Default Value: 0x0
0	WARM_RST_DEVREQEN	Transition behavior between ON and WARM_RST. This bit should not be modified when the PPU is in WARM_RST, or if the PPU is performing a transition, otherwise PPU behavior is UN-PREDICTABLE. 0: The PPU does not perform a device interface handshake when transitioning between ON and WARM_RST. 1: The PPU performs a device interface handshake when transitioning between ON and WARM_RST. This disables all Q-Channels for this transition. Default Value: 0x0

12.1.12 PWRMODE_PPU_MAIN_IMR

Interrupt Mask Register

Address: 0x42211030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		LOCKED_IRQ_MASK	EMU_DENY_IRQ_MASK	EMU_ACCEPT_IRQ_MASK	STA_DENY_IRQ_MASK	STA_ACCEPT_IRQ_MASK	STA_POLICY_TRN_IRQ_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	LOCKED_IRQ_MASK	Reserved Default Value: 0x0
4	EMU_DENY_IRQ_MASK	Reserved Default Value: 0x0
3	EMU_ACCEPT_IRQ_MASK	Reserved Default Value: 0x0
2	STA_DENY_IRQ_MASK	Static transition denial event mask. Default Value: 0x0
1	STA_ACCEPT_IRQ_MASK	Static transition acceptance event mask. For main PPU, keep this bit 1 to mask the event, otherwise the interrupt may trigger a wakeup. Default Value: 0x1
0	STA_POLICY_TRN_IRQ_MASK	Static full policy transition completion event mask. For main PPU, this bit has no function because no static transitions are supported (see PWPR.PWR_DYN_EN). Default Value: 0x0

12.1.13 PWRMODE_PPU_MAIN_AIMR

Additional Interrupt Mask Register

Address: 0x42211034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			STA_POLICY_OP_IRQ_MASK	STA_POLICY_PWR_IRQ_MASK	DYN_DENY_IRQ_MASK	DYN_ACCEPT_IRQ_MASK	UNSPT_POLICY_IRQ_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	STA_POLICY_OP_IRQ_MASK	Reserved Default Value: 0x0
3	STA_POLICY_PWR_IRQ_MASK	Reserved Default Value: 0x0
2	DYN_DENY_IRQ_MASK	Dynamic transition denial event mask. Default Value: 0x1
1	DYN_ACCEPT_IRQ_MASK	Dynamic transition acceptance event mask. For main PPU, keep this bit 1 to mask the event, otherwise the interrupt that occurs when entering a low power mode may trigger a wakeup. Default Value: 0x1
0	UNSPT_POLICY_IRQ_MASK	Unsupported Policy event mask. Default Value: 0x0

12.1.14 PWRMODE_PPU_MAIN_ISR

Interrupt Status Register

Address: 0x42211038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	None	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	None	R	R	R	R	R	R
Name	OTH-ER_IRQ	None	LOCKED_IRQ	EMU_DE-NY_IRQ	EMU_AC-CEPT_IRQ	STA_DE-NY_IRQ	STA_AC-CEPT_IRQ	STA_POLI-CY_TRN_IRQ

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	R							
Name	PWR_ACTIVE_EDGE_IRQ [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW1C		
HW Access	None					R		
Name	None [23:19]					PWR_ACTIVE_EDGE_IRQ [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	R							
Name	OP_ACTIVE_EDGE_IRQ [31:24]							

Bits	Name	Description
31 : 24	OP_ACTIVE_EDGE_IRQ	Indicates which operating mode DEVPACTIVE inputs caused the input edge event. When operating modes are not supported this field is reserved. Default Value: 0x0
18 : 8	PWR_ACTIVE_EDGE_IRQ	Indicates which power mode DEVACTIVE inputs caused the input edge event. Bits for unused channels are the MSBs and are reserved. There is one bit for each device Q-Channel DEVQACTIVE. For example, bit 8 is for the Q-Channel 0 DEVQACTIVE. Refer to PPU_IDR0.DEVCHAN for device channel enumeration. Default Value: 0x00
7	OTHER_IRQ	Indicates there is an interrupt event pending in the Additional Interrupt Status Register (PPU_AISR). Default Value: 0x0
5	LOCKED_IRQ	Reserved Default Value: 0x0
4	EMU_DENY_IRQ	Reserved Default Value: 0x0
3	EMU_ACCEPT_IRQ	Reserved Default Value: 0x0
2	STA_DENY_IRQ	Static transition denial event status. Default Value: 0x0
1	STA_ACCEPT_IRQ	Static transition acceptance event status. Default Value: 0x0

12.1.14 PWRMODE_PPU_MAIN_ISR (continued)

0	STA_POLICY_TRN_IRQ	Static full policy transition completion event status. Default Value: 0x0

12.1.15 PWRMODE_PPU_MAIN_AISR

Additional Interrupt Status Register

Address: 0x4221103C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None			R	R	R	R	R
Name	None [7:5]			STA_POLICY_OP_IRQ	STA_POLICY_PWR_IRQ	DYN_DENY_IRQ	DYN_ACCEPT_IRQ	UNSPT_POLICY_IRQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	STA_POLICY_OP_IRQ	Reserved Default Value: 0x0
3	STA_POLICY_PWR_IRQ	Reserved Default Value: 0x0
2	DYN_DENY_IRQ	Dynamic transition denial event status. Default Value: 0x0
1	DYN_ACCEPT_IRQ	Dynamic transition acceptance event status. Default Value: 0x0
0	UNSPT_POLICY_IRQ	Unsupported Policy event status. Default Value: 0x0

12.1.16 PWRMODE_PPU_MAIN_IESR

Input Edge Sensitivity Register

Address: 0x42211040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE03_EDGE [7:6]		DEVACTIVE02_EDGE [5:4]		DEVACTIVE01_EDGE [3:2]		DEVACTIVE00_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE07_EDGE [15:14]		DEVACTIVE06_EDGE [13:12]		DEVACTIVE05_EDGE [11:10]		DEVACTIVE04_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [23:22]		DEVACTIVE10_EDGE [21:20]		DEVACTIVE09_EDGE [19:18]		DEVACTIVE08_EDGE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21 : 20	DEVACTIVE10_EDGE	Reserved Default Value: 0x0
19 : 18	DEVACTIVE09_EDGE	Reserved Default Value: 0x0
17 : 16	DEVACTIVE08_EDGE	Reserved Default Value: 0x0
15 : 14	DEVACTIVE07_EDGE	Reserved Default Value: 0x0
13 : 12	DEVACTIVE06_EDGE	Reserved Default Value: 0x0
11 : 10	DEVACTIVE05_EDGE	Reserved Default Value: 0x0
9 : 8	DEVACTIVE04_EDGE	Reserved Default Value: 0x0
7 : 6	DEVACTIVE03_EDGE	Reserved Default Value: 0x0
5 : 4	DEVACTIVE02_EDGE	DEVACTIVE 2 edge sensitivity. Default Value: 0x0
3 : 2	DEVACTIVE01_EDGE	DEVACTIVE 1 edge sensitivity. Default Value: 0x0

12.1.16 PWRMODE_PPU_MAIN_IESR (continued)

1 : 0	DEVACTIVE00_EDGE	DEVACTIVE 0 edge sensitivity. Default Value: 0x0

12.1.17 PWRMODE_PPU_MAIN_OPSR

Operating Mode Active Edge Sensitivity Register

Address: 0x42211044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE19_EDGE [7:6]		DEVACTIVE18_EDGE [5:4]		DEVACTIVE17_EDGE [3:2]		DEVACTIVE16_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DEVACTIVE23_EDGE [15:14]		DEVACTIVE22_EDGE [13:12]		DEVACTIVE21_EDGE [11:10]		DEVACTIVE20_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 14	DEVACTIVE23_EDGE	Reserved Default Value: 0x0
13 : 12	DEVACTIVE22_EDGE	Reserved Default Value: 0x0
11 : 10	DEVACTIVE21_EDGE	Reserved Default Value: 0x0
9 : 8	DEVACTIVE20_EDGE	Reserved Default Value: 0x0
7 : 6	DEVACTIVE19_EDGE	Reserved Default Value: 0x0
5 : 4	DEVACTIVE18_EDGE	Reserved Default Value: 0x0
3 : 2	DEVACTIVE17_EDGE	Reserved Default Value: 0x0
1 : 0	DEVACTIVE16_EDGE	Reserved Default Value: 0x0

12.1.18 PWRMODE_PPU_MAIN_FUNRR

Functional Retention RAM Configuration Register

Address: 0x42211050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FUNC_RET_RAM_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	FUNC_RET_RAM_CFG	Reserved Default Value: 0x0

12.1.19 PWRMODE_PPU_MAIN_FULRR

Full Retention RAM Configuration Register

Address: 0x42211054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FULL_RET_RAM_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	FULL_RET_RAM_CFG	Reserved Default Value: 0x0

12.1.20 PWRMODE_PPU_MAIN_MEMRR

Memory Retention RAM Configuration Register

Address: 0x42211058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MEM_RET_RAM_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	MEM_RET_RAM_CFG	Reserved Default Value: 0x0

12.1.21 PWRMODE_PPU_MAIN_EDTR0

Power Mode Entry Delay Register 0

Address: 0x42211160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	OFF_DEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MEM_RET_DEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	LOGIC_RET_DEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	FULL_RET_DEL [31:24]							

Bits	Name	Description
31 : 24	FULL_RET_DEL	Reserved Default Value: 0x00
23 : 16	LOGIC_RET_DEL	Reserved Default Value: 0x00
15 : 8	MEM_RET_DEL	Reserved Default Value: 0x00
7 : 0	OFF_DEL	Reserved Default Value: 0x00

12.1.22 PWRMODE_PPU_MAIN_EDTR1

Power Mode Entry Delay Register 1

Address: 0x42211164

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MEM_OFF_DEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	FUNC_RET_DEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	FUNC_RET_DEL	Reserved Default Value: 0x00
7 : 0	MEM_OFF_DEL	Reserved Default Value: 0x00

12.1.23 PWRMODE_PPU_MAIN_DCDR0

Device Control Delay Configuration Register 0

Address: 0x42211170

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CLKEN_RST_DLY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	ISO_CLKEN_DLY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	RST_HWSTAT_DLY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	RST_HWSTAT_DLY	Reserved Default Value: 0x0
15 : 8	ISO_CLKEN_DLY	Reserved Default Value: 0x0
7 : 0	CLKEN_RST_DLY	Reserved Default Value: 0x0

12.1.24 PWRMODE_PPU_MAIN_DCDR1

Device Control Delay Configuration Register 1

Address: 0x42211174

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ISO_RST_DLY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CLKEN_ISO_DLY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	CLKEN_ISO_DLY	Reserved Default Value: 0x0
7 : 0	ISO_RST_DLY	Reserved Default Value: 0x0

12.1.25 PWRMODE_PPU_MAIN_IDR0

PPU Identification Register 0

Address: 0x42211FB0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	NUM_OPMODE [7:4]				DEVCHAN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	STA_-FUNC_RET_SPT	STA_-FULL_RET_SPT	STA_MEM_OFF_SPT	STA_LG-C_RET_SPT	STA_MEM_RET_EMU_SPT	STA_MEM_RET_SPT	STA_OFF_EMU_SPT	STA_OFF_SPT

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	None	R	R	R
HW Access	RW	RW	RW	RW	None	RW	RW	RW
Name	DY-N_MEM_RET_EMU_SPT	DY-N_MEM_RET_SPT	DY-N_OFF_EMU_SPT	DY-N_OFF_SPT	None	STA_DB-G_RE-COV_SPT	STA_WRM_RST_SPT	STA_ON_SPT

Bits	31	30	29	28	27	26	25	24
SW Access	None		R	R	R	R	R	R
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [31:30]		DY-N_WRM_RST_SPT	DY-N_ON_SPT	DYN_-FUNC_RET_SPT	DYN_-FULL_RET_SPT	DY-N_MEM_OFF_SPT	DYN_LG-C_RET_SPT

Bits	Name	Description
29	DYN_WRM_RST_SPT	Dynamic WARM_RST support. Default Value: 0x0
28	DYN_ON_SPT	Dynamic ON support. Default Value: 0x1
27	DYN_FUNC_RET_SPT	Dynamic FUNC_RET support. Default Value: 0x0
26	DYN_FULL_RET_SPT	Dynamic FULL_RET support. Default Value: 0x1
25	DYN_MEM_OFF_SPT	Dynamic MEM_OFF support. Default Value: 0x0
24	DYN_LGC_RET_SPT	Dynamic LOGIC_RET support. Default Value: 0x0
23	DY-N_MEM_RET_EMU_SPT	Dynamic MEM_RET_EMU support Default Value: 0x0
22	DYN_MEM_RET_SPT	Dynamic MEM_RET support. Default Value: 0x1

12.1.25 PWRMODE_PPU_MAIN_IDR0 (continued)

21	DYN_OFF_EMU_SPT	Dynamic OFF_EMU support. Default Value: 0x0
20	DYN_OFF_SPT	Dynamic OFF support. Default Value: 0x1
18	STA_DBG_RECOV_SPT	DBG_RECOV support. Default Value: 0x0
17	STA_WRM_RST_SPT	WARM_RST support. Ignore this bit. Do not use WARM_RST. Default Value: 0x1
16	STA_ON_SPT	ON support. Default Value: 0x1
15	STA_FUNC_RET_SPT	FUNC_RET support. Default Value: 0x0
14	STA_FULL_RET_SPT	FULL_RET support. Default Value: 0x1
13	STA_MEM_OFF_SPT	MEM_OFF support. Default Value: 0x0
12	STA_LGC_RET_SPT	LOGIC_RET support. Default Value: 0x0
11	STA_MEM_RET_EMU_SPT	MEM_RET_EMU support. Default Value: 0x0
10	STA_MEM_RET_SPT	MEM_RET support. Default Value: 0x1
9	STA_OFF_EMU_SPT	OFF_EMU support. Default Value: 0x0
8	STA_OFF_SPT	OFF support. Default Value: 0x1
7 : 4	NUM_OPMODE	No. of operating modes supported is NUM_OPMODE + 1. Default Value: 0x0
3 : 0	DEVCHAN	No. of Device Interface Channels. 0: This is a P-Channel PPU. Refer to PPU_IDR1.OP_ACTIVE for the number of DEVPACTIVE inputs and their meaning. non-zero: The value is the number of Q-Channels. The device enumeration is: Device 0: PDCM Default Value: 0x1

12.1.26 PWRMODE_PPU_MAIN_IDR1

PPU Identification Register 1

Address: 0x42211FB4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R	R	R	None	R	R	R
HW Access	None	RW	RW	RW	None	RW	RW	RW
Name	None	FUNC_RET_RAM_REG	FULL_RET_RAM_REG	MEM_RET_RAM_REG	None	LOCK_SPT	SW_DEV_DEL_SPT	PWR_MODE_ENTRY_DEL_SPT

Bits	15	14	13	12	11	10	9	8
SW Access	None			R	None	R	R	R
HW Access	None			RW	None	RW	RW	RW
Name	None [15:13]			OFF_MEM_RET_TRANS	None	OP_ACTIVE	STA_POLICY_OP_IRQ_SPT	STA_POLICY_PWR_IRQ_SPT

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	OFF_MEM_RET_TRANS	OFF to MEM_RET direct transition. Indicates if direct transitions from OFF to MEM_RET and from OFF_EMU to MEM_RET_EMU are supported. Default Value: 0x0
10	OP_ACTIVE	Operating mode use model for dynamic transitions. 0: Ladder use model. 1: Independent use model. When operating modes are not supported (PPU_IDR0.NUM_OPMODE==0), this field is reserved. Default Value: 0x0
9	STA_POLICY_OP_IRQ_SPT	Operating policy transition completion event status. Default Value: 0x0
8	STA_POLICY_PWR_IRQ_SPT	Power policy transition completion event status. Default Value: 0x0
6	FUNC_RET_RAM_REG	Indicates if the PPU_FUNRR register is present or reserved. 0: Reserved. 1: Present. Default Value: 0x0
5	FULL_RET_RAM_REG	Indicates if the PPU_FULRR register is present or reserved. 0: Reserved. 1: Present. Default Value: 0x0
4	MEM_RET_RAM_REG	Indicates if the PPU_MEMRR register is present or reserved. 0: Reserved. 1: Present. Default Value: 0x0

12.1.26 PWRMODE_PPU_MAIN_IDR1 (continued)

2	LOCK_SPT	Lock and the lock interrupt event are supported. Default Value: 0x0
1	SW_DEV_DEL_SPT	Software device delay control configuration support. Default Value: 0x0
0	PWR_MODE_EN-TRY_DEL_SPT	Power mode entry delay support. Default Value: 0x0

12.1.27 PWRMODE_PPU_MAIN_IIDR

Implementation Identification Register

Address: 0x42211FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	IMPLEMENTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R				R			
HW Access	RW				RW			
Name	REVISION [15:12]				IMPLEMENTER [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access	RW				RW			
Name	PRODUCT_ID [23:20]				VARIANT [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	PRODUCT_ID [31:24]							

Bits	Name	Description
31 : 20	PRODUCT_ID	PPU part identification. Default Value: 0x0B5
19 : 16	VARIANT	Major revision of the product. Default Value: 0
15 : 12	REVISION	Minor revision of the product. Default Value: 0
11 : 0	IMPLEMENTER	Implementer identification. [11:8] The JEP106 continuation code of the implementer. [7] Always 0. [6:0] The JEP106 identity code of the implementer. For an Arm implementation, bits [11:0] are 0x43B. Default Value: 0x43B

12.1.28 PWRMODE_PPU_MAIN_AIDR

Architecture Identification Register

Address: 0x42211FCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	ARCH_REV_MAJOR [7:4]				ARCH_REV_MINOR [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	ARCH_REV_MAJOR	0x1 - PPU architecture major revision 1. Other Values - Reserved. Default Value: 0x1
3 : 0	ARCH_REV_MINOR	0x1 - PPU Architecture minor revision 1. Other Values - Reserved. Default Value: 0x1

12.1.29 PWRMODE_CLK_SELECT

Clock Selection for Power Mode Components

Address: 0x42212000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CLK_PWR_DIV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						CLK_PWR_MUX [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 16	CLK_PWR_MUX	Selects a source for the clock used by power control components. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. It takes four cycles of the originally selected clock to switch away from it. Do not disable the original clock during this time. Default Value: 0 **0x0: IMO :** IMO - Internal R/C Oscillator **0x1: IHO :** IHO - Internal High-speed Oscillator **0x2: RESERVED :** reserved
7 : 0	CLK_PWR_DIV	clk_pwr is generated by dividing the CLK_PWR_MUX selection by (CLK_PWR_DIV+1). Default Value: 0

13 Backup registers

This section discusses the Backup registers. It lists all the registers in mapping tables, in address order.

13.1 Register details

Register	Address	Description
BACKUP_CTL	0x42220000	Control
BACKUP_RTC_RW	0x42220008	RTC Read Write register
BACKUP_CAL_CTL	0x4222000C	Oscillator calibration for absolute frequency
BACKUP_STATUS	0x42220010	Status
BACKUP_RTC_TIME	0x42220014	Calendar Seconds, Minutes, Hours, Day of Week
BACKUP_RTC_DATE	0x42220018	Calendar Day of Month, Month, Year
BACKUP_ALM1_TIME	0x4222001C	Alarm 1 Seconds, Minute, Hours, Day of Week
BACKUP_ALM1_DATE	0x42220020	Alarm 1 Day of Month, Month
BACKUP_ALM2_TIME	0x42220024	Alarm 2 Seconds, Minute, Hours, Day of Week
BACKUP_ALM2_DATE	0x42220028	Alarm 2 Day of Month, Month
BACKUP_INTR	0x4222002C	Interrupt request register
BACKUP_INTR_SET	0x42220030	Interrupt set request register
BACKUP_INTR_MASK	0x42220034	Interrupt mask register
BACKUP_INTR_MASKED	0x42220038	Interrupt masked request register
BACKUP_RESET	0x42220048	Backup reset register
BACKUP_WCO_STATUS	0x42220090	WCO Status Register
BACKUP_BREG_SET00	0x42221000	Backup register region 0
BACKUP_BREG_SET01	0x42221004	Backup register region 0. See BACKUP_BREG_SET00 for the details of bit fields.
BACKUP_BREG_SET02	0x42221008	Backup register region 0. See BACKUP_BREG_SET00 for the details of bit fields.
BACKUP_BREG_SET03	0x4222100C	Backup register region 0. See BACKUP_BREG_SET00 for the details of bit fields.
BACKUP_BREG_SET10	0x42221010	Backup register region 1
BACKUP_BREG_SET11	0x42221014	Backup register region 1. See BACKUP_BREG_SET10 for the details of bit fields.
BACKUP_BREG_SET12	0x42221018	Backup register region 1. See BACKUP_BREG_SET10 for the details of bit fields.
BACKUP_BREG_SET13	0x4222101C	Backup register region 1. See BACKUP_BREG_SET10 for the details of bit fields.
BACKUP_BREG_SET20	0x42221020	Backup register region 2
BACKUP_BREG_SET21	0x42221024	Backup register region 2. See BACKUP_BREG_SET20 for the details of bit fields.
BACKUP_BREG_SET22	0x42221028	Backup register region 2. See BACKUP_BREG_SET20 for the details of bit fields.

Backup registers

Register	Address	Description
BACKUP_BREG_SET23	0x4222102C	Backup register region 2. See BACKUP_BREG_SET20 for the details of bit fields.
BACKUP_BREG_SET24	0x42221030	Backup register region 2. See BACKUP_BREG_SET20 for the details of bit fields.
BACKUP_BREG_SET25	0x42221034	Backup register region 2. See BACKUP_BREG_SET20 for the details of bit fields.
BACKUP_BREG_SET26	0x42221038	Backup register region 2. See BACKUP_BREG_SET20 for the details of bit fields.
BACKUP_BREG_SET27	0x4222103C	Backup register region 2. See BACKUP_BREG_SET20 for the details of bit fields.
BACKUP_BREG_SET30	0x42221080	Backup register region 3
BACKUP_BREG_SET31	0x42221084	Backup register region 3. See BACKUP_BREG_SET30 for the details of bit fields.
BACKUP_BREG_SET32	0x42221088	Backup register region 3. See BACKUP_BREG_SET30 for the details of bit fields.
BACKUP_BREG_SET33	0x4222108C	Backup register region 3. See BACKUP_BREG_SET30 for the details of bit fields.
BACKUP_BREG_SET34	0x42221090	Backup register region 3. See BACKUP_BREG_SET30 for the details of bit fields.
BACKUP_BREG_SET35	0x42221094	Backup register region 3. See BACKUP_BREG_SET30 for the details of bit fields.
BACKUP_BREG_SET36	0x42221098	Backup register region 3. See BACKUP_BREG_SET30 for the details of bit fields.
BACKUP_BREG_SET37	0x4222109C	Backup register region 3. See BACKUP_BREG_SET30 for the details of bit fields.
BACKUP_BREG_SET38	0x422210A0	Backup register region 3. See BACKUP_BREG_SET30 for the details of bit fields.
BACKUP_BREG_SET39	0x422210A4	Backup register region 3. See BACKUP_BREG_SET30 for the details of bit fields.
BACKUP_BREG_SET310	0x422210A8	Backup register region 3. See BACKUP_BREG_SET30 for the details of bit fields.
BACKUP_BREG_SET311	0x422210AC	Backup register region 3. See BACKUP_BREG_SET30 for the details of bit fields.
BACKUP_BREG_SET312	0x422210B0	Backup register region 3. See BACKUP_BREG_SET30 for the details of bit fields.
BACKUP_BREG_SET313	0x422210B4	Backup register region 3. See BACKUP_BREG_SET30 for the details of bit fields.
BACKUP_BREG_SET314	0x422210B8	Backup register region 3. See BACKUP_BREG_SET30 for the details of bit fields.
BACKUP_BREG_SET315	0x422210BC	Backup register region 3. See BACKUP_BREG_SET30 for the details of bit fields.

13.1.1 BACKUP_CTL

Control

Address: 0x42220000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	None		
HW Access	None				A	None		
Name	None [7:4]				WCO_EN	None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW		
HW Access	None		A		None	A		
Name	None [15:14]		PRESCALER [13:12]		None	CLK_SEL [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW	RW		RW
HW Access	None				A	A		A
Name	None [23:20]				VBACK-UP_MEAS	VDDBAK_CTL [18:17]		WCO_BY-PASS

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	EN_CHARGE_KEY [31:24]							

Bits	Name	Description
31 : 24	EN_CHARGE_KEY	When set to 3C, the supercap charger circuit is enabled. Any other code disables the supercap charger. THIS CHARGING CIRCUIT IS FOR A SUPERCAP ONLY AND CANNOT SAFELY CHARGE A BATTERY. DO NOT WRITE THIS KEY WHEN VBACKUP IS CONNECTED TO A BATTERY. Enabling this supercap charger with a depleted supercap can cause a temporary IR drop on the power rail supplying the logic in the backup domain. During cold boot, FW can determine that this condition could exist by seeing that any backup domain register has been reset. The charging time is 2.2*R*C, where R=100Kohm. So for a 100uF supercap, FW should wait for the charging time of 22seconds before issuing BACKUP.RESET and then enabling the WCO/PILO/ILO clock source and expecting data in BREGs to be retained. Default Value: 0
19	VBACKUP_MEAS	Connect vbackup supply to the vbackup_meas output for measurement by an ADC attached to amuxbusa_adft_vddd. The vbackup_meas signal is scaled to 10% of vbackup, so it is within the supply range of the ADC. Default Value: 0
18 : 17	VDDBAK_CTL	Controls the behavior of the switch that generates vddbak from vbackup or vddd. 0: automatically select vddd if its brownout detector says it is valid. If the brownout says its not valid, then use vmax which is the highest of vddd or vbackup. 1,2,3: force vddbak and vmax to select vbackup, regardless of its voltage. Default Value: 0

13.1.1 BACKUP_CTL (continued)

16	WCO_BYPASS	Configures the WCO for different board-level connections to the WCO pins. For example, this can be used to connect an external watch crystal oscillator instead of a watch crystal. In all cases, the two related GPIO pins (WCO input and output pins) must be configured as analog connections using GPIO registers, and they must be hooked at the board level as described below. Configure this field before enabling the WCO, and do not change this setting when WCO_EN=1. 0: Watch crystal. Connect a 32.768 kHz watch crystal between WCO input and output pins. 1: Clock signal, either a square wave or sine wave. See PRESCALER field for connection information. Default Value: 0
13 : 12	PRESCALER	Prescaler for real time clock used when WCO_BYPASS=1 and CLK_SEL = WCO. Configure this field before enabling the WCO, and do not change this setting when WCO_EN=1. 0: 32768 Hz square wave. Connect a 32768 Hz square wave to WCO output pin. Do not connect WCO input pin. 1: 60 Hz sine wave. Connect an AC-coupled sine wave to WCO input pin. Do not connect the WCO output pin at the board level. When connecting to 120V, 60Hz mains, use a capacitive divider with 2.2nF (200V) from mains to WCO input and 220nF (6V) from WCO input to ground. 2: 50 Hz sine wave. Connect an AC-couple sine wave to WCO input pin. Do not connect the WCO output pin at the board level. When connecting to 220V, 50Hz mains, use a capacitive divider with 1nF (250V) from mains to WCO input and 220nF (6V) from WCO input to ground. 3: reserved Default Value: 0
10 : 8	CLK_SEL	Clock select for RTC clock Default Value: 0 **0x0: WCO :** Watch-crystal oscillator input, available in Active, DeepSleep, Hibernate, and XRES. For products with an independent vbackup supply, it can continue operating in OFF w/Backup mode. **0x1: ALTBAK :** This allows to use the LFCLK selection as an alternate backup domain clock. Note that LFCLK is only available in Active and DeepSleep power modes. Note that LFCLK clock glitches can propagate into the backup logic when the clock is stopped. For this reason, if the WCO or ILO is intended as the clock source then choose it directly instead of routing through LFCLK. **0x2: ILO :** Internal Low frequency Oscillator, available in Active, DeepSleep, Hibernate, and XRES. For products with an independent vbackup supply, it can continue operating in OFF w/Backup mode. For Hibernate operation CLK_ILO0_CONFIG. ILO_BACKUP must be set. If there are multiple ILO, this is ILO0. **0x3: LPECO_PRESCALER :** Low-power external crystal oscillator prescaler output, available in Active, DeepSleep, Hibernate, and XRES. For products with an independent vbackup supply, it can continue operating in OFF w/Backup mode. **0x4: PILO :** Precision internal low-speed oscillator, available in Active, DeepSleep, Hibernate, and XRES. For products with an independent vbackup supply, it can continue operating in OFF w/Backup mode.
3	WCO_EN	Watch-crystal oscillator (WCO) enable. If there is a write in progress when this bit is cleared, the WCO will be internally kept on until the write completes. After enabling the WCO software must wait until STATUS.WCO_OK=1 before configuring any component that depends on clk_lf/clk_bak, like for example RTC or WDTs. Follow the procedure in BACKUP_RTC_RW to access this bit. Default Value: 0

13.1.2 BACKUP_RTC_RW

RTC Read Write register

Address: 0x42220008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						A	A
Name	None [7:2]						WRITE	READ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	WRITE	Write bit Only when this bit is set can the RTC registers be written to (otherwise writes are ignored). This bit cannot be set if the RTC is still busy with a previous update (see RTC_BUSY bit) or if the Read bit is set or getting set. The user writes to the RTC user registers, when the Write bit is cleared by the user then the user registers content is copied to the actual RTC registers. Only user RTC registers that were written to will get copied, others will not be affected. When the SECONDS field is updated then TICKS will also be reset (WDT is not affected). When the Write bit is cleared by a reset (brown out/DeepSleep) then the RTC update will be ignored/lost. Do not set the Write bit if the RTC if the RTC is still busy with a previous update (see RTC_BUSY). Do not set the Write bit at the same time that the Read bit is cleared. Default Value: 0
0	READ	Read bit When this bit is set the RTC registers will be copied to user registers and frozen so that a coherent RTC value can safely be read. The RTC will keep on running. Do not set the read bit if the RTC is still busy with a previous update (see RTC_BUSY bit) or if the Write bit is set. Do not set the Read bit at the same time that the Write bit is cleared. Default Value: 0

13.1.3 BACKUP_CAL_CTL

Oscillator calibration for absolute frequency

Address: 0x4222000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW					
HW Access	None	A	A					
Name	None	CALIB_-SIGN	CALIB_VAL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						A	
Name	None [23:18]						CAL_COMP_PER_MIN [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None	RW		None			
HW Access	A	None	A		None			
Name	CAL_OUT	None	CAL_SEL [29:28]		None [27:24]			

Bits	Name	Description
31	CAL_OUT	Output enable for wave signal for calibration and allow CALIB_VAL to be written. Default Value: 0
29 : 28	CAL_SEL	Select calibration wave output signal Default Value: 0 **0x0: CAL512 :** 512Hz wave, not affected by calibration setting (not supported for 50/60Hz input clock: CTL.PRESCALER!=0) **0x1: RESERVED :** reserved **0x2: CAL2 :** 2Hz wave, includes the effect of the calibration setting, (not supported for 50/60Hz input clock: CTL.PRESCALER!=0) **0x3: CAL1 :** 1Hz wave, includes the effect of the calibration setting (supported for all input clocks)

13.1.3 BACKUP_CAL_CTL (continued)

17 : 16	CAL_COMP_PER_MIN	Select how many time calibration is performed per minute per step of 64 , each time a 64 step is added or substracted one unit 2/4/8/16*CALIB_VAL is substracted. Default Value: 0 **0x0: 2 :** Calibration of 64 each is performed twice per minute for 2*CALIB_VAL per hour **0x1: 4 :** Calibration of 64 each is performed four times per minute for 4*CALIB_VAL per hour **0x2: 8 :** Calibration of 64 each is performed eight times per minute for 8*CALIB_VAL per hour **0x3: 16 :** Calibration of 64 each is performed sixteen times per minute for 16*CALIB_VAL per hour
6	CALIB_SIGN	Calibration sign: 0= Negative sign: remove pulses (it takes more clock ticks to count one second) 1= Positive sign: add pulses (it takes less clock ticks to count one second) Default Value: 0
5 : 0	CALIB_VAL	Calibration value for absolute frequency (at a fixed temperature). Each step causes 128 ticks to be added or removed each hour. Effectively that means that each step is 1.085ppm (= 128/(60*60*32,768)) when CAL_COMP_PER_MIN is set at default value. Positive values 0x01-0x3c (1..60) add pulses, negative values remove pulses, thus giving a range of +/-65.1 ppm (limited by 60 minutes per hour, not the range of this field) when CAL_-COMP_PER_MIN is set at default value . Calibration is performed hourly, starting at 59 minutes and 59 seconds, and applied as 64 ticks every 30 seconds until there have been 2*CALIB_VAL adjustments when CAL_COM-P_PER_MIN is set at default value . Default Value: 0

13.1.4 BACKUP_STATUS

Status

Address: 0x42220010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	None	R
HW Access	None					W	None	W
Name	None [7:3]					WCO_OK	None	RTC_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	WCO_OK	Obsolete. Use WCO_STATUS.WCO_OK for future designs. Default Value: 0
0	RTC_BUSY	Pending RTC write Default Value: 0

13.1.5 BACKUP_RTC_TIME

Calendar Seconds, Minutes, Hours, Day of Week

Address: 0x42220014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		A					
Name	None [7:6]		RTC_SEC [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW					
HW Access	None		A					
Name	None [15:14]		RTC_MIN [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW	None	RW				
HW Access	None	A	None	A				
Name	None	CTRL_12HR	None	RTC_HOUR [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					A		
Name	None [31:27]					RTC_DAY [26:24]		

Bits	Name	Description
26 : 24	RTC_DAY	Calendar Day of the week, 1-7 It is up to the user to define the meaning of the values, but 1=Monday is recommended Default Value: 1
22	CTRL_12HR	Select 12/24HR mode: 1=12HR, 0=24HR Default Value: 0
20 : 16	RTC_HOUR	Calendar hours, value depending on 12/24HR mode 0=24HR: [20:16]=0-23 1=12HR: [20]:0=AM, 1=PM, [19:16]=1-12 Default Value: 0
13 : 8	RTC_MIN	Calendar minutes, 0-59 Default Value: 0
5 : 0	RTC_SEC	Calendar seconds, 0-59 Default Value: 0

13.1.6 BACKUP_RTC_DATE

Calendar Day of Month, Month, Year

Address: 0x42220018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			A				
Name	None [7:5]			RTC_DATE [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				A			
Name	None [15:12]				RTC_MON [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	A						
Name	None	RTC_YEAR [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
22 : 16	RTC_YEAR	Calendar year, 0-99 Default Value: 0
11 : 8	RTC_MON	Calendar Month, 1-12 Default Value: 1
4 : 0	RTC_DATE	Calendar Day of the Month, 1-31 Automatic Leap Year Correction Default Value: 1

13.1.7 BACKUP_ALM1_TIME

Alarm 1 Seconds, Minute, Hours, Day of Week

Address: 0x4222001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	None	RW					
HW Access	A	None	A					
Name	ALM_SEC_EN	None	ALM_SEC [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW	None	RW					
HW Access	A	None	A					
Name	ALM_MIN_EN	None	ALM_MIN [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None		RW				
HW Access	A	None		A				
Name	ALM_HOUR_EN	None [22:21]		ALM_HOUR [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None				RW		
HW Access	A	None				A		
Name	ALM_-DAY_EN	None [30:27]				ALM_DAY [26:24]		

Bits	Name	Description
31	ALM_DAY_EN	Alarm Day of the Week enable: 0=ignore, 1=match Default Value: 0
26 : 24	ALM_DAY	Alarm Day of the week, 1-7 It is up to the user to define the meaning of the values, but 1=Monday is recommended Default Value: 1
23	ALM_HOUR_EN	Alarm hour enable: 0=ignore, 1=match Default Value: 0
20 : 16	ALM_HOUR	Alarm hours, value depending on 12/24HR mode 24HR: [4:0]=0-23 12HR: [4]:0=AM, 1=PM, [3:0]=1-12 Default Value: 0
15	ALM_MIN_EN	Alarm minutes enable: 0=ignore, 1=match Default Value: 0
13 : 8	ALM_MIN	Alarm minutes, 0-59 Default Value: 0
7	ALM_SEC_EN	Alarm second enable: 0=ignore, 1=match Default Value: 0
5 : 0	ALM_SEC	Alarm seconds, 0-59 Default Value: 0

13.1.8 BACKUP_ALM1_DATE

Alarm 1 Day of Month, Month

Address: 0x42220020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	None		RW				
HW Access	A	None		A				
Name	ALM_-DATE_EN	None [6:5]		ALM_DATE [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	RW	None			RW			
HW Access	A	None			A			
Name	ALM_MON_EN	None [14:12]			ALM_MON [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	A	None						
Name	ALM_EN	None [30:24]						

Bits	Name	Description
31	ALM_EN	Master enable for alarm 1. 0: Alarm 1 is disabled. Fields for date and time are ignored. 1: Alarm 1 is enabled. Alarm triggers whenever the new date and time matches all the enabled date and time fields, which can happen more than once depending on configuration. If none of the date and time fields are enabled, then this alarm triggers once every second. Default Value: 0
15	ALM_MON_EN	Alarm Month enable: 0=ignore, 1=match Default Value: 0
11 : 8	ALM_MON	Alarm Month, 1-12 Default Value: 1
7	ALM_DATE_EN	Alarm Day of the Month enable: 0=ignore, 1=match Default Value: 0
4 : 0	ALM_DATE	Alarm Day of the Month, 1-31 Leap Year corrected Default Value: 1

13.1.9 BACKUP_ALM2_TIME

Alarm 2 Seconds, Minute, Hours, Day of Week

Address: 0x42220024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	None	RW					
HW Access	A	None	A					
Name	ALM_SEC_EN	None	ALM_SEC [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW	None	RW					
HW Access	A	None	A					
Name	ALM_MIN_EN	None	ALM_MIN [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None		RW				
HW Access	A	None		A				
Name	ALM_HOUR_EN	None [22:21]		ALM_HOUR [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None				RW		
HW Access	A	None				A		
Name	ALM_-DAY_EN	None [30:27]				ALM_DAY [26:24]		

Bits	Name	Description
31	ALM_DAY_EN	Alarm Day of the Week enable: 0=ignore, 1=match Default Value: 0
26 : 24	ALM_DAY	Alarm Day of the week, 1-7 It is up to the user to define the meaning of the values, but 1=Monday is recommended Default Value: 1
23	ALM_HOUR_EN	Alarm hour enable: 0=ignore, 1=match Default Value: 0
20 : 16	ALM_HOUR	Alarm hours, value depending on 12/24HR mode 24HR: [4:0]=0-23 12HR: [4]:0=AM, 1=PM, [3:0]=1-12 Default Value: 0
15	ALM_MIN_EN	Alarm minutes enable: 0=ignore, 1=match Default Value: 0
13 : 8	ALM_MIN	Alarm minutes, 0-59 Default Value: 0
7	ALM_SEC_EN	Alarm second enable: 0=ignore, 1=match Default Value: 0
5 : 0	ALM_SEC	Alarm seconds, 0-59 Default Value: 0

13.1.10 BACKUP_ALM2_DATE

Alarm 2 Day of Month, Month

Address: 0x42220028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	None		RW				
HW Access	A	None		A				
Name	ALM_-DATE_EN	None [6:5]		ALM_DATE [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	RW	None			RW			
HW Access	A	None			A			
Name	ALM_MON_EN	None [14:12]			ALM_MON [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	A	None						
Name	ALM_EN	None [30:24]						

Bits	Name	Description
31	ALM_EN	Master enable for alarm 2. 0: Alarm 2 is disabled. Fields for date and time are ignored. 1: Alarm 2 is enabled. Alarm triggers whenever the new date and time matches all the enabled date and time fields, which can happen more than once depending on configuration. If none of the date and time fields are enabled, then this alarm triggers once every second. Default Value: 0
15	ALM_MON_EN	Alarm Month enable: 0=ignore, 1=match Default Value: 0
11 : 8	ALM_MON	Alarm Month, 1-12 Default Value: 1
7	ALM_DATE_EN	Alarm Day of the Month enable: 0=ignore, 1=match Default Value: 0
4 : 0	ALM_DATE	Alarm Day of the Month, 1-31 Leap Year corrected Default Value: 1

13.1.11 BACKUP_INTR

Interrupt request register

Address: 0x4222002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [7:3]					CENTURY	ALARM2	ALARM1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CENTURY	Century overflow interrupt Default Value: 0
1	ALARM2	Alarm 2 Interrupt Default Value: 0
0	ALARM1	Alarm 1 Interrupt Default Value: 0

13.1.12 BACKUP_INTR_SET

Interrupt set request register

Address: 0x42220030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [7:3]					CENTURY	ALARM2	ALARM1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CENTURY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	ALARM2	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	ALARM1	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

13.1.13 BACKUP_INTR_MASK

Interrupt mask register

Address: 0x42220034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					CENTURY	ALARM2	ALARM1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CENTURY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	ALARM2	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	ALARM1	Mask bit for corresponding bit in interrupt request register. Default Value: 0

13.1.14 BACKUP_INTR_MASKED

Interrupt masked request register

Address: 0x42220038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					RW	RW	RW
Name	None [7:3]					CENTURY	ALARM2	ALARM1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CENTURY	Logical and of corresponding request and mask bits. Default Value: 0
1	ALARM2	Logical and of corresponding request and mask bits. Default Value: 0
0	ALARM1	Logical and of corresponding request and mask bits. Default Value: 0

13.1.15 BACKUP_RESET

Backup reset register

Address: 0x42220048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	None						
HW Access	A	None						
Name	RESET	None [30:24]						

Bits	Name	Description
31	RESET	Writing 1 to this register resets the backup logic. Hardware clears it when the reset is complete. After setting this register, firmware should confirm it reads as 0 before attempting to write other backup registers. Default Value: 0

13.1.16 BACKUP_WCO_STATUS

WCO Status Register

Address: 0x42220090

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	None	
HW Access	None					W	None	
Name	None [7:3]					WCO_OK	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	WCO_OK	Indicates that output has transitioned. Default Value: 0

13.1.17 BACKUP_BREG_SET00

Backup register region 0

Address: 0x42221000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	BREG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	BREG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	BREG [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	BREG [31:24]							

Bits	Name	Description
31 : 0	BREG	Backup memory that contains application-specific data. Memory is retained on vbackup supply. Default Value: 0

13.1.18 BACKUP_BREG_SET10

Backup register region 1

Address: 0x42221010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	BREG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	BREG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	BREG [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	BREG [31:24]							

Bits	Name	Description
31 : 0	BREG	Backup memory that contains application-specific data. Memory is retained on vbackup supply. Default Value: 0

13.1.19 BACKUP_BREG_SET20

Backup register region 2

Address: 0x42221020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	BREG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	BREG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	BREG [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	BREG [31:24]							

Bits	Name	Description
31 : 0	BREG	Backup memory that contains application-specific data. Memory is retained on vbackup supply. Default Value: 0

13.1.20 BACKUP_BREG_SET30

Backup register region 3

Address: 0x42221080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	BREG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	BREG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	BREG [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	BREG [31:24]							

Bits	Name	Description
31 : 0	BREG	Backup memory that contains application-specific data. Memory is retained on vbackup supply. Default Value: 0

14 IO Subsystem registers

This section discusses the IO Subsystem registers. It lists all the registers in mapping tables, in address order.

14.1 Register details

Register	Address	Description
HSIOM_PRT0_PORT_SEL0	0x42400000	Port selection 0
HSIOM_PRT1_PORT_SEL0	0x42400010	Port selection 0
HSIOM_PRT2_PORT_SEL0	0x42400020	Port selection 0. See HSIOM_PRT1_PORT_SEL0 for the details of bit fields.
HSIOM_PRT3_PORT_SEL0	0x42400030	Port selection 0. See HSIOM_PRT1_PORT_SEL0 for the details of bit fields.
HSIOM_PRT4_PORT_SEL0	0x42400040	Port selection 0. See HSIOM_PRT1_PORT_SEL0 for the details of bit fields.
HSIOM_PRT4_PORT_SEL1	0x42400044	Port selection 1
HSIOM_PRT5_PORT_SEL0	0x42400050	Port selection 0. See HSIOM_PRT1_PORT_SEL0 for the details of bit fields.
HSIOM_PRT6_PORT_SEL0	0x42400060	Port selection 0. See HSIOM_PRT1_PORT_SEL0 for the details of bit fields.
HSIOM_PRT7_PORT_SEL0	0x42400070	Port selection 0. See HSIOM_PRT1_PORT_SEL0 for the details of bit fields.
HSIOM_PRT7_PORT_SEL1	0x42400074	Port selection 1. See HSIOM_PRT4_PORT_SEL1 for the details of bit fields.
HSIOM_PRT8_PORT_SEL0	0x42400080	Port selection 0. See HSIOM_PRT1_PORT_SEL0 for the details of bit fields.
HSIOM_PRT8_PORT_SEL1	0x42400084	Port selection 1
HSIOM_PRT9_PORT_SEL0	0x42400090	Port selection 0. See HSIOM_PRT1_PORT_SEL0 for the details of bit fields.
HSIOM_PRT9_PORT_SEL1	0x42400094	Port selection 1. See HSIOM_PRT8_PORT_SEL1 for the details of bit fields.
HSIOM_SECURE_PRT0_NONSECURE_MASK	0x42401000	Non-Secure Mask
HSIOM_SECURE_PRT1_NONSECURE_MASK	0x42401010	Non-Secure Mask
HSIOM_SECURE_PRT2_NONSECURE_MASK	0x42401020	Non-Secure Mask. See HSIOM_SECURE_PRT1_NONSECURE_MASK for the details of bit fields.
HSIOM_SECURE_PRT3_NONSECURE_MASK	0x42401030	Non-Secure Mask. See HSIOM_SECURE_PRT1_NONSECURE_MASK for the details of bit fields.
HSIOM_SECURE_PRT4_NONSECURE_MASK	0x42401040	Non-Secure Mask

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Register	Address	Description
HSIOM_SECURE_PRT5_NONSECURE_MASK	0x42401050	Non-Secure Mask. See HSIOM_SECURE_PRT1_NONSECURE_MASK for the details of bit fields.
HSIOM_SECURE_PRT6_NONSECURE_MASK	0x42401060	Non-Secure Mask. See HSIOM_SECURE_PRT1_NONSECURE_MASK for the details of bit fields.
HSIOM_SECURE_PRT7_NONSECURE_MASK	0x42401070	Non-Secure Mask. See HSIOM_SECURE_PRT4_NONSECURE_MASK for the details of bit fields.
HSIOM_SECURE_PRT8_NONSECURE_MASK	0x42401080	Non-Secure Mask
HSIOM_SECURE_PRT9_NONSECURE_MASK	0x42401090	Non-Secure Mask. See HSIOM_SECURE_PRT8_NONSECURE_MASK for the details of bit fields.
HSIOM_AMUX_SPLIT_CTL0	0x42402000	AMUX splitter cell control
HSIOM_AMUX_SPLIT_CTL1	0x42402004	AMUX splitter cell control. See HSIOM_AMUX_SPLIT_CTL0 for the details of bit fields.
HSIOM_AMUX_SPLIT_CTL2	0x42402008	AMUX splitter cell control. See HSIOM_AMUX_SPLIT_CTL0 for the details of bit fields.
HSIOM_AMUX_SPLIT_CTL3	0x4240200C	AMUX splitter cell control. See HSIOM_AMUX_SPLIT_CTL0 for the details of bit fields.
GPIO_PRT0_OUT	0x42410000	Port output data register
GPIO_PRT0_OUT_CLR	0x42410004	Port output data clear register
GPIO_PRT0_OUT_SET	0x42410008	Port output data set register
GPIO_PRT0_OUT_INV	0x4241000C	Port output data invert register
GPIO_PRT0_IN	0x42410010	Port input state register
GPIO_PRT0_INTR	0x42410014	Port interrupt status register
GPIO_PRT0_INTR_MASK	0x42410018	Port interrupt mask register
GPIO_PRT0_INTR_MASKED	0x4241001C	Port interrupt masked status register
GPIO_PRT0_INTR_SET	0x42410020	Port interrupt set register
GPIO_PRT0_INTR_CFG	0x42410040	Port interrupt configuration register
GPIO_PRT0_CFG	0x42410044	Port configuration register
GPIO_PRT0_CFG_IN	0x42410048	Port input buffer configuration register
GPIO_PRT0_CFG_OUT	0x4241004C	Port output buffer configuration register
GPIO_PRT0_CFG_SLEW_EXT	0x42410064	Port output buffer slew extension configuration register
GPIO_PRT0_CFG_DRIVE_EXT0	0x42410068	Port output buffer drive sel extension configuration register
GPIO_PRT0_CFG_DRIVE_EXT1	0x4241006C	Port output buffer drive sel extension configuration register
GPIO_PRT1_OUT	0x42410080	Port output data register
GPIO_PRT1_OUT_CLR	0x42410084	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.

IO Subsystem registers

Register	Address	Description
GPIO_PRT1_OUT_SET	0x42410088	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT1_OUT_INV	0x4241008C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT1_IN	0x42410090	Port input state register
GPIO_PRT1_INTR	0x42410094	Port interrupt status register
GPIO_PRT1_INTR_MASK	0x42410098	Port interrupt mask register
GPIO_PRT1_INTR_MASKED	0x4241009C	Port interrupt masked status register
GPIO_PRT1_INTR_SET	0x424100A0	Port interrupt set register
GPIO_PRT1_INTR_CFG	0x424100C0	Port interrupt configuration register
GPIO_PRT1_CFG	0x424100C4	Port configuration register
GPIO_PRT1_CFG_IN	0x424100C8	Port input buffer configuration register
GPIO_PRT1_CFG_OUT	0x424100CC	Port output buffer configuration register
GPIO_PRT1_CFG_SLEW_EXT	0x424100E4	Port output buffer slew extension configuration register. See GPIO_PRT0_CFG_SLEW_EXT for the details of bit fields.
GPIO_PRT1_CFG_DRIVE_EXT0	0x424100E8	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT0 for the details of bit fields.
GPIO_PRT1_CFG_DRIVE_EXT1	0x424100EC	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT1 for the details of bit fields.
GPIO_PRT2_OUT	0x42410100	Port output data register. See GPIO_PRT1_OUT for the details of bit fields.
GPIO_PRT2_OUT_CLR	0x42410104	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT2_OUT_SET	0x42410108	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT2_OUT_INV	0x4241010C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT2_IN	0x42410110	Port input state register. See GPIO_PRT1_IN for the details of bit fields.
GPIO_PRT2_INTR	0x42410114	Port interrupt status register. See GPIO_PRT1_INTR for the details of bit fields.
GPIO_PRT2_INTR_MASK	0x42410118	Port interrupt mask register. See GPIO_PRT1_INTR_MASK for the details of bit fields.
GPIO_PRT2_INTR_MASKED	0x4241011C	Port interrupt masked status register. See GPIO_PRT1_INTR_MASKED for the details of bit fields.
GPIO_PRT2_INTR_SET	0x42410120	Port interrupt set register. See GPIO_PRT1_INTR_SET for the details of bit fields.
GPIO_PRT2_INTR_CFG	0x42410140	Port interrupt configuration register. See GPIO_PRT1_INTR_CFG for the details of bit fields.

IO Subsystem registers

Register	Address	Description
GPIO_PRT2_CFG	0x42410144	Port configuration register. See GPIO_PRT1_CFG for the details of bit fields.
GPIO_PRT2_CFG_IN	0x42410148	Port input buffer configuration register. See GPIO_PRT1_CFG_IN for the details of bit fields.
GPIO_PRT2_CFG_OUT	0x4241014C	Port output buffer configuration register. See GPIO_PRT1_CFG_OUT for the details of bit fields.
GPIO_PRT2_CFG_SLEW_EXT	0x42410164	Port output buffer slew extension configuration register. See GPIO_PRT0_CFG_SLEW_EXTfor the details of bit fields.
GPIO_PRT2_CFG_DRIVE_EXT0	0x42410168	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT0 for the details of bit fields.
GPIO_PRT2_CFG_DRIVE_EXT1	0x4241016C	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT1 for the details of bit fields.
GPIO_PRT3_OUT	0x42410180	Port output data register. See GPIO_PRT1_OUT for the details of bit fields.
GPIO_PRT3_OUT_CLR	0x42410184	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT3_OUT_SET	0x42410188	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT3_OUT_INV	0x4241018C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT3_IN	0x42410190	Port input state register. See GPIO_PRT1_IN for the details of bit fields.
GPIO_PRT3_INTR	0x42410194	Port interrupt status register. See GPIO_PRT1_INTR for the details of bit fields.
GPIO_PRT3_INTR_MASK	0x42410198	Port interrupt mask register. See GPIO_PRT1_INTR_MASK for the details of bit fields.
GPIO_PRT3_INTR_MASKED	0x4241019C	Port interrupt masked status register. See GPIO_PRT1_INTR_MASKED for the details of bit fields.
GPIO_PRT3_INTR_SET	0x424101A0	Port interrupt set register. See GPIO_PRT1_INTR_SET for the details of bit fields.
GPIO_PRT3_INTR_CFG	0x424101C0	Port interrupt configuration register. See GPIO_PRT1_INTR_CFG for the details of bit fields.
GPIO_PRT3_CFG	0x424101C4	Port configuration register. See GPIO_PRT1_CFG for the details of bit fields.
GPIO_PRT3_CFG_IN	0x424101C8	Port input buffer configuration register. See GPIO_PRT1_CFG_IN for the details of bit fields.
GPIO_PRT3_CFG_OUT	0x424101CC	Port output buffer configuration register. See GPIO_PRT1_CFG_OUT for the details of bit fields.

IO Subsystem registers

Register	Address	Description
GPIO_PRT3_CFG_SLEW_EXT	0x424101E4	Port output buffer slew extension configuration register. See GPIO_PRT0_CFG_SLEW_EXT for the details of bit fields.
GPIO_PRT3_CFG_DRIVE_EXT0	0x424101E8	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT0 for the details of bit fields.
GPIO_PRT3_CFG_DRIVE_EXT1	0x424101EC	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT1 for the details of bit fields.
GPIO_PRT4_OUT	0x42410200	Port output data register
GPIO_PRT4_OUT_CLR	0x42410204	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT4_OUT_SET	0x42410208	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT4_OUT_INV	0x4241020C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT4_IN	0x42410210	Port input state register
GPIO_PRT4_INTR	0x42410214	Port interrupt status register
GPIO_PRT4_INTR_MASK	0x42410218	Port interrupt mask register
GPIO_PRT4_INTR_MASKED	0x4241021C	Port interrupt masked status register
GPIO_PRT4_INTR_SET	0x42410220	Port interrupt set register
GPIO_PRT4_INTR_CFG	0x42410240	Port interrupt configuration register
GPIO_PRT4_CFG	0x42410244	Port configuration register
GPIO_PRT4_CFG_IN	0x42410248	Port input buffer configuration register
GPIO_PRT4_CFG_OUT	0x4241024C	Port output buffer configuration register
GPIO_PRT4_CFG_SLEW_EXT	0x42410264	Port output buffer slew extension configuration register. See GPIO_PRT0_CFG_SLEW_EXT for the details of bit fields.
GPIO_PRT4_CFG_DRIVE_EXT0	0x42410268	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT0 for the details of bit fields.
GPIO_PRT4_CFG_DRIVE_EXT1	0x4241026C	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT1 for the details of bit fields.
GPIO_PRT5_OUT	0x42410280	Port output data register. See GPIO_PRT1_OUT for the details of bit fields.
GPIO_PRT5_OUT_CLR	0x42410284	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT5_OUT_SET	0x42410288	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT5_OUT_INV	0x4241028C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.

IO Subsystem registers

Register	Address	Description
GPIO_PRT5_IN	0x42410290	Port input state register. See GPIO_PRT1_IN for the details of bit fields.
GPIO_PRT5_INTR	0x42410294	Port interrupt status register. See GPIO_PRT1_INTR for the details of bit fields.
GPIO_PRT5_INTR_MASK	0x42410298	Port interrupt mask register. See GPIO_PRT1_INTR_MASK for the details of bit fields.
GPIO_PRT5_INTR_MASKED	0x4241029C	Port interrupt masked status register. See GPIO_PRT1_INTR_MASKED for the details of bit fields.
GPIO_PRT5_INTR_SET	0x424102A0	Port interrupt set register. See GPIO_PRT1_INTR_SET for the details of bit fields.
GPIO_PRT5_INTR_CFG	0x424102C0	Port interrupt configuration register. See GPIO_PRT1_INTR_CFG for the details of bit fields.
GPIO_PRT5_CFG	0x424102C4	Port configuration register. See GPIO_PRT1_CFG for the details of bit fields.
GPIO_PRT5_CFG_IN	0x424102C8	Port input buffer configuration register. See GPIO_PRT1_CFG_IN for the details of bit fields.
GPIO_PRT5_CFG_OUT	0x424102CC	Port output buffer configuration register. See GPIO_PRT1_CFG_IN for the details of bit fields.
GPIO_PRT5_CFG_SLEW_EXT	0x424102E4	Port output buffer slew extension configuration register. See GPIO_PRT0_CFG_SLEW_EXT for the details of bit fields.
GPIO_PRT5_CFG_DRIVE_EXT0	0x424102E8	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT0 for the details of bit fields.
GPIO_PRT5_CFG_DRIVE_EXT1	0x424102EC	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT1 for the details of bit fields.
GPIO_PRT6_OUT	0x42410300	Port output data register. See GPIO_PRT1_OUT for the details of bit fields.
GPIO_PRT6_OUT_CLR	0x42410304	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT6_OUT_SET	0x42410308	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT6_OUT_INV	0x4241030C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT6_IN	0x42410310	Port input state register. See GPIO_PRT1_IN for the details of bit fields.
GPIO_PRT6_INTR	0x42410314	Port interrupt status register. See GPIO_PRT1_INTR for the details of bit fields.
GPIO_PRT6_INTR_MASK	0x42410318	Port interrupt mask register. See GPIO_PRT1_INTR_MASK for the details of bit fields.
GPIO_PRT6_INTR_MASKED	0x4241031C	Port interrupt masked status register. See GPIO_PRT1_INTR_MASKED for the details of bit fields.

IO Subsystem registers

Register	Address	Description
GPIO_PRT6_INTR_SET	0x42410320	Port interrupt set register. See GPIO_PRT1_INTR_SET for the details of bit fields.
GPIO_PRT6_INTR_CFG	0x42410340	Port interrupt configuration register. See GPIO_PRT1_INTR_CFG for the details of bit fields.
GPIO_PRT6_CFG	0x42410344	Port configuration register. See GPIO_PRT1_CFG for the details of bit fields.
GPIO_PRT6_CFG_IN	0x42410348	Port input buffer configuration register. See GPIO_PRT1_CFG_IN for the details of bit fields.
GPIO_PRT6_CFG_OUT	0x4241034C	Port output buffer configuration register. See GPIO_PRT1_CFG_OUT for the details of bit fields.
GPIO_PRT6_CFG_SLEW_EXT	0x42410364	Port output buffer slew extension configuration register. See GPIO_PRT0_CFG_SLEW_EXT for the details of bit fields.
GPIO_PRT6_CFG_DRIVE_EXT0	0x42410368	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT0 for the details of bit fields.
GPIO_PRT6_CFG_DRIVE_EXT1	0x4241036C	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT1 for the details of bit fields.
GPIO_PRT7_OUT	0x42410380	Port output data register. See GPIO_PRT4_OUT for the details of bit fields.
GPIO_PRT7_OUT_CLR	0x42410384	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT7_OUT_SET	0x42410388	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT7_OUT_INV	0x4241038C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT7_IN	0x42410390	Port input state register. See GPIO_PRT4_IN for the details of bit fields.
GPIO_PRT7_INTR	0x42410394	Port interrupt status register. See GPIO_PRT4_INTR for the details of bit fields.
GPIO_PRT7_INTR_MASK	0x42410398	Port interrupt mask register. See GPIO_PRT4_INTR_MASK for the details of bit fields.
GPIO_PRT7_INTR_MASKED	0x4241039C	Port interrupt masked status register. See GPIO_PRT4_INTR_MASK for the details of bit fields.
GPIO_PRT7_INTR_SET	0x424103A0	Port interrupt set register. See GPIO_PRT4_INTR_SET for the details of bit fields.
GPIO_PRT7_INTR_CFG	0x424103C0	Port interrupt configuration register. See GPIO_PRT4_INTR_CFG for the details of bit fields.
GPIO_PRT7_CFG	0x424103C4	Port configuration register. See GPIO_PRT4_CFG for the details of bit fields.
GPIO_PRT7_CFG_IN	0x424103C8	Port input buffer configuration register. See GPIO_PRT4_CFG_IN for the details of bit fields.

IO Subsystem registers

Register	Address	Description
GPIO_PRT7_CFG_OUT	0x424103CC	Port output buffer configuration register. See GPIO_PRT4_CFG_OUT for the details of bit fields.
GPIO_PRT7_CFG_SLEW_EXT	0x424103E4	Port output buffer slew extension configuration register. See GPIO_PRT0_CFG_SLEW_EXT for the details of bit fields.
GPIO_PRT7_CFG_DRIVE_EXT0	0x424103E8	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT0 for the details of bit fields.
GPIO_PRT7_CFG_DRIVE_EXT1	0x424103EC	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT1 for the details of bit fields.
GPIO_PRT8_OUT	0x42410400	Port output data register
GPIO_PRT8_OUT	0x42410404	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT8_OUT_SET	0x42410408	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT8_OUT_INV	0x4241040C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT8_IN	0x42410410	Port input state register
GPIO_PRT8_INTR	0x42410414	Port interrupt status register
GPIO_PRT8_INTR_MASK	0x42410418	Port interrupt mask register
GPIO_PRT8_INTR_MASKED	0x4241041C	Port interrupt masked status register
GPIO_PRT8_INTR_SET	0x42410420	Port interrupt set register
GPIO_PRT8_INTR_CFG	0x42410440	Port interrupt configuration register
GPIO_PRT8_CFG	0x42410444	Port configuration register
GPIO_PRT8_CFG_IN	0x42410448	Port input buffer configuration register
GPIO_PRT8_CFG_OUT	0x4241044C	Port output buffer configuration register
GPIO_PRT8_CFG_SLEW_EXT	0x42410464	Port output buffer slew extension configuration register. See GPIO_PRT0_CFG_SLEW_EXT for the details of bit fields.
GPIO_PRT8_CFG_DRIVE_EXT0	0x42410468	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT0 for the details of bit fields.
GPIO_PRT8_CFG_DRIVE_EXT1	0x4241046C	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT1 for the details of bit fields.
GPIO_PRT9_OUT	0x42410480	Port output data register. See GPIO_PRT8_OUT for the details of bit fields.
GPIO_PRT9_OUT_CLR	0x42410484	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT9_OUT_SET	0x42410488	Port output data set register. See GPIO_PRT0_OUT_CLR for the details of bit fields.

IO Subsystem registers

Register	Address	Description
GPIO_PRT9_OUT_INV	0x4241048C	Port output data invert register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT9_IN	0x42410490	Port input state register. See GPIO_PRT8_IN for the details of bit fields.
GPIO_PRT9_INTR	0x42410494	Port interrupt status register. See GPIO_PRT8_INTR for the details of bit fields.
GPIO_PRT9_INTR_MASK	0x42410498	Port interrupt mask register. See GPIO_PRT8_INTR_MASK for the details of bit fields.
GPIO_PRT9_INTR_MASKED	0x4241049C	Port interrupt masked status register. See GPIO_PRT8_INTR_MASKED for the details of bit fields.
GPIO_PRT9_INTR_SET	0x424104A0	Port interrupt set register. See GPIO_PRT8_INTR_SET for the details of bit fields.
GPIO_PRT9_INTR_CFG	0x424104C0	Port interrupt configuration register. See GPIO_PRT8_INTR_CFG for the details of bit fields.
GPIO_PRT9_CFG	0x424104C4	Port configuration register. See GPIO_PRT8_CFG for the details of bit fields.
GPIO_PRT9_CFG_IN	0x424104C8	Port input buffer configuration register. See GPIO_PRT8_CFG_IN for the details of bit fields.
GPIO_PRT9_CFG_OUT	0x424104CC	Port output buffer configuration register. See GPIO_PRT8_CFG_OUT for the details of bit fields.
GPIO_PRT9_CFG_SLEW_EXT	0x424104E4	Port output buffer slew extension configuration register. See GPIO_PRT0_CFG_SLEW_EXT for the details of bit fields.
GPIO_PRT9_CFG_DRIVE_EXT0	0x424104E8	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT0 for the details of bit fields.
GPIO_PRT9_CFG_DRIVE_EXT1	0x424104EC	Port output buffer drive sel extension configuration register. See GPIO_PRT0_CFG_DRIVE_EXT1 for the details of bit fields.
GPIO_SEC_INTR_CAUSE0	0x42417000	Secure Interrupt port cause register 0
GPIO_INTR_CAUSE0	0x42418000	Interrupt port cause register 0
GPIO_VDD_ACTIVE	0x42418010	Extern power supply detection register
GPIO_VDD_INTR	0x42418014	Supply detection interrupt register
GPIO_VDD_INTR_MASK	0x42418018	Supply detection interrupt mask register
GPIO_VDD_INTR_MASKED	0x4241801C	Supply detection interrupt masked register
GPIO_VDD_INTR_SET	0x42418020	Supply detection interrupt set register
SMARTIO_PRT0_CTL	0x42420000	Control register
SMARTIO_PRT0_SYNC_CTL	0x42420010	Synchronization control register
SMARTIO_PRT0_LUT_SEL0	0x42420020	LUT component input selection
SMARTIO_PRT0_LUT_SEL1	0x42420024	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.

IO Subsystem registers

Register	Address	Description
SMARTIO_PRT0_LUT_SEL2	0x42420028	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT0_LUT_SEL3	0x4242002C	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT0_LUT_SEL4	0x42420030	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT0_LUT_SEL5	0x42420034	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT0_LUT_SEL6	0x42420038	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT0_LUT_SEL7	0x4242003C	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT0_LUT_CTL0	0x42420040	LUT component control register
SMARTIO_PRT0_LUT_CTL1	0x42420044	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT0_LUT_CTL2	0x42420048	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT0_LUT_CTL3	0x4242004C	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT0_LUT_CTL4	0x42420050	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT0_LUT_CTL5	0x42420054	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT0_LUT_CTL6	0x42420058	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT0_LUT_CTL7	0x4242005C	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT0_DU_SEL	0x424200C0	Data unit component input selection
SMARTIO_PRT0_DU_CTL	0x424200C4	Data unit component control register
SMARTIO_PRT0_DATA	0x424200F0	Data register
SMARTIO_PRT1_CTL	0x42420100	Control register. See SMARTIO_PRT0_CTL for the details of bit fields.
SMARTIO_PRT1_SYNC_CTL	0x42420110	Synchronization control register. See SMARTIO_PRT0_SYNC_CTL for the details of bit fields.
SMARTIO_PRT1_LUT_SEL0	0x42420120	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT1_LUT_SEL1	0x42420124	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT1_LUT_SEL2	0x42420128	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT1_LUT_SEL3	0x4242012C	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.

IO Subsystem registers

Register	Address	Description
SMARTIO_PRT1_LUT_SEL4	0x42420130	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT1_LUT_SEL5	0x42420134	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT1_LUT_SEL6	0x42420138	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT1_LUT_SEL7	0x4242013C	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT1_LUT_CTL0	0x42420140	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT1_LUT_CTL1	0x42420144	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT1_LUT_CTL2	0x42420148	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT1_LUT_CTL3	0x4242014C	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT1_LUT_CTL4	0x42420150	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT1_LUT_CTL5	0x42420154	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT1_LUT_CTL6	0x42420158	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT1_LUT_CTL7	0x4242015C	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT1_DU_SEL	0x424201C0	Data unit component input selection. See SMARTIO_PRT0_DU_SEL for the details of bit fields.
SMARTIO_PRT1_DU_CTL	0x424201C4	Data unit component control register. See SMARTIO_PRT0_DU_CTL for the details of bit fields.
SMARTIO_PRT1_DATA	0x424201F0	Data register. See SMARTIO_PRT0_DATA for the details of bit fields.
SMARTIO_PRT2_CTL	0x42420200	Control register. See SMARTIO_PRT0_CTL for the details of bit fields.
SMARTIO_PRT2_SYNC_CTL	0x42420210	Synchronization control register. See SMARTIO_PRT0_SYNC_CTL for the details of bit fields.
SMARTIO_PRT2_LUT_SEL0	0x42420220	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT2_LUT_SEL1	0x42420224	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT2_LUT_SEL2	0x42420228	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT2_LUT_SEL3	0x4242022C	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.

IO Subsystem registers

Register	Address	Description
SMARTIO_PRT2_LUT_SEL4	0x42420230	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT2_LUT_SEL5	0x42420234	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT2_LUT_SEL6	0x42420238	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT2_LUT_SEL7	0x4242023C	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT2_LUT_CTL0	0x42420240	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT2_LUT_CTL1	0x42420244	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT2_LUT_CTL2	0x42420248	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT2_LUT_CTL3	0x4242024C	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT2_LUT_CTL4	0x42420250	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT2_LUT_CTL5	0x42420254	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT2_LUT_CTL6	0x42420258	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT2_LUT_CTL7	0x4242025C	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT2_DU_SEL	0x424202C0	Data unit component input selection. See SMARTIO_PRT0_DU_SEL for the details of bit fields.
SMARTIO_PRT2_DU_CTL	0x424202C4	Data unit component control register. See SMARTIO_PRT0_DU_CTL for the details of bit fields.
SMARTIO_PRT2_DATA	0x424202F0	Data register. See SMARTIO_PRT0_DATA for the details of bit fields.
SMARTIO_PRT3_CTL	0x42420300	Control register. See SMARTIO_PRT0_CTL for the details of bit fields.
SMARTIO_PRT3_SYNC_CTL	0x42420310	Synchronization control register. See SMARTIO_PRT0_SYNC_CTL for the details of bit fields.
SMARTIO_PRT3_LUT_SEL0	0x42420320	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT3_LUT_SEL1	0x42420324	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT3_LUT_SEL2	0x42420328	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT3_LUT_SEL3	0x4242032C	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.

IO Subsystem registers

Register	Address	Description
SMARTIO_PRT3_LUT_SEL4	0x42420330	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT3_LUT_SEL5	0x42420334	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT3_LUT_SEL6	0x42420338	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT3_LUT_SEL7	0x4242033C	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT3_LUT_CTL0	0x42420340	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT3_LUT_CTL1	0x42420344	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT3_LUT_CTL2	0x42420348	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT3_LUT_CTL3	0x4242034C	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT3_LUT_CTL4	0x42420350	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT3_LUT_CTL5	0x42420354	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT3_LUT_CTL6	0x42420358	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT3_LUT_CTL7	0x4242035C	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT3_DU_SEL	0x424203C0	Data unit component input selection. See SMARTIO_PRT0_DU_SEL for the details of bit fields.
SMARTIO_PRT3_DU_CTL	0x424203C4	Data unit component control register. See SMARTIO_PRT0_DU_CTL for the details of bit fields.
SMARTIO_PRT3_DATA	0x424203F0	Data register. See SMARTIO_PRT0_DATA for the details of bit fields.
SMARTIO_PRT5_CTL	0x42420500	Control register. See SMARTIO_PRT0_CTL for the details of bit fields.
SMARTIO_PRT5_SYNC_CTL	0x42420510	Synchronization control register. See SMARTIO_PRT0_SYNC_CTL for the details of bit fields.
SMARTIO_PRT5_LUT_SEL0	0x42420520	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT5_LUT_SEL1	0x42420524	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT5_LUT_SEL2	0x42420528	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT5_LUT_SEL3	0x4242052C	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.

IO Subsystem registers

Register	Address	Description
SMARTIO_PRT5_LUT_SEL4	0x42420530	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT5_LUT_SEL5	0x42420534	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT5_LUT_SEL6	0x42420538	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT5_LUT_SEL7	0x4242053C	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT5_LUT_CTL0	0x42420540	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT5_LUT_CTL1	0x42420544	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT5_LUT_CTL2	0x42420548	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT5_LUT_CTL3	0x4242054C	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT5_LUT_CTL4	0x42420550	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT5_LUT_CTL5	0x42420554	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT5_LUT_CTL6	0x42420558	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT5_LUT_CTL7	0x4242055C	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT5_DU_SEL	0x424205C0	Data unit component input selection. See SMARTIO_PRT0_DU_SEL for the details of bit fields.
SMARTIO_PRT5_DU_CTL	0x424205C4	Data unit component control register. See SMARTIO_PRT0_DU_CTL for the details of bit fields.
SMARTIO_PRT5_DATA	0x424205F0	Data register. See SMARTIO_PRT0_DATA for the details of bit fields.
SMARTIO_PRT6_CTL	0x42420600	Control register. See SMARTIO_PRT0_CTL for the details of bit fields.
SMARTIO_PRT6_SYNC_CTL	0x42420610	Synchronization control register. See SMARTIO_PRT0_SYNC_CTL for the details of bit fields.
SMARTIO_PRT6_LUT_SEL0	0x42420620	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT6_LUT_SEL1	0x42420624	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT6_LUT_SEL2	0x42420628	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT6_LUT_SEL3	0x4242062C	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.

IO Subsystem registers

Register	Address	Description
SMARTIO_PRT6_LUT_SEL4	0x42420630	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT6_LUT_SEL5	0x42420634	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT6_LUT_SEL6	0x42420638	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT6_LUT_SEL7	0x4242063C	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT6_LUT_CTL0	0x42420640	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT6_LUT_CTL1	0x42420644	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT6_LUT_CTL2	0x42420648	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT6_LUT_CTL3	0x4242064C	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT6_LUT_CTL4	0x42420650	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT6_LUT_CTL5	0x42420654	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT6_LUT_CTL6	0x42420658	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT6_LUT_CTL7	0x4242065C	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT6_DU_SEL	0x424206C0	Data unit component input selection. See SMARTIO_PRT0_DU_SEL for the details of bit fields.
SMARTIO_PRT6_DU_CTL	0x424206C4	Data unit component control register. See SMARTIO_PRT0_DU_CTL for the details of bit fields.
SMARTIO_PRT6_DATA	0x424206F0	Data register. See SMARTIO_PRT0_DATA for the details of bit fields.
SMARTIO_PRT9_CTL	0x42420900	Control register. See SMARTIO_PRT0_CTL for the details of bit fields.
SMARTIO_PRT9_SYNC_CTL	0x42420910	Synchronization control register. See SMARTIO_PRT0_SYNC_CTL for the details of bit fields.
SMARTIO_PRT9_LUT_SEL0	0x42420920	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT9_LUT_SEL1	0x42420924	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT9_LUT_SEL2	0x42420928	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT9_LUT_SEL3	0x4242092C	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.

IO Subsystem registers

Register	Address	Description
SMARTIO_PRT9_LUT_SEL4	0x42420930	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT9_LUT_SEL5	0x42420934	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT9_LUT_SEL6	0x42420938	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT9_LUT_SEL7	0x4242093C	LUT component input selection. See SMARTIO_PRT0_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT9_LUT_CTL0	0x42420940	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT9_LUT_CTL1	0x42420944	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT9_LUT_CTL2	0x42420948	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT9_LUT_CTL3	0x4242094C	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT9_LUT_CTL4	0x42420950	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT9_LUT_CTL5	0x42420954	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT9_LUT_CTL6	0x42420958	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT9_LUT_CTL7	0x4242095C	LUT component control register. See SMARTIO_PRT0_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT9_DU_SEL	0x424209C0	Data unit component input selection. See SMARTIO_PRT0_DU_SEL for the details of bit fields.
SMARTIO_PRT9_DU_CTL	0x424209C4	Data unit component control register. See SMARTIO_PRT0_DU_CTL for the details of bit fields.
SMARTIO_PRT9_DATA	0x424209F0	Data register. See SMARTIO_PRT0_DATA for the details of bit fields.

14.1.1 HSIOM_PRT0_PORT_SEL0

Port selection 0

Address: 0x42400000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			RW				
Name	None [7:5]			IO0_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			RW				
Name	None [15:13]			IO1_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12 : 8	IO1_SEL	Selects connection for IO pin 1 route. Default Value: 0
4 : 0	IO0_SEL	Selects connection for IO pin 0 route. Default Value: 0 **0x0: GPIO :** GPIO controls "out" **0x1: GPIO_DSI :** GPIO controls "out", DSI controls "output enable" **0x2: DSI_DSI :** DSI controls "out" and "output enable" **0x3: DSI_GPIO :** DSI controls "out", GPIO controls "output enable" **0x4: AMUXA :** Analog mux bus A

14.1.1 HSIOM_PRT0_PORT_SEL0 (continued)

0x5: AMUXB :

Analog mux bus B

0x6: AMUXA_DSI :

Analog mux bus A, DSI control

0x7: AMUXB_DSI :

Analog mux bus B, DSI control

0x8: ACT_0 :

Active functionality 0

0x9: ACT_1 :

Active functionality 1

0xa: ACT_2 :

Active functionality 2

0xb: ACT_3 :

Active functionality 3

0xc: DS_0 :

DeepSleep functionality 0

0xd: DS_1 :

DeepSleep functionality 1

0xe: DS_2 :

DeepSleep functionality 2

0xf: DS_3 :

DeepSleep functionality 3

0x10: ACT_4 :

Active functionality 4

0x11: ACT_5 :

Active functionality 5

0x12: ACT_6 :

Active functionality 6

14.1.1 HSIOM_PRT0_PORT_SEL0 (continued)

0x13: ACT_7 :

Active functionality 7

0x14: ACT_8 :

Active functionality 8

0x15: ACT_9 :

Active functionality 9

0x16: ACT_10 :

Active functionality 10

0x17: ACT_11 :

Active functionality 11

0x18: ACT_12 :

Active functionality 12

0x19: ACT_13 :

Active functionality 13

0x1a: ACT_14 :

Active functionality 14

0x1b: ACT_15 :

Active functionality 15

0x1c: DS_4 :

DeepSleep functionality 4

0x1d: DS_5 :

DeepSleep functionality 5

0x1e: DS_6 :

DeepSleep functionality 6

0x1f: DS_7 :

DeepSleep functionality 7

14.1.2 HSIOM_PRT1_PORT_SEL0

Port selection 0

Address: 0x42400010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			RW				
Name	None [7:5]			IO0_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			RW				
Name	None [15:13]			IO1_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			RW				
Name	None [23:21]			IO2_SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			RW				
Name	None [31:29]			IO3_SEL [28:24]				

Bits	Name	Description
28 : 24	IO3_SEL	Selects connection for IO pin 3 route. Default Value: 0
20 : 16	IO2_SEL	Selects connection for IO pin 2 route. Default Value: 0
12 : 8	IO1_SEL	Selects connection for IO pin 1 route. Default Value: 0
4 : 0	IO0_SEL	Selects connection for IO pin 0 route. Default Value: 0 **0x0: GPIO :** GPIO controls "out" **0x1: GPIO_DSI :** GPIO controls "out", DSI controls "output enable" **0x2: DSI_DSI :** DSI controls "out" and "output enable" **0x3: DSI_GPIO :** DSI controls "out", GPIO controls "output enable"

14.1.2 HSIOM_PRT1_PORT_SEL0 (continued)

0x4: AMUXA :

Analog mux bus A

0x5: AMUXB :

Analog mux bus B

0x6: AMUXA_DSI :

Analog mux bus A, DSI control

0x7: AMUXB_DSI :

Analog mux bus B, DSI control

0x8: ACT_0 :

Active functionality 0

0x9: ACT_1 :

Active functionality 1

0xa: ACT_2 :

Active functionality 2

0xb: ACT_3 :

Active functionality 3

0xc: DS_0 :

DeepSleep functionality 0

0xd: DS_1 :

DeepSleep functionality 1

0xe: DS_2 :

DeepSleep functionality 2

0xf: DS_3 :

DeepSleep functionality 3

0x10: ACT_4 :

Active functionality 4

0x11: ACT_5 :

Active functionality 5

14.1.2 HSIOM_PRT1_PORT_SEL0 (continued)

0x12: ACT_6 :

Active functionality 6

0x13: ACT_7 :

Active functionality 7

0x14: ACT_8 :

Active functionality 8

0x15: ACT_9 :

Active functionality 9

0x16: ACT_10 :

Active functionality 10

0x17: ACT_11 :

Active functionality 11

0x18: ACT_12 :

Active functionality 12

0x19: ACT_13 :

Active functionality 13

0x1a: ACT_14 :

Active functionality 14

0x1b: ACT_15 :

Active functionality 15

0x1c: DS_4 :

DeepSleep functionality 4

0x1d: DS_5 :

DeepSleep functionality 5

0x1e: DS_6 :

DeepSleep functionality 6

0x1f: DS_7 :

DeepSleep functionality 7

14.1.3 HSIOM_PRT4_PORT_SEL1

Port selection 1

Address: 0x42400044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			RW				
Name	None [7:5]			IO4_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			RW				
Name	None [15:13]			IO5_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			RW				
Name	None [23:21]			IO6_SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			RW				
Name	None [31:29]			IO7_SEL [28:24]				

Bits	Name	Description
28 : 24	IO7_SEL	Selects connection for IO pin 7 route. Default Value: 0
20 : 16	IO6_SEL	Selects connection for IO pin 6 route. Default Value: 0
12 : 8	IO5_SEL	Selects connection for IO pin 5 route. Default Value: 0
4 : 0	IO4_SEL	Selects connection for IO pin 4 route. See PORT_SEL0 for connection details. Default Value: 0

14.1.4 HSIOM_PRT8_PORT_SEL1

Port selection 1

Address: 0x42400084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			RW				
Name	None [7:5]			IO4_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			RW				
Name	None [15:13]			IO5_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12 : 8	IO5_SEL	Selects connection for IO pin 5 route. Default Value: 0
4 : 0	IO4_SEL	Selects connection for IO pin 4 route. See PORT_SEL0 for connection details. Default Value: 0

14.1.5 HSIOM_SECURE_PRT0_NONSECURE_MASK

Non-Secure Mask

Address: 0x42401000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW	RW
Name	None [7:2]						NONSE-CURE1	NONSE-CURE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	NONSECURE1	Non-secure attribute for IO1. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1
0	NONSECURE0	Non-secure attribute for IO0. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1

14.1.6 HSIOM_SECURE_PRT1_NONSECURE_MASK

Non-Secure Mask

Address: 0x42401010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				NONSE-CURE3	NONSE-CURE2	NONSE-CURE1	NONSE-CURE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	NONSECURE3	Non-secure attribute for IO3. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1
2	NONSECURE2	Non-secure attribute for IO2. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1
1	NONSECURE1	Non-secure attribute for IO1. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1
0	NONSECURE0	Non-secure attribute for IO0. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1

14.1.7 HSIOM_SECURE_PRT4_NONSECURE_MASK

Non-Secure Mask

Address: 0x42401040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	NONSE-CURE7	NONSE-CURE6	NONSE-CURE5	NONSE-CURE4	NONSE-CURE3	NONSE-CURE2	NONSE-CURE1	NONSE-CURE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	NONSECURE7	Non-secure attribute for IO7. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1
6	NONSECURE6	Non-secure attribute for IO6. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1
5	NONSECURE5	Non-secure attribute for IO5. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1
4	NONSECURE4	Non-secure attribute for IO4. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1
3	NONSECURE3	Non-secure attribute for IO3. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1
2	NONSECURE2	Non-secure attribute for IO2. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1

14.1.7 HSIOM_SECURE_PRT4_NONSECURE_MASK (continued)

1	NONSECURE1	Non-secure attribute for IO1. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1
0	NONSECURE0	Non-secure attribute for IO0. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1

14.1.8 HSIOM_SECURE_PRT8_NONSECURE_MASK

Non-Secure Mask

Address: 0x42401080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [7:6]		NONSE-CURE5	NONSE-CURE4	NONSE-CURE3	NONSE-CURE2	NONSE-CURE1	NONSE-CURE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	NONSECURE5	Non-secure attribute for IO5. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1
4	NONSECURE4	Non-secure attribute for IO4. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1
3	NONSECURE3	Non-secure attribute for IO3. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1
2	NONSECURE2	Non-secure attribute for IO2. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1
1	NONSECURE1	Non-secure attribute for IO1. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1
0	NONSECURE0	Non-secure attribute for IO0. 0 - Allows Secure access only. 1 - Allows Non-secure access only. Default Value: 1

14.1.9 HSIOM_AMUX_SPLIT_CTL0

AMUX splitter cell control

Address: 0x42402000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW	RW	RW
HW Access	None	R	R	R	None	R	R	R
Name	None	SWITCH_BB_S0	SWITCH_BB_SR	SWITCH_BB_SL	None	SWITCH_AA_S0	SWITCH_AA_SR	SWITCH_AA_SL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6	SWITCH_BB_S0	T-switch control for AMUXBUSB vssa/ground switch. Default Value: 0
5	SWITCH_BB_SR	T-switch control for Right AMUXBUSB switch. Default Value: 0
4	SWITCH_BB_SL	T-switch control for Left AMUXBUSB switch. Default Value: 0
2	SWITCH_AA_S0	T-switch control for AMUXBUSA vssa/ground switch: '0': switch open. '1': switch closed. Default Value: 0
1	SWITCH_AA_SR	T-switch control for Right AMUXBUSA switch: '0': switch open. '1': switch closed. Default Value: 0
0	SWITCH_AA_SL	T-switch control for Left AMUXBUSA switch: '0': switch open. '1': switch closed. Default Value: 0

14.1.10 GPIO_PRT0_OUT

Port output data register

Address: 0x42410000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW	RW
Name	None [7:2]						OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	OUT1	IO output data for pin 1 Default Value: 0
0	OUT0	IO output data for pin 0 '0': Output state set to '0' '1': Output state set to '1' Default Value: 0

14.1.11 GPIO_PRT0_OUT_CLR

Port output data clear register

Address: 0x42410004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	A	A	A	A	A	A	A	A
Name	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	OUT7	IO clear output for pin 7 Default Value: 0
6	OUT6	IO clear output for pin 6 Default Value: 0
5	OUT5	IO clear output for pin 5 Default Value: 0
4	OUT4	IO clear output for pin 4 Default Value: 0
3	OUT3	IO clear output for pin 3 Default Value: 0
2	OUT2	IO clear output for pin 2 Default Value: 0
1	OUT1	IO clear output for pin 1 Default Value: 0
0	OUT0	IO clear output for pin 0: '0': Output state not affected. '1': Output state set to '0'. Default Value: 0

14.1.12 GPIO_PRT0_OUT_SET

Port output data set register

Address: 0x42410008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	A	A	A	A	A	A	A	A
Name	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	OUT7	IO set output for pin 7 Default Value: 0
6	OUT6	IO set output for pin 6 Default Value: 0
5	OUT5	IO set output for pin 5 Default Value: 0
4	OUT4	IO set output for pin 4 Default Value: 0
3	OUT3	IO set output for pin 3 Default Value: 0
2	OUT2	IO set output for pin 2 Default Value: 0
1	OUT1	IO set output for pin 1 Default Value: 0
0	OUT0	IO set output for pin 0: '0': Output state not affected. '1': Output state set to '1'. Default Value: 0

14.1.13 GPIO_PRT0_OUT_INV

Port output data invert register

Address: 0x4241000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	A	A	A	A	A	A	A	A
Name	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	OUT7	IO invert output for pin 7 Default Value: 0
6	OUT6	IO invert output for pin 6 Default Value: 0
5	OUT5	IO invert output for pin 5 Default Value: 0
4	OUT4	IO invert output for pin 4 Default Value: 0
3	OUT3	IO invert output for pin 3 Default Value: 0
2	OUT2	IO invert output for pin 2 Default Value: 0
1	OUT1	IO invert output for pin 1 Default Value: 0
0	OUT0	IO invert output for pin 0: '0': Output state not affected. '1': Output state inverted ('0' => '1', '1' => '0'). Default Value: 0

14.1.14 GPIO_PRT0_IN

Port input state register

Address: 0x42410010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						IN1	IN0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_IN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_IN	Reads of this register return the logical state of the filtered pin as selected in the IN-TR_CFG.FLT_SEL register. Default Value: 0
1	IN1	IO pin state for pin 1 Default Value: 0
0	IN0	IO pin state for pin 0 '0': Low logic level present on pin. '1': High logic level present on pin. On reset assertion , IN register will get reset. The Pad value takes 2 clock cycles to be reflected into IN Register. The default value is transient. Default Value: 0

14.1.15 GPIO_PRT0_INTR

Port interrupt status register

Address: 0x42410014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						A	A
Name	None [7:2]						EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None						R	R
HW Access	None						W	W
Name	None [23:18]						IN_IN1	IN_IN0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							FLT_IN_IN

Bits	Name	Description
24	FLT_IN_IN	Filtered pin state for pin selected by INTR_CFG.FLT_SEL Default Value: 0
17	IN_IN1	IO pin state for pin 1 Default Value: 0
16	IN_IN0	IO pin state for pin 0 Default Value: 0
8	FLT_EDGE	Edge detected on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
1	EDGE1	Edge detect for IO pin 1 Default Value: 0
0	EDGE0	Edge detect for IO pin 0 '0': No edge was detected on pin. '1': An edge was detected on pin. Default Value: 0

14.1.16 GPIO_PRT0_INTR_MASK

Port interrupt mask register

Address: 0x42410018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Masks edge interrupt on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
1	EDGE1	Masks edge interrupt on IO pin 1 Default Value: 0
0	EDGE0	Masks edge interrupt on IO pin 0 '0': Pin interrupt forwarding disabled '1': Pin interrupt forwarding enabled Default Value: 0

14.1.17 GPIO_PRT0_INTR_MASKED

Port interrupt masked status register

Address: 0x4241001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Edge detected and masked on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
1	EDGE1	Edge detected and masked on IO pin 1 Default Value: 0
0	EDGE0	Edge detected AND masked on IO pin 0 '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU Default Value: 0

14.1.18 GPIO_PRT0_INTR_SET

Port interrupt set register

Address: 0x42410020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1S
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Sets edge detect interrupt for filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
1	EDGE1	Sets edge detect interrupt for IO pin 1 Default Value: 0
0	EDGE0	Sets edge detect interrupt for IO pin 0 '0': Interrupt state not affected '1': Interrupt set Default Value: 0

14.1.19 GPIO_PRT0_INTR_CFG

Port interrupt configuration register

Address: 0x42410040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [7:4]				EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by INTR_CFG.FLT_SEL Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pin 1 Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pin 0 Default Value: 0

14.1.19 GPIO_PRT0_INTR_CFG (continued)

0x0: DISABLE :

Disabled

0x1: RISING :

Rising edge

0x2: FALLING :

Falling edge

0x3: BOTH :

Both rising and falling edges

14.1.20 GPIO_PRT0_CFG

Port configuration register

Address: 0x42410044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN1	DRIVE_MODE1 [6:4]			IN_EN0	DRIVE_MODE0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	IN_EN1	Enables the input buffer for IO pin 1 Default Value: 0
6 : 4	DRIVE_MODE1	The GPIO drive mode for IO pin 1 Default Value: 0
3	IN_EN0	Enables the input buffer for IO pin 0. This bit should be cleared when analog signals are present on the pin to avoid crowbar currents. The output buffer can be used to drive analog signals high or low without issue. '0': Input buffer disabled '1': Input buffer enabled Default Value: 0
2 : 0	DRIVE_MODE0	The GPIO drive mode for IO pin 0. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0 **0x0: HIGHZ :** Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance

14.1.20 GPIO_PRT0_CFG (continued)

0x1: RESERVED :

This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases.
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance

0x2: PULLUP :

Resistive pull up
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Weak/resistive pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull up
D_OUT = '1': Weak/resistive pull up

0x3: PULLDOWN :

Resistive pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull down

14.1.20 GPIO_PRT0_CFG (continued)

0x4: OD_DRIVESLOW :

Open drain, drives low
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': High Impedance
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x5: OD_DRIVESHIGH :

Open drain, drives high
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': High Impedance
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x6: STRONG :

Strong D_OUTput buffer
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

14.1.20 GPIO_PRT0_CFG (continued)

0x7: PULLUP_DOWN :

Pull up or pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = '0':
GPIO_DSI_OUT = '0': Weak/resistive pull down
GPIO_DSI_OUT = '1': Weak/resistive pull up
where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT.
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull up

14.1.21 GPIO_PRT0_CFG_IN

Port input buffer configuration register

Address: 0x42410048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						VTRIP_-SEL1_0	VTRIP_-SEL0_0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	VTRIP_SEL1_0	Configures the pin 1 input buffer mode (trip points and hysteresis) Default Value: 0
0	VTRIP_SEL0_0	Configures the pin 0 input buffer mode (trip points and hysteresis) Default Value: 0 **0x0: CMOS :** Input buffer compatible with CMOS and I2C interfaces **0x1: TTL :** Input buffer compatible with TTL and MediaLB interfaces

14.1.22 GPIO_PRT0_CFG_OUT

Port output buffer configuration register

Address: 0x4241004C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [23:20]				DRIVE_SEL1 [19:18]		DRIVE_SEL0 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 18	DRIVE_SEL1	Sets the GPIO drive strength for IO pin 1 Default Value: 0
17 : 16	DRIVE_SEL0	Sets the GPIO drive strength for IO pin 0 Default Value: 0 **0x0: DRIVE_SEL_ZERO :** Full drive strength: Max drive current **0x1: DRIVE_SEL_ONE :** 1/2 drive strength: 1/2 drive current **0x2: DRIVE_SEL_TWO :** 1/4 drive strength: 1/4 drive current **0x3: DRIVE_SEL_THREE :** 1/8 drive strength: 1/8 drive current

14.1.23 GPIO_PRT0_CFG_SLEW_EXT

Port output buffer slew extension configuration register

Address: 0x42410064

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None			RW
HW Access	None			R	None			R
Name	None [7:5]			SLEW1	None [3:1]			SLEW0

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None			RW
HW Access	None			R	None			R
Name	None [15:13]			SLEW3	None [11:9]			SLEW2

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	None			RW
HW Access	None			R	None			R
Name	None [23:21]			SLEW5	None [19:17]			SLEW4

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	None			RW
HW Access	None			R	None			R
Name	None [31:29]			SLEW7	None [27:25]			SLEW6

Bits	Name	Description
28	SLEW7	Slew rate for IO pin 7 Default Value: 0
24	SLEW6	Slew rate for IO pin 6 Default Value: 0
20	SLEW5	Slew rate for IO pin 5 Default Value: 0
16	SLEW4	Slew rate for IO pin 4 Default Value: 0
12	SLEW3	Slew rate for IO pin 3 Default Value: 0
8	SLEW2	Slew rate for IO pin 2 Default Value: 0
4	SLEW1	Slew rate for IO pin 1 Default Value: 0
0	SLEW0	Enables slow slew rate for IO pin 0 '0': Fast slew rate '1': Slow slew rate Default Value: 0

14.1.24 GPIO_PRT0_CFG_DRIVE_EXT0

Port output buffer drive sel extension configuration register

Address: 0x42410068

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					DRIVE_SEL_EXT0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					R		
Name	None [15:11]					DRIVE_SEL_EXT1 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					R		
Name	None [23:19]					DRIVE_SEL_EXT2 [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					DRIVE_SEL_EXT3 [26:24]		

Bits	Name	Description
26 : 24	DRIVE_SEL_EXT3	Sets the GPIO drive strength for IO pin 3 Default Value: 0
18 : 16	DRIVE_SEL_EXT2	Sets the GPIO drive strength for IO pin 2 Default Value: 0
10 : 8	DRIVE_SEL_EXT1	Sets the GPIO drive strength for IO pin 1 Default Value: 0
2 : 0	DRIVE_SEL_EXT0	Sets the GPIO drive strength for IO pin 0 Default Value: 0

14.1.25 GPIO_PRT0_CFG_DRIVE_EXT1

Port output buffer drive sel extension configuration register

Address: 0x4241006C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					DRIVE_SEL_EXT4 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					R		
Name	None [15:11]					DRIVE_SEL_EXT5 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					R		
Name	None [23:19]					DRIVE_SEL_EXT6 [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					DRIVE_SEL_EXT7 [26:24]		

Bits	Name	Description
26 : 24	DRIVE_SEL_EXT7	Sets the GPIO drive strength for IO pin 7 Default Value: 0
18 : 16	DRIVE_SEL_EXT6	Sets the GPIO drive strength for IO pin 6 Default Value: 0
10 : 8	DRIVE_SEL_EXT5	Sets the GPIO drive strength for IO pin 5 Default Value: 0
2 : 0	DRIVE_SEL_EXT4	Sets the GPIO drive strength for IO pin 4 Default Value: 0

14.1.26 GPIO_PRT1_OUT

Port output data register

Address: 0x42410080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	OUT3	IO output data for pin 3 Default Value: 0
2	OUT2	IO output data for pin 2 Default Value: 0
1	OUT1	IO output data for pin 1 Default Value: 0
0	OUT0	IO output data for pin 0 '0': Output state set to '0' '1': Output state set to '1' Default Value: 0

14.1.27 GPIO_PRT1_IN

Port input state register

Address: 0x42410090

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				IN3	IN2	IN1	IN0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_IN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_IN	Reads of this register return the logical state of the filtered pin as selected in the IN-TR_CFG.FLT_SEL register. Default Value: 0
3	IN3	IO pin state for pin 3 Default Value: 0
2	IN2	IO pin state for pin 2 Default Value: 0
1	IN1	IO pin state for pin 1 Default Value: 0
0	IN0	IO pin state for pin 0 '0': Low logic level present on pin. '1': High logic level present on pin. On reset assertion , IN register will get reset. The Pad value takes 2 clock cycles to be reflected into IN Register. The default value is transient. Default Value: 0

14.1.28 GPIO_PRT1_INTR

Port interrupt status register

Address: 0x42410094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [23:20]				IN_IN3	IN_IN2	IN_IN1	IN_IN0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							FLT_IN_IN

Bits	Name	Description
24	FLT_IN_IN	Filtered pin state for pin selected by INTR_CFG.FLT_SEL Default Value: 0
19	IN_IN3	IO pin state for pin 3 Default Value: 0
18	IN_IN2	IO pin state for pin 2 Default Value: 0
17	IN_IN1	IO pin state for pin 1 Default Value: 0
16	IN_IN0	IO pin state for pin 0 Default Value: 0
8	FLT_EDGE	Edge detected on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
3	EDGE3	Edge detect for IO pin 3 Default Value: 0
2	EDGE2	Edge detect for IO pin 2 Default Value: 0
1	EDGE1	Edge detect for IO pin 1 Default Value: 0
0	EDGE0	Edge detect for IO pin 0 '0': No edge was detected on pin. '1': An edge was detected on pin. Default Value: 0

14.1.29 GPIO_PRT1_INTR_MASK

Port interrupt mask register

Address: 0x42410098

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Masks edge interrupt on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
3	EDGE3	Masks edge interrupt on IO pin 3 Default Value: 0
2	EDGE2	Masks edge interrupt on IO pin 2 Default Value: 0
1	EDGE1	Masks edge interrupt on IO pin 1 Default Value: 0
0	EDGE0	Masks edge interrupt on IO pin 0 '0': Pin interrupt forwarding disabled '1': Pin interrupt forwarding enabled Default Value: 0

14.1.30 GPIO_PRT1_INTR_MASKED

Port interrupt masked status register

Address: 0x4241009C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Edge detected and masked on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
3	EDGE3	Edge detected and masked on IO pin 3 Default Value: 0
2	EDGE2	Edge detected and masked on IO pin 2 Default Value: 0
1	EDGE1	Edge detected and masked on IO pin 1 Default Value: 0
0	EDGE0	Edge detected AND masked on IO pin 0 '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU Default Value: 0

14.1.31 GPIO_PRT1_INTR_SET

Port interrupt set register

Address: 0x424100A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [7:4]				EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1S
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Sets edge detect interrupt for filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
3	EDGE3	Sets edge detect interrupt for IO pin 3 Default Value: 0
2	EDGE2	Sets edge detect interrupt for IO pin 2 Default Value: 0
1	EDGE1	Sets edge detect interrupt for IO pin 1 Default Value: 0
0	EDGE0	Sets edge detect interrupt for IO pin 0 '0': Interrupt state not affected '1': Interrupt set Default Value: 0

14.1.32 GPIO_PRT1_INTR_CFG

Port interrupt configuration register

Address: 0x424100C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by INTR_CFG.FLT_SEL Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pin 3 Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pin 2 Default Value: 0

14.1.32 GPIO_PRT1_INTR_CFG (continued)

3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pin 1 Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pin 0 Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges

14.1.33 GPIO_PRT1_CFG

Port configuration register

Address: 0x424100C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN1	DRIVE_MODE1 [6:4]			IN_EN0	DRIVE_MODE0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN3	DRIVE_MODE3 [14:12]			IN_EN2	DRIVE_MODE2 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	IN_EN3	Enables the input buffer for IO pin 3 Default Value: 0
14 : 12	DRIVE_MODE3	The GPIO drive mode for IO pin 3 Default Value: 0
11	IN_EN2	Enables the input buffer for IO pin 2 Default Value: 0
10 : 8	DRIVE_MODE2	The GPIO drive mode for IO pin 2 Default Value: 0
7	IN_EN1	Enables the input buffer for IO pin 1 Default Value: 0
6 : 4	DRIVE_MODE1	The GPIO drive mode for IO pin 1 Default Value: 0
3	IN_EN0	Enables the input buffer for IO pin 0. This bit should be cleared when analog signals are present on the pin to avoid crowbar currents. The output buffer can be used to drive analog signals high or low without issue. '0': Input buffer disabled '1': Input buffer enabled Default Value: 0

14.1.33 GPIO_PRT1_CFG (continued)

2 : 0	DRIVE_MODE0	The GPIO drive mode for IO pin 0. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0 **0x0: HIGHZ :** Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance **0x1: RESERVED :** This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance **0x2: PULLUP :** Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up

14.1.33 GPIO_PRT1_CFG (continued)

0x3: PULLDOWN :

Resistive pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull down

0x4: OD_DRIVESLOW :

Open drain, drives low
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': High Impedance
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x5: OD_DRIVESHIGH :

Open drain, drives high
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': High Impedance
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

14.1.33 GPIO_PRT1_CFG (continued)

0x6: STRONG :

Strong D_OUTput buffer
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x7: PULLUP_DOWN :

Pull up or pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = '0':
GPIO_DSI_OUT = '0': Weak/resistive pull down
GPIO_DSI_OUT = '1': Weak/resistive pull up
where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT.
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull up

14.1.34 GPIO_PRT1_CFG_IN

Port input buffer configuration register

Address: 0x424100C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				VTRIP_-SEL3_0	VTRIP_-SEL2_0	VTRIP_-SEL1_0	VTRIP_-SEL0_0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	VTRIP_SEL3_0	Configures the pin 3 input buffer mode (trip points and hysteresis) Default Value: 0
2	VTRIP_SEL2_0	Configures the pin 2 input buffer mode (trip points and hysteresis) Default Value: 0
1	VTRIP_SEL1_0	Configures the pin 1 input buffer mode (trip points and hysteresis) Default Value: 0
0	VTRIP_SEL0_0	Configures the pin 0 input buffer mode (trip points and hysteresis) Default Value: 0 **0x0: CMOS :** Input buffer compatible with CMOS and I2C interfaces **0x1: TTL :** Input buffer compatible with TTL and MediaLB interfaces

14.1.35 GPIO_PRT1_CFG_OUT

Port output buffer configuration register

Address: 0x424100CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DRIVE_SEL3 [23:22]		DRIVE_SEL2 [21:20]		DRIVE_SEL1 [19:18]		DRIVE_SEL0 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 22	DRIVE_SEL3	Sets the GPIO drive strength for IO pin 3 Default Value: 0
21 : 20	DRIVE_SEL2	Sets the GPIO drive strength for IO pin 2 Default Value: 0
19 : 18	DRIVE_SEL1	Sets the GPIO drive strength for IO pin 1 Default Value: 0
17 : 16	DRIVE_SEL0	Sets the GPIO drive strength for IO pin 0 Default Value: 0 **0x0: DRIVE_SEL_ZERO :** Full drive strength: Max drive current **0x1: DRIVE_SEL_ONE :** 1/2 drive strength: 1/2 drive current **0x2: DRIVE_SEL_TWO :** 1/4 drive strength: 1/4 drive current **0x3: DRIVE_SEL_THREE :** 1/8 drive strength: 1/8 drive current

14.1.36 GPIO_PRT4_OUT

Port output data register

Address: 0x42410200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	OUT7	IO output data for pin 7 Default Value: 0
6	OUT6	IO output data for pin 6 Default Value: 0
5	OUT5	IO output data for pin 5 Default Value: 0
4	OUT4	IO output data for pin 4 Default Value: 0
3	OUT3	IO output data for pin 3 Default Value: 0
2	OUT2	IO output data for pin 2 Default Value: 0
1	OUT1	IO output data for pin 1 Default Value: 0
0	OUT0	IO output data for pin 0 '0': Output state set to '0' '1': Output state set to '1' Default Value: 0

14.1.37 GPIO_PRT4_IN

Port input state register

Address: 0x42410210

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_IN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_IN	Reads of this register return the logical state of the filtered pin as selected in the IN-TR_CFG.FLT_SEL register. Default Value: 0
7	IN7	IO pin state for pin 7 Default Value: 0
6	IN6	IO pin state for pin 6 Default Value: 0
5	IN5	IO pin state for pin 5 Default Value: 0
4	IN4	IO pin state for pin 4 Default Value: 0
3	IN3	IO pin state for pin 3 Default Value: 0
2	IN2	IO pin state for pin 2 Default Value: 0
1	IN1	IO pin state for pin 1 Default Value: 0
0	IN0	IO pin state for pin 0 '0': Low logic level present on pin. '1': High logic level present on pin. On reset assertion , IN register will get reset. The Pad value takes 2 clock cycles to be reflected into IN Register. The default value is transient. Default Value: 0

14.1.38 GPIO_PRT4_INTR

Port interrupt status register

Address: 0x42410214

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	IN_IN7	IN_IN6	IN_IN5	IN_IN4	IN_IN3	IN_IN2	IN_IN1	IN_IN0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							FLT_IN_IN

Bits	Name	Description
24	FLT_IN_IN	Filtered pin state for pin selected by INTR_CFG.FLT_SEL Default Value: 0
23	IN_IN7	IO pin state for pin 7 Default Value: 0
22	IN_IN6	IO pin state for pin 6 Default Value: 0
21	IN_IN5	IO pin state for pin 5 Default Value: 0
20	IN_IN4	IO pin state for pin 4 Default Value: 0
19	IN_IN3	IO pin state for pin 3 Default Value: 0
18	IN_IN2	IO pin state for pin 2 Default Value: 0
17	IN_IN1	IO pin state for pin 1 Default Value: 0
16	IN_IN0	IO pin state for pin 0 Default Value: 0
8	FLT_EDGE	Edge detected on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Edge detect for IO pin 7 Default Value: 0

14.1.38 GPIO_PRT4_INTR (continued)

6	EDGE6	Edge detect for IO pin 6 Default Value: 0
5	EDGE5	Edge detect for IO pin 5 Default Value: 0
4	EDGE4	Edge detect for IO pin 4 Default Value: 0
3	EDGE3	Edge detect for IO pin 3 Default Value: 0
2	EDGE2	Edge detect for IO pin 2 Default Value: 0
1	EDGE1	Edge detect for IO pin 1 Default Value: 0
0	EDGE0	Edge detect for IO pin 0 '0': No edge was detected on pin. '1': An edge was detected on pin. Default Value: 0

14.1.39 GPIO_PRT4_INTR_MASK

Port interrupt mask register

Address: 0x42410218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Masks edge interrupt on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Masks edge interrupt on IO pin 7 Default Value: 0
6	EDGE6	Masks edge interrupt on IO pin 6 Default Value: 0
5	EDGE5	Masks edge interrupt on IO pin 5 Default Value: 0
4	EDGE4	Masks edge interrupt on IO pin 4 Default Value: 0
3	EDGE3	Masks edge interrupt on IO pin 3 Default Value: 0
2	EDGE2	Masks edge interrupt on IO pin 2 Default Value: 0
1	EDGE1	Masks edge interrupt on IO pin 1 Default Value: 0
0	EDGE0	Masks edge interrupt on IO pin 0 '0': Pin interrupt forwarding disabled '1': Pin interrupt forwarding enabled Default Value: 0

14.1.40 GPIO_PRT4_INTR_MASKED

Port interrupt masked status register

Address: 0x4241021C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Edge detected and masked on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Edge detected and masked on IO pin 7 Default Value: 0
6	EDGE6	Edge detected and masked on IO pin 6 Default Value: 0
5	EDGE5	Edge detected and masked on IO pin 5 Default Value: 0
4	EDGE4	Edge detected and masked on IO pin 4 Default Value: 0
3	EDGE3	Edge detected and masked on IO pin 3 Default Value: 0
2	EDGE2	Edge detected and masked on IO pin 2 Default Value: 0
1	EDGE1	Edge detected and masked on IO pin 1 Default Value: 0
0	EDGE0	Edge detected AND masked on IO pin 0 '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU Default Value: 0

14.1.41 GPIO_PRT4_INTR_SET

Port interrupt set register

Address: 0x42410220

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1S
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Sets edge detect interrupt for filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Sets edge detect interrupt for IO pin 7 Default Value: 0
6	EDGE6	Sets edge detect interrupt for IO pin 6 Default Value: 0
5	EDGE5	Sets edge detect interrupt for IO pin 5 Default Value: 0
4	EDGE4	Sets edge detect interrupt for IO pin 4 Default Value: 0
3	EDGE3	Sets edge detect interrupt for IO pin 3 Default Value: 0
2	EDGE2	Sets edge detect interrupt for IO pin 2 Default Value: 0
1	EDGE1	Sets edge detect interrupt for IO pin 1 Default Value: 0
0	EDGE0	Sets edge detect interrupt for IO pin 0 '0': Interrupt state not affected '1': Interrupt set Default Value: 0

14.1.42 GPIO_PRT4_INTR_CFG

Port interrupt configuration register

Address: 0x42410240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by INTR_CFG.FLT_SEL Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges
15 : 14	EDGE7_SEL	Sets which edge will trigger an IRQ for IO pin 7 Default Value: 0
13 : 12	EDGE6_SEL	Sets which edge will trigger an IRQ for IO pin 6 Default Value: 0

14.1.42 GPIO_PRT4_INTR_CFG (continued)

11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for IO pin 5 Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for IO pin 4 Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pin 3 Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pin 2 Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pin 1 Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pin 0 Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges

14.1.43 GPIO_PRT4_CFG

Port configuration register

Address: 0x42410244

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN1	DRIVE_MODE1 [6:4]			IN_EN0	DRIVE_MODE0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN3	DRIVE_MODE3 [14:12]			IN_EN2	DRIVE_MODE2 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN5	DRIVE_MODE5 [22:20]			IN_EN4	DRIVE_MODE4 [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN7	DRIVE_MODE7 [30:28]			IN_EN6	DRIVE_MODE6 [26:24]		

Bits	Name	Description
31	IN_EN7	Enables the input buffer for IO pin 7 Default Value: 0
30 : 28	DRIVE_MODE7	The GPIO drive mode for IO pin 7 Default Value: 0
27	IN_EN6	Enables the input buffer for IO pin 6 Default Value: 0
26 : 24	DRIVE_MODE6	The GPIO drive mode for IO pin 6 Default Value: 0
23	IN_EN5	Enables the input buffer for IO pin 5 Default Value: 0
22 : 20	DRIVE_MODE5	The GPIO drive mode for IO pin 5 Default Value: 0
19	IN_EN4	Enables the input buffer for IO pin 4 Default Value: 0
18 : 16	DRIVE_MODE4	The GPIO drive mode for IO pin4 Default Value: 0
15	IN_EN3	Enables the input buffer for IO pin 3 Default Value: 0
14 : 12	DRIVE_MODE3	The GPIO drive mode for IO pin 3 Default Value: 0
11	IN_EN2	Enables the input buffer for IO pin 2 Default Value: 0

14.1.43 GPIO_PRT4_CFG (continued)

10 : 8	DRIVE_MODE2	The GPIO drive mode for IO pin 2 Default Value: 0
7	IN_EN1	Enables the input buffer for IO pin 1 Default Value: 0
6 : 4	DRIVE_MODE1	The GPIO drive mode for IO pin 1 Default Value: 0
3	IN_EN0	Enables the input buffer for IO pin 0. This bit should be cleared when analog signals are present on the pin to avoid crowbar currents. The output buffer can be used to drive analog signals high or low without issue. '0': Input buffer disabled '1': Input buffer enabled Default Value: 0
2 : 0	DRIVE_MODE0	The GPIO drive mode for IO pin 0. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0 **0x0: HIGHZ :** Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance **0x1: RESERVED :** This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance

14.1.43 GPIO_PRT4_CFG (continued)

0x2: PULLUP :

Resistive pull up
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Weak/resistive pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull up
D_OUT = '1': Weak/resistive pull up

0x3: PULLDOWN :

Resistive pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull down

0x4: OD_DRIVESLOW :

Open drain, drives low
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': High Impedance
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

14.1.43 GPIO_PRT4_CFG (continued)

0x5: OD_DRIVESHIGH :

Open drain, drives high
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': High Impedance
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x6: STRONG :

Strong D_OUTput buffer
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x7: PULLUP_DOWN :

Pull up or pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = '0':
GPIO_DSI_OUT = '0': Weak/resistive pull down
GPIO_DSI_OUT = '1': Weak/resistive pull up
where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT.
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull up

14.1.44 GPIO_PRT4_CFG_IN

Port input buffer configuration register

Address: 0x42410248

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	VTRIP_-SEL7_0	VTRIP_-SEL6_0	VTRIP_-SEL5_0	VTRIP_-SEL4_0	VTRIP_-SEL3_0	VTRIP_-SEL2_0	VTRIP_-SEL1_0	VTRIP_-SEL0_0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	VTRIP_SEL7_0	Configures the pin 7 input buffer mode (trip points and hysteresis) Default Value: 0
6	VTRIP_SEL6_0	Configures the pin 6 input buffer mode (trip points and hysteresis) Default Value: 0
5	VTRIP_SEL5_0	Configures the pin 5 input buffer mode (trip points and hysteresis) Default Value: 0
4	VTRIP_SEL4_0	Configures the pin 4 input buffer mode (trip points and hysteresis) Default Value: 0
3	VTRIP_SEL3_0	Configures the pin 3 input buffer mode (trip points and hysteresis) Default Value: 0
2	VTRIP_SEL2_0	Configures the pin 2 input buffer mode (trip points and hysteresis) Default Value: 0
1	VTRIP_SEL1_0	Configures the pin 1 input buffer mode (trip points and hysteresis) Default Value: 0
0	VTRIP_SEL0_0	Configures the pin 0 input buffer mode (trip points and hysteresis) Default Value: 0
		0x0: CMOS : Input buffer compatible with CMOS and I2C interfaces

14.1.44 GPIO_PRT4_CFG_IN (continued)

0x1: TTL :

Input buffer compatible with TTL and MediaLB interfaces

14.1.45 GPIO_PRT4_CFG_OUT

Port output buffer configuration register

Address: 0x4241024C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DRIVE_SEL3 [23:22]		DRIVE_SEL2 [21:20]		DRIVE_SEL1 [19:18]		DRIVE_SEL0 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DRIVE_SEL7 [31:30]		DRIVE_SEL6 [29:28]		DRIVE_SEL5 [27:26]		DRIVE_SEL4 [25:24]	

Bits	Name	Description
31 : 30	DRIVE_SEL7	Sets the GPIO drive strength for IO pin 7 Default Value: 0
29 : 28	DRIVE_SEL6	Sets the GPIO drive strength for IO pin 6 Default Value: 0
27 : 26	DRIVE_SEL5	Sets the GPIO drive strength for IO pin 5 Default Value: 0
25 : 24	DRIVE_SEL4	Sets the GPIO drive strength for IO pin 4 Default Value: 0
23 : 22	DRIVE_SEL3	Sets the GPIO drive strength for IO pin 3 Default Value: 0
21 : 20	DRIVE_SEL2	Sets the GPIO drive strength for IO pin 2 Default Value: 0
19 : 18	DRIVE_SEL1	Sets the GPIO drive strength for IO pin 1 Default Value: 0
17 : 16	DRIVE_SEL0	Sets the GPIO drive strength for IO pin 0 Default Value: 0
		0x0: DRIVE_SEL_ZERO : Full drive strength: Max drive current

14.1.45 GPIO_PRT4_CFG_OUT (continued)

0x1: DRIVE_SEL_ONE :

1/2 drive strength: 1/2 drive current

0x2: DRIVE_SEL_TWO :

1/4 drive strength: 1/4 drive current

0x3: DRIVE_SEL_THREE :

1/8 drive strength: 1/8 drive current

14.1.46 GPIO_PRT8_OUT

Port output data register

Address: 0x42410400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [7:6]		OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	OUT5	IO output data for pin 5 Default Value: 0
4	OUT4	IO output data for pin 4 Default Value: 0
3	OUT3	IO output data for pin 3 Default Value: 0
2	OUT2	IO output data for pin 2 Default Value: 0
1	OUT1	IO output data for pin 1 Default Value: 0
0	OUT0	IO output data for pin 0 '0': Output state set to '0' '1': Output state set to '1' Default Value: 0

14.1.47 GPIO_PRT8_IN

Port input state register

Address: 0x42410410

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		IN5	IN4	IN3	IN2	IN1	IN0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_IN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_IN	Reads of this register return the logical state of the filtered pin as selected in the IN-TR_CFG.FLT_SEL register. Default Value: 0
5	IN5	IO pin state for pin 5 Default Value: 0
4	IN4	IO pin state for pin 4 Default Value: 0
3	IN3	IO pin state for pin 3 Default Value: 0
2	IN2	IO pin state for pin 2 Default Value: 0
1	IN1	IO pin state for pin 1 Default Value: 0
0	IN0	IO pin state for pin 0 '0': Low logic level present on pin. '1': High logic level present on pin. On reset assertion , IN register will get reset. The Pad value takes 2 clock cycles to be reflected into IN Register. The default value is transient. Default Value: 0

14.1.48 GPIO_PRT8_INTR

Port interrupt status register

Address: 0x42410414

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None		A	A	A	A	A	A
Name	None [7:6]		EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [23:22]		IN_IN5	IN_IN4	IN_IN3	IN_IN2	IN_IN1	IN_IN0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							FLT_IN_IN

Bits	Name	Description
24	FLT_IN_IN	Filtered pin state for pin selected by INTR_CFG.FLT_SEL Default Value: 0
21	IN_IN5	IO pin state for pin 5 Default Value: 0
20	IN_IN4	IO pin state for pin 4 Default Value: 0
19	IN_IN3	IO pin state for pin 3 Default Value: 0
18	IN_IN2	IO pin state for pin 2 Default Value: 0
17	IN_IN1	IO pin state for pin 1 Default Value: 0
16	IN_IN0	IO pin state for pin 0 Default Value: 0
8	FLT_EDGE	Edge detected on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
5	EDGE5	Edge detect for IO pin 5 Default Value: 0
4	EDGE4	Edge detect for IO pin 4 Default Value: 0
3	EDGE3	Edge detect for IO pin 3 Default Value: 0

14.1.48 GPIO_PRT8_INTR (continued)

2	EDGE2	Edge detect for IO pin 2 Default Value: 0
1	EDGE1	Edge detect for IO pin 1 Default Value: 0
0	EDGE0	Edge detect for IO pin 0 '0': No edge was detected on pin. '1': An edge was detected on pin. Default Value: 0

14.1.49 GPIO_PRT8_INTR_MASK

Port interrupt mask register

Address: 0x42410418

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Masks edge interrupt on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
5	EDGE5	Masks edge interrupt on IO pin 5 Default Value: 0
4	EDGE4	Masks edge interrupt on IO pin 4 Default Value: 0
3	EDGE3	Masks edge interrupt on IO pin 3 Default Value: 0
2	EDGE2	Masks edge interrupt on IO pin 2 Default Value: 0
1	EDGE1	Masks edge interrupt on IO pin 1 Default Value: 0
0	EDGE0	Masks edge interrupt on IO pin 0 '0': Pin interrupt forwarding disabled '1': Pin interrupt forwarding enabled Default Value: 0

14.1.50 GPIO_PRT8_INTR_MASKED

Port interrupt masked status register

Address: 0x4241041C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Edge detected and masked on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
5	EDGE5	Edge detected and masked on IO pin 5 Default Value: 0
4	EDGE4	Edge detected and masked on IO pin 4 Default Value: 0
3	EDGE3	Edge detected and masked on IO pin 3 Default Value: 0
2	EDGE2	Edge detected and masked on IO pin 2 Default Value: 0
1	EDGE1	Edge detected and masked on IO pin 1 Default Value: 0
0	EDGE0	Edge detected AND masked on IO pin 0 '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU Default Value: 0

14.1.51 GPIO_PRT8_INTR_SET

Port interrupt set register

Address: 0x42410420

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	None		A	A	A	A	A	A
Name	None [7:6]		EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1S
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Sets edge detect interrupt for filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
5	EDGE5	Sets edge detect interrupt for IO pin 5 Default Value: 0
4	EDGE4	Sets edge detect interrupt for IO pin 4 Default Value: 0
3	EDGE3	Sets edge detect interrupt for IO pin 3 Default Value: 0
2	EDGE2	Sets edge detect interrupt for IO pin 2 Default Value: 0
1	EDGE1	Sets edge detect interrupt for IO pin 1 Default Value: 0
0	EDGE0	Sets edge detect interrupt for IO pin 0 '0': Interrupt state not affected '1': Interrupt set Default Value: 0

14.1.52 GPIO_PRT8_INTR_CFG

Port interrupt configuration register

Address: 0x42410440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [15:12]				EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by INTR_CFG.FLT_SEL Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges
11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for IO pin 5 Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for IO pin 4 Default Value: 0

14.1.52 GPIO_PRT8_INTR_CFG (continued)

7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pin 3 Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pin 2 Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pin 1 Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pin 0 Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges

14.1.53 GPIO_PRT8_CFG

Port configuration register

Address: 0x42410444

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN1	DRIVE_MODE1 [6:4]			IN_EN0	DRIVE_MODE0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN3	DRIVE_MODE3 [14:12]			IN_EN2	DRIVE_MODE2 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN5	DRIVE_MODE5 [22:20]			IN_EN4	DRIVE_MODE4 [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	IN_EN5	Enables the input buffer for IO pin 5 Default Value: 0
22 : 20	DRIVE_MODE5	The GPIO drive mode for IO pin 5 Default Value: 0
19	IN_EN4	Enables the input buffer for IO pin 4 Default Value: 0
18 : 16	DRIVE_MODE4	The GPIO drive mode for IO pin4 Default Value: 0
15	IN_EN3	Enables the input buffer for IO pin 3 Default Value: 0
14 : 12	DRIVE_MODE3	The GPIO drive mode for IO pin 3 Default Value: 0
11	IN_EN2	Enables the input buffer for IO pin 2 Default Value: 0
10 : 8	DRIVE_MODE2	The GPIO drive mode for IO pin 2 Default Value: 0
7	IN_EN1	Enables the input buffer for IO pin 1 Default Value: 0
6 : 4	DRIVE_MODE1	The GPIO drive mode for IO pin 1 Default Value: 0

14.1.53 GPIO_PRT8_CFG (continued)

3	IN_EN0	Enables the input buffer for IO pin 0. This bit should be cleared when analog signals are present on the pin to avoid crowbar currents. The output buffer can be used to drive analog signals high or low without issue. '0': Input buffer disabled '1': Input buffer enabled Default Value: 0
2 : 0	DRIVE_MODE0	The GPIO drive mode for IO pin 0. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0 **0x0: HIGHZ :** Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance **0x1: RESERVED :** This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance **0x2: PULLUP :** Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up

14.1.53 GPIO_PRT8_CFG (continued)

0x3: PULLDOWN :

Resistive pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull down

0x4: OD_DRIVESLOW :

Open drain, drives low
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': High Impedance
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x5: OD_DRIVESHIGH :

Open drain, drives high
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': High Impedance
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

14.1.53 GPIO_PRT8_CFG (continued)

0x6: STRONG :

Strong D_OUTput buffer
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x7: PULLUP_DOWN :

Pull up or pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = '0':
GPIO_DSI_OUT = '0': Weak/resistive pull down
GPIO_DSI_OUT = '1': Weak/resistive pull up
where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT.
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull up

14.1.54 GPIO_PRT8_CFG_IN

Port input buffer configuration register

Address: 0x42410448

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		VTRIP_-SEL5_0	VTRIP_-SEL4_0	VTRIP_-SEL3_0	VTRIP_-SEL2_0	VTRIP_-SEL1_0	VTRIP_-SEL0_0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	VTRIP_SEL5_0	Configures the pin 5 input buffer mode (trip points and hysteresis) Default Value: 0
4	VTRIP_SEL4_0	Configures the pin 4 input buffer mode (trip points and hysteresis) Default Value: 0
3	VTRIP_SEL3_0	Configures the pin 3 input buffer mode (trip points and hysteresis) Default Value: 0
2	VTRIP_SEL2_0	Configures the pin 2 input buffer mode (trip points and hysteresis) Default Value: 0
1	VTRIP_SEL1_0	Configures the pin 1 input buffer mode (trip points and hysteresis) Default Value: 0
0	VTRIP_SEL0_0	Configures the pin 0 input buffer mode (trip points and hysteresis) Default Value: 0 **0x0: CMOS :** Input buffer compatible with CMOS and I2C interfaces **0x1: TTL :** Input buffer compatible with TTL and MediaLB interfaces

14.1.55 GPIO_PRT8_CFG_OUT

Port output buffer configuration register

Address: 0x4241044C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DRIVE_SEL3 [23:22]		DRIVE_SEL2 [21:20]		DRIVE_SEL1 [19:18]		DRIVE_SEL0 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [31:28]				DRIVE_SEL5 [27:26]		DRIVE_SEL4 [25:24]	

Bits	Name	Description
27 : 26	DRIVE_SEL5	Sets the GPIO drive strength for IO pin 5 Default Value: 0
25 : 24	DRIVE_SEL4	Sets the GPIO drive strength for IO pin 4 Default Value: 0
23 : 22	DRIVE_SEL3	Sets the GPIO drive strength for IO pin 3 Default Value: 0
21 : 20	DRIVE_SEL2	Sets the GPIO drive strength for IO pin 2 Default Value: 0
19 : 18	DRIVE_SEL1	Sets the GPIO drive strength for IO pin 1 Default Value: 0
17 : 16	DRIVE_SEL0	Sets the GPIO drive strength for IO pin 0 Default Value: 0 **0x0: DRIVE_SEL_ZERO :** Full drive strength: Max drive current **0x1: DRIVE_SEL_ONE :** 1/2 drive strength: 1/2 drive current

14.1.55 GPIO_PRT8_CFG_OUT (continued)

0x2: DRIVE_SEL_TWO :

1/4 drive strength: 1/4 drive current

0x3: DRIVE_SEL_THREE :

1/8 drive strength: 1/8 drive current

14.1.56 GPIO_SEC_INTR_CAUSE0

Secure Interrupt port cause register 0

Address: 0x42417000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	PORT_INT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						W	
Name	None [15:10]						PORT_INT [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	PORT_INT	Each IO port has an associated bit field in this register. The bit field reflects the IO port's interrupt line (bit field i reflects "gpio_interrupts[i]" for IO port i). The register is used when the system uses a combined interrupt line "gpio_interrupt". The software ISR reads the register to determine which IO port(s) is responsible for the combined interrupt line. Once, the IO port(s) is determined, the IO port's GPIO_PRT_INTR register is read to determine the IO pin(s) in the IO port that caused the interrupt. '0': Port has no pending interrupt '1': Port has pending interrupt Default Value: 0

14.1.57 GPIO_INTR_CAUSE0

Interrupt port cause register 0

Address: 0x42418000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	PORT_INT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						W	
Name	None [15:10]						PORT_INT [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	PORT_INT	Each IO port has an associated bit field in this register. The bit field reflects the IO port's interrupt line (bit field i reflects "gpio_interrupts[i]" for IO port i). The register is used when the system uses a combined interrupt line "gpio_interrupt". The software ISR reads the register to determine which IO port(s) is responsible for the combined interrupt line. Once, the IO port(s) is determined, the IO port's GPIO_PRT_INTR register is read to determine the IO pin(s) in the IO port that caused the interrupt. '0': Port has no pending interrupt '1': Port has pending interrupt Default Value: 0

14.1.58 GPIO_VDD_ACTIVE

Extern power supply detection register

Address: 0x42418010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R		
HW Access	None					W		
Name	None [7:3]					VDDIO_ACTIVE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	W	W	None					
Name	VDDD_ACTIVE	VDDA_ACTIVE	None [29:24]					

Bits	Name	Description
31	VDDD_ACTIVE	This bit indicates presence of the VDDD supply. This bit will always read-back 1. The VDDD supply has robust brown-out protection monitoring and it is not possible to read back this register without a valid supply. (This bit is used in certain test-modes to observe the brown-out detector status.) Default Value: 0
30	VDDA_ACTIVE	Same as VDDIO_ACTIVE for the analog supply VDDA. Default Value: 0
2 : 0	VDDIO_ACTIVE	Indicates presence or absence of VDDIO supplies (i.e. other than VDDD, VDDA) on the device (supplies are numbered 0..n-1). Note that VDDIO supplies have basic (crude) supply detectors only. If separate, robust, brown-out detection is desired on IO supplies, on-chip or off-chip analog resources need to provide it. For these bits to work reliable, the supply must be within valid spec range (per datasheet) or held at ground. Any in-between voltage has an undefined result. '0': Supply is not present '1': Supply is present When multiple VDDIO supplies are present, they will be assigned in alphanumeric ascending order to these bits during implementation. For example "vddusb, vddio_0, vddio_a, vbackup, vddio_r, vddio_1" are present then they will be assigned to these bits as below: 0: vbackup, 1: vddio_0, 2: vddio_1, 3: vddio_a, 4: vddio_r, 5: vddusb" Default Value: 0

14.1.59 GPIO_VDD_INTR

Supply detection interrupt register

Address: 0x42418014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1C		
HW Access	None					A		
Name	None [7:3]					VDDIO_ACTIVE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C	RW1C	None					
HW Access	A	A	None					
Name	VDDD_ACTIVE	VDDA_ACTIVE	None [29:24]					

Bits	Name	Description
31	VDDD_ACTIVE	The VDDD supply is always present during operation so a supply transition can not occur. This bit will always read back '1'. Default Value: 0
30	VDDA_ACTIVE	Same as VDDIO_ACTIVE for the analog supply VDDA. Default Value: 0
2 : 0	VDDIO_ACTIVE	Supply state change detected. '0': No change to supply detected '1': Change to supply detected Default Value: 0

14.1.60 GPIO_VDD_INTR_MASK

Supply detection interrupt mask register

Address: 0x42418018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					VDDIO_ACTIVE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	VDDD_ACTIVE	VDDA_ACTIVE	None [29:24]					

Bits	Name	Description
31	VDDD_ACTIVE	Same as VDDIO_ACTIVE for the digital supply VDDD. Default Value: 0
30	VDDA_ACTIVE	Same as VDDIO_ACTIVE for the analog supply VDDA. Default Value: 0
2 : 0	VDDIO_ACTIVE	Masks supply interrupt on VDDIO. '0': VDDIO interrupt forwarding disabled '1': VDDIO interrupt forwarding enabled Default Value: 0

14.1.61 GPIO_VDD_INTR_MASKED

Supply detection interrupt masked register

Address: 0x4241801C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R		
HW Access	None					W		
Name	None [7:3]					VDDIO_ACTIVE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	W	W	None					
Name	VDDD_ACTIVE	VDDA_ACTIVE	None [29:24]					

Bits	Name	Description
31	VDDD_ACTIVE	Same as VDDIO_ACTIVE for the digital supply VDDD. Default Value: 0
30	VDDA_ACTIVE	Same as VDDIO_ACTIVE for the analog supply VDDA. Default Value: 0
2 : 0	VDDIO_ACTIVE	Supply transition detected AND masked '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU Default Value: 0

14.1.62 GPIO_VDD_INTR_SET

Supply detection interrupt set register

Address: 0x42418020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1S		
HW Access	None					A		
Name	None [7:3]					VDDIO_ACTIVE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	RW1S	None					
HW Access	A	A	None					
Name	VDDD_ACTIVE	VDDA_ACTIVE	None [29:24]					

Bits	Name	Description
31	VDDD_ACTIVE	Same as VDDIO_ACTIVE for the digital supply VDDD. Default Value: 0
30	VDDA_ACTIVE	Same as VDDIO_ACTIVE for the analog supply VDDA. Default Value: 0
2 : 0	VDDIO_ACTIVE	Sets supply interrupt. '0': Interrupt state not affected '1': Interrupt set Default Value: 0

14.1.63 SMARTIO_PRT0_CTL

Control register

Address: 0x42420000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BYPASS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			CLOCK_SRC [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None					RW	RW
HW Access	R	None					R	R
Name	ENABLED	None [30:26]					PIPE-LINE_EN	HLD_OVR

Bits	Name	Description
31	ENABLED	Enable for programmable IO. Should only be set to '1' when the programmable IO is completely configured: '0': Disabled (signals are bypassed; behavior as if BYPASS is 0xFF). When disabled, the fabric (data unit and LUTs) reset is activated. If the IP is disabled: - The PIPELINE_EN register field should be set to '1', to ensure low power consumption by preventing combinatorial loops. - The CLOCK_SRC register field should be set to "20"-"30" (clock is constant '0'), to ensure low power consumption. '1': Enabled. Once enabled, it takes 3 "clk_fabric" clock cycles till the fabric reset is de-activated and the fabric becomes fully functional. This ensures that the IO pins' input synchronizer states are flushed when the fabric is fully functional. Default Value: 0
25	PIPELINE_EN	Enable for pipeline register: '0': Disabled (register is bypassed). '1': Enabled. Default Value: 1

14.1.63 SMARTIO_PRT0_CTL (continued)

24	HLD_OVR	IO cell hold override functionality. In DeepSleep power mode, the HSIOM holds the IO cell output and output enable signals if Active functionality is connected to the IO pads. This is undesirable if the SMARTIO is supposed to deliver DeepSleep output functionality on these IO pads. This field is used to control the hold override functionality from the SMARTIO: '0': The HSIOM controls the IO cell hold override functionality ("hsiom_hld_ovr"). '1': The SMARTIO controls the IO cel hold override functionality: - In bypass mode (ENABLED is '0' or BYPASS[i] is '1'), the HSIOM control is used. - In NON bypass mode (ENABLED is '1' and BYPASS[i] is '0'), the SMARTIO sets hold override to "pwr_hld_ovr_hib" to enable SMARTIO functionality in DeepSleep power mode (but disables it in Hibernate or Stop power mode). Default Value: Undefined
12 : 8	CLOCK_SRC	Clock ("clk_fabric") and reset ("rst_fabric_n") source selection: "0": io_data_in[0]/'1'. ... "7": io_data_in[7]/'1'. "8": chip_data[0]/'1'. ... "15": chip_data[7]/'1'. "16": clk_smartio/rst_sys_act_n. Used for both Active functionality synchronous logic on "clk_smartio". This selection is intended for synchronous operation on a PCLK specified clock frequency ("clock_smartio_pos_en"). Note that the fabric's clocked elements are frequency aligned, but NOT phase aligned to "clk_sys". "17": clk_smartio/rst_sys_dpslp_n. Used for both DeepSleep functionality synchronous logic on "clk_smartio" (note that "clk_smartio" is NOT available in DeepSleep and Hibernate power modes). This selection is intended for synchronous operation on a PCLK specified clock frequency ("clock_smartio_pos_en"). Note that the fabric's clocked elements are frequency aligned, but NOT phase aligned to "clk_sys". "18": Same as "17". Note that the M0S8 SMARTIO version used the Hibernate reset for this value, but the MXS40 SMARTIO version does not support Hibernate functionality. "19": clk_lf/rst_lf_dpslp_n (note that "clk_lf" is available in DeepSleep power mode). This selection is intended for synchronous operation on"clk_lf". Note that the fabric's clocked elements are frequency aligned, but NOT phase aligned to other "clk_lf" clocked elements. "20"-"30": Clock source is constant '0'. Any of these clock sources should be selected when the IP is disabled to ensure low power consumption. "31": asynchronous mode/'1'. Select this when clockless operation is configured. NOTE: Two positive edges of the selected clock are required for the block to be enabled (to deactivate reset). In asynchronous (clockless) mode clk_sys is used to enable the block, but is not available for clocking. Default Value: 0x14
7 : 0	BYPASS	Bypass of the programmable IO, one bit for each IO pin: BYPASS[i] is for IO pin i. When ENABLED is '1', this field is used. When ENABLED is '0', this field is NOT used and SMARTIO fabric is always bypassed. '0': No bypass (programmable SMARTIO fabric is exposed). '1': Bypass (programmable SMARTIOIO fabric is hidden). Default Value: Undefined

14.1.64 SMARTIO_PRT0_SYNC_CTL

Synchronization control register

Address: 0x42420010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	IO_SYNC_EN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CHIP_SYNC_EN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	CHIP_SYNC_EN	Synchronization of the chip input signals to "clk_fabric", one bit for each input: CHIP_SYNC_EN[i] is for input i. '0': No synchronization. '1': Synchronization. Default Value: Undefined
7 : 0	IO_SYNC_EN	Synchronization of the IO pin input signals to "clk_fabric", one bit for each IO pin: IO_SYNC_EN[i] is for IO pin i. '0': No synchronization. '1': Synchronization. Default Value: Undefined

14.1.65 SMARTIO_PRT0_LUT_SEL0

LUT component input selection

Address: 0x42420020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				LUT_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				LUT_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				LUT_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	LUT_TR2_SEL	LUT input signal "tr2_in" source selection. Encoding is the same as for LUT_TR1_SEL. Default Value: Undefined
11 : 8	LUT_TR1_SEL	LUT input signal "tr1_in" source selection: "0": LUT 0 output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

14.1.65 SMARTIO_PRT0_LUT_SEL0 (continued)

3 : 0	LUT_TR0_SEL	LUT input signal "tr0_in" source selection: "0": Data unit output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

14.1.66 SMARTIO_PRT0_LUT_CTL0

LUT component control register

Address: 0x42420040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						LUT_OPC [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	LUT_OPC	LUT opcode specifies the LUT operation: "0": Combinatoral output, no feedback. tr_out = LUT[{tr2_in, tr1_in, tr0_in}]. "1": Combinatorial output, feedback. tr_out = LUT[{lut_reg, tr1_in, tr0_in}]. On clock: lut_reg <= tr_in2. "2": Sequential output, no feedback. temp = LUT[{tr2_in, tr1_in, tr0_in}]. tr_out = lut_reg. On clock: lut_reg <= temp. "3": Register with asynchronous set and reset. tr_out = lut_reg. enable = (tr2_in ^ LUT[4]) | LUT[5]. set = enable & (tr1_in ^ LUT[2]) & LUT[3]. clr = enable & (tr0_in ^ LUT[0]) & LUT[1]. Asynchronously (no clock required): lut_reg <= if (clr) '0' else if (set) '1' Default Value: Undefined
7 : 0	LUT	LUT configuration. Depending on the LUT opcode LUT_OPC, the internal state lut_reg (captured in a flip-flop) and the LUT input signals tr0_in, tr1_in, tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state (lut_reg). Default Value: Undefined

14.1.67 SMARTIO_PRT0_DU_SEL

Data unit component input selection

Address: 0x424200C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DU_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				DU_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				DU_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW		None		RW	
HW Access	None		R		None		R	
Name	None [31:30]		DU_DATA1_SEL [29:28]		None [27:26]		DU_DATA0_SEL [25:24]	

Bits	Name	Description
29 : 28	DU_DATA1_SEL	Data unit input data "data1_in" source selection. Encoding is the same as for DU_DATA0_SEL. Default Value: Undefined
25 : 24	DU_DATA0_SEL	Data unit input data "data0_in" source selection: "0": Constant "0". "1": chip_data[7:0]. "2": io_data_in[7:0]. "3": DATA.DATA MMIO register field. Default Value: Undefined
19 : 16	DU_TR2_SEL	Data unit input signal "tr2_in" source selection. Encoding is the same as for DU_TR0_SEL. Default Value: Undefined
11 : 8	DU_TR1_SEL	Data unit input signal "tr1_in" source selection. Encoding is the same as for DU_TR0_SEL. Default Value: Undefined
3 : 0	DU_TR0_SEL	Data unit input signal "tr0_in" source selection: "0": Constant '0'. "1": Constant '1'. "2": Data unit output. "10-3": LUT 7 - 0 outputs. Otherwise: Undefined. Default Value: Undefined

14.1.68 SMARTIO_PRT0_DU_CTL

Data unit component control register

Address: 0x424200C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					DU_SIZE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				DU_OPC [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 8	DU_OPC	Data unit opcode specifies the data unit operation: "1": INCR "2": DECR "3": INCR_WRAP "4": DECR_WRAP "5": INCR_DECR "6": INCR_DECR_WRAP "7": ROR "8": SHR "9": AND_OR "10": SHR_MAJ3 "11": SHR_EQL. Otherwise: Undefined. Default Value: Undefined
2 : 0	DU_SIZE	Size/width of the data unit data operands (in bits) is DU_SIZE+1. E.g., if DU_SIZE is 7, the width is 8 bits. Default Value: Undefined

14.1.69 SMARTIO_PRT0_DATA

Data register

Address: 0x424200F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	Data unit input data source. Default Value: Undefined

15 Timer, Counter, and Pulse Width Modulator (TCPWM) registers

This section discusses the TCPWM registers. It lists all the registers in mapping tables, in address order.

15.1 Register details

Register	Address	Description
TCPWM0_GRP0_CNT0_CTRL	0x42A00000	Counter control register
TCPWM0_GRP0_CNT0_STATUS	0x42A00004	Counter status register
TCPWM0_GRP0_CNT0_COUNTER	0x42A00008	Counter count register
TCPWM0_GRP0_CNT0_CC0	0x42A00010	Counter compare/capture 0 register
TCPWM0_GRP0_CNT0_CC0_BUFF	0x42A00014	Counter buffered compare/capture 0 register
TCPWM0_GRP0_CNT0_CC1	0x42A00018	Counter compare/capture 1 register
TCPWM0_GRP0_CNT0_CC1_BUFF	0x42A0001C	Counter buffered compare/capture 1 register
TCPWM0_GRP0_CNT0_PERIOD	0x42A00020	Counter period register
TCPWM0_GRP0_CNT0_PERIOD_BUFF	0x42A00024	Counter buffered period register
TCPWM0_GRP0_CNT0_LINE_SEL	0x42A00028	Counter line selection register
TCPWM0_GRP0_CNT0_LINE_SEL_BUFF	0x42A0002C	Counter buffered line selection register
TCPWM0_GRP0_CNT0_DT	0x42A00030	Counter PWM dead time register
TCPWM0_GRP0_CNT0_DT_BUFF	0x42A00034	Counter buffered PWM dead time register
TCPWM0_GRP0_CNT0_PS	0x42A00038	Counter prescalar register
TCPWM0_GRP0_CNT0_TR_CMD	0x42A00040	Counter trigger command register
TCPWM0_GRP0_CNT0_TR_IN_SEL0	0x42A00044	Counter input trigger selection register 0
TCPWM0_GRP0_CNT0_TR_IN_SEL1	0x42A00048	Counter input trigger selection register 1
TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL	0x42A0004C	Counter input trigger edge selection register
TCPWM0_GRP0_CNT0_TR_PWM_CTRL	0x42A00050	Counter trigger PWM control register
TCPWM0_GRP0_CNT0_TR_OUT_SEL	0x42A00054	Counter output trigger selection register
TCPWM0_GRP0_CNT0_INTR	0x42A00070	Interrupt request register
TCPWM0_GRP0_CNT0_INTR_SET	0x42A00074	Interrupt set request register
TCPWM0_GRP0_CNT0_INTR_MASK	0x42A00078	Interrupt mask register
TCPWM0_GRP0_CNT0_INTR_MASKED	0x42A0007C	Interrupt masked request register
TCPWM0_GRP0_CNT0_ONE_GF0	0x42A00084	Glitch filter register for one to one trigger
TCPWM0_GRP0_CNT0_TR_ONE_SYNC_BYPASS	0x42A000A4	Sync bypass register for one to one trigger
TCPWM0_GRP0_CNT0_HRPWM_CTRL	0x42A000B0	Counter control register for HRPWM feature
TCPWM0_GRP0_CNT1_CTRL	0x42A00100	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT1_STATUS	0x42A00104	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.

Register	Address	Description
TCPWM0_GRP0_CNT1_COUNTER	0x42A00108	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT1_CC0	0x42A00110	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT1_CC0_BUFF	0x42A00114	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT1_CC1	0x42A00118	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT1_CC1_BUFF	0x42A0011C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT1_PERIOD	0x42A00120	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT1_PERIOD_BUFF	0x42A00124	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT1_LINE_SEL	0x42A00128	Counter line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT1_LINE_SEL_BUFF	0x42A0012C	Counter buffered line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT1_DT	0x42A00130	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT1_DT_BUFF	0x42A00134	Counter buffered PWM dead time register. See TCPWM0_GRP0_CNT0_DT_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT1_PS	0x42A00138	Counter prescalar register. See TCPWM0_GRP0_CNT0_PS for the details of bit fields.
TCPWM0_GRP0_CNT1_TR_CMD	0x42A00140	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT1_TR_IN_SEL0	0x42A00144	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT1_TR_IN_SEL1	0x42A00148	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT1_TR_IN_EDGE_SEL	0x42A0014C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.

Register	Address	Description
TCPWM0_GRP0_CNT1_TR_PWM_CTRL	0x42A00150	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT1_TR_OUT_SEL	0x42A00154	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT1_INTR	0x42A00170	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT1_INTR_SET	0x42A00174	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT1_INTR_MASK	0x42A00178	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT1_INTR_MASKED	0x42A0017C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT1_ONE_GF0	0x42A00184	Glitch filter register for one to one trigger. See TCPWM0_GRP0_CNT0_ONE_GF0 for the details of bit fields.
TCPWM0_GRP0_CNT1_TR_ONE_SYNC_BYPASS	0x42A001A4	Sync bypass register for one to one trigger. See TCPWM0_GRP0_CNT0_TR_ONE_SYNC_BYPASS for the details of bit fields.
TCPWM0_GRP0_CNT1_HRPWM_CTRL	0x42A001B0	Counter control register for HRPWM feature. See TCPWM0_GRP0_CNT0_HRPWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT2_CTRL	0x42A00200	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT2_STATUS	0x42A00204	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT2_COUNTER	0x42A00208	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT2_CC0	0x42A00210	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT2_CC0_BUFF	0x42A00214	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT2_CC1	0x42A00218	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.

Register	Address	Description
TCPWM0_GRP0_CNT2_CC1_BUFF	0x42A0021C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT2_PERIOD	0x42A00220	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT2_PERIOD_BUFF	0x42A00224	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT2_LINE_SEL	0x42A00228	Counter line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT2_LINE_SEL_BUFF	0x42A0022C	Counter buffered line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT2_DT	0x42A00230	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT2_DT_BUFF	0x42A00234	Counter buffered PWM dead time register. See TCPWM0_GRP0_CNT0_DT_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT2_PS	0x42A00238	Counter prescalar register. See TCPWM0_GRP0_CNT0_PS for the details of bit fields.
TCPWM0_GRP0_CNT2_TR_CMD	0x42A00240	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT2_TR_IN_SEL0	0x42A00244	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT2_TR_IN_SEL1	0x42A00248	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT2_TR_IN_EDGE_SEL	0x42A0024C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT2_TR_PWM_CTRL	0x42A00250	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT2_TR_OUT_SEL	0x42A00254	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT2_INTR	0x42A00270	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.

Register	Address	Description
TCPWM0_GRP0_CNT2_INTR_SET	0x42A00274	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT2_INTR_MASK	0x42A00278	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT2_INTR_MASKED	0x42A0027C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT2_ONE_GF0	0x42A00284	Glitch filter register for one to one trigger. See TCPWM0_GRP0_CNT0_ONE_GF0 for the details of bit fields.
TCPWM0_GRP0_CNT2_TR_ONE_SYNC_BYPASS	0x42A002A4	Sync bypass register for one to one trigger. See TCPWM0_GRP0_CNT0_TR_ONE_SYNC_BYPASS for the details of bit fields.
TCPWM0_GRP0_CNT2_HRPWM_CTRL	0x42A002B0	Counter control register for HRPWM feature. See TCPWM0_GRP0_CNT0_HRPWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT3_CTRL	0x42A00300	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT3_STATUS	0x42A00304	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT3_COUNTER	0x42A00308	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT3_CC0	0x42A00310	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT3_CC0_BUFF	0x42A00314	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT3_CC1	0x42A00318	Counter compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP0_CNT3_CC1_BUFF	0x42A0031C	Counter buffered compare/capture 1 register. See TCPWM0_GRP0_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT3_PERIOD	0x42A00320	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT3_PERIOD_BUFF	0x42A00324	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.

Register	Address	Description
TCPWM0_GRP0_CNT3_LINE_SEL	0x42A00328	Counter line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT3_LINE_SEL_BUFF	0x42A0032C	Counter buffered line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT3_DT	0x42A00330	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT3_DT_BUFF	0x42A00334	Counter buffered PWM dead time register. See TCPWM0_GRP0_CNT0_DT_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT3_PS	0x42A00338	Counter prescalar register. See TCPWM0_GRP0_CNT0_PS for the details of bit fields.
TCPWM0_GRP0_CNT3_TR_CMD	0x42A00340	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT3_TR_IN_SEL0	0x42A00344	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT3_TR_IN_SEL1	0x42A00348	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT3_TR_IN_EDGE_SEL	0x42A0034C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT3_TR_PWM_CTRL	0x42A00350	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT3_TR_OUT_SEL	0x42A00354	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT3_INTR	0x42A00370	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT3_INTR_SET	0x42A00374	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT3_INTR_MASK	0x42A00378	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT3_INTR_MASKED	0x42A0037C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.

Register	Address	Description
TCPWM0_GRP0_CNT3_ONE_GF0	0x42A00384	Glitch filter register for one to one trigger. See TCPWM0_GRP0_CNT0_ONE_GF0 for the details of bit fields.
TCPWM0_GRP0_CNT3_TR_ONE_SYNC_BYPASS	0x42A003A4	Sync bypass register for one to one trigger. See TCPWM0_GRP0_CNT0_TR_ONE_SYNC_BYPASS for the details of bit fields.
TCPWM0_GRP0_CNT3_HRPWM_CTRL	0x42A003B0	Counter control register for HRPWM feature. See TCPWM0_GRP0_CNT0_HRPWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT0_CTRL	0x42A10000	Counter control register
TCPWM0_GRP1_CNT0_STATUS	0x42A10004	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT0_COUNTER	0x42A10008	Counter count register
TCPWM0_GRP1_CNT0_CC0	0x42A10010	Counter compare/capture 0 register
TCPWM0_GRP1_CNT0_CC0_BUFF	0x42A10014	Counter buffered compare/capture 0 register
TCPWM0_GRP1_CNT0_CC1	0x42A10018	Counter compare/capture 1 register
TCPWM0_GRP1_CNT0_CC1_BUFF	0x42A1001C	Counter buffered compare/capture 1 register
TCPWM0_GRP1_CNT0_PERIOD	0x42A10020	Counter period register
TCPWM0_GRP1_CNT0_PERIOD_BUFF	0x42A10024	Counter buffered period register
TCPWM0_GRP1_CNT0_LINE_SEL	0x42A10028	Counter line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT0_LINE_SEL_BUFF	0x42A1002C	Counter buffered line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT0_DT	0x42A10030	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT0_DT_BUFF	0x42A10034	Counter buffered PWM dead time register. See TCPWM0_GRP0_CNT0_DT_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT0_PS	0x42A10038	Counter prescalar register. See TCPWM0_GRP0_CNT0_PS for the details of bit fields.
TCPWM0_GRP1_CNT0_TR_CMD	0x42A10040	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT0_TR_IN_SEL0	0x42A10044	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT0_TR_IN_SEL1	0x42A10048	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.

Timer, Counter, and Pulse Width Modulator (TCPWM) registers

Register	Address	Description
TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL	0x42A1004C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT0_TR_PWM_CTRL	0x42A10050	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT0_TR_OUT_SEL	0x42A10054	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT0_INTR	0x42A10070	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT0_INTR_SET	0x42A10074	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT0_INTR_MASK	0x42A10078	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT0_INTR_MASKED	0x42A1007C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT0_LFSR	0x42A10080	LFSR register
TCPWM0_GRP1_CNT0_ONE_GF0	0x42A10084	Glitch filter register for one to one trigger. See TCPWM0_GRP0_CNT0_ONE_GF0 for the details of bit fields.
TCPWM0_GRP1_CNT0_TR_ONE_SYNC_BYPASS	0x42A100A4	Sync bypass register for one to one trigger. See TCPWM0_GRP0_CNT0_TR_ONE_SYNC_BYPASS for the details of bit fields.
TCPWM0_GRP1_CNT1_CTRL	0x42A10100	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT1_STATUS	0x42A10104	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT1_COUNTER	0x42A10108	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT1_CC0	0x42A10110	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT1_CC0_BUFF	0x42A10114	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT1_CC1	0x42A10118	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.

Register	Address	Description
TCPWM0_GRP1_CNT1_CC1_BUFF	0x42A1011C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT1_PERIOD	0x42A10120	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT1_PERIOD_BUFF	0x42A10124	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT1_LINE_SEL	0x42A10128	Counter line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT1_LINE_SEL_BUFF	0x42A1012C	Counter buffered line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT1_DT	0x42A10130	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT1_DT_BUFF	0x42A10134	Counter buffered PWM dead time register. See TCPWM0_GRP0_CNT0_DT_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT1_PS	0x42A10138	Counter prescalar register. See TCPWM0_GRP0_CNT0_PS for the details of bit fields.
TCPWM0_GRP1_CNT1_TR_CMD	0x42A10140	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT1_TR_IN_SEL0	0x42A10144	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT1_TR_IN_SEL1	0x42A10148	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT1_TR_IN_EDGE_SEL	0x42A1014C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT1_TR_PWM_CTRL	0x42A10150	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT1_TR_OUT_SEL	0x42A10154	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT1_INTR	0x42A10170	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.

Register	Address	Description
TCPWM0_GRP1_CNT1_INTR_SET	0x42A10174	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT1_INTR_MASK	0x42A10178	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT1_INTR_MASKED	0x42A1017C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT1_LFSR	0x42A10180	LFSR register. See TCPWM0_GRP1_CNT0_LFSR for the details of bit fields.
TCPWM0_GRP1_CNT1_ONE_GF0	0x42A10184	Glitch filter register for one to one trigger. See TCPWM0_GRP0_CNT0_ONE_GF0 for the details of bit fields.
TCPWM0_GRP1_CNT1_TR_ONE_SYNC_BYPASS	0x42A101A4	Sync bypass register for one to one trigger. See TCPWM0_GRP0_CNT0_TR_ONE_SYNC_BYPASS for the details of bit fields.
TCPWM0_GRP1_CNT2_CTRL	0x42A10200	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT2_STATUS	0x42A10204	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT2_COUNTER	0x42A10208	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT2_CC0	0x42A10210	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT2_CC0_BUFF	0x42A10214	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT2_CC1	0x42A10218	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT2_CC1_BUFF	0x42A1021C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT2_PERIOD	0x42A10220	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT2_PERIOD_BUFF	0x42A10224	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.

Register	Address	Description
TCPWM0_GRP1_CNT2_LINE_SEL	0x42A10228	Counter line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT2_LINE_SEL_BUFF	0x42A1022C	Counter buffered line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT2_DT	0x42A10230	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT2_DT_BUFF	0x42A10234	Counter buffered PWM dead time register. See TCPWM0_GRP0_CNT0_DT_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT2_PS	0x42A10238	Counter prescalar register. See TCPWM0_GRP0_CNT0_PS for the details of bit fields.
TCPWM0_GRP1_CNT2_TR_CMD	0x42A10240	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT2_TR_IN_SEL0	0x42A10244	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT2_TR_IN_SEL1	0x42A10248	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT2_TR_IN_EDGE_SEL	0x42A1024C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT2_TR_PWM_CTRL	0x42A10250	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT2_TR_OUT_SEL	0x42A10254	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT2_INTR	0x42A10270	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT2_INTR_SET	0x42A10274	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT2_INTR_MASK	0x42A10278	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT2_INTR_MASKED	0x42A1027C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.

Timer, Counter, and Pulse Width Modulator (TCPWM) registers

Register	Address	Description
TCPWM0_GRP1_CNT2_LFSR	0x42A10280	LFSR register. See TCPWM0_GRP1_CNT0_LFSR for the details of bit fields.
TCPWM0_GRP1_CNT2_ONE_GF0	0x42A10284	Glitch filter register for one to one trigger. See TCPWM0_GRP0_CNT0_ONE_GF0 for the details of bit fields.
TCPWM0_GRP1_CNT2_TR_ONE_SYNC_BYPASS	0x42A102A4	Sync bypass register for one to one trigger. See TCPWM0_GRP0_CNT0_TR_ONE_SYNC_BYPASS for the details of bit fields.
TCPWM0_GRP1_CNT3_CTRL	0x42A10300	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT3_STATUS	0x42A10304	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT3_COUNTER	0x42A10308	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT3_CC0	0x42A10310	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT3_CC0_BUFF	0x42A10314	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT3_CC1	0x42A10318	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT3_CC1_BUFF	0x42A1031C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT3_PERIOD	0x42A10320	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT3_PERIOD_BUFF	0x42A10324	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT3_LINE_SEL	0x42A10328	Counter line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT3_LINE_SEL_BUFF	0x42A1032C	Counter buffered line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT3_DT	0x42A10330	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT3_DT_BUFF	0x42A10334	Counter buffered PWM dead time register. See TCPWM0_GRP0_CNT0_DT_BUFF for the details of bit fields.

Register	Address	Description
TCPWM0_GRP1_CNT3_PS	0x42A10338	Counter prescalar register. See TCPWM0_GRP0_CNT0_PS for the details of bit fields.
TCPWM0_GRP1_CNT3_TR_CMD	0x42A10340	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT3_TR_IN_SEL0	0x42A10344	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT3_TR_IN_SEL1	0x42A10348	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT3_TR_IN_EDGE_SEL	0x42A1034C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT3_TR_PWM_CTRL	0x42A10350	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT3_TR_OUT_SEL	0x42A10354	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT3_INTR	0x42A10370	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT3_INTR_SET	0x42A10374	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT3_INTR_MASK	0x42A10378	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT3_INTR_MASKED	0x42A1037C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT3_LFSR	0x42A10380	LFSR register. See TCPWM0_GRP1_CNT0_LFSR for the details of bit fields.
TCPWM0_GRP1_CNT3_ONE_GF0	0x42A10384	Glitch filter register for one to one trigger. See TCPWM0_GRP0_CNT0_ONE_GF0 for the details of bit fields.
TCPWM0_GRP1_CNT3_TR_ONE_SYNC_BYPASS	0x42A103A4	Sync bypass register for one to one trigger. See TCPWM0_GRP0_CNT0_TR_ONE_SYNC_BYPASS for the details of bit fields.
TCPWM0_GRP1_CNT4_CTRL	0x42A10400	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.

Register	Address	Description
TCPWM0_GRP1_CNT4_STATUS	0x42A10404	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT4_COUNTER	0x42A10408	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT4_CC0	0x42A10410	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT4_CC0_BUFF	0x42A10414	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT4_CC1	0x42A10418	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT4_CC1_BUFF	0x42A1041C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT4_PERIOD	0x42A10420	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT4_PERIOD_BUFF	0x42A10424	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT4_LINE_SEL	0x42A10428	Counter line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT4_LINE_SEL_BUFF	0x42A1042C	Counter buffered line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT4_DT	0x42A10430	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT4_DT_BUFF	0x42A10434	Counter buffered PWM dead time register. See TCPWM0_GRP0_CNT0_DT_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT4_PS	0x42A10438	Counter prescalar register. See TCPWM0_GRP0_CNT0_PS for the details of bit fields.
TCPWM0_GRP1_CNT4_TR_CMD	0x42A10440	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT4_TR_IN_SEL0	0x42A10444	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT4_TR_IN_SEL1	0x42A10448	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.

Register	Address	Description
TCPWM0_GRP1_CNT4_TR_IN_EDGE_SEL	0x42A1044C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT4_TR_PWM_CTRL	0x42A10450	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT4_TR_OUT_SEL	0x42A10454	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT4_INTR	0x42A10470	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT4_INTR_SET	0x42A10474	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT4_INTR_MASK	0x42A10478	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT4_INTR_MASKED	0x42A1047C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT4_LFSR	0x42A10480	LFSR register. See TCPWM0_GRP1_CNT0_LFSR for the details of bit fields.
TCPWM0_GRP1_CNT4_ONE_GF0	0x42A10484	Glitch filter register for one to one trigger. See TCPWM0_GRP0_CNT0_ONE_GF0 for the details of bit fields.
TCPWM0_GRP1_CNT4_TR_ONE_SYNC_BYPASS	0x42A104A4	Sync bypass register for one to one trigger. See TCPWM0_GRP0_CNT0_TR_ONE_SYNC_BYPASS for the details of bit fields.
TCPWM0_GRP1_CNT5_CTRL	0x42A10500	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT5_STATUS	0x42A10504	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT5_COUNTER	0x42A10508	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT5_CC0	0x42A10510	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT5_CC0_BUFF	0x42A10514	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.

Register	Address	Description
TCPWM0_GRP1_CNT5_CC1	0x42A10518	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT5_CC1_BUFF	0x42A1051C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT5_PERIOD	0x42A10520	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT5_PERIOD_BUFF	0x42A10524	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT5_LINE_SEL	0x42A10528	Counter line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT5_LINE_SEL_BUFF	0x42A1052C	Counter buffered line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT5_DT	0x42A10530	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT5_DT_BUFF	0x42A10534	Counter buffered PWM dead time register. See TCPWM0_GRP0_CNT0_DT_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT5_PS	0x42A10538	Counter prescalar register. See TCPWM0_GRP0_CNT0_PS for the details of bit fields.
TCPWM0_GRP1_CNT5_TR_CMD	0x42A10540	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT5_TR_IN_SEL0	0x42A10544	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT5_TR_IN_SEL1	0x42A10548	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT5_TR_IN_EDGE_SEL	0x42A1054C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT5_TR_PWM_CTRL	0x42A10550	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT5_TR_OUT_SEL	0x42A10554	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.

Register	Address	Description
TCPWM0_GRP1_CNT5_INTR	0x42A10570	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT5_INTR_SET	0x42A10574	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT5_INTR_MASK	0x42A10578	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT5_INTR_MASKED	0x42A1057C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT5_LFSR	0x42A10580	LFSR register. See TCPWM0_GRP1_CNT0_LFSR for the details of bit fields.
TCPWM0_GRP1_CNT5_ONE_GF0	0x42A10584	Glitch filter register for one to one trigger. See TCPWM0_GRP0_CNT0_ONE_GF0 for the details of bit fields.
TCPWM0_GRP1_CNT5_TR_ONE_SYNC_BYPASS	0x42A105A4	Sync bypass register for one to one trigger. See TCPWM0_GRP0_CNT0_TR_ONE_SYNC_BYPASS for the details of bit fields.
TCPWM0_GRP1_CNT6_CTRL	0x42A10600	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT6_STATUS	0x42A10604	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT6_COUNTER	0x42A10608	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT6_CC0	0x42A10610	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT6_CC0_BUFF	0x42A10614	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT6_CC1	0x42A10618	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT6_CC1_BUFF	0x42A1061C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT6_PERIOD	0x42A10620	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.

Register	Address	Description
TCPWM0_GRP1_CNT6_PERIOD_BUFF	0x42A10624	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT6_LINE_SEL	0x42A10628	Counter line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT6_LINE_SEL_BUFF	0x42A1062C	Counter buffered line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT6_DT	0x42A10630	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT6_DT_BUFF	0x42A10634	Counter buffered PWM dead time register. See TCPWM0_GRP0_CNT0_DT_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT6_PS	0x42A10638	Counter prescalar register. See TCPWM0_GRP0_CNT0_PS for the details of bit fields.
TCPWM0_GRP1_CNT6_TR_CMD	0x42A10640	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT6_TR_IN_SEL0	0x42A10644	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT6_TR_IN_SEL1	0x42A10648	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT6_TR_IN_EDGE_SEL	0x42A1064C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT6_TR_PWM_CTRL	0x42A10650	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT6_TR_OUT_SEL	0x42A10654	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT6_INTR	0x42A10670	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT6_INTR_SET	0x42A10674	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT6_INTR_MASK	0x42A10678	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.

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Register	Address	Description
TCPWM0_GRP1_CNT6_INTR_MASKED	0x42A1067C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT6_LFSR	0x42A10680	LFSR register. See TCPWM0_GRP1_CNT0_LFSR for the details of bit fields.
TCPWM0_GRP1_CNT6_ONE_GF0	0x42A10684	Glitch filter register for one to one trigger. See TCPWM0_GRP0_CNT0_ONE_GF0 for the details of bit fields.
TCPWM0_GRP1_CNT6_TR_ONE_SYNC_BYPASS	0x42A106A4	Sync bypass register for one to one trigger. See TCPWM0_GRP0_CNT0_TR_ONE_SYNC_BYPASS for the details of bit fields.
TCPWM0_GRP1_CNT7_CTRL	0x42A10700	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT7_STATUS	0x42A10704	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT7_COUNTER	0x42A10708	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT7_CC0	0x42A10710	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT7_CC0_BUFF	0x42A10714	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT7_CC1	0x42A10718	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT7_CC1_BUFF	0x42A1071C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT7_PERIOD	0x42A10720	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT7_PERIOD_BUFF	0x42A10724	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT7_LINE_SEL	0x42A10728	Counter line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT7_LINE_SEL_BUFF	0x42A1072C	Counter buffered line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT7_DT	0x42A10730	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.

Register	Address	Description
TCPWM0_GRP1_CNT7_DT_BUFF	0x42A10734	Counter buffered PWM dead time register. See TCPWM0_GRP0_CNT0_DT_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT7_PS	0x42A10738	Counter prescalar register. See TCPWM0_GRP0_CNT0_PS for the details of bit fields.
TCPWM0_GRP1_CNT7_TR_CMD	0x42A10740	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT7_TR_IN_SEL0	0x42A10744	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT7_TR_IN_SEL1	0x42A10748	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT7_TR_IN_EDGE_SEL	0x42A1074C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT7_TR_PWM_CTRL	0x42A10750	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT7_TR_OUT_SEL	0x42A10754	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT7_INTR	0x42A10770	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT7_INTR_SET	0x42A10774	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT7_INTR_MASK	0x42A10778	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT7_INTR_MASKED	0x42A1077C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT7_LFSR	0x42A10780	LFSR register. See TCPWM0_GRP1_CNT0_LFSR for the details of bit fields.
TCPWM0_GRP1_CNT7_ONE_GF0	0x42A10784	Glitch filter register for one to one trigger. See TCPWM0_GRP0_CNT0_ONE_GF0 for the details of bit fields.
TCPWM0_GRP1_CNT7_TR_ONE_SYNC_BYPASS	0x42A107A4	Sync bypass register for one to one trigger. See TCPWM0_GRP0_CNT0_TR_ONE_SYNC_BYPASS for the details of bit fields.

Register	Address	Description
TCPWM0_GRP2_CNT0_CTRL	0x42A20000	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP2_CNT0_STATUS	0x42A20004	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP2_CNT0_COUNTER	0x42A20008	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP2_CNT0_CC0	0x42A20010	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP2_CNT0_CC0_BUFF	0x42A20014	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT0_CC1	0x42A20018	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP2_CNT0_CC1_BUFF	0x42A2001C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT0_PERIOD	0x42A20020	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP2_CNT0_PERIOD_BUFF	0x42A20024	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT0_LINE_SEL	0x42A20028	Counter line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL for the details of bit fields.
TCPWM0_GRP2_CNT0_LINE_SEL_BUFF	0x42A2002C	Counter buffered line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT0_DT	0x42A20030	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP2_CNT0_DT_BUFF	0x42A20034	Counter buffered PWM dead time register. See TCPWM0_GRP0_CNT0_DT_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT0_PS	0x42A20038	Counter prescalar register. See TCPWM0_GRP0_CNT0_PS for the details of bit fields.
TCPWM0_GRP2_CNT0_TR_CMD	0x42A20040	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP2_CNT0_TR_IN_SEL0	0x42A20044	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.

Register	Address	Description
TCPWM0_GRP2_CNT0_TR_IN_SEL1	0x42A20048	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP2_CNT0_TR_IN_EDGE_SEL	0x42A2004C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP2_CNT0_TR_PWM_CTRL	0x42A20050	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP2_CNT0_TR_OUT_SEL	0x42A20054	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP2_CNT0_INTR	0x42A20070	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP2_CNT0_INTR_SET	0x42A20074	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP2_CNT0_INTR_MASK	0x42A20078	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP2_CNT0_INTR_MASKED	0x42A2007C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP2_CNT0_LFSR	0x42A20080	LFSR register. See TCPWM0_GRP1_CNT0_LFSR for the details of bit fields.
TCPWM0_GRP2_CNT0_ONE_GF0	0x42A20084	Glitch filter register for one to one trigger. See TCPWM0_GRP0_CNT0_ONE_GF0 for the details of bit fields.
TCPWM0_GRP2_CNT0_TR_ONE_SYNC_BYPASS	0x42A200A4	Sync bypass register for one to one trigger. See TCPWM0_GRP0_CNT0_TR_ONE_SYNC_BYPASS for the details of bit fields.
TCPWM0_GRP2_CNT1_CTRL	0x42A20100	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP2_CNT1_STATUS	0x42A20104	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP2_CNT1_COUNTER	0x42A20108	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP2_CNT1_CC0	0x42A20110	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.

Register	Address	Description
TCPWM0_GRP2_CNT1_CC0_BUFF	0x42A20114	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT1_CC1	0x42A20118	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP2_CNT1_CC1_BUFF	0x42A2011C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT1_PERIOD	0x42A20120	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP2_CNT1_PERIOD_BUFF	0x42A20124	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT1_LINE_SEL	0x42A20128	Counter line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL for the details of bit fields.
TCPWM0_GRP2_CNT1_LINE_SEL_BUFF	0x42A2012C	Counter buffered line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT1_DT	0x42A20130	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP2_CNT1_DT_BUFF	0x42A20134	Counter buffered PWM dead time register. See TCPWM0_GRP0_CNT0_DT_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT1_PS	0x42A20138	Counter prescalar register. See TCPWM0_GRP0_CNT0_PS for the details of bit fields.
TCPWM0_GRP2_CNT1_TR_CMD	0x42A20140	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP2_CNT1_TR_IN_SEL0	0x42A20144	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP2_CNT1_TR_IN_SEL1	0x42A20148	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP2_CNT1_TR_IN_EDGE_SEL	0x42A2014C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP2_CNT1_TR_PWM_CTRL	0x42A20150	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.

Register	Address	Description
TCPWM0_GRP2_CNT1_TR_OUT_SEL	0x42A20154	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP2_CNT1_INTR	0x42A20170	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP2_CNT1_INTR_SET	0x42A20174	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP2_CNT1_INTR_MASK	0x42A20178	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP2_CNT1_INTR_MASKED	0x42A2017C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP2_CNT1_LFSR	0x42A20180	LFSR register. See TCPWM0_GRP1_CNT0_LFSR for the details of bit fields.
TCPWM0_GRP2_CNT1_ONE_GF0	0x42A20184	Glitch filter register for one to one trigger. See TCPWM0_GRP0_CNT0_ONE_GF0 for the details of bit fields.
TCPWM0_GRP2_CNT1_TR_ONE_SYNC_BYPASS	0x42A201A4	Sync bypass register for one to one trigger. See TCPWM0_GRP0_CNT0_TR_ONE_SYNC_BYPASS for the details of bit fields.
TCPWM0_GRP2_CNT2_CTRL	0x42A20200	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP2_CNT2_STATUS	0x42A20204	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP2_CNT2_COUNTER	0x42A20208	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP2_CNT2_CC0	0x42A20210	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP2_CNT2_CC0_BUFF	0x42A20214	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT2_CC1	0x42A20218	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP2_CNT2_CC1_BUFF	0x42A2021C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.

Register	Address	Description
TCPWM0_GRP2_CNT2_PERIOD	0x42A20220	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP2_CNT2_PERIOD_BUFF	0x42A20224	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT2_LINE_SEL	0x42A20228	Counter line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL for the details of bit fields.
TCPWM0_GRP2_CNT2_LINE_SEL_BUFF	0x42A2022C	Counter buffered line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT2_DT	0x42A20230	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP2_CNT2_DT_BUFF	0x42A20234	Counter buffered PWM dead time register. See TCPWM0_GRP0_CNT0_DT_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT2_PS	0x42A20238	Counter prescalar register. See TCPWM0_GRP0_CNT0_PS for the details of bit fields.
TCPWM0_GRP2_CNT2_TR_CMD	0x42A20240	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP2_CNT2_TR_IN_SEL0	0x42A20244	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP2_CNT2_TR_IN_SEL1	0x42A20248	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP2_CNT2_TR_IN_EDGE_SEL	0x42A2024C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP2_CNT2_TR_PWM_CTRL	0x42A20250	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP2_CNT2_TR_OUT_SEL	0x42A20254	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP2_CNT2_INTR	0x42A20270	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP2_CNT2_INTR_SET	0x42A20274	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.

Register	Address	Description
TCPWM0_GRP2_CNT2_INTR_MASK	0x42A20278	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP2_CNT2_INTR_MASKED	0x42A2027C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP2_CNT2_LFSR	0x42A20280	LFSR register. See TCPWM0_GRP1_CNT0_LFSR for the details of bit fields.
TCPWM0_GRP2_CNT2_ONE_GF0	0x42A20284	Glitch filter register for one to one trigger. See TCPWM0_GRP0_CNT0_ONE_GF0 for the details of bit fields.
TCPWM0_GRP2_CNT2_TR_ONE_SYNC_BYPASS	0x42A202A4	Sync bypass register for one to one trigger. See TCPWM0_GRP0_CNT0_TR_ONE_SYNC_BYPASS for the details of bit fields.
TCPWM0_GRP2_CNT3_CTRL	0x42A20300	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP2_CNT3_STATUS	0x42A20304	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP2_CNT3_COUNTER	0x42A20308	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP2_CNT3_CC0	0x42A20310	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP2_CNT3_CC0_BUFF	0x42A20314	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT3_CC1	0x42A20318	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP2_CNT3_CC1_BUFF	0x42A2031C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT3_PERIOD	0x42A20320	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP2_CNT3_PERIOD_BUFF	0x42A20324	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT3_LINE_SEL	0x42A20328	Counter line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL for the details of bit fields.

Register	Address	Description
TCPWM0_GRP2_CNT3_LINE_SEL_BUFF	0x42A2032C	Counter buffered line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT3_DT	0x42A20330	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP2_CNT3_DT_BUFF	0x42A20334	Counter buffered PWM dead time register. See TCPWM0_GRP0_CNT0_DT_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT3_PS	0x42A20338	Counter prescalar register. See TCPWM0_GRP0_CNT0_PS for the details of bit fields.
TCPWM0_GRP2_CNT3_TR_CMD	0x42A20340	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP2_CNT3_TR_IN_SEL0	0x42A20344	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP2_CNT3_TR_IN_SEL1	0x42A20348	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP2_CNT3_TR_IN_EDGE_SEL	0x42A2034C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP2_CNT3_TR_PWM_CTRL	0x42A20350	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP2_CNT3_TR_OUT_SEL	0x42A20354	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP2_CNT3_INTR	0x42A20370	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP2_CNT3_INTR_SET	0x42A20374	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP2_CNT3_INTR_MASK	0x42A20378	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP2_CNT3_INTR_MASKED	0x42A2037C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP2_CNT3_LFSR	0x42A20380	LFSR register. See TCPWM0_GRP1_CNT0_LFSR for the details of bit fields.

Register	Address	Description
TCPWM0_GRP2_CNT3_ONE_GF0	0x42A20384	Glitch filter register for one to one trigger. See TCPWM0_GRP0_CNT0_ONE_GF0 for the details of bit fields.
TCPWM0_GRP2_CNT3_TR_ONE_SYNC_BYPASS	0x42A203A4	Sync bypass register for one to one trigger. See TCPWM0_GRP0_CNT0_TR_ONE_SYNC_BYPASS for the details of bit fields.
TCPWM0_GRP2_CNT4_CTRL	0x42A20400	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP2_CNT4_STATUS	0x42A20404	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP2_CNT4_COUNTER	0x42A20408	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP2_CNT4_CC0	0x42A20410	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP2_CNT4_CC0_BUFF	0x42A20414	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT4_CC1	0x42A20418	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP2_CNT4_CC1_BUFF	0x42A2041C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT4_PERIOD	0x42A20420	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP2_CNT4_PERIOD_BUFF	0x42A20424	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT4_LINE_SEL	0x42A20428	Counter line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL for the details of bit fields.
TCPWM0_GRP2_CNT4_LINE_SEL_BUFF	0x42A2042C	Counter buffered line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT4_DT	0x42A20430	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP2_CNT4_DT_BUFF	0x42A20434	Counter buffered PWM dead time register. See TCPWM0_GRP0_CNT0_DT_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT4_PS	0x42A20438	Counter prescalar register. See TCPWM0_GRP0_CNT0_PS for the details of bit fields.

Register	Address	Description
TCPWM0_GRP2_CNT4_TR_CMD	0x42A20440	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP2_CNT4_TR_IN_SEL0	0x42A20444	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP2_CNT4_TR_IN_SEL1	0x42A20448	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP2_CNT4_TR_IN_EDGE_SEL	0x42A2044C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP2_CNT4_TR_PWM_CTRL	0x42A20450	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP2_CNT4_TR_OUT_SEL	0x42A20454	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP2_CNT4_INTR	0x42A20470	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP2_CNT4_INTR_SET	0x42A20474	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP2_CNT4_INTR_MASK	0x42A20478	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP2_CNT4_INTR_MASKED	0x42A2047C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP2_CNT4_LFSR	0x42A20480	LFSR register. See TCPWM0_GRP1_CNT0_LFSR for the details of bit fields.
TCPWM0_GRP2_CNT4_ONE_GF0	0x42A20484	Glitch filter register for one to one trigger. See TCPWM0_GRP0_CNT0_ONE_GF0 for the details of bit fields.
TCPWM0_GRP2_CNT4_TR_ONE_SYNC_BYPASS	0x42A204A4	Sync bypass register for one to one trigger. See TCPWM0_GRP0_CNT0_TR_ONE_SYNC_BYPASS for the details of bit fields.
TCPWM0_GRP2_CNT5_CTRL	0x42A20500	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP2_CNT5_STATUS	0x42A20504	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.

Register	Address	Description
TCPWM0_GRP2_CNT5_COUNTER	0x42A20508	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP2_CNT5_CC0	0x42A20510	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP2_CNT5_CC0_BUFF	0x42A20514	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT5_CC1	0x42A20518	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP2_CNT5_CC1_BUFF	0x42A2051C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT5_PERIOD	0x42A20520	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP2_CNT5_PERIOD_BUFF	0x42A20524	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT5_LINE_SEL	0x42A20528	Counter line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL for the details of bit fields.
TCPWM0_GRP2_CNT5_LINE_SEL_BUFF	0x42A2052C	Counter buffered line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT5_DT	0x42A20530	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP2_CNT5_DT_BUFF	0x42A20534	Counter buffered PWM dead time register. See TCPWM0_GRP0_CNT0_DT_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT5_PS	0x42A20538	Counter prescalar register. See TCPWM0_GRP0_CNT0_PS for the details of bit fields.
TCPWM0_GRP2_CNT5_TR_CMD	0x42A20540	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP2_CNT5_TR_IN_SEL0	0x42A20544	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP2_CNT5_TR_IN_SEL1	0x42A20548	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP2_CNT5_TR_IN_EDGE_SEL	0x42A2054C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.

Register	Address	Description
TCPWM0_GRP2_CNT5_TR_PWM_CTRL	0x42A20550	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP2_CNT5_TR_OUT_SEL	0x42A20554	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP2_CNT5_INTR	0x42A20570	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP2_CNT5_INTR_SET	0x42A20574	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP2_CNT5_INTR_MASK	0x42A20578	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP2_CNT5_INTR_MASKED	0x42A2057C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP2_CNT5_LFSR	0x42A20580	LFSR register. See TCPWM0_GRP1_CNT0_LFSR for the details of bit fields.
TCPWM0_GRP2_CNT5_ONE_GF0	0x42A20584	Glitch filter register for one to one trigger. See TCPWM0_GRP0_CNT0_ONE_GF0 for the details of bit fields.
TCPWM0_GRP2_CNT5_TR_ONE_SYNC_BYPASS	0x42A205A4	Sync bypass register for one to one trigger. See TCPWM0_GRP0_CNT0_TR_ONE_SYNC_BYPASS for the details of bit fields.
TCPWM0_GRP2_CNT6_CTRL	0x42A20600	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP2_CNT6_STATUS	0x42A20604	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP2_CNT6_COUNTER	0x42A20608	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP2_CNT6_CC0	0x42A20610	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP2_CNT6_CC0_BUFF	0x42A20614	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT6_CC1	0x42A20618	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.

Register	Address	Description
TCPWM0_GRP2_CNT6_CC1_BUFF	0x42A2061C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT6_PERIOD	0x42A20620	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP2_CNT6_PERIOD_BUFF	0x42A20624	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT6_LINE_SEL	0x42A20628	Counter line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL for the details of bit fields.
TCPWM0_GRP2_CNT6_LINE_SEL_BUFF	0x42A2062C	Counter buffered line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT6_DT	0x42A20630	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP2_CNT6_DT_BUFF	0x42A20634	Counter buffered PWM dead time register. See TCPWM0_GRP0_CNT0_DT_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT6_PS	0x42A20638	Counter prescalar register. See TCPWM0_GRP0_CNT0_PS for the details of bit fields.
TCPWM0_GRP2_CNT6_TR_CMD	0x42A20640	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP2_CNT6_TR_IN_SEL0	0x42A20644	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP2_CNT6_TR_IN_SEL1	0x42A20648	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP2_CNT6_TR_IN_EDGE_SEL	0x42A2064C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP2_CNT6_TR_PWM_CTRL	0x42A20650	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP2_CNT6_TR_OUT_SEL	0x42A20654	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP2_CNT6_INTR	0x42A20670	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.

Register	Address	Description
TCPWM0_GRP2_CNT6_INTR_SET	0x42A20674	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP2_CNT6_INTR_MASK	0x42A20678	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP2_CNT6_INTR_MASKED	0x42A2067C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP2_CNT6_LFSR	0x42A20680	LFSR register. See TCPWM0_GRP1_CNT0_LFSR for the details of bit fields.
TCPWM0_GRP2_CNT6_ONE_GF0	0x42A20684	Glitch filter register for one to one trigger. See TCPWM0_GRP0_CNT0_ONE_GF0 for the details of bit fields.
TCPWM0_GRP2_CNT6_TR_ONE_SYNC_BYPASS	0x42A206A4	Sync bypass register for one to one trigger. See TCPWM0_GRP0_CNT0_TR_ONE_SYNC_BYPASS for the details of bit fields.
TCPWM0_GRP2_CNT7_CTRL	0x42A20700	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP2_CNT7_STATUS	0x42A20704	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP2_CNT7_COUNTER	0x42A20708	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP2_CNT7_CC0	0x42A20710	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP2_CNT7_CC0_BUFF	0x42A20714	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT7_CC1	0x42A20718	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP2_CNT7_CC1_BUFF	0x42A2071C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT7_PERIOD	0x42A20720	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP2_CNT7_PERIOD_BUFF	0x42A20724	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.

Register	Address	Description
TCPWM0_GRP2_CNT7_LINE_SEL	0x42A20728	Counter line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL for the details of bit fields.
TCPWM0_GRP2_CNT7_LINE_SEL_BUFF	0x42A2072C	Counter buffered line selection register. See TCPWM0_GRP0_CNT0_LINE_SEL_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT7_DT	0x42A20730	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP2_CNT7_DT_BUFF	0x42A20734	Counter buffered PWM dead time register. See TCPWM0_GRP0_CNT0_DT_BUFF for the details of bit fields.
TCPWM0_GRP2_CNT7_PS	0x42A20738	Counter prescalar register. See TCPWM0_GRP0_CNT0_PS for the details of bit fields.
TCPWM0_GRP2_CNT7_TR_CMD	0x42A20740	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP2_CNT7_TR_IN_SEL0	0x42A20744	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP2_CNT7_TR_IN_SEL1	0x42A20748	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP2_CNT7_TR_IN_EDGE_SEL	0x42A2074C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP2_CNT7_TR_PWM_CTRL	0x42A20750	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP2_CNT7_TR_OUT_SEL	0x42A20754	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP2_CNT7_INTR	0x42A20770	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP2_CNT7_INTR_SET	0x42A20774	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP2_CNT7_INTR_MASK	0x42A20778	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP2_CNT7_INTR_MASKED	0x42A2077C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.

Register	Address	Description
TCPWM0_GRP2_CNT7_LFSR	0x42A20780	LFSR register. See TCPWM0_GRP1_CNT0_LFSR for the details of bit fields.
TCPWM0_GRP2_CNT7_ONE_GF0	0x42A20784	Glitch filter register for one to one trigger. See TCPWM0_GRP0_CNT0_ONE_GF0 for the details of bit fields.
TCPWM0_GRP2_CNT7_TR_ONE_SYNC_BYPASS	0x42A207A4	Sync bypass register for one to one trigger. See TCPWM0_GRP0_CNT0_TR_ONE_SYNC_BYPASS for the details of bit fields.
TCPWM0_TR_ALL_GF_ALL_GF0	0x42A80000	Glitch filter register for All Group Triggers
TCPWM0_TR_ALL_GF_ALL_GF1	0x42A80004	Glitch filter register for All Group Triggers. See TCPWM0_TR_ALL_GF_ALL_GF0 for the details of bit fields.
TCPWM0_TR_ALL_GF_ALL_GF2	0x42A80008	Glitch filter register for All Group Triggers. See TCPWM0_TR_ALL_GF_ALL_GF0 for the details of bit fields.
TCPWM0_TR_ALL_GF_ALL_GF3	0x42A8000C	Glitch filter register for All Group Triggers. See TCPWM0_TR_ALL_GF_ALL_GF0 for the details of bit fields.
TCPWM0_TR_ALL_GF_ALL_GF4	0x42A80010	Glitch filter register for All Group Triggers. See TCPWM0_TR_ALL_GF_ALL_GF0 for the details of bit fields.
TCPWM0_TR_ALL_GF_ALL_GF5	0x42A80014	Glitch filter register for All Group Triggers. See TCPWM0_TR_ALL_GF_ALL_GF0 for the details of bit fields.
TCPWM0_TR_ALL_GF_ALL_GF6	0x42A80018	Glitch filter register for All Group Triggers. See TCPWM0_TR_ALL_GF_ALL_GF0 for the details of bit fields.
TCPWM0_TR_ALL_GF_ALL_GF7	0x42A8001C	Glitch filter register for All Group Triggers. See TCPWM0_TR_ALL_GF_ALL_GF0 for the details of bit fields.
TCPWM0_TR_ALL_GF_ALL_GF8	0x42A80020	Glitch filter register for All Group Triggers. See TCPWM0_TR_ALL_GF_ALL_GF0 for the details of bit fields.
TCPWM0_TR_ALL_GF_ALL_GF9	0x42A80024	Glitch filter register for All Group Triggers. See TCPWM0_TR_ALL_GF_ALL_GF0 for the details of bit fields.
TCPWM0_TR_ALL_GF_ALL_GF10	0x42A80028	Glitch filter register for All Group Triggers. See TCPWM0_TR_ALL_GF_ALL_GF0 for the details of bit fields.
TCPWM0_TR_ALL_GF_ALL_GF11	0x42A8002C	Glitch filter register for All Group Triggers. See TCPWM0_TR_ALL_GF_ALL_GF0 for the details of bit fields.

Timer, Counter, and Pulse Width Modulator (TCPWM) registers

Register	Address	Description
TCPWM0_TR_ALL_GF_ALL_GF12	0x42A80030	Glitch filter register for All Group Triggers. See TCPWM0_TR_ALL_GF_ALL_GF0 for the details of bit fields.
TCPWM0_TR_ALL_GF_ALL_GF13	0x42A80034	Glitch filter register for All Group Triggers. See TCPWM0_TR_ALL_GF_ALL_GF0 for the details of bit fields.
TCPWM0_TR_ALL_GF_ALL_GF14	0x42A80038	Glitch filter register for All Group Triggers. See TCPWM0_TR_ALL_GF_ALL_GF0 for the details of bit fields.
TCPWM0_TR_ALL_GF_ALL_GF15	0x42A8003C	Glitch filter register for All Group Triggers. See TCPWM0_TR_ALL_GF_ALL_GF0 for the details of bit fields.
TCPWM0_TR_ALL_SYNC_BYPASS_TR_ALL_SYNC_BYPASS0	0x42A90000	Trigger Sync bypass for group trigger
TCPWM0_MOTIF_GRP1_MOTIF0_PCONF	0x42AA4000	Global control register
TCPWM0_MOTIF_GRP1_MOTIF0_PSUS	0x42AA4004	Suspend Configuration
TCPWM0_MOTIF_GRP1_MOTIF0_PRUNS	0x42AA4008	MOTIF run bit set
TCPWM0_MOTIF_GRP1_MOTIF0_PRUN	0x42AA4010	MOTIF run bit status
TCPWM0_MOTIF_GRP1_MOTIF0_HIST	0x42AA4024	Hall Inputs Sample Trigger
TCPWM0_MOTIF_GRP1_MOTIF0_HMEC	0x42AA4028	Hall Mode Extra Config
TCPWM0_MOTIF_GRP1_MOTIF0_HALP	0x42AA4030	Hall Current and Expected patterns
TCPWM0_MOTIF_GRP1_MOTIF0_HALPS	0x42AA4034	Hall Current and Expected shadow patterns
TCPWM0_MOTIF_GRP1_MOTIF0_HOSC	0x42AA4038	Hall Sensor Output Config
TCPWM0_MOTIF_GRP1_MOTIF0_MCM	0x42AA4040	Multi-Channel Mode Pattern
TCPWM0_MOTIF_GRP1_MOTIF0_MCSM	0x42AA4044	Multi-Channel Mode shadow Pattern LUT0
TCPWM0_MOTIF_GRP1_MOTIF0_MCMS	0x42AA4048	Multi-Channel Mode Control set
TCPWM0_MOTIF_GRP1_MOTIF0_MCMC	0x42AA404C	Multi-Channel Mode Control clear
TCPWM0_MOTIF_GRP1_MOTIF0_MCMF	0x42AA4050	Multi-Channel Mode flag status
TCPWM0_MOTIF_GRP1_MOTIF0_MCPF	0x42AA4054	Multi-Channel Pattern Fault
TCPWM0_MOTIF_GRP1_MOTIF0_MOSC	0x42AA4058	Multi-Channel Output Config
TCPWM0_MOTIF_GRP1_MOTIF0_QDC	0x42AA4060	Quadrature Decoder Configuration
TCPWM0_MOTIF_GRP1_MOTIF0_QOSC	0x42AA4064	Quadrature Output Config
TCPWM0_MOTIF_GRP1_MOTIF0_MCMEC	0x42AA4068	Multi-Channel Extra Config
TCPWM0_MOTIF_GRP1_MOTIF0_PFLG	0x42AA4070	MOTIF interrupt status
TCPWM0_MOTIF_GRP1_MOTIF0_PFLGE	0x42AA4074	MOTIF interrupt enable
TCPWM0_MOTIF_GRP1_MOTIF0_SPFLG	0x42AA4078	Interrupt set register
TCPWM0_MOTIF_GRP1_MOTIF0_RPFLG	0x42AA407C	Interrupt clear register
TCPWM0_MOTIF_GRP1_MOTIF0_MCSM1	0x42AA4080	Multi-Channel Mode shadow pattern LUT1
TCPWM0_MOTIF_GRP1_MOTIF0_MCSM2	0x42AA4084	Multi-Channel Mode shadow pattern LUT2
TCPWM0_MOTIF_GRP1_MOTIF0_MCSM3	0x42AA4088	Multi-Channel Mode shadow pattern LUT3

Timer, Counter, and Pulse Width Modulator (TCPWM) registers

Register	Address	Description
TCPWM0_MOTIF_GRP1_MOTIF0_MCSM4	0x42AA408C	Multi-Channel Mode shadow pattern LUT4
TCPWM0_MOTIF_GRP1_MOTIF0_MCSM5	0x42AA4090	Multi-Channel Mode shadow pattern LUT5
TCPWM0_MOTIF_GRP1_MOTIF0_CLUT	0x42AA4094	Hall Mode LUT config
TCPWM0_MOTIF_GRP1_MOTIF0_SLUT	0x42AA4098	Hall Mode LUT status
TCPWM0_MOTIF_GRP1_MOTIF0_PDBG	0x42AA4100	MOTIF Debug Register
TCPWM0_MOTIF_GRP1_MOTIF0_PLP0S	0x42AA4104	MOTIF Low Pass 0 Status
TCPWM0_MOTIF_GRP1_MOTIF0_PLP1S	0x42AA4108	MOTIF Low Pass 1 Status
TCPWM0_MOTIF_GRP1_MOTIF0_PLP2S	0x42AA410C	MOTIF Low Pass 2 Status

15.1.1 TCPWM0_GRP0_CNT0_CTRL

Counter control register

Address: 0x42A00000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	CC1_-MATCH_DOWN_EN	CC1_-MATCH_UP_EN	CC0_-MATCH_DOWN_EN	CC0_-MATCH_UP_EN	AUTO_RE-LOAD_LINE_SEL	AUTO_RE-LOAD_PE-RIOD	AUTO_RE-LOAD_CC1	AUTO_RE-LOAD_CC0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW		RW	RW	RW	RW
HW Access	R	R	R		R	R	R	R
Name	PWM_SYN-C_KILL_DT	PW-M_TC_SYN C_KILL_DT	PWM_DISABLE_MODE [13:12]		SWAP_EN-ABLE	PWM_SYN-C_KILL	PW-M_STOP_O N_KILL	PWM_IM-M_KILL

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		QUAD_ENCODING_-MODE [21:20]		None	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW		RW		
HW Access	R	R	R	R		R		
Name	ENABLED	DBG_-FREEZE_EN	DBG_-SUS_EN	KILL_LINE_POLARITY [28:27]		MODE [26:24]		

Bits	Name	Description
31	ENABLED	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_-SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). Default Value: 0

15.1.1 TCPWM0_GRP0_CNT0_CTRL (continued)

30	DBG_FREEZE_EN	Specifies the counter behavior in debug mode. '0': The counter operation depends on DBG_SUS_EN value, when ='0', counter operation continues; when ='1', Counter Freeze after roll over (tc event) and enters safe state. '1': The counter operation freezes in debug mode depending on DBG_SUS_EN value; when='0', Counter Freeze; when ='1', Counter Freeze immediately and enters safe state and running bit to be made ='0'. Safet state values are defined on line_out and line_compl_out by the corressponding kill_line_out_polarity and kill_line_compl_out_polarity Default Value: 0
29	DBG_SUS_EN	Specifies the counter behavior in debug mode when suspend is enabled '0': The counter operation continues in debug mode as given by bit DBG_FREEZE_EN '1': The counter operation freezes in debug mode depending on DBG_FREEZE_EN value; when = '0', Counter Freeze after roll over (tc event) and enters safe state; when ='1', Counter Freeze immediately and enters safe state and running bit to be made ='0'. Safet state values are defined on line_out and line_compl_out by the corressponding kill_line_out_polarity and kill_line_compl_out_polarity Default Value: 0
28 : 27	KILL_LINE_POLARITY	In PWM and PWM_DT modes, these two bits can be used to invert "line_out" and "line_compl_out" during kill mode Default Value: 0 **0x0: KILL_LINE_POLARITY :** When '0' it is disabled. **0x1: KILL_LINE_OUT_POLARITY :** When bit 0 is '1', inverts the suppressed "line_out" during KILL (PWM/PWM_DT/PWM_DISABLE modes). In the debug mode the safe state of the line_out is defined by this bit value. 1 - line_out will be high 0 - line_out will be low **0x2: KILL_LINE_COMPL_OUT_POLARITY :** When bit 1 is '1', inverts the suppressed "line_comp_out" during KILL (PWM/PWM_DT/PWM_DISABLE modes). In the debug mode the safe state of the line_compl_out is defined by this bit value. 1 - line_compl_out will be high 0 - line_compl_out will be low
26 : 24	MODE	Counter mode. Default Value: 0 **0x0: TIMER :** Timer mode **0x1: Reserved1 :** This setting is reserved. Do not use. **0x2: CAPTURE :** Capture mode **0x3: Reserved3 :** This setting is reserved. Do not use.

15.1.1 TCPWM0_GRP0_CNT0_CTRL (continued)

		0x4: PWM : Pulse width modulation (PWM) mode. HRPWM feature is supported in this mode through HRPWM_CTRL register. **0x5: PWM_DT :** PWM with deadtime insertion mode. HRPWM feature is supported in this mode through HRPWM_CTRL register. **0x6: Reserved6 :** This setting is reserved. Do not use. **0x7: Reserved7 :** This setting is reserved. Do not use.
21 : 20	QUAD_ENCODING_MODE	In PWM, these two bits can be used to invert "line_out" and "line_compl_out". Inversion is the last step in generation of "line_out" and "line_compl_out"; i.e. a disabled output line "line_out" has the value QUAD_ENCODING_MODE[0] and a disabled output line "line_compl_out" has the value QUAD_ENCODING_MODE[1]. In TIMER mode, QUAD_ENCODING_MODE[1:0] is used to enable count up/down based on falling edges, rising edge or level of external capture0 event. Default Value: 0 **0x1: INV_OUT :** In PWM/PWM_DT modes, when bit 0 is '1', QUADRATURE_ENCODING_MODE[0] inverts "line_out" **0x2: INV_COMPL_OUT :** In PWM/PWM_DT modes, when bit 1 is '1', QUADRATURE_ENCODING_MODE[1] inverts "line_compl_out" **0x0: EXT_DIR_DISABLE :** In Timer Mode: Counter changes current count direction is disabled **0x1: EXT_DIR_FALLING :** In Timer Mode: Counter changes current count direction based on falling edge of capture0 input **0x2: EXT_DIR_RISING :** In Timer Mode: Counter changes current count direction based on rising edge of capture0 input **0x3: EXT_DIR_LEVEL :** In Timer Mode: Counter count increase when capture0 level equal to high, counter count decrease when capture0 level equals to low.
18	ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	UP_DOWN_MODE	Determines counter direction. In QUAD mode this field acts as QUAD_RANGE_MODE field selecting between different counter range, reload value and compare / capture behavior. Default Value: 0

15.1.1 TCPWM0_GRP0_CNT0_CTRL (continued)

		0x0: COUNT_UP : Count up (to PERIOD). An overflow event is generated when the counter changes from a state in which COUNTER equals PERIOD. A terminal count event is generated when the counter changes from a state in which COUNTER equals PERIOD. **0x1: COUNT_DOWN :** Count down (to "0"). An underflow event is generated when the counter changes from a state in which COUNTER equals "0". A terminal count event is generated when the counter changes from a state in which COUNTER equals "0". **0x2: COUNT_UPDN1 :** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter changes from a state in which COUNTER equals PERIOD. An underflow event is generated when the counter changes from a state in which COUNTER equals "0". A terminal count event is generated when the counter changes from a state in which COUNTER equals "0". **0x3: COUNT_UPDN2 :** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter changes from a state in which COUNTER equals PERIOD. An underflow event is generated when the counter changes from a state in which COUNTER equals "0". A terminal count event is generated when the counter changes from a state in which COUNTER equals "0" AND when the counter changes from a state in which COUNTER equals PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).
15	PWM_SYNC_KILL_DT	Specifies synchronous DT kill behavior: '1': synchronous DT kill mode: the kill event disables the "line_out" immediately whereas "line_compl_out" signals will be disable after dead time till the next terminal count event (synchronous DT kill). "Line_out" and "line_compl_out" get enable at next tc event after kill input is inactive. In synchronous DT kill mode, STOP_EDGE should be RISING_EDGE. '0': synchronous DT kill mode: Disable This field has a function in PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
14	PWM_TC_SYNC_KILL_DT	Specifies TC synchronour DT kill behavior: '1': TC synchronous DT kill mode: the kill event disables the "line_out" and "line_compl_out" signals at the next terminal count event and till the next terminal count event (synchronous 3 kill). If dead time is enabled, output get disables after the tc event + dead time. "Line_out" and "line_comp_out" get enable at next tc event after input input is inactive In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': TC synchronous DT kill mode: Disable This field has a function in PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
13 : 12	PWM_DISABLE_MODE	Specifies the behavior of the PWM outputs "line_out" and "line_compl_out" while the TCPWM counter is disabled (CTRL.ENABLED='0') or stopped. Note: The output signal of this selection can be further modified by the immediate kill logic and line_out polarity settings (CTRL.QUAL_ENCODING_MODE). Default Value: 0 **0x0: Z :** The behavior is the same is in previous mxtcpwm (version 1). When the counter is disabled the PWM outputs "line_out" and "line_compl_out" are NOT driven by the TCPWM. Instead the port default level configuration applies, e.g. "Z" (high impedance). Note: This is realized by driving the TCPWM output "line_out_en" to 0. When the counter is stopped upon a stop event the PWM outputs are deactivated (to the polarity defined by CTRL.KILL_LINE_POLARITY).

15.1.1 TCPWM0_GRP0_CNT0_CTRL (continued)

		0x1: RETAIN : When the counter is disabled the PWM outputs "line_out" and "line_compl_out" are driven by the TCPWM. When the counter is disabled or stopped upon a stop event the PWM outputs are retained (keep their previous levels). While the counter is disabled or stopped the PWM outputs can be changed via LINE_SEL (when parameter GRP_SMC_PRESENT = 1). **0x2: L :** When the counter is disabled the PWM outputs "line_out" and "line_compl_out" are driven by the TCPWM. When the counter is disabled or stopped upon a stop event the PWM output "line_out" is driven as a fixed '0' and the PWM output "line_compl_out" is driven as a fixed '1'. **0x3: H :** When the counter is disabled the PWM outputs "line_out" and "line_compl_out" are driven by the TCPWM. When the counter is disabled or stopped upon a stop event the PWM output "line_out" is driven as a fixed '1' and the PWM output "line_compl_out" is driven as a fixed '0'.
11	SWAP_ENABLE	Specifies whether swapping mechanism between CC0 and buffered CC0, CC1 and buffered CC1, PERIOD and buffered PERIOD, DT and buffered DT are disabled '0': swap is disable '1': swap is enable Default Value: 0
10	PWM_SYNC_KILL	Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "line_out" and "line_compl_out" signals immediately. "Line_out" and "Line_compl_out" will be enable at the next terminal count event (synchronous kill) after kill event is inactive. In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
9	PWM_STOP_ON_KILL	Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter. This field has a function in PWM and PWM_DT modes only. Default Value: 0
8	PWM_IMM_KILL	Specifies whether the kill event immediately deactivates the "line_out" and "line_compl_out" signals or with the next module clock ("active count" pre-scaled "clk_counter"). '0': synchronous kill activation. Deactivates the "line_out" and "line_compl_out" signals with the next module clock ("active count" pre-scaled "clk_counter"). '1': immediate kill activation. Immediately deactivates the "dt_line_out" and "dt_line_compl_out" signals. This field has a function in PWM and PWM_DT modes only. Default Value: 0
7	CC1_MATCH_DOWN_EN	Enables / disables the compare match 1 event generation (COUNTER equals CC0 register) when counting down (STATUS.DOWN = 1) in CNT_UPDN1/2 mode. '0': compare match 1 event generation disabled when counting down '1': compare match 1 event generation enabled when counting down This field has a function in PWM and PWM_DT modes only. Default Value: 1

15.1.1 TCPWM0_GRP0_CNT0_CTRL (continued)

6	CC1_MATCH_UP_EN	Enables / disables the compare match 1 event generation (COUNTER equals CC0 register) when counting up (STATUS.DOWN = 0) in CNT_UPDN1/2 mode. '0': compare match 1 event generation disabled when counting up '1': compare match 1 event generation enabled when counting up This field has a function in PWM and PWM_DT modes only. Default Value: 1
5	CC0_MATCH_DOWN_EN	Enables / disables the compare match 0 event generation (COUNTER equals CC0 register) when counting down (STATUS.DOWN = 1) in CNT_UPDN1/2 mode. '0': compare match 0 event generation disabled when counting down '1': compare match 0 event generation enabled when counting down This field has a function in PWM and PWM_DT modes only. Default Value: 1
4	CC0_MATCH_UP_EN	Enables / disables the compare match 0 event generation (COUNTER equals CC0 register) when counting up (STATUS.DOWN = 0) in CNT_UPDN1/2 mode. '0': compare match 0 event generation disabled when counting up '1': compare match 0 event generation enabled when counting up This field has a function in PWM and PWM_DT modes only. Default Value: 1
3	AUTO_RELOAD_LINE_-SEL	Specifies switching of the LINE_SEL and LINE_BUFF_SEL values. This field has a function in PWM mode. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. Default Value: 0
2	AUTO_RELOAD_PERIOD	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff. Default Value: 0
1	AUTO_RELOAD_CC1	Specifies switching of the CC1 and buffered CC1 values. This field has a function in TIMER, PWM and PWM_DT modes. Timer modes: '0': never switch. '1': switch on a compare match 1 event. PWM and PWM_DT modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0
0	AUTO_RELOAD_CC0	Specifies switching of the CC0 and buffered CC0 values. This field has a function in TIMER, PWM and PWM_DT modes. Timer mode: '0': never switch. '1': switch on a compare match 0 event. PWM and PWM_DT modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0

15.1.2 TCPWM0_GRP0_CNT0_STATUS

Counter status register

Address: 0x42A00004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	TR_STOP	TR_RE-LOAD	TR_COUNT	TR_CAP-TURE0	KILL_STA-TUS	CC1_READ_MISS	CC0_READ_MISS	DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R	None			R	R	R	R
HW Access	RW	None			RW	RW	RW	RW
Name	RUNNING	None [14:12]			LINE_COM-PL_OUT	LINE_OUT	TR_CAP-TURE1	TR_START

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	DT_CNT_L [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	DT_CNT_H [31:24]							

Bits	Name	Description
31 : 24	DT_CNT_H	High byte of 16-bit dead time counter. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this field has no effect. Note: This field only exists when parameter GRP_AMC_PRESENT for advanced motor control is set to 1. Otherwise the dead time is only 8bit wide and the only the field DT_CNT_L is used as dead time counter. Default Value: 0
23 : 16	DT_CNT_L	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion (8bit dead time counter or low byte of 16-bit dead time counter). Default Value: 0
15	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. This field is used to indicate that the counter is running after a start/reload event and that the counter is stopped after a stop event. When a running counter operation is paused in debug state (see CTRL.DBG_PAUSE) then the RUNNING bit is still '1'. Default Value: 0
11	LINE_COMPL_OUT	Indicates the actual level of the complementary PWM line output signal. Default Value: 0
10	LINE_OUT	Indicates the actual level of the PWM line output signal. Default Value: 0
9	TR_CAPTURE1	Indicates the actual level of the selected capture 1 trigger. Default Value: 0

15.1.2 TCPWM0_GRP0_CNT0_STATUS (continued)

8	TR_START	Indicates the actual level of the selected start trigger. Default Value: 0
7	TR_STOP	Indicates the actual level of the selected stop trigger. Default Value: 0
6	TR_RELOAD	Indicates the actual level of the selected reload trigger. Default Value: 0
5	TR_COUNT	Indicates the actual level of the selected count trigger. Default Value: 1
4	TR_CAPTURE0	Indicates the actual level of the selected capture 0 trigger. Default Value: 0
3	KILL_STATUS	When '0', There is no kill event in pwm, pwm_dt operation When '1', There is kill event currently active in pwm, pwm_dt operation Default Value: 0
2	CC1_READ_MISS	When '0', CPU did not miss reading capture1 event information When '1', CPU miss reading past capture1 event information Default Value: 0
1	CC0_READ_MISS	When '0', CPU did not miss reading capture0 event information When '1', CPU miss reading past capture0 event information Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down.

15.1.3 TCPWM0_GRP0_CNT0_COUNTER

Counter count register

Address: 0x42A00008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	COUNTER [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	COUNTER [31:24]							

Bits	Name	Description
31 : 0	COUNTER	16-bit / 32-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

15.1.4 TCPWM0_GRP0_CNT0_CC0

Counter compare/capture 0 register

Address: 0x42A00010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	CC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	CC [31:24]							

Bits	Name	Description
31 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. In compare mode 6 LSBs is used for HRPWM generation when HRPWM is enabled. Default Value: 4294967295

15.1.5 TCPWM0_GRP0_CNT0_CC0_BUFF

Counter buffered compare/capture 0 register

Address: 0x42A00014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	CC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	CC [31:24]							

Bits	Name	Description
31 : 0	CC	Additional buffer for counter CC register. In compare mode 6 LSBs is used for HRPWM generation when HRPWM is enabled. Default Value: 4294967295

15.1.6 TCPWM0_GRP0_CNT0_CC1

Counter compare/capture 1 register

Address: 0x42A00018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	CC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	CC [31:24]							

Bits	Name	Description
31 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. In compare mode 6 LSBs is used for HRPWM generation when HRPWM is enabled. Default Value: 4294967295

15.1.7 TCPWM0_GRP0_CNT0_CC1_BUFF

Counter buffered compare/capture 1 register

Address: 0x42A0001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	CC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	CC [31:24]							

Bits	Name	Description
31 : 0	CC	Additional buffer for counter CC1 register. In compare mode 6 LSBs is used for HRPWM generation when HRPWM is enabled. Default Value: 4294967295

15.1.8 TCPWM0_GRP0_CNT0_PERIOD

Counter period register

Address: 0x42A00020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	PERIOD [31:24]							

Bits	Name	Description
31 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. In PWM and PWM_DT mode 6 LSBs given by are used for HRPWM generation when HRPWM is enabled. Default Value: 4294967295

15.1.9 TCPWM0_GRP0_CNT0_PERIOD_BUFF

Counter buffered period register

Address: 0x42A00024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	PERIOD [31:24]							

Bits	Name	Description
31 : 0	PERIOD	Additional buffer for counter PERIOD register. In PWM and PWM_DT mode 6 LSBs given by are used for HRPWM generation when HRPWM is enabled. Note: GRP_HRPWM_WIDTH is 6 Default Value: 4294967295

15.1.10 TCPWM0_GRP0_CNT0_LINE_SEL

Counter line selection register

Address: 0x42A00028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	RW			None	RW		
Name	None	COMPL_OUT_SEL [6:4]			None	OUT_SEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 4	COMPL_OUT_SEL	Selects the source for the output signal "line_compl_out". Default setting is the inverted PWM signal "line". Other settings are useful for Stepper Motor Control. This field has a function in PWM and PWM_DT modes only. Note: The output signal of this selection can be further modified by the stop / kill logic and line_-compl_out polarity setting (CTRL.KILL_LINE_COMPL_OUT_POLARITY). Default Value: 3 **0x0: L :** fixed '0' **0x1: H :** fixed '1' **0x2: PWM :** PWM signal "line" **0x3: PWM_INV :** inverted PWM signal "line"

15.1.10 TCPWM0_GRP0_CNT0_LINE_SEL (continued)

0x4: Z :

The output "line_compl_out" is not driven by the TCPWM. Instead the port default level configuration applies, e.g. "Z" (high impedance).
Note: This is realized by driving the output "line_compl_out_en" to 0.

0x5: MOTIF :

The source for PWM signal conditioning comes from MOTIF modulation output control signals. "line_compl_out" can be set to '0' , '1' or PWM.

0x6: Reserved6 :

This setting is reserved. Do not use.

0x7: Reserved7 :

This setting is reserved. Do not use.

2 : 0	OUT_SEL	Selects the source for the output signal "line_out". Default setting is the PWM signal "line". Other settings are useful for Stepper Motor Control. This field has a function in PWM and PWM_DT modes only. Note: The output signal of this selection can be further modified by the stop / kill logic and line_out polarity setting (CTRL.KILL_LINE_OUT_POLARITY). Default Value: 2

0x0: L :

fixed '0'

0x1: H :

fixed '1'

0x2: PWM :

PWM signal "line"

0x3: PWM_INV :

inverted PWM signal "line"

0x4: Z :

The output "line_out" is not driven by the TCPWM. Instead the port default level configuration applies, e.g. "Z" (high impedance).
Note: This is realized by driving the output "line_out_en" to 0.

0x5: MOTIF :

The source for PWM signal conditioning comes from MOTIF modulation output control signals. "line_out" can be set to '0' , '1' or PWM.

0x6: Reserved6 :

This setting is reserved. Do not use.

15.1.10 TCPWM0_GRP0_CNT0_LINE_SEL (continued)

0x7: Reserved7 :

This setting is reserved. Do not use.

15.1.11 TCPWM0_GRP0_CNT0_LINE_SEL_BUFF

Counter buffered line selection register

Address: 0x42A0002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	RW			None	RW		
Name	None	COMPL_OUT_SEL [6:4]			None	OUT_SEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 4	COMPL_OUT_SEL	Buffer for LINE_SEL.COMPL.OUT_SEL. Can be exchanged with LINE_SEL.LINE_COMPL_OUT_SEL on a terminal count event with an actively pending switch event. This field has a function in PWM and PWM_DT modes only. Default Value: 3
2 : 0	OUT_SEL	Buffer for LINE_SEL.OUT_SEL. Can be exchanged with LINE_SEL.LINE_OUT_SEL on a terminal count event with an actively pending switch event. This field has a function in PWM and PWM_DT modes only. Default Value: 2

15.1.12 TCPWM0_GRP0_CNT0_DT

Counter PWM dead time register

Address: 0x42A00030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DT_LINE_OUT_L [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DT_LINE_OUT_H [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DT_LINE_COMPL_OUT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DT_LINE_COMPL_OUT [31:24]							

Bits	Name	Description
31 : 16	DT_LINE_COMPL_OUT	In PWM_DT mode, this field is used to determine the dead time before activating the complementary PWM line output signal "line_compl_out": amount of dead time cycles in the counter clock domain. In all other modes, this field has no effect. In PWM_DT mode 6 LSBs given by are used for HRPWM generation when HRPWM is enabled. Note: This field only exists when parameter GRP_AMC_PRESENT for advanced motor control is set to 1. Otherwise the dead time is only 8 bit wide and the same dead time specified by field DT_LINE_OUT_L is used before activating "line_out" and "line_compl_out". Default Value: 0
15 : 8	DT_LINE_OUT_H	In PWM_DT mode, this field is used to determine the high byte of the dead time before activating the PWM line output signal "line_out": amount of dead time cycles in the counter clock domain. In all other modes, this field has no effect. In PWM_DT mode 6 LSBs given by are used for HRPWM generation when HRPWM is enabled. Note: This field only exists when parameter GRP_AMC_PRESENT for advanced motor control is set to 1. Otherwise the dead time is only 8 bit wide and the same dead time specified by field DT_LINE_OUT_L is used before activating "line_out" and "line_compl_out". Default Value: 0
7 : 0	DT_LINE_OUT_L	In PWM_DT mode, this field is used to determine the low byte of the dead time before activating the PWM line output signal "line_out": amount of dead time cycles in the counter clock domain. Note: This field determines the low byte of the 16-bit dead time before activating "line_out" when parameter GRP_AMC_PRESENT for advanced motor control is set to 1. Otherwise the dead time is only 8 bit wide and the same dead time specified by this DT_LINE_OUT_L field is used before activating "line_out" and "line_compl_out". Default Value: 0

15.1.13 TCPWM0_GRP0_CNT0_DT_BUFF

Counter buffered PWM dead time register

Address: 0x42A00034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DT_LINE_OUT_L [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DT_LINE_OUT_H [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DT_LINE_COMPL_OUT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DT_LINE_COMPL_OUT [31:24]							

Bits	Name	Description
31 : 16	DT_LINE_COMPL_OUT	Buffer for DT.DT_LINE_COMPL_OUT register Data will shadow transfer to DT.DT_LINE_COMPL_OUT on a terminal count event with an actively pending switch when CTRL.SWAP_ENABLE is set to 0. In PWM_DT mode, the data in this field will be shadow transfer to DT.DT_LINE_COMPL_OUT Note: This field only exists when parameter GRP_AMC_PRESENT for advanced motor control is set to 1. Otherwise, the dead time is only 8 bit wide and the same dead time specified by field DT_LINE_OUT_L is used. In PWM_DT mode 6 LSBs given by are used for HRPWM generation when HRPWM is enabled. Default Value: 0
15 : 8	DT_LINE_OUT_H	Buffer for DT.DT_LINE_OUT_H register Data will shadow transfer to DT.DT_LINE_OUT_H on a terminal count event with an actively pending switch event when CTRL.SWAP_ENABLE is set to 0. In PWM_DT mode, the data in this field will be shadow transfer to DT.DT_LINE_OUT_H to determine the high byte of the dead time. In PWM_DT mode 6 LSBs given by are used for HRPWM generation when HRPWM is enabled. Note: This field only exists when parameter GRP_AMC_PRESENT for advanced motor control is set to 1. Otherwise, the dead time buffer is only 8 bit wide Default Value: 0
7 : 0	DT_LINE_OUT_L	Buffer for DT.DT_LINE_OUT_L register Data will shadow transfer to DT.DT_LINE_OUT_L on a terminal count event with an actively pending switch event when CTRL.SWAP_ENABLE is set to 0. In PWM_DT mode, the data in this field will be shadow transfer to DT.DT_LINE_OUT_L to determine the low byte of the dead time Note: This field determines the low byte of the 16-bit dead time buffer when parameter GRP_AMC_PRESENT for advanced motor control is set to 1. Otherwise the dead time buffer is only 8 bit wide. Default Value: 0

15.1.14 TCPWM0_GRP0_CNT0_PS

Counter prescalar register

Address: 0x42A00038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					PS_DIV [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	PS_DIV	Select the pre-scaling of the selected counter clock. If HRPWM is intended to be used for the counter output, this value shall be set to default '0' else the HRPWM feature will not work. Default Value: 0 **0x0: DIVBY1 :** Pre-scaling of the selected counter clock. Divide by 1 **0x1: DIVBY2 :** Pre-scaling of the selected counter clock. Divide by 2 **0x2: DIVBY4 :** Pre-scaling of the selected counter clock. Divide by 4 **0x3: DIVBY8 :** Pre-scaling of the selected counter clock. Divide by 8 **0x4: DIVBY16 :** Pre-scaling of the selected counter clock. Divide by 16

15.1.14 TCPWM0_GRP0_CNT0_PS (continued)

0x5: DIVBY32 :

Pre-scaling of the selected counter clock. Divide by 32

0x6: DIVBY64 :

Pre-scaling of the selected counter clock. Divide by 64

0x7: DIVBY128 :

Pre-scaling of the selected counter clock. Divide by 128

15.1.15 TCPWM0_GRP0_CNT0_TR_CMD

Counter trigger command register

Address: 0x42A00040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1S	RW1S	RW1S	RW1S	None	RW1S
HW Access	None		RW1C	RW1C	RW1C	RW1C	None	RW1C
Name	None [7:6]		CAPTURE1	START	STOP	RELOAD	None	CAPTURE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	CAPTURE1	SW capture 1 trigger. For HW behavior, see COUNTER_CAPTURE0 field. Default Value: 0
4	START	SW start trigger. For HW behavior, see COUNTER_CAPTURE0 field. Default Value: 0
3	STOP	SW stop trigger. For HW behavior, see COUNTER_CAPTURE0 field. Default Value: 0
2	RELOAD	SW reload trigger. For HW behavior, see COUNTER_CAPTURE0 field. Default Value: 0
0	CAPTURE0	SW capture 0 trigger. When written with '1', a capture 0 trigger is generated and the HW sets the field to '0' when the SW trigger has taken effect. It should be noted that the HW operates on the counter frequency. If the counter is disabled through CTRL.ENABLED, the field is immediately set to '0'. Default Value: 0

15.1.16 TCPWM0_GRP0_CNT0_TR_IN_SEL0

Counter input trigger selection register 0

Address: 0x42A00044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		CAPTURE0_SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW					
HW Access	None		R					
Name	None [15:14]		COUNT_SEL [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW					
HW Access	None		R					
Name	None [23:22]		RELOAD_SEL [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW					
HW Access	None		R					
Name	None [31:30]		STOP_SEL [29:24]					

Bits	Name	Description
29 : 24	STOP_SEL	Selects one of the 256 input triggers as a stop trigger. In PWM and PWM_DT modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
21 : 16	RELOAD_SEL	Selects one of the 256 input triggers as a reload trigger. Default Value: 0
13 : 8	COUNT_SEL	Selects one of the 256 input triggers as a count trigger. Note: In the modes: TIMER, CAPTURE, PWM, PWM_DT, and SR, If the counter is externally triggered (COUNT_SEL > 1), an external trigger will be required for each TR_CMD to execute. For example, a write to TR_CMD.START will not start the counter until the trigger selected by COUNT_SEL asserts. The next trigger will increment the counter since the counter is now running. This goes for all TR_CMD fields. Default Value: 1
5 : 0	CAPTURE0_SEL	Selects one of the up to 256 input triggers as a capture0 trigger. Input trigger 0 is always '0' and input trigger 1 is always '1'. If existing, the one-to-one trigger inputs "tr_one_cnt_in" (different to each counter) are selected by setting 2 and above. The settings above are used for the general purpose trigger inputs "tr_all_cnt_in" connected to all counters selected. In the PWM and PWM_DT modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0

15.1.17 TCPWM0_GRP0_CNT0_TR_IN_SEL1

Counter input trigger selection register 1

Address: 0x42A00048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		START_SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW					
HW Access	None		R					
Name	None [15:14]		CAPTURE1_SEL [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13 : 8	CAPTURE1_SEL	Selects one of the 256 input triggers as a capture 1 trigger. Default Value: 0
5 : 0	START_SEL	Selects one of the 256 input triggers as a start trigger. Default Value: 0

15.1.18 TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL

Counter input trigger edge selection register

Address: 0x42A0004C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE0_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [15:12]				CAPTURE1_EDGE [11:10]		START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 10	CAPTURE1_EDGE	A capture 1 event will copy the counter value into the CC1 register. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event. **0x2: ANY_EDGE :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.
9 : 8	START_EDGE	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event.

15.1.18 TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL (continued)

		0x1: FALLING_EDGE : Falling edge. Any falling edge generates an event. **0x2: ANY_EDGE :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.
7 : 6	STOP_EDGE	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event. **0x2: ANY_EDGE :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.
5 : 4	RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event. **0x2: ANY_EDGE :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.
3 : 2	COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event.

15.1.18 TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL (continued)

		0x1: FALLING_EDGE : Falling edge. Any falling edge generates an event. **0x2: ANY_EDGE :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.
1 : 0	CAPTURE0_EDGE	A capture 0 event will copy the counter value into the CC0 register. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event. **0x2: ANY_EDGE :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.

15.1.19 TCPWM0_GRP0_CNT0_TR_PWM_CTRL

Counter trigger PWM control register

Address: 0x42A00050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	CC1_MATCH_MODE [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC0_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	CC1_MATCH_MODE	Determines the effect of a compare match 1 event (COUNTER equals CC1 register) on the "line_out" output signals. Default Value: 3 **0x0: SET :** Set to '1' **0x1: CLEAR :** Set to '0' **0x2: INVERT :** Invert **0x3: NO_CHANGE :** No Change
5 : 4	UNDERFLOW_MODE	Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3

15.1.19 TCPWM0_GRP0_CNT0_TR_PWM_CTRL (continued)

		0x0: SET : Set to '1' **0x1: CLEAR :** Set to '0' **0x2: INVERT :** Invert **0x3: NO_CHANGE :** No Change
3 : 2	OVERFLOW_MODE	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3 **0x0: SET :** Set to '1' **0x1: CLEAR :** Set to '0' **0x2: INVERT :** Invert **0x3: NO_CHANGE :** No Change
1 : 0	CC0_MATCH_MODE	Determines the effect of a compare match 0 event (COUNTER equals CC0 register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0%, the counter CC0 register should be set to "0". For a 100% duty cycle, the counter CC0 register should be set to larger than the counter PERIOD register. Default Value: 3 **0x0: SET :** Set to '1' **0x1: CLEAR :** Set to '0' **0x2: INVERT :** Invert **0x3: NO_CHANGE :** No Change

15.1.20 TCPWM0_GRP0_CNT0_TR_OUT_SEL

Counter output trigger selection register

Address: 0x42A00054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	OUT1 [6:4]			None	OUT0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 4	OUT1	Selects one of the internal events to generate the output trigger 1. Default setting selects the compare match 0 event. Default Value: 3 **0x0: OVERFLOW :** Overflow event **0x1: UNDERFLOW :** Underflow event **0x2: TC :** Terminal count event **0x3: CC0_MATCH :** Compare match 0 event (default selection) **0x4: CC1_MATCH :** Compare match 1 event

15.1.20 TCPWM0_GRP0_CNT0_TR_OUT_SEL (continued)

		0x5: LINE_OUT : PWM output signal "line_out" **0x6: CC0_CC1_MATCH :** Compare match 0 event or Compare match 1 event **0x7: Disabled :** Output trigger disabled.
2 : 0	OUT0	Selects one of the internal events to generate the output trigger 0. Default setting selects the terminal count event. Default Value: 2 **0x0: OVERFLOW :** Overflow event **0x1: UNDERFLOW :** Underflow event **0x2: TC :** Terminal count event (default selection) **0x3: CC0_MATCH :** Compare match 0 event **0x4: CC1_MATCH :** Compare match 1 event **0x5: LINE_OUT :** PWM output signal "line_out" **0x6: CC0_CC1_MATCH :** Compare match 0 event or Compare match 1 event **0x7: Disabled :** Output trigger disabled.

15.1.21 TCPWM0_GRP0_CNT0_INTR

Interrupt request register

Address: 0x42A00070

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [7:3]					CC1_-MATCH	CC0_-MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CC1_MATCH	Counter matches CC1 register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
1	CC0_MATCH	Counter matches CC0 register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

15.1.22 TCPWM0_GRP0_CNT0_INTR_SET

Interrupt set request register

Address: 0x42A00074

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [7:3]					CC1_-MATCH	CC0_-MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CC1_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	CC0_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

15.1.23 TCPWM0_GRP0_CNT0_INTR_MASK

Interrupt mask register

Address: 0x42A00078

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					CC1_-MATCH	CC0_-MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CC1_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	CC0_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

15.1.24 TCPWM0_GRP0_CNT0_INTR_MASKED

Interrupt masked request register

Address: 0x42A0007C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [7:3]					CC1_-MATCH	CC0_-MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CC1_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
1	CC0_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	TC	Logical and of corresponding request and mask bits. Default Value: 0

15.1.25 TCPWM0_GRP0_CNT0_ONE_GF0

Glitch filter register for one to one trigger

Address: 0x42A00084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW		RW		
HW Access	None			R		R		
Name	None [7:5]			GFPS_DIV [4:3]		GF_DEPTH [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 3	GFPS_DIV	Select the glitch filter pre-scaling of the selected counter clock Default Value: 0 **0x0: GFPS_DIVBY1 :** Glitch filter pre-scaling of the selected counter clock. Divide by 1 **0x1: GFPS_DIVBY2 :** Glitch filter pre-scaling of the selected counter clock. Divide by 2 **0x2: GFPS_DIVBY4 :** Glitch filter pre-scaling of the selected counter clock. Divide by 4 **0x3: GFPS_DIVBY8 :** Glitch filter pre-scaling of the selected counter clock. Divide by 8
2 : 0	GF_DEPTH	Select the glitch filter depth Default Value: 0 **0x0: DEPTHX0 :** Glitch filter is turned off

15.1.25 TCPWM0_GRP0_CNT0_ONE_GF0 (continued)

0x1: DEPTHX1 :

Glitch filter depth is set to 1 x GFPS_DIVBYx of prescalar, where x is 1, 2, 4, 8

0x2: DEPTHX2 :

Glitch filter depth is set to 2 x GFPS_DIVBYx of prescalar, where x is 1, 2, 4, 8

0x3: DEPTHX4 :

Glitch filter depth is set to 4 x GFPS_DIVBYx of prescalar, where x is 1, 2, 4, 8

0x4: DEPTHX8 :

Glitch filter depth is set to 8 x GFPS_DIVBYx of prescalar, where x is 1, 2, 4, 8

0x5: DEPTHX16 :

Glitch filter depth is set to 16 x GFPS_DIVBYx of prescalar, where x is 1, 2, 4, 8

0x6: DEPTHX32 :

Glitch filter depth is set to 32 x GFPS_DIVBYx of prescalar, where x is 1, 2, 4, 8

0x7: DEPTHX64 :

Glitch filter depth is set to 64 x GFPS_DIVBYx of prescalar, where x is 1, 2, 4, 8

15.1.26 TCPWM0_GRP0_CNT0_TR_ONE_SYNC_BYPASS

Sync bypass register for one to one trigger

Address: 0x42A000A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					SYNC_BYPASS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	SYNC_BYPASS	When set='1', bypass the sync stage for the corresponding one to one trigger Default Value: 0

15.1.27 TCPWM0_GRP0_CNT0_HRPWM_CTRL

Counter control register for HRPWM feature

Address: 0x42A000B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		None				RW
HW Access	None	R		None				R
Name	None	FREQ_SEL [6:5]		None [4:1]				HRPW-M_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 5	FREQ_SEL	Selects the frequency of operation of HRPWM feature. Microtick is adjusted based on this information. These bits specifies the frequency of CLK_OUT from TCPWM counter. CLK_OUT = CLK_PERI = CLK_HF3 Default Value: 0 **0x0: FREQ_SELX0 :** CLK_OUT = 80 MHz or 100 MHz **0x1: FREQ_SELX1 :** CLK_OUT = 160MHz or 180 MHz **0x2: FREQ_SELX2 :** CLK_OUT = CLK_OUT = 160MHz or 180 MHz **0x3: FREQ_SELX3 :** Reserved
0	HRPWM_EN	When '0' HRPWM feature is bypass, when '1' HRPWM feature is enabled. When enabled HRPWM feature is only available in PWM and PWM_DT mode. In other modes this bit will have no effect and HRPWM feature remain bypass Default Value: 0

15.1.28 TCPWM0_GRP1_CNT0_CTRL

Counter control register

Address: 0x42A10000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	CC1_-MATCH_DOWN_EN	CC1_-MATCH_UP_EN	CC0_-MATCH_DOWN_EN	CC0_-MATCH_UP_EN	AUTO_RE-LOAD_LINE_SEL	AUTO_RE-LOAD_PE-RIOD	AUTO_RE-LOAD_CC1	AUTO_RE-LOAD_CC0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW		RW	RW	RW	RW
HW Access	R	R	R		R	R	R	R
Name	PWM_SYN-C_KILL_DT	PW-M_TC_SYN C_KILL_DT	PWM_DISABLE_MODE [13:12]		SWAP_EN-ABLE	PWM_SYN-C_KILL	PW-M_STOP_O N_KILL	PWM_IM-M_KILL

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW		None	RW	RW	
HW Access	R		R		None	R	R	
Name	DITHEREN [23:22]		QUAD_ENCODING_-MODE [21:20]		None	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW		RW		
HW Access	R	R	R	R		R		
Name	ENABLED	DBG_-FREEZE_EN	DBG_-SUS_EN	KILL_LINE_POLARITY [28:27]		MODE [26:24]		

Bits	Name	Description
31	ENABLED	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_-SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). Default Value: 0

15.1.28 TCPWM0_GRP1_CNT0_CTRL (continued)

30	DBG_FREEZE_EN	Specifies the counter behavior in debug mode. '0': The counter operation depends on DBG_SUS_EN value, when ='0', counter operation continues; when ='1', Counter Freeze after roll over (tc event) and enters safe state. '1': The counter operation freezes in debug mode depending on DBG_SUS_EN value; when='0', Counter Freeze; when ='1', Counter Freeze immediately and enters safe state and running bit to be made ='0'. Safet state values are defined on line_out and line_compl_out by the corressponding kill_line_out_polarity and kill_line_compl_out_polarity Default Value: 0
29	DBG_SUS_EN	Specifies the counter behavior in debug mode when suspend is enabled '0': The counter operation continues in debug mode as given by bit DBG_FREEZE_EN '1': The counter operation freezes in debug mode depending on DBG_FREEZE_EN value; when = '0', Counter Freeze after roll over (tc event) and enters safe state; when ='1', Counter Freeze immediately and enters safe state and running bit to be made ='0'. Safet state values are defined on line_out and line_compl_out by the corressponding kill_line_out_polarity and kill_line_compl_out_polarity Default Value: 0
28 : 27	KILL_LINE_POLARITY	In PWM and PWM_DT modes, these two bits can be used to invert "line_out" and "line_compl_out" during kill mode Default Value: 0 **0x0: KILL_LINE_POLARITY :** When '0' it is disabled. **0x1: KILL_LINE_OUT_POLARITY :** When bit 0 is '1', inverts the suppressed "line_out" during KILL (PWM/PWM_DT/PWM_DISABLE modes). In the debug mode the safe state of the line_out is defined by this bit value. 1 - line_out will be high 0 - line_out will be low **0x2: KILL_LINE_COMPL_OUT_POLARITY :** When bit 1 is '1', inverts the suppressed "line_comp_out" during KILL (PWM/PWM_DT/PWM_DISABLE modes). In the debug mode the safe state of the line_compl_out is defined by this bit value. 1 - line_compl_out will be high 0 - line_compl_out will be low
26 : 24	MODE	Counter mode. Default Value: 0 **0x0: TIMER :** Timer mode **0x1: Reserved1 :** This setting is reserved. Do not use. **0x2: CAPTURE :** Capture mode **0x3: Reserved3 :** This setting is reserved. Do not use.

15.1.28 TCPWM0_GRP1_CNT0_CTRL (continued)

		0x4: PWM : Pulse width modulation (PWM) mode. HRPWM feature is supported in this mode through HRPWM_CTRL register. **0x5: PWM_DT :** PWM with deadtime insertion mode. HRPWM feature is supported in this mode through HRPWM_CTRL register. **0x6: Reserved6 :** This setting is reserved. Do not use. **0x7: Reserved7 :** This setting is reserved. Do not use.
23 : 22	DITHEREN	When '0', dithering is disabled Default Value: 0 **0x1: PERIOD_DITHEN :** Period dithering is enabled **0x2: DUTY_DITHEN :** Duty dithering is enabled **0x3: PER_DUTY_DITHEN :** Period and Duty dithering is enabled
21 : 20	QUAD_ENCODING_MODE	In PWM, these two bits can be used to invert "line_out" and "line_compl_out". Inversion is the last step in generation of "line_out" and "line_compl_out"; i.e. a disabled output line "line_out" has the value QUAD_ENCODING_MODE[0] and a disabled output line "line_compl_out" has the value QUAD_ENCODING_MODE[1]. In TIMER mode, QUAD_ENCODING_MODE[1:0] is used to enable count up/down based on falling edges, rising edge or level of external capture0 event. Default Value: 0 **0x1: INV_OUT :** In PWM/PWM_DT modes, when bit 0 is '1', QUADRATURE_ENCODING_MODE[0] inverts "line_out" **0x2: INV_COMPL_OUT :** In PWM/PWM_DT modes, when bit 1 is '1', QUADRATURE_ENCODING_MODE[1] inverts "line_compl_out" **0x0: EXT_DIR_DISABLE :** In Timer Mode: Counter changes current count direction is disabled **0x1: EXT_DIR_FALLING :** In Timer Mode: Counter changes current count direction based on falling edge of capture0 input

15.1.28 TCPWM0_GRP1_CNT0_CTRL (continued)

		0x2: EXT_DIR_RISING : In Timer Mode: Counter changes current count direction based on rising edge of capture0 input **0x3: EXT_DIR_LEVEL :** In Timer Mode: Counter count increase when capture0 level equal to high, counter count decrease when capture0 level equals to low.
18	ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	UP_DOWN_MODE	Determines counter direction. Default Value: 0 **0x0: COUNT_UP :** Count up (to PERIOD). An overflow event is generated when the counter changes from a state in which COUNTER equals PERIOD. A terminal count event is generated when the counter changes from a state in which COUNTER equals PERIOD. **0x1: COUNT_DOWN :** Count down (to "0"). An underflow event is generated when the counter changes from a state in which COUNTER equals "0". A terminal count event is generated when the counter changes from a state in which COUNTER equals "0". **0x2: COUNT_UPDN1 :** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter changes from a state in which COUNTER equals PERIOD. An underflow event is generated when the counter changes from a state in which COUNTER equals "0". A terminal count event is generated when the counter changes from a state in which COUNTER equals "0". **0x3: COUNT_UPDN2 :** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter changes from a state in which COUNTER equals PERIOD. An underflow event is generated when the counter changes from a state in which COUNTER equals "0". A terminal count event is generated when the counter changes from a state in which COUNTER equals "0" AND when the counter changes from a state in which COUNTER equals PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).
15	PWM_SYNC_KILL_DT	Specifies synchronous DT kill behavior: '1': synchronous DT kill mode: the kill event disables the "line_out" immediately whereas "line_compl_out" signals will be disable after dead time till the next terminal count event (synchronous DT kill). "Line_out" and "line_compl_out" get enable at next tc event after kill input is inactive. In synchronous DT kill mode, STOP_EDGE should be RISING_EDGE. '0': synchronous DT kill mode: Disable This field has a function in PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0

15.1.28 TCPWM0_GRP1_CNT0_CTRL (continued)

14	PWM_TC_SYNC_KILL_DT	Specifies TC synchronour DT kill behavior: '1': TC synchronous DT kill mode: the kill event disables the "line_out" and "line_compl_out" signals at the next terminal count event and till the next terminal count event (synchronous 3 kill). If dead time is enabled, output get disables after the tc event + dead time. "Line_out" and "line_comp_out" get enable at next tc event after input input is inactive In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': TC synchronous DT kill mode: Disable This field has a function in PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
13 : 12	PWM_DISABLE_MODE	Specifies the behavior of the PWM outputs "line_out" and "line_compl_out" while the TCPWM counter is disabled (CTRL.ENABLED='0') or stopped. Note: The output signal of this selection can be further modified by the immediate kill logic and line_out polarity settings (CTRL.QUAL_ENCODING_MODE). Default Value: 0 **0x0: Z :** The behavior is the same is in previous mxtcpwm (version 1). When the counter is disabled the PWM outputs "line_out" and "line_compl_out" are NOT driven by the TCPWM. Instead the port default level configuration applies, e.g. "Z" (high impedance). Note: This is realized by driving the TCPWM output "line_out_en" to 0. When the counter is stopped upon a stop event the PWM outputs are deactivated (to the polarity defined by CTRL.KILL_LINE_POLARITY). **0x1: RETAIN :** When the counter is disabled the PWM outputs "line_out" and "line_compl_out" are driven by the TCPWM. When the counter is disabled or stopped upon a stop event the PWM outputs are retained (keep their previous levels). While the counter is disabled or stopped the PWM outputs can be changed via LINE_SEL (when parameter GRP_SMC_PRESENT = 1). **0x2: L :** When the counter is disabled the PWM outputs "line_out" and "line_compl_out" are driven by the TCPWM. When the counter is disabled or stopped upon a stop event the PWM output "line_out" is driven as a fixed '0' and the PWM output "line_compl_out" is driven as a fixed '1'. **0x3: H :** When the counter is disabled the PWM outputs "line_out" and "line_compl_out" are driven by the TCPWM. When the counter is disabled or stopped upon a stop event the PWM output "line_out" is driven as a fixed '1' and the PWM output "line_compl_out" is driven as a fixed '0'.
11	SWAP_ENABLE	Specifies whether swapping mechanism between CC0 and buffered CC0, CC1 and buffered CC1, PERIOD and buffered PERIOD, DT and buffered DT are disabled '0': swap is disable '1': swap is enable Default Value: 0

15.1.28 TCPWM0_GRP1_CNT0_CTRL (continued)

10	PWM_SYNC_KILL	Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "line_out" and "line_compl_out" signals immediately. "Line_out" and "Line_compl_out" will be enable at the next terminal count event (synchronous kill) after kill event is inactive. In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
9	PWM_STOP_ON_KILL	Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter. This field has a function in PWM and PWM_DT modes only. Default Value: 0
8	PWM_IMM_KILL	Specifies whether the kill event immediately deactivates the "line_out" and "line_compl_out" signals or with the next module clock ("active count" pre-scaled "clk_counter"). '0': synchronous kill activation. Deactivates the "line_out" and "line_compl_out" signals with the next module clock ("active count" pre-scaled "clk_counter"). '1': immediate kill activation. Immediately deactivates the "dt_line_out" and "dt_line_compl_out" signals. This field has a function in PWM and PWM_DT modes only. Default Value: 0
7	CC1_MATCH_DOWN_EN	Enables / disables the compare match 1 event generation (COUNTER equals CC0 register) when counting down (STATUS.DOWN = 1) in CNT_UPDN1/2 mode. '0': compare match 1 event generation disabled when counting down '1': compare match 1 event generation enabled when counting down This field has a function in PWM and PWM_DT modes only. Default Value: 1
6	CC1_MATCH_UP_EN	Enables / disables the compare match 1 event generation (COUNTER equals CC0 register) when counting up (STATUS.DOWN = 0) in CNT_UPDN1/2 mode. '0': compare match 1 event generation disabled when counting up '1': compare match 1 event generation enabled when counting up This field has a function in PWM and PWM_DT modes only. Default Value: 1
5	CC0_MATCH_DOWN_EN	Enables / disables the compare match 0 event generation (COUNTER equals CC0 register) when counting down (STATUS.DOWN = 1) in CNT_UPDN1/2 mode. '0': compare match 0 event generation disabled when counting down '1': compare match 0 event generation enabled when counting down This field has a function in PWM and PWM_DT modes only. Default Value: 1
4	CC0_MATCH_UP_EN	Enables / disables the compare match 0 event generation (COUNTER equals CC0 register) when counting up (STATUS.DOWN = 0) in CNT_UPDN1/2 mode. '0': compare match 0 event generation disabled when counting up '1': compare match 0 event generation enabled when counting up This field has a function in PWM and PWM_DT modes only. Default Value: 1
3	AUTO_RELOAD_LINE_SEL	Specifies switching of the LINE_SEL and LINE_BUFF_SEL values. This field has a function in PWM mode. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. Default Value: 0
2	AUTO_RELOAD_PERIOD	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff. Default Value: 0

15.1.28 TCPWM0_GRP1_CNT0_CTRL (continued)

1	AUTO_RELOAD_CC1	Specifies switching of the CC1 and buffered CC1 values. This field has a function in TIMER, PWM and PWM_DT modes. Timer modes: '0': never switch. '1': switch on a compare match 1 event. PWM and PWM_DT modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0
0	AUTO_RELOAD_CC0	Specifies switching of the CC0 and buffered CC0 values. This field has a function in TIMER, PWM and PWM_DT modes. Timer modes: '0': never switch. '1': switch on a compare match 0 event. PWM and PWM_DT modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0

15.1.29 TCPWM0_GRP1_CNT0_COUNTER

Counter count register

Address: 0x42A10008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	16-bit / 32-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

15.1.30 TCPWM0_GRP1_CNT0_CC0

Counter compare/capture 0 register

Address: 0x42A10010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. In compare mode 6 LSBs is used for HRPWM generation when HRPWM is enabled. Default Value: 65535

15.1.31 TCPWM0_GRP1_CNT0_CC0_BUFF

Counter buffered compare/capture 0 register

Address: 0x42A10014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC register. In compare mode 6 LSBs is used for HRPWM generation when HRPWM is enabled. Default Value: 65535

15.1.32 TCPWM0_GRP1_CNT0_CC1

Counter compare/capture 1 register

Address: 0x42A10018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. In compare mode 6 LSBs is used for HRPWM generation when HRPWM is enabled. Default Value: 65535

15.1.33 TCPWM0_GRP1_CNT0_CC1_BUFF

Counter buffered compare/capture 1 register

Address: 0x42A1001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC1 register. In compare mode 6 LSBs is used for HRPWM generation when HRPWM is enabled. Default Value: 65535

15.1.34 TCPWM0_GRP1_CNT0_PERIOD

Counter period register

Address: 0x42A10020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. In PWM and PWM_DT mode 6 LSBs given by are used for HRPWM generation when HRPWM is enabled. Default Value: 65535

15.1.35 TCPWM0_GRP1_CNT0_PERIOD_BUFF

Counter buffered period register

Address: 0x42A10024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Additional buffer for counter PERIOD register. In PWM and PWM_DT mode 6 LSBs given by are used for HRPWM generation when HRPWM is enabled. Note: GRP_HRPWM_WIDTH is 6 Default Value: 65535

15.1.36 TCPWM0_GRP1_CNT0_LFSR

LFSR register

Address: 0x42A10080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PLFSR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DLFSR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					R		
Name	None [23:19]					Limiter [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
18 : 16	Limiter	Limiter register. It defines the magnitude of the pseudo-random value to be added to period/CC0/CC1. PLFSR[7]/DLFSR[7] is the sign polarity Default Value: 0x07 **0x1: Limit_1 :** When Limit_1 is '1', the PLFSR[0]/DLFSR[0] is magnitude of the value to be added to period/ CC0/CC1 **0x2: Limit_2 :** When Limit_2 is '1', the PLFSR[1:0]/DLFSR[1:0] is magnitude of the value to be added to period/ CC0/CC1 **0x3: Limit_3 :** When Limit_3 is '1', the PLFSR[2:0]/DLFSR[2:0] is magnitude of the value to be added to period/ CC0/CC1 **0x4: Limit_4 :** When Limit_4 is '1', the PLFSR[3:0]/DLFSR[3:0] is magnitude of the value to be added to period/ CC0/CC1

15.1.36 TCPWM0_GRP1_CNT0_LFSR (continued)

		0x5: Limit_5 : When Limit_5 is '1', the PLFSR[4:0]/DLFSR[4:0] is magnitude of the value to be added to period/ CC0/CC1 **0x6: Limit_6 :** When Limit_6 is '1', the PLFSR[5:0]/DLFSR[5:0] is magnitude of the value to be added to period/ CC0/CC1 **0x7: Limit_7 :** When Limit_7 is '1', the PLFSR[6:0]/DLFSR[6:0] is magnitude of the value to be added to period/ CC0/CC1
15 : 8	DLFSR	DLFSR register. DLFSR defines pseudo-random value for CC0/CC1. SW need to be initialized to non 0 (seed value) before dithering is enabled MSB of DLFSR will be the sign polarity. The magnitude of the randomness to be added to CC0/ CC1 is in the range of -2^(N-1) to 2^(N-1)-1 where N is the width of the DLFSR register. Default Value: 0xFF
7 : 0	PLFSR	PLFSR register. PLFSR defines pseudo-random value for period. SW need to be initialized to non 0 (seed value) before dithering is enabled MSB of PLFSR will be the sign polarity. The magnitude of the randomness to be added to period is in the range of -2^(N-1) to 2^(N-1)-1 where N is the width of the PLFSR register Default Value: 0xFF

15.1.37 TCPWM0_TR_ALL_GF_ALL_GF0

Glitch filter register for All Group Triggers

Address: 0x42A80000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW		RW		
HW Access	None			R		R		
Name	None [7:5]			GFPS_DIV [4:3]		GF_DEPTH [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 3	GFPS_DIV	Select the glitch filter pre-scaling of the selected counter clock Default Value: 0 **0x0: GFPS_DIVBY1 :** Glitch filter pre-scaling of the selected counter clock. Divide by 1 **0x1: GFPS_DIVBY2 :** Glitch filter pre-scaling of the selected counter clock. Divide by 2 **0x2: GFPS_DIVBY4 :** Glitch filter pre-scaling of the selected counter clock. Divide by 4 **0x3: GFPS_DIVBY8 :** Glitch filter pre-scaling of the selected counter clock. Divide by 8
2 : 0	GF_DEPTH	Select the glitch filter depth Default Value: 0 **0x0: DEPTHX0 :** Glitch filter is turned off

15.1.37 TCPWM0_TR_ALL_GF_ALL_GF0 (continued)

0x1: DEPTHX1 :

Glitch filter depth is set to 1 x GFPS_DIVBYx of prescalar, where x is 1, 2, 4, 8

0x2: DEPTHX2 :

Glitch filter depth is set to 2 x GFPS_DIVBYx of prescalar, where x is 1, 2, 4, 8

0x3: DEPTHX4 :

Glitch filter depth is set to 4 x GFPS_DIVBYx of prescalar, where x is 1, 2, 4, 8

0x4: DEPTHX8 :

Glitch filter depth is set to 8 x GFPS_DIVBYx of prescalar, where x is 1, 2, 4, 8

0x5: DEPTHX16 :

Glitch filter depth is set to 16 x GFPS_DIVBYx of prescalar, where x is 1, 2, 4, 8

0x6: DEPTHX32 :

Glitch filter depth is set to 32 x GFPS_DIVBYx of prescalar, where x is 1, 2, 4, 8

0x7: DEPTHX64 :

Glitch filter depth is set to 64 x GFPS_DIVBYx of prescalar, where x is 1, 2, 4, 8

15.1.38 TCPWM0_TR_ALL_SYNC_BYPASS_TR_ALL_SYNC_BYPASS0

Trigger Sync bypass for group trigger

Address: 0x42A90000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SYNC_BYPASS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SYNC_BYPASS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SYNC_BYPASS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	SYNC_BYPASS [31:24]							

Bits	Name	Description
31 : 0	SYNC_BYPASS	When set='1', bypass the sync stage for the corresponding group trigger Default Value: 0

15.1.39 TCPWM0_MOTIF_GRP1_MOTIF0_PCONF

Global control register

Address: 0x42AA4000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW	RW	RW		RW
HW Access	R		R	R	R	R		R
Name	FTS [7:6]		MCUE	HIDG	QDCM	FSEL [2:1]		ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	CHEC [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW	RW	None			RW	None
HW Access	None	R	R	None			R	None
Name	None	MSYES	MSES	None [20:18]			SPES	None

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW	RW	None	
HW Access	R				R	R	None	
Name	LPC [31:28]				EWIL	EWIE	None [25:24]	

Bits	Name	Description
31 : 28	LPC	Low Pass Filters Configuration Default Value: 0 **0x0: LP_DISABLE :** Low pass filter disabled **0x1: LP1 :** Low pass of 1 clock cycle **0x2: LP2 :** Low pass of 2 clock cycle **0x3: LP4 :** Low pass of 4 clock cycle **0x4: LP8 :** Low pass of 8 clock cycle

15.1.39 TCPWM0_MOTIF_GRP1_MOTIF0_PCONF (continued)

0x5: LP16 :

Low pass of 16 clock cycle

0x6: LP32 :

Low pass of 32 clock cycle

0x7: LP64 :

Low pass of 64 clock cycle

0x8: LP128 :

Low pass of 128 clock cycle

0x9: LP256 :

Low pass of 256 clock cycle

0xa: LP512 :

Low pass of 512 clock cycle

0xb: LP1024 :

Low pass of 1024 clock cycle

0xc: Reserved12 :

Reserved (as disabled)

0xd: Reserved13 :

Reserved (as disabled)

0xe: Reserved14 :

Reserved (as disabled)

0xf: Reserved15 :

Reserved (as disabled)

27	EWIL	External Wrong Hall Event active level 0 - MOTIFx.EWHE signal is active HIGH 1 - MOTIFx.EWHE signal is active LOW Default Value: 0
26	EWIE	External Wrong Hall Event enable 0 - External wrong hall event emulation signal, MOTIFx.EWHE, is disabled 1 - External wrong hall event emulation signal, MOTIFx.EWHE, is enabled. Default Value: 0
22	MSYES	Multi-Channel pattern update msync trigger edge 0 - The signal used to enable a msync pattern update is active on the rising edge 1 - The signal used to enable a msync pattern update is active on the falling edge Default Value: 0

15.1.39 TCPWM0_MOTIF_GRP1_MOTIF0_PCONF (continued)

21	MSES	Multi-Channel pattern update mset trigger edge 0 - The signal used to enable a mset pattern update is active on the rising edge 1 - The signal used to enable a mset pattern update is active on the falling edge Default Value: 0
17	SPES	Edge selector for the sampling trigger This field selects which edge is used of the selected MOTIFx.HSD signal to trigger a sample of the Hall inputs. 0 - Rising edge 1 - Falling edge Default Value: 0
15 : 14	CHEC	Correct Hall Event Clear selection Default Value: 0 **0x0: WHE_OR_MP :** OR between wrong hall event and module pin (MOTIFx.EWHE) **0x1: WHE :** Wrong Hall Event **0x2: MODPIN :** Module Pin - MOTIFx.EWHE **0x3: Reserved3 :** Reserved
7 : 6	FTS	Fault Hall event Selection Default Value: 0 **0x0: WHE_OR_MP :** OR between wrong hall event and module pin (MOTIFx.EWHE) **0x1: WHE :** Wrong Hall Event **0x2: MODPIN :** Module Pin - MOTIFx.EWHE **0x3: Reserved3 :** Reserved
5	MCUE	Multi-Channel Pattern SW update enable 0 - Multi-Channel pattern update is controlled via HW 1 - Multi-Channel pattern update is controlled via SW Default Value: 0
4	HIDG	Idle generation enable Setting this field to 1 disables the generation of the IDLE signal that forces a clear on the Multi-Channel pattern and run bit. Default Value: 0

15.1.39 TCPWM0_MOTIF_GRP1_MOTIF0_PCONF (continued)

3	QDCM	Position Decoder Mode selection This field selects if the Position Decoder block is in Quadrature Mode or Direction Count Mode. In Quadrature mode, the position encoder is providing the phase signals, while in Direction Count Mode is providing a clock and a direction signal. 0 - Position encoder is in Quadrature Mode 1 - Position encoder is in Direction Count Mode. Default Value: 0
2 : 1	FSEL	Function Selector Default Value: 0 **0x0: HALLEN :** Hall Sensor Mode enabled **0x1: QUADEN :** Quadrature Decoder Mode enabled **0x2: STANDM :** stand-alone Multi-Channel Mode enabled **0x3: QDSTAN :** Quadrature Decoder and stand-alone Multi_x0002_Channel Mode enabled
0	ENABLE	MOTIF enable 0 - MOTIF disabled. 1 - MOTIF enabled. Enable MOTIF shall have the following effect: MOTIF clock is enabled,MOTIF registers are out of reset. Disable MOTIF shall have the following effect:MOTIF clock is gated, MOTIF non-retention registers get reset to default value, MOTIF retention register do not get reset, Output events get reset to default value, Interrupt output get reset to default value Modulation output get reset to default value. Default Value: 0

15.1.40 TCPWM0_MOTIF_GRP1_MOTIF0_PSUS

Suspend Configuration

Address: 0x42AA4004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					SUS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	SUS	MOTIF Mode Suspend Config This field controls the entering in suspend for the MOTIF module. Default Value: 0 **0x0: REQ_IGN :** Suspend request ignored **0x1: STOP :** Stop immediately **0x2: SUS_IDX :** In quad mode and quad with stand-alone mode, suspend in the next index occurrence (QDCM =0). In any other mode. Stop immediately. When QDCM =1, it is considered as in other mode. **0x3: SUS_PHA :** In quad mode and quad with stand-alone mode (QDCM =0), suspend in the next phase (PhaseA or PhaseB) In any other mode. Stop immediately. When QDCM =1, it is considered as in other mode.

15.1.40 TCPWM0_MOTIF_GRP1_MOTIF0_PSUS (continued)

0x4: STOP_RST :

Stop immediately. Multi-Channel pattern is set to the reset value.

0x5: SUS_SYN :

Suspend with the synchronization of the PWM signal. Multi-Channel pattern is set to the reset value at the same time of the synchronization.
In quad mode, stop immediately.

0x6: Reserved1 :

Reserved (as disabled)

0x7: Reserved2 :

Reserved (as disabled)

15.1.41 TCPWM0_MOTIF_GRP1_MOTIF0_PRUNS

MOTIF run bit set

Address: 0x42AA4008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							RW
Name	None [7:1]							SRB

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	SRB	Set Run bit 0- Stop MOTIF. Writing an 0 into this bit stop the MOTIF and bring the state machine back to idle. 1- Start MOTIF. Writing an 1 into this bit sets the run bit of the module.A rising edge triggers the start machine. When a Fault event is detected, the Hardware can clear this bit to '0' and stop MOTIF as saftey mechanisim. The SW needs to re-configure MOTIF and start again MOTIF later. if LUT mode is enabled, LUTEN=1. The hardware can clear this bit to '0' and stop MOTIF as saftey mechanism when previous pattern is detected or when pattern mismatch is detetcted. Default Value: 0

15.1.42 TCPWM0_MOTIF_GRP1_MOTIF0_PRUN

MOTIF run bit status

Address: 0x42AA4010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							RB

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	RB	Run Bit This field indicates if the module is in running or IDLE state. 0 - IDLE 1 - Running Default Value: 0

15.1.43 TCPWM0_MOTIF_GRP1_MOTIF0_HIST

Hall Inputs Sample Trigger

Address: 0x42AA4024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							W
HW Access	None							RW
Name	None [7:1]							HIS

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	HIS	Hall Inputs Sample Writting this bitfield with 1, will trigger a sample of the current hall inputs into the PDBG.HSP field. The hardware will automatically clear the HIS to 0. The sample of the hall inputs can be done even when the run bit of the module is not set. Requesting a sample when the module is running/ normal operation, may incurr in wrong behavior. Read always returns 0. Default Value: 0

15.1.44 TCPWM0_MOTIF_GRP1_MOTIF0_HMEC

Hall Mode Extra Config

Address: 0x42AA4028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						HPPE	HDBP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	HPPE	Previous Pattern Compare Enable Setting this bitfield to 1, enables the compare logic between the sampled hall input values and the previous hall pattern - HALP.HPP. This will be used together with the comparison of the current and expected pattern to generate a wrong hall event. 0 - Comparison between previous pattern and sampled pattern not used to generate a wrong hall event. 1 - Comparison between previous pattern and sampled pattern used to generate a wrong hall event. Default Value: 0
0	HDBP	Hall Sensor Debounce Stage Bypass Setting this bitfield to 1, will disable the usage of the debounce delay pins, MOTIFx.HSD. This means that after the low pass filter, the hall inputs are immediately sampled and compared against the expected and current patterns. 0 - The hall inputs are only sampled after a valid transition at the MOTIFx.HSD pin. 1 - The hall inputs are sampled after the filtering stage and the MOTIFx.HSD pin usage is disabled. Default Value: 0

15.1.45 TCPWM0_MOTIF_GRP1_MOTIF0_HALP

Hall Current and Expected patterns

Address: 0x42AA4030

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R			R		
HW Access	None		RW			RW		
Name	None [7:6]		HEP [5:3]			HCP [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None					R		
HW Access	None					RW		
Name	None [15:11]					HPP [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10 : 8	HPP	Hall Previous Pattern if LUTEN = 0, this field contains the Hall Previous pattern. This field is updated with the HALPS.HPPS values every time that a correct hall event occurs. if LUTEN = 1, this field contains the Hall Previous pattern. This field is updated with the Hall LUT value every time that a correct hall event occurs. Default Value: 0
5 : 3	HEP	Hall Expected Pattern if LUTEN = 0, this field contains the Hall Expected pattern. This field is updated with the HALPS.HEPS values every time that a correct hall event occurs. if LUTEN = 1, this field contains the Hall Expected pattern. This field is updated with the Hall LUT value every time that a correct hall event occurs. Default Value: 0
2 : 0	HCP	Hall Current Pattern if LUTEN = 0, this field contains the Hall Current pattern. This field is updated with the HALPS.HCPS value every time that a correct hall event occurs. if LUTEN = 1, this field contains the Hall Current pattern. This field is updated with the Hall LUT value every time that a correct hall event occurs. Default Value: 0

15.1.46 TCPWM0_MOTIF_GRP1_MOTIF0_HALPS

Hall Current and Expected shadow patterns

Address: 0x42AA4034

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW			RW		
HW Access	None		R			R		
Name	None [7:6]		HEPS1 [5:3]			HCPS0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					R		
Name	None [15:11]					HPPS2 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW			RW		
HW Access	None		R			R		
Name	None [23:22]		HLUT4 [21:19]			HLUT3 [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					HLUT5 [26:24]		

Bits	Name	Description
26 : 24	HLUT5	Hall LUT data position 5 if LUTEN = 0 bitfield not used if LUTEN = 1 bitfield works as LUT position 5 Default Value: 0
21 : 19	HLUT4	Hall LUT data position 4 if LUTEN = 0 bitfield not used if LUTEN = 1 bitfield works as LUT position 4 Default Value: 0
18 : 16	HLUT3	Hall LUT data position 3 if LUTEN = 0 bitfield not used if LUTEN = 1 bitfield works as LUT position 3 Default Value: 0
10 : 8	HPPS2	Shadow Hall Previous Pattern - HLUT2 if LUTEN = 0, this field contains the next Hall Previous pattern. This field is set on the HALP.HPP field every time that a correct hall event occurs. HPPS[0] - Hall Input 1 HPPS[1] - Hall Input 2 HPPS[2] - Hall Input 3 if LUTEN = 1 bitfield works as LUT position 2 Default Value: 0

15.1.46 TCPWM0_MOTIF_GRP1_MOTIF0_HALPS (continued)

5 : 3	HEPS1	Shadow Hall expected Pattern - HLUT1 if LUTEN = 0, this field contains the next Hall Expected pattern. This field is set on the HALP.HEP field every time that a correct hall event occurs. HEPS[0] - Hall Input 1 HEPS[1] - Hall Input 2 HEPS[2] - Hall Input 3 if LUTEN = 1 bitfield works as LUT position 1 Default Value: 0
2 : 0	HCPS0	Shadow Hall Current Pattern - HLUT0 if LUTEN = 0, this field contains the next Hall Current pattern value. This field is set on the HALP.HCP field every time that a correct hall event occurs. HCPS[0] - Hall Input 1 HCPS[1] - Hall Input 2 HCPS[2] - Hall Input 3 if HLUTEN = 1 bitfield works as LUT position 0 Default Value: 0

15.1.47 TCPWM0_MOTIF_GRP1_MOTIF0_HOSC

Hall Sensor Output Config

Address: 0x42AA4038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	CHN [6:4]			None	EDN [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	HSTN [14:12]			None	IDN [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	CPN [22:20]			None	SPN [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					PPN [26:24]		

Bits	Name	Description
26 : 24	PPN	Previous Pattern Match Event Output Node This field selects to which output the event signalizing that the Hall Sensor inputs match the previous pattern is forward. Same coding description as the EDN field. Default Value: 0
22 : 20	CPN	Current Pattern Match Event Output Node This field selects to which output the event signalizing that the Hall Sensor inputs match the current pattern is forward. Same coding description as the EDN field. Default Value: 0
18 : 16	SPN	Stop Counters/Pattern Mismatch Event Output Node This field selects to which output the event signalizing that the Hall Sensor inputs do not match the current, the expected or the previous pattern is forward. Same coding description as the EDN field. Default Value: 0
14 : 12	HSTN	Start Event Output Node This field selects to which output the event signalizing that the run bit was set is forward. Same coding description as the EDN field. Default Value: 0
10 : 8	IDN	Idle/Wrong Hall Event Output Node This field selects to which output the OR event between the external fault pins, MOTIFx.EWHE, and the Wrong Hall Event is forward. Same coding description as the EDN field. Default Value: 0

15.1.47 TCPWM0_MOTIF_GRP1_MOTIF0_HOSC (continued)

6 : 4	CHN	Correct Hall Event Output Node This field selects to which output the event signalizing that a correct hall event has been detected is forward. Same coding description as the EDN field. Default Value: 0
2 : 0	EDN	Edge Detection Event Output Node This field selects to which output the event signalizing that an modification on the Hall Inputs is forward. Default Value: 0 **0x0: NO_FWD :** Signal is not forward to any output **0x1: FWD0 :** Forward to MOTIFx.OUT0 **0x2: FWD1 :** Forward to MOTIFx.OUT1 **0x3: FWD2 :** Forward to MOTIFx.OUT2 **0x4: FWD3 :** Forward to MOTIFx.OUT3 **0x5: FWD4 :** Forward to MOTIFx.OUT4 **0x6: FWD5 :** Forward to MOTIFx.OUT5 **0x7: FWD6 :** Forward to MOTIFx.OUT6

15.1.48 TCPWM0_MOTIF_GRP1_MOTIF0_MCM

Multi-Channel Mode Pattern

Address: 0x42AA4040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	MCMP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	MCMP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	MCMP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	MCMP [31:24]							

Bits	Name	Description
31 : 0	MCMP	Multi-Channel Pattern This field contains the Multi-Channel Pattern that is going to be applied to the Multi-Channel outputs, MOTIFx.MOUT[31:0]. if MLUTEN=0, this field is updated with the value of the MCSM.MCMPS every time that a Multi-Channel pattern update is triggered. if MLUTEN=1, this bitfield is updated with the value select in MLUT0,1,2,3,4,5. These values get transferred to MOTIFx.MOUT[31:0] Default Value: 0xAAAAAAAA

15.1.49 TCPWM0_MOTIF_GRP1_MOTIF0_MCSM

Multi-Channel Mode shadow Pattern LUT0

Address: 0x42AA4044

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MCMPS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MCMPS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MCMPS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	MCMPS [31:24]							

Bits	Name	Description
31 : 0	MCMPS	Shadow Multi-Channel Pattern if MLUTEN=0, This field contains the next Multi-Channel Pattern. Every time that a Multi-Channel pattern transfer is triggered, this value is passed into the field MCM.MCMP. if MLUTEN=1, This field contains the Multi-Channel Pattern stored in Look-up table position 0. If Multi-Channel pattern transfer is triggered and MLUT0 is selected, this value is passed into field MCM.MCMP[31:0] Default Value: 0

15.1.50 TCPWM0_MOTIF_GRP1_MOTIF0_MCMS

Multi-Channel Mode Control set

Address: 0x42AA4048

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					W	W	W
HW Access	None					RW	RW	RW
Name	None [7:3]					STMR	STHR	MNPS

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	STMR	Multi-Channel Shadow Transfer Request Writing a 1 into this field leads to an immediate update of the field MCM.MCMP. A read always returns 0. Default Value: 0
1	STHR	Hall Pattern Shadow Transfer Request Writing a 1 into this field leads to an immediate update of the fields HALP.HCP, HALP.HEP and HALP.HPP. A read always returns 0. Default Value: 0
0	MNPS	Multi-Channel Pattern Update Enable Set Writing a 1 into this field enables the Multi-Channel pattern update (sets the MCMF.MSS bit). The update is not done immediately due to the fact that the trigger that synchronizes the update with the PWM is still needed. A read always returns 0. Default Value: 0

15.1.51 TCPWM0_MOTIF_GRP1_MOTIF0_MCMC

Multi-Channel Mode Control clear

Address: 0x42AA404C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						W	W
HW Access	None						RW	RW
Name	None [7:2]						MPC	MNPC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	MPC	Multi-Channel Pattern clear Writing a 1 into this field clears the Multi-Channel Pattern value with the content of the MCPF register. A read always returns 0. Default Value: 0
0	MNPC	Multi-Channel Pattern Update Enable Clear Writing a 1 into this field clears the MCMF.MSS bit. A read always returns 0. Default Value: 0

15.1.52 TCPWM0_MOTIF_GRP1_MOTIF0_MCMF

Multi-Channel Mode flag status

Address: 0x42AA4050

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							MSS

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	MSS	Multi-Channel Pattern update status This field indicates if the Multi-Channel pattern is ready to be updated or not. When this field is set, the Multi-Channel pattern is updated when the triggering signal, selected from the MOTIFx.MSYNC, becomes active. 0 - Update of the Multi-Channel pattern is set 1 - Update of the Multi-Channel pattern is not set Default Value: 0

15.1.53 TCPWM0_MOTIF_GRP1_MOTIF0_MCPF

Multi-Channel Pattern Fault

Address: 0x42AA4054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MCFV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MCFV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MCFV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	MCFV [31:24]							

Bits	Name	Description
31 : 0	MCFV	Multi-Channel Fault Value This register contains the value that is going to be loaded into the Multi-Channel patter, MCP register, and fed consequently to the outputs, MOTIFx.MOUT[31:0]. This value is loaded into the MCP register whenever a fault is detected (via a wrong hall event or one of the MOTIFx.EWHEy pins) or whenever the software requests a pattern clear via the MCMC.MPC bitfield. Default Value: 0

15.1.54 TCPWM0_MOTIF_GRP1_MOTIF0_MOSC

Multi-Channel Output Config

Address: 0x42AA4058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	SHN [6:4]			None	PUN [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					R		
Name	None [15:11]					MSTN [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10 : 8	MSTN	Start Event Output Node This field selects to which output the event signalizing that the run bit was set is forward. Same coding description as the PUN field. Default Value: 0
6 : 4	SHN	Update Sync Event Output Node This field selects to which output, the event that is used to synchronize the Multi-Channel Pattern update has happened after MSYNC edge detected, is forward. Same coding description as the PUN field. Default Value: 0
2 : 0	PUN	Pattern Update Event Output Node This field selects to which output, the event signalizing that a Multi-Channel pattern update is enabled (MSS is set), is forward. Default Value: 0 **0x0: NO_FWD :** Signal is not forward to any output **0x1: FWD0 :** Forward to MOTIFx.OUT0 **0x2: FWD1 :** Forward to MOTIFx.OUT1

15.1.54 TCPWM0_MOTIF_GRP1_MOTIF0_MOSC (continued)

0x3: FWD2 :

Forward to MOTIFx.OUT2

0x4: FWD3 :

Forward to MOTIFx.OUT3

0x5: FWD4 :

Forward to MOTIFx.OUT4

0x6: FWD5 :

Forward to MOTIFx.OUT5

0x7: FWD6 :

Forward to MOTIFx.OUT6

15.1.55 TCPWM0_MOTIF_GRP1_MOTIF0_QDC

Quadrature Decoder Configuration

Address: 0x42AA4060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW	RW	RW	RW
HW Access	None		R		R	R	R	R
Name	None [7:6]		ICM [5:4]		INDS	PHS	PBLS	PALS

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		None			R
HW Access	R		R		None			RW
Name	PBEM [15:14]		PAEM [13:12]		None [11:9]			DVAL

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None		RW	
HW Access	None		R		None		R	
Name	None [23:22]		PBDS [21:20]		None [19:18]		PACS [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						IDS [25:24]	

Bits	Name	Description
25 : 24	IDS	Index Selector Selects which signal is used as Index signal if in Quadrature Decoder Mode: Default Value: 0 **0x0: DISABLE :** Disabled **0x1: POSI0 :** POSI0 **0x2: POSI1 :** POSI1 **0x3: POSI2 :** POSI2
21 : 20	PBDS	Phase B or Direction Selector Selects which signal is used as Phase B signal if in Quadrature Decoder Mode or as Direction if in Direction Count Mode: Default Value: 0

15.1.55 TCPWM0_MOTIF_GRP1_MOTIF0_QDC (continued)

0x0: DISABLE :

Disabled

0x1: POSI0 :

POSI0

0x2: POSI1 :

POSI1

0x3: POSI2 :

POSI2

17 : 16 PACS

Phase A or Clock Selector
Selects which signal is used as Phase A signal if in Quadrature Decoder Mode or as Clock if in Direction Count Mode:
Default Value: 0

0x0: DISABLE :

Disabled

0x1: POSI0 :

POSI0

0x2: POSI1 :

POSI1

0x3: POSI2 :

POSI2

15 : 14 PBEM

Phase B Edge Mode
Note: Selecting BOTH in one PHASE, implies that other PHASE should not be RISE/FALL. Selecting NONE in one PHASE, implies that other PHASE should not be NONE. Invalid combination can lead to unexpected behavior
Default Value: 0

0x0: BOTH :

clock is decoded on rising and falling edges of the Phase B signal

0x1: RISE :

clock is decoded on rising edge of the Phase B signal

0x2: FALL :

clock is decoded on falling edge of the Phase B signal

0x3: NONE :

Clock is not decoded for PHASE B

15.1.55 TCPWM0_MOTIF_GRP1_MOTIF0_QDC (continued)

13 : 12	PAEM	Phase A Edge Mode Note: Selecting BOTH in one PHASE, implies that other PHASE should not be RISE/FALL. Selecting NONE in one PHASE, implies that other PHASE should not be NONE. Invalid combination can lead to unexpected behavior Default Value: 0 **0x0: BOTH :** clock is decoded on rising and falling edges of the Phase A signal **0x1: RISE :** clock is decoded on rising edge of the Phase A signal **0x2: FALL :** clock is decoded on falling edge of the Phase A signal **0x3: NONE :** Clock is not decoded for PHASE A
8	DVAL	Current rotation direction 0 - Counterclockwise rotation 1 - Clockwise rotation Default Value: 0
5 : 4	ICM	Index Marker generations control This field controls the generation of the index marker that is linked PRGINDX event. Default Value: 0 **0x0: NO_IDX :** No index marker generation **0x1: 1ST_IDX :** Only first index occurrence generated **0x2: ALL_IDX :** All index occurrences generated **0x3: Reserved3 :** Reserved
3	INDS	Index Signal Level selector 0 - Index signal is active HIGH 1 - Index signal is active LOW Default Value: 0
2	PHS	Phase signals swap 0 - Phase A is the leading signal for clockwise rotation 1 - Phase B is the leading signal for clockwise rotation Default Value: 0
1	PBLS	Phase B Level selector 0 - Phase B is active HIGH 1 - Phase B is active LOW Default Value: 0

15.1.55 TCPWM0_MOTIF_GRP1_MOTIF0_QDC (continued)

0	PALS	Phase A Level selector 0 - Phase A is active HIGH 1 - Phase A is active LOW Default Value: 0

15.1.56 TCPWM0_MOTIF_GRP1_MOTIF0_QOSC

Quadrature Output Config

Address: 0x42AA4064

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	DON [6:4]			None	QCN [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	CCN [14:12]			None	PCN [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	QSTN [22:20]			None	IXN [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
22 : 20	QSTN	Start Event Output Node This field selects to which output the event signalizing that the run bit was set is forward. Same coding description as the QCN field. Default Value: 0
18 : 16	IXN	Index Event Output Node This field selects to which output the event signalizing that an index/zero marker was detected, is forward. This event is only generated when the index input has been detected and the rotation direction did not change (between two index occurrences). internal indx Same coding description as the QCN field. Default Value: 0
14 : 12	CCN	Clear/Capture Event Output Node This field selects to which output the event signalizing that an index/zero marker was detected, is forward. This can be used as a capture or clear function for a timer, to measure time between index events. internal prgindx Same coding description as the QCN field. Default Value: 0
10 : 8	PCN	Period Clock Event Output Node This field selects to which output, the period clock (PCLK) event, is forward. Same coding description as the QCN field. Default Value: 0
6 : 4	DON	Direction Event Output Node This field selects to which output, the direction signal (QDIR), is forward. Same coding description as the QCN field. Default Value: 0

15.1.56 TCPWM0_MOTIF_GRP1_MOTIF0_QOSC (continued)

2 : 0	QCN	Quadrature Clock Event Output Node This field selects to which output, the quadrature clock (QCLK) event, is forward. Default Value: 0 **0x0: NO_FWD :** Signal is not forward to any output **0x1: FWD0 :** Forward to MOTIFx.OUT0 **0x2: FWD1 :** Forward to MOTIFx.OUT1 **0x3: FWD2 :** Forward to MOTIFx.OUT2 **0x4: FWD3 :** Forward to MOTIFx.OUT3 **0x5: FWD4 :** Forward to MOTIFx.OUT4 **0x6: FWD5 :** Forward to MOTIFx.OUT5 **0x7: FWD6 :** Forward to MOTIFx.OUT6

15.1.57 TCPWM0_MOTIF_GRP1_MOTIF0_MCMEC

Multi-Channel Extra Config

Address: 0x42AA4068

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [7:5]			MFCE	None [3:2]		MEBP	MSBP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	MFCE	Multi-Channel Fault Clear Enable Setting this bitfield to 1 will enable a clear of the Multi-Channel pattern, whenever a Hall Fault Event is detected. The Multi-Channel pattern will be cleared with the value programmed in the MCFV field. 0 - Multi-Channel pattern clear with Hall Fault Event disabled. 1 - Multi-Channel pattern clear with Hall Fault Event enabled. Default Value: 0
1	MEBP	Multi-Channel Pattern Enable Delay Bypass Setting this bitfield to 1 will bypass the delay between a Correct Hall Event and the enable of the Multi-Channel Patter update. 0 - Enable of the Multi-Channel Pattern update is only done after the external SET signal is detected - MOTIFx.MSET. 1 - Enable of the Multi-Channel Pattern update is done immediately after a Correct Hall Event is detected - only valid when PCONF.MCUE is 0. Default Value: 0
0	MSBP	Multi-Channel Mode Sync Bypass Setting this bitfield to 1 will dictate that whenever the MCMF.MSS bitfield is 1, a pattern update will occur immediately (without waiting for the sync signal - MOTIFx.MSYNC). 0 - Update of the Multi-Channel pattern is only done after the sync signal is detected - MOTIFx.MSYNC. 1 - Update of the Multi-Channel pattern is done immediately after the MCMF.MSS field is set. Default Value: 0

15.1.58 TCPWM0_MOTIF_GRP1_MOTIF0_PFLG

MOTIF interrupt status

Address: 0x42AA4070

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	None	R	R	R
HW Access	None			RW	None	RW	RW	RW
Name	None [7:5]			MSTS	None	HIES	WHES	CHES

Bits	15	14	13	12	11	10	9	8
SW Access	None	R	R	R	R	R	R	R
HW Access	None	RW	RW	RW	RW	RW	RW	RW
Name	None	PPES	CPES	PCLKS	DIRS	CNTS	ERRS	INDXS

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14	PPES	Previous Pattern Match Status 0 - Equality between Sampled Hall input values and Previous Pattern value not detected. 1 - Equality between Sampled Hall input values and Previous Pattern value detected. Default Value: 0
13	CPES	Current Pattern Match Status 0 - Equality between Sampled Hall input values and Current Pattern value not detected. 1 - Equality between Sampled Hall input values and Current Pattern value detected. Default Value: 0
12	PCLKS	Quadrature Period Clk Status 0 - Period clock not generated 1 - Period clock generated Default Value: 0
11	DIRS	Quadrature Direction Change 0 - Change on direction not detected 1 - Change on direction detected Default Value: 0
10	CNTS	Quadrature CLK Status 0 - Quadrature clock not generated 1 - Quadrature clock generated Default Value: 0
9	ERRS	Quadrature Phase Error Status 0 - Phase Error event not detected 1 - Phase Error event detected Default Value: 0

15.1.58 TCPWM0_MOTIF_GRP1_MOTIF0_PFLG (continued)

8	INDXS	Quadrature Index Status 0 - Index event not detected 1 - Index event detected Default Value: 0
4	MSTS	Multi-Channel pattern shadow transfer status 0 - Shadow transfer not done 1 - Shadow transfer done Default Value: 0
2	HIES	Hall Inputs Update Status 0 - Transition on the Hall Inputs not detected 1 - Transition on the Hall Inputs detected Default Value: 0
1	WHES	Wrong Hall Event Status 0 - Wrong Hall Event not detected 1 - Wrong Hall Event detected Default Value: 0
0	CHES	Correct Hall Event Status 0 - Correct Hall Event not detected 1 - Correct Hall Event detected Default Value: 0

15.1.59 TCPWM0_MOTIF_GRP1_MOTIF0_PFLGE

MOTIF interrupt enable

Address: 0x42AA4074

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	RW
HW Access	None			R	None	R	R	R
Name	None [7:5]			EMST	None	EHIE	EWHE	ECHE

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW	RW	RW	RW	RW	RW	RW
HW Access	None	R	R	R	R	R	R	R
Name	None	EPPE	ECPE	EPCLK	EDIR	ECNT	EERR	EINDX

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	None	RW	RW	RW
HW Access	None			R	None	R	R	R
Name	None [23:21]			MSTSEL	None	HIESEL	WHESEL	CHESEL

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW	RW	RW	RW	RW	RW	RW
HW Access	None	R	R	R	R	R	R	R
Name	None	PPSEL	CPSEL	PCLSEL	DIRSEL	CNTSEL	ERRSEL	INDSEL

Bits	Name	Description
30	PPSEL	Previous Pattern Match Event Service Request Selector 0 - Previous Pattern Match Event interrupt forward to MOTIFx.SR0 1 - Previous Pattern Match Event interrupt forward to MOTIFx.SR1 Default Value: 0
29	CPSEL	Current Pattern Match Event Service Request Selector 0 - Current Pattern Match Event interrupt forward to MOTIFx.SR0 1 - Current Pattern Match Event interrupt forward to MOTIFx.SR1 Default Value: 0
28	PCLSEL	Quadrature Period clock Event Service Request Selector 0 - Quadrature Period clock Event interrupt forward to MOTIFx.SR0 1 - Quadrature Period clock Event interrupt forward to MOTIFx.SR1 Default Value: 0
27	DIRSEL	Quadrature Direction Update Event Service Request Selector 0 - Quadrature Direction Update Event interrupt forward to MOTIFx.SR0 1 - Quadrature Direction Update Event interrupt forward to MOTIFx.SR1 Default Value: 0
26	CNTSEL	Quadrature Clock Event Service Request Selector 0 - Quadrature Clock Event interrupt forward to MOTIFx.SR0 1 - Quadrature Clock Event interrupt forward to MOTIFx.SR1 Default Value: 0
25	ERRSEL	Quadrature Phase Error Event Service Request Selector 0 - Quadrature Phase error Event interrupt forward to MOTIFx.SR0 1 - Quadrature Phase error Event interrupt forward to MOTIFx.SR1 Default Value: 0

15.1.59 TCPWM0_MOTIF_GRP1_MOTIF0_PFLGE (continued)

24	INDSEL	Quadrature Index Event Service Request Selector 0 - Quadrature Index Event interrupt forward to MOTIFx.SR0 1 - Quadrature Index Event interrupt forward to MOTIFx.SR1 Default Value: 0
20	MSTSEL	Multi-Channel pattern Update Event Service Request Selector 0 - Multi-Channel pattern Update Event interrupt forward to MOTIFx.SR0 1 - Multi-Channel pattern Update Event interrupt forward to MOTIFx.SR1 Default Value: 0
18	HIESEL	Hall Inputs Update Event Service Request Selector 0 - Hall Inputs Update Event interrupt forward to MOTIFx.SR0 1 - Hall Inputs Update Event interrupt forward to MOTIFx.SR1 Default Value: 0
17	WHESEL	Wrong Hall Event Service Request Selector 0 - Wrong Hall Event interrupt forward to MOTIFx.SR0 1 - Wrong Hall Event interrupt forward to MOTIFx.SR1 Default Value: 0
16	CHESEL	Correct Hall Event Service Request Selector 0 - Correct Hall Event interrupt forward to MOTIFx.SR0 1 - Correct Hall Event interrupt forward to MOTIFx.SR1 Default Value: 0
14	EPPE	Previous Pattern Match interrupt Enable 0 - Previous Pattern Match event interrupt disabled 1 - Previous Pattern Match event interrupt enabled Default Value: 0
13	ECPE	Current Pattern Match interrupt Enable 0 - Current Pattern Match event interrupt disabled 1 - Current Pattern Match event interrupt enabled Default Value: 0
12	EPCLK	Quadrature Period CLK interrupt Enable 0 - Quadrature Period CLK event interrupt disabled 1 - Quadrature Period CLK event interrupt enabled Default Value: 0
11	EDIR	Quadrature direction change interrupt Enable 0 - Direction change event interrupt disabled 1 - Direction change event interrupt enabled Default Value: 0
10	ECNT	Quadrature CLK interrupt Enable 0 - Quadrature CLK event interrupt disabled 1 - Quadrature CLK event interrupt enabled Default Value: 0
9	EERR	Quadrature Phase Error Enable 0 - Phase error event interrupt disabled 1 - Phase error event interrupt enabled Default Value: 0
8	EINDX	Quadrature Index Event Enable 0 - Index event interrupt disabled 1 - Index event interrupt enabled Default Value: 0
4	EMST	Multi-Channel pattern shadow transfer enable 0 - Shadow transfer event interrupt disabled 1 - Shadow transfer event interrupt enabled Default Value: 0
2	EHIE	Hall Input Update Enable 0 - Update of the Hall Inputs interrupt is disabled 1 - Update of the Hall Inputs interrupt is enabled Default Value: 0

15.1.59 TCPWM0_MOTIF_GRP1_MOTIF0_PFLGE (continued)

1	EWHE	Wrong Hall Event Enable 0 - Wrong Hall Event interrupt disabled 1 - Wrong Hall Event interrupt enabled Default Value: 0
0	ECHE	Correct Hall Event Enable 0 - Correct Hall Event interrupt disabled 1 - Correct Hall Event interrupt enabled Default Value: 0

15.1.60 TCPWM0_MOTIF_GRP1_MOTIF0_SPFLG

Interrupt set register

Address: 0x42AA4078

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			W	None	W	W	W
HW Access	None			RW	None	RW	RW	RW
Name	None [7:5]			SMST	None	SHIE	SWHE	SCHE

Bits	15	14	13	12	11	10	9	8
SW Access	None	W	W	W	W	W	W	W
HW Access	None	RW	RW	RW	RW	RW	RW	RW
Name	None	SPP	SCP	SPCLK	SDIR	SCNT	SERR	SINDX

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14	SPP	Previous Pattern Match flag set Writing a 1B to this field sets the PFLG.PPES bit field. An interrupt pulse is generated. A read always returns 0. Default Value: 0
13	SCP	Current Pattern Match flag set Writing a 1 to this field sets the PFLG.CPES bit field. An interrupt pulse is generated. A read always returns 0. Default Value: 0
12	SPCLK	Quadrature period clock flag set Writing a 1 to this field sets the PFLG.PCLKS bit field. An interrupt pulse is generated. A read always returns 0. Default Value: 0
11	SDIR	Quadrature Direction flag set Writing a 1 to this field sets the PFLG.DIRS bit field. An interrupt pulse is generated. A read always returns 0. Default Value: 0
10	SCNT	Quadrature CLK flag set Writing a 1 to this field sets the PFLG.CNTS bit field. An interrupt pulse is generated. A read always returns 0. Default Value: 0
9	SERR	Quadrature Phase Error flag set Writing a 1 to this field sets the PFLG.ERRS bit field. An interrupt pulse is generated. A read always returns 0. Default Value: 0

15.1.60 TCPWM0_MOTIF_GRP1_MOTIF0_SPFLG (continued)

8	SINDX	Quadrature Index flag set Writing a 1 to this field sets the PFLG.INDXS bit field. An interrupt pulse is generated. A read always returns 0. Default Value: 0
4	SMST	Multi-Channel Pattern shadow transfer flag set Writing a 1 to this field sets the PFLG.MSTS bit field. An interrupt pulse is generated. A read always returns 0. Default Value: 0
2	SHIE	Hall Inputs Update Event flag set Writing a 1 to this field sets the PFLG.HIES bit field. An interrupt pulse is generated. A read always returns 0. Default Value: 0
1	SWHE	Wrong Hall Event flag set Writing a 1 to this field sets the PFLG.WHES bit field. An interrupt pulse is generated. A read always returns 0. Default Value: 0
0	SCHE	Correct Hall Event flag set Writing a 1 to this field sets the PFLG.CHES bit field. An interrupt pulse is generated. A read always returns 0. Default Value: 0

15.1.61 TCPWM0_MOTIF_GRP1_MOTIF0_RPFLG

Interrupt clear register

Address: 0x42AA407C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			W	None	W	W	W
HW Access	None			RW	None	RW	RW	RW
Name	None [7:5]			RMST	None	RHIE	RWHE	RCHE

Bits	15	14	13	12	11	10	9	8
SW Access	None	W	W	W	W	W	W	W
HW Access	None	RW	RW	RW	RW	RW	RW	RW
Name	None	RPP	RCP	RPCLK	RDIR	RCNT	RERR	RINDX

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14	RPP	Previous Pattern Match flag clear Writing a 1 to this field clears the PFLG.PPES bit field. A read always returns 0. Default Value: 0
13	RCP	Current Pattern Match flag clear Writing a 1 to this field clears the PFLG.CPES bit field. A read always returns 0. Default Value: 0
12	RPCLK	Quadrature period clock flag clear Writing a 1 to this field clears the PFLG.PCLKS bit field. A read always returns 0. Default Value: 0
11	RDIR	Quadrature Direction flag clear Writing a 1 to this field clears the PFLG.DIRS bit field. A read always returns 0. Default Value: 0
10	RCNT	Quadrature CLK flag clear Writing a 1 to this field clears the PFLG.CNTS bit field. A read always returns 0. Default Value: 0
9	RERR	Quadrature Phase Error flag clear Writing a 1 to this field clears the PFLG.ERRS bit field. A read always returns 0. Default Value: 0

15.1.61 TCPWM0_MOTIF_GRP1_MOTIF0_RPFLG (continued)

8	RINDX	Quadrature Index flag clear Writing a 1 to this field clears the PFLG.INDXS bit field. A read always returns 0. Default Value: 0
4	RMST	Multi-Channel Pattern shadow transfer flag clear Writing a 1 to this field clears the PFLG.MSTS bit field. A read always returns 0. Default Value: 0
2	RHIE	Hall Inputs Update Event flag clear Writing a 1 to this field clears the PFLG.HIES bit field. A read always returns 0. Default Value: 0
1	RWHE	Wrong Hall Event flag clear Writing a 1 to this field clears the PFLG.WHES bit field. A read always returns 0. Default Value: 0
0	RCHE	Correct Hall Event flag clear Writing a 1 to this field clears the PFLG.CHES bit field. A read always returns 0. Default Value: 0

15.1.62 TCPWM0_MOTIF_GRP1_MOTIF0_MCSM1

Multi-Channel Mode shadow pattern LUT1

Address: 0x42AA4080

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MLUT1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MLUT1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MLUT1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	MLUT1 [31:24]							

Bits	Name	Description
31 : 0	MLUT1	Multi-Channel LUT 1 if MLUTEN=0 this bitfield is not used if MLUTEN=1 this field contains the Multi-Channel Pattern stored in Look-up table position 1. If Multi-Channel pattern transfer is triggered and MLUT1 is selected, this value is passed into the field MCM.MCMP[31:0] Default Value: 0

15.1.63 TCPWM0_MOTIF_GRP1_MOTIF0_MCSM2

Multi-Channel Mode shadow pattern LUT2

Address: 0x42AA4084

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MLUT2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MLUT2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MLUT2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	MLUT2 [31:24]							

Bits	Name	Description
31 : 0	MLUT2	Multi-Channel LUT 2 if MLUTEN=0 this bitfield is not used if MLUTEN=1 this field contains the Multi-Channel Pattern stored in Look-up table position 2. If Multi-Channel pattern transfer is triggered and MLUT2 is selected, this value is passed into the field MCM.MCMP[31:0] Default Value: 0

15.1.64 TCPWM0_MOTIF_GRP1_MOTIF0_MCSM3

Multi-Channel Mode shadow pattern LUT3

Address: 0x42AA4088

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MLUT3 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MLUT3 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MLUT3 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	MLUT3 [31:24]							

Bits	Name	Description
31 : 0	MLUT3	Multi-Channel LUT 3 if MLUTEN=0 this bitfield is not used if MLUTEN=1 this field contains the Multi-Channel Pattern stored in Look-up table position 3. If Multi-Channel pattern transfer is triggered and MLUT3 is selected, this value is passed into the field MCM.MCMP[31:0] Default Value: 0

15.1.65 TCPWM0_MOTIF_GRP1_MOTIF0_MCSM4

Multi-Channel Mode shadow pattern LUT4

Address: 0x42AA408C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MLUT4 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MLUT4 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MLUT4 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	MLUT4 [31:24]							

Bits	Name	Description
31 : 0	MLUT4	Multi-Channel LUT 4 if MLUTEN=0 this bitfield is not used if MLUTEN=1 this field contains the Multi-Channel Pattern stored in Look-up table position 4. If Multi-Channel pattern transfer is triggered and MLUT4 is selected, this value is passed into the field MCM.MCMP[31:0] Default Value: 0

15.1.66 TCPWM0_MOTIF_GRP1_MOTIF0_MCSM5

Multi-Channel Mode shadow pattern LUT5

Address: 0x42AA4090

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MLUT5 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MLUT5 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MLUT5 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	MLUT5 [31:24]							

Bits	Name	Description
31 : 0	MLUT5	Multi-Channel LUT 5 if MLUTEN=0 this bitfield is not used if MLUTEN=1 this field contains the Multi-Channel Pattern stored in Look-up table position 5. If Multi-Channel pattern transfer is triggered and MLUT5 is selected, this value is passed into the field MCM.MCMP[31:0] Default Value: 0

15.1.67 TCPWM0_MOTIF_GRP1_MOTIF0_CLUT

Hall Mode LUT config

Address: 0x42AA4094

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							LUTEN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	LUTEN	HALL LUT enable Setting this bitfield to 1, will enable the usage of the Hall Look-up table. 0 - Hall LUT disabled, HCPS, HEPS, HPPS are used. HLUT3, HLUT4,HLUT5 not used. 1 - Hall LUT enabled, HCPS, HEPS, HPPS, HLUT3, HLUT4,HLUT5 works as data container for the LUT. Every time that a correct hall event occurs the LUT provides new values to HALP register Default Value: 0

15.1.68 TCPWM0_MOTIF_GRP1_MOTIF0_SLUT

Hall Mode LUT status

Address: 0x42AA4098

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R		
HW Access	None					RW		
Name	None [7:3]					PTR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	PTR	HALL LUT Pointer status This field contains the pointer address to HALL LUT current pattern. LUTEN must be set, if LUTEN is 0, this bitfield is always 0. Valid values are 0,1,2,3,4,5. Invalid values 6,7 Default Value: 0

15.1.69 TCPWM0_MOTIF_GRP1_MOTIF0_PDBG

MOTIF Debug Register

Address: 0x42AA4100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R	R			R		
HW Access	None	RW	RW			RW		
Name	None	IVAL	QPSV [5:3]			QCSV [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None	R	R	R	None	R		
HW Access	None	RW	RW	RW	None	RW		
Name	None	LPF2V	LPF1V	LPF0V	None	HSP [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14	LPF2V	Low Pass filter 2 valid state 0 - Low pass filter has not output valid data 1 - Low pass filter has output valid data Default Value: 0
13	LPF1V	Low Pass filter 1 valid state 0 - Low pass filter has not output valid data 1 - Low pass filter has output valid data Default Value: 0
12	LPF0V	Low Pass filter 0 valid state 0 - Low pass filter has not output valid data 1 - Low pass filter has output valid data Default Value: 0
10 : 8	HSP	Hall Current Sampled Pattern HSP[0] - Hall Input 1 HSP[1] - Hall Input 2 HSP[2] - Hall Input 3 Default Value: 0
6	IVAL	Current Index Value Default Value: 0

15.1.69 TCPWM0_MOTIF_GRP1_MOTIF0_PDBG (continued)

5 : 3	QPSV	Quadrature Decoder Previous state This field stores the previous state of the quadrature decoder state machine. The ready indicates that the state machine has processed the first values present at the MOTIF inputs (this may not be immediate due to the propgation time of the low pass filters - if enabled). QPSV[0] - Phase B QPSV[1] - Phase A QPSV[2] - ready Default Value: 0
2 : 0	QCSV	Quadrature Decoder Current state This field stores the current state of the quadrature decoder state machine. The ready indicates that the state machine has processed the first values present at the MOTIF inputs (this may not be immediate due to the propgation time of the low pass filters - if enabled). QCSV[0] - Phase B QCSV[1] - Phase A QCSV[2] - ready Default Value: 0

15.1.70 TCPWM0_MOTIF_GRP1_MOTIF0_PLP0S

MOTIF Low Pass 0 Status

Address: 0x42AA4104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	LPP0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						RW	
Name	None [15:10]						LPP0 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	LPP0	Actual count of the Low Pass Filter Default Value: 0

15.1.71 TCPWM0_MOTIF_GRP1_MOTIF0_PLP1S

MOTIF Low Pass 1 Status

Address: 0x42AA4108

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	LPP1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						RW	
Name	None [15:10]						LPP1 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	LPP1	Actual count of the Low Pass Filter Default Value: 0

15.1.72 TCPWM0_MOTIF_GRP1_MOTIF0_PLP2S

MOTIF Low Pass 2 Status

Address: 0x42AA410C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	LPP2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						RW	
Name	None [15:10]						LPP2 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	LPP2	Actual count of the Low Pass Filter Default Value: 0

16 Serial Communication Block (SCB) registers

This section discusses the SCB registers. It lists all the registers in mapping tables, in address order.

16.1 Register details

Register	Address	Description
SCB0_CTRL	0x42820000	Generic control
SCB0_STATUS	0x42820004	Generic status
SCB0_CMD_RESP_CTRL	0x42820008	Command/response control
SCB0_CMD_RESP_STATUS	0x4282000C	Command/response status
SCB0_SPI_CTRL	0x42820020	SPI control
SCB0_SPI_STATUS	0x42820024	SPI status
SCB0_SPI_TX_CTRL	0x42820028	SPI transmitter control
SCB0_SPI_RX_CTRL	0x4282002C	SPI receiver control
SCB0_UART_CTRL	0x42820040	UART control
SCB0_UART_TX_CTRL	0x42820044	UART transmitter control
SCB0_UART_RX_CTRL	0x42820048	UART receiver control
SCB0_UART_RX_STATUS	0x4282004C	UART receiver status
SCB0_UART_FLOW_CTRL	0x42820050	UART flow control
SCB0_I2C_CTRL	0x42820060	I2C control
SCB0_I2C_STATUS	0x42820064	I2C status
SCB0_I2C_M_CMD	0x42820068	I2C master command
SCB0_I2C_S_CMD	0x4282006C	I2C slave command
SCB0_I2C_CFG	0x42820070	I2C configuration
SCB0_I2C_STRETCH_CTRL	0x42820074	I2C stretch control
SCB0_I2C_STRETCH_STATUS	0x42820078	I2C stretch status
SCB0_TX_CTRL	0x42820200	Transmitter control
SCB0_TX_FIFO_CTRL	0x42820204	Transmitter FIFO control
SCB0_TX_FIFO_STATUS	0x42820208	Transmitter FIFO status
SCB0_TX_FIFO_WR	0x42820240	Transmitter FIFO write
SCB0_RX_CTRL	0x42820300	Receiver control
SCB0_RX_FIFO_CTRL	0x42820304	Receiver FIFO control
SCB0_RX_FIFO_STATUS	0x42820308	Receiver FIFO status
SCB0_RX_MATCH	0x42820310	Slave address and mask
SCB0_RX_FIFO_RD	0x42820340	Receiver FIFO read
SCB0_RX_FIFO_RD_SILENT	0x42820344	Receiver FIFO read silent

Serial Communication Block (SCB) registers

Register	Address	Description
SCB0_EZ_DATA0	0x42820400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB0_EZ_DATA0 to SCB0_EZ_DATA255).
SCB0_INTR_CAUSE	0x42820E00	Active clocked interrupt signal
SCB0_INTR_I2C_EC	0x42820E80	Externally clocked I2C interrupt request
SCB0_INTR_I2C_EC_MASK	0x42820E88	Externally clocked I2C interrupt mask
SCB0_INTR_I2C_EC_MASKED	0x42820E8C	Externally clocked I2C interrupt masked
SCB0_INTR_SPI_EC	0x42820EC0	Externally clocked SPI interrupt request
SCB0_INTR_SPI_EC_MASK	0x42820EC8	Externally clocked SPI interrupt mask
SCB0_INTR_SPI_EC_MASKED	0x42820ECC	Externally clocked SPI interrupt masked
SCB0_INTR_M	0x42820F00	Master interrupt request
SCB0_INTR_M_SET	0x42820F04	Master interrupt set request
SCB0_INTR_M_MASK	0x42820F08	Master interrupt mask
SCB0_INTR_M_MASKED	0x42820F0C	Master interrupt masked request
SCB0_INTR_S	0x42820F40	Slave interrupt request
SCB0_INTR_S_SET	0x42820F44	Slave interrupt set request
SCB0_INTR_S_MASK	0x42820F48	Slave interrupt mask
SCB0_INTR_S_MASKED	0x42820F4C	Slave interrupt masked request
SCB0_INTR_TX	0x42820F80	Transmitter interrupt request
SCB0_INTR_TX_SET	0x42820F84	Transmitter interrupt set request
SCB0_INTR_TX_MASK	0x42820F88	Transmitter interrupt mask
SCB0_INTR_TX_MASKED	0x42820F8C	Transmitter interrupt masked request
SCB0_INTR_RX	0x42820FC0	Receiver interrupt request
SCB0_INTR_RX_SET	0x42820FC4	Receiver interrupt set request
SCB0_INTR_RX_MASK	0x42820FC8	Receiver interrupt mask
SCB0_INTR_RX_MASKED	0x42820FCC	Receiver interrupt masked request
SCB5_CTRL	0x42C00000	Generic control. See SCB0_CTRL for the details of bit fields.
SCB5_STATUS	0x42C00004	Generic status. See SCB0_STATUS for the details of bit fields.
SCB5_CMD_RESP_CTRL	0x42C00008	Command/response control. See SCB0_CMD_RESP_CTRL for the details of bit fields.
SCB5_CMD_RESP_STATUS	0x42C0000C	Command/response status. See SCB0_CMD_RESP_STATUS for the details of bit fields.
SCB5_SPI_CTRL	0x42C00020	SPI control. See SCB0_SPI_CTRL for the details of bit fields.

Serial Communication Block (SCB) registers

Register	Address	Description
SCB5_SPI_STATUS	0x42C00024	SPI status. See SCB0_SPI_STATUS for the details of bit fields.
SCB5_SPI_TX_CTRL	0x42C00028	SPI transmitter control. See SCB0_SPI_TX_CTRL for the details of bit fields.
SCB5_SPI_RX_CTRL	0x42C0002C	SPI receiver control. See SCB0_SPI_RX_CTRL for the details of bit fields.
SCB5_UART_CTRL	0x42C00040	UART control. See SCB0_UART_CTRL for the details of bit fields.
SCB5_UART_TX_CTRL	0x42C00044	UART transmitter control. See SCB0_UART_TX_CTRL for the details of bit fields.
SCB5_UART_RX_CTRL	0x42C00048	UART receiver control. See SCB0_UART_RX_CTRL for the details of bit fields.
SCB5_UART_RX_STATUS	0x42C0004C	UART receiver status. See SCB0_UART_RX_STATUS for the details of bit fields.
SCB5_UART_FLOW_CTRL	0x42C00050	UART flow control. See SCB0_UART_FLOW_CTRL for the details of bit fields.
SCB5_I2C_CTRL	0x42C00060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB5_I2C_STATUS	0x42C00064	I2C status. See SCB0_I2C_STATUS for the details of bit fields.
SCB5_I2C_M_CMD	0x42C00068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB5_I2C_S_CMD	0x42C0006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB5_I2C_CFG	0x42C00070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB5_I2C_STRETCH_CTRL	0x42C00074	I2C stretch control. See SCB0_I2C_STRETCH_CTRL for the details of bit fields.
SCB5_I2C_STRETCH_STATUS	0x42C00078	I2C stretch status. See SCB0_I2C_STRETCH_STATUS for the details of bit fields.
SCB5_TX_CTRL	0x42C00200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB5_TX_FIFO_CTRL	0x42C00204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB5_TX_FIFO_STATUS	0x42C00208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB5_TX_FIFO_WR	0x42C00240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.

Serial Communication Block (SCB) registers

Register	Address	Description
SCB5_RX_CTRL	0x42C00300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB5_RX_FIFO_CTRL	0x42C00304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB5_RX_FIFO_STATUS	0x42C00308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB5_RX_MATCH	0x42C00310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB5_RX_FIFO_RD	0x42C00340	Receiver FIFO read. See SCB0_RX_FIFO_RD for the details of bit fields.
SCB5_RX_FIFO_RD_SILENT	0x42C00344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB5_EZ_DATA0	0x42C00400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB5_EZ_DATA0 to SCB5_EZ_DATA255). See SCB0_EZ_DATA0 for the details of bit fields.
SCB5_INTR_CAUSE	0x42C00E00	Active clocked interrupt signal. See SCB0_INTR_CAUSE for the details of bit fields.
SCB5_INTR_I2C_EC	0x42C00E80	Externally clocked I2C interrupt request. See SCB0_INTR_I2C_EC for the details of bit fields.
SCB5_INTR_I2C_EC_MASK	0x42C00E88	Externally clocked I2C interrupt mask. See SCB0_INTR_I2C_EC_MASK for the details of bit fields.
SCB5_INTR_I2C_EC_MASKED	0x42C00E8C	Externally clocked I2C interrupt masked. See SCB0_INTR_I2C_EC_MASKED for the details of bit fields.
SCB5_INTR_SPI_EC	0x42C00EC0	Externally clocked SPI interrupt request. See SCB0_INTR_SPI_EC for the details of bit fields.
SCB5_INTR_SPI_EC_MASK	0x42C00EC8	Externally clocked SPI interrupt mask. See SCB0_INTR_SPI_EC_MASK for the details of bit fields.
SCB5_INTR_SPI_EC_MASKED	0x42C00ECC	Externally clocked SPI interrupt masked. See SCB0_INTR_SPI_EC_MASKED for the details of bit fields.
SCB5_INTR_M	0x42C00F00	Master interrupt request. See SCB0_INTR_M for the details of bit fields.
SCB5_INTR_M_SET	0x42C00F04	Master interrupt set request. See SCB0_INTR_M_SET for the details of bit fields.
SCB5_INTR_M_MASK	0x42C00F08	Master interrupt mask. See SCB0_INTR_M_MASK for the details of bit fields.
SCB5_INTR_M_MASKED	0x42C00F0C	Master interrupt masked request. See SCB0_INTR_M_MASKED for the details of bit fields.

Serial Communication Block (SCB) registers

Register	Address	Description
SCB5_INTR_S	0x42C00F40	Slave interrupt request. See SCB0_INTR_S for the details of bit fields.
SCB5_INTR_S_SET	0x42C00F44	Slave interrupt set request. See SCB0_INTR_S_SET for the details of bit fields.
SCB5_INTR_S_MASK	0x42C00F48	Slave interrupt mask. See SCB0_INTR_S_MASK for the details of bit fields.
SCB5_INTR_S_MASKED	0x42C00F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKED for the details of bit fields.
SCB5_INTR_TX	0x42C00F80	Transmitter interrupt request. See SCB0_INTR_TX for the details of bit fields.
SCB5_INTR_TX_SET	0x42C00F84	Transmitter interrupt set request. See SCB0_INTR_TX_SET for the details of bit fields.
SCB5_INTR_TX_MASK	0x42C00F88	Transmitter interrupt mask. See SCB0_INTR_TX_MASK for the details of bit fields.
SCB5_INTR_TX_MASKED	0x42C00F8C	Transmitter interrupt masked request. See SCB0_INTR_TX_MASKED for the details of bit fields.
SCB5_INTR_RX	0x42C00FC0	Receiver interrupt request. See SCB0_INTR_RX for the details of bit fields.
SCB5_INTR_RX_SET	0x42C00FC4	Receiver interrupt set request. See SCB0_INTR_RX_SET for the details of bit fields.
SCB5_INTR_RX_MASK	0x42C00FC8	Receiver interrupt mask. See SCB0_INTR_RX_MASK for the details of bit fields.
SCB5_INTR_RX_MASKED	0x42C00FCC	Receiver interrupt masked request. See SCB0_INTR_RX_MASKED for the details of bit fields.

16.1.1 SCB0_CTRL

Generic control

Address: 0x42820000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None	RW	None	RW	RW	RW
HW Access	R		None	R	None	R	R	R
Name	MEM_WIDTH [15:14]		None	CMD_RESP_MODE	None	EZ_MODE	EC_OP_MODE	EC_AM_MODE

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						BLOCK	ADDR_ACCEPT

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None		RW	None		RW	
HW Access	R	None		R	None		R	
Name	ENABLED	None [30:29]		EC_ACCESS	None [27:26]		MODE [25:24]	

Bits	Name	Description
31	ENABLED	SCB block is enabled ('1') or not ('0'). The proper order in which to initialize SCB is as follows: - Program protocol specific information using SPI_CTRL, UART_CTRL (and UART_TX_CTRL and UART_RX_CTRL) or I2C_CTRL registers. This includes selection of a submode, master/slave functionality and transmitter/receiver functionality when applicable. - Program generic transmitter (TX_CTRL) and receiver (RX_CTRL) information. This includes enabling of the transmitter and receiver functionality. - Program transmitter FIFO (TX_FIFO_CTRL) and receiver FIFO (RX_FIFO_CTRL) information. - Program CTRL register to enable SCB, select the specific operation mode and oversampling factor. Generally when this block is enabled, no control information should be changed. Changes should be made AFTER disabling this block, e.g. to modify the operation mode (from I2C to SPI) or to go from externally to internally clocked. The change takes effect after the block is re-enabled. Note that disabling the block will cause re-initialization of the design and associated state is lost (e.g. FIFO content). Specific to SPI master case, when SCB is idle, below registers can be changed without disabling SCB block, TX_CTRL TX_FIFO_CTRL RX_CTRL RX_FIFO_CTRL SPI_CTRL.SSEL, Default Value: 0

16.1.1 SCB0_CTRL (continued)

28	EC_ACCESS	EC_ACCESS is used to enable I2CS_EC or SPIS_EC access to internal EZ memory. 1: enable clk_scb 0: disable clk_scb Before going to deepsleep this field should be set to 1. when waking up from DeepSleep power mode, and PLL is locked (clk_scb is at expected frequency), this filed should be set to 0. Default Value: 0
25 : 24	MODE	Mode of operation (3: Reserved) Default Value: 3 **0x0: I2C :** Inter-Integrated Circuits (I2C) mode. **0x1: SPI :** Serial Peripheral Interface (SPI) mode. **0x2: UART :** Universal Asynchronous Receiver/Transmitter (UART) mode.
17	BLOCK	Only used in externally clocked mode. If the externally clocked logic and the internal CPU accesses to EZ memory coincide/collide, this bit determines whether the CPU access should block and result in bus wait states ('BLOCK is 1') or not (BLOCK is '0'). IF BLOCK is '0' and the accesses collide, CPU read operations return 0xffff:ffff and CPU write operations are ignored. Colliding accesses are registered as interrupt causes: INTR_TX.BLOCKED and INTR_RX.BLOCKED. Default Value: 0
16	ADDR_ACCEPT	Determines whether a received matching address is accepted in the RX FIFO ('1') or not ('0'). In I2C mode, this field is used to allow the slave to put the received slave address or general call address in the RX FIFO. Note that a received matching address is put in the RX FIFO when this bit is '1' for both I2C read and write transfers. In multi-processor UART receiver mode, this field is used to allow the receiver to put the received address in the RX FIFO. Note: non-matching addresses are never put in the RX FIFO. Default Value: 0
15 : 14	MEM_WIDTH	Determines the number of bits per FIFO data element, depending on physical SRAM cell data width. On M0S8/MXS40S platform, the SRAM data width is 16 bit, so WORD (2) is not supported. On MXS40E platform, the SRAM data width is 32 bits. Default Value: 1 **0x0: BYTE :** 8-bit FIFO data elements. This mode provides the biggest amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 7]. **0x1: HALFWORD :** 16-bit FIFO data elements. TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 15]. **0x2: WORD :** 32-bit FIFO data elements. This mode provides the smallest amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH can be in a range of [0, 31].

16.1.1 SCB0_CTRL (continued)

		0x3: Reserved : This setting is reserved. Do not use.
12	CMD_RESP_MODE	Determines CMD_RESP mode of operation: '0': CMD_RESP mode disabled. '1': CMD_RESP mode enabled (also requires EC_AM_MODE and EC_OP_MODE to be set to '1'). Default Value: 0
10	EZ_MODE	Non EZ mode ('0') or EZ mode ('1'). In EZ mode, a meta protocol is applied to the serial interface protocol. This meta protocol adds meaning to the data frames transferred by the serial interface protocol: a data frame can represent a memory address, a write memory data element or a read memory data element. EZ mode is only used for synchronous serial interface protocols: SPI and I2C. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported and the transmitter should use continuous data frames; i.e. data frames not separated by slave deselection. This mode is only applicable to slave functionality. In EZ mode, the slave can read from and write to an addressable memory structure of 32 bytes. In EZ mode, data frames should 8-bit in size and should be transmitted and received with the Most Significant Bit (MSB) first. In UART mode this field should be '0'. Default Value: 0
9	EC_OP_MODE	This field specifies the clocking for the SCB block '0': Internally clocked mode '1': externally clocked mode In internally clocked mode, the serial interface protocols run off the SCB clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked operation mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode AND EZ mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. The maximum SPI slave, EZ mode bitrate is 48 Mbps (transmission and IO delays outside the IP will degrade the effective bitrate). In UART mode this field should be '0'. Default Value: 0
8	EC_AM_MODE	This field specifies the clocking for the address matching (I2C) or slave selection detection logic (SPI) '0': Internally clocked mode '1': Externally clocked mode In internally clocked mode, the serial interface protocols run off the SCB clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. The clocking for the rest of the logic is determined by CTRL.EC_OP_MODE. Externally clocked mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. In UART mode this field should be '0'. Default Value: 0

16.1.1 SCB0_CTRL (continued)

3 : 0	OVS	Serial interface bit period oversampling factor expressed in SCB clock cycles. Used for SPI and UART functionality. OVS + 1 SCB clock cycles constitute a single serial interface clock/bit cycle. This field is NOT used in externally clocked mode. If OVS is odd, the oversampling factor is even and the low and high phase of the interface clock period are the same. If OVS is even, the oversampling factor is odd and the low and high phase can differ by 1 SCB clock period. In SPI master mode, the valid range is [3, 15]. At an SCB frequency of 48 MHz, the maximum SPI bit rate is 12 Mbps, assuming ideal (0 ns) IO cell and routing (chip and board) delay. The calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. The effective system bit rate is dependent on the external SPI slave that we communicate with. If the SPI output clock to SPI MISO input round trip delay is significant (multiple SPI output clock cycles), it may be necessary to increase OVS and/or to set SPI_CTRL.LATE_MISO_SAMPLE to '1' to achieve the maximum possible system bit rate. In SPI slave mode, the OVS field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the SPI input clock (IF) on the interface to guarantee functional correct behavior. This requirement is expressed as a ratio: SCB clock/IF clock. The ratio is dependent on the setting of RX_CTRL.MEDIAN and the external SPI master's capability to support "late MISO sample" functionality (similar to our SPI master functionality represented by SPI_CTRL.LATE_MISO_SAMPLE): - MEDIAN is '0' and external SPI master has NO "late MISO sample functionality": SCB clock/IF clock >= 6. At a SCB frequency of 48 MHz, the maximum bit rate is 8 Mbps. - MEDIAN is '0' and external SPI master has "late MISO sample functionality": SCB clock/IF clock >= 3. At a SCB frequency of 48 MHz, the maximum bit rate is 16 Mbps. - MEDIAN is '1' and external SPI master has NO "late MISO sample functionality": SCB clock/IF clock >= 8. At a SCB frequency of 48 MHz, the maximum bit rate is 6 Mbps. - MEDIAN is '1' and external SPI master has "late MISO sample functionality": SCB clock/IF clock >= 4. At a SCB frequency of 48 MHz, the maximum bit rate is 12 Mbps. As discussed earlier, the calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. In UART standard submode (including LIN), the valid range is [7, 15]. In UART SmartCard submode, the valid range is [7, 15]. In UART TX IrDA submode this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. Only normal transmission mode is supported, the pulse is roughly 3/16 of the bit period (for all bit rates). There is only one valid OVS value: - 0: 16 times oversampling. SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. SCB clock frequency of 16*57.6 KHz for 57.6 Kbps. SCB clock frequency of 16*38.4 KHz for 38.4 Kbps. SCB clock frequency of 16*19.2 KHz for 19.2 Kbps. SCB clock frequency of 16*9.6 KHz for 9.6 Kbps. SCB clock frequency of 16*2.4 KHz for 2.4 Kbps. SCB clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. In UART RX IrDA submode (1.2, 2.4, 9.6, 19.2, 38.4, 57.6 and 115.2 Kbps) this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. In normal transmission mode, this pulse is roughly 3/16 of the bit period (for all bit rates). In low power transmission mode, this pulse is potentially smaller (down to 1.62 us typical and 1.41 us minimal) than 3/16 of the bit period (for < 115.2 Kbps bitrates). Pulse widths greater or equal than two SCB clock cycles are guaranteed to be detected by the receiver. Pulse widths less than two SCB clock cycles and greater or equal than one SCB clock cycle may be detected by the receiver. Pulse widths less than one SCB clock cycle will not be detected by the receiver. RX_CTRL.MEDIAN should be set to '1' for IrDA receiver functionality. The SCB clock (as provided by the programmable clock block) and the oversampling together determine the IrDA bitrate. Normal mode, OVS field values (with the required SCB clock frequency): - 0: 16 times oversampling. SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. SCB clock frequency of 16*57.6 KHz for 57.6 Kbps. SCB clock frequency of 16*38.4 KHz for 38.4 Kbps. SCB clock frequency of 16*19.2 KHz for 19.2 Kbps. SCB clock frequency of 16*9.6 KHz for 9.6 Kbps. SCB clock frequency of 16*2.4 KHz for 2.4 Kbps. SCB clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. Low power mode, OVS field values (with the required SCB clock frequency): - 0: 16 times oversampling. SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. - 1: 32 times oversampling. SCB clock frequency of 32*57.6 KHz for 57.6 Kbps. - 2: 48 times oversampling. SCB clock frequency of 48*38.4 KHz for 38.4 Kbps. - 3: 96 times oversampling. SCB clock frequency of 96*19.2 KHz for 19.2 Kbps. - 4: 192 times oversampling. SCB clock frequency of 192*9.6 KHz for 9.6 Kbps. - 5: 768 times oversampling. SCB clock frequency of 768*2.4 KHz for 2.4 Kbps. - 6: 1536 times oversampling. SCB clock frequency of 1536*1.2 KHz for 1.2 Kbps. - all other values are not used in low power mode. Default Value: 15

16.1.2 SCB0_STATUS

Generic status

Address: 0x42820004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							EC_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	EC_BUSY	Indicates whether the externally clocked logic is potentially accessing the EZ memory (this is only possible in EZ mode). This bit can be used by SW to determine whether it is safe to issue a SW access to the EZ memory (without bus wait states (a blocked SW access) or bus errors being generated). Note that the INTR_TX.BLOCKED and INTR_RX.BLOCKED interrupt causes are used to indicate whether a SW access was actually blocked by externally clocked logic. Default Value: Undefined

16.1.3 SCB0_CMD_RESP_CTRL

Command/response control

Address: 0x42820008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BASE_RD_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	BASE_WR_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_WR_ADDR	I2C/SPI write base address for CMD_RESP mode. At the start of a write transfer this BASE_WR_ADDR is copied to CMD_RESP_STATUS.CURR_WR_ADDR. This field should not be modified during ongoing bus transfers. Default Value: 0
7 : 0	BASE_RD_ADDR	I2C/SPI read base address for CMD_RESP mode. At the start of a read transfer this BASE_RD_ADDR is copied to CMD_RESP_STATUS.CURR_RD_ADDR. This field should not be modified during ongoing bus transfers. Default Value: 0

16.1.4 SCB0_CMD_RESP_STATUS

Command/response status

Address: 0x4282000C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CURR_RD_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	CURR_WR_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	W	W	None					
Name	CMD_RESP_EC_BUSY	CMD_RESP_EC_BUS_BUSY	None [29:24]					

Bits	Name	Description
31	CMD_RESP_EC_BUSY	Indicates whether the CURR_RD_ADDR and CURR_WR_ADDR fields in this register are reliable (when CMD_RESP_EC_BUSY is '0') or not reliable (when CMD_RESP_EC_BUSY is '1'). Note: - When there is no ongoing bus transfer, CMD_RESP_EC_BUSY is '0' (reliable). - When there is a ongoing bus transfer, CMD_RESP_EC_BUSY is '0' (reliable), when the CURR_RD_ADDR and CURR_WR_ADDR are not being updated by the HW. - When there is a ongoing bus transfer, CMD_RESP_EC_BUSY is '1' (not reliable), when the CURR_RD_ADDR or CURR_WR_ADDR are being updated by the HW. Note that this update lasts one I2C clock cycle, or two SPI clock cycles. Default Value: Undefined
30	CMD_RESP_EC_BUS_BUSY	Indicates whether there is an ongoing bus transfer to the IP. '0': no ongoing bus transfer. '1': ongoing bus transfer. For SPI, the field is '1' when slave mode is selected. For I2C, the field is set to '1' at a I2C START/RESTART. In case of an address match, the field is set to '0' on a I2C STOP. In case of NO address match, the field is set to '0' after the failing address match. Default Value: Undefined

16.1.4 SCB0_CMD_RESP_STATUS (continued)

23 : 16	CURR_WR_ADDR	I2C/SPI write current address for CMD_RESP mode. HW increments the field after a write access to the memory buffer. However, when the last memory buffer address is reached, the address is NOT incremented (but remains at the maximum memory buffer address). The field is used to determine how many bytes have been written (# bytes = CURR_WR_ADDR - CMD_RESP_CTRL.BASE_WR_ADDR). This field is reliable when there is no bus transfer. This field is potentially unreliable when there is a ongoing bus transfer, i.e. when CMD_RESP_EC_BUSY is '0', the field is reliable. Default Value: Undefined
7 : 0	CURR_RD_ADDR	I2C/SPI read current address for CMD_RESP mode. HW increments the field after a read access to the memory buffer. However, when the last memory buffer address is reached, the address is NOT incremented (but remains at the maximum memory buffer address). The field is used to determine how many bytes have been read (# bytes = CURR_RD_ADDR - CMD_RESP_CTRL.BASE_RD_ADDR). This field is reliable when there is no bus transfer. This field is potentially unreliable when there is a ongoing bus transfer, i.e. when CMD_RESP_EC_BUSY is '0', the field is reliable. Default Value: Undefined

16.1.5 SCB0_SPI_CTRL

SPI control

Address: 0x42820020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		SCLK_-CONTINU-OUS	LATE_SAM-PLE	CPOL	CPHA	SE-LECT_PRE-CEDE	SSEL_-CONTINU-OUS

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW	RW	RW	RW	RW	RW	RW
HW Access	None	R	R	R	R	R	R	R
Name	None	SSEL_INTER_-FRAME_DEL	SSEL_HOLD_DEL	SSEL_SET-UP_DEL	SSEL_PO-LARITY3	SSEL_PO-LARITY2	SSEL_PO-LARITY1	SSEL_PO-LARITY0

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None			RW		RW	
HW Access	R	None			R		R	
Name	MASTER_-MODE	None [30:28]			SSEL [27:26]		MODE [25:24]	

Bits	Name	Description
31	MASTER_MODE	Master ('1') or slave ('0') mode. In master mode, transmission will commence on availability of data frames in the TX FIFO. In slave mode, when selected and there is no data frame in the TX FIFO, the slave will transmit all '1's. In both master and slave modes, received data frames will be lost if the RX FIFO is full. Default Value: 0
27 : 26	SSEL	Selects one of the four incoming/outgoing SPI slave select signals: - 0: Slave 0, SSEL[0]. - 1: Slave 1, SSEL[1]. - 2: Slave 2, SSEL[2]. - 3: Slave 3, SSEL[3]. SCB block should be disabled when changes are made to this field. Default Value: 0
25 : 24	MODE	Submode of SPI operation (3: Reserved). Default Value: 3

16.1.5 SCB0_SPI_CTRL (continued)

		0x0: SPI_MOTOROLA : SPI Motorola submode. In master mode, when not transmitting data (Slave SELECT is inactive), SCLK is stable at CPOL. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive. **0x1: SPI_TI :** SPI Texas Instruments submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive; i.e. no pulse is generated. **0x2: SPI_NS :** SPI National Semiconductors submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive.
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only used in master mode. Not used in National Semiconductors submode. '0': No local loopback '1': the SPI master MISO line is connected to the SPI master MOSI line. In other words, in loop-back mode the SPI master receives on MISO what it transmits on MOSI. Default Value: 0
14	SSEL_INTER_-FRAME_DEL	Indicates the SPI SELECT inter-dataframe delay (between SELECT deactivation and SELECT activation). '0': 1.5 SPI clock cycles '1': 2.5 SPI clock cycles Only applies in SPI MOTOROLA submode and when SPI_CTRL.SSEL_CONTINUOUS=0, CTRL.OVS>=3. above are ideal case at SCB block level, and there is inaccuracy of one clk_scb cycle. Default Value: 0
13	SSEL_HOLD_DEL	Indicates the SPI SELECT hold delay (between SPI clock edge to sample the last MOSI bit, and SELECT deactivation). '0': 0.75 SPI clock cycles '1': 1.75 SPI clock cycles Only applies in SPI MOTOROLA submode and when SCLK_CONTINUOUS=0, CTRL.OVS>=3. above are ideal case at SCB block level, and there is inaccuracy of one clk_scb cycle. Default Value: 0
12	SSEL_SETUP_DEL	Indicates the SPI SELECT setup delay (between SELECT activation and SCLK clock edge to sample the first MOSI bit). '0': 0.75 SPI clock cycles '1': 1.75 SPI clock cycles Only applies in SPI MOTOROLA submode and when SCLK_CONTINUOUS=0, CTRL.OVS>=3. above are ideal case at SCB block level, and there is inaccuracy of one clk_scb cycle. Default Value: 0
11	SSEL_POLARITY3	Slave select polarity. Default Value: 0
10	SSEL_POLARITY2	Slave select polarity. Default Value: 0
9	SSEL_POLARITY1	Slave select polarity. Default Value: 0

16.1.5 SCB0_SPI_CTRL (continued)

8	SSEL_POLARITY0	Slave select polarity. SSEL_POLARITY0 applies to the outgoing SPI slave select signal 0 (master mode) and to the incoming SPI slave select signal (slave mode). For Motorola and National Semiconductors submodes: '0': slave select is low/'0' active. '1': slave select is high/'1' active. For Texas Instruments submode: '0': high/'1' active precede/coincide pulse. '1': low/'0' active precede/coincide pulse. Default Value: 0
5	SCLK_CONTINUOUS	Only applicable in master mode. '0': SCLK is generated, when the SPI master is enabled and data is transmitted. '1': SCLK is generated, when the SPI master is enabled. This mode is useful for slave devices that use SCLK for functional operation other than just SPI functionality. Default Value: 0
4	LATE_SAMPLE	Changes the SCLK edge on which MISO is captured in master mode, or MOSI is captured in slave mode. When '0', the default applies, for Motorola as determined by CPOL and CPHA, for Texas Instruments on the falling edge of SCLK(CPOL is '0' and CPHA is '1'), for National Semiconductors on the rising edge of SCLK(CPOL is '0' and CPHA is '0'). When '1', the alternate clock edge is used (which comes half a SPI SCLK period later). for master, applicable to all Motorola, TI and National Semiconductors flavors, and CPOL/CPHA timing mdoes. for slave, applicable to Motorola flavor only, and CPHA=0 timing modes only, and internally-clocked mode only. Late sampling addresses the round trip delay associated with transmitting SCLK from the master to the slave and transmitting MISO from the slave to the master. Default Value: 1
3	CPOL	Indicates the clock polarity. This field, together with the CPHA field, indicates when MOSI data is driven and MISO data is captured: - CPOL is '0': SCLK is '0' when not transmitting data. - CPOL is '1': SCLK is '1' when not transmitting data. Default Value: 0
2	CPHA	Indicates the clock phase. This field, together with the CPOL field, indicates when MOSI data is driven and MISO data is captured: - Motorola mode 0. CPOL is '0', CPHA is '0': MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. - Motorola mode 1. CPOL is '0', CPHA is '1': MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 2. CPOL is '1', CPHA is '0': MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 3. CPOL is '1', CPHA is '1': MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. In SPI Motorola submode, all four CPOL/CPHA modes are valid. in SPI NS submode, only CPOL=0 CPHA=0 mode is valid. in SPI TI submode, only CPOL=0 CPHA=1 mode is valid. Default Value: 0
1	SELECT_PRECEDE	Only used in SPI Texas Instruments' submode. When '1', the data frame start indication is a pulse on the Slave SELECT line that precedes the transfer of the first data frame bit. When '0', the data frame start indication is a pulse on the Slave SELECT line that coincides with the transfer of the first data frame bit. Default Value: 0

16.1.5 SCB0_SPI_CTRL (continued)

0	SSEL_CONTINUOUS	Continuous SPI data transfers enabled ('1') or not ('0'). This field is used in master mode. In slave mode, both continuous and non-continuous SPI data transfers are supported independent of this field. When continuous transfers are enabled individual data frame transfers are not necessarily separated by slave deselection (as indicated by the level or pulse on the SELECT line): if the TX FIFO has multiple data frames, data frames are send out without slave deselection. When continuous transfers are not enabled individual data frame transfers are always separated by slave deselection: independent of the availability of TX FIFO data frames, data frames are sent out with slave deselection. Default Value: 0

16.1.6 SCB0_SPI_STATUS

SPI status

Address: 0x42820024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						SPI_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	SPI base EZ address. Address as provided by a SPI write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	SPI current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when SPI_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
1	SPI_EC_BUSY	Indicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	SPI bus is busy. The bus is considered busy ('1') during an ongoing transaction. For Motorola and National submodes, the busy bit is '1', when the slave selection is activated. For TI submode, the busy bit is '1' from the time the preceding/coinciding slave select is activated for the first transmitted data frame, till the last MOSI/MISO bit of the last data frame is transmitted. Default Value: Undefined

16.1.7 SCB0_SPI_TX_CTRL

SPI transmitter control

Address: 0x42820028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	None			
HW Access	None		R	R	None			
Name	None [7:6]		PARITY_ENABLED	PARITY	None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							MOSI_IDLE_HIGH

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	MOSI_IDLE_HIGH	SPI master MOSI output level when SELECT output inactive, 0: retain the level of last data bit 1: change to high, (MOSI level is high, before the first data bit time, and after data bit time, defined SSEL/SCLK driving edge with CPOL/CPHA) Default Value: 0
5	PARITY_ENABLED	Parity generation enabled ('1') or not ('0'). Default Value: 0
4	PARITY	Parity bit. When '0', the transmitter generates an even parity. When '1', the transmitter generates an odd parity. Default Value: 0

16.1.8 SCB0_SPI_RX_CTRL

SPI receiver control

Address: 0x4282002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	None			
HW Access	None		R	R	None			
Name	None [7:6]		PARITY_ENABLED	PARITY	None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							DROP_ON_PARITY_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	DROP_ON_PARITY_ERROR	Behavior when a parity check fails. When '0', received data is send to the RX FIFO. When '1', received data is dropped and lost. Default Value: 0
5	PARITY_ENABLED	Parity checking enabled ('1') or not ('0'). Default Value: 0
4	PARITY	Parity bit. When '0', the receiver expects an even parity. When '1', the receiver expects an odd parity. Default Value: 0

16.1.9 SCB0_UART_CTRL

UART control

Address: 0x42820040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						MODE [25:24]	

Bits	Name	Description
25 : 24	MODE	Submode of UART operation (3: Reserved) Default Value: 3 **0x0: UART_STD :** Standard UART submode. **0x1: UART_SMARTCARD :** SmartCard (ISO7816) submode. Support for negative acknowledgement (NACK) on the receiver side and retransmission on the transmitter side. **0x2: UART_IRDA :** Infrared Data Association (IrDA) submode. Return to Zero modulation scheme. In this mode, the oversampling factor should be 16, that is OVS should be set to 15.
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). 0: Loopback is not enabled 1: UART_TX is connected to UART_RX. UART_RTS is connected to UART_CTS. This allows a SCB UART transmitter to communicate with its receiver counterpart. Default Value: 0

16.1.10 SCB0_UART_TX_CTRL

UART transmitter control

Address: 0x42820044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	None	RW		
HW Access	None		R	R	None	R		
Name	None [7:6]		PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RETRY_ON_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	RETRY_ON_NACK	When '1', a data frame is retransmitted when a negative acknowledgement is received. Only applicable to the SmartCard submode. Default Value: 0
5	PARITY_ENABLED	Parity generation enabled ('1') or not ('0'). Only applicable in standard UART submodes. In SmartCard submode, parity generation is always enabled through hardware. In IrDA submode, parity generation is always disabled through hardware Default Value: 0
4	PARITY	Parity bit. When '0', the transmitter generates an even parity. When '1', the transmitter generates an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0
2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. Default Value: 2

16.1.11 SCB0_UART_RX_CTRL

UART receiver control

Address: 0x42820048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW		
HW Access	None	R	R	R	None	R		
Name	None	POLARITY	PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW	RW	RW	None	RW	RW	RW
HW Access	None	R	R	R	None	R	R	R
Name	None	HDRXEN	SKIP_START	LIN_MODE	None	MP_MODE	DROP_ON_FRAME_ERROR	DROP_ON_PARITY_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				BREAK_WIDTH [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							BREAK_LEVEL

Bits	Name	Description
24	BREAK_LEVEL	0: low level pulse detection, like Break field in LIN protocol 1: high level pulse detection, like IFS field in CXPI protocol, or idle line state in UART Default Value: 0
19 : 16	BREAK_WIDTH	Break width. BREAK_WIDTH + 1 is the minimum width in bit periods of a break. During a break the transmitted/received line value is '0'. This feature is useful for standard UART submode and LIN submode ("break field" detection). Once, the break is detected, the INTR_RX.BREAK_DETECT bit is set to '1'. Note that break detection precedes baud rate detection, which is used to synchronize/refine the receiver clock to the transmitter clock. As a result, break detection operates with an unsynchronized/unrefined receiver clock. Therefore, the receiver's definition of a bit period is imprecise and the setting of this field should take this imprecision into account. The LIN standard also accounts for this imprecision: a LIN start bit followed by 8 data bits allows for up to 9 consecutive '0' bit periods during regular transmission, whereas the LIN break detection should be at least 13 consecutive '0' bit periods. This provides for a margin of 4 bit periods. Therefore, the default value of this field is set to 10, representing a minimal break field with of 10+1 = 11 bit periods; a value in between the 9 consecutive bit periods of a regular transmission and the 13 consecutive bit periods of a break field. This provides for slight imprecisions of the receiver clock wrt. the transmitter clock. There should not be a need to program this field to any value other than its default value. Default Value: 10

16.1.11 SCB0_UART_RX_CTRL (continued)

14	HDRXEN	Only applicable in standard UART submode. When '0' the transmission and receiving pad are separated and full-duplex communication is enabled. When '1', the receiver is connected to the input path of the transmission pad. Therefore only half-duplex communication is enabled. The arbitration between sending and receiving device needs to be done on a higher protocol level. During transmission, reception is not possible. All features of standard UART submode are supported - except parallel communication. Default Value: 0
13	SKIP_START	Only applicable in standard UART submode. When '1', the receiver skips start bit detection for the first received data frame. Instead, it synchronizes on the first received data frame bit, which should be a '1'. This functionality is intended for wake up from DeepSleep when receiving a data frame. The transition from idle ('1') to START ('0') on the RX line is used to wake up the CPU. The transition detection (and the associated wake up functionality) is performed by the GPIO2 IP. The woken up CPU will enable the SCB's UART receiver functionality. Once enabled, it is assumed that the START bit is ongoing (the CPU wakeup and SCB enable time should be less than the START bit period). The SCB will synchronize to a '0' to '1' transition, which indicates the first data frame bit is received (first data frame bit should be '1'). After synchronization to the first data frame bit, the SCB will resume normal UART functionality: subsequent data frames will be synchronized on the receipt of a START bit. Default Value: 0
12	LIN_MODE	Only applicable in standard UART submode. When '1', the receiver performs break detection and baud rate detection on the incoming data. First, break detection counts the amount of bit periods that have a line value of '0'. BREAK_WIDTH specifies the minimum required amount of bit periods. Successful break detection sets the INTR_RX.BREAK_DETECT interrupt cause to '1'. Second, baud rate detection counts the amount of peripheral clock periods that are use to receive the synchronization byte (0x55; least significant bit first). The count is available through UART_RX_STATUS.BR_COUNTER. Successful baud rate detection sets the INTR_RX.BAUD_DETECT interrupt cause to '1' (BR_COUNTER is reliable). This functionality is used to synchronize/refine the receiver clock to the transmitter clock. The receiver software can use the BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Default Value: 0
10	MP_MODE	Multi-processor mode. When '1', multi-processor mode is enabled. In this mode, RX_CTRL.DATA_WIDTH should indicate a 9-bit data frame. In multi-processor mode, the 9th received bit of a data frame separates addresses (bit is '1') from data (bit is '0'). A received address is matched with RX_MATCH.DATA and RX_MATCH.MASK. In the case of a match, subsequent received data are sent to the RX FIFO. In the case of NO match, subsequent received data are dropped. Default Value: 0
9	DROP_ON_FRAME_ERROR	Behavior when an error is detected in a start or stop period. When '0', received data is sent to the RX FIFO. When '1', received data is dropped and lost. Default Value: 0
8	DROP_ON_PARITY_ERROR	Behavior when a parity check fails. When '0', received data is sent to the RX FIFO. When '1', received data is dropped and lost. Only applicable in standard UART and SmartCard submodes (negatively acknowledged SmartCard data frames may be dropped with this field). Default Value: 0
6	POLARITY	Inverts incoming RX line signal. Inversion is after local loopback. This functionality is intended for IrDA receiver functionality. Default Value: 0
5	PARITY_ENABLED	Parity checking enabled ('1') or not ('0'). Only applicable in standard UART submode. In SmartCard submode, parity checking is always enabled through hardware. In IrDA submode, parity checking is always disabled through hardware. Default Value: 0
4	PARITY	Parity bit. When '0', the receiver expects an even parity. When '1', the receiver expects an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0

16.1.11 SCB0_UART_RX_CTRL (continued)

2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of half bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. Note that in case of a stop bits error, the successive data frames may get lost as the receiver needs to resynchronize its start bit detection. The amount of lost data frames depends on both the amount of stop bits, the idle time between data frames and the data frame value. Default Value: 2

16.1.12 SCB0_UART_RX_STATUS

UART receiver status

Address: 0x4282004C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	BR_COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				BR_COUNTER [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 0	BR_COUNTER	Amount of SCB clock periods that constitute the transmission of a 0x55 data frame (sent least significant bit first) as determined by the receiver. BR_COUNTER / 8 is the amount of SCB clock periods that constitute a bit period. This field has valid data when INTR_RX.BAUD_DETECT is set to '1'. Default Value: Undefined

16.1.13 SCB0_UART_FLOW_CTRL

UART flow control

Address: 0x42820050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	TRIGGER_LEVEL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							RTS_POLARITY

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						CTS_ENABLED	CTS_POLARITY

Bits	Name	Description
25	CTS_ENABLED	Enable use of CTS input signal by the UART transmitter: '0': Disabled. The UART transmitter ignores the CTS input signal and transmits when a data frame is available for transmission in the TX FIFO or the TX shift register. '1': Enabled. The UART transmitter uses CTS input signal to qualify the transmission of data. It transmits when CTS input signal is active and a data frame is available for transmission in the TX FIFO or the TX shift register. If UART_CTRL.LOOPBACK is '1', the CTS input signal is driven by the RTS output signal locally in SCB (both signals are subjected to signal polarity changes are indicated by RTS_POLARITY and CTS_POLARITY). Default Value: 0
24	CTS_POLARITY	Polarity of the CTS input signal '0': CTS is active low ; '1': CTS is active high; Default Value: 0
16	RTS_POLARITY	Polarity of the RTS output signal: '0': RTS is active low; '1': RTS is active high; During SCB reset (Hibernate system power mode), RTS output signal is '1'. This represents an inactive state assuming an active low polarity. Default Value: 0
6 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has less entries than the amount of this field, a Ready To Send (RTS) output signal is activated. By setting this field to "0", flow control is effectively disabled (may be useful for debug purposes). Default Value: 0

16.1.14 SCB0_I2C_CTRL

I2C control

Address: 0x42820060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LOW_PHASE_OVS [7:4]				HIGH_PHASE_OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	None	RW	RW
HW Access	R	R	R	R	R	None	R	R
Name	S_NOT_READY_-DATA_NACK	S_NOT_READY_ADDR_NACK	S_READY_DATA_ACK	S_READY_ADDR_ACK	S_GENERAL_IGNORE	None	M_NOT_READY_-DATA_NACK	M_READY_DATA_ACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	MASTER_-MODE	SLAVE_-MODE	None [29:24]					

Bits	Name	Description
31	MASTER_MODE	Master mode enabled ('1') or not ('0'). Note that both master and slave modes can be enabled at the same time. This allows the IP to address itself. Default Value: 0
30	SLAVE_MODE	Slave mode enabled ('1') or not ('0'). Default Value: 0
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only applicable in master/slave mode. When '0', no loopback When '1', loopback is enabled internally in the peripheral, and as a result unaffected by other I2C devices. This allows a SCB I2C peripheral to address itself. Default Value: 0
15	S_NOT_READY_-DATA_NACK	Only used when: - non EZ mode Functionality is as follows: - 1: a received data element byte the slave is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). Default Value: 1

16.1.14 SCB0_I2C_CTRL (continued)

14	S_NOT_READY_ADDR_NACK	This field is used during an address match or general call address in internally clocked mode Only used when: - EC_AM_MODE is '0', EC_OP_MODE is '0', S_GENERAL_IGNORE is '0] and non EZ mode. Functionality is as follows: - 1: a received (matching) slave address is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). For externally clocked logic (EC_AM is '1') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when (NOT used when EC_AM is '1' and EC_OP is '1' and address match and EZ mode): - EC_AM is '1' and EC_OP is '0'. - EC_AM is '1' and general call address match. - EC_AM is '1' and non EZ mode. Functionality is as follows: - 1: a received (matching or general) slave address is always immediately NACK'd. There are two possibilities: 1). the SCB clock is available (in Active system power mode) and it handles the rest of the current transfer. In this case the I2C master will not observe the NACK. 2).SCB clock is not present (in DeepSleep system power mode). In this case the I2C master will observe the NACK and may retry the transfer in the future (which gives the internally clocked logic the time to wake up from DeepSleep system power mode). - 0: clock stretching is performed (till the SCB clock is available). The logic will handle the ongoing transfer as soon as the clock is enabled. Default Value: 1
13	S_READY_DATA_ACK	When '1', a received data element by the slave is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
12	S_READY_ADDR_ACK	When '1', a received (matching) slave address is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
11	S_GENERAL_IGNORE	When '1', a received general call slave address is immediately NACK'd (no ACK or clock stretching) and treated as a non matching slave address. This is useful for slaves that do not need any data supplied within the general call structure. Default Value: 1
9	M_NOT_READY_DATA_NACK	for I2C master, the NACKed byte should be properly received. it write the data byte, before ACK/NACK decision. When '1', if a received data element byte is written, and the receiver FIFO become full, the master send out NACK . if the reciever FIFO is full (the received data byte cannot be written), it stretch SCL(extend SCL low phase) until the receiver FIFO changes to not full, to write the last byte, then send out NACK. When '0', clock stretching is used instead (till the receiver FIFO is no longer full). Default Value: 1
8	M_READY_DATA_ACK	When '1', a received data element by the master is immediately ACK'd when the receiver FIFO is not full. Default Value: 1
7 : 4	LOW_PHASE_OVS	Serial I2C interface low phase oversampling factor. LOW_PHASE_OVS + 1 SCB clock periods constitute the low phase of a bit period. The valid range is [7, 15] with input signal median filtering and [6, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the regular (no stretching) interface (IF) low time to guarantee functionally correct behavior. With input signal median filtering, the IF low time should be >= 8 SCB clock cycles and <= 16 IP clock cycles. Without input signal median filtering, the IF low time should be >= 7 SCB clock cycles and <= 16 SCB clock cycles. in slave mode, this field is used to define number of clk_scb cycles for tSU-DAT timing (from ACK/NACK/data ready, to SCL rising edge (released from I2C slave clock stretching)) Default Value: 8

16.1.14 SCB0_I2C_CTRL (continued)

3 : 0	HIGH_PHASE_OVS	Serial I2C interface high phase oversampling factor. HIGH_PHASE_OVS + 1 SCB clock periods constitute the high phase of a bit period. The valid range is [5, 15] with input signal median filtering and [4, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the regular interface (IF) high time to guarantee functional correct behavior. With input signal median filtering, the IF high time should be >= 6 SCB clock cycles and <= 16 SCB clock cycles. Without input signal median filtering, the IF high time should be >= 5 SCB clock cycles and <= 16 SCB clock cycles. Default Value: 8

16.1.15 SCB0_I2C_STATUS

I2C status

Address: 0x42820064

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	None	R	R	R
HW Access	None		W	W	None	W	W	W
Name	None [7:6]		M_READ	S_READ	None	I2CS_IC_BUSY	I2C_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	I2C slave base EZ address. Address as provided by an I2C write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	I2C slave current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when I2C_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
5	M_READ	I2C master read transfer ('1') or I2C master write transfer ('0'). When the I2C master is inactive/idle or transmitting START, REPEATED START, STOP or an address, this field is '0". Default Value: 0
4	S_READ	I2C slave read transfer ('1') or I2C slave write transfer ('0'). When the I2C slave is inactive/idle or receiving START, REPEATED START, STOP or an address, this field is '0". Default Value: 0
2	I2CS_IC_BUSY	Indicates whether the internally clocked slave logic is being accessed by external I2C master. --set at ADDR_MATCH --clear at START/RESET, STOP detection, or BUS_ERROR This bit can be used by SW to determine whether I2CS_IC is busy before entering DeepSleep. Default Value: 0
1	I2C_EC_BUSY	Indicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_EZ_ADDR or CURR_EZ_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_EZ_ADDR and CURR_EZ_ADDR are reliable. Default Value: Undefined

16.1.15 SCB0_I2C_STATUS (continued)

0	BUS_BUSY	I2C bus is busy. The bus is considered busy ('1'), from the time a START is detected or from the time the SCL line is '0'. The bus is considered idle ('0'), from the time a STOP is detected. If SCB block is disabled, BUS_BUSY is '0'. After enabling the block, it takes time for the BUS_BUSY to detect a busy bus. This time is the maximum high time of the SCL line. For a 100 kHz interface frequency, this maximum high time may last roughly 5 us (half a bit period). For single master systems, BUS_BUSY does not have to be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START (no bus collisions). For multi-master systems, BUS_BUSY can be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START_ON_IDLE (to prevent bus collisions). Default Value: 0

16.1.16 SCB0_I2C_M_CMD

I2C master command

Address: 0x42820068

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [7:5]			M_STOP	M_NACK	M_ACK	M_START_ON_IDLE	M_START

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	M_STOP	When '1', attempt to transmit a STOP. When this action is performed, the hardware sets this field to '0'. I2C_M_CMD.M_START has a higher priority than this command: in situations where both a STOP and a REPEATED START could be transmitted, M_START takes precedence over M_STOP. Default Value: 0
3	M_NACK	for I2C master, the NACKed byte should be properly received. it write the data byte, before ACK/NACK decision. When '1', attempt to transmit a negative acknowledgement (NACK). if the reciever FIFO is full (the received data byte cannot be written), it stretch SCL(extend SCL low phase) until the receiver FIFO changes to not full, to write the last byte, then send out NACK. When this action is performed, the hardware sets this field to '0'. Default Value: 0
2	M_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0
1	M_START_ON_IDLE	When '1', transmit a START as soon as the bus is idle (I2C_STATUS.BUS_BUSY is '0', note that BUSY has a default value of '0'). For bus idle detection the hardware relies on STOP detection. As a result, bus idle detection is only functional after at least one I2C bus transfer has been detected on the bus (default/reset value of BUSY is '0') . A START is only transmitted when the master state machine is in the default state. When this action is performed, the hardware sets this field to '0'. Default Value: 0

16.1.16 SCB0_I2C_M_CMD (continued)

0	M_START	When '1', transmit a START or REPEATED START. Whether a START or REPEATED START is transmitted depends on the state of the master state machine. A START is only transmitted when the master state machine is in the default state. A REPEATED START is transmitted when the master state machine is not in the default state, but is working on an ongoing transaction. The REPEATED START can only be transmitted after a NACK or ACK has been received for a transmitted data element or after a NACK has been transmitted for a received data element. When this action is performed, the hardware sets this field to '0'. Default Value: 0

16.1.17 SCB0_I2C_S_CMD

I2C slave command

Address: 0x4282006C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	RW1C	RW1C
Name	None [7:3]					S_TX-_ONES_ON_EMPTY	S_NACK	S_ACK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	S_TX_ONES_ON_EMP-TY	When '1', attempt to send ones when TX_FIFO is empty. Once hardware starts to send ones, it will continue send ones until NACK is received, regardless of TX_FIFO status (even if new data is written into TX_FIFO). This bit is used to avoid stretching SCL, which is not expected for some master devices. Default Value: 0
1	S_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). This command has a higher priority than I2C_S_CMD.S_ACK, I2C_CTRL.S_READY_ADDR_ACK or I2C_CTRL.S_READY_DATA_ACK. Default Value: 0
0	S_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). Default Value: 0

16.1.18 SCB0_I2C_CFG

I2C configuration

Address: 0x42820070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [7:5]			SDA_IN_-FILT_SEL	None [3:2]		SDA_IN_FILT_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [15:13]			SCL_IN_-FILT_SEL	None [11:10]		SCL_IN_FILT_TRIM [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [23:22]		SDA_OUT_FILT2_TRIM [21:20]		SDA_OUT_FILT1_TRIM [19:18]		SDA_OUT_FILT0_TRIM [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW		None			
HW Access	None		R		None			
Name	None [31:30]		SDA_OUT_FILT_SEL [29:28]		None [27:24]			

Bits	Name	Description
29 : 28	SDA_OUT_FILT_SEL	Selection of cumulative filter delay on SDA output to meet tHD_DAT parameter "0": 0 ns. "1": 50 ns (filter 0 enabled). "2": 100 ns (filters 0 and 1 enabled). "3": 150 ns (filters 0, 1 and 2 enabled). Default Value: 0
21 : 20	SDA_OUT_FILT2_TRIM	Trim settings for the 50ns delay filter on SDA output used to guarantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required Default Value: 2
19 : 18	SDA_OUT_FILT1_TRIM	Trim settings for the 50ns delay filter on SDA output used to guarantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required Default Value: 2
17 : 16	SDA_OUT_FILT0_TRIM	Trim settings for the 50ns delay filter on SDA output used to guarantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required Default Value: 2
12	SCL_IN_FILT_SEL	Enable for 50ns glitch filter on SCL input '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1

16.1.18 SCB0_I2C_CFG (continued)

9 : 8	SCL_IN_FILT_TRIM	Trim settings for the 50ns glitch filter on the SDA input. Default setting meets the I2C glitch rejections specs. Programmability available if required Default Value: 0
4	SDA_IN_FILT_SEL	Enable for 50ns glitch filter on SDA input '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
1 : 0	SDA_IN_FILT_TRIM	Trim settings for the 50ns glitch filter on the SDA input. Default setting meets the I2C glitch rejections specs. Programmability available if required Default Value: 3

16.1.19 SCB0_I2C_STRETCH_CTRL

I2C stretch control

Address: 0x42820074

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				STRETCH_THRESHOLD [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	STRETCH_THRESHOLD	stretch threthold. Typically it is the SCL turaound delay (including IO cell delay, SCL rise time, analog filter delay), in number of clk_scb cycles. When STRETCH_COUNT is higher than this STRETCH_THRESHOLD, STRETCH_DETECTED will be set. STRETCH_DETECTED should be less than "HOVS-2", HOVS means I2C_CTRL.HIGH_PHASE_OVS, or I2C_CTRL_HS.HOVS_HS. Default Value: 0

16.1.20 SCB0_I2C_STRETCH_STATUS

I2C stretch status

Address: 0x42820078

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R			
HW Access	None		W	W	W			
Name	None [7:6]		SYNC_DE-TECTED	STRETCH_ DETECTED	STRETCH_COUNT [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							STRETCH-ING

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	STRETCHING	I2C SCL is stretched by this block (DUT), for I2C master, this can happen when TX FIFO is empty, or RX_FIFO is full, or ACK/NACK is not decided, or RESTART/STOP is not decided. For I2C slave, this can heppend, TX FIFO is empty, or RX_FIFO is full, or ACK/NACK is not decided. Default Value: 0
5	SYNC_DETECTED	synchronization detected. Set when I2C falling edge comes in earler than expected (suppressed by another I2C master during synchronization). Default Value: 0
4	STRETCH_DETECTED	stretch detected. Set when I2C rising edge comes later than expected (suppressed by another master or slave), and STRETCH_COUNT is higher than STRETCH_THRESHOLD. Default Value: 0
3 : 0	STRETCH_COUNT	stretch count. Started when I2C device start to drive high phase on internal SCL output signal, stalled when it detected high level on SCL input signal. Default Value: 0

16.1.21 SCB0_TX_CTRL

Transmitter control

Address: 0x42820200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			DATA_WIDTH [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							MSB_-FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						OPEN_DRAIN_SCL	OPEN_DRAIN

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	OPEN_DRAIN_SCL	Each IO cell "xxx" has two associated IP output signals "xxx_out_en" and "xxx_out". '0': Normal operation mode. Typically, this operation mode is used for IO cells that are connected to (board) wires/lines that are driven by a single IO cell. In this operation mode, for an IO cell "xxx" that is used as an output, the "xxx_out_en" output enable signal is typically constant '1' the "xxx_out" output is the outputted value. In other words, in normal operation mode, the "xxx_out" output is used to control the IO cell output value: "xxx_out" is '0' to drive an IO cell output value of '0' and "xxx_out" is '1' to drive an IO cell output value of '1'. '1': Open drain operation mode. Typically this operation mode is used for IO cells that are connected to (board) wires/lines that are driven by multiple IO cells (possibly on multiple chips). In this operation mode, for and IO cell "xxx" that is used as an output, the "xxx_out_en" output controls the outputted value. Typically, open drain operation mode drives low/'0' and the "xxx_out" output is constant '1'. In other words, in open drain operation mode, the "xxx_out_en" output is used to control the IO cell output value: in drive low/'0' mode: "xxx_out_en" is '1' (drive enabled) to drive an IO cell output value of '0' and "xxx_out_en" is '1' (drive disabled) to not drive an IO cell output value (another IO cell can drive the wire/line or a pull up results in a wire/line value '1'). this bit is applicable to I2C SCL only. I2C SDA always work in open-drain mode. this is not applicable to M0S8, which does not need special control in SCB for open-drain drive mode. Default Value: 1

16.1.21 SCB0_TX_CTRL (continued)

16	OPEN_DRAIN	Each IO cell "xxx" has two associated IP output signals "xxx_out_en" and "xxx_out". '0': Normal operation mode. Typically, this operation mode is used for IO cells that are connected to (board) wires/lines that are driven by a single IO cell. In this operation mode, for an IO cell "xxx" that is used as an output, the "xxx_out_en" output enable signal is typically constant '1' the "xxx_out" output is the outputted value. In other words, in normal operation mode, the "xxx_out" output is used to control the IO cell output value: "xxx_out" is '0' to drive an IO cell output value of '0' and "xxx_out" is '1' to drive an IO cell output value of '1'. '1': Open drain operation mode. Typically this operation mode is used for IO cells that are connected to (board) wires/lines that are driven by multiple IO cells (possibly on multiple chips). In this operation mode, for and IO cell "xxx" that is used as an output, the "xxx_out_en" output controls the outputted value. Typically, open drain operation mode drives low/'0' and the "xxx_out" output is constant '1'. In other words, in open drain operation mode, the "xxx_out_en" output is used to control the IO cell output value: in drive low/'0' mode: "xxx_out_en" is '1' (drive enabled) to drive an IO cell output value of '0' and "xxx_out_en" is '1' (drive disabled) to not drive an IO cell output value (another IO cell can drive the wire/line or a pull up results in a wire/line value '1'). The open drain mode is supported for: - UART mode, "uart_tx" IO cell. - SPI mode, "spi_miso" IO cell. this bit is not applicable to I2C mode, "i2c_scl" and "i2c_sda" IO cells. Default Value: 0
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
4 : 0	DATA_WIDTH	Dataframe width, depending on CTRL.MEM_WIDTH. DATA_WIDTH + 1 is the amount of bits in a transmitted data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 31]. For I2C the only valid value is 7. In EZ mode (for both SPI and I2C), the only valid value is 7. Default Value: 7

16.1.22 SCB0_TX_FIFO_CTRL

Transmitter FIFO control

Address: 0x42820204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	TRIGGER_LEVEL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware reads from the transmitter FIFO do not remove FIFO entries. Freeze will not advance the TX FIFO read pointer. Default Value: 0
16	CLEAR	When '1', the transmitter FIFO and transmitter shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
6 : 0	TRIGGER_LEVEL	Trigger level. When the transmitter FIFO has less entries than the number of this field, a transmitter trigger event INTR_TX.TRIGGER is generated. Default Value: 0

16.1.23 SCB0_TX_FIFO_STATUS

Transmitter FIFO status

Address: 0x42820208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	USED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None	R						
HW Access	None	W						
Name	None	RD_PTR [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None	R						
HW Access	None	W						
Name	None	WR_PTR [30:24]						

Bits	Name	Description
30 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written. Default Value: 0
22 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read by the hardware. Default Value: 0
15	SR_VALID	Indicates whether the TX shift registers holds a valid data frame ('1') or not ('0'). The shift register can be considered the top of the TX FIFO (the data frame is not included in the USED field of the TX FIFO). The shift register is a working register and holds the data frame that is currently transmitted (when the protocol state machine is transmitting a data frame) or the data frame that is transmitted next (when the protocol state machine is not transmitting a data frame). Default Value: 0
7 : 0	USED	Amount of entries in the transmitter FIFO. The value of this field ranges from 0 to FF_DATA_NR (EZ_DATA_NR/2). Default Value: 0

16.1.24 SCB0_TX_FIFO_WR

Transmitter FIFO write

Address: 0x42820240

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data frame written into the transmitter FIFO. Behavior is similar to that of a PUSH operation. Note that when CTRL.MEM_WIDTH is "0", only DATA[7:0] are used and when CTRL.MEM_WIDTH is "1", only DATA[15:0] are used. A write to a full TX FIFO sets INTR_TX.OVERFLOW to '1'. Default Value: 0

16.1.25 SCB0_RX_CTRL

Receiver control

Address: 0x42820300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			DATA_WIDTH [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						MEDIAN	MSB_-FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	MEDIAN	Median filter. When '1', a digital 3 taps median filter is performed on input interface lines. This filter should reduce the susceptibility to errors. However, its requires higher oversampling values. For UART IrDA submode, this field should always be '1'. Default Value: 0
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
4 : 0	DATA_WIDTH	Dataframe width, depending on CTRL.MEM_WIDTH. DATA_WIDTH + 1 is the expected amount of bits in received data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 31]. For I2C the only valid value is 7. In EZ mode (for both SPI and I2C), the only valid value is 7. Default Value: 7

16.1.26 SCB0_RX_FIFO_CTRL

Receiver FIFO control

Address: 0x42820304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	TRIGGER_LEVEL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware writes to the receiver FIFO have no effect. Freeze will not advance the RX FIFO write pointer. Default Value: 0
16	CLEAR	When '1', the receiver FIFO and receiver shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
6 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has more entries than the number of this field, a receiver trigger event INTR_RX.TRIGGER is generated. Default Value: 0

16.1.27 SCB0_RX_FIFO_STATUS

Receiver FIFO status

Address: 0x42820308

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	USED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None	R						
HW Access	None	W						
Name	None	RD_PTR [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None	R						
HW Access	None	W						
Name	None	WR_PTR [30:24]						

Bits	Name	Description
30 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written by the hardware. Default Value: 0
22 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read. Default Value: 0
15	SR_VALID	Indicates whether the RX shift registers holds a (partial) valid data frame ('1') or not ('0'). The shift register can be considered the bottom of the RX FIFO (the data frame is not included in the USED field of the RX FIFO). The shift register is a working register and holds the data frame that is currently being received (when the protocol state machine is receiving a data frame). Default Value: 0
7 : 0	USED	Amount of entries in the receiver FIFO. The value of this field ranges from 0 to FF_DATA_NR (EZ_DATA_NR/2). Default Value: 0

16.1.28 SCB0_RX_MATCH

Slave address and mask

Address: 0x42820310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	MASK	Slave device address mask. This field is a mask that specifies which of the slave address bits take part in the matching. MATCH = ((ADDR & MASK) == ("slave address" & MASK)). Default Value: 0
7 : 0	ADDR	Slave device address. In UART multi-processor mode, all 8 bits are used. In I2C slave mode, only bits 7 down to 1 are used. This reflects the organization of the first transmitted byte in a I2C transfer: the first 7 bits represent the address of the addressed slave, and the last 1 bit is a read/write indicator ('0': write, '1': read). Default Value: 0

16.1.29 SCB0_RX_FIFO_RD

Receiver FIFO read

Address: 0x42820340

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will remove the data frame from the FIFO; i.e. behavior is similar to that of a POP operation. Note that when CTRL.MEM_WIDTH is "0", only DATA[7:0] are used and when CTRL.MEM_WIDTH is "1", only DATA[15:0] are used A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. When this register is read through the debugger, the data frame will not be removed from the FIFO. Similar in operation to RX_FIFO_RD_SILENT Default Value: Undefined

16.1.30 SCB0_RX_FIFO_RD_SILENT

Receiver FIFO read silent

Address: 0x42820344

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will NOT remove the data frame from the FIFO; i.e. behavior is similar to that of a PEEK operation. Note that when CTRL.MEM_WIDTH is "0", only DATA[7:0] are used and when CTRL.MEM_WIDTH is "1", only DATA[15:0] are used A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. Default Value: Undefined

16.1.31 SCB0_EZ_DATA0

Memory buffer

Address: 0x42820400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

16.1.32 SCB0_INTR_CAUSE

Active clocked interrupt signal

Address: 0x42820E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		SPI_EC	I2C_EC	RX	TX	S	M

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	SPI_EC	Externally clocked SPI interrupt active ("interrupt_spi_ec"): INTR_SPI_EC_MASKED != 0. Default Value: 0
4	I2C_EC	Externally clock I2C interrupt active ("interrupt_i2c_ec"): INTR_I2C_EC_MASKED != 0. Default Value: 0
3	RX	Receiver interrupt active ("interrupt_rx"): INTR_RX_MASKED != 0. Default Value: 0
2	TX	Transmitter interrupt active ("interrupt_tx"): INTR_TX_MASKED != 0. Default Value: 0
1	S	Slave interrupt active ("interrupt_slave"): INTR_S_MASKED != 0. Default Value: 0
0	M	Master interrupt active ("interrupt_master"): INTR_M_MASKED != 0. Default Value: 0

16.1.33 SCB0_INTR_I2C_EC

Externally clocked I2C interrupt request

Address: 0x42820E80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (I2C STOP). This event is an indication that a buffer memory location has been read from. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (I2C STOP). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'. Default Value: 0
1	EZ_STOP	STOP detection. Activated on the end of a every transfer (I2C STOP). Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'. Default Value: 0
0	WAKE_UP	Wake up request. Active on incoming slave request (with address match). Only used when CTRL.EC_AM_MODE is '1'. Default Value: 0

16.1.34 SCB0_INTR_I2C_EC_MASK

Externally clocked I2C interrupt mask

Address: 0x42820E88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

16.1.35 SCB0_INTR_I2C_EC_MASKED

Externally clocked I2C interrupt masked

Address: 0x42820E8C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

16.1.36 SCB0_INTR_SPI_EC

Externally clocked SPI interrupt request

Address: 0x42820EC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (SPI de-selection). This event is an indication that a buffer memory location has been read from. Only used in EZ and CMD_RESP modes and when CTRL.EC_OP_MODE is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (SPI de-selection). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only used in EZ and CMD_RESP modes and when CTRL.EC_OP_MODE is '1'. Default Value: 0
1	EZ_STOP	STOP detection. Activated on the end of a every transfer (SPI deselection). Only available in EZ and CMD_RESP mode and when CTRL.EC_OP_MODE is '1'. Default Value: 0
0	WAKE_UP	Wake up request. Active on incoming slave request when externally clocked selection is '1'. Only used when CTRL.EC_AM_MODE is '1'. Default Value: 0

16.1.37 SCB0_INTR_SPI_EC_MASK

Externally clocked SPI interrupt mask

Address: 0x42820EC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

16.1.38 SCB0_INTR_SPI_EC_MASKED

Externally clocked SPI interrupt masked

Address: 0x42820ECC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

16.1.39 SCB0_INTR_M

Master interrupt request

Address: 0x42820F00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	None	RW1C	RW1C	RW1C
HW Access	None			RW1S	None	RW1S	RW1S	RW1S
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	SPI master transfer done event: all data frames in the transmit FIFO are sent, the transmit FIFO is empty (both TX FIFO and transmit shifter register are empty), and SPI select output pin is de-selected. Default Value: 0
8	I2C_BUS_ERROR	I2C master bus error (unexpected detection of START or STOP condition). Default Value: 0
4	I2C_STOP	I2C master STOP. Set to '1', when the master has transmitted a STOP. Default Value: 0
2	I2C_ACK	I2C master acknowledgement. Set to '1', when the master receives a ACK (typically after the master transmitted the slave address or TX data). Default Value: 0
1	I2C_NACK	I2C master negative acknowledgement. Set to '1', when the master receives a NACK (typically after the master transmitted the slave address or TX data). Default Value: 0
0	I2C_ARB_LOST	I2C master lost arbitration: the value driven by the master on the SDA line is not the same as the value observed on the SDA line. The Firmware should clear the TX FIFO, to re-do this transfer. Default Value: 0

16.1.40 SCB0_INTR_M_SET

Master interrupt set request

Address: 0x42820F04

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	None	RW1S	RW1S	RW1S
HW Access	None			A	None	A	A	A
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

16.1.41 SCB0_INTR_M_MASK

Master interrupt mask

Address: 0x42820F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	RW
HW Access	None			R	None	R	R	R
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

16.1.42 SCB0_INTR_M_MASKED

Master interrupt masked request

Address: 0x42820F0C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	None	R	R	R
HW Access	None			W	None	W	W	W
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	R
HW Access	None						W	W
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

16.1.43 SCB0_INTR_S

Slave interrupt request

Address: 0x42820F40

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [23:17]							I2C_RE-START

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	I2C_RESTART	I2C slave RESTART received. Set to '1', when REPEATED START event is detected. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') AND clock stretching is performed (I2C_CTRL.S_NOT_READY_ADDR_NACK is '0'), this field is NOT set. this is not applicable when address in previous transfer is master-code. Default Value: 0
11	SPI_BUS_ERROR	SPI slave deselected at an unexpected time in the SPI transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0
10	SPI_EZ_STOP	SPI slave deselected after any EZ SPI transfer occurred. Default Value: 0
9	SPI_EZ_WRITE_STOP	SPI slave deselected after a write EZ SPI transfer occurred. Default Value: 0
8	I2C_BUS_ERROR	I2C slave bus error (unexpected detection of START or STOP condition). This should not occur, it represents erroneous I2C bus behavior. In case of a bus error, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

16.1.43 SCB0_INTR_S (continued)

7	I2C_GENERAL	I2C slave general call address received. If CTRL.ADDR_ACCEPT, the received address 0x00 (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
6	I2C_ADDR_MATCH	I2C slave matching address received. If CTRL.ADDR_ACCEPT, the received address (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
5	I2C_START	I2C slave START received. Set to '1', when START or REPEATED START event is detected. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') AND clock stretching is performed (I2C_CTRL.S_NOT_READY_ADDR_NACK is '0'), this field is NOT set. The Firmware should use INTR_S_EC.WAKE_UP, INTR_S.I2C_ADDR_MATCH and INTR_S.I2C_GENERAL. Default Value: 0
4	I2C_STOP	I2C STOP event for I2C (read or write) transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. The event is detected on any I2C transfer intended for this slave. Note that a I2C address intended for the slave (address is matching) will result in a I2C_STOP event independent of whether the I2C address is ACK'd or NACK'd. this is not applicable when address in previous transfer is master-code. Default Value: 0
3	I2C_WRITE_STOP	I2C STOP event for I2C write transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. In non EZ mode, the event is detected on any I2C write transfer intended for this slave. Note that a I2C write address intended for the slave (address is matching and a it is a write transfer) will result in a I2C_WRITE_STOP event independent of whether the I2C address is ACK'd or NACK'd. In EZ mode, the event is detected only on I2C write transfers that have EZ data written to the memory structure (an I2C write transfer that only communicates an I2C address and EZ address, will not result in this event being detected). this is not applicable when address in previous transfer is master-code. Default Value: 0
2	I2C_ACK	I2C slave acknowledgement received. Set to '1', when the slave receives a ACK (typically after the slave transmitted TX data). Default Value: 0
1	I2C_NACK	I2C slave negative acknowledgement received. Set to '1', when the slave receives a NACK (typically after the slave transmitted TX data). Default Value: 0
0	I2C_ARB_LOST	I2C slave lost arbitration: the value driven on the SDA line is not the same as the value observed on the SDA line (while the SCL line is '1'). This should not occur, it represents erroneous I2C bus behavior. In case of lost arbitration, the I2C slave state machine aborts the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

16.1.44 SCB0_INTR_S_SET

Slave interrupt set request

Address: 0x42820F44

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW1S
HW Access	None							A
Name	None [23:17]							I2C_RE-START

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	I2C_RESTART	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
11	SPI_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

16.1.44 SCB0_INTR_S_SET (continued)

2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

16.1.45 SCB0_INTR_S_MASK

Slave interrupt mask

Address: 0x42820F48

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							I2C_RE-START

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	I2C_RESTART	Mask bit for corresponding bit in interrupt request register. Default Value: 0
11	SPI_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

16.1.45 SCB0_INTR_S_MASK (continued)

2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

16.1.46 SCB0_INTR_S_MASKED

Slave interrupt masked request

Address: 0x42820F4C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							W
Name	None [23:17]							I2C_RE-START

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	I2C_RESTART	Logical and of corresponding request and mask bits. Default Value: 0
11	SPI_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
10	SPI_EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
9	SPI_EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	I2C_GENERAL	Logical and of corresponding request and mask bits. Default Value: 0
6	I2C_ADDR_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
5	I2C_START	Logical and of corresponding request and mask bits. Default Value: 0
4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
3	I2C_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0

16.1.46 SCB0_INTR_S_MASKED (continued)

2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

16.1.47 SCB0_INTR_TX

Transmitter interrupt request

Address: 0x42820F80

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	None		RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NAC K

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	UART lost arbitration: the value driven on the TX line is not the same as the value observed on the RX line. This condition event is useful when transmitter and receiver share a TX/RX line. This is the case in LIN or SmartCard modes. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
9	UART_DONE	UART transmitter done event. This happens when the IP is done transferring all data in the TX FIFO, and the last stop field is transmitted (both TX FIFO and transmit shifter register are empty). Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
8	UART_NACK	UART transmitter received a negative acknowledgement in SmartCard mode. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
7	BLOCKED	SW cannot get access to the EZ memory (EZ data access), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0
6	UNDERFLOW	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full TX FIFO. Only used in FIFO mode. Default Value: 0

16.1.47 SCB0_INTR_TX (continued)

4	EMPTY	TX FIFO is empty; i.e. it has 0 entries. Only used in FIFO mode. Default Value: 0
1	NOT_FULL	TX FIFO is not full. Dependent on CTRL.MEM_WIDTH: (FF_DATA_NR = EZ_DATA_NR/2) MEM_WIDTH is "0": # entries != FF_DATA_NR. MEM_WIDTH is "1": # entries != FF_DATA_NR/2. MEM_WIDTH is "2": # entries != FF_DATA_NR/4. Only used in FIFO mode. Default Value: 0
0	TRIGGER	Less entries in the TX FIFO than the value specified by TX_FIFO_CTRL.TRIGGER_LEVEL. Only used in FIFO mode. Default Value: 0

16.1.48 SCB0_INTR_TX_SET

Transmitter interrupt set request

Address: 0x42820F84

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
HW Access	A	A	A	A	None		A	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	NOT_FULL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

16.1.49 SCB0_INTR_TX_MASK

Transmitter interrupt mask

Address: 0x42820F88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None		RW	RW
HW Access	R	R	R	R	None		R	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	NOT_FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

16.1.50 SCB0_INTR_TX_MASKED

Transmitter interrupt masked request

Address: 0x42820F8C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	None		R	R
HW Access	W	W	W	W	None		W	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0
9	UART_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	UART_NACK	Logical and of corresponding request and mask bits. Default Value: 0
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
4	EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
1	NOT_FULL	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

16.1.51 SCB0_INTR_RX

Receiver interrupt request

Address: 0x42820FC0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	None	RW1C	RW1C	None	RW1C
HW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Break detection is successful: the line is '0' for UART_RX_CTRL.BREAK_WIDTH + 1 bit period. Can occur at any time to address unanticipated break fields; i.e. "break-in-data" is supported. This feature is supported for the UART standard and LIN submodes. For the UART standard submodes, ongoing receipt of data frames is NOT affected; i.e. Firmware is expected to take the proper action. For the LIN submode, possible ongoing receipt of a data frame is stopped and the (partially) received data frame is dropped and baud rate detection is started. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
10	BAUD_DETECT	LIN baudrate detection is completed. The receiver software uses the UART_RX_STA-TUS.BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guaran-tee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
9	PARITY_ERROR	Parity error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '1', the received frame is dropped. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '0', the received frame is send to the RX FIFO. In SmartCard submode, negatively acknowledged data frames generate a parity error. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO. Default Value: 0

16.1.51 SCB0_INTR_RX (continued)

8	FRAME_ERROR	Frame error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. This can be either a start or stop bit(s) error: Start bit error: after the detection of the beginning of a start bit period (RX line changes from '1' to '0'), the middle of the start bit period is sampled erroneously (RX line is '1'). Note: a start bit error is detected BEFORE a data frame is received. Stop bit error: the RX line is sampled as '0', but a '1' was expected. Note: a stop bit error may result in failure to receive successive data frame(s). Note: a stop bit error is detected AFTER a data frame is received. A stop bit error is detected after a data frame is received, and the UART_RX_CTL.DROP_ON_-FRAME_ERROR field specifies whether the received frame is dropped or send to the RX FIFO. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '1', the received data frame is dropped. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '0', the received data frame is send to the RX FIFO. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO; i.e. the RX FIFO does not have error flags to tag erroneous data frames. Default Value: 0
7	BLOCKED	SW cannot get access to the EZ memory (EZ_DATA accesses), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0
6	UNDERFLOW	Attempt to read from an empty RX FIFO. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full RX FIFO. Note: in I2C mode, the OVERFLOW is set when a data frame is received and the RX FIFO is full, independent of whether it is ACK'd or NACK'd. Only used in FIFO mode. Default Value: 0
3	FULL	RX FIFO is full. Note that received data frames are lost when the RX FIFO is full. Dependent on CTRL.MEM_WIDTH: (FF_DATA_NR = EZ_DATA_NR/2) MEM_WIDTH is "0": # entries == FF_DATA_NR. MEM_WIDTH is "1": # entries == FF_DATA_NR/2. MEM_WIDTH is "2": # entries == FF_DATA_NR/4. Only used in FIFO mode. Default Value: 0
2	NOT_EMPTY	RX FIFO is not empty. Only used in FIFO mode. Default Value: 0
0	TRIGGER	More entries in the RX FIFO than the value specified by RX_FIFO_CTRL.TRIGGER_LEVEL. Only used in FIFO mode. Default Value: 0

16.1.52 SCB0_INTR_RX_SET

Receiver interrupt set request

Address: 0x42820FC4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
HW Access	A	A	A	None	A	A	None	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
10	BAUD_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
9	PARITY_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
8	FRAME_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
7	BLOCKED	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
3	FULL	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
2	NOT_EMPTY	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

16.1.53 SCB0_INTR_RX_MASK

Receiver interrupt mask

Address: 0x42820FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	None	RW	RW	None	RW
HW Access	R	R	R	None	R	R	None	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	BAUD_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	PARITY_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	FRAME_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	NOT_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

16.1.54 SCB0_INTR_RX_MASKED

Receiver interrupt masked request

Address: 0x42820FCC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	None	R	R	None	R
HW Access	W	W	W	None	W	W	None	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
10	BAUD_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
9	PARITY_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
8	FRAME_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
3	FULL	Logical and of corresponding request and mask bits. Default Value: 0
2	NOT_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

17 Controller Area Network Flexible Data-Rate (CAN-FD) registers

This section discusses the CAN-FD registers. It lists all the registers in mapping tables, in address order.

17.1 Register details

Register	Address	Description
CANFD0_CH0_CREL	0x42800000	Core Release Register
CANFD0_CH0_ENDN	0x42800004	Endian Register
CANFD0_CH0_DBTP	0x4280000C	Data Bit Timing & Prescaler Register
CANFD0_CH0_TEST	0x42800010	Test Register
CANFD0_CH0_RWD	0x42800014	RAM Watchdog
CANFD0_CH0_CCCR	0x42800018	CC Control Register
CANFD0_CH0_NBTP	0x4280001C	Nominal Bit Timing & Prescaler Register
CANFD0_CH0_TSCC	0x42800020	Timestamp Counter Configuration
CANFD0_CH0_TSCV	0x42800024	Timestamp Counter Value
CANFD0_CH0_TOCC	0x42800028	Timeout Counter Configuration
CANFD0_CH0_TOCV	0x4280002C	Timeout Counter Value
CANFD0_CH0_ECR	0x42800040	Error Counter Register
CANFD0_CH0_PSR	0x42800044	Protocol Status Register
CANFD0_CH0_TDCR	0x42800048	Transmitter Delay Compensation Register
CANFD0_CH0_IR	0x42800050	Interrupt Register
CANFD0_CH0_IE	0x42800054	Interrupt Enable
CANFD0_CH0_ILS	0x42800058	Interrupt Line Select
CANFD0_CH0_ILE	0x4280005C	Interrupt Line Enable
CANFD0_CH0_GFC	0x42800080	Global Filter Configuration
CANFD0_CH0_SIDFC	0x42800084	Standard ID Filter Configuration
CANFD0_CH0_XIDFC	0x42800088	Extended ID Filter Configuration
CANFD0_CH0_XIDAM	0x42800090	Extended ID AND Mask
CANFD0_CH0_HPMS	0x42800094	High Priority Message Status
CANFD0_CH0_NDAT1	0x42800098	New Data 1
CANFD0_CH0_NDAT2	0x4280009C	New Data 2
CANFD0_CH0_RXF0C	0x428000A0	Rx FIFO 0 Configuration
CANFD0_CH0_RXF0S	0x428000A4	Rx FIFO 0 Status
CANFD0_CH0_RXF0A	0x428000A8	Rx FIFO 0 Acknowledge
CANFD0_CH0_RXBC	0x428000AC	Rx Buffer Configuration
CANFD0_CH0_RXF1C	0x428000B0	Rx FIFO 1 Configuration
CANFD0_CH0_RXF1S	0x428000B4	Rx FIFO 1 Status

Controller Area Network Flexible Data-Rate (CAN-FD) registers

Register	Address	Description
CANFD0_CH0_RXF1A	0x428000B8	Rx FIFO 1 Acknowledge
CANFD0_CH0_RXESC	0x428000BC	Rx Buffer / FIFO Element Size Configuration
CANFD0_CH0_TXBC	0x428000C0	Tx Buffer Configuration
CANFD0_CH0_TXFQS	0x428000C4	Tx FIFO/Queue Status
CANFD0_CH0_TXESC	0x428000C8	Tx Buffer Element Size Configuration
CANFD0_CH0_TXBRP	0x428000CC	Tx Buffer Request Pending
CANFD0_CH0_TXBAR	0x428000D0	Tx Buffer Add Request
CANFD0_CH0_TXBCR	0x428000D4	Tx Buffer Cancellation Request
CANFD0_CH0_TXBTO	0x428000D8	Tx Buffer Transmission Occurred
CANFD0_CH0_TXBCF	0x428000DC	Tx Buffer Cancellation Finished
CANFD0_CH0_TXBTIE	0x428000E0	Tx Buffer Transmission Interrupt Enable
CANFD0_CH0_TXBCIE	0x428000E4	Tx Buffer Cancellation Finished Interrupt Enable
CANFD0_CH0_TXEFC	0x428000F0	Tx Event FIFO Configuration
CANFD0_CH0_TXEFS	0x428000F4	Tx Event FIFO Status
CANFD0_CH0_TXEFA	0x428000F8	Tx Event FIFO Acknowledge
CANFD0_CH0_TTTMC	0x42800100	TT Trigger Memory Configuration
CANFD0_CH0_TTRMC	0x42800104	TT Reference Message Configuration
CANFD0_CH0_TTOCF	0x42800108	TT Operation Configuration
CANFD0_CH0_TTMLM	0x4280010C	TT Matrix Limits
CANFD0_CH0_TURCF	0x42800110	TUR Configuration
CANFD0_CH0_TTOCN	0x42800114	TT Operation Control
CANFD0_CH0_TTGTP	0x42800118	TT Global Time Preset
CANFD0_CH0_TTTMK	0x4280011C	TT Time Mark
CANFD0_CH0_TTIR	0x42800120	TT Interrupt Register
CANFD0_CH0_TTIE	0x42800124	TT Interrupt Enable
CANFD0_CH0_TTILS	0x42800128	TT Interrupt Line Select
CANFD0_CH0_TTOST	0x4280012C	TT Operation Status
CANFD0_CH0_TURNA	0x42800130	TUR Numerator Actual
CANFD0_CH0_TTLGT	0x42800134	TT Local & Global Time
CANFD0_CH0_TTCTC	0x42800138	TT Cycle Time & Count
CANFD0_CH0_TTCPT	0x4280013C	TT Capture Time
CANFD0_CH0_TTCSM	0x42800140	TT Cycle Sync Mark
CANFD0_CH0_RXFTOP_CTL	0x42800180	Receive FIFO Top control
CANFD0_CH0_RXFTOP0_STAT	0x428001A0	Receive FIFO 0 Top Status
CANFD0_CH0_RXFTOP0_DATA	0x428001A8	Receive FIFO 0 Top Data
CANFD0_CH0_RXFTOP1_STAT	0x428001B0	Receive FIFO 1 Top Status

Controller Area Network Flexible Data-Rate (CAN-FD) registers

Register	Address	Description
CANFD0_CH0_RXFTOP1_DATA	0x428001B8	Receive FIFO 1 Top Data
CANFD0_CH1_CREL	0x42800200	Core Release Register. See CANFD0_CH0_CREL for the details of bit fields.
CANFD0_CH1_ENDN	0x42800204	Endian Register. See CANFD0_CH0_ENDN for the details of bit fields.
CANFD0_CH1_DBTP	0x4280020C	Data Bit Timing & Prescaler Register. See CANFD0_CH0_DBTP for the details of bit fields.
CANFD0_CH1_TEST	0x42800210	Test Register. See CANFD0_CH0_TEST for the details of bit fields.
CANFD0_CH1_RWD	0x42800214	RAM Watchdog. See CANFD0_CH0_RWD for the details of bit fields.
CANFD0_CH1_CCCR	0x42800218	CC Control Register. See CANFD0_CH0_CCCR for the details of bit fields.
CANFD0_CH1_NBTP	0x4280021C	Nominal Bit Timing & Prescaler Register. See CANFD0_CH0_NBTP for the details of bit fields.
CANFD0_CH1_TSCC	0x42800220	Timestamp Counter Configuration. See CANFD0_CH0_TSCC for the details of bit fields.
CANFD0_CH1_TSCV	0x42800224	Timestamp Counter Value. See CANFD0_CH0_TSCV for the details of bit fields.
CANFD0_CH1_TOCC	0x42800228	Timeout Counter Configuration. See CANFD0_CH0_TOCC for the details of bit fields.
CANFD0_CH1_TOCV	0x4280022C	Timeout Counter Value. See CANFD0_CH0_TOCV for the details of bit fields.
CANFD0_CH1_ECR	0x42800240	Error Counter Register. See CANFD0_CH0_ECR for the details of bit fields.
CANFD0_CH1_PSR	0x42800244	Protocol Status Register. See CANFD0_CH0_PSR for the details of bit fields.
CANFD0_CH1_TDCR	0x42800248	Transmitter Delay Compensation Register. See CANFD0_CH0_TDCR for the details of bit fields.
CANFD0_CH1_IR	0x42800250	Interrupt Register. See CANFD0_CH0_IR for the details of bit fields.
CANFD0_CH1_IE	0x42800254	Interrupt Enable. See CANFD0_CH0_IE for the details of bit fields.
CANFD0_CH1_ILS	0x42800258	Interrupt Line Select. See CANFD0_CH0_ILS for the details of bit fields.
CANFD0_CH1_ILE	0x4280025C	Interrupt Line Enable. See CANFD0_CH0_ILE for the details of bit fields.

Controller Area Network Flexible Data-Rate (CAN-FD) registers

Register	Address	Description
CANFD0_CH1_GFC	0x42800280	Global Filter Configuration. See CANFD0_CH0_GFC for the details of bit fields.
CANFD0_CH1_SIDFC	0x42800284	Standard ID Filter Configuration. See CANFD0_CH0_SIDFC for the details of bit fields.
CANFD0_CH1_XIDFC	0x42800288	Extended ID Filter Configuration. See CANFD0_CH0_XIDFC for the details of bit fields.
CANFD0_CH1_XIDAM	0x42800290	Extended ID AND Mask. See CANFD0_CH0_XIDAM for the details of bit fields.
CANFD0_CH1_HPMS	0x42800294	High Priority Message Status. See CANFD0_CH0_HPMS for the details of bit fields.
CANFD0_CH1_NDAT1	0x42800298	New Data 1. See CANFD0_CH0_NDAT1 for the details of bit fields.
CANFD0_CH1_NDAT2	0x4280029C	New Data 2. See CANFD0_CH0_NDAT2 for the details of bit fields.
CANFD0_CH1_RXF0C	0x428002A0	Rx FIFO 0 Configuration. See CANFD0_CH0_RXF0C for the details of bit fields.
CANFD0_CH1_RXF0S	0x428002A4	Rx FIFO 0 Status. See CANFD0_CH0_RXF0S for the details of bit fields.
CANFD0_CH1_RXF0A	0x428002A8	Rx FIFO 0 Acknowledge. See CANFD0_CH0_RXF0A for the details of bit fields.
CANFD0_CH1_RXBC	0x428002AC	Rx Buffer Configuration. See CANFD0_CH0_RXBC for the details of bit fields.
CANFD0_CH1_RXF1C	0x428002B0	Rx FIFO 1 Configuration. See CANFD0_CH0_RXF1C for the details of bit fields.
CANFD0_CH1_RXF1S	0x428002B4	Rx FIFO 1 Status. See CANFD0_CH0_RXF1S for the details of bit fields.
CANFD0_CH1_RXF1A	0x428002B8	Rx FIFO 1 Acknowledge. See CANFD0_CH0_RXF1A for the details of bit fields.
CANFD0_CH1_RXESC	0x428002BC	Rx Buffer / FIFO Element Size Configuration. See CANFD0_CH0_RXESC for the details of bit fields.
CANFD0_CH1_TXBC	0x428002C0	Tx Buffer Configuration. See CANFD0_CH0_TXBC for the details of bit fields.
CANFD0_CH1_TXFQS	0x428002C4	Tx FIFO/Queue Status. See CANFD0_CH0_TXFQS for the details of bit fields.
CANFD0_CH1_TXESC	0x428002C8	Tx Buffer Element Size Configuration. See CANFD0_CH0_TXESC for the details of bit fields.
CANFD0_CH1_TXBRP	0x428002CC	Tx Buffer Request Pending. See CANFD0_CH0_TXBRP for the details of bit fields.

Controller Area Network Flexible Data-Rate (CAN-FD) registers

Register	Address	Description
CANFD0_CH1_TXBAR	0x428002D0	Tx Buffer Add Request. See CANFD0_CH0_TXBAR for the details of bit fields.
CANFD0_CH1_TXBCR	0x428002D4	Tx Buffer Cancellation Request. See CANFD0_CH0_TXBCR for the details of bit fields.
CANFD0_CH1_TXBTO	0x428002D8	Tx Buffer Transmission Occurred. See CANFD0_CH0_TXBTO for the details of bit fields.
CANFD0_CH1_TXBCF	0x428002DC	Tx Buffer Cancellation Finished. See CANFD0_CH0_TXBCF for the details of bit fields.
CANFD0_CH1_TXBTIE	0x428002E0	Tx Buffer Transmission Interrupt Enable. See CANFD0_CH0_TXBTIE for the details of bit fields.
CANFD0_CH1_TXBCIE	0x428002E4	Tx Buffer Cancellation Finished Interrupt Enable. See CANFD0_CH0_TXBCIE for the details of bit fields.
CANFD0_CH1_TXEFC	0x428002F0	Tx Event FIFO Configuration. See CANFD0_CH0_TXEFC for the details of bit fields.
CANFD0_CH1_TXEFS	0x428002F4	Tx Event FIFO Status. See CANFD0_CH0_TXEFS for the details of bit fields.
CANFD0_CH1_TXEFA	0x428002F8	Tx Event FIFO Acknowledge. See CANFD0_CH0_TXEFA for the details of bit fields.
CANFD0_CH1_TTTMC	0x42800300	TT Trigger Memory Configuration. See CANFD0_CH0_TTTMC for the details of bit fields.
CANFD0_CH1_TTRMC	0x42800304	TT Reference Message Configuration. See CANFD0_CH0_TTRMC for the details of bit fields.
CANFD0_CH1_TTOCF	0x42800308	TT Operation Configuration. See CANFD0_CH0_TTOCF for the details of bit fields.
CANFD0_CH1_TTMLM	0x4280030C	TT Matrix Limits. See CANFD0_CH0_TTMLM for the details of bit fields.
CANFD0_CH1_TURCF	0x42800310	TUR Configuration. See CANFD0_CH0_TURCF for the details of bit fields.
CANFD0_CH1_TTOCN	0x42800314	TT Operation Control. See CANFD0_CH0_TTOCN for the details of bit fields.
CANFD0_CH1_TTGTP	0x42800318	TT Global Time Preset. See CANFD0_CH0_TTGTP for the details of bit fields.
CANFD0_CH1_TTTMK	0x4280031C	TT Time Mark. See CANFD0_CH0_TTTMK for the details of bit fields.
CANFD0_CH1_TTIR	0x42800320	TT Interrupt Register. See CANFD0_CH0_TTIR for the details of bit fields.
CANFD0_CH1_TTIE	0x42800324	TT Interrupt Enable. See CANFD0_CH0_TTIE for the details of bit fields.

Controller Area Network Flexible Data-Rate (CAN-FD) registers

Register	Address	Description
CANFD0_CH1_TTILS	0x42800328	TT Interrupt Line Select. See CANFD0_CH0_TTILS for the details of bit fields.
CANFD0_CH1_TTOST	0x4280032C	TT Operation Status. See CANFD0_CH0_TTOST for the details of bit fields.
CANFD0_CH1_TURNA	0x42800330	TUR Numerator Actual. See CANFD0_CH0_TURNA for the details of bit fields.
CANFD0_CH1_TTLGT	0x42800334	TT Local & Global Time. See CANFD0_CH0_TTLGT for the details of bit fields.
CANFD0_CH1_TTCTC	0x42800338	TT Cycle Time & Count. See CANFD0_CH0_TTCTC for the details of bit fields.
CANFD0_CH1_TTCPT	0x4280033C	TT Capture Time. See CANFD0_CH0_TTCPT for the details of bit fields.
CANFD0_CH1_TTCSM	0x42800340	TT Cycle Sync Mark. See CANFD0_CH0_TTCSM for the details of bit fields.
CANFD0_CH1_RXFTOP_CTL	0x42800380	Receive FIFO Top control. See CANFD0_CH0_RXFTOP_CTL for the details of bit fields.
CANFD0_CH1_RXFTOP0_STAT	0x428003A0	Receive FIFO 0 Top Status. See CANFD0_CH0_RXFTOP0_STAT for the details of bit fields.
CANFD0_CH1_RXFTOP0_DATA	0x428003A8	Receive FIFO 0 Top Data. See CANFD0_CH0_RXFTOP0_DATA for the details of bit fields.
CANFD0_CH1_RXFTOP1_STAT	0x428003B0	Receive FIFO 1 Top Status. See CANFD0_CH0_RXFTOP1_STAT for the details of bit fields.
CANFD0_CH1_RXFTOP1_DATA	0x428003B8	Receive FIFO 1 Top Data. See CANFD0_CH0_RXFTOP1_DATA for the details of bit fields.
CANFD0_CTL	0x42801000	Global CAN control register
CANFD0_STATUS	0x42801004	Global CAN status register
CANFD0_INTR0_CAUSE	0x42801010	Consolidated interrupt0 cause register
CANFD0_INTR1_CAUSE	0x42801014	Consolidated interrupt1 cause register
CANFD0_TS_CTL	0x42801020	Time Stamp control register
CANFD0_TS_CNT	0x42801024	Time Stamp counter value

17.1.1 CANFD0_CH0_CREL

Core Release Register

Address: 0x42800000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	DAY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	MON [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access	R				R			
Name	SUBSTEP [23:20]				YEAR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R				R			
HW Access	R				R			
Name	REL [31:28]				STEP [27:24]			

Bits	Name	Description
31 : 28	REL	Core Release One digit, BCD-coded. Default Value: 0x3
27 : 24	STEP	Step of Core Release One digit, BCD-coded. Default Value: 0x2
23 : 20	SUBSTEP	Sub-step of Core Release One digit, BCD-coded. Default Value: 0x3
19 : 16	YEAR	Time Stamp Year One digit, BCD-coded. This field is set by generic parameter on M_TTCAN synthesis. Default Value: 0x8
15 : 8	MON	Time Stamp Month Two digits, BCD-coded. This field is set by generic parameter on M_TTCAN synthesis. Default Value: 0x06
7 : 0	DAY	Time Stamp Day Two digits, BCD-coded. This field is set by generic parameter on M_TTCAN synthesis. Default Value: 0x09

17.1.2 CANFD0_CH0_ENDN

Endian Register

Address: 0x42800004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	ETV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ETV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ETV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ETV [31:24]							

Bits	Name	Description
31 : 0	ETV	Endianness Test Value The endianness test value is 0x87654321. Default Value: 0x87654321

17.1.3 CANFD0_CH0_DBTP

Data Bit Timing & Prescaler Register

Address: 0x4280000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DTSEG2 [7:4]				DSJW [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			DTSEG1 [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None		RW				
HW Access	R	None		R				
Name	TDC	None [22:21]		DBRP [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	TDC	Transmitter Delay Compensation 0= Transmitter Delay Compensation disabled 1= Transmitter Delay Compensation enabled Default Value: 0
20 : 16	DBRP	Data Bit Rate Prescaler 0x00-0x1F The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Bit Rate Prescaler are 0 to 31. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Default Value: 0
12 : 8	DTSEG1	Data time segment before sample point 0x00-0x1F Valid values are 0 to 31. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Default Value: 0xA
7 : 4	DTSEG2	Data time segment after sample point 0x0-0xF Valid values are 0 to 15. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Default Value: 3
3 : 0	DSJW	Data (Re)Synchronization Jump Width 0x0-0xF Valid values are 0 to 15. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Default Value: 3

17.1.4 CANFD0_CH0_TEST

Test Register

Address: 0x42800010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	RW		RW	RW	RW	RW	RW
HW Access	R	R		R	R	R	R	R
Name	RX	TX [6:5]		LBCK	CAT	CAM	TAT	TAM

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	RX	Receive Pin Monitors the actual value of pin m_ttcan_rx 0= The CAN bus is dominant (m_ttcan_rx = '0') 1= The CAN bus is recessive (m_ttcan_rx = '1') Default Value: Undefined
6 : 5	TX	Control of Transmit Pin 00 Reset value, m_ttcan_tx controlled by the CAN Core, updated at the end of the CAN bit time 01 Sample Point can be monitored at pin m_ttcan_tx 10 Dominant ('0') level at pin m_ttcan_tx 11 Recessive ('1') at pin m_ttcan_tx Default Value: 0
4	LBCK	Loop Back Mode 0= Reset value, Loop Back Mode is disabled 1= Loop Back Mode is enabled (see Section 3.1.9, Test Modes) Default Value: 0
3	CAT	ASC is not supported by M_TTCAN Check ASC Transmit Control Monitors level at output pin m_ttcan_asct. 0= Output pin m_ttcan_asct = '0' Default Value: 0
2	CAM	ASC is not supported by M_TTCAN Check ASC Multiplexer Control Monitors level at output pin m_ttcan_ascm. 0= Output pin m_ttcan_ascm = '0' 1= Output pin m_ttcan_ascm = '1' Default Value: 0

17.1.4 CANFD0_CH0_TEST (continued)

1	TAT	ASC is not supported by M_TTCAN Test ASC Transmit Control Controls output pin m_ttcan_asct in test mode, ORed with the signal from the FSE 0= Level at pin m_ttcan_asct controlled by FSE 1= Level at pin m_ttcan_asct = '1' Default Value: 0
0	TAM	ASC is not supported by M_TTCAN Test ASC Multiplexer Control Controls output pin m_ttcan_ascm in test mode, ORed with the signal from the FSE 0= Level at pin m_ttcan_ascm controlled by FSE 1= Level at pin m_ttcan_ascm = '1' Default Value: 0

17.1.5 CANFD0_CH0_RWD

RAM Watchdog

Address: 0x42800014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WDC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	WDV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	WDV	Watchdog Value Actual Message RAM Watchdog Counter Value. Default Value: 0
7 : 0	WDC	Watchdog Configuration Start value of the Message RAM Watchdog Counter. With the reset value of '00' the counter is disabled. Default Value: 0

17.1.6 CANFD0_CH0_CCCR

CC Control Register

Address: 0x42800018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	TEST	DAR	MON_	CSR	CSA	ASM	CCE	INIT

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	None		RW	RW
HW Access	R	R	R	R	None		R	R
Name	NISO	TXP	EFBI	PXHD	None [11:10]		BRSE	FDOE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	NISO	Non ISO Operation If this bit is set, the M_TTCAN uses the CAN FD frame format as specified by the Bosch CAN FD Specification V1.0. 0= CAN FD frame format according to ISO 11898-1:2015 1= CAN FD frame format according to Bosch CAN FD Specification V1.0 addressing the non-ISO CAN FD Default Value: 0
14	TXP	Transmit Pause If this bit is set, the M_TTCAN pauses for two CAN bit times before starting the next transmission after itself has successfully transmitted a frame (see Section 3.5). 0= Transmit pause disabled 1= Transmit pause enabled Default Value: 0
13	EFBI	Edge Filtering during Bus Integration 0= Edge filtering disabled 1= Two consecutive dominant tq required to detect an edge for hard synchronization Default Value: 0
12	PXHD	Protocol Exception Handling Disable 0= Protocol exception handling enabled 1= Protocol exception handling disabled Default Value: 0
9	BRSE	Bit Rate Switch Enable 0= Bit rate switching for transmissions disabled 1= Bit rate switching for transmissions enabled Default Value: 0

17.1.6 CANFD0_CH0_CCCR (continued)

8	FDOE	FD Operation Enable 0= FD operation disabled 1= FD operation enabled Default Value: 0
7	TEST	Test Mode Enable 0= Normal operation, register TEST holds reset values 1= Test Mode, write access to register TEST enabled Default Value: 0
6	DAR	Disable Automatic Retransmission 0= Automatic retransmission of messages not transmitted successfully enabled 1= Automatic retransmission disabled Default Value: 0
5	MON_	Bus Monitoring Mode Bit MON can only be set by the Host when both CCE and INIT are set to '1'. The bit can be reset by the Host at any time. 0= Bus Monitoring Mode is disabled 1= Bus Monitoring Mode is enabled Default Value: 0
4	CSR	Clock Stop Request, not supported by M_TTCAN use CTL.STOP_REQ at the group level instead. 0= No clock stop is requested 1= Clock stop requested. When clock stop is requested, first INIT and then CSA will be set after all pending transfer requests have been completed and the CAN bus reached idle. Default Value: 0
3	CSA	Clock Stop Acknowledge 0= No clock stop acknowledged 1= M_TTCAN may be set in power down by stopping m_ttcan_hclk and m_ttcan_cclk Default Value: 0
2	ASM	Restricted Operation Mode Bit ASM can only be set by the Host when both CCE and INIT are set to '1'. The bit can be reset by the Host at any time. For a description of the Restricted Operation Mode see Section 3.1.5. 0= Normal CAN operation 1= Restricted Operation Mode active Default Value: 0
1	CCE	Configuration Change Enable 0= The CPU has no write access to the protected configuration registers 1= The CPU has write access to the protected configuration registers (while CCCR.INIT = '1') Default Value: 0
0	INIT	Initialization 0= Normal Operation 1= Initialization is started Default Value: 1

17.1.7 CANFD0_CH0_NBTP

Nominal Bit Timing & Prescaler Register

Address: 0x4280001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	NTSEG2 [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	NTSEG1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	NBRP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							RW
HW Access	R							R
Name	NSJW [31:25]							NBRP

Bits	Name	Description
31 : 25	NSJW	Nominal (Re)Synchronization Jump Width 0x00-0x7F Valid values are 0 to 127. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Default Value: 3
24 : 16	NBRP	Nominal Bit Rate Prescaler 0x000-0x1FFThe value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Bit Rate Prescaler are 0 to 511. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Default Value: 0
15 : 8	NTSEG1	Nominal Time segment before sample point 0x01-0xFF Valid values are 1 to 255. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Default Value: 0xA
6 : 0	NTSEG2	Nominal Time segment after sample point 0x01-0x7F Valid values are 1 to 127. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Default Value: 3

17.1.8 CANFD0_CH0_TSCC

Timestamp Counter Configuration

Address: 0x42800020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						TSS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				TCP [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	TCP	Timestamp Counter Prescaler (still used for TOCC) 0x0-0xF Configures the timestamp and timeout counters time unit in multiples of CAN bit times [1...16]. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Default Value: 0
1 : 0	TSS	Timestamp Select, should always be set to external timestamp counter 00= Timestamp counter value always 0x0000 01= Timestamp counter value incremented according to TCP 10= External timestamp counter value used 11= Same as '00' Default Value: 0

17.1.9 CANFD0_CH0_TSCV

Timestamp Counter Value

Address: 0x42800024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TSC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TSC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	TSC	Timestamp Counter, not used for M_TTCAN The internal/external Timestamp Counter value is captured on start of frame (both Rx and Tx). When TSCC.TSS = '01', the Timestamp Counter is incremented in multiples of CAN bit times [1...16] depending on the configuration of TSCC.TCP. A wrap around sets interrupt flag IR.TSW. Write access resets the counter to zero. When TSCC.TSS = '10', TSC reflects the external Timestamp Counter value. A write access has no impact. Default Value: 0

17.1.10 CANFD0_CH0_TOCC

Timeout Counter Configuration

Address: 0x42800028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		RW
HW Access	None					R		R
Name	None [7:3]					TOS [2:1]		ETOC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	TOP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	TOP [31:24]							

Bits	Name	Description
31 : 16	TOP	Timeout Period Start value of the Timeout Counter (down-counter). Configures the Timeout Period. Default Value: 0xFFFF
2 : 1	TOS	Timeout Select When operating in Continuous mode, a write to TOCV presets the counter to the value configured by TOCC.TOP and continues down-counting. When the Timeout Counter is controlled by one of the FIFOs, an empty FIFO presets the counter to the value configured by TOCC.TOP. Down-counting is started when the first FIFO element is stored. 00= Continuous operation 01= Timeout controlled by Tx Event FIFO 10= Timeout controlled by Rx FIFO 0 11= Timeout controlled by Rx FIFO 1 Default Value: 0
0	ETOC	Enable Timeout Counter 0= Timeout Counter disabled 1= Timeout Counter enabled Default Value: 0

17.1.11 CANFD0_CH0_TOCV

Timeout Counter Value

Address: 0x4280002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TOC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TOC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	TOC	Timeout Counter The Timeout Counter is decremented in multiples of CAN bit times [1...16] depending on the configuration of TSCC.TCP. When decremented to zero, interrupt flag IR.TOO is set and the Timeout Counter is stopped. Start and reset/restart conditions are configured via TOCC.TOS. Default Value: 0xFFFF

17.1.12 CANFD0_CH0_ECR

Error Counter Register

Address: 0x42800040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TEC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R	R						
HW Access	RW	RW						
Name	RP	REC [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW1C							
Name	CEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	CEL	CAN Error Logging The counter is incremented each time when a CAN protocol error causes the Transmit Error Counter or the Receive Error Counter to be incremented. It is reset by read access to CEL. The counter stops at 0xFF; the next increment of TEC or REC sets interrupt flag IR.ELO. Default Value: 0
15	RP	Receive Error Passive 0= The Receive Error Counter is below the error passive level of 128 1= The Receive Error Counter has reached the error passive level of 128 Default Value: 0
14 : 8	REC	Receive Error Counter Actual state of the Receive Error Counter, values between 0 and 127 Default Value: 0
7 : 0	TEC	Transmit Error Counter Actual state of the Transmit Error Counter, values between 0 and 255 Default Value: 0

17.1.13 CANFD0_CH0_PSR

Protocol Status Register

Address: 0x42800044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R		R		
HW Access	RW	RW	RW	RW		RW1S		
Name	BO	EW	EP	ACT [4:3]		LEC [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None	R	R	R	R	R		
HW Access	None	RW1C	RW1C	RW1C	RW1C	RW1S		
Name	None	PXE	RFDF	RBRS	RESI	DLEC [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None	R						
HW Access	None	RW						
Name	None	TDCV [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
22 : 16	TDCV	Transmitter Delay Compensation Value 0x00-0x7F Position of the secondary sample point, defined by the sum of the measured delay from m_can_tx to m_can_rx and TDCR.TDCO. The SSP position is, in the data phase, the number of mtq between the start of the transmitted bit and the secondary sample point. Valid values are 0 to 127 mtq. Default Value: 0
14	PXE	Protocol Exception Event , Reset on Read 0= No protocol exception event occurred since last read access 1= Protocol exception event occurred Default Value: 0
13	RFDF	Received a CAN FD Message , Reset on Read This bit is set independent of acceptance filtering. 0= Since this bit was reset by the CPU, no CAN FD message has been received 1= Message in CAN FD format with FDF flag set has been received Default Value: 0
12	RBRS	BRS flag of last received CAN FD Message , Reset on Read This bit is set together with RFDF, independent of acceptance filtering. 0= Last received CAN FD message did not have its BRS flag set 1= Last received CAN FD message had its BRS flag set Default Value: 0

17.1.13 CANFD0_CH0_PSR (continued)

11	RESI	ESI flag of last received CAN FD Message , Reset on Read This bit is set together with RFDF, independent of acceptance filtering. 0= Last received CAN FD message did not have its ESI flag set 1= Last received CAN FD message had its ESI flag set Default Value: 0
10 : 8	DLEC	Data Phase Last Error Code , Set on Read Type of last error that occurred in the data phase of a CAN FD format frame with its BRS flag set. Coding is the same as for LEC. This field will be cleared to zero when a CAN FD format frame with its BRS flag set has been transferred (reception or transmission) without error. Default Value: 7
7	BO	Bus_Off Status 0= The M_CAN is not Bus_Off 1= The M_CAN is in Bus_Off state Default Value: 0
6	EW	Warning Status 0= Both error counters are below the Error_Warning limit of 96 1= At least one of error counter has reached the Error_Warning limit of 96 Default Value: 0
5	EP	Error Passive 0= The M_CAN is in the Error_Active state. It normally takes part in bus communication and sends an active error flag when an error has been detected 1= The M_CAN is in the Error_Passive state Default Value: 0
4 : 3	ACT	Activity Monitors the module's CAN communication state. 00= Synchronizing - node is synchronizing on CAN communication 01= Idle - node is neither receiver nor transmitter 10= Receiver - node is operating as receiver 11= Transmitter - node is operating as transmitter Default Value: 0
2 : 0	LEC	Last Error Code, Set on Read0 The LEC indicates the type of the last error to occur on the CAN bus. This field will be cleared to '0' when a message has been transferred (reception or transmission) without error. 0= No Error: No error occurred since LEC has been reset by successful reception or transmission. 1= Stuff Error: More than 5 equal bits in a sequence have occurred in a part of a received message where this is not allowed. 2= Form Error: A fixed format part of a received frame has the wrong format. 3= AckError: The message transmitted by the M_TTCAN was not acknowledged by another node. 4= Bit1Error: During the transmission of a message (with the exception of the arbitration field), the device wanted to send a recessive level (bit of logical value '1'), but the monitored bus value was dominant. 5= Bit0Error: During the transmission of a message (or acknowledge bit, or active error flag, or overload flag), the device wanted to send a dominant level (data or identifier bit logical value 0'), but the monitored bus value was recessive. During Bus_Off recovery this status is set each time a sequence of 11 recessive bits has been monitored. This enables the CPU to monitor the proceeding of the Bus_Off recovery sequence (indicating the bus is not stuck at dominant or continuously disturbed). 6= CRCError: The CRC check sum of a received message was incorrect. The CRC of an incoming message does not match with the CRC calculated from the received data. 7= NoChange: Any read access to the Protocol Status Register re-initializes the LEC to '7'. When the LEC shows the value '7', no CAN bus event was detected since the last CPU read access to the Protocol Status Register. Default Value: 7

17.1.14 CANFD0_CH0_TDCR

Transmitter Delay Compensation Register

Address: 0x42800048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	TDCF [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW						
HW Access	None	R						
Name	None	TDCO [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14 : 8	TDCO	Transmitter Delay Compensation Offset 0x00-0x7F Offset value defining the distance between the measured delay from m_ttcan_tx to m_ttcan_rx and the secondary sample point. Valid values are 0 to 127 mtq. Default Value: 0
6 : 0	TDCF	Transmitter Delay Compensation Filter Window Length 0x00-0x7F Defines the minimum value for the SSP position, dominant edges on m_ttcan_rx that would result in an earlier SSP position are ignored for transmitter delay measurement. The feature is enabled when TDCF is configured to a value greater than TDCO. Valid values are 0 to 127 mtq Default Value: 0

17.1.15 CANFD0_CH0_IR

Interrupt Register

Address: 0x42800050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	RF1L_	RF1F	RF1W	RF1N	RF0L_	RF0F	RF0W	RF0N

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	TEFL_	TEFF	TEFW	TEFN	TFE	TCF	TC	HPM

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	EP_	ELO	BEU	BEC	DRX	TOO	MRAF	TSW

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [31:30]		ARA	PED	PEA	WDI	BO_	EW_

Bits	Name	Description
29	ARA	Access to Reserved Address 0= No access to reserved address occurred 1= Access to reserved address occurred Default Value: 0
28	PED	Protocol Error in Data Phase (Data Bit Time is used) 0= No protocol error in data phase 1= Protocol error in data phase detected (PSR.DLEC != 0,7) Default Value: 0
27	PEA	Protocol Error in Arbitration Phase (Nominal Bit Time is used) 0= No protocol error in arbitration phase 1= Protocol error in arbitration phase detected (PSR.LEC != 0,7) Default Value: 0
26	WDI	Watchdog Interrupt 0= No Message RAM Watchdog event occurred 1= Message RAM Watchdog event due to missing READY Default Value: 0
25	BO_	Bus_Off Status 0= Bus_Off status unchanged 1= Bus_Off status changed Default Value: 0
24	EW_	Warning Status 0= Error_Warning status unchanged 1= Error_Warning status changed Default Value: 0

17.1.15 CANFD0_CH0_IR (continued)

23	EP_	Error Passive 0= Error_Passive status unchanged 1= Error_Passive status changed Default Value: 0
22	ELO	Error Logging Overflow 0= CAN Error Logging Counter did not overflow 1= Overflow of CAN Error Logging Counter occurred Default Value: 0
21	BEU	Bit Error Uncorrected Message RAM bit error detected, uncorrected. The flag is set in the folloiwng cases. - M_TTCAN detects uncorrectable ECC error from Message RAM when ECC is enabled and ECC error injection is disabled. - M_TTCAN reads from an out of range Message RAM address. Message RAM bit error sets CCCR.INIT to '1'. This is done to avoid transmission of corrupted data. 0= No bit error detected when reading from Message RAM 1= Bit error detected, uncorrected Default Value: 0
20	BEC	Bit Error Corrected This bit always reads as 0. Default Value: 0
19	DRX	Message stored to Dedicated Rx Buffer The flag is set whenever a received message has been stored into a dedicated Rx Buffer. 0= No Rx Buffer updated 1= At least one received message stored into a Rx Buffer Default Value: 0
18	TOO	Timeout Occurred 0= No timeout 1= Timeout reached Default Value: 0
17	MRAF	Message RAM Access Failure The flag is set, when the Rx Handler - has not completed acceptance filtering or storage of an accepted message until the arbitration field of the following message has been received. In this case acceptance filtering or message storage is aborted and the Rx Handler starts processing of the following message. - was not able to write a message to the Message RAM. In this case message storage is aborted. In both cases the FIFO put index is not updated resp. the New Data flag for a dedicated Rx Buffer is not set, a partly stored message is overwritten when the next message is stored to this location. The flag is also set when the Tx Handler was not able to read a message from the Message RAM in time. In this case message transmission is aborted. In case of a Tx Handler access failure the M_TTCAN is switched into Restricted Operation Mode (see Section 3.1.5). To leave Restricted Operation Mode, the Host CPU has to reset CCCR.ASM. 0= No Message RAM access failure occurred 1= Message RAM access failure occurred Default Value: 0
16	TSW	Timestamp Wraparound 0= No timestamp counter wrap-around 1= Timestamp counter wrapped around Default Value: 0
15	TEFL_	Tx Event FIFO Element Lost 0= No Tx Event FIFO element lost 1= Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero Default Value: 0
14	TEFF	Tx Event FIFO Full 0= Tx Event FIFO not full 1= Tx Event FIFO full Default Value: 0

17.1.15 CANFD0_CH0_IR (continued)

13	TEFW	Tx Event FIFO Watermark Reached 0= Tx Event FIFO fill level below watermark 1= Tx Event FIFO fill level reached watermark Default Value: 0
12	TEFN	Tx Event FIFO New Entry 0= Tx Event FIFO unchanged 1= Tx Handler wrote Tx Event FIFO element Default Value: 0
11	TFE	Tx FIFO Empty 0= Tx FIFO non-empty 1= Tx FIFO empty Default Value: 0
10	TCF	Transmission Cancellation Finished 0= No transmission cancellation finished 1= Transmission cancellation finished Default Value: 0
9	TC	Transmission Completed 0= No transmission completed 1= Transmission completed Default Value: 0
8	HPM	High Priority Message 0= No high priority message received 1= High priority message received Default Value: 0
7	RF1L_	Rx FIFO 1 Message Lost 0= No Rx FIFO 1 message lost 1= Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero Default Value: 0
6	RF1F	Rx FIFO 1 Full 0= Rx FIFO 1 not full 1= Rx FIFO 1 full Default Value: 0
5	RF1W	Rx FIFO 1 Watermark Reached 0= Rx FIFO 1 fill level below watermark 1= Rx FIFO 1 fill level reached watermark Default Value: 0
4	RF1N	Rx FIFO 1 New Message 0= No new message written to Rx FIFO 1 1= New message written to Rx FIFO 1 Default Value: 0
3	RF0L_	Rx FIFO 0 Message Lost 0= No Rx FIFO 0 message lost 1= Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero Default Value: 0
2	RF0F	Rx FIFO 0 Full 0= Rx FIFO 0 not full 1= Rx FIFO 0 full Default Value: 0
1	RF0W	Rx FIFO 0 Watermark Reached 0= Rx FIFO 0 fill level below watermark 1= Rx FIFO 0 fill level reached watermark Default Value: 0
0	RF0N	Rx FIFO 0 New Message 0= No new message written to Rx FIFO 0 1= New message written to Rx FIFO 0 Default Value: 0

17.1.16 CANFD0_CH0_IE

Interrupt Enable

Address: 0x42800054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	RF1LE	RF1FE	RF1WE	RF1NE	RF0LE	RF0FE	RF0WE	RF0NE

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	TEFLE	TEFFE	TEFWE	TEFNE	TFEE	TCFE	TCE	HPME

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	EPE	ELOE	BEUE	BECE	DRXE	TOOE	MRAFE	TSWE

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [31:30]		ARAE	PEDE	PEAE	WDIE	BOE	EWE

Bits	Name	Description
29	ARAE	Access to Reserved Address Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
28	PEDE	Protocol Error in Data Phase Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
27	PEAE	Protocol Error in Arbitration Phase Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
26	WDIE	Watchdog Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
25	BOE	Bus_Off Status Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
24	EWE	Warning Status Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0

17.1.16 CANFD0_CH0_IE (continued)

23	EPE	Error Passive Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
22	ELOE	Error Logging Overflow Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
21	BEUE	Bit Error Uncorrected Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
20	BECE	Bit Error Corrected Interrupt Enable (not used in M_TTCAN) 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
19	DRXE	Message stored to Dedicated Rx Buffer Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
18	TOOE	Timeout Occurred Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
17	MRAFE	Message RAM Access Failure Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
16	TSWE	Timestamp Wraparound Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
15	TEFLE	Tx Event FIFO Event Lost Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
14	TEFFE	Tx Event FIFO Full Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
13	TEFWE	Tx Event FIFO Watermark Reached Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
12	TEFNE	Tx Event FIDO New Entry Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
11	TFEE	Tx FIFO Empty Interrupt Enable 0= Interrupt Disabled 1= Interrupt EnabledTx FIFO Empty Interrupt Enable Default Value: 0
10	TCFE	Transmission Cancellation Finished Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0

17.1.16 CANFD0_CH0_IE (continued)

9	TCE	Transmission Completed Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
8	HPME	High Priority Message Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
7	RF1LE	Rx FIFO 1 Message Lost Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
6	RF1FE	Rx FIFO 1 Full Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
5	RF1WE	Rx FIFO 1 Watermark Reached Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
4	RF1NE	Rx FIFO 1 New Message Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
3	RF0LE	Rx FIFO 0 Message Lost Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
2	RF0FE	Rx FIFO 0 Full Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
1	RF0WE	Rx FIFO 0 Watermark Reached Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
0	RF0NE	Rx FIFO 0 New Message Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0

17.1.17 CANFD0_CH0_ILS

Interrupt Line Select

Address: 0x42800058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	RF1LL	RF1FL	RF1WL	RF1NL	RF0LL	RF0FL	RF0WL	RF0NL

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	TEFLL	TEFFL	TEFWL	TEFNL	TFEL	TCFL	TCL	HPML

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	EPL	ELOL	BEUL	BECL	DRXL	TOOL	MRAFL	TSWL

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [31:30]		ARAL	PEDL	PEAL	WDIL	BOL	EWL

Bits	Name	Description
29	ARAL	Access to Reserved Address Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
28	PEDL	Protocol Error in Data Phase Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
27	PEAL	Protocol Error in Arbitration Phase Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
26	WDIL	Watchdog Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
25	BOL	Bus_Off Status Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
24	EWL	Warning Status Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0

17.1.17 CANFD0_CH0_ILS (continued)

23	EPL	Error Passive Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
22	ELOL	Error Logging Overflow Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
21	BEUL	Bit Error Uncorrected Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
20	BECL	Bit Error Corrected Interrupt Select (not used in M_TTCAN) 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
19	DRXL	Message stored to Dedicated Rx Buffer Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
18	TOOL	Timeout Occurred Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
17	MRAFL	Message RAM Access Failure Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
16	TSWL	Timestamp Wraparound Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
15	TEFLL	Tx Event FIFO Event Lost Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
14	TEFFL	Tx Event FIFO Full Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
13	TEFWL	Tx Event FIFO Watermark Reached Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
12	TEFNL	Tx Event FIFO New Entry Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
11	TFEL	Tx FIFO Empty Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
10	TCFL	Transmission Cancellation Finished Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0

17.1.17 CANFD0_CH0_ILS (continued)

9	TCL	Transmission Completed Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
8	HPML	High Priority Message Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
7	RF1LL	Rx FIFO 1 Message Lost Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
6	RF1FL	Rx FIFO 1 Full Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
5	RF1WL	Rx FIFO 1 Watermark Reached Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
4	RF1NL	Rx FIFO 1 New Message Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
3	RF0LL	Rx FIFO 0 Message Lost Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
2	RF0FL	Rx FIFO 0 Full Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
1	RF0WL	Rx FIFO 0 Watermark Reached Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
0	RF0NL	Rx FIFO 0 New Message Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0

17.1.18 CANFD0_CH0_ILE

Interrupt Line Enable

Address: 0x4280005C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						EINT1	EINT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	EINT1	Enable Interrupt Line 1 0= Interrupt line m_ttcan_int1 disabled 1= Interrupt line m_ttcan_int1 enabled Default Value: 0
0	EINT0	Enable Interrupt Line 0 0= Interrupt line m_ttcan_int0 disabled 1= Interrupt line m_ttcan_int0 enabled Default Value: 0

17.1.19 CANFD0_CH0_GFC

Global Filter Configuration

Address: 0x42800080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	RW
HW Access	None		R		R		R	R
Name	None [7:6]		ANFS [5:4]		ANFE [3:2]		RRFS	RRFE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	ANFS	Accept Non-matching Frames Standard Defines how received messages with 11-bit IDs that do not match any element of the filter list are treated. 00= Accept in Rx FIFO 0 01= Accept in Rx FIFO 1 10= Reject 11= Reject Default Value: 0
3 : 2	ANFE	Accept Non-matching Frames Extended Defines how received messages with 29-bit IDs that do not match any element of the filter list are treated. 00= Accept in Rx FIFO 0 01= Accept in Rx FIFO 1 10= Reject 11= Reject Default Value: 0
1	RRFS	Reject Remote Frames Standard 0= Filter remote frames with 11-bit standard IDs 1= Reject all remote frames with 11-bit standard IDs Default Value: 0
0	RRFE	Reject Remote Frames Extended 0= Filter remote frames with 29-bit extended IDs 1= Reject all remote frames with 29-bit extended IDs Default Value: 0

17.1.20 CANFD0_CH0_SIDFC

Standard ID Filter Configuration

Address: 0x42800084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	FLSSA [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	FLSSA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	LSS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	LSS	List Size Standard 0= No standard Message ID filter 1-128= Number of standard Message ID filter elements 128= Values greater than 128 are interpreted as 128 Default Value: 0
15 : 2	FLSSA	Filter List Standard Start Address Start address of standard Message ID filter list (32-bit word address, see Figure 2). Default Value: 0

17.1.21 CANFD0_CH0_XIDFC

Extended ID Filter Configuration

Address: 0x42800088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	FLESA [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	FLESA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	LSE [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
22 : 16	LSE	List Size Extended 0= No extended Message ID filter 1-64= Number of extended Message ID filter elements 64= Values greater than 64 are interpreted as 64 Default Value: 0
15 : 2	FLESA	Filter List Extended Start Address Start address of extended Message ID filter list (32-bit word address, see Figure 2). Default Value: 0

17.1.22 CANFD0_CH0_XIDAM

Extended ID AND Mask

Address: 0x42800090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	EIDM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	EIDM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	EIDM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			R				
Name	None [31:29]			EIDM [28:24]				

Bits	Name	Description
28 : 0	EIDM	Extended ID Mask For acceptance filtering of extended frames the Extended ID AND Mask is ANDed with the Message ID of a received frame. Intended for masking of 29-bit IDs in SAE J1939. With the reset value of all bits set to one the mask is not active. Default Value: 0x1FFFFFFF

17.1.23 CANFD0_CH0_HPMS

High Priority Message Status

Address: 0x42800094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		R					
HW Access	RW		RW					
Name	MSI [7:6]		BIDX [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R	R						
HW Access	RW	RW						
Name	FLST	FIDX [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	FLST	Filter List Indicates the filter list of the matching filter element. 0= Standard Filter List 1= Extended Filter List Default Value: 0
14 : 8	FIDX	Filter Index Index of matching filter element. Range is 0 to SIDFC.LSS - 1 resp. XIDFC.LSE - 1. Default Value: 0
7 : 6	MSI	Message Storage Indicator 00= No FIFO selected 01= FIFO message lost 10= Message stored in FIFO 0 11= Message stored in FIFO 1 Default Value: 0
5 : 0	BIDX	Buffer Index Index of Rx FIFO element to which the message was stored. Only valid when MSI[1] = '1'. Default Value: 0

17.1.24 CANFD0_CH0_NDAT1

New Data 1

Address: 0x42800098

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW							
Name	ND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW							
Name	ND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	RW							
Name	ND [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	RW							
Name	ND [31:24]							

Bits	Name	Description
31 : 0	ND	New Data The register holds the New Data flags of Rx Buffers 0 to 31. The flags are set when the respective Rx Buffer has been updated from a received frame. The flags remain set until the Host clears them. A flag is cleared by writing a '1' to the corresponding bit position. Writing a '0' has no effect. A hard reset will clear the register. 0= Rx Buffer not updated 1= Rx Buffer updated from new message Default Value: 0

17.1.25 CANFD0_CH0_NDAT2

New Data 2

Address: 0x4280009C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW							
Name	ND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW							
Name	ND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	RW							
Name	ND [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	RW							
Name	ND [31:24]							

Bits	Name	Description
31 : 0	ND	New Data The register holds the New Data flags of Rx Buffers 32 to 63. The flags are set when the respective Rx Buffer has been updated from a received frame. The flags remain set until the Host clears them. A flag is cleared by writing a '1' to the corresponding bit position. Writing a '0' has no effect. A hard reset will clear the register. 0= Rx Buffer not updated 1= Rx Buffer updated from new message Default Value: 0

17.1.26 CANFD0_CH0_RXF0C

Rx FIFO 0 Configuration

Address: 0x428000A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	F0SA [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	F0SA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	F0S [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW						
HW Access	R	R						
Name	F0OM	F0WM [30:24]						

Bits	Name	Description
31	F0OM	FIFO 0 Operation Mode FIFO 0 can be operated in blocking or in overwrite mode (see Section 3.4.2). 0= FIFO 0 blocking mode 1= FIFO 0 overwrite mode Default Value: 0
30 : 24	F0WM	Rx FIFO 0 Watermark 0= Watermark interrupt disabled 1-64= Level for Rx FIFO 0 watermark interrupt (IR.RF0W) 64= Watermark interrupt disabled Default Value: 0
22 : 16	F0S	Rx FIFO 0 Size 0= No Rx FIFO 0 1-64= Number of Rx FIFO 0 elements 64= Values greater than 64 are interpreted as 64 The Rx FIFO 0 elements are indexed from 0 to F0S-1 Default Value: 0
15 : 2	F0SA	Rx FIFO 0 Start Address Start address of Rx FIFO 0 in Message RAM (32-bit word address, see Figure 2). Default Value: 0

17.1.27 CANFD0_CH0_RXF0S

Rx FIFO 0 Status

Address: 0x428000A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R						
HW Access	None	RW						
Name	None	F0FL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None		R					
HW Access	None		RW					
Name	None [15:14]		F0GI [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None		R					
HW Access	None		RW					
Name	None [23:22]		F0PI [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	None						R	R
HW Access	None						RW	RW
Name	None [31:26]						RF0L	F0F

Bits	Name	Description
25	RF0L	Rx FIFO 0 Message Lost This bit is a copy of interrupt flag IR.RF0L. When IR.RF0L is reset, this bit is also reset. 0= No Rx FIFO 0 message lost 1= Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero Default Value: 0
24	F0F	Rx FIFO 0 Full 0= Rx FIFO 0 not full 1= Rx FIFO 0 full Default Value: 0
21 : 16	F0PI	Rx FIFO 0 Put Index Rx FIFO 0 write index pointer, range 0 to 63. Default Value: 0
13 : 8	F0GI	Rx FIFO 0 Get Index Rx FIFO 0 read index pointer, range 0 to 63. This field is updated by the software writing to RXF0A.F0AI. When the software reading the value immediately after writing to RXF0A.F0AI, this value should be read twice to ensure that the update is reflected. Default Value: 0
6 : 0	F0FL	Rx FIFO 0 Fill Level Number of elements stored in Rx FIFO 0, range 0 to 64. When the software reading the value immediately after writing to RXF0A.F0AI, this value should be read twice to ensure that the update is reflected. Default Value: 0

17.1.28 CANFD0_CH0_RXF0A

Rx FIFO 0 Acknowledge

Address: 0x428000A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		A					
Name	None [7:6]		F0AI [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	F0AI	Rx FIFO 0 Acknowledge Index After the Host has read a message or a sequence of messages from Rx FIFO 0 it has to write the buffer index of the last element read from Rx FIFO 0 to F0AI. This will set the Rx FIFO 0 Get Index RXF0S.F0GI to F0AI + 1 and update the FIFO 0 Fill Level RXF0S.F0FL. Default Value: 0

17.1.29 CANFD0_CH0_RXBC

Rx Buffer Configuration

Address: 0x428000AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	RBSA [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RBSA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 2	RBSA	Rx Buffer Start Address Configures the start address of the Rx Buffers section in the Message RAM (32-bit word address). Also used to reference debug messages A,B,C. Default Value: 0

17.1.30 CANFD0_CH0_RXF1C

Rx FIFO 1 Configuration

Address: 0x428000B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	F1SA [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	F1SA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	F1S [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW						
HW Access	R	R						
Name	F1OM	F1WM [30:24]						

Bits	Name	Description
31	F1OM	FIFO 1 Operation Mode FIFO 1 can be operated in blocking or in overwrite mode (see Section 3.4.2). 0= FIFO 1 blocking mode 1= FIFO 1 overwrite mode Default Value: 0
30 : 24	F1WM	Rx FIFO 1 Watermark 0= Watermark interrupt disabled 1-64= Level for Rx FIFO 1 watermark interrupt (IR.RF1W) 64= Watermark interrupt disabled Default Value: 0
22 : 16	F1S	Rx FIFO 1 Size 0= No Rx FIFO 1 1-64= Number of Rx FIFO 1 elements 64= Values greater than 64 are interpreted as 64 The Rx FIFO 1 elements are indexed from 0 to F1S - 1 Default Value: 0
15 : 2	F1SA	Rx FIFO 1 Start Address Start address of Rx FIFO 1 in Message RAM (32-bit word address, see Figure 2). Default Value: 0

17.1.31 CANFD0_CH0_RXF1S

Rx FIFO 1 Status

Address: 0x428000B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R						
HW Access	None	RW						
Name	None	F1FL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None		R					
HW Access	None		RW					
Name	None [15:14]		F1GI [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None		R					
HW Access	None		RW					
Name	None [23:22]		F1PI [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	R		None				R	R
HW Access	RW		None				RW	RW
Name	DMS [31:30]		None [29:26]				RF1L	F1F

Bits	Name	Description
31 : 30	DMS	Debug Message Status 00= Idle state, wait for reception of debug messages, DMA request is cleared 01= Debug message A received 10= Debug messages A, B received 11= Debug messages A, B, C received, DMA request is set Default Value: 0
25	RF1L	Rx FIFO 1 Message Lost This bit is a copy of interrupt flag IR.RF1L. When IR.RF1L is reset, this bit is also reset. 0= No Rx FIFO 1 message lost 1= Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero Default Value: 0
24	F1F	Rx FIFO 1 Full 0= Rx FIFO 1 not full 1= Rx FIFO 1 full Default Value: 0
21 : 16	F1PI	Rx FIFO 1 Put Index Rx FIFO 1 write index pointer, range 0 to 63. Default Value: 0
13 : 8	F1GI	Rx FIFO 1 Get Index Rx FIFO 1 read index pointer, range 0 to 63. This field is updated by the software writing to RXF1A.F1AI. When the software reading the value immediately after writing to RXF1A.F1AI, this value should be read twice to ensure that the update is reflected. Default Value: 0

17.1.31 CANFD0_CH0_RXF1S (continued)

6 : 0	F1FL	Rx FIFO 1 Fill Level Number of elements stored in Rx FIFO 1, range 0 to 64. When the software reading the value immediately after writing to RXF1A.F1AI, this value should be read twice to ensure that the update is reflected. Default Value: 0

17.1.32 CANFD0_CH0_RXF1A

Rx FIFO 1 Acknowledge

Address: 0x428000B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		A					
Name	None [7:6]		F1AI [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	F1AI	Rx FIFO 1 Acknowledge Index After the Host has read a message or a sequence of messages from Rx FIFO 1 it has to write the buffer index of the last element read from Rx FIFO 1 to F1AI. This will set the Rx FIFO 1 Get Index RXF1S.F1GI to F1AI + 1 and update the FIFO 1 Fill Level RXF1S.F1FL. Default Value: 0

17.1.33 CANFD0_CH0_RXESC

Rx Buffer / FIFO Element Size Configuration

Address: 0x428000BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	F1DS [6:4]			None	F0DS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					R		
Name	None [15:11]					RBDS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10 : 8	RBDS	Rx Buffer Data Field Size 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field Default Value: 0
6 : 4	F1DS	Rx FIFO 1 Data Field Size 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field Default Value: 0

17.1.33 CANFD0_CH0_RXESC (continued)

2 : 0	F0DS	Rx FIFO 0 Data Field Size 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field Default Value: 0

17.1.34 CANFD0_CH0_TXBC

Tx Buffer Configuration

Address: 0x428000C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	TBSA [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TBSA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW					
HW Access	None		R					
Name	None [23:22]		NDTB [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW	RW					
HW Access	None	R	R					
Name	None	TFQM	TFQS [29:24]					

Bits	Name	Description
30	TFQM	Tx FIFO/Queue Mode 0= Tx FIFO operation 1= Tx Queue operation Default Value: 0
29 : 24	TFQS	Transmit FIFO/Queue Size 0= No Tx FIFO/Queue 1-32= Number of Tx Buffers used for Tx FIFO/Queue 32= Values greater than 32 are interpreted as 32 Default Value: 0
21 : 16	NDTB	Number of Dedicated Transmit Buffers 0= No Dedicated Tx Buffers 1-32= Number of Dedicated Tx Buffers 32= Values greater than 32 are interpreted as 32 Default Value: 0
15 : 2	TBSA	Tx Buffers Start Address Start address of Tx Buffers section in Message RAM (32-bit word address, see Figure 2). Default Value: 0

17.1.35 CANFD0_CH0_TXFQS

Tx FIFO/Queue Status

Address: 0x428000C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R					
HW Access	None		RW					
Name	None [7:6]		TFFL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None			R				
HW Access	None			RW				
Name	None [15:13]			TFGI [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None		R	R				
HW Access	None		RW	RW				
Name	None [23:22]		TFQF	TFQPI [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	TFQF	Tx FIFO/Queue Full 0= Tx FIFO/Queue not full 1= Tx FIFO/Queue full Default Value: 0
20 : 16	TFQPI	Tx FIFO/Queue Put Index Tx FIFO/Queue write index pointer, range 0 to 31. Default Value: 0
12 : 8	TFGI	Tx FIFO Get Index Tx FIFO read index pointer, range 0 to 31. Read as zero when Tx Queue operation is configured TXBC.TFQM = '1'). Default Value: 0
5 : 0	TFFL	Tx FIFO Free Level Number of consecutive free Tx FIFO elements starting from TFGI, range 0 to 32. Read as zero when Tx Queue operation is configured (TXBC.TFQM = '1') Default Value: 0

17.1.36 CANFD0_CH0_TXESC

Tx Buffer Element Size Configuration

Address: 0x428000C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					TBDS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	TBDS	Tx Buffer Data Field Size 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field Default Value: 0

17.1.37 CANFD0_CH0_TXBRP

Tx Buffer Request Pending

Address: 0x428000CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TRP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	TRP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	TRP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	TRP [31:24]							

Bits	Name	Description
31 : 0	TRP	Transmission Request Pending Each Tx Buffer has its own Transmission Request Pending bit. The bits are set via register TX-BAR. The bits are reset after a requested transmission has completed or has been cancelled via register TXBCR. TXBRP bits are set only for those Tx Buffers configured via TXBC. After a TXBRP bit has been set, a Tx scan (see Section 3.5, Tx Handling) is started to check for the pending Tx request with the highest priority (Tx Buffer with lowest Message ID). A cancellation request resets the corresponding transmission request pending bit of register TXBRP. In case a transmission has already been started when a cancellation is requested, this is done at the end of the transmission, regardless whether the transmission was successful or not. The cancellation request bits are reset directly after the corresponding TXBRP bit has been reset. After a cancellation has been requested, a finished cancellation is signaled via TXBCF after successful transmission together with the corresponding TXBTO bit when the transmission has not yet been started at the point of cancellation when the transmission has been aborted due to lost arbitration when an error occurred during frame transmission In DAR mode all transmissions are automatically cancelled if they are not successful. The corresponding TXBCF bit is set for all unsuccessful transmissions. 0= No transmission request pending 1= Transmission request pending Default Value: 0

17.1.38 CANFD0_CH0_TXBAR

Tx Buffer Add Request

Address: 0x428000D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	AR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	AR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	AR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	AR [31:24]							

Bits	Name	Description
31 : 0	AR	Add Request Each Tx Buffer has its own Add Request bit. Writing a '1' will set the corresponding Add Request bit; writing a '0' has no impact. This enables the Host to set transmission requests for multiple Tx Buffers with one write to TXBAR. TXBAR bits are set only for those Tx Buffers configured via TXBC. When no Tx scan is running, the bits are reset immediately, else the bits remain set until the Tx scan process has completed. 0= No transmission request added 1= Transmission requested added Default Value: 0

17.1.39 CANFD0_CH0_TXBCR

Tx Buffer Cancellation Request

Address: 0x428000D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	CR [31:24]							

Bits	Name	Description
31 : 0	CR	Cancellation Request Each Tx Buffer has its own Cancellation Request bit. Writing a '1' will set the corresponding Cancellation Request bit; writing a '0' has no impact. This enables the Host to set cancellation requests for multiple Tx Buffers with one write to TXBCR. TXBCR bits are set only for those Tx Buffers configured via TXBC. The bits remain set until the corresponding bit of TXBRP is reset. 0= No cancellation pending 1= Cancellation pending Default Value: 0

17.1.40 CANFD0_CH0_TXBTO

Tx Buffer Transmission Occurred

Address: 0x428000D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TO [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	TO [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	TO [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	TO [31:24]							

Bits	Name	Description
31 : 0	TO	Transmission Occurred Each Tx Buffer has its own Transmission Occurred bit. The bits are set when the corresponding TXBRP bit is cleared after a successful transmission. The bits are reset when a new transmission is requested by writing a '1' to the corresponding bit of register TXBAR. 0= No transmission occurred 1= Transmission occurred Default Value: 0

17.1.41 CANFD0_CH0_TXBCF

Tx Buffer Cancellation Finished

Address: 0x428000DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CF [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	CF [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	CF [31:24]							

Bits	Name	Description
31 : 0	CF	Cancellation Finished Each Tx Buffer has its own Cancellation Finished bit. The bits are set when the corresponding TXBRP bit is cleared after a cancellation was requested via TXBCR. In case the corresponding TXBRP bit was not set at the point of cancellation, CF is set immediately. The bits are reset when a new transmission is requested by writing a '1' to the corresponding bit of register TXBAR. 0= No transmit buffer cancellation 1= Transmit buffer cancellation finished Default Value: 0

17.1.42 CANFD0_CH0_TXBTIE

Tx Buffer Transmission Interrupt Enable

Address: 0x428000E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TIE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TIE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	TIE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	TIE [31:24]							

Bits	Name	Description
31 : 0	TIE	Transmission Interrupt Enable Each Tx Buffer has its own Transmission Interrupt Enable bit. 0= Transmission interrupt disabled 1= Transmission interrupt enable Default Value: 0

17.1.43 CANFD0_CH0_TXBCIE

Tx Buffer Cancellation Finished Interrupt Enable

Address: 0x428000E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CFIE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CFIE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CFIE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	CFIE [31:24]							

Bits	Name	Description
31 : 0	CFIE	Cancellation Finished Interrupt Enable Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0= Cancellation finished interrupt disabled 1= Cancellation finished interrupt enabled Default Value: 0

17.1.44 CANFD0_CH0_TXEFC

Tx Event FIFO Configuration

Address: 0x428000F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	EFSA [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	EFSA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW					
HW Access	None		R					
Name	None [23:22]		EFS [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW					
HW Access	None		R					
Name	None [31:30]		EFWM [29:24]					

Bits	Name	Description
29 : 24	EFWM	Event FIFO Watermark 0= Watermark interrupt disabled 1-32= Level for Tx Event FIFO watermark interrupt (IR.TEFW) 32= Watermark interrupt disabled Default Value: 0
21 : 16	EFS	Event FIFO Size 0= Tx Event FIFO disabled 1-32= Number of Tx Event FIFO elements 32= Values greater than 32 are interpreted as 32 The Tx Event FIFO elements are indexed from 0 to EFS-1 Default Value: 0
15 : 2	EFSA	Event FIFO Start Address Start address of Tx Event FIFO in Message RAM (32-bit word address, see Figure 2). Default Value: 0

17.1.45 CANFD0_CH0_TXEFS

Tx Event FIFO Status

Address: 0x428000F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R					
HW Access	None		RW					
Name	None [7:6]		EFFL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None			R				
HW Access	None			RW				
Name	None [15:13]			EFGI [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			R				
HW Access	None			RW				
Name	None [23:21]			EFPI [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None						R	R
HW Access	None						RW	RW
Name	None [31:26]						TEFL	EFF

Bits	Name	Description
25	TEFL	Tx Event FIFO Element Lost This bit is a copy of interrupt flag IR.TEFL. When IR.TEFL is reset, this bit is also reset. 0= No Tx Event FIFO element lost 1= Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero. Default Value: 0
24	EFF	Event FIFO Full 0= Tx Event FIFO not full 1= Tx Event FIFO full Default Value: 0
20 : 16	EFPI	Event FIFO Put Index Tx Event FIFO write index pointer, range 0 to 31. Default Value: 0
12 : 8	EFGI	Event FIFO Get Index Tx Event FIFO read index pointer, range 0 to 31. This field is updated by the software writing to TXEFA.EFAI. When the software reading the value immediately after writing to TXEFA.EFAI, this value should be read twice to ensure that the update is reflected. Default Value: 0
5 : 0	EFFL	Event FIFO Fill Level Number of elements stored in Tx Event FIFO, range 0 to 32. When the software reading the value immediately after writing to TXEFA.EFAI, this value should be read twice to ensure that the update is reflected. Default Value: 0

17.1.46 CANFD0_CH0_TXEFA

Tx Event FIFO Acknowledge

Address: 0x428000F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			EFAI [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	EFAI	Event FIFO Acknowledge Index After the Host has read an element or a sequence of elements from the Tx Event FIFO it has to write the index of the last element read from Tx Event FIFO to EFAI. This will set the Tx Event FIFO Get Index TXEFS.EFGI to EFAI + 1 and update the Event FIFO Fill Level TXEFS.EFFL. Default Value: 0

17.1.47 CANFD0_CH0_TTTMC

TT Trigger Memory Configuration

Address: 0x42800100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	TMSA [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TMSA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	TME [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
22 : 16	TME	Trigger Memory Elements 0= No Trigger Memory 1-64= Number of Trigger Memory elements 64= Values greater than 64 are interpreted as 64 Default Value: 0
15 : 2	TMSA	Trigger Memory Start Address Start address of Trigger Memory in Message RAM (32-bit word address, see Figure 2). Default Value: 0

17.1.48 CANFD0_CH0_TTRMC

TT Reference Message Configuration

Address: 0x42800104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None	RW				
HW Access	R	R	None	R				
Name	RMPS	XTD	None	RID [28:24]				

Bits	Name	Description
31	RMPS	Reference Message Payload Select Ignored in case of time slaves. 0= Reference message has no additional payload 1= The following elements are taken from Tx Buffer 0: Message Marker MM, Event FIFO Control EFC, Data Length Code DLC, Data Bytes DB Level 1: bytes 2-8, Level 0,2: bytes 5-8) Default Value: 0
30	XTD	Extended Identifier 0= 11-bit standard identifier 1= 29-bit extended identifier Default Value: 0
28 : 0	RID	Reference Identifier Identifier transmitted with reference message and used for reference message filtering. Standard or extended reference identifier depending on bit XTD. A standard identifier has to be written to ID[28:18]. Default Value: 0

17.1.49 CANFD0_CH0_TTOCF

TT Operation Configuration

Address: 0x42800108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW	RW	None	RW	
HW Access	R			R	R	None	R	
Name	LDSDL [7:5]			TM	GEN	None	OM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW						
HW Access	R	R						
Name	EECS	IRTO [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	AWL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [31:27]					EVTP	ECC	EGTF

Bits	Name	Description
26	EVTP	Event Trigger Polarity 0= Rising edge trigger 1= Falling edge trigger Default Value: 0
25	ECC	Enable Clock Calibration 0= Automatic clock calibration in TTCAN Level 0,2 is disabled 1= Automatic clock calibration in TTCAN Level 0,2 is enabled Default Value: 0
24	EGTF	Enable Global Time Filtering 0= Global time filtering in TTCAN Level 0,2 is disabled 1= Global time filtering in TTCAN Level 0,2 is enabled Default Value: 0
23 : 16	AWL	Application Watchdog Limit The application watchdog can be disabled by programming AWL to 0x00. 0x00-FF Maximum time after which the application has to serve the application watchdog. The application watchdog is incremented once each 256 NTUs. Default Value: 1
15	EECS	Enable External Clock Synchronization If enabled, TUR configuration (TURCF.NCL only) may be updated during TTCAN operation. 0= External clock synchronization in TTCAN Level 0,2 disabled 1= External clock synchronization in TTCAN Level 0,2 enabled Default Value: 0
14 : 8	IRTO	Initial Reference Trigger Offset 0x00-7F Positive offset, range from 0 to 127 Default Value: 0

17.1.49 CANFD0_CH0_TTOCF (continued)

7 : 5	LDSDL	LD of Synchronization Deviation Limit The Synchronization Deviation Limit SDL is configured by its dual logarithm LDSDL with SDL = 2(LDSDL + 5). It should not exceed the clock tolerance given by the CAN bit timing configuration. 0x0-7 LD of Synchronization Deviation Limit (SDL <= 32...4096) Default Value: 0
4	TM	Time Master 0= Time Master function disabled 1= Potential Time Master Default Value: 0
3	GEN	Gap Enable 0= Strictly time-triggered operation 1= External event-synchronized time-triggered operation Default Value: 0
1 : 0	OM	Operation Mode 00= Event-driven CAN communication, default 01= TTCAN level 1 10= TTCAN level 2 11= TTCAN level 0 Default Value: 0

17.1.50 CANFD0_CH0_TTMLM

TT Matrix Limits

Address: 0x4280010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW					
HW Access	R		R					
Name	CSS [7:6]		CCM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				TXEW [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ENTT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None				RW			
HW Access	None				R			
Name	None [31:28]				ENTT [27:24]			

Bits	Name	Description
27 : 16	ENTT	Expected Number of Tx Triggers 0x000-FFF Expected number of Tx Triggers in one Matrix Cycle Default Value: 0
11 : 8	TXEW	Tx Enable Window 0x0-F Length of Tx enable window, 1-16 NTU cycles Default Value: 0
7 : 6	CSS	Cycle Start Synchronization Enables sync pulse output at pin m_ttcan_soc. 00= No sync pulse 01= Sync pulse at start of basic cycle 10= Sync pulse at start of matrix cycle 11= Reserved Default Value: 0
5 : 0	CCM	Cycle Count Max 0x00 1 Basic Cycle per Matrix Cycle 0x01 2 Basic Cycles per Matrix Cycle 0x03 4 Basic Cycles per Matrix Cycle 0x07 8 Basic Cycles per Matrix Cycle 0x0F 16 Basic Cycles per Matrix Cycle 0x1F 32 Basic Cycles per Matrix Cycle 0x3F 64 Basic Cycles per Matrix Cycle others Reserved Default Value: 0

17.1.51 CANFD0_CH0_TURCF

TUR Configuration

Address: 0x42800110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	NCL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	NCL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None	RW					
HW Access	R	None	R					
Name	ELT	None	DC [29:24]					

Bits	Name	Description
31	ELT	Enable Local Time 0= Local time is stopped, default 1= Local time is enabled Default Value: 0
29 : 16	DC	Denominator Configuration 0x0000 Illegal value 0x0001-3FFF Denominator Configuration Default Value: 0x1000
15 : 0	NCL	Numerator Configuration Low Write access to the TUR Numerator Configuration Low is only possible during configuration with TURCF.ELT = '0' or if TTOCF.EECS (external clock synchronization enabled) is set. When a new value for NCL is written outside TT Configuration Mode, the new value takes effect when TTOST.WECS is cleared to '0'. NCL is locked TTOST.WECS is '1'. 0x0000-FFFF Numerator Configuration Low Default Value: 0

17.1.52 CANFD0_CH0_TTOCN

TT Operation Control

Address: 0x42800114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW		RW	RW	RW
HW Access	R		R	R		R	R	R
Name	TMC [7:6]		RTIE	SWS [4:3]		SWP	ECS	SGT

Bits	15	14	13	12	11	10	9	8
SW Access	R	None	RW	RW	RW	RW	RW	RW
HW Access	RW	None	R	R	R	R	R	R
Name	LCKC	None	ESCN	NIG	TMG	FGP	GCS	TTIE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	LCKC	TT Operation Control Register Locked Set by a write access to register TTOCN. Reset when the updated configuration has been synchronized into the CAN clock domain. 0= Write access to TTOCN enabled 1= Write access to TTOCN locked Default Value: 0
13	ESCN	External Synchronization Control If enabled the M_TTCAN synchronizes its cycle time phase to an external event signaled by a rising edge at pin m_ttcan_evt (see Section 4.11). 0= External synchronization disabled 1= External synchronization enabled Default Value: 0
12	NIG	Next is Gap This bit can only be set when the M_TTCAN is the actual Time Master and when it is configured for external event-synchronized time-triggered operation (TTOCF.GEN = '1') 0= No action, reset by reception of any reference message 1= Transmit next reference message with Next_is_Gap = '1' Default Value: 0
11	TMG	Time Mark Gap 0= Reset by each reference message 1= Next reference message started when Register Time Mark interrupt TTIR.RTMI is activated Default Value: 0

17.1.52 CANFD0_CH0_TTOCN (continued)

10	FGP	Finish Gap Set by the CPU, reset by each reference message 0= No reference message requested 1= Application requested start of reference message Default Value: 0
9	GCS	Gap Control Select 0= Gap control independent from m_ttcan_evt 1= Gap control by input pin m_ttcan_evt Default Value: 0
8	TTIE	Trigger Time Mark Interrupt Pulse Enable External time mark events are configured by trigger memory element TMEX (see Section 2.4.7). A trigger time mark interrupt pulse is generated when the trigger memory element becomes active, and the M_TTCAN is in synchronization state In_Schedule or In_Gap. 0= Trigger Time Mark Interrupt output m_ttcan_tmp disabled 1= Trigger Time Mark Interrupt output m_ttcan_tmp enabled Default Value: 0
7 : 6	TMC	Register Time Mark Compare 00= No Register Time Mark Interrupt generated 01= Register Time Mark Interrupt if Time Mark = cycle time 10= Register Time Mark Interrupt if Time Mark = local time 11= Register Time Mark Interrupt if Time Mark = global time Default Value: 0
5	RTIE	Register Time Mark Interrupt Pulse Enable Register time mark interrupts are configured by register TTTMK. A register time mark interrupt pulse with the length of one NTU is generated when the time referenced by TTOCN.TMC (cycle, local, or global) equals TTTMK.TM, independent of the synchronization state. 0= Register Time Mark Interrupt output m_ttcan_rtp disabled 1= Register Time Mark Interrupt output m_ttcan_rtp enabled Default Value: 0
4 : 3	SWS	Stop Watch Source 00= Stop Watch disabled 01= Actual value of cycle time is copied to TTCPT.SWV 10= Actual value of local time is copied to TTCPT.SWV 11= Actual value of global time is copied to TTCPT.SWV Default Value: 0
2	SWP	Stop Watch Polarity 0= Rising edge trigger 1= Falling edge trigger Default Value: 0
1	ECS	External Clock Synchronization Writing a '1' to ECS sets TTOST.WECS if the node is the actual Time Master. ECS is reset after one Host clock period. The external clock synchronization takes effect at the start of the next basic cycle. Default Value: 0
0	SGT	Set Global time Writing a '1' to SGT sets TTOST.WGDT if the node is the actual Time Master. SGT is reset after one Host clock period. The global time preset takes effect when the node transmits the next reference message with the Master_Ref_Mark modified by the preset value written to TTGTP. Default Value: 0

17.1.53 CANFD0_CH0_TTGTP

TT Global Time Preset

Address: 0x42800118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CTP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	CTP [31:24]							

Bits	Name	Description
31 : 16	CTP	Cycle Time Target Phase CTP is write-protected while TTOCN.ESCN or TTOST.SPL are set (see Section 4.11). 0x0000-FFFF Defines target value of cycle time when a rising edge of m_ttcan_evt is expected Default Value: 0
15 : 0	TP	Time Preset TP is write-protected while TTOST.WGTD is set. 0x0000-7FFF Next Master Reference Mark = Master Reference Mark + TP 0x8000 reserved 0x8001-FFFF Next Master Reference Mark = Master Reference Mark - (0x10000 - TP) Default Value: 0

17.1.54 CANFD0_CH0_TTTMK

TT Time Mark

Address: 0x4280011C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TM_ [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TM_ [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	TICC [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	LCKM	None [30:24]						

Bits	Name	Description
31	LCKM	TT Time Mark Register Locked Always set by a write access to registers TTOCN. Set by write access to register TTTMK when TTOCN.TMC != '00'. Reset when the registers have been synchronized into the CAN clock domain. 0= Write access to TTTMK enabled 1= Write access to TTTMK locked Default Value: 0
22 : 16	TICC	Time Mark Cycle Code Cycle count for which the time mark is valid. 0b000000x valid for all cycles 0b000001c valid every second cycle at cycle count mod2 = c 0b00001cc valid every fourth cycle at cycle count mod4 = cc 0b0001ccc valid every eighth cycle at cycle count mod8 = ccc 0b001cccc valid every sixteenth cycle at cycle count mod16 = cccc 0b01ccccc valid every thirty-second cycle at cycle count mod32 = ccccc 0b1cccccc valid every sixty-fourth cycle at cycle count mod64 = cccccc Default Value: 0
15 : 0	TM_	Time Mark 0x0000-FFFF Time Mark Default Value: 0

17.1.55 CANFD0_CH0_TTIR

TT Interrupt Register

Address: 0x42800120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	GTW	SWE	TTMI	RTMI	SOG	CSM_	SMC	SBC

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	IWT	ELC	SE2	SE1	TXO	TXU	GTE	GTD

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW	RW	RW
Name	None [23:19]					CER	AW	WT

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
18	CER	Configuration Error Trigger out of order. 0= No error found in trigger list 1= Error found in trigger list Default Value: 0
17	AW	Application Watchdog 0= Application watchdog served in time 1= Application watchdog not served in time Default Value: 0
16	WT	Watch Trigger 0= No missing reference message 1= Missing reference message (Level 0: cycle time 0xFF00) Default Value: 0
15	IWT	Initialization Watch Trigger The initialization is restarted by resetting IWT. 0= No missing reference message during system startup 1= No system startup due to missing reference message Default Value: 0
14	ELC	Error Level Changed Not set when error level changed during initialization. 0= No change in error level 1= Error level changed Default Value: 0

17.1.55 CANFD0_CH0_TTIR (continued)

13	SE2	Scheduling Error 2 0= No scheduling error 2 1= Scheduling error 2 occurred Default Value: 0
12	SE1	Scheduling Error 1 0= No scheduling error 1 1= Scheduling error 1 occurred Default Value: 0
11	TXO	Tx Count Overflow 0= Number of Tx Trigger as expected 1= More Tx trigger than expected in one matrix cycle Default Value: 0
10	TXU	Tx Count Underflow 0= Number of Tx Trigger as expected 1= Less Tx trigger than expected in one matrix cycle Default Value: 0
9	GTE	Global Time Error Synchronization deviation SD exceeds limit specified by TTOCF.LDSDL, TTCAN Level 0,2 only. 0= Synchronization deviation within limit 1= Synchronization deviation exceeded limit Default Value: 0
8	GTD	Global Time Discontinuity 0= No discontinuity of global time 1= Discontinuity of global time Default Value: 0
7	GTW	Global Time Wrap 0= No global time wrap occurred 1= Global time wrap from 0xFFFF to 0x0000 occurred Default Value: 0
6	SWE	Stop Watch Event 0= No rising/falling edge at stop watch trigger pin m_ttcan_swt detected 1= Rising/falling edge at stop watch trigger pin m_ttcan_swt detected Default Value: 0
5	TTMI	Trigger Time Mark Event Internal Internal time mark events are configured by trigger memory element TMIN (see Section 2.4.7). Set when the trigger memory element becomes active, and the M_TTCAN is in synchronization state In_Gap or In_Schedule. 0= Time mark not reached 1= Time mark reached (Level 0: cycle time TTOCF.IRTO * 0x200) Default Value: 0
4	RTMI	Register Time Mark Interrupt Set when time referenced by TTOCN.TMC (cycle, local, or global) equals TTTMK.TM, independent of the synchronization state. 0= Time mark not reached 1= Time mark reached Default Value: 0
3	SOG	Start of Gap 0= No reference message seen with Next_is_Gap bit set 1= Reference message with Next_is_Gap bit set becomes valid Default Value: 0
2	CSM_	Change of Synchronization Mode 0= No change in master to slave relation or schedule synchronization 1= Master to slave relation or schedule synchronization changed, also set when TTOST.SPL is reset Default Value: 0

17.1.55 CANFD0_CH0_TTIR (continued)

1	SMC	Start of Matrix Cycle 0= No Matrix Cycle started since bit has been reset 1= Matrix Cycle started Default Value: 0
0	SBC	Start of Basic Cycle 0= No Basic Cycle started since bit has been reset 1= Basic Cycle started Default Value: 0

17.1.56 CANFD0_CH0_TTIE

TT Interrupt Enable

Address: 0x42800124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	GTWE	SWEE	TTMIE	RTMIE	SOGE	CSME	SMCE	SBCE

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	IWTE	ELCE	SE2E	SE1E	TXOE	TXUE	GTEE	GTDE

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [23:19]					CERE	AWE_	WTE

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
18	CERE	Configuration Error Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
17	AWE_	Application Watchdog Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
16	WTE	Watch Trigger Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
15	IWTE	Initialization Watch Trigger Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
14	ELCE	Change Error Level Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
13	SE2E	Scheduling Error 2 Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0

17.1.56 CANFD0_CH0_TTIE (continued)

12	SE1E	Scheduling Error 1 Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
11	TXOE	Tx Count Overflow Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
10	TXUE	Tx Count Underflow Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
9	GTEE	Global Time Error Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
8	GTDE	Global Time Discontinuity Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
7	GTWE	Global Time Wrap Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
6	SWEE	Stop Watch Event Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
5	TTMIE	Trigger Time Mark Event Internal Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
4	RTMIE	Register Time Mark Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
3	SOGE	Start of Gap Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
2	CSME	Change of Synchronization Mode Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
1	SMCE	Start of Matrix Cycle Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
0	SBCE	Start of Basic Cycle Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0

17.1.57 CANFD0_CH0_TTILS

TT Interrupt Line Select

Address: 0x42800128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	GTWL	SWEL	TTMIL	RTMIL	SOGL	CSML	SMCL	SBCL

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	IWTL	ELCL	SE2L	SE1L	TXOL	TXUL	GTEL	GTDL

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [23:19]					CERL	AWL_	WTL

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
18	CERL	Configuration Error Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
17	AWL_	Application Watchdog Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
16	WTL	Watch Trigger Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
15	IWTL	Initialization Watch Trigger Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
14	ELCL	Change Error Level Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
13	SE2L	Scheduling Error 2 Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0

17.1.57 CANFD0_CH0_TTILS (continued)

12	SE1L	Scheduling Error 1 Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
11	TXOL	Tx Count Overflow Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
10	TXUL	Tx Count Underflow Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
9	GTEL	Global Time Error Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
8	GTDL	Global Time Discontinuity Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
7	GTWL	Global Time Wrap Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
6	SWEL	Stop Watch Event Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
5	TTMIL	Trigger Time Mark Event Internal Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
4	RTMIL	Register Time Mark Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
3	SOGL	Start of Gap Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
2	CSML	Change of Synchronization Mode Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
1	SMCL	Start of Matrix Cycle Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
0	SBCL	Start of Basic Cycle Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0

17.1.58 CANFD0_CH0_TTOST

TT Operation Status

Address: 0x4280012C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R		R		R	
HW Access	RW	RW	RW		RW		RW	
Name	QCS	QGTP	SYS [5:4]		MS [3:2]		EL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	RTO [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	None					
HW Access	RW	RW	None					
Name	GFI	WGTD	None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	R	R	R		
HW Access	RW	RW	RW	RW	RW	RW		
Name	SPL	WECS	AWE	WFE	GSI	TMP [26:24]		

Bits	Name	Description
31	SPL	Schedule Phase Lock The bit is valid only when external synchronization is enabled (TTOCN.ESCN = '1'). In this case it signals that the difference between cycle time configured by TTGTP.CTP and the cycle time at the rising edge at pin m_ttcan_evt is less or equal 9 NTU (see Section 4.11). 0= Phase outside range 1= Phase inside range Default Value: 0
30	WECS	Wait for External Clock Synchronization 0= No external clock synchronization pending 1= Node waits for external clock synchronization to take effect. The bit is reset at the start of the next basic cycle. Default Value: 0
29	AWE	Application Watchdog Event The application watchdog is served by reading TTOST. When the watchdog is not served in time, bit AWE is set, all TTCAN communication is stopped, and the M_TTCAN is set into Bus Monitor-ing Mode. 0= Application Watchdog served in time 1= Failed to serve Application Watchdog in time Default Value: 0
28	WFE	Wait for Event 0= No Gap announced, reset by a reference message with Next_is_Gap = '0' 1= Reference message with Next_is_Gap = '1' received Default Value: 0

17.1.58 CANFD0_CH0_TTOST (continued)

27	GSI	Gap Started Indicator 0= No Gap in schedule, reset by each reference message and for all time slaves 1= Gap time after Basic Cycle has started Default Value: 0
26 : 24	TMP	Time Master Priority 0x0-7 Priority of actual Time Master Default Value: 0
23	GFI	Gap Finished Indicator Set when the CPU writes TTOCN.FGP, or by a time mark interrupt if TMG = '1', or via input pin m_ttcan_evt if TTOCN.GCS = '1'. Not set by Ref_Trigger_Gap or when Gap is finished by another node sending a reference message. 0= Reset at the end of each reference message 1= Gap finished by M_TTCAN Default Value: 0
22	WGTD	Wait for Global Time Discontinuity 0= No global time preset pending 1= Node waits for the global time preset to take effect. The bit is reset when the node has transmitted a reference message with Disc_Bit = '1' or after it received a reference message. Default Value: 0
15 : 8	RTO	Reference Trigger Offset The Reference Trigger Offset value is a signed integer with a range from -127 (0x81) to 127 (0x7F). There is no notification when the lower limit of -127 is reached. In case the M_TTCAN becomes Time Master (MS[1:0] = '11'), the reset of RTO is delayed due to synchronization between Host and CAN clock domain. For time slaves the value configured by TTOCF.IRTO is read. 0x00-FF Actual Reference Trigger offset value Default Value: 0
7	QCS	Quality of Clock Speed Only relevant in TTCAN Level 0 and Level 2, otherwise fixed to '1'. 0= Local clock speed not synchronized to Time Master clock speed 1= Synchronization Deviation <= SDL Default Value: 1
6	QGTP	Quality of Global Time Phase Only relevant in TTCAN Level 0 and Level 2, otherwise fixed to '0'. 0= Global time not valid 1= Global time in phase with Time Master Default Value: 0
5 : 4	SYS	Synchronization State 00= Out of Synchronization 01= Synchronizing to TTCAN communication 10= Schedule suspended by Gap (In_Gap) 11= Synchronized to schedule (In_Schedule) Default Value: 0
3 : 2	MS	Master State 00= Master_Off, no master properties relevant 01= Operating as Time Slave 10= Operating as Backup Time Master 11= Operating as current Time Master Default Value: 0
1 : 0	EL	Error Level 00= Severity 0 - No Error 01= Severity 1 - Warning 10= Severity 2 - Error 11= Severity 3 - Severe Error Default Value: 0

17.1.59 CANFD0_CH0_TURNA

TUR Numerator Actual

Address: 0x42800130

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	NAV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	NAV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						R	
HW Access	None						RW	
Name	None [23:18]						NAV [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 0	NAV	Numerator Actual Value 0x0EFFF reserved 0x0F000-20FFF Actual numerator value 0x21000 reserved Default Value: 0x10000

17.1.60 CANFD0_CH0_TTLGT

TT Local & Global Time

Address: 0x42800134

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	LT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	LT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	GT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	GT [31:24]							

Bits	Name	Description
31 : 16	GT	Global Time Non-fractional part of the sum of the node's local time and its local offset (see Section 4.5). 0x0000-FFFF Global time value of TTCAN network Default Value: 0
15 : 0	LT	Local Time Non-fractional part of local time, incremented once each local NTU (see Section 4.5). 0x0000-FFFF Local time value of TTCAN node Default Value: 0

17.1.61 CANFD0_CH0_TTCTC

TT Cycle Time & Count

Address: 0x42800138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		R					
HW Access	None		RW					
Name	None [23:22]		CC [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21 : 16	CC	Cycle Count 0x00-3F Number of actual Basic Cycle in the System Matrix Default Value: 0x3F
15 : 0	CT	Cycle Time Non-fractional part of the difference of the node's local time and Ref_Mark (see Section 4.5). 0x0000-FFFF Cycle time value of TTCAN Basic Cycle Default Value: 0

17.1.62 CANFD0_CH0_TTCPT

TT Capture Time

Address: 0x4280013C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R					
HW Access	None		RW					
Name	None [7:6]		CCV [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	SWV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	SWV [31:24]							

Bits	Name	Description
31 : 16	SWV	Stop Watch Value On a rising/falling edge (as configured via TTOCN.SWP) at the Stop Watch Trigger pin m_ttcan_swt, when TTOCN.SWS is != '00' and TTIR.SWE is '0', the actual time value as selected by TTOCN.SWS (cycle, local, global) is copied to SWV and TTIR.SWE will be set to '1'. Capturing of the next stop watch value is enabled by resetting TTIR.SWE. 0x0000-FFFF Captured Stop Watch value Default Value: 0
5 : 0	CCV	Cycle Count Value Cycle count value captured together with SWV. 0x00-3F Captured cycle count value Default Value: 0

17.1.63 CANFD0_CH0_TTCSM

TT Cycle Sync Mark

Address: 0x42800140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CSM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CSM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CSM	Cycle Sync Mark The Cycle Sync Mark is measured Default Value: 0

17.1.64 CANFD0_CH0_RXFTOP_CTL

Receive FIFO Top control

Address: 0x42800180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						F1TPE	F0TPE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	F1TPE	FIFO 1 Top Pointer Enable. Default Value: 0
0	F0TPE	FIFO 0 Top Pointer Enable. This enables the FIFO top pointer logic to set the FIFO Top Address (FnTA) and message word counter. This logic is also disabled when the IP is being reconfigured (CCCR.CCE=1). When this logic is disabled a Read from RXFTOP0_DATA is undefined. Default Value: 0

17.1.65 CANFD0_CH0_RXFTOP0_STAT

Receive FIFO 0 Top Status

Address: 0x428001A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	F0TA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	F0TA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	F0TA	Current FIFO 0 Top Address. This is a pointer to the next word in the message buffer defined by the FIFO Start Address (FnSA), Get Index (FnGI), the FIFO message size (FnDS) and the message word counter (FnMWC) FnTA = FnSA + FnGI * msg_size[FnDS] + FnMWC Default Value: 0

17.1.66 CANFD0_CH0_RXFTOP0_DATA

Receive FIFO 0 Top Data

Address: 0x428001A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	F0TD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	F0TD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	F0TD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	F0TD [31:24]							

Bits	Name	Description
31 : 0	F0TD	When enabled (F0TPE=1) read data from MRAM at location FnTA. This register can have a read side effect if the following conditions are met: - M_TTCAN not being reconfigured (CCCR.CCE=0) - FIFO Top Pointer logic is enabled (FnTPE=1) - FIFO is not empty (FnFL!=0) The read side effect is as follows: - if FnMWC pointed to the last word of the message (as indicated by FnDS) then the corresponding message index (FnGI) is automatically acknowledge by a write to FnAI - FnMWC is incremented (or restarted if FnMWC pointed to the last word of the message) - the FIFO top address FnTA is incremented (with FIFO wrap around) When this logic is disabled (F0TPE=0) a Read from this register returns undefined data. Default Value: Undefined

17.1.67 CANFD0_CH0_RXFTOP1_STAT

Receive FIFO 1 Top Status

Address: 0x428001B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	F1TA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	F1TA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	F1TA	See F0TA description Default Value: 0

17.1.68 CANFD0_CH0_RXFTOP1_DATA

Receive FIFO 1 Top Data

Address: 0x428001B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	F1TD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	F1TD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	F1TD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	F1TD [31:24]							

Bits	Name	Description
31 : 0	F1TD	See F0TD description Default Value: Undefined

17.1.69 CANFD0_CTL

Global CAN control register

Address: 0x42801000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						STOP_REQ [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	STOP_REQ	Clock Stop Request for each TTCAN IP . The m_ttcan_clkstop_req of each TTCAN IP is directly driven by these bits. Default Value: 0

17.1.70 CANFD0_STATUS

Global CAN status register

Address: 0x42801004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	
HW Access	None						RW	
Name	None [7:2]						STOP_ACK [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	STOP_ACK	Clock Stop Acknowledge for each TTCAN IP. These bits are directly driven by m_ttcan_clkstop_ack of each TTCAN IP. When this bit is set the corresponding TTCAN IP clocks will be gated off, except HCLK will enabled for each AHB write Default Value: 0

17.1.71 CANFD0_INTR0_CAUSE

Consolidated interrupt0 cause register

Address: 0x42801010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	
HW Access	None						RW	
Name	None [7:2]						INT0 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	INT0	Show pending m_ttcan_int0 of each channel Default Value: 0

17.1.72 CANFD0_INTR1_CAUSE

Consolidated interrupt1 cause register

Address: 0x42801014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	
HW Access	None						RW	
Name	None [7:2]						INT1 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	INT1	Show pending m_ttcan_int1 of each channel Default Value: 0

17.1.73 CANFD0_TS_CTL

Time Stamp control register

Address: 0x42801020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PRESCALE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PRESCALE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	Counter enable bit 0 = Count disabled. Stop counting up and keep the counter value 1 = Count enabled. Start counting up from the current value Default Value: 0
15 : 0	PRESCALE	Time Stamp counter prescale value. When enabled divide the Host clock (HCLK) by PRESCALE+1 to create Time Stamp clock ticks. Default Value: 0

17.1.74 CANFD0_TS_CNT

Time Stamp counter value

Address: 0x42801024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	VALUE	The counter value of the Time Stamp Counter. When enabled this counter will count Time Stamp clock ticks from the pre-scaler. When written this counter and the pre-scaler will reset to 0 (write data is ignored). Default Value: 0

18 Coordinate Rotation Digital Computer (CORDIC) registers

This section discusses the CORDIC registers. It lists all the registers in mapping tables, in address order.

18.1 Register details

Register	Address	Description
MXCORDIC_1_0_CTL	0x42240000	
MXCORDIC_1_0_ID	0x42240008	Module Identification Register
MXCORDIC_1_0_INTR	0x42240010	Interrupt Cause Register
MXCORDIC_1_0_INTR_SET	0x42240014	Interrupt Set Register
MXCORDIC_1_0_INTR_MASK	0x42240018	Interrupt Mask Register
MXCORDIC_1_0_INTR_MASKED	0x4224001C	Interrupt Masked Register
MXCORDIC_1_0_KEEP	0x42240040	CORDIC Keep Register
MXCORDIC_1_0_CON	0x42240044	CORDIC Control Register
MXCORDIC_1_0_CORDX	0x42240048	CORDIC X Data Register
MXCORDIC_1_0_CORDY	0x4224004C	CORDIC Y Data Register
MXCORDIC_1_0_CORDZ	0x42240050	CORDIC Z Data Register
MXCORDIC_1_0_CORRX	0x42240054	CORDIC X Result Register
MXCORDIC_1_0_CORRY	0x42240058	CORDIC Y Result Register
MXCORDIC_1_0_CORRZ	0x4224005C	CORDIC Z Result Register
MXCORDIC_1_0_STAT	0x42240060	CORDIC Status Register
MXCORDIC_1_0_START_CMD	0x42240064	CORDIC Start Command Register

18.1.1 MXCORDIC_1_0_CTL

Module Enables/Disables Register

Address: 0x42240000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	Enables/Disables IP Default Value: 0x0

18.1.2 MXCORDIC_1_0_ID

Module Identification Register

Address: 0x42240008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	MOD_REV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	MOD_TYPE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	MOD_NUMBER [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	MOD_NUMBER [31:24]							

Bits	Name	Description
31 : 16	MOD_NUMBER	Module Number Value - MOD_NUMBER Default Value: 0xDCB2
15 : 8	MOD_TYPE	Module Type - MOD_TYPE Default Value: 0xC0
7 : 0	MOD_REV	Module Revision Number - MOD_REV Default Value: 0x1

18.1.3 MXCORDIC_1_0_INTR

Interrupt Cause Register

Address: 0x42240010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	None	
HW Access	None				R	R	None	
Name	None [7:4]				CDERR	CDEOC	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	CDERR	CORDIC Error Event Flag - CDERR Default Value: 0x0
2	CDEOC	CORDIC End of Calculation Event Flag - CDEOC Default Value: 0x0

18.1.4 MXCORDIC_1_0_INTR_SET

Interrupt Set Register

Address: 0x42240014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S	RW1S	None	
HW Access	None				R	R	None	
Name	None [7:4]				CDERR	CDEOC	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	CDERR	CORDIC Error Event Flag Set - CDERR Default Value: 0x0
2	CDEOC	CORDIC Event Flag Set - CDEOC Default Value: 0x0

18.1.5 MXCORDIC_1_0_INTR_MASK

Interrupt Mask Register

Address: 0x42240018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	None	
HW Access	None				R	R	None	
Name	None [7:4]				CDERR	CDEOC	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	CDERR	CORDIC Error Interrupt Mask - CDERR Default Value: 0x0
2	CDEOC	CORDIC End of Calculation Interrupt Mask- CDEOC Default Value: 0x0

18.1.6 MXCORDIC_1_0_INTR_MASKED

Interrupt Masked Register

Address: 0x4224001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	None	
HW Access	None				W	W	None	
Name	None [7:4]				CDERR	CDEOC	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	CDERR	CORDIC Error Interrupt Masked - CDERR Default Value: 0x0
2	CDEOC	CORDIC End of Calculation Interrupt Masked- CDEOC Default Value: 0x0

18.1.7 MXCORDIC_1_0_KEEP

CORDIC Keep Register

Address: 0x42240040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	None				
HW Access	R	R	R	None				
Name	KEEPZ	KEEPY	KEEPX	None [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	KEEPZ	Last Z Result as Initial Data for New Calculation - KEEPZ Default Value: 0x0
6	KEEPY	Last Y Result as Initial Data for New Calculation - KEEPY Default Value: 0x0
5	KEEPX	Last X Result as Initial Data for New Calculation - KEEPX Default Value: 0x0

18.1.8 MXCORDIC_1_0_CON

CORDIC Control Register

Address: 0x42240044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW	RW	RW		None
HW Access	R		R	R	R	R		None
Name	MPS [7:6]		X_USIGN	ST_MODE	ROTVEC	MODE [2:1]		None

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					R		
Name	None [15:11]					N_ITER [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10 : 8	N_ITER	Number of CORDIC iterations divided by 4 Default Value: 0x0 **0x1: N_ITER_4 :** **0x2: N_ITER_8 :** **0x3: N_ITER_12 :** **0x4: N_ITER_16 :** **0x5: N_ITER_20 :** **0x6: N_ITER_24 :** **0x7: N_ITER_28 :**
7 : 6	MPS	X and Y Magnitude Prescaler - MPS Default Value: 0x1 **0x0: DIVIDE_BY_1 :** **0x1: DIVIDE_BY_2 :**

18.1.8 MXCORDIC_1_0_CON (continued)

		0x2: DIVIDE_BY_4 : **0x3: Reserved :**
5	X_USIGN	Result Data Format for X in Circular Vectoring Mode - X_USIGN Default Value: 0x1 **0x0: SIGNED :** **0x1: UNSIGNED :**
4	ST_MODE	Start Method - ST_MODE Default Value: 0x0 **0x0: AUTO :** Operation starts with write into CORDZ register **0x1: ST :** Operation starts with write into START_CMD register
3	ROTVEC	Rotation Vectoring Selection - ROTVEC Default Value: 0x0 **0x0: VECTORING :** **0x1: ROTATION :**
2 : 1	MODE	Operating Mode - MODE Default Value: 0x1 **0x0: Reserved :** **0x1: CIRCULAR :** **0x2: Reserved :** **0x3: HYPERBOLIC :**

18.1.9 MXCORDIC_1_0_CORDX

CORDIC X Data Register

Address: 0x42240048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 8	DATA	Initial X Parameter Data - DATA Default Value: 0x0

18.1.10 MXCORDIC_1_0_CORDY

CORDIC Y Data Register

Address: 0x4224004C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 8	DATA	Initial Y Parameter Data - DATA Default Value: 0x0

18.1.11 MXCORDIC_1_0_CORDZ

CORDIC Z Data Register

Address: 0x42240050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 8	DATA	Initial Z Parameter Data - DATA Default Value: 0x0

18.1.12 MXCORDIC_1_0_CORRX

CORDIC X Result Register

Address: 0x42240054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	RESULT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	RESULT [31:24]							

Bits	Name	Description
31 : 8	RESULT	X Calculation Result - RESULT Default Value: 0x0

18.1.13 MXCORDIC_1_0_CORRY

CORDIC Y Result Register

Address: 0x42240058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	RESULT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	RESULT [31:24]							

Bits	Name	Description
31 : 8	RESULT	Y Calculation Result - RESULT Default Value: 0x0

18.1.14 MXCORDIC_1_0_CORRZ

CORDIC Z Result Register

Address: 0x4224005C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	RESULT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	RESULT [31:24]							

Bits	Name	Description
31 : 8	RESULT	Z Calculation Result - RESULT Default Value: 0x0

18.1.15 MXCORDIC_1_0_STAT

CORDIC Status Register

Address: 0x42240060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							BSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	BSY	Busy Indication - BSY Default Value: 0x0

18.1.16 MXCORDIC_1_0_START_CMD

CORDIC Start Command Register

Address: 0x42240064

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							ST

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	ST	Start Calculation Set - ST Default Value: 0x0

19 Cryptographic Accelerator registers (CRYPTOLITE)

This section discusses the CRYPTOLITE registers. It lists all the registers in mapping tables, in address order.

19.1 Register details

Register	Address	Description
CRYPTOLITE_CTL	0x42230000	Control
CRYPTOLITE_STATUS	0x42230004	Status
CRYPTOLITE_AES_DESCR	0x42230040	AES descriptor pointer
CRYPTOLITE_VU_DESCR	0x42230080	VU descriptor pointer
CRYPTOLITE_SHA_DESCR	0x422300C0	SHA descriptor pointer
CRYPTOLITE_INTR_ERROR	0x422300F0	Error interrupt
CRYPTOLITE_INTR_ERROR_SET	0x422300F4	Error interrupt set
CRYPTOLITE_INTR_ERROR_SET	0x422300F8	Error interrupt mask
CRYPTOLITE_INTR_ERROR_MASKED	0x422300FC	Error interrupt masked
CRYPTOLITE_TRNG_CTL0	0x42230100	TRNG control 0
CRYPTOLITE_TRNG_CTL1	0x42230104	TRNG control 1
CRYPTOLITE_TRNG_STATUS	0x4223010C	TRNG status
CRYPTOLITE_TRNG_RESULT	0x42230110	TRNG result
CRYPTOLITE_TRNG_GARO_CTL	0x42230120	TRNG GARO control
CRYPTOLITE_TRNG_FIRO_CTL	0x42230124	TRNG FIRO control
CRYPTOLITE_TRNG_MON_CTL	0x42230140	TRNG monitor control
CRYPTOLITE_TRNG_MON_RC_CTL	0x42230150	TRNG monitor RC control
CRYPTOLITE_TRNG_MON_RC_STATUS0	0x42230158	TRNG monitor RC status 0
CRYPTOLITE_TRNG_MON_RC_STATUS1	0x4223015C	TRNG monitor RC status 1
CRYPTOLITE_TRNG_MON_AP_CTL	0x42230160	TRNG monitor AP control
CRYPTOLITE_TRNG_MON_AP_STATUS0	0x42230168	TRNG monitor AP status 0
CRYPTOLITE_TRNG_MON_AP_STATUS1	0x4223016C	TRNG monitor AP status 1
CRYPTOLITE_INTR_TRNG	0x422301F0	TRNG interrupt
CRYPTOLITE_INTR_TRNG_SET	0x422301F4	TRNG Interrupt set
CRYPTOLITE_INTR_TRNG_MASK	0x422301F8	TRNG Interrupt mask
CRYPTOLITE_INTR_TRNG_MASKED	0x422301FC	TRNG Interrupt masked

19.1.1 CRYPTOLITE_CTL

Control

Address: 0x42230000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None		R	R
HW Access	W				None		W	W
Name	PC [7:4]				None [3:2]		NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				MS [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 8	MS	Master identifier of the cryptography IP. This is a design time configurable parameter. Default Value: 14
7 : 4	PC	Protection context. This field is set with the protection context of the transaction that writes any (including possible memory holes in the IP aperture) of the CRYPTO component registers; i.e. the context is inherited from the write transaction and not specified by the transaction write data. All CRYPTO component master transactions use the PC field for the protection context. Default Value: Undefined
1	NS	Secure/on-secure access control: '0': secure. '1': non-secure. This field is set with the secure/non-secure access control of the transaction that writes any (including possible memory holes in the IP aperture) of the CRYPTO component registers; i.e. the access control is inherited from the write transaction and not specified by the transaction write data. All CRYPTO component master transactions use the NS field for the secure/non-secure access control ("hprot[4]"). Default Value: Undefined

19.1.1 CRYPTOLITE_CTL (continued)

0	P	User/privileged access control: '0': user mode. '1': privileged mode. This field is set with the user/privileged access control of the transaction that writes any (including possible memory holes in the IP aperture) of the CRYPTO component registers; i.e. the access control is inherited from the write transaction and not specified by the transaction write data. All CRYPTO component master transactions use the P field for the user/privileged access control ("hprot[1]"). Default Value: Undefined

19.1.2 CRYPTOLITE_STATUS

Status

Address: 0x42230004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	BUSY	Busy indication: '0': IP not busy. '1': IP busy (AES, SHA or VU functionality (TRNG functionality NOT included)). Default Value: 0

19.1.3 CRYPTOLITE_AES_DESCR

AES descriptor pointer

Address: 0x42230040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	RW						None	
Name	PTR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PTR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	PTR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	PTR [31:24]							

Bits	Name	Description
31 : 2	PTR	AES descriptor pointer. The descriptor points to a structure with 32-bit words: Word 0: Pointer to a 128-bit AES key. Word 1: Pointer to a 128-bit source/plaintext. Word 2: Pointer to a 128-bit destination/ciphertext. A write to this register automatically starts a 128-bit AES encryption in ECB mode. The write ONLY takes effect when the IP is NOT busy (STATUS.BUSY is '0'). The write will be made pending/blocked as long as the IP is busy. Note: the pointers must be 4B aligned. Note: HW updates this field when the AES engine is busy. Default Value: Undefined

19.1.4 CRYPTOLITE_VU_DESCR

VU descriptor pointer

Address: 0x42230080

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	RW						None	
Name	PTR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PTR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	PTR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	PTR [31:24]							

Bits	Name	Description
31 : 2	PTR	VU descriptor pointer. The descriptor points to a structure with 32-bit words: Word 0: Control word. Specifies operand size in 32-bit word multiples. - WORD[7:0]: Source operand 0 32-bit words (minus 1). - WORD[15:8]: Source operand 1 32-bit words (minus 1). - WORD[24:16]: Destination operand 32-bit words (minus 1). - WORD[31:28]: Opcode. "0": multiplication (MUL), "1": addition (ADD), "2": subtraction (SUB), "3": exclusive or (XOR), "4": binary multiplication (XMUL), "5": logical shift right by 1 (LSR1), "6": logical shift left by 1 (LSL1), "7": logical shift right (LSR), "8": conditional syubtraction (COND_-SUB). "9": move (MOV). Word 1: Pointer to source 0. Word 2: Pointer to source 1. Word 3: Pointer to destination. A write to this register automatically starts a VU operation. The write ONLY takes effect when the IP is NOT busy (STATUS.BUSY is '0'). The write will be made pending/blocked as long as the IP is busy. Note: the pointers must be 4B aligned. Note: HW updates this field when the VU engine is busy. Default Value: Undefined

19.1.5 CRYPTOLITE_SHA_DESCR

SHA descriptor pointer

Address: 0x422300C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	RW						None	
Name	PTR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PTR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	PTR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	PTR [31:24]							

Bits	Name	Description
31 : 2	PTR	SHA-256 descriptor pointer. The descriptor points to a structure with 32-bit words: For message schedule function: Word 0: Control word. - WORD0[28]: '0' for message schedule function. Word 1: Pointer to 512 b message chunk (input). Word 2: Pointer to 64 * 32 b word message schedule array (output). For process function: Word 0: Control word. - WORD0[28]: '1' for process function. Word 1: Pointer to 8 * 32 b word current hash value (input) and new hash value (output). Word 2: Pointer to 64 * 32 b word message schedule array (input). A write to this register automatically starts a SHA-256 operation. The write ONLY takes effect when the IP is NOT busy (STATUS.BUSY is '0'). The write will be made pending/blocked as long as the IP is busy. Note: the pointers must be 32-bit word aligned. Note: HW updates this field when the SHA-256 engine is busy. Default Value: Undefined

19.1.6 CRYPTOLITE_INTR_ERROR

Error interrupt

Address: 0x422300F0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [7:1]							BUS_ER-ROR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	BUS_ERROR	AHB-Lite master interface bus error or ECC error. Note that the IP terminates its AES, SHA or VU functionality when it detects an error. Note: The error is sticky. This allows SW to check for an error after a series of operations, rather than checking after every individual operation. Default Value: 0

19.1.7 CRYPTOLITE_INTR_ERROR_SET

Error interrupt set

Address: 0x422300F4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							A
Name	None [7:1]							BUS_ER-ROR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	BUS_ERROR	Write this field with '1' to set corresponding INTR_ERROR field to '1' (a write of '0' has no effect). Default Value: 0

19.1.8 CRYPTOLITE_INTR_ERROR_MASK

Error interrupt mask

Address: 0x422300F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							BUS_ER-ROR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	BUS_ERROR	Mask for corresponding field in INTR_ERROR register. Default Value: 0

19.1.9 CRYPTOLITE_INTR_ERROR_MASKED

Error interrupt masked

Address: 0x422300FC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							BUS_ER-ROR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	BUS_ERROR	Logical and of corresponding INTR_ERROR and INTR_ERROR_MASK fields. Default Value: 0

19.1.10 CRYPTOLITE_TRNG_CTL0

TRNG control 0

Address: 0x42230100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SAMPLE_CLOCK_DIV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RED_CLOCK_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INIT_DELAY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW	RW	None		RW	RW
HW Access	None		R	R	None		R	R
Name	None [31:30]		STOP_ON_RC_DETECT	STOP_ON_AP_DETECT	None [27:26]		FEEDBACK_EN	VON_NEUMAN_N_CORR

Bits	Name	Description
29	STOP_ON_RC_DETECT	Specifies if TRNG functionality is stopped on a repetition count test detection (when HW sets INTR_ERROR.TRNG_RC_DETECT to '1'): '0': Functionality is NOT stopped. '1': Functionality is stopped (TRNG_CTL1 fields are set to '0' by HW). The DAS bitstream is set to '0'. Default Value: 1
28	STOP_ON_AP_DETECT	Specifies if TRNG functionality is stopped on an adaptive proportion test detection (when HW sets INTR_ERROR.TRNG_AP_DETECT to '1'): '0': Functionality is NOT stopped. '1': Functionality is stopped (TRNG_CTL1 fields are set to '0' by HW). The DAS bitstream is set to '0'. Default Value: 1
25	FEEDBACK_EN	Specifies if the feedback of the reducution state is enabled: '0': Disabled. '1': Enabled. Note: This field is added in the "mxcryptolite" IP to address CDT#337111, in which it was observed that the reduction state feedback reduces the effectiveness of the "von Neumann corrector". The default value is '1' to provide backward compatibility. Default Value: 1

19.1.10 CRYPTOLITE_TRNG_CTL0 (continued)

24	VON_NEUMANN_CORR	Specifies if the "von Neumann corrector" is disabled or enabled: '0': disabled. '1': enabled. The "von Neumann corrector" post-processes the reduced bits to remove a '0' or '1' bias. The corrector operates on reduced bit pairs ("oldest bit, newest bit"): "00": no bit is produced. "01": '0' bit is produced (oldest bit). "10": '1' bit is produced (oldest bit). "11": no bit is produced. Note that the corrector produces bits at a random pace and at a frequency that is 1/4 of the reduced bit frequency (reduced bits are processed in pairs, and half of the pairs do NOT produce a bit). Default Value: 1
23 : 16	INIT_DELAY	Specifies an initialization delay: number of removed/dropped samples before reduced bits are generated. This field should be programmed in the range [1, 255]. After starting the oscillators, at least the first 2 samples should be removed/dropped to clear the state of internal synchronizers. In addition, it is advised to drop at least the second 2 samples from the oscillators (to circumvent the semi-predictable oscillator startup behavior). This result in the default field value of "3". Field encoding is as follows: "0": 1 sample is dropped. "1": 2 samples are dropped. ... "255": 256 samples are dropped. The INTR.INITIALIZED interrupt cause is set to '1', when the initialization delay is passed. Default Value: 3
15 : 8	RED_CLOCK_DIV	Specifies the clock divider that is used to produce reduced bits. "0": 1 reduced bit is produced for each sample. "1": 1 reduced bit is produced for each 2 samples. ... "255": 1 reduced bit is produced for each 256 samples. The reduced bits are considered random bits and shifted into TRNG_RESULT.DATA. Default Value: 0
7 : 0	SAMPLE_CLOCK_DIV	Specifies the clock divider that is used to sample oscillator data. This clock divider is wrt. The IP clock. "0": sample clock is the IP clock. "1": sample clock is the IP clock divided by 2. ... "255": sample clock is the IP clock divided by 256. Default Value: 0

19.1.11 CRYPTOLITE_TRNG_CTL1

TRNG control 1

Address: 0x42230104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [7:6]		FIRO31_EN	FIRO15_EN	GA-RO31_EN	GA-RO15_EN	RO15_EN	RO11_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	FIRO31_EN	FW sets this field to '1' to enable the programmable Fibonacci ring oscillator with up to 31 inverters. The TRNG_FIRO_CTL register specifies the programmable polynomial. Default Value: 0
4	FIRO15_EN	FW sets this field to '1' to enable the fixed Fibonacci ring oscillator with 15 inverters. Default Value: 0
3	GARO31_EN	FW sets this field to '1' to enable the programmable Galois ring oscillator with up to 31 inverters. The TRNG_GARO_CTL register specifies the programmable polynomial. Default Value: 0
2	GARO15_EN	FW sets this field to '1' to enable the fixed Galois ring oscillator with 15 inverters. Default Value: 0
1	RO15_EN	FW sets this field to '1' to enable the ring oscillator with 15 inverters. Default Value: 0
0	RO11_EN	FW sets this field to '1' to enable the ring oscillator with 11 inverters. Default Value: 0

19.1.12 CRYPTOLITE_TRNG_STATUS

TRNG status

Address: 0x4223010C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							INITIAL-IZED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	INITIALIZED	Reflects the state of the true random number generator: '0': Not initialized (TRNG_CTL0.INIT_DELAY has NOT passed). '1': Initialized (TRNG_CTL0.INIT_DELAY has passed). Default Value: 0

19.1.13 CRYPTOLITE_TRNG_RESULT

TRNG result

Address: 0x42230110

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Generated 32-bit true random number. The INTR.DATA_AVAILABLE interrupt cause is activated when the number is generated. Default Value: Undefined

19.1.14 CRYPTOLITE_TRNG_GARO_CTL

TRNG GARO control

Address: 0x42230120

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW						
HW Access	None	R						
Name	None	POLYNOMIAL [30:24]						

Bits	Name	Description
30 : 0	POLYNOMIAL	Polynomial for programmable Galois ring oscillator. The polynomial is represented WITHOUT the high order bit (this bit is always assumed '1'). The polynomial should be aligned such that the more significant bits (bit 30 and down) contain the polynomial and the less significant bits (bit 0 and up) contain padding '0's. Note: Default value per GESC#113. Default Value: 0x21F81910

19.1.15 CRYPTOLITE_TRNG_FIRO_CTL

TRNG FIRO control

Address: 0x42230124

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW						
HW Access	None	R						
Name	None	POLYNOMIAL [30:24]						

Bits	Name	Description
30 : 0	POLYNOMIAL	Polynomial for programmable Fibonacci ring oscillator. The polynomial is represented WITHOUT the high order bit (this bit is always assumed '1'). The polynomial should be aligned such that the more significant bits (bit 30 and down) contain the polynomial and the less significant bits (bit 0 and up) contain padding '0's. Note: Default value per GESC#113. Default Value: 0x696F0221

19.1.16 CRYPTOLITE_TRNG_MON_CTL

TRNG monitor control

Address: 0x42230140

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						BITSTREAM_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						RW1C	RW1C
Name	None [15:10]						RC	AP

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	RC	Repetition count (RC) test enable: '0': Disabled. '1': Enabled. On a RC detection, HW sets this field to '0' and sets INTR_ERROR.TRNG_RC_DETECT to '1. Default Value: 0
8	AP	Adaptive proportion (AP) test enable: '0': Disabled. '1': Enabled. On a AP detection, HW sets this field to '0' and sets INTR_ERROR.TRNG_AP_DETECT to '1. Default Value: 0
1 : 0	BITSTREAM_SEL	Selection of the bitstream: "0": DAS bitstream. "1": RED bitstream. "2": TR bitstream. "3": Undefined. Default Value: 2

19.1.17 CRYPTOLITE_TRNG_MON_RC_CTL

TRNG monitor RC control

Address: 0x42230150

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CUTOFF_COUNT8 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CUTOFF_COUNT8	Cutoff count (legal range is [1, 255]): "0": Illegal. "1": 1 repetition. ... "255": 255 repetitions. Default Value: 255

19.1.18 CRYPTOLITE_TRNG_MON_RC_STATUS0

TRNG monitor RC status 0

Address: 0x42230158

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							BIT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	BIT	Current active bit value: '0': '0'. '1': '1'. This field is only valid when TRNG_MON_RC_STATUS1.REP_COUNT is NOT equal to "0". Default Value: 0

19.1.19 CRYPTOLITE_TRNG_MON_RC_STATUS1

TRNG monitor RC status 1

Address: 0x4223015C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	REP_COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	REP_COUNT	Number of repetitions of the current active bit counter: "0": 0 repetitions. ... "255": 255 repetitions. Default Value: 0

19.1.20 CRYPTOLITE_TRNG_MON_AP_CTL

TRNG monitor AP control

Address: 0x42230160

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CUTOFF_COUNT16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CUTOFF_COUNT16 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	WINDOW_SIZE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	WINDOW_SIZE [31:24]							

Bits	Name	Description
31 : 16	WINDOW_SIZE	Window size (minus 1) : "0": 1 bit. ... "65535": 65536 bits. Default Value: 65535
15 : 0	CUTOFF_COUNT16	Cutoff count (legal range is [1, 65535]). "0": Illegal. "1": 1 occurrence. ... "65535": 65535 occurrences. Default Value: 65535

19.1.21 CRYPTOLITE_TRNG_MON_AP_STATUS0

TRNG monitor AP status 0

Address: 0x42230168

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							BIT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	BIT	Current active bit value: '0': '0'. '1': '1'. This field is only valid when TRNG_MON_AP_STATUS1.OCC_COUNT is NOT equal to "0". Default Value: 0

19.1.22 CRYPTOLITE_TRNG_MON_AP_STATUS1

TRNG monitor AP status 1

Address: 0x4223016C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	OCC_COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	OCC_COUNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	WINDOW_INDEX [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	WINDOW_INDEX [31:24]							

Bits	Name	Description
31 : 16	WINDOW_INDEX	Counter to keep track of the current index in the window (counts from "0" to TRNG_MON_AP_CTL.WINDOW_SIZE to "0"). Default Value: 0
15 : 0	OCC_COUNT	Number of occurrences of the current active bit counter: "0": 0 occurrences ... "65535": 65535 occurrences Default Value: 0

19.1.23 CRYPTOLITE_INTR_TRNG

TRNG interrupt

Address: 0x422301F0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [7:4]				RC_DE-TECT	AP_DE-TECT	DATA_AVAI LABLE	INITIAL-IZED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	RC_DETECT	This interrupt cause is activated (HW sets the field to '1') when the TRNG monitor detects an "repetition count" error. Default Value: 0
2	AP_DETECT	This interrupt cause is activated (HW sets the field to '1') when the TRNG monitor detects an "adaptive proportion" error. Default Value: 0
1	DATA_AVAILABLE	This interrupt cause is activated (HW sets the field to '1') when 32 bits of TRNG data becomes available in TRNG_RESULT. Default Value: 0
0	INITIALIZED	This interrupt cause is activated (HW sets the field to '1') when the TRNG is initialized. Default Value: 0

19.1.24 CRYPTOLITE_INTR_TRNG_SET

TRNG Interrupt set

Address: 0x422301F4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [7:4]				RC_DE-TECT	AP_DE-TECT	DATA_AVAI LABLE	INITIAL-IZED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	RC_DETECT	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
2	AP_DETECT	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
1	DATA_AVAILABLE	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
0	INITIALIZED	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0

19.1.25 CRYPTOLITE_INTR_TRNG_MASK

TRNG Interrupt mask

Address: 0x422301F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				RC_DE-TECT	AP_DE-TECT	DATA_AVAI LABLE	INITIAL-IZED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	RC_DETECT	Mask bit for corresponding field in interrupt request register. Default Value: 0
2	AP_DETECT	Mask bit for corresponding field in interrupt request register. Default Value: 0
1	DATA_AVAILABLE	Mask bit for corresponding field in interrupt request register. Default Value: 0
0	INITIALIZED	Mask bit for corresponding field in interrupt request register. Default Value: 0

19.1.26 CRYPTOLITE_INTR_TRNG_MASKED

TRNG Interrupt masked

Address: 0x422301FC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				RC_DE-TECT	AP_DE-TECT	DATA_AVAI LABLE	INITIAL-IZED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	RC_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
2	AP_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
1	DATA_AVAILABLE	Logical and of corresponding request and mask bits. Default Value: 0
0	INITIALIZED	Logical and of corresponding request and mask bits. Default Value: 0

20 High Performance Programmable Analog Sub-System (HPPASS) registers

This section discusses the HPPASS registers. It lists all the registers in mapping tables, in address order.

20.1 Register details

Register	Address	Description
HPPASS_SARADC_CALOFFST0	0x42B70010	SARADC Offset Calibration Values
HPPASS_SARADC_CALOFFST1	0x42B70014	SARADC Offset Calibration Values. See HPPASS_SARADC_CALOFFST0 for the details of bit fields.
HPPASS_SARADC_CALOFFST2	0x42B70018	SARADC Offset Calibration Values. See HPPASS_SARADC_CALOFFST0 for the details of bit fields.
HPPASS_SARADC_CALOFFST3	0x42B7001C	SARADC Offset Calibration Values. See HPPASS_SARADC_CALOFFST0 for the details of bit fields.
HPPASS_SARADC_CALLIN0	0x42B70020	SARADC Linearity Calibration Values
HPPASS_SARADC_CALLIN1	0x42B70024	SARADC Linearity Calibration Values. See HPPASS_SARADC_CALLIN0 for the details of bit fields.
HPPASS_SARADC_CALLIN2	0x42B70028	SARADC Linearity Calibration Values. See HPPASS_SARADC_CALLIN0 for the details of bit fields.
HPPASS_SARADC_CALLIN3	0x42B7002C	SARADC Linearity Calibration Values. See HPPASS_SARADC_CALLIN0 for the details of bit fields.
HPPASS_SARADC_CALLIN4	0x42B70030	SARADC Linearity Calibration Values. See HPPASS_SARADC_CALLIN0 for the details of bit fields.
HPPASS_SARADC_CALLIN5	0x42B70034	SARADC Linearity Calibration Values. See HPPASS_SARADC_CALLIN0 for the details of bit fields.
HPPASS_SARADC_CALLIN6	0x42B70038	SARADC Linearity Calibration Values. See HPPASS_SARADC_CALLIN0 for the details of bit fields.
HPPASS_SARADC_CALLIN7	0x42B7003C	SARADC Linearity Calibration Values. See HPPASS_SARADC_CALLIN0 for the details of bit fields.
HPPASS_SARADC_CALLIN8	0x42B70040	SARADC Linearity Calibration Values. See HPPASS_SARADC_CALLIN0 for the details of bit fields.
HPPASS_SARADC_CALLIN9	0x42B70044	SARADC Linearity Calibration Values. See HPPASS_SARADC_CALLIN0 for the details of bit fields.
HPPASS_SARADC_CALLIN10	0x42B70048	SARADC Linearity Calibration Values. See HPPASS_SARADC_CALLIN0 for the details of bit fields.
HPPASS_SARADC_CALLIN11	0x42B7004C	SARADC Linearity Calibration Values. See HPPASS_SARADC_CALLIN0 for the details of bit fields.
HPPASS_SARADC_CALLIN12	0x42B70050	SARADC Linearity Calibration Values. See HPPASS_SARADC_CALLIN0 for the details of bit fields.

High Performance Programmable Analog Sub-System (HPPASS) registers

Register	Address	Description
HPPASS_SARADC_CALLIN13	0x42B70054	SARADC Linearity Calibration Values. See HPPASS_SARADC_CALLIN0 for the details of bit fields.
HPPASS_SARADC_CALLIN14	0x42B70058	SARADC Linearity Calibration Values. See HPPASS_SARADC_CALLIN0 for the details of bit fields.
HPPASS_SARADC_CALLIN15	0x42B7005C	SARADC Linearity Calibration Values. See HPPASS_SARADC_CALLIN0 for the details of bit fields.
HPPASS_SARADC_CALGAINC	0x42B70060	SARADC Coarse-grained Gain Calibration Values
HPPASS_SARADC_CALGAINF	0x42B70064	SARADC Fine-grained Gain Calibration Values
HPPASS_SAR_SEQ_ENTRY0	0x42B80100	SAR Sequencer Table Entries
HPPASS_SAR_SEQ_ENTRY1	0x42B80104	SAR Sequencer Table Entries. See HPPASS_SAR_SEQ_ENTRY0 for the details of bit fields.
HPPASS_SAR_SEQ_ENTRY2	0x42B80108	SAR Sequencer Table Entries. See HPPASS_SAR_SEQ_ENTRY0 for the details of bit fields.
HPPASS_SAR_SEQ_ENTRY3	0x42B8010C	SAR Sequencer Table Entries. See HPPASS_SAR_SEQ_ENTRY0 for the details of bit fields.
HPPASS_SAR_SEQ_ENTRY4	0x42B80110	SAR Sequencer Table Entries. See HPPASS_SAR_SEQ_ENTRY0 for the details of bit fields.
HPPASS_SAR_SEQ_ENTRY5	0x42B80114	SAR Sequencer Table Entries. See HPPASS_SAR_SEQ_ENTRY0 for the details of bit fields.
HPPASS_SAR_SEQ_ENTRY6	0x42B80118	SAR Sequencer Table Entries. See HPPASS_SAR_SEQ_ENTRY0 for the details of bit fields.
HPPASS_SAR_SEQ_ENTRY7	0x42B8011C	SAR Sequencer Table Entries. See HPPASS_SAR_SEQ_ENTRY0 for the details of bit fields.
HPPASS_SAR_ENTRY_MUX_SEL_ALIAS0	0x42B80200	SAR Sequencer MUX select alias registers
HPPASS_SAR_ENTRY_MUX_SEL_ALIAS1	0x42B80204	SAR Sequencer MUX select alias registers. See HPPASS_SAR_ENTRY_MUX_SEL_ALIAS0 for the details of bit fields.
HPPASS_SAR_ENTRY_MUX_SEL_ALIAS2	0x42B80208	SAR Sequencer MUX select alias registers. See HPPASS_SAR_ENTRY_MUX_SEL_ALIAS0 for the details of bit fields.
HPPASS_SAR_ENTRY_MUX_SEL_ALIAS3	0x42B8020C	SAR Sequencer MUX select alias registers. See HPPASS_SAR_ENTRY_MUX_SEL_ALIAS0 for the details of bit fields.
HPPASS_SAR_ENTRY_MUX_SEL_ALIAS4	0x42B80210	SAR Sequencer MUX select alias registers. See HPPASS_SAR_ENTRY_MUX_SEL_ALIAS0 for the details of bit fields.
HPPASS_SAR_ENTRY_MUX_SEL_ALIAS5	0x42B80214	SAR Sequencer MUX select alias registers. See HPPASS_SAR_ENTRY_MUX_SEL_ALIAS0 for the details of bit fields.
HPPASS_SAR_ENTRY_MUX_SEL_ALIAS6	0x42B80218	SAR Sequencer MUX select alias registers. See HPPASS_SAR_ENTRY_MUX_SEL_ALIAS0 for the details of bit fields.

High Performance Programmable Analog Sub-System (HPPASS) registers

Register	Address	Description
HPPASS_SAR_ENTRY_MUX_SEL_ALIAS7	0x42B8021C	SAR Sequencer MUX select alias registers. See HPPASS_SAR_ENTRY_MUX_SEL_ALIAS0 for the details of bit fields.
HPPASS_SAR_CFG_CTRL	0x42B80400	Control register
HPPASS_SAR_CFG_SAMP_EN	0x42B80404	Sampler static enable configuration register
HPPASS_SAR_CFG_SAMP_GAIN	0x42B80408	Sampler gain configuration register
HPPASS_SAR_CFG_SAMPLE_TIME0	0x42B80410	Sample Time configuration register
HPPASS_SAR_CFG_SAMPLE_TIME1	0x42B80414	Sample Time configuration register. See HPPASS_SAR_CFG_SAMPLE_TIME0 for the details of bit fields.
HPPASS_SAR_CFG_SAMPLE_TIME2	0x42B80418	Sample Time configuration register. See HPPASS_SAR_CFG_SAMPLE_TIME0 for the details of bit fields.
HPPASS_SAR_CFG_FIR_CFG0	0x42B80420	FIR configuration register
HPPASS_SAR_CFG_FIR_CFG1	0x42B80424	FIR configuration register. See HPPASS_SAR_CFG_FIR_CFG0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_CFG0	0x42B80430	SAR Channel configuration register
HPPASS_SAR_CFG_CHAN_CFG1	0x42B80434	SAR Channel configuration register. See HPPASS_SAR_CFG_CHAN_CFG0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_CFG2	0x42B80438	SAR Channel configuration register. See HPPASS_SAR_CFG_CHAN_CFG0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_CFG3	0x42B8043C	SAR Channel configuration register. See HPPASS_SAR_CFG_CHAN_CFG0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_CFG4	0x42B80440	SAR Channel configuration register. See HPPASS_SAR_CFG_CHAN_CFG0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_CFG5	0x42B80444	SAR Channel configuration register. See HPPASS_SAR_CFG_CHAN_CFG0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_CFG6	0x42B80448	SAR Channel configuration register. See HPPASS_SAR_CFG_CHAN_CFG0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_CFG7	0x42B8044C	SAR Channel configuration register. See HPPASS_SAR_CFG_CHAN_CFG0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_CFG8	0x42B80450	SAR Channel configuration register. See HPPASS_SAR_CFG_CHAN_CFG0 for the details of bit fields.

High Performance Programmable Analog Sub-System (HPPASS) registers

Register	Address	Description
HPPASS_SAR_CFG_CHAN_CFG9	0x42B80454	SAR Channel configuration register. See HPPASS_SAR_CFG_CHAN_CFG0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_CFG10	0x42B80458	SAR Channel configuration register. See HPPASS_SAR_CFG_CHAN_CFG0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_CFG11	0x42B8045C	SAR Channel configuration register. See HPPASS_SAR_CFG_CHAN_CFG0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_CFG12	0x42B80460	SAR Channel configuration register. See HPPASS_SAR_CFG_CHAN_CFG0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_CFG13	0x42B80464	SAR Channel configuration register. See HPPASS_SAR_CFG_CHAN_CFG0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_CFG14	0x42B80468	SAR Channel configuration register. See HPPASS_SAR_CFG_CHAN_CFG0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_CFG15	0x42B8046C	SAR Channel configuration register. See HPPASS_SAR_CFG_CHAN_CFG0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_CFG16	0x42B80470	SAR Channel configuration register. See HPPASS_SAR_CFG_CHAN_CFG0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_CFG17	0x42B80474	SAR Channel configuration register. See HPPASS_SAR_CFG_CHAN_CFG0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_CFG18	0x42B80478	SAR Channel configuration register. See HPPASS_SAR_CFG_CHAN_CFG0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_CFG19	0x42B8047C	SAR Channel configuration register. See HPPASS_SAR_CFG_CHAN_CFG0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_CFG20	0x42B80480	SAR Channel configuration register. See HPPASS_SAR_CFG_CHAN_CFG0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_CFG21	0x42B80484	SAR Channel configuration register. See HPPASS_SAR_CFG_CHAN_CFG0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_CFG22	0x42B80488	SAR Channel configuration register. See HPPASS_SAR_CFG_CHAN_CFG0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_CFG23	0x42B8048C	SAR Channel configuration register. See HPPASS_SAR_CFG_CHAN_CFG0 for the details of bit fields.

High Performance Programmable Analog Sub-System (HPPASS) registers

Register	Address	Description
HPPASS_SAR_CFG_CHAN_CFG24	0x42B80490	SAR Channel configuration register. See HPPASS_SAR_CFG_CHAN_CFG0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_CFG25	0x42B80494	SAR Channel configuration register. See HPPASS_SAR_CFG_CHAN_CFG0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_CFG26	0x42B80498	SAR Channel configuration register. See HPPASS_SAR_CFG_CHAN_CFG0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_CFG27	0x42B8049C	SAR Channel configuration register. See HPPASS_SAR_CFG_CHAN_CFG0 for the details of bit fields.
HPPASS_SAR_CFG_RANGE_CFG0	0x42B804B0	Range detect configuration register.
HPPASS_SAR_CFG_RANGE_CFG1	0x42B804B4	Range detect configuration register. See HPPASS_SAR_CFG_RANGE_CFG0 for the details of bit fields.
HPPASS_SAR_CFG_RANGE_CFG2	0x42B804B8	Range detect configuration register. See HPPASS_SAR_CFG_RANGE_CFG0 for the details of bit fields.
HPPASS_SAR_CFG_RANGE_CFG3	0x42B804BC	Range detect configuration register. See HPPASS_SAR_CFG_RANGE_CFG0 for the details of bit fields.
HPPASS_SAR_CFG_RANGE_CFG4	0x42B804C0	Range detect configuration register. See HPPASS_SAR_CFG_RANGE_CFG0 for the details of bit fields.
HPPASS_SAR_CFG_RANGE_CFG5	0x42B804C4	Range detect configuration register. See HPPASS_SAR_CFG_RANGE_CFG0 for the details of bit fields.
HPPASS_SAR_CFG_RANGE_CFG6	0x42B804C8	Range detect configuration register. See HPPASS_SAR_CFG_RANGE_CFG0 for the details of bit fields.
HPPASS_SAR_CFG_RANGE_CFG7	0x42B804CC	Range detect configuration register. See HPPASS_SAR_CFG_RANGE_CFG0 for the details of bit fields.
HPPASS_SAR_CFG_RANGE_LOW0	0x42B804D0	Range detect low value register.
HPPASS_SAR_CFG_RANGE_LOW1	0x42B804D4	Range detect low value register. See HPPASS_SAR_CFG_RANGE_LOW0 for the details of bit fields.
HPPASS_SAR_CFG_RANGE_LOW2	0x42B804D8	Range detect low value register. See HPPASS_SAR_CFG_RANGE_LOW0 for the details of bit fields.
HPPASS_SAR_CFG_RANGE_LOW3	0x42B804DC	Range detect low value register. See HPPASS_SAR_CFG_RANGE_LOW0 for the details of bit fields.

High Performance Programmable Analog Sub-System (HPPASS) registers

Register	Address	Description
HPPASS_SAR_CFG_RANGE_LOW4	0x42B804E0	Range detect low value register. See HPPASS_SAR_CFG_RANGE_LOW0 for the details of bit fields.
HPPASS_SAR_CFG_RANGE_LOW5	0x42B804E4	Range detect low value register. See HPPASS_SAR_CFG_RANGE_LOW0 for the details of bit fields.
HPPASS_SAR_CFG_RANGE_LOW6	0x42B804E8	Range detect low value register. See HPPASS_SAR_CFG_RANGE_LOW0 for the details of bit fields.
HPPASS_SAR_CFG_RANGE_LOW7	0x42B804EC	Range detect low value register. See HPPASS_SAR_CFG_RANGE_LOW0 for the details of bit fields.
HPPASS_SAR_CFG_RANGE_HIGH0	0x42B804F0	Range detect high value register.
HPPASS_SAR_CFG_RANGE_HIGH1	0x42B804F4	Range detect high value register. See HPPASS_SAR_CFG_RANGE_HIGH0 for the details of bit fields.
HPPASS_SAR_CFG_RANGE_HIGH2	0x42B804F8	Range detect high value register. See HPPASS_SAR_CFG_RANGE_HIGH0 for the details of bit fields.
HPPASS_SAR_CFG_RANGE_HIGH3	0x42B804FC	Range detect high value register. See HPPASS_SAR_CFG_RANGE_HIGH0 for the details of bit fields.
HPPASS_SAR_CFG_RANGE_HIGH4	0x42B80500	Range detect high value register. See HPPASS_SAR_CFG_RANGE_HIGH0 for the details of bit fields.
HPPASS_SAR_CFG_RANGE_HIGH5	0x42B80504	Range detect high value register. See HPPASS_SAR_CFG_RANGE_HIGH0 for the details of bit fields.
HPPASS_SAR_CFG_RANGE_HIGH6	0x42B80508	Range detect high value register. See HPPASS_SAR_CFG_RANGE_HIGH0 for the details of bit fields.
HPPASS_SAR_CFG_RANGE_HIGH7	0x42B8050C	Range detect high value register. See HPPASS_SAR_CFG_RANGE_HIGH0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT0	0x42B80510	Channel result register
HPPASS_SAR_CFG_CHAN_RESULT1	0x42B80514	Channel result register. See HPPASS_SAR_CFG_CHAN_RESULT0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT2	0x42B80518	Channel result register. See HPPASS_SAR_CFG_CHAN_RESULT0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT3	0x42B8051C	Channel result register. See HPPASS_SAR_CFG_CHAN_RESULT0 for the details of bit fields.

High Performance Programmable Analog Sub-System (HPPASS) registers

Register	Address	Description
HPPASS_SAR_CFG_CHAN_RESULT4	0x42B80520	Channel result register. See HPPASS_SAR_CFG_CHAN_RESULT0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT5	0x42B80524	Channel result register. See HPPASS_SAR_CFG_CHAN_RESULT0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT6	0x42B80528	Channel result register. See HPPASS_SAR_CFG_CHAN_RESULT0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT7	0x42B8052C	Channel result register. See HPPASS_SAR_CFG_CHAN_RESULT0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT8	0x42B80530	Channel result register. See HPPASS_SAR_CFG_CHAN_RESULT0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT9	0x42B80534	Channel result register. See HPPASS_SAR_CFG_CHAN_RESULT0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT10	0x42B80538	Channel result register. See HPPASS_SAR_CFG_CHAN_RESULT0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT11	0x42B8053C	Channel result register. See HPPASS_SAR_CFG_CHAN_RESULT0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT12	0x42B80540	Channel result register. See HPPASS_SAR_CFG_CHAN_RESULT0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT13	0x42B80544	Channel result register. See HPPASS_SAR_CFG_CHAN_RESULT0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT14	0x42B80548	Channel result register. See HPPASS_SAR_CFG_CHAN_RESULT0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT15	0x42B8054C	Channel result register. See HPPASS_SAR_CFG_CHAN_RESULT0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT16	0x42B80550	Channel result register. See HPPASS_SAR_CFG_CHAN_RESULT0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT17	0x42B80554	Channel result register. See HPPASS_SAR_CFG_CHAN_RESULT0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT18	0x42B80558	Channel result register. See HPPASS_SAR_CFG_CHAN_RESULT0 for the details of bit fields.

High Performance Programmable Analog Sub-System (HPPASS) registers

Register	Address	Description
HPPASS_SAR_CFG_CHAN_RESULT19	0x42B8055C	Channel result register. See HPPASS_SAR_CFG_CHAN_RESULT0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT20	0x42B80560	Channel result register. See HPPASS_SAR_CFG_CHAN_RESULT0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT21	0x42B80564	Channel result register. See HPPASS_SAR_CFG_CHAN_RESULT0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT22	0x42B80568	Channel result register. See HPPASS_SAR_CFG_CHAN_RESULT0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT23	0x42B8056C	Channel result register. See HPPASS_SAR_CFG_CHAN_RESULT0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT24	0x42B80570	Channel result register. See HPPASS_SAR_CFG_CHAN_RESULT0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT25	0x42B80574	Channel result register. See HPPASS_SAR_CFG_CHAN_RESULT0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT26	0x42B80578	Channel result register. See HPPASS_SAR_CFG_CHAN_RESULT0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT27	0x42B8057C	Channel result register. See HPPASS_SAR_CFG_CHAN_RESULT0 for the details of bit fields.
HPPASS_SAR_CFG_FIR_RESULT0	0x42B80580	FIR result register
HPPASS_SAR_CFG_FIR_RESULT1	0x42B80584	FIR result register. See HPPASS_SAR_CFG_FIR_RESULT0 for the details of bit fields.
HPPASS_SAR_CFG_RESULT_MASK	0x42B80590	Channel result mask
HPPASS_SAR_CFG_RESULT_UPDATED	0x42B80594	Channel result register status
HPPASS_SAR_CFG_RANGE_STATUS	0x42B80598	Range status register
HPPASS_SAR_CFG_SAR_STATUS	0x42B8059C	SAR status register
HPPASS_SAR_CFG_RESULT_OVERFLOW	0x42B805A0	Entry overflow status
HPPASS_SAR_CFG_ENTRY_TR_COLLISION	0x42B805A4	Entry trigger collision status
HPPASS_SAR_CFG_ENTRY_HOLD_VIOLATION	0x42B805A8	Entry hold violation status
HPPASS_SAR_CFG_ENTRY_HOLD_CNT	0x42B805AC	Entry hold violation count
HPPASS_SAR_CFG_SAR_RESULT_INTR	0x42B80600	SAR Interrupt register

High Performance Programmable Analog Sub-System (HPPASS) registers

Register	Address	Description
HPPASS_SAR_CFG_SAR_RESULT_INTR_SET	0x42B80604	SAR Interrupt request set register
HPPASS_SAR_CFG_SAR_RESULT_INTR_MASK	0x42B80608	SAR Interrupt request mask
HPPASS_SAR_CFG_SAR_RESULT_INTR_MASKED	0x42B8060C	SAR Interrupt request masked
HPPASS_SAR_CFG_SAR_RANGE_INTR	0x42B80610	SAR Range Interrupt register
HPPASS_SAR_CFG_SAR_RANGE_INTR_SET	0x42B80614	SAR Range Interrupt request set register
HPPASS_SAR_CFG_SAR_RANGE_INTR_MASK	0x42B80618	SAR Range Interrupt request mask
HPPASS_SAR_CFG_SAR_RANGE_INTR_MASKED	0x42B8061C	SAR Range Interrupt request masked
HPPASS_SAR_CFG_CHAN_RESULT_PACKED0	0x42B80630	Channel result register packed with 2 results per register
HPPASS_SAR_CFG_CHAN_RESULT_PACKED1	0x42B80634	Channel result register packed with 2 results per register. See HPPASS_SAR_CFG_CHAN_RESULT_PACKED0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT_PACKED2	0x42B80638	Channel result register packed with 2 results per register. See HPPASS_SAR_CFG_CHAN_RESULT_PACKED0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT_PACKED3	0x42B8063C	Channel result register packed with 2 results per register. See HPPASS_SAR_CFG_CHAN_RESULT_PACKED0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT_PACKED4	0x42B80640	Channel result register packed with 2 results per register. See HPPASS_SAR_CFG_CHAN_RESULT_PACKED0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT_PACKED5	0x42B80644	Channel result register packed with 2 results per register. See HPPASS_SAR_CFG_CHAN_RESULT_PACKED0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT_PACKED6	0x42B80648	Channel result register packed with 2 results per register. See HPPASS_SAR_CFG_CHAN_RESULT_PACKED0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT_PACKED7	0x42B8064C	Channel result register packed with 2 results per register. See HPPASS_SAR_CFG_CHAN_RESULT_PACKED0 for the details of bit fields.

High Performance Programmable Analog Sub-System (HPPASS) registers

Register	Address	Description
HPPASS_SAR_CFG_CHAN_RESULT_PACKED8	0x42B80650	Channel result register packed with 2 results per register. See HPPASS_SAR_CFG_CHAN_RESULT_PACKED0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT_PACKED9	0x42B80654	Channel result register packed with 2 results per register. See HPPASS_SAR_CFG_CHAN_RESULT_PACKED0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT_PACKED10	0x42B80658	Channel result register packed with 2 results per register. See HPPASS_SAR_CFG_CHAN_RESULT_PACKED0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT_PACKED11	0x42B8065C	Channel result register packed with 2 results per register. See HPPASS_SAR_CFG_CHAN_RESULT_PACKED0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT_PACKED12	0x42B80660	Channel result register packed with 2 results per register. See HPPASS_SAR_CFG_CHAN_RESULT_PACKED0 for the details of bit fields.
HPPASS_SAR_CFG_CHAN_RESULT_PACKED13	0x42B80664	Channel result register packed with 2 results per register. See HPPASS_SAR_CFG_CHAN_RESULT_PACKED0 for the details of bit fields.
HPPASS_SAR_CFG_AROUTE_CTRL_MODE	0x42B80700	AROUTE control mode
HPPASS_SAR_CFG_AROUTE_FW_CTRL	0x42B80704	AROUTE firmware switch control set (individual)
HPPASS_SAR_CFG_AROUTE_FW_CTRL_CLR	0x42B80708	AROUTE firmware switch control clear (individual)
HPPASS_SAR_CFG_AROUTE_STATUS	0x42B8070C	AROUTE switch status
HPPASS_SAR_CFG_TEMPSENSE_CTRL	0x42B80710	Temperature Sensor Control
HPPASS_SAR_FIR0_FIR_COEFS0	0x42B80800	FIR Coeffecients
HPPASS_SAR_FIR0_FIR_COEFS1	0x42B80804	FIR Coeffecients. See HPPASS_SAR_FIR0_FIR_COEFS0 for the details of bit fields.
HPPASS_SAR_FIR0_FIR_COEFS2	0x42B80808	FIR Coeffecients. See HPPASS_SAR_FIR0_FIR_COEFS0 for the details of bit fields.
HPPASS_SAR_FIR0_FIR_COEFS3	0x42B8080C	FIR Coeffecients. See HPPASS_SAR_FIR0_FIR_COEFS0 for the details of bit fields.
HPPASS_SAR_FIR0_FIR_COEFS4	0x42B80810	FIR Coeffecients. See HPPASS_SAR_FIR0_FIR_COEFS0 for the details of bit fields.
HPPASS_SAR_FIR0_FIR_COEFS5	0x42B80814	FIR Coeffecients. See HPPASS_SAR_FIR0_FIR_COEFS0 for the details of bit fields.
HPPASS_SAR_FIR0_FIR_COEFS6	0x42B80818	FIR Coeffecients. See HPPASS_SAR_FIR0_FIR_COEFS0 for the details of bit fields.

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Register	Address	Description
HPPASS_SAR_FIR0_FIR_COEFS7	0x42B8081C	FIR Coeffecients. See HPPASS_SAR_FIR0_FIR_COEFS0 for the details of bit fields.
HPPASS_SAR_FIR0_FIR_COEFS8	0x42B80820	FIR Coeffecients. See HPPASS_SAR_FIR0_FIR_COEFS0 for the details of bit fields.
HPPASS_SAR_FIR0_FIR_COEFS9	0x42B80824	FIR Coeffecients. See HPPASS_SAR_FIR0_FIR_COEFS0 for the details of bit fields.
HPPASS_SAR_FIR0_FIR_COEFS10	0x42B80828	FIR Coeffecients. See HPPASS_SAR_FIR0_FIR_COEFS0 for the details of bit fields.
HPPASS_SAR_FIR0_FIR_COEFS11	0x42B8082C	FIR Coeffecients. See HPPASS_SAR_FIR0_FIR_COEFS0 for the details of bit fields.
HPPASS_SAR_FIR0_FIR_COEFS12	0x42B80830	FIR Coeffecients. See HPPASS_SAR_FIR0_FIR_COEFS0 for the details of bit fields.
HPPASS_SAR_FIR0_FIR_COEFS13	0x42B80834	FIR Coeffecients. See HPPASS_SAR_FIR0_FIR_COEFS0 for the details of bit fields.
HPPASS_SAR_FIR0_FIR_COEFS14	0x42B80838	FIR Coeffecients. See HPPASS_SAR_FIR0_FIR_COEFS0 for the details of bit fields.
HPPASS_SAR_FIR0_FIR_COEFS15	0x42B8083C	FIR Coeffecients. See HPPASS_SAR_FIR0_FIR_COEFS0 for the details of bit fields.
HPPASS_SAR_FIR0_FIR_TAPS0	0x42B80840	FIR Taps
HPPASS_SAR_FIR0_FIR_TAPS1	0x42B80844	FIR Taps. See HPPASS_SAR_FIR0_FIR_TAPS0 for the details of bit fields.
HPPASS_SAR_FIR0_FIR_TAPS2	0x42B80848	FIR Taps. See HPPASS_SAR_FIR0_FIR_TAPS0 for the details of bit fields.
HPPASS_SAR_FIR0_FIR_TAPS3	0x42B8084C	FIR Taps. See HPPASS_SAR_FIR0_FIR_TAPS0 for the details of bit fields.
HPPASS_SAR_FIR0_FIR_TAPS4	0x42B80850	FIR Taps. See HPPASS_SAR_FIR0_FIR_TAPS0 for the details of bit fields.
HPPASS_SAR_FIR0_FIR_TAPS5	0x42B80854	FIR Taps. See HPPASS_SAR_FIR0_FIR_TAPS0 for the details of bit fields.
HPPASS_SAR_FIR0_FIR_TAPS6	0x42B80858	FIR Taps. See HPPASS_SAR_FIR0_FIR_TAPS0 for the details of bit fields.
HPPASS_SAR_FIR0_FIR_TAPS7	0x42B8085C	FIR Taps. See HPPASS_SAR_FIR0_FIR_TAPS0 for the details of bit fields.
HPPASS_SAR_FIR0_FIR_TAPS8	0x42B80860	FIR Taps. See HPPASS_SAR_FIR0_FIR_TAPS0 for the details of bit fields.
HPPASS_SAR_FIR0_FIR_TAPS9	0x42B80864	FIR Taps. See HPPASS_SAR_FIR0_FIR_TAPS0 for the details of bit fields.
HPPASS_SAR_FIR0_FIR_TAPS10	0x42B80868	FIR Taps. See HPPASS_SAR_FIR0_FIR_TAPS0 for the details of bit fields.
HPPASS_SAR_FIR0_FIR_TAPS11	0x42B8086C	FIR Taps. See HPPASS_SAR_FIR0_FIR_TAPS0 for the details of bit fields.
HPPASS_SAR_FIR0_FIR_TAPS12	0x42B80870	FIR Taps. See HPPASS_SAR_FIR0_FIR_TAPS0 for the details of bit fields.

High Performance Programmable Analog Sub-System (HPPASS) registers

Register	Address	Description
HPPASS_SAR_FIR0_FIR_TAPS13	0x42B80874	FIR Taps. See HPPASS_SAR_FIR0_FIR_TAPS0 for the details of bit fields.
HPPASS_SAR_FIR0_FIR_TAPS14	0x42B80878	FIR Taps. See HPPASS_SAR_FIR0_FIR_TAPS0 for the details of bit fields.
HPPASS_SAR_FIR0_FIR_TAPS15	0x42B8087C	FIR Taps. See HPPASS_SAR_FIR0_FIR_TAPS0 for the details of bit fields.
HPPASS_SAR_FIR1_FIR_COEFS0	0x42B80880	FIR Coeffecients. See HPPASS_SAR_FIR0_FIR_COEFS0 for the details of bit fields.
HPPASS_SAR_FIR1_FIR_COEFS1	0x42B80884	FIR Coeffecients. See HPPASS_SAR_FIR0_FIR_COEFS0 for the details of bit fields.
HPPASS_SAR_FIR1_FIR_COEFS2	0x42B80888	FIR Coeffecients. See HPPASS_SAR_FIR0_FIR_COEFS0 for the details of bit fields.
HPPASS_SAR_FIR1_FIR_COEFS3	0x42B8088C	FIR Coeffecients. See HPPASS_SAR_FIR0_FIR_COEFS0 for the details of bit fields.
HPPASS_SAR_FIR1_FIR_COEFS4	0x42B80890	FIR Coeffecients. See HPPASS_SAR_FIR0_FIR_COEFS0 for the details of bit fields.
HPPASS_SAR_FIR1_FIR_COEFS5	0x42B80894	FIR Coeffecients. See HPPASS_SAR_FIR0_FIR_COEFS0 for the details of bit fields.
HPPASS_SAR_FIR1_FIR_COEFS6	0x42B80898	FIR Coeffecients. See HPPASS_SAR_FIR0_FIR_COEFS0 for the details of bit fields.
HPPASS_SAR_FIR1_FIR_COEFS7	0x42B8089C	FIR Coeffecients. See HPPASS_SAR_FIR0_FIR_COEFS0 for the details of bit fields.
HPPASS_SAR_FIR1_FIR_COEFS8	0x42B808A0	FIR Coeffecients. See HPPASS_SAR_FIR0_FIR_COEFS0 for the details of bit fields.
HPPASS_SAR_FIR1_FIR_COEFS9	0x42B808A4	FIR Coeffecients. See HPPASS_SAR_FIR0_FIR_COEFS0 for the details of bit fields.
HPPASS_SAR_FIR1_FIR_COEFS10	0x42B808A8	FIR Coeffecients. See HPPASS_SAR_FIR0_FIR_COEFS0 for the details of bit fields.
HPPASS_SAR_FIR1_FIR_COEFS11	0x42B808AC	FIR Coeffecients. See HPPASS_SAR_FIR0_FIR_COEFS0 for the details of bit fields.
HPPASS_SAR_FIR1_FIR_COEFS12	0x42B808B0	FIR Coeffecients. See HPPASS_SAR_FIR0_FIR_COEFS0 for the details of bit fields.
HPPASS_SAR_FIR1_FIR_COEFS13	0x42B808B4	FIR Coeffecients. See HPPASS_SAR_FIR0_FIR_COEFS0 for the details of bit fields.
HPPASS_SAR_FIR1_FIR_COEFS14	0x42B808B8	FIR Coeffecients. See HPPASS_SAR_FIR0_FIR_COEFS0 for the details of bit fields.
HPPASS_SAR_FIR1_FIR_COEFS15	0x42B808BC	FIR Coeffecients. See HPPASS_SAR_FIR0_FIR_COEFS0 for the details of bit fields.
HPPASS_SAR_FIR1_FIR_TAPS0	0x42B808C0	FIR Taps. See HPPASS_SAR_FIR0_FIR_TAPS0 for the details of bit fields.
HPPASS_SAR_FIR1_FIR_TAPS1	0x42B808C4	FIR Taps. See HPPASS_SAR_FIR0_FIR_TAPS0 for the details of bit fields.

High Performance Programmable Analog Sub-System (HPPASS) registers

Register	Address	Description
HPPASS_SAR_FIR1_FIR_TAPS2	0x42B808C8	FIR Taps. See HPPASS_SAR_FIR0_FIR_TAPS0 for the details of bit fields.
HPPASS_SAR_FIR1_FIR_TAPS3	0x42B808CC	FIR Taps. See HPPASS_SAR_FIR0_FIR_TAPS0 for the details of bit fields.
HPPASS_SAR_FIR1_FIR_TAPS4	0x42B808D0	FIR Taps. See HPPASS_SAR_FIR0_FIR_TAPS0 for the details of bit fields.
HPPASS_SAR_FIR1_FIR_TAPS5	0x42B808D4	FIR Taps. See HPPASS_SAR_FIR0_FIR_TAPS0 for the details of bit fields.
HPPASS_SAR_FIR1_FIR_TAPS6	0x42B808D8	FIR Taps. See HPPASS_SAR_FIR0_FIR_TAPS0 for the details of bit fields.
HPPASS_SAR_FIR1_FIR_TAPS7	0x42B808DC	FIR Taps. See HPPASS_SAR_FIR0_FIR_TAPS0 for the details of bit fields.
HPPASS_SAR_FIR1_FIR_TAPS8	0x42B808E0	FIR Taps. See HPPASS_SAR_FIR0_FIR_TAPS0 for the details of bit fields.
HPPASS_SAR_FIR1_FIR_TAPS9	0x42B808E4	FIR Taps. See HPPASS_SAR_FIR0_FIR_TAPS0 for the details of bit fields.
HPPASS_SAR_FIR1_FIR_TAPS10	0x42B808E8	FIR Taps. See HPPASS_SAR_FIR0_FIR_TAPS0 for the details of bit fields.
HPPASS_SAR_FIR1_FIR_TAPS11	0x42B808EC	FIR Taps. See HPPASS_SAR_FIR0_FIR_TAPS0 for the details of bit fields.
HPPASS_SAR_FIR1_FIR_TAPS12	0x42B808F0	FIR Taps. See HPPASS_SAR_FIR0_FIR_TAPS0 for the details of bit fields.
HPPASS_SAR_FIR1_FIR_TAPS13	0x42B808F4	FIR Taps. See HPPASS_SAR_FIR0_FIR_TAPS0 for the details of bit fields.
HPPASS_SAR_FIR1_FIR_TAPS14	0x42B808F8	FIR Taps. See HPPASS_SAR_FIR0_FIR_TAPS0 for the details of bit fields.
HPPASS_SAR_FIR1_FIR_TAPS15	0x42B808FC	FIR Taps. See HPPASS_SAR_FIR0_FIR_TAPS0 for the details of bit fields.
HPPASS_CSG_SLICE0_CMP_CFG	0x42BB0000	Comparator Control Register
HPPASS_CSG_SLICE0_DAC_CFG	0x42BB0004	DAC Control Register
HPPASS_CSG_SLICE0_DAC_PARAM_SYNC	0x42BB0008	DAC Parameter Synchronized Update
HPPASS_CSG_SLICE0_DAC_MODE_START	0x42BB000C	DAC Mode Start
HPPASS_CSG_SLICE0_DAC_VAL_A	0x42BB0010	DAC .Value A Buffer
HPPASS_CSG_SLICE0_DAC_VAL_B	0x42BB0014	DAC Value B Buffer
HPPASS_CSG_SLICE0_DAC_PERIOD	0x42BB0018	DAC Period Buffer
HPPASS_CSG_SLICE0_DAC_VAL	0x42BB001C	DAC FW write
HPPASS_CSG_SLICE0_DAC_STATUS	0x42BB0020	Read of Current DAC Value
HPPASS_CSG_SLICE0_CMP_STATUS	0x42BB0024	Read of Comparator Value

High Performance Programmable Analog Sub-System (HPPASS) registers

Register	Address	Description
HPPASS_CSG_SLICE1_CMP_CFG	0x42BB0040	Comparator Control Register. See HPPASS_CSG_SLICE0_CMP_CFG for the details of bit fields.
HPPASS_CSG_SLICE1_DAC_CFG	0x42BB0044	DAC Control Register. See HPPASS_CSG_SLICE0_DAC_CFG for the details of bit fields.
HPPASS_CSG_SLICE1_DAC_PARAM_SYNC	0x42BB0048	DAC Parameter Synchronized Update. See HPPASS_CSG_SLICE0_DAC_PARAM_SYNC for the details of bit fields.
HPPASS_CSG_SLICE1_DAC_MODE_START	0x42BB004C	DAC Mode Start. See HPPASS_CSG_SLICE0_DAC_MODE_START for the details of bit fields.
HPPASS_CSG_SLICE1_DAC_VAL_A	0x42BB0050	DAC Value A Buffer. See HPPASS_CSG_SLICE0_DAC_VAL_A for the details of bit fields.
HPPASS_CSG_SLICE1_DAC_VAL_B	0x42BB0054	DAC Value B Buffer. See HPPASS_CSG_SLICE0_DAC_VAL_B for the details of bit fields.
HPPASS_CSG_SLICE1_DAC_PERIOD	0x42BB0058	DAC Period Buffer. See HPPASS_CSG_SLICE0_DAC_PERIOD for the details of bit fields.
HPPASS_CSG_SLICE1_DAC_VAL	0x42BB005C	DAC FW write. See HPPASS_CSG_SLICE0_DAC_VAL for the details of bit fields.
HPPASS_CSG_SLICE1_DAC_STATUS	0x42BB0060	Read of Current DAC Value. See HPPASS_CSG_SLICE0_DAC_STATUS for the details of bit fields.
HPPASS_CSG_SLICE1_CMP_STATUS	0x42BB0064	Read of Comparator Value. See HPPASS_CSG_SLICE0_CMP_STATUS for the details of bit fields.
HPPASS_CSG_SLICE2_CMP_CFG	0x42BB0080	Comparator Control Register. See HPPASS_CSG_SLICE0_CMP_CFG for the details of bit fields.
HPPASS_CSG_SLICE2_DAC_CFG	0x42BB0084	DAC Control Register. See HPPASS_CSG_SLICE0_DAC_CFG for the details of bit fields.
HPPASS_CSG_SLICE2_DAC_PARAM_SYNC	0x42BB0088	DAC Parameter Synchronized Update. See HPPASS_CSG_SLICE0_DAC_PARAM_SYNC for the details of bit fields.
HPPASS_CSG_SLICE2_DAC_MODE_START	0x42BB008C	DAC Mode Start. See HPPASS_CSG_SLICE0_DAC_MODE_START for the details of bit fields.
HPPASS_CSG_SLICE2_DAC_VAL_A	0x42BB0090	DAC .Value A Buffer. See HPPASS_CSG_SLICE0_DAC_VAL_A for the details of bit fields.

High Performance Programmable Analog Sub-System (HPPASS) registers

Register	Address	Description
HPPASS_CSG_SLICE2_DAC_VAL_B	0x42BB0094	DAC Value B Buffer. See HPPASS_CSG_SLICE0_DAC_VAL_B for the details of bit fields.
HPPASS_CSG_SLICE2_DAC_PERIOD	0x42BB0098	DAC Period Buffer. See HPPASS_CSG_SLICE0_DAC_PERIOD for the details of bit fields.
HPPASS_CSG_SLICE2_DAC_VAL	0x42BB009C	DAC FW write. See HPPASS_CSG_SLICE0_DAC_VAL for the details of bit fields.
HPPASS_CSG_SLICE2_DAC_STATUS	0x42BB00A0	Read of Current DAC Value. See HPPASS_CSG_SLICE0_DAC_STATUS for the details of bit fields.
HPPASS_CSG_SLICE2_CMP_STATUS	0x42BB00A4	Read of Comparator Value. See HPPASS_CSG_SLICE0_CMP_STATUS for the details of bit fields.
HPPASS_CSG_SLICE3_CMP_CFG	0x42BB00C0	Comparator Control Register. See HPPASS_CSG_SLICE0_CMP_CFG for the details of bit fields.
HPPASS_CSG_SLICE3_DAC_CFG	0x42BB00C4	DAC Control Register. See HPPASS_CSG_SLICE0_DAC_CFG for the details of bit fields.
HPPASS_CSG_SLICE3_DAC_PARAM_SYNC	0x42BB00C8	DAC Parameter Synchronized Update. See HPPASS_CSG_SLICE0_DAC_PARAM_SYNC for the details of bit fields.
HPPASS_CSG_SLICE3_DAC_MODE_START	0x42BB00CC	DAC Mode Start. See HPPASS_CSG_SLICE0_DAC_MODE_START for the details of bit fields.
HPPASS_CSG_SLICE3_DAC_VAL_A	0x42BB00D0	DAC .Value A Buffer. See HPPASS_CSG_SLICE0_DAC_VAL_A for the details of bit fields.
HPPASS_CSG_SLICE3_DAC_VAL_B	0x42BB00D4	DAC Value B Buffer. See HPPASS_CSG_SLICE0_DAC_VAL_B for the details of bit fields.
HPPASS_CSG_SLICE3_DAC_PERIOD	0x42BB00D8	DAC Period Buffer. See HPPASS_CSG_SLICE0_DAC_PERIOD for the details of bit fields.
HPPASS_CSG_SLICE3_DAC_VAL	0x42BB00DC	DAC FW write. See HPPASS_CSG_SLICE0_DAC_VAL for the details of bit fields.
HPPASS_CSG_SLICE3_DAC_STATUS	0x42BB00E0	Read of Current DAC Value. See HPPASS_CSG_SLICE0_DAC_STATUS for the details of bit fields.
HPPASS_CSG_SLICE3_CMP_STATUS	0x42BB00E4	Read of Comparator Value. See HPPASS_CSG_SLICE0_CMP_STATUS for the details of bit fields.

High Performance Programmable Analog Sub-System (HPPASS) registers

Register	Address	Description
HPPASS_CSG_SLICE4_CMP_CFG	0x42BB0100	Comparator Control Register. See HPPASS_CSG_SLICE0_CMP_CFG for the details of bit fields.
HPPASS_CSG_SLICE4_DAC_CFG	0x42BB0104	DAC Control Register. See HPPASS_CSG_SLICE0_DAC_CFG for the details of bit fields.
HPPASS_CSG_SLICE4_DAC_PARAM_SYNC	0x42BB0108	DAC Parameter Synchronized Update. See HPPASS_CSG_SLICE0_DAC_PARAM_SYNC for the details of bit fields.
HPPASS_CSG_SLICE4_DAC_MODE_START	0x42BB010C	DAC Mode Start. See HPPASS_CSG_SLICE0_DAC_MODE_START for the details of bit fields.
HPPASS_CSG_SLICE4_DAC_VAL_A	0x42BB0110	DAC .Value A Buffer. See HPPASS_CSG_SLICE0_DAC_VAL_A for the details of bit fields.
HPPASS_CSG_SLICE4_DAC_VAL_B	0x42BB0114	DAC Value B Buffer. See HPPASS_CSG_SLICE0_DAC_VAL_B for the details of bit fields.
HPPASS_CSG_SLICE4_DAC_PERIOD	0x42BB0118	DAC Period Buffer. See HPPASS_CSG_SLICE0_DAC_PERIOD for the details of bit fields.
HPPASS_CSG_SLICE4_DAC_VAL	0x42BB011C	DAC FW write. See HPPASS_CSG_SLICE0_DAC_VAL for the details of bit fields.
HPPASS_CSG_SLICE4_DAC_STATUS	0x42BB0120	Read of Current DAC Value. See HPPASS_CSG_SLICE0_DAC_STATUS for the details of bit fields.
HPPASS_CSG_SLICE4_CMP_STATUS	0x42BB0124	Read of Comparator Value. See HPPASS_CSG_SLICE0_CMP_STATUS for the details of bit fields.
HPPASS_CSG_LUT_CFG0_LUT_DATA0	0x42BB0400	LUT Wave form Data. This is the starting address of a register bank containing 128 registers (HPPASS_CSG_LUT_CFG0_LUT_DATA0 to HPPASS_CSG_LUT_CFG0_LUT_DATA127).
HPPASS_CSG_LUT_CFG1_LUT_DATA0	0x42BB0600	LUT Wave form Data. This is the starting address of a register bank containing 128 registers (HPPASS_CSG_LUT_CFG1_LUT_DATA0 to HPPASS_CSG_LUT_CFG1_LUT_DATA127). See HPPASS_CSG_LUT_CFG0_LUT_DATA0 for the details of bit fields.
HPPASS_CSG_CSG_CTRL	0x42BB0A00	CSG control register
HPPASS_CSG_DAC_INTR	0x42BB0B00	DAC Interrupt register
HPPASS_CSG_DAC_INTR_SET	0x42BB0B04	DAC Interrupt request set register
HPPASS_CSG_DAC_INTR_MASK	0x42BB0B08	DAC Interrupt request mask
HPPASS_CSG_DAC_INTR_MASKED	0x42BB0B0C	DAC Interrupt request masked

High Performance Programmable Analog Sub-System (HPPASS) registers

Register	Address	Description
HPPASS_CSG_CMP_INTR	0x42BB0B10	CMP Interrupt register
HPPASS_CSG_CMP_INTR_SET	0x42BB0B14	CMP Interrupt request set register
HPPASS_CSG_CMP_INTR_MASK	0x42BB0B18	CMP Interrupt request mask
HPPASS_CSG_CMP_INTR_MASKED	0x42BB0B1C	CMP Interrupt request masked
HPPASS_CSG_VDAC_OUT_BLANK	0x42BB0B20	Blanking control for DAC Observability
HPPASS_CSG_CSG_SYNC	0x42BB0B30	CSG Sync Enable register
HPPASS_ACTRLR_CTRL	0x42BD0000	Control register
HPPASS_ACTRLR_CMD_RUN	0x42BD0004	Run Command register
HPPASS_ACTRLR_CMD_STATE	0x42BD0008	State Override register
HPPASS_ACTRLR_BLOCK_STATUS	0x42BD0010	Block Ready status register
HPPASS_ACTRLR_STATUS	0x42BD0020	AC Status register
HPPASS_ACTRLR_CFG	0x42BD0024	AC Config register
HPPASS_ACTRLR_CNTR_STATUS0	0x42BD0100	Loop/Interval counter status register
HPPASS_ACTRLR_CNTR_STATUS1	0x42BD0104	Loop/Interval counter status register. See HPPASS_ACTRLR_CNTR_STATUS0 for the details of bit fields.
HPPASS_ACTRLR_TTCFG0_TT_CFG0	0x42BD0800	AC Configuration 0
HPPASS_ACTRLR_TTCFG0_TT_CFG1	0x42BD0804	AC Configuration 1
HPPASS_ACTRLR_TTCFG0_TT_CFG2	0x42BD0808	AC Configuration 2
HPPASS_ACTRLR_TTCFG0_TT_CFG3	0x42BD080C	AC Configuration 3
HPPASS_ACTRLR_TTCFG1_TT_CFG0	0x42BD0810	AC Configuration 0. See HPPASS_ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
HPPASS_ACTRLR_TTCFG1_TT_CFG1	0x42BD0814	AC Configuration 1. See HPPASS_ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
HPPASS_ACTRLR_TTCFG1_TT_CFG2	0x42BD0818	AC Configuration 2. See HPPASS_ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
HPPASS_ACTRLR_TTCFG1_TT_CFG3	0x42BD081C	AC Configuration 3. See HPPASS_ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
HPPASS_ACTRLR_TTCFG2_TT_CFG0	0x42BD0820	AC Configuration 0. See HPPASS_ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
HPPASS_ACTRLR_TTCFG2_TT_CFG1	0x42BD0824	AC Configuration 1. See HPPASS_ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
HPPASS_ACTRLR_TTCFG2_TT_CFG2	0x42BD0828	AC Configuration 2. See HPPASS_ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.

High Performance Programmable Analog Sub-System (HPPASS) registers

Register	Address	Description
HPPASS_ACTRLR_TTCFG2_TT_CFG3	0x42BD082C	AC Configuration 3. See HPPASS_ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
HPPASS_ACTRLR_TTCFG3_TT_CFG0	0x42BD0830	AC Configuration 0. See HPPASS_ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
HPPASS_ACTRLR_TTCFG3_TT_CFG1	0x42BD0834	AC Configuration 1. See HPPASS_ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
HPPASS_ACTRLR_TTCFG3_TT_CFG2	0x42BD0838	AC Configuration 2. See HPPASS_ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
HPPASS_ACTRLR_TTCFG3_TT_CFG3	0x42BD083C	AC Configuration 3. See HPPASS_ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
HPPASS_ACTRLR_TTCFG4_TT_CFG0	0x42BD0840	AC Configuration 0. See HPPASS_ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
HPPASS_ACTRLR_TTCFG4_TT_CFG1	0x42BD0844	AC Configuration 1. See HPPASS_ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
HPPASS_ACTRLR_TTCFG4_TT_CFG2	0x42BD0848	AC Configuration 2. See HPPASS_ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
HPPASS_ACTRLR_TTCFG4_TT_CFG3	0x42BD084C	AC Configuration 3. See HPPASS_ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
HPPASS_ACTRLR_TTCFG5_TT_CFG0	0x42BD0850	AC Configuration 0. See HPPASS_ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
HPPASS_ACTRLR_TTCFG5_TT_CFG1	0x42BD0854	AC Configuration 1. See HPPASS_ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
HPPASS_ACTRLR_TTCFG5_TT_CFG2	0x42BD0858	AC Configuration 2. See HPPASS_ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
HPPASS_ACTRLR_TTCFG5_TT_CFG3	0x42BD085C	AC Configuration 3. See HPPASS_ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
HPPASS_ACTRLR_TTCFG6_TT_CFG0	0x42BD0860	AC Configuration 0. See HPPASS_ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
HPPASS_ACTRLR_TTCFG6_TT_CFG1	0x42BD0864	AC Configuration 1. See HPPASS_ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.

High Performance Programmable Analog Sub-System (HPPASS) registers

Register	Address	Description
HPPASS_ACTRLR_TTCFG6_TT_CFG2	0x42BD0868	AC Configuration 2. See HPPASS_ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
HPPASS_ACTRLR_TTCFG6_TT_CFG3	0x42BD086C	AC Configuration 3. See HPPASS_ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
HPPASS_ACTRLR_TTCFG7_TT_CFG0	0x42BD0870	AC Configuration 0. See HPPASS_ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
HPPASS_ACTRLR_TTCFG7_TT_CFG1	0x42BD0874	AC Configuration 1. See HPPASS_ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
HPPASS_ACTRLR_TTCFG7_TT_CFG2	0x42BD0878	AC Configuration 2. See HPPASS_ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
HPPASS_ACTRLR_TTCFG7_TT_CFG3	0x42BD087C	AC Configuration 3. See HPPASS_ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
HPPASS_ACTRLR_TTCFG8_TT_CFG0	0x42BD0880	AC Configuration 0. See HPPASS_ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
HPPASS_ACTRLR_TTCFG8_TT_CFG1	0x42BD0884	AC Configuration 1. See HPPASS_ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
HPPASS_ACTRLR_TTCFG8_TT_CFG2	0x42BD0888	AC Configuration 2. See HPPASS_ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
HPPASS_ACTRLR_TTCFG8_TT_CFG3	0x42BD088C	AC Configuration 3. See HPPASS_ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
HPPASS_ACTRLR_TTCFG9_TT_CFG0	0x42BD0890	AC Configuration 0. See HPPASS_ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
HPPASS_ACTRLR_TTCFG9_TT_CFG1	0x42BD0894	AC Configuration 1. See HPPASS_ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
HPPASS_ACTRLR_TTCFG9_TT_CFG2	0x42BD0898	AC Configuration 2. See HPPASS_ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
HPPASS_ACTRLR_TTCFG9_TT_CFG3	0x42BD089C	AC Configuration 3. See HPPASS_ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
HPPASS_ACTRLR_TTCFG10_TT_CFG0	0x42BD08A0	AC Configuration 0. See HPPASS_ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.

High Performance Programmable Analog Sub-System (HPPASS) registers

Register	Address	Description
HPPASS_ACTRLR_TTCFG10_TT_CFG1	0x42BD08A4	AC Configuration 1. See HPPASS_ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
HPPASS_ACTRLR_TTCFG10_TT_CFG2	0x42BD08A8	AC Configuration 2. See HPPASS_ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
HPPASS_ACTRLR_TTCFG10_TT_CFG3	0x42BD08AC	AC Configuration 3. See HPPASS_ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
HPPASS_ACTRLR_TTCFG11_TT_CFG0	0x42BD08B0	AC Configuration 0. See HPPASS_ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
HPPASS_ACTRLR_TTCFG11_TT_CFG1	0x42BD08B4	AC Configuration 1. See HPPASS_ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
HPPASS_ACTRLR_TTCFG11_TT_CFG2	0x42BD08B8	AC Configuration 2. See HPPASS_ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
HPPASS_ACTRLR_TTCFG11_TT_CFG3	0x42BD08BC	AC Configuration 3. See HPPASS_ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
HPPASS_ACTRLR_TTCFG12_TT_CFG0	0x42BD08C0	AC Configuration 0. See HPPASS_ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
HPPASS_ACTRLR_TTCFG12_TT_CFG1	0x42BD08C4	AC Configuration 1. See HPPASS_ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
HPPASS_ACTRLR_TTCFG12_TT_CFG2	0x42BD08C8	AC Configuration 2. See HPPASS_ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
HPPASS_ACTRLR_TTCFG12_TT_CFG3	0x42BD08CC	AC Configuration 3. See HPPASS_ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
HPPASS_ACTRLR_TTCFG13_TT_CFG0	0x42BD08D0	AC Configuration 0. See HPPASS_ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
HPPASS_ACTRLR_TTCFG13_TT_CFG1	0x42BD08D4	AC Configuration 1. See HPPASS_ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
HPPASS_ACTRLR_TTCFG13_TT_CFG2	0x42BD08D8	AC Configuration 2. See HPPASS_ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
HPPASS_ACTRLR_TTCFG13_TT_CFG3	0x42BD08DC	AC Configuration 3. See HPPASS_ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.

High Performance Programmable Analog Sub-System (HPPASS) registers

Register	Address	Description
HPPASS_ACTRLR_TTCFG14_TT_CFG0	0x42BD08E0	AC Configuration 0. See HPPASS_ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
HPPASS_ACTRLR_TTCFG14_TT_CFG1	0x42BD08E4	AC Configuration 1. See HPPASS_ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
HPPASS_ACTRLR_TTCFG14_TT_CFG2	0x42BD08E8	AC Configuration 2. See HPPASS_ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
HPPASS_ACTRLR_TTCFG14_TT_CFG3	0x42BD08EC	AC Configuration 3. See HPPASS_ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
HPPASS_ACTRLR_TTCFG15_TT_CFG0	0x42BD08F0	AC Configuration 0. See HPPASS_ACTRLR_TTCFG0_TT_CFG0 for the details of bit fields.
HPPASS_ACTRLR_TTCFG15_TT_CFG1	0x42BD08F4	AC Configuration 1. See HPPASS_ACTRLR_TTCFG0_TT_CFG1 for the details of bit fields.
HPPASS_ACTRLR_TTCFG15_TT_CFG2	0x42BD08F8	AC Configuration 2. See HPPASS_ACTRLR_TTCFG0_TT_CFG2 for the details of bit fields.
HPPASS_ACTRLR_TTCFG15_TT_CFG3	0x42BD08FC	AC Configuration 3. See HPPASS_ACTRLR_TTCFG0_TT_CFG3 for the details of bit fields.
HPPASS_INFRA_TR_IN_SEL	0x42BE0000	Trigger Input Select
HPPASS_INFRA_HW_TR_MODE	0x42BE0004	HW Trigger Mode
HPPASS_INFRA_FW_TR_PULSE	0x42BE0008	FW Pulse Mode Trigger
HPPASS_INFRA_FW_TR_LEVEL	0x42BE000C	FW Level Mode Trigger
HPPASS_INFRA_CLOCK_STARTUP_DIV	0x42BE0020	Startup Clock Divider
HPPASS_INFRA_STARTUP_CFG0	0x42BE0030	Startup configuration
HPPASS_INFRA_STARTUP_CFG1	0x42BE0034	Startup configuration. See HPPASS_INFRA_STARTUP_CFG0 for the details of bit fields.
HPPASS_INFRA_STARTUP_CFG2	0x42BE0038	Startup configuration. See HPPASS_INFRA_STARTUP_CFG0 for the details of bit fields.
HPPASS_INFRA_STARTUP_CFG3	0x42BE003C	Startup configuration. See HPPASS_INFRA_STARTUP_CFG0 for the details of bit fields.
HPPASS_INFRA_VDDA_STATUS	0x42BE0050	Analog Voltage Status
HPPASS_INFRA_ANA_CTRL	0x42BE0070	Analog Control
HPPASS_INFRA_AREFv2_AREF_CTRL	0x42BE0E00	AREF control
HPPASS_INFRA_VREF_TRIM0	0x42BE0F00	VREF Trim bits

High Performance Programmable Analog Sub-System (HPPASS) registers

Register	Address	Description
HPPASS_INFRA_VREF_TRIM1	0x42BE0F04	VREF Trim bits
HPPASS_INFRA_VREF_TRIM2	0x42BE0F08	VREF Trim bits
HPPASS_INFRA_VREF_TRIM3	0x42BE0F0C	VREF Trim bits
HPPASS_INFRA_IZTAT_TRIM0	0x42BE0F10	IZTAT Trim bits
HPPASS_INFRA_IZTAT_TRIM1	0x42BE0F14	IZTAT Trim bits
HPPASS_INFRA_IPTAT_TRIM0	0x42BE0F18	IPTAT Trim bits
HPPASS_INFRA_ICTAT_TRIM0	0x42BE0F1C	ICTAT Trim bits
HPPASS_MMIO_FIFO_INTR	0x42BF0000	FIFO Interrupt request register
HPPASS_MMIO_FIFO_INTR_SET	0x42BF0010	FIFO Interrupt set request register
HPPASS_MMIO_FIFO_INTR_MASK	0x42BF0020	FIFO Interrupt mask register
HPPASS_MMIO_FIFO_INTR_MASKED	0x42BF0030	FIFO Interrupt masked request register
HPPASS_MMIO_HPPASS_INTR	0x42BF0040	HPPASS Interrupt request register
HPPASS_MMIO_HPPASS_INTR_SET	0x42BF0044	HPPASS Interrupt set request register
HPPASS_MMIO_HPPASS_INTR_MASK	0x42BF0048	HPPASS Interrupt mask register
HPPASS_MMIO_HPPASS_INTR_MASKED	0x42BF004C	HPPASS Interrupt masked request register
HPPASS_MMIO_TR_LEVEL_CFG	0x42BF0050	LEVEL Trigger out configuration
HPPASS_MMIO_TR_LEVEL_OUT0	0x42BF0060	LEVEL Trigger out select register
HPPASS_MMIO_TR_LEVEL_OUT1	0x42BF0064	LEVEL Trigger out select register. See HPPASS_MMIO_TR_LEVEL_OUT0 for the details of bit fields.
HPPASS_MMIO_TR_LEVEL_OUT2	0x42BF0068	LEVEL Trigger out select register. See HPPASS_MMIO_TR_LEVEL_OUT0 for the details of bit fields.
HPPASS_MMIO_TR_LEVEL_OUT3	0x42BF006C	LEVEL Trigger out select register. See HPPASS_MMIO_TR_LEVEL_OUT0 for the details of bit fields.
HPPASS_MMIO_TR_LEVEL_OUT4	0x42BF0070	LEVEL Trigger out select register. See HPPASS_MMIO_TR_LEVEL_OUT0 for the details of bit fields.
HPPASS_MMIO_TR_LEVEL_OUT5	0x42BF0074	LEVEL Trigger out select register. See HPPASS_MMIO_TR_LEVEL_OUT0 for the details of bit fields.
HPPASS_MMIO_TR_LEVEL_OUT6	0x42BF0078	LEVEL Trigger out select register. See HPPASS_MMIO_TR_LEVEL_OUT0 for the details of bit fields.
HPPASS_MMIO_TR_LEVEL_OUT7	0x42BF007C	LEVEL Trigger out select register. See HPPASS_MMIO_TR_LEVEL_OUT0 for the details of bit fields.
HPPASS_MMIO_TR_PULSE_OUT0	0x42BF0080	PULSE Trigger out select register
HPPASS_MMIO_TR_PULSE_OUT1	0x42BF0084	PULSE Trigger out select register. See HPPASS_MMIO_TR_PULSE_OUT0 for the details of bit fields.

High Performance Programmable Analog Sub-System (HPPASS) registers

Register	Address	Description
HPPASS_MMIO_TR_PULSE_OUT2	0x42BF0088	PULSE Trigger out select register. See HPPASS_MMIO_TR_PULSE_OUT0 for the details of bit fields.
HPPASS_MMIO_TR_PULSE_OUT3	0x42BF008C	PULSE Trigger out select register. See HPPASS_MMIO_TR_PULSE_OUT0 for the details of bit fields.
HPPASS_MMIO_TR_PULSE_OUT4	0x42BF0090	PULSE Trigger out select register. See HPPASS_MMIO_TR_PULSE_OUT0 for the details of bit fields.
HPPASS_MMIO_TR_PULSE_OUT5	0x42BF0094	PULSE Trigger out select register. See HPPASS_MMIO_TR_PULSE_OUT0 for the details of bit fields.
HPPASS_MMIO_TR_PULSE_OUT6	0x42BF0098	PULSE Trigger out select register. See HPPASS_MMIO_TR_PULSE_OUT0 for the details of bit fields.
HPPASS_MMIO_TR_PULSE_OUT7	0x42BF009C	PULSE Trigger out select register. See HPPASS_MMIO_TR_PULSE_OUT0 for the details of bit fields.
HPPASS_MMIO_FIFO_CFG	0x42BF0100	FIFO configuration register.
HPPASS_MMIO_FIFO_CLR	0x42BF0104	FIFO FW clear register
HPPASS_MMIO_FIFO_LEVEL0	0x42BF0110	FIFO level register.
HPPASS_MMIO_FIFO_LEVEL1	0x42BF0114	FIFO level register. See HPPASS_MMIO_FIFO_LEVEL0 for the details of bit fields.
HPPASS_MMIO_FIFO_LEVEL2	0x42BF0118	FIFO level register. See HPPASS_MMIO_FIFO_LEVEL0 for the details of bit fields.
HPPASS_MMIO_FIFO_LEVEL3	0x42BF011C	FIFO level register. See HPPASS_MMIO_FIFO_LEVEL0 for the details of bit fields.
HPPASS_MMIO_FIFO_RD_DATA0	0x42BF0130	FIFO 32-bit read data register
HPPASS_MMIO_FIFO_RD_DATA1	0x42BF0134	FIFO 32-bit read data register. See HPPASS_MMIO_FIFO_RD_DATA0 for the details of bit fields.
HPPASS_MMIO_FIFO_RD_DATA2	0x42BF0138	FIFO 32-bit read data register. See HPPASS_MMIO_FIFO_RD_DATA0 for the details of bit fields.
HPPASS_MMIO_FIFO_RD_DATA3	0x42BF013C	FIFO 32-bit read data register. See HPPASS_MMIO_FIFO_RD_DATA0 for the details of bit fields.
HPPASS_MMIO_FIFO_USED0	0x42BF0150	FIFO used register
HPPASS_MMIO_FIFO_USED1	0x42BF0154	FIFO used register. See HPPASS_MMIO_FIFO_USED0 for the details of bit fields.
HPPASS_MMIO_FIFO_USED2	0x42BF0158	FIFO used register. See HPPASS_MMIO_FIFO_USED0 for the details of bit fields.

High Performance Programmable Analog Sub-System (HPPASS) registers

Register	Address	Description
HPPASS_MMIO_FIFO_USED3	0x42BF015C	FIFO used register. See HPPASS_MMIO_FIFO_USED0 for the details of bit fields.
HPPASS_MMIO_FIFO_STATUS0	0x42BF0170	FIFO status register
HPPASS_MMIO_FIFO_STATUS1	0x42BF0174	FIFO status register. See HPPASS_MMIO_FIFO_STATUS0 for the details of bit fields.
HPPASS_MMIO_FIFO_STATUS2	0x42BF0178	FIFO status register. See HPPASS_MMIO_FIFO_STATUS0 for the details of bit fields.
HPPASS_MMIO_FIFO_STATUS3	0x42BF017C	FIFO status register. See HPPASS_MMIO_FIFO_STATUS0 for the details of bit fields.

20.1.1 HPPASS_SARADC_CALOFFST0

SARADC Offset Calibration Values

Address: 0x42B70010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	RW						
Name	None	OFFSET_4N_0 [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW						
HW Access	None	RW						
Name	None	OFFSET_4N_1 [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	RW						
Name	None	OFFSET_4N_2 [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW						
HW Access	None	RW						
Name	None	OFFSET_4N_3 [30:24]						

Bits	Name	Description
30 : 24	OFFSET_4N_3	7-bit signed offset calibration value for sampler 4n + 3 Default Value: 0
22 : 16	OFFSET_4N_2	7-bit signed offset calibration value for sampler 4n + 2 Default Value: 0
14 : 8	OFFSET_4N_1	7-bit signed offset calibration value for sampler 4n + 1 Default Value: 0
6 : 0	OFFSET_4N_0	7-bit signed offset calibration value for sampler 4n + 0 Default Value: 0

20.1.2 HPPASS_SARADC_CALLIN0

SARADC Linearity Calibration Values

Address: 0x42B70020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	RW						
Name	None	LIN9 [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW						
HW Access	None	RW						
Name	None	LIIN10 [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	RW						
Name	None	LIN11 [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW						
HW Access	None	RW						
Name	None	LIN12 [30:24]						

Bits	Name	Description
30 : 24	LIN12	7 bit signed linearity calibration value for bit 12 of this sampler Default Value: 0
22 : 16	LIN11	7 bit signed linearity calibration value for bit 11 of this sampler Default Value: 0
14 : 8	LIIN10	7 bit signed linearity calibration value for bit 10 of this sampler Default Value: 0
6 : 0	LIN9	7 bit signed linearity calibration value for bit 9 of this sampler Default Value: 0

20.1.3 HPPASS_SARADC_CALGAINC

SARADC Coarse-grained Gain Calibration Values

Address: 0x42B70060

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				RW			
Name	None [7:4]				GAINC3 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				RW			
Name	None [15:12]				GAINC6 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				RW			
Name	None [23:20]				GAINC12 [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	GAINC12	Coarse-grained gain calibration value for gain=12 setting see description of GAINC3 Default Value: 0
11 : 8	GAINC6	Coarse-grained gain calibration value for gain=6 setting see description of GAINC3 Default Value: 0
3 : 0	GAINC3	Coarse-grained gain calibration value for gain=3 setting bit 3: SIGN, bits <2:0> : VALUE 0xF => -7: Voltage correction -14mV 0xE => -6: Voltage correction -12mV 0xD => -5: Voltage correction -10mV 0xC => -4: Voltage correction -8mV 0xB => -3: Voltage correction -6mV 0xA => -2: Voltage correction -4mV 0x9 => -1: Voltage correction -2mV 0x8 == 0x0 => 0: Voltage correction 0mV 0x1 => 1: Voltage correction +2mV 0x2 => 2: Voltage correction +4mV 0x3 => 3: Voltage correction +6mV 0x4 => 4: Voltage correction +8mV 0x5 => 5: Voltage correction +10mV 0x6 => 6: Voltage correction +12mV 0x7 => 7: Voltage correction +14mV Default Value: 0

20.1.4 HPPASS_SARADC_CALGAINF

SARADC Fine-grained Gain Calibration Values

Address: 0x42B70064

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	RW						
Name	None	GAINF3 [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW						
HW Access	None	RW						
Name	None	GAINF6 [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	RW						
Name	None	GAINF12 [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
22 : 16	GAINF12	7-bit signed fine-grained gain calibration value for gain=12 setting Default Value: 0
14 : 8	GAINF6	7-bit signed fine-grained gain calibration value for gain=6 setting Default Value: 0
6 : 0	GAINF3	7-bit signed fine-grained gain calibration value for gain=3 setting Default Value: 0

20.1.5 HPPASS_SAR_SEQ_ENTRY0

SAR Sequencer Table Entries

Address: 0x42B80100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DIRECT_SAMPLER_EN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	MUXED_SAMPLER_EN [15:12]				DIRECT_SAMPLER_EN [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	MUX3_SEL [23:22]		MUX2_SEL [21:20]		MUX1_SEL [19:18]		MUX0_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		RW			
HW Access	R	R	R		R			
Name	CONT	PRIORITY	SAMP_TIME_SEL [29:28]		TR_SEL [27:24]			

Bits	Name	Description
31	CONT	This bit enables continuous conversion for this entry. When this bit is set, this entry will trigger immediately when the SAR is ENABLED, and will be automatically re-triggered when this ENTRY has been completed. NOTE: Due to this automatic triggering, the TR_SEL field must be set to DISABLED for this ENTRY A continuous Entry should have sample time (SAMP_TIME_SEL is not DISABLED), otherwise this Entry will be continously triggered and use the majority of the SAR performance bandwidth. In other words, sample time is the only way to set the periodicity of a continous Entry. Default Value: 0
30	PRIORITY	This bit selects the priority for this entry. High Priority samplers ready for conversion witll be processed before Low Priority samplers. 0: Low Priority 1: High Priority If the application configures a combination of High and Low Priority Entries, depending on the usage demand on the SAR from High Priority Entries, a Low Priority Entry might stay in HOLD state beyond a spec limit (See SAR_CFG.HOLD_VIOLATION and SAR_CFG.HOLD_CNT for more details). To ensure that the Low priority Entry did not stay in HOLD state beyond this limit, before reading a Low Priority Entry result, check the SAR_CFG.HOLD_VIOLATION status to ensure that the result is within spec. Default Value: 0
29 : 28	SAMP_TIME_SEL	Sample Time Select. By default there is no additional sample time after the trigger (samplers are transitioned to HOLD state immediately on a trigger event) or select 1 of 3 available Sample Times in SAR_CFG.SAMPLE_TIME registers Default Value: 0 **0x0: DISBALED :**

20.1.5 HPPASS_SAR_SEQ_ENTRY0 (continued)

		0x1: SAMPLE_TIME_SEL0 :
		0x2: SAMPLE_TIME_SEL1 :
		0x3: SAMPLE_TIME_SEL2 :
27 : 24	TR_SEL	Trigger select for this Entry. By default disabled, or select 1 of 8 hardware triggers or AC trigger. Normally HPPASS internal triggers are PULSE triggers (see INFRA/TR_HW_MODE), however, a LEVEL trigger may also be used, but the trigger event is always on the positive edge of a LEVEL trigger. Once this ENTRY is triggered, the user must wait for SAR_ENTRY_DONE status to trigger this entry again. Otherwise a trigger collision status will be set for this ENTRY (see SAR_CFG.SAR_TR_COLLISION and HPPASS_MMIO.HPPASS_INTR) Default Value: 0 **0x0: DISABLED :** **0x1: TR0 :** **0x2: TR1 :** **0x3: TR2 :** **0x4: TR3 :** **0x5: TR4 :** **0x6: TR5 :** **0x7: TR6 :** **0x8: TR7 :** **0x9: AC :**
23 : 22	MUX3_SEL	These bits control the input mux selection for sampler 15 Default Value: 0
21 : 20	MUX2_SEL	These bits control the input mux selection for sampler 14 Default Value: 0
19 : 18	MUX1_SEL	These bits control the input mux selection for sampler 13 Default Value: 0
17 : 16	MUX0_SEL	These bits control the input mux selection for sampler 12 Default Value: 0

20.1.5 HPPASS_SAR_SEQ_ENTRY0 (continued)

15 : 12	MUXED_SAMPLER_EN	These bits enable the 4 muxed samplers in this Entry. When this Entry is triggered any samplers with a bit set to '1' will be simultaneously sampled, held, and then converted. The mux setting for these samplers is determined by the following MUX(i)_SEL fields. Each one of these samplers maps to 4 result channels as determined by the mux setting 0,1,2, or 3 in order. The mapping is: MUXED_SAMPLER_EN - bit 12 (sampler 12) CHAN RESULTS are found in SAR_CFG.CHAN_RESULT12,13,14,15 MUXED_SAMPLER_EN - bit 13 (sampler 13) CHAN RESULTS are found in SAR_CFG.CHAN_RESULT16,17,18,19 MUXED_SAMPLER_EN - bit 14 (sampler 14) CHAN RESULTS are found in SAR_CFG.CHAN_RESULT20,21,22,23 MUXED_SAMPLER_EN - bit 15 (sampler 15) CHAN RESULTS are found in SAR_CFG.CHAN_RESULT24,25,26,27 Muxed samplers may also be specified as pseudo differential sampler pairs, but as described in SAR_CFG.CHAN_CFG.DIFF_EN, there are four possible inputs to each sampler in the even odd sampler pairs 12/13 or 14/15. Set DIFF_EN for the positive input (also configure post processing and storage specification) and also set MUX(even)_SEL to match this positive selection. To select the negative input, set the correspoing MUX(odd)_SEL. The odd bits of this field are ignored when the even sampler is enabled for PD. Default Value: 0
11 : 0	DIRECT_SAMPLER_EN	These bits enable the 12 direct samplers in this Entry. When this Entry is triggered, any samplers with a bit set to '1' will be simultaneously sampled, held, and then converted. There is a 1-1 correspondence between these 12 samplers and the first 12 result channels. Therefore SAR results may be found in SAR_CFG.CHAN_RESULT0 - CHAN_RESULT12 When pseudo differential or PD is enabled in an even channel (SAR_CFG.CHAN_CFG.DIFF_EN) that sampler/channel it is the positive input of the PD pair, and the corresponding odd channel becomes the negative input. The result is processed and stored as specified in the even channel (e.g. AVG, FIR, RESULT REG,FIFO) Default Value: 0

20.1.6 HPPASS_SAR_ENTRY_MUX_SEL_ALIAS0

SAR Sequencer MUX select alias registers

Address: 0x42B80200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	MUX3_SEL [23:22]		MUX2_SEL [21:20]		MUX1_SEL [19:18]		MUX0_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 22	MUX3_SEL	Update SEQ_ENTRY.MUX3_SEL field Default Value: 0
21 : 20	MUX2_SEL	Update SEQ_ENTRY.MUX2_SEL field Default Value: 0
19 : 18	MUX1_SEL	Update SEQ_ENTRY.MUX1_SEL field Default Value: 0
17 : 16	MUX0_SEL	Update SEQ_ENTRY.MUX0_SEL field Using this alias register, the user can read/write directly to the associated routing select fields in a given entry, without the need to do a read-modify-write operation on a SEQ_ENTRY register Default Value: 0

20.1.7 HPPASS_SAR_CFG_CTRL

Control register

Address: 0x42B80400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW	RW	
HW Access	None	R	R	R	None	R	R	
Name	None	STARTUP_-CAL_GAIN_EN	STARTUP_-CAL_LIN-EARITY_EN	STARTUP_-CAL_OFF-SET_EN	None	LOW_SUP-PLY_MODE	VREF_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							CHAN_ID_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	CHAN_ID_EN	FIFO Channel Number Identifier Enable Default Value: 0 **0x0: DISABLED :** When the FIFO is selected for a channel or FIR result (optional), 16-bit result data is stored in FIFO without tagging in the following format <00000>, <16-bit result> **0x1: ENABLED :** Result data is stored in FIFO is tagged with channel number identifier and stored as follows <5-bit chan_num>, <16-bit result>, where the 5-bit chan_num is 0-27 for channel results, and 30, 31 for FIR results
6	STARTUP_-CAL_GAIN_EN	Calibrate Gain on SAR Enable Default Value: 0 **0x0: DISABLED :** **0x1: ENABLED :**

20.1.7 HPPASS_SAR_CFG_CTRL (continued)

5	STARTUP_CAL_LINEAR-ITY_EN	Calibration Linearity on SAR Enable Default Value: 0 **0x0: DISABLED :** **0x1: ENABLED :**
4	STARTUP_CAL_OFF-SET_EN	Calibration Offset on SAR Enable All selected CAL routines (OFFSET, LINEARITY, GAIN) in this register are run if these bits are set when the AC enables the SAR. The user must wait for BLOCK_READY (polling or interrupt) at which time SAR CAL and initialization is complete, before starting the application. Default Value: 0 **0x0: DISABLED :** **0x1: ENABLED :**
2	LOW_SUPPLY_MODE	Low Supply Mode control - set this bit if VDDA supply range < 2.7V Default Value: 0 **0x0: DISABLED :** Disabled, VDDA supply is >= 2.7V **0x1: ENABLED :** Enabled, VDDA supply is < 2.7V
1 : 0	VREF_SEL	SARADC VREF selection. Default Value: 0 **0x0: VDDA :** **0x1: EXT_REF :** **0x2: RESERVED_2 :** **0x3: RESERVED_3 :**

20.1.8 HPPASS_SAR_CFG_SAMP_EN

Sampler static enable configuration register

Address: 0x42B80404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DIRECT_SAMP_EN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	MUXED_SAMP_EN [15:12]				DIRECT_SAMP_EN [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 12	MUXED_SAMP_EN	Static Enables for Muxed Samplers. Must be set if in use by application, otherwise it is OFF and must not be selected in any SAR Entry. Default Value: 0
11 : 0	DIRECT_SAMP_EN	Static Enables for Direct Samplers. Must be set if in use by application, otherwise it is OFF and must not be selected in any SAR Entry. A given SAR Entry is considered invalid if 1) There are no Samplers enabled and 2) For the given set of enabled Samplers, they all must be powered ON with this static setting. If the Entry is invalid, no action will be taken in the SAR sequencer if this Entry is triggered. Default Value: 0

20.1.9 HPPASS_SAR_CFG_SAMP_GAIN

Sampler gain configuration register

Address: 0x42B80408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SAMP_GAIN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SAMP_GAIN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SAMP_GAIN [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	SAMP_GAIN [31:24]							

Bits	Name	Description
31 : 0	SAMP_GAIN	Static Sampler Gain Configure this register BEFORE enabling the SAR, it must be static during SAR operation. 0 = GAIN of 1 (default) 1 = GAIN of 3 2 = GAIN of 6 3 = GAIN of 12 Two bits per sampler: Sampler0 gain in [1:0] Sampler1 gain in [3:2] Sampler2 gain in [5:4] ... Sampler14 gain in [29:28] Sampler15 gain in [31:30] NOTE: If Psuedo Differential (PD) mode is enabled for a given Channel (see CHAN_CFG.DIFFERENTIAL_EN), then the associated samplers in the pseudo differential operation must be configured manually in this register to have the same SAMP_GAIN. For example if CHAN_CFG0 is set for PD mode, the associated differential samplers 0 and 1 should be set to the same gain. Default Value: 0

20.1.10 HPPASS_SAR_CFG_SAMPLE_TIME0

Sample Time configuration register

Address: 0x42B80410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SAMPLE_TIME [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SAMPLE_TIME [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	SAMPLE_TIME	Sample time (aperture) in given by (SAMPLE_TIME+1) clock cycles of CLK_HF/2. The range is 0..1023, which results in: 1*CLK_HF/2 - 1024 * CLK_HF/2 cycles There are 3 sample time registers and each ENTRY (SEQ_ENTRY.SAMPLE_TIME_SEL) can select DISABLED if no sample time is needed (see below) or one of these 3 registers if sample time is needed. WHEN SAMPLE TIME IS NOT REQUIRED: If 0 sample time is selected in SEQ_ENTRY.SAMPLE_TIME_SEL, this means when the trigger for that ENTRY is asserted, all the channels in that ENTRY are transitioned to HOLD state immediately and are queued for conversion. This scenario works well for DIRECT CHANNELS, because each input has a dedicated sampler which is either sampling, holding for conversion. Therefore after a given trigger, if the subsequent trigger is spaced out is time greater than or equal to the time required for all ENTRY channels to convert, plus a minimum sample time, no additional sample time (as would be programmed in this register) will be needed. WHEN SAMPLE TIME IS REQUIRED In the case of MUXed samplers, sample time is normally required because the routing is switched to the configured selections (SEQ_TABLE.MUXn_SEL) on trigger assertion. In this case minimum sample time is required. In a special case, however, if the mux selection is fixed and not changing, then it is equivalent to a direct connection, and in that case additional sampling time may not be required. Default Value: 31

20.1.11 HPPASS_SAR_CFG_FIR_CFG0

FIR configuration register

Address: 0x42B80420

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			CHANNEL_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							WAIT_TAP_INIT

Bits	23	22	21	20	19	18	17	16
SW Access	RW				None			
HW Access	R				None			
Name	RANGE_SEL [23:20]				None [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW			None			
HW Access	None	R			None			
Name	None	FIFO_SEL [30:28]			None [27:24]			

Bits	Name	Description
30 : 28	FIFO_SEL	FIFO selections. Select 1 of the 4 for FIFOs for data storage There is a global setting for the number of FIFOs to be configured in LPPASS_MMIO/FIFO_CFG/CFG. If te indicated FIFO in this field is not configured, this setting will be ignored. Default Value: 0 **0x0: DISABLED :** **0x1: FIFO_0 :** **0x2: FIFO_1 :** **0x3: FIFO_2 :** **0x4: FIFO_3 :**
23 : 20	RANGE_SEL	Range detection. Select 1 of the 8 RANGE detection modules Default Value: 0 **0x0: DISABLED :** **0x1: RANGE_0 :** **0x2: RANGE_1 :**

20.1.11 HPPASS_SAR_CFG_FIR_CFG0 (continued)

		0x3: RANGE_2 :
		0x4: RANGE_3 :
		0x5: RANGE_4 :
		0x6: RANGE_5 :
		0x7: RANGE_6 :
		0x8: RANGE_7 :
8	WAIT_TAP_INIT	Wait for 16 samples before the first output is stored into a FIR_RESULT register or FIFO. This allows the user to ignore the FIR outputs until the FIR pipeline is initialized. . Default Value: 1
		0x0: DISABLED :
		0x1: ENABLED :
4 : 0	CHANNEL_SEL	Select which SAR channel will be the source for a given FIR input. When a new conversion output is available, the 16-tap FIR calculation is initiated (17 cycles for 16 taps), and a new FIR output is generated. Default Value: 0
		0x0: DISABLED :
		0x1: CHANNEL_0 :
		0x2: CHANNEL_1 :
		0x3: CHANNEL_2 :
		0x4: CHANNEL_3 :
		0x5: CHANNEL_4 :
		0x6: CHANNEL_5 :
		0x7: CHANNEL_6 :
		0x8: CHANNEL_7 :
		0x9: CHANNEL_8 :
		0xa: CHANNEL_9 :
		0xb: CHANNEL_10 :
		0xc: CHANNEL_11 :
		0xd: CHANNEL_12 :

20.1.11 HPPASS_SAR_CFG_FIR_CFG0 (continued)

0xe: CHANNEL_13 :

0xf: CHANNEL_14 :

0x10: CHANNEL_15 :

0x11: CHANNEL_16 :

0x12: CHANNEL_17 :

0x13: CHANNEL_18 :

0x14: CHANNEL_19 :

0x15: CHANNEL_20 :

0x16: CHANNEL_21 :

0x17: CHANNEL_22 :

0x18: CHANNEL_23 :

0x19: CHANNEL_24 :

0x1a: CHANNEL_25 :

0x1b: CHANNEL_26 :

0x1c: CHANNEL_27 :

20.1.12 HPPASS_SAR_CFG_CHAN_CFG0

SAR Channel configuration register

Address: 0x42B80430

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						SIGNED	DIFFEREN-TIAL_EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	RESERVED_15_12 [15:12]				RESERVED_11_8 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				None			
HW Access	R				None			
Name	RANGE_SEL [23:20]				None [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	FIFO_SEL [30:28]			None	AVG_SEL [26:24]		

Bits	Name	Description
30 : 28	FIFO_SEL	FIFO Select. Select 1 of the 4 for FIFO data storage. There is a global setting for the number of FIFOs to be configured in LPPASS_MMIO/FIFO_CFG/CFG. If te indicated FIFO in this field is not configured, this setting will be ignored. Default Value: 0 **0x0: DISABLED :** **0x1: FIFO_0 :** **0x2: FIFO_1 :** **0x3: FIFO_2 :** **0x4: FIFO_3 :**
26 : 24	AVG_SEL	Enable averaging for this channel. This implementation is accumulation only. There is no hardware shift option. For example, if AVG_2 is selected, the RESULT register (or FIFO) will contain a 13-bit result, for AVG_4 the RESULT register will contain a 14-bit result, etc. Default Value: 0 **0x0: DISABLED :** **0x1: AVG_2 :**

20.1.12 HPPASS_SAR_CFG_CHAN_CFG0 (continued)

		0x2: AVG_4 :
		0x3: AVG_8 :
		0x4: AVG_16 :
		0x5: RESERVED_5 :
		0x6: RESERVED_6 :
		0x7: RESERVED_7 :
23 : 20	RANGE_SEL	Enable and select a RANGE resource for this channel Default Value: 0
		0x0: DISABLED :
		0x1: RANGE_0 :
		0x2: RANGE_1 :
		0x3: RANGE_2 :
		0x4: RANGE_3 :
		0x5: RANGE_4 :
		0x6: RANGE_5 :
		0x7: RANGE_6 :
		0x8: RANGE_7 :
15 : 12	RESERVED_15_12	Reserved, leave these bits as default 0 state Default Value: 0
11 : 8	RESERVED_11_8	Reserved, leave these bits as default 0 state Default Value: 0
1	SIGNED	Signed Data Option Default Value: 0
		0x0: UNSIGNED :
		Result data unsigned
		0x1: SIGNED :
		Result data is signed (sign extended if needed)
0	DIFFERENTIAL_EN	Differential Enable. Default Value: 0
		0x0: DISABLED :
		Single Ended operation

20.1.12 HPPASS_SAR_CFG_CHAN_CFG0 (continued)

0x1: ENABLED :

Pseudo Differential operation
NOTE: Averaging (AVG_SEL below) is not available for this channel if Pseudo Differential is enabled. AVG_SEL must be set to the default DISABLED.
POS and NEG inputs are simultaneously sampled, and then subtracted in hardware. Result is stored in the associated POS Channel RESULT reg
Channels 0 - 11: There are 6 differential (even, odd) pairs.
Example: Setting DIFFERENTIAL_EN in CHAN CFG 0 configures Sampler 0 as the POS input, and then Channel 1/Sampler 1 is automatically set as the NEG input. The result is stored in CHAN_RESULT 0.
Channels 12 - 27: These are muxed channels which operate with 4 Samplers. so there are two differential pair groups
Pair 1: CHAN 12-15, Sampler 12 (POS), CHAN 16-19, Sampler 13 (NEG)
Pair 2: CHAN 20-23, Sampler 14 (POS), CHAN 24-27, Sampler 15 (NEG)
Any channel of the even sampler could be PD-paired with any channel from the odd sampler
Example: Setting DIFFERENTIAL_EN in CHAN_CFG 14, implies that Sampler 12 is the POS input where the SEQ_ENTRY.MUX0_SEL select must be set to 2 in the Entry configuration (see SEQ_ENTRY.MUXED_SAMPLER_EN for this mapping). Sampler 13 is automatically configured as the NEG input where input selection/routing is controlled by the SEQ_ENTRY.MUX1_SEL .The result is stored in CHAN_RESULT 14.
This setting will be ignored for the NEG input channels 1,3,5,7,9,11, 16-19, 24-28

20.1.13 HPPASS_SAR_CFG_RANGE_CFG0

Range detect configuration register.

Address: 0x42B804B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						RANGE_COND [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	RANGE_COND	Range condition select. Default Value: 0 **0x0: BELOW :** result < RANGE_LOW **0x1: INSIDE :** RANGE_LOW <= result < RANGE_HIGH **0x2: ABOVE :** result > RANGE_HIGH **0x3: OUTSIDE :** result < RANGE_LOW || result >= RANGE_HIGH

20.1.14 HPPASS_SAR_CFG_RANGE_LOW0

Range detect low value register.

Address: 0x42B804D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RANGE_LOW [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RANGE_LOW [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RANGE_LOW	Low threshold for range detect NOTE on unsigned/signed ADC RESULT RANGE (inclding averaging): If the channel that is selecting a given RANGE is declared as signed (CHAN_CFG.SIGNED), then the RANGE_HIGH and RANGE_LOW will be considered as signed 16-bit values, otherwise they will be considered as unsigned 16-bit values. FIR RESULT RANGE:The FIR output is considered as signed, therefore the RANGE_HIGH and RANGE_LOW for FIR comparison are always considered as signed 16-bit values. Default Value: 0

20.1.15 HPPASS_SAR_CFG_RANGE_HIGH0

Range detect high value register.

Address: 0x42B804F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RANGE_HIGH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RANGE_HIGH [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RANGE_HIGH	High threshold for range detect See RANGE_LOW for signed/unsigned usage rules Default Value: 0

20.1.16 HPPASS_SAR_CFG_CHAN_RESULT0

Channel result register

Address: 0x42B80510

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RESULT	SAR conversion working data of the channel. The data is written here if the corresponding bit if RESULT_MASK is set. (default is to write to CHAN_RESULT). The RESULT_MASK may be cleared if the channel data is targeted for the FIFO. Default Value: Undefined

20.1.17 HPPASS_SAR_CFG_FIR_RESULT0

FIR result register

Address: 0x42B80580

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RESULT	FIR output data. The data is written here if the corresponding bit in RESULT_MASK is set. (default is to write to FIR_RESULT) . The RESULT_MASK may be cleared if the FIR data is targeted for the FIFO. Default Value: Undefined

20.1.18 HPPASS_SAR_CFG_RESULT_MASK

Channel result mask

Address: 0x42B80590

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CHAN_RESULT_MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CHAN_RESULT_MASK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CHAN_RESULT_MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	FIR_RESULT_MASK [31:30]		None [29:28]		CHAN_RESULT_MASK [27:24]			

Bits	Name	Description
31 : 30	FIR_RESULT_MASK	If set (default) the FIR_RESULT register will be used to store SAR conversion data for a given Entry and the associated ENTRY_DONE Interrupt will be generated. If this bit isn't set, the channel must be configured to store the result in a FIFO and the ENTRY_DONE Interrupt will not be generated. Default Value: 3
27 : 0	CHAN_RESULT_MASK	If set (default) the CHAN_RESULT register will be used to store SAR conversion data for a given Entry and the associated ENTRY_DONE Interrupt will be generated. If this bit isn't set, the channel must be configured to store the result in a FIFO and the ENTRY_DONE Interrupt will not be generated. Default Value: 268435455

20.1.19 HPPASS_SAR_CFG_RESULT_UPDATED

Channel result register status

Address: 0x42B80594

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	CHAN_RESULT_UPDATED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW1S							
Name	CHAN_RESULT_UPDATED [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	RW1S							
Name	CHAN_RESULT_UPDATED [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C		None		RW1C			
HW Access	RW1S		None		RW1S			
Name	FIR_RESULT_UPDATED [31:30]		None [29:28]		CHAN_RESULT_UPDATED [27:24]			

Bits	Name	Description
31 : 30	FIR_RESULT_UPDATED	Each bit will be set when the corresponding FIR_RESULT register is updated with a new result. Write 1 to clear. Default Value: 0
27 : 0	CHAN_RESULT_UPDATED	Each bit will be set when the corresponding CHAN_RESULT register is updated with a new result. Write 1 to clear. Default Value: 0

20.1.20 HPPASS_SAR_CFG_RANGE_STATUS

Range status register

Address: 0x42B80598

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	CHAN_RANGE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW1S							
Name	CHAN_RANGE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	RW1S							
Name	CHAN_RANGE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C		None		RW1C			
HW Access	RW1S		None		RW1S			
Name	FIR_RANGE [31:30]		None [29:28]		CHAN_RANGE [27:24]			

Bits	Name	Description
31 : 30	FIR_RANGE	A given bit in this register will be set if the conversion result (after averaging) of that channel met the condition specified by the selected RANGE registers. Write with '1' to clear bit. Default Value: 0
27 : 0	CHAN_RANGE	A given bit in this register will be set if the conversion result (after averaging) of that channel met the condition specified by the selected RANGE registers. Write with '1' to clear bit. Default Value: 0

20.1.21 HPPASS_SAR_CFG_SAR_STATUS

SAR status register

Address: 0x42B8059C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	BUSY	None [30:24]						

Bits	Name	Description
31	BUSY	If high then the SAR is busy with a conversion. This bit is always high when CONTINUOUS is set. Firmware should wait for this bit to be low before putting the SAR in power down. Default Value: 0

20.1.22 HPPASS_SAR_CFG_RESULT_OVERFLOW

Entry overflow status

Address: 0x42B805A0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	ENTRY_RESULT_OVF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW1C	
HW Access	None						RW1S	
Name	None [23:18]						FIR_RESULT_OVF [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 16	FIR_RESULT_OVF	The associated bit is set in this register if the new FIR results are written before the associated SAR_RESULT_INTR/FIR_DONE bit has been cleared from the previous trigger.. This bit may be cleared by writing a '1' to the associated bit. Any bit set in this register will cause the HPPASS_INTR.RESULT_OVF bit to be set and this may be confgured to generate an interrupt (see HPPASS_MMIO). Default Value: 0
7 : 0	ENTRY_RESULT_OVF	The associated bit is set in this register if the new Entry results are written before the associated SAR_RESULT_INTR/ENTRY_DONE bit has been cleared from the previous trigger. This bit may be cleared by writing a '1' to the associated bit. Any bit set in this register will cause the HPPASS_INTR.RESULT_OVF bit to be set and this may be confgured to generate an interrupt (see HPPASS_MMIO). Default Value: 0

20.1.23 HPPASS_SAR_CFG_ENTRY_TR_COLLISION

Entry trigger collision status

Address: 0x42B805A4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	ENTRY_COL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	ENTRY_COL	The associated bit is set in this register if an Entry is triggered while processing for the previous trigger is still in progress, including sampling, conversion and post processing. Write a '1' to clear status in this register. Any bit set in this register will sety the HPPASS_INTR.ENTRY_TR_COLLISION to be set and this may be configured to generate an interrupt (see HPPASS_MMIO/HPPASS_INTR register). Default Value: 0

20.1.24 HPPASS_SAR_CFG_ENTRY_HOLD_VIOLATION

Entry hold violation status

Address: 0x42B805A8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	HOLD_VIOL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	HOLD_VIOL	The associated bit is set in this register if an Entry (and it's associated samplers) are in HOLD state greater than the ENTRY_HOLD_CNT value (see directly below), which indicates the associated channel results may not meet ADC accuracy specs. Write a '1' to clear status in this register. Any bit set in this register will sety the HPPASS_INTR.ENTRY_HOLD_VIOLATION to be set and this may be configured to generate an interrupt (see HPPASS_MMIO/HPPASS_INTR register). Default Value: 0

20.1.25 HPPASS_SAR_CFG_ENTRY_HOLD_CNT

Entry hold violation count

Address: 0x42B805AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HOLD_CNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	HOLD_CNT	This is the a global max HOLD count applied to all Entries. (See ENTRY_HOLD_VIOLATION above). The resolution of each count is 16 high frequency clock counts. For example, in PSOC™ C3 the high frequency clock is 160MHz, so each count will be 16/ 160MHz = 100ns. The default max HOLD time is 3us, thus the default value for this register is 29 (30 counts) NOTE: The violation can be asserted in the range of HOLD_CNT and HOLD_CNT+1 Default Value: 29

20.1.26 HPPASS_SAR_CFG_SAR_RESULT_INTR

SAR Interrupt register

Address: 0x42B80600

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	ENTRY_DONE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW1C	
HW Access	None						RW1S	
Name	None [23:18]						FIR_DONE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 16	FIR_DONE	The associated FIR_DONE(N) status is set. The FIR_RESULT registers for the FIR modules are ready for reading Default Value: 0
7 : 0	ENTRY_DONE	The associated ENTRY_DONE(N) status is set. The CHAN_RESULT registers for channels in this entry are ready for reading. Default Value: 0

20.1.27 HPPASS_SAR_CFG_SAR_RESULT_INTR_SET

SAR Interrupt request set register

Address: 0x42B80604

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	ENTRY_DONE_SET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW1S	
HW Access	None						A	
Name	None [23:18]						FIR_DONE_SET [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 16	FIR_DONE_SET	Write with '1' to set corresponding bit in interrupt request register. (a write of '0' has no effect). Default Value: 0
7 : 0	ENTRY_DONE_SET	Write with '1' to set corresponding bit in interrupt request register. (a write of '0' has no effect). Default Value: 0

20.1.28 HPPASS_SAR_CFG_SAR_RESULT_INTR_MASK

SAR Interrupt request mask

Address: 0x42B80608

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ENTRY_DONE_MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						FIR_DONE_MASK [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 16	FIR_DONE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7 : 0	ENTRY_DONE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

20.1.29 HPPASS_SAR_CFG_SAR_RESULT_INTR_MASKED

SAR Interrupt request masked

Address: 0x42B8060C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ENTRY_DONE_MASKED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						R	
HW Access	None						W	
Name	None [23:18]						FIR_DONE_MASKED [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 16	FIR_DONE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
7 : 0	ENTRY_DONE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

20.1.30 HPPASS_SAR_CFG_SAR_RANGE_INTR

SAR Range Interrupt register

Address: 0x42B80610

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	RANGE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	RANGE	The associated RANGE(N) status is set. The associated RANGE_STATUS is also set and available for reading. Default Value: 0

20.1.31 HPPASS_SAR_CFG_SAR_RANGE_INTR_SET

SAR Range Interrupt request set register

Address: 0x42B80614

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	RANGE_SET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	RANGE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

20.1.32 HPPASS_SAR_CFG_SAR_RANGE_INTR_MASK

SAR Range Interrupt request mask

Address: 0x42B80618

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RANGE_SET_MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	RANGE_SET_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

20.1.33 HPPASS_SAR_CFG_SAR_RANGE_INTR_MASKED

SAR Range Interrupt request masked

Address: 0x42B8061C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RANGE_SET_MASKED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	RANGE_SET_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

20.1.34 HPPASS_SAR_CFG_CHAN_RESULT_PACKED0

Channel result register packed with 2 results per register

Address: 0x42B80630

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT_EVEN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT_EVEN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	RESULT_ODD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	RESULT_ODD [31:24]							

Bits	Name	Description
31 : 16	RESULT_ODD	Odd numbered channel results. (e.g. 1, 3, 5, ... , 27) Default Value: Undefined
15 : 0	RESULT_EVEN	Even numbered channel results (e.g. 0, 2, 4, ... , 26) Default Value: Undefined

20.1.35 HPPASS_SAR_CFG_AROUTE_CTRL_MODE

AROUTE control mode

Address: 0x42B80700

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	MUX3_CTRL [7:6]		MUX2_CTRL [5:4]		MUX1_CTRL [3:2]		MUX0_CTRL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	AROUTE_ENABLED	TEMP-SENSE_ENABLED	None [29:24]					

Bits	Name	Description
31	AROUTE_ENABLED	Global AROUTE Enable 1: Enabled (default), controlled using selected MUXn_CTRL method 0: Disabled, all switches open, overrides all other switch controls. Default Value: 1
30	TEMPSENSE_ENABLED	NOTE: This register field has been depricated and no longer in use. It may be left at the default value of '1' or it may be cleared to '0'. Default Value: 1
7 : 6	MUX3_CTRL	The associated AROUTE MUX is controlled by the SAR sequencer or by FW, or AC Default Value: 0
5 : 4	MUX2_CTRL	The associated AROUTE MUX is controlled by the SAR sequencer or by FW, or AC Default Value: 0
3 : 2	MUX1_CTRL	The associated AROUTE MUX is controlled by the SAR sequencer or by FW, or AC Default Value: 0

20.1.35 HPPASS_SAR_CFG_AROUTE_CTRL_MODE (continued)

1 : 0	MUX0_CTRL	The associated AROUTE MUX is controlled by the SAR sequencer by static FW setting, or AC 0 (default) - Controlled by SAR sequencer using values in SEQ_ENTRY table MUXi_SEL fields or ENTRY_MUX_SEL_ALIAS register. This programming is explicit and easy to use and is intended for the majority of applications Setting 1 and 2 below are for advanced usage only. These settings override any SEQ_ENTRY setting. Therefore care must be taken to program SEQ_ENTRYs to NOT mix AROUTE_CTRL_MODE settings for the MUXes used in a given ENTRY. Also, for a given MUX using any of these below modes, only 1 ENTRY should specify the usage of that MUX. 1 - Controlled by FW using AROUTE_FW_SET and AROUTE_FW_CLR registers below. This mode must be used with care. Configuration is by individual switch control - buy only 1 switch may be set for each MUX, otherwise the routes will be shorted to each other. 2 - Controlled by AC using ACTRLR/TIMER_TABLE/TT_CFG3/SAR_AROUTE_TR and SAR_AROUTE_SEL fields. When this mode is used, the AC must be programmed to fully control that ENTRY. In that case, for example, the external trigger will be routed to the AC code that sets the MUX, triggers that ENTRY, waits for the ENTRY to be completed, switched the MUX to the next selection, triggers that ENTRY again, etc. Default Value: 0

20.1.36 HPPASS_SAR_CFG_AROUTE_FW_CTRL

AROUTE firmware switch control set (individual)

Address: 0x42B80704

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	MUX1_SW3	MUX1_SW2	MUX1_SW1	MUX1_SW0	MUX0_SW3	MUX0_SW2	MUX0_SW1	MUX0_SW0

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	MUX3_SW3	MUX3_SW2	MUX3_SW1	MUX3_SW0	MUX2_SW3	MUX2_SW2	MUX2_SW1	MUX2_SW0

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	MUX3_SW3	Default Value: 0
14	MUX3_SW2	Default Value: 0
13	MUX3_SW1	Default Value: 0
12	MUX3_SW0	Default Value: 0
11	MUX2_SW3	Default Value: 0
10	MUX2_SW2	Default Value: 0
9	MUX2_SW1	Default Value: 0
8	MUX2_SW0	Default Value: 0
7	MUX1_SW3	Default Value: 0
6	MUX1_SW2	Default Value: 0
5	MUX1_SW1	Default Value: 0
4	MUX1_SW0	Default Value: 0
3	MUX0_SW3	Default Value: 0
2	MUX0_SW2	Default Value: 0
1	MUX0_SW1	Default Value: 0
0	MUX0_SW0	Firmware control: 0=open, 1=close switch. Write with '1' to set bit. To clear this bit write a '1' to the associated bit in AROUTE_FW_CLR register Default Value: 0

20.1.37 HPPASS_SAR_CFG_AROUTE_FW_CTRL_CLR

AROUTE firmware switch control clear (individual)

Address: 0x42B80708

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	MUX1_SW3	MUX1_SW2	MUX1_SW1	MUX1_SW0	MUX0_SW3	MUX0_SW2	MUX0_SW1	MUX0_SW0

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	MUX3_SW3	MUX3_SW2	MUX3_SW1	MUX3_SW0	MUX2_SW3	MUX2_SW2	MUX2_SW1	MUX2_SW0

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	MUX3_SW3	Default Value: 0
14	MUX3_SW2	Default Value: 0
13	MUX3_SW1	Default Value: 0
12	MUX3_SW0	Default Value: 0
11	MUX2_SW3	Default Value: 0
10	MUX2_SW2	Default Value: 0
9	MUX2_SW1	Default Value: 0
8	MUX2_SW0	Default Value: 0
7	MUX1_SW3	Default Value: 0
6	MUX1_SW2	Default Value: 0
5	MUX1_SW1	Default Value: 0
4	MUX1_SW0	Default Value: 0
3	MUX0_SW3	Default Value: 0
2	MUX0_SW2	Default Value: 0
1	MUX0_SW1	Default Value: 0
0	MUX0_SW0	Write '1' to clear corresponding bit in AROUTE_FW_CTRL. A read of this register returns the values of AROUTE_FW_CTRL. Default Value: 0

20.1.38 HPPASS_SAR_CFG_AROUTE_STATUS

AROUTE switch status

Address: 0x42B8070C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	MUX1_SW3	MUX1_SW2	MUX1_SW1	MUX1_SW0	MUX0_SW3	MUX0_SW2	MUX0_SW1	MUX0_SW0

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	MUX3_SW3	MUX3_SW2	MUX3_SW1	MUX3_SW0	MUX2_SW3	MUX2_SW2	MUX2_SW1	MUX2_SW0

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	MUX3_SW3	Default Value: 0
14	MUX3_SW2	Default Value: 0
13	MUX3_SW1	Default Value: 0
12	MUX3_SW0	Default Value: 0
11	MUX2_SW3	Default Value: 0
10	MUX2_SW2	Default Value: 0
9	MUX2_SW1	Default Value: 0
8	MUX2_SW0	Default Value: 0
7	MUX1_SW3	Default Value: 0
6	MUX1_SW2	Default Value: 0
5	MUX1_SW1	Default Value: 0
4	MUX1_SW0	Default Value: 0
3	MUX0_SW3	Default Value: 0
2	MUX0_SW2	Default Value: 0
1	MUX0_SW1	Default Value: 0
0	MUX0_SW0	Read back the current state of the associated switch control (regardless of mode) Default Value: 0

20.1.39 HPPASS_SAR_CFG_TEMPSENSE_CTRL

Temperture Sensor Control

Address: 0x42B80710

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TEMP-SENSE_CURRENT_-SEL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TEMPSENSE_CUR-RENT_SEL	Used for Delta Vbe Temperature Sensor Algoritm (see BROS for full details) 0: BJT current is 1uA (default) 1: Add 8uA to BJT current Default Value: 0

20.1.40 HPPASS_SAR_FIR0_FIR_COEFS0

FIR Coeffecients

Address: 0x42B80800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	COEF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	COEF [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COEF	FIR Coefficient Value The coefficient values can range from -1+1/215 to 1-1/215 with a resolution of 1/215. The coefficient uses twos-complement notation and the decimal point is fixed to the right of the most significant bit. Examples: -0.25 = 0xE000 and 0.25 = 0x2000 NOTE: The max absolute value of the FIR gain must be less than 8 (sum of the coeffients), otherwise the result may overflow the allocated 16-bits. Default Value: 0

20.1.41 HPPASS_SAR_FIR0_FIR_TAPS0

FIR Taps

Address: 0x42B80840

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	TAP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	TAP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	TAP	FIR Tap Value In normal operation R/W by hardware Only when HPPASS IP is enabled and SAR is enabled - these registers may be written to and read by software, typically for debug puposes. Default Value: 0

20.1.42 HPPASS_CSG_SLICE0_CMP_CFG

Comparator Control Register

Address: 0x42BB0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		None	RW
HW Access	None		R		R		None	R
Name	None [7:6]		CMP_BLANK_MODE [5:4]		CMP_NEG_SEL [3:2]		None	CMP_POS_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		RW			
HW Access	None		R		R			
Name	None [15:14]		CMP_EDGE_MODE [13:12]		CMP_BLANK_TR_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							CMP_POLARITY

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	CMP_POLARITY	Comparator Polarity Default Value: 0 **0x0: True :** Comparator output is not intverted **0x1: INV :** Comparator output is inverted
13 : 12	CMP_EDGE_MODE	Comparator signal mode for Interrupt generation and AC status Default Value: 0 **0x0: DISABLE :** Disabled, no interrupts will be asserted **0x1: RISING :** Rising edge

20.1.42 HPPASS_CSG_SLICE0_CMP_CFG (continued)

		0x2: FALLING : Falling edge **0x3: BOTH :** Both rising and falling edges
11 : 8	CMP_BLANK_TR_SEL	Copmarator Blank Trigger Select. Select one of the available input HPPASS HW/FW LEVEL mode triggers. Default Value: 0 **0x0: DISABLED :** **0x1: TR0 :** **0x2: TR1 :** **0x3: TR2 :** **0x4: TR3 :** **0x5: TR4 :** **0x6: TR5 :** **0x7: TR6 :** **0x8: TR7 :**
5 : 4	CMP_BLANK_MODE	Comparator Blanking Mode. Select a level input trigger from CMP_BLANK_TR_SEL to gate the comparators output of this slice to 0. Polarity of active signal is selectable. Default Value: 0 **0x0: DISABLED :** Comparator output is not gated **0x1: GATE_ON_ONE :** Comparator output is gated to 0 by a '1' level **0x2: GATE_ON_ZERO :** Comparator output is gated to 0 by a '0' level
3 : 2	CMP_NEG_SEL	Comparator Negative Input Select (Select positive input from CMP_POS_SEL) Default Value: 0 **0x0: DAC :** DAC is negative input **0x1: RESERVED_1 :** Reserved

20.1.42 HPPASS_CSG_SLICE0_CMP_CFG (continued)

		0x2: AIN_NA : Analog input NA **0x3: AIN_NB :** Analog input NB
0	CMP_POS_SEL	Comparator Positive Input Select (Select negative input from CMP_NEG_SEL) Default Value: 0 **0x0: AIN_PA :** Analog input PA **0x1: AIN_PB :** Analog input PB

20.1.43 HPPASS_CSG_SLICE0_DAC_CFG

DAC Control Register

Address: 0x42BB0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DAC_TR_UPDATE_SEL [7:4]				DAC_TR_START_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	None	RW		
HW Access	R	R	R	R	None	R		
Name	DAC_PARAM_SYNC_EN	DAC_CASCADE_EN	DAC_SKIP_TR_EN	DAC_CONT	None	DAC_MODE [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW				None			
HW Access	R				None			
Name	DAC_STEP [23:20]				None [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW			None		RW	
HW Access	None	R			None		R	
Name	None	DAC_DEGLITCH [30:28]			None [27:26]		DAC_STEP [25:24]	

Bits	Name	Description
30 : 28	DAC_DEGLITCH	DAC Deglitch Configuration. Default is disabled. If enabled, on any DAC value update,the CMP output is latched in it's current state for the number of cycles indicated. Default Value: 0 **0x0: DISABLED :** **0x1: ONE_CYCLE :** **0x2: TWO_CYCLES :** **0x3: THREE_CYCLES :** **0x4: FOUR_CYCLES :** **0x5: FIVE_CYCLES :** **0x6: SIX_CYCLES :** **0x7: SEVEN_CYCLES :**

20.1.43 HPPASS_CSG_SLICE0_DAC_CFG (continued)

25 : 20	DAC_STEP	Static value of 6 bit DAC step size. Step size is DAC_STEP +1 (default is '1') , range is 1 - 64, only valid in SLOPE/LUT modes. NOTE: In LUT mode each step jumps to a new LUT value on WORD boundaries. So for example: DAC_STEP = 0 (default Step size of 1) advances the LUT address by 4 (LUT WORD boundary) DAC_STEP = 1 (Step size of 2) advances the LUT address by 8, etc Default Value: 0
15	DAC_PARAM_SYNC_EN	Parameter Sync Enable. 0: Disabled. Always update parameters on DAC trigger (as defined by DAC_MODE) 1: Enabled. Only update parameters on DAC trigger if DAC_PARAM_SYNC.READY is set. Default Value: 0
14	DAC_CASCADE_EN	Cascade Enable. Synchronize parameter update with previous CSG slice in the case of multi-phase operation. 0: Disabled. 1: Enabled. This CSG updates it's parameters on a DAC trigger only after the previous numbered CSG has updated it's parameters. Default Value: 0
13	DAC_SKIP_TR_EN	Skip the first DAC hardware update trigger afer a mode is enabled. Allows for a minimum of a full trigger period before the first hardware update occurs. 0: First trigger following DAC_MODE_EN updates the DAC value. 1: First trigger following DAC_MODE_EN is skipped. Following trigger updates the DAC value. Default Value: 0
12	DAC_CONT	DAC Continuous Mode (Only valid for Slope and LUT modes) 0: Slope/LUT operation is One-Shot, last output value is held 1: Slope/LUT operation is Continuous, operation is restarted when end value is reached Default Value: 0
10 : 8	DAC_MODE	DAC Operating Mode. This setting may only be changed when the mode is disabled. See DAC_-MODE_START. Default Value: 0 **0x0: BUFFERED :** Single Value Buffered Mode Transfer data from DAC_VAL_A to DAC_VAL and assert DAC_BUF_EMPTY interrupt. The first transfer occurs when the mode is started (see DAC_MODE_START). Subsequent transfers occur on the DAC_TR_UPDATE trigger. This mode will stay in effect until the mode is stopped. **0x1: HYSTERETIC :** Two Value Hysteretic Buffered Mode Toggle DAC_VAL between a high threshold (DAC_VAL_A) and a low threshold (DAC_VAL_B) on DAC_TR_UPDATE trigger level.. The first transfer occurs from DAC_VAL_A (high threshold) to DAC_VAL when the mode is start-ed (see DAC_MODE_START). When the trigger transitions from 0 to 1 (e.g. rising voltage), DAC_VAL_B is output (low thresh-old) When the trigger transitions from 1 to 0 (e.g. falling voltage), DAC_VAL_A is output (high thresh-old) On the DAC_VAL_B update a DAC_BUF_EMPTY interrupt and both the A and B values are buff-ered and may be updated. (See DAC_PARAM_SYNC_EN to enable synchronized parameter updates.) This mode will stay in effect until the mode is stopped. NOTE: The comparator may be used in this mode as an UPDATE trigger - which may also be inverted to provide flexibility.

20.1.43 HPPASS_CSG_SLICE0_DAC_CFG (continued)

0x2: SLOPE_RISING :

Rising Slope Mode
DAC_VAL_A is the start value, DAC_VAL_B is the end value. Configure DAC_STEP if needed and DAC_PERIOD if selected as the DAC_TR_UPDATE trigger. It is assumed that DAC_VAL_A < DAC_VAL_B for Rising Slope Mode.
DAC_VAL_A (start value) is transferred to DAC_VAL when the mode is started (see DAC_-MODE_START) and a DAC_SLOPE_START interrupt is generated.
On the UPDATE trigger, DAC_VAL is incremented by DAC_STEP
This continues until DAC_VAL >= DAC_VAL_B, at which point the operation completes and a DAC_SLOPE_DONE interrupt is generated.
If DAC_OONT is '0', operation is stopped on slope done and DAC_MODE_EN is reset to '0'
If DAC_CONT is '1' then the slope operation will continuously repeat.
In continuous mode, buffered parameters will be updated at the start of the ramp (see DAC_PARAM_SYNC_EN)

0x3: SLOPE_FALLING :

Falling Slope Mode
Same operation as Rising Slope Mode, but DAC_VAL is decremented. It is assumed that DAC_VAL_A is greater than DAC_VAL_B for Falling Slope Mode.
For other details - see Rising Slope Mode description

0x4: SLOPE_TRIANGULAR :

Triangular Slope Mode
This mode combines Rising and Falling Slope Modes. It first generates a Rising Slope, then when DAC_VAL >= DAC_VAL_B, a Falling Slope is generated. Then when DAC_VAL <= DAC_VAL_A the operation is completed.
For other details - see Rising Slope Mode description

0x5: LUT_FORWARD :

LUT Forward Mode
LUT waveform is output with incrementing addresses. DAC_VAL_A is start address and DAC_VAL_B is end address. DAC_STEP is the address step size. It is assumed that DAC_VAL_A < DAC_VAL_B.
NOTE: For LUT mode, the maximum update rate is limited to CLK_CSG/2 (i.e. Need at least 1 cycle gap between triggers)
For other details see Slope Rising Mode description

0x6: LUT_REVERSE :

LUT Reverse Mode
LUT waveform is output with decrementing addresses. DAC_VAL_A is start address and DAC_VAL_B is end address. DAC_STEP is the address step size. It is assumed that DAC_VAL_A > DAC_VAL_B.
NOTE: For LUT mode, the maximum update rate is limited to CLK_CSG/2 (i.e. Need at least 1 cycle gap between triggers)
For other details see Slope Rising Mode description

0x7: LUT_FWD_REV :

LUT Forward Reverse Mode
LUT waveform is output first with incrementing address, then when the address is >= DAC_VAL_B, a decrementint address is generated. When the address <= DAC_VAL_A, the operation is completed.
NOTE: For LUT mode, the maximum update rate is limited to CLK_CSG/2 (i.e. Need at least 1 cycle gap between triggers)
For other details see Slope Rising Mode description

20.1.43 HPPASS_CSG_SLICE0_DAC_CFG (continued)

7 : 4	DAC_TR_UPDATE_SEL	DAC Trigger Update Select. Select one of the triggers or internal events. See DAC_MODE for detailed operation. If one of the HPPASS HW or FW triggers are selected (see INFRA), then the trigger must be PULSE mode. In addition, the maximum frequency of the active trigger edge must be less than or equal to CSG CLOCK/2 (every other clock). Default Value: 0 **0x0: DISABLED :** **0x1: TR0 :** HW (or FW) input triggers **0x2: TR1 :** **0x3: TR2 :** **0x4: TR3 :** **0x5: TR4 :** **0x6: TR5 :** **0x7: TR6 :** **0x8: TR7 :** **0x9: AC :** AC trigger **0xa: DAC_PERIOD_TC :** Period terminal count. Period divider value is programmed in DAC_PERIOD register **0xb: CMP_LEVEL :** Use comparator output as Update Trigger: (Used only in Hysteretic Mode) With DAC_VAL_A as high threshold and DAC_VAL_B as low threshold, CMP 0 to 1 transition (voltage high) outputs DAC_VAL_B CMP 1 to 0 transition (voltage low) outputs DAC_VAL_A **0xc: CMP_LEVEL_INV :** Use inverted comparator output as Update Trigger (Used only in Hysteretic Mode) (e.g. in the case CMP_POLARITY is set)
3 : 0	DAC_TR_START_SEL	DAC Trigger Start Select. Select one of the HPPASS HW or FW triggers. Trigger must be PULSE mode (see INFRA). See DAC_MODE_START register to select this as the DAC start trigger. Default Value: 0 **0x0: DISABLED :** **0x1: TR0 :** HW (or FW) input triggers

20.1.43 HPPASS_CSG_SLICE0_DAC_CFG (continued)

0x2: TR1 :

0x3: TR2 :

0x4: TR3 :

0x5: TR4 :

0x6: TR5 :

0x7: TR6 :

0x8: TR7 :

0x9: AC :

AC trigger

20.1.44 HPPASS_CSG_SLICE0_DAC_PARAM_SYNC

DAC Parameter Synchronized Update

Address: 0x42BB0008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							READY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	READY	Use this bit to synchronize the update of multiple DAC parameters. If DAC_PARAM_SYNC_EN bit is '1', then set this bit after writes to all parameter registers (VAL_A, VAL_B, DAC_PERIOD, DAC_STEP) are complete to synchronize parameter update on a subsequent DAC trigger This allows for writes to multiple registers to be written before new parameters are updated to avoid partial updates. This bit is cleared by HW on the parameter update event. if DAC_PARAM_SYNC_EN is '0', this bit is ignored and parameters are updated on the following UPDATE trigger. NOTE: This bit can be used in conjunction with DAC_CASCADE_EN to synchronize the parameter update of multiple CSG slices. Default Value: 0

20.1.45 HPPASS_CSG_SLICE0_DAC_MODE_START

DAC Mode Start

Address: 0x42BB000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	RW1C	RW1C	None					
Name	FW_START	HW_START	None [29:24]					

Bits	Name	Description
31	FW_START	1: Starts the selected mode on this FW write. 0: Stops the selected mode. When this bit is cleared, the current DAC_VAL will not change unless it is over-written directly - or a new DAC mode is started. This field is automatically reset to '0' on DAC_SLOPE_DONE event (unless DAC_CONT is set for continous mode). Default Value: 0
30	HW_START	1: Wait for subsequent DAC_START_TR to start the selected mode. 0: Stops the selected mode. When this bit is cleared, the current DAC_VAL will not change unless it is over-written directly - or a new DAC mode is started. This field is automatically reset to '0' on DAC_SLOPE_DONE event (unless DAC_CONT is set for continous mode). Default Value: 0
0	BUSY	Read only bit to indicate that a DAC MODE has been enabled and is currently in progress. If FW_START is used to start the mode, then the FW_START bit is equivalent to this bit and low when the mode is completed or stopped. If HW_START is used to start the mode, then this status bit goes high on the DAC_START_TR event, and low when the mode is completed or stopped. NOTE: This read only bit refects the state of the DAC controller which is reset in DeepSleep and therefore this bit is not a retention bit. Default Value: 0

20.1.46 HPPASS_CSG_SLICE0_DAC_VAL_A

DAC Vaue A Buffer

Address: 0x42BB0010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						VALUE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	VALUE	DAC A Value, usage is mode dependent (see DAC_MODE) NOTE: In LUT modes this is the Start Address of the LUT waveform in byte address format (e.g. 0, 4, 8, ... 1F8, 1FC) Default Value: 0

20.1.47 HPPASS_CSG_SLICE0_DAC_VAL_B

DAC Value B Buffer

Address: 0x42BB0014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						VALUE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	VALUE	DAC B Value, usage is mode dependent (see DAC_MODE) NOTE: In LUT modes this is the End Address of the LUT waveform in byte address format (e.g. 0, 4, 8, ... 1F8, 1FC) Default Value: 0

20.1.48 HPPASS_CSG_SLICE0_DAC_PERIOD

DAC Period Buffer

Address: 0x42BB0018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	R					None		
Name	PERIOD_FRAC [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PERIOD_INT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				PERIOD_INT [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 8	PERIOD_INT	12-bit Integer Divide Value. Integer count by (1+PERIOD_INT). Allows for integer counts in the range [1, 4096]. Default Value: 0
7 : 3	PERIOD_FRAC	5-bit Fractional Divide Value. Allows for fractional count in the range [0, 31/32] Default Value: 0

20.1.49 HPPASS_CSG_SLICE0_DAC_VAL

DAC FW write

Address: 0x42BB001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						VALUE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	VALUE	Direct drive to DAC Hard IP for output. When DAC_MODE_EN is '0', the value in this register is output. A write to this register also STOPs the current DAC_MODE operation, and subsequent DAC triggers are ignored. Default Value: 0

20.1.50 HPPASS_CSG_SLICE0_DAC_STATUS

Read of Current DAC Value

Address: 0x42BB0020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DAC_VAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						W	
Name	None [15:10]						DAC_VAL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	DAC_VAL	Read Only value of current digital DAC output Default Value: 0

20.1.51 HPPASS_CSG_SLICE0_CMP_STATUS

Read of Comparator Value

Address: 0x42BB0024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							CMP_VAL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CMP_VAL	Read Only value of comparator output Default Value: 0

20.1.52 HPPASS_CSG_LUT_CFG0_LUT_DATA0

LUT Waveform Data

Address: 0x42BB0400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						DATA [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	DATA	DAC waveform Default Value: Undefined

20.1.53 HPPASS_CSG_CSG_CTRL

CSG control register

Address: 0x42BB0A00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				VDAC_OUT_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							CSG_-CLK_DIV_BYP

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	CSG_CLK_DIV_BYP	NOTE: This function has been deprecated and is no longer in use. This register bit is now reserved and should be left as '0' value. Default Value: 0
3 : 0	VDAC_OUT_SEL	Select the DAC output for SAR conversion Default Value: 0 **0x0: DISABLED :** Hi-Z (Disabled) **0x1: DAC0 :** Connect DAC0 to ADC input **0x2: DAC1 :** Connect DAC1 to ADC input **0x3: DAC2 :** Connect DAC2 to ADC input

20.1.53 HPPASS_CSG_CSG_CTRL (continued)

0x4: DAC3 :

Connect DAC3 to ADC input

0x5: DAC4 :

Connect DAC4 to ADC input

20.1.54 HPPASS_CSG_DAC_INTR

DAC Interrupt register

Address: 0x42BB0B00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	DAC_HW_START [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW1S							
Name	DAC_SLOPE_DONE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	RW1S							
Name	DAC_BUF_EMPTY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	DAC_BUF_EMPTY	When BUFFERED or HYSTERETIC mode is enabled, this interrupt is set when there is a DAC UPDATE trigger that transfers the buffered value(s) to active value(s) (see mode operation) and it means that the user may write new values to the buffer registers. Default Value: 0
15 : 8	DAC_SLOPE_DONE	When SLOPE or LUT mode is enabled, this interrupt is set when the SLOPE (or LUT waveform) has completed. This interrupt is also set periodically on the last value of a DAC SLOPE in continuous mode Default Value: 0
7 : 0	DAC_HW_START	This DAC_MODE operation was started with a HW START trigger. Default Value: 0

20.1.55 HPPASS_CSG_DAC_INTR_SET

DAC Interrupt request set register

Address: 0x42BB0B04

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	DAC_HW_START [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	A							
Name	DAC_SLOPE_DONE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S							
HW Access	A							
Name	DAC_BUF_EMPTY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	DAC_BUF_EMPTY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
15 : 8	DAC_SLOPE_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7 : 0	DAC_HW_START	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

20.1.56 HPPASS_CSG_DAC_INTR_MASK

DAC Interrupt request mask

Address: 0x42BB0B08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DAC_HW_START [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DAC_SLOPE_DONE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DAC_BUF_EMPTY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	DAC_BUF_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
15 : 8	DAC_SLOPE_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7 : 0	DAC_HW_START	Mask bit for corresponding bit in interrupt request register. Default Value: 0

20.1.57 HPPASS_CSG_DAC_INTR_MASKED

DAC Interrupt request masked

Address: 0x42BB0B0C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DAC_HW_START [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DAC_SLOPE_DONE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DAC_BUF_EMPTY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	DAC_BUF_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
15 : 8	DAC_SLOPE_DONE	Logical and of corresponding request and mask bits. Default Value: 0
7 : 0	DAC_HW_START	Logical and of corresponding request and mask bits. Default Value: 0

20.1.58 HPPASS_CSG_CMP_INTR

CMP Interrupt register

Address: 0x42BB0B10

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	CMP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CMP	This CMP(n) state has generated an interrupt request (see CSG_SLICE.CMP_CTRL.CMP_-MODE) Default Value: 0

20.1.59 HPPASS_CSG_CMP_INTR_SET

CMP Interrupt request set register

Address: 0x42BB0B14

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	CMP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CMP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

20.1.60 HPPASS_CSG_CMP_INTR_MASK

CMP Interrupt request mask

Address: 0x42BB0B18

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CMP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CMP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

20.1.61 HPPASS_CSG_CMP_INTR_MASKED

CMP Interrupt request masked

Address: 0x42BB0B1C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CMP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CMP	Logical and of corresponding request and mask bits. Default Value: 0

20.1.62 HPPASS_CSG_VDAC_OUT_BLANK

Blanking control for DAC Observability

Address: 0x42BB0B20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			BLANK_CNT [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	BLANK_CNT	This field enables blanking iin CLK_CSG cycles of the Comparator output when one of the DACs in a CSG SLICE is connected as an input for SAR conversion (See CTRL.VDAC_OUT_SEL) Disabled: BLANK_CNT = 0 Enabled : BLANK_CNT is between 1 and 31 When the DAC output is first connected to the SAR sampler input, the DAC may have a short transient (50ns). If the DAC is also an active input to the Comparator, this transient may cause false transitions on the Comparator output. To mitigate this, the Comparator output is latched for the duration of the BLANK_CNT value. This 5-bit value is the number of clock cycles to blank (latch) the Comparator output. This count is in CLK_CSG cycles as programmed in the MXPERI divider. The recommended value is 50ns blanking. Examples are: CLK_CSG @40MHz, use 2 cycles CLK_CSG @80MHz, use 4 cycles CLK_CSG @120MHz, use 8 cycles Default Value: 0

20.1.63 HPPASS_CSG_CSG_SYNC

CSG Sync Enable register

Address: 0x42BB0B30

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							SYNC_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	SYNC_EN	Risk Mitigation only. By default the CSG Hard IP and comparator output is synchronous to CLK_CSG. When this bit is set to '1', the CSG comparator output is double synced. Default Value: 0

20.1.64 HPPASS_ACTRLR_CTRL

Control register

Address: 0x42BD0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	0: HPPASS IP disabled - All mision logic and status is reset, all analog controls are disabled, all clocking is disabled (only available function is AHB access). NOTE: The SARADC trim is also reset and therefore the SAR needs to be re-calibrated, or previously saved trim values re-written if the IP is disabled. The only functioing system is the AHB register access when the IP is disabled. 1: HPPASS IP enabled. Clocks ungated, Reset negated Default Value: 0

20.1.65 HPPASS_ACTRLR_CMD_RUN

Run Command register

Address: 0x42BD0004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							RUN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	RUN	When firmware writes a '1' here it will trigger the Autonomous Controller to run, hardware clears this bit when the Autonomous Controller acknowledges the run command. This command has no action if the Autonomous Controller is already running. When the AC is stopped, the AC may be set back into running state by setting the CMD STATE to the address ofone ore more instructions and by setting this RUN bit to '1' Default Value: 0

20.1.66 HPPASS_ACTRLR_CMD_STATE

State Override register

Address: 0x42BD0008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				RW			
Name	None [7:4]				STATE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	STATE	Autonomous Controller CMD_STATE register. This register indicates which instruction the AC will start execution from when it receives a RUN command. Software can overrwrite this field only when STATUS.STATUS=STOPPED to set the AC to execute from a specific STATE when triggered by the RUN command. When first enabled, this register is reset to 0, so by default the AC starts executing at state 0. Default Value: 0

20.1.67 HPPASS_ACTRLR_BLOCK_STATUS

Block Ready status register

Address: 0x42BD0010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							READY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	READY	This bit reflects the AC BLOCK_READY condition, which can be polled by SW to determine if all the enabled blocks have settled and are ready for use Default Value: 0

20.1.68 HPPASS_ACTRLR_STATUS

AC Status register

Address: 0x42BD0020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				CUR_STATE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						W	
Name	None [15:10]						STATUS [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	STATUS	This field indicates if the Autonomous Controller is busy Default Value: 0 **0x0: STOPPED :** Autonomous Controller is stopped **0x1: RUNNING :** Autonomous Controller is running **0x2: RESERVED2 :** **0x3: RESERVED3 :**
3 : 0	CUR_STATE	This register indicates where in memory the AC is currently executing instructions. Default Value: 0

20.1.69 HPPASS_ACTRLR_CFG

AC Config register

Address: 0x42BD0024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			DOUT_EN [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	DOUT_EN	DOUT_EN controls the GPIO output drive mode though the HSIOM This register enables the DOUT feature, where up to 5 GPIOs can be controlled programatically with the AC (ACTRLR.TIMER_TABLE.TT_CFG0.DOUT). To use this feature: 1) The HSIOM (High Speed I/O Mux) device configuration must be set to select one or more DOUT/DOUT_EN bits to drive the associated GPIOs. 2) The associated bit(s) in this register must be set to enable the GPIO for output drive mode. 0 :DOUT[n] GPIO output disabled 1: DOUT[n] GPIO output enabled Default Value: 0

20.1.70 HPPASS_ACTRLR_CNTR_STATUS0

Loop/Interval counter status register

Address: 0x42BD0100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				CUR_STATE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CUR_CNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				CUR_CNT [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	BUSY	None [30:24]						

Bits	Name	Description
31	BUSY	This field indicates if the counter is busy Default Value: 0
19 : 8	CUR_CNT	This field indicates the count value for the given counter. Default Value: 0
3 : 0	CUR_STATE	This field indicates which Timer Table State the counter is assigned. Valid numbers are 0-15 Default Value: 0

20.1.71 HPPASS_ACTRLR_TTCFG0_TT_CFG0

AC Configuration 0

Address: 0x42BD0800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None			
HW Access	None			R	None			
Name	None [7:5]			SAR_UN-LOCK	None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CSG_UNLOCK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW				None			RW
HW Access	R				None			R
Name	DOUT [23:20]				None [19:17]			DOUT_UN-LOCK

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							DOUT

Bits	Name	Description
24 : 20	DOUT	HPPASS data out generation When this function is enabled (see ACTRLR.CFG.DOUT_EN), any enabled bits in this field will be driven through HSIOM to the associated GPIO pads for output. This allows the AC to digital control to an off chip resource (e.g. enable a sensor) as part of AC programming. Default Value: 0
16	DOUT_UNLOCK	DOUT Unlock 0: Lock: DOUT does NOT get updated 1: Unlock: DOUT does get updated Default Value: 0
15 : 8	CSG_UNLOCK	CSG Unlock 0: Lock: CSG fields: EN does NOT get updated 1: Unlock: CSG fields: EN does get updated Default Value: 0
4	SAR_UNLOCK	SAR Unlock 0: Lock: SAR fields: EN does NOT get updated 1: Unlock: SAR fields: EN does get updated These fields are used to prevent unintentional mode transitions. For example, when you wish to enable the SAR, you set this SAR_UNLOCK bit to '1' in that state. As other states will have a '0' for this field, and therefore the SAR_EN will not be inadvertantly be set to '0' in other states. If you want to disable the SAR, set this SAR_UNLOCK bit to '1' again and the SAR_EN to '0' for the disable to take effect. Default Value: 0

20.1.72 HPPASS_ACTRLR_TTCFG0_TT_CFG1

AC Configuration 1

Address: 0x42BD0804

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	NC_7_4 [7:4]				BR_ADDR [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW					
HW Access	R		R					
Name	NC_15_14 [15:14]		COND [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW	RW		
HW Access	R				R	R		
Name	CNT [23:20]				INTR_SET	ACTION [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	CNT [31:24]							

Bits	Name	Description
31 : 20	CNT	This field is used to set the timer/counter values for either interval and loop counts. The actual count is CNT value + 1. Therefore, the range is 1 to 4096. The value of 1 is degenerate. Default Value: Undefined
19	INTR_SET	AC Interrupt Set. This will generate a CPU interrupt or Hardware Trigger output if configured. If ACTION=WAIT_FOR, the interrupt is generated after the COND occurs. The AC Interrupt may be configured in HPPASS_MMIO.HPPASS_INTR. The AC Hardware trigger may be configured in HPPASS_MMIO.TR_PULSE_OUT Default Value: Undefined
18 : 16	ACTION	Autonomous Controller Action Default Value: Undefined **0x0: STOP :** Stop the autonomous controller **0x1: NEXT :** Execute the current state and proceed to the next state **0x2: WAIT_FOR :** Wait for the associated COND to occur before moving to the next state If COND=FALSE, stay in the present state indefinitely. If COND=TRUE, move to the next state.

20.1.72 HPPASS_ACTRLR_TTCFG0_TT_CFG1 (continued)

0x3: BRANCH_IF_TRUE :

Check if COND has occurred, If it has, take the indicated branch (BR ADDR), if not, proceed to the next state.
If COND=FALSE, proceed to the next state. If COND=TRUE, take the indicated branch (BR_ADDR).

0x4: BRANCH_IF_FALSE :

Check if COND has occurred, If it has proceed to the next state, if not, take the indicated branch (BR ADDR)
If COND=FALSE, take the indicated branch (BR_ADDR). If COND=TRUE, proceed to the next state.

0x5: RESERVED_0 :

0x6: RESERVED_1 :

0x7: RESERVED_2 :

15 : 14	NC_15_14	Default Value: Undefined
13 : 8	COND	Autonomous Controller Condition Default Value: Undefined

0x0: False :

Hardcoded FALSE value

0x1: True :

Hardcoded TRUE value

0x2: BLOCK_READY :

Enabled block(s) are ready for use.

0x3: CNT_DONE :

if the ACTION is WAIT_FOR - this is an interval timer.
If the ACTION is BRANCH IF - this is a loop counter.

0x4: SAR_ENTRY0_DONE :

SAR Sequencer Entry Done

0x5: SAR_ENTRY1_DONE :

0x6: SAR_ENTRY2_DONE :

0x7: SAR_ENTRY3_DONE :

0x8: SAR_ENTRY4_DONE :

0x9: SAR_ENTRY5_DONE :

20.1.72 HPPASS_ACTRLR_TTCFG0_TT_CFG1 (continued)

0xa: SAR_ENTRY6_DONE :

0xb: SAR_ENTRY7_DONE :

0xc: SAR_RANGE0 :

SAR Range Detected

0xd: SAR_RANGE1 :

0xe: SAR_RANGE2 :

0xf: SAR_RANGE3 :

0x10: SAR_RANGE4 :

0x11: SAR_RANGE5 :

0x12: SAR_RANGE6 :

0x13: SAR_RANGE7 :

0x14: SAR_BUSY :

SAR Busy

0x15: SAR_FIR0_DONE :

SAR FIR0 Done. All FIR outputs, that is, not gated by FIR_CFG/TAP_WAIT_INIT

0x16: SAR_FIR1_DONE :

SAR FIR1 Done. All FIR outputs, that is, not gated by FIR_CFG/TAP_WAIT_INIT

0x17: SAR_QUEUE_HI_EMPTY :

SAR Hi priority Queue is empty

0x18: SAR_QUEUE_LO_EMPTY :

SAR Lo priority Queue is empty

0x19: SAR_QUEUES_EMPTY :

Both Queues are empty

0x1a: RESERVED26 :

0x1b: RESERVED27 :

0x1c: RESERVED28 :

0x1d: RESERVED29 :

20.1.72 HPPASS_ACTRLR_TTCFG0_TT_CFG1 (continued)

0x1e: RESERVED30 :

0x1f: RESERVED31 :

0x20: HW_TR0_IN :

HW/FW Trigger from INFRA

0x21: HW_TR1_IN :

0x22: HW_TR2_IN :

0x23: HW_TR3_IN :

0x24: HW_TR4_IN :

0x25: HW_TR5_IN :

0x26: HW_TR6_IN :

0x27: HW_TR7_IN :

0x28: RESERVED40 :

0x29: RESERVED41 :

0x2a: FIFO_LEVEL0 :

FIFO Level

0x2b: FIFO_LEVEL1 :

0x2c: FIFO_LEVEL2 :

0x2d: FIFO_LEVEL3 :

0x2e: RESERVED46 :

0x2f: RESERVED47 :

0x30: CSG0_SLOPE_DONE :

CSG Slope/LUT waveform Done

0x31: CSG1_SLOPE_DONE :

0x32: CSG2_SLOPE_DONE :

0x33: CSG3_SLOPE_DONE :

0x34: CSG4_SLOPE_DONE :

20.1.72 HPPASS_ACTRLR_TTCFG0_TT_CFG1 (continued)

0x35: CSG5_SLOPE_DONE :

0x36: CSG6_SLOPE_DONE :

0x37: CSG7_SLOPE_DONE :

0x38: CSG0_CMP_TR :

CSG Comparator Trip. Condition is set by CSG.CSG_SLICE.CMP_CFG.CMP_EDGE_MODE

0x39: CSG1_CMP_TR :

0x3a: CSG2_CMP_TR :

0x3b: CSG3_CMP_TR :

0x3c: CSG4_CMP_TR :

0x3d: CSG5_CMP_TR :

0x3e: CSG6_CMP_TR :

0x3f: CSG7_CMP_TR :

7 : 4	NC_7_4	Reserved Default Value: Undefined
3 : 0	BR_ADDR	Absolute address of the branch if taken (0-15 possible) Default Value: Undefined

20.1.73 HPPASS_ACTRLR_TTCFG0_TT_CFG2

AC Configuration 2

Address: 0x42BD0808

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CSG_EN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CSG_DAC_TR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	NC_31_16 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	NC_31_16 [31:24]							

Bits	Name	Description
31 : 16	NC_31_16	Reserved Default Value: Undefined
15 : 8	CSG_DAC_TR	CSG Slice Triggers. After the block is ready for use - these bits may be used for CSG DAC START and UPDATE triggers. The type of trigger is programmed in the CSG_SLICE register block. If ACTION=WAIT_FOR, the trigger always occurs in the fir cycle of that state Default Value: Undefined
7 : 0	CSG_EN	CSG Slice Enables. The CSG UNLOCK bits must be set in the same state as these bits (see TT_CFG0) to enable or disable. These bits are normally used in conjunction with ACTION=WAIT_FOR and COND=BLOCK_READY Default Value: Undefined

20.1.74 HPPASS_ACTRLR_TTCFG0_TT_CFG3

AC Configuration 3

Address: 0x42BD080C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SAR_TR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			RW
HW Access	R				R			R
Name	SAR_AROUTE_TR [15:12]				NC_11_9 [11:9]			SAR_EN

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SAR_AROUTE_SEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	NC_31_24 [31:24]							

Bits	Name	Description
31 : 24	NC_31_24	Reserved Default Value: Undefined
23 : 16	SAR_AROUTE_SEL	SAR Route setting (2 bits per mux) to select the routing input. The routing bits in this field are only valid if the associated SAR_ROUTE_TR is set. Default Value: Undefined
15 : 12	SAR_AROUTE_TR	SAR Aroute Trigger (1 bit per mux) to change Route setting for one or more AROUTE MUXes. Set this bit in conjuction with a new SAR_AROUTE_SEL value. Default Value: Undefined
11 : 9	NC_11_9	Reserved Default Value: Undefined
8	SAR_EN	SARADC Enable The SAR UNLOCK bit must be set in the same state as this bit (see TT_CFG0) to enable or disable. This bit is normally used in conjunction with ACTION=WAIT_FOR and COND=BLOCK_READY Default Value: Undefined
7 : 0	SAR_TR	SAR Table Entry Triggers. After the block is ready for use - these bits may be used to trigger one ore more SAR Entries. If ACTION=WAIT_FOR, the trigger always occurs in the fir cycle of that state Default Value: Undefined

20.1.75 HPPASS_INFRA_TR_IN_SEL

Trigger Input Select

Address: 0x42BE0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	TR1_SEL [6:4]			None	TR0_SEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	TR3_SEL [14:12]			None	TR2_SEL [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	TR5_SEL [22:20]			None	TR4_SEL [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	TR7_SEL [30:28]			None	TR6_SEL [26:24]		

Bits	Name	Description
30 : 28	TR7_SEL	Default Value: 0
26 : 24	TR6_SEL	Default Value: 0
22 : 20	TR5_SEL	Default Value: 0
18 : 16	TR4_SEL	Default Value: 0
14 : 12	TR3_SEL	Default Value: 0
10 : 8	TR2_SEL	Default Value: 0
6 : 4	TR1_SEL	Default Value: 0
2 : 0	TR0_SEL	Trigger selection. NOTE: ALL TRIGGERS ARE GATED (DISABLED) BY HARDWARE UNTIL BLOCK READY IS '1" Default Value: 0 **0x0: DISABLED :** Trigger is off **0x1: HW_TR_A :** Select an external HW trigger from A trigger inputs. For additional options see HW_TR_MODE

20.1.75 HPPASS_INFRA_TR_IN_SEL (continued)

0x2: HW_TR_B :

Select the external HW trigger from B trigger inputs. For additional options see HW_TR_MODE

0x3: FW_PULSE :

Select FW PULSE trigger. See FW_TR_IN_PULSE.

0x4: FW_LEVEL :

Select FW LEVEL trigger. See FW_TR_IN_LEVEL.

20.1.76 HPPASS_INFRA_HW_TR_MODE

HW Trigger Mode

Address: 0x42BE0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	HW_TR1_MODE [7:4]				HW_TR0_MODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	HW_TR3_MODE [15:12]				HW_TR2_MODE [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	HW_TR5_MODE [23:20]				HW_TR4_MODE [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	HW_TR7_MODE [31:28]				HW_TR6_MODE [27:24]			

Bits	Name	Description
31 : 28	HW_TR7_MODE	Default Value: 0
27 : 24	HW_TR6_MODE	Default Value: 0
23 : 20	HW_TR5_MODE	Default Value: 0
19 : 16	HW_TR4_MODE	Default Value: 0
15 : 12	HW_TR3_MODE	Default Value: 0
11 : 8	HW_TR2_MODE	Default Value: 0
7 : 4	HW_TR1_MODE	Default Value: 0
3 : 0	HW_TR0_MODE	If HW trigger is selected, this controls the trigger mode. Default Value: 0 **0x0: PULSE_ON_POS_DOUBLE_SYNC :** HW trigger is assumed to be async in FC, it is double synced and converted to pulse on positive edge. **0x1: PULSE_ON_NEG_DOUBLE_SYNC :** HW trigger is assumed to be async in FC, it is double synced and converted to synchronous pulse on negative edge.

20.1.76 HPPASS_INFRA_HW_TR_MODE (continued)

0x2: PULSE_ON_BOTH_DOUBLE_SYNC :

HW trigger is assumed to be async in FC, it is double synced and converted to synchronous pulse on both edges.

0x3: LEVEL_DOUBLE_SYNC :

HW trigger is assumed to be async in FC, it is double synced and used as a level trigger. NOTE: Level trigger selection is only for use by a CSG Slice in Hyteretic Mode and the minimum duration of the high or low level must be greater than or equal to the CSG clock period.

0x4: PULSE_ON_POS_SINGLE_SYNC :

HW trigger is assumed to sync in FC, captured in a register, and then converted to pulse on positive edge

0x5: PULSE_ON_NEG_SINGLE_SYNC :

HW trigger is assumed to sync in FC, captured in a register, and then converted to pulse on negative edge

0x6: PULSE_ON_BOTH_SINGLE_SYNC :

HW trigger is assumed to sync in FC, captured in a register, and then converted to pulse on both edges

0x7: LEVEL_SINGLE_SYNC :

HW trigger is assumed to be async in FC, captured in a register, and used as a level trigger. NOTE: Level trigger selection is only for use by a CSG Slice in Hyteretic Mode and the minimum duration of the high or low level must be greater than or equal to the CSG clock period.

20.1.77 HPPASS_INFRA_FW_TR_PULSE

FW Pulse Mode Trigger

Address: 0x42BE0008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	RW1C							
Name	FW_TR_PULSE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	FW_TR_PULSE	If FW is selected in TR_IN_SEL, A write of '1' to this register will generate an internal PULSE trigger. These bits will be cleared automatically by HW. Default Value: 0

20.1.78 HPPASS_INFRA_FW_TR_LEVEL

FW Level Mode Trigger

Address: 0x42BE000C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FW_TR_LEVEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	FW_TR_LEVEL	If FW is selected in TR_IN_SEL, Writes to this register will be passed to the internal trigger as a LEVEL '1' or '0. NOTE: LEVEL mode trigger is only valid for CSG module, Do not use for SAR Entry. Default Value: 0

20.1.79 HPPASS_INFRA_CLOCK_STARTUP_DIV

Startup Clock Divder

Address: 0x42BE0020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DIV_VAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DIV_VAL	Divide HPPASS a prescaled clock divide to generate block startup delays. Actual divide value is DIV_VAL+1. Typically this register should be set to give a period of 200ns, so the count depends on CLK_HF. NOTE: This counter is clocked on CLK_HF/2 Examples: For CLK_HF = 80MHz (CLK_INFRA = 40MHz), set DIV_VAL to 7 (8 cycles * 25ns = 200ns, default) For CLK_HF = 160MHz (CLK_INFRA = 80MHz) set DIV_VAL to 15 (16 cycles * 12.5ns = 200ns) For CLK_HF = 240MHz (CLK_INFRA = 120MHz) set DIV_VAL to 23 (24 cycles * 8.33ns = 200ns Default Value: 7

20.1.80 HPPASS_INFRA_STARTUP_CFG0

Startup configuration

Address: 0x42BE0030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	COUNT_VAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				CSG_READY	CSG_PWR_EN_SLICE	CSG_CH_EN	SAR_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	CSG_READY	CSG Auto Zero/Comparator gate startup When this bit is set, the associated COUNT_VAL must be calculated relative to the CLK_CSG divide and the resulting period must be 33 CLK_CSG periods Examples: Assuming we have 200ns prescale value programmed into CLOCK_STARTUP_DIV.DIV_VAL. With the examples of CLK_CSG as configured by MXPERI at the following frequencies: For CSG at 40 MHz, 25ns x 33 cycles = 825ns. roundup(825/200) = 5 (COUNT_VAL = 4) For CSG at 80 Mhz, 12.5ns x 33 cycles = 412ns roundup(412/200) = 3 (COUNT_VAL = 2) For CSG at 120 MHz, 8.33 ns x 33 cycles = 275ns roundup(275/200) = 2 (COUNT_VAL = 1) Default Value: 0
10	CSG_PWR_EN_SLICE	CSG Slice Enable startup Default Value: 0
9	CSG_CH_EN	CSG Channel Enable startup Default Value: 0
8	SAR_EN	SAR startup Default Value: 0
7 : 0	COUNT_VAL	Actual count value is COUNT_VAL+1 Default Value: 0

20.1.81 HPPASS_INFRA_VDDA_STATUS

Analog Voltage Status

Address: 0x42BE0050

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							VDDA_OK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	VDDA_OK	Read only status bit to determine the presence of VDDA. This bit is set by HW and it must be 1 prior to enabling the SAR or CSG. 0: VDDA is below minimum threshold 1: VDDA is at or above minimum threhold Default Value: 0

20.1.82 HPPASS_INFRA_ANA_CTRL

Analog Control

Address: 0x42BE0070

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				FORCE_OVER-LOAD_EN_1	FORCE_OVER-LOAD_EN_0	FORCE_POR_1	FORCE_POR_0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	FORCE_OVER-LOAD_EN_1	Override for Analog OVERLOAD Hardware circuit 0: (default) OVERLOAD enable is controlled by ACTRL.CTRL.ENABLED bit 1: Force OVERLOAD enable on NOTE: If this bit is set to 1, FORCE_OVERLOAD_EN_0 must be 0 Default Value: 0
2	FORCE_OVER-LOAD_EN_0	Override for Analog OVERLOAD Hardware circuit. 0: (default) OVERLOAD enable is controlled by ACTRL.CTRL.ENABLED bit 1: Force OVERLOAD enable off NOTE: If this bit is set to 1, FORCE_OVERLOAD_EN_1 must be 0 Default Value: 0
1	FORCE_POR_1	Override for Analog POR Hardware circuit. 0: (default) POR is controlled by analog hardware 1: Force POR negated (POR is an active low signal) NOTE: If this bit is set to 1, FORCE_POR_0 must be 0. Default Value: 0
0	FORCE_POR_0	Override for Analog POR Hardware circuit. 0: (default) POR is controlled by analog hardware 1: Force POR asserted (POR is an active low signal) If the HPPASS is not in use, set this bit to '1' to achieve the lowest level of IP leakage NOTE: If this bit is set to 1, FORCE_POR_1 must be 0. Default Value: 0

20.1.83 HPPASS_INFRA_AREFv2_AREF_CTRL

AREF control

Address: 0x42BE0E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW		None	RW
HW Access	R	R			R		None	R
Name	CTB_IP-TAT_S-CALE	AREF_RMB [6:4]			AREF_BIAS_SCALE [3:2]		None	AREF_-MODE

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CTB_IPTAT_REDIRECT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None			RW
HW Access	None		R		None			R
Name	None [23:22]		VREF_SEL [21:20]		None [19:17]			IZTAT_SEL

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	- 0: AREF disabled - 1: AREF enabled Default Value: 0
21 : 20	VREF_SEL	bandgap voltage select control Default Value: 0 **0x0: RESERVED :** Reserved, for normal operation, set to '1' selection (LOCAL) **0x1: LOCAL :** Use locally generated Vref **0x2: EXTERNAL :** Use externally supplied Vref (aref_ext_vref)
16	IZTAT_SEL	iztat current select control Default Value: 0 **0x0: RESERVED :** Reserved, for normal operation, set to '1' selection (LOCAL)

20.1.83 HPPASS_INFRA_AREFv2_AREF_CTRL (continued)

		0x1: LOCAL : Use locally generated 250nA
15 : 8	CTB_IPTAT_REDIRECT	RESERVED - all bits must be set to 0 Default Value: 0
7	CTB_IPTAT_SCALE	RESERVED - set this bit to 0 Default Value: 0
6 : 4	AREF_RMB	RESERVED - all bits must be set to 0 Default Value: 0
3 : 2	AREF_BIAS_SCALE	RESERVED - This field must be set to b01 Default Value: 0
0	AREF_MODE	RESERVED - This bit must be set to 0 Default Value: 0

20.1.84 HPPASS_INFRA_VREF_TRIM0

VREF Trim bits

Address: 0x42BE0F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VREF_ABS_TRIM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	VREF_ABS_TRIM	bandgap absolute voltage output trim (in signed magnitude format) 0x00 : No Voltage Trim Adjustment 0x00 to 0x1F : Maximum Negative Trim Adjustment (-20mV) 0x20 to 0x3F : Maximum Positive Trim Adjustment (+20mV) Bits [7:6] are reserved. Default Value: 0

20.1.85 HPPASS_INFRA_VREF_TRIM1

VREF Trim bits

Address: 0x42BE0F04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VREF_TEMPCO_TRIM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	VREF_TEMPCO_TRIM	bandgap voltage temperature correction trim 0x00 : Minimum temperature correction (smallest PTAT voltage) 0x3F : Maximum temperature correction (largest PTAT voltage) Bits [7:6] are reserved. Default Value: 0

20.1.86 HPPASS_INFRA_VREF_TRIM2

VREF Trim bits

Address: 0x42BE0F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VREF_CURV_TRIM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	VREF_CURV_TRIM	bandgap voltage curvature correction trim 0x00 : No Curvature Correction 0x1F : Maximum Curvature Correction (2uA PTAT2 Current (at 125C)) Bits [7:5] are reserved. Default Value: 0

20.1.87 HPPASS_INFRA_VREF_TRIM3

VREF Trim bits

Address: 0x42BE0F0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				VREF_ATTEN_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	VREF_ATTEN_TRIM	Obsolete Default Value: 0

20.1.88 HPPASS_INFRA_IZTAT_TRIM0

IZTAT Trim bits

Address: 0x42BE0F10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	IZTAT_ABS_TRIM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	IZTAT_ABS_TRIM	IZTAT absolute current output trim 0x00 : Minimum IZTAT output current (~500nA) 0x3F : Maximum IZTAT output current (~1.5uA) Bits [7:6] are reserved. Default Value: 0

20.1.89 HPPASS_INFRA_IZTAT_TRIM1

IZTAT Trim bits

Address: 0x42BE0F14

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	IZTAT_TC_TRIM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	IZTAT_TC_TRIM	IZTAT temperature correction trim (RMB) 0x00 : No IZTAT temperature correction 0xFF : Maximum IZTAT temperature correction As this is a Risk Mitigation Register, it should be loaded with 0x08. Default Value: 0

20.1.90 HPPASS_INFRA_IPTAT_TRIM0

IPTAT Trim bits

Address: 0x42BE0F18

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	IPTAT_CTBM_TRIM [7:4]				IPTAT_CORE_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	IPTAT_CTBM_TRIM	CTMB PTAT Current Trim 0x0 : Minimum CTMB IPTAT Current (~875nA) 0xF : Maximum CTMB IPTAT Current (~1.1uA) Default Value: 0
3 : 0	IPTAT_CORE_TRIM	IPTAT trim 0x0 : Minimum IPTAT current (~150nA at room) 0xF : Maximum IPTAT current (~350nA at room) Default Value: 0

20.1.91 HPPASS_INFRA_ICTAT_TRIM0

ICTAT Trim bits

Address: 0x42BE0F1C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				ICTAT_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	ICTAT_TRIM	ICTAT trim 0x00 : Minimum ICTAT current (~150nA at room) 0x0F : Maximum ICTAT current (~350nA at room) Default Value: 0

20.1.92 HPPASS_MMIO_FIFO_INTR

FIFO Interrupt request register

Address: 0x42BF0000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				FIFO_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	FIFO_LEVEL	This field will be '1', when STATUS.USED >= CTRL.LEVEL+1 and '0' when STATUS.USED < CTRL.LEVEL+1 for the indicated FIFO. This interrupt is level based. Default Value: 0

20.1.93 HPPASS_MMIO_FIFO_INTR_SET

FIFO Interrupt set request register

Address: 0x42BF0010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				FIFO_LEVEL_SET [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	FIFO_LEVEL_SET	Write with '1' to set corresponding bit in interrupt request register. Write with '0' to clear corresponding bit in interrupt request register. NOTE: This register has different functionality than normal event based interrupt register as this interrupt is LEVEL based Default Value: 0

20.1.94 HPPASS_MMIO_FIFO_INTR_MASK

FIFO Interrupt mask register

Address: 0x42BF0020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				FIFO_LEVEL_MASK [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	FIFO_LEVEL_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

20.1.95 HPPASS_MMIO_FIFO_INTR_MASKED

FIFO Interrupt masked request register

Address: 0x42BF0030

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				FIFO_LEVEL_MASKED [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	FIFO_LEVEL_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

20.1.96 HPPASS_MMIO_HPPASS_INTR

HPPASS Interrupt request register

Address: 0x42BF0040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C				RW1C			
HW Access	RW1S				RW1S			
Name	FIFO_UNDERFLOW [7:4]				FIFO_OVERFLOW [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW1C	None	RW1C	RW1C	RW1C
HW Access	None			RW1S	None	RW1S	RW1S	RW1S
Name	None [15:13]			AC_INT	None	ENTRY_HOLD_VIOLATION	ENTRY_TR_COLLISION	RESULT_OVERFLOW

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	AC_INT	HW sets this field to '1', when the AC generates a programmed interrupt. Write with '1' to clear bit. Default Value: 0
10	ENTRY_HOLD_VIOLATION	HW sets this bit if the samplers in a SAR Entry are in HOLD state longer than the programmed count value . Write a '1' to clear this bit. Default Value: 0
9	ENTRY_TR_COLLISION	HW sets this bit if a SAR Entry trigger is asserted while that Entry is in progress, from triggering until conversion is complete. Write a '1' to clear this bit. Default Value: 0
8	RESULT_OVERFLOW	HW sets this field to '1 on RESULT overflow. This bit is set when new SAR Entry or FIR results are written and the associated bit the the INTR_SAR_RESULT register bit is set, implying the previous results have not been read. To determine which Entry or FIR results caused this see SAR_CFG/RESULT_OVERFLOW. Write a '1' to clear this bit. Default Value: 0
7 : 4	FIFO_UNDERFLOW	HW sets this field to '1', when reading from an empty FIFO.. See FIFO_CFG/STATUS (read and write pointers) and FIFO_CFG/USED register for detailed infomration. Write with '1' to clear bit. Default Value: 0

20.1.96 HPPASS_MMIO_HPPASS_INTR (continued)

3 : 0	FIFO_OVERFLOW	HW sets this field to '1', when writing to a full FIFO. See FIFO_CFG/STATUS (read and write pointers) and FIFO_CFG/USED register for detailed infomration. Write with '1' to clear bit. Default Value: 0

20.1.97 HPPASS_MMIO_HPPASS_INTR_SET

HPPASS Interrupt set request register

Address: 0x42BF0044

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S				RW1S			
HW Access	A				A			
Name	FIFO_UNDERFLOW_SET [7:4]				FIFO_OVERFLOW_SET [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW1S	None	RW1S	RW1S	RW1S
HW Access	None			A	None	A	A	A
Name	None [15:13]			AC_INT_SET	None	ENTRY_HOLD_VIOLATION_SET	ENTRY_TR_COLLISION_SET	RESULT_OVERFLOW_SET

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	AC_INT_SET	Write with '1' to set corresponding bit in interrupt request register. (a write of '0' has no effect). Default Value: 0
10	ENTRY_HOLD_VIOLATION_SET	Write with '1' to set corresponding bit in interrupt request register. (a write of '0' has no effect). Default Value: 0
9	ENTRY_TR_COLLISION_SET	Write with '1' to set corresponding bit in interrupt request register. (a write of '0' has no effect). Default Value: 0
8	RESULT_OVERFLOW_SET	Write with '1' to set corresponding bit in interrupt request register. (a write of '0' has no effect). Default Value: 0
7 : 4	FIFO_UNDERFLOW_SET	Write with '1' to set corresponding bit in interrupt request register. (a write of '0' has no effect). Default Value: 0
3 : 0	FIFO_OVERFLOW_SET	Write with '1' to set corresponding bit in interrupt request register. (a write of '0' has no effect). Default Value: 0

20.1.98 HPPASS_MMIO_HPPASS_INTR_MASK

HPPASS Interrupt mask register

Address: 0x42BF0048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	FIFO_UNDERFLOW_MASK [7:4]				FIFO_OVERFLOW_MASK [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None	RW	RW	RW
HW Access	None			R	None	R	R	R
Name	None [15:13]			AC_INT_MASK	None	ENTRY_HOLD_VIOLATION_MASK	ENTRY_TR_COLLISION_MASK	RESULT_OVERFLOW_MASK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	AC_INT_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	ENTRY_HOLD_VIOLATION_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	ENTRY_TR_COLLISION_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	RESULT_OVERFLOW_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7 : 4	FIFO_UNDERFLOW_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3 : 0	FIFO_OVERFLOW_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

20.1.99 HPPASS_MMIO_HPPASS_INTR_MASKED

HPPASS Interrupt masked request register

Address: 0x42BF004C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	W				W			
Name	FIFO_UNDERFLOW_MASKED [7:4]				FIFO_OVERFLOW_MASKED [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None			R	None	R	R	R
HW Access	None			W	None	W	W	W
Name	None [15:13]			AC_INT_MASKED	None	ENTRY_HOLD_VIOLATION_MASKED	ENTRY_TR_COLLISION_MASKED	RESULT_OVERFLOW_MASKED

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	AC_INT_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
10	ENTRY_HOLD_VIOLATION_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
9	ENTRY_TR_COLLISION_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
8	RESULT_OVERFLOW_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
7 : 4	FIFO_UNDERFLOW_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
3 : 0	FIFO_OVERFLOW_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

20.1.100 HPPASS_MMIO_TR_LEVEL_CFG

LEVEL Trigger out configuration

Address: 0x42BF0050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BYPASS_SYNC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	BYPASS_SYNC	When this bit is set, the output flip-flop for the given TR_LEVEL_OUT is bypassed. This option may only be used if the trigger is considered asynchronous and the destination has double sync input. Default Value: 0

20.1.101 HPPASS_MMIO_TR_LEVEL_OUT0

LEVEL Trigger out select register

Address: 0x42BF0060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CMP_TR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SAR_RANGE_TR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	SAR_RANGE_TR	Enable the selected SAR_RANGE output which are then ORed and routed to the associated trigger Default Value: 0
7 : 0	CMP_TR	Enable the selected CMP outputs which are then ORed and routed to the associated trigger Default Value: 0

20.1.102 HPPASS_MMIO_TR_PULSE_OUT0

PULSE Trigger out select register

Address: 0x42BF0080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	SEL	Enable one of the available pulse trigger outputs for the associated trigger Default Value: 0 **0x0: DISABLED :** **0x1: SAR_ENTRY0_DONE :** Entry results are ready for reading in the CHAN_RESULT registers **0x2: SAR_ENTRY1_DONE :** **0x3: SAR_ENTRY2_DONE :** **0x4: SAR_ENTRY3_DONE :** **0x5: SAR_ENTRY4_DONE :** **0x6: SAR_ENTRY5_DONE :** **0x7: SAR_ENTRY6_DONE :** **0x8: SAR_ENTRY7_DONE :**

20.1.102 HPPASS_MMIO_TR_PULSE_OUT0 (continued)

0x9: SAR_FIR0_DONE :

FIR results are ready for reading in the FIR_RESULT registers

0xa: SAR_FIR1_DONE :

0xb: AC_TR :

20.1.103 HPPASS_MMIO_FIFO_CFG

FIFO configuration register.

Address: 0x42BF0100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				None		RW	
HW Access	R				None		R	
Name	FIFO_TR_EN [7:4]				None [3:2]		SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	FIFO_TR_EN	Enable associated FIFO trigger Default Value: 0
1 : 0	SEL	FIFO Configuration Selection 0: FIFO configured for 1-32 Entry FIFO (FIFO0) 1: FIFO configured for 2-16 Entry FIFOs: (FIFO0, FIFO1) 2: FIFO configured for 4-8 Entry FIFOs: (FIFO0, FIFO1, FIFO2, FIFO3) 3: RESERVED Default Value: 0

20.1.104 HPPASS_MMIO_FIFO_CLR

FIFO FW clear register

Address: 0x42BF0104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S			
HW Access	None				RW1C			
Name	None [7:4]				CLR [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	CLR	Write a '1' to clear status for associtaed FIFO. This doesn't actually clear the data, it just resets the pointers. HW write a '1' to clear the bit when the reset is completed. Default Value: 0

20.1.105 HPPASS_MMIO_FIFO_LEVEL0

FIFO level register.

Address: 0x42BF0110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			LEVEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	LEVEL	FIFO level set. A trigger (and optional interrupt) event occurs when USED.USED = LEVEL+1. Default Value: 0

20.1.106 HPPASS_MMIO_FIFO_RD_DATA0

FIFO 32-bit read data register

Address: 0x42BF0130

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			R				
HW Access	None			W				
Name	None [23:21]			RESULT [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 0	RESULT	5-bit Channel ID (upper bits), 16-bit SAR/FIR result (lower bits) See SAR_CFG.CHAN_CFG.FIFO_SEL and SAR_CFG.FIR_CFG.FIFO_SEL registers to select a target FIFO. See SAR_CFG.CTRL.CHAN_ID_EN to optionally include a channel ID, otherwise these bits are 0 Default Value: Undefined

20.1.107 HPPASS_MMIO_FIFO_USED0

FIFO used register

Address: 0x42BF0150

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R					
HW Access	None		W					
Name	None [7:6]		USED [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	USED	Number of used/occupied entries in the FIFO. Default Value: 0

20.1.108 HPPASS_MMIO_FIFO_STATUS0

FIFO status register

Address: 0x42BF0170

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			W				
Name	None [7:5]			RD_PTR [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			R				
HW Access	None			W				
Name	None [23:21]			WR_PTR [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 16	WR_PTR	FIFO write pointer: FIFO location at which a new data is written by the hardware. Note: This functionality is intended for debugging purposes. Default Value: 0
4 : 0	RD_PTR	FIFO read pointer: FIFO location from which a data is read. Note: This functionality is intended for debugging purposes. Default Value: 0

21 Low-power Comparator (LPCOMP) registers

This section discusses the LPCOMP registers. It lists all the registers in mapping tables, in address order.

21.1 Register details

Register	Address	Description
LPCOMP_CONFIG	0x42430000	LPCOMP Configuration Register
LPCOMP_STATUS	0x42430004	LPCOMP Status Register
LPCOMP_INTR	0x42430010	LPCOMP Interrupt request register
LPCOMP_INTR_SET	0x42430014	LPCOMP Interrupt set register
LPCOMP_INTR_MASK	0x42430018	LPCOMP Interrupt request mask
LPCOMP_INTR_MASKED	0x4243001C	LPCOMP Interrupt request masked
LPCOMP_CMP0_CTRL	0x42430040	Comparator 0 control Register
LPCOMP_CMP0_SW	0x42430050	Comparator 0 switch control
LPCOMP_CMP0_SW_CLEAR	0x42430054	Comparator 0 switch control clear
LPCOMP_CMP1_CTRL	0x42430080	Comparator 1 control Register
LPCOMP_CMP1_SW	0x42430090	Comparator 1 switch control
LPCOMP_CMP1_SW_CLEAR	0x42430094	Comparator 1 switch control clear

21.1.1 LPCOMP_CONFIG

LPCOMP Configuration Register

Address: 0x42430000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	ENABLED	LPREF_EN	None [29:24]					

Bits	Name	Description
31	ENABLED	- 0: LPCOMP disabled (puts analog in power down, opens all switches, all clocks turned off) - 1: LPCOMP enabled Default Value: 0
30	LPREF_EN	Enable the local reference generator circuit to generate the local Vref and Ibias. Ibias current is an alternative to the reference current IREF generated by SRSS. This bit must be set for System Deep Sleep and System Hibernate operation. Default Value: 0

21.1.2 LPCOMP_STATUS

LPCOMP Status Register

Address: 0x42430004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							RW
Name	None [23:17]							OUT1

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	OUT1	Current output value of the comparator 1. Default Value: 0
0	OUT0	Current output value of the comparator 0. Default Value: 0

21.1.3 LPCOMP_INTR

LPCOMP Interrupt request register

Address: 0x42430010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						A	A
Name	None [7:2]						COMP1	COMP0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1	Comparator 1 Interrupt: hardware sets this interrupt when comparator 1 triggers. Write with '1' to clear bit. Default Value: 0
0	COMP0	Comparator 0 Interrupt: hardware sets this interrupt when comparator 0 triggers. Write with '1' to clear bit. Default Value: 0

21.1.4 LPCOMP_INTR_SET

LPCOMP Interrupt set register

Address: 0x42430014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						COMP1	COMP0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	COMP0	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

21.1.5 LPCOMP_INTR_MASK

LPCOMP Interrupt request mask

Address: 0x42430018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						COMP1_MASK	COMP0_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	COMP0_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

21.1.6 LPCOMP_INTR_MASKED

LPCOMP Interrupt request masked

Address: 0x4243001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						COMP1_MASKED	COMP0_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
0	COMP0_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

21.1.7 LPCOMP_CMP0_CTRL

Comparator 0 control Register

Address: 0x42430040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	None			RW	
HW Access	R		R	None			R	
Name	INTTYPE0 [7:6]		HYST0	None [4:2]			MODE0 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	None	
HW Access	None				R	R	None	
Name	None [15:12]				DSI_LEV-EL0	DSI_BY-PASS0	None [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	DSI_LEVEL0	Synchronous comparator output (trigger): 0=pulse 1=level Default Value: 0
10	DSI_BYPASS0	Asynchronous: bypass comparator output synchronization: 0=synchronize (level or pulse) 1=bypass (output async) Note that in System Deep Sleep mode, this bit needs to be set to observe the output on the dedicated pin. Default Value: 0
7 : 6	INTTYPE0	Sets which edge will trigger an IRQ Default Value: 0 **0x0: DISABLE :** Disabled, no interrupts will be detected **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge

21.1.7 LPCOMP_CMP0_CTRL (continued)

		0x3: BOTH : Both rising and falling edges
5	HYST0	Add hysteresis to the comparator 0= Disable Hysteresis 1= Enable Hysteresis Default Value: 0
1 : 0	MODE0	Operating mode for the comparator Default Value: 0 **0x0: OFF :** Off **0x1: ULP :** Ultra low power operating mode. This mode must be used for System Deep Sleep and System Hibernate operation. In this mode, local Ibias is used. **0x2: LP :** Low Power operating mode. In this mode, IREF from SRSS is used. **0x3: NORMAL :** Normal power, full speed operating mode. In this mode, IREF from SRSS is used.

21.1.8 LPCOMP_CMP0_SW

Comparator 0 switch control

Address: 0x42430050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	None	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	None	RW1C	RW1C	RW1C
Name	CMP0_VN0	CMP0_BN0	CMP0_AN0	CMP0_IN0	None	CMP0_BP0	CMP0_AP0	CMP0_IP0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	CMP0_VN0	Comparator 0 negative terminal switch to local Vref (LPREF_EN must be set) Default Value: 0
6	CMP0_BN0	Comparator 0 negative terminal switch to amuxbusB Default Value: 0
5	CMP0_AN0	Comparator 0 negative terminal switch to amuxbusA Default Value: 0
4	CMP0_IN0	Comparator 0 negative terminal isolation switch to GPIO Default Value: 0
2	CMP0_BP0	Comparator 0 positive terminal switch to amuxbusB Default Value: 0
1	CMP0_AP0	Comparator 0 positive terminal switch to amuxbusA Default Value: 0
0	CMP0_IP0	Comparator 0 positive terminal isolation switch to GPIO Default Value: 0

21.1.9 LPCOMP_CMP0_SW_CLEAR

Comparator 0 switch control clear

Address: 0x42430054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	None	RW1C	RW1C	RW1C
HW Access	A	A	A	A	None	A	A	A
Name	CMP0_VN0	CMP0_BN0	CMP0_AN0	CMP0_IN0	None	CMP0_BP0	CMP0_AP0	CMP0_IP0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	CMP0_VN0	see corresponding bit in CMP0_SW Default Value: 0
6	CMP0_BN0	see corresponding bit in CMP0_SW Default Value: 0
5	CMP0_AN0	see corresponding bit in CMP0_SW Default Value: 0
4	CMP0_IN0	see corresponding bit in CMP0_SW Default Value: 0
2	CMP0_BP0	see corresponding bit in CMP0_SW Default Value: 0
1	CMP0_AP0	see corresponding bit in CMP0_SW Default Value: 0
0	CMP0_IP0	see corresponding bit in CMP0_SW Default Value: 0

21.1.10 LPCOMP_CMP1_CTRL

Comparator 1 control Register

Address: 0x42430080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	None			RW	
HW Access	R		R	None			R	
Name	INTTYPE1 [7:6]		HYST1	None [4:2]			MODE1 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	None	
HW Access	None				R	R	None	
Name	None [15:12]				DSI_LEV-EL1	DSI_BY-PASS1	None [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	DSI_LEVEL1	Synchronous comparator output (trigger): 0=pulse 1=level Default Value: 0
10	DSI_BYPASS1	Asynchronous: bypass comparator output synchronization: 0=synchronize (level or pulse) 1=bypass (output async) Note that in System Deep Sleep mode, this bit needs to be set to observe the output on the dedicated pin. Default Value: 0
7 : 6	INTTYPE1	Sets which edge will trigger an IRQ Default Value: 0 **0x0: DISABLE :** Disabled, no interrupts will be detected **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge

21.1.10 LPCOMP_CMP1_CTRL (continued)

		0x3: BOTH : Both rising and falling edges
5	HYST1	Add hysteresis to the comparator 0= Disable Hysteresis 1= Enable Hysteresis Default Value: 0
1 : 0	MODE1	Operating mode for the comparator Default Value: 0 **0x0: OFF :** Off **0x1: ULP :** Ultra low power operating mode. This mode must be used for System Deep Sleep and System Hibernate operation. In this mode, local Ibias is used. **0x2: LP :** Low Power operating mode. In this mode, IREF from SRSS is used. **0x3: NORMAL :** Normal power, full speed operating mode. In this mode, IREF from SRSS is used.

21.1.11 LPCOMP_CMP1_SW

Comparator 1 switch control

Address: 0x42430090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	None	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	None	RW1C	RW1C	RW1C
Name	CMP1_VN1	CMP1_BN1	CMP1_AN1	CMP1_IN1	None	CMP1_BP1	CMP1_AP1	CMP1_IP1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	CMP1_VN1	Comparator 1 negative terminal switch to local Vref (LPREF_EN must be set) Default Value: 0
6	CMP1_BN1	Comparator 1 negative terminal switch to amuxbusB Default Value: 0
5	CMP1_AN1	Comparator 1 negative terminal switch to amuxbusA Default Value: 0
4	CMP1_IN1	Comparator 1 negative terminal isolation switch to GPIO Default Value: 0
2	CMP1_BP1	Comparator 1 positive terminal switch to amuxbusB Default Value: 0
1	CMP1_AP1	Comparator 1 positive terminal switch to amuxbusA Default Value: 0
0	CMP1_IP1	Comparator 1 positive terminal isolation switch to GPIO Default Value: 0

21.1.12 LPCOMP_CMP1_SW_CLEAR

Comparator 1 switch control clear

Address: 0x42430094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	None	RW1C	RW1C	RW1C
HW Access	A	A	A	A	None	A	A	A
Name	CMP1_VN1	CMP1_BN1	CMP1_AN1	CMP1_IN1	None	CMP1_BP1	CMP1_AP1	CMP1_IP1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	CMP1_VN1	see corresponding bit in CMP1_SW Default Value: 0
6	CMP1_BN1	see corresponding bit in CMP1_SW Default Value: 0
5	CMP1_AN1	see corresponding bit in CMP1_SW Default Value: 0
4	CMP1_IN1	see corresponding bit in CMP1_SW Default Value: 0
2	CMP1_BP1	see corresponding bit in CMP1_SW Default Value: 0
1	CMP1_AP1	see corresponding bit in CMP1_SW Default Value: 0
0	CMP1_IP1	see corresponding bit in CMP1_SW Default Value: 0

Revision history

Document version	Date of release	Description of changes
**	2024-02-05	Initial release.
*A	2024-06-02	Updated the following registers: • **"FLASH registers"** on page 518 • **"Supervisory Flash (SFLASH) registers"** on page 602 • **"System Resources and Clocking registers"** on page 999 • **"Device Power Modes registers"** on page 1144 • **"IO Subsystem registers"** on page 1204 • **"Timer, Counter, and Pulse Width Modulator (TCPWM) registers"** on page 1317 • **"High Performance Programmable Analog Sub-System (HPPASS) registers"** on page 1690
*B	2024-11-28	Updated the following registers: • **"CPU Subsystem (CPUSS) registers"** on page 7 • **"FLASH registers"** on page 518 • **"Supervisory Flash (SFLASH) registers"** on page 602 • **"Fault Monitoring registers"** on page 677 • **"Peripheral registers"** on page 962 • **"System Resources and Clocking registers"** on page 999 • **"Device Power Modes registers"** on page 1144 • **"Backup registers"** on page 1180 • **"IO Subsystem registers"** on page 1204 • **"Timer, Counter, and Pulse Width Modulator (TCPWM) registers"** on page 1317 • **"Coordinate Rotation Digital Computer (CORDIC) registers"** on page 1643 • **"High Performance Programmable Analog Sub-System (HPPASS) registers"** on page 1690

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Edition 2024-11-28
Published by

Infineon Technologies AG
81726 Munich, Germany

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Document reference
002-39445 Rev. *B

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