Please note that Cypress is an Infineon Technologies Company.
The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content
The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers
Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

PSoC 6 MCU: CY8C61x4, CY8C62x4 Registers Technical Reference Manual (TRM)

PSoC 61, PSoC 62 MCU

Document Number: 002-30426 Rev. *B

June 30, 2021

Cypress Semiconductor
An Infineon Technologies Company
198 Champion Court
San Jose, CA 95134-1709
www.cypress.com
www.infineon.com

Copyrights

© Cypress Semiconductor Corporation, 2020-2021. This document is the property of Cypress Semiconductor Corporation, an Infineon Technologies company, and its affiliates (“Cypress”). This document, including any software or firmware included or referenced in this document (“Software”), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress’s patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress shall have no liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. CYPRESS DOES NOT REPRESENT, WARRANT, OR GUARANTEE THAT CYPRESS PRODUCTS, OR SYSTEMS CREATED USING CYPRESS PRODUCTS, WILL BE FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (collectively, “Security Breach”). Cypress disclaims any liability relating to any Security Breach, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any Security Breach. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. “High-Risk Device” means any device or system whose failure could cause personal injury, death, or property damage Examples of High-Risk Devices are weapons, nuclear installations, surgical implants, and other medical devices. “Critical Component” means any component of a High-Risk Device whose failure to perform can be reasonably expected to cause, directly or indirectly, the failure of the High-Risk Device, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any use of a Cypress product as a Critical Component in a High-Risk Device. You shall indemnify and hold Cypress, including its affiliates, and its directors, officers, employees, agents, distributors, and assigns harmless from and against all claims, costs, damages, and expenses, arising out of any claim, including claims for product liability, personal injury or death, or property damage arising from any use of a Cypress product as a Critical Component in a High-Risk Device. Cypress products are not intended or authorized for use as a Critical Component in any High-Risk Device except to the limited extent that (i) Cypress’s published data sheet for the product explicitly states Cypress has qualified the product for use in a specific High-Risk Device, or (ii) Cypress has given you advance written authorization to use the product as a Critical Component in the specific High-Risk Device and you have signed a separate indemnification agreement.

Cypress, the Cypress logo, and combinations thereof, PSoC, CapSense, EZ-USB, F-RAM, Traveo, WICED, and ModusToolbox are trademarks or registered trademarks of Cypress or a subsidiary of Cypress in the United States or in other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.

Contents

Register Mapping **5**

Section A: Supervisory Flash Registers **9**
1. Supervisory Flash Registers 10

Section B: Peripheral Group 0 **16**
2. Peripheral Registers 17

Section C: Peripheral Group 1 **652**
3. Cryptography Registers 653

Section D: Peripheral Group 2 **721**
4. CPU Sub System Registers 722
5. Fault Registers 773
6. Inter-Processor Communication Registers 798
7. Protection Unit Registers 814
8. Flash Controller Registers 860
9. System Resources Subsystem Registers 939
10. Multi-Counter WDT Registers 1014
11. Backup System Registers 1028
12. Direct Memory Access Registers 1054
13. eFuse Registers 1124

Section E: Peripheral Group 3 **1131**
14. High Speed IO Matrix Registers 1132
15. General Purpose I/O Registers 1153
16. Smart I/O Registers 1330
17. Low-Power Comparator Registers 1342
18. Timer, Counter, PWM Registers 1357
19. Segment LCD Drive Registers 1429
20. USB Registers 1437

Section F: Peripheral Group 4 **1590**
21. Serial Memory Interface Registers 1591

Section G: Peripheral Group 5 **1648**
22. CAN FD Controller 1649

Section H: Peripheral Group 6 **1759**
23. Serial Communication Block Registers 1760

Section I: Peripheral Group 9 **1861**
24. Analog Reference Block Registers 1862
25. Continuous-Time Block Mini (CTBm) Registers 1866
26. Continuous-Time DAC Registers 1896
27. SAR ADC Registers 1907
28. FIFO Registers 1966
29. Timer Registers 1979
30. Low Power Oscillator Registers 1983
31. Programmable Analog Subsystem Registers 1986

Section J: System Registers **2012**

Register Mapping

The Register Mapping section discusses the registers and lists all the registers in mapping tables, in address order. For Architecture details, refer to PSoC 6 MCU: CY8C62x4 Architecture Technical Reference Manual (TRM).

Note that memory mapped I/O (MMIO) registers support only 32-bit access, unless otherwise specified in the register description.

Register General Conventions

The register conventions specific to this section and the Register Reference chapter are listed in this table.

Convention	Description	Explanation
RW	Read/Write	These bits can be both read and written.
R	Read only	These bits can only be read. Writing has no effect on the bit value.
W	Write only	These bits can only be written. Reading the bit returns the reset value.
RW1C	Read/Write ‘1’ to clear	These bits can be read as well as cleared by writing ‘1’. Writing ‘0’ has no effect on the bit value.
RW0C	Read/Write ‘0’ to clear	These bits can be read as well as cleared by writing ‘0’. Writing ‘1’ has no effect on the bit value.
RW1S	Read/Write ‘1’ to set	These bits can be read as well as set by writing ‘1’. Writing ‘0’ has no effect on the bit value.
A	Alias	This register is an additional alias for another register. This convention is used when a physical register is mapped to multiple addresses, typically for firm-ware debug purposes. See the corresponding register descriptions for more details.
None / Reserved	Reserved bits	Keep these bits at the default value
‘x’ in a register /bit field name	Multiple instances	Multiple instances/address ranges of the same register/bit field

Acronyms

This table lists the acronyms used in this document

Table 3-1. Acronyms

Symbol	Unit of Measure
ABUS	analog output bus
AC	alternating current
ADC	analog-to-digital converter
AHB	AMBA (advanced microcontroller bus architecture) high-per formance bus, an ARM data transfer bus
API	application programming interface
APOR	analog power-on reset
BC	broadcast clock
BOM	bill of materials
BR	bit rate
BRA	bus request acknowledge
BRQ	bus request
CAN	controller area network

Table 3-1. Acronyms

Symbol	Unit of Measure
CI	carry in
CMP	compare
CO	carry out
CPU	central processing unit
CRC	cyclic redundancy check
CSD	CapSense sigma delta
CT	continuous time
CTBm	continuous time block-mini
DAC	digital-to-analog converter
DC	direct current
DI	digital or data input
DMA	direct memory access
DNL	differential nonlinearity
DO	digital or data output
DSI	digital signal interface
DSM	deep-sleep mode
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read only memory
EMIF	external memory interface
FB	feedback
FIFO	first in first out
FSR	full scale range
GPIO	general purpose I/O
HCI	host-controller interface
HFCLK	high-frequency clock
I^2C	inter-integrated circuit
IDE	integrated development environment
ILO	internal low-speed oscillator
IMO	internal main oscillator
INL	integral nonlinearity
I/O	input/output
IOR	I/O read
IOW	I/O write
IRES	initial power on reset
IRA	interrupt request acknowledge
IRQ	interrupt request
ISR	interrupt service routine
IVR	interrupt vector read
L2CAP	logical link control and adaptation protocol
LPCOMP	low-power comparator
LRb	last received bit
LRB	last received byte
LSb	least significant bit
LSB	least significant byte

Table 3-1. Acronyms

Symbol	Unit of Measure
LUT	lookup table
MISO	master-in-slave-out
MMIO	memory mapped input/output
MOSI	master-out-slave-in
MSb	most significant bit
MSB	most significant byte
PC	program counter
PCH	program counter high
PCL	program counter low
PD	power down
PGA	programmable gain amplifier
PM	power management
PMA	PSoC memory arbiter
POR	power-on reset
PPOR	precision power-on reset
PRS	pseudo random sequence
PSoC®	Programmable System-on-Chip
PSRR	power supply rejection ratio
PSSDC	power system sleep duty cycle
PWM	pulse width modulator
RAM	random-access memory
RETI	return from interrupt
RF	radio frequency
ROM	read only memory
RW	read/write
SAR	successive approximation register
SC	switched capacitor
SCB	serial communication block
SIE	serial interface engine
SIO	special I/O
SE0	single-ended zero
SNR	signal-to-noise ratio
SOF	start of frame
SOI	start of instruction
SP	stack pointer
SPD	sequential phase detector
SPI	serial peripheral interconnect
SPIM	serial peripheral interconnect master
SPIS	serial peripheral interconnect slave
SRAM	static random-access memory
SRSS	system resources sub-system
SROM	supervisory read only memory
SSADC	single slope ADC
SSC	supervisory system call

Table 3-1. Acronyms

Symbol	Unit of Measure
SYSCLK	system clock
SWD	single wire debug
TC	terminal count
TD	transaction descriptors
UART	universal asynchronous receiver/transmitter
UDB	universal digital block
USB	universal serial bus
USBIO	USB I/O
WCO	watch crystal oscillator
WDT	watchdog timer
WDR	watchdog reset
XRES	external reset
XRES_N	external reset, active low

Section A: Supervisory Flash Registers

This section encompasses the following chapter:

- Supervisory Flash Registers chapter on page 10

1 Supervisory Flash Registers

This section discusses the Supervisory Flash registers. It lists all the registers in mapping tables, in address order.

1.1 Register Details

Register	Address	Description
SFLASH_SI_REVISION_ID	0x16000001	Indicates Silicon Revision ID of the device
SFLASH_SILICON_ID	0x16000002	Indicates Silicon ID of the device
SFLASH_FAMILY_ID	0x1600000C	Indicates Family ID of the device
SFLASH_SAR_TEMP_MULTIPLIER	0x16000648	SAR Temperature Sensor Multiplication Factor
SFLASH_SAR_TEMP_OFFSET	0x1600064A	SAR Temperature Sensor Offset

1.1.1 SFLASH_SI_REVISION_ID

Indicates Silicon Revision ID of the device

Address: 0x16000001

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	SI_REVISION_ID [7:0]							

Bits	Name	Description
7 : 0	SI_REVISION_ID	Silicon Revision ID Default Value: X

1.1.2 SFLASH_SILICON_ID

Indicates Silicon ID of the device

Address: 0x16000002

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	ID [15:8]							

Bits	Name	Description
15 : 0	ID	Silicon ID Default Value: X

1.1.3 SFLASH_FAMILY_ID

Indicates Family ID of the device

Address: 0x1600000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	FAMILY_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	FAMILY_ID [15:8]							

Bits	Name	Description
15 : 0	FAMILY_ID	Indicates Family ID of the device Default Value: X

1.1.4 SFLASH_SAR_TEMP_MULTIPLIER

SAR Temperature Sensor Multiplication Factor

Address: 0x16000648

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	TEMP_MULTIPLIER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	TEMP_MULTIPLIER [15:8]							

Bits	Name	Description
15 : 0	TEMP_MULTIPLIER	Multiplier value for SAR temperature sensor Default Value: X

1.1.5 SFLASH_SAR_TEMP_OFFSET

SAR Temperature Sensor Offset

Address: 0x1600064A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	TEMP_OFFSET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	TEMP_OFFSET [15:8]							

Bits	Name	Description
15 : 0	TEMP_OFFSET	Offset value for SAR temperature sensor Default Value: X

Section B: Peripheral Group 0

This section encompasses the following chapters:

- Peripheral Registers chapter on page 17

2 Peripheral Registers

This section discusses the Peripheral registers. It lists all the registers in mapping tables, in address order.

2.1 Register Details

Register	Address	Description
PERI_TIMEOUT_CTL	0x40000200	Timeout control
PERI_TR_CMD	0x40000220	Trigger command
PERI_DIV_CMD	0x40000400	Divider command
PERI_CLOCK_CTL0	0x40000C00	Clock control
PERI_CLOCK_CTL1	0x40000C04	Clock control. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL2	0x40000C08	Clock control. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL3	0x40000C0C	Clock control. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL4	0x40000C10	Clock control. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL5	0x40000C14	Clock control. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL6	0x40000C18	Clock control. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL7	0x40000C1C	Clock control. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL8	0x40000C20	Clock control. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL9	0x40000C24	Clock control. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL10	0x40000C28	Clock control. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL11	0x40000C2C	Clock control. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL12	0x40000C30	Clock control. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL13	0x40000C34	Clock control. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL14	0x40000C38	Clock control. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL15	0x40000C3C	Clock control. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL16	0x40000C40	Clock control. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL17	0x40000C44	Clock control. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL18	0x40000C48	Clock control. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL19	0x40000C4C	Clock control. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL20	0x40000C50	Clock control. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL21	0x40000C54	Clock control. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL22	0x40000C58	Clock control. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL23	0x40000C5C	Clock control. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL24	0x40000C60	Clock control. See PERI_CLOCK_CTL0 for the details of bit fields.

Register	Address	Description
PERI_CLOCK_CTL25	0x40000C64	Clock control. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL26	0x40000C68	Clock control. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL27	0x40000C6C	Clock control. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_DIV_8_CTL0	0x40001000	Divider control (for 8.0 divider)
PERI_DIV_8_CTL1	0x40001004	Divider control (for 8.0 divider). See PERI_DIV_8_CTL0 for the details of bit fields.
PERI_DIV_8_CTL2	0x40001008	Divider control (for 8.0 divider). See PERI_DIV_8_CTL0 for the details of bit fields.
PERI_DIV_8_CTL3	0x4000100C	Divider control (for 8.0 divider). See PERI_DIV_8_CTL0 for the details of bit fields.
PERI_DIV_16_CTL0	0x40001400	Divider control (for 16.0 divider)
PERI_DIV_16_CTL1	0x40001404	Divider control (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL2	0x40001408	Divider control (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL3	0x4000140C	Divider control (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL4	0x40001410	Divider control (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL5	0x40001414	Divider control (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL6	0x40001418	Divider control (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL7	0x4000141C	Divider control (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_5_CTL0	0x40001800	Divider control (for 16.5 divider)
PERI_DIV_16_5_CTL1	0x40001804	Divider control (for 16.5 divider). See PERI_DIV_16_5_CTL0 for the details of bit fields.
PERI_DIV_24_5_CTL0	0x40001C00	Divider control (for 24.5 divider)
PERI_GR0_SL_CTL	0x40004010	Slave control
PERI_GR1_SL_CTL	0x40004030	Slave control
PERI_GR2_SL_CTL	0x40004050	Slave control (Note: Writing to this register to disable group 2 slaves could disable all Protection Units. This register itself should be protected from writes for Protection Contexts (PC) > 0)
PERI_GR3_CLOCK_CTL	0x40004060	Clock control
PERI_GR3_SL_CTL	0x40004070	Slave control
PERI_GR4_CLOCK_CTL	0x40004080	Clock control. See PERI_GR3_CLOCK_CTL for the details of bit fields.
PERI_GR4_SL_CTL	0x40004090	Slave control
PERI_GR5_CLOCK_CTL	0x400040A0	Clock control. See PERI_GR3_CLOCK_CTL for the details of bit fields.
PERI_GR5_SL_CTL	0x400040B0	Slave control. See PERI_GR4_SL_CTL for the details of bit fields.
PERI_GR6_CLOCK_CTL	0x400040C0	Clock control. See PERI_GR3_CLOCK_CTL for the details of bit fields.
PERI_GR6_SL_CTL	0x400040D0	Slave control
PERI_GR9_CLOCK_CTL	0x40004120	Clock control. See PERI_GR3_CLOCK_CTL for the details of bit fields.
PERI_GR9_SL_CTL	0x40004130	Slave control. See PERI_GR1_SL_CTL for the details of bit fields.
PERI_TR_GR0_TR_CTL0	0x40008000	Trigger control register
PERI_TR_GR0_TR_CTL1	0x40008004	Trigger control register. See PERI_TR_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_GR0_TR_CTL2	0x40008008	Trigger control register. See PERI_TR_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_GR0_TR_CTL3	0x4000800C	Trigger control register. See PERI_TR_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_GR0_TR_CTL4	0x40008010	Trigger control register. See PERI_TR_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_GR0_TR_CTL5	0x40008014	Trigger control register. See PERI_TR_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_GR0_TR_CTL6	0x40008018	Trigger control register. See PERI_TR_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_GR0_TR_CTL7	0x4000801C	Trigger control register. See PERI_TR_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_GR1_TR_CTL0	0x40008400	Trigger control register. See PERI_TR_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_GR1_TR_CTL1	0x40008404	Trigger control register. See PERI_TR_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_GR1_TR_CTL2	0x40008408	Trigger control register. See PERI_TR_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_GR1_TR_CTL3	0x4000840C	Trigger control register. See PERI_TR_GR0_TR_CTL0 for the details of bit fields.

Register	Address	Description
PERI_TR_GR1_TR_CTL4	0x40008410	Trigger control register. See PERI_TR_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_GR1_TR_CTL5	0x40008414	Trigger control register. See PERI_TR_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_GR1_TR_CTL6	0x40008418	Trigger control register. See PERI_TR_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_GR1_TR_CTL7	0x4000841C	Trigger control register. See PERI_TR_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_GR2_TR_CTL0	0x40008800	Trigger control register
PERI_TR_GR2_TR_CTL1	0x40008804	Trigger control register. See PERI_TR_GR2_TR_CTL0 for the details of bit fields.
PERI_TR_GR2_TR_CTL2	0x40008808	Trigger control register. See PERI_TR_GR2_TR_CTL0 for the details of bit fields.
PERI_TR_GR2_TR_CTL3	0x4000880C	Trigger control register. See PERI_TR_GR2_TR_CTL0 for the details of bit fields.
PERI_TR_GR2_TR_CTL4	0x40008810	Trigger control register. See PERI_TR_GR2_TR_CTL0 for the details of bit fields.
PERI_TR_GR2_TR_CTL5	0x40008814	Trigger control register. See PERI_TR_GR2_TR_CTL0 for the details of bit fields.
PERI_TR_GR2_TR_CTL6	0x40008818	Trigger control register. See PERI_TR_GR2_TR_CTL0 for the details of bit fields.
PERI_TR_GR2_TR_CTL7	0x4000881C	Trigger control register. See PERI_TR_GR2_TR_CTL0 for the details of bit fields.
PERI_TR_GR2_TR_CTL8	0x40008820	Trigger control register. See PERI_TR_GR2_TR_CTL0 for the details of bit fields.
PERI_TR_GR2_TR_CTL9	0x40008824	Trigger control register. See PERI_TR_GR2_TR_CTL0 for the details of bit fields.
PERI_TR_GR2_TR_CTL10	0x40008828	Trigger control register. See PERI_TR_GR2_TR_CTL0 for the details of bit fields.
PERI_TR_GR2_TR_CTL11	0x4000882C	Trigger control register. See PERI_TR_GR2_TR_CTL0 for the details of bit fields.
PERI_TR_GR2_TR_CTL12	0x40008830	Trigger control register. See PERI_TR_GR2_TR_CTL0 for the details of bit fields.
PERI_TR_GR2_TR_CTL13	0x40008834	Trigger control register. See PERI_TR_GR2_TR_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_CTL0	0x40008C00	Trigger control register. See PERI_TR_GR2_TR_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_CTL1	0x40008C04	Trigger control register. See PERI_TR_GR2_TR_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_CTL2	0x40008C08	Trigger control register. See PERI_TR_GR2_TR_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_CTL3	0x40008C0C	Trigger control register. See PERI_TR_GR2_TR_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_CTL4	0x40008C10	Trigger control register. See PERI_TR_GR2_TR_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_CTL5	0x40008C14	Trigger control register. See PERI_TR_GR2_TR_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_CTL6	0x40008C18	Trigger control register. See PERI_TR_GR2_TR_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_CTL7	0x40008C1C	Trigger control register. See PERI_TR_GR2_TR_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_CTL8	0x40008C20	Trigger control register. See PERI_TR_GR2_TR_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_CTL9	0x40008C24	Trigger control register. See PERI_TR_GR2_TR_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_CTL10	0x40008C28	Trigger control register. See PERI_TR_GR2_TR_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_CTL11	0x40008C2C	Trigger control register. See PERI_TR_GR2_TR_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_CTL12	0x40008C30	Trigger control register. See PERI_TR_GR2_TR_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_CTL13	0x40008C34	Trigger control register. See PERI_TR_GR2_TR_CTL0 for the details of bit fields.
PERI_TR_GR4_TR_CTL0	0x40009000	Trigger control register
PERI_TR_GR4_TR_CTL1	0x40009004	Trigger control register. See PERI_TR_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_GR5_TR_CTL0	0x40009400	Trigger control register. See PERI_TR_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_GR5_TR_CTL1	0x40009404	Trigger control register. See PERI_TR_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_GR6_TR_CTL0	0x40009800	Trigger control register
PERI_TR_GR6_TR_CTL1	0x40009804	Trigger control register. See PERI_TR_GR6_TR_CTL0 for the details of bit fields.
PERI_TR_GR7_TR_CTL0	0x40009C00	Trigger control register
PERI_TR_GR7_TR_CTL1	0x40009C04	Trigger control register. See PERI_TR_GR7_TR_CTL0 for the details of bit fields.
PERI_TR_GR8_TR_CTL0	0x4000A000	Trigger control register
PERI_TR_GR9_TR_CTL0	0x4000A400	Trigger control register
PERI_TR_GR9_TR_CTL1	0x4000A404	Trigger control register. See PERI_TR_GR9_TR_CTL0 for the details of bit fields.
PERI_TR_GR10_TR_CTL0	0x4000A800	Trigger control register

Register	Address	Description
PERI_TR_GR11_TR_CTL0	0x4000AC00	Trigger control register
PERI_TR_1TO1_GR0_TR_CTL0	0x4000C000	Trigger control register
PERI_TR_1TO1_GR0_TR_CTL1	0x4000C004	Trigger control register. See PERI_TR_1TO1_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR0_TR_CTL2	0x4000C008	Trigger control register. See PERI_TR_1TO1_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR0_TR_CTL3	0x4000C00C	Trigger control register. See PERI_TR_1TO1_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR0_TR_CTL4	0x4000C010	Trigger control register. See PERI_TR_1TO1_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR0_TR_CTL5	0x4000C014	Trigger control register. See PERI_TR_1TO1_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR0_TR_CTL6	0x4000C018	Trigger control register. See PERI_TR_1TO1_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR0_TR_CTL7	0x4000C01C	Trigger control register. See PERI_TR_1TO1_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR0_TR_CTL8	0x4000C020	Trigger control register. See PERI_TR_1TO1_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR0_TR_CTL9	0x4000C024	Trigger control register. See PERI_TR_1TO1_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR0_TR_CTL10	0x4000C028	Trigger control register. See PERI_TR_1TO1_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR0_TR_CTL11	0x4000C02C	Trigger control register. See PERI_TR_1TO1_GR0_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR1_TR_CTL0	0x4000C400	Trigger control register
PERI_TR_1TO1_GR1_TR_CTL1	0x4000C404	Trigger control register. See PERI_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR1_TR_CTL2	0x4000C408	Trigger control register. See PERI_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR1_TR_CTL3	0x4000C40C	Trigger control register. See PERI_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR1_TR_CTL4	0x4000C410	Trigger control register. See PERI_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR1_TR_CTL5	0x4000C414	Trigger control register. See PERI_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR1_TR_CTL6	0x4000C418	Trigger control register. See PERI_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR1_TR_CTL7	0x4000C41C	Trigger control register. See PERI_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR1_TR_CTL8	0x4000C420	Trigger control register. See PERI_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR1_TR_CTL9	0x4000C424	Trigger control register. See PERI_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR1_TR_CTL10	0x4000C428	Trigger control register. See PERI_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR1_TR_CTL11	0x4000C42C	Trigger control register. See PERI_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR1_TR_CTL12	0x4000C430	Trigger control register. See PERI_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR1_TR_CTL13	0x4000C434	Trigger control register. See PERI_TR_1TO1_GR1_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR2_TR_CTL0	0x4000C800	Trigger control register
PERI_TR_1TO1_GR3_TR_CTL0	0x4000CC00	Trigger control register
PERI_TR_1TO1_GR3_TR_CTL1	0x4000CC04	Trigger control register. See PERI_TR_1TO1_GR3_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR3_TR_CTL2	0x4000CC08	Trigger control register. See PERI_TR_1TO1_GR3_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR3_TR_CTL3	0x4000CC0C	Trigger control register. See PERI_TR_1TO1_GR3_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR3_TR_CTL4	0x4000CC10	Trigger control register. See PERI_TR_1TO1_GR3_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR3_TR_CTL5	0x4000CC14	Trigger control register. See PERI_TR_1TO1_GR3_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR3_TR_CTL6	0x4000CC18	Trigger control register. See PERI_TR_1TO1_GR3_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR4_TR_CTL0	0x4000D000	Trigger control register
PERI_TR_1TO1_GR4_TR_CTL1	0x4000D004	Trigger control register. See PERI_TR_1TO1_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR4_TR_CTL2	0x4000D008	Trigger control register. See PERI_TR_1TO1_GR4_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR5_TR_CTL0	0x4000D400	Trigger control register
PERI_TR_1TO1_GR5_TR_CTL1	0x4000D404	Trigger control register. See PERI_TR_1TO1_GR5_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR5_TR_CTL2	0x4000D408	Trigger control register. See PERI_TR_1TO1_GR5_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR5_TR_CTL3	0x4000D40C	Trigger control register. See PERI_TR_1TO1_GR5_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR5_TR_CTL4	0x4000D410	Trigger control register. See PERI_TR_1TO1_GR5_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR5_TR_CTL5	0x4000D414	Trigger control register. See PERI_TR_1TO1_GR5_TR_CTL0 for the details of bit fields.

Register	Address	Description
PERI_TR_1TO1_GR5_TR_CTL6	0x4000D418	Trigger control register. See PERI_TR_1TO1_GR5_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR5_TR_CTL7	0x4000D41C	Trigger control register. See PERI_TR_1TO1_GR5_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR6_TR_CTL0	0x4000D800	Trigger control register. See PERI_TR_1TO1_GR5_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR6_TR_CTL1	0x4000D804	Trigger control register. See PERI_TR_1TO1_GR5_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR6_TR_CTL2	0x4000D808	Trigger control register. See PERI_TR_1TO1_GR5_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR6_TR_CTL3	0x4000D80C	Trigger control register. See PERI_TR_1TO1_GR5_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR6_TR_CTL4	0x4000D810	Trigger control register. See PERI_TR_1TO1_GR5_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR6_TR_CTL5	0x4000D814	Trigger control register. See PERI_TR_1TO1_GR5_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR6_TR_CTL6	0x4000D818	Trigger control register. See PERI_TR_1TO1_GR5_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR6_TR_CTL7	0x4000D81C	Trigger control register. See PERI_TR_1TO1_GR5_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR7_TR_CTL0	0x4000DC00	Trigger control register. See PERI_TR_1TO1_GR2_TR_CTL0 for the details of bit fields.
PERI_TR_1TO1_GR8_TR_CTL0	0x4000E000	Trigger control register. See PERI_TR_1TO1_GR2_TR_CTL0 for the details of bit fields.
PERI_MS_PPU_PR0_SL_ADDR	0x40010000	Slave region, base address
PERI_MS_PPU_PR0_SL_SIZE	0x40010004	Slave region, size
PERI_MS_PPU_PR0_SL_ATT0	0x40010010	Slave attributes 0
PERI_MS_PPU_PR0_SL_ATT1	0x40010014	Slave attributes 1
PERI_MS_PPU_PR0_SL_ATT2	0x40010018	Slave attributes 2
PERI_MS_PPU_PR0_SL_ATT3	0x4001001C	Slave attributes 3
PERI_MS_PPU_PR0_MS_ADDR	0x40010020	Master region, base address
PERI_MS_PPU_PR0_MS_SIZE	0x40010024	Master region, size
PERI_MS_PPU_PR0_MS_ATT0	0x40010030	Master attributes 0
PERI_MS_PPU_PR0_MS_ATT1	0x40010034	Master attributes 1
PERI_MS_PPU_PR0_MS_ATT2	0x40010038	Master attributes 2
PERI_MS_PPU_PR0_MS_ATT3	0x4001003C	Master attributes 3
PERI_MS_PPU_PR1_SL_ADDR	0x40010040	Slave region, base address. See PERI_MS_PPU_PR0_SL_ADDR for the details of bit fields.
PERI_MS_PPU_PR1_SL_SIZE	0x40010044	Slave region, size. See PERI_MS_PPU_PR0_SL_SIZE for the details of bit fields.
PERI_MS_PPU_PR1_SL_ATT0	0x40010050	Slave attributes 0. See PERI_MS_PPU_PR0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_PR1_SL_ATT1	0x40010054	Slave attributes 1. See PERI_MS_PPU_PR0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_PR1_SL_ATT2	0x40010058	Slave attributes 2. See PERI_MS_PPU_PR0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_PR1_SL_ATT3	0x4001005C	Slave attributes 3. See PERI_MS_PPU_PR0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_PR1_MS_ADDR	0x40010060	Master region, base address
PERI_MS_PPU_PR1_MS_SIZE	0x40010064	Master region, size. See PERI_MS_PPU_PR0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_PR1_MS_ATT0	0x40010070	Master attributes 0. See PERI_MS_PPU_PR0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_PR1_MS_ATT1	0x40010074	Master attributes 1. See PERI_MS_PPU_PR0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_PR1_MS_ATT2	0x40010078	Master attributes 2. See PERI_MS_PPU_PR0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_PR1_MS_ATT3	0x4001007C	Master attributes 3. See PERI_MS_PPU_PR0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_PR2_SL_ADDR	0x40010080	Slave region, base address. See PERI_MS_PPU_PR0_SL_ADDR for the details of bit fields.
PERI_MS_PPU_PR2_SL_SIZE	0x40010084	Slave region, size. See PERI_MS_PPU_PR0_SL_SIZE for the details of bit fields.
PERI_MS_PPU_PR2_SL_ATT0	0x40010090	Slave attributes 0. See PERI_MS_PPU_PR0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_PR2_SL_ATT1	0x40010094	Slave attributes 1. See PERI_MS_PPU_PR0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_PR2_SL_ATT2	0x40010098	Slave attributes 2. See PERI_MS_PPU_PR0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_PR2_SL_ATT3	0x4001009C	Slave attributes 3. See PERI_MS_PPU_PR0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_PR2_MS_ADDR	0x400100A0	Master region, base address
PERI_MS_PPU_PR2_MS_SIZE	0x400100A4	Master region, size. See PERI_MS_PPU_PR0_MS_SIZE for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_PR2_MS_ATT0	0x400100B0	Master attributes 0. See PERI_MS_PPU_PR0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_PR2_MS_ATT1	0x400100B4	Master attributes 1. See PERI_MS_PPU_PR0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_PR2_MS_ATT2	0x400100B8	Master attributes 2. See PERI_MS_PPU_PR0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_PR2_MS_ATT3	0x400100BC	Master attributes 3. See PERI_MS_PPU_PR0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_PR3_SL_ADDR	0x400100C0	Slave region, base address. See PERI_MS_PPU_PR0_SL_ADDR for the details of bit fields.
PERI_MS_PPU_PR3_SL_SIZE	0x400100C4	Slave region, size. See PERI_MS_PPU_PR0_SL_SIZE for the details of bit fields.
PERI_MS_PPU_PR3_SL_ATT0	0x400100D0	Slave attributes 0. See PERI_MS_PPU_PR0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_PR3_SL_ATT1	0x400100D4	Slave attributes 1. See PERI_MS_PPU_PR0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_PR3_SL_ATT2	0x400100D8	Slave attributes 2. See PERI_MS_PPU_PR0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_PR3_SL_ATT3	0x400100DC	Slave attributes 3. See PERI_MS_PPU_PR0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_PR3_MS_ADDR	0x400100E0	Master region, base address
PERI_MS_PPU_PR3_MS_SIZE	0x400100E4	Master region, size. See PERI_MS_PPU_PR0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_PR3_MS_ATT0	0x400100F0	Master attributes 0. See PERI_MS_PPU_PR0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_PR3_MS_ATT1	0x400100F4	Master attributes 1. See PERI_MS_PPU_PR0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_PR3_MS_ATT2	0x400100F8	Master attributes 2. See PERI_MS_PPU_PR0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_PR3_MS_ATT3	0x400100FC	Master attributes 3. See PERI_MS_PPU_PR0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_PR4_SL_ADDR	0x40010100	Slave region, base address. See PERI_MS_PPU_PR0_SL_ADDR for the details of bit fields.
PERI_MS_PPU_PR4_SL_SIZE	0x40010104	Slave region, size. See PERI_MS_PPU_PR0_SL_SIZE for the details of bit fields.
PERI_MS_PPU_PR4_SL_ATT0	0x40010110	Slave attributes 0. See PERI_MS_PPU_PR0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_PR4_SL_ATT1	0x40010114	Slave attributes 1. See PERI_MS_PPU_PR0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_PR4_SL_ATT2	0x40010118	Slave attributes 2. See PERI_MS_PPU_PR0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_PR4_SL_ATT3	0x4001011C	Slave attributes 3. See PERI_MS_PPU_PR0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_PR4_MS_ADDR	0x40010120	Master region, base address
PERI_MS_PPU_PR4_MS_SIZE	0x40010124	Master region, size. See PERI_MS_PPU_PR0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_PR4_MS_ATT0	0x40010130	Master attributes 0. See PERI_MS_PPU_PR0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_PR4_MS_ATT1	0x40010134	Master attributes 1. See PERI_MS_PPU_PR0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_PR4_MS_ATT2	0x40010138	Master attributes 2. See PERI_MS_PPU_PR0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_PR4_MS_ATT3	0x4001013C	Master attributes 3. See PERI_MS_PPU_PR0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_PR5_SL_ADDR	0x40010140	Slave region, base address. See PERI_MS_PPU_PR0_SL_ADDR for the details of bit fields.
PERI_MS_PPU_PR5_SL_SIZE	0x40010144	Slave region, size. See PERI_MS_PPU_PR0_SL_SIZE for the details of bit fields.
PERI_MS_PPU_PR5_SL_ATT0	0x40010150	Slave attributes 0. See PERI_MS_PPU_PR0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_PR5_SL_ATT1	0x40010154	Slave attributes 1. See PERI_MS_PPU_PR0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_PR5_SL_ATT2	0x40010158	Slave attributes 2. See PERI_MS_PPU_PR0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_PR5_SL_ATT3	0x4001015C	Slave attributes 3. See PERI_MS_PPU_PR0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_PR5_MS_ADDR	0x40010160	Master region, base address
PERI_MS_PPU_PR5_MS_SIZE	0x40010164	Master region, size. See PERI_MS_PPU_PR0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_PR5_MS_ATT0	0x40010170	Master attributes 0. See PERI_MS_PPU_PR0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_PR5_MS_ATT1	0x40010174	Master attributes 1. See PERI_MS_PPU_PR0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_PR5_MS_ATT2	0x40010178	Master attributes 2. See PERI_MS_PPU_PR0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_PR5_MS_ATT3	0x4001017C	Master attributes 3. See PERI_MS_PPU_PR0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_PR6_SL_ADDR	0x40010180	Slave region, base address. See PERI_MS_PPU_PR0_SL_ADDR for the details of bit fields.
PERI_MS_PPU_PR6_SL_SIZE	0x40010184	Slave region, size. See PERI_MS_PPU_PR0_SL_SIZE for the details of bit fields.
PERI_MS_PPU_PR6_SL_ATT0	0x40010190	Slave attributes 0. See PERI_MS_PPU_PR0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_PR6_SL_ATT1	0x40010194	Slave attributes 1. See PERI_MS_PPU_PR0_SL_ATT1 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_PR6_SL_ATT2	0x40010198	Slave attributes 2. See PERI_MS_PPU_PR0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_PR6_SL_ATT3	0x4001019C	Slave attributes 3. See PERI_MS_PPU_PR0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_PR6_MS_ADDR	0x400101A0	Master region, base address
PERI_MS_PPU_PR6_MS_SIZE	0x400101A4	Master region, size. See PERI_MS_PPU_PR0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_PR6_MS_ATT0	0x400101B0	Master attributes 0. See PERI_MS_PPU_PR0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_PR6_MS_ATT1	0x400101B4	Master attributes 1. See PERI_MS_PPU_PR0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_PR6_MS_ATT2	0x400101B8	Master attributes 2. See PERI_MS_PPU_PR0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_PR6_MS_ATT3	0x400101BC	Master attributes 3. See PERI_MS_PPU_PR0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_PR7_SL_ADDR	0x400101C0	Slave region, base address. See PERI_MS_PPU_PR0_SL_ADDR for the details of bit fields.
PERI_MS_PPU_PR7_SL_SIZE	0x400101C4	Slave region, size. See PERI_MS_PPU_PR0_SL_SIZE for the details of bit fields.
PERI_MS_PPU_PR7_SL_ATT0	0x400101D0	Slave attributes 0. See PERI_MS_PPU_PR0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_PR7_SL_ATT1	0x400101D4	Slave attributes 1. See PERI_MS_PPU_PR0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_PR7_SL_ATT2	0x400101D8	Slave attributes 2. See PERI_MS_PPU_PR0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_PR7_SL_ATT3	0x400101DC	Slave attributes 3. See PERI_MS_PPU_PR0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_PR7_MS_ADDR	0x400101E0	Master region, base address
PERI_MS_PPU_PR7_MS_SIZE	0x400101E4	Master region, size. See PERI_MS_PPU_PR0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_PR7_MS_ATT0	0x400101F0	Master attributes 0. See PERI_MS_PPU_PR0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_PR7_MS_ATT1	0x400101F4	Master attributes 1. See PERI_MS_PPU_PR0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_PR7_MS_ATT2	0x400101F8	Master attributes 2. See PERI_MS_PPU_PR0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_PR7_MS_ATT3	0x400101FC	Master attributes 3. See PERI_MS_PPU_PR0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX0_SL_ADDR	0x40010800	Slave region, base address
PERI_MS_PPU_FX0_SL_SIZE	0x40010804	Slave region, size
PERI_MS_PPU_FX0_SL_ATT0	0x40010810	Slave attributes 0
PERI_MS_PPU_FX0_SL_ATT1	0x40010814	Slave attributes 1
PERI_MS_PPU_FX0_SL_ATT2	0x40010818	Slave attributes 2
PERI_MS_PPU_FX0_SL_ATT3	0x4001081C	Slave attributes 3
PERI_MS_PPU_FX0_MS_ADDR	0x40010820	Master region, base address
PERI_MS_PPU_FX0_MS_SIZE	0x40010824	Master region, size
PERI_MS_PPU_FX0_MS_ATT0	0x40010830	Master attributes 0
PERI_MS_PPU_FX0_MS_ATT1	0x40010834	Master attributes 1
PERI_MS_PPU_FX0_MS_ATT2	0x40010838	Master attributes 2
PERI_MS_PPU_FX0_MS_ATT3	0x4001083C	Master attributes 3
PERI_MS_PPU_FX1_SL_ADDR	0x40010840	Slave region, base address
PERI_MS_PPU_FX1_SL_SIZE	0x40010844	Slave region, size
PERI_MS_PPU_FX1_SL_ATT0	0x40010850	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX1_SL_ATT1	0x40010854	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX1_SL_ATT2	0x40010858	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX1_SL_ATT3	0x4001085C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX1_MS_ADDR	0x40010860	Master region, base address
PERI_MS_PPU_FX1_MS_SIZE	0x40010864	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX1_MS_ATT0	0x40010870	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX1_MS_ATT1	0x40010874	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX1_MS_ATT2	0x40010878	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX1_MS_ATT3	0x4001087C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX2_SL_ADDR	0x40010880	Slave region, base address
PERI_MS_PPU_FX2_SL_SIZE	0x40010884	Slave region, size. See PERI_MS_PPU_FX1_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX2_SL_ATT0	0x40010890	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX2_SL_ATT1	0x40010894	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX2_SL_ATT2	0x40010898	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX2_SL_ATT3	0x4001089C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX2_MS_ADDR	0x400108A0	Master region, base address
PERI_MS_PPU_FX2_MS_SIZE	0x400108A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX2_MS_ATT0	0x400108B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX2_MS_ATT1	0x400108B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX2_MS_ATT2	0x400108B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX2_MS_ATT3	0x400108BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX3_SL_ADDR	0x400108C0	Slave region, base address
PERI_MS_PPU_FX3_SL_SIZE	0x400108C4	Slave region, size. See PERI_MS_PPU_FX1_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX3_SL_ATT0	0x400108D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX3_SL_ATT1	0x400108D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX3_SL_ATT2	0x400108D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX3_SL_ATT3	0x400108DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX3_MS_ADDR	0x400108E0	Master region, base address
PERI_MS_PPU_FX3_MS_SIZE	0x400108E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX3_MS_ATT0	0x400108F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX3_MS_ATT1	0x400108F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX3_MS_ATT2	0x400108F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX3_MS_ATT3	0x400108FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX4_SL_ADDR	0x40010900	Slave region, base address
PERI_MS_PPU_FX4_SL_SIZE	0x40010904	Slave region, size
PERI_MS_PPU_FX4_SL_ATT0	0x40010910	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX4_SL_ATT1	0x40010914	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX4_SL_ATT2	0x40010918	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX4_SL_ATT3	0x4001091C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX4_MS_ADDR	0x40010920	Master region, base address
PERI_MS_PPU_FX4_MS_SIZE	0x40010924	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX4_MS_ATT0	0x40010930	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX4_MS_ATT1	0x40010934	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX4_MS_ATT2	0x40010938	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX4_MS_ATT3	0x4001093C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX5_SL_ADDR	0x40010940	Slave region, base address
PERI_MS_PPU_FX5_SL_SIZE	0x40010944	Slave region, size. See PERI_MS_PPU_FX4_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX5_SL_ATT0	0x40010950	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX5_SL_ATT1	0x40010954	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX5_SL_ATT2	0x40010958	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX5_SL_ATT3	0x4001095C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX5_MS_ADDR	0x40010960	Master region, base address
PERI_MS_PPU_FX5_MS_SIZE	0x40010964	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX5_MS_ATT0	0x40010970	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX5_MS_ATT1	0x40010974	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX5_MS_ATT2	0x40010978	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX5_MS_ATT3	0x4001097C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX6_SL_ADDR	0x40010980	Slave region, base address
PERI_MS_PPU_FX6_SL_SIZE	0x40010984	Slave region, size. See PERI_MS_PPU_FX4_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX6_SL_ATT0	0x40010990	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX6_SL_ATT1	0x40010994	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX6_SL_ATT2	0x40010998	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX6_SL_ATT3	0x4001099C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX6_MS_ADDR	0x400109A0	Master region, base address
PERI_MS_PPU_FX6_MS_SIZE	0x400109A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX6_MS_ATT0	0x400109B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX6_MS_ATT1	0x400109B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX6_MS_ATT2	0x400109B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX6_MS_ATT3	0x400109BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX7_SL_ADDR	0x400109C0	Slave region, base address
PERI_MS_PPU_FX7_SL_SIZE	0x400109C4	Slave region, size. See PERI_MS_PPU_FX4_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX7_SL_ATT0	0x400109D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX7_SL_ATT1	0x400109D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX7_SL_ATT2	0x400109D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX7_SL_ATT3	0x400109DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX7_MS_ADDR	0x400109E0	Master region, base address
PERI_MS_PPU_FX7_MS_SIZE	0x400109E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX7_MS_ATT0	0x400109F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX7_MS_ATT1	0x400109F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX7_MS_ATT2	0x400109F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX7_MS_ATT3	0x400109FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX8_SL_ADDR	0x40010A00	Slave region, base address
PERI_MS_PPU_FX8_SL_SIZE	0x40010A04	Slave region, size. See PERI_MS_PPU_FX4_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX8_SL_ATT0	0x40010A10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX8_SL_ATT1	0x40010A14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX8_SL_ATT2	0x40010A18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX8_SL_ATT3	0x40010A1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX8_MS_ADDR	0x40010A20	Master region, base address
PERI_MS_PPU_FX8_MS_SIZE	0x40010A24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX8_MS_ATT0	0x40010A30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX8_MS_ATT1	0x40010A34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX8_MS_ATT2	0x40010A38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX8_MS_ATT3	0x40010A3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX9_SL_ADDR	0x40010A40	Slave region, base address
PERI_MS_PPU_FX9_SL_SIZE	0x40010A44	Slave region, size
PERI_MS_PPU_FX9_SL_ATT0	0x40010A50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX9_SL_ATT1	0x40010A54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX9_SL_ATT2	0x40010A58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX9_SL_ATT3	0x40010A5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX9_MS_ADDR	0x40010A60	Master region, base address
PERI_MS_PPU_FX9_MS_SIZE	0x40010A64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX9_MS_ATT0	0x40010A70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX9_MS_ATT1	0x40010A74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX9_MS_ATT2	0x40010A78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX9_MS_ATT3	0x40010A7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX10_SL_ADDR	0x40010A80	Slave region, base address
PERI_MS_PPU_FX10_SL_SIZE	0x40010A84	Slave region, size
PERI_MS_PPU_FX10_SL_ATT0	0x40010A90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX10_SL_ATT1	0x40010A94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX10_SL_ATT2	0x40010A98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX10_SL_ATT3	0x40010A9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX10_MS_ADDR	0x40010AA0	Master region, base address
PERI_MS_PPU_FX10_MS_SIZE	0x40010AA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX10_MS_ATT0	0x40010AB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX10_MS_ATT1	0x40010AB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX10_MS_ATT2	0x40010AB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX10_MS_ATT3	0x40010ABC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX11_SL_ADDR	0x40010AC0	Slave region, base address
PERI_MS_PPU_FX11_SL_SIZE	0x40010AC4	Slave region, size
PERI_MS_PPU_FX11_SL_ATT0	0x40010AD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX11_SL_ATT1	0x40010AD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX11_SL_ATT2	0x40010AD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX11_SL_ATT3	0x40010ADC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX11_MS_ADDR	0x40010AE0	Master region, base address
PERI_MS_PPU_FX11_MS_SIZE	0x40010AE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX11_MS_ATT0	0x40010AF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX11_MS_ATT1	0x40010AF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX11_MS_ATT2	0x40010AF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX11_MS_ATT3	0x40010AFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX12_SL_ADDR	0x40010B00	Slave region, base address
PERI_MS_PPU_FX12_SL_SIZE	0x40010B04	Slave region, size
PERI_MS_PPU_FX12_SL_ATT0	0x40010B10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX12_SL_ATT1	0x40010B14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX12_SL_ATT2	0x40010B18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX12_SL_ATT3	0x40010B1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX12_MS_ADDR	0x40010B20	Master region, base address
PERI_MS_PPU_FX12_MS_SIZE	0x40010B24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX12_MS_ATT0	0x40010B30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX12_MS_ATT1	0x40010B34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX12_MS_ATT2	0x40010B38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX12_MS_ATT3	0x40010B3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX13_SL_ADDR	0x40010B40	Slave region, base address
PERI_MS_PPU_FX13_SL_SIZE	0x40010B44	Slave region, size. See PERI_MS_PPU_FX1_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX13_SL_ATT0	0x40010B50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX13_SL_ATT1	0x40010B54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX13_SL_ATT2	0x40010B58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX13_SL_ATT3	0x40010B5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX13_MS_ADDR	0x40010B60	Master region, base address
PERI_MS_PPU_FX13_MS_SIZE	0x40010B64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX13_MS_ATT0	0x40010B70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX13_MS_ATT1	0x40010B74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX13_MS_ATT2	0x40010B78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX13_MS_ATT3	0x40010B7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX14_SL_ADDR	0x40010B80	Slave region, base address
PERI_MS_PPU_FX14_SL_SIZE	0x40010B84	Slave region, size. See PERI_MS_PPU_FX1_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX14_SL_ATT0	0x40010B90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX14_SL_ATT1	0x40010B94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX14_SL_ATT2	0x40010B98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX14_SL_ATT3	0x40010B9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX14_MS_ADDR	0x40010BA0	Master region, base address
PERI_MS_PPU_FX14_MS_SIZE	0x40010BA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX14_MS_ATT0	0x40010BB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX14_MS_ATT1	0x40010BB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX14_MS_ATT2	0x40010BB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX14_MS_ATT3	0x40010BBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX15_SL_ADDR	0x40010BC0	Slave region, base address
PERI_MS_PPU_FX15_SL_SIZE	0x40010BC4	Slave region, size
PERI_MS_PPU_FX15_SL_ATT0	0x40010BD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX15_SL_ATT1	0x40010BD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX15_SL_ATT2	0x40010BD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX15_SL_ATT3	0x40010BDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX15_MS_ADDR	0x40010BE0	Master region, base address
PERI_MS_PPU_FX15_MS_SIZE	0x40010BE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX15_MS_ATT0	0x40010BF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX15_MS_ATT1	0x40010BF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX15_MS_ATT2	0x40010BF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX15_MS_ATT3	0x40010BFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX16_SL_ADDR	0x40010C00	Slave region, base address
PERI_MS_PPU_FX16_SL_SIZE	0x40010C04	Slave region, size. See PERI_MS_PPU_FX10_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX16_SL_ATT0	0x40010C10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX16_SL_ATT1	0x40010C14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX16_SL_ATT2	0x40010C18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX16_SL_ATT3	0x40010C1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX16_MS_ADDR	0x40010C20	Master region, base address
PERI_MS_PPU_FX16_MS_SIZE	0x40010C24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX16_MS_ATT0	0x40010C30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX16_MS_ATT1	0x40010C34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX16_MS_ATT2	0x40010C38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX16_MS_ATT3	0x40010C3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX17_SL_ADDR	0x40010C40	Slave region, base address
PERI_MS_PPU_FX17_SL_SIZE	0x40010C44	Slave region, size. See PERI_MS_PPU_FX15_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX17_SL_ATT0	0x40010C50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX17_SL_ATT1	0x40010C54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX17_SL_ATT2	0x40010C58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX17_SL_ATT3	0x40010C5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX17_MS_ADDR	0x40010C60	Master region, base address
PERI_MS_PPU_FX17_MS_SIZE	0x40010C64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX17_MS_ATT0	0x40010C70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX17_MS_ATT1	0x40010C74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX17_MS_ATT2	0x40010C78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX17_MS_ATT3	0x40010C7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX18_SL_ADDR	0x40010C80	Slave region, base address
PERI_MS_PPU_FX18_SL_SIZE	0x40010C84	Slave region, size
PERI_MS_PPU_FX18_SL_ATT0	0x40010C90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX18_SL_ATT1	0x40010C94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX18_SL_ATT2	0x40010C98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX18_SL_ATT3	0x40010C9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX18_MS_ADDR	0x40010CA0	Master region, base address
PERI_MS_PPU_FX18_MS_SIZE	0x40010CA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX18_MS_ATT0	0x40010CB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX18_MS_ATT1	0x40010CB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX18_MS_ATT2	0x40010CB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX18_MS_ATT3	0x40010CBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX19_SL_ADDR	0x40010CC0	Slave region, base address
PERI_MS_PPU_FX19_SL_SIZE	0x40010CC4	Slave region, size. See PERI_MS_PPU_FX10_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX19_SL_ATT0	0x40010CD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX19_SL_ATT1	0x40010CD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX19_SL_ATT2	0x40010CD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX19_SL_ATT3	0x40010CDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX19_MS_ADDR	0x40010CE0	Master region, base address
PERI_MS_PPU_FX19_MS_SIZE	0x40010CE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX19_MS_ATT0	0x40010CF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX19_MS_ATT1	0x40010CF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX19_MS_ATT2	0x40010CF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX19_MS_ATT3	0x40010CFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX20_SL_ADDR	0x40010D00	Slave region, base address
PERI_MS_PPU_FX20_SL_SIZE	0x40010D04	Slave region, size. See PERI_MS_PPU_FX10_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX20_SL_ATT0	0x40010D10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX20_SL_ATT1	0x40010D14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX20_SL_ATT2	0x40010D18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX20_SL_ATT3	0x40010D1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX20_MS_ADDR	0x40010D20	Master region, base address
PERI_MS_PPU_FX20_MS_SIZE	0x40010D24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX20_MS_ATT0	0x40010D30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX20_MS_ATT1	0x40010D34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX20_MS_ATT2	0x40010D38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX20_MS_ATT3	0x40010D3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX21_SL_ADDR	0x40010D40	Slave region, base address
PERI_MS_PPU_FX21_SL_SIZE	0x40010D44	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX21_SL_ATT0	0x40010D50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX21_SL_ATT1	0x40010D54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX21_SL_ATT2	0x40010D58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX21_SL_ATT3	0x40010D5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX21_MS_ADDR	0x40010D60	Master region, base address
PERI_MS_PPU_FX21_MS_SIZE	0x40010D64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX21_MS_ATT0	0x40010D70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX21_MS_ATT1	0x40010D74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX21_MS_ATT2	0x40010D78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX21_MS_ATT3	0x40010D7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX22_SL_ADDR	0x40010D80	Slave region, base address
PERI_MS_PPU_FX22_SL_SIZE	0x40010D84	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX22_SL_ATT0	0x40010D90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX22_SL_ATT1	0x40010D94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX22_SL_ATT2	0x40010D98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX22_SL_ATT3	0x40010D9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX22_MS_ADDR	0x40010DA0	Master region, base address
PERI_MS_PPU_FX22_MS_SIZE	0x40010DA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX22_MS_ATT0	0x40010DB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX22_MS_ATT1	0x40010DB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX22_MS_ATT2	0x40010DB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX22_MS_ATT3	0x40010DBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX23_SL_ADDR	0x40010DC0	Slave region, base address
PERI_MS_PPU_FX23_SL_SIZE	0x40010DC4	Slave region, size. See PERI_MS_PPU_FX4_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX23_SL_ATT0	0x40010DD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX23_SL_ATT1	0x40010DD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX23_SL_ATT2	0x40010DD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX23_SL_ATT3	0x40010DDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX23_MS_ADDR	0x40010DE0	Master region, base address
PERI_MS_PPU_FX23_MS_SIZE	0x40010DE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX23_MS_ATT0	0x40010DF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX23_MS_ATT1	0x40010DF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX23_MS_ATT2	0x40010DF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX23_MS_ATT3	0x40010DFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX24_SL_ADDR	0x40010E00	Slave region, base address
PERI_MS_PPU_FX24_SL_SIZE	0x40010E04	Slave region, size. See PERI_MS_PPU_FX4_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX24_SL_ATT0	0x40010E10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX24_SL_ATT1	0x40010E14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX24_SL_ATT2	0x40010E18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX24_SL_ATT3	0x40010E1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX24_MS_ADDR	0x40010E20	Master region, base address
PERI_MS_PPU_FX24_MS_SIZE	0x40010E24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX24_MS_ATT0	0x40010E30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX24_MS_ATT1	0x40010E34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX24_MS_ATT2	0x40010E38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX24_MS_ATT3	0x40010E3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX25_SL_ADDR	0x40010E40	Slave region, base address
PERI_MS_PPU_FX25_SL_SIZE	0x40010E44	Slave region, size. See PERI_MS_PPU_FX4_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX25_SL_ATT0	0x40010E50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX25_SL_ATT1	0x40010E54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX25_SL_ATT2	0x40010E58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX25_SL_ATT3	0x40010E5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX25_MS_ADDR	0x40010E60	Master region, base address
PERI_MS_PPU_FX25_MS_SIZE	0x40010E64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX25_MS_ATT0	0x40010E70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX25_MS_ATT1	0x40010E74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX25_MS_ATT2	0x40010E78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX25_MS_ATT3	0x40010E7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX26_SL_ADDR	0x40010E80	Slave region, base address
PERI_MS_PPU_FX26_SL_SIZE	0x40010E84	Slave region, size. See PERI_MS_PPU_FX4_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX26_SL_ATT0	0x40010E90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX26_SL_ATT1	0x40010E94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX26_SL_ATT2	0x40010E98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX26_SL_ATT3	0x40010E9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX26_MS_ADDR	0x40010EA0	Master region, base address
PERI_MS_PPU_FX26_MS_SIZE	0x40010EA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX26_MS_ATT0	0x40010EB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX26_MS_ATT1	0x40010EB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX26_MS_ATT2	0x40010EB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX26_MS_ATT3	0x40010EBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX27_SL_ADDR	0x40010EC0	Slave region, base address
PERI_MS_PPU_FX27_SL_SIZE	0x40010EC4	Slave region, size. See PERI_MS_PPU_FX4_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX27_SL_ATT0	0x40010ED0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX27_SL_ATT1	0x40010ED4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX27_SL_ATT2	0x40010ED8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX27_SL_ATT3	0x40010EDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX27_MS_ADDR	0x40010EE0	Master region, base address
PERI_MS_PPU_FX27_MS_SIZE	0x40010EE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX27_MS_ATT0	0x40010EF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX27_MS_ATT1	0x40010EF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX27_MS_ATT2	0x40010EF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX27_MS_ATT3	0x40010EFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX28_SL_ADDR	0x40010F00	Slave region, base address
PERI_MS_PPU_FX28_SL_SIZE	0x40010F04	Slave region, size. See PERI_MS_PPU_FX4_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX28_SL_ATT0	0x40010F10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX28_SL_ATT1	0x40010F14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX28_SL_ATT2	0x40010F18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX28_SL_ATT3	0x40010F1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX28_MS_ADDR	0x40010F20	Master region, base address
PERI_MS_PPU_FX28_MS_SIZE	0x40010F24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX28_MS_ATT0	0x40010F30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX28_MS_ATT1	0x40010F34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX28_MS_ATT2	0x40010F38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX28_MS_ATT3	0x40010F3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX29_SL_ADDR	0x40010F40	Slave region, base address
PERI_MS_PPU_FX29_SL_SIZE	0x40010F44	Slave region, size. See PERI_MS_PPU_FX4_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX29_SL_ATT0	0x40010F50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX29_SL_ATT1	0x40010F54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX29_SL_ATT2	0x40010F58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX29_SL_ATT3	0x40010F5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX29_MS_ADDR	0x40010F60	Master region, base address
PERI_MS_PPU_FX29_MS_SIZE	0x40010F64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX29_MS_ATT0	0x40010F70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX29_MS_ATT1	0x40010F74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX29_MS_ATT2	0x40010F78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX29_MS_ATT3	0x40010F7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX30_SL_ADDR	0x40010F80	Slave region, base address
PERI_MS_PPU_FX30_SL_SIZE	0x40010F84	Slave region, size. See PERI_MS_PPU_FX4_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX30_SL_ATT0	0x40010F90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX30_SL_ATT1	0x40010F94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX30_SL_ATT2	0x40010F98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX30_SL_ATT3	0x40010F9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX30_MS_ADDR	0x40010FA0	Master region, base address
PERI_MS_PPU_FX30_MS_SIZE	0x40010FA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX30_MS_ATT0	0x40010FB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX30_MS_ATT1	0x40010FB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX30_MS_ATT2	0x40010FB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX30_MS_ATT3	0x40010FBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX31_SL_ADDR	0x40010FC0	Slave region, base address
PERI_MS_PPU_FX31_SL_SIZE	0x40010FC4	Slave region, size. See PERI_MS_PPU_FX4_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX31_SL_ATT0	0x40010FD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX31_SL_ATT1	0x40010FD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX31_SL_ATT2	0x40010FD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX31_SL_ATT3	0x40010FDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX31_MS_ADDR	0x40010FE0	Master region, base address
PERI_MS_PPU_FX31_MS_SIZE	0x40010FE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX31_MS_ATT0	0x40010FF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX31_MS_ATT1	0x40010FF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX31_MS_ATT2	0x40010FF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX31_MS_ATT3	0x40010FFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX32_SL_ADDR	0x40011000	Slave region, base address
PERI_MS_PPU_FX32_SL_SIZE	0x40011004	Slave region, size. See PERI_MS_PPU_FX4_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX32_SL_ATT0	0x40011010	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX32_SL_ATT1	0x40011014	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX32_SL_ATT2	0x40011018	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX32_SL_ATT3	0x4001101C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX32_MS_ADDR	0x40011020	Master region, base address
PERI_MS_PPU_FX32_MS_SIZE	0x40011024	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX32_MS_ATT0	0x40011030	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX32_MS_ATT1	0x40011034	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX32_MS_ATT2	0x40011038	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX32_MS_ATT3	0x4001103C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX33_SL_ADDR	0x40011040	Slave region, base address
PERI_MS_PPU_FX33_SL_SIZE	0x40011044	Slave region, size. See PERI_MS_PPU_FX4_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX33_SL_ATT0	0x40011050	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX33_SL_ATT1	0x40011054	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX33_SL_ATT2	0x40011058	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX33_SL_ATT3	0x4001105C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX33_MS_ADDR	0x40011060	Master region, base address
PERI_MS_PPU_FX33_MS_SIZE	0x40011064	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX33_MS_ATT0	0x40011070	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX33_MS_ATT1	0x40011074	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX33_MS_ATT2	0x40011078	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX33_MS_ATT3	0x4001107C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX34_SL_ADDR	0x40011080	Slave region, base address
PERI_MS_PPU_FX34_SL_SIZE	0x40011084	Slave region, size. See PERI_MS_PPU_FX4_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX34_SL_ATT0	0x40011090	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX34_SL_ATT1	0x40011094	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX34_SL_ATT2	0x40011098	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX34_SL_ATT3	0x4001109C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX34_MS_ADDR	0x400110A0	Master region, base address
PERI_MS_PPU_FX34_MS_SIZE	0x400110A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX34_MS_ATT0	0x400110B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX34_MS_ATT1	0x400110B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX34_MS_ATT2	0x400110B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX34_MS_ATT3	0x400110BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX35_SL_ADDR	0x400110C0	Slave region, base address
PERI_MS_PPU_FX35_SL_SIZE	0x400110C4	Slave region, size. See PERI_MS_PPU_FX4_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX35_SL_ATT0	0x400110D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX35_SL_ATT1	0x400110D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX35_SL_ATT2	0x400110D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX35_SL_ATT3	0x400110DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX35_MS_ADDR	0x400110E0	Master region, base address
PERI_MS_PPU_FX35_MS_SIZE	0x400110E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX35_MS_ATT0	0x400110F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX35_MS_ATT1	0x400110F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX35_MS_ATT2	0x400110F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX35_MS_ATT3	0x400110FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX36_SL_ADDR	0x40011100	Slave region, base address
PERI_MS_PPU_FX36_SL_SIZE	0x40011104	Slave region, size. See PERI_MS_PPU_FX4_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX36_SL_ATT0	0x40011110	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX36_SL_ATT1	0x40011114	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX36_SL_ATT2	0x40011118	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX36_SL_ATT3	0x4001111C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX36_MS_ADDR	0x40011120	Master region, base address
PERI_MS_PPU_FX36_MS_SIZE	0x40011124	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX36_MS_ATT0	0x40011130	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX36_MS_ATT1	0x40011134	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX36_MS_ATT2	0x40011138	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX36_MS_ATT3	0x4001113C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX37_SL_ADDR	0x40011140	Slave region, base address
PERI_MS_PPU_FX37_SL_SIZE	0x40011144	Slave region, size. See PERI_MS_PPU_FX4_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX37_SL_ATT0	0x40011150	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX37_SL_ATT1	0x40011154	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX37_SL_ATT2	0x40011158	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX37_SL_ATT3	0x4001115C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX37_MS_ADDR	0x40011160	Master region, base address
PERI_MS_PPU_FX37_MS_SIZE	0x40011164	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX37_MS_ATT0	0x40011170	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX37_MS_ATT1	0x40011174	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX37_MS_ATT2	0x40011178	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX37_MS_ATT3	0x4001117C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX38_SL_ADDR	0x40011180	Slave region, base address
PERI_MS_PPU_FX38_SL_SIZE	0x40011184	Slave region, size. See PERI_MS_PPU_FX4_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX38_SL_ATT0	0x40011190	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX38_SL_ATT1	0x40011194	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX38_SL_ATT2	0x40011198	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX38_SL_ATT3	0x4001119C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX38_MS_ADDR	0x400111A0	Master region, base address
PERI_MS_PPU_FX38_MS_SIZE	0x400111A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX38_MS_ATT0	0x400111B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX38_MS_ATT1	0x400111B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX38_MS_ATT2	0x400111B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX38_MS_ATT3	0x400111BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX39_SL_ADDR	0x400111C0	Slave region, base address
PERI_MS_PPU_FX39_SL_SIZE	0x400111C4	Slave region, size
PERI_MS_PPU_FX39_SL_ATT0	0x400111D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX39_SL_ATT1	0x400111D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX39_SL_ATT2	0x400111D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX39_SL_ATT3	0x400111DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX39_MS_ADDR	0x400111E0	Master region, base address
PERI_MS_PPU_FX39_MS_SIZE	0x400111E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX39_MS_ATT0	0x400111F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX39_MS_ATT1	0x400111F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX39_MS_ATT2	0x400111F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX39_MS_ATT3	0x400111FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX40_SL_ADDR	0x40011200	Slave region, base address
PERI_MS_PPU_FX40_SL_SIZE	0x40011204	Slave region, size. See PERI_MS_PPU_FX39_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX40_SL_ATT0	0x40011210	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX40_SL_ATT1	0x40011214	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX40_SL_ATT2	0x40011218	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX40_SL_ATT3	0x4001121C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX40_MS_ADDR	0x40011220	Master region, base address
PERI_MS_PPU_FX40_MS_SIZE	0x40011224	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX40_MS_ATT0	0x40011230	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX40_MS_ATT1	0x40011234	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX40_MS_ATT2	0x40011238	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX40_MS_ATT3	0x4001123C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX41_SL_ADDR	0x40011240	Slave region, base address
PERI_MS_PPU_FX41_SL_SIZE	0x40011244	Slave region, size. See PERI_MS_PPU_FX39_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX41_SL_ATT0	0x40011250	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX41_SL_ATT1	0x40011254	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX41_SL_ATT2	0x40011258	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX41_SL_ATT3	0x4001125C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX41_MS_ADDR	0x40011260	Master region, base address
PERI_MS_PPU_FX41_MS_SIZE	0x40011264	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX41_MS_ATT0	0x40011270	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX41_MS_ATT1	0x40011274	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX41_MS_ATT2	0x40011278	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX41_MS_ATT3	0x4001127C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX42_SL_ADDR	0x40011280	Slave region, base address
PERI_MS_PPU_FX42_SL_SIZE	0x40011284	Slave region, size. See PERI_MS_PPU_FX39_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX42_SL_ATT0	0x40011290	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX42_SL_ATT1	0x40011294	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX42_SL_ATT2	0x40011298	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX42_SL_ATT3	0x4001129C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX42_MS_ADDR	0x400112A0	Master region, base address
PERI_MS_PPU_FX42_MS_SIZE	0x400112A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX42_MS_ATT0	0x400112B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX42_MS_ATT1	0x400112B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX42_MS_ATT2	0x400112B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX42_MS_ATT3	0x400112BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX43_SL_ADDR	0x400112C0	Slave region, base address
PERI_MS_PPU_FX43_SL_SIZE	0x400112C4	Slave region, size. See PERI_MS_PPU_FX39_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX43_SL_ATT0	0x400112D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX43_SL_ATT1	0x400112D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX43_SL_ATT2	0x400112D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX43_SL_ATT3	0x400112DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX43_MS_ADDR	0x400112E0	Master region, base address
PERI_MS_PPU_FX43_MS_SIZE	0x400112E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX43_MS_ATT0	0x400112F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX43_MS_ATT1	0x400112F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX43_MS_ATT2	0x400112F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX43_MS_ATT3	0x400112FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX44_SL_ADDR	0x40011300	Slave region, base address
PERI_MS_PPU_FX44_SL_SIZE	0x40011304	Slave region, size. See PERI_MS_PPU_FX39_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX44_SL_ATT0	0x40011310	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX44_SL_ATT1	0x40011314	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX44_SL_ATT2	0x40011318	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX44_SL_ATT3	0x4001131C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX44_MS_ADDR	0x40011320	Master region, base address
PERI_MS_PPU_FX44_MS_SIZE	0x40011324	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX44_MS_ATT0	0x40011330	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX44_MS_ATT1	0x40011334	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX44_MS_ATT2	0x40011338	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX44_MS_ATT3	0x4001133C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX45_SL_ADDR	0x40011340	Slave region, base address
PERI_MS_PPU_FX45_SL_SIZE	0x40011344	Slave region, size. See PERI_MS_PPU_FX39_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX45_SL_ATT0	0x40011350	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX45_SL_ATT1	0x40011354	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX45_SL_ATT2	0x40011358	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX45_SL_ATT3	0x4001135C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX45_MS_ADDR	0x40011360	Master region, base address
PERI_MS_PPU_FX45_MS_SIZE	0x40011364	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX45_MS_ATT0	0x40011370	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX45_MS_ATT1	0x40011374	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX45_MS_ATT2	0x40011378	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX45_MS_ATT3	0x4001137C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX46_SL_ADDR	0x40011380	Slave region, base address
PERI_MS_PPU_FX46_SL_SIZE	0x40011384	Slave region, size. See PERI_MS_PPU_FX39_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX46_SL_ATT0	0x40011390	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX46_SL_ATT1	0x40011394	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX46_SL_ATT2	0x40011398	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX46_SL_ATT3	0x4001139C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX46_MS_ADDR	0x400113A0	Master region, base address
PERI_MS_PPU_FX46_MS_SIZE	0x400113A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX46_MS_ATT0	0x400113B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX46_MS_ATT1	0x400113B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX46_MS_ATT2	0x400113B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX46_MS_ATT3	0x400113BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX47_SL_ADDR	0x400113C0	Slave region, base address
PERI_MS_PPU_FX47_SL_SIZE	0x400113C4	Slave region, size. See PERI_MS_PPU_FX39_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX47_SL_ATT0	0x400113D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX47_SL_ATT1	0x400113D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX47_SL_ATT2	0x400113D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX47_SL_ATT3	0x400113DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX47_MS_ADDR	0x400113E0	Master region, base address
PERI_MS_PPU_FX47_MS_SIZE	0x400113E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX47_MS_ATT0	0x400113F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX47_MS_ATT1	0x400113F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX47_MS_ATT2	0x400113F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX47_MS_ATT3	0x400113FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX48_SL_ADDR	0x40011400	Slave region, base address
PERI_MS_PPU_FX48_SL_SIZE	0x40011404	Slave region, size. See PERI_MS_PPU_FX39_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX48_SL_ATT0	0x40011410	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX48_SL_ATT1	0x40011414	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX48_SL_ATT2	0x40011418	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX48_SL_ATT3	0x4001141C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX48_MS_ADDR	0x40011420	Master region, base address
PERI_MS_PPU_FX48_MS_SIZE	0x40011424	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX48_MS_ATT0	0x40011430	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX48_MS_ATT1	0x40011434	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX48_MS_ATT2	0x40011438	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX48_MS_ATT3	0x4001143C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX49_SL_ADDR	0x40011440	Slave region, base address
PERI_MS_PPU_FX49_SL_SIZE	0x40011444	Slave region, size. See PERI_MS_PPU_FX39_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX49_SL_ATT0	0x40011450	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX49_SL_ATT1	0x40011454	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX49_SL_ATT2	0x40011458	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX49_SL_ATT3	0x4001145C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX49_MS_ADDR	0x40011460	Master region, base address
PERI_MS_PPU_FX49_MS_SIZE	0x40011464	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX49_MS_ATT0	0x40011470	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX49_MS_ATT1	0x40011474	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX49_MS_ATT2	0x40011478	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX49_MS_ATT3	0x4001147C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX50_SL_ADDR	0x40011480	Slave region, base address
PERI_MS_PPU_FX50_SL_SIZE	0x40011484	Slave region, size. See PERI_MS_PPU_FX39_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX50_SL_ATT0	0x40011490	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX50_SL_ATT1	0x40011494	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX50_SL_ATT2	0x40011498	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX50_SL_ATT3	0x4001149C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX50_MS_ADDR	0x400114A0	Master region, base address
PERI_MS_PPU_FX50_MS_SIZE	0x400114A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX50_MS_ATT0	0x400114B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX50_MS_ATT1	0x400114B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX50_MS_ATT2	0x400114B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX50_MS_ATT3	0x400114BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX51_SL_ADDR	0x400114C0	Slave region, base address
PERI_MS_PPU_FX51_SL_SIZE	0x400114C4	Slave region, size. See PERI_MS_PPU_FX39_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX51_SL_ATT0	0x400114D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX51_SL_ATT1	0x400114D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX51_SL_ATT2	0x400114D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX51_SL_ATT3	0x400114DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX51_MS_ADDR	0x400114E0	Master region, base address
PERI_MS_PPU_FX51_MS_SIZE	0x400114E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX51_MS_ATT0	0x400114F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX51_MS_ATT1	0x400114F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX51_MS_ATT2	0x400114F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX51_MS_ATT3	0x400114FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX52_SL_ADDR	0x40011500	Slave region, base address
PERI_MS_PPU_FX52_SL_SIZE	0x40011504	Slave region, size. See PERI_MS_PPU_FX39_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX52_SL_ATT0	0x40011510	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX52_SL_ATT1	0x40011514	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX52_SL_ATT2	0x40011518	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX52_SL_ATT3	0x4001151C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX52_MS_ADDR	0x40011520	Master region, base address
PERI_MS_PPU_FX52_MS_SIZE	0x40011524	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX52_MS_ATT0	0x40011530	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX52_MS_ATT1	0x40011534	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX52_MS_ATT2	0x40011538	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX52_MS_ATT3	0x4001153C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX53_SL_ADDR	0x40011540	Slave region, base address
PERI_MS_PPU_FX53_SL_SIZE	0x40011544	Slave region, size. See PERI_MS_PPU_FX39_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX53_SL_ATT0	0x40011550	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX53_SL_ATT1	0x40011554	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX53_SL_ATT2	0x40011558	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX53_SL_ATT3	0x4001155C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX53_MS_ADDR	0x40011560	Master region, base address
PERI_MS_PPU_FX53_MS_SIZE	0x40011564	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX53_MS_ATT0	0x40011570	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX53_MS_ATT1	0x40011574	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX53_MS_ATT2	0x40011578	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX53_MS_ATT3	0x4001157C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX54_SL_ADDR	0x40011580	Slave region, base address
PERI_MS_PPU_FX54_SL_SIZE	0x40011584	Slave region, size. See PERI_MS_PPU_FX39_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX54_SL_ATT0	0x40011590	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX54_SL_ATT1	0x40011594	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX54_SL_ATT2	0x40011598	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX54_SL_ATT3	0x4001159C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX54_MS_ADDR	0x400115A0	Master region, base address
PERI_MS_PPU_FX54_MS_SIZE	0x400115A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX54_MS_ATT0	0x400115B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX54_MS_ATT1	0x400115B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX54_MS_ATT2	0x400115B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX54_MS_ATT3	0x400115BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX55_SL_ADDR	0x400115C0	Slave region, base address
PERI_MS_PPU_FX55_SL_SIZE	0x400115C4	Slave region, size
PERI_MS_PPU_FX55_SL_ATT0	0x400115D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX55_SL_ATT1	0x400115D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX55_SL_ATT2	0x400115D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX55_SL_ATT3	0x400115DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX55_MS_ADDR	0x400115E0	Master region, base address
PERI_MS_PPU_FX55_MS_SIZE	0x400115E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX55_MS_ATT0	0x400115F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX55_MS_ATT1	0x400115F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX55_MS_ATT2	0x400115F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX55_MS_ATT3	0x400115FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX56_SL_ADDR	0x40011600	Slave region, base address
PERI_MS_PPU_FX56_SL_SIZE	0x40011604	Slave region, size. See PERI_MS_PPU_FX1_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX56_SL_ATT0	0x40011610	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX56_SL_ATT1	0x40011614	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX56_SL_ATT2	0x40011618	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX56_SL_ATT3	0x4001161C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX56_MS_ADDR	0x40011620	Master region, base address
PERI_MS_PPU_FX56_MS_SIZE	0x40011624	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX56_MS_ATT0	0x40011630	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX56_MS_ATT1	0x40011634	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX56_MS_ATT2	0x40011638	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX56_MS_ATT3	0x4001163C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX57_SL_ADDR	0x40011640	Slave region, base address
PERI_MS_PPU_FX57_SL_SIZE	0x40011644	Slave region, size. See PERI_MS_PPU_FX1_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX57_SL_ATT0	0x40011650	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX57_SL_ATT1	0x40011654	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX57_SL_ATT2	0x40011658	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX57_SL_ATT3	0x4001165C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX57_MS_ADDR	0x40011660	Master region, base address
PERI_MS_PPU_FX57_MS_SIZE	0x40011664	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX57_MS_ATT0	0x40011670	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX57_MS_ATT1	0x40011674	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX57_MS_ATT2	0x40011678	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX57_MS_ATT3	0x4001167C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX58_SL_ADDR	0x40011680	Slave region, base address
PERI_MS_PPU_FX58_SL_SIZE	0x40011684	Slave region, size. See PERI_MS_PPU_FX10_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX58_SL_ATT0	0x40011690	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX58_SL_ATT1	0x40011694	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX58_SL_ATT2	0x40011698	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX58_SL_ATT3	0x4001169C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX58_MS_ADDR	0x400116A0	Master region, base address
PERI_MS_PPU_FX58_MS_SIZE	0x400116A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX58_MS_ATT0	0x400116B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX58_MS_ATT1	0x400116B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX58_MS_ATT2	0x400116B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX58_MS_ATT3	0x400116BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX59_SL_ADDR	0x400116C0	Slave region, base address
PERI_MS_PPU_FX59_SL_SIZE	0x400116C4	Slave region, size
PERI_MS_PPU_FX59_SL_ATT0	0x400116D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX59_SL_ATT1	0x400116D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX59_SL_ATT2	0x400116D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX59_SL_ATT3	0x400116DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX59_MS_ADDR	0x400116E0	Master region, base address
PERI_MS_PPU_FX59_MS_SIZE	0x400116E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX59_MS_ATT0	0x400116F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX59_MS_ATT1	0x400116F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX59_MS_ATT2	0x400116F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX59_MS_ATT3	0x400116FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX60_SL_ADDR	0x40011700	Slave region, base address
PERI_MS_PPU_FX60_SL_SIZE	0x40011704	Slave region, size. See PERI_MS_PPU_FX1_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX60_SL_ATT0	0x40011710	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX60_SL_ATT1	0x40011714	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX60_SL_ATT2	0x40011718	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX60_SL_ATT3	0x4001171C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX60_MS_ADDR	0x40011720	Master region, base address
PERI_MS_PPU_FX60_MS_SIZE	0x40011724	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX60_MS_ATT0	0x40011730	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX60_MS_ATT1	0x40011734	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX60_MS_ATT2	0x40011738	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX60_MS_ATT3	0x4001173C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX61_SL_ADDR	0x40011740	Slave region, base address
PERI_MS_PPU_FX61_SL_SIZE	0x40011744	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX61_SL_ATT0	0x40011750	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX61_SL_ATT1	0x40011754	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX61_SL_ATT2	0x40011758	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX61_SL_ATT3	0x4001175C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX61_MS_ADDR	0x40011760	Master region, base address
PERI_MS_PPU_FX61_MS_SIZE	0x40011764	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX61_MS_ATT0	0x40011770	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX61_MS_ATT1	0x40011774	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX61_MS_ATT2	0x40011778	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX61_MS_ATT3	0x4001177C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX62_SL_ADDR	0x40011780	Slave region, base address
PERI_MS_PPU_FX62_SL_SIZE	0x40011784	Slave region, size
PERI_MS_PPU_FX62_SL_ATT0	0x40011790	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX62_SL_ATT1	0x40011794	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX62_SL_ATT2	0x40011798	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX62_SL_ATT3	0x4001179C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX62_MS_ADDR	0x400117A0	Master region, base address
PERI_MS_PPU_FX62_MS_SIZE	0x400117A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX62_MS_ATT0	0x400117B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX62_MS_ATT1	0x400117B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX62_MS_ATT2	0x400117B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX62_MS_ATT3	0x400117BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX63_SL_ADDR	0x400117C0	Slave region, base address
PERI_MS_PPU_FX63_SL_SIZE	0x400117C4	Slave region, size. See PERI_MS_PPU_FX62_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX63_SL_ATT0	0x400117D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX63_SL_ATT1	0x400117D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX63_SL_ATT2	0x400117D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX63_SL_ATT3	0x400117DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX63_MS_ADDR	0x400117E0	Master region, base address
PERI_MS_PPU_FX63_MS_SIZE	0x400117E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX63_MS_ATT0	0x400117F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX63_MS_ATT1	0x400117F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX63_MS_ATT2	0x400117F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX63_MS_ATT3	0x400117FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX64_SL_ADDR	0x40011800	Slave region, base address
PERI_MS_PPU_FX64_SL_SIZE	0x40011804	Slave region, size. See PERI_MS_PPU_FX1_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX64_SL_ATT0	0x40011810	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX64_SL_ATT1	0x40011814	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX64_SL_ATT2	0x40011818	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX64_SL_ATT3	0x4001181C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX64_MS_ADDR	0x40011820	Master region, base address
PERI_MS_PPU_FX64_MS_SIZE	0x40011824	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX64_MS_ATT0	0x40011830	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX64_MS_ATT1	0x40011834	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX64_MS_ATT2	0x40011838	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX64_MS_ATT3	0x4001183C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX65_SL_ADDR	0x40011840	Slave region, base address
PERI_MS_PPU_FX65_SL_SIZE	0x40011844	Slave region, size. See PERI_MS_PPU_FX1_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX65_SL_ATT0	0x40011850	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX65_SL_ATT1	0x40011854	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX65_SL_ATT2	0x40011858	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX65_SL_ATT3	0x4001185C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX65_MS_ADDR	0x40011860	Master region, base address
PERI_MS_PPU_FX65_MS_SIZE	0x40011864	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX65_MS_ATT0	0x40011870	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX65_MS_ATT1	0x40011874	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX65_MS_ATT2	0x40011878	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX65_MS_ATT3	0x4001187C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX66_SL_ADDR	0x40011880	Slave region, base address
PERI_MS_PPU_FX66_SL_SIZE	0x40011884	Slave region, size. See PERI_MS_PPU_FX1_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX66_SL_ATT0	0x40011890	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX66_SL_ATT1	0x40011894	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX66_SL_ATT2	0x40011898	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX66_SL_ATT3	0x4001189C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX66_MS_ADDR	0x400118A0	Master region, base address
PERI_MS_PPU_FX66_MS_SIZE	0x400118A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX66_MS_ATT0	0x400118B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX66_MS_ATT1	0x400118B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX66_MS_ATT2	0x400118B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX66_MS_ATT3	0x400118BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX67_SL_ADDR	0x400118C0	Slave region, base address
PERI_MS_PPU_FX67_SL_SIZE	0x400118C4	Slave region, size. See PERI_MS_PPU_FX1_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX67_SL_ATT0	0x400118D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX67_SL_ATT1	0x400118D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX67_SL_ATT2	0x400118D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX67_SL_ATT3	0x400118DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX67_MS_ADDR	0x400118E0	Master region, base address
PERI_MS_PPU_FX67_MS_SIZE	0x400118E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX67_MS_ATT0	0x400118F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX67_MS_ATT1	0x400118F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX67_MS_ATT2	0x400118F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX67_MS_ATT3	0x400118FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX68_SL_ADDR	0x40011900	Slave region, base address
PERI_MS_PPU_FX68_SL_SIZE	0x40011904	Slave region, size. See PERI_MS_PPU_FX15_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX68_SL_ATT0	0x40011910	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX68_SL_ATT1	0x40011914	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX68_SL_ATT2	0x40011918	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX68_SL_ATT3	0x4001191C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX68_MS_ADDR	0x40011920	Master region, base address
PERI_MS_PPU_FX68_MS_SIZE	0x40011924	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX68_MS_ATT0	0x40011930	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX68_MS_ATT1	0x40011934	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX68_MS_ATT2	0x40011938	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX68_MS_ATT3	0x4001193C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX69_SL_ADDR	0x40011940	Slave region, base address
PERI_MS_PPU_FX69_SL_SIZE	0x40011944	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX69_SL_ATT0	0x40011950	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX69_SL_ATT1	0x40011954	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX69_SL_ATT2	0x40011958	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX69_SL_ATT3	0x4001195C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX69_MS_ADDR	0x40011960	Master region, base address
PERI_MS_PPU_FX69_MS_SIZE	0x40011964	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX69_MS_ATT0	0x40011970	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX69_MS_ATT1	0x40011974	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX69_MS_ATT2	0x40011978	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX69_MS_ATT3	0x4001197C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX70_SL_ADDR	0x40011980	Slave region, base address
PERI_MS_PPU_FX70_SL_SIZE	0x40011984	Slave region, size. See PERI_MS_PPU_FX39_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX70_SL_ATT0	0x40011990	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX70_SL_ATT1	0x40011994	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX70_SL_ATT2	0x40011998	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX70_SL_ATT3	0x4001199C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX70_MS_ADDR	0x400119A0	Master region, base address
PERI_MS_PPU_FX70_MS_SIZE	0x400119A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX70_MS_ATT0	0x400119B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX70_MS_ATT1	0x400119B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX70_MS_ATT2	0x400119B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX70_MS_ATT3	0x400119BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX71_SL_ADDR	0x400119C0	Slave region, base address
PERI_MS_PPU_FX71_SL_SIZE	0x400119C4	Slave region, size. See PERI_MS_PPU_FX39_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX71_SL_ATT0	0x400119D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX71_SL_ATT1	0x400119D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX71_SL_ATT2	0x400119D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX71_SL_ATT3	0x400119DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX71_MS_ADDR	0x400119E0	Master region, base address
PERI_MS_PPU_FX71_MS_SIZE	0x400119E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX71_MS_ATT0	0x400119F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX71_MS_ATT1	0x400119F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX71_MS_ATT2	0x400119F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX71_MS_ATT3	0x400119FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX72_SL_ADDR	0x40011A00	Slave region, base address
PERI_MS_PPU_FX72_SL_SIZE	0x40011A04	Slave region, size. See PERI_MS_PPU_FX62_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX72_SL_ATT0	0x40011A10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX72_SL_ATT1	0x40011A14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX72_SL_ATT2	0x40011A18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX72_SL_ATT3	0x40011A1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX72_MS_ADDR	0x40011A20	Master region, base address
PERI_MS_PPU_FX72_MS_SIZE	0x40011A24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX72_MS_ATT0	0x40011A30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX72_MS_ATT1	0x40011A34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX72_MS_ATT2	0x40011A38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX72_MS_ATT3	0x40011A3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX73_SL_ADDR	0x40011A40	Slave region, base address
PERI_MS_PPU_FX73_SL_SIZE	0x40011A44	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX73_SL_ATT0	0x40011A50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX73_SL_ATT1	0x40011A54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX73_SL_ATT2	0x40011A58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX73_SL_ATT3	0x40011A5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX73_MS_ADDR	0x40011A60	Master region, base address
PERI_MS_PPU_FX73_MS_SIZE	0x40011A64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX73_MS_ATT0	0x40011A70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX73_MS_ATT1	0x40011A74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX73_MS_ATT2	0x40011A78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX73_MS_ATT3	0x40011A7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX74_SL_ADDR	0x40011A80	Slave region, base address
PERI_MS_PPU_FX74_SL_SIZE	0x40011A84	Slave region, size. See PERI_MS_PPU_FX10_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX74_SL_ATT0	0x40011A90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX74_SL_ATT1	0x40011A94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX74_SL_ATT2	0x40011A98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX74_SL_ATT3	0x40011A9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX74_MS_ADDR	0x40011AA0	Master region, base address
PERI_MS_PPU_FX74_MS_SIZE	0x40011AA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX74_MS_ATT0	0x40011AB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX74_MS_ATT1	0x40011AB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX74_MS_ATT2	0x40011AB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX74_MS_ATT3	0x40011ABC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX75_SL_ADDR	0x40011AC0	Slave region, base address
PERI_MS_PPU_FX75_SL_SIZE	0x40011AC4	Slave region, size. See PERI_MS_PPU_FX59_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX75_SL_ATT0	0x40011AD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX75_SL_ATT1	0x40011AD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX75_SL_ATT2	0x40011AD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX75_SL_ATT3	0x40011ADC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX75_MS_ADDR	0x40011AE0	Master region, base address
PERI_MS_PPU_FX75_MS_SIZE	0x40011AE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX75_MS_ATT0	0x40011AF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX75_MS_ATT1	0x40011AF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX75_MS_ATT2	0x40011AF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX75_MS_ATT3	0x40011AFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX76_SL_ADDR	0x40011B00	Slave region, base address
PERI_MS_PPU_FX76_SL_SIZE	0x40011B04	Slave region, size. See PERI_MS_PPU_FX15_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX76_SL_ATT0	0x40011B10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX76_SL_ATT1	0x40011B14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX76_SL_ATT2	0x40011B18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX76_SL_ATT3	0x40011B1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX76_MS_ADDR	0x40011B20	Master region, base address
PERI_MS_PPU_FX76_MS_SIZE	0x40011B24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX76_MS_ATT0	0x40011B30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX76_MS_ATT1	0x40011B34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX76_MS_ATT2	0x40011B38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX76_MS_ATT3	0x40011B3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX77_SL_ADDR	0x40011B40	Slave region, base address
PERI_MS_PPU_FX77_SL_SIZE	0x40011B44	Slave region, size. See PERI_MS_PPU_FX62_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX77_SL_ATT0	0x40011B50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX77_SL_ATT1	0x40011B54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX77_SL_ATT2	0x40011B58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX77_SL_ATT3	0x40011B5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX77_MS_ADDR	0x40011B60	Master region, base address
PERI_MS_PPU_FX77_MS_SIZE	0x40011B64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX77_MS_ATT0	0x40011B70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX77_MS_ATT1	0x40011B74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX77_MS_ATT2	0x40011B78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX77_MS_ATT3	0x40011B7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX78_SL_ADDR	0x40011B80	Slave region, base address
PERI_MS_PPU_FX78_SL_SIZE	0x40011B84	Slave region, size
PERI_MS_PPU_FX78_SL_ATT0	0x40011B90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX78_SL_ATT1	0x40011B94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX78_SL_ATT2	0x40011B98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX78_SL_ATT3	0x40011B9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX78_MS_ADDR	0x40011BA0	Master region, base address
PERI_MS_PPU_FX78_MS_SIZE	0x40011BA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX78_MS_ATT0	0x40011BB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX78_MS_ATT1	0x40011BB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX78_MS_ATT2	0x40011BB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX78_MS_ATT3	0x40011BBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX79_SL_ADDR	0x40011BC0	Slave region, base address
PERI_MS_PPU_FX79_SL_SIZE	0x40011BC4	Slave region, size. See PERI_MS_PPU_FX62_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX79_SL_ATT0	0x40011BD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX79_SL_ATT1	0x40011BD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX79_SL_ATT2	0x40011BD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX79_SL_ATT3	0x40011BDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX79_MS_ADDR	0x40011BE0	Master region, base address
PERI_MS_PPU_FX79_MS_SIZE	0x40011BE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX79_MS_ATT0	0x40011BF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX79_MS_ATT1	0x40011BF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX79_MS_ATT2	0x40011BF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX79_MS_ATT3	0x40011BFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX80_SL_ADDR	0x40011C00	Slave region, base address
PERI_MS_PPU_FX80_SL_SIZE	0x40011C04	Slave region, size. See PERI_MS_PPU_FX62_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX80_SL_ATT0	0x40011C10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX80_SL_ATT1	0x40011C14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX80_SL_ATT2	0x40011C18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX80_SL_ATT3	0x40011C1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX80_MS_ADDR	0x40011C20	Master region, base address
PERI_MS_PPU_FX80_MS_SIZE	0x40011C24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX80_MS_ATT0	0x40011C30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX80_MS_ATT1	0x40011C34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX80_MS_ATT2	0x40011C38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX80_MS_ATT3	0x40011C3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX81_SL_ADDR	0x40011C40	Slave region, base address
PERI_MS_PPU_FX81_SL_SIZE	0x40011C44	Slave region, size. See PERI_MS_PPU_FX62_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX81_SL_ATT0	0x40011C50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX81_SL_ATT1	0x40011C54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX81_SL_ATT2	0x40011C58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX81_SL_ATT3	0x40011C5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX81_MS_ADDR	0x40011C60	Master region, base address
PERI_MS_PPU_FX81_MS_SIZE	0x40011C64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX81_MS_ATT0	0x40011C70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX81_MS_ATT1	0x40011C74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX81_MS_ATT2	0x40011C78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX81_MS_ATT3	0x40011C7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX82_SL_ADDR	0x40011C80	Slave region, base address
PERI_MS_PPU_FX82_SL_SIZE	0x40011C84	Slave region, size. See PERI_MS_PPU_FX62_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX82_SL_ATT0	0x40011C90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX82_SL_ATT1	0x40011C94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX82_SL_ATT2	0x40011C98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX82_SL_ATT3	0x40011C9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX82_MS_ADDR	0x40011CA0	Master region, base address
PERI_MS_PPU_FX82_MS_SIZE	0x40011CA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX82_MS_ATT0	0x40011CB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX82_MS_ATT1	0x40011CB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX82_MS_ATT2	0x40011CB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX82_MS_ATT3	0x40011CBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX83_SL_ADDR	0x40011CC0	Slave region, base address
PERI_MS_PPU_FX83_SL_SIZE	0x40011CC4	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX83_SL_ATT0	0x40011CD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX83_SL_ATT1	0x40011CD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX83_SL_ATT2	0x40011CD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX83_SL_ATT3	0x40011CDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX83_MS_ADDR	0x40011CE0	Master region, base address
PERI_MS_PPU_FX83_MS_SIZE	0x40011CE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX83_MS_ATT0	0x40011CF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX83_MS_ATT1	0x40011CF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX83_MS_ATT2	0x40011CF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX83_MS_ATT3	0x40011CFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX84_SL_ADDR	0x40011D00	Slave region, base address
PERI_MS_PPU_FX84_SL_SIZE	0x40011D04	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX84_SL_ATT0	0x40011D10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX84_SL_ATT1	0x40011D14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX84_SL_ATT2	0x40011D18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX84_SL_ATT3	0x40011D1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX84_MS_ADDR	0x40011D20	Master region, base address
PERI_MS_PPU_FX84_MS_SIZE	0x40011D24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX84_MS_ATT0	0x40011D30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX84_MS_ATT1	0x40011D34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX84_MS_ATT2	0x40011D38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX84_MS_ATT3	0x40011D3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX85_SL_ADDR	0x40011D40	Slave region, base address
PERI_MS_PPU_FX85_SL_SIZE	0x40011D44	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX85_SL_ATT0	0x40011D50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX85_SL_ATT1	0x40011D54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX85_SL_ATT2	0x40011D58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX85_SL_ATT3	0x40011D5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX85_MS_ADDR	0x40011D60	Master region, base address
PERI_MS_PPU_FX85_MS_SIZE	0x40011D64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX85_MS_ATT0	0x40011D70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX85_MS_ATT1	0x40011D74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX85_MS_ATT2	0x40011D78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX85_MS_ATT3	0x40011D7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX86_SL_ADDR	0x40011D80	Slave region, base address
PERI_MS_PPU_FX86_SL_SIZE	0x40011D84	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX86_SL_ATT0	0x40011D90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX86_SL_ATT1	0x40011D94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX86_SL_ATT2	0x40011D98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX86_SL_ATT3	0x40011D9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX86_MS_ADDR	0x40011DA0	Master region, base address
PERI_MS_PPU_FX86_MS_SIZE	0x40011DA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX86_MS_ATT0	0x40011DB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX86_MS_ATT1	0x40011DB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX86_MS_ATT2	0x40011DB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX86_MS_ATT3	0x40011DBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX87_SL_ADDR	0x40011DC0	Slave region, base address
PERI_MS_PPU_FX87_SL_SIZE	0x40011DC4	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX87_SL_ATT0	0x40011DD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX87_SL_ATT1	0x40011DD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX87_SL_ATT2	0x40011DD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX87_SL_ATT3	0x40011DDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX87_MS_ADDR	0x40011DE0	Master region, base address
PERI_MS_PPU_FX87_MS_SIZE	0x40011DE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX87_MS_ATT0	0x40011DF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX87_MS_ATT1	0x40011DF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX87_MS_ATT2	0x40011DF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX87_MS_ATT3	0x40011DFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX88_SL_ADDR	0x40011E00	Slave region, base address
PERI_MS_PPU_FX88_SL_SIZE	0x40011E04	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX88_SL_ATT0	0x40011E10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX88_SL_ATT1	0x40011E14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX88_SL_ATT2	0x40011E18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX88_SL_ATT3	0x40011E1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX88_MS_ADDR	0x40011E20	Master region, base address
PERI_MS_PPU_FX88_MS_SIZE	0x40011E24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX88_MS_ATT0	0x40011E30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX88_MS_ATT1	0x40011E34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX88_MS_ATT2	0x40011E38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX88_MS_ATT3	0x40011E3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX89_SL_ADDR	0x40011E40	Slave region, base address
PERI_MS_PPU_FX89_SL_SIZE	0x40011E44	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX89_SL_ATT0	0x40011E50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX89_SL_ATT1	0x40011E54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX89_SL_ATT2	0x40011E58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX89_SL_ATT3	0x40011E5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX89_MS_ADDR	0x40011E60	Master region, base address
PERI_MS_PPU_FX89_MS_SIZE	0x40011E64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX89_MS_ATT0	0x40011E70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX89_MS_ATT1	0x40011E74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX89_MS_ATT2	0x40011E78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX89_MS_ATT3	0x40011E7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX90_SL_ADDR	0x40011E80	Slave region, base address
PERI_MS_PPU_FX90_SL_SIZE	0x40011E84	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX90_SL_ATT0	0x40011E90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX90_SL_ATT1	0x40011E94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX90_SL_ATT2	0x40011E98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX90_SL_ATT3	0x40011E9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX90_MS_ADDR	0x40011EA0	Master region, base address
PERI_MS_PPU_FX90_MS_SIZE	0x40011EA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX90_MS_ATT0	0x40011EB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX90_MS_ATT1	0x40011EB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX90_MS_ATT2	0x40011EB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX90_MS_ATT3	0x40011EBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX91_SL_ADDR	0x40011EC0	Slave region, base address
PERI_MS_PPU_FX91_SL_SIZE	0x40011EC4	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX91_SL_ATT0	0x40011ED0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX91_SL_ATT1	0x40011ED4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX91_SL_ATT2	0x40011ED8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX91_SL_ATT3	0x40011EDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX91_MS_ADDR	0x40011EE0	Master region, base address
PERI_MS_PPU_FX91_MS_SIZE	0x40011EE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX91_MS_ATT0	0x40011EF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX91_MS_ATT1	0x40011EF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX91_MS_ATT2	0x40011EF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX91_MS_ATT3	0x40011EFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX92_SL_ADDR	0x40011F00	Slave region, base address
PERI_MS_PPU_FX92_SL_SIZE	0x40011F04	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX92_SL_ATT0	0x40011F10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX92_SL_ATT1	0x40011F14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX92_SL_ATT2	0x40011F18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX92_SL_ATT3	0x40011F1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX92_MS_ADDR	0x40011F20	Master region, base address
PERI_MS_PPU_FX92_MS_SIZE	0x40011F24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX92_MS_ATT0	0x40011F30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX92_MS_ATT1	0x40011F34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX92_MS_ATT2	0x40011F38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX92_MS_ATT3	0x40011F3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX93_SL_ADDR	0x40011F40	Slave region, base address
PERI_MS_PPU_FX93_SL_SIZE	0x40011F44	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX93_SL_ATT0	0x40011F50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX93_SL_ATT1	0x40011F54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX93_SL_ATT2	0x40011F58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX93_SL_ATT3	0x40011F5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX93_MS_ADDR	0x40011F60	Master region, base address
PERI_MS_PPU_FX93_MS_SIZE	0x40011F64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX93_MS_ATT0	0x40011F70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX93_MS_ATT1	0x40011F74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX93_MS_ATT2	0x40011F78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX93_MS_ATT3	0x40011F7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX94_SL_ADDR	0x40011F80	Slave region, base address
PERI_MS_PPU_FX94_SL_SIZE	0x40011F84	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX94_SL_ATT0	0x40011F90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX94_SL_ATT1	0x40011F94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX94_SL_ATT2	0x40011F98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX94_SL_ATT3	0x40011F9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX94_MS_ADDR	0x40011FA0	Master region, base address
PERI_MS_PPU_FX94_MS_SIZE	0x40011FA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX94_MS_ATT0	0x40011FB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX94_MS_ATT1	0x40011FB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX94_MS_ATT2	0x40011FB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX94_MS_ATT3	0x40011FBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX95_SL_ADDR	0x40011FC0	Slave region, base address
PERI_MS_PPU_FX95_SL_SIZE	0x40011FC4	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX95_SL_ATT0	0x40011FD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX95_SL_ATT1	0x40011FD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX95_SL_ATT2	0x40011FD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX95_SL_ATT3	0x40011FDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX95_MS_ADDR	0x40011FE0	Master region, base address
PERI_MS_PPU_FX95_MS_SIZE	0x40011FE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX95_MS_ATT0	0x40011FF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX95_MS_ATT1	0x40011FF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX95_MS_ATT2	0x40011FF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX95_MS_ATT3	0x40011FFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX96_SL_ADDR	0x40012000	Slave region, base address
PERI_MS_PPU_FX96_SL_SIZE	0x40012004	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX96_SL_ATT0	0x40012010	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX96_SL_ATT1	0x40012014	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX96_SL_ATT2	0x40012018	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX96_SL_ATT3	0x4001201C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX96_MS_ADDR	0x40012020	Master region, base address
PERI_MS_PPU_FX96_MS_SIZE	0x40012024	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX96_MS_ATT0	0x40012030	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX96_MS_ATT1	0x40012034	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX96_MS_ATT2	0x40012038	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX96_MS_ATT3	0x4001203C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX97_SL_ADDR	0x40012040	Slave region, base address
PERI_MS_PPU_FX97_SL_SIZE	0x40012044	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX97_SL_ATT0	0x40012050	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX97_SL_ATT1	0x40012054	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX97_SL_ATT2	0x40012058	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX97_SL_ATT3	0x4001205C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX97_MS_ADDR	0x40012060	Master region, base address
PERI_MS_PPU_FX97_MS_SIZE	0x40012064	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX97_MS_ATT0	0x40012070	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX97_MS_ATT1	0x40012074	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX97_MS_ATT2	0x40012078	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX97_MS_ATT3	0x4001207C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX98_SL_ADDR	0x40012080	Slave region, base address
PERI_MS_PPU_FX98_SL_SIZE	0x40012084	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX98_SL_ATT0	0x40012090	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX98_SL_ATT1	0x40012094	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX98_SL_ATT2	0x40012098	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX98_SL_ATT3	0x4001209C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX98_MS_ADDR	0x400120A0	Master region, base address
PERI_MS_PPU_FX98_MS_SIZE	0x400120A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX98_MS_ATT0	0x400120B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX98_MS_ATT1	0x400120B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX98_MS_ATT2	0x400120B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX98_MS_ATT3	0x400120BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX99_SL_ADDR	0x400120C0	Slave region, base address
PERI_MS_PPU_FX99_SL_SIZE	0x400120C4	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX99_SL_ATT0	0x400120D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX99_SL_ATT1	0x400120D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX99_SL_ATT2	0x400120D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX99_SL_ATT3	0x400120DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX99_MS_ADDR	0x400120E0	Master region, base address
PERI_MS_PPU_FX99_MS_SIZE	0x400120E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX99_MS_ATT0	0x400120F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX99_MS_ATT1	0x400120F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX99_MS_ATT2	0x400120F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX99_MS_ATT3	0x400120FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX100_SL_ADDR	0x40012100	Slave region, base address
PERI_MS_PPU_FX100_SL_SIZE	0x40012104	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX100_SL_ATT0	0x40012110	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX100_SL_ATT1	0x40012114	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX100_SL_ATT2	0x40012118	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX100_SL_ATT3	0x4001211C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX100_MS_ADDR	0x40012120	Master region, base address
PERI_MS_PPU_FX100_MS_SIZE	0x40012124	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX100_MS_ATT0	0x40012130	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX100_MS_ATT1	0x40012134	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX100_MS_ATT2	0x40012138	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX100_MS_ATT3	0x4001213C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX101_SL_ADDR	0x40012140	Slave region, base address
PERI_MS_PPU_FX101_SL_SIZE	0x40012144	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX101_SL_ATT0	0x40012150	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX101_SL_ATT1	0x40012154	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX101_SL_ATT2	0x40012158	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX101_SL_ATT3	0x4001215C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX101_MS_ADDR	0x40012160	Master region, base address
PERI_MS_PPU_FX101_MS_SIZE	0x40012164	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX101_MS_ATT0	0x40012170	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX101_MS_ATT1	0x40012174	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX101_MS_ATT2	0x40012178	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX101_MS_ATT3	0x4001217C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX102_SL_ADDR	0x40012180	Slave region, base address
PERI_MS_PPU_FX102_SL_SIZE	0x40012184	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX102_SL_ATT0	0x40012190	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX102_SL_ATT1	0x40012194	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX102_SL_ATT2	0x40012198	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX102_SL_ATT3	0x4001219C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX102_MS_ADDR	0x400121A0	Master region, base address
PERI_MS_PPU_FX102_MS_SIZE	0x400121A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX102_MS_ATT0	0x400121B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX102_MS_ATT1	0x400121B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX102_MS_ATT2	0x400121B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX102_MS_ATT3	0x400121BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX103_SL_ADDR	0x400121C0	Slave region, base address
PERI_MS_PPU_FX103_SL_SIZE	0x400121C4	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX103_SL_ATT0	0x400121D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX103_SL_ATT1	0x400121D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX103_SL_ATT2	0x400121D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX103_SL_ATT3	0x400121DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX103_MS_ADDR	0x400121E0	Master region, base address
PERI_MS_PPU_FX103_MS_SIZE	0x400121E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX103_MS_ATT0	0x400121F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX103_MS_ATT1	0x400121F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX103_MS_ATT2	0x400121F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX103_MS_ATT3	0x400121FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX104_SL_ADDR	0x40012200	Slave region, base address
PERI_MS_PPU_FX104_SL_SIZE	0x40012204	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX104_SL_ATT0	0x40012210	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX104_SL_ATT1	0x40012214	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX104_SL_ATT2	0x40012218	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX104_SL_ATT3	0x4001221C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX104_MS_ADDR	0x40012220	Master region, base address
PERI_MS_PPU_FX104_MS_SIZE	0x40012224	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX104_MS_ATT0	0x40012230	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX104_MS_ATT1	0x40012234	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX104_MS_ATT2	0x40012238	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX104_MS_ATT3	0x4001223C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX105_SL_ADDR	0x40012240	Slave region, base address
PERI_MS_PPU_FX105_SL_SIZE	0x40012244	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX105_SL_ATT0	0x40012250	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX105_SL_ATT1	0x40012254	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX105_SL_ATT2	0x40012258	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX105_SL_ATT3	0x4001225C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX105_MS_ADDR	0x40012260	Master region, base address
PERI_MS_PPU_FX105_MS_SIZE	0x40012264	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX105_MS_ATT0	0x40012270	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX105_MS_ATT1	0x40012274	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX105_MS_ATT2	0x40012278	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX105_MS_ATT3	0x4001227C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX106_SL_ADDR	0x40012280	Slave region, base address
PERI_MS_PPU_FX106_SL_SIZE	0x40012284	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX106_SL_ATT0	0x40012290	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX106_SL_ATT1	0x40012294	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX106_SL_ATT2	0x40012298	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX106_SL_ATT3	0x4001229C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX106_MS_ADDR	0x400122A0	Master region, base address
PERI_MS_PPU_FX106_MS_SIZE	0x400122A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX106_MS_ATT0	0x400122B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX106_MS_ATT1	0x400122B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX106_MS_ATT2	0x400122B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX106_MS_ATT3	0x400122BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX107_SL_ADDR	0x400122C0	Slave region, base address
PERI_MS_PPU_FX107_SL_SIZE	0x400122C4	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX107_SL_ATT0	0x400122D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX107_SL_ATT1	0x400122D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX107_SL_ATT2	0x400122D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX107_SL_ATT3	0x400122DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX107_MS_ADDR	0x400122E0	Master region, base address
PERI_MS_PPU_FX107_MS_SIZE	0x400122E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX107_MS_ATT0	0x400122F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX107_MS_ATT1	0x400122F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX107_MS_ATT2	0x400122F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX107_MS_ATT3	0x400122FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX108_SL_ADDR	0x40012300	Slave region, base address
PERI_MS_PPU_FX108_SL_SIZE	0x40012304	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX108_SL_ATT0	0x40012310	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX108_SL_ATT1	0x40012314	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX108_SL_ATT2	0x40012318	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX108_SL_ATT3	0x4001231C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX108_MS_ADDR	0x40012320	Master region, base address
PERI_MS_PPU_FX108_MS_SIZE	0x40012324	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX108_MS_ATT0	0x40012330	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX108_MS_ATT1	0x40012334	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX108_MS_ATT2	0x40012338	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX108_MS_ATT3	0x4001233C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX109_SL_ADDR	0x40012340	Slave region, base address
PERI_MS_PPU_FX109_SL_SIZE	0x40012344	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX109_SL_ATT0	0x40012350	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX109_SL_ATT1	0x40012354	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX109_SL_ATT2	0x40012358	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX109_SL_ATT3	0x4001235C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX109_MS_ADDR	0x40012360	Master region, base address
PERI_MS_PPU_FX109_MS_SIZE	0x40012364	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX109_MS_ATT0	0x40012370	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX109_MS_ATT1	0x40012374	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX109_MS_ATT2	0x40012378	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX109_MS_ATT3	0x4001237C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX110_SL_ADDR	0x40012380	Slave region, base address
PERI_MS_PPU_FX110_SL_SIZE	0x40012384	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX110_SL_ATT0	0x40012390	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX110_SL_ATT1	0x40012394	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX110_SL_ATT2	0x40012398	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX110_SL_ATT3	0x4001239C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX110_MS_ADDR	0x400123A0	Master region, base address
PERI_MS_PPU_FX110_MS_SIZE	0x400123A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX110_MS_ATT0	0x400123B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX110_MS_ATT1	0x400123B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX110_MS_ATT2	0x400123B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX110_MS_ATT3	0x400123BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX111_SL_ADDR	0x400123C0	Slave region, base address
PERI_MS_PPU_FX111_SL_SIZE	0x400123C4	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX111_SL_ATT0	0x400123D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX111_SL_ATT1	0x400123D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX111_SL_ATT2	0x400123D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX111_SL_ATT3	0x400123DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX111_MS_ADDR	0x400123E0	Master region, base address
PERI_MS_PPU_FX111_MS_SIZE	0x400123E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX111_MS_ATT0	0x400123F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX111_MS_ATT1	0x400123F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX111_MS_ATT2	0x400123F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX111_MS_ATT3	0x400123FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX112_SL_ADDR	0x40012400	Slave region, base address
PERI_MS_PPU_FX112_SL_SIZE	0x40012404	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX112_SL_ATT0	0x40012410	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX112_SL_ATT1	0x40012414	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX112_SL_ATT2	0x40012418	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX112_SL_ATT3	0x4001241C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX112_MS_ADDR	0x40012420	Master region, base address
PERI_MS_PPU_FX112_MS_SIZE	0x40012424	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX112_MS_ATT0	0x40012430	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX112_MS_ATT1	0x40012434	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX112_MS_ATT2	0x40012438	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX112_MS_ATT3	0x4001243C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX113_SL_ADDR	0x40012440	Slave region, base address
PERI_MS_PPU_FX113_SL_SIZE	0x40012444	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX113_SL_ATT0	0x40012450	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX113_SL_ATT1	0x40012454	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX113_SL_ATT2	0x40012458	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX113_SL_ATT3	0x4001245C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX113_MS_ADDR	0x40012460	Master region, base address
PERI_MS_PPU_FX113_MS_SIZE	0x40012464	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX113_MS_ATT0	0x40012470	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX113_MS_ATT1	0x40012474	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX113_MS_ATT2	0x40012478	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX113_MS_ATT3	0x4001247C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX114_SL_ADDR	0x40012480	Slave region, base address
PERI_MS_PPU_FX114_SL_SIZE	0x40012484	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX114_SL_ATT0	0x40012490	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX114_SL_ATT1	0x40012494	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX114_SL_ATT2	0x40012498	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX114_SL_ATT3	0x4001249C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX114_MS_ADDR	0x400124A0	Master region, base address
PERI_MS_PPU_FX114_MS_SIZE	0x400124A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX114_MS_ATT0	0x400124B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX114_MS_ATT1	0x400124B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX114_MS_ATT2	0x400124B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX114_MS_ATT3	0x400124BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX115_SL_ADDR	0x400124C0	Slave region, base address
PERI_MS_PPU_FX115_SL_SIZE	0x400124C4	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX115_SL_ATT0	0x400124D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX115_SL_ATT1	0x400124D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX115_SL_ATT2	0x400124D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX115_SL_ATT3	0x400124DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX115_MS_ADDR	0x400124E0	Master region, base address
PERI_MS_PPU_FX115_MS_SIZE	0x400124E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX115_MS_ATT0	0x400124F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX115_MS_ATT1	0x400124F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX115_MS_ATT2	0x400124F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX115_MS_ATT3	0x400124FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX116_SL_ADDR	0x40012500	Slave region, base address
PERI_MS_PPU_FX116_SL_SIZE	0x40012504	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX116_SL_ATT0	0x40012510	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX116_SL_ATT1	0x40012514	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX116_SL_ATT2	0x40012518	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX116_SL_ATT3	0x4001251C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX116_MS_ADDR	0x40012520	Master region, base address
PERI_MS_PPU_FX116_MS_SIZE	0x40012524	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX116_MS_ATT0	0x40012530	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX116_MS_ATT1	0x40012534	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX116_MS_ATT2	0x40012538	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX116_MS_ATT3	0x4001253C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX117_SL_ADDR	0x40012540	Slave region, base address
PERI_MS_PPU_FX117_SL_SIZE	0x40012544	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX117_SL_ATT0	0x40012550	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX117_SL_ATT1	0x40012554	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX117_SL_ATT2	0x40012558	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX117_SL_ATT3	0x4001255C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX117_MS_ADDR	0x40012560	Master region, base address
PERI_MS_PPU_FX117_MS_SIZE	0x40012564	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX117_MS_ATT0	0x40012570	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX117_MS_ATT1	0x40012574	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX117_MS_ATT2	0x40012578	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX117_MS_ATT3	0x4001257C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX118_SL_ADDR	0x40012580	Slave region, base address
PERI_MS_PPU_FX118_SL_SIZE	0x40012584	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX118_SL_ATT0	0x40012590	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX118_SL_ATT1	0x40012594	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX118_SL_ATT2	0x40012598	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX118_SL_ATT3	0x4001259C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX118_MS_ADDR	0x400125A0	Master region, base address
PERI_MS_PPU_FX118_MS_SIZE	0x400125A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX118_MS_ATT0	0x400125B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX118_MS_ATT1	0x400125B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX118_MS_ATT2	0x400125B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX118_MS_ATT3	0x400125BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX119_SL_ADDR	0x400125C0	Slave region, base address
PERI_MS_PPU_FX119_SL_SIZE	0x400125C4	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX119_SL_ATT0	0x400125D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX119_SL_ATT1	0x400125D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX119_SL_ATT2	0x400125D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX119_SL_ATT3	0x400125DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX119_MS_ADDR	0x400125E0	Master region, base address
PERI_MS_PPU_FX119_MS_SIZE	0x400125E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX119_MS_ATT0	0x400125F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX119_MS_ATT1	0x400125F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX119_MS_ATT2	0x400125F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX119_MS_ATT3	0x400125FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX120_SL_ADDR	0x40012600	Slave region, base address
PERI_MS_PPU_FX120_SL_SIZE	0x40012604	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX120_SL_ATT0	0x40012610	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX120_SL_ATT1	0x40012614	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX120_SL_ATT2	0x40012618	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX120_SL_ATT3	0x4001261C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX120_MS_ADDR	0x40012620	Master region, base address
PERI_MS_PPU_FX120_MS_SIZE	0x40012624	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX120_MS_ATT0	0x40012630	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX120_MS_ATT1	0x40012634	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX120_MS_ATT2	0x40012638	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX120_MS_ATT3	0x4001263C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX121_SL_ADDR	0x40012640	Slave region, base address
PERI_MS_PPU_FX121_SL_SIZE	0x40012644	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX121_SL_ATT0	0x40012650	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX121_SL_ATT1	0x40012654	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX121_SL_ATT2	0x40012658	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX121_SL_ATT3	0x4001265C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX121_MS_ADDR	0x40012660	Master region, base address
PERI_MS_PPU_FX121_MS_SIZE	0x40012664	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX121_MS_ATT0	0x40012670	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX121_MS_ATT1	0x40012674	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX121_MS_ATT2	0x40012678	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX121_MS_ATT3	0x4001267C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX122_SL_ADDR	0x40012680	Slave region, base address
PERI_MS_PPU_FX122_SL_SIZE	0x40012684	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX122_SL_ATT0	0x40012690	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX122_SL_ATT1	0x40012694	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX122_SL_ATT2	0x40012698	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX122_SL_ATT3	0x4001269C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX122_MS_ADDR	0x400126A0	Master region, base address
PERI_MS_PPU_FX122_MS_SIZE	0x400126A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX122_MS_ATT0	0x400126B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX122_MS_ATT1	0x400126B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX122_MS_ATT2	0x400126B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX122_MS_ATT3	0x400126BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX123_SL_ADDR	0x400126C0	Slave region, base address
PERI_MS_PPU_FX123_SL_SIZE	0x400126C4	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX123_SL_ATT0	0x400126D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX123_SL_ATT1	0x400126D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX123_SL_ATT2	0x400126D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX123_SL_ATT3	0x400126DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX123_MS_ADDR	0x400126E0	Master region, base address
PERI_MS_PPU_FX123_MS_SIZE	0x400126E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX123_MS_ATT0	0x400126F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX123_MS_ATT1	0x400126F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX123_MS_ATT2	0x400126F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX123_MS_ATT3	0x400126FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX124_SL_ADDR	0x40012700	Slave region, base address
PERI_MS_PPU_FX124_SL_SIZE	0x40012704	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX124_SL_ATT0	0x40012710	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX124_SL_ATT1	0x40012714	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX124_SL_ATT2	0x40012718	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX124_SL_ATT3	0x4001271C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX124_MS_ADDR	0x40012720	Master region, base address
PERI_MS_PPU_FX124_MS_SIZE	0x40012724	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX124_MS_ATT0	0x40012730	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX124_MS_ATT1	0x40012734	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX124_MS_ATT2	0x40012738	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX124_MS_ATT3	0x4001273C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX125_SL_ADDR	0x40012740	Slave region, base address
PERI_MS_PPU_FX125_SL_SIZE	0x40012744	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX125_SL_ATT0	0x40012750	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX125_SL_ATT1	0x40012754	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX125_SL_ATT2	0x40012758	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX125_SL_ATT3	0x4001275C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX125_MS_ADDR	0x40012760	Master region, base address
PERI_MS_PPU_FX125_MS_SIZE	0x40012764	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX125_MS_ATT0	0x40012770	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX125_MS_ATT1	0x40012774	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX125_MS_ATT2	0x40012778	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX125_MS_ATT3	0x4001277C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX126_SL_ADDR	0x40012780	Slave region, base address
PERI_MS_PPU_FX126_SL_SIZE	0x40012784	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX126_SL_ATT0	0x40012790	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX126_SL_ATT1	0x40012794	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX126_SL_ATT2	0x40012798	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX126_SL_ATT3	0x4001279C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX126_MS_ADDR	0x400127A0	Master region, base address
PERI_MS_PPU_FX126_MS_SIZE	0x400127A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX126_MS_ATT0	0x400127B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX126_MS_ATT1	0x400127B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX126_MS_ATT2	0x400127B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX126_MS_ATT3	0x400127BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX127_SL_ADDR	0x400127C0	Slave region, base address
PERI_MS_PPU_FX127_SL_SIZE	0x400127C4	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX127_SL_ATT0	0x400127D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX127_SL_ATT1	0x400127D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX127_SL_ATT2	0x400127D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX127_SL_ATT3	0x400127DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX127_MS_ADDR	0x400127E0	Master region, base address
PERI_MS_PPU_FX127_MS_SIZE	0x400127E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX127_MS_ATT0	0x400127F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX127_MS_ATT1	0x400127F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX127_MS_ATT2	0x400127F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX127_MS_ATT3	0x400127FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX128_SL_ADDR	0x40012800	Slave region, base address
PERI_MS_PPU_FX128_SL_SIZE	0x40012804	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX128_SL_ATT0	0x40012810	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX128_SL_ATT1	0x40012814	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX128_SL_ATT2	0x40012818	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX128_SL_ATT3	0x4001281C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX128_MS_ADDR	0x40012820	Master region, base address
PERI_MS_PPU_FX128_MS_SIZE	0x40012824	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX128_MS_ATT0	0x40012830	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX128_MS_ATT1	0x40012834	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX128_MS_ATT2	0x40012838	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX128_MS_ATT3	0x4001283C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX129_SL_ADDR	0x40012840	Slave region, base address
PERI_MS_PPU_FX129_SL_SIZE	0x40012844	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX129_SL_ATT0	0x40012850	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX129_SL_ATT1	0x40012854	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX129_SL_ATT2	0x40012858	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX129_SL_ATT3	0x4001285C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX129_MS_ADDR	0x40012860	Master region, base address
PERI_MS_PPU_FX129_MS_SIZE	0x40012864	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX129_MS_ATT0	0x40012870	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX129_MS_ATT1	0x40012874	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX129_MS_ATT2	0x40012878	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX129_MS_ATT3	0x4001287C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX130_SL_ADDR	0x40012880	Slave region, base address
PERI_MS_PPU_FX130_SL_SIZE	0x40012884	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX130_SL_ATT0	0x40012890	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX130_SL_ATT1	0x40012894	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX130_SL_ATT2	0x40012898	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX130_SL_ATT3	0x4001289C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX130_MS_ADDR	0x400128A0	Master region, base address
PERI_MS_PPU_FX130_MS_SIZE	0x400128A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX130_MS_ATT0	0x400128B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX130_MS_ATT1	0x400128B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX130_MS_ATT2	0x400128B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX130_MS_ATT3	0x400128BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX131_SL_ADDR	0x400128C0	Slave region, base address
PERI_MS_PPU_FX131_SL_SIZE	0x400128C4	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX131_SL_ATT0	0x400128D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX131_SL_ATT1	0x400128D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX131_SL_ATT2	0x400128D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX131_SL_ATT3	0x400128DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX131_MS_ADDR	0x400128E0	Master region, base address
PERI_MS_PPU_FX131_MS_SIZE	0x400128E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX131_MS_ATT0	0x400128F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX131_MS_ATT1	0x400128F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX131_MS_ATT2	0x400128F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX131_MS_ATT3	0x400128FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX132_SL_ADDR	0x40012900	Slave region, base address
PERI_MS_PPU_FX132_SL_SIZE	0x40012904	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX132_SL_ATT0	0x40012910	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX132_SL_ATT1	0x40012914	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX132_SL_ATT2	0x40012918	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX132_SL_ATT3	0x4001291C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX132_MS_ADDR	0x40012920	Master region, base address
PERI_MS_PPU_FX132_MS_SIZE	0x40012924	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX132_MS_ATT0	0x40012930	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX132_MS_ATT1	0x40012934	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX132_MS_ATT2	0x40012938	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX132_MS_ATT3	0x4001293C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX133_SL_ADDR	0x40012940	Slave region, base address
PERI_MS_PPU_FX133_SL_SIZE	0x40012944	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX133_SL_ATT0	0x40012950	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX133_SL_ATT1	0x40012954	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX133_SL_ATT2	0x40012958	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX133_SL_ATT3	0x4001295C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX133_MS_ADDR	0x40012960	Master region, base address
PERI_MS_PPU_FX133_MS_SIZE	0x40012964	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX133_MS_ATT0	0x40012970	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX133_MS_ATT1	0x40012974	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX133_MS_ATT2	0x40012978	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX133_MS_ATT3	0x4001297C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX134_SL_ADDR	0x40012980	Slave region, base address
PERI_MS_PPU_FX134_SL_SIZE	0x40012984	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX134_SL_ATT0	0x40012990	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX134_SL_ATT1	0x40012994	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX134_SL_ATT2	0x40012998	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX134_SL_ATT3	0x4001299C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX134_MS_ADDR	0x400129A0	Master region, base address
PERI_MS_PPU_FX134_MS_SIZE	0x400129A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX134_MS_ATT0	0x400129B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX134_MS_ATT1	0x400129B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX134_MS_ATT2	0x400129B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX134_MS_ATT3	0x400129BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX135_SL_ADDR	0x400129C0	Slave region, base address
PERI_MS_PPU_FX135_SL_SIZE	0x400129C4	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX135_SL_ATT0	0x400129D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX135_SL_ATT1	0x400129D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX135_SL_ATT2	0x400129D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX135_SL_ATT3	0x400129DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX135_MS_ADDR	0x400129E0	Master region, base address
PERI_MS_PPU_FX135_MS_SIZE	0x400129E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX135_MS_ATT0	0x400129F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX135_MS_ATT1	0x400129F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX135_MS_ATT2	0x400129F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX135_MS_ATT3	0x400129FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX136_SL_ADDR	0x40012A00	Slave region, base address
PERI_MS_PPU_FX136_SL_SIZE	0x40012A04	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX136_SL_ATT0	0x40012A10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX136_SL_ATT1	0x40012A14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX136_SL_ATT2	0x40012A18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX136_SL_ATT3	0x40012A1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX136_MS_ADDR	0x40012A20	Master region, base address
PERI_MS_PPU_FX136_MS_SIZE	0x40012A24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX136_MS_ATT0	0x40012A30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX136_MS_ATT1	0x40012A34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX136_MS_ATT2	0x40012A38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX136_MS_ATT3	0x40012A3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX137_SL_ADDR	0x40012A40	Slave region, base address
PERI_MS_PPU_FX137_SL_SIZE	0x40012A44	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX137_SL_ATT0	0x40012A50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX137_SL_ATT1	0x40012A54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX137_SL_ATT2	0x40012A58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX137_SL_ATT3	0x40012A5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX137_MS_ADDR	0x40012A60	Master region, base address
PERI_MS_PPU_FX137_MS_SIZE	0x40012A64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX137_MS_ATT0	0x40012A70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX137_MS_ATT1	0x40012A74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX137_MS_ATT2	0x40012A78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX137_MS_ATT3	0x40012A7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX138_SL_ADDR	0x40012A80	Slave region, base address
PERI_MS_PPU_FX138_SL_SIZE	0x40012A84	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX138_SL_ATT0	0x40012A90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX138_SL_ATT1	0x40012A94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX138_SL_ATT2	0x40012A98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX138_SL_ATT3	0x40012A9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX138_MS_ADDR	0x40012AA0	Master region, base address
PERI_MS_PPU_FX138_MS_SIZE	0x40012AA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX138_MS_ATT0	0x40012AB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX138_MS_ATT1	0x40012AB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX138_MS_ATT2	0x40012AB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX138_MS_ATT3	0x40012ABC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX139_SL_ADDR	0x40012AC0	Slave region, base address
PERI_MS_PPU_FX139_SL_SIZE	0x40012AC4	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX139_SL_ATT0	0x40012AD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX139_SL_ATT1	0x40012AD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX139_SL_ATT2	0x40012AD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX139_SL_ATT3	0x40012ADC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX139_MS_ADDR	0x40012AE0	Master region, base address
PERI_MS_PPU_FX139_MS_SIZE	0x40012AE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX139_MS_ATT0	0x40012AF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX139_MS_ATT1	0x40012AF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX139_MS_ATT2	0x40012AF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX139_MS_ATT3	0x40012AFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX140_SL_ADDR	0x40012B00	Slave region, base address
PERI_MS_PPU_FX140_SL_SIZE	0x40012B04	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX140_SL_ATT0	0x40012B10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX140_SL_ATT1	0x40012B14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX140_SL_ATT2	0x40012B18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX140_SL_ATT3	0x40012B1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX140_MS_ADDR	0x40012B20	Master region, base address
PERI_MS_PPU_FX140_MS_SIZE	0x40012B24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX140_MS_ATT0	0x40012B30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX140_MS_ATT1	0x40012B34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX140_MS_ATT2	0x40012B38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX140_MS_ATT3	0x40012B3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX141_SL_ADDR	0x40012B40	Slave region, base address
PERI_MS_PPU_FX141_SL_SIZE	0x40012B44	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX141_SL_ATT0	0x40012B50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX141_SL_ATT1	0x40012B54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX141_SL_ATT2	0x40012B58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX141_SL_ATT3	0x40012B5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX141_MS_ADDR	0x40012B60	Master region, base address
PERI_MS_PPU_FX141_MS_SIZE	0x40012B64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX141_MS_ATT0	0x40012B70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX141_MS_ATT1	0x40012B74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX141_MS_ATT2	0x40012B78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX141_MS_ATT3	0x40012B7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX142_SL_ADDR	0x40012B80	Slave region, base address
PERI_MS_PPU_FX142_SL_SIZE	0x40012B84	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX142_SL_ATT0	0x40012B90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX142_SL_ATT1	0x40012B94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX142_SL_ATT2	0x40012B98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX142_SL_ATT3	0x40012B9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX142_MS_ADDR	0x40012BA0	Master region, base address
PERI_MS_PPU_FX142_MS_SIZE	0x40012BA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX142_MS_ATT0	0x40012BB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX142_MS_ATT1	0x40012BB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX142_MS_ATT2	0x40012BB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX142_MS_ATT3	0x40012BBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX143_SL_ADDR	0x40012BC0	Slave region, base address
PERI_MS_PPU_FX143_SL_SIZE	0x40012BC4	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX143_SL_ATT0	0x40012BD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX143_SL_ATT1	0x40012BD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX143_SL_ATT2	0x40012BD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX143_SL_ATT3	0x40012BDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX143_MS_ADDR	0x40012BE0	Master region, base address
PERI_MS_PPU_FX143_MS_SIZE	0x40012BE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX143_MS_ATT0	0x40012BF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX143_MS_ATT1	0x40012BF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX143_MS_ATT2	0x40012BF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX143_MS_ATT3	0x40012BFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX144_SL_ADDR	0x40012C00	Slave region, base address
PERI_MS_PPU_FX144_SL_SIZE	0x40012C04	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX144_SL_ATT0	0x40012C10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX144_SL_ATT1	0x40012C14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX144_SL_ATT2	0x40012C18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX144_SL_ATT3	0x40012C1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX144_MS_ADDR	0x40012C20	Master region, base address
PERI_MS_PPU_FX144_MS_SIZE	0x40012C24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX144_MS_ATT0	0x40012C30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX144_MS_ATT1	0x40012C34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX144_MS_ATT2	0x40012C38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX144_MS_ATT3	0x40012C3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX145_SL_ADDR	0x40012C40	Slave region, base address
PERI_MS_PPU_FX145_SL_SIZE	0x40012C44	Slave region, size. See PERI_MS_PPU_FX39_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX145_SL_ATT0	0x40012C50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX145_SL_ATT1	0x40012C54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX145_SL_ATT2	0x40012C58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX145_SL_ATT3	0x40012C5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX145_MS_ADDR	0x40012C60	Master region, base address
PERI_MS_PPU_FX145_MS_SIZE	0x40012C64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX145_MS_ATT0	0x40012C70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX145_MS_ATT1	0x40012C74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX145_MS_ATT2	0x40012C78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX145_MS_ATT3	0x40012C7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX146_SL_ADDR	0x40012C80	Slave region, base address
PERI_MS_PPU_FX146_SL_SIZE	0x40012C84	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX146_SL_ATT0	0x40012C90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX146_SL_ATT1	0x40012C94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX146_SL_ATT2	0x40012C98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX146_SL_ATT3	0x40012C9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX146_MS_ADDR	0x40012CA0	Master region, base address
PERI_MS_PPU_FX146_MS_SIZE	0x40012CA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX146_MS_ATT0	0x40012CB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX146_MS_ATT1	0x40012CB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX146_MS_ATT2	0x40012CB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX146_MS_ATT3	0x40012CBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX147_SL_ADDR	0x40012CC0	Slave region, base address
PERI_MS_PPU_FX147_SL_SIZE	0x40012CC4	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX147_SL_ATT0	0x40012CD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX147_SL_ATT1	0x40012CD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX147_SL_ATT2	0x40012CD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX147_SL_ATT3	0x40012CDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX147_MS_ADDR	0x40012CE0	Master region, base address
PERI_MS_PPU_FX147_MS_SIZE	0x40012CE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX147_MS_ATT0	0x40012CF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX147_MS_ATT1	0x40012CF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX147_MS_ATT2	0x40012CF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX147_MS_ATT3	0x40012CFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX148_SL_ADDR	0x40012D00	Slave region, base address
PERI_MS_PPU_FX148_SL_SIZE	0x40012D04	Slave region, size. See PERI_MS_PPU_FX62_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX148_SL_ATT0	0x40012D10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX148_SL_ATT1	0x40012D14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX148_SL_ATT2	0x40012D18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX148_SL_ATT3	0x40012D1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX148_MS_ADDR	0x40012D20	Master region, base address
PERI_MS_PPU_FX148_MS_SIZE	0x40012D24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX148_MS_ATT0	0x40012D30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX148_MS_ATT1	0x40012D34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX148_MS_ATT2	0x40012D38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX148_MS_ATT3	0x40012D3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX149_SL_ADDR	0x40012D40	Slave region, base address
PERI_MS_PPU_FX149_SL_SIZE	0x40012D44	Slave region, size. See PERI_MS_PPU_FX18_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX149_SL_ATT0	0x40012D50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX149_SL_ATT1	0x40012D54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX149_SL_ATT2	0x40012D58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX149_SL_ATT3	0x40012D5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX149_MS_ADDR	0x40012D60	Master region, base address
PERI_MS_PPU_FX149_MS_SIZE	0x40012D64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX149_MS_ATT0	0x40012D70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX149_MS_ATT1	0x40012D74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX149_MS_ATT2	0x40012D78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX149_MS_ATT3	0x40012D7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX150_SL_ADDR	0x40012D80	Slave region, base address
PERI_MS_PPU_FX150_SL_SIZE	0x40012D84	Slave region, size. See PERI_MS_PPU_FX59_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX150_SL_ATT0	0x40012D90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX150_SL_ATT1	0x40012D94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX150_SL_ATT2	0x40012D98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX150_SL_ATT3	0x40012D9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX150_MS_ADDR	0x40012DA0	Master region, base address
PERI_MS_PPU_FX150_MS_SIZE	0x40012DA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX150_MS_ATT0	0x40012DB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX150_MS_ATT1	0x40012DB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX150_MS_ATT2	0x40012DB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX150_MS_ATT3	0x40012DBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX151_SL_ADDR	0x40012DC0	Slave region, base address
PERI_MS_PPU_FX151_SL_SIZE	0x40012DC4	Slave region, size. See PERI_MS_PPU_FX59_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX151_SL_ATT0	0x40012DD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX151_SL_ATT1	0x40012DD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX151_SL_ATT2	0x40012DD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX151_SL_ATT3	0x40012DDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX151_MS_ADDR	0x40012DE0	Master region, base address
PERI_MS_PPU_FX151_MS_SIZE	0x40012DE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX151_MS_ATT0	0x40012DF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX151_MS_ATT1	0x40012DF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX151_MS_ATT2	0x40012DF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX151_MS_ATT3	0x40012DFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX152_SL_ADDR	0x40012E00	Slave region, base address
PERI_MS_PPU_FX152_SL_SIZE	0x40012E04	Slave region, size. See PERI_MS_PPU_FX59_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX152_SL_ATT0	0x40012E10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX152_SL_ATT1	0x40012E14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX152_SL_ATT2	0x40012E18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX152_SL_ATT3	0x40012E1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX152_MS_ADDR	0x40012E20	Master region, base address
PERI_MS_PPU_FX152_MS_SIZE	0x40012E24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX152_MS_ATT0	0x40012E30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX152_MS_ATT1	0x40012E34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX152_MS_ATT2	0x40012E38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX152_MS_ATT3	0x40012E3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX153_SL_ADDR	0x40012E40	Slave region, base address
PERI_MS_PPU_FX153_SL_SIZE	0x40012E44	Slave region, size. See PERI_MS_PPU_FX59_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX153_SL_ATT0	0x40012E50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX153_SL_ATT1	0x40012E54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX153_SL_ATT2	0x40012E58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX153_SL_ATT3	0x40012E5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX153_MS_ADDR	0x40012E60	Master region, base address
PERI_MS_PPU_FX153_MS_SIZE	0x40012E64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX153_MS_ATT0	0x40012E70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX153_MS_ATT1	0x40012E74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX153_MS_ATT2	0x40012E78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX153_MS_ATT3	0x40012E7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX154_SL_ADDR	0x40012E80	Slave region, base address
PERI_MS_PPU_FX154_SL_SIZE	0x40012E84	Slave region, size. See PERI_MS_PPU_FX59_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX154_SL_ATT0	0x40012E90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX154_SL_ATT1	0x40012E94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX154_SL_ATT2	0x40012E98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX154_SL_ATT3	0x40012E9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX154_MS_ADDR	0x40012EA0	Master region, base address
PERI_MS_PPU_FX154_MS_SIZE	0x40012EA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX154_MS_ATT0	0x40012EB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX154_MS_ATT1	0x40012EB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX154_MS_ATT2	0x40012EB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX154_MS_ATT3	0x40012EBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX155_SL_ADDR	0x40012EC0	Slave region, base address
PERI_MS_PPU_FX155_SL_SIZE	0x40012EC4	Slave region, size. See PERI_MS_PPU_FX59_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX155_SL_ATT0	0x40012ED0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX155_SL_ATT1	0x40012ED4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX155_SL_ATT2	0x40012ED8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX155_SL_ATT3	0x40012EDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX155_MS_ADDR	0x40012EE0	Master region, base address
PERI_MS_PPU_FX155_MS_SIZE	0x40012EE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX155_MS_ATT0	0x40012EF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX155_MS_ATT1	0x40012EF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX155_MS_ATT2	0x40012EF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX155_MS_ATT3	0x40012EFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX156_SL_ADDR	0x40012F00	Slave region, base address
PERI_MS_PPU_FX156_SL_SIZE	0x40012F04	Slave region, size. See PERI_MS_PPU_FX59_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX156_SL_ATT0	0x40012F10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX156_SL_ATT1	0x40012F14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX156_SL_ATT2	0x40012F18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX156_SL_ATT3	0x40012F1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX156_MS_ADDR	0x40012F20	Master region, base address
PERI_MS_PPU_FX156_MS_SIZE	0x40012F24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX156_MS_ATT0	0x40012F30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX156_MS_ATT1	0x40012F34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX156_MS_ATT2	0x40012F38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX156_MS_ATT3	0x40012F3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX157_SL_ADDR	0x40012F40	Slave region, base address
PERI_MS_PPU_FX157_SL_SIZE	0x40012F44	Slave region, size. See PERI_MS_PPU_FX59_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX157_SL_ATT0	0x40012F50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX157_SL_ATT1	0x40012F54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX157_SL_ATT2	0x40012F58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX157_SL_ATT3	0x40012F5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX157_MS_ADDR	0x40012F60	Master region, base address
PERI_MS_PPU_FX157_MS_SIZE	0x40012F64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX157_MS_ATT0	0x40012F70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX157_MS_ATT1	0x40012F74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX157_MS_ATT2	0x40012F78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX157_MS_ATT3	0x40012F7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX158_SL_ADDR	0x40012F80	Slave region, base address
PERI_MS_PPU_FX158_SL_SIZE	0x40012F84	Slave region, size. See PERI_MS_PPU_FX59_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX158_SL_ATT0	0x40012F90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX158_SL_ATT1	0x40012F94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX158_SL_ATT2	0x40012F98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX158_SL_ATT3	0x40012F9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX158_MS_ADDR	0x40012FA0	Master region, base address
PERI_MS_PPU_FX158_MS_SIZE	0x40012FA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX158_MS_ATT0	0x40012FB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX158_MS_ATT1	0x40012FB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX158_MS_ATT2	0x40012FB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX158_MS_ATT3	0x40012FBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX159_SL_ADDR	0x40012FC0	Slave region, base address
PERI_MS_PPU_FX159_SL_SIZE	0x40012FC4	Slave region, size. See PERI_MS_PPU_FX59_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX159_SL_ATT0	0x40012FD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX159_SL_ATT1	0x40012FD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX159_SL_ATT2	0x40012FD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX159_SL_ATT3	0x40012FDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX159_MS_ADDR	0x40012FE0	Master region, base address
PERI_MS_PPU_FX159_MS_SIZE	0x40012FE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX159_MS_ATT0	0x40012FF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX159_MS_ATT1	0x40012FF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX159_MS_ATT2	0x40012FF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX159_MS_ATT3	0x40012FFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX160_SL_ADDR	0x40013000	Slave region, base address
PERI_MS_PPU_FX160_SL_SIZE	0x40013004	Slave region, size. See PERI_MS_PPU_FX59_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX160_SL_ATT0	0x40013010	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX160_SL_ATT1	0x40013014	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX160_SL_ATT2	0x40013018	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX160_SL_ATT3	0x4001301C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX160_MS_ADDR	0x40013020	Master region, base address
PERI_MS_PPU_FX160_MS_SIZE	0x40013024	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX160_MS_ATT0	0x40013030	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX160_MS_ATT1	0x40013034	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX160_MS_ATT2	0x40013038	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX160_MS_ATT3	0x4001303C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX161_SL_ADDR	0x40013040	Slave region, base address
PERI_MS_PPU_FX161_SL_SIZE	0x40013044	Slave region, size. See PERI_MS_PPU_FX59_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX161_SL_ATT0	0x40013050	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX161_SL_ATT1	0x40013054	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX161_SL_ATT2	0x40013058	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX161_SL_ATT3	0x4001305C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX161_MS_ADDR	0x40013060	Master region, base address
PERI_MS_PPU_FX161_MS_SIZE	0x40013064	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX161_MS_ATT0	0x40013070	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX161_MS_ATT1	0x40013074	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX161_MS_ATT2	0x40013078	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX161_MS_ATT3	0x4001307C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX162_SL_ADDR	0x40013080	Slave region, base address
PERI_MS_PPU_FX162_SL_SIZE	0x40013084	Slave region, size. See PERI_MS_PPU_FX59_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX162_SL_ATT0	0x40013090	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX162_SL_ATT1	0x40013094	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX162_SL_ATT2	0x40013098	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX162_SL_ATT3	0x4001309C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX162_MS_ADDR	0x400130A0	Master region, base address
PERI_MS_PPU_FX162_MS_SIZE	0x400130A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX162_MS_ATT0	0x400130B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX162_MS_ATT1	0x400130B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX162_MS_ATT2	0x400130B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX162_MS_ATT3	0x400130BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX163_SL_ADDR	0x400130C0	Slave region, base address
PERI_MS_PPU_FX163_SL_SIZE	0x400130C4	Slave region, size. See PERI_MS_PPU_FX59_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX163_SL_ATT0	0x400130D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX163_SL_ATT1	0x400130D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX163_SL_ATT2	0x400130D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX163_SL_ATT3	0x400130DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX163_MS_ADDR	0x400130E0	Master region, base address
PERI_MS_PPU_FX163_MS_SIZE	0x400130E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX163_MS_ATT0	0x400130F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX163_MS_ATT1	0x400130F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX163_MS_ATT2	0x400130F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX163_MS_ATT3	0x400130FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX164_SL_ADDR	0x40013100	Slave region, base address
PERI_MS_PPU_FX164_SL_SIZE	0x40013104	Slave region, size. See PERI_MS_PPU_FX59_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX164_SL_ATT0	0x40013110	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX164_SL_ATT1	0x40013114	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX164_SL_ATT2	0x40013118	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX164_SL_ATT3	0x4001311C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX164_MS_ADDR	0x40013120	Master region, base address
PERI_MS_PPU_FX164_MS_SIZE	0x40013124	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX164_MS_ATT0	0x40013130	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX164_MS_ATT1	0x40013134	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX164_MS_ATT2	0x40013138	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX164_MS_ATT3	0x4001313C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX165_SL_ADDR	0x40013140	Slave region, base address
PERI_MS_PPU_FX165_SL_SIZE	0x40013144	Slave region, size. See PERI_MS_PPU_FX4_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX165_SL_ATT0	0x40013150	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX165_SL_ATT1	0x40013154	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX165_SL_ATT2	0x40013158	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX165_SL_ATT3	0x4001315C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX165_MS_ADDR	0x40013160	Master region, base address
PERI_MS_PPU_FX165_MS_SIZE	0x40013164	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX165_MS_ATT0	0x40013170	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX165_MS_ATT1	0x40013174	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX165_MS_ATT2	0x40013178	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX165_MS_ATT3	0x4001317C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX166_SL_ADDR	0x40013180	Slave region, base address
PERI_MS_PPU_FX166_SL_SIZE	0x40013184	Slave region, size. See PERI_MS_PPU_FX39_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX166_SL_ATT0	0x40013190	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX166_SL_ATT1	0x40013194	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX166_SL_ATT2	0x40013198	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX166_SL_ATT3	0x4001319C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX166_MS_ADDR	0x400131A0	Master region, base address
PERI_MS_PPU_FX166_MS_SIZE	0x400131A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX166_MS_ATT0	0x400131B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX166_MS_ATT1	0x400131B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX166_MS_ATT2	0x400131B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX166_MS_ATT3	0x400131BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX167_SL_ADDR	0x400131C0	Slave region, base address
PERI_MS_PPU_FX167_SL_SIZE	0x400131C4	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX167_SL_ATT0	0x400131D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX167_SL_ATT1	0x400131D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX167_SL_ATT2	0x400131D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX167_SL_ATT3	0x400131DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX167_MS_ADDR	0x400131E0	Master region, base address
PERI_MS_PPU_FX167_MS_SIZE	0x400131E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX167_MS_ATT0	0x400131F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX167_MS_ATT1	0x400131F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX167_MS_ATT2	0x400131F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX167_MS_ATT3	0x400131FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX168_SL_ADDR	0x40013200	Slave region, base address
PERI_MS_PPU_FX168_SL_SIZE	0x40013204	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX168_SL_ATT0	0x40013210	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX168_SL_ATT1	0x40013214	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX168_SL_ATT2	0x40013218	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX168_SL_ATT3	0x4001321C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX168_MS_ADDR	0x40013220	Master region, base address
PERI_MS_PPU_FX168_MS_SIZE	0x40013224	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX168_MS_ATT0	0x40013230	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX168_MS_ATT1	0x40013234	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX168_MS_ATT2	0x40013238	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX168_MS_ATT3	0x4001323C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX169_SL_ADDR	0x40013240	Slave region, base address
PERI_MS_PPU_FX169_SL_SIZE	0x40013244	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX169_SL_ATT0	0x40013250	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX169_SL_ATT1	0x40013254	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX169_SL_ATT2	0x40013258	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX169_SL_ATT3	0x4001325C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX169_MS_ADDR	0x40013260	Master region, base address
PERI_MS_PPU_FX169_MS_SIZE	0x40013264	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX169_MS_ATT0	0x40013270	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX169_MS_ATT1	0x40013274	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX169_MS_ATT2	0x40013278	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX169_MS_ATT3	0x4001327C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX170_SL_ADDR	0x40013280	Slave region, base address
PERI_MS_PPU_FX170_SL_SIZE	0x40013284	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX170_SL_ATT0	0x40013290	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX170_SL_ATT1	0x40013294	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX170_SL_ATT2	0x40013298	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX170_SL_ATT3	0x4001329C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX170_MS_ADDR	0x400132A0	Master region, base address
PERI_MS_PPU_FX170_MS_SIZE	0x400132A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX170_MS_ATT0	0x400132B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX170_MS_ATT1	0x400132B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX170_MS_ATT2	0x400132B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX170_MS_ATT3	0x400132BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX171_SL_ADDR	0x400132C0	Slave region, base address
PERI_MS_PPU_FX171_SL_SIZE	0x400132C4	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX171_SL_ATT0	0x400132D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX171_SL_ATT1	0x400132D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX171_SL_ATT2	0x400132D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX171_SL_ATT3	0x400132DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX171_MS_ADDR	0x400132E0	Master region, base address
PERI_MS_PPU_FX171_MS_SIZE	0x400132E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX171_MS_ATT0	0x400132F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX171_MS_ATT1	0x400132F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX171_MS_ATT2	0x400132F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX171_MS_ATT3	0x400132FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX172_SL_ADDR	0x40013300	Slave region, base address
PERI_MS_PPU_FX172_SL_SIZE	0x40013304	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX172_SL_ATT0	0x40013310	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX172_SL_ATT1	0x40013314	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX172_SL_ATT2	0x40013318	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX172_SL_ATT3	0x4001331C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX172_MS_ADDR	0x40013320	Master region, base address
PERI_MS_PPU_FX172_MS_SIZE	0x40013324	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX172_MS_ATT0	0x40013330	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX172_MS_ATT1	0x40013334	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX172_MS_ATT2	0x40013338	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX172_MS_ATT3	0x4001333C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX173_SL_ADDR	0x40013340	Slave region, base address
PERI_MS_PPU_FX173_SL_SIZE	0x40013344	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX173_SL_ATT0	0x40013350	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX173_SL_ATT1	0x40013354	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX173_SL_ATT2	0x40013358	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX173_SL_ATT3	0x4001335C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX173_MS_ADDR	0x40013360	Master region, base address
PERI_MS_PPU_FX173_MS_SIZE	0x40013364	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX173_MS_ATT0	0x40013370	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX173_MS_ATT1	0x40013374	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX173_MS_ATT2	0x40013378	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX173_MS_ATT3	0x4001337C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX174_SL_ADDR	0x40013380	Slave region, base address
PERI_MS_PPU_FX174_SL_SIZE	0x40013384	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX174_SL_ATT0	0x40013390	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX174_SL_ATT1	0x40013394	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX174_SL_ATT2	0x40013398	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX174_SL_ATT3	0x4001339C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX174_MS_ADDR	0x400133A0	Master region, base address
PERI_MS_PPU_FX174_MS_SIZE	0x400133A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX174_MS_ATT0	0x400133B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX174_MS_ATT1	0x400133B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX174_MS_ATT2	0x400133B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX174_MS_ATT3	0x400133BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX175_SL_ADDR	0x400133C0	Slave region, base address
PERI_MS_PPU_FX175_SL_SIZE	0x400133C4	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX175_SL_ATT0	0x400133D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX175_SL_ATT1	0x400133D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX175_SL_ATT2	0x400133D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX175_SL_ATT3	0x400133DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX175_MS_ADDR	0x400133E0	Master region, base address
PERI_MS_PPU_FX175_MS_SIZE	0x400133E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX175_MS_ATT0	0x400133F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX175_MS_ATT1	0x400133F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX175_MS_ATT2	0x400133F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX175_MS_ATT3	0x400133FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX176_SL_ADDR	0x40013400	Slave region, base address
PERI_MS_PPU_FX176_SL_SIZE	0x40013404	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX176_SL_ATT0	0x40013410	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX176_SL_ATT1	0x40013414	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX176_SL_ATT2	0x40013418	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX176_SL_ATT3	0x4001341C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX176_MS_ADDR	0x40013420	Master region, base address
PERI_MS_PPU_FX176_MS_SIZE	0x40013424	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX176_MS_ATT0	0x40013430	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX176_MS_ATT1	0x40013434	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX176_MS_ATT2	0x40013438	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX176_MS_ATT3	0x4001343C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX177_SL_ADDR	0x40013440	Slave region, base address
PERI_MS_PPU_FX177_SL_SIZE	0x40013444	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX177_SL_ATT0	0x40013450	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX177_SL_ATT1	0x40013454	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX177_SL_ATT2	0x40013458	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX177_SL_ATT3	0x4001345C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX177_MS_ADDR	0x40013460	Master region, base address
PERI_MS_PPU_FX177_MS_SIZE	0x40013464	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX177_MS_ATT0	0x40013470	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX177_MS_ATT1	0x40013474	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX177_MS_ATT2	0x40013478	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX177_MS_ATT3	0x4001347C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX178_SL_ADDR	0x40013480	Slave region, base address
PERI_MS_PPU_FX178_SL_SIZE	0x40013484	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX178_SL_ATT0	0x40013490	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX178_SL_ATT1	0x40013494	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX178_SL_ATT2	0x40013498	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX178_SL_ATT3	0x4001349C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX178_MS_ADDR	0x400134A0	Master region, base address
PERI_MS_PPU_FX178_MS_SIZE	0x400134A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX178_MS_ATT0	0x400134B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX178_MS_ATT1	0x400134B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX178_MS_ATT2	0x400134B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX178_MS_ATT3	0x400134BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX179_SL_ADDR	0x400134C0	Slave region, base address
PERI_MS_PPU_FX179_SL_SIZE	0x400134C4	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX179_SL_ATT0	0x400134D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX179_SL_ATT1	0x400134D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX179_SL_ATT2	0x400134D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX179_SL_ATT3	0x400134DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX179_MS_ADDR	0x400134E0	Master region, base address
PERI_MS_PPU_FX179_MS_SIZE	0x400134E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX179_MS_ATT0	0x400134F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX179_MS_ATT1	0x400134F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX179_MS_ATT2	0x400134F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX179_MS_ATT3	0x400134FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX180_SL_ADDR	0x40013500	Slave region, base address
PERI_MS_PPU_FX180_SL_SIZE	0x40013504	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX180_SL_ATT0	0x40013510	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX180_SL_ATT1	0x40013514	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX180_SL_ATT2	0x40013518	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX180_SL_ATT3	0x4001351C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX180_MS_ADDR	0x40013520	Master region, base address
PERI_MS_PPU_FX180_MS_SIZE	0x40013524	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX180_MS_ATT0	0x40013530	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX180_MS_ATT1	0x40013534	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX180_MS_ATT2	0x40013538	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX180_MS_ATT3	0x4001353C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX181_SL_ADDR	0x40013540	Slave region, base address
PERI_MS_PPU_FX181_SL_SIZE	0x40013544	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX181_SL_ATT0	0x40013550	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX181_SL_ATT1	0x40013554	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX181_SL_ATT2	0x40013558	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX181_SL_ATT3	0x4001355C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX181_MS_ADDR	0x40013560	Master region, base address
PERI_MS_PPU_FX181_MS_SIZE	0x40013564	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX181_MS_ATT0	0x40013570	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX181_MS_ATT1	0x40013574	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX181_MS_ATT2	0x40013578	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX181_MS_ATT3	0x4001357C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX182_SL_ADDR	0x40013580	Slave region, base address
PERI_MS_PPU_FX182_SL_SIZE	0x40013584	Slave region, size. See PERI_MS_PPU_FX39_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX182_SL_ATT0	0x40013590	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX182_SL_ATT1	0x40013594	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX182_SL_ATT2	0x40013598	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX182_SL_ATT3	0x4001359C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX182_MS_ADDR	0x400135A0	Master region, base address
PERI_MS_PPU_FX182_MS_SIZE	0x400135A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX182_MS_ATT0	0x400135B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX182_MS_ATT1	0x400135B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX182_MS_ATT2	0x400135B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX182_MS_ATT3	0x400135BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX183_SL_ADDR	0x400135C0	Slave region, base address
PERI_MS_PPU_FX183_SL_SIZE	0x400135C4	Slave region, size. See PERI_MS_PPU_FX39_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX183_SL_ATT0	0x400135D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX183_SL_ATT1	0x400135D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX183_SL_ATT2	0x400135D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX183_SL_ATT3	0x400135DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX183_MS_ADDR	0x400135E0	Master region, base address
PERI_MS_PPU_FX183_MS_SIZE	0x400135E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX183_MS_ATT0	0x400135F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX183_MS_ATT1	0x400135F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX183_MS_ATT2	0x400135F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX183_MS_ATT3	0x400135FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX184_SL_ADDR	0x40013600	Slave region, base address
PERI_MS_PPU_FX184_SL_SIZE	0x40013604	Slave region, size. See PERI_MS_PPU_FX39_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX184_SL_ATT0	0x40013610	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX184_SL_ATT1	0x40013614	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX184_SL_ATT2	0x40013618	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX184_SL_ATT3	0x4001361C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX184_MS_ADDR	0x40013620	Master region, base address
PERI_MS_PPU_FX184_MS_SIZE	0x40013624	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX184_MS_ATT0	0x40013630	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX184_MS_ATT1	0x40013634	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX184_MS_ATT2	0x40013638	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX184_MS_ATT3	0x4001363C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX185_SL_ADDR	0x40013640	Slave region, base address
PERI_MS_PPU_FX185_SL_SIZE	0x40013644	Slave region, size. See PERI_MS_PPU_FX39_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX185_SL_ATT0	0x40013650	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX185_SL_ATT1	0x40013654	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX185_SL_ATT2	0x40013658	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX185_SL_ATT3	0x4001365C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX185_MS_ADDR	0x40013660	Master region, base address
PERI_MS_PPU_FX185_MS_SIZE	0x40013664	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX185_MS_ATT0	0x40013670	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX185_MS_ATT1	0x40013674	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX185_MS_ATT2	0x40013678	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX185_MS_ATT3	0x4001367C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX186_SL_ADDR	0x40013680	Slave region, base address
PERI_MS_PPU_FX186_SL_SIZE	0x40013684	Slave region, size. See PERI_MS_PPU_FX59_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX186_SL_ATT0	0x40013690	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX186_SL_ATT1	0x40013694	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX186_SL_ATT2	0x40013698	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX186_SL_ATT3	0x4001369C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX186_MS_ADDR	0x400136A0	Master region, base address
PERI_MS_PPU_FX186_MS_SIZE	0x400136A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX186_MS_ATT0	0x400136B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX186_MS_ATT1	0x400136B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX186_MS_ATT2	0x400136B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX186_MS_ATT3	0x400136BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX187_SL_ADDR	0x400136C0	Slave region, base address
PERI_MS_PPU_FX187_SL_SIZE	0x400136C4	Slave region, size. See PERI_MS_PPU_FX39_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX187_SL_ATT0	0x400136D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX187_SL_ATT1	0x400136D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX187_SL_ATT2	0x400136D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX187_SL_ATT3	0x400136DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX187_MS_ADDR	0x400136E0	Master region, base address
PERI_MS_PPU_FX187_MS_SIZE	0x400136E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX187_MS_ATT0	0x400136F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX187_MS_ATT1	0x400136F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX187_MS_ATT2	0x400136F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX187_MS_ATT3	0x400136FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX188_SL_ADDR	0x40013700	Slave region, base address
PERI_MS_PPU_FX188_SL_SIZE	0x40013704	Slave region, size. See PERI_MS_PPU_FX39_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX188_SL_ATT0	0x40013710	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX188_SL_ATT1	0x40013714	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX188_SL_ATT2	0x40013718	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX188_SL_ATT3	0x4001371C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX188_MS_ADDR	0x40013720	Master region, base address
PERI_MS_PPU_FX188_MS_SIZE	0x40013724	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX188_MS_ATT0	0x40013730	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX188_MS_ATT1	0x40013734	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX188_MS_ATT2	0x40013738	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX188_MS_ATT3	0x4001373C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX189_SL_ADDR	0x40013740	Slave region, base address
PERI_MS_PPU_FX189_SL_SIZE	0x40013744	Slave region, size. See PERI_MS_PPU_FX39_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX189_SL_ATT0	0x40013750	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX189_SL_ATT1	0x40013754	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX189_SL_ATT2	0x40013758	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX189_SL_ATT3	0x4001375C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX189_MS_ADDR	0x40013760	Master region, base address
PERI_MS_PPU_FX189_MS_SIZE	0x40013764	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX189_MS_ATT0	0x40013770	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX189_MS_ATT1	0x40013774	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX189_MS_ATT2	0x40013778	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX189_MS_ATT3	0x4001377C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX190_SL_ADDR	0x40013780	Slave region, base address
PERI_MS_PPU_FX190_SL_SIZE	0x40013784	Slave region, size. See PERI_MS_PPU_FX39_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX190_SL_ATT0	0x40013790	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX190_SL_ATT1	0x40013794	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX190_SL_ATT2	0x40013798	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX190_SL_ATT3	0x4001379C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX190_MS_ADDR	0x400137A0	Master region, base address
PERI_MS_PPU_FX190_MS_SIZE	0x400137A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX190_MS_ATT0	0x400137B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX190_MS_ATT1	0x400137B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX190_MS_ATT2	0x400137B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX190_MS_ATT3	0x400137BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX191_SL_ADDR	0x400137C0	Slave region, base address
PERI_MS_PPU_FX191_SL_SIZE	0x400137C4	Slave region, size. See PERI_MS_PPU_FX39_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX191_SL_ATT0	0x400137D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX191_SL_ATT1	0x400137D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX191_SL_ATT2	0x400137D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX191_SL_ATT3	0x400137DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX191_MS_ADDR	0x400137E0	Master region, base address
PERI_MS_PPU_FX191_MS_SIZE	0x400137E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX191_MS_ATT0	0x400137F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX191_MS_ATT1	0x400137F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX191_MS_ATT2	0x400137F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX191_MS_ATT3	0x400137FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX192_SL_ADDR	0x40013800	Slave region, base address
PERI_MS_PPU_FX192_SL_SIZE	0x40013804	Slave region, size. See PERI_MS_PPU_FX39_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX192_SL_ATT0	0x40013810	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX192_SL_ATT1	0x40013814	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX192_SL_ATT2	0x40013818	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX192_SL_ATT3	0x4001381C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX192_MS_ADDR	0x40013820	Master region, base address
PERI_MS_PPU_FX192_MS_SIZE	0x40013824	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX192_MS_ATT0	0x40013830	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX192_MS_ATT1	0x40013834	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX192_MS_ATT2	0x40013838	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX192_MS_ATT3	0x4001383C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX193_SL_ADDR	0x40013840	Slave region, base address
PERI_MS_PPU_FX193_SL_SIZE	0x40013844	Slave region, size. See PERI_MS_PPU_FX39_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX193_SL_ATT0	0x40013850	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX193_SL_ATT1	0x40013854	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX193_SL_ATT2	0x40013858	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX193_SL_ATT3	0x4001385C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX193_MS_ADDR	0x40013860	Master region, base address
PERI_MS_PPU_FX193_MS_SIZE	0x40013864	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX193_MS_ATT0	0x40013870	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX193_MS_ATT1	0x40013874	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX193_MS_ATT2	0x40013878	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX193_MS_ATT3	0x4001387C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX194_SL_ADDR	0x40013880	Slave region, base address
PERI_MS_PPU_FX194_SL_SIZE	0x40013884	Slave region, size. See PERI_MS_PPU_FX39_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX194_SL_ATT0	0x40013890	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX194_SL_ATT1	0x40013894	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX194_SL_ATT2	0x40013898	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX194_SL_ATT3	0x4001389C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX194_MS_ADDR	0x400138A0	Master region, base address
PERI_MS_PPU_FX194_MS_SIZE	0x400138A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX194_MS_ATT0	0x400138B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX194_MS_ATT1	0x400138B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX194_MS_ATT2	0x400138B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX194_MS_ATT3	0x400138BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX195_SL_ADDR	0x400138C0	Slave region, base address
PERI_MS_PPU_FX195_SL_SIZE	0x400138C4	Slave region, size. See PERI_MS_PPU_FX59_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX195_SL_ATT0	0x400138D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX195_SL_ATT1	0x400138D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX195_SL_ATT2	0x400138D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX195_SL_ATT3	0x400138DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX195_MS_ADDR	0x400138E0	Master region, base address
PERI_MS_PPU_FX195_MS_SIZE	0x400138E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX195_MS_ATT0	0x400138F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX195_MS_ATT1	0x400138F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX195_MS_ATT2	0x400138F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX195_MS_ATT3	0x400138FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX196_SL_ADDR	0x40013900	Slave region, base address
PERI_MS_PPU_FX196_SL_SIZE	0x40013904	Slave region, size. See PERI_MS_PPU_FX59_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX196_SL_ATT0	0x40013910	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX196_SL_ATT1	0x40013914	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX196_SL_ATT2	0x40013918	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX196_SL_ATT3	0x4001391C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX196_MS_ADDR	0x40013920	Master region, base address
PERI_MS_PPU_FX196_MS_SIZE	0x40013924	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX196_MS_ATT0	0x40013930	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX196_MS_ATT1	0x40013934	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX196_MS_ATT2	0x40013938	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX196_MS_ATT3	0x4001393C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX197_SL_ADDR	0x40013940	Slave region, base address
PERI_MS_PPU_FX197_SL_SIZE	0x40013944	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX197_SL_ATT0	0x40013950	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX197_SL_ATT1	0x40013954	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX197_SL_ATT2	0x40013958	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX197_SL_ATT3	0x4001395C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX197_MS_ADDR	0x40013960	Master region, base address
PERI_MS_PPU_FX197_MS_SIZE	0x40013964	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX197_MS_ATT0	0x40013970	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX197_MS_ATT1	0x40013974	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX197_MS_ATT2	0x40013978	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX197_MS_ATT3	0x4001397C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX198_SL_ADDR	0x40013980	Slave region, base address
PERI_MS_PPU_FX198_SL_SIZE	0x40013984	Slave region, size. See PERI_MS_PPU_FX59_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX198_SL_ATT0	0x40013990	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX198_SL_ATT1	0x40013994	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX198_SL_ATT2	0x40013998	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX198_SL_ATT3	0x4001399C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX198_MS_ADDR	0x400139A0	Master region, base address
PERI_MS_PPU_FX198_MS_SIZE	0x400139A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX198_MS_ATT0	0x400139B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX198_MS_ATT1	0x400139B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX198_MS_ATT2	0x400139B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX198_MS_ATT3	0x400139BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX199_SL_ADDR	0x400139C0	Slave region, base address
PERI_MS_PPU_FX199_SL_SIZE	0x400139C4	Slave region, size. See PERI_MS_PPU_FX12_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX199_SL_ATT0	0x400139D0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX199_SL_ATT1	0x400139D4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX199_SL_ATT2	0x400139D8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX199_SL_ATT3	0x400139DC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX199_MS_ADDR	0x400139E0	Master region, base address
PERI_MS_PPU_FX199_MS_SIZE	0x400139E4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX199_MS_ATT0	0x400139F0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX199_MS_ATT1	0x400139F4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX199_MS_ATT2	0x400139F8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX199_MS_ATT3	0x400139FC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX200_SL_ADDR	0x40013A00	Slave region, base address
PERI_MS_PPU_FX200_SL_SIZE	0x40013A04	Slave region, size. See PERI_MS_PPU_FX78_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX200_SL_ATT0	0x40013A10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX200_SL_ATT1	0x40013A14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX200_SL_ATT2	0x40013A18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX200_SL_ATT3	0x40013A1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX200_MS_ADDR	0x40013A20	Master region, base address
PERI_MS_PPU_FX200_MS_SIZE	0x40013A24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX200_MS_ATT0	0x40013A30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX200_MS_ATT1	0x40013A34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX200_MS_ATT2	0x40013A38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX200_MS_ATT3	0x40013A3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX201_SL_ADDR	0x40013A40	Slave region, base address
PERI_MS_PPU_FX201_SL_SIZE	0x40013A44	Slave region, size. See PERI_MS_PPU_FX15_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX201_SL_ATT0	0x40013A50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX201_SL_ATT1	0x40013A54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX201_SL_ATT2	0x40013A58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX201_SL_ATT3	0x40013A5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX201_MS_ADDR	0x40013A60	Master region, base address
PERI_MS_PPU_FX201_MS_SIZE	0x40013A64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX201_MS_ATT0	0x40013A70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX201_MS_ATT1	0x40013A74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX201_MS_ATT2	0x40013A78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX201_MS_ATT3	0x40013A7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX202_SL_ADDR	0x40013A80	Slave region, base address
PERI_MS_PPU_FX202_SL_SIZE	0x40013A84	Slave region, size. See PERI_MS_PPU_FX62_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX202_SL_ATT0	0x40013A90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX202_SL_ATT1	0x40013A94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX202_SL_ATT2	0x40013A98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX202_SL_ATT3	0x40013A9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX202_MS_ADDR	0x40013AA0	Master region, base address
PERI_MS_PPU_FX202_MS_SIZE	0x40013AA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX202_MS_ATT0	0x40013AB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX202_MS_ATT1	0x40013AB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX202_MS_ATT2	0x40013AB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX202_MS_ATT3	0x40013ABC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX203_SL_ADDR	0x40013AC0	Slave region, base address
PERI_MS_PPU_FX203_SL_SIZE	0x40013AC4	Slave region, size. See PERI_MS_PPU_FX62_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX203_SL_ATT0	0x40013AD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX203_SL_ATT1	0x40013AD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX203_SL_ATT2	0x40013AD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX203_SL_ATT3	0x40013ADC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX203_MS_ADDR	0x40013AE0	Master region, base address
PERI_MS_PPU_FX203_MS_SIZE	0x40013AE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX203_MS_ATT0	0x40013AF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX203_MS_ATT1	0x40013AF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX203_MS_ATT2	0x40013AF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX203_MS_ATT3	0x40013AFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX204_SL_ADDR	0x40013B00	Slave region, base address
PERI_MS_PPU_FX204_SL_SIZE	0x40013B04	Slave region, size. See PERI_MS_PPU_FX62_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX204_SL_ATT0	0x40013B10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX204_SL_ATT1	0x40013B14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX204_SL_ATT2	0x40013B18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX204_SL_ATT3	0x40013B1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX204_MS_ADDR	0x40013B20	Master region, base address
PERI_MS_PPU_FX204_MS_SIZE	0x40013B24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX204_MS_ATT0	0x40013B30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX204_MS_ATT1	0x40013B34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX204_MS_ATT2	0x40013B38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX204_MS_ATT3	0x40013B3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX205_SL_ADDR	0x40013B40	Slave region, base address
PERI_MS_PPU_FX205_SL_SIZE	0x40013B44	Slave region, size. See PERI_MS_PPU_FX62_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX205_SL_ATT0	0x40013B50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX205_SL_ATT1	0x40013B54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX205_SL_ATT2	0x40013B58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX205_SL_ATT3	0x40013B5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX205_MS_ADDR	0x40013B60	Master region, base address
PERI_MS_PPU_FX205_MS_SIZE	0x40013B64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX205_MS_ATT0	0x40013B70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX205_MS_ATT1	0x40013B74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX205_MS_ATT2	0x40013B78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX205_MS_ATT3	0x40013B7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX206_SL_ADDR	0x40013B80	Slave region, base address
PERI_MS_PPU_FX206_SL_SIZE	0x40013B84	Slave region, size. See PERI_MS_PPU_FX62_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX206_SL_ATT0	0x40013B90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX206_SL_ATT1	0x40013B94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX206_SL_ATT2	0x40013B98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX206_SL_ATT3	0x40013B9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX206_MS_ADDR	0x40013BA0	Master region, base address
PERI_MS_PPU_FX206_MS_SIZE	0x40013BA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX206_MS_ATT0	0x40013BB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX206_MS_ATT1	0x40013BB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX206_MS_ATT2	0x40013BB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX206_MS_ATT3	0x40013BBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX207_SL_ADDR	0x40013BC0	Slave region, base address
PERI_MS_PPU_FX207_SL_SIZE	0x40013BC4	Slave region, size. See PERI_MS_PPU_FX62_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX207_SL_ATT0	0x40013BD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX207_SL_ATT1	0x40013BD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX207_SL_ATT2	0x40013BD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX207_SL_ATT3	0x40013BDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX207_MS_ADDR	0x40013BE0	Master region, base address
PERI_MS_PPU_FX207_MS_SIZE	0x40013BE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX207_MS_ATT0	0x40013BF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX207_MS_ATT1	0x40013BF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX207_MS_ATT2	0x40013BF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX207_MS_ATT3	0x40013BFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX208_SL_ADDR	0x40013C00	Slave region, base address
PERI_MS_PPU_FX208_SL_SIZE	0x40013C04	Slave region, size. See PERI_MS_PPU_FX62_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX208_SL_ATT0	0x40013C10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX208_SL_ATT1	0x40013C14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX208_SL_ATT2	0x40013C18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX208_SL_ATT3	0x40013C1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX208_MS_ADDR	0x40013C20	Master region, base address
PERI_MS_PPU_FX208_MS_SIZE	0x40013C24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX208_MS_ATT0	0x40013C30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX208_MS_ATT1	0x40013C34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX208_MS_ATT2	0x40013C38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX208_MS_ATT3	0x40013C3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX209_SL_ADDR	0x40013C40	Slave region, base address
PERI_MS_PPU_FX209_SL_SIZE	0x40013C44	Slave region, size. See PERI_MS_PPU_FX62_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX209_SL_ATT0	0x40013C50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX209_SL_ATT1	0x40013C54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX209_SL_ATT2	0x40013C58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX209_SL_ATT3	0x40013C5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX209_MS_ADDR	0x40013C60	Master region, base address
PERI_MS_PPU_FX209_MS_SIZE	0x40013C64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX209_MS_ATT0	0x40013C70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX209_MS_ATT1	0x40013C74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX209_MS_ATT2	0x40013C78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX209_MS_ATT3	0x40013C7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX210_SL_ADDR	0x40013C80	Slave region, base address
PERI_MS_PPU_FX210_SL_SIZE	0x40013C84	Slave region, size. See PERI_MS_PPU_FX62_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX210_SL_ATT0	0x40013C90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX210_SL_ATT1	0x40013C94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX210_SL_ATT2	0x40013C98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX210_SL_ATT3	0x40013C9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX210_MS_ADDR	0x40013CA0	Master region, base address
PERI_MS_PPU_FX210_MS_SIZE	0x40013CA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX210_MS_ATT0	0x40013CB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX210_MS_ATT1	0x40013CB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX210_MS_ATT2	0x40013CB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX210_MS_ATT3	0x40013CBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX211_SL_ADDR	0x40013CC0	Slave region, base address
PERI_MS_PPU_FX211_SL_SIZE	0x40013CC4	Slave region, size. See PERI_MS_PPU_FX62_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX211_SL_ATT0	0x40013CD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX211_SL_ATT1	0x40013CD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX211_SL_ATT2	0x40013CD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX211_SL_ATT3	0x40013CDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX211_MS_ADDR	0x40013CE0	Master region, base address
PERI_MS_PPU_FX211_MS_SIZE	0x40013CE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX211_MS_ATT0	0x40013CF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX211_MS_ATT1	0x40013CF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX211_MS_ATT2	0x40013CF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX211_MS_ATT3	0x40013CFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX212_SL_ADDR	0x40013D00	Slave region, base address
PERI_MS_PPU_FX212_SL_SIZE	0x40013D04	Slave region, size. See PERI_MS_PPU_FX62_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX212_SL_ATT0	0x40013D10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX212_SL_ATT1	0x40013D14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX212_SL_ATT2	0x40013D18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX212_SL_ATT3	0x40013D1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX212_MS_ADDR	0x40013D20	Master region, base address
PERI_MS_PPU_FX212_MS_SIZE	0x40013D24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX212_MS_ATT0	0x40013D30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX212_MS_ATT1	0x40013D34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX212_MS_ATT2	0x40013D38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX212_MS_ATT3	0x40013D3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX213_SL_ADDR	0x40013D40	Slave region, base address
PERI_MS_PPU_FX213_SL_SIZE	0x40013D44	Slave region, size. See PERI_MS_PPU_FX62_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX213_SL_ATT0	0x40013D50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX213_SL_ATT1	0x40013D54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX213_SL_ATT2	0x40013D58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX213_SL_ATT3	0x40013D5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX213_MS_ADDR	0x40013D60	Master region, base address
PERI_MS_PPU_FX213_MS_SIZE	0x40013D64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX213_MS_ATT0	0x40013D70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX213_MS_ATT1	0x40013D74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX213_MS_ATT2	0x40013D78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX213_MS_ATT3	0x40013D7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX214_SL_ADDR	0x40013D80	Slave region, base address
PERI_MS_PPU_FX214_SL_SIZE	0x40013D84	Slave region, size. See PERI_MS_PPU_FX78_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX214_SL_ATT0	0x40013D90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX214_SL_ATT1	0x40013D94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX214_SL_ATT2	0x40013D98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX214_SL_ATT3	0x40013D9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX214_MS_ADDR	0x40013DA0	Master region, base address
PERI_MS_PPU_FX214_MS_SIZE	0x40013DA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX214_MS_ATT0	0x40013DB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX214_MS_ATT1	0x40013DB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX214_MS_ATT2	0x40013DB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX214_MS_ATT3	0x40013DBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX215_SL_ADDR	0x40013DC0	Slave region, base address
PERI_MS_PPU_FX215_SL_SIZE	0x40013DC4	Slave region, size. See PERI_MS_PPU_FX78_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX215_SL_ATT0	0x40013DD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX215_SL_ATT1	0x40013DD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX215_SL_ATT2	0x40013DD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX215_SL_ATT3	0x40013DDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX215_MS_ADDR	0x40013DE0	Master region, base address
PERI_MS_PPU_FX215_MS_SIZE	0x40013DE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX215_MS_ATT0	0x40013DF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX215_MS_ATT1	0x40013DF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX215_MS_ATT2	0x40013DF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX215_MS_ATT3	0x40013DFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX216_SL_ADDR	0x40013E00	Slave region, base address
PERI_MS_PPU_FX216_SL_SIZE	0x40013E04	Slave region, size. See PERI_MS_PPU_FX78_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX216_SL_ATT0	0x40013E10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX216_SL_ATT1	0x40013E14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX216_SL_ATT2	0x40013E18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX216_SL_ATT3	0x40013E1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX216_MS_ADDR	0x40013E20	Master region, base address
PERI_MS_PPU_FX216_MS_SIZE	0x40013E24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX216_MS_ATT0	0x40013E30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX216_MS_ATT1	0x40013E34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX216_MS_ATT2	0x40013E38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX216_MS_ATT3	0x40013E3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX217_SL_ADDR	0x40013E40	Slave region, base address
PERI_MS_PPU_FX217_SL_SIZE	0x40013E44	Slave region, size. See PERI_MS_PPU_FX18_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX217_SL_ATT0	0x40013E50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX217_SL_ATT1	0x40013E54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX217_SL_ATT2	0x40013E58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX217_SL_ATT3	0x40013E5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX217_MS_ADDR	0x40013E60	Master region, base address
PERI_MS_PPU_FX217_MS_SIZE	0x40013E64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX217_MS_ATT0	0x40013E70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX217_MS_ATT1	0x40013E74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX217_MS_ATT2	0x40013E78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX217_MS_ATT3	0x40013E7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX218_SL_ADDR	0x40013E80	Slave region, base address
PERI_MS_PPU_FX218_SL_SIZE	0x40013E84	Slave region, size. See PERI_MS_PPU_FX55_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX218_SL_ATT0	0x40013E90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX218_SL_ATT1	0x40013E94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX218_SL_ATT2	0x40013E98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX218_SL_ATT3	0x40013E9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX218_MS_ADDR	0x40013EA0	Master region, base address
PERI_MS_PPU_FX218_MS_SIZE	0x40013EA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX218_MS_ATT0	0x40013EB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX218_MS_ATT1	0x40013EB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX218_MS_ATT2	0x40013EB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX218_MS_ATT3	0x40013EBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX219_SL_ADDR	0x40013EC0	Slave region, base address
PERI_MS_PPU_FX219_SL_SIZE	0x40013EC4	Slave region, size. See PERI_MS_PPU_FX78_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX219_SL_ATT0	0x40013ED0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX219_SL_ATT1	0x40013ED4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX219_SL_ATT2	0x40013ED8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX219_SL_ATT3	0x40013EDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX219_MS_ADDR	0x40013EE0	Master region, base address
PERI_MS_PPU_FX219_MS_SIZE	0x40013EE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX219_MS_ATT0	0x40013EF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX219_MS_ATT1	0x40013EF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX219_MS_ATT2	0x40013EF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX219_MS_ATT3	0x40013EFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX220_SL_ADDR	0x40013F00	Slave region, base address
PERI_MS_PPU_FX220_SL_SIZE	0x40013F04	Slave region, size. See PERI_MS_PPU_FX78_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX220_SL_ATT0	0x40013F10	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX220_SL_ATT1	0x40013F14	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX220_SL_ATT2	0x40013F18	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX220_SL_ATT3	0x40013F1C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX220_MS_ADDR	0x40013F20	Master region, base address
PERI_MS_PPU_FX220_MS_SIZE	0x40013F24	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX220_MS_ATT0	0x40013F30	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX220_MS_ATT1	0x40013F34	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX220_MS_ATT2	0x40013F38	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX220_MS_ATT3	0x40013F3C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX221_SL_ADDR	0x40013F40	Slave region, base address
PERI_MS_PPU_FX221_SL_SIZE	0x40013F44	Slave region, size. See PERI_MS_PPU_FX78_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX221_SL_ATT0	0x40013F50	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX221_SL_ATT1	0x40013F54	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX221_SL_ATT2	0x40013F58	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX221_SL_ATT3	0x40013F5C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX221_MS_ADDR	0x40013F60	Master region, base address
PERI_MS_PPU_FX221_MS_SIZE	0x40013F64	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX221_MS_ATT0	0x40013F70	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX221_MS_ATT1	0x40013F74	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX221_MS_ATT2	0x40013F78	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX221_MS_ATT3	0x40013F7C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX222_SL_ADDR	0x40013F80	Slave region, base address
PERI_MS_PPU_FX222_SL_SIZE	0x40013F84	Slave region, size. See PERI_MS_PPU_FX78_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX222_SL_ATT0	0x40013F90	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX222_SL_ATT1	0x40013F94	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX222_SL_ATT2	0x40013F98	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX222_SL_ATT3	0x40013F9C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX222_MS_ADDR	0x40013FA0	Master region, base address
PERI_MS_PPU_FX222_MS_SIZE	0x40013FA4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX222_MS_ATT0	0x40013FB0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX222_MS_ATT1	0x40013FB4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX222_MS_ATT2	0x40013FB8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX222_MS_ATT3	0x40013FBC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX223_SL_ADDR	0x40013FC0	Slave region, base address
PERI_MS_PPU_FX223_SL_SIZE	0x40013FC4	Slave region, size. See PERI_MS_PPU_FX78_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX223_SL_ATT0	0x40013FD0	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX223_SL_ATT1	0x40013FD4	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX223_SL_ATT2	0x40013FD8	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX223_SL_ATT3	0x40013FDC	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX223_MS_ADDR	0x40013FE0	Master region, base address
PERI_MS_PPU_FX223_MS_SIZE	0x40013FE4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX223_MS_ATT0	0x40013FF0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX223_MS_ATT1	0x40013FF4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX223_MS_ATT2	0x40013FF8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX223_MS_ATT3	0x40013FFC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX224_SL_ADDR	0x40014000	Slave region, base address
PERI_MS_PPU_FX224_SL_SIZE	0x40014004	Slave region, size. See PERI_MS_PPU_FX78_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX224_SL_ATT0	0x40014010	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX224_SL_ATT1	0x40014014	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX224_SL_ATT2	0x40014018	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX224_SL_ATT3	0x4001401C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX224_MS_ADDR	0x40014020	Master region, base address
PERI_MS_PPU_FX224_MS_SIZE	0x40014024	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX224_MS_ATT0	0x40014030	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX224_MS_ATT1	0x40014034	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX224_MS_ATT2	0x40014038	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX224_MS_ATT3	0x4001403C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX225_SL_ADDR	0x40014040	Slave region, base address
PERI_MS_PPU_FX225_SL_SIZE	0x40014044	Slave region, size. See PERI_MS_PPU_FX78_SL_SIZE for the details of bit fields.
PERI_MS_PPU_FX225_SL_ATT0	0x40014050	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX225_SL_ATT1	0x40014054	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX225_SL_ATT2	0x40014058	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX225_SL_ATT3	0x4001405C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX225_MS_ADDR	0x40014060	Master region, base address
PERI_MS_PPU_FX225_MS_SIZE	0x40014064	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.

Register	Address	Description
PERI_MS_PPU_FX225_MS_ATT0	0x40014070	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX225_MS_ATT1	0x40014074	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX225_MS_ATT2	0x40014078	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX225_MS_ATT3	0x4001407C	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.
PERI_MS_PPU_FX226_SL_ADDR	0x40014080	Slave region, base address
PERI_MS_PPU_FX226_SL_SIZE	0x40014084	Slave region, size
PERI_MS_PPU_FX226_SL_ATT0	0x40014090	Slave attributes 0. See PERI_MS_PPU_FX0_SL_ATT0 for the details of bit fields.
PERI_MS_PPU_FX226_SL_ATT1	0x40014094	Slave attributes 1. See PERI_MS_PPU_FX0_SL_ATT1 for the details of bit fields.
PERI_MS_PPU_FX226_SL_ATT2	0x40014098	Slave attributes 2. See PERI_MS_PPU_FX0_SL_ATT2 for the details of bit fields.
PERI_MS_PPU_FX226_SL_ATT3	0x4001409C	Slave attributes 3. See PERI_MS_PPU_FX0_SL_ATT3 for the details of bit fields.
PERI_MS_PPU_FX226_MS_ADDR	0x400140A0	Master region, base address
PERI_MS_PPU_FX226_MS_SIZE	0x400140A4	Master region, size. See PERI_MS_PPU_FX0_MS_SIZE for the details of bit fields.
PERI_MS_PPU_FX226_MS_ATT0	0x400140B0	Master attributes 0. See PERI_MS_PPU_FX0_MS_ATT0 for the details of bit fields.
PERI_MS_PPU_FX226_MS_ATT1	0x400140B4	Master attributes 1. See PERI_MS_PPU_FX0_MS_ATT1 for the details of bit fields.
PERI_MS_PPU_FX226_MS_ATT2	0x400140B8	Master attributes 2. See PERI_MS_PPU_FX0_MS_ATT2 for the details of bit fields.
PERI_MS_PPU_FX226_MS_ATT3	0x400140BC	Master attributes 3. See PERI_MS_PPU_FX0_MS_ATT3 for the details of bit fields.

2.1.1 PERI_TIMEOUT_CTL

Timeout control

Address: 0x40000200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TIMEOUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TIMEOUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	TIMEOUT	This field specifies a number of clock cycles (clk_slow). If an AHB-Lite bus transfer takes more than the specified number of cycles (timeout detection), the bus transfer is terminated with an AHB-Lite bus error and a fault is generated (and possibly recorded in the fault report structure(s)). "0x0000"-"0xfffe": Number of clock cycles. "0xffff": This value is the default/reset value and specifies that no timeout detection is performed: a bus transfer will never be terminated and a fault will never be generated. Default Value: 0xFFFF

2.1.2 PERI_TR_CMD

Trigger command

Address: 0x40000220

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TR_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			GROUP_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	None				
HW Access	RW1C	R	R	None				
Name	ACTIVATE	OUT_SEL	TR_EDGE	None [28:24]				

Bits	Name	Description
31	ACTIVATE	SW sets this field to '1' to activate (set to '1') a trigger as identified by TR_SEL, TR_EDGE and OUT_SEL. HW sets this field to '0' for edge sensitive triggers AFTER the selected trigger is activated for two clk_peri cycles. Note: when ACTIVATE is '1', SW should not modify the other register fields. Default Value: 0
30	OUT_SEL	Specifies whether trigger activation is for a specific input or output trigger of the trigger multiplexer. Activation of a specific input trigger, will result in activation of all output triggers that have the specific input trigger selected through their TR_OUT_CTL.TR_SEL field. Activation of a specific output trigger, will result in activation of the specified TR_SEL output trigger only. '0': TR_SEL selection and trigger activation is for an input trigger to the trigger multiplexer. '1': TR_SEL selection and trigger activation is for an output trigger from the trigger multiplexer. Note: this field is not used for trigger 1-to-1 groups. Default Value: 0
29	TR_EDGE	Specifies if the activated trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. The trigger reflects TR_CMD.ACTIVATE. '1': edge sensitive trigger. The trigger is activated for two clk_peri cycles. Default Value: 0

2.1.2 PERI_TR_CMD (continued)

12 : 8	GROUP_SEL	Specifies the trigger group: "0"-"15": trigger multiplexer groups. "16"-"31": trigger 1-to-1 groups. Default Value: 0
7 : 0	TR_SEL	Specifies the activated trigger when ACTIVATE is '1'. If the specified trigger is not present, the trigger activation has no effect. Default Value: 0

2.1.3 PERI_DIV_CMD

Divider command

Address: 0x40000400

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DIV_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						TYPE_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	PA_DIV_SEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None				RW	
HW Access	RW1C	RW1C	None				R	
Name	ENABLE	DISABLE	None [29:26]				PA_TYPE_SEL [25:24]	

Bits	Name	Description
31	ENABLE	Clock divider enable command (mutually exclusive with DISABLE). Typically, SW sets this field to '1' to enable a divider and HW sets this field to '0' to indicate that divider enabling has completed. When a divider is enabled, its integer and fractional (if present) counters are initialized to "0". If a divider is to be re-enabled using different integer and fractional divider values, the SW should follow these steps: 0: Disable the divider using the DIV_CMD.DISABLE field. 1: Configure the divider's DIV_XXX_CTL register. 2: Enable the divider using the DIV_CMD_ENABLE field. The DIV_SEL and TYPE_SEL fields specify which divider is to be enabled. The enabled divider may be phase aligned to either "clk_peri" (typical usage) or to ANY enabled divider. The PA_DIV_SEL and PA_TYPE_SEL fields specify the reference divider. The HW sets the ENABLE field to '0' when the enabling is performed and the HW set the DIV_XXX_CTL.EN field of the divider to '1' when the enabling is performed. Note that enabling with phase alignment to a low frequency divider takes time. E.g. To align to a divider that generates a clock of "clk_peri"/n (with n being the integer divider value INT_DIV+1), up to n cycles may be required to perform alignment. Phase alignment to "clk_peri" takes affect immediately. SW can set this field to '0' during phase alignment to abort the enabling process. Default Value: 0

2.1.3 PERI_DIV_CMD (continued)

30	DISABLE	Clock divider disable command (mutually exclusive with ENABLE). SW sets this field to '1' and HW sets this field to '0'. The DIV_SEL and TYPE_SEL fields specify which divider is to be disabled. The HW sets the DISABLE field to '0' immediately and the HW sets the DIV_XXX_CTL.EN field of the divider to '0' immediately. Default Value: 0
25 : 24	PA_TYPE_SEL	Specifies the divider type of the divider to which phase alignment is performed for the clock enable command: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
23 : 16	PA_DIV_SEL	(PA_TYPE_SEL, PA_DIV_SEL) specifies the divider to which phase alignment is performed for the clock enable command. Any enabled divider can be used as reference. This allows all dividers to be aligned with each other, even when they are enabled at different times. If PA_DIV_SEL is "255" and PA_TYPE_SEL is "3", "clk_peri" is used as reference. Default Value: 255
9 : 8	TYPE_SEL	Specifies the divider type of the divider on which the command is performed: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
7 : 0	DIV_SEL	(TYPE_SEL, DIV_SEL) specifies the divider on which the command (DISABLE/ENABLE) is performed. If DIV_SEL is "255" and TYPE_SEL is "3" (default/reset value), no divider is specified and no clock signal(s) are generated. Default Value: 255

2.1.4 PERI_CLOCK_CTL0

Clock control

Address: 0x40000C00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					DIV_SEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						TYPE_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	TYPE_SEL	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
2 : 0	DIV_SEL	Specifies one of the dividers of the divider type specified by TYPE_SEL. If DIV_SEL is "255" and TYPE_SEL is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out-of-phase dividers, spurious clock control signals may be generated for one "clk_peri" cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (DIV_SEL is "255" and TYPE_-SEL is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 7

2.1.5 PERI_DIV_8_CTL0

Divider control (for 8.0 divider)

Address: 0x40001000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT8_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	INT8_DIV	Integer division by (1+INT8_DIV). Allows for integer divisions in the range [1, 256]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 256]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 256]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

2.1.6 PERI_DIV_16_CTL0

Divider control (for 16.0 divider)

Address: 0x40001400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

2.1.7 PERI_DIV_16_5_CTL0

Divider control (for 16.5 divider)

Address: 0x40001800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		R
HW Access	R					None		RW
Name	FRAC5_DIV [7:3]					None [2:1]		EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: combined with fractional division, this divider type allows for a division in the range [1, 65,536 31/32] in 1/32 increments. For the generation of a divided clock, the division range is restricted to [2, 65,536 31/32]. For the generation of a 50/50% duty cycle divided clock, the division range is restricted to [2, 65,536]. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
7 : 3	FRAC5_DIV	Fractional division by (FRAC5_DIV/32). Allows for fractional divisions in the range [0, 31/32]. Note that fractional division results in clock jitter as some clock periods may be 1 "clk_peri" cycle longer than other clock periods. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0

2.1.7 PERI_DIV_16_5_CTL0 (continued)

0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

2.1.8 PERI_DIV_24_5_CTL0

Divider control (for 24.5 divider)

Address: 0x40001C00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		R
HW Access	R					None		RW
Name	FRAC5_DIV [7:3]					None [2:1]		EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT24_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT24_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	INT24_DIV [31:24]							

Bits	Name	Description
31 : 8	INT24_DIV	Integer division by (1+INT24_DIV). Allows for integer divisions in the range [1, 16,777,216]. Note: combined with fractional division, this divider type allows for a division in the range [1, 16,777,216 31/32] in 1/32 increments. For the generation of a divided clock, the integer division range is restricted to [2, 16,777,216 31/32]. For the generation of a 50/50% duty cycle divided clock, the division range is restricted to [2, 16,777,216]. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
7 : 3	FRAC5_DIV	Fractional division by (FRAC5_DIV/32). Allows for fractional divisions in the range [0, 31/32]. Note that fractional division results in clock jitter as some clock periods may be 1 "clk_peri" cycle longer than other clock periods. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0

2.1.8 PERI_DIV_24_5_CTL0 (continued)

0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

2.1.9 PERI_GR0_SL_CTL

Slave control

Address: 0x40004010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						ENABLED_1	ENABLED_0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW1S	RW1S
HW Access	None						R	R
Name	None [23:18]						DISABLED_1	DISABLED_0

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	DISABLED_1	Default Value: 0
16	DISABLED_0	Peripheral group, slave 0 permanent disable. Setting this bit to 1 has the same effect as setting ENABLED_0 to 0. However, once set to 1, this bit cannot be changed back to 0 anymore. Default Value: 0
1	ENABLED_1	Peripheral group, slave 1 enable. If the slave is disabled, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 (the peripheral interconnect, master interface MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. Default Value: 1
0	ENABLED_0	Peripheral group, slave 0 enable. If the slave is disabled, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 (the peripheral interconnect MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. Default Value: 1

2.1.10 PERI_GR1_SL_CTL

Slave control

Address: 0x40004030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							ENABLED_0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW1S
HW Access	None							R
Name	None [23:17]							DISABLED_0

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	DISABLED_0	Peripheral group, slave 0 permanent disable. Setting this bit to 1 has the same effect as setting ENABLED_0 to 0. However, once set to 1, this bit cannot be changed back to 0 anymore. Default Value: 0
0	ENABLED_0	Peripheral group, slave 0 enable. If the slave is disabled, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 (the peripheral interconnect MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. Default Value: 1

2.1.11 PERI_GR2_SL_CTL

Slave control
(Note: Writing to this register to disable group 2 slaves could disable all Protection Units. This register itself should be protected from writes for Protection Contexts (PC) > 0)

Address: 0x40004050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	None	RW	RW	RW	RW	RW
HW Access	R	R	None	R	R	R	R	R
Name	EN-ABLED_7	EN-ABLED_6	None	EN-ABLED_4	EN-ABLED_3	EN-ABLED_2	EN-ABLED_1	EN-ABLED_0

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None	RW	RW	RW
HW Access	None			R	None	R	R	R
Name	None [15:13]			EN-ABLED_12	None	EN-ABLED_10	EN-ABLED_9	EN-ABLED_8

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S	RW1S	None	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	R	R	None	R	R	R	R	R
Name	DIS-ABLED_7	DIS-ABLED_6	None	DIS-ABLED_4	DIS-ABLED_3	DIS-ABLED_2	DIS-ABLED_1	DIS-ABLED_0

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW1S	None	RW1S	RW1S	RW1S
HW Access	None			R	None	R	R	R
Name	None [31:29]			DIS-ABLED_12	None	DIS-ABLED_10	DIS-ABLED_9	DIS-ABLED_8

Bits	Name	Description
28	DISABLED_12	Default Value: 0
26	DISABLED_10	Default Value: 0
25	DISABLED_9	Default Value: 0
24	DISABLED_8	Default Value: 0
23	DISABLED_7	Default Value: 0
22	DISABLED_6	Default Value: 0
20	DISABLED_4	Default Value: 0
19	DISABLED_3	Default Value: 0
18	DISABLED_2	Default Value: 0

2.1.11 PERI_GR2_SL_CTL (continued)

17	DISABLED_1	Default Value: 0
16	DISABLED_0	Peripheral group, slave 0 permanent disable. Setting this bit to 1 has the same effect as setting ENABLED_0 to 0. However, once set to 1, this bit cannot be changed back to 0 anymore. Default Value: 0
12	ENABLED_12	Default Value: 1
10	ENABLED_10	Default Value: 1
9	ENABLED_9	Default Value: 1
8	ENABLED_8	Default Value: 1
7	ENABLED_7	Default Value: 1
6	ENABLED_6	Default Value: 1
4	ENABLED_4	Default Value: 1
3	ENABLED_3	Default Value: 1
2	ENABLED_2	Default Value: 1
1	ENABLED_1	Peripheral group, slave 1 enable. If the slave is disabled, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 (the peripheral interconnect, master interface MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. Default Value: 1
0	ENABLED_0	Peripheral group, slave 0 enable. If the slave is disabled, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 (the peripheral interconnect MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. Default Value: 1

2.1.12 PERI_GR3_CLOCK_CTL

Clock control

Address: 0x40004060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT8_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	INT8_DIV	Specifies a group clock divider (from the peripheral clock "clk_peri" to the group clock "clk_group[3/4/5/...15]"). Integer division by (1+INT8_DIV). Allows for integer divisions in the range [1, 256]. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0

2.1.13 PERI_GR3_SL_CTL

Slave control

Address: 0x40004070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	None		RW	RW	RW
HW Access	None	R	R	None		R	R	R
Name	None	EN-ABLED_6	EN-ABLED_5	None [4:3]		EN-ABLED_2	EN-ABLED_1	EN-ABLED_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	None			RW	None		RW
HW Access	R	None			R	None		R
Name	EN-ABLED_15	None [14:12]			EN-ABLED_11	None [10:9]		EN-ABLED_8

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW1S	RW1S	None		RW1S	RW1S	RW1S
HW Access	None	R	R	None		R	R	R
Name	None	DIS-ABLED_6	DIS-ABLED_5	None [20:19]		DIS-ABLED_2	DIS-ABLED_1	DIS-ABLED_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	None			RW1S	None		RW1S
HW Access	R	None			R	None		R
Name	DIS-ABLED_15	None [30:28]			DIS-ABLED_11	None [26:25]		DIS-ABLED_8

Bits	Name	Description
31	DISABLED_15	Default Value: 0
27	DISABLED_11	Default Value: 0
24	DISABLED_8	Default Value: 0
22	DISABLED_6	Default Value: 0
21	DISABLED_5	Default Value: 0
18	DISABLED_2	Default Value: 0
17	DISABLED_1	Default Value: 0
16	DISABLED_0	Peripheral group, slave 0 permanent disable. Setting this bit to 1 has the same effect as setting ENABLED_0 to 0. However, once set to 1, this bit cannot be changed back to 0 anymore. Default Value: 0
15	ENABLED_15	Default Value: 1

2.1.13 PERI_GR3_SL_CTL (continued)

11	ENABLED_11	Default Value: 1
8	ENABLED_8	Default Value: 1
6	ENABLED_6	Default Value: 1
5	ENABLED_5	Default Value: 1
2	ENABLED_2	Default Value: 1
1	ENABLED_1	Peripheral group, slave 1 enable. If the slave is disabled, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 (the peripheral interconnect, master interface MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. Default Value: 1
0	ENABLED_0	Peripheral group, slave 0 enable. If the slave is disabled, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 (the peripheral interconnect MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. Default Value: 1

2.1.14 PERI_GR4_SL_CTL

Slave control

Address: 0x40004090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	None	
HW Access	None					R	None	
Name	None [7:3]					ENABLED_2	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW1S	None	
HW Access	None					R	None	
Name	None [23:19]					DISABLED_2	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
18	DISABLED_2	Default Value: 0
2	ENABLED_2	Default Value: 1

2.1.15 PERI_GR6_SL_CTL

Slave control

Address: 0x400040D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW	RW	RW
HW Access	None	R	R	R	None	R	R	R
Name	None	EN-ABLED_6	EN-ABLED_5	EN-ABLED_4	None	EN-ABLED_2	EN-ABLED_1	EN-ABLED_0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW1S	RW1S	RW1S	None	RW1S	RW1S	RW1S
HW Access	None	R	R	R	None	R	R	R
Name	None	DIS-ABLED_6	DIS-ABLED_5	DIS-ABLED_4	None	DIS-ABLED_2	DIS-ABLED_1	DIS-ABLED_0

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
22	DISABLED_6	Default Value: 0
21	DISABLED_5	Default Value: 0
20	DISABLED_4	Default Value: 0
18	DISABLED_2	Default Value: 0
17	DISABLED_1	Default Value: 0
16	DISABLED_0	Peripheral group, slave 0 permanent disable. Setting this bit to 1 has the same effect as setting ENABLED_0 to 0. However, once set to 1, this bit cannot be changed back to 0 anymore. Default Value: 0
6	ENABLED_6	Default Value: 1
5	ENABLED_5	Default Value: 1
4	ENABLED_4	Default Value: 1
2	ENABLED_2	Default Value: 1

2.1.15 PERI_GR6_SL_CTL (continued)

1	ENABLED_1	Peripheral group, slave 1 enable. If the slave is disabled, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 (the peripheral interconnect, master interface MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. Default Value: 1
0	ENABLED_0	Peripheral group, slave 0 enable. If the slave is disabled, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 (the peripheral interconnect MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. Default Value: 1

2.1.16 PERI_TR_GR0_TR_CTL0

Trigger control register

Address: 0x40008000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	TR_SEL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_-FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
6 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

2.1.17 PERI_TR_GR2_TR_CTL0

Trigger control register

Address: 0x40008800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TR_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_-FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
7 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

2.1.18 PERI_TR_GR4_TR_CTL0

Trigger control register

Address: 0x40009000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TR_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_-FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
7 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

2.1.19 PERI_TR_GR6_TR_CTL0

Trigger control register

Address: 0x40009800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			TR_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_-FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
4 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

2.1.20 PERI_TR_GR7_TR_CTL0

Trigger control register

Address: 0x40009C00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						TR_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_-FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
1 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

2.1.21 PERI_TR_GR8_TR_CTL0

Trigger control register

Address: 0x4000A000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TR_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_-FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
7 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

2.1.22 PERI_TR_GR9_TR_CTL0

Trigger control register

Address: 0x4000A400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	TR_SEL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_-FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
6 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

2.1.23 PERI_TR_GR10_TR_CTL0

Trigger control register

Address: 0x4000A800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TR_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_-FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

2.1.24 PERI_TR_GR11_TR_CTL0

Trigger control register

Address: 0x4000AC00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		TR_SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_-FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
5 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

2.1.25 PERI_TR_1TO1_GR0_TR_CTL0

Trigger control register

Address: 0x4000C000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TR_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_-FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
0	TR_SEL	Specifies input trigger: '0'': constant signal level '0'. '1': input trigger. Default Value: 0

2.1.26 PERI_TR_1TO1_GR1_TR_CTL0

Trigger control register

Address: 0x4000C400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TR_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_-FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
0	TR_SEL	Specifies input trigger: '0'': constant signal level '0'. '1': input trigger. Default Value: 0

2.1.27 PERI_TR_1TO1_GR2_TR_CTL0

Trigger control register

Address: 0x4000C800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TR_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_-FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
0	TR_SEL	Specifies input trigger: '0'': constant signal level '0'. '1': input trigger. Default Value: 0

2.1.28 PERI_TR_1TO1_GR3_TR_CTL0

Trigger control register

Address: 0x4000CC00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TR_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_-FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
0	TR_SEL	Specifies input trigger: '0'': constant signal level '0'. '1': input trigger. Default Value: 0

2.1.29 PERI_TR_1TO1_GR4_TR_CTL0

Trigger control register

Address: 0x4000D000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TR_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_-FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
0	TR_SEL	Specifies input trigger: '0'': constant signal level '0'. '1': input trigger. Default Value: 0

2.1.30 PERI_TR_1TO1_GR5_TR_CTL0

Trigger control register

Address: 0x4000D400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TR_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			DBG_-FREEZE_EN	None [11:10]		TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	DBG_FREEZE_EN	Specifies if the output trigger is blocked in debug mode. When set high tr_dbg_freeze will block the output trigger generation. Default Value: 0
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
0	TR_SEL	Specifies input trigger: '0'': constant signal level '0'. '1': input trigger. Default Value: 0

2.1.31 PERI_MS_PPU_PR0_SL_ADDR

Slave region, base address

Address: 0x40010000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: Undefined

2.1.32 PERI_MS_PPU_PR0_SL_SIZE

Slave region, size

Address: 0x40010004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None		RW				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Slave region enable: '0': Disabled. A disabled region will never result in a match on the transfer address. '1': Enabled. Default Value: 0

2.1.32 PERI_MS_PPU_PR0_SL_SIZE (continued)

28 : 24	REGION_SIZE	This field specifies the size of the slave region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: Undefined

2.1.33 PERI_MS_PPU_PR0_SL_ATT0

Slave attributes 0

Address: 0x40010010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	R	R	R	R
HW Access	None			R	R	R	R	R
Name	None [7:5]			PC0_NS	PC0_PW	PC0_PR	PC0_UW	PC0_UR

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [15:13]			PC1_NS	PC1_PW	PC1_PR	PC1_UW	PC1_UR

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [23:21]			PC2_NS	PC2_PW	PC2_PR	PC2_UW	PC2_UR

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [31:29]			PC3_NS	PC3_PW	PC3_PR	PC3_UW	PC3_UR

Bits	Name	Description
28	PC3_NS	Protection context 3, non-secure. Default Value: 1
27	PC3_PW	Protection context 3, privileged write enable. Default Value: 1
26	PC3_PR	Protection context 3, privileged read enable. Default Value: 1
25	PC3_UW	Protection context 3, user write enable. Default Value: 1
24	PC3_UR	Protection context 3, user read enable. Default Value: 1
20	PC2_NS	Protection context 2, non-secure. Default Value: 1
19	PC2_PW	Protection context 2, privileged write enable. Default Value: 1
18	PC2_PR	Protection context 2, privileged read enable. Default Value: 1

2.1.33 PERI_MS_PPU_PR0_SL_ATT0 (continued)

17	PC2_UW	Protection context 2, user write enable. Default Value: 1
16	PC2_UR	Protection context 2, user read enable. Default Value: 1
12	PC1_NS	Protection context 1, non-secure. Default Value: 1
11	PC1_PW	Protection context 1, privileged write enable. Default Value: 1
10	PC1_PR	Protection context 1, privileged read enable. Default Value: 1
9	PC1_UW	Protection context 1, user write enable. Default Value: 1
8	PC1_UR	Protection context 1, user read enable. Default Value: 1
4	PC0_NS	Protection context 0, non-secure: '0': Secure (secure accesses allowed, non-secure access NOT allowed). '1': Non-secure (both secure and non-secure accesses allowed). Default Value: 1
3	PC0_PW	Protection context 0, privileged write enable: '0': Disabled (privileged, write accesses are NOT allowed). '1': Enabled (privileged, write accesses are allowed). Default Value: 1
2	PC0_PR	Protection context 0, privileged read enable: '0': Disabled (privileged, read accesses are NOT allowed). '1': Enabled (privileged, read accesses are allowed). Default Value: 1
1	PC0_UW	Protection context 0, user write enable: '0': Disabled (user, write accesses are NOT allowed). '1': Enabled (user, write accesses are allowed). Default Value: 1
0	PC0_UR	Protection context 0, user read enable: '0': Disabled (user, read accesses are NOT allowed). '1': Enabled (user, read accesses are allowed). Default Value: 1

2.1.34 PERI_MS_PPU_PR0_SL_ATT1

Slave attributes 1

Address: 0x40010014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			PC4_NS	PC4_PW	PC4_PR	PC4_UW	PC4_UR

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [15:13]			PC5_NS	PC5_PW	PC5_PR	PC5_UW	PC5_UR

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [23:21]			PC6_NS	PC6_PW	PC6_PR	PC6_UW	PC6_UR

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [31:29]			PC7_NS	PC7_PW	PC7_PR	PC7_UW	PC7_UR

Bits	Name	Description
28	PC7_NS	Protection context 7, non-secure. Default Value: 1
27	PC7_PW	Protection context 7, privileged write enable. Default Value: 1
26	PC7_PR	Protection context 7, privileged read enable. Default Value: 1
25	PC7_UW	Protection context 7, user write enable. Default Value: 1
24	PC7_UR	Protection context 7, user read enable. Default Value: 1
20	PC6_NS	Protection context 6, non-secure. Default Value: 1
19	PC6_PW	Protection context 6, privileged write enable. Default Value: 1
18	PC6_PR	Protection context 6, privileged read enable. Default Value: 1

2.1.34 PERI_MS_PPU_PR0_SL_ATT1 (continued)

17	PC6_UW	Protection context 6, user write enable. Default Value: 1
16	PC6_UR	Protection context 6, user read enable. Default Value: 1
12	PC5_NS	Protection context 5, non-secure. Default Value: 1
11	PC5_PW	Protection context 5, privileged write enable. Default Value: 1
10	PC5_PR	Protection context 5, privileged read enable. Default Value: 1
9	PC5_UW	Protection context 5, user write enable. Default Value: 1
8	PC5_UR	Protection context 5, user read enable. Default Value: 1
4	PC4_NS	Protection context 4, non-secure. Default Value: 1
3	PC4_PW	Protection context 4, privileged write enable. Default Value: 1
2	PC4_PR	Protection context 4, privileged read enable. Default Value: 1
1	PC4_UW	Protection context 4, user write enable. Default Value: 1
0	PC4_UR	Protection context 4, user read enable. Default Value: 1

2.1.35 PERI_MS_PPU_PR0_SL_ATT2

Slave attributes 2

Address: 0x40010018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			PC8_NS	PC8_PW	PC8_PR	PC8_UW	PC8_UR

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [15:13]			PC9_NS	PC9_PW	PC9_PR	PC9_UW	PC9_UR

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [23:21]			PC10_NS	PC10_PW	PC10_PR	PC10_UW	PC10_UR

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [31:29]			PC11_NS	PC11_PW	PC11_PR	PC11_UW	PC11_UR

Bits	Name	Description
28	PC11_NS	Protection context 11, non-secure. Default Value: 1
27	PC11_PW	Protection context 11, privileged write enable. Default Value: 1
26	PC11_PR	Protection context 11, privileged read enable. Default Value: 1
25	PC11_UW	Protection context 11, user write enable. Default Value: 1
24	PC11_UR	Protection context 11, user read enable. Default Value: 1
20	PC10_NS	Protection context 10, non-secure. Default Value: 1
19	PC10_PW	Protection context 10, privileged write enable. Default Value: 1
18	PC10_PR	Protection context 10, privileged read enable. Default Value: 1

2.1.35 PERI_MS_PPU_PR0_SL_ATT2 (continued)

17	PC10_UW	Protection context 10, user write enable. Default Value: 1
16	PC10_UR	Protection context 10, user read enable. Default Value: 1
12	PC9_NS	Protection context 9, non-secure. Default Value: 1
11	PC9_PW	Protection context 9, privileged write enable. Default Value: 1
10	PC9_PR	Protection context 9, privileged read enable. Default Value: 1
9	PC9_UW	Protection context 9, user write enable. Default Value: 1
8	PC9_UR	Protection context 9, user read enable. Default Value: 1
4	PC8_NS	Protection context 8, non-secure. Default Value: 1
3	PC8_PW	Protection context 8, privileged write enable. Default Value: 1
2	PC8_PR	Protection context 8, privileged read enable. Default Value: 1
1	PC8_UW	Protection context 8, user write enable. Default Value: 1
0	PC8_UR	Protection context 8, user read enable. Default Value: 1

2.1.36 PERI_MS_PPU_PR0_SL_ATT3

Slave attributes 3

Address: 0x4001001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			PC12_NS	PC12_PW	PC12_PR	PC12_UW	PC12_UR

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [15:13]			PC13_NS	PC13_PW	PC13_PR	PC13_UW	PC13_UR

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [23:21]			PC14_NS	PC14_PW	PC14_PR	PC14_UW	PC14_UR

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [31:29]			PC15_NS	PC15_PW	PC15_PR	PC15_UW	PC15_UR

Bits	Name	Description
28	PC15_NS	Protection context 15, non-secure. Default Value: 1
27	PC15_PW	Protection context 15, privileged write enable. Default Value: 1
26	PC15_PR	Protection context 15, privileged read enable. Default Value: 1
25	PC15_UW	Protection context 15, user write enable. Default Value: 1
24	PC15_UR	Protection context 15, user read enable. Default Value: 1
20	PC14_NS	Protection context 14, non-secure. Default Value: 1
19	PC14_PW	Protection context 14, privileged write enable. Default Value: 1
18	PC14_PR	Protection context 14, privileged read enable. Default Value: 1

2.1.36 PERI_MS_PPU_PR0_SL_ATT3 (continued)

17	PC14_UW	Protection context 14, user write enable. Default Value: 1
16	PC14_UR	Protection context 14, user read enable. Default Value: 1
12	PC13_NS	Protection context 13, non-secure. Default Value: 1
11	PC13_PW	Protection context 13, privileged write enable. Default Value: 1
10	PC13_PR	Protection context 13, privileged read enable. Default Value: 1
9	PC13_UW	Protection context 13, user write enable. Default Value: 1
8	PC13_UR	Protection context 13, user read enable. Default Value: 1
4	PC12_NS	Protection context 12, non-secure. Default Value: 1
3	PC12_PW	Protection context 12, privileged write enable. Default Value: 1
2	PC12_PR	Protection context 12, privileged read enable. Default Value: 1
1	PC12_UW	Protection context 12, user write enable. Default Value: 1
0	PC12_UR	Protection context 12, user read enable. Default Value: 1

2.1.37 PERI_MS_PPU_PR0_MS_ADDR

Master region, base address

Address: 0x40010020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778240

2.1.38 PERI_MS_PPU_PR0_MS_SIZE

Master region, size

Address: 0x40010024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None		R				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Master region enable: '1': Enabled. Default Value: 1
28 : 24	REGION_SIZE	This field specifies the size of the master region: "5": 64 B region The master region includes the SL_ADDR, SL_SIZE, SL_ATT0, ..., SL_ATT3, MS_ADDR, MS_-SIZE, MS_ATT0, ..., MS_ATT3 registers. Therefore, the access privileges for all these registers is determined by MS_ATT0, ..., MS_ATT3. Default Value: 0x05

2.1.39 PERI_MS_PPU_PR0_MS_ATT0

Master attributes 0

Address: 0x40010030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	R	R	R	R
HW Access	None			R	R	R	R	R
Name	None [7:5]			PC0_NS	PC0_PW	PC0_PR	PC0_UW	PC0_UR

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [15:13]			PC1_NS	PC1_PW	PC1_PR	PC1_UW	PC1_UR

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [23:21]			PC2_NS	PC2_PW	PC2_PR	PC2_UW	PC2_UR

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [31:29]			PC3_NS	PC3_PW	PC3_PR	PC3_UW	PC3_UR

Bits	Name	Description
28	PC3_NS	Protection context 3, non-secure. Default Value: 1
27	PC3_PW	Protection context 3, privileged write enable. Default Value: 1
26	PC3_PR	Protection context 3, privileged read enable. Default Value: 1
25	PC3_UW	Protection context 3, user write enable. Default Value: 1
24	PC3_UR	Protection context 3, user read enable. Default Value: 1
20	PC2_NS	Protection context 2, non-secure. Default Value: 1
19	PC2_PW	Protection context 2, privileged write enable. Default Value: 1
18	PC2_PR	Protection context 2, privileged read enable. Default Value: 1

2.1.39 PERI_MS_PPU_PR0_MS_ATT0 (continued)

17	PC2_UW	Protection context 2, user write enable. Default Value: 1
16	PC2_UR	Protection context 2, user read enable. Default Value: 1
12	PC1_NS	Protection context 1, non-secure. Default Value: 1
11	PC1_PW	Protection context 1, privileged write enable. Default Value: 1
10	PC1_PR	Protection context 1, privileged read enable. Default Value: 1
9	PC1_UW	Protection context 1, user write enable. Default Value: 1
8	PC1_UR	Protection context 1, user read enable. Default Value: 1
4	PC0_NS	Protection context 0, non-secure: '0': Secure (secure accesses allowed, non-secure access NOT allowed). '1': Non-secure (both secure and non-secure accesses allowed). Default Value: 1
3	PC0_PW	Protection context 0, privileged write enable: '0': Disabled (privileged, write accesses are NOT allowed). '1': Enabled (privileged, write accesses are allowed). Default Value: 1
2	PC0_PR	Protection context 0, privileged read enable: '0': Disabled (privileged, read accesses are NOT allowed). '1': Enabled (privileged, read accesses are allowed). Default Value: 1
1	PC0_UW	Protection context 0, user write enable: '0': Disabled (user, write accesses are NOT allowed). '1': Enabled (user, write accesses are allowed). Default Value: 1
0	PC0_UR	Protection context 0, user read enable: '0': Disabled (user, read accesses are NOT allowed). '1': Enabled (user, read accesses are allowed). Default Value: 1

2.1.40 PERI_MS_PPU_PR0_MS_ATT1

Master attributes 1

Address: 0x40010034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [7:5]			PC4_NS	PC4_PW	PC4_PR	PC4_UW	PC4_UR

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [15:13]			PC5_NS	PC5_PW	PC5_PR	PC5_UW	PC5_UR

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [23:21]			PC6_NS	PC6_PW	PC6_PR	PC6_UW	PC6_UR

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [31:29]			PC7_NS	PC7_PW	PC7_PR	PC7_UW	PC7_UR

Bits	Name	Description
28	PC7_NS	Protection context 7, non-secure. Default Value: 1
27	PC7_PW	Protection context 7, privileged write enable. Default Value: 1
26	PC7_PR	Protection context 7, privileged read enable. Default Value: 1
25	PC7_UW	Protection context 7, user write enable. Default Value: 1
24	PC7_UR	Protection context 7, user read enable. Default Value: 1
20	PC6_NS	Protection context 6, non-secure. Default Value: 1
19	PC6_PW	Protection context 6, privileged write enable. Default Value: 1
18	PC6_PR	Protection context 6, privileged read enable. Default Value: 1

2.1.40 PERI_MS_PPU_PR0_MS_ATT1 (continued)

17	PC6_UW	Protection context 6, user write enable. Default Value: 1
16	PC6_UR	Protection context 6, user read enable. Default Value: 1
12	PC5_NS	Protection context 5, non-secure. Default Value: 1
11	PC5_PW	Protection context 5, privileged write enable. Default Value: 1
10	PC5_PR	Protection context 5, privileged read enable. Default Value: 1
9	PC5_UW	Protection context 5, user write enable. Default Value: 1
8	PC5_UR	Protection context 5, user read enable. Default Value: 1
4	PC4_NS	Protection context 4, non-secure. Default Value: 1
3	PC4_PW	Protection context 4, privileged write enable. Default Value: 1
2	PC4_PR	Protection context 4, privileged read enable. Default Value: 1
1	PC4_UW	Protection context 4, user write enable. Default Value: 1
0	PC4_UR	Protection context 4, user read enable. Default Value: 1

2.1.41 PERI_MS_PPU_PR0_MS_ATT2

Master attributes 2

Address: 0x40010038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [7:5]			PC8_NS	PC8_PW	PC8_PR	PC8_UW	PC8_UR

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [15:13]			PC9_NS	PC9_PW	PC9_PR	PC9_UW	PC9_UR

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [23:21]			PC10_NS	PC10_PW	PC10_PR	PC10_UW	PC10_UR

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [31:29]			PC11_NS	PC11_PW	PC11_PR	PC11_UW	PC11_UR

Bits	Name	Description
28	PC11_NS	Protection context 11, non-secure. Default Value: 1
27	PC11_PW	Protection context 11, privileged write enable. Default Value: 1
26	PC11_PR	Protection context 11, privileged read enable. Default Value: 1
25	PC11_UW	Protection context 11, user write enable. Default Value: 1
24	PC11_UR	Protection context 11, user read enable. Default Value: 1
20	PC10_NS	Protection context 10, non-secure. Default Value: 1
19	PC10_PW	Protection context 10, privileged write enable. Default Value: 1
18	PC10_PR	Protection context 10, privileged read enable. Default Value: 1

2.1.41 PERI_MS_PPU_PR0_MS_ATT2 (continued)

17	PC10_UW	Protection context 10, user write enable. Default Value: 1
16	PC10_UR	Protection context 10, user read enable. Default Value: 1
12	PC9_NS	Protection context 9, non-secure. Default Value: 1
11	PC9_PW	Protection context 9, privileged write enable. Default Value: 1
10	PC9_PR	Protection context 9, privileged read enable. Default Value: 1
9	PC9_UW	Protection context 9, user write enable. Default Value: 1
8	PC9_UR	Protection context 9, user read enable. Default Value: 1
4	PC8_NS	Protection context 8, non-secure. Default Value: 1
3	PC8_PW	Protection context 8, privileged write enable. Default Value: 1
2	PC8_PR	Protection context 8, privileged read enable. Default Value: 1
1	PC8_UW	Protection context 8, user write enable. Default Value: 1
0	PC8_UR	Protection context 8, user read enable. Default Value: 1

2.1.42 PERI_MS_PPU_PR0_MS_ATT3

Master attributes 3

Address: 0x4001003C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [7:5]			PC12_NS	PC12_PW	PC12_PR	PC12_UW	PC12_UR

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [15:13]			PC13_NS	PC13_PW	PC13_PR	PC13_UW	PC13_UR

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [23:21]			PC14_NS	PC14_PW	PC14_PR	PC14_UW	PC14_UR

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [31:29]			PC15_NS	PC15_PW	PC15_PR	PC15_UW	PC15_UR

Bits	Name	Description
28	PC15_NS	Protection context 15, non-secure. Default Value: 1
27	PC15_PW	Protection context 15, privileged write enable. Default Value: 1
26	PC15_PR	Protection context 15, privileged read enable. Default Value: 1
25	PC15_UW	Protection context 15, user write enable. Default Value: 1
24	PC15_UR	Protection context 15, user read enable. Default Value: 1
20	PC14_NS	Protection context 14, non-secure. Default Value: 1
19	PC14_PW	Protection context 14, privileged write enable. Default Value: 1
18	PC14_PR	Protection context 14, privileged read enable. Default Value: 1

2.1.42 PERI_MS_PPU_PR0_MS_ATT3 (continued)

17	PC14_UW	Protection context 14, user write enable. Default Value: 1
16	PC14_UR	Protection context 14, user read enable. Default Value: 1
12	PC13_NS	Protection context 13, non-secure. Default Value: 1
11	PC13_PW	Protection context 13, privileged write enable. Default Value: 1
10	PC13_PR	Protection context 13, privileged read enable. Default Value: 1
9	PC13_UW	Protection context 13, user write enable. Default Value: 1
8	PC13_UR	Protection context 13, user read enable. Default Value: 1
4	PC12_NS	Protection context 12, non-secure. Default Value: 1
3	PC12_PW	Protection context 12, privileged write enable. Default Value: 1
2	PC12_PR	Protection context 12, privileged read enable. Default Value: 1
1	PC12_UW	Protection context 12, user write enable. Default Value: 1
0	PC12_UR	Protection context 12, user read enable. Default Value: 1

2.1.43 PERI_MS_PPU_PR1_MS_ADDR

Master region, base address

Address: 0x40010060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778241

2.1.44 PERI_MS_PPU_PR2_MS_ADDR

Master region, base address

Address: 0x400100A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778242

2.1.45 PERI_MS_PPU_PR3_MS_ADDR

Master region, base address

Address: 0x400100E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778243

2.1.46 PERI_MS_PPU_PR4_MS_ADDR

Master region, base address

Address: 0x40010120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778244

2.1.47 PERI_MS_PPU_PR5_MS_ADDR

Master region, base address

Address: 0x40010160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778245

2.1.48 PERI_MS_PPU_PR6_MS_ADDR

Master region, base address

Address: 0x400101A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778246

2.1.49 PERI_MS_PPU_PR7_MS_ADDR

Master region, base address

Address: 0x400101E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778247

2.1.50 PERI_MS_PPU_FX0_SL_ADDR

Slave region, base address

Address: 0x40010800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268435456

2.1.51 PERI_MS_PPU_FX0_SL_SIZE

Slave region, size

Address: 0x40010804

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None		R				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Slave region enable: '0': Disabled. A disabled region will never result in a match on the transfer address. '1': Enabled. Default Value: 1

2.1.51 PERI_MS_PPU_FX0_SL_SIZE (continued)

28 : 24	REGION_SIZE	This field specifies the size of the slave region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 12

2.1.52 PERI_MS_PPU_FX0_SL_ATT0

Slave attributes 0

Address: 0x40010810

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	R	R	R	R
HW Access	None			R	R	R	R	R
Name	None [7:5]			PC0_NS	PC0_PW	PC0_PR	PC0_UW	PC0_UR

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [15:13]			PC1_NS	PC1_PW	PC1_PR	PC1_UW	PC1_UR

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [23:21]			PC2_NS	PC2_PW	PC2_PR	PC2_UW	PC2_UR

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [31:29]			PC3_NS	PC3_PW	PC3_PR	PC3_UW	PC3_UR

Bits	Name	Description
28	PC3_NS	Protection context 3, non-secure. Default Value: 1
27	PC3_PW	Protection context 3, privileged write enable. Default Value: 1
26	PC3_PR	Protection context 3, privileged read enable. Default Value: 1
25	PC3_UW	Protection context 3, user write enable. Default Value: 1
24	PC3_UR	Protection context 3, user read enable. Default Value: 1
20	PC2_NS	Protection context 2, non-secure. Default Value: 1
19	PC2_PW	Protection context 2, privileged write enable. Default Value: 1
18	PC2_PR	Protection context 2, privileged read enable. Default Value: 1

2.1.52 PERI_MS_PPU_FX0_SL_ATT0 (continued)

17	PC2_UW	Protection context 2, user write enable. Default Value: 1
16	PC2_UR	Protection context 2, user read enable. Default Value: 1
12	PC1_NS	Protection context 1, non-secure. Default Value: 1
11	PC1_PW	Protection context 1, privileged write enable. Default Value: 1
10	PC1_PR	Protection context 1, privileged read enable. Default Value: 1
9	PC1_UW	Protection context 1, user write enable. Default Value: 1
8	PC1_UR	Protection context 1, user read enable. Default Value: 1
4	PC0_NS	Protection context 0, non-secure: '0': Secure (secure accesses allowed, non-secure access NOT allowed). '1': Non-secure (both secure and non-secure accesses allowed). Default Value: 1
3	PC0_PW	Protection context 0, privileged write enable: '0': Disabled (privileged, write accesses are NOT allowed). '1': Enabled (privileged, write accesses are allowed). Default Value: 1
2	PC0_PR	Protection context 0, privileged read enable: '0': Disabled (privileged, read accesses are NOT allowed). '1': Enabled (privileged, read accesses are allowed). Default Value: 1
1	PC0_UW	Protection context 0, user write enable: '0': Disabled (user, write accesses are NOT allowed). '1': Enabled (user, write accesses are allowed). Default Value: 1
0	PC0_UR	Protection context 0, user read enable: '0': Disabled (user, read accesses are NOT allowed). '1': Enabled (user, read accesses are allowed). Default Value: 1

2.1.53 PERI_MS_PPU_FX0_SL_ATT1

Slave attributes 1

Address: 0x40010814

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			PC4_NS	PC4_PW	PC4_PR	PC4_UW	PC4_UR

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [15:13]			PC5_NS	PC5_PW	PC5_PR	PC5_UW	PC5_UR

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [23:21]			PC6_NS	PC6_PW	PC6_PR	PC6_UW	PC6_UR

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [31:29]			PC7_NS	PC7_PW	PC7_PR	PC7_UW	PC7_UR

Bits	Name	Description
28	PC7_NS	Protection context 7, non-secure. Default Value: 1
27	PC7_PW	Protection context 7, privileged write enable. Default Value: 1
26	PC7_PR	Protection context 7, privileged read enable. Default Value: 1
25	PC7_UW	Protection context 7, user write enable. Default Value: 1
24	PC7_UR	Protection context 7, user read enable. Default Value: 1
20	PC6_NS	Protection context 6, non-secure. Default Value: 1
19	PC6_PW	Protection context 6, privileged write enable. Default Value: 1
18	PC6_PR	Protection context 6, privileged read enable. Default Value: 1

2.1.53 PERI_MS_PPU_FX0_SL_ATT1 (continued)

17	PC6_UW	Protection context 6, user write enable. Default Value: 1
16	PC6_UR	Protection context 6, user read enable. Default Value: 1
12	PC5_NS	Protection context 5, non-secure. Default Value: 1
11	PC5_PW	Protection context 5, privileged write enable. Default Value: 1
10	PC5_PR	Protection context 5, privileged read enable. Default Value: 1
9	PC5_UW	Protection context 5, user write enable. Default Value: 1
8	PC5_UR	Protection context 5, user read enable. Default Value: 1
4	PC4_NS	Protection context 4, non-secure. Default Value: 1
3	PC4_PW	Protection context 4, privileged write enable. Default Value: 1
2	PC4_PR	Protection context 4, privileged read enable. Default Value: 1
1	PC4_UW	Protection context 4, user write enable. Default Value: 1
0	PC4_UR	Protection context 4, user read enable. Default Value: 1

2.1.54 PERI_MS_PPU_FX0_SL_ATT2

Slave attributes 2

Address: 0x40010818

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			PC8_NS	PC8_PW	PC8_PR	PC8_UW	PC8_UR

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [15:13]			PC9_NS	PC9_PW	PC9_PR	PC9_UW	PC9_UR

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [23:21]			PC10_NS	PC10_PW	PC10_PR	PC10_UW	PC10_UR

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [31:29]			PC11_NS	PC11_PW	PC11_PR	PC11_UW	PC11_UR

Bits	Name	Description
28	PC11_NS	Protection context 11, non-secure. Default Value: 1
27	PC11_PW	Protection context 11, privileged write enable. Default Value: 1
26	PC11_PR	Protection context 11, privileged read enable. Default Value: 1
25	PC11_UW	Protection context 11, user write enable. Default Value: 1
24	PC11_UR	Protection context 11, user read enable. Default Value: 1
20	PC10_NS	Protection context 10, non-secure. Default Value: 1
19	PC10_PW	Protection context 10, privileged write enable. Default Value: 1
18	PC10_PR	Protection context 10, privileged read enable. Default Value: 1

2.1.54 PERI_MS_PPU_FX0_SL_ATT2 (continued)

17	PC10_UW	Protection context 10, user write enable. Default Value: 1
16	PC10_UR	Protection context 10, user read enable. Default Value: 1
12	PC9_NS	Protection context 9, non-secure. Default Value: 1
11	PC9_PW	Protection context 9, privileged write enable. Default Value: 1
10	PC9_PR	Protection context 9, privileged read enable. Default Value: 1
9	PC9_UW	Protection context 9, user write enable. Default Value: 1
8	PC9_UR	Protection context 9, user read enable. Default Value: 1
4	PC8_NS	Protection context 8, non-secure. Default Value: 1
3	PC8_PW	Protection context 8, privileged write enable. Default Value: 1
2	PC8_PR	Protection context 8, privileged read enable. Default Value: 1
1	PC8_UW	Protection context 8, user write enable. Default Value: 1
0	PC8_UR	Protection context 8, user read enable. Default Value: 1

2.1.55 PERI_MS_PPU_FX0_SL_ATT3

Slave attributes 3

Address: 0x4001081C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			PC12_NS	PC12_PW	PC12_PR	PC12_UW	PC12_UR

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [15:13]			PC13_NS	PC13_PW	PC13_PR	PC13_UW	PC13_UR

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [23:21]			PC14_NS	PC14_PW	PC14_PR	PC14_UW	PC14_UR

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [31:29]			PC15_NS	PC15_PW	PC15_PR	PC15_UW	PC15_UR

Bits	Name	Description
28	PC15_NS	Protection context 15, non-secure. Default Value: 1
27	PC15_PW	Protection context 15, privileged write enable. Default Value: 1
26	PC15_PR	Protection context 15, privileged read enable. Default Value: 1
25	PC15_UW	Protection context 15, user write enable. Default Value: 1
24	PC15_UR	Protection context 15, user read enable. Default Value: 1
20	PC14_NS	Protection context 14, non-secure. Default Value: 1
19	PC14_PW	Protection context 14, privileged write enable. Default Value: 1
18	PC14_PR	Protection context 14, privileged read enable. Default Value: 1

2.1.55 PERI_MS_PPU_FX0_SL_ATT3 (continued)

17	PC14_UW	Protection context 14, user write enable. Default Value: 1
16	PC14_UR	Protection context 14, user read enable. Default Value: 1
12	PC13_NS	Protection context 13, non-secure. Default Value: 1
11	PC13_PW	Protection context 13, privileged write enable. Default Value: 1
10	PC13_PR	Protection context 13, privileged read enable. Default Value: 1
9	PC13_UW	Protection context 13, user write enable. Default Value: 1
8	PC13_UR	Protection context 13, user read enable. Default Value: 1
4	PC12_NS	Protection context 12, non-secure. Default Value: 1
3	PC12_PW	Protection context 12, privileged write enable. Default Value: 1
2	PC12_PR	Protection context 12, privileged read enable. Default Value: 1
1	PC12_UW	Protection context 12, user write enable. Default Value: 1
0	PC12_UR	Protection context 12, user read enable. Default Value: 1

2.1.56 PERI_MS_PPU_FX0_MS_ADDR

Master region, base address

Address: 0x40010820

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778272

2.1.57 PERI_MS_PPU_FX0_MS_SIZE

Master region, size

Address: 0x40010824

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None		R				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Master region enable: '1': Enabled. Default Value: 1
28 : 24	REGION_SIZE	This field specifies the size of the master region: "5": 64 B region The master region includes the SL_ADDR, SL_SIZE, SL_ATT0, ..., SL_ATT3, MS_ADDR, MS_-SIZE, MS_ATT0, ..., MS_ATT3 registers. Therefore, the access privileges for all these registers is determined by MS_ATT0, ..., MS_ATT3. Default Value: 0x05

2.1.58 PERI_MS_PPU_FX0_MS_ATT0

Master attributes 0

Address: 0x40010830

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	R	R	R	R
HW Access	None			R	R	R	R	R
Name	None [7:5]			PC0_NS	PC0_PW	PC0_PR	PC0_UW	PC0_UR

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [15:13]			PC1_NS	PC1_PW	PC1_PR	PC1_UW	PC1_UR

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [23:21]			PC2_NS	PC2_PW	PC2_PR	PC2_UW	PC2_UR

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [31:29]			PC3_NS	PC3_PW	PC3_PR	PC3_UW	PC3_UR

Bits	Name	Description
28	PC3_NS	Protection context 3, non-secure. Default Value: 1
27	PC3_PW	Protection context 3, privileged write enable. Default Value: 1
26	PC3_PR	Protection context 3, privileged read enable. Default Value: 1
25	PC3_UW	Protection context 3, user write enable. Default Value: 1
24	PC3_UR	Protection context 3, user read enable. Default Value: 1
20	PC2_NS	Protection context 2, non-secure. Default Value: 1
19	PC2_PW	Protection context 2, privileged write enable. Default Value: 1
18	PC2_PR	Protection context 2, privileged read enable. Default Value: 1

2.1.58 PERI_MS_PPU_FX0_MS_ATT0 (continued)

17	PC2_UW	Protection context 2, user write enable. Default Value: 1
16	PC2_UR	Protection context 2, user read enable. Default Value: 1
12	PC1_NS	Protection context 1, non-secure. Default Value: 1
11	PC1_PW	Protection context 1, privileged write enable. Default Value: 1
10	PC1_PR	Protection context 1, privileged read enable. Default Value: 1
9	PC1_UW	Protection context 1, user write enable. Default Value: 1
8	PC1_UR	Protection context 1, user read enable. Default Value: 1
4	PC0_NS	Protection context 0, non-secure: '0': Secure (secure accesses allowed, non-secure access NOT allowed). '1': Non-secure (both secure and non-secure accesses allowed). Default Value: 1
3	PC0_PW	Protection context 0, privileged write enable: '0': Disabled (privileged, write accesses are NOT allowed). '1': Enabled (privileged, write accesses are allowed). Default Value: 1
2	PC0_PR	Protection context 0, privileged read enable: '0': Disabled (privileged, read accesses are NOT allowed). '1': Enabled (privileged, read accesses are allowed). Default Value: 1
1	PC0_UW	Protection context 0, user write enable: '0': Disabled (user, write accesses are NOT allowed). '1': Enabled (user, write accesses are allowed). Default Value: 1
0	PC0_UR	Protection context 0, user read enable: '0': Disabled (user, read accesses are NOT allowed). '1': Enabled (user, read accesses are allowed). Default Value: 1

2.1.59 PERI_MS_PPU_FX0_MS_ATT1

Master attributes 1

Address: 0x40010834

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [7:5]			PC4_NS	PC4_PW	PC4_PR	PC4_UW	PC4_UR

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [15:13]			PC5_NS	PC5_PW	PC5_PR	PC5_UW	PC5_UR

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [23:21]			PC6_NS	PC6_PW	PC6_PR	PC6_UW	PC6_UR

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [31:29]			PC7_NS	PC7_PW	PC7_PR	PC7_UW	PC7_UR

Bits	Name	Description
28	PC7_NS	Protection context 7, non-secure. Default Value: 1
27	PC7_PW	Protection context 7, privileged write enable. Default Value: 1
26	PC7_PR	Protection context 7, privileged read enable. Default Value: 1
25	PC7_UW	Protection context 7, user write enable. Default Value: 1
24	PC7_UR	Protection context 7, user read enable. Default Value: 1
20	PC6_NS	Protection context 6, non-secure. Default Value: 1
19	PC6_PW	Protection context 6, privileged write enable. Default Value: 1
18	PC6_PR	Protection context 6, privileged read enable. Default Value: 1

2.1.59 PERI_MS_PPU_FX0_MS_ATT1 (continued)

17	PC6_UW	Protection context 6, user write enable. Default Value: 1
16	PC6_UR	Protection context 6, user read enable. Default Value: 1
12	PC5_NS	Protection context 5, non-secure. Default Value: 1
11	PC5_PW	Protection context 5, privileged write enable. Default Value: 1
10	PC5_PR	Protection context 5, privileged read enable. Default Value: 1
9	PC5_UW	Protection context 5, user write enable. Default Value: 1
8	PC5_UR	Protection context 5, user read enable. Default Value: 1
4	PC4_NS	Protection context 4, non-secure. Default Value: 1
3	PC4_PW	Protection context 4, privileged write enable. Default Value: 1
2	PC4_PR	Protection context 4, privileged read enable. Default Value: 1
1	PC4_UW	Protection context 4, user write enable. Default Value: 1
0	PC4_UR	Protection context 4, user read enable. Default Value: 1

2.1.60 PERI_MS_PPU_FX0_MS_ATT2

Master attributes 2

Address: 0x40010838

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [7:5]			PC8_NS	PC8_PW	PC8_PR	PC8_UW	PC8_UR

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [15:13]			PC9_NS	PC9_PW	PC9_PR	PC9_UW	PC9_UR

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [23:21]			PC10_NS	PC10_PW	PC10_PR	PC10_UW	PC10_UR

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [31:29]			PC11_NS	PC11_PW	PC11_PR	PC11_UW	PC11_UR

Bits	Name	Description
28	PC11_NS	Protection context 11, non-secure. Default Value: 1
27	PC11_PW	Protection context 11, privileged write enable. Default Value: 1
26	PC11_PR	Protection context 11, privileged read enable. Default Value: 1
25	PC11_UW	Protection context 11, user write enable. Default Value: 1
24	PC11_UR	Protection context 11, user read enable. Default Value: 1
20	PC10_NS	Protection context 10, non-secure. Default Value: 1
19	PC10_PW	Protection context 10, privileged write enable. Default Value: 1
18	PC10_PR	Protection context 10, privileged read enable. Default Value: 1

2.1.60 PERI_MS_PPU_FX0_MS_ATT2 (continued)

17	PC10_UW	Protection context 10, user write enable. Default Value: 1
16	PC10_UR	Protection context 10, user read enable. Default Value: 1
12	PC9_NS	Protection context 9, non-secure. Default Value: 1
11	PC9_PW	Protection context 9, privileged write enable. Default Value: 1
10	PC9_PR	Protection context 9, privileged read enable. Default Value: 1
9	PC9_UW	Protection context 9, user write enable. Default Value: 1
8	PC9_UR	Protection context 9, user read enable. Default Value: 1
4	PC8_NS	Protection context 8, non-secure. Default Value: 1
3	PC8_PW	Protection context 8, privileged write enable. Default Value: 1
2	PC8_PR	Protection context 8, privileged read enable. Default Value: 1
1	PC8_UW	Protection context 8, user write enable. Default Value: 1
0	PC8_UR	Protection context 8, user read enable. Default Value: 1

2.1.61 PERI_MS_PPU_FX0_MS_ATT3

Master attributes 3

Address: 0x4001083C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [7:5]			PC12_NS	PC12_PW	PC12_PR	PC12_UW	PC12_UR

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [15:13]			PC13_NS	PC13_PW	PC13_PR	PC13_UW	PC13_UR

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [23:21]			PC14_NS	PC14_PW	PC14_PR	PC14_UW	PC14_UR

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	RW	R	RW	R
HW Access	None			R	R	R	R	R
Name	None [31:29]			PC15_NS	PC15_PW	PC15_PR	PC15_UW	PC15_UR

Bits	Name	Description
28	PC15_NS	Protection context 15, non-secure. Default Value: 1
27	PC15_PW	Protection context 15, privileged write enable. Default Value: 1
26	PC15_PR	Protection context 15, privileged read enable. Default Value: 1
25	PC15_UW	Protection context 15, user write enable. Default Value: 1
24	PC15_UR	Protection context 15, user read enable. Default Value: 1
20	PC14_NS	Protection context 14, non-secure. Default Value: 1
19	PC14_PW	Protection context 14, privileged write enable. Default Value: 1
18	PC14_PR	Protection context 14, privileged read enable. Default Value: 1

2.1.61 PERI_MS_PPU_FX0_MS_ATT3 (continued)

17	PC14_UW	Protection context 14, user write enable. Default Value: 1
16	PC14_UR	Protection context 14, user read enable. Default Value: 1
12	PC13_NS	Protection context 13, non-secure. Default Value: 1
11	PC13_PW	Protection context 13, privileged write enable. Default Value: 1
10	PC13_PR	Protection context 13, privileged read enable. Default Value: 1
9	PC13_UW	Protection context 13, user write enable. Default Value: 1
8	PC13_UR	Protection context 13, user read enable. Default Value: 1
4	PC12_NS	Protection context 12, non-secure. Default Value: 1
3	PC12_PW	Protection context 12, privileged write enable. Default Value: 1
2	PC12_PR	Protection context 12, privileged read enable. Default Value: 1
1	PC12_UW	Protection context 12, user write enable. Default Value: 1
0	PC12_UR	Protection context 12, user read enable. Default Value: 1

2.1.62 PERI_MS_PPU_FX1_SL_ADDR

Slave region, base address

Address: 0x40010840

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268439556

2.1.63 PERI_MS_PPU_FX1_SL_SIZE

Slave region, size

Address: 0x40010844

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None		R				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Slave region enable: '0': Disabled. A disabled region will never result in a match on the transfer address. '1': Enabled. Default Value: 1

2.1.63 PERI_MS_PPU_FX1_SL_SIZE (continued)

28 : 24	REGION_SIZE	This field specifies the size of the slave region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 1

2.1.64 PERI_MS_PPU_FX1_MS_ADDR

Master region, base address

Address: 0x40010860

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778273

2.1.65 PERI_MS_PPU_FX2_SL_ADDR

Slave region, base address

Address: 0x40010880

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268439564

2.1.66 PERI_MS_PPU_FX2_MS_ADDR

Master region, base address

Address: 0x400108A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778274

2.1.67 PERI_MS_PPU_FX3_SL_ADDR

Slave region, base address

Address: 0x400108C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268439572

2.1.68 PERI_MS_PPU_FX3_MS_ADDR

Master region, base address

Address: 0x400108E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778275

2.1.69 PERI_MS_PPU_FX4_SL_ADDR

Slave region, base address

Address: 0x40010900

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268439576

2.1.70 PERI_MS_PPU_FX4_SL_SIZE

Slave region, size

Address: 0x40010904

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None		R				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Slave region enable: '0': Disabled. A disabled region will never result in a match on the transfer address. '1': Enabled. Default Value: 1

2.1.70 PERI_MS_PPU_FX4_SL_SIZE (continued)

28 : 24	REGION_SIZE	This field specifies the size of the slave region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 4

2.1.71 PERI_MS_PPU_FX4_MS_ADDR

Master region, base address

Address: 0x40010920

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778276

2.1.72 PERI_MS_PPU_FX5_SL_ADDR

Slave region, base address

Address: 0x40010940

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268439584

2.1.73 PERI_MS_PPU_FX5_MS_ADDR

Master region, base address

Address: 0x40010960

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778277

2.1.74 PERI_MS_PPU_FX6_SL_ADDR

Slave region, base address

Address: 0x40010980

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268439592

2.1.75 PERI_MS_PPU_FX6_MS_ADDR

Master region, base address

Address: 0x400109A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778278

2.1.76 PERI_MS_PPU_FX7_SL_ADDR

Slave region, base address

Address: 0x400109C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268439600

2.1.77 PERI_MS_PPU_FX7_MS_ADDR

Master region, base address

Address: 0x400109E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778279

2.1.78 PERI_MS_PPU_FX8_SL_ADDR

Slave region, base address

Address: 0x40010A00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268439624

2.1.79 PERI_MS_PPU_FX8_MS_ADDR

Master region, base address

Address: 0x40010A20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778280

2.1.80 PERI_MS_PPU_FX9_SL_ADDR

Slave region, base address

Address: 0x40010A40

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268443648

2.1.81 PERI_MS_PPU_FX9_SL_SIZE

Slave region, size

Address: 0x40010A44

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None		R				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Slave region enable: '0': Disabled. A disabled region will never result in a match on the transfer address. '1': Enabled. Default Value: 1

2.1.81 PERI_MS_PPU_FX9_SL_SIZE (continued)

28 : 24	REGION_SIZE	This field specifies the size of the slave region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 14

2.1.82 PERI_MS_PPU_FX9_MS_ADDR

Master region, base address

Address: 0x40010A60

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778281

2.1.83 PERI_MS_PPU_FX10_SL_ADDR

Slave region, base address

Address: 0x40010A80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268697600

2.1.84 PERI_MS_PPU_FX10_SL_SIZE

Slave region, size

Address: 0x40010A84

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None		R				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Slave region enable: '0': Disabled. A disabled region will never result in a match on the transfer address. '1': Enabled. Default Value: 1

2.1.84 PERI_MS_PPU_FX10_SL_SIZE (continued)

28 : 24	REGION_SIZE	This field specifies the size of the slave region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 9

2.1.85 PERI_MS_PPU_FX10_MS_ADDR

Master region, base address

Address: 0x40010AA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778282

2.1.86 PERI_MS_PPU_FX11_SL_ADDR

Slave region, base address

Address: 0x40010AC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268698624

2.1.87 PERI_MS_PPU_FX11_SL_SIZE

Slave region, size

Address: 0x40010AC4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None		R				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Slave region enable: '0': Disabled. A disabled region will never result in a match on the transfer address. '1': Enabled. Default Value: 1

2.1.87 PERI_MS_PPU_FX11_SL_SIZE (continued)

28 : 24	REGION_SIZE	This field specifies the size of the slave region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 10

2.1.88 PERI_MS_PPU_FX11_MS_ADDR

Master region, base address

Address: 0x40010AE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778283

2.1.89 PERI_MS_PPU_FX12_SL_ADDR

Slave region, base address

Address: 0x40010B00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268699648

2.1.90 PERI_MS_PPU_FX12_SL_SIZE

Slave region, size

Address: 0x40010B04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None		R				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Slave region enable: '0': Disabled. A disabled region will never result in a match on the transfer address. '1': Enabled. Default Value: 1

2.1.90 PERI_MS_PPU_FX12_SL_SIZE (continued)

28 : 24	REGION_SIZE	This field specifies the size of the slave region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 7

2.1.91 PERI_MS_PPU_FX12_MS_ADDR

Master region, base address

Address: 0x40010B20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778284

2.1.92 PERI_MS_PPU_FX13_SL_ADDR

Slave region, base address

Address: 0x40010B40

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268699712

2.1.93 PERI_MS_PPU_FX13_MS_ADDR

Master region, base address

Address: 0x40010B60

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778285

2.1.94 PERI_MS_PPU_FX14_SL_ADDR

Slave region, base address

Address: 0x40010B80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268699720

2.1.95 PERI_MS_PPU_FX14_MS_ADDR

Master region, base address

Address: 0x40010BA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778286

2.1.96 PERI_MS_PPU_FX15_SL_ADDR

Slave region, base address

Address: 0x40010BC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268705792

2.1.97 PERI_MS_PPU_FX15_SL_SIZE

Slave region, size

Address: 0x40010BC4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None		R				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Slave region enable: '0': Disabled. A disabled region will never result in a match on the transfer address. '1': Enabled. Default Value: 1

2.1.97 PERI_MS_PPU_FX15_SL_SIZE (continued)

28 : 24	REGION_SIZE	This field specifies the size of the slave region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 11

2.1.98 PERI_MS_PPU_FX15_MS_ADDR

Master region, base address

Address: 0x40010BE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778287

2.1.99 PERI_MS_PPU_FX16_SL_ADDR

Slave region, base address

Address: 0x40010C00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268959744

2.1.100 PERI_MS_PPU_FX16_MS_ADDR

Master region, base address

Address: 0x40010C20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778288

2.1.101 PERI_MS_PPU_FX17_SL_ADDR

Slave region, base address

Address: 0x40010C40

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268960768

2.1.102 PERI_MS_PPU_FX17_MS_ADDR

Master region, base address

Address: 0x40010C60

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778289

2.1.103 PERI_MS_PPU_FX18_SL_ADDR

Slave region, base address

Address: 0x40010C80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268961792

2.1.104 PERI_MS_PPU_FX18_SL_SIZE

Slave region, size

Address: 0x40010C84

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None		R				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Slave region enable: '0': Disabled. A disabled region will never result in a match on the transfer address. '1': Enabled. Default Value: 1

2.1.104 PERI_MS_PPU_FX18_SL_SIZE (continued)

28 : 24	REGION_SIZE	This field specifies the size of the slave region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 8

2.1.105 PERI_MS_PPU_FX18_MS_ADDR

Master region, base address

Address: 0x40010CA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778290

2.1.106 PERI_MS_PPU_FX19_SL_ADDR

Slave region, base address

Address: 0x40010CC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268967936

2.1.107 PERI_MS_PPU_FX19_MS_ADDR

Master region, base address

Address: 0x40010CE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778291

2.1.108 PERI_MS_PPU_FX20_SL_ADDR

Slave region, base address

Address: 0x40010D00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268969984

2.1.109 PERI_MS_PPU_FX20_MS_ADDR

Master region, base address

Address: 0x40010D20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778292

2.1.110 PERI_MS_PPU_FX21_SL_ADDR

Slave region, base address

Address: 0x40010D40

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268976128

2.1.111 PERI_MS_PPU_FX21_MS_ADDR

Master region, base address

Address: 0x40010D60

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778293

2.1.112 PERI_MS_PPU_FX22_SL_ADDR

Slave region, base address

Address: 0x40010D80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268976192

2.1.113 PERI_MS_PPU_FX22_MS_ADDR

Master region, base address

Address: 0x40010DA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778294

2.1.114 PERI_MS_PPU_FX23_SL_ADDR

Slave region, base address

Address: 0x40010DC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268992512

2.1.115 PERI_MS_PPU_FX23_MS_ADDR

Master region, base address

Address: 0x40010DE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778295

2.1.116 PERI_MS_PPU_FX24_SL_ADDR

Slave region, base address

Address: 0x40010E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268992520

2.1.117 PERI_MS_PPU_FX24_MS_ADDR

Master region, base address

Address: 0x40010E20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778296

2.1.118 PERI_MS_PPU_FX25_SL_ADDR

Slave region, base address

Address: 0x40010E40

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268992528

2.1.119 PERI_MS_PPU_FX25_MS_ADDR

Master region, base address

Address: 0x40010E60

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778297

2.1.120 PERI_MS_PPU_FX26_SL_ADDR

Slave region, base address

Address: 0x40010E80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268992536

2.1.121 PERI_MS_PPU_FX26_MS_ADDR

Master region, base address

Address: 0x40010EA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778298

2.1.122 PERI_MS_PPU_FX27_SL_ADDR

Slave region, base address

Address: 0x40010EC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268992544

2.1.123 PERI_MS_PPU_FX27_MS_ADDR

Master region, base address

Address: 0x40010EE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778299

2.1.124 PERI_MS_PPU_FX28_SL_ADDR

Slave region, base address

Address: 0x40010F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268992552

2.1.125 PERI_MS_PPU_FX28_MS_ADDR

Master region, base address

Address: 0x40010F20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778300

2.1.126 PERI_MS_PPU_FX29_SL_ADDR

Slave region, base address

Address: 0x40010F40

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268992560

2.1.127 PERI_MS_PPU_FX29_MS_ADDR

Master region, base address

Address: 0x40010F60

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778301

2.1.128 PERI_MS_PPU_FX30_SL_ADDR

Slave region, base address

Address: 0x40010F80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268992568

2.1.129 PERI_MS_PPU_FX30_MS_ADDR

Master region, base address

Address: 0x40010FA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778302

2.1.130 PERI_MS_PPU_FX31_SL_ADDR

Slave region, base address

Address: 0x40010FC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268992576

2.1.131 PERI_MS_PPU_FX31_MS_ADDR

Master region, base address

Address: 0x40010FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778303

2.1.132 PERI_MS_PPU_FX32_SL_ADDR

Slave region, base address

Address: 0x40011000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268992584

2.1.133 PERI_MS_PPU_FX32_MS_ADDR

Master region, base address

Address: 0x40011020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778304

2.1.134 PERI_MS_PPU_FX33_SL_ADDR

Slave region, base address

Address: 0x40011040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268992592

2.1.135 PERI_MS_PPU_FX33_MS_ADDR

Master region, base address

Address: 0x40011060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778305

2.1.136 PERI_MS_PPU_FX34_SL_ADDR

Slave region, base address

Address: 0x40011080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268992600

2.1.137 PERI_MS_PPU_FX34_MS_ADDR

Master region, base address

Address: 0x400110A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778306

2.1.138 PERI_MS_PPU_FX35_SL_ADDR

Slave region, base address

Address: 0x400110C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268992608

2.1.139 PERI_MS_PPU_FX35_MS_ADDR

Master region, base address

Address: 0x400110E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778307

2.1.140 PERI_MS_PPU_FX36_SL_ADDR

Slave region, base address

Address: 0x40011100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268992616

2.1.141 PERI_MS_PPU_FX36_MS_ADDR

Master region, base address

Address: 0x40011120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778308

2.1.142 PERI_MS_PPU_FX37_SL_ADDR

Slave region, base address

Address: 0x40011140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268992624

2.1.143 PERI_MS_PPU_FX37_MS_ADDR

Master region, base address

Address: 0x40011160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778309

2.1.144 PERI_MS_PPU_FX38_SL_ADDR

Slave region, base address

Address: 0x40011180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268992632

2.1.145 PERI_MS_PPU_FX38_MS_ADDR

Master region, base address

Address: 0x400111A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778310

2.1.146 PERI_MS_PPU_FX39_SL_ADDR

Slave region, base address

Address: 0x400111C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268993536

2.1.147 PERI_MS_PPU_FX39_SL_SIZE

Slave region, size

Address: 0x400111C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None		R				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Slave region enable: '0': Disabled. A disabled region will never result in a match on the transfer address. '1': Enabled. Default Value: 1

2.1.147 PERI_MS_PPU_FX39_SL_SIZE (continued)

28 : 24	REGION_SIZE	This field specifies the size of the slave region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 3

2.1.148 PERI_MS_PPU_FX39_MS_ADDR

Master region, base address

Address: 0x400111E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778311

2.1.149 PERI_MS_PPU_FX40_SL_ADDR

Slave region, base address

Address: 0x40011200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268993544

2.1.150 PERI_MS_PPU_FX40_MS_ADDR

Master region, base address

Address: 0x40011220

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778312

2.1.151 PERI_MS_PPU_FX41_SL_ADDR

Slave region, base address

Address: 0x40011240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268993552

2.1.152 PERI_MS_PPU_FX41_MS_ADDR

Master region, base address

Address: 0x40011260

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778313

2.1.153 PERI_MS_PPU_FX42_SL_ADDR

Slave region, base address

Address: 0x40011280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268993560

2.1.154 PERI_MS_PPU_FX42_MS_ADDR

Master region, base address

Address: 0x400112A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778314

2.1.155 PERI_MS_PPU_FX43_SL_ADDR

Slave region, base address

Address: 0x400112C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268993568

2.1.156 PERI_MS_PPU_FX43_MS_ADDR

Master region, base address

Address: 0x400112E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778315

2.1.157 PERI_MS_PPU_FX44_SL_ADDR

Slave region, base address

Address: 0x40011300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268993576

2.1.158 PERI_MS_PPU_FX44_MS_ADDR

Master region, base address

Address: 0x40011320

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778316

2.1.159 PERI_MS_PPU_FX45_SL_ADDR

Slave region, base address

Address: 0x40011340

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268993584

2.1.160 PERI_MS_PPU_FX45_MS_ADDR

Master region, base address

Address: 0x40011360

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778317

2.1.161 PERI_MS_PPU_FX46_SL_ADDR

Slave region, base address

Address: 0x40011380

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268993592

2.1.162 PERI_MS_PPU_FX46_MS_ADDR

Master region, base address

Address: 0x400113A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778318

2.1.163 PERI_MS_PPU_FX47_SL_ADDR

Slave region, base address

Address: 0x400113C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268993600

2.1.164 PERI_MS_PPU_FX47_MS_ADDR

Master region, base address

Address: 0x400113E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778319

2.1.165 PERI_MS_PPU_FX48_SL_ADDR

Slave region, base address

Address: 0x40011400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268993608

2.1.166 PERI_MS_PPU_FX48_MS_ADDR

Master region, base address

Address: 0x40011420

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778320

2.1.167 PERI_MS_PPU_FX49_SL_ADDR

Slave region, base address

Address: 0x40011440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268993616

2.1.168 PERI_MS_PPU_FX49_MS_ADDR

Master region, base address

Address: 0x40011460

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778321

2.1.169 PERI_MS_PPU_FX50_SL_ADDR

Slave region, base address

Address: 0x40011480

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268993624

2.1.170 PERI_MS_PPU_FX50_MS_ADDR

Master region, base address

Address: 0x400114A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778322

2.1.171 PERI_MS_PPU_FX51_SL_ADDR

Slave region, base address

Address: 0x400114C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268993632

2.1.172 PERI_MS_PPU_FX51_MS_ADDR

Master region, base address

Address: 0x400114E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778323

2.1.173 PERI_MS_PPU_FX52_SL_ADDR

Slave region, base address

Address: 0x40011500

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268993640

2.1.174 PERI_MS_PPU_FX52_MS_ADDR

Master region, base address

Address: 0x40011520

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778324

2.1.175 PERI_MS_PPU_FX53_SL_ADDR

Slave region, base address

Address: 0x40011540

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268993648

2.1.176 PERI_MS_PPU_FX53_MS_ADDR

Master region, base address

Address: 0x40011560

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778325

2.1.177 PERI_MS_PPU_FX54_SL_ADDR

Slave region, base address

Address: 0x40011580

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 268993656

2.1.178 PERI_MS_PPU_FX54_MS_ADDR

Master region, base address

Address: 0x400115A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778326

2.1.179 PERI_MS_PPU_FX55_SL_ADDR

Slave region, base address

Address: 0x400115C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269008896

2.1.180 PERI_MS_PPU_FX55_SL_SIZE

Slave region, size

Address: 0x400115C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None		R				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Slave region enable: '0': Disabled. A disabled region will never result in a match on the transfer address. '1': Enabled. Default Value: 1

2.1.180 PERI_MS_PPU_FX55_SL_SIZE (continued)

28 : 24	REGION_SIZE	This field specifies the size of the slave region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 5

2.1.181 PERI_MS_PPU_FX55_MS_ADDR

Master region, base address

Address: 0x400115E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778327

2.1.182 PERI_MS_PPU_FX56_SL_ADDR

Slave region, base address

Address: 0x40011600

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269012992

2.1.183 PERI_MS_PPU_FX56_MS_ADDR

Master region, base address

Address: 0x40011620

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778328

2.1.184 PERI_MS_PPU_FX57_SL_ADDR

Slave region, base address

Address: 0x40011640

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269016576

2.1.185 PERI_MS_PPU_FX57_MS_ADDR

Master region, base address

Address: 0x40011660

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778329

2.1.186 PERI_MS_PPU_FX58_SL_ADDR

Slave region, base address

Address: 0x40011680

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269016832

2.1.187 PERI_MS_PPU_FX58_MS_ADDR

Master region, base address

Address: 0x400116A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778330

2.1.188 PERI_MS_PPU_FX59_SL_ADDR

Slave region, base address

Address: 0x400116C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269025280

2.1.189 PERI_MS_PPU_FX59_SL_SIZE

Slave region, size

Address: 0x400116C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None		R				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Slave region enable: '0': Disabled. A disabled region will never result in a match on the transfer address. '1': Enabled. Default Value: 1

2.1.189 PERI_MS_PPU_FX59_SL_SIZE (continued)

28 : 24	REGION_SIZE	This field specifies the size of the slave region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 2

2.1.190 PERI_MS_PPU_FX59_MS_ADDR

Master region, base address

Address: 0x400116E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778331

2.1.191 PERI_MS_PPU_FX60_SL_ADDR

Slave region, base address

Address: 0x40011700

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269025282

2.1.192 PERI_MS_PPU_FX60_MS_ADDR

Master region, base address

Address: 0x40011720

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778332

2.1.193 PERI_MS_PPU_FX61_SL_ADDR

Slave region, base address

Address: 0x40011740

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269025408

2.1.194 PERI_MS_PPU_FX61_MS_ADDR

Master region, base address

Address: 0x40011760

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778333

2.1.195 PERI_MS_PPU_FX62_SL_ADDR

Slave region, base address

Address: 0x40011780

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269025536

2.1.196 PERI_MS_PPU_FX62_SL_SIZE

Slave region, size

Address: 0x40011784

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None		R				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Slave region enable: '0': Disabled. A disabled region will never result in a match on the transfer address. '1': Enabled. Default Value: 1

2.1.196 PERI_MS_PPU_FX62_SL_SIZE (continued)

28 : 24	REGION_SIZE	This field specifies the size of the slave region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 6

2.1.197 PERI_MS_PPU_FX62_MS_ADDR

Master region, base address

Address: 0x400117A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778334

2.1.198 PERI_MS_PPU_FX63_SL_ADDR

Slave region, base address

Address: 0x400117C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269025568

2.1.199 PERI_MS_PPU_FX63_MS_ADDR

Master region, base address

Address: 0x400117E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778335

2.1.200 PERI_MS_PPU_FX64_SL_ADDR

Slave region, base address

Address: 0x40011800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269025600

2.1.201 PERI_MS_PPU_FX64_MS_ADDR

Master region, base address

Address: 0x40011820

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778336

2.1.202 PERI_MS_PPU_FX65_SL_ADDR

Slave region, base address

Address: 0x40011840

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269025632

2.1.203 PERI_MS_PPU_FX65_MS_ADDR

Master region, base address

Address: 0x40011860

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778337

2.1.204 PERI_MS_PPU_FX66_SL_ADDR

Slave region, base address

Address: 0x40011880

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269025664

2.1.205 PERI_MS_PPU_FX66_MS_ADDR

Master region, base address

Address: 0x400118A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778338

2.1.206 PERI_MS_PPU_FX67_SL_ADDR

Slave region, base address

Address: 0x400118C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269025696

2.1.207 PERI_MS_PPU_FX67_MS_ADDR

Master region, base address

Address: 0x400118E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778339

2.1.208 PERI_MS_PPU_FX68_SL_ADDR

Slave region, base address

Address: 0x40011900

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269040640

2.1.209 PERI_MS_PPU_FX68_MS_ADDR

Master region, base address

Address: 0x40011920

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778340

2.1.210 PERI_MS_PPU_FX69_SL_ADDR

Slave region, base address

Address: 0x40011940

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269058048

2.1.211 PERI_MS_PPU_FX69_MS_ADDR

Master region, base address

Address: 0x40011960

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778341

2.1.212 PERI_MS_PPU_FX70_SL_ADDR

Slave region, base address

Address: 0x40011980

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269058112

2.1.213 PERI_MS_PPU_FX70_MS_ADDR

Master region, base address

Address: 0x400119A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778342

2.1.214 PERI_MS_PPU_FX71_SL_ADDR

Slave region, base address

Address: 0x400119C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269058144

2.1.215 PERI_MS_PPU_FX71_MS_ADDR

Master region, base address

Address: 0x400119E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778343

2.1.216 PERI_MS_PPU_FX72_SL_ADDR

Slave region, base address

Address: 0x40011A00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269058176

2.1.217 PERI_MS_PPU_FX72_MS_ADDR

Master region, base address

Address: 0x40011A20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778344

2.1.218 PERI_MS_PPU_FX73_SL_ADDR

Slave region, base address

Address: 0x40011A40

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269058240

2.1.219 PERI_MS_PPU_FX73_MS_ADDR

Master region, base address

Address: 0x40011A60

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778345

2.1.220 PERI_MS_PPU_FX74_SL_ADDR

Slave region, base address

Address: 0x40011A80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269058304

2.1.221 PERI_MS_PPU_FX74_MS_ADDR

Master region, base address

Address: 0x40011AA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778346

2.1.222 PERI_MS_PPU_FX75_SL_ADDR

Slave region, base address

Address: 0x40011AC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269058560

2.1.223 PERI_MS_PPU_FX75_MS_ADDR

Master region, base address

Address: 0x40011AE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778347

2.1.224 PERI_MS_PPU_FX76_SL_ADDR

Slave region, base address

Address: 0x40011B00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269065216

2.1.225 PERI_MS_PPU_FX76_MS_ADDR

Master region, base address

Address: 0x40011B20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778348

2.1.226 PERI_MS_PPU_FX77_SL_ADDR

Slave region, base address

Address: 0x40011B40

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269074368

2.1.227 PERI_MS_PPU_FX77_MS_ADDR

Master region, base address

Address: 0x40011B60

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778349

2.1.228 PERI_MS_PPU_FX78_SL_ADDR

Slave region, base address

Address: 0x40011B80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269074432

2.1.229 PERI_MS_PPU_FX78_SL_SIZE

Slave region, size

Address: 0x40011B84

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None		R				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Slave region enable: '0': Disabled. A disabled region will never result in a match on the transfer address. '1': Enabled. Default Value: 1

2.1.229 PERI_MS_PPU_FX78_SL_SIZE (continued)

28 : 24	REGION_SIZE	This field specifies the size of the slave region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 15

2.1.230 PERI_MS_PPU_FX78_MS_ADDR

Master region, base address

Address: 0x40011BA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778350

2.1.231 PERI_MS_PPU_FX79_SL_ADDR

Slave region, base address

Address: 0x40011BC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269090816

2.1.232 PERI_MS_PPU_FX79_MS_ADDR

Master region, base address

Address: 0x40011BE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778351

2.1.233 PERI_MS_PPU_FX80_SL_ADDR

Slave region, base address

Address: 0x40011C00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269107200

2.1.234 PERI_MS_PPU_FX80_MS_ADDR

Master region, base address

Address: 0x40011C20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778352

2.1.235 PERI_MS_PPU_FX81_SL_ADDR

Slave region, base address

Address: 0x40011C40

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269090880

2.1.236 PERI_MS_PPU_FX81_MS_ADDR

Master region, base address

Address: 0x40011C60

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778353

2.1.237 PERI_MS_PPU_FX82_SL_ADDR

Slave region, base address

Address: 0x40011C80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269107264

2.1.238 PERI_MS_PPU_FX82_MS_ADDR

Master region, base address

Address: 0x40011CA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778354

2.1.239 PERI_MS_PPU_FX83_SL_ADDR

Slave region, base address

Address: 0x40011CC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099008

2.1.240 PERI_MS_PPU_FX83_MS_ADDR

Master region, base address

Address: 0x40011CE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778355

2.1.241 PERI_MS_PPU_FX84_SL_ADDR

Slave region, base address

Address: 0x40011D00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099024

2.1.242 PERI_MS_PPU_FX84_MS_ADDR

Master region, base address

Address: 0x40011D20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778356

2.1.243 PERI_MS_PPU_FX85_SL_ADDR

Slave region, base address

Address: 0x40011D40

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099040

2.1.244 PERI_MS_PPU_FX85_MS_ADDR

Master region, base address

Address: 0x40011D60

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778357

2.1.245 PERI_MS_PPU_FX86_SL_ADDR

Slave region, base address

Address: 0x40011D80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099056

2.1.246 PERI_MS_PPU_FX86_MS_ADDR

Master region, base address

Address: 0x40011DA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778358

2.1.247 PERI_MS_PPU_FX87_SL_ADDR

Slave region, base address

Address: 0x40011DC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099072

2.1.248 PERI_MS_PPU_FX87_MS_ADDR

Master region, base address

Address: 0x40011DE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778359

2.1.249 PERI_MS_PPU_FX88_SL_ADDR

Slave region, base address

Address: 0x40011E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099088

2.1.250 PERI_MS_PPU_FX88_MS_ADDR

Master region, base address

Address: 0x40011E20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778360

2.1.251 PERI_MS_PPU_FX89_SL_ADDR

Slave region, base address

Address: 0x40011E40

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099104

2.1.252 PERI_MS_PPU_FX89_MS_ADDR

Master region, base address

Address: 0x40011E60

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778361

2.1.253 PERI_MS_PPU_FX90_SL_ADDR

Slave region, base address

Address: 0x40011E80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099120

2.1.254 PERI_MS_PPU_FX90_MS_ADDR

Master region, base address

Address: 0x40011EA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778362

2.1.255 PERI_MS_PPU_FX91_SL_ADDR

Slave region, base address

Address: 0x40011EC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099136

2.1.256 PERI_MS_PPU_FX91_MS_ADDR

Master region, base address

Address: 0x40011EE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778363

2.1.257 PERI_MS_PPU_FX92_SL_ADDR

Slave region, base address

Address: 0x40011F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099152

2.1.258 PERI_MS_PPU_FX92_MS_ADDR

Master region, base address

Address: 0x40011F20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778364

2.1.259 PERI_MS_PPU_FX93_SL_ADDR

Slave region, base address

Address: 0x40011F40

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099168

2.1.260 PERI_MS_PPU_FX93_MS_ADDR

Master region, base address

Address: 0x40011F60

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778365

2.1.261 PERI_MS_PPU_FX94_SL_ADDR

Slave region, base address

Address: 0x40011F80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099184

2.1.262 PERI_MS_PPU_FX94_MS_ADDR

Master region, base address

Address: 0x40011FA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778366

2.1.263 PERI_MS_PPU_FX95_SL_ADDR

Slave region, base address

Address: 0x40011FC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099200

2.1.264 PERI_MS_PPU_FX95_MS_ADDR

Master region, base address

Address: 0x40011FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778367

2.1.265 PERI_MS_PPU_FX96_SL_ADDR

Slave region, base address

Address: 0x40012000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099216

2.1.266 PERI_MS_PPU_FX96_MS_ADDR

Master region, base address

Address: 0x40012020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778368

2.1.267 PERI_MS_PPU_FX97_SL_ADDR

Slave region, base address

Address: 0x40012040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099232

2.1.268 PERI_MS_PPU_FX97_MS_ADDR

Master region, base address

Address: 0x40012060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778369

2.1.269 PERI_MS_PPU_FX98_SL_ADDR

Slave region, base address

Address: 0x40012080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099248

2.1.270 PERI_MS_PPU_FX98_MS_ADDR

Master region, base address

Address: 0x400120A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778370

2.1.271 PERI_MS_PPU_FX99_SL_ADDR

Slave region, base address

Address: 0x400120C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099264

2.1.272 PERI_MS_PPU_FX99_MS_ADDR

Master region, base address

Address: 0x400120E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778371

2.1.273 PERI_MS_PPU_FX100_SL_ADDR

Slave region, base address

Address: 0x40012100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099280

2.1.274 PERI_MS_PPU_FX100_MS_ADDR

Master region, base address

Address: 0x40012120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778372

2.1.275 PERI_MS_PPU_FX101_SL_ADDR

Slave region, base address

Address: 0x40012140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099296

2.1.276 PERI_MS_PPU_FX101_MS_ADDR

Master region, base address

Address: 0x40012160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778373

2.1.277 PERI_MS_PPU_FX102_SL_ADDR

Slave region, base address

Address: 0x40012180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099312

2.1.278 PERI_MS_PPU_FX102_MS_ADDR

Master region, base address

Address: 0x400121A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778374

2.1.279 PERI_MS_PPU_FX103_SL_ADDR

Slave region, base address

Address: 0x400121C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099328

2.1.280 PERI_MS_PPU_FX103_MS_ADDR

Master region, base address

Address: 0x400121E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778375

2.1.281 PERI_MS_PPU_FX104_SL_ADDR

Slave region, base address

Address: 0x40012200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099344

2.1.282 PERI_MS_PPU_FX104_MS_ADDR

Master region, base address

Address: 0x40012220

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778376

2.1.283 PERI_MS_PPU_FX105_SL_ADDR

Slave region, base address

Address: 0x40012240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099360

2.1.284 PERI_MS_PPU_FX105_MS_ADDR

Master region, base address

Address: 0x40012260

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778377

2.1.285 PERI_MS_PPU_FX106_SL_ADDR

Slave region, base address

Address: 0x40012280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099376

2.1.286 PERI_MS_PPU_FX106_MS_ADDR

Master region, base address

Address: 0x400122A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778378

2.1.287 PERI_MS_PPU_FX107_SL_ADDR

Slave region, base address

Address: 0x400122C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099392

2.1.288 PERI_MS_PPU_FX107_MS_ADDR

Master region, base address

Address: 0x400122E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778379

2.1.289 PERI_MS_PPU_FX108_SL_ADDR

Slave region, base address

Address: 0x40012300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099408

2.1.290 PERI_MS_PPU_FX108_MS_ADDR

Master region, base address

Address: 0x40012320

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778380

2.1.291 PERI_MS_PPU_FX109_SL_ADDR

Slave region, base address

Address: 0x40012340

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099424

2.1.292 PERI_MS_PPU_FX109_MS_ADDR

Master region, base address

Address: 0x40012360

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778381

2.1.293 PERI_MS_PPU_FX110_SL_ADDR

Slave region, base address

Address: 0x40012380

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099440

2.1.294 PERI_MS_PPU_FX110_MS_ADDR

Master region, base address

Address: 0x400123A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778382

2.1.295 PERI_MS_PPU_FX111_SL_ADDR

Slave region, base address

Address: 0x400123C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099456

2.1.296 PERI_MS_PPU_FX111_MS_ADDR

Master region, base address

Address: 0x400123E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778383

2.1.297 PERI_MS_PPU_FX112_SL_ADDR

Slave region, base address

Address: 0x40012400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269099472

2.1.298 PERI_MS_PPU_FX112_MS_ADDR

Master region, base address

Address: 0x40012420

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778384

2.1.299 PERI_MS_PPU_FX113_SL_ADDR

Slave region, base address

Address: 0x40012440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115392

2.1.300 PERI_MS_PPU_FX113_MS_ADDR

Master region, base address

Address: 0x40012460

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778385

2.1.301 PERI_MS_PPU_FX114_SL_ADDR

Slave region, base address

Address: 0x40012480

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115408

2.1.302 PERI_MS_PPU_FX114_MS_ADDR

Master region, base address

Address: 0x400124A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778386

2.1.303 PERI_MS_PPU_FX115_SL_ADDR

Slave region, base address

Address: 0x400124C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115424

2.1.304 PERI_MS_PPU_FX115_MS_ADDR

Master region, base address

Address: 0x400124E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778387

2.1.305 PERI_MS_PPU_FX116_SL_ADDR

Slave region, base address

Address: 0x40012500

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115440

2.1.306 PERI_MS_PPU_FX116_MS_ADDR

Master region, base address

Address: 0x40012520

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778388

2.1.307 PERI_MS_PPU_FX117_SL_ADDR

Slave region, base address

Address: 0x40012540

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115456

2.1.308 PERI_MS_PPU_FX117_MS_ADDR

Master region, base address

Address: 0x40012560

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778389

2.1.309 PERI_MS_PPU_FX118_SL_ADDR

Slave region, base address

Address: 0x40012580

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115472

2.1.310 PERI_MS_PPU_FX118_MS_ADDR

Master region, base address

Address: 0x400125A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778390

2.1.311 PERI_MS_PPU_FX119_SL_ADDR

Slave region, base address

Address: 0x400125C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115488

2.1.312 PERI_MS_PPU_FX119_MS_ADDR

Master region, base address

Address: 0x400125E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778391

2.1.313 PERI_MS_PPU_FX120_SL_ADDR

Slave region, base address

Address: 0x40012600

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115504

2.1.314 PERI_MS_PPU_FX120_MS_ADDR

Master region, base address

Address: 0x40012620

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778392

2.1.315 PERI_MS_PPU_FX121_SL_ADDR

Slave region, base address

Address: 0x40012640

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115520

2.1.316 PERI_MS_PPU_FX121_MS_ADDR

Master region, base address

Address: 0x40012660

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778393

2.1.317 PERI_MS_PPU_FX122_SL_ADDR

Slave region, base address

Address: 0x40012680

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115536

2.1.318 PERI_MS_PPU_FX122_MS_ADDR

Master region, base address

Address: 0x400126A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778394

2.1.319 PERI_MS_PPU_FX123_SL_ADDR

Slave region, base address

Address: 0x400126C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115552

2.1.320 PERI_MS_PPU_FX123_MS_ADDR

Master region, base address

Address: 0x400126E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778395

2.1.321 PERI_MS_PPU_FX124_SL_ADDR

Slave region, base address

Address: 0x40012700

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115568

2.1.322 PERI_MS_PPU_FX124_MS_ADDR

Master region, base address

Address: 0x40012720

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778396

2.1.323 PERI_MS_PPU_FX125_SL_ADDR

Slave region, base address

Address: 0x40012740

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115584

2.1.324 PERI_MS_PPU_FX125_MS_ADDR

Master region, base address

Address: 0x40012760

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778397

2.1.325 PERI_MS_PPU_FX126_SL_ADDR

Slave region, base address

Address: 0x40012780

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115600

2.1.326 PERI_MS_PPU_FX126_MS_ADDR

Master region, base address

Address: 0x400127A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778398

2.1.327 PERI_MS_PPU_FX127_SL_ADDR

Slave region, base address

Address: 0x400127C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115616

2.1.328 PERI_MS_PPU_FX127_MS_ADDR

Master region, base address

Address: 0x400127E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778399

2.1.329 PERI_MS_PPU_FX128_SL_ADDR

Slave region, base address

Address: 0x40012800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115632

2.1.330 PERI_MS_PPU_FX128_MS_ADDR

Master region, base address

Address: 0x40012820

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778400

2.1.331 PERI_MS_PPU_FX129_SL_ADDR

Slave region, base address

Address: 0x40012840

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115648

2.1.332 PERI_MS_PPU_FX129_MS_ADDR

Master region, base address

Address: 0x40012860

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778401

2.1.333 PERI_MS_PPU_FX130_SL_ADDR

Slave region, base address

Address: 0x40012880

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115664

2.1.334 PERI_MS_PPU_FX130_MS_ADDR

Master region, base address

Address: 0x400128A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778402

2.1.335 PERI_MS_PPU_FX131_SL_ADDR

Slave region, base address

Address: 0x400128C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115680

2.1.336 PERI_MS_PPU_FX131_MS_ADDR

Master region, base address

Address: 0x400128E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778403

2.1.337 PERI_MS_PPU_FX132_SL_ADDR

Slave region, base address

Address: 0x40012900

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115696

2.1.338 PERI_MS_PPU_FX132_MS_ADDR

Master region, base address

Address: 0x40012920

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778404

2.1.339 PERI_MS_PPU_FX133_SL_ADDR

Slave region, base address

Address: 0x40012940

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115712

2.1.340 PERI_MS_PPU_FX133_MS_ADDR

Master region, base address

Address: 0x40012960

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778405

2.1.341 PERI_MS_PPU_FX134_SL_ADDR

Slave region, base address

Address: 0x40012980

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115728

2.1.342 PERI_MS_PPU_FX134_MS_ADDR

Master region, base address

Address: 0x400129A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778406

2.1.343 PERI_MS_PPU_FX135_SL_ADDR

Slave region, base address

Address: 0x400129C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115744

2.1.344 PERI_MS_PPU_FX135_MS_ADDR

Master region, base address

Address: 0x400129E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778407

2.1.345 PERI_MS_PPU_FX136_SL_ADDR

Slave region, base address

Address: 0x40012A00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115760

2.1.346 PERI_MS_PPU_FX136_MS_ADDR

Master region, base address

Address: 0x40012A20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778408

2.1.347 PERI_MS_PPU_FX137_SL_ADDR

Slave region, base address

Address: 0x40012A40

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115776

2.1.348 PERI_MS_PPU_FX137_MS_ADDR

Master region, base address

Address: 0x40012A60

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778409

2.1.349 PERI_MS_PPU_FX138_SL_ADDR

Slave region, base address

Address: 0x40012A80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115792

2.1.350 PERI_MS_PPU_FX138_MS_ADDR

Master region, base address

Address: 0x40012AA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778410

2.1.351 PERI_MS_PPU_FX139_SL_ADDR

Slave region, base address

Address: 0x40012AC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115808

2.1.352 PERI_MS_PPU_FX139_MS_ADDR

Master region, base address

Address: 0x40012AE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778411

2.1.353 PERI_MS_PPU_FX140_SL_ADDR

Slave region, base address

Address: 0x40012B00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115824

2.1.354 PERI_MS_PPU_FX140_MS_ADDR

Master region, base address

Address: 0x40012B20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778412

2.1.355 PERI_MS_PPU_FX141_SL_ADDR

Slave region, base address

Address: 0x40012B40

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115840

2.1.356 PERI_MS_PPU_FX141_MS_ADDR

Master region, base address

Address: 0x40012B60

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778413

2.1.357 PERI_MS_PPU_FX142_SL_ADDR

Slave region, base address

Address: 0x40012B80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115856

2.1.358 PERI_MS_PPU_FX142_MS_ADDR

Master region, base address

Address: 0x40012BA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778414

2.1.359 PERI_MS_PPU_FX143_SL_ADDR

Slave region, base address

Address: 0x40012BC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115872

2.1.360 PERI_MS_PPU_FX143_MS_ADDR

Master region, base address

Address: 0x40012BE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778415

2.1.361 PERI_MS_PPU_FX144_SL_ADDR

Slave region, base address

Address: 0x40012C00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269115888

2.1.362 PERI_MS_PPU_FX144_MS_ADDR

Master region, base address

Address: 0x40012C20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778416

2.1.363 PERI_MS_PPU_FX145_SL_ADDR

Slave region, base address

Address: 0x40012C40

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269123584

2.1.364 PERI_MS_PPU_FX145_MS_ADDR

Master region, base address

Address: 0x40012C60

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778417

2.1.365 PERI_MS_PPU_FX146_SL_ADDR

Slave region, base address

Address: 0x40012C80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269124608

2.1.366 PERI_MS_PPU_FX146_MS_ADDR

Master region, base address

Address: 0x40012CA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778418

2.1.367 PERI_MS_PPU_FX147_SL_ADDR

Slave region, base address

Address: 0x40012CC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269124672

2.1.368 PERI_MS_PPU_FX147_MS_ADDR

Master region, base address

Address: 0x40012CE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778419

2.1.369 PERI_MS_PPU_FX148_SL_ADDR

Slave region, base address

Address: 0x40012D00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269156352

2.1.370 PERI_MS_PPU_FX148_MS_ADDR

Master region, base address

Address: 0x40012D20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778420

2.1.371 PERI_MS_PPU_FX149_SL_ADDR

Slave region, base address

Address: 0x40012D40

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269156864

2.1.372 PERI_MS_PPU_FX149_MS_ADDR

Master region, base address

Address: 0x40012D60

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778421

2.1.373 PERI_MS_PPU_FX150_SL_ADDR

Slave region, base address

Address: 0x40012D80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221888

2.1.374 PERI_MS_PPU_FX150_MS_ADDR

Master region, base address

Address: 0x40012DA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778422

2.1.375 PERI_MS_PPU_FX151_SL_ADDR

Slave region, base address

Address: 0x40012DC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221892

2.1.376 PERI_MS_PPU_FX151_MS_ADDR

Master region, base address

Address: 0x40012DE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778423

2.1.377 PERI_MS_PPU_FX152_SL_ADDR

Slave region, base address

Address: 0x40012E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221896

2.1.378 PERI_MS_PPU_FX152_MS_ADDR

Master region, base address

Address: 0x40012E20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778424

2.1.379 PERI_MS_PPU_FX153_SL_ADDR

Slave region, base address

Address: 0x40012E40

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221900

2.1.380 PERI_MS_PPU_FX153_MS_ADDR

Master region, base address

Address: 0x40012E60

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778425

2.1.381 PERI_MS_PPU_FX154_SL_ADDR

Slave region, base address

Address: 0x40012E80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221904

2.1.382 PERI_MS_PPU_FX154_MS_ADDR

Master region, base address

Address: 0x40012EA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778426

2.1.383 PERI_MS_PPU_FX155_SL_ADDR

Slave region, base address

Address: 0x40012EC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221908

2.1.384 PERI_MS_PPU_FX155_MS_ADDR

Master region, base address

Address: 0x40012EE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778427

2.1.385 PERI_MS_PPU_FX156_SL_ADDR

Slave region, base address

Address: 0x40012F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221912

2.1.386 PERI_MS_PPU_FX156_MS_ADDR

Master region, base address

Address: 0x40012F20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778428

2.1.387 PERI_MS_PPU_FX157_SL_ADDR

Slave region, base address

Address: 0x40012F40

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221916

2.1.388 PERI_MS_PPU_FX157_MS_ADDR

Master region, base address

Address: 0x40012F60

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778429

2.1.389 PERI_MS_PPU_FX158_SL_ADDR

Slave region, base address

Address: 0x40012F80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221920

2.1.390 PERI_MS_PPU_FX158_MS_ADDR

Master region, base address

Address: 0x40012FA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778430

2.1.391 PERI_MS_PPU_FX159_SL_ADDR

Slave region, base address

Address: 0x40012FC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221924

2.1.392 PERI_MS_PPU_FX159_MS_ADDR

Master region, base address

Address: 0x40012FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778431

2.1.393 PERI_MS_PPU_FX160_SL_ADDR

Slave region, base address

Address: 0x40013000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221928

2.1.394 PERI_MS_PPU_FX160_MS_ADDR

Master region, base address

Address: 0x40013020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778432

2.1.395 PERI_MS_PPU_FX161_SL_ADDR

Slave region, base address

Address: 0x40013040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221932

2.1.396 PERI_MS_PPU_FX161_MS_ADDR

Master region, base address

Address: 0x40013060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778433

2.1.397 PERI_MS_PPU_FX162_SL_ADDR

Slave region, base address

Address: 0x40013080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221936

2.1.398 PERI_MS_PPU_FX162_MS_ADDR

Master region, base address

Address: 0x400130A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778434

2.1.399 PERI_MS_PPU_FX163_SL_ADDR

Slave region, base address

Address: 0x400130C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221940

2.1.400 PERI_MS_PPU_FX163_MS_ADDR

Master region, base address

Address: 0x400130E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778435

2.1.401 PERI_MS_PPU_FX164_SL_ADDR

Slave region, base address

Address: 0x40013100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269221944

2.1.402 PERI_MS_PPU_FX164_MS_ADDR

Master region, base address

Address: 0x40013120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778436

2.1.403 PERI_MS_PPU_FX165_SL_ADDR

Slave region, base address

Address: 0x40013140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269223936

2.1.404 PERI_MS_PPU_FX165_MS_ADDR

Master region, base address

Address: 0x40013160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778437

2.1.405 PERI_MS_PPU_FX166_SL_ADDR

Slave region, base address

Address: 0x40013180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269224064

2.1.406 PERI_MS_PPU_FX166_MS_ADDR

Master region, base address

Address: 0x400131A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778438

2.1.407 PERI_MS_PPU_FX167_SL_ADDR

Slave region, base address

Address: 0x400131C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238272

2.1.408 PERI_MS_PPU_FX167_MS_ADDR

Master region, base address

Address: 0x400131E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778439

2.1.409 PERI_MS_PPU_FX168_SL_ADDR

Slave region, base address

Address: 0x40013200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238304

2.1.410 PERI_MS_PPU_FX168_MS_ADDR

Master region, base address

Address: 0x40013220

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778440

2.1.411 PERI_MS_PPU_FX169_SL_ADDR

Slave region, base address

Address: 0x40013240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238336

2.1.412 PERI_MS_PPU_FX169_MS_ADDR

Master region, base address

Address: 0x40013260

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778441

2.1.413 PERI_MS_PPU_FX170_SL_ADDR

Slave region, base address

Address: 0x40013280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238368

2.1.414 PERI_MS_PPU_FX170_MS_ADDR

Master region, base address

Address: 0x400132A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778442

2.1.415 PERI_MS_PPU_FX171_SL_ADDR

Slave region, base address

Address: 0x400132C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238400

2.1.416 PERI_MS_PPU_FX171_MS_ADDR

Master region, base address

Address: 0x400132E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778443

2.1.417 PERI_MS_PPU_FX172_SL_ADDR

Slave region, base address

Address: 0x40013300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238432

2.1.418 PERI_MS_PPU_FX172_MS_ADDR

Master region, base address

Address: 0x40013320

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778444

2.1.419 PERI_MS_PPU_FX173_SL_ADDR

Slave region, base address

Address: 0x40013340

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238464

2.1.420 PERI_MS_PPU_FX173_MS_ADDR

Master region, base address

Address: 0x40013360

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778445

2.1.421 PERI_MS_PPU_FX174_SL_ADDR

Slave region, base address

Address: 0x40013380

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238496

2.1.422 PERI_MS_PPU_FX174_MS_ADDR

Master region, base address

Address: 0x400133A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778446

2.1.423 PERI_MS_PPU_FX175_SL_ADDR

Slave region, base address

Address: 0x400133C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238528

2.1.424 PERI_MS_PPU_FX175_MS_ADDR

Master region, base address

Address: 0x400133E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778447

2.1.425 PERI_MS_PPU_FX176_SL_ADDR

Slave region, base address

Address: 0x40013400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238560

2.1.426 PERI_MS_PPU_FX176_MS_ADDR

Master region, base address

Address: 0x40013420

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778448

2.1.427 PERI_MS_PPU_FX177_SL_ADDR

Slave region, base address

Address: 0x40013440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238592

2.1.428 PERI_MS_PPU_FX177_MS_ADDR

Master region, base address

Address: 0x40013460

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778449

2.1.429 PERI_MS_PPU_FX178_SL_ADDR

Slave region, base address

Address: 0x40013480

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238624

2.1.430 PERI_MS_PPU_FX178_MS_ADDR

Master region, base address

Address: 0x400134A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778450

2.1.431 PERI_MS_PPU_FX179_SL_ADDR

Slave region, base address

Address: 0x400134C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238656

2.1.432 PERI_MS_PPU_FX179_MS_ADDR

Master region, base address

Address: 0x400134E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778451

2.1.433 PERI_MS_PPU_FX180_SL_ADDR

Slave region, base address

Address: 0x40013500

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238688

2.1.434 PERI_MS_PPU_FX180_MS_ADDR

Master region, base address

Address: 0x40013520

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778452

2.1.435 PERI_MS_PPU_FX181_SL_ADDR

Slave region, base address

Address: 0x40013540

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238720

2.1.436 PERI_MS_PPU_FX181_MS_ADDR

Master region, base address

Address: 0x40013560

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778453

2.1.437 PERI_MS_PPU_FX182_SL_ADDR

Slave region, base address

Address: 0x40013580

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238288

2.1.438 PERI_MS_PPU_FX182_MS_ADDR

Master region, base address

Address: 0x400135A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778454

2.1.439 PERI_MS_PPU_FX183_SL_ADDR

Slave region, base address

Address: 0x400135C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238320

2.1.440 PERI_MS_PPU_FX183_MS_ADDR

Master region, base address

Address: 0x400135E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778455

2.1.441 PERI_MS_PPU_FX184_SL_ADDR

Slave region, base address

Address: 0x40013600

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238352

2.1.442 PERI_MS_PPU_FX184_MS_ADDR

Master region, base address

Address: 0x40013620

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778456

2.1.443 PERI_MS_PPU_FX185_SL_ADDR

Slave region, base address

Address: 0x40013640

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238384

2.1.444 PERI_MS_PPU_FX185_MS_ADDR

Master region, base address

Address: 0x40013660

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778457

2.1.445 PERI_MS_PPU_FX186_SL_ADDR

Slave region, base address

Address: 0x40013680

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238416

2.1.446 PERI_MS_PPU_FX186_MS_ADDR

Master region, base address

Address: 0x400136A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778458

2.1.447 PERI_MS_PPU_FX187_SL_ADDR

Slave region, base address

Address: 0x400136C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238448

2.1.448 PERI_MS_PPU_FX187_MS_ADDR

Master region, base address

Address: 0x400136E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778459

2.1.449 PERI_MS_PPU_FX188_SL_ADDR

Slave region, base address

Address: 0x40013700

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238480

2.1.450 PERI_MS_PPU_FX188_MS_ADDR

Master region, base address

Address: 0x40013720

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778460

2.1.451 PERI_MS_PPU_FX189_SL_ADDR

Slave region, base address

Address: 0x40013740

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238512

2.1.452 PERI_MS_PPU_FX189_MS_ADDR

Master region, base address

Address: 0x40013760

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778461

2.1.453 PERI_MS_PPU_FX190_SL_ADDR

Slave region, base address

Address: 0x40013780

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238544

2.1.454 PERI_MS_PPU_FX190_MS_ADDR

Master region, base address

Address: 0x400137A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778462

2.1.455 PERI_MS_PPU_FX191_SL_ADDR

Slave region, base address

Address: 0x400137C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238576

2.1.456 PERI_MS_PPU_FX191_MS_ADDR

Master region, base address

Address: 0x400137E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778463

2.1.457 PERI_MS_PPU_FX192_SL_ADDR

Slave region, base address

Address: 0x40013800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238608

2.1.458 PERI_MS_PPU_FX192_MS_ADDR

Master region, base address

Address: 0x40013820

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778464

2.1.459 PERI_MS_PPU_FX193_SL_ADDR

Slave region, base address

Address: 0x40013840

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238640

2.1.460 PERI_MS_PPU_FX193_MS_ADDR

Master region, base address

Address: 0x40013860

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778465

2.1.461 PERI_MS_PPU_FX194_SL_ADDR

Slave region, base address

Address: 0x40013880

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238672

2.1.462 PERI_MS_PPU_FX194_MS_ADDR

Master region, base address

Address: 0x400138A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778466

2.1.463 PERI_MS_PPU_FX195_SL_ADDR

Slave region, base address

Address: 0x400138C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238704

2.1.464 PERI_MS_PPU_FX195_MS_ADDR

Master region, base address

Address: 0x400138E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778467

2.1.465 PERI_MS_PPU_FX196_SL_ADDR

Slave region, base address

Address: 0x40013900

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269238736

2.1.466 PERI_MS_PPU_FX196_MS_ADDR

Master region, base address

Address: 0x40013920

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778468

2.1.467 PERI_MS_PPU_FX197_SL_ADDR

Slave region, base address

Address: 0x40013940

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269242368

2.1.468 PERI_MS_PPU_FX197_MS_ADDR

Master region, base address

Address: 0x40013960

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778469

2.1.469 PERI_MS_PPU_FX198_SL_ADDR

Slave region, base address

Address: 0x40013980

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269243392

2.1.470 PERI_MS_PPU_FX198_MS_ADDR

Master region, base address

Address: 0x400139A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778470

2.1.471 PERI_MS_PPU_FX199_SL_ADDR

Slave region, base address

Address: 0x400139C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269255232

2.1.472 PERI_MS_PPU_FX199_MS_ADDR

Master region, base address

Address: 0x400139E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778471

2.1.473 PERI_MS_PPU_FX200_SL_ADDR

Slave region, base address

Address: 0x40013A00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269303808

2.1.474 PERI_MS_PPU_FX200_MS_ADDR

Master region, base address

Address: 0x40013A20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778472

2.1.475 PERI_MS_PPU_FX201_SL_ADDR

Slave region, base address

Address: 0x40013A40

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269320192

2.1.476 PERI_MS_PPU_FX201_MS_ADDR

Master region, base address

Address: 0x40013A60

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778473

2.1.477 PERI_MS_PPU_FX202_SL_ADDR

Slave region, base address

Address: 0x40013A80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269352960

2.1.478 PERI_MS_PPU_FX202_MS_ADDR

Master region, base address

Address: 0x40013AA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778474

2.1.479 PERI_MS_PPU_FX203_SL_ADDR

Slave region, base address

Address: 0x40013AC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269352992

2.1.480 PERI_MS_PPU_FX203_MS_ADDR

Master region, base address

Address: 0x40013AE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778475

2.1.481 PERI_MS_PPU_FX204_SL_ADDR

Slave region, base address

Address: 0x40013B00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269353024

2.1.482 PERI_MS_PPU_FX204_MS_ADDR

Master region, base address

Address: 0x40013B20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778476

2.1.483 PERI_MS_PPU_FX205_SL_ADDR

Slave region, base address

Address: 0x40013B40

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269353056

2.1.484 PERI_MS_PPU_FX205_MS_ADDR

Master region, base address

Address: 0x40013B60

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778477

2.1.485 PERI_MS_PPU_FX206_SL_ADDR

Slave region, base address

Address: 0x40013B80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269361152

2.1.486 PERI_MS_PPU_FX206_MS_ADDR

Master region, base address

Address: 0x40013BA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778478

2.1.487 PERI_MS_PPU_FX207_SL_ADDR

Slave region, base address

Address: 0x40013BC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269361184

2.1.488 PERI_MS_PPU_FX207_MS_ADDR

Master region, base address

Address: 0x40013BE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778479

2.1.489 PERI_MS_PPU_FX208_SL_ADDR

Slave region, base address

Address: 0x40013C00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269361216

2.1.490 PERI_MS_PPU_FX208_MS_ADDR

Master region, base address

Address: 0x40013C20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778480

2.1.491 PERI_MS_PPU_FX209_SL_ADDR

Slave region, base address

Address: 0x40013C40

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269361248

2.1.492 PERI_MS_PPU_FX209_MS_ADDR

Master region, base address

Address: 0x40013C60

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778481

2.1.493 PERI_MS_PPU_FX210_SL_ADDR

Slave region, base address

Address: 0x40013C80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269361280

2.1.494 PERI_MS_PPU_FX210_MS_ADDR

Master region, base address

Address: 0x40013CA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778482

2.1.495 PERI_MS_PPU_FX211_SL_ADDR

Slave region, base address

Address: 0x40013CC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269361312

2.1.496 PERI_MS_PPU_FX211_MS_ADDR

Master region, base address

Address: 0x40013CE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778483

2.1.497 PERI_MS_PPU_FX212_SL_ADDR

Slave region, base address

Address: 0x40013D00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269361344

2.1.498 PERI_MS_PPU_FX212_MS_ADDR

Master region, base address

Address: 0x40013D20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778484

2.1.499 PERI_MS_PPU_FX213_SL_ADDR

Slave region, base address

Address: 0x40013D40

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269361376

2.1.500 PERI_MS_PPU_FX213_MS_ADDR

Master region, base address

Address: 0x40013D60

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778485

2.1.501 PERI_MS_PPU_FX214_SL_ADDR

Slave region, base address

Address: 0x40013D80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269402112

2.1.502 PERI_MS_PPU_FX214_MS_ADDR

Master region, base address

Address: 0x40013DA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778486

2.1.503 PERI_MS_PPU_FX215_SL_ADDR

Slave region, base address

Address: 0x40013DC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269467648

2.1.504 PERI_MS_PPU_FX215_MS_ADDR

Master region, base address

Address: 0x40013DE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778487

2.1.505 PERI_MS_PPU_FX216_SL_ADDR

Slave region, base address

Address: 0x40013E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269516800

2.1.506 PERI_MS_PPU_FX216_MS_ADDR

Master region, base address

Address: 0x40013E20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778488

2.1.507 PERI_MS_PPU_FX217_SL_ADDR

Slave region, base address

Address: 0x40013E40

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269778944

2.1.508 PERI_MS_PPU_FX217_MS_ADDR

Master region, base address

Address: 0x40013E60

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778489

2.1.509 PERI_MS_PPU_FX218_SL_ADDR

Slave region, base address

Address: 0x40013E80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269779968

2.1.510 PERI_MS_PPU_FX218_MS_ADDR

Master region, base address

Address: 0x40013EA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778490

2.1.511 PERI_MS_PPU_FX219_SL_ADDR

Slave region, base address

Address: 0x40013EC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 269795328

2.1.512 PERI_MS_PPU_FX219_MS_ADDR

Master region, base address

Address: 0x40013EE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778491

2.1.513 PERI_MS_PPU_FX220_SL_ADDR

Slave region, base address

Address: 0x40013F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270008320

2.1.514 PERI_MS_PPU_FX220_MS_ADDR

Master region, base address

Address: 0x40013F20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778492

2.1.515 PERI_MS_PPU_FX221_SL_ADDR

Slave region, base address

Address: 0x40013F40

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270024704

2.1.516 PERI_MS_PPU_FX221_MS_ADDR

Master region, base address

Address: 0x40013F60

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778493

2.1.517 PERI_MS_PPU_FX222_SL_ADDR

Slave region, base address

Address: 0x40013F80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270041088

2.1.518 PERI_MS_PPU_FX222_MS_ADDR

Master region, base address

Address: 0x40013FA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778494

2.1.519 PERI_MS_PPU_FX223_SL_ADDR

Slave region, base address

Address: 0x40013FC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270073856

2.1.520 PERI_MS_PPU_FX223_MS_ADDR

Master region, base address

Address: 0x40013FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778495

2.1.521 PERI_MS_PPU_FX224_SL_ADDR

Slave region, base address

Address: 0x40014000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270090240

2.1.522 PERI_MS_PPU_FX224_MS_ADDR

Master region, base address

Address: 0x40014020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778496

2.1.523 PERI_MS_PPU_FX225_SL_ADDR

Slave region, base address

Address: 0x40014040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270106624

2.1.524 PERI_MS_PPU_FX225_MS_ADDR

Master region, base address

Address: 0x40014060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778497

2.1.525 PERI_MS_PPU_FX226_SL_ADDR

Slave region, base address

Address: 0x40014080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	R						None	
Name	ADDR30 [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR30 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR30 [31:24]							

Bits	Name	Description
31 : 2	ADDR30	This field specifies the base address of the slave region. The region size is defined by SL_-SIZE.REGION_SIZE. A region of n Bytes must be n Byte aligned. Therefore, some of the lesser significant address bits of ADDR30 must be '0's. E.g., a 64 KB address region (REGION_SIZE is "15") must be 64 KByte aligned, and ADDR30[13:0] must be '0's. Default Value: 270794752

2.1.526 PERI_MS_PPU_FX226_SL_SIZE

Slave region, size

Address: 0x40014084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None		R				
HW Access	R	None		R				
Name	VALID	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	VALID	Slave region enable: '0': Disabled. A disabled region will never result in a match on the transfer address. '1': Enabled. Default Value: 1

2.1.526 PERI_MS_PPU_FX226_SL_SIZE (continued)

28 : 24	REGION_SIZE	This field specifies the size of the slave region: "0": Undefined. "1": 4 B region (this is the smallest region size). "2": 8 B region "3": 16 B region "4": 32 B region "5": 64 B region "6": 128 B region "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: 19

2.1.527 PERI_MS_PPU_FX226_MS_ADDR

Master region, base address

Address: 0x400140A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		None					
HW Access	R		None					
Name	ADDR26 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR26 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR26 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR26 [31:24]							

Bits	Name	Description
31 : 6	ADDR26	This field specifies the base address of the master region. The base address of the region is the address of the SL_ADDR register. Default Value: 16778498

Section C: Peripheral Group 1

This section encompasses the following chapters:

- Cryptography Registers chapter on page 653

3 Cryptography Registers

This section discusses the Cryptography Registers (CRYPTO) registers. It lists all the registers in mapping tables, in address order.

3.1 Register Details

Register	Address	Description
CRYPTO_CTL	0x40100000	Control
CRYPTO_RAM_PWR_CTL	0x40100008	SRAM power control
CRYPTO_RAM_PWR_DELAY_CTL	0x4010000C	SRAM power delay control
CRYPTO_ERROR_STATUS0	0x40100020	Error status 0
CRYPTO_ERROR_STATUS1	0x40100024	Error status 1
CRYPTO_INTR	0x40100100	Interrupt register
CRYPTO_INTR_SET	0x40100104	Interrupt set register
CRYPTO_INTR_MASK	0x40100108	Interrupt mask register
CRYPTO_INTR_MASKED	0x4010010C	Interrupt masked register
CRYPTO_PR_LFSR_CTL0	0x40100200	Pseudo random LFSR control 0
CRYPTO_PR_LFSR_CTL1	0x40100204	Pseudo random LFSR control 1
CRYPTO_PR_LFSR_CTL2	0x40100208	Pseudo random LFSR control 2
CRYPTO_PR_MAX_CTL	0x4010020C	Pseudo random maximum control
CRYPTO_PR_CMD	0x40100210	Pseudo random command
CRYPTO_PR_RESULT	0x40100218	Pseudo random result
CRYPTO_TR_CTL0	0x40100280	True random control 0
CRYPTO_TR_CTL1	0x40100284	True random control 1
CRYPTO_TR_CTL2	0x40100288	True random control 2
CRYPTO_TR_STATUS	0x4010028C	True random status
CRYPTO_TR_CMD	0x40100290	True random command
CRYPTO_TR_RESULT	0x40100298	True random result
CRYPTO_TR_GARO_CTL	0x401002A0	True random GARO control
CRYPTO_TR_FIRO_CTL	0x401002A4	True random FIRO control
CRYPTO_TR_MON_CTL	0x401002C0	True random monitor control
CRYPTO_TR_MON_CMD	0x401002C8	True random monitor command
CRYPTO_TR_MON_RC_CTL	0x401002D0	True random monitor RC control

Register	Address	Description
CRYPTO_TR_MON_RC_STATUS0	0x401002D8	True random monitor RC status 0
CRYPTO_TR_MON_RC_STATUS1	0x401002DC	True random monitor RC status 1
CRYPTO_TR_MON_AP_CTL	0x401002E0	True random monitor AP control
CRYPTO_TR_MON_AP_STATUS0	0x401002E8	True random monitor AP status 0
CRYPTO_TR_MON_AP_STATUS1	0x401002EC	True random monitor AP status 1
CRYPTO_STATUS	0x40101004	Status
CRYPTO_INSTR_FF_CTL	0x40101040	Instruction FIFO control
CRYPTO_INSTR_FF_STATUS	0x40101044	Instruction FIFO status
CRYPTO_INSTR_FF_WR	0x40101048	Instruction FIFO write
CRYPTO_LOAD0_FF_STATUS	0x401010C0	Load 0 FIFO status
CRYPTO_LOAD1_FF_STATUS	0x401010D0	Load 1 FIFO status
CRYPTO_STORE_FF_STATUS	0x401010F0	Store FIFO status
CRYPTO_AES_CTL	0x40101100	AES control
CRYPTO_RESULT	0x40101180	Result
CRYPTO_CRC_CTL	0x40101400	CRC control
CRYPTO_CRC_DATA_CTL	0x40101410	CRC data control
CRYPTO_CRC_POL_CTL	0x40101420	CRC polynomial control
CRYPTO_CRC_REM_CTL	0x40101440	CRC remainder control
CRYPTO_CRC_REM_RESULT	0x40101448	CRC remainder result
CRYPTO_VU_CTL0	0x40101480	Vector unit control 0
CRYPTO_VU_CTL1	0x40101484	Vector unit control 1
CRYPTO_VU_CTL2	0x40101488	Vector unit control 2
CRYPTO_VU_STATUS	0x40101490	Vector unit status
CRYPTO_VU_RF_DATA0	0x401014C0	Vector unit register-file
CRYPTO_VU_RF_DATA1	0x401014C4	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA2	0x401014C8	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA3	0x401014CC	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA4	0x401014D0	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA5	0x401014D4	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA6	0x401014D8	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA7	0x401014DC	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA8	0x401014E0	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA9	0x401014E4	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA10	0x401014E8	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA11	0x401014EC	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA12	0x401014F0	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA13	0x401014F4	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA14	0x401014F8	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_VU_RF_DATA15	0x401014FC	Vector unit register-file. See CRYPTO_VU_RF_DATA0 for the details of bit fields.
CRYPTO_DEV_KEY_ADDR0_CTL	0x40102000	Device key address 0 control
CRYPTO_DEV_KEY_ADDR0	0x40102004	Device key address 0
CRYPTO_DEV_KEY_ADDR1_CTL	0x40102020	Device key address 1 control

Register	Address	Description
CRYPTO_DEV_KEY_ADDR1	0x40102024	Device key address 1 control
CRYPTO_DEV_KEY_STATUS	0x40102080	Device key status
CRYPTO_DEV_KEY_CTL0	0x40102100	Device key control 0
CRYPTO_DEV_KEY_CTL1	0x40102120	Device key control 1
CRYPTO_MEM_BUFF0	0x40108000	Memory buffer. This is the starting address of a register bank containing 1024 registers (CRYPTO_MEM_BUFF0 to CRYPTO_MEM_BUFF1023).

3.1.1 CRYPTO_CTL

Control

Address: 0x40100000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				None		RW	RW
HW Access	R				None		R	R
Name	PC [7:4]				None [3:2]		NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	IP enable: '0': Disabled. All non-retention registers (command and status registers, instruct FIFO, internal component state machines) are reset to their default value when the IP is disabled. All retention registers retain their value when the IP is disabled. '1': Enabled. When the IP is enabled, the IP register buffer is set to "0". Default Value: 0 **0x0: DISABLED :** **0x1: ENABLED :**
7 : 4	PC	Protection context. This field is set with the protection context of the transaction that writes this register; i.e. the context is inherited from the write transaction and not specified by the transaction write data. All IP master transactions use the PC field for the protection context. There is one exception: the LOAD_DEV_KEY instruction IP master transactions are always performed with protection context "0". Default Value: 0

3.1.1 CRYPTO_CTL (continued)

1	NS	Secure/on-secure access control: '0': secure. '1': non-secure. This field is set with the secure/non-secure access control of the transaction that writes this register; i.e. the access control is inherited from the write transaction and not specified by the transaction write data. All IP master transactions use the NS field for the secure/non-secure access control ("hprot[4]"). Default Value: 1
0	P	User/privileged access control: '0': user mode. '1': privileged mode. This field is set with the user/privileged access control of the transaction that writes this register; i.e. the access control is inherited from the write transaction and not specified by the transaction write data. All IP master transactions use the P field for the user/privileged access control ("hprot[1]"). Default Value: 0

3.1.2 CRYPTO_RAM_PWR_CTL

SRAM power control

Address: 0x40100008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	PWR_MODE	Set power mode for memory buffer SRAM. Default Value: 3 **0x0: OFF :** See CM4_PWR_CTL **0x1: RESERVED :** undefined **0x2: RETAINED :** See CM4_PWR_CTL **0x3: ENABLED :** See CM4_PWR_CTL

3.1.3 CRYPTO_RAM_PWR_DELAY_CTL

SRAM power delay control

Address: 0x4010000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	UP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						UP [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	UP	Number clock cycles delay needed after power domain power up Default Value: 150

3.1.4 CRYPTO_ERROR_STATUS0

Error status 0

Address: 0x40100020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Specifies error description information. - For INSTR_OPC_ERROR/ INSTR_CC_ERROR/ INSTR_DEV_KEY_ERROR: - Violating instruction (from instruction FIFO). - For BUS_ERROR: - Violating transfer, address. Default Value: Undefined

3.1.5 CRYPTO_ERROR_STATUS1

Error status 1

Address: 0x40100024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	DATA24 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	DATA24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	DATA24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None				R		
HW Access	RW	None				RW		
Name	VALID	None [30:27]				IDX [26:24]		

Bits	Name	Description
31	VALID	Specifies if ERROR_STATUS0 and ERROR_STATUS1 specify valid error information. No new error information is captured as long as VALID is '1'; i.e. the error information of the first detected error is NOT overwritten. Default Value: 0
26 : 24	IDX	Error source: "0": INSTR_OPC_ERROR (instruction FIFO decoder error). "1": INSTR_CC_ERROR (instruction FIFO decoder, VU CC error). "2": BUS_ERROR (bus master interface AHB-Lite bus error). "3": TR_AP_DETECT_ERROR. "4": TR_RC_DETECT_ERROR. "5": INSTR_DEV_KEY_ERROR. "6"-"7": Undefined. Default Value: Undefined
23 : 0	DATA24	Specifies error description information. - For BUS_ERROR: - Violating transfer, read attribute (DATA[0]). - Violating transfer, size attribute (DATA[5:4]). "0": 8-bit transfer, "1": 16 bits transfer, "2": 32-bit transfer. Default Value: Undefined

3.1.6 CRYPTO_INTR

Interrupt register

Address: 0x40100100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None			RW1S	RW1S	RW1S	RW1S	RW1S
Name	None [7:5]			PR_-DATA_AVAILABLE	TR_-DATA_AVAILABLE	TR_INITIALIZED	INSTR_FF_OVERFLOW	INSTR_FF_LEVEL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None		RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	None [23:22]		INSTR_DEV_KEY_ERROR	TR_RC_-DETECT_ERROR	TR_AP_DETECT_ERROR	BUS_ERROR	INSTR_CC_ERROR	INSTR_OPC_ERROR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	INSTR_DEV_KEY_ERROR	This interrupt cause is activated (HW sets the field to '1') when the LOAD_DEV_KEY instruction tries to load a device key whose DEV_KEY_ADDR_CTL.VALID or DEV_KEY_CTL.ALLOWED is set to '0'. Default Value: 0
20	TR_RC_DETECT_ERROR	This interrupt cause is activated (HW sets the field to '1') when the true random number generator monitor adaptive proportion test detects a disproportionate occurrence of a specific bit value. Default Value: 0
19	TR_AP_DETECT_ERROR	This interrupt cause is activated (HW sets the field to '1') when the true random number generator monitor adaptive proportion test detects a repetition of a specific bit value. Default Value: 0

3.1.6 CRYPTO_INTR (continued)

18	BUS_ERROR	This interrupt cause is activated (HW sets the field to '1') when a AHB-Lite bus error is observed on the AHB-Lite master interface. When the interrupt cause is activated, HW sets INSTR_FF_CTL.CLEAR to '1'. Default Value: 0
17	INSTR_CC_ERROR	This interrupt cause is activated (HW sets the field to '1') when the instruction decoder encounters an instruction with a non-defined condition code. This error is only generated for VU instructions. When the interrupt cause is activated, HW sets INSTR_FF_CTL.CLEAR to '1'. Default Value: 0
16	INSTR_OPC_ERROR	This interrupt cause is activated (HW sets the field to '1') when the instruction decoder encounters an instruction with a non-defined operation code (opcode). When the interrupt cause is activated, HW sets INSTR_FF_CTL.CLEAR to '1'. Default Value: 0
4	PR_DATA_AVAILABLE	This interrupt cause is activated (HW sets the field to '1') when the pseudo random number generator has generated a data value. Default Value: 0
3	TR_DATA_AVAILABLE	This interrupt cause is activated (HW sets the field to '1') when the true random number generator has generated a data value of the specified bit size. Default Value: 0
2	TR_INITIALIZED	This interrupt cause is activated (HW sets the field to '1') when the true random number generator is initialized. Default Value: 0
1	INSTR_FF_OVERFLOW	This interrupt cause is activated (HW sets the field to '1') when the instruction FIFO overflows (an attempt is made to write to a full FIFO). Default Value: 0
0	INSTR_FF_LEVEL	This interrupt cause is activated (HW sets the field to '1') when the instruction FIFO event is activated. Default Value: 0

3.1.7 CRYPTO_INTR_SET

Interrupt set register

Address: 0x40100104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	None			A	A	A	A	A
Name	None [7:5]			PR_-DATA_AVAILABLE	TR_-DATA_AVAILABLE	TR_INI-TIALIZED	IN-STR_FF_OVERFLOW	IN-STR_FF_LEVEL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	None		A	A	A	A	A	A
Name	None [23:22]		IN-STR_DEV_KEY_ER-ROR	TR_RC_-DE-TECT_ERROR	TR_AP_DE-TECT_ER-ROR	BUS_ER-ROR	INSTR_C-C_ERROR	INSTR_OP-C_ERROR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	INSTR_DEV_KEY_ER-ROR	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
20	TR_RC_DETECT_ER-ROR	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
19	TR_AP_DETECT_ER-ROR	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
18	BUS_ERROR	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
17	INSTR_CC_ERROR	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
16	INSTR_OPC_ERROR	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0

3.1.7 CRYPTO_INTR_SET (continued)

4	PR_DATA_AVAILABLE	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
3	TR_DATA_AVAILABLE	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
2	TR_INITIALIZED	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
1	INSTR_FF_OVERFLOW	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
0	INSTR_FF_LEVEL	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0

3.1.8 CRYPTO_INTR_MASK

Interrupt mask register

Address: 0x40100108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			PR_DATA_AVAILABLE	TR_DATA_AVAILABLE	TR_INITIALIZED	INSTR_FF_OVERFLOW	INSTR_FF_LEVEL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [23:22]		INSTR_DEV_KEY_ERROR	TR_RC_DETECT_ERROR	TR_AP_DETECT_ERROR	BUS_ERROR	INSTR_CC_ERROR	INSTR_OPC_ERROR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	INSTR_DEV_KEY_ERROR	Mask bit for corresponding field in interrupt request register. Default Value: 0
20	TR_RC_DETECT_ERROR	Mask bit for corresponding field in interrupt request register. Default Value: 0
19	TR_AP_DETECT_ERROR	Mask bit for corresponding field in interrupt request register. Default Value: 0
18	BUS_ERROR	Mask bit for corresponding field in interrupt request register. Default Value: 0
17	INSTR_CC_ERROR	Mask bit for corresponding field in interrupt request register. Default Value: 0
16	INSTR_OPC_ERROR	Mask bit for corresponding field in interrupt request register. Default Value: 0
4	PR_DATA_AVAILABLE	Mask bit for corresponding field in interrupt request register. Default Value: 0

3.1.8 CRYPTO_INTR_MASK (continued)

3	TR_DATA_AVAILABLE	Mask bit for corresponding field in interrupt request register. Default Value: 0
2	TR_INITIALIZED	Mask bit for corresponding field in interrupt request register. Default Value: 0
1	INSTR_FF_OVERFLOW	Mask bit for corresponding field in interrupt request register. Default Value: 0
0	INSTR_FF_LEVEL	Mask bit for corresponding field in interrupt request register. Default Value: 0

3.1.9 CRYPTO_INTR_MASKED

Interrupt masked register

Address: 0x4010010C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	R	R	R	R
HW Access	None			W	W	W	W	W
Name	None [7:5]			PR_-DATA_AVAILABLE	TR_-DATA_AVAILABLE	TR_INITIALIZED	INSTR_FF_OVERFLOW	INSTR_FF_LEVEL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [23:22]		INSTR_DEV_KEY_ERROR	TR_RC_-DETECT_ERROR	TR_AP_DETECT_ERROR	BUS_ERROR	INSTR_CC_ERROR	INSTR_OPC_ERROR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	INSTR_DEV_KEY_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
20	TR_RC_DETECT_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
19	TR_AP_DETECT_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
18	BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
17	INSTR_CC_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
16	INSTR_OPC_ERROR	Logical and of corresponding request and mask bits. Default Value: 0

3.1.9 CRYPTO_INTR_MASKED (continued)

4	PR_DATA_AVAILABLE	Logical and of corresponding request and mask bits. Default Value: 0
3	TR_DATA_AVAILABLE	Logical and of corresponding request and mask bits. Default Value: 0
2	TR_INITIALIZED	Logical and of corresponding request and mask bits. Default Value: 0
1	INSTR_FF_OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
0	INSTR_FF_LEVEL	Logical and of corresponding request and mask bits. Default Value: 0

3.1.10 CRYPTO_PR_LFSR_CTL0

Pseudo random LFSR control 0

Address: 0x40100200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	LFSR32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	LFSR32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	LFSR32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	LFSR32 [31:24]							

Bits	Name	Description
31 : 0	LFSR32	State of a 32-bit Linear Feedback Shift Registers (LFSR) that is used to generate a pseudo random bit sequence. This register needs to be initialized by SW. The initialization value should be different from "0". The three PR_LFSR_CTL registers represents the state of a 32-bit, 31-bit and 29-bit LFSR. Individually, these LFSRs generate a pseudo random bit sequence that repeats itself after (2^32)-1, (2^31)-1 and (2^29)-1 bits. The numbers (2^32)-1, (2^31)-1 and (2^29)-1 are relatively prime (their greatest common denominator is "1"). The three bit sequence are combined (XOR'd) into a single bitstream to create a pseudo random bit sequence that repeats itself after ((2^32)-1) * ((2^31)-1) * ((2*29)-1) bits. The following polynomials are used: - 32-bit irreducible polynomial: x^32+x^30+x^26+x^25+1. - 31-bit irreducible polynomial: x^31+x^28+1. - 29-bit irreducible polynomial: x^29+x^27+1. Default Value: 3633683401

3.1.11 CRYPTO_PR_LFSR_CTL1

Pseudo random LFSR control 1

Address: 0x40100204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	LFSR31 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	LFSR31 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	LFSR31 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW						
HW Access	None	RW						
Name	None	LFSR31 [30:24]						

Bits	Name	Description
30 : 0	LFSR31	State of a 31-bit Linear Feedback Shift Registers (LFSR) that is used to generate a pseudo random bit sequence. See PR_LFSR_CTL0. Default Value: 733549048

3.1.12 CRYPTO_PR_LFSR_CTL2

Pseudo random LFSR control 2

Address: 0x40100208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	LFSR29 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	LFSR29 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	LFSR29 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			RW				
Name	None [31:29]			LFSR29 [28:24]				

Bits	Name	Description
28 : 0	LFSR29	State of a 29-bit Linear Feedback Shift Registers (LFSR) that is used to generate a pseudo random bit sequence. See PR_LFSR_CTL0. Default Value: 101462455

3.1.13 CRYPTO_PR_MAX_CTL

Pseudo random maximum control

Address: 0x4010020C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Maximum value of to be generated random number Default Value: 4294967295

3.1.14 CRYPTO_PR_CMD

Pseudo random command

Address: 0x40100210

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							START

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	START	Pseudo random command. On a generated number, HW sets this field to '0' and sets INTR.PR_DATA_AVAILABLE to '1. Default Value: 0

3.1.15 CRYPTO_PR_RESULT

Pseudo random result

Address: 0x40100218

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Result of a pseudo random number generation operation. The resulting value DATA is in the range [0, PR_MAX_CTL.DATA32]. The PR_DATA_AVAILABLE interrupt cause is activated when the number is generated. Note that SW can write this field. This functionality can be used prevent information leakage. Default Value: 0

3.1.16 CRYPTO_TR_CTL0

True random control 0

Address: 0x40100280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SAMPLE_CLOCK_DIV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RED_CLOCK_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INIT_DELAY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW	RW	None			RW
HW Access	None		R	R	None			R
Name	None [31:30]		STOP_ON_RC_DETECT	STOP_ON_AP_DETECT	None [27:25]			VON_NEUMAN_N_CORR

Bits	Name	Description
29	STOP_ON_RC_DETECT	Specifies if TRNG functionality is stopped on a repetition count test detection (when HW sets INTR.TR_RC_DETECT to '1'): '0': Functionality is NOT stopped. '1': Functionality is stopped (TR_CTL1 fields are set to '0' by HW). Default Value: 0
28	STOP_ON_AP_DETECT	Specifies if TRNG functionality is stopped on an adaptive proportion test detection (when HW sets INTR.TR_AP_DETECT to '1'): '0': Functionality is NOT stopped. '1': Functionality is stopped (TR_CTL1 fields are set to '0' by HW). Default Value: 0

3.1.16 CRYPTO_TR_CTL0 (continued)

24	VON_NEUMANN_CORR	Specifies if the "von Neumann corrector" is disabled or enabled: '0': disabled. '1': enabled. The "von Neumann corrector" post-processes the reduced bits to remove a '0' or '1' bias. The corrector operates on reduced bit pairs ("oldest bit, newest bit"): "00": no bit is produced. "01": '0' bit is produced (oldest bit). "10": '1' bit is produced (oldest bit). "11": no bit is produced. Note that the corrector produces bits at a random pace and at a frequency that is 1/4 of the reduced bit frequency (reduced bits are processed in pairs, and half of the pairs do NOT produce a bit). Default Value: 0
23 : 16	INIT_DELAY	Specifies an initialization delay: number of removed/dropped samples before reduced bits are generated. This field should be programmed in the range [1, 255]. After starting the oscillators, at least the first 2 samples should be removed/dropped to clear the state of internal synchronizers. In addition, it is advised to drop at least the second 2 samples from the oscillators (to circumvent the semi-predictable oscillator startup behavior). This result in the default field value of "3". Field encoding is as follows: "0": 1 sample is dropped. "1": 2 samples are dropped. ... "255": 256 samples are dropped. The TR_INITIALIZED interrupt cause is set to '1', when the initialization delay is passed. Default Value: 3
15 : 8	RED_CLOCK_DIV	Specifies the clock divider that is used to produce reduced bits. "0": 1 reduced bit is produced for each sample. "1": 1 reduced bit is produced for each 2 samples. ... "255": 1 reduced bit is produced for each 256 samples. The reduced bits are considered random bits and shifted into TR_RESULT0.DATA32. Default Value: 0
7 : 0	SAMPLE_CLOCK_DIV	Specifies the clock divider that is used to sample oscillator data. This clock divider is wrt. "clk_sys". "0": sample clock is "clk_sys". "1": sample clock is "clk_sys"/2. ... "255": sample clock is "clk_sys"/256. Default Value: 0

3.1.17 CRYPTO_TR_CTL1

True random control 1

Address: 0x40100284

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [7:6]		FIRO31_EN	FIRO15_EN	GA-RO31_EN	GA-RO15_EN	RO15_EN	RO11_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	FIRO31_EN	FW sets this field to '1' to enable the programmable Fibonacci ring oscillator with up to 31 inverters. The TR_FIRO_CTL register specifies the programmable polynomial. Default Value: 0
4	FIRO15_EN	FW sets this field to '1' to enable the fixed Fibonacci ring oscillator with 15 inverters. Default Value: 0
3	GARO31_EN	FW sets this field to '1' to enable the programmable Galois ring oscillator with up to 31 inverters. The TR_GARO_CTL register specifies the programmable polynomial. Default Value: 0
2	GARO15_EN	FW sets this field to '1' to enable the fixed Galois ring oscillator with 15 inverters. Default Value: 0
1	RO15_EN	FW sets this field to '1' to enable the ring oscillator with 15 inverters. Default Value: 0
0	RO11_EN	FW sets this field to '1' to enable the ring oscillator with 11 inverters. Default Value: 0

3.1.18 CRYPTO_TR_CTL2

True random control 2

Address: 0x40100288

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		SIZE [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	SIZE	Bit size of generated random number in TR_RESULT. Legal range is in [0, 32]. Default Value: 0

3.1.19 CRYPTO_TR_STATUS

True random status

Address: 0x4010028C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							INITIAL-IZED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	INITIALIZED	Reflects the state of the true random number generator: '0': Not initialized (TR_CTL0.INIT_DELAY has NOT passed). '1': Initialized (TR_CTL0.INIT_DELAY has passed). Default Value: 0

3.1.20 CRYPTO_TR_CMD

True random command

Address: 0x40100290

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							START

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	START	True random command. On completion of the command, HW sets this field to '0' and sets INTR.TR_DATA_AVAILABLE to '1 when: - A random number is generated in TR_RESULT. - All ring oscillators are off (per TR_CTL1). - A repetition count (RC) or adaptive proportion (AP) error is detected during the random number generation (INTR.TR_RC/AP_DETECT_ERROR). Note: On completion of the command, SW should check TR_CTL1 and INTR.TR_RC/AP_DETECT_ERROR to ensure that no unexpected error occurred during random number generation. Default Value: 0

3.1.21 CRYPTO_TR_RESULT

True random result

Address: 0x40100298

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Generated true random number. HW generates the number in the least significant bit positions (TR_CTL2.SIZE) of this field. The TR_DATA_AVAILABLE interrupt cause is activated when the number is generated. Note that SW can write this field. This functionality can be used prevent information leakage. Default Value: 0

3.1.22 CRYPTO_TR_GARO_CTL

True random GARO control

Address: 0x401002A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW						
HW Access	None	R						
Name	None	POLYNOMIAL31 [30:24]						

Bits	Name	Description
30 : 0	POLYNOMIAL31	Polynomial for programmable Galois ring oscillator. The polynomial is represented WITHOUT the high order bit (this bit is always assumed '1'). The polynomial should be aligned such that the more significant bits (bit 30 and down) contain the polynomial and the less significant bits (bit 0 and up) contain padding '0's. Default Value: 0

3.1.23 CRYPTO_TR_FIRO_CTL

True random FIRO control

Address: 0x401002A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW						
HW Access	None	R						
Name	None	POLYNOMIAL31 [30:24]						

Bits	Name	Description
30 : 0	POLYNOMIAL31	Polynomial for programmable Fibonacci ring oscillator. The polynomial is represented WITHOUT the high order bit (this bit is always assumed '1'). The polynomial should be aligned such that the more significant bits (bit 30 and down) contain the polynomial and the less significant bits (bit 0 and up) contain padding '0's. Default Value: 0

3.1.24 CRYPTO_TR_MON_CTL

True random monitor control

Address: 0x401002C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						BITSTREAM_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	BITSTREAM_SEL	Selection of the bitstream: "0": DAS bitstream. "1": RED bitstream. "2": TR bitstream. "3": Undefined. Default Value: 2

3.1.25 CRYPTO_TR_MON_CMD

True random monitor command

Address: 0x401002C8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW1C	RW1C
Name	None [7:2]						START_RC	START_AP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	START_RC	Repetition count (RC) test enable: '0': Disabled. '1': Enabled. On a RC detection, HW sets this field to '0' and sets INTR.TR_RC_DETECT to '1. Default Value: 0
0	START_AP	Adaptive proportion (AP) test enable: '0': Stopped. '1': Started. On a AP detection, HW sets this field to '0' and sets INTR.TR_AP_DETECT to '1. Default Value: 0

3.1.26 CRYPTO_TR_MON_RC_CTL

True random monitor RC control

Address: 0x401002D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CUTOFF_COUNT8 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CUTOFF_COUNT8	Cutoff count (legal range is [1, 255]): "0": Illegal. "1": 1 repetition. ... "255": 255 repetitions. Default Value: 255

3.1.27 CRYPTO_TR_MON_RC_STATUS0

True random monitor RC status 0

Address: 0x401002D8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							BIT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	BIT	Current active bit value: '0': '0'. '1': '1'. This field is only valid when TR_MON_RC_STATUS1.REP_COUNT is NOT equal to "0". Default Value: 0

3.1.28 CRYPTO_TR_MON_RC_STATUS1

True random monitor RC status 1

Address: 0x401002DC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	REP_COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	REP_COUNT	Number of repetitions of the current active bit counter: "0": 0 repetitions. ... "255": 255 repetitions. Default Value: 0

3.1.29 CRYPTO_TR_MON_AP_CTL

True random monitor AP control

Address: 0x401002E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CUTOFF_COUNT16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CUTOFF_COUNT16 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	WINDOW_SIZE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	WINDOW_SIZE [31:24]							

Bits	Name	Description
31 : 16	WINDOW_SIZE	Window size (minus 1) : "0": 1 bit. ... "65535": 65536 bits. Default Value: 65535
15 : 0	CUTOFF_COUNT16	Cutoff count (legal range is [1, 65535]). "0": Illegal. "1": 1 occurrence. ... "65535": 65535 occurrences. Default Value: 65535

3.1.30 CRYPTO_TR_MON_AP_STATUS0

True random monitor AP status 0

Address: 0x401002E8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							BIT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	BIT	Current active bit value: '0': '0'. '1': '1'. This field is only valid when TR_MON_AP_STATUS1.OCC_COUNT is NOT equal to "0". Default Value: 0

3.1.31 CRYPTO_TR_MON_AP_STATUS1

True random monitor AP status 1

Address: 0x401002EC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	OCC_COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	OCC_COUNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	WINDOW_INDEX [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	WINDOW_INDEX [31:24]							

Bits	Name	Description
31 : 16	WINDOW_INDEX	Counter to keep track of the current index in the window (counts from "0" to TR_MON_AP_CTL.WINDOW_SIZE to "0"). Default Value: 0
15 : 0	OCC_COUNT	Number of occurrences of the current active bit counter: "0": 0 occurrences ... "65535": 65535 occurrences Default Value: 0

3.1.32 CRYPTO_STATUS

Status

Address: 0x40101004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	BUSY	None						

Bits	Name	Description
31	BUSY	Reflects the state of the IP: '0': Idle/no busy. '1': Busy: - Instruction is pending in the instruction FIFO. - Instruction is busy in a IP component (e.g. SHA1, SHA2, SHA3, DES, TDES, AES, CHACHA, ...). - Store FIFO is busy. - TR or PR command is busy. Default Value: 0

3.1.33 CRYPTO_INSTR_FF_CTL

Instruction FIFO control

Address: 0x40101040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					EVENT_LEVEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	RW1S
Name	None [23:18]						BLOCK	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	BLOCK	This field specifies the behavior when an instruction is written to a full FIFO (INSTR_FIFO_WR MMIO register): '0': The write is ignored/dropped and the INTR.INSTR_FF_OVERFLOW interrupt cause is set to '1'. '1': The write is blocked, resulting in AHB-Lite wait states and the INTR.INSTR_FF_OVERFLOW interrupt cause is set to '1' (this cause may be masked out). The instruction is written to the FIFO as soon as a FIFO entry becomes available. The maximum time is roughly the time of the execution of the slowest/longest instruction. Note that this setting may "lock up" /stall the CPU. When the CPU is "locked up"/stalled it can not respond to any system interrupts. As a result, the interrupt latency is increased. Note that this may not be an issue if the associated CPU is only performing cryptography functionality, e.g. the CM0+ during boot time. Default Value: 1
16	CLEAR	When '1', the instruction FIFO is cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. HW sets this field to '1' on when a INSTR_OPC_ERROR, INSTR_CC_ERROR or BUS_ERROR interrupt cause is activated. Default Value: 0

3.1.33 CRYPTO_INSTR_FF_CTL (continued)

2 : 0	EVENT_LEVEL	Event level. When the number of entries in the instruction FIFO is less than the amount of this field, an event is generated: - "event" = INSTR_FF_STATUS.USED < EVENT_LEVEL. Default Value: 0

3.1.34 CRYPTO_INSTR_FF_STATUS

Instruction FIFO status

Address: 0x40101044

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				USED [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							W
Name	None [23:17]							EVENT

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	EVENT	Instruction FIFO event. Default Value: 0
3 : 0	USED	Number of instructions in the instruction FIFO. The value of this field ranges from 0 to 8. Default Value: 0

3.1.35 CRYPTO_INSTR_FF_WR

Instruction FIFO write

Address: 0x40101048

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Instruction or instruction operand data that is written to the instruction FIFO. Default Value: 0

3.1.36 CRYPTO_LOAD0_FF_STATUS

Load 0 FIFO status

Address: 0x401010C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			W				
Name	None [7:5]			USED5 [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	BUSY	None [30:24]						

Bits	Name	Description
31	BUSY	Reflects the state of the FIFO: '0': FIFO load engine is idle and a new FIFO instruction can be accepted. '1': FIFO load engine is busy and NO new FIFO instruction can be accepted. Default Value: 0
4 : 0	USED5	Number of Bytes in the FIFO. The value of this field is in the range [0, 19]. Default Value: 0

3.1.37 CRYPTO_LOAD1_FF_STATUS

Load 1 FIFO status

Address: 0x401010D0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			W				
Name	None [7:5]			USED5 [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	BUSY	None [30:24]						

Bits	Name	Description
31	BUSY	See LOAD1_FF_STATUS.BUSY. Default Value: 0
4 : 0	USED5	See LOAD1_FF_STATUS.USED. Default Value: 0

3.1.38 CRYPTO_STORE_FF_STATUS

Store FIFO status

Address: 0x401010F0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			W				
Name	None [7:5]			USED5 [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	BUSY	None [30:24]						

Bits	Name	Description
31	BUSY	Reflects the state of the FIFO: '0': FIFO store engine is idle and a new FIFO instruction can be accepted (USED is "0"). '1': FIFO store engine is busy and NO new FIFO instruction can be accepted. Default Value: 0
4 : 0	USED5	Number of Bytes in the FIFO. The value of this field is in the range [0, 16]. Default Value: 0

3.1.39 CRYPTO_AES_CTL

AES control

Address: 0x40101100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						KEY_SIZE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	KEY_SIZE	AES key size: "0": 128-bit key, 10 rounds AES (inverse) cipher operation. "1": 192-bit key, 12 rounds AES (inverse) cipher operation. "2": 256-bit key, 14 rounds AES (inverse) cipher operation. "3": Undefined Default Value: 0 **0x0: AES128 :** **0x1: AES192 :** **0x2: AES256 :**

3.1.40 CRYPTO_RESULT

Result

Address: 0x40101180

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	BLOCK_CMP operation (DATA[0]): "0": source 0 equals source 1. "1": source 0 does NOT equal source 1. CRC operation (DATA[31:0]). State of a 32-bit Linear Feedback Shift Registers (LFSR) that is used to implement CRC. This register needs to be initialized by SW to provide the CRC seed value. The seed value should be aligned such that the more significant bits (bit 31 and down) contain the seed value and the less significant bits (bit 0 and up) contain padding '0's. Note that SW can write this field. This functionality can be used prevent information leakage. Default Value: 0

3.1.41 CRYPTO_CRC_CTL

CRC control

Address: 0x40101400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							DATA_REVERSE

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							REM_REVERSE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	REM_REVERSE	Specifies whether the remainder is bit reversed (reversal is performed after XORing): '0': No. '1': Yes. Default Value: 0
0	DATA_REVERSE	Specifies the bit order in which a data Byte is processed (reversal is performed after XORing): '0': Most significant bit (bit 1) first. '1': Least significant bit (bit 0) first. Default Value: 0

3.1.42 CRYPTO_CRC_DATA_CTL

CRC data control

Address: 0x40101410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA_XOR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA_XOR	Specifies a byte mask with which each data byte is XOR'd. The XOR is performed before data reversal. Default Value: 0

3.1.43 CRYPTO_CRC_POL_CTL

CRC polynomial control

Address: 0x40101420

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [31:24]							

Bits	Name	Description
31 : 0	POLYNOMIAL	CRC polynomial. The polynomial is represented WITHOUT the high order bit (this bit is always assumed '1'). The polynomial should be aligned/shifted such that the more significant bits (bit 31 and down) contain the polynomial and the less significant bits (bit 0 and up) contain padding '0's. Some frequently used polynomials: - CRC32: POLYNOMIAL is 0x04c11db7 (x^32 + x^26 + x^23 + x^22 + x^16 + x^12 + x^11 + x^10 + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1). - CRC16: POLYNOMIAL is 0x80050000 (x^16 + x^15 + x^2 + 1, shifted by 16 bit positions). - CRC16 CCITT: POLYNOMIAL is 0x10210000 (x^16 + x^12 + x^5 + 1, shifted by 16 bit positions). Default Value: 0

3.1.44 CRYPTO_CRC_REM_CTL

CRC remainder control

Address: 0x40101440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	REM_XOR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	REM_XOR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	REM_XOR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	REM_XOR [31:24]							

Bits	Name	Description
31 : 0	REM_XOR	Specifies a mask with which the CRC_LFSR_CTL.LFSR32 register is XOR'd to produce a remainder. The XOR is performed before remainder reversal. Default Value: 0

3.1.45 CRYPTO_CRC_REM_RESULT

CRC remainder result

Address: 0x40101448

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	REM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	REM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	REM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	REM [31:24]							

Bits	Name	Description
31 : 0	REM	Remainder value. The alignment of the remainder depends on CRC_REM_CTL0.REM_REVERSE: '0': the more significant bits (bit 31 and down) contain the remainder. '1': the less significant bits (bit 0 and up) contain the remainder. Note: This field is combinatorially derived from CRC_LFSR_CTL.LFSR32, CRC_REM_CTL0.REM_REVERSE and CRC_REM_CTL1.REM_XOR. Default Value: 0

3.1.46 CRYPTO_VU_CTL0

Vector unit control 0

Address: 0x40101480

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							ALWAYS_EXECUTE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	ALWAYS_EXECUTE	Specifies if a conditional instruction is executed or not, when its condition code evaluates to false/'0'. '0': The instruction is NOT executed. As a result, the instruction may be handled faster than when it is executed. '1': The instruction is executed, but the execution result (including status field information) is not reflected in the IP. The instruction is handled just as fast as when it is executed. Note: a conditional instruction with a condition code that evaluates to false/'0' does not affect the architectural state: VU_STATUS fields, memory or register-file data. Note: Always execution is useful to prevent/complicate differential timing and differential power attacks. Default Value: 0

3.1.47 CRYPTO_VU_CTL1

Vector unit control 1

Address: 0x40101484

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	Specifies the memory address for the vector unit operand memory region. The register-file registers provide 13-bit word offsets within this memory region. Given ADDR[31:8], VU_VTL2.MASK[14:8] and a 13-bit word offset offset[14:2], a vector operand memory address VU_OPERAND_ADDR[31:0] is calculated as follows: - VU_OPERAND_ADDR[31:15] = ADDR[31:15] - VU_OPERAND_ADDR[14:8] = (ADDR[14:8] & MASK[14:8]) | (offset[14:8] & ~MASK[14:8]) - VU_OPERAND_ADDR[7:2] = offset[7:2] - VU_OPERAND_ADDR[1:0] = 0 (always word aligned) The vector unit operand memory region uses either the IP's memory buffer or system memory. For best performance, the IP's memory buffer should be used and ADDR should be set to MEM_BUFF and MASK should specify the IP memory buffer size. If a vector operand memory address is mapped on a memory hole, read accesses return a "0" and write accesses are ignored. Default Value: 0

3.1.48 CRYPTO_VU_CTL2

Vector unit control 2

Address: 0x40101488

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW						
HW Access	None	R						
Name	None	MASK [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14 : 8	MASK	Specifies the size of the vector operand memory region. Legal values: "0b0000000": 32 KB memory region (VU_VTL1.ADDR[14:8] ignored). "0b1000000": 16 KB memory region (VU_VTL1.ADDR[13:8] ignored). "0b1100000": 8 KB memory region (VU_VTL1.ADDR[12:8] ignored). "0b1110000": 4 KB memory region (VU_VTL1.ADDR[11:8] ignored). "0b1111000": 2 KB memory region (VU_VTL1.ADDR[10:8] ignored). "0b1111100": 1 KB memory region (VU_VTL1.ADDR[9:8] ignored). "0b1111110": 512 B memory region (VU_VTL1.ADDR[8] ignored). "0b1111111": 256 B memory region. Note: the default specifies a 256 B memory region. Default Value: 127

3.1.49 CRYPTO_VU_STATUS

Vector unit status

Address: 0x40101490

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				ONE	ZERO	EVEN	CARRY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	ONE	STATUS ONE field. Default Value: 0
2	ZERO	STATUS ZERO field. Default Value: 0
1	EVEN	STATUS EVEN field. Default Value: 0
0	CARRY	STATUS CARRY field. Default Value: 0

3.1.50 CRYPTO_VU_RF_DATA0

Vector unit register-file

Address: 0x401014C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Vector unit register-file data. A register-file register has the following layout: DATA[28:16]: data (typically used as a word offset in vector unit operand memory). DATA[12:0]: bit size minus 1. Default Value: 0

3.1.51 CRYPTO_DEV_KEY_ADDR0_CTL

Device key address 0 control

Address: 0x40102000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	VALID	None						

Bits	Name	Description
31	VALID	Specifies if the address in the associated DEV_KEY_ADDR0 is valid: '0': Address not valid; i.e. no device key specified. '1': Address valid; i.e. device key specified. Note: A LOAD_DEV_KEY instruction requires that the device key's valid field is '1'. Default Value: 0

3.1.52 CRYPTO_DEV_KEY_ADDR0

Device key address 0

Address: 0x40102004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR32 [31:24]							

Bits	Name	Description
31 : 0	ADDR32	Specifies the memory address of the device key in memory. A LOAD_DEV_KEY instruction uses this address to load a device key from memory into the IP register buffer blocks 4 and 5. Default Value: 0

3.1.53 CRYPTO_DEV_KEY_ADDR1_CTL

Device key address 1 control

Address: 0x40102020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	VALID	None						

Bits	Name	Description
31	VALID	See DEV_KEY_ADDR0_CTL. Default Value: 0

3.1.54 CRYPTO_DEV_KEY_ADDR1

Device key address 1 control

Address: 0x40102024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR32 [31:24]							

Bits	Name	Description
31 : 0	ADDR32	See DEV_KEY_ADDR0. Default Value: 0

3.1.55 CRYPTO_DEV_KEY_STATUS

Device key status

Address: 0x40102080

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							LOADED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	LOADED	Specifies if a device key is present in the IP register buffer blocks 4 and 5. HW sets this field to '1' on successful completion of a LOAD_DEV_KEY instruction. HW clears this field to '0' when a CLEAR instruction is executed (the CLEAR instruction also sets the IP register buffer to "0"). Default Value: 0

3.1.56 CRYPTO_DEV_KEY_CTL0

Device key control 0

Address: 0x40102100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							ALLOWED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	ALLOWED	Specifies if a LOAD_DEV_KEY instruction is allowed to use the device key in memory: '0': Not allowed. '1': Allowed. Note: For successful completion of a LOAD_DEV_KEY instruction, both the associated DEV_KEY_ADDR_CTL.VALID and DEV_KEY_CTL.ALLOWED fields must be '1'. On successful instruction completion, DEV_KEY_STATUS.LOADED is set to '1'. On unsuccessful completion, the instruction FIFO is cleared and the IP is locked; an Active reset or an IP reset (CTL.ENABLED), which reinitializes the IP, is required. Note: A LOAD_DEV_KEY loads the device key from memory with protection context "0". Default Value: 0

3.1.57 CRYPTO_DEV_KEY_CTL1

Device key control 1

Address: 0x40102120

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							ALLOWED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	ALLOWED	See DEV_KEY_CTL0. Default Value: 0

3.1.58 CRYPTO_MEM_BUFF0

Memory buffer

Address: 0x40108000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: Undefined

Section D: Peripheral Group 2

This section encompasses the following chapters:

- CPU Sub System Registers chapter on page 722
- Fault Registers chapter on page 773
- Inter-Processor Communication Registers chapter on page 798
- Protection Unit Registers chapter on page 814
- Flash Controller Registers chapter on page 860
- System Resources Subsystem Registers chapter on page 939
- Multi-Counter WDT Registers chapter on page 1014
- Backup System Registers chapter on page 1028
- Direct Memory Access Registers chapter on page 1054
- eFuse Registers chapter on page 1124

4 CPU Sub System Registers

This section discusses the CPU Sub System (CPUSS) registers. It lists all the registers in mapping tables, in address order.

4.1 Register Details

Register	Address	Description
CPUSS_IDENTITY	0x40200000	Identity
CPUSS_CM4_STATUS	0x40200004	CM4 status
CPUSS_CM4_CLOCK_CTL	0x40200008	CM4 clock control
CPUSS_CM4_CTL	0x4020000C	CM4 control
CPUSS_CM4_VECTOR_TABLE_BASE	0x40200200	CM4 vector table base
CPUSS_CM4_NMI_CTL0	0x40200240	CM4 NMI control
CPUSS_CM4_NMI_CTL1	0x40200244	CM4 NMI control. See CPUSS_CM4_NMI_CTL0 for the details of bit fields.
CPUSS_CM4_NMI_CTL2	0x40200248	CM4 NMI control. See CPUSS_CM4_NMI_CTL0 for the details of bit fields.
CPUSS_CM4_NMI_CTL3	0x4020024C	CM4 NMI control. See CPUSS_CM4_NMI_CTL0 for the details of bit fields.
CPUSS_CM0_CTL	0x40201000	CM0+ control
CPUSS_CM0_STATUS	0x40201004	CM0+ status
CPUSS_CM0_CLOCK_CTL	0x40201008	CM0+ clock control
CPUSS_CM0_INT0_STATUS	0x40201100	CM0+ interrupt 0 status
CPUSS_CM0_INT1_STATUS	0x40201104	CM0+ interrupt 1 status
CPUSS_CM0_INT2_STATUS	0x40201108	CM0+ interrupt 2 status
CPUSS_CM0_INT3_STATUS	0x4020110C	CM0+ interrupt 3 status
CPUSS_CM0_INT4_STATUS	0x40201110	CM0+ interrupt 4 status
CPUSS_CM0_INT5_STATUS	0x40201114	CM0+ interrupt 5 status
CPUSS_CM0_INT6_STATUS	0x40201118	CM0+ interrupt 6 status
CPUSS_CM0_INT7_STATUS	0x4020111C	CM0+ interrupt 7 status
CPUSS_CM0_VECTOR_TABLE_BASE	0x40201120	CM0+ vector table base
CPUSS_CM0_NMI_CTL0	0x40201140	CM0+ NMI control
CPUSS_CM0_NMI_CTL1	0x40201144	CM0+ NMI control. See CPUSS_CM0_NMI_CTL0 for the details of bit fields.
CPUSS_CM0_NMI_CTL2	0x40201148	CM0+ NMI control. See CPUSS_CM0_NMI_CTL0 for the details of bit fields.
CPUSS_CM0_NMI_CTL3	0x4020114C	CM0+ NMI control. See CPUSS_CM0_NMI_CTL0 for the details of bit fields.
CPUSS_CM4_PWR_CTL	0x40201200	CM4 power control
CPUSS_CM4_PWR_DELAY_CTL	0x40201204	CM4 power control
CPUSS_RAM0_CTL0	0x40201300	RAM 0 control
CPUSS_RAM0_PWR_MACRO_CTL0	0x40201340	RAM 0 power control
CPUSS_RAM0_PWR_MACRO_CTL1	0x40201344	RAM 0 power control. See CPUSS_RAM0_PWR_MACRO_CTL0 for the details of bit fields.

Register	Address	Description
CPUSS_RAM0_PWR_MACRO_CTL2	0x40201348	RAM 0 power control. See CPUSS_RAM0_PWR_MACRO_CTL0 for the details of bit fields.
CPUSS_RAM0_PWR_MACRO_CTL3	0x4020134C	RAM 0 power control. See CPUSS_RAM0_PWR_MACRO_CTL0 for the details of bit fields.
CPUSS_RAM_PWR_DELAY_CTL	0x402013C0	Power up delay used for all SRAM power domains
CPUSS_ROM_CTL	0x402013C4	ROM control
CPUSS_PRODUCT_ID	0x40201400	Product identifier and version (same as CoreSight RomTables)
CPUSS_DP_STATUS	0x40201410	Debug port status
CPUSS_AP_CTL	0x40201414	Access port control
CPUSS_BUFF_CTL	0x40201500	Buffer control
CPUSS_SYSTICK_CTL	0x40201600	SysTick timer control
CPUSS_MBIST_STAT	0x40201704	Memory BIST status
CPUSS_CAL_SUP_SET	0x40201800	Calibration support set and read
CPUSS_CAL_SUP_CLR	0x40201804	Calibration support clear and reset
CPUSS_CM0_PC_CTL	0x40202000	CM0+ protection context control
CPUSS_CM0_PC0_HANDLER	0x40202040	CM0+ protection context 0 handler
CPUSS_CM0_PC1_HANDLER	0x40202044	CM0+ protection context 1 handler
CPUSS_CM0_PC2_HANDLER	0x40202048	CM0+ protection context 2 handler
CPUSS_CM0_PC3_HANDLER	0x4020204C	CM0+ protection context 3 handler
CPUSS_PROTECTION	0x402020C4	Protection status
CPUSS_TRIM_ROM_CTL	0x40202100	ROM trim control
CPUSS_TRIM_RAM_CTL	0x40202104	RAM trim control
CPUSS_CM0_SYSTEM_INT_CTL0	0x40208000	CM0+ system interrupt control. This is the starting address of a register bank containing 175 registers (CPUSS_CM0_SYSTEM_INT_CTL0 to CPUSS_CM0_SYSTEM_INT_CTL174).

4.1.1 CPUSS_IDENTITY

Identity

Address: 0x40200000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None		R	R
HW Access	W				None		W	W
Name	PC [7:4]				None [3:2]		NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				MS [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 8	MS	This field specifies the bus master identifier of the transfer that reads the register. Default Value: Undefined
7 : 4	PC	This field specifies the protection context of the transfer that reads the register. Default Value: Undefined
1	NS	This field specifies the security setting ('0': secure mode; '1': non-secure mode) of the transfer that reads the register. Default Value: Undefined
0	P	This field specifies the privileged setting ('0': user mode; '1': privileged mode) of the transfer that reads the register. Default Value: Undefined

4.1.2 CPUSS_CM4_STATUS

CM4 status

Address: 0x40200004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	None		R	R
HW Access	None			W	None		W	W
Name	None [7:5]			PWR_-DONE	None [3:2]		SLEEP-DEEP	SLEEPING

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	PWR_DONE	After a PWR_MODE change this flag indicates if the new power mode has taken effect or not. Note: this flag can also change as a result of a change in debug power up req Default Value: 1
1	SLEEPDEEP	Specifies if the CPU is in Sleep or DeepSleep power mode. See SLEEPING field. Default Value: 1
0	SLEEPING	Specifies if the CPU is in Active, Sleep or DeepSleep power mode: - Active power mode: SLEEPING is '0'. - Sleep power mode: SLEEPING is '1' and SLEEPDEEP is '0'. - DeepSleep power mode: SLEEPING is '1' and SLEEPDEEP is '1'. Default Value: 1

4.1.3 CPUSS_CM4_CLOCK_CTL

CM4 clock control

Address: 0x40200008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	FAST_INT_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	FAST_INT_DIV	Specifies the fast clock divider (from the high frequency clock "clk_hf" to the peripheral clock "clk_fast"). Integer division by (1+FAST_INT_DIV). Allows for integer divisions in the range [1, 256] (FAST_INT_DIV is in the range [0, 255]). Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0

4.1.4 CPUSS_CM4_CTL

CM4 control

Address: 0x4020000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None		RW	RW	RW	RW	RW
HW Access	R	None		R	R	R	R	R
Name	IDC_MASK	None [30:29]		IXC_MASK	UFC_MASK	OFC_MASK	DZC_MASK	IOC_MASK

Bits	Name	Description
31	IDC_MASK	CPU FPU exception mask for the CPU's FPCSR.IDC "input denormalized" exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. Note: if the CPU FPCSR.FZ field is set to '1', denormalized inputs are "flushed to zero". Dependent on the FPU algorithm, this may or may not occur frequently. To prevent frequent CPU FPU interrupts as a result of denormalized inputs, this field may be set to '0'. Default Value: 0
28	IXC_MASK	CPU FPU exception mask for the CPU's FPCSR.IXC "inexact" exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. Note: the "inexact" condition is set as a result of rounding. Rounding may occur frequently and is typically not an error condition. To prevent frequent CPU FPU interrupts as a result of rounding, this field is typically set to '0'. Default Value: 0
27	UFC_MASK	CPU FPU exception mask for the CPU's FPCSR.UFC "underflow" exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. Default Value: 0

4.1.4 CPUSS_CM4_CTL (continued)

26	OFC_MASK	CPU FPU exception mask for the CPU's FPCSR.OFC "overflow" exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. Default Value: 0
25	DZC_MASK	CPU FPU exception mask for the CPU's FPCSR.DZC "divide by zero" exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. Default Value: 0
24	IOC_MASK	CPU floating point unit (FPU) exception mask for the CPU's FPCSR.IOC "invalid operation" exception condition: '0': The CPU's exception condition does NOT activate the CPU's floating point interrupt. '1': the CPU's exception condition activates the CPU's floating point interrupt. Note: the ARM architecture does NOT support FPU exceptions; i.e. there is no precise FPU exception handler. Instead, FPU conditions are captured in the CPU's FPCSR register and the conditions are provided as CPU interface signals. The interface signals are "masked" with the fields a provide by this register (CM7_0_CTL). The "masked" signals are reduced/OR-ed into a single CPU floating point interrupt signal. The associated CPU interrupt handler allows for imprecise handling of FPU exception conditions. Note: the CPU's FPCSR exception conditions are "sticky". Typically, the CPU FPU interrupt handler will clear the exception condition(s) to '0'. Note: by default, the FPU exception masks are '0'. Therefore, FPU exception conditions will NOT activate the CPU's floating point interrupt. Default Value: 0

4.1.5 CPUSS_CM4_VECTOR_TABLE_BASE

CM4 vector table base

Address: 0x40200200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW						None	
HW Access							None	
Name	ADDR22 [15:10]						None [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	ADDR22 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	ADDR22 [31:24]							

Bits	Name	Description
31 : 10	ADDR22	Address of CM4 vector table. This register is used for CM4 warm and cold boot purposes: the CM0+ CPU initializes the CM4_VECTOR_TABLE_BASE register and the CM4 boot code uses the register to initialize the CM4 internal VTOR register. Note: the CM4 vector table is at an address that is a 1024 B multiple. Default Value: 0

4.1.6 CPUSS_CM4_NMI_CTL0

CM4 NMI control

Address: 0x40200240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SYSTEM_INT_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SYSTEM_INT_IDX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	SYSTEM_INT_IDX	System interrupt select for CPU NMI. The reset value ("1023") ensures that the CPU NMI is NOT connected to any system interrupt after DeepSleep reset. Default Value: 1023

4.1.7 CPUSS_CM0_CTL

CM0+ control

Address: 0x40201000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW1S	R
Name	None [7:2]						ENABLED	SLV_STALL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VECTKEYSTAT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VECTKEYSTAT [31:24]							

Bits	Name	Description
31 : 16	VECTKEYSTAT	Register key (to prevent accidental writes). - Should be written with a 0x05fa key value for the write to take effect. - Always reads as 0xfa05. Default Value: 64005
1	ENABLED	Processor enable: '0': Disabled. Processor clock is turned off and reset is activated. After SW clears this field to '0', HW automatically sets this field to '1'. This effectively results in a CM0+ reset, followed by a CM0+ warm boot. '1': Enabled. Note: The intent is that this bit is modified only through an external probe or by the CM4 while the CM0+ is in Sleep or DeepSleep power mode. If this field is cleared to '0' by the CM0+ itself, it should be done under controlled conditions (such that undesirable side effects can be prevented). Note: The CM0+ CPU has a AIRCR.SYSRESETREQ register field that allows the CM0+ to reset the complete device (ENABLED only disables/enables the CM0+), resulting in a warm boot. This CPU register field has similar "built-in protection" as this CM0_CTL register to prevent accidental system writes (the upper 16-bits of the register need to be written with a 0x05fa key value; see CPU user manual for more details). Default Value: 1

4.1.7 CPUSS_CM0_CTL (continued)

0	SLV_STALL	Processor debug access control: '0': Access. '1': Stall access. This field is used to stall/delay debug accesses. This is useful to protect execution of code that needs to be protected from debug accesses. Default Value: 0

4.1.8 CPUSS_CM0_STATUS

CM0+ status

Address: 0x40201004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						SLEEP-DEEP	SLEEPING

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	SLEEPDEEP	Specifies if the CPU is in Sleep or DeepSleep power mode. See SLEEPING field. Default Value: 0
0	SLEEPING	Specifies if the CPU is in Active, Sleep or DeepSleep power mode: - Active power mode: SLEEPING is '0'. - Sleep power mode: SLEEPING is '1' and SLEEPDEEP is '0'. - DeepSleep power mode: SLEEPING is '1' and SLEEPDEEP is '1'. Default Value: 0

4.1.9 CPUSS_CM0_CLOCK_CTL

CM0+ clock control

Address: 0x40201008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SLOW_INT_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	PERI_INT_DIV [31:24]							

Bits	Name	Description
31 : 24	PERI_INT_DIV	Specifies the peripheral clock divider (from the high frequency clock "clk_hf" to the peripheral clock "clk_peri"). Integer division by (1+PERI_INT_DIV). Allows for integer divisions in the range [1, 256] (PERI_INT_DIV is in the range [0, 255]). Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Note that Fperi <= Fperi_max. Fperi_max is likely to be smaller than Fhf_max. In other words, if Fhf = Fhf_max, PERI_INT_DIV should not be set to "0". Default Value: 0
15 : 8	SLOW_INT_DIV	Specifies the slow clock divider (from the peripheral clock "clk_peri" to the slow clock "clk_slow"). Integer division by (1+SLOW_INT_DIV). Allows for integer divisions in the range [1, 256] (SLOW_INT_DIV is in the range [0, 255]). Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0

4.1.10 CPUSS_CM0_INT0_STATUS

CM0+ interrupt 0 status

Address: 0x40201100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SYSTEM_INT_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						W	
Name	None [15:10]						SYSTEM_INT_IDX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	SYSTEM_INT_VALID	None [30:24]						

Bits	Name	Description
31	SYSTEM_INT_VALID	Valid indication for SYSTEM_INT_IDX. When '0', no system interrupt for CPU interrupt 0 is valid/activated. Default Value: 0
9 : 0	SYSTEM_INT_IDX	Lowest CM0+ activated system interrupt index for CPU interrupt 0. Multiple system interrupts can be mapped on the same CPU interrupt. The selected system interrupt is the system interrupt with the lowest system interrupt index that has an activated interrupt request at the time of the fetch (system_interrupts[SYSTEM_INT_IDX] is '1'). The CPU interrupt handler SW can read SYSTEM_INT_IDX to determine the system interrupt that activated the handler. Default Value: Undefined

4.1.11 CPUSS_CM0_INT1_STATUS

CM0+ interrupt 1 status

Address: 0x40201104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SYSTEM_INT_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						W	
Name	None [15:10]						SYSTEM_INT_IDX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	SYSTEM_INT_VALID	None [30:24]						

Bits	Name	Description
31	SYSTEM_INT_VALID	See description of CM0_INT0_STATUS. Default Value: 0
9 : 0	SYSTEM_INT_IDX	Lowest CM0+ activated system interrupt index for CPU interrupt 1. See description of CM0_INT0_STATUS. Default Value: Undefined

4.1.12 CPUSS_CM0_INT2_STATUS

CM0+ interrupt 2 status

Address: 0x40201108

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SYSTEM_INT_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						W	
Name	None [15:10]						SYSTEM_INT_IDX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	SYSTEM_INT_VALID	None [30:24]						

Bits	Name	Description
31	SYSTEM_INT_VALID	See description of CM0_INT0_STATUS. Default Value: 0
9 : 0	SYSTEM_INT_IDX	Lowest CM0+ activated system interrupt index for CPU interrupt 2. See description of CM0_INT0_STATUS. Default Value: Undefined

4.1.13 CPUSS_CM0_INT3_STATUS

CM0+ interrupt 3 status

Address: 0x4020110C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SYSTEM_INT_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						W	
Name	None [15:10]						SYSTEM_INT_IDX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	SYSTEM_INT_VALID	None [30:24]						

Bits	Name	Description
31	SYSTEM_INT_VALID	See description of CM0_INT0_STATUS. Default Value: 0
9 : 0	SYSTEM_INT_IDX	Lowest CM0+ activated system interrupt index for CPU interrupt 3. See description of CM0_INT0_STATUS. Default Value: Undefined

4.1.14 CPUSS_CM0_INT4_STATUS

CM0+ interrupt 4 status

Address: 0x40201110

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SYSTEM_INT_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						W	
Name	None [15:10]						SYSTEM_INT_IDX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	SYSTEM_INT_VALID	None [30:24]						

Bits	Name	Description
31	SYSTEM_INT_VALID	See description of CM0_INT0_STATUS. Default Value: 0
9 : 0	SYSTEM_INT_IDX	Lowest CM0+ activated system interrupt index for CPU interrupt 4. See description of CM0_INT0_STATUS. Default Value: Undefined

4.1.15 CPUSS_CM0_INT5_STATUS

CM0+ interrupt 5 status

Address: 0x40201114

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SYSTEM_INT_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						W	
Name	None [15:10]						SYSTEM_INT_IDX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	SYSTEM_INT_VALID	None [30:24]						

Bits	Name	Description
31	SYSTEM_INT_VALID	See description of CM0_INT0_STATUS. Default Value: 0
9 : 0	SYSTEM_INT_IDX	Lowest CM0+ activated system interrupt index for CPU interrupt 5. See description of CM0_INT0_STATUS. Default Value: Undefined

4.1.16 CPUSS_CM0_INT6_STATUS

CM0+ interrupt 6 status

Address: 0x40201118

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SYSTEM_INT_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						W	
Name	None [15:10]						SYSTEM_INT_IDX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	SYSTEM_INT_VALID	None [30:24]						

Bits	Name	Description
31	SYSTEM_INT_VALID	See description of CM0_INT0_STATUS. Default Value: 0
9 : 0	SYSTEM_INT_IDX	Lowest CM0+ activated system interrupt index for CPU interrupt 6. See description of CM0_INT0_STATUS. Default Value: Undefined

4.1.17 CPUSS_CM0_INT7_STATUS

CM0+ interrupt 7 status

Address: 0x4020111C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SYSTEM_INT_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						W	
Name	None [15:10]						SYSTEM_INT_IDX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	SYSTEM_INT_VALID	None [30:24]						

Bits	Name	Description
31	SYSTEM_INT_VALID	See description of CM0_INT0_STATUS. Default Value: 0
9 : 0	SYSTEM_INT_IDX	Lowest CM0+ activated system interrupt index for CPU interrupt 7. See description of CM0_INT0_STATUS. Default Value: Undefined

4.1.18 CPUSS_CM0_VECTOR_TABLE_BASE

CM0+ vector table base

Address: 0x40201120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	Address of CM0+ vector table. This register is used for CM0+ warm boot purposes: the CM0+ warm boot code uses the register to initialize the CM0+ internal VTOR register. Note: the CM0+ vector table is at an address that is a 256 B multiple. Default Value: 0

4.1.19 CPUSS_CM0_NMI_CTL0

CM0+ NMI control

Address: 0x40201140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SYSTEM_INT_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SYSTEM_INT_IDX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	SYSTEM_INT_IDX	System interrupt select for CPU NMI. The reset value ("1023") ensures that the CPU NMI is NOT connected to any system interrupt after DeepSleep reset. Default Value: 1023

4.1.20 CPUSS_CM4_PWR_CTL

CM4 power control

Address: 0x40201200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VECTKEYSTAT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VECTKEYSTAT [31:24]							

Bits	Name	Description
31 : 16	VECTKEYSTAT	Register key (to prevent accidental writes). - Should be written with a 0x05fa key value for the write to take effect. - Always reads as 0xfa05. Default Value: 64005
1 : 0	PWR_MODE	Power mode. Default Value: 1 **0x0: OFF :** Switch CM4 off Power off, clock off, isolate, reset and no retain. **0x1: RESET :** Reset CM4 Clock off, no isolated, no retain and reset. Note: The CM4 CPU has a AIRCR.SYSRESETREQ register field that allows the CM4 to reset the complete device (RESET only resets the CM4), resulting in a warm boot.

4.1.20 CPUSS_CM4_PWR_CTL (continued)

0x2: RETAINED :

Put CM4 in Retained mode
This can only become effective if CM4 is in SleepDeep mode. Check PWR_DONE flag to see if CM4 RETAINED state has been reached.
Power off, clock off, isolate, no reset and retain.

0x3: ENABLED :

Switch CM4 on.
Power on, clock on, no isolate, no reset and no retain.

4.1.21 CPUSS_CM4_PWR_DELAY_CTL

CM4 power control

Address: 0x40201204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	UP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						UP [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	UP	Number clock cycles delay needed after power domain power up Default Value: 300

4.1.22 CPUSS_RAM0_CTL0

RAM 0 control

Address: 0x40201300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						SLOW_WS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						FAST_WS [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	FAST_WS	Memory wait states for the fast clock domain ("clk_fast"). The number of wait states is expressed in "clk_hf" clock domain cycles. Default Value: 0
1 : 0	SLOW_WS	Memory wait states for the slow clock domain ("clk_slow"). The number of wait states is expressed in "clk_hf" clock domain cycles. Default Value: 1

4.1.23 CPUSS_RAM0_PWR_MACRO_CTL0

RAM 0 power control

Address: 0x40201340

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VECTKEYSTAT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VECTKEYSTAT [31:24]							

Bits	Name	Description
31 : 16	VECTKEYSTAT	Register key (to prevent accidental writes). - Should be written with a 0x05fa key value for the write to take effect. - Always reads as 0xfa05. Default Value: 64005
1 : 0	PWR_MODE	SRAM Power mode. Default Value: 3 **0x0: OFF :** Turn OFF the SRAM. This will trun OFF both array and periphery power of the SRAM and SRAM memory contents are lost. **0x1: RESERVED :** undefined

4.1.23 CPUSS_RAM0_PWR_MACRO_CTL0 (continued)

0x2: RETAINED :

Keep SRAM in Retained mode. This will turn OFF the SRAM periphery power, but array power is ON to retain memory contents.
The SRAM contents will be retained in DeepSleep system power mode.

0x3: ENABLED :

Enable SRAM for regular operation.
The SRAM contents will be retained in DeepSleep system power mode.

4.1.24 CPUSS_RAM_PWR_DELAY_CTL

Power up delay used for all SRAM power domains

Address: 0x402013C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	UP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						UP [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	UP	Number clock cycles delay needed after power domain power up Default Value: 150

4.1.25 CPUSS_ROM_CTL

ROM control

Address: 0x402013C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						SLOW_WS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						FAST_WS [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	FAST_WS	Memory wait states for the fast clock domain ("clk_fast"). The number of wait states is expressed in "clk_hf" clock domain cycles. Default Value: 0
1 : 0	SLOW_WS	Memory wait states for the slow clock domain ("clk_slow"). The number of wait states is expressed in "clk_hf" clock domain cycles. Timing paths to and from the memory have a (fixed) minimum duration that always needs to be considered/met. The "clk_hf" clock domain frequency determines this field's value such that the timing paths minimum duration is met. A table/formula will be provided for this field's values for different "clk_hf" frequencies. Default Value: 1

4.1.26 CPUSS_PRODUCT_ID

Product identifier and version (same as CoreSight RomTables)

Address: 0x40201400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	FAMILY_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				FAMILY_ID [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access	W				W			
Name	MINOR_REV [23:20]				MAJOR_REV [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 20	MINOR_REV	Minor Revision, starts with 1, increments with metal layer only tape-out (implemented with metal ECO-able tie-off) Default Value: Undefined
19 : 16	MAJOR_REV	Major Revision, starts with 1, increments with all layer tape-out (implemented with metal ECO-able tie-off) Default Value: Undefined
11 : 0	FAMILY_ID	Family ID a.k.a. Partnumber a.k.a. Silicon ID Default Value: 270

4.1.27 CPUSS_DP_STATUS

Debug port status

Address: 0x40201410

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [7:3]					SWJ_-JTAG_SEL	SWJ_DE-BUG_EN	SWJ_CON-NECTED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	SWJ_JTAG_SEL	Specifies if the JTAG or SWD interface is selected. This signal is valid when DP_CTL.PTM_SEL is '0' (SWJ mode selected) and SWJ_CONNECTED is '1' (SWJ is connected). '0': SWD selected. '1': JTAG selected. Default Value: 1
1	SWJ_DEBUG_EN	Specifies if SWJ debug is enabled, i.e. CDBGPWRUPACK is '1' and thus debug clocks are on: '0': Disabled. '1': Enabled. Default Value: 0
0	SWJ_CONNECTED	Specifies if the SWJ debug port is connected; i.e. debug host interface is active: '0': Not connected/not active. '1': Connected/active. Default Value: 0

4.1.28 CPUSS_AP_CTL

Access port control

Address: 0x40201414

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					SYS_EN-ABLE	CM4_EN-ABLE	CM0_EN-ABLE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					R	R	R
Name	None [23:19]					SYS_DIS-ABLE	CM4_DIS-ABLE	CM0_DIS-ABLE

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
18	SYS_DISABLE	Disables the system AP interface: '0': Enabled. '1': Disabled. Typically, this field is set by the Cypress boot code with information from eFUSE. The access port is only enabled when SYS_DISABLE is '0' and SYS_ENABLE is '1'. Default Value: 0
17	CM4_DISABLE	Disables the CM4 AP interface: '0': Enabled. '1': Disabled. Typically, this field is set by the Cypress boot code with information from eFUSE. The access port is only enabled when CM4_DISABLE is '0' and CM4_ENABLE is '1'. Default Value: 0

4.1.28 CPUSS_AP_CTL (continued)

16	CM0_DISABLE	Disables the CM0 AP interface: '0': Enabled. '1': Disabled. Typically, this field is set by the Cypress boot code with information from eFUSE. The access port is only enabled when CM0_DISABLE is '0' and CM0_ENABLE is '1'. Default Value: 0
2	SYS_ENABLE	Enables the system AP interface: '0': Disabled. '1': Enabled. Default Value: 0
1	CM4_ENABLE	Enables the CM4 AP interface: '0': Disabled. '1': Enabled. Default Value: 0
0	CM0_ENABLE	Enables the CM0 AP interface: '0': Disabled. '1': Enabled. Default Value: 0

4.1.29 CPUSS_BUFF_CTL

Buffer control

Address: 0x40201500

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							WRITE_BUFF

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	WRITE_BUFF	Specifies if write transfer can be buffered in the bus infrastructure bridges: '0': Write transfers are not buffered, independent of the transfer's bufferable attribute. '1': Write transfers can be buffered, if the transfer's bufferable attribute indicates that the transfer is a bufferable/posted write. Default Value: 1

4.1.30 CPUSS_SYSTICK_CTL

SysTick timer control

Address: 0x40201600

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TENMS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TENMS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	TENMS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None				RW	
HW Access	R	R	None				R	
Name	NOREF	SKEW	None [29:26]				CLOCK_SOURCE [25:24]	

Bits	Name	Description
31	NOREF	Specifies if an external clock source is provided: '0': An external clock source is provided. '1': An external clock source is NOT provided and only the CPU internal clock can be used as SysTick timer clock source. Default Value: 0
30	SKEW	Specifies the precision of the clock source and if the TENMS field represents exactly 10 ms (clock source frequency is a multiple of 100 Hz). This affects the suitability of the SysTick timer as a SW real-time clock: '0': Precise. '1': Imprecise. Default Value: 1

4.1.30 CPUSS_SYSTICK_CTL (continued)

25 : 24	CLOCK_SOURCE	Specifies an external clock source: "0": The low frequency clock "clk_lf" is selected. The precision of this clock depends on whether the low frequency clock source is a SRSS internal RC oscillator (imprecise) or a device external crystal oscillator (precise). "1": The internal main oscillator (IMO) clock "clk_imo" is selected. The MXS40 platform uses a fixed frequency IMO clock. o "2": The external crystal oscillator (ECO) clock "clk_eco" is selected. "3": The SRSS "clk_timer" is selected ("clk_timer" is a divided/gated version of "clk_hf" or "clk_imo"). Note: If NOREF is '1', the CLOCK_SOURCE value is NOT used. Note: It is SW's responsibility to provide the correct NOREF, SKEW and TENMS field values for the selected clock source. Default Value: 0
23 : 0	TENMS	Specifies the number of clock source cycles (minus 1) that make up 10 ms. E.g., for a 32,768 Hz reference clock, TENMS is 328 - 1 = 327. Default Value: 327

4.1.31 CPUSS_MBIST_STAT

Memory BIST status

Address: 0x40201704

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						RW	RW
Name	None [7:2]						SFP_FAIL	SFP_READY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	SFP_FAIL	Report status of the BIST run, only valid if SFP_READY=1 Default Value: 0
0	SFP_READY	Flag indicating the BIST run is done. Note that after starting a BIST run this flag must be set before a new run can be started. For the first BIST run this will be 0. Default Value: 0

4.1.32 CPUSS_CAL_SUP_SET

Calibration support set and read

Address: 0x40201800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Read without side effect, write 1 to set Default Value: 0

4.1.33 CPUSS_CAL_SUP_CLR

Calibration support clear and reset

Address: 0x40201804

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	A							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	A							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	A							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Read side effect: when read all bits are cleared, write 1 to clear a specific bit Note: no exception for the debug host, it also causes the read side effect Default Value: 0

4.1.34 CPUSS_CM0_PC_CTL

CM0+ protection context control

Address: 0x40202000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				VALID [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	VALID	Valid fields for the protection context handler CM0_PCi_HANDLER registers: Bit 0: Valid field for CM0_PC0_HANDLER. Bit 1: Valid field for CM0_PC1_HANDLER. Bit 2: Valid field for CM0_PC2_HANDLER. Bit 3: Valid field for CM0_PC3_HANDLER. Default Value: 0

4.1.35 CPUSS_CM0_PC0_HANDLER

CM0+ protection context 0 handler

Address: 0x40202040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Address of the protection context 0 handler. This field is used to detect entry to Cypress "trusted" code through an exception/interrupt. Default Value: 0

4.1.36 CPUSS_CM0_PC1_HANDLER

CM0+ protection context 1 handler

Address: 0x40202044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Address of the protection context 1 handler. Default Value: 0

4.1.37 CPUSS_CM0_PC2_HANDLER

CM0+ protection context 2 handler

Address: 0x40202048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Address of the protection context 2 handler. Default Value: 0

4.1.38 CPUSS_CM0_PC3_HANDLER

CM0+ protection context 3 handler

Address: 0x4020204C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Address of the protection context 3 handler. Default Value: 0

4.1.39 CPUSS_PROTECTION

Protection status

Address: 0x402020C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					STATE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	STATE	Protection state: "0": UNKNOWN. "1": VIRGIN. "2": NORMAL. "3": SECURE. "4": DEAD. The following state transitions are allowed (and enforced by HW): - UNKNOWN => VIRGIN/NORMAL/SECURE/DEAD - NORMAL => DEAD - SECURE => DEAD An attempt to make a NOT allowed state transition will NOT affect this register field. Default Value: 0

4.1.40 CPUSS_TRIM_ROM_CTL

ROM trim control

Address: 0x40202100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			TRIM [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	TRIM	For ARM ROMs the bits are defined as follows [2:0] EMA: Extra Margin Adjustment (0 is the fastest setting) Recommended default value: EMA=2 (ROM_TRIM_DEFAULT=0x0000_0002, ROM_TRIM_WIDTH=3) For Synopsys ROMs the bits are defined as follows: [3:0] RM: Read-Write margin control. This is used for setting the Read-Write margin. It programs the sense amplifier differential setting and allows the trade off between speed and robustness. - RM[1:0] values control access time and cycle time of the memory. RM[1:0] = "0" is the slowest possible mode of operation for the memory. This setting is required for VDDMIN operation. - RM[3:2] are factory pins reserved for debug mode and should be set to "0". [4] RME: Read-Write margin enable control. This selects between the default Read-Write margin setting, and the external pin Read-Write margin setting. Recommended default value for LP: RME=1, RM=2 (ROM_TRIM_DEFAULT=0x0000_0012, ROM_TRIM_WIDTH=5) Recommended default value for ULP: RME=1, RM=3 (ROM_TRIM_DEFAULT=0x0000_0013, ROM_TRIM_WIDTH=5) Default Value: 18

4.1.41 CPUSS_TRIM_RAM_CTL

RAM trim control

Address: 0x40202104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TRIM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW						
HW Access	None	R						
Name	None	TRIM [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description

4.1.41 CPUSS_TRIM_RAM_CTL (continued)

14 : 0	TRIM	For ARM RAMs the bits are defined as follows [2:0] EMA: Extra Margin Adjustment (0 is the fastest setting) [4:3] EMAW: Extra Margin Adjustment for Writes (0 is the fastest setting) [7:5] CTL_BIAS: Control the bias circuit in the SRAM power switches for SRAMC0: 0=OFF, 7=max Recommended default value: CTL_BIAS=3, EMAW=0, EMA=2 (RAM_TRIM_DEFAULT=0x0000_0062, RAM_TRIM_WIDTH=8) For Synopsys RAMs the bits are defined as follows: [3:0] Read-Write margin control. This is used for setting the Read-Write margin. It programs the sense amplifier differential setting and allows the trade off between speed and robustness. - RM[1:0] values control access time and cycle time of the memory. RM[1:0] = "0" is the slowest possible mode of operation for the memory. This setting is required for VDDMIN operation. - RM[3:2] are factory pins reserved for debug mode and should be set to "0". [4] RME: Read-Write margin enable control. This selects between the default Read-Write margin setting, and the external RM[3:0] Read-Write margin setting. [7:5] WPULSE: Write Assist Pulse to control pulse width of negative voltage on SRAM bitline. [9:8] RA: Read Assist control for WL under-drive. [14:12] WA: Write assist enable control (Active High). - WA[2:0] Write Assist pins to control negative voltage on SRAM bitline. Recommended default value for LP: WA=4, RA=0, WPULSE=0, RME=1, RM=3 (RAM_TRIM_DEFAULT=0x0000_4013, RAM_TRIM_WIDTH=15) Recommended default value for ULP: WA=6, RA=0, WPULSE=0, RME=1, RM=2 (RAM_TRIM_DEFAULT=0x0000_6012, RAM_TRIM_WIDTH=15) Default Value: 24594

4.1.42 CPUSS_CM0_SYSTEM_INT_CTL0

CM0+ system interrupt control

Address: 0x40208000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					CPU_INT_IDX [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	CPU_INT_VALID	None [30:24]						

Bits	Name	Description
31	CPU_INT_VALID	Interrupt enable: '0': Disabled. The system interrupt will NOT be mapped to any CPU interrupt. '1': Enabled. The system interrupt is mapped on CPU interrupt CPU_INT_IDX. Note: the CPUs have dedicated XXX_SYSTEM_INT_CTL registers. In other words, the CPUs can use different CPU interrupts for the same system interrupt. However, typically only one of the CPUs will have the ENABLED field of a specific system interrupt set to '1'. Default Value: 0
2 : 0	CPU_INT_IDX	CPU interrupt index (legal range [0, 7]). This field specifies to which CPU interrupt the system interrupt is mapped. E.g., if CPU_INT_IDX is "6", the system interrupt is mapped to CPU interrupt "6". Note: it is possible to map multiple system interrupts to the same CPU interrupt. It is advised to assign different priorities to the CPU interrupts and to assign system interrupts to CPU interrupts accordingly. Default Value: Undefined

5 Fault Registers

This section discusses the Fault registers. It lists all the registers in mapping tables, in address order.

5.1 Register Details

Register	Address	Description
FAULT_STRUCT0_CTL	0x40210000	Fault control
FAULT_STRUCT0_STATUS	0x4021000C	Fault status
FAULT_STRUCT0_DATA0	0x40210010	Fault data
FAULT_STRUCT0_DATA1	0x40210014	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT0_DATA2	0x40210018	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT0_DATA3	0x4021001C	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT0_PENDING0	0x40210040	Fault pending 0
FAULT_STRUCT0_PENDING1	0x40210044	Fault pending 1
FAULT_STRUCT0_PENDING2	0x40210048	Fault pending 2
FAULT_STRUCT0_MASK0	0x40210050	Fault mask 0
FAULT_STRUCT0_MASK1	0x40210054	Fault mask 1
FAULT_STRUCT0_MASK2	0x40210058	Fault mask 2
FAULT_STRUCT0_INTR	0x402100C0	Interrupt
FAULT_STRUCT0_INTR_SET	0x402100C4	Interrupt set
FAULT_STRUCT0_INTR_MASK	0x402100C8	Interrupt mask
FAULT_STRUCT0_INTR_MASKED	0x402100CC	Interrupt masked
FAULT_STRUCT1_CTL	0x40210100	Fault control. See FAULT_STRUCT0_CTL for the details of bit fields.
FAULT_STRUCT1_STATUS	0x4021010C	Fault status. See FAULT_STRUCT0_STATUS for the details of bit fields.
FAULT_STRUCT1_DATA0	0x40210110	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT1_DATA1	0x40210114	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT1_DATA2	0x40210118	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT1_DATA3	0x4021011C	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT1_PENDING0	0x40210140	Fault pending 0. See FAULT_STRUCT0_PENDING0 for the details of bit fields.
FAULT_STRUCT1_PENDING1	0x40210144	Fault pending 1. See FAULT_STRUCT0_PENDING1 for the details of bit fields.
FAULT_STRUCT1_PENDING2	0x40210148	Fault pending 2. See FAULT_STRUCT0_PENDING2 for the details of bit fields.
FAULT_STRUCT1_MASK0	0x40210150	Fault mask 0. See FAULT_STRUCT0_MASK0 for the details of bit fields.
FAULT_STRUCT1_MASK1	0x40210154	Fault mask 1. See FAULT_STRUCT0_MASK1 for the details of bit fields.

Register	Address	Description
FAULT_STRUCT1_MASK2	0x40210158	Fault mask 2. See FAULT_STRUCT0_MASK2 for the details of bit fields.
FAULT_STRUCT1_INTR	0x402101C0	Interrupt. See FAULT_STRUCT0_INTR for the details of bit fields.
FAULT_STRUCT1_INTR_SET	0x402101C4	Interrupt set. See FAULT_STRUCT0_INTR_SET for the details of bit fields.
FAULT_STRUCT1_INTR_MASK	0x402101C8	Interrupt mask. See FAULT_STRUCT0_INTR_MASK for the details of bit fields.
FAULT_STRUCT1_INTR_MASKED	0x402101CC	Interrupt masked. See FAULT_STRUCT0_INTR_MASKED for the details of bit fields.

5.1.1 FAULT_STRUCT0_CTL

Fault control

Address: 0x40210000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					RESET_REQ_EN	OUT_EN	TR_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	RESET_REQ_EN	Reset request enable: '0': Disabled. '1': Enabled. The output reset request signal "fault_reset_req" reflects STATUS.VALID. This reset causes a warm/soft/core reset. This warm/soft/core reset does not affect the fault logic STATUS, DATA0, ..., DATA3 registers (allowing for post soft reset failure analysis). The "fault_reset_req" signals of the individual fault report structures are combined (logically OR'd) into a single SRSS "fault_reset_req" signal. Default Value: 0
1	OUT_EN	IO output signal enable: '0': Disabled. The IO output signal "fault_out" is '0'. The IO output enable signal "fault_out_en" is '0'. '1': Enabled. The IO output signal "fault_out" reflects STATUS.VALID. The IO output enable signal "fault_out_en" is '1'. Default Value: 0

5.1.1 FAULT_STRUCT0_CTL (continued)

0	TR_EN	Trigger output enable: '0': Disabled. The trigger output "tr_fault" is '0'. '1': Enabled. The trigger output "tr_fault" reflects STATUS.VALID. The trigger can be used to initiate a Datawire transfer of the FAULT data (FAULT_DATA0 through FAULT_DATA3). Default Value: 0

5.1.2 FAULT_STRUCT0_STATUS

Fault status

Address: 0x4021000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	W						
Name	None	IDX [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW1S	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	Valid indication: '0': Invalid. '1': Valid. STATUS.IDX, DATA0, ..., DATA3 specify the fault. Note: Typically, HW sets this field to '1' (on an activated HW fault source that is "enabled" by the MASK registers) and SW clears this field to '0' (typically by boot code SW (after a warm system reset, when the fault is handled). In this typical use case scenario, the HW source fault data is simultaneously captured into DATA0, ..., DATA3 when the VALID field is set to '1'. An exceptional SW use case scenario is identified as well. In this scenario, SW sets this field to '1' with a fault source index different to one of the defined HW fault sources. SW update is not restricted by the MASK registers). In both use case scenarios, the following holds: - STATUS.IDX, DATA0, ..., DATA3 can only be written when STATUS.VALID is '0'; the fault structure is not in use yet. Writing STATUS.VALID to '1' effectively locks the fault structure (until SW clears STATUS.VALID to '0'). This restriction requires a SW update to sequentially update the DATA registers followed by an update of the STATUS register. Note: For the exceptional SW use case, sequential updates to the DATA and STATUS registers may be "interrupted" by a HW fault capture. In this case, the SW DATA register updates are over-written by the HW update (and the STATUS.IDX field will reflect the HW capture) Default Value: 0

5.1.2 FAULT_STRUCT0_STATUS (continued)

6 : 0	IDX	The fault source index for which fault information is captured in DATA0 through DATA3. The fault information is fault source specific and described below. Note: this register field (and associated fault source data in DATA0 through DATA3) should only be considered valid, when VALID is '1'. Default Value: Undefined **0x0: MPU_0 :** Bus master 0 MPU/SMPU. DATA0[31:0]: Violating address. DATA1[0]: User read. DATA1[1]: User write. DATA1[2]: User execute. DATA1[3]: Privileged read. DATA1[4]: Privileged write. DATA1[5]: Privileged execute. DATA1[6]: Non-secure. DATA1[11:8]: Master identifier. DATA1[15:12]: Protection context identifier. DATA1[31]: '0' MPU violation; '1': SMPU violation. **0x1: MPU_1 :** Bus master 1 MPU. See MPU_0 description. **0x2: MPU_2 :** Bus master 2 MPU. See MPU_0 description. **0x3: MPU_3 :** Bus master 3 MPU. See MPU_0 description. **0x4: MPU_4 :** Bus master 4 MPU. See MPU_0 description. **0x5: MPU_5 :** Bus master 5 MPU. See MPU_0 description. **0x6: MPU_6 :** Bus master 6 MPU. See MPU_0 description. **0x7: MPU_7 :** Bus master 7 MPU. See MPU_0 description. **0x8: MPU_8 :** Bus master 8 MPU. See MPU_0 description.

5.1.2 FAULT_STRUCT0_STATUS (continued)

0x9: MPU_9 :

Bus master 9 MPU. See MPU_0 description.

0xa: MPU_10 :

Bus master 10 MPU. See MPU_0 description.

0xb: MPU_11 :

Bus master 11 MPU. See MPU_0 description.

0xc: MPU_12 :

Bus master 12 MPU. See MPU_0 description.

0xd: MPU_13 :

Bus master 13 MPU. See MPU_0 description.

0xe: MPU_14 :

Bus master 14 MPU. See MPU_0 description.

0xf: MPU_15 :

Bus master 15 MPU. See MPU_0 description.

0x10: CM4_SYS_MPU :

CM4 system bus AHB-Lite interface MPU. See MPU_0 description.

0x11: CM4_CODE_MPU :

CM4 code bus AHB-Lite interface MPU for non flash controller accesses. See MPU_0 description.

0x12: CM4_CODE_FLASHC_MPU :

CM4 code bus AHB-Lite interface MPU for flash controller accesses. See MPU_0 description.

0x19: MS_PPU_4 :

Peripheral interconnect, master interface 4 PPU. See MS_PPU_0 description.

0x1a: PERI_ECC :

Peripheral interconnect, protection structures SRAM, correctable ECC error:
DATA0[10:0]: Violating address.
DATA1[7:0]: Syndrome of SRAM word.

5.1.2 FAULT_STRUCT0_STATUS (continued)

0x1b: PERI_NC_ECC :

Peripheral interconnect, protection structures SRAM, non-correctable ECC error. See PERI_ECC description.

0x1c: MS_PPU_0 :

Peripheral interconnect, master interface 0 PPU.
DATA0[31:0]: Violating address.
DATA1[0]: User read.
DATA1[1]: User write.
DATA1[2]: User execute.
DATA1[3]: Privileged read.
DATA1[4]: Privileged write.
DATA1[5]: Privileged execute.
DATA1[6]: Non-secure.
DATA1[11:8]: Master identifier.
DATA1[15:12]: Protection context identifier.
DATA1[31:28]: "0": master interface, PPU violation, "1': timeout detected, "2": bus error, other: undefined.

0x1d: MS_PPU_1 :

Peripheral interconnect, master interface 1 PPU. See MS_PPU_0 description.

0x1e: MS_PPU_2 :

Peripheral interconnect, master interface 2 PPU. See MS_PPU_0 description.

0x1f: MS_PPU_3 :

Peripheral interconnect, master interface 3 PPU. See MS_PPU_0 description.

0x20: GROUP_FAULT_0 :

Peripheral group 0 fault detection.
DATA0[31:0]: Violating address.
DATA1[0]: User read.
DATA1[1]: User write.
DATA1[2]: User execute.
DATA1[3]: Privileged read.
DATA1[4]: Privileged write.
DATA1[5]: Privileged execute.
DATA1[6]: Non-secure.
DATA1[11:8]: Master identifier.
DATA1[15:12]: Protection context identifier.
DATA1[31:28]: "0": decoder or peripheral bus error, other: undefined.

0x21: GROUP_FAULT_1 :

Peripheral group 1 fault detection. See GROUP_FAULT_0 description.

5.1.2 FAULT_STRUCT0_STATUS (continued)

0x22: GROUP_FAULT_2 :

Peripheral group 2 fault detection. See GROUP_FAULT_0 description.

0x23: GROUP_FAULT_3 :

Peripheral group 3 fault detection. See GROUP_FAULT_0 description.

0x24: GROUP_FAULT_4 :

Peripheral group 4 fault detection. See GROUP_FAULT_0 description.

0x25: GROUP_FAULT_5 :

Peripheral group 5 fault detection. See GROUP_FAULT_0 description.

0x26: GROUP_FAULT_6 :

Peripheral group 6 fault detection. See GROUP_FAULT_0 description.

0x27: GROUP_FAULT_7 :

Peripheral group 7 fault detection. See GROUP_FAULT_0 description.

0x28: GROUP_FAULT_8 :

Peripheral group 8 fault detection. See GROUP_FAULT_0 description.

0x29: GROUP_FAULT_9 :

Peripheral group 9 fault detection. See GROUP_FAULT_0 description.

0x2a: GROUP_FAULT_10 :

Peripheral group 10 fault detection. See GROUP_FAULT_0 description.

0x2b: GROUP_FAULT_11 :

Peripheral group 11 fault detection. See GROUP_FAULT_0 description.

0x2c: GROUP_FAULT_12 :

Peripheral group 12 fault detection. See GROUP_FAULT_0 description.

0x2d: GROUP_FAULT_13 :

Peripheral group 13 fault detection. See GROUP_FAULT_0 description.

5.1.2 FAULT_STRUCT0_STATUS (continued)

0x2e: GROUP_FAULT_14 :

Peripheral group 14 fault detection. See GROUP_FAULT_0 description.

0x2f: GROUP_FAULT_15 :

Peripheral group 15 fault detection. See GROUP_FAULT_0 description.

0x30: FLASHC_MAIN_BUS_ERROR :

Flash controller, main interface, bus error:
FAULT_DATA0[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address.
FAULT_DATA1[11:8]: Master identifier.

0x31: FLASHC_MAIN_C_ECC :

Flash controller, main interface, correctable ECC error:
DATA[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address.
DATA1[7:0]: Syndrome of 64-bit word (at address offset 0x00).
DATA1[15:8]: Syndrome of 64-bit word (at address offset 0x08).
DATA1[23:16]: Syndrome of 64-bit word (at address offset 0x10).
DATA1[31:24]: Syndrome of 64-bit word (at address offset 0x18).

0x32: FLASHC_MAIN_NC_ECC :

Flash controller, main interface, non-correctable ECC error. See FLASHC_MAIN_C_ECC description.

0x33: FLASHC_WORK_BUS_ERROR :

Flash controller, work interface, bus error.
FAULT_DATA0[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address.
FAULT_DATA1[11:8]: Master identifier.

0x34: FLASHC_WORK_C_ECC :

Flash controller, work interface, correctable ECC error:
DATA0[26:0]: Violating address. Append 5'b00010 as most significant bits to derive 32-bit system address.
DATA1[6:0]: Syndrome of 32-bit word.

0x35: FLASHC_WORK_NC_ECC :

Flash controller, work interface, non-correctable ECC error. See FLASHC_WORK_C_ECC description.

5.1.2 FAULT_STRUCT0_STATUS (continued)

0x36: FLASHC_CM0_CA_C_ECC :

Flash controller, CM0+ cache, correctable ECC error:
DATA0[26:0]: Violating address.
DATA1[6:0]: Syndrome of 32-bit SRAM word (at address offset 0x0).
DATA1[14:8]: Syndrome of 32-bit SRAM word (at address offset 0x4).
DATA1[22:16]: Syndrome of 32-bit SRAM word (at address offset 0x8).
DATA1[30:24]: Syndrome of 32-bit SRAM word (at address offset 0xc).

0x37: FLASHC_CM0_CA_NC_ECC :

Flash controller, CM0+ cache, non-correctable ECC error. See FLASHC_CM0_CA_C_ECC description.

0x38: FLASHC_CM4_CA_C_ECC :

Flash controller, CM4 cache, correctable ECC error. See FLASHC_CM0_CA_C_ECC description.

0x39: FLASHC_CM4_CA_NC_ECC :

Flash controller, CM4 cache, non-correctable ECC error. See FLASHC_CM0_CA_C_ECC description.

0x3a: RAMC0_C_ECC :

System SRAM 0 correctable ECC error:
DATA0[31:0]: Violating address.
DATA1[6:0]: Syndrome of 32-bit SRAM code word.

0x3b: RAMC0_NC_ECC :

System SRAM 0 non-correctable ECC error. See RAMC0_C_ECC description.

0x3c: RAMC1_C_ECC :

System SRAM 1 correctable ECC error. See RAMC0_C_ECC description.

0x3d: RAMC1_NC_ECC :

System SRAM 1 non-correctable ECC error. See RAMC0_C_ECC description.

0x3e: RAMC2_C_ECC :

System SRAM 2 correctable ECC error. See RAMC0_C_ECC description.

0x3f: RAMC2_NC_ECC :

System SRAM 2 non-correctable ECC error. See RAMC0_C_ECC description.

5.1.2 FAULT_STRUCT0_STATUS (continued)

0x40: CRYPTO_C_ECC :

Cryptography SRAM correctable ECC error.
DATA0[31:0]: Violating address.
DATA1[6:0]: Syndrome of Least Significant 32-bit SRAM.
DATA1[14:8]: Syndrome of Most Significant 32-bit SRAM.

0x41: CRYPTO_NC_ECC :

Cryptography SRAM non-correctable ECC error. See CRYPTO_C_ECC description.

0x46: DW0_C_ECC :

DataWire 0 SRAM 1 correctable ECC error:
DATA0[11:0]: Violating DW SRAM address (word address, assuming byte addressable).
DATA1[6:0]: Syndrome of 32-bit SRAM code word.

0x47: DW0_NC_ECC :

DataWire 0 SRAM 1 non-correctable ECC error. See DW0_C_ECC description.

0x48: DW1_C_ECC :

DataWire 1 SRAM 1 correctable ECC error. See DW0_C_ECC description.

0x49: DW1_NC_ECC :

DataWire 1 SRAM 1 non-correctable ECC error. See DW0_C_ECC description.

0x4a: FM_SRAM_C_ECC :

eCT Flash SRAM (for embedded operations) correctable ECC error:
DATA0[15:0]: Address location in the eCT Flash SRAM.
DATA1[6:0]: Syndrome of 32-bit SRAM word.

0x4b: FM_SRAM_NC_ECC :

eCT Flash SRAM non-correctable ECC error: See FM_SRAM_C_ECC description.

0x50: CAN0_C_ECC :

CAN controller 0 MRAM correctable ECC error:
DATA0[15:0]: Violating address.
DATA0[22:16]: ECC violating data[38:32] from MRAM.
DATA0[27:24]: Master ID: 0-7 = CAN channel ID within mxttcanfd cluster, 8 = AHB I/F
DATA1[31:0]: ECC violating data[31:0] from MRAM.

5.1.2 FAULT_STRUCT0_STATUS (continued)

0x51: CAN0_NC_ECC :

CAN controller 0 MRAM non-correctable ECC error:
DATA0[15:0]: Violating address.
DATA0[22:16]: ECC violating data[38:32] from MRAM (not for Address Error).
DATA0[27:24]: Master ID: 0-7 = CAN channel ID within mxttcanfd cluster, 8 = AHB I/F
DATA0[30]: Write access, only possible for Address Error
DATA0[31]: Address Error: a CAN channel did an MRAM access above MRAM_SIZE
DATA1[31:0]: ECC violating data[31:0] from MRAM (not for Address Error).

0x52: CAN1_C_ECC :

CAN controller 1 MRAM correctable ECC error. See CAN0_C_ECC description.

0x53: CAN1_NC_ECC :

CAN controller 1 MRAM non-correctable ECC error. See CAN0_NC_ECC description.

0x54: CAN2_C_ECC :

CAN controller 2 MRAM correctable ECC error. See CAN0_C_ECC description.

0x55: CAN2_NC_ECC :

CAN controller 2 MRAM non-correctable ECC error. See CAN0_NC_ECC description.

0x5a: SRSS_CSV :

SRSS Clock SuperVisor (CSV) violation detected. Multiple CSV can detect a violation at the same time.
DATA0[15:0]: CSV violation occurred on corresponding clk_hf* root clock
DATA0[24]: CSV violation occurred on reference clock for clk_hf CSVs
DATA0[25]: CSV violation occurred on clk_lf
DATA0[26]: CSV violation occurred on clk_ilo0

0x5b: SRSS_SSV :

SRSS Supply SuperVisor (SSV) violation detected. Multiple SSV can detect a violation at the same time.
DATA0[0]: BOD detected on VDDA
DATA0[1]: OVD detected on VDDA
DATA0[16]: violation detected on LVD/HVD #1
DATA0[17]: violation detected on LVD/HVD #2

0x5c: SRSS_MCWDT0 :

SRSS Multi-Counter Watch Dog Timer (MCWDT) #0 violation detected. Multiple counters can detect a violation at the same time.
DATA0[0]: MCWDT subcounter 0 LOWER_LIMIT
DATA0[1]: MCWDT subcounter 0 UPPER_LIMIT
DATA0[2]: MCWDT subcounter 1 LOWER_LIMIT
DATA0[3]: MCWDT subcounter 1 UPPER_LIMIT

5.1.2 FAULT_STRUCT0_STATUS (continued)

0x5d: SRSS_MCWDT1 :

SRSS Multi-Counter Watch Dog Timer (MCWDT) #1 violation detected. See SRSS_MCWDT0 description.

0x5e: SRSS_MCWDT2 :

SRSS Multi-Counter Watch Dog Timer (MCWDT) #2 violation detected. See SRSS_MCWDT0 description.

0x5f: SRSS_MCWDT3 :

SRSS Multi-Counter Watch Dog Timer (MCWDT) #3 violation detected. See SRSS_MCWDT0 description.

5.1.3 FAULT_STRUCT0_DATA0

Fault data

Address: 0x40210010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Captured fault source data. Note: the DATA registers can only be written when STATUS.VALID is '0'. Note: the fault source index STATUS.IDX specifies the format of the DATA registers. Default Value: Undefined

5.1.4 FAULT_STRUCT0_PENDING0

Fault pending 0

Address: 0x40210040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SOURCE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SOURCE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	SOURCE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	SOURCE [31:24]							

Bits	Name	Description
31 : 0	SOURCE	This field specifies the following sources: Bit 0: CM0 MPU. Bit 1: CRYPTO MPU. Bit 2: DW 0 MPU. Bit 3: DW 1 MPU. Bit 4: DMA controller MPU. ... Bit 15: DAP MPU. Bit 16: CM4 system bus MPU. Bit 17: CM4 code bus MPU (for non FLASH controller accesses). Bit 18: CM4 code bus MPU (for FLASH controller accesses). Default Value: Undefined

5.1.5 FAULT_STRUCT0_PENDING1

Fault pending 1

Address: 0x40210044

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SOURCE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SOURCE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	SOURCE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	SOURCE [31:24]							

Bits	Name	Description
31 : 0	SOURCE	This field specifies the following sources: Bit 0: Peripheral group 0 PPU. Bit 1: Peripheral group 1 PPU. Bit 2: Peripheral group 2 PPU. Bit 3: Peripheral group 3 PPU. Bit 4: Peripheral group 4 PPU. Bit 5: Peripheral group 5 PPU. Bit 6: Peripheral group 6 PPU. Bit 7: Peripheral group 7 PPU. ... Bit 15: Peripheral group 15 PPU. Bit 16 - 31: See STATUS register. Default Value: Undefined

5.1.6 FAULT_STRUCT0_PENDING2

Fault pending 2

Address: 0x40210048

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SOURCE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SOURCE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	SOURCE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	SOURCE [31:24]							

Bits	Name	Description
31 : 0	SOURCE	This field specifies the following sources: Bit 0 - 31: See STATUS register. Default Value: Undefined

5.1.7 FAULT_STRUCT0_MASK0

Fault mask 0

Address: 0x40210050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SOURCE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SOURCE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SOURCE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	SOURCE [31:24]							

Bits	Name	Description
31 : 0	SOURCE	Fault source enables: Bits 31-0: Fault sources 31 to 0. Default Value: 0

5.1.8 FAULT_STRUCT0_MASK1

Fault mask 1

Address: 0x40210054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SOURCE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SOURCE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SOURCE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	SOURCE [31:24]							

Bits	Name	Description
31 : 0	SOURCE	Fault source enables: Bits 31-0: Fault sources 63 to 32. Default Value: 0

5.1.9 FAULT_STRUCT0_MASK2

Fault mask 2

Address: 0x40210058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SOURCE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SOURCE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SOURCE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	SOURCE [31:24]							

Bits	Name	Description
31 : 0	SOURCE	Fault source enables: Bits 31-0: Fault sources 95 to 64. Default Value: 0

5.1.10 FAULT_STRUCT0_INTR

Interrupt

Address: 0x402100C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [7:1]							FAULT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	FAULT	This interrupt cause field is activated (HW sets the field to '1') when an enabled (MASK0/MASK1/MASK2) pending fault source is captured: - STATUS.VALID is set to '1'. - STATUS.IDX specifies the fault source index. - DATA0 through DATA3 captures the fault source data. SW writes a '1' to this field to clear the interrupt cause to '0'. SW clear STATUS.VALID to '0' to enable capture of the next fault. Note that when there is an enabled pending fault source, the pending fault source is captured immediately and INTR.FAULT is immediately activated (set to '1'). Default Value: 0

5.1.11 FAULT_STRUCT0_INTR_SET

Interrupt set

Address: 0x402100C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							A
Name	None [7:1]							FAULT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	FAULT	SW writes a '1' to this field to set the corresponding field in the INTR register. Default Value: 0

5.1.12 FAULT_STRUCT0_INTR_MASK

Interrupt mask

Address: 0x402100C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							FAULT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	FAULT	Mask bit for corresponding field in the INTR register. Default Value: 0

5.1.13 FAULT_STRUCT0_INTR_MASKED

Interrupt masked

Address: 0x402100CC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							FAULT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	FAULT	Logical and of corresponding INTR and INTR_MASK fields. Default Value: 0

6 Inter-Processor Communication Registers

This section discusses the Inter-Processor Communication (IPC) registers. It lists all the registers in mapping tables, in address order.

6.1 Register Details

Register	Address	Description
IPC_STRUCT0_ACQUIRE	0x40220000	IPC acquire
IPC_STRUCT0_RELEASE	0x40220004	IPC release
IPC_STRUCT0_NOTIFY	0x40220008	IPC notification
IPC_STRUCT0_DATA0	0x4022000C	IPC data 0
IPC_STRUCT0_DATA1	0x40220010	IPC data 1
IPC_STRUCT0_LOCK_STATUS	0x4022001C	IPC lock status
IPC_STRUCT1_ACQUIRE	0x40220020	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT1_RELEASE	0x40220024	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT1_NOTIFY	0x40220028	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT1_DATA0	0x4022002C	IPC data 0. See IPC_STRUCT0_DATA0 for the details of bit fields.
IPC_STRUCT1_DATA1	0x40220030	IPC data 1. See IPC_STRUCT0_DATA1 for the details of bit fields.
IPC_STRUCT1_LOCK_STATUS	0x4022003C	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT2_ACQUIRE	0x40220040	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT2_RELEASE	0x40220044	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT2_NOTIFY	0x40220048	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT2_DATA0	0x4022004C	IPC data 0. See IPC_STRUCT0_DATA0 for the details of bit fields.
IPC_STRUCT2_DATA1	0x40220050	IPC data 1. See IPC_STRUCT0_DATA1 for the details of bit fields.
IPC_STRUCT2_LOCK_STATUS	0x4022005C	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT3_ACQUIRE	0x40220060	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT3_RELEASE	0x40220064	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT3_NOTIFY	0x40220068	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT3_DATA0	0x4022006C	IPC data 0. See IPC_STRUCT0_DATA0 for the details of bit fields.
IPC_STRUCT3_DATA1	0x40220070	IPC data 1. See IPC_STRUCT0_DATA1 for the details of bit fields.
IPC_STRUCT3_LOCK_STATUS	0x4022007C	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT4_ACQUIRE	0x40220080	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT4_RELEASE	0x40220084	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.

Register	Address	Description
IPC_STRUCT4_NOTIFY	0x40220088	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT4_DATA0	0x4022008C	IPC data 0. See IPC_STRUCT0_DATA0 for the details of bit fields.
IPC_STRUCT4_DATA1	0x40220090	IPC data 1. See IPC_STRUCT0_DATA1 for the details of bit fields.
IPC_STRUCT4_LOCK_STATUS	0x4022009C	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT5_ACQUIRE	0x402200A0	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT5_RELEASE	0x402200A4	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT5_NOTIFY	0x402200A8	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT5_DATA0	0x402200AC	IPC data 0. See IPC_STRUCT0_DATA0 for the details of bit fields.
IPC_STRUCT5_DATA1	0x402200B0	IPC data 1. See IPC_STRUCT0_DATA1 for the details of bit fields.
IPC_STRUCT5_LOCK_STATUS	0x402200BC	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT6_ACQUIRE	0x402200C0	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT6_RELEASE	0x402200C4	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT6_NOTIFY	0x402200C8	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT6_DATA0	0x402200CC	IPC data 0. See IPC_STRUCT0_DATA0 for the details of bit fields.
IPC_STRUCT6_DATA1	0x402200D0	IPC data 1. See IPC_STRUCT0_DATA1 for the details of bit fields.
IPC_STRUCT6_LOCK_STATUS	0x402200DC	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT7_ACQUIRE	0x402200E0	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT7_RELEASE	0x402200E4	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT7_NOTIFY	0x402200E8	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT7_DATA0	0x402200EC	IPC data 0. See IPC_STRUCT0_DATA0 for the details of bit fields.
IPC_STRUCT7_DATA1	0x402200F0	IPC data 1. See IPC_STRUCT0_DATA1 for the details of bit fields.
IPC_STRUCT7_LOCK_STATUS	0x402200FC	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT8_ACQUIRE	0x40220100	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT8_RELEASE	0x40220104	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT8_NOTIFY	0x40220108	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT8_DATA0	0x4022010C	IPC data 0. See IPC_STRUCT0_DATA0 for the details of bit fields.
IPC_STRUCT8_DATA1	0x40220110	IPC data 1. See IPC_STRUCT0_DATA1 for the details of bit fields.
IPC_STRUCT8_LOCK_STATUS	0x4022011C	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT9_ACQUIRE	0x40220120	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT9_RELEASE	0x40220124	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT9_NOTIFY	0x40220128	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT9_DATA0	0x4022012C	IPC data 0. See IPC_STRUCT0_DATA0 for the details of bit fields.
IPC_STRUCT9_DATA1	0x40220130	IPC data 1. See IPC_STRUCT0_DATA1 for the details of bit fields.
IPC_STRUCT9_LOCK_STATUS	0x4022013C	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT10_ACQUIRE	0x40220140	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT10_RELEASE	0x40220144	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT10_NOTIFY	0x40220148	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT10_DATA0	0x4022014C	IPC data 0. See IPC_STRUCT0_DATA0 for the details of bit fields.
IPC_STRUCT10_DATA1	0x40220150	IPC data 1. See IPC_STRUCT0_DATA1 for the details of bit fields.
IPC_STRUCT10_LOCK_STATUS	0x4022015C	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT11_ACQUIRE	0x40220160	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT11_RELEASE	0x40220164	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.

Register	Address	Description
IPC_STRUCT11_NOTIFY	0x40220168	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT11_DATA0	0x4022016C	IPC data 0. See IPC_STRUCT0_DATA0 for the details of bit fields.
IPC_STRUCT11_DATA1	0x40220170	IPC data 1. See IPC_STRUCT0_DATA1 for the details of bit fields.
IPC_STRUCT11_LOCK_STATUS	0x4022017C	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT12_ACQUIRE	0x40220180	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT12_RELEASE	0x40220184	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT12_NOTIFY	0x40220188	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT12_DATA0	0x4022018C	IPC data 0. See IPC_STRUCT0_DATA0 for the details of bit fields.
IPC_STRUCT12_DATA1	0x40220190	IPC data 1. See IPC_STRUCT0_DATA1 for the details of bit fields.
IPC_STRUCT12_LOCK_STATUS	0x4022019C	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT13_ACQUIRE	0x402201A0	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT13_RELEASE	0x402201A4	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT13_NOTIFY	0x402201A8	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT13_DATA0	0x402201AC	IPC data 0. See IPC_STRUCT0_DATA0 for the details of bit fields.
IPC_STRUCT13_DATA1	0x402201B0	IPC data 1. See IPC_STRUCT0_DATA1 for the details of bit fields.
IPC_STRUCT13_LOCK_STATUS	0x402201BC	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT14_ACQUIRE	0x402201C0	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT14_RELEASE	0x402201C4	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT14_NOTIFY	0x402201C8	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT14_DATA0	0x402201CC	IPC data 0. See IPC_STRUCT0_DATA0 for the details of bit fields.
IPC_STRUCT14_DATA1	0x402201D0	IPC data 1. See IPC_STRUCT0_DATA1 for the details of bit fields.
IPC_STRUCT14_LOCK_STATUS	0x402201DC	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT15_ACQUIRE	0x402201E0	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT15_RELEASE	0x402201E4	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT15_NOTIFY	0x402201E8	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT15_DATA0	0x402201EC	IPC data 0. See IPC_STRUCT0_DATA0 for the details of bit fields.
IPC_STRUCT15_DATA1	0x402201F0	IPC data 1. See IPC_STRUCT0_DATA1 for the details of bit fields.
IPC_STRUCT15_LOCK_STATUS	0x402201FC	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_INTR_STRUCT0_INTR	0x40221000	Interrupt
IPC_INTR_STRUCT0_INTR_SET	0x40221004	Interrupt set
IPC_INTR_STRUCT0_INTR_MASK	0x40221008	Interrupt mask
IPC_INTR_STRUCT0_INTR_MASKED	0x4022100C	Interrupt masked
IPC_INTR_STRUCT1_INTR	0x40221020	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT1_INTR_SET	0x40221024	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT1_INTR_MASK	0x40221028	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT1_INTR_MASKED	0x4022102C	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.
IPC_INTR_STRUCT2_INTR	0x40221040	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT2_INTR_SET	0x40221044	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT2_INTR_MASK	0x40221048	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT2_INTR_MASKED	0x4022104C	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.
IPC_INTR_STRUCT3_INTR	0x40221060	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT3_INTR_SET	0x40221064	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.

Register	Address	Description
IPC_INTR_STRUCT3_INTR_MASK	0x40221068	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT3_INTR_MASKED	0x4022106C	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.
IPC_INTR_STRUCT4_INTR	0x40221080	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT4_INTR_SET	0x40221084	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT4_INTR_MASK	0x40221088	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT4_INTR_MASKED	0x4022108C	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.
IPC_INTR_STRUCT5_INTR	0x402210A0	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT5_INTR_SET	0x402210A4	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT5_INTR_MASK	0x402210A8	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT5_INTR_MASKED	0x402210AC	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.
IPC_INTR_STRUCT6_INTR	0x402210C0	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT6_INTR_SET	0x402210C4	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT6_INTR_MASK	0x402210C8	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT6_INTR_MASKED	0x402210CC	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.
IPC_INTR_STRUCT7_INTR	0x402210E0	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT7_INTR_SET	0x402210E4	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT7_INTR_MASK	0x402210E8	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT7_INTR_MASKED	0x402210EC	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.
IPC_INTR_STRUCT8_INTR	0x40221100	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT8_INTR_SET	0x40221104	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT8_INTR_MASK	0x40221108	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT8_INTR_MASKED	0x4022110C	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.
IPC_INTR_STRUCT9_INTR	0x40221120	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT9_INTR_SET	0x40221124	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT9_INTR_MASK	0x40221128	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT9_INTR_MASKED	0x4022112C	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.
IPC_INTR_STRUCT10_INTR	0x40221140	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT10_INTR_SET	0x40221144	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT10_INTR_MASK	0x40221148	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT10_INTR_MASKED	0x4022114C	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.
IPC_INTR_STRUCT11_INTR	0x40221160	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT11_INTR_SET	0x40221164	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT11_INTR_MASK	0x40221168	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT11_INTR_MASKED	0x4022116C	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.
IPC_INTR_STRUCT12_INTR	0x40221180	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT12_INTR_SET	0x40221184	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT12_INTR_MASK	0x40221188	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT12_INTR_MASKED	0x4022118C	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.
IPC_INTR_STRUCT13_INTR	0x402211A0	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT13_INTR_SET	0x402211A4	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT13_INTR_MASK	0x402211A8	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT13_INTR_MASKED	0x402211AC	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.

Register	Address	Description
IPC_INTR_STRUCT14_INTR	0x402211C0	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT14_INTR_SET	0x402211C4	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT14_INTR_MASK	0x402211C8	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT14_INTR_MASKED	0x402211CC	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.
IPC_INTR_STRUCT15_INTR	0x402211E0	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT15_INTR_SET	0x402211E4	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT15_INTR_MASK	0x402211E8	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT15_INTR_MASKED	0x402211EC	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.

6.1.1 IPC_STRUCT0_ACQUIRE

IPC acquire

Address: 0x40220000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None		R	R
HW Access	W				None		W	W
Name	PC [7:4]				None [3:2]		NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				MS [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	SUCCESS	None [30:24]						

Bits	Name	Description
31	SUCCESS	Specifies if the lock is successfully acquired or not (reading the ACQUIRE register can have affect on SUCCESS and LOCK_STATUS.ACQUIRED): '0': Not successfully acquired; i.e. the lock was already acquired by another read transaction and not released. The P, NS, PC and MS fields reflect the access attributes of the transaction that previously successfully acuired the lock; the fields are NOT affected by the current access. '1': Successfully acquired. The P, NS, PC and MS fields reflect the access attributes of the current access. Note that this field is NOT SW writable. A lock is released by writing to the associated RELEASE register (irrespective of the write value). Default Value: 0
11 : 8	MS	This field specifies the bus master identifier that successfully acquired the lock. Default Value: Undefined
7 : 4	PC	This field specifies the protection context that successfully acquired the lock. Default Value: Undefined

6.1.1 IPC_STRUCT0_ACQUIRE (continued)

1	NS	Secure/non-secure access control: '0': secure. '1': non-secure. This field is set with the secure/non-secure access control of the access that successfully acquired the lock. Default Value: Undefined
0	P	User/privileged access control: '0': user mode. '1': privileged mode. This field is set with the user/privileged access control of the access that successfully acquired the lock. Default Value: Undefined

6.1.2 IPC_STRUCT0_RELEASE

IPC release

Address: 0x40220004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access								
Name	INTR_RELEASE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access								
Name	INTR_RELEASE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	INTR_RELEASE	Writing this field releases a lock and allows for the generation of release events to the IPC interrupt structures, but only when the lock is acquired (LOCK_STATUS.ACQUIRED is '1'). The IPC release cause fields associated with this IPC structure are set to '1', but only for those IPC interrupt structures for which the corresponding bit field in INTR_RELEASE[] is set to '1'. SW writes a '1' to the bit fields to generate a release event. Due to the transient nature of this event, SW always reads a '0' from this field. Default Value: 0

6.1.3 IPC_STRUCT0_NOTIFY

IPC notification

Address: 0x40220008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access								
Name	INTR_NOTIFY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access								
Name	INTR_NOTIFY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	INTR_NOTIFY	This field allows for the generation of notification events to the IPC interrupt structures. The IPC notification cause fields associated with this IPC structure are set to '1', but only for those IPC interrupt structures for which the corresponding bit field in INTR_NOTIFY[] is set to '1'. SW writes a '1' to the bit fields to generate a notify event. Due to the transient nature of this event, SW always reads a '0' from this field. Default Value: 0

6.1.4 IPC_STRUCT0_DATA0

IPC data 0

Address: 0x4022000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	This field holds a 32-bit data element that is associated with the IPC structure. Default Value: Undefined

6.1.5 IPC_STRUCT0_DATA1

IPC data 1

Address: 0x40220010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	This field holds a 32-bit data element that is associated with the IPC structure. Default Value: Undefined

6.1.6 IPC_STRUCT0_LOCK_STATUS

IPC lock status

Address: 0x4022001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None		R	R
HW Access	W				None		W	W
Name	PC [7:4]				None [3:2]		NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				MS [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	R	None						
Name	ACQUIRED	None [30:24]						

Bits	Name	Description
31	ACQUIRED	Specifies if the lock is acquired. This field is set to '1', if a ACQUIRE read transfer successfully acquires the lock (the ACQUIRE read transfer returns ACQUIRE.SUCCESS as '1'). If zero, P, NS, PC, and MS are not valid. Default Value: 0
11 : 8	MS	This field specifies the bus master identifier that successfully acquired the lock. Default Value: Undefined
7 : 4	PC	This field specifies the protection context that successfully acquired the lock. Default Value: Undefined
1	NS	This field specifies the secure/non-secure access control: '0': secure. '1': non-secure. Default Value: Undefined
0	P	This field specifies the user/privileged access control: '0': user mode. '1': privileged mode. Default Value: Undefined

6.1.7 IPC_INTR_STRUCT0_INTR

Interrupt

Address: 0x40221000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	RELEASE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW1S							
Name	RELEASE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	RW1S							
Name	NOTIFY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	RW1S							
Name	NOTIFY [31:24]							

Bits	Name	Description
31 : 16	NOTIFY	These interrupt cause fields are activated (HW sets the field to '1') when a IPC notification event is detected. One bit field for each master. SW writes a '1' to these field to clear the interrupt cause. Default Value: 0
15 : 0	RELEASE	These interrupt cause fields are activated (HW sets the field to '1') when a IPC release event is detected. One bit field for each master. SW writes a '1' to these field to clear the interrupt cause. Default Value: 0

6.1.8 IPC_INTR_STRUCT0_INTR_SET

Interrupt set

Address: 0x40221004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	RELEASE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	A							
Name	RELEASE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S							
HW Access	A							
Name	NOTIFY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S							
HW Access	A							
Name	NOTIFY [31:24]							

Bits	Name	Description
31 : 16	NOTIFY	SW writes a '1' to this field to set the corresponding field in the INTR register. Default Value: 0
15 : 0	RELEASE	SW writes a '1' to this field to set the corresponding field in the INTR register. Default Value: 0

6.1.9 IPC_INTR_STRUCT0_INTR_MASK

Interrupt mask

Address: 0x40221008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RELEASE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RELEASE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	NOTIFY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	NOTIFY [31:24]							

Bits	Name	Description
31 : 16	NOTIFY	Mask bit for corresponding field in the INTR register. Default Value: 0
15 : 0	RELEASE	Mask bit for corresponding field in the INTR register. Default Value: 0

6.1.10 IPC_INTR_STRUCT0_INTR_MASKED

Interrupt masked

Address: 0x4022100C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RELEASE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RELEASE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	NOTIFY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	NOTIFY [31:24]							

Bits	Name	Description
31 : 16	NOTIFY	Logical and of corresponding INTR and INTR_MASK fields. Default Value: 0
15 : 0	RELEASE	Logical and of corresponding request and mask bits. Default Value: 0

7 Protection Unit Registers

This section discusses the Protection Unit registers. It lists all the registers in mapping tables, in address order.

7.1 Register Details

Register	Address	Description
PROT_SMPU_MS0_CTL	0x40230000	Master 0 protection context control
PROT_SMPU_MS1_CTL	0x40230004	Master 1 protection context control
PROT_SMPU_MS2_CTL	0x40230008	Master 2 protection context control
PROT_SMPU_MS3_CTL	0x4023000C	Master 3 protection context control
PROT_SMPU_MS4_CTL	0x40230010	Master 4 protection context control
PROT_SMPU_MS14_CTL	0x40230038	Master 14 protection context control
PROT_SMPU_MS15_CTL	0x4023003C	Master 15 protection context control
PROT_SMPU_SMPU_STRUCT0_ADDR0	0x40232000	SMPU region address 0 (slave structure)
PROT_SMPU_SMPU_STRUCT0_ATT0	0x40232004	SMPU region attributes 0 (slave structure)
PROT_SMPU_SMPU_STRUCT0_ADDR1	0x40232020	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT0_ATT1	0x40232024	SMPU region attributes 1 (master structure)
PROT_SMPU_SMPU_STRUCT1_ADDR0	0x40232040	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT1_ATT0	0x40232044	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT1_ADDR1	0x40232060	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT1_ATT1	0x40232064	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT2_ADDR0	0x40232080	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT2_ATT0	0x40232084	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT2_ADDR1	0x402320A0	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT2_ATT1	0x402320A4	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT3_ADDR0	0x402320C0	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT3_ATT0	0x402320C4	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT3_ADDR1	0x402320E0	SMPU region address 1 (master structure)

Register	Address	Description
PROT_SMPU_SMPU_STRUCT3_ATT1	0x402320E4	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT4_ADDR0	0x40232100	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT4_ATT0	0x40232104	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT4_ADDR1	0x40232120	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT4_ATT1	0x40232124	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT5_ADDR0	0x40232140	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT5_ATT0	0x40232144	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT5_ADDR1	0x40232160	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT5_ATT1	0x40232164	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT6_ADDR0	0x40232180	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT6_ATT0	0x40232184	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT6_ADDR1	0x402321A0	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT6_ATT1	0x402321A4	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT7_ADDR0	0x402321C0	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT7_ATT0	0x402321C4	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT7_ADDR1	0x402321E0	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT7_ATT1	0x402321E4	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT8_ADDR0	0x40232200	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT8_ATT0	0x40232204	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT8_ADDR1	0x40232220	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT8_ATT1	0x40232224	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT9_ADDR0	0x40232240	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT9_ATT0	0x40232244	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT9_ADDR1	0x40232260	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT9_ATT1	0x40232264	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT10_ADDR0	0x40232280	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT10_ATT0	0x40232284	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT10_ADDR1	0x402322A0	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT10_ATT1	0x402322A4	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.

Register	Address	Description
PROT_SMPU_SMPU_STRUCT11_ADDR0	0x402322C0	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT11_ATT0	0x402322C4	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT11_ADDR1	0x402322E0	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT11_ATT1	0x402322E4	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT12_ADDR0	0x40232300	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT12_ATT0	0x40232304	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT12_ADDR1	0x40232320	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT12_ATT1	0x40232324	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT13_ADDR0	0x40232340	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT13_ATT0	0x40232344	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT13_ADDR1	0x40232360	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT13_ATT1	0x40232364	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT14_ADDR0	0x40232380	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT14_ATT0	0x40232384	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT14_ADDR1	0x402323A0	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT14_ATT1	0x402323A4	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT15_ADDR0	0x402323C0	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT15_ATT0	0x402323C4	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT15_ADDR1	0x402323E0	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT15_ATT1	0x402323E4	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_MPU0_MS_CTL	0x40234000	Master control
PROT_MPU0_MS_CTL_READ_MIR0	0x40234004	Master control read mirror. This is the starting address of a register bank containing 127 registers (PROT_MPU0_MS_CTL_READ_MIR0 to PROT_MPU0_MS_CTL_READ_MIR126).
PROT_MPU14_MS_CTL	0x40237800	Master control
PROT_MPU14_MS_CTL_READ_MIR0	0x40237804	Master control read mirror. This is the starting address of a register bank containing 127 registers (PROT_MPU14_MS_CTL_READ_MIR0 to PROT_MPU14_MS_CTL_READ_MIR126).
PROT_MPU15_MS_CTL	0x40237C00	Master control. See PROT_MPU14_MS_CTL for the details of bit fields.
PROT_MPU15_MS_CTL_READ_MIR0	0x40237C04	Master control read mirror. This is the starting address of a register bank containing 127 registers (PROT_MPU14_MS_CTL_READ_MIR0 to PROT_MPU15_MS_CTL_READ_MIR126). See PROT_MPU14_MS_CTL_READ_MIR0 for the details of bit fields.
PROT_MPU15_MPU_STRUCT0_ADDR	0x40237E00	MPU region address
PROT_MPU15_MPU_STRUCT0_ATT	0x40237E04	MPU region attrributes
PROT_MPU15_MPU_STRUCT1_ADDR	0x40237E20	MPU region address. See PROT_MPU15_MPU_STRUCT0_ADDR for the details of bit fields.

Register	Address	Description
PROT_MPU15_MPU_STRUCT1_ATT	0x40237E24	MPU region attrributes. See PROT_MPU15_MPU_STRUCT0_ATT for the details of bit fields.
PROT_MPU15_MPU_STRUCT2_ADDR	0x40237E40	MPU region address. See PROT_MPU15_MPU_STRUCT0_ADDR for the details of bit fields.
PROT_MPU15_MPU_STRUCT2_ATT	0x40237E44	MPU region attrributes. See PROT_MPU15_MPU_STRUCT0_ATT for the details of bit fields.
PROT_MPU15_MPU_STRUCT3_ADDR	0x40237E60	MPU region address. See PROT_MPU15_MPU_STRUCT0_ADDR for the details of bit fields.
PROT_MPU15_MPU_STRUCT3_ATT	0x40237E64	MPU region attrributes. See PROT_MPU15_MPU_STRUCT0_ATT for the details of bit fields.
PROT_MPU15_MPU_STRUCT4_ADDR	0x40237E80	MPU region address. See PROT_MPU15_MPU_STRUCT0_ADDR for the details of bit fields.
PROT_MPU15_MPU_STRUCT4_ATT	0x40237E84	MPU region attrributes. See PROT_MPU15_MPU_STRUCT0_ATT for the details of bit fields.
PROT_MPU15_MPU_STRUCT5_ADDR	0x40237EA0	MPU region address. See PROT_MPU15_MPU_STRUCT0_ADDR for the details of bit fields.
PROT_MPU15_MPU_STRUCT5_ATT	0x40237EA4	MPU region attrributes. See PROT_MPU15_MPU_STRUCT0_ATT for the details of bit fields.
PROT_MPU15_MPU_STRUCT6_ADDR	0x40237EC0	MPU region address. See PROT_MPU15_MPU_STRUCT0_ADDR for the details of bit fields.
PROT_MPU15_MPU_STRUCT6_ATT	0x40237EC4	MPU region attrributes. See PROT_MPU15_MPU_STRUCT0_ATT for the details of bit fields.
PROT_MPU15_MPU_STRUCT7_ADDR	0x40237EE0	MPU region address. See PROT_MPU15_MPU_STRUCT0_ADDR for the details of bit fields.
PROT_MPU15_MPU_STRUCT7_ATT	0x40237EE4	MPU region attrributes. See PROT_MPU15_MPU_STRUCT0_ATT for the details of bit fields.

7.1.1 PROT_SMPU_MS0_CTL

Master 0 protection context control

Address: 0x40230000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						PRIO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							R
HW Access	R							R
Name	PC_MASK_15_TO_1 [23:17]							PC_MASK_0

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 17	PC_MASK_15_TO_1	Protection context mask for protection contexts "15" down to "1". Bit PC_MASK_15_TO_1[i] indicates if the MPU MS_CTL.PC[3:0] protection context field can be set to the value "i+1": - PC_MASK_15_TO_1[i] is '0': MPU MS_CTL.PC[3:0] can NOT be set to "i+1"; and PC[3:0] is not changed. If the protection context of the write transfer is "0", protection is not applied and PC[3:0] can be changed. - PC_MASK_15_TO_1[i] is '1': MPU MS_CTL.PC[3:0] can be set to "i+1". Note: When CPUSS_CM0_PC_CTL.VALID[i] is '1' (the associated protection context handler is valid), write transfers to PC_MASK_15_TO_1[i-1] always write '0', regardless of data written. This ensures that when valid protection context handlers are used to enter protection contexts 1, 2 or 3 through (HW modifies MPU MS_CTL.PC[3:0] on entry of the handler), it is NOT possible for SW to enter those protection contexts (SW modifies MPU MS_CTL.PC[3:0]). Default Value: 0
16	PC_MASK_0	Protection context mask for protection context "0". This field is a constant '0': - PC_MASK_0 is '0': MPU MS_CTL.PC[3:0] can NOT be set to "0" and PC[3:0] is not changed. If the protection context of the write transfer is "0", protection is not applied and PC[3:0] can be changed. Default Value: 0

7.1.1 PROT_SMPU_MS0_CTL (continued)

9 : 8	PRIO	Device wide bus arbitration priority setting ("0": highest priority, "3": lowest priority). Notes: The AHB-Lite interconnect performs arbitration on the individual beats/transfers of a burst (this optimizes latency over locality/bandwidth). The AXI-Lite interconnects performs a single arbitration for the complete burst (this optimizes locality/bandwidth over latency). Masters with the same priority setting form a "priority group". Within a "priority group", round robin arbitration is performed. Default Value: 3
1	NS	Security setting ('0': secure mode; '1': non-secure mode). Notes: This field is ONLY used for masters that do NOT provide their own secure/non-secure access control attribute. Note that the default/reset field value provides non-secure mode access capabilities to all masters. Default Value: 1
0	P	Privileged setting ('0': user mode; '1': privileged mode). Notes: This field is ONLY used for masters that do NOT provide their own user/privileged access control attribute. The default/reset field value provides privileged mode access capabilities. Default Value: 1

7.1.2 PROT_SMPU_MS1_CTL

Master 1 protection context control

Address: 0x40230004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						PRIO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							R
Name	None [23:17]							PC_MASK_0

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	PC_MASK_0	See MS0_CTL.PC_MASK_0. Default Value: 0
9 : 8	PRIO	See MS0_CTL.PRIO Default Value: 3

7.1.3 PROT_SMPU_MS2_CTL

Master 2 protection context control

Address: 0x40230008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						PRIO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							R
Name	None [23:17]							PC_MASK_0

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	PC_MASK_0	See MS0_CTL.PC_MASK_0. Default Value: 0
9 : 8	PRIO	See MS0_CTL.PRIO Default Value: 3

7.1.4 PROT_SMPU_MS3_CTL

Master 3 protection context control

Address: 0x4023000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						PRIO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							R
Name	None [23:17]							PC_MASK_0

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	PC_MASK_0	See MS0_CTL.PC_MASK_0. Default Value: 0
9 : 8	PRIO	See MS0_CTL.PRIO Default Value: 3

7.1.5 PROT_SMPU_MS4_CTL

Master 4 protection context control

Address: 0x40230010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						PRIO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							R
Name	None [23:17]							PC_MASK_0

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	PC_MASK_0	See MS0_CTL.PC_MASK_0. Default Value: 0
9 : 8	PRIO	See MS0_CTL.PRIO Default Value: 3

7.1.6 PROT_SMPU_MS14_CTL

Master 14 protection context control

Address: 0x40230038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						PRIO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							R
HW Access	R							R
Name	PC_MASK_15_TO_1 [23:17]							PC_MASK_0

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 17	PC_MASK_15_TO_1	See MS0_CTL.PC_MASK_15_TO_1. Default Value: 0
16	PC_MASK_0	See MS0_CTL.PC_MASK_0. Default Value: 0
9 : 8	PRIO	See MS0_CTL.PRIO Default Value: 3
1	NS	See MS0_CTL.NS. Default Value: 1
0	P	See MS0_CTL.P. Default Value: 1

7.1.7 PROT_SMPU_MS15_CTL

Master 15 protection context control

Address: 0x4023003C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						PRIO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							R
HW Access	R							R
Name	PC_MASK_15_TO_1 [23:17]							PC_MASK_0

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 17	PC_MASK_15_TO_1	See MS0_CTL.PC_MASK_15_TO_1. Default Value: 0
16	PC_MASK_0	See MS0_CTL.PC_MASK_0. Default Value: 0
9 : 8	PRIO	See MS0_CTL.PRIO Default Value: 3
1	NS	See MS0_CTL.NS. Default Value: 1
0	P	See MS0_CTL.P. Default Value: 1

7.1.8 PROT_SMPU_SMPU_STRUCT0_ADDR0

SMPU region address 0 (slave structure)

Address: 0x40232000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. The region size is defined by ATT0.REGION_SIZE. A region of n Byte is always n Byte aligned. As a result, some of the lesser significant address bits of ADDR24 may be ignored in determining whether a bus transfer address is within an address region. E.g., a 64 KByte address region (REGION_-SIZE is "15") is 64 KByte aligned, and ADDR24[7:0] are ignored. Default Value: Undefined

7.1.8 PROT_SMPU_SMPU_STRUCT0_ADDR0 (continued)

7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. E.g., a 64 KByte address region (ATT0.REGION_SIZE is "15") has eight 8 KByte subregions. The access control as defined by ATT0 applies if the bus transfer address is within the address region AND the addressed subregion is NOT disabled. Note that the smallest region size is 256 B and the smallest subregion size is 32 B. Default Value: Undefined

7.1.9 PROT_SMPU_SMPU_STRUCT0_ATT0

SMPU region attributes 0 (slave structure)

Address: 0x40232004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	RW	RW	RW	RW
HW Access	None	R	R	R	R	R	R	R
Name	None	NS	PX	PW	PR	UX	UW	UR

Bits	15	14	13	12	11	10	9	8
SW Access	RW							R
HW Access	R							R
Name	PC_MASK_15_TO_1 [15:9]							PC_MASK_0

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None	RW				
HW Access	R	R	None	R				
Name	ENABLED	PC_MATCH	None	REGION_SIZE [28:24]				

Bits	Name	Description
31	ENABLED	Region enable: '0': Disabled. A disabled region will never result in a match on the bus transfer address. '1': Enabled. Note: a disabled address region performs logic gating to reduce dynamic power consumption. Default Value: 0
30	PC_MATCH	This field specifies if the PC field participates in the "matching" process or the "access evaluation" process: '0': PC field participates in "access evaluation". '1': PC field participates in "matching". "Matching" process. For each protection structure, the process identifies if a transfer address is contained within the address range. This identifies the "matching" regions. "Access evaluation" process. For each protection structure, the process evaluates the bus transfer access attributes against the access control attributes. Note that it is possible to define different access control for multiple protection contexts by using multiple protection structures with the same address region and PC_MATCH set to '1'. Default Value: Undefined

7.1.9 PROT_SMPU_SMPU_STRUCT0_ATT0 (continued)

28 : 24	REGION_SIZE	This field specifies the region size: "0"-"6": Undefined. "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "39": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: Undefined
15 : 9	PC_MASK_15_TO_1	This field specifies protection context identifier based access control. Bit i: protection context i+1 enable. If '0', protection context i+1 access is disabled; i.e. not allowed. If '1', protection context i+1 access is enabled; i.e. allowed. Default Value: Undefined
8	PC_MASK_0	This field specifies protection context identifier based access control for protection context "0". Default Value: 1
6	NS	Non-secure: '0': Secure (secure accesses allowed, non-secure access NOT allowed). '1': Non-secure (both secure and non-secure accesses allowed). Default Value: Undefined
5	PX	Privileged execute enable: '0': Disabled (privileged, execute accesses are NOT allowed). '1': Enabled (privileged, execute accesses are allowed). Default Value: Undefined
4	PW	Privileged write enable: '0': Disabled (privileged, write accesses are NOT allowed). '1': Enabled (privileged, write accesses are allowed). Default Value: Undefined
3	PR	Privileged read enable: '0': Disabled (privileged, read accesses are NOT allowed). '1': Enabled (privileged, read accesses are allowed). Default Value: Undefined
2	UX	User execute enable: '0': Disabled (user, execute accesses are NOT allowed). '1': Enabled (user, execute accesses are allowed). Default Value: Undefined

7.1.9 PROT_SMPU_SMPU_STRUCT0_ATT0 (continued)

1	UW	User write enable: '0': Disabled (user, write accesses are NOT allowed). '1': Enabled (user, write accesses are allowed). Default Value: Undefined
0	UR	User read enable: '0': Disabled (user, read accesses are NOT allowed). '1': Enabled (user, read accesses are allowed). Default Value: Undefined

7.1.10 PROT_SMPU_SMPU_STRUCT0_ADDR1

SMPU region address 1 (master structure)

Address: 0x40232020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203296
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

7.1.11 PROT_SMPU_SMPU_STRUCT0_ATT1

SMPU region attributes 1 (master structure)

Address: 0x40232024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	R	RW	R	R	RW	R
HW Access	None	R	R	R	R	R	R	R
Name	None	NS	PX	PW	PR	UX	UW	UR

Bits	15	14	13	12	11	10	9	8
SW Access	RW							R
HW Access	R							R
Name	PC_MASK_15_TO_1 [15:9]							PC_MASK_0

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None	R				
HW Access	R	R	None	R				
Name	ENABLED	PC_MATCH	None	REGION_SIZE [28:24]				

Bits	Name	Description
31	ENABLED	Region enable: '0': Disabled. A disabled region will never result in a match on the bus transfer address. '1': Enabled. Default Value: 0
30	PC_MATCH	This field specifies if the PC field participates in the "matching" process or the "access evaluation" process: '0': PC field participates in "access evaluation". '1': PC field participates in "matching". "Matching" process. For each protection structure, the process identifies if a transfer address is contained within the address range. This identifies the "matching" regions. "Access evaluation" process. For each protection structure, the process evaluates the bus transfer access attributes against the access control attributes. Note that it is possible to define different access control for multiple protection contexts by using multiple protection structures with the same address region and PC_MATCH set to '1'. Default Value: Undefined

7.1.11 PROT_SMPU_SMPU_STRUCT0_ATT1 (continued)

28 : 24	REGION_SIZE	This field specifies the region size: "7": 256 B region (8 32 B subregions) Note: this field is read-only. Default Value: 0x07
15 : 9	PC_MASK_15_TO_1	This field specifies protection context identifier based access control. Bit i: protection context i+1 enable. If '0', protection context i+1 access is disabled; i.e. not allowed. If '1', protection context i+1 access is enabled; i.e. allowed. Default Value: Undefined
8	PC_MASK_0	This field specifies protection context identifier based access control for protection context "0". Default Value: 1
6	NS	Non-secure: '0': Secure (secure accesses allowed, non-secure access NOT allowed). '1': Non-secure (both secure and non-secure accesses allowed). Default Value: Undefined
5	PX	Privileged execute enable: '0': Disabled (privileged, execute accesses are NOT allowed). '1': Enabled (privileged, execute accesses are allowed). Note that this register is constant '0'; i.e. privileged execute accesses are NEVER allowed. Default Value: 0
4	PW	Privileged write enable: '0': Disabled (privileged, write accesses are NOT allowed). '1': Enabled (privileged, write accesses are allowed). Default Value: Undefined
3	PR	Privileged read enable: '0': Disabled (privileged, read accesses are NOT allowed). '1': Enabled (privileged, read accesses are allowed). Note that this register is constant '1'; i.e. privileged read accesses are ALWAYS allowed. Default Value: 1
2	UX	User execute enable: '0': Disabled (user, execute accesses are NOT allowed). '1': Enabled (user, execute accesses are allowed). Note that this register is constant '0'; i.e. user execute accesses are NEVER allowed. Default Value: 0
1	UW	User write enable: '0': Disabled (user, write accesses are NOT allowed). '1': Enabled (user, write accesses are allowed). Default Value: Undefined
0	UR	User read enable: '0': Disabled (user, read accesses are NOT allowed). '1': Enabled (user, read accesses are allowed). Note that this register is constant '1'; i.e. user read accesses are ALWAYS allowed. Default Value: 1

7.1.12 PROT_SMPU_SMPU_STRUCT1_ADDR1

SMPU region address 1 (master structure)

Address: 0x40232060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203296
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

7.1.13 PROT_SMPU_SMPU_STRUCT2_ADDR1

SMPU region address 1 (master structure)

Address: 0x402320A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203296
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

7.1.14 PROT_SMPU_SMPU_STRUCT3_ADDR1

SMPU region address 1 (master structure)

Address: 0x402320E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203296
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 63

7.1.15 PROT_SMPU_SMPU_STRUCT4_ADDR1

SMPU region address 1 (master structure)

Address: 0x40232120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203297
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

7.1.16 PROT_SMPU_SMPU_STRUCT5_ADDR1

SMPU region address 1 (master structure)

Address: 0x40232160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203297
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

7.1.17 PROT_SMPU_SMPU_STRUCT6_ADDR1

SMPU region address 1 (master structure)

Address: 0x402321A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203297
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

7.1.18 PROT_SMPU_SMPU_STRUCT7_ADDR1

SMPU region address 1 (master structure)

Address: 0x402321E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203297
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 63

7.1.19 PROT_SMPU_SMPU_STRUCT8_ADDR1

SMPU region address 1 (master structure)

Address: 0x40232220

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203298
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

7.1.20 PROT_SMPU_SMPU_STRUCT9_ADDR1

SMPU region address 1 (master structure)

Address: 0x40232260

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203298
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

7.1.21 PROT_SMPU_SMPU_STRUCT10_ADDR1

SMPU region address 1 (master structure)

Address: 0x402322A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203298
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

7.1.22 PROT_SMPU_SMPU_STRUCT11_ADDR1

SMPU region address 1 (master structure)

Address: 0x402322E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203298
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 63

7.1.23 PROT_SMPU_SMPU_STRUCT12_ADDR1

SMPU region address 1 (master structure)

Address: 0x40232320

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203299
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

7.1.24 PROT_SMPU_SMPU_STRUCT13_ADDR1

SMPU region address 1 (master structure)

Address: 0x40232360

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203299
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

7.1.25 PROT_SMPU_SMPU_STRUCT14_ADDR1

SMPU region address 1 (master structure)

Address: 0x402323A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203299
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

7.1.26 PROT_SMPU_SMPU_STRUCT15_ADDR1

SMPU region address 1 (master structure)

Address: 0x402323E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203299
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 63

7.1.27 PROT_MPU0_MS_CTL

Master control

Address: 0x40234000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				RW			
Name	None [7:4]				PC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				RW			
Name	None [23:20]				PC_SAVED [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	PC_SAVED	Saved protection context. Modifications to this field are constrained by the associated SMPU MS_CTL.PC_MASK_0 and MS_CTL.PC_MASK_15_TO_1[] fields. Note: this field is ONLY used by the CM0+. Default Value: 0

7.1.27 PROT_MPU0_MS_CTL (continued)

3 : 0	PC	Active protection context (PC). Modifications to this field are constrained by the associated SMPU MS_CTL.PC_MASK_0 and MS_CTL.PC_MASK_15_TO_1[] fields. In addition, a write transfer with protection context "0" can change this field (protection context 0 has unrestricted access).
		The CM0+ MPU MS_CTL register is special: the PC field is modifiable by BOTH HW and SW (for all other masters, the MPU MS_CTL.PC field is modifiable by SW ONLY. For CM0+ PC field HW modifications, the following holds:
		* On entry of a CM0_PC0/1/2/3_HANDLER exception/interrupt handler:
		IF (the new PC is the same as MS_CTL.PC)
		PC is not affected; PC_SAVED is not affected.
		ELSE IF (CM0_PC_CTL.VALID[MS_CTL.PC])
		An AHB-Lite bus error is generated for the exception handler fetch;
		PC is not affected; PC_SAVED is not affected.
		ELSE
		PC = "new PC"; PC_SAVED = PC (push operation).
		* On entry of any other exception/interrupt handler:
		PC = PC_SAVED; PC_SAVED is not affected (pop operation).
		Note that the CM0_PC0/1/2/3_HANDLER and CM0_PC_CTL registers are part of repecitve CPUSS MMIO registers.
		Note: this field is NOT used by the DW controllers, DMA controller, AXI DMA controller, CRYPTO component and VIDEOSS.
		Default Value: 0

7.1.28 PROT_MPU0_MS_CTL_READ_MIR0

Master control read mirror

Address: 0x40234004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				PC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				PC_SAVED [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	PC_SAVED	Read-only mirror of MS_CTL.PC_SAVED Default Value: 0
3 : 0	PC	Read-only mirror of MS_CTL.PC Default Value: 0

7.1.29 PROT_MPU14_MS_CTL

Master control

Address: 0x40237800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				RW			
Name	None [7:4]				PC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description

7.1.29 PROT_MPU14_MS_CTL (continued)

3 : 0	PC	Active protection context (PC). Modifications to this field are constrained by the associated SMPU MS_CTL.PC_MASK_0 and MS_CTL.PC_MASK_15_TO_1[] fields. In addition, a write transfer with protection context "0" can change this field (protection context 0 has unrestricted access).
		The CM0+ MPU MS_CTL register is special: the PC field is modifiable by BOTH HW and SW (for all other masters, the MPU MS_CTL.PC field is modifiable by SW ONLY. For CM0+ PC field HW modifications, the following holds:
		* On entry of a CM0_PC0/1/2/3_HANDLER exception/interrupt handler:
		IF (the new PC is the same as MS_CTL.PC)
		PC is not affected; PC_SAVED is not affected.
		ELSE IF (CM0_PC_CTL.VALID[MS_CTL.PC])
		An AHB-Lite bus error is generated for the exception handler fetch;
		PC is not affected; PC_SAVED is not affected.
		ELSE
		PC = "new PC"; PC_SAVED = PC (push operation).
		* On entry of any other exception/interrupt handler:
		PC = PC_SAVED; PC_SAVED is not affected (pop operation).
		Note that the CM0_PC0/1/2/3_HANDLER and CM0_PC_CTL registers are part of repecitve CPUSS MMIO registers.
		Note: this field is NOT used by the DW controllers, DMA controller, AXI DMA controller, CRYPTO component and VIDEOSS.
		Default Value: 0

7.1.30 PROT_MPU14_MS_CTL_READ_MIR0

Master control read mirror

Address: 0x40237804

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				PC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	PC	Read-only mirror of MS_CTL.PC Default Value: 0

7.1.31 PROT_MPU15_MPU_STRUCT0_ADDR

MPU region address

Address: 0x40237E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. The region size is defined by ATT.REGION_SIZE. A region of n Byte is always n Byte aligned. As a result, some of the lesser significant address bits of ADDR24 may be ignored in determining whether a bus transfer address is within an address region. E.g., a 64 KByte address region (REGION_-SIZE is "15") is 64 KByte aligned, and ADDR24[7:0] are ignored. Default Value: Undefined

7.1.31 PROT_MPU15_MPU_STRUCT0_ADDR (continued)

7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. E.g., a 64 KByte address region (REGION_SIZE is "15") has eight 8 KByte subregions. The access control as defined by MPU_REGION_ATT applies if the bus transfer address is within the address region AND the addressed subregion is NOT disabled. Note that the smallest region size is 256 B and the smallest subregion size is 32 B. Default Value: Undefined

7.1.32 PROT_MPU15_MPU_STRUCT0_ATT

MPU region attrributes

Address: 0x40237E04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	RW	RW	RW	RW
HW Access	None	R	R	R	R	R	R	R
Name	None	NS	PX	PW	PR	UX	UW	UR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None		RW				
HW Access	R	None		R				
Name	ENABLED	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	ENABLED	Region enable: '0': Disabled. A disabled region will never result in a match on the bus transfer address. '1': Enabled. Note: a disabled address region performs logic gating to reduce dynamic power consumption. Default Value: 0

7.1.32 PROT_MPU15_MPU_STRUCT0_ATT (continued)

28 : 24	REGION_SIZE	This field specifies the region size: "0"-"6": Undefined. "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "39": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: Undefined
6	NS	Non-secure: '0': Secure (secure accesses allowed, non-secure access NOT allowed). '1': Non-secure (both secure and non-secure accesses allowed). Default Value: Undefined
5	PX	Privileged execute enable: '0': Disabled (privileged, execute accesses are NOT allowed). '1': Enabled (privileged, execute accesses are allowed). Default Value: Undefined
4	PW	Privileged write enable: '0': Disabled (privileged, write accesses are NOT allowed). '1': Enabled (privileged, write accesses are allowed). Default Value: Undefined
3	PR	Privileged read enable: '0': Disabled (privileged, read accesses are NOT allowed). '1': Enabled (privileged, read accesses are allowed). Default Value: Undefined
2	UX	User execute enable: '0': Disabled (user, execute accesses are NOT allowed). '1': Enabled (user, execute accesses are allowed). Default Value: Undefined
1	UW	User write enable: '0': Disabled (user, write accesses are NOT allowed). '1': Enabled (user, write accesses are allowed). Default Value: Undefined

7.1.32 PROT_MPU15_MPU_STRUCT0_ATT (continued)

0	UR	User read enable: '0': Disabled (user, read accesses are NOT allowed). '1': Enabled (user, read accesses are allowed). Default Value: Undefined

8 Flash Controller Registers

This section discusses the Flash Controller registers. It lists all the registers in mapping tables, in address order.

8.1 Register Details

Register	Address	Description
FLASHC_FLASH_CTL	0x40240000	Control
FLASHC_FLASH_PWR_CTL	0x40240004	Flash power control
FLASHC_FLASH_CMD	0x40240008	Command
FLASHC_CM0_CA_CTL0	0x40240400	CM0+ cache control
FLASHC_CM0_CA_CTL1	0x40240404	CM0+ cache control
FLASHC_CM0_CA_CTL2	0x40240408	CM0+ cache control
FLASHC_CM0_CA_STATUS0	0x40240440	CM0+ cache status 0
FLASHC_CM0_CA_STATUS1	0x40240444	CM0+ cache status 1
FLASHC_CM0_CA_STATUS2	0x40240448	CM0+ cache status 2
FLASHC_CM0_STATUS	0x40240460	CM0+ interface status
FLASHC_CM4_CA_CTL0	0x40240480	CM4 cache control
FLASHC_CM4_CA_CTL1	0x40240484	CM4 cache control
FLASHC_CM4_CA_CTL2	0x40240488	CM4 cache control
FLASHC_CM4_CA_STATUS0	0x402404C0	CM4 cache status 0
FLASHC_CM4_CA_STATUS1	0x402404C4	CM4 cache status 1
FLASHC_CM4_CA_STATUS2	0x402404C8	CM4 cache status 2
FLASHC_CM4_STATUS	0x402404E0	CM4 interface status
FLASHC_CRYPTO_BUFF_CTL	0x40240500	Cryptography buffer control
FLASHC_DW0_BUFF_CTL	0x40240580	Datawire 0 buffer control
FLASHC_DW1_BUFF_CTL	0x40240600	Datawire 1 buffer control
FLASHC_DMAC_BUFF_CTL	0x40240680	DMA controller buffer control
FLASHC_FM_CTL_FM_CTL	0x4024F000	Flash macro control
FLASHC_FM_CTL_STATUS	0x4024F004	Status
FLASHC_FM_CTL_FM_ADDR	0x4024F008	Flash macro address
FLASHC_FM_CTL_BOOKMARK	0x4024F00C	Bookmark register - keeps the current FW HV seq
FLASHC_FM_CTL_GEOMETRY	0x4024F010	Regular flash geometry
FLASHC_FM_CTL_GEOMETRY_SUPERVISORY	0x4024F014	Supervisory flash geometry

Register	Address	Description
FLASHC_FM_CTL_ANA_CTL0	0x4024F018	Analog control 0
FLASHC_FM_CTL_ANA_CTL1	0x4024F01C	Analog control 1
FLASHC_FM_CTL_WAIT_CTL	0x4024F028	Wait State control
FLASHC_FM_CTL_TIMER_CLK_CTL	0x4024F034	Timer prescaler (clk_t to timer clock frequency divider)
FLASHC_FM_CTL_TIMER_CTL	0x4024F038	Timer control
FLASHC_FM_CTL_ACLK_CTL	0x4024F03C	MPCON clock
FLASHC_FM_CTL_INTR	0x4024F040	Interrupt
FLASHC_FM_CTL_INTR_SET	0x4024F044	Interrupt set
FLASHC_FM_CTL_INTR_MASK	0x4024F048	Interrupt mask
FLASHC_FM_CTL_INTR_MASKED	0x4024F04C	Interrupt masked
FLASHC_FM_CTL_CAL_CTL0	0x4024F050	Cal control BG LO trim bits
FLASHC_FM_CTL_CAL_CTL1	0x4024F054	Cal control BG HI trim bits
FLASHC_FM_CTL_CAL_CTL2	0x4024F058	Cal control BG LO&HI trim bits
FLASHC_FM_CTL_CAL_CTL3	0x4024F05C	Cal control osc trim bits, idac, sdac, itim
FLASHC_FM_CTL_CAL_CTL4	0x4024F060	Cal Control Vlim, SA, fdiv, reg_act
FLASHC_FM_CTL_CAL_CTL5	0x4024F064	Cal control
FLASHC_FM_CTL_CAL_CTL6	0x4024F068	SA trim LP/ULP
FLASHC_FM_CTL_CAL_CTL7	0x4024F06C	Cal control
FLASHC_FM_CTL_RED_CTL01	0x4024F080	Redundancy Control normal sectors 0,1
FLASHC_FM_CTL_RED_CTL23	0x4024F084	Redundancy Control normal sectors 2,3
FLASHC_FM_CTL_RED_CTL45	0x4024F088	Redundancy Control normal sectors 4,5
FLASHC_FM_CTL_RED_CTL67	0x4024F08C	Redundancy Control normal sectors 6,7
FLASHC_FM_CTL_RED_CTL_SM01	0x4024F090	Redundancy Control special sectors 0,1
FLASHC_FM_CTL_RGRANT_DELAY_PRG	0x4024F098	R-grant delay for program
FLASHC_FM_CTL_PW_SEQ12	0x4024F0A0	HV Pulse Delay for seq 1&2 pre
FLASHC_FM_CTL_PW_SEQ23	0x4024F0A4	HV Pulse Delay for seq2 post & seq3
FLASHC_FM_CTL_RGRANT_SCALE_ERS	0x4024F0A8	R-grant delay scale for erase
FLASHC_FM_CTL_RGRANT_DELAY_ERS	0x4024F0AC	R-grant delay for erase
FLASHC_FM_CTL_FM_PL_WRDATA_ALL	0x4024F7FC	Flash macro write page latches all
FLASHC_FM_CTL_FM_PL_DATA0	0x4024F800	Flash macro Page Latches data. This is the starting address of a register bank containing 128 registers (FLASHC_FM_CTL_FM_PL_DATA0 to FLASHC_FM_CTL_FM_PL_DATA127).
FLASHC_FM_CTL_FM_MEM_DATA0	0x4024FC00	Flash macro memory sense amplifier and column decoder data. This is the starting address of a register bank containing 128 registers (FLASHC_FM_CTL_FM_MEM_DATA0 to FLASHC_FM_CTL_FM_MEM_DATA127).

8.1.1 FLASHC_FLASH_CTL

Control

Address: 0x40240000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				MAIN_WS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	None		RW	RW
HW Access	None		R	R	None		R	R
Name	None [15:14]		WORK_BANK_MODE	MAIN_BANK_MODE	None [11:10]		WORK_-MAP	MAIN_MAP

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW	None			RW	None	
HW Access	None	R	None			R	None	
Name	None	WORK_ER-R_SILENT	None [21:19]			MAIN_ER-R_SILENT	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description

8.1.1 FLASHC_FLASH_CTL (continued)

22	WORK_ERR_SILENT	Specifies bus transfer behavior for a non-recoverable error on the FLASH macro work interface (either a non-correctable ECC error, a FLASH macro work interface internal error, a FLASH macro work interface memory hole access): 0: Bus transfer has a bus error. 1: Bus transfer does NOT have a bus error; i.e. the error is "silent" In either case, the erroneous FLASH macro data is returned by the bus master interface. The erroneous data is NOT placed in a bus master interface's cache and/or buffer. This field is ONLY used by CPU (and debug i.e. SYS_AP/CM0_AP/CM4_AP) bus transfers. Non-CPU bus transfers always have a bus transfer with a bus error, in case of a non-recoverable error. Note: All CPU bus masters have dedicated status registers (CM0_STATUS and CM4_STATUS) to register the occurrence of FLASH macro work interface internal errors (non-correctable ECC errors and memory hole errors are NOT registered). Note: fault reporting can be used to identify the error that occurred: - FLASH macro work interface internal error. - FLASH macro work interface non-recoverable ECC error. - FLASH macro work interface recoverable ECC error. - FLASH macro work interface memory hole error. Default Value: 0
18	MAIN_ERR_SILENT	Specifies bus transfer behavior for a non-recoverable error on the FLASH macro main interface (either a non-correctable ECC error, a FLASH macro main interface internal error, a FLASH macro main interface memory hole access): 0: Bus transfer has a bus error. 1: Bus transfer does NOT have a bus error; i.e. the error is "silent" In either case, the erroneous FLASH macro data is returned by the bus master interface. The erroneous data is NOT placed in a bus master interface's cache and/or buffer. This field is ONLY used by CPU (and debug i.e. SYS_AP/CM0_AP/CM4_AP) bus transfers. Non-CPU bus transfers always have a bus transfer with a bus error, in case of a non-recoverable error. Note: All CPU bus masters have dedicated status registers (CM0_STATUS and CM4_STATUS) to register the occurrence of FLASH macro main interface internal errors (non-correctable ECC errors and memory hole errors are NOT registered). Note: fault reporting can be used to identify the error that occurred: - FLASH macro main interface internal error. - FLASH macro main interface non-recoverable ECC error. - FLASH macro main interface recoverable ECC error. - FLASH macro main interface memory hole error. Default Value: 0
13	WORK_BANK_MODE	Specifies bank mode of FLASH macro work array. 0: Single bank mode. 1: Dual bank mode. Default Value: 0
12	MAIN_BANK_MODE	Specifies bank mode of FLASH macro main array. 0: Single bank mode. 1: Dual bank mode. Default Value: 0
9	WORK_MAP	Specifies mapping of FLASH macro work array. 0: Mapping A. 1: Mapping B. This field is only used when WORK_BANK_MODE is "1" (dual bank mode). Default Value: 0

8.1.1 FLASHC_FLASH_CTL (continued)

8	MAIN_MAP	Specifies mapping of FLASH macro main array. 0: Mapping A. 1: Mapping B. This field is only used when MAIN_BANK_MODE is "1" (dual bank mode). Default Value: 0
3 : 0	MAIN_WS	FLASH macro main interface wait states: "0": 0 wait states. ... "15": 15 wait states Default Value: 0

8.1.2 FLASHC_FLASH_PWR_CTL

Flash power control

Address: 0x40240004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						EN-ABLE_HV	ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	ENABLE_HV	Enables HV power to the flash memory Default Value: 1
0	ENABLE	Enables power to the flash memory Default Value: 1

8.1.3 FLASHC_FLASH_CMD

Command

Address: 0x40240008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						RW1C	RW1C
Name	None [7:2]						BUFF_INV	INV

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	BUFF_INV	Invalidation of ALL buffers (does not invalidate the caches). SW writes a "1" to clear the buffers. HW sets this field to "0" when the operation is completed. The operation takes a maximum of three clock cycles on the slowest of the clk_slow and clk_fast clocks. Note: the caches only capture FLASH macro main array data. Therefore, invalidating just the buffers (BUFF_INV) does not invalidate captures main array data in the caches. Default Value: 0
0	INV	Invalidation of ALL caches (for CM0+ and CM4) and ALL buffers. SW writes a "1" to clear the caches. HW sets this field to "0" when the operation is completed. The operation takes a maximum of three clock cycles on the slowest of the clk_slow and clk_fast clocks. The caches' LRU structures are also reset to their default state. Default Value: 0

8.1.4 FLASHC_CM0_CA_CTL0

CM0+ cache control

Address: 0x40240400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						WAY [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None			RW		
HW Access	R	R	None			R		
Name	CA_EN	PREF_EN	None [29:27]			SET_ADDR [26:24]		

Bits	Name	Description
31	CA_EN	Cache enable: 0: Disabled. The cache tag valid bits are reset to "0"s and the cache LRU information is set to "1"s (making way 0 the LRU way and way 3 the MRU way). 1: Enabled. Default Value: 1
30	PREF_EN	Prefetch enable: 0: Disabled. 1: Enabled. Prefetching requires the cache to be enabled; i.e. ENABLED is "1". Default Value: 1
26 : 24	SET_ADDR	Specifies the cache set for which cache information is provided in CM0_CA_STATUS0/1/2. Default Value: 0
17 : 16	WAY	Specifies the cache way for which cache information is provided in CM0_CA_STATUS0/1/2. Default Value: 0

8.1.5 FLASHC_CM0_CA_CTL1 (continued)

8.1.5 FLASHC_CM0_CA_CTL1

CM0+ cache control

Address: 0x40240404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VECTKEYSTAT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VECTKEYSTAT [31:24]							

Bits	Name	Description
31 : 16	VECTKEYSTAT	Register key (to prevent accidental writes). - Should be written with a 0x05fa key value for the write to take effect. - Always reads as 0xfa05. Note: Although the SW attribute for this field says "R', SW need to write the key 0x05fa in this field for this register write to happen. This is a built in protection provided to prevent accidental writes from SW. Default Value: 0xFA05
1 : 0	PWR_MODE	Specifies power mode for CM0 cache. The following sequnece should be followed for turning OFF/ON the cache SRAM. Turn OFF sequence: a) Write CM0_CA_CTL0 to disable cache. b) Write CM0_CA_CTL1 to turn OFF cache SRAM. Turn ON sequence: a) Write CM0_CA_CTL1 to turn ON cache SRAM. b) Delay to allow power up of cache SRAM. Delay should be at a minimum of CM0_-CA_CTL2.PWRUP_DELAY CLK_SLOW clock cycles. c) Write CM0_CA_CTL0 to enable cache. Default Value: 3

8.1.5 FLASHC_CM0_CA_CTL1 (continued)

0x0: OFF :

Power OFF the CM0 cache, no retain

0x1: RESERVED :

Undefined

0x2: RETAINED :

Put the CM0 cache in retained mode

0x3: ENABLED :

Enable/Turn ON the CM0 cache SRAM.

8.1.6 FLASHC_CM0_CA_CTL2

CM0+ cache control

Address: 0x40240408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PWRUP_DELAY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						PWRUP_DELAY [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	PWRUP_DELAY	Number clock cycles delay needed after power domain power up Default Value: 0x12C

8.1.7 FLASHC_CM0_CA_STATUS0

CM0+ cache status 0

Address: 0x40240440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VALID32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	VALID32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	VALID32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	VALID32 [31:24]							

Bits	Name	Description
31 : 0	VALID32	Sixteen valid bits of the cache line specified by CM0_CA_CTL.WAY and CM0_-CA_CTL.SET_ADDR. Default Value: 0

8.1.8 FLASHC_CM0_CA_STATUS1

CM0+ cache status 1

Address: 0x40240444

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	TAG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	TAG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	TAG [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	TAG [31:24]							

Bits	Name	Description
31 : 0	TAG	Cache line address of the cache line specified by CM0_CA_CTL.WAY and CM0_-CA_CTL.SET_ADDR. Default Value: Undefined

8.1.9 FLASHC_CM0_CA_STATUS2

CM0+ cache status 2

Address: 0x40240448

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R					
HW Access	None		W					
Name	None [7:6]		LRU [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	LRU	Six bit LRU representation of the cache set specified by CM0_CA_CTL.SET_ADDR. The encoding of the field is as follows ("X_LRU_Y" indicates that way X is Less Recently Used than way Y): Bit 5: 0_LRU_1: way 0 less recently used than way 1. Bit 4: 0_LRU_2. Bit 3: 0_LRU_3. Bit 2: 1_LRU_2. Bit 1: 1_LRU_3. Bit 0: 2_LRU_3. Default Value: Undefined

8.1.10 FLASHC_CM0_STATUS

CM0+ interface status

Address: 0x40240460

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						W1S	W1S
Name	None [7:2]						WORK_INTERNAL_ERR	MAIN_INTERNAL_ERR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	WORK_INTERNAL_ERR	See CM0_STATUS.MAIN_INTERNAL_ERROR. Default Value: 0
0	MAIN_INTERNAL_ERR	Specifies/registers the occurrence of a FLASH macro main interface internal error (typically the result of a read access while a program erase operation is ongoing) as a result of a CM0+ access (or debug access via SYS_AP/CM0_AP). SW clears this field to "0". HW sets this field to "1" on a FLASH macro main interface internal error. Typically, SW reads this field after a code section to detect the occurrence of an error. Note: this field is independent of FLASH_CTL.MAIN_ERR_SILENT. Default Value: 0

8.1.11 FLASHC_CM4_CA_CTL0

CM4 cache control

Address: 0x40240480

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						WAY [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None			RW		
HW Access	R	R	None			R		
Name	CA_EN	PREF_EN	None [29:27]			SET_ADDR [26:24]		

Bits	Name	Description
31	CA_EN	Cache enable: 0: Disabled. The cache tag valid bits are reset to "0"s and the cache LRU information is set to "1"s (making way 0 the LRU way and way 3 the MRU way). 1: Enabled. Default Value: 1
30	PREF_EN	Prefetch enable: 0: Disabled. 1: Enabled. Prefetching requires the cache to be enabled; i.e. ENABLED is "1". Default Value: 1
26 : 24	SET_ADDR	Specifies the cache set for which cache information is provided in CM4_CA_STATUS0/1/2. Default Value: 0
17 : 16	WAY	Specifies the cache way for which cache information is provided in CM4_CA_STATUS0/1/2. Default Value: 0

8.1.12 FLASHC_CM4_CA_CTL1 (continued)

8.1.12 FLASHC_CM4_CA_CTL1

CM4 cache control

Address: 0x40240484

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VECTKEYSTAT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VECTKEYSTAT [31:24]							

Bits	Name	Description
31 : 16	VECTKEYSTAT	Register key (to prevent accidental writes). - Should be written with a 0x05fa key value for the write to take effect. - Always reads as 0xfa05. Note: Although the SW attribute for this field says "R', SW need to write the key 0x05fa in this field for this register write to happen. This is a built in protection provided to prevent accidental writes from SW. Default Value: 0xFA05
1 : 0	PWR_MODE	Specifies power mode for CM4 cache. The following sequnece should be followed for truning OFF/ON the cache SRAM. Turn OFF sequence: a) Write CM4_CA_CTL0 to disable cache. b) Write CM4_CA_CTL1 to turn OFF cache SRAM. Turn ON sequence: a) Write CM4_CA_CTL1 to turn ON cache SRAM. b) Delay to allow power up of cache SRAM. Delay should be at a minimum of CM4_-CA_CTL2.PWRUP_DELAY CLK_SLOW clock cycles. c) Write CM4_CA_CTL0 to enable cache. Default Value: 3

8.1.12 FLASHC_CM4_CA_CTL1 (continued)

0x0: OFF :

Power OFF the CM4 cache, not retained.

0x1: RESERVED :

Undefined

0x2: RETAINED :

Put the CM4 cache in retained mode.

0x3: ENABLED :

Enable/Turn ON the CM4 cache.

8.1.13 FLASHC_CM4_CA_CTL2

CM4 cache control

Address: 0x40240488

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PWRUP_DELAY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						PWRUP_DELAY [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	PWRUP_DELAY	Number clock cycles delay needed after power domain power up Default Value: 0x12C

8.1.14 FLASHC_CM4_CA_STATUS0

CM4 cache status 0

Address: 0x402404C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VALID32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	VALID32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	VALID32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	VALID32 [31:24]							

Bits	Name	Description
31 : 0	VALID32	See CM0_CA_STATUS0. Default Value: 0

8.1.15 FLASHC_CM4_CA_STATUS1

CM4 cache status 1

Address: 0x402404C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	TAG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	TAG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	TAG [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	TAG [31:24]							

Bits	Name	Description
31 : 0	TAG	See CM0_CA_STATUS1. Default Value: Undefined

8.1.16 FLASHC_CM4_CA_STATUS2

CM4 cache status 2

Address: 0x402404C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R					
HW Access	None		W					
Name	None [7:6]		LRU [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	LRU	See CM0_CA_STATUS2. Default Value: Undefined

8.1.17 FLASHC_CM4_STATUS

CM4 interface status

Address: 0x402404E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						W1S	W1S
Name	None [7:2]						WORK_INTERNAL_ERR	MAIN_INTERNAL_ERR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	WORK_INTERNAL_ERR	See CM4_STATUS.MAIN_INTERNAL_ERROR. Default Value: 0
0	MAIN_INTERNAL_ERR	Specifies/registers the occurrence of a FLASH macro main interface internal error (typically the result of a read access while a program erase operation is ongoing) as a result of a CM4 access (or debug access via SYS_AP/CM4_AP). SW clears this field to "0". HW sets this field to "1" on a FLASH macro main interface internal error. Typically, SW reads this field after a code section to detect the occurrence of an error. Note: this field is independent of FLASH_CTL.MAIN_ERR_SILENT. Default Value: 0

8.1.18 FLASHC_CRYPTO_BUFF_CTL

Cryptography buffer control

Address: 0x40240500

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW	None					
HW Access	None	R	None					
Name	None	PREF_EN	None [29:24]					

Bits	Name	Description
30	PREF_EN	Prefetch enable: 0: Disabled. 1: Enabled. A prefetch will be done when there is read "hit" on the last 32-bit word of the buffer. For eCT work Flash, prefetch will not be done. Default Value: 1

8.1.19 FLASHC_DW0_BUFF_CTL

Datawire 0 buffer control

Address: 0x40240580

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW	None					
HW Access	None	R	None					
Name	None	PREF_EN	None [29:24]					

Bits	Name	Description
30	PREF_EN	See CRYPTO_BUFF_CTL. Default Value: 1

8.1.20 FLASHC_DW1_BUFF_CTL

Datawire 1 buffer control

Address: 0x40240600

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW	None					
HW Access	None	R	None					
Name	None	PREF_EN	None [29:24]					

Bits	Name	Description
30	PREF_EN	See CRYPTO_BUFF_CTL. Default Value: 1

8.1.21 FLASHC_DMAC_BUFF_CTL

DMA controller buffer control

Address: 0x40240680

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW	None					
HW Access	None	R	None					
Name	None	PREF_EN	None [29:24]					

Bits	Name	Description
30	PREF_EN	See CRYPTO_BUFF_CTL. Default Value: 1

8.1.22 FLASHC_FM_CTL_FM_CTL (continued)

8.1.22 FLASHC_FM_CTL_FM_CTL

Flash macro control

Address: 0x4024F000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				FM_MODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						FM_SEQ [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	DAA_MUX_SEL [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						WR_EN	IF_SEL

Bits	Name	Description
25	WR_EN	0: normal mode 1: Fm Write Enable Set to enable flash writes. Note: IF_SEL and WR_EN cannot be changed at the same time Default Value: 0
24	IF_SEL	Interface selection. Specifies the interface that is used for flash memory read operations: 0: R interface is used (default value). In this case, the flash memory address is provided as part of the R signal interface. 1: C interface is used. In this case, the flash memory address is provided by FM_MEM_ADDR (the page address) and by the C interface access offset in the FM_MEM_DATA structure. Note: IF_SEL and WR_EN cannot be changed at the same time Default Value: 0
22 : 16	DAA_MUX_SEL	Direct memory cell access address. Default Value: 0
9 : 8	FM_SEQ	Requires (IF_SEL|WR_EN)=1 Flash macro sequence selection Default Value: 0

3 : 0	FM_MODE	Requires (IF_SEL|WR_EN)=1 Flash macro mode selection Default Value: 0

8.1.23 FLASHC_FM_CTL_STATUS (continued)

8.1.23 FLASHC_FM_CTL_STATUS

Status

Address: 0x4024F004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	R_GRANT_DE-LAY_STA-TUS	TIM-ER_STA-TUS	IF-_SEL_MON	WR_EN_MON	TURBO_N	ILLE-GAL_HVOP	HV_REGS_ISOLATED	TIMER_EN-ABLED

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	RE-SET_MM	SEC-TOR0_SR	MAX_D-OUT-_WIDTH	RWW	NEG_PUMP_VHI	POS_PUMP_VLO	FM_READY	FM_BUSY

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	RQ_ER-ROR	CBUS_RED_ROW_EN	CBUS_RA_MATCH	HVO-P_BULK_ALL	HVOP_-SECTOR	HVOP_-SUB_SEC-TOR_N	ROW_EVEN	ROW_ODD

Bits	31	30	29	28	27	26	25	24
SW Access	R				R			
HW Access	W				W			
Name	PUMP_NDAC [31:28]				PUMP_PDAC [27:24]			

Bits	Name	Description
31 : 28	PUMP_NDAC	Test_only, internal node: regif ndac outputs to pos pump Default Value: 0
27 : 24	PUMP_PDAC	Test_only, internal node: regif pdac outputs to pos pump Default Value: 0
23	RQ_ERROR	Test_only, internal node: rq_error sync-de in clk_c domain Default Value: 0
22	CBUS_RED_ROW_EN	Test_only, internal node: mpcon red_row_en Default Value: 0

8.1.23 FLASHC_FM_CTL_STATUS (continued)

21	CBUS_RA_MATCH	Test_only, internal node: mpcon ra match Default Value: 0
20	HVOP_BULK_ALL	Test_only, internal node: mpcon bk_all Default Value: 0
19	HVOP_SECTOR	Test_only, internal node: mpcon bk_sec Default Value: 0
18	HVOP_SUB_SECTOR_N	Test_only, internal node: mpcon bk_subb Default Value: 0
17	ROW_EVEN	Test_only, internal node: mpcon row_even Default Value: 0
16	ROW_ODD	Test_only, internal node: mpcon row_odd Default Value: 0
15	RESET_MM	Test_only, internal node: mpcon reset_mm Default Value: 0
14	SECTOR0_SR	0: Sector 0 does not contain special rows. The special rows are located in separate special sectors. 1: Sector 0 contains special rows Default Value: 0
13	MAX_DOUT_WIDTH	Internal memory core max data out size (number of data out bits per column): 0: x128 bits 1: x256 bits Default Value: 0
12	RWW	FM Type (Read While Write or Not Read While Write): 0: Non RWW FM Type 1: RWW FM Type Default Value: 1
11	NEG_PUMP_VHI	NEG pump VHI Default Value: 1
10	POS_PUMP_VLO	POS pump VLO Default Value: 0
9	FM_READY	0: FM not ready 1: FM ready Default Value: 0
8	FM_BUSY	0': FM not busy 1: FM BUSY : R_GRANT is 0 as result of a busy request from FM ready, or from HV operations. Default Value: 0
7	R_GRANT_DELAY_STATUS	0: R_GRANT_DELAY timer is not running 1: R_GRANT_DELAY timer is running Default Value: 0
6	TIMER_STATUS	The actual timer state sync-ed in clk_c domain: 0: timer is not running: 1: timer is running; Default Value: 0
5	IF_SEL_MON	FM_CTL.IF_SEL bit after being synchronized in clk_r domain Default Value: 0
4	WR_EN_MON	FM_CTL.WR_EN bit after being synchronized in clk_r domain Default Value: 0

3	TURBO_N	After FM power up indicates the analog blocks currents are boosted to faster reach their functional state.. Used in the testchip boot only as an "FM READY" flag. 0: turbo mode 1: normal mode Default Value: 0
2	ILLEGAL_HVOP	Indicates a bulk, sector erase, program has been requested when axa=1 0: no error 1: illegal HV operation error Default Value: 0
1	HV_REGS_ISOLATED	Indicates the isolation status at HV trim and redundancy registers inputs 0: Not isolated, writing permitted 1: isolated writing disabled Default Value: 0
0	TIMER_ENABLED	This is the timer_en bit set by writing a "1" in the TIMER_CTL bit 31. It is reset by HW when the timer expires 0: timer not running 1: Timer is enabled and not expired yet Default Value: 0

8.1.24 FLASHC_FM_CTL_FM_ADDR

Flash macro address

Address: 0x4024F008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	BA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							AXA

Bits	Name	Description
24	AXA	Auxiliary address field: 0: regular flash memory. 1: supervisory flash memory. Default Value: 0
23 : 16	BA	Bank address. Default Value: 0
15 : 0	RA	Row address. Default Value: 0

8.1.25 FLASHC_FM_CTL_BOOKMARK

Bookmark register - keeps the current FW HV seq

Address: 0x4024F00C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BOOKMARK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	BOOKMARK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	BOOKMARK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	BOOKMARK [31:24]							

Bits	Name	Description
31 : 0	BOOKMARK	Used by FW. Keeps the Current HV cycle sequence Default Value: 0

8.1.26 FLASHC_FM_CTL_GEOMETRY (continued)

8.1.26 FLASHC_FM_CTL_GEOMETRY

Regular flash geometry

Address: 0x4024F010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ROW_COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ROW_COUNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BANK_COUNT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R				R			
HW Access	W				W			
Name	PAGE_SIZE_LOG2 [31:28]				WORD_SIZE_LOG2 [27:24]			

Bits	Name	Description
31 : 28	PAGE_SIZE_LOG2	Number of Bytes per page (log 2): 0: 1 Byte 1: 2 Bytes 2: 4 Bytes ... 15: 32768 Bytes The currently planned flash macros have a page size of either 256 Byte or 512 Byte, resulting in PAGE_SIZE_LOG2 settings of 8 and 9 respectively. Default Value: 0

27 : 24	WORD_SIZE_LOG2	Number of Bytes per word (log 2). A word is defined as the data that is read from the flash macro over the R interface with a single read access: 0: 1 Byte 1: 2 Bytes 2: 4 Bytes ... 3: 128 Bytes The currently planned flash macros have a word size of either 32-bit, 64-bit or 128-bit, resulting in WORD_SIZE_LOG2 settings of 2, 3 and 4 respectively. Default Value: 0
23 : 16	BANK_COUNT	Number of banks (minus 1): 0: 1 bank 1: 2 banks ... "255": 256 banks Default Value: 0
15 : 0	ROW_COUNT	Number of rows (minus 1): 0: 1 row 1: 2 rows 2: 3 rows ... "65535": 65536 rows Default Value: 0

8.1.27 FLASHC_FM_CTL_GEOMETRY_SUPERVISORY

Supervisory flash geometry

Address: 0x4024F014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ROW_COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ROW_COUNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BANK_COUNT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R				R			
HW Access	W				W			
Name	PAGE_SIZE_LOG2 [31:28]				WORD_SIZE_LOG2 [27:24]			

Bits	Name	Description
31 : 28	PAGE_SIZE_LOG2	Number of Bytes per page (log 2). See GEOMETRY.PAGE_SIZE_LOG2. Typically, PAGE_-SIZE_LOG2 equals GEOMETRY.PAGE_SIZE_LOG2. Default Value: 0
27 : 24	WORD_SIZE_LOG2	Number of Bytes per word (log 2). See GEOMETRY.WORD_SIZE_LOG2. Typically, WORD_-SIZE_LOG2 equals GEOMETRY.WORD_SIZE_LOG2. Default Value: 0
23 : 16	BANK_COUNT	Number of banks (minus 1). BANK_COUNT is less or equal to GEOMETRY.BANK_COUNT. Default Value: 0
15 : 0	ROW_COUNT	Number of rows (minus 1). ROW_COUNT is typically less than GEOMETRY.ROW_COUNT Default Value: 0

8.1.28 FLASHC_FM_CTL_ANA_CTL0 (continued)

8.1.28 FLASHC_FM_CTL_ANA_CTL0

Analog control 0

Address: 0x4024F018

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MDAC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW	RW		
HW Access	R				R	R		
Name	NDAC_MIN [15:12]				FLIP_AMU XBUS_AB	CSLDAC [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW		RW			
HW Access	R		R		R			
Name	SCALE_PRG_SEQ12 [23:22]		SCALE_PRG_SEQ01 [21:20]		PDAC_MIN [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	SCALE_PRG_PEOFF [31:30]		SCALE_PRG_PEON [29:28]		SCALE_SEQ30 [27:26]		SCALE_PRG_SEQ23 [25:24]	

Bits	Name	Description
31 : 30	SCALE_PRG_PEOFF	PROG_PROG: Scale for R_GRANT_DELAY on PE OFF transition: 00: 0.125uS 01: 1uS 10: 10uS 11: 100uS Default Value: 0
29 : 28	SCALE_PRG_PEON	PROG_PROG: Scale for R_GRANT_DELAY on PE On transition: 00: 0.125uS 01: 1uS 10: 10uS 11: 100uS Default Value: 0

27 : 26	SCALE_SEQ30	PROG_PROG& ERASE: Scale for R_GRANT_DELAY on seq3-seq0 transition: 00: 0.125uS 01: 1uS 10: 10uS 11: 100uS Default Value: 0
25 : 24	SCALE_PRG_SEQ23	PROG_PROG: Scale for R_GRANT_DELAY on seq2-seq3 transition: 00: 0.125uS 01: 1uS 10: 10uS 11: 100uS Default Value: 0
23 : 22	SCALE_PRG_SEQ12	PROG_PROG: Scale for R_GRANT_DELAY on seq1-seq2 transition: 00: 0.125uS 01: 1uS 10: 10uS 11: 100uS Default Value: 0
21 : 20	SCALE_PRG_SEQ01	PROG_PROG: Scale for R_GRANT_DELAY on seq0-seq1 transition: 00: 0.125uS 01: 1uS 10: 10uS 11: 100uS Default Value: 0
19 : 16	PDAC_MIN	PDAC staircase min value Default Value: 0x0
15 : 12	NDAC_MIN	NDAC staircase min value Default Value: 0x0
11	FLIP_AMUXBUS_AB	Flips amuxbusa and amuxbusb 0: amuxbusa, amuxbusb 1: amuxbusb, amuxbusb Default Value: 0
10 : 8	CSLDAC	Trimming of common source line DAC. Default Value: 0x4
7 : 0	MDAC	Trimming of the output margin Voltage as a function of Vpos and Vneg. Default Value: 0

8.1.29 FLASHC_FM_CTL_ANA_CTL1

Analog control 1

Address: 0x4024F01C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	NDAC_STEP [7:4]				NDAC_MAX [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	PDAC_STEP [15:12]				PDAC_MAX [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	NPDAC_STEP_TIME [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	NPDAC_ZERO_TIME [31:24]							

Bits	Name	Description
31 : 24	NPDAC_ZERO_TIME	Ndac/Pdac LO duration: (1uS .. 255uS) * 8 When 0, N/PDAC don't return to 0 Default Value: 0x0D
23 : 16	NPDAC_STEP_TIME	Ndac/Pdac step duration: (1uS .. 255uS) * 8 When = 0 N/PDAC_MAX control the pumps Default Value: 0x32
15 : 12	PDAC_STEP	Pdac step increment Default Value: 0xF
11 : 8	PDAC_MAX	Pdac Max Value.Trimming of positive pump output Voltage: Default Value: 0xA
7 : 4	NDAC_STEP	Ndac step increment Default Value: 0xF
3 : 0	NDAC_MAX	Ndac Max Value.Trimming of negative pump output Voltage. Default Value: 0xA

8.1.30 FLASHC_FM_CTL_WAIT_CTL (continued)

8.1.30 FLASHC_FM_CTL_WAIT_CTL

Wait State control

Address: 0x4024F028

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				WAIT_FM_MEM_RD [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				WAIT_FM_HV_RD [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					R		
Name	None [23:19]					WAIT_FM_HV_WR [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW	RW	RW	RW	RW	
HW Access	None		R	R	R	R	R	
Name	None [31:30]		PL_SOFT-_SET_EN	MBA	DRMM	LV_SPARE_1	FM_RWW_MODE [25:24]	

Bits	Name	Description
29	PL_SOFT_SET_EN	Page latch soft set enable, 0 = disabled, 1 = enabled (at end of seq_2), taken care in API Default Value: 0
28	MBA	0: Normal 1: Test mode to enable Master Bulk Access which allows both normal rows and redundant rows to be erased / programmed in one HV cycle (Bulk / Sector Erase and Sector Program). Default Value: 0
27	DRMM	0: Normal 1: Test mode to enable Margin mode for 2 rows at a time Default Value: 0
26	LV_SPARE_1	Spare register Default Value: 0
25 : 24	FM_RWW_MODE	00: Full CBUS MODE 01: RWW 10: RWW. R_GRANT is stalling r_bus for the whole program/erase duration Default Value: 0

18 : 16	WAIT_FM_HV_WR	Number of C interface wait cycles (on "clk_c") for a write to the high Voltage page latches. Default Value: 3
11 : 8	WAIT_FM_HV_RD	Number of C interface wait cycles (on "clk_c") for a read from the high Voltage page latches. Common for reading HV Page Latches and the DATA_COMP_RESULT bit Default Value: 11
3 : 0	WAIT_FM_MEM_RD	Number of C interface wait cycles (on "clk_c") for a read from the memory Default Value: 9

8.1.31 FLASHC_FM_CTL_TIMER_CLK_CTL (continued)

8.1.31 FLASHC_FM_CTL_TIMER_CLK_CTL

Timer prescaler (clk_t to timer clock frequency divider)

Address: 0x4024F034

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TIMER_CLOCK_FREQ [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RGRANT_DELAY_PRG_PEON [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RGRANT_DELAY_PRG_PEOFF [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	RGRANT_DELAY_PRG_SEQ01 [31:24]							

Bits	Name	Description
31 : 24	RGRANT_DE-LAY_PRG_SEQ01	PROG_PROG: R-grant blocking delay on seq0-seq1 transition. Scale = ANA_CTL0.SCALE_SEQ01 When = 0 R_GRANT_DELAY control is disabled when IF_SEL=1 R_GRANT_DELAY control is disabled Default Value: 0
23 : 16	RGRANT_DE-LAY_PRG_PEOFF	PROG_PROG: R-grant blocking delay on PE OFF. Scale = ANA_CTL0.SCALE_PEOFF When = 0 R_GRANT_DELAY control is disabled when IF_SEL=1 R_GRANT_DELAY control is disabled Default Value: 0
15 : 8	RGRANT_DE-LAY_PRG_PEON	PROG_PROG: R-grant blocking delay on PE ON. Scale = ANA_CTL0.SCALE_PEON When = 0 R_GRANT_DELAY control is disabled when IF_SEL=1 R_GRANT_DELAY control is disabled Default Value: 0

7 : 0	TIMER_CLOCK_FREQ	Clk_t frequency divider to provide the 1MHz reference clock for the Regif Timer. Equal to the frequency in MHz of the timer clock "clk_t". Example: if "clk_t" has a frequency of 4 MHz then this field value is "4" Max clk_t frequency = 100MHz. This field is updated at runtime with the "SW_TIMER_CLOCK_FREQ " value from the HV parameters table Default Value: 0x08

8.1.32 FLASHC_FM_CTL_TIMER_CTL (continued)

8.1.32 FLASHC_FM_CTL_TIMER_CTL

Timer control

Address: 0x4024F038

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW						
HW Access	R	R						
Name	SCALE	PERIOD [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	None		RW	RW	RW
HW Access	RW0C	RW0C	RW0C	None		R	R	RW
Name	TIMER_EN	ACLK_EN	PUMP_EN	None [28:27]		PRE_PROG_CSL	PRE_PROG	AUTO_SEQUENCE

Bits	Name	Description
31	TIMER_EN	Timer enable: 0: disabled 1: enabled. SW sets this field to "1" to start the timer. HW sets this field to "0" when the timer is expired. Default Value: 0
30	ACLK_EN	ACLK enable (generates a single cycle pulse for the FM): 0: disabled 1: enabled. SW set this field to "1" to generate a single cycle pulse. HW sets this field to "0" when the pulse is generated. Default Value: 0

29	PUMP_EN	Pump enable: 0: disabled 1: enabled (also requires FM_CTL.IF_SEL to be"1", this additional restriction is required to prevent non intentional clearing of the FM). SW sets this field to "1" to generate a single PE pulse. HW clears this field when timer is expired. Default Value: 0
26	PRE_PROG_CSL	0: CSL lines driven by CSL_DAC 1: CSL lines driven by VNEG_G Default Value: 1
25	PRE_PROG	1 during pre-program operation Default Value: 0
24	AUTO_SEQUENCE	1': Starts1 the HV automatic sequencing Cleared by HW Default Value: 0
15	SCALE	Timer tick scale: 0: 1 microsecond. 1: 100 microseconds. Default Value: 0
14 : 0	PERIOD	Timer period in either microseconds (SCALE is '0') or 100's of microseconds (SCALE is '1') multiples. Default Value: 1

8.1.33 FLASHC_FM_CTL_ACLK_CTL

MPCON clock

Address: 0x4024F03C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							W
HW Access	None							R
Name	None [7:1]							ACLK_GEN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	ACLK_GEN	A write to this register generates the clock pulse for HV control registers (mpcon outputs) Default Value: 0x0

8.1.34 FLASHC_FM_CTL_INTR

Interrupt

Address: 0x4024F040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [7:1]							TIMER_EXPIRED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER_EXPIRED	Set to '1', when event is detected. Write INTR field with '1', to clear bit. Write INTR_SET field with '1', to set bit. Default Value: 0

8.1.35 FLASHC_FM_CTL_INTR_SET

Interrupt set

Address: 0x4024F044

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							A
Name	None [7:1]							TIMER_EXPIRED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER_EXPIRED	Write INTR_SET field with "1" to set corresponding INTR field (a write of "0" has no effect). Default Value: 0

8.1.36 FLASHC_FM_CTL_INTR_MASK

Interrupt mask

Address: 0x4024F048

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TIMER_EXPIRED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER_EXPIRED	Mask for corresponding field in INTR register. Default Value: 0

8.1.37 FLASHC_FM_CTL_INTR_MASKED

Interrupt masked

Address: 0x4024F04C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							TIMER_EXPIRED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER_EXPIRED	Logical and of corresponding request and mask fields. Default Value: 0

8.1.38 FLASHC_FM_CTL_CAL_CTL0

Cal control BG LO trim bits

Address: 0x4024F050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				
HW Access	R			R				
Name	CDAC_LO_HV [7:5]			VCT_TRIM_LO_HV [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW				
HW Access	R			R				
Name	VBG_TC_TRIM_LO_HV [15:13]			VBG_TRIM_LO_HV [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW	RW		
HW Access	None				R	R		
Name	None [23:20]				IPREF_TRI-MA_LO_HV	ICREF_TC_TRIM_LO_HV [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19	IPREF_TRIMA_LO_HV	Adds 100-150nA boost on IPREF_LO Default Value: 0
18 : 16	ICREF_TC_TRIM_LO_HV	LO Bandgap Current Temperature Compensation trim control Default Value: 0x3
15 : 13	VBG_TC_TRIM_LO_HV	LO Bandgap Voltage Temperature Compensation trim control Default Value: 0x4
12 : 8	VBG_TRIM_LO_HV	LO Bandgap Voltage trim control. Default Value: 0xF
7 : 5	CDAC_LO_HV	LO Temperature compensated trim DAC. To control Vcstat slope for Vpos. Default Value: 0x4
4 : 0	VCT_TRIM_LO_HV	LO Bandgap Voltage Temperature Compensation trim control. Default Value: 0xF

8.1.39 FLASHC_FM_CTL_CAL_CTL1

Cal control BG HI trim bits

Address: 0x4024F054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	CDAC_HI_HV [7:5]				VCT_TRIM_HI_HV [4:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	VBG_TC_TRIM_HI_HV [15:13]				VBG_TRIM_HI_HV [12:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW	RW		
HW Access	None				R	R		
Name	None [23:20]				IPREF_TRIMA_HI_HV	ICREF_TC_TRIM_HI_HV [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19	IPREF_TRIMA_HI_HV	Adds 100-150nA boost on IPREF_HI Default Value: 0
18 : 16	ICREF_TC_TRIM_HI_HV	HI Bandgap Current Temperature Compensation trim control. Default Value: 0x3
15 : 13	VBG_TC_TRIM_HI_HV	HI Bandgap Voltage Temperature Compensation trim control. Default Value: 0x4
12 : 8	VBG_TRIM_HI_HV	HI Bandgap Voltage trim control. Default Value: 0xF
7 : 5	CDAC_HI_HV	HI Temperature compensated trim DAC. To control Vcstat slope for Vpos. Default Value: 0x4
4 : 0	VCT_TRIM_HI_HV	HI Bandgap Voltage Temperature Compensation trim control. Default Value: 0xF

8.1.40 FLASHC_FM_CTL_CAL_CTL2

Cal control BG LO trim bits

Address: 0x4024F058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	ICREF_TRIM_HI_HV [7:5]				ICREF_TRIM_LO_HV [4:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW					RW	
HW Access	R	R					R	
Name	IP-REF_TRIM_HI_HV	IPREF_TRIM_LO_HV [14:10]					ICREF_TRIM_HI_HV [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				IPREF_TRIM_HI_HV [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 15	IPREF_TRIM_HI_HV	HI Bandgap IPTAT trim control. Default Value: 0xF
14 : 10	IPREF_TRIM_LO_HV	LO Bandgap IPTAT trim control. Default Value: 0xF
9 : 5	ICREF_TRIM_HI_HV	HI Bandgap Current trim control. Default Value: 0x10
4 : 0	ICREF_TRIM_LO_HV	LO Bandgap Current trim control. Default Value: 0x10

8.1.41 FLASHC_FM_CTL_CAL_CTL3 (continued)

8.1.41 FLASHC_FM_CTL_CAL_CTL3

Cal control osc trim bits, idac, sdac, itim

Address: 0x4024F05C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW			
HW Access	R	R	R	R	R			
Name	VREF_SEL_HV	IP-REF_TC_HV	VPROT_ACT_HV	OS-C_RANGE_TRIM_HV	OSC_TRIM_HV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW		RW	RW		RW	RW
HW Access	R	R		R	R		R	R
Name	BGLO_EN_HV	TURBO_PULSEW_HV [14:13]		VDDHI_HV	FDIV_TRIM_HV [11:10]		REG_ACT_HV	IREF_SEL_HV

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [23:20]				LP_ULP_SW_HV	R_GRANT_EN_HV	CL_ISO_DIS_HV	BGHI_EN_HV

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19	LP_ULP_SW_HV	LP<-->ULP switch for trim signals: 0: LP 1: ULP Default Value: 0x0
18	R_GRANT_EN_HV	0: r_grant handshake disabled, r_grant always 1. 1: r_grand handshake enabled Default Value: 0
17	CL_ISO_DIS_HV	0: The internal logic controls the CL isolation 1: Forces CL bypass Default Value: 0x0

16	BGHI_EN_HV	0: Normal (Automatic change over from HI to LO) 1: Force enable HI Bandgap When both BGLO_EN_HV and BGHI_EN_HV are HIGH, only BGHI output is used and turbo_h-v_n pulse is active Default Value: 0x0
15	BGLO_EN_HV	0: Normal (Automatic change over from HI to LO) 1: Force enable LO Bandgap Default Value: 0x0
14 : 13	TURBO_PULSEW_HV	Turbo pulse width trim (Typical) 00: 40 us 01: 20 us 10: 15 us 11: 8 us Default Value: 0x1
12	VDDHI_HV	0: vdd < 2.3V 1: vdd >= 2.3V '0' setting can used for vdd > 2.3V also, but with a current penalty. Default Value: 0x0
11 : 10	FDIV_TRIM_HV	FDIV_TRIM_HV[1:0]: Assuming oscillator frequency of 8MHz in standby. Following are the clock frequencies seen by doubler 00: F = 1MHz 01: F = 0.5MHz 10: F = 2MHz 11: F = 4MHz Default Value: 0
9	REG_ACT_HV	0: VBST regulator will operate in active/standby mode based on control signal. 1: Forces the VBST regulator in active mode all the time Default Value: 0
8	IREF_SEL_HV	Current reference: 0: internal current reference 1: external current reference Default Value: 0x0
7	VREF_SEL_HV	Voltage reference: 0: internal bandgap reference 1: external voltage reference Default Value: 0x0
6	IPREF_TC_HV	0: Increases the IPREF Tempco by subtracting ICREF from IPREF - IPREF internal will be 0.5uA 1: Reduces the IPREF Tempco without subtracting ICREF from IPREF - IPREF internal will be 1uA Default Value: 0
5	VPROT_ACT_HV	Forces VPROT in active mode all the time Default Value: 0
4	OSC_RANGE_TRIM_HV	0: Oscillator High Frequency Range 1: Oscillator Low Frequency range Default Value: 0x0
3 : 0	OSC_TRIM_HV	Flash macro pump clock trim control. Default Value: 0x4

8.1.42 FLASHC_FM_CTL_CAL_CTL4 (continued)

8.1.42 FLASHC_FM_CTL_CAL_CTL4

Cal Control Vlim, SA, fdiv, reg_act

Address: 0x4024F060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW				RW	
HW Access	R		R				R	
Name	SDAC_ULP_HV [7:6]		IDAC_ULP_HV [5:2]				VLIM_TRIM_ULP_HV [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW		RW				
HW Access	R	R		R				
Name	SPARE451_ULP_HV	FM_READY_DEL_ULP_HV [14:13]		ITIM_ULP_HV [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [23:20]				UG-B_EN_HV	AUTO_HV-PULSE_HV	VB-ST_S_DIS_HV	READY_RESTART_N_HV

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19	UGB_EN_HV	UGB enable in TM control Default Value: 0
18	AUTO_HVPULSE_HV	0: HV Pulse controlled by FW 1: HV Pulse controlled by Hardware Default Value: 0
17	VBST_S_DIS_HV	0: VBST_S voltage for each sector to allow VBST level to be dropped to VCC during Erase in the selected sector, reducing coupling to GBL. 1: VBST_S voltage for each sector stays at VBST level during Erase in the selected sector. Default Value: 0
16	READY_RESTART_N_HV	Toggle: 1-->0, ready goes low, ready will remain low as long as the bit is low. Toggle the bit back to 1 to activate the ready logic. To be used by API only. Default Value: 1
15	SPARE451_ULP_HV	Default Value: 0

14 : 13	FM_READY_DEL_ULP_HV	00: Default : delay 1ns 01: Delayed by 1.5us 10: Delayed by 2.0us 11: Delayed by 2.5us Default Value: 0x1
12 : 8	ITIM_ULP_HV	Trimming of timing current Default Value: 0xA
7 : 6	SDAC_ULP_HV	Sets the sense current reference temp slope. Refer to trim tables for details. Default Value: 0x3
5 : 2	IDAC_ULP_HV	Sets the sense current reference offset value. Refer to trim tables for details. Default Value: 0x8
1 : 0	VLIM_TRIM_ULP_HV	VLIM_TRIM[1:0]: 00: V2 = 650mV 01: V2 = 600mV 10: V2 = 750mV 11: V2 = 700mV Default Value: 0

8.1.43 FLASHC_FM_CTL_CAL_CTL5 (continued)

8.1.43 FLASHC_FM_CTL_CAL_CTL5

Cal control

Address: 0x4024F064

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW				RW	
HW Access	R		R				R	
Name	SDAC_LP_HV [7:6]		IDAC_LP_HV [5:2]				VLIM_TRIM_LP_HV [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW		RW				
HW Access	R	R		R				
Name	SPARE451_LP_HV	FM_READY_DEL_LP_HV [14:13]		ITIM_LP_HV [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [23:20]				AMUX_SEL_HV [19:18]		SPARE52_HV [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 18	AMUX_SEL_HV	Amux Select in AMUX_UGB 00: Bypass UGB for both amuxbusa and amuxbusb 01: Bypass UGB for amuxbusb while passing amuxbusa through UGB. 10: Bypass UGB for amuxbusa while passing amuxbusb through UGB. 11: UGB Calibrate mode Default Value: 0
17 : 16	SPARE52_HV	Default Value: 0
15	SPARE451_LP_HV	Default Value: 0
14 : 13	FM_READY_DEL_LP_HV	00: Delayed by 1us 01: Delayed by 1.5us 10: Delayed by 2.0us 11: Delayed by 2.5us Default Value: 0x1
12 : 8	ITIM_LP_HV	Trimming of timing current Default Value: 0x0A

7 : 6	SDAC_LP_HV	Sets the sense current reference temp slope. Refer to trim tables for details. Default Value: 0x3
5 : 2	IDAC_LP_HV	Sets the sense current reference offset value. Refer to trim tables for details. Default Value: 0x8
1 : 0	VLIM_TRIM_LP_HV	VLIM_TRIM[1:0]: 00: V2 = 650mV 01: V2 = 600mV 10: V2 = 750mV 11: V2 = 700mV Default Value: 0

8.1.44 FLASHC_FM_CTL_CAL_CTL6 (continued)

8.1.44 FLASHC_FM_CTL_CAL_CTL6

SA trim LP/ULP

Address: 0x4024F068

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW			RW
HW Access	R	R			R			R
Name	SA_CT-L_TRIM_T6_ULP_HV	SA_CTL_TRIM_T5_ULP_HV [6:4]			SA_CTL_TRIM_T4_ULP_HV [3:1]			SA_CT-L_TRIM_T1_ULP_HV

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW			RW	RW	RW
HW Access	R		R			R	R	R
Name	SA_CT-L_TRIM_T5_LP_HV [15:14]		SA_CTL_TRIM_T4_LP_HV [13:11]			SA_CT-L_TRIM_T1_LP_HV	SA_CT-L_TRIM_T8_ULP_HV	SA_CT-L_TRIM_T6_ULP_HV

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW	RW		RW
HW Access	None				R	R		R
Name	None [23:20]				SA_CT-L_TRIM_T8_LP_HV	SA_CT-L_TRIM_T6_LP_HV [18:17]		SA_CT-L_TRIM_T5_LP_HV

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19	SA_CT-L_TRIM_T8_LP_HV	saen3 pulse width trim (Current trim) Default Value: 0x0
18 : 17	SA_CT-L_TRIM_T6_LP_HV	SA_CTL_TRIM_T6_LP_HV<1>= eni (enable current trim) SA_CTL_TRIM_T6_LP_HV<0> = ecn (enable cap trim) Default Value: 0x1
16 : 14	SA_CT-L_TRIM_T5_LP_HV	SA_CTL_TRIM_T5_LP_HV<2>= evi (integration current trim) SA_CTL_TRIM_T5_LP_HV<1:0> = evc (integration cap trim) Default Value: 0x5

13 : 11	SA_CT- L_TRIM_T4_LP_HV	SA_CTL_TRIM_T4_LP_HV<2>= eqi (eq current trim) SA_CTL_TRIM_T4_LP_HV<1:0> = eqc (eq cap trim) Default Value: 0x5
10	SA_CT- L_TRIM_T1_LP_HV	clk_trk delay Default Value: 0x1
9	SA_CT- L_TRIM_T8_ULP_HV	saen3 pulse width trim (Current trim) Default Value: 0x1
8 : 7	SA_CT- L_TRIM_T6_ULP_HV	SA_CTL_TRIM_T6_ULP_HV<1>= eni (enable current trim) SA_CTL_TRIM_T6_ULP_HV<0> = ecn (enable cap trim) Default Value: 0x2
6 : 4	SA_CT- L_TRIM_T5_ULP_HV	SA_CTL_TRIM_T5_ULP_HV<2>= evi (integration current trim) SA_CTL_TRIM_T5_ULP_HV<1:0> = evc (integration cap trim) Default Value: 0x7
3 : 1	SA_CT- L_TRIM_T4_ULP_HV	SA_CTL_TRIM_T4_ULP_HV<2>= eqi (eq current trim) SA_CTL_TRIM_T4_ULP_HV<1:0> = eqc (eq cap trim) Default Value: 0x7
0	SA_CT- L_TRIM_T1_ULP_HV	clk_trk delay Default Value: 0x1

8.1.45 FLASHC_FM_CTL_CAL_CTL7 (continued)

8.1.45 FLASHC_FM_CTL_CAL_CTL7

Cal control

Address: 0x4024F06C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	
HW Access	R	R	R	R	R	R	R	
Name	DISABLE_-LOAD_ON-CE_HV	ERSX-8_EN_ALL_HV	FM_READY_DIS_HV	NP-DAC_HWCTL_DIS_HV	TUR-BO_EX-T_HV	FM_AC-TIVE_HV	ERSX8_CLK_SEL_HV [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW					RW	
HW Access	R	R					R	
Name	SPARE7_LP_HV	SPARE7_ULP_HV [14:10]					SPARE7_HV [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				SPARE7_LP_HV [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 15	SPARE7_LP_HV	Default Value: 0
14 : 10	SPARE7_ULP_HV	Default Value: 0
9 : 8	SPARE7_HV	Default Value: 0
7	DISABLE_LOAD_ON-CE_HV	0: Load common HV params during API HV operations depends on the HV_PARAMS_LOADED bit in RGRANT_DELAY_PRG register. 1: All HV params are loaded during every API HV operation irrespective of HV_PARAMS_LOAD-ED bit in the RGRANT_DELAY_PRG register. Default Value: 0
6	ERSX8_EN_ALL_HV	0': Staggered turn on/off of GWL 1: GWL are turned on/off at the same time (old FM legacy) Default Value: 0

5	FM_READY_DIS_HV	0': fm ready is enabled 1: fm ready is disabled (fm_ready is always "1") Default Value: 0
4	NPDAC_HWCTL_DIS_HV	0': ndac, pdac staircase hardware controlled 1: ndac, pdac staircase disabled. Enables FW control. Default Value: 0
3	TURBO_EXT_HV	0: Normal operation 1: Uses external turbo pulse Default Value: 0x0
2	FM_ACTIVE_HV	0: Normal operation 1: Forces FM SYS in active mode Default Value: 0x0
1 : 0	ERSX8_CLK_SEL_HV	Clock frequency into the ersx8 shift register block 00: Oscillator clock 01: Oscillator clock / 2 10: Oscillator clock / 4 11: Oscillator clock Default Value: 0

8.1.46 FLASHC_FM_CTL_RED_CTL01

Redundancy Control normal sectors 0,1

Address: 0x4024F080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RED_ADDR_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RED_EN_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RED_ADDR_1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							RED_EN_1

Bits	Name	Description
24	RED_EN_1	1: Redundancy Enable for Sector 1 Default Value: 0
23 : 16	RED_ADDR_1	Bad Row Pair Address for Sector 1 Default Value: 0
8	RED_EN_0	1: Redundancy Enable for Sector 0 Default Value: 0
7 : 0	RED_ADDR_0	Bad Row Pair Address for Sector 0 Default Value: 0

8.1.47 FLASHC_FM_CTL_RED_CTL23

Redundancy Control normal sectors 2,3

Address: 0x4024F084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RED_ADDR_2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RED_EN_2

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RED_ADDR_3 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							RED_EN_3

Bits	Name	Description
24	RED_EN_3	1: Redundancy Enable for Sector 3 Default Value: 0
23 : 16	RED_ADDR_3	Bad Row Pair Address for Sector 3 Default Value: 0
8	RED_EN_2	1: Redundancy Enable for Sector 2 Default Value: 0
7 : 0	RED_ADDR_2	Bad Row Pair Address for Sector 2 Default Value: 0

8.1.48 FLASHC_FM_CTL_RED_CTL45

Redundancy Control normal sectors 4,5

Address: 0x4024F088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RED_ADDR_4 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RED_EN_4

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RED_ADDR_5 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							RED_EN_5

Bits	Name	Description
24	RED_EN_5	1: Redundancy Enable for Sector 5 Default Value: 0
23 : 16	RED_ADDR_5	Bad Row Pair Address for Sector 5 Default Value: 0
8	RED_EN_4	1: Redundancy Enable for Sector 4 Default Value: 0
7 : 0	RED_ADDR_4	Bad Row Pair Address for Sector 4 Default Value: 0

8.1.49 FLASHC_FM_CTL_RED_CTL67

Redundancy Control normal sectors 6,7

Address: 0x4024F08C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RED_ADDR_6 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RED_EN_6

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RED_ADDR_7 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							RED_EN_7

Bits	Name	Description
24	RED_EN_7	1: Redundancy Enable for Sector 7 Default Value: 0
23 : 16	RED_ADDR_7	Bad Row Pair Address for Sector 7 Default Value: 0
8	RED_EN_6	1: Redundancy Enable for Sector 6 Default Value: 0
7 : 0	RED_ADDR_6	Bad Row Pair Address for Sector 6 Default Value: 0

8.1.50 FLASHC_FM_CTL_RED_CTL_SM01

Redundancy Control special sectors 0,1

Address: 0x4024F090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RED_ADDR_SM0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RED_EN_SM0

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RED_ADDR_SM1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							RED_EN_SM1

Bits	Name	Description
24	RED_EN_SM1	Redundancy Enable for Special Sector 1 Default Value: 0
23 : 16	RED_ADDR_SM1	Bad Row Pair Address for Special Sector 1 Default Value: 0
8	RED_EN_SM0	Redundancy Enable for Special Sector 0 Default Value: 0
7 : 0	RED_ADDR_SM0	Bad Row Pair Address for Special Sector 0 Default Value: 0

8.1.51 FLASHC_FM_CTL_RGRANT_DELAY_PRG (continued)

8.1.51 FLASHC_FM_CTL_RGRANT_DELAY_PRG

R-grant delay for program

Address: 0x4024F098

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RGRANT_DELAY_PRG_SEQ12 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RGRANT_DELAY_PRG_SEQ23 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RGRANT_DELAY_SEQ30 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None			RW			
HW Access	R	None			R			
Name	HV_PARAMS_LOADED	None [30:28]			RGRANT_DELAY_CLK [27:24]			

Bits	Name	Description
31	HV_PARAMS_LOADED	0: HV Pulse common params not loaded 1: HV Pulse common params loaded: r-grant delays, r-grant scale, prescaler, timer values for seq1,seq2_pre, seq2_post, seq3 Default Value: 0
27 : 24	RGRANT_DELAY_CLK	Frequency divider from clk_t to create the 8MHz reference clock for R_grant delay The value of this field is the integer result of "clk_t frequency / 8". Example: for clk_t=100 this field is INT(100/8) =12. This field is updated at runtime with the "SW_RGRANT_DELAY_CLK " value from the HV parameters table Default Value: 1
23 : 16	RGRANT_DELAY_SEQ30	PROG_PROG & ERASE: R-grant blocking delay on seq3-seq0 transition. Scale = ANA_CTL0.SCALE_SEQ30 When = 0 R_GRANT_DELAY control is disabled when IF_SEL=1 R_GRANT_DELAY control is disabled Default Value: 0

15 : 8	RGRANT_DELAY_PRG_SEQ23	PROG_PROG: R-grant blocking delay on seq2-seq3 transition. Scale = ANA_CTL0.SCALE_SEQ23 When = 0 R_GRANT_DELAY control is disabled when IF_SEL=1 R_GRANT_DELAY control is disabled Default Value: 0
7 : 0	RGRANT_DELAY_PRG_SEQ12	PROG_PROG: R-grant blocking delay on seq1-seq2 transition. Scale = ANA_CTL0.SCALE_SEQ12 When = 0 R_GRANT_DELAY control is disabled when IF_SEL=1 R_GRANT_DELAY control is disabled Default Value: 0

8.1.52 FLASHC_FM_CTL_PW_SEQ12

HV Pulse Delay for seq 1&2 pre

Address: 0x4024F0A0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PW_SEQ1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PW_SEQ1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	PW_SEQ2_PRE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	PW_SEQ2_PRE [31:24]							

Bits	Name	Description
31 : 16	PW_SEQ2_PRE	Seq2 pre delay Default Value: 0
15 : 0	PW_SEQ1	Seq1 delay Default Value: 0

8.1.53 FLASHC_FM_CTL_PW_SEQ23

HV Pulse Delay for seq2 post & seq3

Address: 0x4024F0A4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PW_SEQ2_POST [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PW_SEQ2_POST [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	PW_SEQ3 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	PW_SEQ3 [31:24]							

Bits	Name	Description
31 : 16	PW_SEQ3	Seq3 delay Default Value: 0
15 : 0	PW_SEQ2_POST	Seq2 post delay Default Value: 0

8.1.54 FLASHC_FM_CTL_RGRANT_SCALE_ERS (continued)

8.1.54 FLASHC_FM_CTL_RGRANT_SCALE_ERS

R-grant delay scale for erase

Address: 0x4024F0A8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	SCALE_ERS_PEON [7:6]		SCALE_ERS_SEQ23 [5:4]		SCALE_ERS_SEQ12 [3:2]		SCALE_ERS_SEQ01 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SCALE_ERS_PEOFF [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RGRANT_DELAY_ERS_PEON [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	RGRANT_DELAY_ERS_PEOFF [31:24]							

Bits	Name	Description
31 : 24	RGRANT_DELAY_ERS_PEOFF	ERASE: R-grant blocking delay on PE OFF. Scale = ANA_CTL0.SCALE_PEOFF When = 0 R_GRANT_DELAY control is disabled when IF_SEL=1 R_GRANT_DELAY control is disabled Default Value: 0
23 : 16	RGRANT_DELAY_ERS_PEON	ERASE: R-grant blocking delay on PE ON. Scale = ANA_CTL0.SCALE_PEON When = 0 R_GRANT_DELAY control is disabled when IF_SEL=1 R_GRANT_DELAY control is disabled Default Value: 0
9 : 8	SCALE_ERS_PEOFF	ERASE: Scale for R_GRANT_DELAY on PE OFF transition: 00: 0.125uS 01: 1uS 10: 10uS 11: 100uS Default Value: 0

7 : 6	SCALE_ERS_PEON	ERASE: Scale for R_GRANT_DELAY on PE On transition: 00: 0.125uS 01: 1uS 10: 10uS 11: 100uS Default Value: 0
5 : 4	SCALE_ERS_SEQ23	ERASE: Scale for R_GRANT_DELAY on seq2-seq3 transition: 00: 0.125uS 01: 1uS 10: 10uS 11: 100uS Default Value: 0
3 : 2	SCALE_ERS_SEQ12	ERASE: Scale for R_GRANT_DELAY on seq1-seq2 transition: 00: 0.125uS 01: 1uS 10: 10uS 11: 100uS Default Value: 0
1 : 0	SCALE_ERS_SEQ01	ERASE: Scale for R_GRANT_DELAY on seq0-seq1 transition: 00: 0.125uS 01: 1uS 10: 10uS 11: 100uS Default Value: 0

8.1.55 FLASHC_FM_CTL_RGRANT_DELAY_ERS

R-grant delay for erase

Address: 0x4024F0AC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RGRANT_DELAY_ERS_SEQ01 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RGRANT_DELAY_ERS_SEQ12 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RGRANT_DELAY_ERS_SEQ23 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	RGRANT_DELAY_ERS_SEQ23	ERASE: R-grant blocking delay on seq2-seq3 transition. Scale = ANA_CTL0.SCALE_SEQ23 When = 0 R_GRANT_DELAY control is disabled when IF_SEL=1 R_GRANT_DELAY control is disabled Default Value: 0
15 : 8	RGRANT_DELAY_ERS_SEQ12	ERASE: R-grant blocking delay on seq1-seq2 transition. Scale = ANA_CTL0.SCALE_SEQ12 When = 0 R_GRANT_DELAY control is disabled when IF_SEL=1 R_GRANT_DELAY control is disabled Default Value: 0
7 : 0	RGRANT_DELAY_ERS_SEQ01	ERASE: R-grant blocking delay on seq0-seq1 transition. Scale = ANA_CTL0.SCALE_SEQ01 When = 0 R_GRANT_DELAY control is disabled when IF_SEL=1 R_GRANT_DELAY control is disabled Default Value: 0

8.1.56 FLASHC_FM_CTL_FM_PL_WRDATA_ALL

Flash macro write page latches all

Address: 0x4024F7FC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Write all high Voltage page latches with the same 32-bit data in a single write cycle Read always returns 0. Default Value: 0

8.1.57 FLASHC_FM_CTL_FM_PL_DATA0

Flash macro Page Latches data

Address: 0x4024F800

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Four page latch Bytes When reading the page latches it requires FM_CTL.IF_SEL to be '1' Note: the high Voltage page latches are readable for test mode functionality. Default Value: 0

8.1.58 FLASHC_FM_CTL_FM_MEM_DATA0 (continued)

8.1.58 FLASHC_FM_CTL_FM_MEM_DATA0

Flash macro memory sense amplifier and column decoder data

Address: 0x4024FC00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Sense amplifier and column multiplexer structure Bytes. The read data is dependent on FM_CTL.IF_SEL: - IF_SEL is 0: data as specified by the R interface address - IF_SEL is 1: data as specified by FM_MEM_ADDR and the offset of the accessed FM_MEM_-DATA register. Default Value: 0

9 System Resources Subsystem Registers

This section discusses the System Resources Subsystem (SRSS) registers. It lists all the registers in mapping tables, in address order.

9.1 Register Details

Register	Address	Description
PWR_CTL	0x40260000	Power Mode Control
PWR_HIBERNATE	0x40260004	HIBERNATE Mode Register
PWR_LVD_CTL	0x40260008	Low Voltage Detector (LVD) Configuration Register
PWR_BUCK_CTL	0x40260014	Buck Control Register
PWR_LVD_STATUS	0x4026001C	Low Voltage Detector (LVD) Status Register
PWR_HIB_DATA0	0x40260080	HIBERNATE Data Register
WDT_CTL	0x40260180	Watchdog Counter Control Register
WDT_CNT	0x40260184	Watchdog Counter Count Register
WDT_MATCH	0x40260188	Watchdog Counter Match Register
CLK_DSI_SELECT0	0x40260300	Clock DSI Select Register
CLK_DSI_SELECT1	0x40260304	Clock DSI Select Register. See CLK_DSI_SELECT0 for the details of bit fields.
CLK_DSI_SELECT2	0x40260308	Clock DSI Select Register. See CLK_DSI_SELECT0 for the details of bit fields.
CLK_DSI_SELECT3	0x4026030C	Clock DSI Select Register. See CLK_DSI_SELECT0 for the details of bit fields.
CLK_DSI_SELECT4	0x40260310	Clock DSI Select Register. See CLK_DSI_SELECT0 for the details of bit fields.
CLK_PATH_SELECT0	0x40260340	Clock Path Select Register
CLK_PATH_SELECT1	0x40260344	Clock Path Select Register. See CLK_PATH_SELECT0 for the details of bit fields.
CLK_PATH_SELECT2	0x40260348	Clock Path Select Register. See CLK_PATH_SELECT0 for the details of bit fields.
CLK_PATH_SELECT3	0x4026034C	Clock Path Select Register. See CLK_PATH_SELECT0 for the details of bit fields.
CLK_PATH_SELECT4	0x40260350	Clock Path Select Register. See CLK_PATH_SELECT0 for the details of bit fields.
CLK_ROOT_SELECT0	0x40260380	Clock Root Select Register
CLK_ROOT_SELECT1	0x40260384	Clock Root Select Register. See CLK_ROOT_SELECT0 for the details of bit fields.
CLK_ROOT_SELECT2	0x40260388	Clock Root Select Register. See CLK_ROOT_SELECT0 for the details of bit fields.
CLK_ROOT_SELECT3	0x4026038C	Clock Root Select Register. See CLK_ROOT_SELECT0 for the details of bit fields.
CLK_SELECT	0x40260500	Clock selection register
CLK_TIMER_CTL	0x40260504	Timer Clock Control Register
CLK_ILO_CONFIG	0x4026050C	ILO Configuration

Register	Address	Description
CLK_IMO_CONFIG	0x40260510	IMO Configuration
CLK_OUTPUT_FAST	0x40260514	Fast Clock Output Select Register
CLK_OUTPUT_SLOW	0x40260518	Slow Clock Output Select Register
CLK_CAL_CNT1	0x4026051C	Clock Calibration Counter 1
CLK_CAL_CNT2	0x40260520	Clock Calibration Counter 2
CLK_ECO_CONFIG	0x4026052C	ECO Configuration Register
CLK_ECO_STATUS	0x40260530	ECO Status Register
CLK_MF_SELECT	0x40260544	Medium Frequency Clock Select Register
CLK_MFO_CONFIG	0x40260548	MFO Configuration Register
CLK_FLL_CONFIG	0x40260580	FLL Configuration Register
CLK_FLL_CONFIG2	0x40260584	FLL Configuration Register 2
CLK_FLL_CONFIG3	0x40260588	FLL Configuration Register 3
CLK_FLL_CONFIG4	0x4026058C	FLL Configuration Register 4
CLK_FLL_STATUS	0x40260590	FLL Status Register
CLK_PLL_CONFIG0	0x40260600	PLL Configuration Register
CLK_PLL_STATUS0	0x40260640	PLL Status Register
SRSS_INTR	0x40260700	SRSS Interrupt Register
SRSS_INTR_SET	0x40260704	SRSS Interrupt Set Register
SRSS_INTR_MASK	0x40260708	SRSS Interrupt Mask Register
SRSS_INTR_MASKED	0x4026070C	SRSS Interrupt Masked Register
SRSS_INTR_CFG	0x40260710	SRSS Interrupt Configuration Register
RES_CAUSE	0x40260800	Reset Cause Observation Register
RES_CAUSE2	0x40260804	Reset Cause Observation Register 2
PWR_TRIM_REF_CTL	0x40267F00	Reference Trim Register
PWR_TRIM_BODOVP_CTL	0x40267F04	BOD/OVP Trim Register
CLK_TRIM_CCO_CTL	0x40267F08	CCO Trim Register
CLK_TRIM_CCO_CTL2	0x40267F0C	CCO Trim Register 2
PWR_TRIM_WAKE_CTL	0x40267F30	Wakeup Trim Register
PWR_TRIM_LVD_CTL	0x4026FF10	LVD Trim Register
CLK_TRIM_ILO_CTL	0x4026FF18	ILO Trim Register
PWR_TRIM_PWRSYS_CTL	0x4026FF1C	Power System Trim Register
CLK_TRIM_ECO_CTL	0x4026FF20	ECO Trim Register

9.1.1 PWR_CTL

Power Mode Control

Address: 0x40260000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	None		R	
HW Access	None		RW	RW	None		RW	
Name	None [7:6]		LP-M_READY	DEBUG_-SESSION	None [3:2]		POWER_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	R	RW	None	
HW Access	A	A	A	A	RW	A	None	
Name	LIN-REG_DIS	NWELL_REG_DIS	RET_REG_DIS	DPS-LP_REG_DIS	VREF-BUF_OK	IREF_LP-MODE	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	R	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	A	A	A	R	A	A	A
Name	ACT_REF_OK	ACT_REF_DIS	VREF-BUF_DIS	VREF-BUF_LP-MODE	PLL_LS_BYPASS	BGREF_LP MODE	POR-BOD_LP-MODE	LIN-REG_LP-MODE

Bits	Name	Description
31	ACT_REF_OK	Indicates that the normal mode of the Active Reference is ready. Default Value: 0
30	ACT_REF_DIS	Disables the Active Reference. Firmware must ensure that LPM_READY==1 and BGREF_LP-MODE==1 for at least 1us before disabling the Active Reference. When enabling the Active Reference, use ACT_REF_OK indicator to know when it is ready. This register is only reset by XRES/POR/BOD/HIBERNATE. 0: Active Reference is enabled 1: Active Reference is disabled Default Value: 0
29	VREFBUF_DIS	Disable the 800mV voltage reference buffer. Firmware should only disable the buffer when there is no connected circuit that is using it. SRSS circuits that require it are the PLL and ECO. A particular product may have circuits outside the SRSS that use the buffer. This register is only reset by XRES/POR/BOD/HIBERNATE. Default Value: 0

9.1.1 PWR_CTL (continued)

28	VREFBUF_LPMODE	Control the power mode of the 800mV voltage reference buffer. The value in this register is ignored and normal mode is used until LPM_READY==1. 0: Voltage Reference Buffer operates in normal mode. This register is only reset by XRES/POR/BOD/HIBERNATE. 1: Voltage Reference Buffer operates in low power mode. Power supply rejection is reduced to save current. Default Value: 0
27	PLL_LS_BYPASS	Bypass level shifter inside the PLL. 0: Do not bypass the level shifter. This setting is ok for all operational modes and vccd target voltage. 1: Bypass the level shifter. This may reduce jitter on the PLL output clock, but can only be used when vccd is targeted to 1.1V nominal. Otherwise, it can result in clock degradation and static current. Default Value: 0
26	BGREF_LPMODE	Control the power mode of the Bandgap Voltage and Current References. This applies to voltage and current generation and is different than the reference voltage buffer. The value in this register is ignored and normal mode is used until LPM_READY==1. When lower power mode is used, the Active Reference circuit can be disabled to reduce current. Firmware is responsible to ensure ACT_REF_OK==1 before changing back to normal mode. This register is only reset by XRES/POR/BOD/HIBERNATE. 0: Active Bandgap Voltage and Current Reference operates in normal mode. 1: Active Bandgap Voltage and Current Reference operates in low power mode. Power supply rejection is reduced to save current. The Active Reference may be disabled using ACT_REF_DIS=0. Default Value: 0
25	PORBOD_LPMODE	Control the power mode of the POR/BOD circuits. The value in this register is ignored and normal mode is used until LPM_READY==1. This register is only reset by XRES/POR/BOD/HIBERNATE. 0: POR/BOD circuits operate in normal mode. 1: POR/BOD circuits operate in low power mode. Response time is reduced to save current. Default Value: 0
24	LINREG_LPMODE	Control the power mode of the Linear Regulator. The value in this register is ignored and normal mode is used until LPM_READY==1. This register is only reset by XRES/POR/BOD/HIBERNATE. 0: Linear Regulator operates in normal mode. 1: Linear Regulator operates in low power mode. Load current capability is reduced, and firmware must ensure the current is kept within the limit for this operating mode. Default Value: 0
23	LINREG_DIS	Disable the linear Core Regulator. This is only legal when the on-chip buck regulator supplies vccd, but there is no hardware protection for this case. This register is only reset by XRES/POR/BOD/HIBERNATE. 0: Linear regulator is on. 1: Linear regulator is off. Default Value: 0
22	NWELL_REG_DIS	Disable the Nwell regulator. This is only legal when the on-chip buck regulator supplies vccd, but there is no hardware protection for this case. This register is only reset by XRES/POR/BOD/HIBERNATE. 0: Nwell Regulator is on. 1: Nwell Regulator is off. Default Value: 0

9.1.1 PWR_CTL (continued)

21	RET_REG_DIS	Disable the Retention regulator. This is only legal when the on-chip buck regulator supplies vccd, but there is no hardware protection for this case. This register is only reset by XRES/POR/BOD/HIBERNATE. 0: Retention Regulator is on. 1: Retention Regulator is off. Default Value: 0
20	DPSLP_REG_DIS	Disable the DeepSleep regulator. This is only legal when the on-chip buck regulator supplies vccd, but there is no hardware protection for this case. This register is only reset by XRES/POR/BOD/HIBERNATE. 0: DeepSleep Regulator is on. 1: DeepSleep Regulator is off. Default Value: 0
19	VREFBUF_OK	Indicates that the voltage reference buffer is ready. Due to synchronization delays, it may take two IMO clock cycles for hardware to clear this bit after asserting VREFBUF_DIS=1. Default Value: 0
18	IREF_LPMODE	Control the power mode of the reference current generator. The value in this register is ignored and normal mode is used until LPM_READY==1. This register is only reset by XRES/POR/BOD/HIBERNATE. 0: Current reference generator operates in normal mode. 1: Current reference generator operates in low power mode. Response time is reduced to save current. Default Value: 0
5	LPM_READY	Indicates whether certain low power functions are ready. The low current circuits take longer to startup after XRES/POR/BOD/HIBERNATE wakeup than the normal mode circuits. HIBERNATE mode may be entered regardless of this bit. This register is only reset by XRES/POR/BOD/HIBERNATE. 0: If a low power circuit operation is requested, it will stay in its normal operating mode until it is ready. If DEEPSLEEP is requested by all processors WFI/WFE, the device will instead enter SLEEP. When low power circuits are ready, device will automatically enter the originally requested mode. 1: Normal operation. DEEPSLEEP and low power circuits operate as requested in other registers. Default Value: 0
4	DEBUG_SESSION	Indicates whether a debug session is active (CDBGPWRUPREQ signal is 1) Default Value: 0 **0x0: NO_SESSION :** No debug session active **0x1: SESSION_ACTIVE :** Debug session is active. Power modes behave differently to keep the debug session active, and current consumption may be higher than datasheet specification.
1 : 0	POWER_MODE	Current power mode of the device. Note that this field cannot be read in all power modes on actual silicon. Default Value: 0 **0x0: RESET :** System is resetting.

9.1.1 PWR_CTL (continued)

0x1: ACTIVE :

At least one CPU is running.

0x2: SLEEP :

No CPUs are running. Peripherals may be running.

0x3: DEEPSLEEP :

Main high-frequency clock is off; low speed clocks are available. Communication interface clocks may be present.

9.1.2 PWR_HIBERNATE

HIBERNATE Mode Register

Address: 0x40260004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	TOKEN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	UNLOCK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW	RW	RW	None
HW Access	A				A	A	A	None
Name	POLARITY_HIBPIN [23:20]				MASK_HIB-WDT	MASK_HI-BALARM	FREEZE	None

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW1S	None		RW			
HW Access	A	R	None		A			
Name	HIBER-NATE	HIBER-NATE_DIS-ABLE	None [29:28]		MASK_HIBPIN [27:24]			

Bits	Name	Description
31	HIBERNATE	Firmware sets this bit to enter HIBERNATE mode. The system will enter HIBERNATE mode immediately after writing to this bit and will wakeup only in response to XRES or WAKEUP event. Both UNLOCK and FREEZE must have been set correctly in a previous write operations. Otherwise, it will not enter HIBERNATE. External supplies must have been stable for 250us before entering HIBERNATE mode. Default Value: 0
30	HIBERNATE_DISABLE	Hibernate disable bit. 0: Normal operation, HIBERNATE works as described 1: Further writes to this register are ignored Note: This bit is a write-once bit until the next reset. Avoid changing any other bits in this register while disabling HIBERNATE mode. Also, it is recommended to clear the UNLOCK code, if it was previously written.. Default Value: 0
27 : 24	MASK_HIBPIN	When set, HIBERNATE will wakeup if the corresponding pin input matches the POLARITY_HIBPIN setting. Each bit corresponds to one of the HIBERNATE wakeup pins. Default Value: 0

9.1.2 PWR_HIBERNATE (continued)

23 : 20	POLARITY_HIBPIN	Each bit sets the active polarity of the corresponding wakeup pin. 0: Pin input of 0 will wakeup the part from HIBERNATE 1: Pin input of 1 will wakeup the part from HIBERNATE Default Value: 0
19	MASK_HIBWDT	When set, HIBERNATE will wakeup if WDT matches Default Value: 0
18	MASK_HIBALARM	When set, HIBERNATE will wakeup for a RTC interrupt Default Value: 0
17	FREEZE	Controls whether mode and state of GPIOs and SIOs in the system are frozen. This is intended to be used as part of the HIBERNATE entry and exit sequences. When entering HIBERNATE mode, the first write instructs DEEPSLEEP peripherals that they cannot ignore the upcoming freeze command. This occurs even in the illegal condition where UNLOCK is not set. If UNLOCK and HIBERNATE are properly set, the IOs actually freeze on the second write. Default Value: 0
15 : 8	UNLOCK	This byte must be set to 0x3A for FREEZE or HIBERNATE fields to operate. Any other value in this register will cause FREEZE/HIBERNATE to have no effect, except as noted in the FREEZE description. Default Value: 0
7 : 0	TOKEN	Contains a 8-bit token that is retained through a HIBERNATE/WAKEUP sequence that can be used by firmware to differentiate WAKEUP from a general RESET event. Note that waking up from HIBERNATE using XRES will reset this register. Default Value: 0

9.1.3 PWR_LVD_CTL

Low Voltage Detector (LVD) Configuration Register

Address: 0x40260008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW			
HW Access	A	R			R			
Name	HVLVD1_EN	HVLVD1_SRCSEL [6:4]			HVLVD1_TRIPSEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	HVLVD1_EN	Enable HVLVD1 voltage monitor. When the LVD is enabled, it takes 20us for it to settle. There is no hardware stabilization counter, and it may falsely trigger during settling. It is recommended that firmware keep the interrupt masked for at least 8us, write a 1'b1 to the corresponding SRSS_INTR field to any falsely pended interrupt, and then optionally unmask the interrupt. After enabling, it is further recommended to read the related PWR_LVD_STATUS field, since the interrupt only triggers on edges. This bit is cleared (LVD is disabled) when entering DEEPSLEEP to prevent false interrupts during wakeup. Default Value: 0
6 : 4	HVLVD1_SRCSEL	Source selection for HVLVD1 Default Value: 0 **0x0: VDDD :** Select VDDD **0x1: AMUXBUSA :** Select AMUXBUSA (VDDD branch)

9.1.3 PWR_LVD_CTL (continued)

		0x2: RESERVED : Reserved. Connected AMUXBUSA (VDDD branch) **0x3: VDDIO :** Reserved. Selects VDDD. **0x4: AMUXBUSB :** Select AMUXBUSB (VDDD branch)
3 : 0	HVLVD1_TRIPSEL	Threshold selection for HVLVD1. Disable the LVD (HVLVD1_EN=0) before changing the threshold. 0: rise=1.225V (nom), fall=1.2V (nom) 1: rise=1.425V (nom), fall=1.4V (nom) 2: rise=1.625V (nom), fall=1.6V (nom) 3: rise=1.825V (nom), fall=1.8V (nom) 4: rise=2.025V (nom), fall=2V (nom) 5: rise=2.125V (nom), fall=2.1V (nom) 6: rise=2.225V (nom), fall=2.2V (nom) 7: rise=2.325V (nom), fall=2.3V (nom) 8: rise=2.425V (nom), fall=2.4V (nom) 9: rise=2.525V (nom), fall=2.5V (nom) 10: rise=2.625V (nom), fall=2.6V (nom) 11: rise=2.725V (nom), fall=2.7V (nom) 12: rise=2.825V (nom), fall=2.8V (nom) 13: rise=2.925V (nom), fall=2.9V (nom) 14: rise=3.025V (nom), fall=3.0V (nom) 15: rise=3.125V (nom), fall=3.1V (nom) Default Value: 0

9.1.4 PWR_BUCK_CTL

Buck Control Register

Address: 0x40260014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					A		
Name	None [7:3]					BUCK_OUT1_SEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	A	A	None					
Name	BUCK_OUT1_EN	BUCK_EN	None [29:24]					

Bits	Name	Description
31	BUCK_OUT1_EN	Enable for vccbuck1 output. The value in this register is ignored unless PWR_-BUCK_CTL.BUCK_EN==1. This register is only reset by XRES/POR/BOD/HIBERNATE. The regulator takes up to 600us to charge the external capacitor. If there is additional load current while charging, this will increase the startup time. The TRM specifies the required sequence when transitioning vccd from the LDO to SIMO Buck output #1. Default Value: 0
30	BUCK_EN	Master enable for buck converter. This register is only reset by XRES/POR/BOD/HIBERNATE. Default Value: 0

9.1.4 PWR_BUCK_CTL (continued)

2 : 0	BUCK_OUT1_SEL	Voltage output selection for vccbuck1 output. This register is only reset by XRES/POR/BOD/HIBERNATE. When increasing the voltage, it can take up to 200us for the output voltage to settle. When decreasing the voltage, the settling time depends on the load current. 0: 0.85V 1: 0.875V 2: 0.90V 3: 0.95V 4: 1.05V 5: 1.10V 6: 1.15V 7: 1.20V Default Value: 5

9.1.5 PWR_LVD_STATUS

Low Voltage Detector (LVD) Status Register

Address: 0x4026001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							HVL-VD1_OK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	HVLVD1_OK	HVLVD1 output. 0: below voltage threshold 1: above voltage threshold Default Value: 0

9.1.6 PWR_HIB_DATA0

HIBERNATE Data Register

Address: 0x40260080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	HIB_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	HIB_DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	HIB_DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	HIB_DATA [31:24]							

Bits	Name	Description
31 : 0	HIB_DATA	Additional data that is retained through a HIBERNATE/WAKEUP sequence that can be used by firmware for any application-specific purpose. Note that waking up from HIBERNATE using XRES will reset this register. Default Value: 0

9.1.7 WDT_CTL

Watchdog Counter Control Register

Address: 0x40260180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							A
Name	None [7:1]							WDT_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	A		None					
Name	WDT_LOCK [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	WDT_LOCK	Prohibits writing to WDT_*, CLK_ILO_CONFIG, CLK_SELECT.LFCLK_SEL, and CLK_TRIM_ILO_CTL registers when not equal 0. Requires at least two different writes to unlock. A change in WDT_LOCK takes effect beginning with the next write cycle. Note that this field is 2 bits to force multiple writes only. It represents only a single write protect signal protecting all those registers at the same time. WDT will lock on any reset. This field is not retained during Deep Sleep or Hibernate mode, so the WDT will be locked after wakeup from these modes. Default Value: 3 **0x0: NO_CHG :** No effect **0x1: CLR0 :** Clears bit 0

9.1.7 WDT_CTL (continued)

		0x2: CLR1 : Clears bit 1 **0x3: SET01 :** Sets both bits 0 and 1
0	WDT_EN	Enable this watchdog timer. This field is retained during Deep Sleep and Hibernate modes. Even though the default value is 1, in most cases the Cortex-M0+ executing the SROM code will change the value of this bit to 0. So effectively the user code starts with the WDT disabled. Default Value: 1

9.1.8 WDT_CNT

Watchdog Counter Count Register

Address: 0x40260184

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	Current value of WDT Counter. The write feature of this register is for verification purposes, has no synchronization, and can only be applied when the WDT is off. When writing, the value is updated immediately in the WDT counter, but it will read back as the old value until this register resynchronizes just after the negative edge of ILO. Writes will be ignored if they occur when the WDT is enabled. Default Value: 0

9.1.9 WDT_MATCH

Watchdog Counter Match Register

Address: 0x40260188

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	MATCH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	MATCH [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				A			
Name	None [23:20]				IGNORE_BITS [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	IGNORE_BITS	The number of MSB bits of the watchdog timer that are NOT checked against MATCH. This value provides control over the time-to-reset of the watchdog (which happens after 3 successive matches). Up to 12 MSB can be ignored. Settings >12 behave like a setting of 12. Default Value: 0
15 : 0	MATCH	Match value for Watchdog counter. Every time WDT_COUNTER reaches MATCH an interrupt is generated. Two unserviced interrupts will lead to a system reset (i.e. at the third match). Default Value: 0x1000

9.1.10 CLK_DSI_SELECT0

Clock DSI Select Register

Address: 0x40260300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			DSI_MUX [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	DSI_MUX	Selects a DSI source or low frequency clock for use in a clock path. The output of this mux can be selected for clock PATH *using CLK_PATH_SELECT register. Using the output of this mux as HFCLK source will result in undefined behavior. It can be used to clocks to DSI or to the reference inputs of FLL/PLL, subject to the frequency limits of those circuits. This mux is not glitch free, so do not change the selection while it is an actively selected clock. Default Value: 0* **0x0: DSI_OUT0 :** DSI0 - dsi_out[0] **0x1: DSI_OUT1 :** DSI1 - dsi_out[1] **0x2: DSI_OUT2 :** DSI2 - dsi_out[2]

9.1.10 CLK_DSI_SELECT0 (continued)

0x3: DSI_OUT3 :

DSI3 - dsi_out[3]

0x4: DSI_OUT4 :

DSI4 - dsi_out[4]

0x5: DSI_OUT5 :

DSI5 - dsi_out[5]

0x6: DSI_OUT6 :

DSI6 - dsi_out[6]

0x7: DSI_OUT7 :

DSI7 - dsi_out[7]

0x8: DSI_OUT8 :

DSI8 - dsi_out[8]

0x9: DSI_OUT9 :

DSI9 - dsi_out[9]

0xa: DSI_OUT10 :

DSI10 - dsi_out[10]

0xb: DSI_OUT11 :

DSI11 - dsi_out[11]

0xc: DSI_OUT12 :

DSI12 - dsi_out[12]

0xd: DSI_OUT13 :

DSI13 - dsi_out[13]

0xe: DSI_OUT14 :

DSI14 - dsi_out[14]

9.1.10 CLK_DSI_SELECT0 (continued)

0xf: DSI_OUT15 :

DSI15 - dsi_out[15]

0x10: ILO :

ILO - Internal Low-speed Oscillator

0x11: WCO :

WCO - Watch-Crystal Oscillator

0x12: ALTLF :

ALTLF - Alternate Low-Frequency Clock

0x13: PILO :

PILO - Precision Internal Low-speed Oscillator

9.1.11 CLK_PATH_SELECT0

Clock Path Select Register

Address: 0x40260340

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					PATH_MUX [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	PATH_MUX	Selects a source for clock PATH. *Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. Default Value: 0* **0x0: IMO :** IMO - Internal R/C Oscillator **0x1: EXTCLK :** EXTCLK - External Clock Pin **0x2: ECO :** ECO - External-Crystal Oscillator **0x3: ALTHF :** ALTHF - Alternate High-Frequency clock input (product-specific clock)

9.1.11 CLK_PATH_SELECT0 (continued)

0x4: DSI_MUX :

DSI_MUX - Output of DSI mux for this path. Using a DSI source directly as root of HFCLK will result in undefined behavior.

9.1.12 CLK_ROOT_SELECT0

Clock Root Select Register

Address: 0x40260380

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW			
HW Access	None		R		R			
Name	None [7:6]		ROOT_DIV [5:4]		ROOT_MUX [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	A	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	Enable for this clock root. All clock roots default to disabled (ENABLE==0) except HFCLK0, which cannot be disabled. Default Value: 0
5 : 4	ROOT_DIV	Selects predivider value for this clock root and DSI input. Default Value: 0 **0x0: NO_DIV :** Transparent mode, feed through selected clock source w/o dividing. **0x1: DIV_BY_2 :** Divide selected clock source by 2 **0x2: DIV_BY_4 :** Divide selected clock source by 4

9.1.12 CLK_ROOT_SELECT0 (continued)

0x3: DIV_BY_8 :

Divide selected clock source by 8

3 : 0	ROOT_MUX	Selects a clock path as the root of HFCLK and for SRSS DSI input . Use CLK_PATH_SELECT[i] to configure the desired path. Some paths may have FLL or PLL available (product-specific), and the control and bypass mux selections of these are in other registers. Configure the FLL using CLK_FLL_CONFIG register. Configure a PLL using the related CLK_PLL_CONFIG[k] register. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. Default Value: 0 **0x0: PATH0 :** Select PATH0 (can be configured for FLL) **0x1: PATH1 :** Select PATH1 (can be configured for PLL0, if available in the product) **0x2: PATH2 :** Select PATH2 (can be configured for PLL1, if available in the product) **0x3: PATH3 :** Select PATH3 (can be configured for PLL2, if available in the product) **0x4: PATH4 :** Select PATH4 (can be configured for PLL3, if available in the product) **0x5: PATH5 :** Select PATH5 (can be configured for PLL4, if available in the product) **0x6: PATH6 :** Select PATH6 (can be configured for PLL5, if available in the product) **0x7: PATH7 :** Select PATH7 (can be configured for PLL6, if available in the product) **0x8: PATH8 :** Select PATH8 (can be configured for PLL7, if available in the product) **0x9: PATH9 :** Select PATH9 (can be configured for PLL8, if available in the product)

9.1.12 CLK_ROOT_SELECT0 (continued)

0xa: PATH10 :

Select PATH10 (can be configured for PLL9, if available in the product)

0xb: PATH11 :

Select PATH11 (can be configured for PLL10, if available in the product)

0xc: PATH12 :

Select PATH12 (can be configured for PLL11, if available in the product)

0xd: PATH13 :

Select PATH13 (can be configured for PLL12, if available in the product)

0xe: PATH14 :

Select PATH14 (can be configured for PLL13, if available in the product)

0xf: PATH15 :

Select PATH15 (can be configured for PLL14, if available in the product)

9.1.13 CLK_SELECT

Clock selection register

Address: 0x40260500

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						A	
Name	None [7:2]						LFCLK_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			
HW Access	R	R			R			
Name	PUMP_ENABLE	PUMP_DIV [14:12]			PUMP_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	PUMP_ENABLE	Enable the pump clock. PUMP_ENABLE and the PUMP_SEL mux are not glitch-free to minimize side-effects, avoid changing the PUMP_SEL and PUMP_DIV while changing PUMP_ENABLE. To change the settings, do the following: 1) If the pump clock is enabled, write PUMP_ENABLE=0 without changing PUMP_SEL and PUMP_DIV. 2) Change PUMP_SEL and PUMP_DIV to desired settings with PUMP_ENABLE=0. 3) Write PUMP_ENABLE=1 without changing PUMP_SEL and PUMP_DIV. Default Value: 0
14 : 12	PUMP_DIV	Division ratio for PUMPCLK. Uses selected PUMP_SEL clock as the source. Default Value: 0 **0x0: NO_DIV :** Transparent mode, feed through selected clock source w/o dividing. **0x1: DIV_BY_2 :** Divide selected clock source by 2

9.1.13 CLK_SELECT (continued)

		0x2: DIV_BY_4 : Divide selected clock source by 4 **0x3: DIV_BY_8 :** Divide selected clock source by 8 **0x4: DIV_BY_16 :** Divide selected clock source by 16
11 : 8	PUMP_SEL	Selects clock PATH, where k=PUMP_SEL. The output of this mux goes to the PUMP_DIV to make PUMPCLK Each product has a specific number of available clock paths. Selecting a path that is not implemented on a product will result in undefined behavior. Note that this is not a glitch free mux. Default Value: 0
1 : 0	LFCLK_SEL	Select source for LFCLK. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. Writes to this field are ignored unless the WDT is unlocked using WDT_LOCK register. Default Value: 0 **0x0: ILO :** ILO - Internal Low-speed Oscillator **0x1: WCO :** WCO - Watch-Crystal Oscillator. Requires Backup domain to be present and properly configured (including external watch crystal, if used). **0x2: ALTLF :** ALTLF - Alternate Low-Frequency Clock. Capability is product-specific **0x3: PILO :** PILO - Precision ILO. If present, it works in DEEPSLEEP and higher modes. Does not work in HIBERNATE mode.

9.1.14 CLK_TIMER_CTL

Timer Clock Control Register

Address: 0x40260504

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TIMER_-SEL

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						TIMER_HF0_DIV [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	TIMER_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	Enable for TIMERCLK. 0: TIMERCLK is off 1: TIMERCLK is enabled Default Value: 0
23 : 16	TIMER_DIV	Divide selected timer clock source by (1+TIMER_DIV). The output of this divider is TIMERCLK Allows for integer divisions in the range [1, 256]. Do not change this setting while the timer is enabled. Default Value: 7
9 : 8	TIMER_HF0_DIV	Predivider used when HF0_DIV is selected in TIMER_SEL. If HFCLK0 frequency is less than 100MHz and has approximately 50% duty cycle, then no division is required (NO_DIV). Otherwise, select a divide ratio of 2, 4, or 8 before selected HF0_DIV as the timer clock. Default Value: 0 **0x0: NO_DIV :** Transparent mode, feed through selected clock source w/o dividing or correcting duty cycle.

9.1.14 CLK_TIMER_CTL (continued)

0x1: DIV_BY_2 :

Divide HFCLK0 by 2.

0x2: DIV_BY_4 :

Divide HFCLK0 by 4.

0x3: DIV_BY_8 :

Divide HFCLK0 by 8.

0	TIMER_SEL	Select source for TIMERCLK. The output of this mux can be further divided using TIMER_DIV. Default Value: 0 **0x0: IMO :** IMO - Internal Main Oscillator **0x1: HF0_DIV :** Select the output of the predivider configured by TIMER_HF0_DIV.

9.1.15 CLK_ILO_CONFIG

ILO Configuration

Address: 0x4026050C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							A
Name	None [7:1]							ILO_BACK-UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	A	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	Master enable for ILO. Writes to this field are ignored unless the WDT is unlocked using WDT_LOCK register. After enabling, it takes at most two cycles to reach the accuracy spec. Default Value: 1
0	ILO_BACKUP	If backup domain is present on this product, this register indicates that ILO should stay enabled for use by backup domain during XRES, HIBERNATE mode, and through power-related resets like BOD on VDDD/VCCD. Writes to this field are ignored unless the WDT is unlocked using WDT_LOCK register. 0: ILO turns off at XRES/BOD event or HIBERNATE entry. 1: ILO remains on if backup domain is present and powered even for XRES/BOD or HIBERNATE entry. Default Value: 0

9.1.16 CLK_IMO_CONFIG

IMO Configuration

Address: 0x40260510

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	Master enable for IMO oscillator. This bit must be high at all times for all functions to work properly. Hardware will automatically disable the IMO during HIBERNATE and XRES. It will automatically disable during DEEPSLEEP if CLK_MFO_CONFIG.DPSLP_ENABLE==0. Default Value: 1

9.1.17 CLK_OUTPUT_FAST

Fast Clock Output Select Register

Address: 0x40260514

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PATH_SEL0 [7:4]				FAST_SEL0 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				HFCLK_SEL0 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	PATH_SEL1 [23:20]				FAST_SEL1 [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				RW			
HW Access	None				R			
Name	None [31:28]				HFCLK_SEL1 [27:24]			

Bits	Name	Description
27 : 24	HFCLK_SEL1	Selects a HFCLK tree for use in fast clock output #1 logic Default Value: 0
23 : 20	PATH_SEL1	Selects a clock path to use in fast clock output #1 logic. 0: FLL output 1-15: PLL output on path1-path15 (if available) Default Value: 0
19 : 16	FAST_SEL1	Select signal for fast clock output #1 Default Value: 0 **0x0: NC :** Disabled - output is 0. For power savings, clocks are blocked before entering any muxes, including PATH_SEL1 and HFCLK_SEL1. **0x1: ECO :** External Crystal Oscillator (ECO)

9.1.17 CLK_OUTPUT_FAST (continued)

0x2: EXTCLK :

External clock input (EXTCLK)

0x3: ALTHF :

Alternate High-Frequency (ALTHF) clock input to SRSS

0x4: TIMERCLK :

Timer clock. It is grouped with the fast clocks because it may be a gated version of a fast clock, and therefore may have a short high pulse.

0x5: PATH_SEL1 :

Selects the clock path chosen by PATH_SEL1 field

0x6: HFCLK_SEL1 :

Selects the output of the HFCLK_SEL1 mux

0x7: SLOW_SEL1 :

Selects the output of CLK_OUTPUT_SLOW.SLOW_SEL1

11 : 8	HFCLK_SEL0	Selects a HFCLK tree for use in fast clock output #0 Default Value: 0
7 : 4	PATH_SEL0	Selects a clock path to use in fast clock output #0 logic. 0: FLL output 1-15: PLL output on path1-path15 (if available) Default Value: 0
3 : 0	FAST_SEL0	Select signal for fast clock output #0 Default Value: 0

0x0: NC :

Disabled - output is 0. For power savings, clocks are blocked before entering any muxes, including PATH_SEL0 and HFCLK_SEL0.

0x1: ECO :

External Crystal Oscillator (ECO)

0x2: EXTCLK :

External clock input (EXTCLK)

0x3: ALTHF :

Alternate High-Frequency (ALTHF) clock input to SRSS

9.1.17 CLK_OUTPUT_FAST (continued)

0x4: TIMERCLK :

Timer clock. It is grouped with the fast clocks because it may be a gated version of a fast clock, and therefore may have a short high pulse.

0x5: PATH_SEL0 :

Selects the clock path chosen by PATH_SEL0 field

0x6: HFCLK_SEL0 :

Selects the output of the HFCLK_SEL0 mux

0x7: SLOW_SEL0 :

Selects the output of CLK_OUTPUT_SLOW.SLOW_SEL0

9.1.18 CLK_OUTPUT_SLOW

Slow Clock Output Select Register

Address: 0x40260518

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	SLOW_SEL1 [7:4]				SLOW_SEL0 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	SLOW_SEL1	Select signal for slow clock output #1 Default Value: 0 **0x0: NC :** Disabled - output is 0. For power savings, clocks are blocked before entering any muxes. **0x1: ILO :** Internal Low Speed Oscillator (ILO) **0x2: WCO :** Watch-Crystal Oscillator (WCO) **0x3: BAK :** Root of the Backup domain clock tree (BAK)

9.1.18 CLK_OUTPUT_SLOW (continued)

		0x4: ALTLF : Alternate low-frequency clock input to SRSS (ALTLF) **0x5: LFCLK :** Root of the low-speed clock tree (LFCLK) **0x6: IMO :** Internal Main Oscillator (IMO). This is grouped with the slow clocks so it can be observed during DEEPSLEEP entry/exit. **0x7: SLPCTRL :** Sleep Controller clock (SLPCTRL). This is grouped with the slow clocks so it can be observed during DEEPSLEEP entry/exit. **0x8: PILO :** Precision Internal Low Speed Oscillator (PILO)
3 : 0	SLOW_SEL0	Select signal for slow clock output #0 Default Value: 0 **0x0: NC :** Disabled - output is 0. For power savings, clocks are blocked before entering any muxes. **0x1: ILO :** Internal Low Speed Oscillator (ILO) **0x2: WCO :** Watch-Crystal Oscillator (WCO) **0x3: BAK :** Root of the Backup domain clock tree (BAK) **0x4: ALTLF :** Alternate low-frequency clock input to SRSS (ALTLF) **0x5: LFCLK :** Root of the low-speed clock tree (LFCLK)

9.1.18 CLK_OUTPUT_SLOW (continued)

0x6: IMO :

Internal Main Oscillator (IMO). This is grouped with the slow clocks so it can be observed during DEEPSLEEP entry/exit.

0x7: SLPCTRL :

Sleep Controller clock (SLPCTRL). This is grouped with the slow clocks so it can be observed during DEEPSLEEP entry/exit.

0x8: PILO :

Precision Internal Low Speed Oscillator (PILO)

9.1.19 CLK_CAL_CNT1

Clock Calibration Counter 1

Address: 0x4026051C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	CAL_COUNTER1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	CAL_COUNTER1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	CAL_COUNTER1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CAL_COUNTER_DONE	None [30:24]						

Bits	Name	Description
31	CAL_COUNTER_DONE	Status bit indicating that the internal counter #1 is finished counting and CLK_-CAL_CNT2.COUNTER stopped counting up Default Value: 1
23 : 0	CAL_COUNTER1	Down-counter clocked on fast clock output #0 (see CLK_OUTPUT_FAST). This register always reads as zero. Counting starts internally when this register is written with a nonzero value. CAL_COUNTER_DONE goes immediately low to indicate that the counter has started and will be asserted when the counters are done. Do not write this field unless CAL_COUNTER_-DONE==1. Both clocks must be running or the measurement will not complete. A stalled counter can be recovered by selecting valid clocks, waiting until the measurement completes, and discarding the first result. Default Value: 0

9.1.20 CLK_CAL_CNT2

Clock Calibration Counter 2

Address: 0x40260520

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CAL_COUNTER2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CAL_COUNTER2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	CAL_COUNTER2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	CAL_COUNTER2	Up-counter clocked on fast clock output #1 (see CLK_OUTPUT_FAST). When CLK_-CAL_CNT1.CAL_COUNTER_DONE==1, the counter is stopped and can be read by SW. Do not read this value unless CAL_COUNTER_DONE==1. The expected final value is related to the ratio of clock frequencies used for the two counters and the value loaded into counter 1: CLK_-CAL_CNT2.COUNTER=(F_cnt2/F_cnt1)*(CLK_CAL_CNT1.COUNTER) Default Value: 0

9.1.21 CLK_ECO_CONFIG

ECO Configuration Register

Address: 0x4026052C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	None
HW Access	None						R	None
Name	None [7:2]						AGC_EN	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ECO_EN	None [30:24]						

Bits	Name	Description
31	ECO_EN	Master enable for ECO oscillator. Default Value: 0
1	AGC_EN	Automatic Gain Control (AGC) enable. When set, the oscillation amplitude is controlled to the level selected by ECO_TRIM0.ATRIM. When low, the amplitude is not explicitly controlled and can be as high as the vddd supply. WARNING: use care when disabling AGC because driving a crystal beyond its rated limit can permanently damage the crystal. Default Value: 1

9.1.22 CLK_ECO_STATUS

ECO Status Register

Address: 0x40260530

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						ECO_READY	ECO_OK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	ECO_READY	Indicates the ECO internal oscillator circuit has had enough time to fully stabilize. This is the output of a counter since ECO was enabled, and it does not check the ECO output. It is recommended to also confirm ECO_OK==1. Default Value: 0
0	ECO_OK	Indicates the ECO internal oscillator circuit has sufficient amplitude. It may not meet the PPM accuracy or duty cycle spec. Default Value: 0

9.1.23 CLK_MF_SELECT

Medium Frequency Clock Select Register

Address: 0x40260544

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					MFCLK_SEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MFCLK_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	Enable for MFCLK (clk_mf). Default Value: 0
15 : 8	MFCLK_DIV	Divide selected clock source by (1+MFCLK_DIV). The output of this divider is MFCLK (clk_mf). Allows for integer divisions in the range [1, 256]. Do not change this setting while ENABLE==1. Default Value: 0
2 : 0	MFCLK_SEL	Select source for MFCLK (clk_mf). Note that not all products support all clock sources. Selecting a clock source that is not supported results in undefined behavior. Default Value: 0 **0x0: MFO :** MFO - medium frequency oscillator

9.1.24 CLK_MFO_CONFIG

MFO Configuration Register

Address: 0x40260548

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	ENABLE	DPS-LP_EN-ABLE	None [29:24]					

Bits	Name	Description
31	ENABLE	Enable for MFO. Default Value: 1
30	DPSLP_ENABLE	Enable for MFO during DEEPSLEEP. This bit is ignored when ENABLE==0. When ENABLE==1: 0: MFO is automatically disabled during DEEPSLEEP and enables upon wakeup; 1: MFO is kept enabled throughout DEEPSLEEP Default Value: 0

9.1.25 CLK_FLL_CONFIG

FLL Configuration Register

Address: 0x40260580

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FLL_MULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	FLL_MULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						FLL_MULT [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						RW
HW Access	R	None						R
Name	FLL_ENABLE	None [30:25]						FLL_OUTPUT_DIV

Bits	Name	Description
31	FLL_ENABLE	Master enable for FLL. The FLL requires firmware sequencing when enabling, disabling, and entering/exiting DEEPSLEEP. To enable the FLL, first enable the CCO by writing CLK_FLL_CONFIG4.CCO_ENABLE=1 and wait until CLK_FLL_STATUS.CCO_READY==1. Next, ensure the reference clock has stabilized and CLK_FLL_CONFIG3.BYPASS_SEL=FLL_REF. Next, write FLL_ENABLE=1 and wait until CLK_FLL_STATUS.LOCKED==1. Finally, write CLK_FLL_CONFIG3.BYPASS_SEL=FLL_OUT to switch to the FLL output. It takes seven reference clock cycles plus four FLL output cycles to switch to the FLL output. Do not disable the FLL before this time completes. To disable the FLL, write CLK_FLL_CONFIG3.BYPASS_SEL=FLL_REF and (optionally) read the same register to ensure the write completes. Then, wait at least seven FLL reference clock cycles before disabling it with FLL_ENABLE=0. Lastly, disable the CCO by writing CLK_FLL_CONFIG4.CCO_ENABLE=0. Before entering DEEPSLEEP, either disable the FLL using above sequence or use the following procedure to deselect/select it before/after DEEPSLEEP. Before entering DEEPSLEEP, write CLK_FLL_CONFIG3.BYPASS_SEL=FLL_REF to change the FLL to use its reference clock. After DEEPSLEEP wakeup, wait until CLK_FLL_STATUS.LOCKED==1 and then write CLK_FLL_CONFIG3.BYPASS_SEL=FLL_OUT to switch to the FLL output. 0: Block is powered off 1: Block is powered on Default Value: 0

9.1.25 CLK_FLL_CONFIG (continued)

24	FLL_OUTPUT_DIV	Control bits for Output divider. Set the divide value before enabling the FLL, and do not change it while FLL is enabled. 0: no division 1: divide by 2 Default Value: 1
17 : 0	FLL_MULT	Multiplier to determine CCO frequency in multiples of the frequency of the selected reference clock (Fref). Ffll = (FLL_MULT) * (Fref / REFERENCE_DIV) / (OUTPUT_DIV+1) Default Value: 0

9.1.26 CLK_FLL_CONFIG2

FLL Configuration Register 2

Address: 0x40260584

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FLL_REF_DIV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			FLL_REF_DIV [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	LOCK_TOL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							LOCK_TOL

Bits	Name	Description
24 : 16	LOCK_TOL	Lock tolerance sets the error threshold for when the FLL output is considered locked to the reference input. A high tolerance can be used to lock more quickly or to track a less accurate source. The tolerance should be set so that the FLL does not unlock under normal conditions. The tolerance is the allowed difference between the count value for the ideal formula and the measured value. 0: tolerate error of 1 count value 1: tolerate error of 2 count values ... 511: tolerate error of 512 count values Default Value: 2
12 : 0	FLL_REF_DIV	Control bits for reference divider. Set the divide value before enabling the FLL, and do not change it while FLL is enabled. 0: illegal (undefined behavior) 1: divide by 1 ... 8191: divide by 8191 Default Value: 1

9.1.27 CLK_FLL_CONFIG3

FLL Configuration Register 3

Address: 0x40260588

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	FLL_LF_PGAIN [7:4]				FLL_LF_IGAIN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SETTLING_COUNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			R				
Name	None [23:21]			SETTLING_COUNT [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW		None			
HW Access	None		R		None			
Name	None [31:30]		BYPASS_SEL [29:28]		None [27:24]			

Bits	Name	Description
29 : 28	BYPASS_SEL	Bypass mux located just after FLL output. See FLL_ENABLE description for instructions on how to use this field when enabling/disabling the FLL. Default Value: 0 **0x0: AUTO :** Reserved **0x1: AUTO1 :** Reserved **0x2: FLL_REF :** Select FLL reference input (bypass mode). Ignores lock indicator

9.1.27 CLK_FLL_CONFIG3 (continued)

		0x3: FLL_OUT : Select FLL output. Ignores lock indicator.
20 : 8	SETTLING_COUNT	Number of undivided reference clock cycles to wait after changing the CCO trim until the loop measurement restarts. A delay allows the CCO output to settle and gives a more accurate measurement. The default is tuned to an 8MHz reference clock since the IMO is expected to be the most common use case. 0: no settling time 1: wait one reference clock cycle ... 8191: wait 8191 reference clock cycles Default Value: 40
7 : 4	FLL_LF_PGAIN	FLL Loop Filter Gain Setting #2. The proportional gain is the sum of FLL_LF_IGAIN and FLL_LF_PGAIN. 0: 1/256 1: 1/128 2: 1/64 3: 1/32 4: 1/16 5: 1/8 6: 1/4 7: 1/2 8: 1.0 9: 2.0 10: 4.0 11: 8.0 >=12: illegal Default Value: 0
3 : 0	FLL_LF_IGAIN	FLL Loop Filter Gain Setting #1. The proportional gain is the sum of FLL_LF_IGAIN and FLL_LF_PGAIN. 0: 1/256 1: 1/128 2: 1/64 3: 1/32 4: 1/16 5: 1/8 6: 1/4 7: 1/2 8: 1.0 9: 2.0 10: 4.0 11: 8.0 >=12: illegal Default Value: 0

9.1.28 CLK_FLL_CONFIG4

FLL Configuration Register 4

Address: 0x4026058C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CCO_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					R		
Name	None [15:11]					CCO_RANGE [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	CCO_FREQ [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					RW
HW Access	R	R	None					RW
Name	CCO_EN-ABLE	CCO_HW_UP-DATE_DIS	None [29:25]					CCO_-FREQ

Bits	Name	Description
31	CCO_ENABLE	Enable the CCO. It is required to enable the CCO before using the FLL. 0: Block is powered off 1: Block is powered on Default Value: 0
30	CCO_HW_UPDATE_DIS	Disable CCO frequency update by FLL hardware 0: Hardware update of CCO settings is allowed. Use this setting for normal FLL operation. 1: Hardware update of CCO settings is disabled. Use this setting for open-loop FLL operation. Default Value: 0
24 : 16	CCO_FREQ	CCO frequency code. This is updated by HW when the FLL is enabled. It can be manually updated to use the CCO in an open loop configuration. The meaning of each frequency code depends on the range. Default Value: 0
10 : 8	CCO_RANGE	Frequency range of CCO Default Value: 0

9.1.28 CLK_FLL_CONFIG4 (continued)

		0x0: RANGE0 : Target frequency is in range [48, 64) MHz **0x1: RANGE1 :** Target frequency is in range [64, 85) MHz **0x2: RANGE2 :** Target frequency is in range [85, 113) MHz **0x3: RANGE3 :** Target frequency is in range [113, 150) MHz **0x4: RANGE4 :** Target frequency is in range [150, 200] MHz
7 : 0	CCO_LIMIT	Maximum CCO offset allowed (used to prevent FLL dynamics from selecting an CCO frequency that the logic cannot support) Default Value: 0xFF

9.1.29 CLK_FLL_STATUS

FLL Status Register

Address: 0x40260590

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	RW1C	R
HW Access	None					RW	A	W
Name	None [7:3]					CCO_READY	UNLOCK_OCCURRED	LOCKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CCO_READY	This indicates that the CCO is internally settled and ready to use. Default Value: 0
1	UNLOCK_OCCURRED	Reserved. Do not use. Default Value: 0
0	LOCKED	FLL Lock Indicator. LOCKED is high when FLL is within CLK_FLL_CONFIG2.LOCK_TOL. If FLL is outside LOCK_TOL, LOCKED goes low. Note that this can happen during normal operation, if FLL needs to recalculate due to a change in the reference clock, change in voltage, or change in temperature. Default Value: 0

9.1.30 CLK_PLL_CONFIG0

PLL Configuration Register

Address: 0x40260600

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	FEEDBACK_DIV [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			REFERENCE_DIV [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			R				
Name	None [23:21]			OUTPUT_DIV [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None	RW		RW	None		
HW Access	R	None	R		R	None		
Name	ENABLE	None	BYPASS_SEL [29:28]		PLL_LF_-MODE	None [26:24]		

Bits	Name	Description
31	ENABLE	Master enable for PLL. Setup FEEDBACK_DIV, REFERENCE_DIV, and OUTPUT_DIV at least one cycle before setting ENABLE=1. To disable the PLL, first deselect it using .BYPASS_-SEL=PLL_REF, wait at least six PLL clock cycles, and then disable it with .ENABLE=0. Fpll = (FEEDBACK_DIV) * (Fref / REFERENCE_DIV) / (OUTPUT_DIV) 0: Block is disabled 1: Block is enabled Default Value: 0
29 : 28	BYPASS_SEL	Bypass mux located just after PLL output. This selection is glitch-free and can be changed while the PLL is running. Default Value: 0 **0x0: AUTO :** Automatic using lock indicator. When unlocked, automatically selects PLL reference input (by-pass mode). When locked, automatically selects PLL output.

9.1.30 CLK_PLL_CONFIG0 (continued)

		0x1: AUTO1 : Same as AUTO **0x2: PLL_REF :** Select PLL reference input (bypass mode). Ignores lock indicator **0x3: PLL_OUT :** Select PLL output. Ignores lock indicator.
27	PLL_LF_MODE	VCO frequency range selection. Configure this bit according to the targeted VCO frequency. Do not change this setting while the PLL is enabled. 0: VCO frequency is [200MHz, 400MHz] 1: VCO frequency is [170MHz, 200MHz) Default Value: 0
20 : 16	OUTPUT_DIV	Control bits for Output divider. Set the divide value before enabling the PLL, and do not change it while PLL is enabled. 0: illegal (undefined behavior) 1: illegal (undefined behavior) 2: divide by 2. Suitable for direct usage as HFCLK source. ... 16: divide by 16. Suitable for direct usage as HFCLK source. >16: illegal (undefined behavior) Default Value: 2
12 : 8	REFERENCE_DIV	Control bits for reference divider. Set the divide value before enabling the PLL, and do not change it while PLL is enabled. 0: illegal (undefined behavior) 1: divide by 1 ... 20: divide by 20 others: illegal (undefined behavior) Default Value: 1
6 : 0	FEEDBACK_DIV	Control bits for feedback divider. Set the divide value before enabling the PLL, and do not change it while PLL is enabled. 0-21: illegal (undefined behavior) 22: divide by 22 ... 112: divide by 112 >112: illegal (undefined behavior) Default Value: 22

9.1.31 CLK_PLL_STATUS0

PLL Status Register

Address: 0x40260640

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	R
HW Access	None						A	W
Name	None [7:2]						UN-LOCK_OC-CURRED	LOCKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	UNLOCK_OCCURRED	This bit sets whenever the PLL Lock bit goes low, and stays set until cleared by firmware. Default Value: 0
0	LOCKED	PLL Lock Indicator Default Value: 0

9.1.32 SRSS_INTR

SRSS Interrupt Register

Address: 0x40260700

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1C	None			RW1C	RW1C
HW Access	None		A	None			A	A
Name	None [7:6]		CLK_CAL	None [4:2]			HVLVD1	WDT_-MATCH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	CLK_CAL	Clock calibration counter is done. This field is reset during DEEPSLEEP mode. Default Value: 0
1	HVLVD1	Interrupt for low voltage detector HVLVD1 Default Value: 0
0	WDT_MATCH	WDT Interrupt Request. This bit is set each time WDT_COUNTR==WDT_MATCH. W1C also feeds the watch dog. Missing 2 interrupts in a row will generate a reset. Due to internal synchronization, it takes 2 SYSCLK cycles to update after a W1C. Default Value: 0

9.1.33 SRSS_INTR_SET

SRSS Interrupt Set Register

Address: 0x40260704

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1S	None			RW1S	RW1S
HW Access	None		A	None			A	A
Name	None [7:6]		CLK_CAL	None [4:2]			HVLVD1	WDT_-MATCH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	CLK_CAL	Set interrupt for clock calibration counter done. This field is reset during DEEPSLEEP mode. Default Value: 0
1	HVLVD1	Set interrupt for low voltage detector HVLVD1 Default Value: 0
0	WDT_MATCH	Set interrupt for low voltage detector WDT_MATCH Default Value: 0

9.1.34 SRSS_INTR_MASK

SRSS Interrupt Mask Register

Address: 0x40260708

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	None			RW	RW
HW Access	None		R	None			R	R
Name	None [7:6]		CLK_CAL	None [4:2]			HVLVD1	WDT_-MATCH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	CLK_CAL	Mask for clock calibration done Default Value: 0
1	HVLVD1	Mask for low voltage detector HVLVD1 Default Value: 0
0	WDT_MATCH	Mask for watchdog timer. Clearing this bit will not forward the interrupt to the CPU. It will not, however, disable the WDT reset generation on 2 missed interrupts. When WDT resets the chip, it also internally pends an interrupt that survives the reset. To prevent unintended ISR execution, clear SRSS_INTR.WDT_MATCH before setting this bit. Default Value: 0

9.1.35 SRSS_INTR_MASKED

SRSS Interrupt Masked Register

Address: 0x4026070C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	None			R	R
HW Access	None		RW	None			RW	RW
Name	None [7:6]		CLK_CAL	None [4:2]			HVLVD1	WDT_-MATCH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	CLK_CAL	Logical and of corresponding request and mask bits. Default Value: 0
1	HVLVD1	Logical and of corresponding request and mask bits. Default Value: 0
0	WDT_MATCH	Logical and of corresponding request and mask bits. Default Value: 0

9.1.36 SRSS_INTR_CFG

SRSS Interrupt Configuration Register

Address: 0x40260710

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						HVLVD1_EDGE_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	HVLVD1_EDGE_SEL	Sets which edge(s) will trigger an IRQ for HVLVD1 Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges

9.1.37 RES_CAUSE

Reset Cause Observation Register

Address: 0x40260800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	RE-SET_MCWDT2	RE-SET_MCWDT1	RE-SET_MCWDT0	RESET_-SOFT	RE-SET_CSV_WCO_LOSS	RESET_D-PSLP_-FAULT	RE-SET_ACT_-FAULT	RE-SET_WDT

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							RE-SET_MCWDT3

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	RESET_MCWDT3	Multi-Counter Watchdog timer reset #3 has occurred since last power cycle. This hardware is not present in PSoC6 devices. Default Value: 0
7	RESET_MCWDT2	Multi-Counter Watchdog timer reset #2 has occurred since last power cycle. This hardware is not present in PSoC6 devices. Default Value: 0
6	RESET_MCWDT1	Multi-Counter Watchdog timer reset #1 has occurred since last power cycle. Default Value: 0
5	RESET_MCWDT0	Multi-Counter Watchdog timer reset #0 has occurred since last power cycle. Default Value: 0
4	RESET_SOFT	A CPU requested a system reset through it's SYSRESETREQ. This can be done via a debugger probe or in firmware. Default Value: 0

9.1.37 RES_CAUSE (continued)

3	RESET_CSV_W-CO_LOSS	Clock supervision logic requested a reset due to loss of a watch-crystal clock. Default Value: 0
2	RESET_DPSLP_FAULT	Fault logging system requested a reset from its DeepSleep logic. Default Value: 0
1	RESET_ACT_FAULT	Fault logging system requested a reset from its Active logic. Default Value: 0
0	RESET_WDT	A basic WatchDog Timer (WDT) reset has occurred since last power cycle. Default Value: 0

9.1.38 RES_CAUSE2

Reset Cause Observation Register 2

Address: 0x40260804

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	A							
Name	RESET_CSV_HF_LOSS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	A							
Name	RESET_CSV_HF_LOSS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	A							
Name	RESET_CSV_HF_FREQ [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	A							
Name	RESET_CSV_HF_FREQ [31:24]							

Bits	Name	Description
31 : 16	RESET_CSV_HF_FREQ	Clock supervision logic requested a reset due to frequency error of high-frequency clock. Each bit index K corresponds to a HFCLK. Unimplemented clock bits return zero. Default Value: 0
15 : 0	RESET_CSV_HF_LOSS	Clock supervision logic requested a reset due to loss of a high-frequency clock. Each bit index K corresponds to a HFCLK. Unimplemented clock bits return zero. Default Value: 0

9.1.39 PWR_TRIM_REF_CTL

Reference Trim Register

Address: 0x40267F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	A				A			
Name	ACT_REF_ITRIM [7:4]				ACT_REF_TCTRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW	None	RW				
HW Access	None	A	None	A				
Name	None	ACT_REF_IBOOST	None	ACT_REF_ABSTRIM [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	A				A			
Name	DPSLP_REF_ABSTRIM [23:20]				DPSLP_REF_TCTRIM [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				None			RW
HW Access	A				None			A
Name	DPSLP_REF_ITRIM [31:28]				None [27:25]			DPS-LP_REF_ABSTRIM

Bits	Name	Description
31 : 28	DPSLP_REF_ITRIM	DeepSleep current reference trim. This register is only reset by XRES/POR/BOD/HIBERNATE. Default Value: 7
24 : 20	DPSLP_REF_ABSTRIM	DeepSleep-Reference absolute voltage trim. This register is only reset by XRES/POR/BOD/HIBERNATE. Default Value: 15
19 : 16	DPSLP_REF_TCTRIM	DeepSleep-Reference temperature trim. This register is only reset by XRES/POR/BOD/HIBERNATE. 0 -> default setting at POR; not for trimming use others -> normal trim range Default Value: 0
14	ACT_REF_IBOOST	Active-Reference current boost. This register is only reset by XRES/POR/BOD/HIBERNATE. 0: normal operation others: risk mitigation Default Value: 0

9.1.39 PWR_TRIM_REF_CTL (continued)

12 : 8	ACT_REF_ABSTRIM	Active-Reference absolute voltage trim. This register is only reset by XRES/POR/BOD/HIBERNATE. 0 -> default setting at POR; not for trimming use others -> normal trim range Default Value: 0
7 : 4	ACT_REF_ITRIM	Active-Reference current trim. This register is only reset by XRES/POR/BOD/HIBERNATE. 0 -> default setting at POR; not for trimming use others -> normal trim range Default Value: 0
3 : 0	ACT_REF_TCTRIM	Active-Reference temperature trim. This register is only reset by XRES/POR/BOD/HIBERNATE. 0 -> default setting at POR; not for trimming use others -> normal trim range Default Value: 0

9.1.40 PWR_TRIM_BODOVP_CTL

BOD/OVP Trim Register

Address: 0x40267F04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			None	RW		
HW Access	A	A			None	A		
Name	HVPOR-BOD_ITRIM	HVPORBOD_OFSTRIM [6:4]			None	HVPORBOD_TRIPSEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None	RW			RW	
HW Access	A		None	A			A	
Name	LVPORBOD_OFSTRIM [15:14]		None	LVPORBOD_TRIPSEL [12:10]			HVPORBOD_ITRIM [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			RW
HW Access	None				A			A
Name	None [23:20]				LVPORBOD_ITRIM [19:17]			LVPOR-BOD_OF-STRIM

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 17	LVPORBOD_ITRIM	LVPORBOD current trim. This register is only reset by XRES/POR/BOD/HIBERNATE. Default Value: 2
16 : 14	LVPORBOD_OFSTRIM	LVPORBOD offset trim. This register is only reset by XRES/POR/BOD/HIBERNATE. Default Value: 0
12 : 10	LVPORBOD_TRIPSEL	LVPORBOD trip point selection. Monitors vccd. This register is only reset by XRES/POR/BOD/HIBERNATE. Default Value: 3
9 : 7	HVPORBOD_ITRIM	HVPORBOD current trim. This register is only reset by XRES/POR/BOD/HIBERNATE. Default Value: 2
6 : 4	HVPORBOD_OFSTRIM	HVPORBOD offset trim. This register is only reset by XRES/POR/BOD/HIBERNATE. Default Value: 0
2 : 0	HVPORBOD_TRIPSEL	HVPORBOD trip point selection. Monitors vddd. This register is only reset by XRES/POR/BOD/HIBERNATE. Default Value: 4

9.1.41 CLK_TRIM_CCO_CTL

CCO Trim Register

Address: 0x40267F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		CCO_RCSTRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None	RW					
HW Access	R	None	R					
Name	EN-ABLE_CNT	None	CCO_STABLE_CNT [29:24]					

Bits	Name	Description
31	ENABLE_CNT	Enables the automatic stabilization counter. Default Value: 1
29 : 24	CCO_STABLE_CNT	Terminal count for the stabilization counter from CCO_ENABLE until stable. Default Value: 0x27
5 : 0	CCO_RCSTRIM	CCO reference current source trim. Default Value: 0x20

9.1.42 CLK_TRIM_CCO_CTL2

CCO Trim Register 2

Address: 0x40267F0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				
HW Access	R			R				
Name	CCO_FCTRIM2 [7:5]			CCO_FCTRIM1 [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW					RW	
HW Access	R	R					R	
Name	CCO_FC-TRIM4	CCO_FCTRIM3 [14:10]					CCO_FCTRIM2 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	CCO_FCTRIM5 [23:20]				CCO_FCTRIM4 [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							CCO_FC-TRIM5

Bits	Name	Description
24 : 20	CCO_FCTRIM5	CCO frequency 5th range calibration Default Value: 0x08
19 : 15	CCO_FCTRIM4	CCO frequency 4th range calibration Default Value: 0x10
14 : 10	CCO_FCTRIM3	CCO frequency 3rd range calibration Default Value: 0x10
9 : 5	CCO_FCTRIM2	CCO frequency 2nd range calibration Default Value: 0x08
4 : 0	CCO_FCTRIM1	CCO frequency 1st range calibration Default Value: 0x10

9.1.43 PWR_TRIM_WAKE_CTL

Wakeup Trim Register

Address: 0x40267F30

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WAKE_DELAY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	WAKE_DELAY	Wakeup holdoff. Spec (fastest) wake time is achieved with a setting of 0. Additional delay can be added for debugging or workaround. The delay is counted by the IMO. Default Value: 0

9.1.44 PWR_TRIM_LVD_CTL

LVD Trim Register

Address: 0x4026FF10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	HVLVD1_ITRIM [6:4]			None	HVLVD1_OFSTRIM [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 4	HVLVD1_ITRIM	HVLVD1 current trim Default Value: 2
2 : 0	HVLVD1_OFSTRIM	HVLVD1 offset trim Default Value: 0

9.1.45 CLK_TRIM_ILO_CTL

ILO Trim Register

Address: 0x4026FF18

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		A					
Name	None [7:6]		ILO_FTRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	ILO_FTRIM	ILO frequency trims. LSB step size is 1.5% (typical) of the frequency. Default Value: 0x2C

9.1.46 PWR_TRIM_PWRSYS_CTL

Power System Trim Register

Address: 0x4026FF1C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			A				
Name	None [7:5]			ACT_REG_TRIM [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	A		None					
Name	ACT_REG_BOOST [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	ACT_REG_BOOST	Controls the tradeoff between output current and internal operating current for the Active Regulator. The maximum output current depends on the silicon implementation, but an application may limit its maximum current to less than that. This may allow a reduction in the internal operating current of the regulator. The regulator internal operating current depends on the boost setting: 2'b00: 50uA 2'b01: 100uA 2'b10: 150uA 2'b11: 200uA The allowed setting is a lookup table based on the chip-specific maximum (set in factory) and an application-specific maximum (set by customer). The defaults are set assuming the application consumes the maximum allowed by the chip. 50mA chip: 2'b00 (default); 100mA chip: 2'b00 (default); 150mA chip: 50..100mA app => 2'b00, 150mA app => 2'b01 (default); 200mA chip: 50mA app => 2'b00, 100..150mA app => 2'b01, 200mA app => 2'b10 (default); 250mA chip: 50mA app => 2'b00, 100..150mA app => 2'b01, 200..250mA app => 2'b10 (default); 300mA chip: 50mA app => 2'b00, 100..150mA app => 2'b01, 200..250mA app => 2'b10, 300mA app => 2'b11 (default); This register is only reset by XRES/POR/BOD/HIBERNATE. Default Value: X

9.1.46 PWR_TRIM_PWRSYS_CTL (continued)

4 : 0	ACT_REG_TRIM	Trim for the Active-Regulator. This sets the output voltage level. This register is only reset by XRES/POR/BOD/HIBERNATE. The nominal output voltage is vccd=812.5mV + ACT_REG_TRIM*12.5mV. The actual output voltage will vary depending on conditions and load. The following settings are explicitly shown for convenience, and other values may be calculated using the formula: 5'h07: 900mV (nominal) 5'h17: 1100mV (nominal) Default Value: 0x17

9.1.47 CLK_TRIM_ECO_CTL

ECO Trim Register

Address: 0x4026FF20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				None	RW		
HW Access	R				None	R		
Name	ATRIM [7:4]				None	WDTRIM [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [15:14]		GTRIM [13:12]		RTRIM [11:10]		FTRIM [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW					
HW Access	None		R					
Name	None [23:22]		ITRIM [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21 : 16	ITRIM	Current Trim Default Value: 31
13 : 12	GTRIM	Gain Trim - Startup time Default Value: 0
11 : 10	RTRIM	Feedback resistor Trim Default Value: 0
9 : 8	FTRIM	Filter Trim - 3rd harmonic oscillation Default Value: 0

9.1.47 CLK_TRIM_ECO_CTL (continued)

7 : 4	ATRIM	Amplitude trim to set the crystal drive level when ECO_CONFIG.AGC_EN=1. WARNING: use care when setting this field because driving a crystal beyond its rated limit can permanently damage the crystal. 0x0 - 150mV 0x1 - 175mV 0x2 - 200mV 0x3 - 225mV 0x4 - 250mV 0x5 - 275mV 0x6 - 300mV 0x7 - 325mV 0x8 - 350mV 0x9 - 375mV 0xA - 400mV 0xB - 425mV 0xC - 450mV 0xD - 475mV 0xE - 500mV 0xF - 525mV Default Value: 0
2 : 0	WDTRIM	Watch Dog Trim - Delta voltage below steady state level 0x0 - 50mV 0x1 - 75mV 0x2 - 100mV 0x3 - 125mV 0x4 - 150mV 0x5 - 175mV 0x6 - 200mV 0x7 - 225mV Default Value: 3

10 Multi-Counter WDT Registers

This section discusses the Multi-Counter WDT (MCWDT) registers. It lists all the registers in mapping tables, in address order.

10.1 Register Details

Register	Address	Description
MCWDT_CNTLOW0	0x40260204	Multi-Counter Watchdog Sub-counters 0/1
MCWDT_CNTHIGH0	0x40260208	Multi-Counter Watchdog Sub-counter 2
MCWDT_MATCH0	0x4026020C	Multi-Counter Watchdog Counter Match Register
MCWDT_CONFIG0	0x40260210	Multi-Counter Watchdog Counter Configuration
MCWDT_CTL0	0x40260214	Multi-Counter Watchdog Counter Control
MCWDT_INTR0	0x40260218	Multi-Counter Watchdog Counter Interrupt Register
MCWDT_INTR_SET0	0x4026021C	Multi-Counter Watchdog Counter Interrupt Set Register
MCWDT_INTR_MASK0	0x40260220	Multi-Counter Watchdog Counter Interrupt Mask Register
MCWDT_INTR_MASKED0	0x40260224	Multi-Counter Watchdog Counter Interrupt Masked Register
MCWDT_LOCK0	0x40260228	Multi-Counter Watchdog Counter Lock Register
MCWDT_CNTLOW1	0x40260244	Multi-Counter Watchdog Sub-counters 0/1. See MCWDT_CNTLOW0 for the details of bit fields.
MCWDT_CNTHIGH1	0x40260248	Multi-Counter Watchdog Sub-counter 2. See MCWDT_CNTHIGH0 for the details of bit fields.
MCWDT_MATCH1	0x4026024C	Multi-Counter Watchdog Counter Match Register. See MCWDT_MATCH0 for the details of bit fields.
MCWDT_CONFIG1	0x40260250	Multi-Counter Watchdog Counter Configuration. See MCWDT_CONFIG0 for the details of bit fields.
MCWDT_CTL1	0x40260254	Multi-Counter Watchdog Counter Control. See MCWDT_CTL0 for the details of bit fields.
MCWDT_INTR1	0x40260258	Multi-Counter Watchdog Counter Interrupt Register. See MCWDT_INTR0 for the details of bit fields.
MCWDT_INTR_SET1	0x4026025C	Multi-Counter Watchdog Counter Interrupt Set Register. See MCWDT_INTR_SET0 for the details of bit fields.
MCWDT_INTR_MASK1	0x40260260	Multi-Counter Watchdog Counter Interrupt Mask Register. See MCWDT_INTR_MASK0 for the details of bit fields.
MCWDT_INTR_MASKED1	0x40260264	Multi-Counter Watchdog Counter Interrupt Masked Register. See MCWDT_INTR_MASKED0 for the details of bit fields.
MCWDT_LOCK1	0x40260268	Multi-Counter Watchdog Counter Lock Register. See MCWDT_LOCK0 for the details of bit fields.

10.1.1 MCWDT_CNTLOW0

Multi-Counter Watchdog Sub-counters 0/1

Address: 0x40260204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	WDT_CTR0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	WDT_CTR0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	WDT_CTR1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	WDT_CTR1 [31:24]							

Bits	Name	Description
31 : 16	WDT_CTR1	Current value of sub-counter 1 for this MCWDT. Software writes are ignored when the sub-counter is enabled Default Value: 0
15 : 0	WDT_CTR0	Current value of sub-counter 0 for this MCWDT. Software writes are ignored when the sub-counter is enabled. Default Value: 0

10.1.2 MCWDT_CNTHIGH0

Multi-Counter Watchdog Sub-counter 2

Address: 0x40260208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	WDT_CTR2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	WDT_CTR2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	WDT_CTR2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	WDT_CTR2 [31:24]							

Bits	Name	Description
31 : 0	WDT_CTR2	Current value of sub-counter 2 for this MCWDT. Software writes are ignored when the sub-counter is enabled Default Value: 0

10.1.3 MCWDT_MATCH0

Multi-Counter Watchdog Counter Match Register

Address: 0x4026020C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WDT_MATCH0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	WDT_MATCH0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	WDT_MATCH1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	WDT_MATCH1 [31:24]							

Bits	Name	Description
31 : 16	WDT_MATCH1	Match value for sub-counter 1 of this MCWDT Default Value: 0
15 : 0	WDT_MATCH0	Match value for sub-counter 0 of this MCWDT Default Value: 0

10.1.4 MCWDT_CONFIG0

Multi-Counter Watchdog Counter Configuration

Address: 0x40260210

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	
HW Access	None				R	R	R	
Name	None [7:4]				WDT_CAS-CADE0_1	WDT_-CLEAR0	WDT_MODE0 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	
HW Access	None				R	R	R	
Name	None [15:12]				WDT_CAS-CADE1_2	WDT_-CLEAR1	WDT_MODE1 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							WDT_-MODE2

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			R				
Name	None [31:29]			WDT_BITS2 [28:24]				

Bits	Name	Description
28 : 24	WDT_BITS2	Bit to observe for WDT_INT2: 0: Assert after bit0 of WDT_CTR2 toggles (one int every tick) ... 31: Assert after bit31 of WDT_CTR2 toggles (one int every 2^31 ticks) Default Value: 0
16	WDT_MODE2	Watchdog Counter 2 Mode. Default Value: 0 **0x0: NOTHING :** Free running counter with no interrupt requests **0x1: INT :** Free running counter with interrupt request that occurs one LFCLK cycle after the specified bit in CTR2 toggles (see WDT_BITS2).

10.1.4 MCWDT_CONFIG0 (continued)

11	WDT_CASCADE1_2	Cascade Watchdog Counters 1,2. Counter 2 increments the cycle after WDT_CTR1=WDT_-MATCH1. It is allowed to cascade all three WDT counters. 0: Independent counters 1: Cascaded counters. When cascading all three counters, WDT_CLEAR1 must be 1. Default Value: 0
10	WDT_CLEAR1	Clear Watchdog Counter when WDT_CTR1==WDT_MATCH1. In other words WDT_CTR1 divides LFCLK by (WDT_MATCH1+1). 0: Free running counter 1: Clear on match. In this mode, the minimum legal setting of WDT_MATCH1 is 1. Default Value: 0
9 : 8	WDT_MODE1	Watchdog Counter Action on Match. Action is taken on the next increment after the values match (WDT_CTR1=WDT_MATCH1). Default Value: 0 **0x0: NOTHING :** Do nothing **0x1: INT :** Assert WDT_INTx **0x2: RESET :** Assert WDT Reset **0x3: INT_THEN_RESET :** Assert WDT_INTx, assert WDT Reset after 3rd unhandled interrupt
3	WDT_CASCADE0_1	Cascade Watchdog Counters 0,1. Counter 1 increments the cycle after WDT_CTR0=WDT_-MATCH0. 0: Independent counters 1: Cascaded counters Default Value: 0
2	WDT_CLEAR0	Clear Watchdog Counter when WDT_CTR0=WDT_MATCH0. In other words WDT_CTR0 divides LFCLK by (WDT_MATCH0+1). 0: Free running counter 1: Clear on match. In this mode, the minimum legal setting of WDT_MATCH0 is 1. Default Value: 0
1 : 0	WDT_MODE0	Watchdog Counter Action on Match. Action is taken on the next increment after the values match (WDT_CTR0=WDT_MATCH0). Default Value: 0 **0x0: NOTHING :** Do nothing **0x1: INT :** Assert WDT_INTx

10.1.4 MCWDT_CONFIG0 (continued)

0x2: RESET :

Assert WDT Reset

0x3: INT_THEN_RESET :

Assert WDT_INTx, assert WDT Reset after 3rd unhandled interrupt

10.1.5 MCWDT_CTL0

Multi-Counter Watchdog Counter Control

Address: 0x40260214

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S	None	R	RW
HW Access	None				RW0C	None	RW	R
Name	None [7:4]				WDT_RESET0	None	WDT_ENABLED0	WDT_ENABLE0

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	None	R	RW
HW Access	None				RW0C	None	RW	R
Name	None [15:12]				WDT_RESET1	None	WDT_ENABLED1	WDT_ENABLE1

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW1S	None	R	RW
HW Access	None				RW0C	None	RW	R
Name	None [23:20]				WDT_RESET2	None	WDT_ENABLED2	WDT_ENABLE2

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19	WDT_RESET2	Resets counter 2 back to 0000. Hardware will reset this bit after counter was reset. This will take up to one LFCLK cycle to take effect. Default Value: 0
17	WDT_ENABLED2	Indicates actual state of counter. May lag WDT_ENABLE2 by up to two LFCLK cycles. Default Value: 0
16	WDT_ENABLE2	Enable subcounter 2. May take up to 2 LFCLK cycles to take effect. 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) Default Value: 0
11	WDT_RESET1	Resets counter 1 back to 0000. Hardware will reset this bit after counter was reset. This will take up to one LFCLK cycle to take effect. Default Value: 0
9	WDT_ENABLED1	Indicates actual state of counter. May lag WDT_ENABLE1 by up to two LFCLK cycles. Default Value: 0

10.1.5 MCWDT_CTL0 (continued)

8	WDT_ENABLE1	Enable subcounter 1. May take up to 2 LFCLK cycles to take effect. 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) Default Value: 0
3	WDT_RESET0	Resets counter 0 back to 0000. Hardware will reset this bit after counter was reset. This will take up to one LFCLK cycle to take effect. Default Value: 0
1	WDT_ENABLED0	Indicates actual state of counter. May lag WDT_ENABLE0 by up to two LFCLK cycles. Default Value: 0
0	WDT_ENABLE0	Enable subcounter 0. May take up to 2 LFCLK cycles to take effect. 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) Default Value: 0

10.1.6 MCWDT_INTR0

Multi-Counter Watchdog Counter Interrupt Register

Address: 0x40260218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					A	A	A
Name	None [7:3]					MCWDT_INT2	MCWDT_INT1	MCWDT_INT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	MCWDT_INT2	MCWDT Interrupt Request for sub-counter 2. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. Clearing this bit also prevents Reset from happening when WDT_MODE2=3. Default Value: 0
1	MCWDT_INT1	MCWDT Interrupt Request for sub-counter 1. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. Clearing this bit also prevents Reset from happening when WDT_MODE1=3. Default Value: 0
0	MCWDT_INT0	MCWDT Interrupt Request for sub-counter 0. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. Clearing this bit also prevents Reset from happening when WDT_MODE0=3. Default Value: 0

10.1.7 MCWDT_INTR_SET0

Multi-Counter Watchdog Counter Interrupt Set Register

Address: 0x4026021C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [7:3]					MCWDT_INT2	MCWDT_INT1	MCWDT_INT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	MCWDT_INT2	Set interrupt for MCWDT_INT2 Default Value: 0
1	MCWDT_INT1	Set interrupt for MCWDT_INT1 Default Value: 0
0	MCWDT_INT0	Set interrupt for MCWDT_INT0 Default Value: 0

10.1.8 MCWDT_INTR_MASK0

Multi-Counter Watchdog Counter Interrupt Mask Register

Address: 0x40260220

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					MCWDT_INT2	MCWDT_INT1	MCWDT_INT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	MCWDT_INT2	Interrupt Mask for sub-counter 2. The bit controls if the interrupt is forwarded to the CPU. The interrupt is blocked when the value of the bit is 0. The interrupt is forwarded if the value of the bit is 1. Default Value: 0
1	MCWDT_INT1	Interrupt Mask for sub-counter 1. The bit controls if the interrupt is forwarded to the CPU. The interrupt is blocked when the value of the bit is 0. The interrupt is forwarded if the value of the bit is 1. Default Value: 0
0	MCWDT_INT0	Interrupt Mask for sub-counter 0. The bit controls if the interrupt is forwarded to the CPU. The interrupt is blocked when the value of the bit is 0. The interrupt is forwarded if the value of the bit is 1. Default Value: 0

10.1.9 MCWDT_INTR_MASKED0

Multi-Counter Watchdog Counter Interrupt Masked Register

Address: 0x40260224

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					RW	RW	RW
Name	None [7:3]					MCWDT_INT2	MCWDT_INT1	MCWDT_INT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	MCWDT_INT2	Logical and of corresponding request and mask bits. Default Value: 0
1	MCWDT_INT1	Logical and of corresponding request and mask bits. Default Value: 0
0	MCWDT_INT0	Logical and of corresponding request and mask bits. Default Value: 0

10.1.10 MCWDT_LOCK0

Multi-Counter Watchdog Counter Lock Register

Address: 0x40260228

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	A		None					
Name	MCWDT_LOCK [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	MCWDT_LOCK	Prohibits writing control and configuration registers related to this MCWDT when not equal 0 (as specified in the other register descriptions). Requires at least two different writes to unlock. Note that this field is 2 bits to force multiple writes only. Each MCWDT has a separate local lock. LFCLK settings are locked by the global WDT_LOCK register, and this register has no effect on that. Default Value: 0 **0x0: NO_CHG :** No effect **0x1: CLR0 :** Clears bit 0 **0x2: CLR1 :** Clears bit 1 **0x3: SET01 :** Sets both bits 0 and 1

11 Backup System Registers

This section discusses the Backup System registers. It lists all the registers in mapping tables, in address order.

11.1 Register Details

Register	Address	Description
BACKUP_CTL	0x40270000	Control
BACKUP_RTC_RW	0x40270008	RTC Read Write register
BACKUP_CAL_CTL	0x4027000C	Oscillator calibration for absolute frequency
BACKUP_STATUS	0x40270010	Status
BACKUP_RTC_TIME	0x40270014	Calendar Seconds, Minutes, Hours, Day of Week
BACKUP_RTC_DATE	0x40270018	Calendar Day of Month, Month, Year
BACKUP_ALM1_TIME	0x4027001C	Alarm 1 Seconds, Minute, Hours, Day of Week
BACKUP_ALM1_DATE	0x40270020	Alarm 1 Day of Month, Month
BACKUP_ALM2_TIME	0x40270024	Alarm 2 Seconds, Minute, Hours, Day of Week
BACKUP_ALM2_DATE	0x40270028	Alarm 2 Day of Month, Month
BACKUP_INTR	0x4027002C	Interrupt request register
BACKUP_INTR_SET	0x40270030	Interrupt set request register
BACKUP_INTR_MASK	0x40270034	Interrupt mask register
BACKUP_INTR_MASKED	0x40270038	Interrupt masked request register
BACKUP_OSCCNT	0x4027003C	32kHz oscillator counter
BACKUP_TICKS	0x40270040	128Hz tick counter
BACKUP_PMIC_CTL	0x40270044	PMIC control register
BACKUP_RESET	0x40270048	Backup reset register
BACKUP_BREG0	0x40271000	Backup register region
BACKUP_BREG1	0x40271004	Backup register region. See BACKUP_BREG0 for the details of bit fields.
BACKUP_BREG2	0x40271008	Backup register region. See BACKUP_BREG0 for the details of bit fields.
BACKUP_BREG3	0x4027100C	Backup register region. See BACKUP_BREG0 for the details of bit fields.
BACKUP_BREG4	0x40271010	Backup register region. See BACKUP_BREG0 for the details of bit fields.
BACKUP_BREG5	0x40271014	Backup register region. See BACKUP_BREG0 for the details of bit fields.
BACKUP_BREG6	0x40271018	Backup register region. See BACKUP_BREG0 for the details of bit fields.
BACKUP_BREG7	0x4027101C	Backup register region. See BACKUP_BREG0 for the details of bit fields.
BACKUP_BREG8	0x40271020	Backup register region. See BACKUP_BREG0 for the details of bit fields.
BACKUP_BREG9	0x40271024	Backup register region. See BACKUP_BREG0 for the details of bit fields.

Register	Address	Description
BACKUP_BREG10	0x40271028	Backup register region. See BACKUP_BREG0 for the details of bit fields.
BACKUP_BREG11	0x4027102C	Backup register region. See BACKUP_BREG0 for the details of bit fields.
BACKUP_BREG12	0x40271030	Backup register region. See BACKUP_BREG0 for the details of bit fields.
BACKUP_BREG13	0x40271034	Backup register region. See BACKUP_BREG0 for the details of bit fields.
BACKUP_BREG14	0x40271038	Backup register region. See BACKUP_BREG0 for the details of bit fields.
BACKUP_BREG15	0x4027103C	Backup register region. See BACKUP_BREG0 for the details of bit fields.
BACKUP_TRIM	0x4027FF00	Trim Register

11.1.1 BACKUP_CTL

Control

Address: 0x40270000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	None		
HW Access	None				A	None		
Name	None [7:4]				WCO_EN	None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None		RW	
HW Access	None		A		None		A	
Name	None [15:14]		PRESCALER [13:12]		None [11:10]		CLK_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW	RW		RW
HW Access	None				A	A		A
Name	None [23:20]				VBACK-UP_MEAS	VDDBAK_CTL [18:17]		WCO_BY-PASS

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	EN_CHARGE_KEY [31:24]							

Bits	Name	Description
31 : 24	EN_CHARGE_KEY	When set to 3C, the supercap charger circuit is enabled. Any other code disables the supercap charger. THIS CHARGING CIRCUIT IS FOR A SUPERCAP ONLY AND CANNOT SAFELY CHARGE A BATTERY. DO NOT WRITE THIS KEY WHEN VBACKUP IS CONNECTED TO A BATTERY. Default Value: 0
19	VBACKUP_MEAS	Connect vbackup supply to the vbackup_meas output for measurement by an ADC attached to amuxbusa_adft_vddd. The vbackup_meas signal is scaled to 10% of vbackup, so it is within the supply range of the ADC. Default Value: 0
18 : 17	VDDBAK_CTL	Controls the behavior of the switch that generates vddbak from vbackup or vddd. 0: automatically select vddd if its brownout detector says it is valid. If the brownout says its not valid, then use vmax which is the highest of vddd or vbackup. 1,2,3: force vddbak and vmax to select vbackup, regardless of its voltage. Default Value: 0

11.1.1 BACKUP_CTL (continued)

16	WCO_BYPASS	Configures the WCO for different board-level connections to the WCO pins. For example, this can be used to connect an external watch crystal oscillator instead of a watch crystal. In all cases, the two related GPIO pins (WCO input and output pins) must be configured as analog connections using GPIO registers, and they must be hooked at the board level as described below. Configure this field before enabling the WCO, and do not change this setting when WCO_EN=1. 0: Watch crystal. Connect a 32.768 kHz watch crystal between WCO input and output pins. 1: Clock signal, either a square wave or sine wave. See PRESCALER field for connection information. Default Value: 0
13 : 12	PRESCALER	Prescaler for real time clock used when WCO_BYPASS=1. Configure this field before enabling the WCO, and do not change this setting when WCO_EN=1. 0: 32768 Hz square wave. Connect a 32768 Hz square wave to WCO output pin. Do not connect WCO input pin. 1: 60 Hz sine wave. Connect an AC-coupled sine wave to WCO input pin. Do not connect the WCO output pin at the board level. 2: 50 Hz sine wave. Connect an AC-couple sine wave to WCO input pin. Do not connect the WCO output pin at the board level. 3: reserved (32768 Hz) Default Value: 0
9 : 8	CLK_SEL	Clock select for BAK clock Default Value: 0 **0x0: WCO :** Watch-crystal oscillator input. **0x1: ALTBAK :** This allows to use the LFCLK selection as an alternate backup domain clock. Note that LFCLK is not available in all power modes, and clock glitches can propagate into the backup logic when the clock is stopped. For this reason, if the WCO is intended as the clock source then choose it directly instead of routing through LFCLK.
3	WCO_EN	Watch-crystal oscillator (WCO) enable. If there is a write in progress when this bit is cleared, the WCO will be internally kept on until the write completes. After enabling the WCO software must wait until STATUS.WCO_OK=1 before configuring any component that depends on clk_lf/clk_bak, like for example RTC or WDTs. Follow the procedure in BACKUP_RTC_RW to access this bit. Default Value: 0

11.1.2 BACKUP_RTC_RW

RTC Read Write register

Address: 0x40270008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						A	A
Name	None [7:2]						WRITE	READ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	WRITE	Write bit Only when this bit is set can the RTC registers be written to (otherwise writes are ignored). This bit cannot be set if the RTC is still busy with a previous update (see RTC_BUSY bit) or if the Read bit is set or getting set. The user writes to the RTC user registers, when the Write bit is cleared by the user then the user registers content is copied to the actual RTC registers. Only user RTC registers that were written to will get copied, others will not be affected. When the SECONDS field is updated then TICKS will also be reset (WDT is not affected). When the Write bit is cleared by a reset (brown out/DeepSleep) then the RTC update will be ignored/lost. Do not set the Write bit if the RTC if the RTC is still busy with a previous update (see RTC_BUSY). Do not set the Write bit at the same time that the Read bit is cleared. Default Value: 0
0	READ	Read bit When this bit is set the RTC registers will be copied to user registers and frozen so that a coherent RTC value can safely be read. The RTC will keep on running. Do not set the read bit if the RTC is still busy with a previous update (see RTC_BUSY bit) or if the Write bit is set. Do not set the Read bit at the same time that the Write bit is cleared. Default Value: 0

11.1.3 BACKUP_CAL_CTL

Oscillator calibration for absolute frequency

Address: 0x4027000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW					
HW Access	None	A	A					
Name	None	CALIB_-SIGN	CALIB_VAL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	A	None						
Name	CAL_OUT	None [30:24]						

Bits	Name	Description
31	CAL_OUT	Output enable for 512Hz signal for calibration and allow CALIB_VAL to be written. Note that calibration does not affect the 512Hz output signal. Default Value: 0
6	CALIB_SIGN	Calibration sign: 0= Negative sign: remove pulses (it takes more clock ticks to count one second) 1= Positive sign: add pulses (it takes less clock ticks to count one second) Default Value: 0
5 : 0	CALIB_VAL	Calibration value for absolute frequency (at a fixed temperature). Each step causes 128 ticks to be added or removed each hour. Effectively that means that each step is 1.085ppm (= 128/(60*60*32,768)). Positive values 0x01-0x3c (1..60) add pulses, negative values remove pulses, thus giving a range of +/-65.1 ppm (limited by 60 minutes per hour, not the range of this field) Calibration is performed hourly, starting at 59 minutes and 59 seconds, and applied as 64 ticks every 30 seconds until there have been 2*CALIB_VAL adjustments. Default Value: 0

11.1.4 BACKUP_STATUS

Status

Address: 0x40270010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	None	R
HW Access	None					W	None	W
Name	None [7:3]					WCO_OK	None	RTC_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	WCO_OK	Indicates that output has transitioned. Default Value: 0
0	RTC_BUSY	pending RTC write Default Value: 0

11.1.5 BACKUP_RTC_TIME

Calendar Seconds, Minutes, Hours, Day of Week

Address: 0x40270014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	A						
Name	None	RTC_SEC [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW						
HW Access	None	A						
Name	None	RTC_MIN [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW	RW					
HW Access	None	A	A					
Name	None	CTRL_12HR	RTC_HOUR [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					A		
Name	None [31:27]					RTC_DAY [26:24]		

Bits	Name	Description
26 : 24	RTC_DAY	Calendar Day of the week in BCD, 1-7 It is up to the user to define the meaning of the values, but 1=Monday is recommended Default Value: 0
22	CTRL_12HR	Select 12/24HR mode: 1=12HR, 0=24HR Default Value: 0
21 : 16	RTC_HOUR	Calendar hours in BCD, value depending on 12/24HR mode 0=24HR: [21:16]=0-23 1=12HR: [21]:0=AM, 1=PM, [20:16]=1-12 Default Value: 0
14 : 8	RTC_MIN	Calendar minutes in BCD, 0-59 Default Value: 0
6 : 0	RTC_SEC	Calendar seconds in BCD, 0-59 Default Value: 0

11.1.6 BACKUP_RTC_DATE

Calendar Day of Month, Month, Year

Address: 0x40270018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		A					
Name	None [7:6]		RTC_DATE [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			A				
Name	None [15:13]			RTC_MON [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	RTC_YEAR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	RTC_YEAR	Calendar year in BCD, 0-99 Default Value: 0
12 : 8	RTC_MON	Calendar Month in BCD, 1-12 Default Value: 0
5 : 0	RTC_DATE	Calendar Day of the Month in BCD, 1-31 Automatic Leap Year Correction Default Value: 0

11.1.7 BACKUP_ALM1_TIME

Alarm 1 Seconds, Minute, Hours, Day of Week

Address: 0x4027001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW						
HW Access	A	A						
Name	ALM_SEC_EN	ALM_SEC [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW						
HW Access	A	A						
Name	ALM_MIN_EN	ALM_MIN [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW					
HW Access	A	None	A					
Name	ALM_HOUR_EN	None	ALM_HOUR [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None				RW		
HW Access	A	None				A		
Name	ALM_-DAY_EN	None [30:27]				ALM_DAY [26:24]		

Bits	Name	Description
31	ALM_DAY_EN	Alarm Day of the Week enable: 0=ignore, 1=match Default Value: 0
26 : 24	ALM_DAY	Alarm Day of the week in BCD, 1-7 It is up to the user to define the meaning of the values, but 1=Monday is recommended Default Value: 1
23	ALM_HOUR_EN	Alarm hour enable: 0=ignore, 1=match Default Value: 0
21 : 16	ALM_HOUR	Alarm hours in BCD, value depending on 12/24HR mode 12HR: [5]:0=AM, 1=PM, [4:0]=1-12 24HR: [5:0]=0-23 Default Value: 0
15	ALM_MIN_EN	Alarm minutes enable: 0=ignore, 1=match Default Value: 0

11.1.7 BACKUP_ALM1_TIME (continued)

14 : 8	ALM_MIN	Alarm minutes in BCD, 0-59 Default Value: 0
7	ALM_SEC_EN	Alarm second enable: 0=ignore, 1=match Default Value: 0
6 : 0	ALM_SEC	Alarm seconds in BCD, 0-59 Default Value: 0

11.1.8 BACKUP_ALM1_DATE

Alarm 1 Day of Month, Month

Address: 0x40270020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	None	RW					
HW Access	A	None	A					
Name	ALM_-DATE_EN	None	ALM_DATE [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW	None		RW				
HW Access	A	None		A				
Name	ALM_MON_EN	None [14:13]		ALM_MON [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	A	None						
Name	ALM_EN	None [30:24]						

Bits	Name	Description
31	ALM_EN	Master enable for alarm 1. 0: Alarm 1 is disabled. Fields for date and time are ignored. 1: Alarm 1 is enabled. Alarm triggers whenever the new date and time matches all the enabled date and time fields, which can happen more than once depending on configuration. If none of the date and time fields are enabled, then this alarm triggers once every second. Default Value: 0
15	ALM_MON_EN	Alarm Month enable: 0=ignore, 1=match Default Value: 0
12 : 8	ALM_MON	Alarm Month in BCD, 1-12 Default Value: 1
7	ALM_DATE_EN	Alarm Day of the Month enable: 0=ignore, 1=match Default Value: 0
5 : 0	ALM_DATE	Alarm Day of the Month in BCD, 1-31 Leap Year corrected Default Value: 1

11.1.9 BACKUP_ALM2_TIME

Alarm 2 Seconds, Minute, Hours, Day of Week

Address: 0x40270024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW						
HW Access	A	A						
Name	ALM_SEC_EN	ALM_SEC [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW						
HW Access	A	A						
Name	ALM_MIN_EN	ALM_MIN [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW					
HW Access	A	None	A					
Name	ALM_HOUR_EN	None	ALM_HOUR [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None				RW		
HW Access	A	None				A		
Name	ALM_-DAY_EN	None [30:27]				ALM_DAY [26:24]		

Bits	Name	Description
31	ALM_DAY_EN	Alarm Day of the Week enable: 0=ignore, 1=match Default Value: 0
26 : 24	ALM_DAY	Alarm Day of the week in BCD, 1-7 It is up to the user to define the meaning of the values, but 1=Monday is recommended Default Value: 1
23	ALM_HOUR_EN	Alarm hour enable: 0=ignore, 1=match Default Value: 0
21 : 16	ALM_HOUR	Alarm hours in BCD, value depending on 12/24HR mode 12HR: [5]:0=AM, 1=PM, [4:0]=1-12 24HR: [5:0]=0-23 Default Value: 0
15	ALM_MIN_EN	Alarm minutes enable: 0=ignore, 1=match Default Value: 0

11.1.9 BACKUP_ALM2_TIME (continued)

14 : 8	ALM_MIN	Alarm minutes in BCD, 0-59 Default Value: 0
7	ALM_SEC_EN	Alarm second enable: 0=ignore, 1=match Default Value: 0
6 : 0	ALM_SEC	Alarm seconds in BCD, 0-59 Default Value: 0

11.1.10 BACKUP_ALM2_DATE

Alarm 2 Day of Month, Month

Address: 0x40270028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	None	RW					
HW Access	A	None	A					
Name	ALM_-DATE_EN	None	ALM_DATE [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW	None		RW				
HW Access	A	None		A				
Name	ALM_MON_EN	None [14:13]		ALM_MON [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	A	None						
Name	ALM_EN	None [30:24]						

Bits	Name	Description
31	ALM_EN	Master enable for alarm 2. 0: Alarm 2 is disabled. Fields for date and time are ignored. 1: Alarm 2 is enabled. Alarm triggers whenever the new date and time matches all the enabled date and time fields, which can happen more than once depending on configuration. If none of the date and time fields are enabled, then this alarm triggers once every second. Default Value: 0
15	ALM_MON_EN	Alarm Month enable: 0=ignore, 1=match Default Value: 0
12 : 8	ALM_MON	Alarm Month in BCD, 1-12 Default Value: 1
7	ALM_DATE_EN	Alarm Day of the Month enable: 0=ignore, 1=match Default Value: 0
5 : 0	ALM_DATE	Alarm Day of the Month in BCD, 1-31 Leap Year corrected Default Value: 1

11.1.11 BACKUP_INTR

Interrupt request register

Address: 0x4027002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [7:3]					CENTURY	ALARM2	ALARM1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CENTURY	Century overflow interrupt Default Value: 0
1	ALARM2	Alarm 2 Interrupt Default Value: 0
0	ALARM1	Alarm 1 Interrupt Default Value: 0

11.1.12 BACKUP_INTR_SET

Interrupt set request register

Address: 0x40270030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [7:3]					CENTURY	ALARM2	ALARM1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CENTURY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	ALARM2	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	ALARM1	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

11.1.13 BACKUP_INTR_MASK

Interrupt mask register

Address: 0x40270034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					CENTURY	ALARM2	ALARM1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CENTURY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	ALARM2	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	ALARM1	Mask bit for corresponding bit in interrupt request register. Default Value: 0

11.1.14 BACKUP_INTR_MASKED

Interrupt masked request register

Address: 0x40270038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					RW	RW	RW
Name	None [7:3]					CENTURY	ALARM2	ALARM1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CENTURY	Logical and of corresponding request and mask bits. Default Value: 0
1	ALARM2	Logical and of corresponding request and mask bits. Default Value: 0
0	ALARM1	Logical and of corresponding request and mask bits. Default Value: 0

11.1.15 BACKUP_OSCCNT

32kHz oscillator counter

Address: 0x4027003C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	A							
Name	CNT32KHZ [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CNT32KHZ	32kHz oscillator count (msb=128Hz), calibration can cause bit 6 to skip. Reset when RTC_-TIME.RTC_SEC fields is written. Default Value: 0

11.1.16 BACKUP_TICKS

128Hz tick counter

Address: 0x40270040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R					
HW Access	None		A					
Name	None [7:6]		CNT128HZ [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	CNT128HZ	128Hz counter (msb=2Hz) When SECONDS is written this field will be reset. Default Value: 0

11.1.17 BACKUP_PMIC_CTL

PMIC control register

Address: 0x40270044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	UNLOCK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							A
Name	None [23:17]							POLARITY

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW1S	RW	None				
HW Access	A	R	A	None				
Name	PMIC_EN	PMIC_AL-WAYSEN	PMIC_EN_OUTEN	None [28:24]				

Bits	Name	Description
31	PMIC_EN	Enable for external PMIC that supplies vddd (if present). This bit will only clear if UNLOCK was written correctly in a previous write operation and PMIC_ALWAYSEN=0. When PMIC_EN=0, the system functions normally until vddd is no longer present (OFF w/Backup mode). Firmware can set this bit, if it does so before vddd is actually removed. This bit is also set by any RTC alarm or PMIC pin wakeup event regardless of UNLOCK setting. Default Value: 1
30	PMIC_ALWAYSEN	Override normal PMIC controls to prevent accidentally turning off the PMIC by errant firmware. 0: Normal operation, PMIC_EN and PMIC_OUTEN work as described 1: PMIC_EN and PMIC_OUTEN are ignored and the output pad is forced enabled. Note: This bit is a write-once bit until the next backup reset. Default Value: 0
29	PMIC_EN_OUTEN	Output enable for the output driver in the PMIC_EN pad. 0: Output pad is tristate for PMIC_EN pin. This can allow this pin to be used for another purpose. Tristate condition is kept only if the UNLOCK key (0x3A) is present 1: Output pad is enabled for PMIC_EN pin. Default Value: 1

11.1.17 BACKUP_PMIC_CTL (continued)

16	POLARITY	Set polarity of wakeup signal used to enable the PMIC. Always write this bit "1". 0: reserved for future use, 1: PMIC enables when wakeup signal is high. Default Value: 0
15 : 8	UNLOCK	This byte must be set to 0x3A for PMIC to be disabled. When the UNLOCK code is not present: writes to PMIC_EN field are ignored and the hardware ignores the value in PMIC_EN. Do not change PMIC_EN in the same write cycle as setting/clearing the UNLOCK code; do these in separate write cycles. Default Value: 0

11.1.18 BACKUP_RESET

Backup reset register

Address: 0x40270048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	None						
HW Access	A	None						
Name	RESET	None [30:24]						

Bits	Name	Description
31	RESET	Writing 1 to this register resets the backup logic. Hardware clears it when the reset is complete. After setting this register, firmware should confirm it reads as 0 before attempting to write other backup registers. Default Value: 0

11.1.19 BACKUP_BREG0

Backup register region

Address: 0x40271000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	BREG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	BREG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	BREG [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	BREG [31:24]							

Bits	Name	Description
31 : 0	BREG	Backup memory that contains application-specific data. Memory is retained on vbackup supply. Default Value: 0

11.1.20 BACKUP_TRIM

Trim Register

Address: 0x4027FF00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	TRIM	WCO trim Default Value: 0

12 Direct Memory Access Registers

This section discusses the Direct Memory Access (DMA) registers. It lists all the registers in mapping tables, in address order.

12.1 Register Details

Register	Address	Description
DW0_CTL0	0x40280000	Control
DW0_STATUS0	0x40280004	Status
DW0_ACT_DESCR_CTL0	0x40280020	Active descriptor control
DW0_ACT_DESCR_SRC0	0x40280024	Active descriptor source
DW0_ACT_DESCR_DST0	0x40280028	Active descriptor destination
DW0_ACT_DESCR_X_CTL0	0x40280030	Active descriptor X loop control
DW0_ACT_DESCR_Y_CTL0	0x40280034	Active descriptor Y loop control
DW0_ACT_DESCR_NEXT_PTR0	0x40280038	Active descriptor next pointer
DW0_ACT_SRC0	0x40280040	Active source
DW0_ACT_DST0	0x40280044	Active destination
DW0_CRC_CTL0	0x40280100	CRC control
DW0_CRC_DATA_CTL0	0x40280110	CRC data control
DW0_CRC_POL_CTL0	0x40280120	CRC polynomial control
DW0_CRC_LFSR_CTL0	0x40280130	CRC LFSR control
DW0_CRC_REM_CTL0	0x40280140	CRC remainder control
DW0_CRC_REM_RESULT0	0x40280148	CRC remainder result
DW0_CH_STRUCT0_CH_CTL	0x40288000	Channel control
DW0_CH_STRUCT0_CH_STATUS	0x40288004	Channel status
DW0_CH_STRUCT0_CH_IDX	0x40288008	Channel current indices
DW0_CH_STRUCT0_CH_CURR_PTR	0x4028800C	Channel current descriptor pointer
DW0_CH_STRUCT0_INTR	0x40288010	Interrupt
DW0_CH_STRUCT0_INTR_SET	0x40288014	Interrupt set
DW0_CH_STRUCT0_INTR_MASK	0x40288018	Interrupt mask
DW0_CH_STRUCT0_INTR_MASKED	0x4028801C	Interrupt masked
DW0_CH_STRUCT1_CH_CTL	0x40288040	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT1_CH_STATUS	0x40288044	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT1_CH_IDX	0x40288048	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT1_CH_CURR_PTR	0x4028804C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.

Register	Address	Description
DW0_CH_STRUCT1_INTR	0x40288050	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT1_INTR_SET	0x40288054	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT1_INTR_MASK	0x40288058	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT1_INTR_MASKED	0x4028805C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT2_CH_CTL	0x40288080	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT2_CH_STATUS	0x40288084	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT2_CH_IDX	0x40288088	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT2_CH_CURR_PTR	0x4028808C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT2_INTR	0x40288090	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT2_INTR_SET	0x40288094	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT2_INTR_MASK	0x40288098	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT2_INTR_MASKED	0x4028809C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT3_CH_CTL	0x402880C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT3_CH_STATUS	0x402880C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT3_CH_IDX	0x402880C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT3_CH_CURR_PTR	0x402880CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT3_INTR	0x402880D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT3_INTR_SET	0x402880D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT3_INTR_MASK	0x402880D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT3_INTR_MASKED	0x402880DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT4_CH_CTL	0x40288100	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT4_CH_STATUS	0x40288104	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT4_CH_IDX	0x40288108	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT4_CH_CURR_PTR	0x4028810C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT4_INTR	0x40288110	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT4_INTR_SET	0x40288114	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT4_INTR_MASK	0x40288118	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT4_INTR_MASKED	0x4028811C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT5_CH_CTL	0x40288140	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT5_CH_STATUS	0x40288144	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT5_CH_IDX	0x40288148	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT5_CH_CURR_PTR	0x4028814C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT5_INTR	0x40288150	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT5_INTR_SET	0x40288154	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT5_INTR_MASK	0x40288158	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT5_INTR_MASKED	0x4028815C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT6_CH_CTL	0x40288180	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT6_CH_STATUS	0x40288184	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT6_CH_IDX	0x40288188	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT6_CH_CURR_PTR	0x4028818C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT6_INTR	0x40288190	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.

Register	Address	Description
DW0_CH_STRUCT6_INTR_SET	0x40288194	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT6_INTR_MASK	0x40288198	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT6_INTR_MASKED	0x4028819C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT7_CH_CTL	0x402881C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT7_CH_STATUS	0x402881C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT7_CH_IDX	0x402881C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT7_CH_CURR_PTR	0x402881CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT7_INTR	0x402881D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT7_INTR_SET	0x402881D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT7_INTR_MASK	0x402881D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT7_INTR_MASKED	0x402881DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT8_CH_CTL	0x40288200	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT8_CH_STATUS	0x40288204	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT8_CH_IDX	0x40288208	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT8_CH_CURR_PTR	0x4028820C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT8_INTR	0x40288210	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT8_INTR_SET	0x40288214	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT8_INTR_MASK	0x40288218	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT8_INTR_MASKED	0x4028821C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT9_CH_CTL	0x40288240	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT9_CH_STATUS	0x40288244	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT9_CH_IDX	0x40288248	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT9_CH_CURR_PTR	0x4028824C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT9_INTR	0x40288250	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT9_INTR_SET	0x40288254	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT9_INTR_MASK	0x40288258	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT9_INTR_MASKED	0x4028825C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT10_CH_CTL	0x40288280	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT10_CH_STATUS	0x40288284	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT10_CH_IDX	0x40288288	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT10_CH_CURR_PTR	0x4028828C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT10_INTR	0x40288290	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT10_INTR_SET	0x40288294	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT10_INTR_MASK	0x40288298	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT10_INTR_MASKED	0x4028829C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT11_CH_CTL	0x402882C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT11_CH_STATUS	0x402882C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT11_CH_IDX	0x402882C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT11_CH_CURR_PTR	0x402882CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT11_INTR	0x402882D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT11_INTR_SET	0x402882D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.

Register	Address	Description
DW0_CH_STRUCT11_INTR_MASK	0x402882D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT11_INTR_MASKED	0x402882DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT12_CH_CTL	0x40288300	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT12_CH_STATUS	0x40288304	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT12_CH_IDX	0x40288308	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT12_CH_CURR_PTR	0x4028830C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT12_INTR	0x40288310	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT12_INTR_SET	0x40288314	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT12_INTR_MASK	0x40288318	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT12_INTR_MASKED	0x4028831C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT13_CH_CTL	0x40288340	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT13_CH_STATUS	0x40288344	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT13_CH_IDX	0x40288348	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT13_CH_CURR_PTR	0x4028834C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT13_INTR	0x40288350	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT13_INTR_SET	0x40288354	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT13_INTR_MASK	0x40288358	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT13_INTR_MASKED	0x4028835C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT14_CH_CTL	0x40288380	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT14_CH_STATUS	0x40288384	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT14_CH_IDX	0x40288388	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT14_CH_CURR_PTR	0x4028838C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT14_INTR	0x40288390	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT14_INTR_SET	0x40288394	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT14_INTR_MASK	0x40288398	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT14_INTR_MASKED	0x4028839C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT15_CH_CTL	0x402883C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT15_CH_STATUS	0x402883C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT15_CH_IDX	0x402883C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT15_CH_CURR_PTR	0x402883CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT15_INTR	0x402883D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT15_INTR_SET	0x402883D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT15_INTR_MASK	0x402883D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT15_INTR_MASKED	0x402883DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT16_CH_CTL	0x40288400	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT16_CH_STATUS	0x40288404	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT16_CH_IDX	0x40288408	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT16_CH_CURR_PTR	0x4028840C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT16_INTR	0x40288410	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT16_INTR_SET	0x40288414	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT16_INTR_MASK	0x40288418	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.

Register	Address	Description
DW0_CH_STRUCT16_INTR_MASKED	0x4028841C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT17_CH_CTL	0x40288440	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT17_CH_STATUS	0x40288444	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT17_CH_IDX	0x40288448	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT17_CH_CURR_PTR	0x4028844C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT17_INTR	0x40288450	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT17_INTR_SET	0x40288454	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT17_INTR_MASK	0x40288458	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT17_INTR_MASKED	0x4028845C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT18_CH_CTL	0x40288480	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT18_CH_STATUS	0x40288484	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT18_CH_IDX	0x40288488	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT18_CH_CURR_PTR	0x4028848C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT18_INTR	0x40288490	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT18_INTR_SET	0x40288494	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT18_INTR_MASK	0x40288498	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT18_INTR_MASKED	0x4028849C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT19_CH_CTL	0x402884C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT19_CH_STATUS	0x402884C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT19_CH_IDX	0x402884C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT19_CH_CURR_PTR	0x402884CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT19_INTR	0x402884D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT19_INTR_SET	0x402884D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT19_INTR_MASK	0x402884D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT19_INTR_MASKED	0x402884DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT20_CH_CTL	0x40288500	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT20_CH_STATUS	0x40288504	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT20_CH_IDX	0x40288508	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT20_CH_CURR_PTR	0x4028850C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT20_INTR	0x40288510	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT20_INTR_SET	0x40288514	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT20_INTR_MASK	0x40288518	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT20_INTR_MASKED	0x4028851C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT21_CH_CTL	0x40288540	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT21_CH_STATUS	0x40288544	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT21_CH_IDX	0x40288548	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT21_CH_CURR_PTR	0x4028854C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT21_INTR	0x40288550	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT21_INTR_SET	0x40288554	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT21_INTR_MASK	0x40288558	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT21_INTR_MASKED	0x4028855C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.

Register	Address	Description
DW0_CH_STRUCT22_CH_CTL	0x40288580	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT22_CH_STATUS	0x40288584	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT22_CH_IDX	0x40288588	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT22_CH_CURR_PTR	0x4028858C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT22_INTR	0x40288590	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT22_INTR_SET	0x40288594	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT22_INTR_MASK	0x40288598	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT22_INTR_MASKED	0x4028859C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT23_CH_CTL	0x402885C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT23_CH_STATUS	0x402885C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT23_CH_IDX	0x402885C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT23_CH_CURR_PTR	0x402885CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT23_INTR	0x402885D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT23_INTR_SET	0x402885D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT23_INTR_MASK	0x402885D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT23_INTR_MASKED	0x402885DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT24_CH_CTL	0x40288600	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT24_CH_STATUS	0x40288604	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT24_CH_IDX	0x40288608	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT24_CH_CURR_PTR	0x4028860C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT24_INTR	0x40288610	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT24_INTR_SET	0x40288614	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT24_INTR_MASK	0x40288618	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT24_INTR_MASKED	0x4028861C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT25_CH_CTL	0x40288640	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT25_CH_STATUS	0x40288644	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT25_CH_IDX	0x40288648	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT25_CH_CURR_PTR	0x4028864C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT25_INTR	0x40288650	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT25_INTR_SET	0x40288654	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT25_INTR_MASK	0x40288658	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT25_INTR_MASKED	0x4028865C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT26_CH_CTL	0x40288680	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT26_CH_STATUS	0x40288684	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT26_CH_IDX	0x40288688	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT26_CH_CURR_PTR	0x4028868C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT26_INTR	0x40288690	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT26_INTR_SET	0x40288694	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT26_INTR_MASK	0x40288698	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT26_INTR_MASKED	0x4028869C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT27_CH_CTL	0x402886C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.

Register	Address	Description
DW0_CH_STRUCT27_CH_STATUS	0x402886C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT27_CH_IDX	0x402886C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT27_CH_CURR_PTR	0x402886CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT27_INTR	0x402886D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT27_INTR_SET	0x402886D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT27_INTR_MASK	0x402886D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT27_INTR_MASKED	0x402886DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT28_CH_CTL	0x40288700	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT28_CH_STATUS	0x40288704	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT28_CH_IDX	0x40288708	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT28_CH_CURR_PTR	0x4028870C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT28_INTR	0x40288710	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT28_INTR_SET	0x40288714	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT28_INTR_MASK	0x40288718	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT28_INTR_MASKED	0x4028871C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT29_CH_CTL	0x40288740	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT29_CH_STATUS	0x40288744	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT29_CH_IDX	0x40288748	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT29_CH_CURR_PTR	0x4028874C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT29_INTR	0x40288750	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW0_CH_STRUCT29_INTR_SET	0x40288754	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW0_CH_STRUCT29_INTR_MASK	0x40288758	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT29_INTR_MASKED	0x4028875C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CTL0	0x40290000	Control. See DW0_CTL0 for the details of bit fields.
DW1_STATUS0	0x40290004	Status. See DW0_STATUS0 for the details of bit fields.
DW1_ACT_DESCR_CTL0	0x40290020	Active descriptor control. See DW0_ACT_DESCR_CTL0 for the details of bit fields.
DW1_ACT_DESCR_SRC0	0x40290024	Active descriptor source. See DW0_ACT_DESCR_SRC0 for the details of bit fields.
DW1_ACT_DESCR_DST0	0x40290028	Active descriptor destination. See DW0_ACT_DESCR_DST0 for the details of bit fields.
DW1_ACT_DESCR_X_CTL0	0x40290030	Active descriptor X loop control. See DW0_ACT_DESCR_X_CTL0 for the details of bit fields.
DW1_ACT_DESCR_Y_CTL0	0x40290034	Active descriptor Y loop control. See DW0_ACT_DESCR_Y_CTL0 for the details of bit fields.
DW1_ACT_DESCR_NEXT_PTR0	0x40290038	Active descriptor next pointer. See DW0_ACT_DESCR_NEXT_PTR0 for the details of bit fields.
DW1_ACT_SRC0	0x40290040	Active source. See DW0_ACT_SRC0 for the details of bit fields.
DW1_ACT_DST0	0x40290044	Active destination. See DW0_ACT_DST0 for the details of bit fields.
DW1_CRC_CTL0	0x40290100	CRC control. See DW0_CRC_CTL0 for the details of bit fields.
DW1_CRC_DATA_CTL0	0x40290110	CRC data control. See DW0_CRC_DATA_CTL0 for the details of bit fields.
DW1_CRC_POL_CTL0	0x40290120	CRC polynomial control. See DW0_CRC_POL_CTL0 for the details of bit fields.
DW1_CRC_LFSR_CTL0	0x40290130	CRC LFSR control. See DW0_CRC_LFSR_CTL0 for the details of bit fields.
DW1_CRC_REM_CTL0	0x40290140	CRC remainder control. See DW0_CRC_REM_CTL0 for the details of bit fields.
DW1_CRC_REM_RESULT0	0x40290148	CRC remainder result. See DW0_CRC_REM_RESULT0 for the details of bit fields.
DW1_CH_STRUCT0_CH_CTL	0x40298000	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT0_CH_STATUS	0x40298004	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT0_CH_IDX	0x40298008	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.

Register	Address	Description
DW1_CH_STRUCT0_CH_CURR_PTR	0x4029800C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT0_INTR	0x40298010	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT0_INTR_SET	0x40298014	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT0_INTR_MASK	0x40298018	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT0_INTR_MASKED	0x4029801C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT1_CH_CTL	0x40298040	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT1_CH_STATUS	0x40298044	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT1_CH_IDX	0x40298048	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT1_CH_CURR_PTR	0x4029804C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT1_INTR	0x40298050	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT1_INTR_SET	0x40298054	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT1_INTR_MASK	0x40298058	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT1_INTR_MASKED	0x4029805C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT2_CH_CTL	0x40298080	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT2_CH_STATUS	0x40298084	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT2_CH_IDX	0x40298088	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT2_CH_CURR_PTR	0x4029808C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT2_INTR	0x40298090	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT2_INTR_SET	0x40298094	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT2_INTR_MASK	0x40298098	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT2_INTR_MASKED	0x4029809C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT3_CH_CTL	0x402980C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT3_CH_STATUS	0x402980C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT3_CH_IDX	0x402980C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT3_CH_CURR_PTR	0x402980CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT3_INTR	0x402980D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT3_INTR_SET	0x402980D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT3_INTR_MASK	0x402980D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT3_INTR_MASKED	0x402980DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT4_CH_CTL	0x40298100	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT4_CH_STATUS	0x40298104	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT4_CH_IDX	0x40298108	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT4_CH_CURR_PTR	0x4029810C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT4_INTR	0x40298110	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT4_INTR_SET	0x40298114	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT4_INTR_MASK	0x40298118	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT4_INTR_MASKED	0x4029811C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT5_CH_CTL	0x40298140	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT5_CH_STATUS	0x40298144	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT5_CH_IDX	0x40298148	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT5_CH_CURR_PTR	0x4029814C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.

Register	Address	Description
DW1_CH_STRUCT5_INTR	0x40298150	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT5_INTR_SET	0x40298154	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT5_INTR_MASK	0x40298158	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT5_INTR_MASKED	0x4029815C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT6_CH_CTL	0x40298180	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT6_CH_STATUS	0x40298184	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT6_CH_IDX	0x40298188	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT6_CH_CURR_PTR	0x4029818C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT6_INTR	0x40298190	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT6_INTR_SET	0x40298194	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT6_INTR_MASK	0x40298198	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT6_INTR_MASKED	0x4029819C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT7_CH_CTL	0x402981C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT7_CH_STATUS	0x402981C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT7_CH_IDX	0x402981C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT7_CH_CURR_PTR	0x402981CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT7_INTR	0x402981D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT7_INTR_SET	0x402981D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT7_INTR_MASK	0x402981D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT7_INTR_MASKED	0x402981DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT8_CH_CTL	0x40298200	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT8_CH_STATUS	0x40298204	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT8_CH_IDX	0x40298208	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT8_CH_CURR_PTR	0x4029820C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT8_INTR	0x40298210	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT8_INTR_SET	0x40298214	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT8_INTR_MASK	0x40298218	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT8_INTR_MASKED	0x4029821C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT9_CH_CTL	0x40298240	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT9_CH_STATUS	0x40298244	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT9_CH_IDX	0x40298248	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT9_CH_CURR_PTR	0x4029824C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT9_INTR	0x40298250	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT9_INTR_SET	0x40298254	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT9_INTR_MASK	0x40298258	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT9_INTR_MASKED	0x4029825C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT10_CH_CTL	0x40298280	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT10_CH_STATUS	0x40298284	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT10_CH_IDX	0x40298288	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT10_CH_CURR_PTR	0x4029828C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT10_INTR	0x40298290	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.

Register	Address	Description
DW1_CH_STRUCT10_INTR_SET	0x40298294	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT10_INTR_MASK	0x40298298	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT10_INTR_MASKED	0x4029829C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT11_CH_CTL	0x402982C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT11_CH_STATUS	0x402982C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT11_CH_IDX	0x402982C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT11_CH_CURR_PTR	0x402982CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT11_INTR	0x402982D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT11_INTR_SET	0x402982D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT11_INTR_MASK	0x402982D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT11_INTR_MASKED	0x402982DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT12_CH_CTL	0x40298300	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT12_CH_STATUS	0x40298304	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT12_CH_IDX	0x40298308	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT12_CH_CURR_PTR	0x4029830C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT12_INTR	0x40298310	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT12_INTR_SET	0x40298314	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT12_INTR_MASK	0x40298318	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT12_INTR_MASKED	0x4029831C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT13_CH_CTL	0x40298340	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT13_CH_STATUS	0x40298344	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT13_CH_IDX	0x40298348	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT13_CH_CURR_PTR	0x4029834C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT13_INTR	0x40298350	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT13_INTR_SET	0x40298354	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT13_INTR_MASK	0x40298358	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT13_INTR_MASKED	0x4029835C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT14_CH_CTL	0x40298380	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT14_CH_STATUS	0x40298384	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT14_CH_IDX	0x40298388	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT14_CH_CURR_PTR	0x4029838C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT14_INTR	0x40298390	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT14_INTR_SET	0x40298394	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT14_INTR_MASK	0x40298398	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT14_INTR_MASKED	0x4029839C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT15_CH_CTL	0x402983C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT15_CH_STATUS	0x402983C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT15_CH_IDX	0x402983C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT15_CH_CURR_PTR	0x402983CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT15_INTR	0x402983D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT15_INTR_SET	0x402983D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.

Register	Address	Description
DW1_CH_STRUCT15_INTR_MASK	0x402983D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT15_INTR_MASKED	0x402983DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT16_CH_CTL	0x40298400	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT16_CH_STATUS	0x40298404	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT16_CH_IDX	0x40298408	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT16_CH_CURR_PTR	0x4029840C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT16_INTR	0x40298410	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT16_INTR_SET	0x40298414	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT16_INTR_MASK	0x40298418	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT16_INTR_MASKED	0x4029841C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT17_CH_CTL	0x40298440	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT17_CH_STATUS	0x40298444	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT17_CH_IDX	0x40298448	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT17_CH_CURR_PTR	0x4029844C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT17_INTR	0x40298450	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT17_INTR_SET	0x40298454	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT17_INTR_MASK	0x40298458	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT17_INTR_MASKED	0x4029845C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT18_CH_CTL	0x40298480	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT18_CH_STATUS	0x40298484	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT18_CH_IDX	0x40298488	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT18_CH_CURR_PTR	0x4029848C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT18_INTR	0x40298490	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT18_INTR_SET	0x40298494	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT18_INTR_MASK	0x40298498	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT18_INTR_MASKED	0x4029849C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT19_CH_CTL	0x402984C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT19_CH_STATUS	0x402984C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT19_CH_IDX	0x402984C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT19_CH_CURR_PTR	0x402984CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT19_INTR	0x402984D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT19_INTR_SET	0x402984D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT19_INTR_MASK	0x402984D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT19_INTR_MASKED	0x402984DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT20_CH_CTL	0x40298500	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT20_CH_STATUS	0x40298504	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT20_CH_IDX	0x40298508	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT20_CH_CURR_PTR	0x4029850C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT20_INTR	0x40298510	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT20_INTR_SET	0x40298514	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT20_INTR_MASK	0x40298518	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.

Register	Address	Description
DW1_CH_STRUCT20_INTR_MASKED	0x4029851C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT21_CH_CTL	0x40298540	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT21_CH_STATUS	0x40298544	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT21_CH_IDX	0x40298548	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT21_CH_CURR_PTR	0x4029854C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT21_INTR	0x40298550	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT21_INTR_SET	0x40298554	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT21_INTR_MASK	0x40298558	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT21_INTR_MASKED	0x4029855C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT22_CH_CTL	0x40298580	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT22_CH_STATUS	0x40298584	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT22_CH_IDX	0x40298588	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT22_CH_CURR_PTR	0x4029858C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT22_INTR	0x40298590	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT22_INTR_SET	0x40298594	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT22_INTR_MASK	0x40298598	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT22_INTR_MASKED	0x4029859C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT23_CH_CTL	0x402985C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT23_CH_STATUS	0x402985C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT23_CH_IDX	0x402985C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT23_CH_CURR_PTR	0x402985CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT23_INTR	0x402985D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT23_INTR_SET	0x402985D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT23_INTR_MASK	0x402985D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT23_INTR_MASKED	0x402985DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT24_CH_CTL	0x40298600	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT24_CH_STATUS	0x40298604	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT24_CH_IDX	0x40298608	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT24_CH_CURR_PTR	0x4029860C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT24_INTR	0x40298610	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT24_INTR_SET	0x40298614	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT24_INTR_MASK	0x40298618	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT24_INTR_MASKED	0x4029861C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT25_CH_CTL	0x40298640	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT25_CH_STATUS	0x40298644	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT25_CH_IDX	0x40298648	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT25_CH_CURR_PTR	0x4029864C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT25_INTR	0x40298650	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT25_INTR_SET	0x40298654	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT25_INTR_MASK	0x40298658	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT25_INTR_MASKED	0x4029865C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.

Register	Address	Description
DW1_CH_STRUCT26_CH_CTL	0x40298680	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT26_CH_STATUS	0x40298684	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT26_CH_IDX	0x40298688	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT26_CH_CURR_PTR	0x4029868C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT26_INTR	0x40298690	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT26_INTR_SET	0x40298694	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT26_INTR_MASK	0x40298698	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT26_INTR_MASKED	0x4029869C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT27_CH_CTL	0x402986C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT27_CH_STATUS	0x402986C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT27_CH_IDX	0x402986C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT27_CH_CURR_PTR	0x402986CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT27_INTR	0x402986D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT27_INTR_SET	0x402986D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT27_INTR_MASK	0x402986D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT27_INTR_MASKED	0x402986DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT28_CH_CTL	0x40298700	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT28_CH_STATUS	0x40298704	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT28_CH_IDX	0x40298708	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT28_CH_CURR_PTR	0x4029870C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT28_INTR	0x40298710	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT28_INTR_SET	0x40298714	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT28_INTR_MASK	0x40298718	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT28_INTR_MASKED	0x4029871C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT29_CH_CTL	0x40298740	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT29_CH_STATUS	0x40298744	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT29_CH_IDX	0x40298748	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT29_CH_CURR_PTR	0x4029874C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT29_INTR	0x40298750	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT29_INTR_SET	0x40298754	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT29_INTR_MASK	0x40298758	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT29_INTR_MASKED	0x4029875C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT30_CH_CTL	0x40298780	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT30_CH_STATUS	0x40298784	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT30_CH_IDX	0x40298788	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT30_CH_CURR_PTR	0x4029878C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT30_INTR	0x40298790	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT30_INTR_SET	0x40298794	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT30_INTR_MASK	0x40298798	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT30_INTR_MASKED	0x4029879C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT31_CH_CTL	0x402987C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.

Register	Address	Description
DW1_CH_STRUCT31_CH_STATUS	0x402987C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT31_CH_IDX	0x402987C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT31_CH_CURR_PTR	0x402987CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT31_INTR	0x402987D0	Interrupt. See DW0_CH_STRUCT0_INTR for the details of bit fields.
DW1_CH_STRUCT31_INTR_SET	0x402987D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SET for the details of bit fields.
DW1_CH_STRUCT31_INTR_MASK	0x402987D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT31_INTR_MASKED	0x402987DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DMAC_CTL	0x402A0000	Control
DMAC_ACTIVE	0x402A0008	Active channels
DMAC_CH0_CTL	0x402A1000	Channel control
DMAC_CH0_IDX	0x402A1010	Channel current indices
DMAC_CH0_SRC	0x402A1014	Channel current source address
DMAC_CH0_DST	0x402A1018	Channel current destination address
DMAC_CH0_CURR	0x402A1020	Channel current descriptor pointer
DMAC_CH0_DESCR_STATUS	0x402A1040	Channel descriptor status
DMAC_CH0_DESCR_CTL	0x402A1060	Channel descriptor control
DMAC_CH0_DESCR_SRC	0x402A1064	Channel descriptor source
DMAC_CH0_DESCR_DST	0x402A1068	Channel descriptor destination
DMAC_CH0_DESCR_X_SIZE	0x402A106C	Channel descriptor X size
DMAC_CH0_DESCR_X_INCR	0x402A1070	Channel descriptor X increment
DMAC_CH0_DESCR_Y_SIZE	0x402A1074	Channel descriptor Y size
DMAC_CH0_DESCR_Y_INCR	0x402A1078	Channel descriptor Y increment
DMAC_CH0_DESCR_NEXT	0x402A107C	Channel descriptor next pointer
DMAC_CH0_INTR	0x402A1080	Interrupt
DMAC_CH0_INTR_SET	0x402A1084	Interrupt set
DMAC_CH0_INTR_MASK	0x402A1088	Interrupt mask
DMAC_CH0_INTR_MASKED	0x402A108C	Interrupt masked
DMAC_CH1_CTL	0x402A1100	Channel control. See DMAC_CH0_CTL for the details of bit fields.
DMAC_CH1_IDX	0x402A1110	Channel current indices. See DMAC_CH0_IDX for the details of bit fields.
DMAC_CH1_SRC	0x402A1114	Channel current source address. See DMAC_CH0_SRC for the details of bit fields.
DMAC_CH1_DST	0x402A1118	Channel current destination address. See DMAC_CH0_DST for the details of bit fields.
DMAC_CH1_CURR	0x402A1120	Channel current descriptor pointer. See DMAC_CH0_CURR for the details of bit fields.
DMAC_CH1_DESCR_STATUS	0x402A1140	Channel descriptor status. See DMAC_CH0_DESCR_STATUS for the details of bit fields.
DMAC_CH1_DESCR_CTL	0x402A1160	Channel descriptor control. See DMAC_CH0_DESCR_CTL for the details of bit fields.
DMAC_CH1_DESCR_SRC	0x402A1164	Channel descriptor source. See DMAC_CH0_DESCR_SRC for the details of bit fields.
DMAC_CH1_DESCR_DST	0x402A1168	Channel descriptor destination. See DMAC_CH0_DESCR_DST for the details of bit fields.
DMAC_CH1_DESCR_X_SIZE	0x402A116C	Channel descriptor X size. See DMAC_CH0_DESCR_X_SIZE for the details of bit fields.
DMAC_CH1_DESCR_X_INCR	0x402A1170	Channel descriptor X increment. See DMAC_CH0_DESCR_X_INCR for the details of bit fields.
DMAC_CH1_DESCR_Y_SIZE	0x402A1174	Channel descriptor Y size. See DMAC_CH0_DESCR_Y_SIZE for the details of bit fields.
DMAC_CH1_DESCR_Y_INCR	0x402A1178	Channel descriptor Y increment. See DMAC_CH0_DESCR_Y_INCR for the details of bit fields.
DMAC_CH1_DESCR_NEXT	0x402A117C	Channel descriptor next pointer. See DMAC_CH0_DESCR_NEXT for the details of bit fields.
DMAC_CH1_INTR	0x402A1180	Interrupt. See DMAC_CH0_INTR for the details of bit fields.
DMAC_CH1_INTR_SET	0x402A1184	Interrupt set. See DMAC_CH0_INTR_SET for the details of bit fields.

Register	Address	Description
DMAC_CH1_INTR_MASK	0x402A1188	Interrupt mask. See DMAC_CH0_INTR_MASK for the details of bit fields.
DMAC_CH1_INTR_MASKED	0x402A118C	Interrupt masked. See DMAC_CH0_INTR_MASKED for the details of bit fields.

12.1.1 DW0_CTL0

Control

Address: 0x40280000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	IP enable: '0': Disabled. Disabling the IP activates the IP's Active logic reset: Active logic and non-retention MMIO registers are reset (retention MMIO registers are not affected). '1': Enabled. Default Value: 0

12.1.2 DW0_STATUS0

Status

Address: 0x40280004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None	R	R	R
HW Access	RW				None	RW	RW	RW
Name	PC [7:4]				None	B	NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	None	R	
HW Access	None				W	None	W	
Name	None [15:12]				PREEMPT-ABLE	None	PRIO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			R				
HW Access	None			W				
Name	None [23:21]			CH_IDX [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	R	R			None			
HW Access	W	W			None			
Name	ACTIVE	STATE [30:28]			None [27:24]			

Bits	Name	Description
31	ACTIVE	Active channel present: '0': No. '1': Yes. Default Value: 0
30 : 28	STATE	State of the DW controller. "0": Default/inactive state. "1": Loading descriptor. "2": Loading data element from source location. "3": Storing data element to destination location. "4": CRC functionality (only used for CRC transfer descriptor type). "5": Update of active control information (e.g. source and destination addresses) and wait for trigger de-activation. "6": Error. Default Value: 0
20 : 16	CH_IDX	Active channel index. Default Value: Undefined
11	PREEMPTABLE	Active channel preemptable. Default Value: Undefined

12.1.2 DW0_STATUS0 (continued)

9 : 8	PRIO	Active channel priority. Default Value: Undefined
7 : 4	PC	Active channel protection context. Default Value: Undefined
2	B	Active channel, non-bufferable/bufferable access control: '0': non-bufferable '1': bufferable. Default Value: Undefined
1	NS	Active channel, secure/non-secure access control: '0': secure. '1': non-secure. Default Value: Undefined
0	P	Active channel, user/privileged access control: '0': user mode. '1': privileged mode. Default Value: Undefined

12.1.3 DW0_ACT_DESCR_CTL0

Active descriptor control

Address: 0x40280020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description

12.1.3 DW0_ACT_DESCR_CTL0 (continued)

31 : 0	DATA	Copy of DESCR_CTL of the currently active descriptor. [1:0] WAIT_FOR_DEACT Specifies whether the controller should wait for the input trigger to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controller with the agent that generated the trigger. This field is ONLY used at the completion of the transfer as specified by TR_IN. E.g., a TX FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the controller AND received by the agent. Furthermore, the agent's trigger may be delayed by a few cycles before it reaches the controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW controller performance. "0": Do not wait for trigger de-activation (for pulse sensitive triggers). "1": Wait for up to 4 cycles. "2": Wait for up to 16 cycles. "3": Wait indefinitely. This option may result in controller lockup if the trigger is not de-activated. [3:2] INTR_TYPE Specifies the input trigger type (not to be confused with the descriptor type): "0": A trigger results in the execution of a single transfer. The descriptor type can be single, 1D or 2D. "1": A trigger results in the execution of a single 1D transfer. - If the descriptor type is "single", the trigger results in the execution of a single transfer. - If the descriptor type is "1D" or "2D", the trigger results in the execution of a 1D transfer. "2": A trigger results in the execution of the current descriptor. "3": A trigger results in the execution of the current descriptor and continues (without requiring another input trigger) with the execution of the next descriptor using the next descriptor's information. [5:4] TR_OUT_TYPE Specifies when an output trigger is generated: "0": An output trigger is generated after a single transfer. "1": An output trigger is generated after a single 1D transfer. - If the descriptor type is "single", the output trigger is generated after a single transfer. - If the descriptor type is "1D", "CRC" or "2D", the output trigger is generated after the execution of a 1D transfer. "2": An output trigger is generated after the execution of the current descriptor. "3": An output trigger is generated after the execution of a descriptor list: after the execution of the current descriptor AND the current descriptor DESCR_NEXT_PTR.ADDR is "0". [7:6] TR_IN_TYPE Specifies the input trigger type (not to be confused with the descriptor type): "0": A trigger results in the execution of a single transfer. The descriptor type can be single, 1D or 2D. "1": A trigger results in the execution of a single 1D transfer. - If the descriptor type is "single", the trigger results in the execution of a single transfer. - If the descriptor type is "1D" or "2D", the trigger results in the execution of a 1D transfer. "2": A trigger results in the execution of the current descriptor. "3": A trigger results in the execution of the current descriptor and continues (without requiring another input trigger) with the execution of the next descriptor using the next descriptor's information. [24] CH_DISABLE Specifies whether the channel is disabled or not after completion of the current descriptor (independent of the value of the DESCR_NEXT_PTR value): '0': Channel is not disabled. '1': Channel is disabled. Note: a disabled channel will ignore its input trigger. [26] SRC_TRANSFER_SIZE Specifies the bus transfer size to the source location: '0': As specified by DATA_SIZE. '1': Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element. [27] DST_TRANSFER_SIZE Specifies the bus transfer size to the destination location: '0': As specified by DATA_SIZE. '1': Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element. [29:28] DATA_SIZE Specifies the data element size: "0": Byte (8 bits). "1": Halfword (16 bits). "2": Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: - DATA is 8 bit, SRC is 8 bit, DST is 8 bit. - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit. - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made "0"). - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made "0"). - DATA is 16 bit, SRC is 16 bit, DST is 16 bit. - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit. - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made "0"). - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made "0"). - DATA is 32 bit, SRC is 32 bit, DST is 32 bit. [31:30] DESCR_TYPE Specifies the descriptor type (not to be confused with the trigger type): "0": Single transfer. The DESCR_X_CTL and DESCR_Y_CTL registers are not present and DESCR_NEXT_PTR is at offset 0x0c. "1": 1D transfer. The DESCR_X_CTL register is present, the DESCR_Y_CTL is not present and DESCR_NEXT_PTR is at offset 0x10. A 1D transfer consists out of DESCR_X_CTL.X_COUNT single transfers. "2": 2D transfer. The DESCR_X_CTL and DESCR_Y_CTL registers are present and DESCR_NEXT_PTR is at offset 0x14. A 2D transfer consists of DESCR_X_CTL.X_COUNT*DESCR_Y_CTL.Y_COUNT single transfers. "3": CRC transfer. The DESCR_X_CTL register is present, theDESCR_Y_CTL is not present and DESCR_NEXT_PTR is at offset 0x10. A CRC transfer consists out of DESCR_X_CTL.X_COUNT single transfers. After the execution of the current descriptor, the DESCR_NEXT_PTR address is copied to the channel's CH_CURR_PTR address and CH_STATUS.X_IDX and CH_STATUS.Y_IDX are set to "0". Default Value: Undefined

12.1.4 DW0_ACT_DESCR_SRC0

Active descriptor source

Address: 0x40280024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Copy of DESCR_SRC of the currently active descriptor. Base address of source location. Default Value: Undefined

12.1.5 DW0_ACT_DESCR_DST0

Active descriptor destination

Address: 0x40280028

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Copy of DESCR_DST of the currently active descriptor. Base address of destination location. Note: For a CRC transfer descriptor, this field should be programmed with the address of the CRC_LFSR_CTL register. The calculated CRC LFSR state is written to this address (through the CRYPTO AHB-Lite master interface) when the input trigger is processed. The write transfer will be submitted to the CPUSS and PERI protection schemes. Default Value: Undefined

12.1.6 DW0_ACT_DESCR_X_CTL0

Active descriptor X loop control

Address: 0x40280030

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Copy of DESCR_X_CTL of the currently active descriptor. [11:0] SRC_X_INCR Specifies increment of source address for each X loop iteration (in multiples of SRC_TRANSFER_SIZE). This field is a signed number in the range [-2048, 2047]. If this field is "0", the source address is not incremented. This is useful for reading from RX FIFO structures. [23:12] DST_X_INCR Specifies increment of destination address for each X loop iteration (in multiples of DST_TRANSFER_SIZE). This field is a signed number in the range [-2048, 2047]. If this field is "0", the destination address is not incremented. This is useful for writing to TX FIFO structures. Note: this field is not used for CRC transfer descriptors and must be set to "0". [31:24] X_COUNT Number of iterations (minus 1) of the "X loop" (X_COUNT+1 is the number of single transfers in a 1D transfer). This field is an unsigned number in the range [0, 255], representing 1 through 256 iterations. For a single transfer descriptor type, descriptor will not have X_CTL. Default Value: Undefined

12.1.7 DW0_ACT_DESCR_Y_CTL0

Active descriptor Y loop control

Address: 0x40280034

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Copy of DESCR_Y_CTL of the currently active descriptor. [11:0] SRC_Y_INCR Specifies increment of source address for each Y loop iteration (in multiples of SRC_TRANSFER_SIZE). This field is a signed number in the range [-2048, 2047]. [23:12] DST_Y_INCR Specifies increment of destination address for each Y loop iteration (in multiples of DST_TRANSFER_SIZE). This field is a signed number in the range [-2048, 2047]. [31:24] Y_COUNT Number of iterations (minus 1) of the "Y loop" (X_COUNT+1)*(Y_COUNT+1) is the number of single transfers in a 2D transfer). This field is an unsigned number in the range [0, 255], representing 1 through 256 iterations. For single, 1D and CRC transfer descriptor types, descriptor will not have Y_CTL. Default Value: Undefined

12.1.8 DW0_ACT_DESCR_NEXT_PTR0

Active descriptor next pointer

Address: 0x40280038

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 2	ADDR	Copy of DESCR_NEXT_PTR of the currently active descriptor. [31:2] ADDR Address of next descriptor in descriptor list. When this field is "0", this is the last descriptor in the descriptor list. Default Value: Undefined

12.1.9 DW0_ACT_SRC0

Active source

Address: 0x40280040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SRC_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SRC_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	SRC_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	SRC_ADDR [31:24]							

Bits	Name	Description
31 : 0	SRC_ADDR	Current address of source location. Default Value: Undefined

12.1.10 DW0_ACT_DST0

Active destination

Address: 0x40280044

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DST_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DST_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DST_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DST_ADDR [31:24]							

Bits	Name	Description
31 : 0	DST_ADDR	Current address of destination location. Default Value: Undefined

12.1.11 DW0_CRC_CTL0

CRC control

Address: 0x40280100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							DATA_REVERSE

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							REM_REVERSE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	REM_REVERSE	Specifies whether the remainder is bit reversed (reversal is performed after XORing): '0': No. '1': Yes. Default Value: 0
0	DATA_REVERSE	Specifies the bit order in which a data Byte is processed (reversal is performed after XORing): '0': Most significant bit (bit 1) first. '1': Least significant bit (bit 0) first. Default Value: 0

12.1.12 DW0_CRC_DATA_CTL0

CRC data control

Address: 0x40280110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA_XOR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA_XOR	Specifies a byte mask with which each data byte is XOR'd. The XOR is performed before data reversal. Default Value: 0

12.1.13 DW0_CRC_POL_CTL0

CRC polynomial control

Address: 0x40280120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [31:24]							

Bits	Name	Description
31 : 0	POLYNOMIAL	CRC polynomial. The polynomial is represented WITHOUT the high order bit (this bit is always assumed '1'). The polynomial should be aligned/shifted such that the more significant bits (bit 31 and down) contain the polynomial and the less significant bits (bit 0 and up) contain padding '0's. Some frequently used polynomials: - CRC32: POLYNOMIAL is 0x04c11db7 (x^32 + x^26 + x^23 + x^22 + x^16 + x^12 + x^11 + x^10 + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1). - CRC16: POLYNOMIAL is 0x80050000 (x^16 + x^15 + x^2 + 1, shifted by 16 bit positions). - CRC16 CCITT: POLYNOMIAL is 0x10210000 (x^16 + x^12 + x^5 + 1, shifted by 16 bit positions). Default Value: 0

12.1.14 DW0_CRC_LFSR_CTL0

CRC LFSR control

Address: 0x40280130

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	LFSR32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	LFSR32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	LFSR32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	LFSR32 [31:24]							

Bits	Name	Description
31 : 0	LFSR32	State of a 32-bit Linear Feedback Shift Registers (LFSR) that is used to implement CRC. This register needs to be initialized by SW to provide the CRC seed value. The seed value should be aligned such that the more significant bits (bit 31 and down) contain the seed value and the less significant bits (bit 0 and up) contain padding '0's. Note that SW can write this field. This functionality can be used prevent information leakage (through either CRC_LFSR_CTL or CRC_REM_RESULT). Default Value: 0

12.1.15 DW0_CRC_REM_CTL0

CRC remainder control

Address: 0x40280140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	REM_XOR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	REM_XOR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	REM_XOR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	REM_XOR [31:24]							

Bits	Name	Description
31 : 0	REM_XOR	Specifies a mask with which the CRC_LFSR_CTL.LFSR32 register is XOR'd to produce a remainder. The XOR is performed before remainder reversal. Default Value: 0

12.1.16 DW0_CRC_REM_RESULT0

CRC remainder result

Address: 0x40280148

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	REM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	REM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	REM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	REM [31:24]							

Bits	Name	Description
31 : 0	REM	Remainder value. The alignment of the remainder depends on CRC_REM_CTL0.REM_REVERSE: '0': the more significant bits (bit 31 and down) contain the remainder. '1': the less significant bits (bit 0 and up) contain the remainder. Note: This field is combinatorially derived from CRC_LFSR_CTL.LFSR32, CRC_CTL.REM_REVERSE and CRC_REM_CTL.REM_XOR. Default Value: 0

12.1.17 DW0_CH_STRUCT0_CH_CTL

Channel control

Address: 0x40288000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				None	RW	RW	RW
HW Access	R				None	R	R	R
Name	PC [7:4]				None	B	NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	None	RW	
HW Access	None				R	None	R	
Name	None [15:12]				PREEMPT-ABLE	None	PRIO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW1C	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	Channel enable: '0': Disabled. The channel's trigger is ignored and the channel cannot be made pending and therefore cannot be made active. If a pending channel is disabled, the channel is made non pending. If the activate channel is disabled, the channel is de-activated (bus transactions are completed). '1': Enabled. SW sets this field to '1' to enable a specific channel. HW sets this field to '0' on an error interrupt cause (the specific error is specified by CH_STATUS.INTR_CAUSE). Default Value: 0
11	PREEMPTABLE	Specifies if the channel is preemptable. '0': Not preemptable. '1': Preemptable. This field allows higher priority pending channels (from a higher priority group; i.e. an active channel can NOT be preempted by a pending channel in the same priority group) to preempt the active channel in between "single transfers" (a 1D transfer consists out of X_COUNT single transfers; a 2D transfer consists out of X_COUNT*Y_COUNT single transfers). Preemption will NOT affect the pending status of channel. As a result, after completion of a higher priority activated channel, the current channel may be reactivated. Default Value: Undefined

12.1.17 DW0_CH_STRUCT0_CH_CTL (continued)

9 : 8	PRIO	Channel priority: "0": highest priority. "1" "2" "3": lowest priority. Channels with the same priority constitute a priority group. Priority decoding determines the highest priority pending channel. This channel is determined as follows. First, the highest priority group with pending channels is identified. Second, within this priority group, round robin arbitration is applied. Round robin arbitration (within a priority group) gives the highest priority to the lower channel indices (within the priority group). Default Value: 0
7 : 4	PC	Protection context. This field is set with the protection context of the transaction that writes this register; i.e. the 'write data' is ignored and instead the context is inherited from the write transaction (note the field attributes should be HW:RW, SW:R). All transactions for this channel uses the PC field for the protection context. Default Value: Undefined
2	B	Non-bufferable/bufferable access control: '0': non-bufferable. '1': bufferable. This field is used to indicate to an AMBA bridge that a write transaction can complete without waiting for the destination to accept the write transaction data. All transactions for this channel uses the B field for the non-bufferable/bufferable access control ("hprot[2]"). Default Value: Undefined
1	NS	Secure/on-secure access control: '0': secure. '1': non-secure. This field is set with the secure/non-secure access control of the transaction that writes this register; i.e. the 'write data' is ignored and instead the access control is inherited from the write transaction (note the field attributes should be HW:RW, SW:R). All transactions for this channel use the NS field for the secure/non-secure access control ("hprot[4]"). Default Value: Undefined
0	P	User/privileged access control: '0': user mode. '1': privileged mode. This field is set with the user/privileged access control of the transaction that writes this register; i.e. the 'write data' is ignored and instead the access control is inherited from the write transaction (note the field attributes should be HW:RW, SW:R). All transactions for this channel use the P field for the user/privileged access control ("hprot[1]"). Default Value: Undefined

12.1.18 DW0_CH_STRUCT0_CH_STATUS

Channel status

Address: 0x40288004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				INTR_CAUSE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	PENDING	None [30:24]						

Bits	Name	Description
31	PENDING	Specifies pending DW channels; i.e. enabled channels whose trigger got activated. This field includes all channels that are in the pending state (not scheduled) or active state (scheduled and performing data transfer(s)). Default Value: 0
3 : 0	INTR_CAUSE	Specifies the source of the interrupt cause: "0": No interrupt generated "1": Interrupt based on transfer complettion configuration based on INTR_TYPE "2": Source transfer bus error "3": Destination transfer bus error "4": Source address misalignment "5": Destination address misalignment "6": Current descriptor pointer is null "7": Active channel is disabled "8": Descriptor bus error "9"-"15": Not used. For error related interrupt causes (INTR_CAUSE is "2", "3", ..., "8"), the channel is disabled (HW sets CH_CTL.ENABLED to '0'). Default Value: Undefined

12.1.19 DW0_CH_STRUCT0_CH_IDX

Channel current indices

Address: 0x40288008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	X_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	Y_IDX [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	Y_IDX	Specifies the Y loop index, with X_COUNT taken from the current descriptor. Note: HW sets this field to "0" when it updates the current descriptor pointer CH_CURR_PTR with DESCR_NEXT_PTR after execution of the current descriptor. Note: SW should set this field to "0" when it updates CH_CURR_PTR. Default Value: Undefined
7 : 0	X_IDX	Specifies the X loop index. In the range of [0, X_COUNT], with X_COUNT taken from the current descriptor. Note: HW sets this field to "0" when it updates the current descriptor pointer CH_CURR_PTR with DESCR_NEXT_PTR after execution of the current descriptor. Note: SW should set this field to "0" when it updates CH_CURR_PTR. Default Value: Undefined

12.1.20 DW0_CH_STRUCT0_CH_CURR_PTR

Channel current descriptor pointer

Address: 0x4028800C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	RW						None	
Name	ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 2	ADDR	Address of current descriptor. When this field is "0", there is no valid descriptor. Note: HW updates the current descriptor pointer CH_CURR_PTR with DESCR_NEXT_PTR after execution of the current descriptor. Note: Typically, when SW updates the current descriptor pointer CH_CURR_PTR, it also sets CH_IDX.X_IDX and CH_IDX.Y_IDX to "0". Default Value: Undefined

12.1.21 DW0_CH_STRUCT0_INTR

Interrupt

Address: 0x40288010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [7:1]							CH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CH	Set to '1', when event (as specified by CH_STATUS.INTR_CAUSE) is detected. Write INTR.CH field with '1', to clear bit. Write INTR_SET.CH field with '1', to set bit. Default Value: 0

12.1.22 DW0_CH_STRUCT0_INTR_SET

Interrupt set

Address: 0x40288014

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							A
Name	None [7:1]							CH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CH	Write INTR_SET field with '1' to set corresponding INTR.CH field (a write of '0' has no effect). Default Value: 0

12.1.23 DW0_CH_STRUCT0_INTR_MASK

Interrupt mask

Address: 0x40288018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							CH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CH	Mask for corresponding field in INTR register. Default Value: 0

12.1.24 DW0_CH_STRUCT0_INTR_MASKED

Interrupt masked

Address: 0x4028801C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							CH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CH	Logical and of corresponding INTR and INTR_MASK fields. Default Value: 0

12.1.25 DMAC_CTL

Control

Address: 0x402A0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	IP enable: '0': Disabled. All non-retention registers (command and status registers) are reset to their default value when the IP is disabled. All retention registers retain their value when the IP is disabled. '1': Enabled. Default Value: 0 **0x0: DISABLED :** **0x1: ENABLED :**

12.1.26 DMAC_ACTIVE

Active channels

Address: 0x402A0008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	
HW Access	None						W	
Name	None [7:2]						ACTIVE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	ACTIVE	Specifies active channels; i.e. enabled channels whose trigger got activated. Default Value: 0

12.1.27 DMAC_CH0_CTL

Channel control

Address: 0x402A1000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				None	RW	RW	RW
HW Access	R				None	R	R	R
Name	PC [7:4]				None	B	NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						PRIO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW1C	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	Channel enable: '0': Disabled. The channel's trigger is ignored and the channel cannot be made pending and therefore cannot be made active. If a pending channel is disabled, the channel is made non pending. If the activate channel is disabled, the channel is de-activated (bus transactions are completed). '1': Enabled. SW sets this field to '1' to enable a specific channel. HW sets this field to '0' when an error interrupt cause is activated. Default Value: 0

12.1.27 DMAC_CH0_CTL (continued)

9 : 8	PRIO	Channel priority: "0": highest priority. "1" "2" "3": lowest priority. Channels with the same priority constitute a priority group and within this priority group, the following "roundrobin" arbitration is applied. A "round" consists of a contiguous sequence of channel activations, within this priority group, without any repetition. Within a round, higher priority is given to the lower channel indices. The notion of a round guarantees that within a group, higher channel indices do not yield to lower indices indefinitely. Default Value: 0
7 : 4	PC	Protection context. This field is set with the protection context of the transaction that writes this register; i.e. the context is inherited from the write transaction and not specified by the transaction write data. All transactions for this channel uses the PC field for the protection context. Default Value: 0
2	B	Non-bufferable/bufferable access control: '0': non-bufferable. '1': bufferable. This field is used to indicate to an AMBA bridge that a write transaction can complete without waiting for the destination to accept the write transaction data. All transactions for this channel uses the B field for the non-bufferable/bufferable access control ("hprot[2]"). Default Value: 0
1	NS	Secure/on-secure access control: '0': secure. '1': non-secure. This field is set with the secure/non-secure access control of the transaction that writes this register; i.e. the access control is inherited from the write transaction and not specified by the transaction write data. All transactions for this channel use the NS field for the secure/non-secure access control ("hprot[4]"). Default Value: 1
0	P	User/privileged access control: '0': user mode. '1': privileged mode. This field is set with the user/privileged access control of the transaction that writes this register; i.e. the access control is inherited from the write transaction and not specified by the transaction write data. All transactions for this channel use the P field for the user/privileged access control ("hprot[1]"). Default Value: 0

12.1.28 DMAC_CH0_IDX

Channel current indices

Address: 0x402A1010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	X [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	X [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	Y [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	Y [31:24]							

Bits	Name	Description
31 : 16	Y	Specifies the Y loop index, with Y_COUNT taken from the current descriptor. Note: HW sets this field to "0" when it loads a descriptor.. Default Value: Undefined
15 : 0	X	Specifies the X loop index. In the range of [0, X_COUNT], with X_COUNT taken from the current descriptor. Note: HW sets this field to "0" when it loads a descriptor. Default Value: Undefined

12.1.29 DMAC_CH0_SRC

Channel current source address

Address: 0x402A1014

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Current address of source location. Default Value: Undefined

12.1.30 DMAC_CH0_DST

Channel current destination address

Address: 0x402A1018

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Current address of destination location. Default Value: Undefined

12.1.31 DMAC_CH0_CURR

Channel current descriptor pointer

Address: 0x402A1020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	RW						None	
Name	PTR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PTR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	PTR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	PTR [31:24]							

Bits	Name	Description
31 : 2	PTR	Address of current descriptor. When this field is "0", there is no valid descriptor. Note: HW updates the current descriptor pointer CH_CURR_PTR with DESCR_NEXT_PTR after execution of the current descriptor. Default Value: Undefined

12.1.32 DMAC_CH0_DESCR_STATUS

Channel descriptor status

Address: 0x402A1040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	Indicates whether the descriptor information present in DESCR_CTL, DESCR_SRC, DESCR_DST, DESCR_X_SIZE, DESCR_X_INCR, DESCR_Y_SIZE, DESCR_Y_INCR, DESCR_NEXT status registers is valid or not. Default Value: 0

12.1.33 DMAC_CH0_DESCR_CTL

Channel descriptor control

Address: 0x402A1060

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		R		R		R	
HW Access	W		W		W		W	
Name	TR_IN_TYPE [7:6]		TR_OUT_TYPE [5:4]		INTR_TYPE [3:2]		WAIT_FOR_DEACT [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							DATA_PRE FETCH

Bits	23	22	21	20	19	18	17	16
SW Access	None						R	
HW Access	None						W	
Name	None [23:18]						DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None	R			R	R	None	R
HW Access	None	W			W	W	None	W
Name	None	DESCR_TYPE [30:28]			DST_TRAN SFER_SIZE	SRC_TRAN SFER_SIZE	None	CH_DIS- ABLE

Bits	Name	Description

12.1.33 DMAC_CH0_DESCR_CTL (continued)

30 : 28	DESCR_TYPE	Specifies the descriptor type (not to be confused with the trigger type): "0": Single transfer. The DESCR_X_SIZE, DESCR_X_INCR, DESCR_Y_SIZE and DESCR_Y_INCR registers are NOT present. The DESCR_NEXT_PTR is at offset 0x0c. "1": 1D transfer. The DESCR_X_SIZE and DESCR_X_INCR registers are present, the DESCR_Y_SIZE and DESCR_Y_INCR are NOT present. A 1D transfer consists out of DESCR_X_SIZE.X_COUNT+1 single transfers. The DESCR_NEXT_PTR is at offset 0x14. "2": 2D transfer. The DESCR_X_SIZE, DESCR_X_INCR, DESCR_Y_SIZE and DESCR_Y_INCR registers are present. A 2D transfer consists of (DESCR_X_SIZE.X_COUNT+1)*(DESCR_Y_SIZE.Y_COUNT+1) single transfers. The DESCR_NEXT_PTR is at offset 0x1c. "3": Memory copy. The DESCR_X_SIZE register is present, the DESCR_X_INCR, DESCR_Y_SIZE and DESCR_Y_INCR are NOT present. A memory copy transfer copies DESCR_X_SIZE.X_COUNT+1 Bytes and may use Byte, halfword and word transfers. The DESCR_NEXT_PTR is at offset 0x10. "4": Scatter transfer. The DESCR_X_SIZE register is present, the DESCR_DST, DESCR_X_INCR, DESCR_Y_SIZE and DESCR_Y_INCR are NOT present. "5"-"7": Undefined. After the execution of the current descriptor, the DESCR_NEXT_PTR address is copied to the channel's CH_CURR_PTR address and CH_STATUS.X_IDX and CH_STATUS.Y_IDX are set to "0". Default Value: Undefined
27	DST_TRANSFER_SIZE	Specifies the bus transfer size to the destination location: '0': As specified by DATA_SIZE. '1': Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element. Note: this field is not used for a "memory copy" descriptor type. Note: this field must be set to '1' for a "scatter" descriptor type. Default Value: Undefined
26	SRC_TRANSFER_SIZE	Specifies the bus transfer size to the source location: '0': As specified by DATA_SIZE. '1': Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element. Note: this field is not used for a "memory copy" descriptor type. Note: this field must be set to '1' for a "scatter" descriptor type. Default Value: Undefined
24	CH_DISABLE	Specifies whether the channel is disabled or not after completion of the current descriptor (independent of the value of the DESCR_NEXT_PTR value): '0': Channel is not disabled. '1': Channel is disabled. Default Value: Undefined

12.1.33 DMAC_CH0_DESCR_CTL (continued)

17 : 16	DATA_SIZE	Specifies the data element size: "0": Byte (8 bits). "1": Halfword (16 bits). "2": Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: - DATA is 8 bit, SRC is 8 bit, DST is 8 bit. - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit. - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made "0"). - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made "0"). - DATA is 16 bit, SRC is 16 bit, DST is 16 bit. - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit. - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made "0"). - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made "0"). - DATA is 32 bit, SRC is 32 bit, DST is 32 bit. Note: this field is not used for a "memory copy" descriptor type. Note: this field must be set to "2" for a "initialization" descriptor type. Default Value: Undefined
8	DATA_PREFETCH	Source data prefetch: '0': No source data prefetch. Source data transfers are only initiated AFTER the input trigger is activated. '1': Source data prefetch. Source data transfers are initiated as soon as the channel is enabled, the current descriptor pointer is NOT "0" and there is space available in the channel's data FIFO. When the input trigger is activated, the trigger can initiate destination data transfers with data that is already in the channel's data FIFO. This effectively shortens the initial delay of the data transfer. Note: data prefetch should be used with care, to ensure that data coherency is guaranteed and that prefetches do not cause undesired side effects. Default Value: Undefined
7 : 6	TR_IN_TYPE	Specifies the input trigger type (not to be confused with the descriptor type): "0": A trigger results in the execution of a single transfer. The descriptor type can be single, 1D or 2D. "1": A trigger results in the execution of a single 1D transfer. - If the descriptor type is "single", the trigger results in the execution of a single transfer. - If the descriptor type is "1D" or "2D", the trigger results in the execution of a 1D transfer. - If the descriptor type is "memory copy", the trigger results in the execution of a memory copy transfer. - If the descriptor type is "scatter", the trigger results in the execution of an scatter transfer. "2": A trigger results in the execution of the current descriptor. "3": A trigger results in the execution of the current descriptor and continues (without requiring another input trigger) with the execution of the next descriptor using the next descriptor's information. Default Value: Undefined

12.1.33 DMAC_CH0_DESCR_CTL (continued)

5 : 4	TR_OUT_TYPE	Specifies when an output trigger is generated: "0": An output trigger is generated after a single transfer. "1": An output trigger is generated after a single 1D transfer or a memory copy transfer. - If the descriptor type is "single", the output trigger is generated after a single transfer. - If the descriptor type is "1D" or "2D", the output trigger is generated after the execution of a 1D transfer. - If the descriptor type is "memory copy", the output trigger is generated after the execution of a memory copy transfer. - If the descriptor type is "scatter", the output trigger is generated after the execution of a scatter transfer. "2": An output trigger is generated after the execution of the current descriptor. "3": An output trigger is generated after the execution of a descriptor list: after the execution of the current descriptor AND the current descriptor's DESCR_NEXT_PTR.ADDR is "0'. Default Value: Undefined
3 : 2	INTR_TYPE	Specifies when a completion interrupt is generated (CH_STATUS.INTR_CAUSE is set to COMPLETION): "0": An interrupt is generated after a single transfer. "1": An interrupt is generated after a single 1D transfer or a memory copy transfer - If the descriptor type is "single", the interrupt is generated after a single transfer. - If the descriptor type is "1D" or "2D", the interrupt is generated after the execution of a 1D transfer. - If the descriptor type is "memory copy", the interrupt is generated after the execution of a memory copy transfer. - If the descriptor type is "scatter" the interrupt is generated after the execution of a scatter transfer. "2": An interrupt is generated after the execution of the current descriptor (independent of the value of DESCR_NEXT_PTR.ADDR of the current descriptor). "3": An interrupt is generated after the execution of the current descriptor and the current descriptor's DESCR_NEXT_PTR.ADDR is "0'. Default Value: Undefined
1 : 0	WAIT_FOR_DEACT	Specifies whether the controller should wait for the input trigger to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controller with the agent that generated the trigger. This field is ONLY used at the completion of the transfer as specified by TR_IN. E.g., a TX FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the controller AND received by the agent. Furthermore, the agent's trigger may be delayed by a few cycles before it reaches the controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW controller performance. "0": Do not wait for trigger de-activation (for pulse sensitive triggers). "1": Wait for up to 4 cycles. "2": Wait for up to 16 cycles. "3": Wait indefinitely. This option may result in controller lockup if the trigger is not de-activated. Default Value: Undefined

12.1.34 DMAC_CH0_DESCR_SRC

Channel descriptor source

Address: 0x402A1064

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. Default Value: Undefined

12.1.35 DMAC_CH0_DESCR_DST

Channel descriptor destination

Address: 0x402A1068

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. Default Value: Undefined

12.1.36 DMAC_CH0_DESCR_X_SIZE

Channel descriptor X size

Address: 0x402A106C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	X_COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	X_COUNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	X_COUNT	Number of iterations (minus 1) of the "X loop" (X_COUNT+1 is the number of single transfers in a 1D transfer). This field is an unsigned number in the range [0, 65535], representing 1 through 65536 iterations. For the "memory copy" descriptor type, (X_COUNT + 1) is the number of transferred Bytes. For the "scatter" descriptor type, ceiling(X_COUNT/2) is the number of (address, write data) initialization pairs processed. Default Value: Undefined

12.1.37 DMAC_CH0_DESCR_X_INCR

Channel descriptor X increment

Address: 0x402A1070

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SRC_X [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SRC_X [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DST_X [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DST_X [31:24]							

Bits	Name	Description
31 : 16	DST_X	Specifies increment of destination address for each X loop iteration (in multiples of DST_TRANSFER_SIZE). This field is a signed number (sign-magnitude format) in the range [-32768, 32767]. If this field is "0", the destination address is not incremented. This is useful for writing to TX FIFO structures. Default Value: Undefined
15 : 0	SRC_X	Specifies increment of source address for each X loop iteration (in multiples of SRC_TRANSFER_SIZE). This field is a signed number (sign-magnitude format) in the range [-32768, 32767]. If this field is "0", the source address is not incremented. This is useful for reading from RX FIFO structures. Default Value: Undefined

12.1.38 DMAC_CH0_DESCR_Y_SIZE

Channel descriptor Y size

Address: 0x402A1074

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	Y_COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	Y_COUNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	Y_COUNT	Number of iterations (minus 1) of the "Y loop" (X_COUNT+1)*(Y_COUNT+1) is the number of single transfers in a 2D transfer). This field is an unsigned number in the range [0, 65535], representing 1 through 65536 iterations. Default Value: Undefined

12.1.39 DMAC_CH0_DESCR_Y_INCR

Channel descriptor Y increment

Address: 0x402A1078

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SRC_Y [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SRC_Y [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DST_Y [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DST_Y [31:24]							

Bits	Name	Description
31 : 16	DST_Y	Specifies increment of destination address for each Y loop iteration (in multiples of DST_TRANSFER_SIZE). This field is a signed number in the range [-32768, 32767]. Default Value: Undefined
15 : 0	SRC_Y	Specifies increment of source address for each Y loop iteration (in multiples of SRC_TRANSFER_SIZE). This field is a signed number in the range [-32768, 32767]. Default Value: Undefined

12.1.40 DMAC_CH0_DESCR_NEXT

Channel descriptor next pointer

Address: 0x402A107C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	PTR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	PTR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	PTR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	PTR [31:24]							

Bits	Name	Description
31 : 2	PTR	Address of next descriptor in descriptor list. When this field is "0", this is the last descriptor in the descriptor list. Default Value: Undefined

12.1.41 DMAC_CH0_INTR

Interrupt

Address: 0x402A1080

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	DE-SCR_BUS_ERROR	AC-TIVE_CH_-DISABLED	CUR-R_PTR_NULL	DST_MIS-AL	SRC_MIS-AL	DST_BUS_ERROR	SRC_BUS_ERROR	COMPLE-TION

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DESCR_BUS_ERROR	Activated (set to '1') on a bus error for a load of the descriptor. Default Value: 0
6	ACTIVE_CH_DISABLED	Activated (set to '1') if the channel is disabled by SW (accidentally/incorrectly) when the data transfer engine is busy. Default Value: 0
5	CURR_PTR_NULL	Activated (set to '1') when the channel is enabled (CH_CTL.ENABLED is '1') and CH_CUR-R_PTR is "0". Default Value: 0
4	DST_MISAL	Activated (set to '1') on a misalignment of the destination address. Default Value: 0
3	SRC_MISAL	Activated (set to '1') on a misalignment of the source address. Default Value: 0
2	DST_BUS_ERROR	Activated (set to '1') on a bus error for a store to the destination. Default Value: 0

12.1.41 DMAC_CH0_INTR (continued)

1	SRC_BUS_ERROR	Activated (set to '1') on a bus error for a load from the source. Default Value: 0
0	COMPLETION	Activated (set to '1') on completion of data transfer(s) as specified by the descriptor's CH_DESCR_CTL.INTR_TYPE. Default Value: 0

12.1.42 DMAC_CH0_INTR_SET

Interrupt set

Address: 0x402A1084

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	DE-SCR_BUS_ERROR	AC-TIVE_CH_-DISABLED	CUR-R_PTR_NULL	DST_MIS-AL	SRC_MIS-AL	DST_BUS_ERROR	SRC_BUS_ERROR	COMPLE-TION

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DESCR_BUS_ERROR	Write this field with '1' to set INTR.DESCR_BUS_ERROR field to '1' (a write of '0' has no effect). Default Value: 0
6	ACTIVE_CH_DISABLED	Write this field with '1' to set INTR.ACT_CH_DISABLED field to '1' (a write of '0' has no effect). Default Value: 0
5	CURR_PTR_NULL	Write this field with '1' to set INTR.CURR_PTR_NULL field to '1' (a write of '0' has no effect). Default Value: 0
4	DST_MISAL	Write this field with '1' to set INTR.DST_MISAL field to '1' (a write of '0' has no effect). Default Value: 0
3	SRC_MISAL	Write this field with '1' to set INTR.SRC_MISAL field to '1' (a write of '0' has no effect). Default Value: 0
2	DST_BUS_ERROR	Write this field with '1' to set INTR.DST_BUS_ERROR field to '1' (a write of '0' has no effect). Default Value: 0
1	SRC_BUS_ERROR	Write this field with '1' to set INTR.SRC_BUS_ERROR field to '1' (a write of '0' has no effect). Default Value: 0

12.1.42 DMAC_CH0_INTR_SET (continued)

0	COMPLETION	Write this field with '1' to set INTR.COMPLETION field to '1' (a write of '0' has no effect). Default Value: 0

12.1.43 DMAC_CH0_INTR_MASK

Interrupt mask

Address: 0x402A1088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	DE-SCR_BUS_ERROR	AC-TIVE_CH_-DISABLED	CUR-R_PTR_NULL	DST_MIS-AL	SRC_MIS-AL	DST_BUS_ERROR	SRC_BUS_ERROR	COMPLE-TION

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DESCR_BUS_ERROR	Mask for INTR.DESCR_BUS_ERROR interrupt. Default Value: 0
6	ACTIVE_CH_DISABLED	Mask for INTR.ACTIVE_CH_DISABLED interrupt. Default Value: 0
5	CURR_PTR_NULL	Mask for INTR.CURR_PTR_NULL interrupt. Default Value: 0
4	DST_MISAL	Mask for INTR.DST_MISAL interrupt. Default Value: 0
3	SRC_MISAL	Mask for INTR.SRC_MISAL interrupt. Default Value: 0
2	DST_BUS_ERROR	Mask for INTR.DST_BUS_ERROR interrupt. Default Value: 0
1	SRC_BUS_ERROR	Mask for INTR.SRC_BUS_ERROR interrupt. Default Value: 0

12.1.43 DMAC_CH0_INTR_MASK (continued)

0	COMPLETION	Mask for INTR.COMPLETION interrupt. Default Value: 0

12.1.44 DMAC_CH0_INTR_MASKED

Interrupt masked

Address: 0x402A108C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	DE-SCR_BUS_ERROR	AC-TIVE_CH_-DISABLED	CUR-R_PTR_NULL	DST_MIS-AL	SRC_MIS-AL	DST_BUS_ERROR	SRC_BUS_ERROR	COMPLE-TION

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DESCR_BUS_ERROR	Logical and of corresponding INTR.DESCR_BUS_ERROR and INTR_MASK.DE-SCR_BUS_ERROR fields. Default Value: 0
6	ACTIVE_CH_DISABLED	Logical and of corresponding INTR.ACTIVE_CH_DISABLED and INTR_MASK.ACTIVE_CH_-DISABLED fields. Default Value: 0
5	CURR_PTR_NULL	Logical and of corresponding INTR.CURR_PTR_NULL and INTR_MASK.CURR_PTR_NULL fields. Default Value: 0
4	DST_MISAL	Logical and of corresponding INTR.DST_MISAL and INTR_MASK.DST_MISAL fields. Default Value: 0
3	SRC_MISAL	Logical and of corresponding INTR.SRC_MISAL and INTR_MASK.SRC_MISAL fields. Default Value: 0
2	DST_BUS_ERROR	Logical and of corresponding INTR.DST_BUS_ERROR and INTR_MASK.DST_BUS_ERROR fields. Default Value: 0

12.1.44 DMAC_CH0_INTR_MASKED (continued)

1	SRC_BUS_ERROR	Logical and of corresponding INTR.SRC_BUS_ERROR and INTR_MASK.SRC_BUS_ERROR fields. Default Value: 0
0	COMPLETION	Logical and of corresponding INTR.COMPLETION and INTR_MASK.COMPLETION fields. Default Value: 0

13 eFuse Registers

This section discusses the eFuse registers. It lists all the registers in mapping tables, in address order.

13.1 Register Details

Register	Address	Description
EFUSE_DATA_DEAD_ACCESS_RESTRICT0	0x402C0827	Access restrictions for DEAD life cycle stage
EFUSE_DATA_DEAD_ACCESS_RESTRICT1	0x402C0828	Access restrictions for DEAD life cycle stage
EFUSE_DATA_SECURE_ACCESS_RESTRICT0	0x402C0829	Access restrictions for SECURE life cycle stage
EFUSE_DATA_SECURE_ACCESS_RESTRICT1	0x402C082A	Access restrictions for SECURE life cycle stage
EFUSE_DATA_LIFECYCLE_STAGE	0x402C082B	NORMAL, SECURE_WITH_DEBUG, SECURE, and RMA fuse bits
EFUSE_DATA_CUSTOMER_DATA0	0x402C0851	Customer data. This is the starting address of a register bank containing 47 registers (EFUSE_DATA_CUSTOMER_DATA0 to EFUSE_DATA_CUSTOMER_DATA46).

13.1.1 EFUSE_DATA_DEAD_ACCESS_RESTRICT0

Access restrictions for DEAD life cycle stage

Address: 0x402C0827

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	MMIO_ALLOWED [7:6]		SFLASH_ALLOWED [5:4]		SYS-_AP_M-PU_ENABLE	SYS_DIS-ABLE	CM4_DIS-ABLE	CM0_DIS-ABLE

Bits	Name	Description
7 : 6	MMIO_ALLOWED	This field indicates what portion of the MMIO region is accessible through the system debug access port. Encoding is as follows: "0": All MMIO registers "1": Only IPC MMIO registers accessible (system calls) "2", "3": No MMIO access Default Value: 0
5 : 4	SFLASH_ALLOWED	This field indicates what portion of Supervisory Flash is accessible through the system debug access port. Only a portion of Supervisory Flash starting at the bottom of the area is exposed. Encoding is as follows: "0": entire region "1": 1/2 "2": 1/4th "3": nothing Default Value: 0
3	SYS_AP_MPU_ENABLE	Indicates that the MPU on the system debug access port must be programmed and locked according to the settings in the next 5 fields. Default Value: 0
2	SYS_DISABLE	Indicates that this device does not allow access to the system debug access port (DAP). Default Value: 0
1	CM4_DISABLE	Indicates that this device does not allow access to the M4 debug access port (DAP). Default Value: 0
0	CM0_DISABLE	Indicates that this device does not allow access to the M0+ debug access port (DAP). Default Value: 0

13.1.2 EFUSE_DATA_DEAD_ACCESS_RESTRICT1

Access restrictions for DEAD life cycle stage

Address: 0x402C0828

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW			RW		
HW Access	R	R	R			R		
Name	DIRECT_EXECUTE_DISABLE	UNUSED	SRAM_ALLOWED [5:3]			FLASH_ALLOWED [2:0]		

Bits	Name	Description
7	DIRECT_EXECUTE_DISABLE	Disables DirectExecute system call functionality (implemented in software). Default Value: 0
6	UNUSED	UNUSED Default Value: 0
5 : 3	SRAM_ALLOWED	This field indicates what portion of SRAM 0 is accessible through the system access port. Only a portion of SRAM starting at the bottom of the area is exposed. Encoding is the same as FLASH_ALLOWED. Default Value: 0
2 : 0	FLASH_ALLOWED	This field indicates what portion of Main Flash is accessible through the system debug access port. Only a portion of Main Flash starting at the bottom of the area is exposed. Encoding is as follows: "0": entire region "1": 7/8th "2": 3/4th "3": 1/2 "4": 1/4th "5": 1/8th "6": 1/16th "7": nothing Default Value: 0

13.1.3 EFUSE_DATA_SECURE_ACCESS_RESTRICT0

Access restrictions for SECURE life cycle stage

Address: 0x402C0829

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	MMIO_ALLOWED [7:6]		SFLASH_ALLOWED [5:4]		SYS-_AP_M-PU_ENABLE	SYS_DIS-ABLE	CM4_DIS-ABLE	CM0_DIS-ABLE

Bits	Name	Description
7 : 6	MMIO_ALLOWED	This field indicates what portion of the MMIO region is accessible through the system debug access port. Encoding is as follows: "0": All MMIO registers "1": Only IPC MMIO registers accessible (system calls) "2", "3": No MMIO access Default Value: 0
5 : 4	SFLASH_ALLOWED	This field indicates what portion of Supervisory Flash is accessible through the system debug access port. Only a portion of Supervisory Flash starting at the bottom of the area is exposed. Encoding is as follows: "0": entire region "1": 1/2 "2": 1/4th "3": nothing Default Value: 0
3	SYS_AP_MPU_ENABLE	Indicates that the MPU on the system debug access port must be programmed and locked according to the settings in the next 5 fields. Default Value: 0
2	SYS_DISABLE	Indicates that this device does not allow access to the system debug access port (DAP). Default Value: 0
1	CM4_DISABLE	Indicates that this device does not allow access to the M4 debug access port (DAP). Default Value: 0
0	CM0_DISABLE	Indicates that this device does not allow access to the M0+ debug access port (DAP). Default Value: 0

13.1.4 EFUSE_DATA_SECURE_ACCESS_RESTRICT1

Access restrictions for SECURE life cycle stage

Address: 0x402C082A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW			RW		
HW Access	R	R	R			R		
Name	DIRECT_EXECUTE_DISABLE	UNUSED	SRAM_ALLOWED [5:3]			FLASH_ALLOWED [2:0]		

Bits	Name	Description
7	DIRECT_EXECUTE_DISABLE	Disables DirectExecute system call functionality (implemented in software). Default Value: 0
6	UNUSED	UNUSED Default Value: 0
5 : 3	SRAM_ALLOWED	This field indicates what portion of SRAM 0 is accessible through the system debug access port. Only a portion of SRAM starting at the bottom of the area is exposed. Encoding is the same as FLASH_ALLOWED. Default Value: 0
2 : 0	FLASH_ALLOWED	This field indicates what portion of Main Flash is accessible through the system debug access port. Only a portion of Main Flash starting at the bottom of the area is exposed. Encoding is as follows: "0": entire region "1": 7/8th "2": 3/4th "3": 1/2 "4": 1/4th "5": 1/8th "6": 1/16th "7": nothing Default Value: 0

13.1.5 EFUSE_DATA_LIFECYCLE_STAGE

NORMAL, SECURE_WITH_DEBUG, SECURE, and RMA fuse bits

Address: 0x402C082B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				RMA	SECURE	SECURE_WITH_DEBUG	NORMAL

Bits	Name	Description
3	RMA	This life cycle stage allows one to perform Failure Analysis (FA). The customer transitions the part to RMA life cycle stage when the customer wants Cypress to perform failure analysis on the part. The customer erases all the sensitive data prior to invoking the system call that transitions the part to RMA. Default Value: 0
2	SECURE	This is the life cycle stage of a secure device. Prior to transitioning to this stage, the SECURE_HASH must have been programmed in eFuse and valid application code must have been programmed in the Main Flash Default Value: 0
1	SECURE_WITH_DEBUG	This is same as SECURE life cycle stage, except the device allows for debugging. Prior to transitioning to this stage, the SECURE_HASH must have been programmed in eFuse and valid application code must have been programmed in the Main Flash. Default Value: 0
0	NORMAL	This is the life cycle stage of a device after trimming and testing is complete in the factory. All configuration and trimming information is complete. Valid FLASH boot code has been programmed in the Supervisory Flash. Default Value: 0

13.1.6 EFUSE_DATA_CUSTOMER_DATA0

Customer data

Address: 0x402C0851

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CUSTOMER_USE [7:0]							

Bits	Name	Description
7 : 0	CUSTOMER_USE	Fuses left over are available for customer use. Default Value: 0

Section E: Peripheral Group 3

This section encompasses the following chapter:

- High Speed IO Matrix Registers chapter on page 1132
- General Purpose I/O Registers chapter on page 1153
- Smart I/O Registers chapter on page 1330
- Low-Power Comparator Registers chapter on page 1342
- Timer, Counter, PWM Registers chapter on page 1357
- Segment LCD Drive Registers chapter on page 1429
- USB Registers chapter on page 1437

14 High Speed IO Matrix Registers

This section discusses the High-Speed I/O Matrix (HSIOM) registers. It lists all the registers in mapping tables, in address order.

14.1 Register Details

Register	Address	Description
HSIOM_PRT0_PORT_SEL0	0x40300000	Port selection 0
HSIOM_PRT0_PORT_SEL1	0x40300004	Port selection 1
HSIOM_PRT1_PORT_SEL0	0x40300010	Port selection 0
HSIOM_PRT2_PORT_SEL0	0x40300020	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT2_PORT_SEL1	0x40300024	Port selection 1
HSIOM_PRT3_PORT_SEL0	0x40300030	Port selection 0
HSIOM_PRT5_PORT_SEL0	0x40300050	Port selection 0. See HSIOM_PRT1_PORT_SEL0 for the details of bit fields.
HSIOM_PRT5_PORT_SEL1	0x40300054	Port selection 1
HSIOM_PRT6_PORT_SEL0	0x40300060	Port selection 0
HSIOM_PRT6_PORT_SEL1	0x40300064	Port selection 1. See HSIOM_PRT2_PORT_SEL1 for the details of bit fields.
HSIOM_PRT7_PORT_SEL0	0x40300070	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT7_PORT_SEL1	0x40300074	Port selection 1
HSIOM_PRT8_PORT_SEL0	0x40300080	Port selection 0. See HSIOM_PRT3_PORT_SEL0 for the details of bit fields.
HSIOM_PRT9_PORT_SEL0	0x40300090	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT9_PORT_SEL1	0x40300094	Port selection 1. See HSIOM_PRT0_PORT_SEL1 for the details of bit fields.
HSIOM_PRT10_PORT_SEL0	0x403000A0	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT10_PORT_SEL1	0x403000A4	Port selection 1. See HSIOM_PRT2_PORT_SEL1 for the details of bit fields.
HSIOM_PRT11_PORT_SEL0	0x403000B0	Port selection 0
HSIOM_PRT11_PORT_SEL1	0x403000B4	Port selection 1. See HSIOM_PRT2_PORT_SEL1 for the details of bit fields.
HSIOM_PRT12_PORT_SEL1	0x403000C4	Port selection 1. See HSIOM_PRT5_PORT_SEL1 for the details of bit fields.
HSIOM_PRT14_PORT_SEL0	0x403000E0	Port selection 0. See HSIOM_PRT3_PORT_SEL0 for the details of bit fields.
HSIOM_AMUX_SPLIT_CTL0	0x40302000	AMUX splitter cell control
HSIOM_AMUX_SPLIT_CTL1	0x40302004	AMUX splitter cell control. See HSIOM_AMUX_SPLIT_CTL0 for the details of bit fields.
HSIOM_AMUX_SPLIT_CTL2	0x40302008	AMUX splitter cell control. See HSIOM_AMUX_SPLIT_CTL0 for the details of bit fields.
HSIOM_AMUX_SPLIT_CTL3	0x4030200C	AMUX splitter cell control. See HSIOM_AMUX_SPLIT_CTL0 for the details of bit fields.
HSIOM_AMUX_SPLIT_CTL4	0x40302010	AMUX splitter cell control. See HSIOM_AMUX_SPLIT_CTL0 for the details of bit fields.

Register	Address	Description
HSIOM_AMUX_SPLIT_CTL5	0x40302014	AMUX splitter cell control. See HSIOM_AMUX_SPLIT_CTL0 for the details of bit fields.

14.1.1 HSIOM_PRT0_PORT_SEL0

Port selection 0

Address: 0x40300000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			RW				
Name	None [7:5]			IO0_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			RW				
Name	None [15:13]			IO1_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			RW				
Name	None [23:21]			IO2_SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			RW				
Name	None [31:29]			IO3_SEL [28:24]				

Bits	Name	Description
28 : 24	IO3_SEL	Selects the peripheral connections of Pin 3. Default Value: 0
20 : 16	IO2_SEL	Selects the peripheral connections of Pin 2. Default Value: 0
12 : 8	IO1_SEL	Selects the peripheral connections of Pin 1. Default Value: 0
4 : 0	IO0_SEL	Selects the peripheral connections of Pin 0. Note that available connectivity options vary depending on the device, port and the pin. See the device Datasheet for a list of peripheral connections available at each pin. Default Value: 0 **0x0: GPIO :** GPIO controls "out" **0x1: GPIO_DSI :** GPIO controls "out", DSI controls "output enable"

14.1.1 HSIOM_PRT0_PORT_SEL0 (continued)

0x2: DSI_DSI :
DSI controls "out" and "output enable"

0x3: DSI_GPIO :
DSI controls "out", GPIO controls "output enable"

0x4: AMUXA :
AMUXBUS A

0x5: AMUXB :
AMUXBUS B

0x6: AMUXA_DSI :
Analog mux bus A, DSI control

0x7: AMUXB_DSI :
Analog mux bus B, DSI control

0x8: ACT_0 :
Active peripheral 0

0x9: ACT_1 :
Active peripheral 1

0xa: ACT_2 :
Active peripheral 2

0xb: ACT_3 :
Active peripheral 3

0xc: DS_0 :
Deep Sleep peripheral 0

0xd: DS_1 :
Deep Sleep peripheral 1

0xe: DS_2 :
Deep Sleep peripheral 2

0xf: DS_3 :
Deep Sleep peripheral 3

0x10: ACT_4 :
Active peripheral 4

0x11: ACT_5 :
Active peripheral 5

0x12: ACT_6 :
Active peripheral 6

0x13: ACT_7 :
Active peripheral 7

0x14: ACT_8 :
Active peripheral 8

0x15: ACT_9 :
Active peripheral 9

0x16: ACT_10 :
Active peripheral 10

0x17: ACT_11 :
Active peripheral 11

14.1.1 HSIOM_PRT0_PORT_SEL0 (continued)

0x18: ACT_12 :
Active peripheral 12

0x19: ACT_13 :
Active peripheral 13

0x1a: ACT_14 :
Active peripheral 14

0x1b: ACT_15 :
Active peripheral 15

0x1c: DS_4 :
Deep Sleep peripheral 4

0x1d: DS_5 :
Deep Sleep peripheral 5

0x1e: DS_6 :
Deep Sleep peripheral 6

0x1f: DS_7 :
Deep Sleep peripheral 7

14.1.2 HSIOM_PRT0_PORT_SEL1 (continued)

14.1.2 HSIOM_PRT0_PORT_SEL1

Port selection 1

Address: 0x40300004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			RW				
Name	None [7:5]			IO4_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			RW				
Name	None [15:13]			IO5_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12 : 8	IO5_SEL	Selects the peripheral connections of Pin 4. Default Value: 0
4 : 0	IO4_SEL	Selects the peripheral connections of Pin 4. See PORT_SEL0 for connection details. Default Value: 0

14.1.3 HSIOM_PRT1_PORT_SEL0

Port selection 0

Address: 0x40300010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			RW				
Name	None [7:5]			IO0_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			RW				
Name	None [15:13]			IO1_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			RW				
Name	None [23:21]			IO2_SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 16	IO2_SEL	Selects the peripheral connections of Pin 2. Default Value: 0
12 : 8	IO1_SEL	Selects the peripheral connections of Pin 1. Default Value: 0
4 : 0	IO0_SEL	Selects the peripheral connections of Pin 0. Note that available connectivity options vary depending on the device, port and the pin. See the device Datasheet for a list of peripheral connections available at each pin. Default Value: 0 **0x0: GPIO :** GPIO controls "out" **0x1: GPIO_DSI :** GPIO controls "out", DSI controls "output enable"

14.1.3 HSIOM_PRT1_PORT_SEL0 (continued)

0x2: DSI_DSI :

DSI controls "out" and "output enable"

0x3: DSI_GPIO :

DSI controls "out", GPIO controls "output enable"

0x4: AMUXA :

AMUXBUS A

0x5: AMUXB :

AMUXBUS B

0x6: AMUXA_DSI :

Analog mux bus A, DSI control

0x7: AMUXB_DSI :

Analog mux bus B, DSI control

0x8: ACT_0 :

Active peripheral 0

0x9: ACT_1 :

Active peripheral 1

0xa: ACT_2 :

Active peripheral 2

0xb: ACT_3 :

Active peripheral 3

0xc: DS_0 :

Deep Sleep peripheral 0

0xd: DS_1 :

Deep Sleep peripheral 1

14.1.3 HSIOM_PRT1_PORT_SEL0 (continued)

0xe: DS_2 :

Deep Sleep peripheral 2

0xf: DS_3 :

Deep Sleep peripheral 3

0x10: ACT_4 :

Active peripheral 4

0x11: ACT_5 :

Active peripheral 5

0x12: ACT_6 :

Active peripheral 6

0x13: ACT_7 :

Active peripheral 7

0x14: ACT_8 :

Active peripheral 8

0x15: ACT_9 :

Active peripheral 9

0x16: ACT_10 :

Active peripheral 10

0x17: ACT_11 :

Active peripheral 11

0x18: ACT_12 :

Active peripheral 12

0x19: ACT_13 :

Active peripheral 13

14.1.3 HSIOM_PRT1_PORT_SEL0 (continued)

0x1a: ACT_14 :

Active peripheral 14

0x1b: ACT_15 :

Active peripheral 15

0x1c: DS_4 :

Deep Sleep peripheral 4

0x1d: DS_5 :

Deep Sleep peripheral 5

0x1e: DS_6 :

Deep Sleep peripheral 6

0x1f: DS_7 :

Deep Sleep peripheral 7

14.1.4 HSIOM_PRT2_PORT_SEL1 (continued)

14.1.4 HSIOM_PRT2_PORT_SEL1

Port selection 1

Address: 0x40300024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			RW				
Name	None [7:5]			IO4_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			RW				
Name	None [15:13]			IO5_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			RW				
Name	None [23:21]			IO6_SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			RW				
Name	None [31:29]			IO7_SEL [28:24]				

Bits	Name	Description
28 : 24	IO7_SEL	Selects the peripheral connections of Pin 6. Default Value: 0
20 : 16	IO6_SEL	Selects the peripheral connections of Pin 5. Default Value: 0
12 : 8	IO5_SEL	Selects the peripheral connections of Pin 4. Default Value: 0
4 : 0	IO4_SEL	Selects the peripheral connections of Pin 4. See PORT_SEL0 for connection details. Default Value: 0

14.1.5 HSIOM_PRT3_PORT_SEL0

Port selection 0

Address: 0x40300030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			RW				
Name	None [7:5]			IO0_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			RW				
Name	None [15:13]			IO1_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12 : 8	IO1_SEL	Selects the peripheral connections of Pin 1. Default Value: 0
4 : 0	IO0_SEL	Selects the peripheral connections of Pin 0. Note that available connectivity options vary depending on the device, port and the pin. See the device Datasheet for a list of peripheral connections available at each pin. Default Value: 0 **0x0: GPIO :** GPIO controls "out" **0x1: GPIO_DSI :** GPIO controls "out", DSI controls "output enable" **0x2: DSI_DSI :** DSI controls "out" and "output enable"

14.1.5 HSIOM_PRT3_PORT_SEL0 (continued)

0x3: DSI_GPIO :

DSI controls "out", GPIO controls "output enable"

0x4: AMUXA :

AMUXBUS A

0x5: AMUXB :

AMUXBUS B

0x6: AMUXA_DSI :

Analog mux bus A, DSI control

0x7: AMUXB_DSI :

Analog mux bus B, DSI control

0x8: ACT_0 :

Active peripheral 0

0x9: ACT_1 :

Active peripheral 1

0xa: ACT_2 :

Active peripheral 2

0xb: ACT_3 :

Active peripheral 3

0xc: DS_0 :

Deep Sleep peripheral 0

0xd: DS_1 :

Deep Sleep peripheral 1

0xe: DS_2 :

Deep Sleep peripheral 2

14.1.5 HSIOM_PRT3_PORT_SEL0 (continued)

0xf: DS_3 :

Deep Sleep peripheral 3

0x10: ACT_4 :

Active peripheral 4

0x11: ACT_5 :

Active peripheral 5

0x12: ACT_6 :

Active peripheral 6

0x13: ACT_7 :

Active peripheral 7

0x14: ACT_8 :

Active peripheral 8

0x15: ACT_9 :

Active peripheral 9

0x16: ACT_10 :

Active peripheral 10

0x17: ACT_11 :

Active peripheral 11

0x18: ACT_12 :

Active peripheral 12

0x19: ACT_13 :

Active peripheral 13

0x1a: ACT_14 :

Active peripheral 14

14.1.5 HSIOM_PRT3_PORT_SEL0 (continued)

0x1b: ACT_15 :

Active peripheral 15

0x1c: DS_4 :

Deep Sleep peripheral 4

0x1d: DS_5 :

Deep Sleep peripheral 5

0x1e: DS_6 :

Deep Sleep peripheral 6

0x1f: DS_7 :

Deep Sleep peripheral 7

14.1.6 HSIOM_PRT5_PORT_SEL1 (continued)

14.1.6 HSIOM_PRT5_PORT_SEL1

Port selection 1

Address: 0x40300054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			RW				
Name	None [23:21]			IO6_SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			RW				
Name	None [31:29]			IO7_SEL [28:24]				

Bits	Name	Description
28 : 24	IO7_SEL	Selects the peripheral connections of Pin 6. Default Value: 0
20 : 16	IO6_SEL	Selects the peripheral connections of Pin 5. Default Value: 0

14.1.7 HSIOM_PRT6_PORT_SEL0

Port selection 0

Address: 0x40300060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			RW				
Name	None [23:21]			IO2_SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			RW				
Name	None [31:29]			IO3_SEL [28:24]				

Bits	Name	Description
28 : 24	IO3_SEL	Selects the peripheral connections of Pin 3. Default Value: 0
20 : 16	IO2_SEL	Selects the peripheral connections of Pin 2. Default Value: 0

14.1.8 HSIOM_PRT7_PORT_SEL1

Port selection 1

Address: 0x40300074

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			RW				
Name	None [7:5]			IO4_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			RW				
Name	None [15:13]			IO5_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			RW				
Name	None [31:29]			IO7_SEL [28:24]				

Bits	Name	Description
28 : 24	IO7_SEL	Selects the peripheral connections of Pin 6. Default Value: 0
12 : 8	IO5_SEL	Selects the peripheral connections of Pin 4. Default Value: 0
4 : 0	IO4_SEL	Selects the peripheral connections of Pin 4. See PORT_SEL0 for connection details. Default Value: 0

14.1.9 HSIOM_PRT11_PORT_SEL0

Port selection 0

Address: 0x403000B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			RW				
Name	None [15:13]			IO1_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			RW				
Name	None [23:21]			IO2_SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			RW				
Name	None [31:29]			IO3_SEL [28:24]				

Bits	Name	Description
28 : 24	IO3_SEL	Selects the peripheral connections of Pin 3. Default Value: 0
20 : 16	IO2_SEL	Selects the peripheral connections of Pin 2. Default Value: 0
12 : 8	IO1_SEL	Selects the peripheral connections of Pin 1. Default Value: 0

14.1.10 HSIOM_AMUX_SPLIT_CTL0

AMUX splitter cell control

Address: 0x40302000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW	RW	RW
HW Access	None	R	R	R	None	R	R	R
Name	None	SWITCH_B-B_S0	SWITCH_B-B_SR	SWITCH_B-B_SL	None	SWITCH_AA_S0	SWITCH_AA_SR	SWITCH_AA_SL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6	SWITCH_BB_S0	T-switch control for AMUXBUSB vssa/ground switch. Default Value: 0
5	SWITCH_BB_SR	T-switch control for Right AMUXBUSB switch. Default Value: 0
4	SWITCH_BB_SL	T-switch control for Left AMUXBUSB switch. Default Value: 0
2	SWITCH_AA_S0	T-switch control for AMUXBUSA vssa/ground switch: '0': switch open. '1': switch closed. Default Value: 0
1	SWITCH_AA_SR	T-switch control for Right AMUXBUSA switch: '0': switch open. '1': switch closed. Default Value: 0

14.1.10 HSIOM_AMUX_SPLIT_CTL0 (continued)

0	SWITCH_AA_SL	T-switch control for Left AMUXBUSA switch: '0': switch open. '1': switch closed. Default Value: 0

15 General Purpose I/O Registers

This section discusses the General Purpose I/O (GPIO) registers. It lists all the registers in mapping tables, in address order.

15.1 Register Details

Register	Address	Description
GPIO_PRT0_OUT	0x40310000	Port output data register
GPIO_PRT0_OUT_CLR	0x40310004	Port output data clear register
GPIO_PRT0_OUT_SET	0x40310008	Port output data set register
GPIO_PRT0_OUT_INV	0x4031000C	Port output data invert register
GPIO_PRT0_IN	0x40310010	Port input state register
GPIO_PRT0_INTR	0x40310014	Port interrupt status register
GPIO_PRT0_INTR_MASK	0x40310018	Port interrupt mask register
GPIO_PRT0_INTR_MASKED	0x4031001C	Port interrupt masked status register
GPIO_PRT0_INTR_SET	0x40310020	Port interrupt set register
GPIO_PRT0_INTR_CFG	0x40310040	Port interrupt configuration register
GPIO_PRT0_CFG	0x40310044	Port configuration register
GPIO_PRT0_CFG_IN	0x40310048	Port input buffer configuration register
GPIO_PRT0_CFG_OUT	0x4031004C	Port output buffer configuration register
GPIO_PRT1_OUT	0x40310080	Port output data register
GPIO_PRT1_OUT_CLR	0x40310084	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT1_OUT_SET	0x40310088	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT1_OUT_INV	0x4031008C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT1_IN	0x40310090	Port input state register
GPIO_PRT1_INTR	0x40310094	Port interrupt status register
GPIO_PRT1_INTR_MASK	0x40310098	Port interrupt mask register
GPIO_PRT1_INTR_MASKED	0x4031009C	Port interrupt masked status register
GPIO_PRT1_INTR_SET	0x403100A0	Port interrupt set register
GPIO_PRT1_INTR_CFG	0x403100C0	Port interrupt configuration register
GPIO_PRT1_CFG	0x403100C4	Port configuration register
GPIO_PRT1_CFG_IN	0x403100C8	Port input buffer configuration register
GPIO_PRT1_CFG_OUT	0x403100CC	Port output buffer configuration register
GPIO_PRT2_OUT	0x40310100	Port output data register

Register	Address	Description
GPIO_PRT1_OUT_CLR	0x40310104	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT1_OUT_SET	0x40310108	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT1_OUT_INV	0x4031010C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT2_IN	0x40310110	Port input state register
GPIO_PRT2_INTR	0x40310114	Port interrupt status register
GPIO_PRT2_INTR_MASK	0x40310118	Port interrupt mask register
GPIO_PRT2_INTR_MASKED	0x4031011C	Port interrupt masked status register
GPIO_PRT2_INTR_SET	0x40310120	Port interrupt set register
GPIO_PRT2_INTR_CFG	0x40310140	Port interrupt configuration register
GPIO_PRT2_CFG	0x40310144	Port configuration register
GPIO_PRT2_CFG_IN	0x40310148	Port input buffer configuration register
GPIO_PRT2_CFG_OUT	0x4031014C	Port output buffer configuration register
GPIO_PRT3_OUT	0x40310180	Port output data register
GPIO_PRT3_OUT_CLR	0x40310184	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT3_OUT_SET	0x40310188	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT3_OUT_INV	0x4031018C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT3_IN	0x40310190	Port input state register
GPIO_PRT3_INTR	0x40310194	Port interrupt status register
GPIO_PRT3_INTR_MASK	0x40310198	Port interrupt mask register
GPIO_PRT3_INTR_MASKED	0x4031019C	Port interrupt masked status register
GPIO_PRT3_INTR_SET	0x403101A0	Port interrupt set register
GPIO_PRT3_CFG	0x403101C0	Port interrupt configuration register
GPIO_PRT3_CFG	0x403101C4	Port configuration register
GPIO_PRT3_CFG_IN	0x403101C8	Port input buffer configuration register
GPIO_PRT3_CFG_OUT	0x403101CC	Port output buffer configuration register
GPIO_PRT4_OUT_CLR	0x40310204	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT4_OUT_SET	0x40310208	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT4_OUT_INV	0x4031020C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT4_IN	0x40310210	Port input state register
GPIO_PRT4_INTRTR	0x40310214	Port interrupt status register
GPIO_PRT4_INTR_MASK	0x40310218	Port interrupt mask register
GPIO_PRT4_INTR_MASKED	0x4031021C	Port interrupt masked status register
GPIO_PRT4_INTR_SET	0x40310220	Port interrupt set register
GPIO_PRT4_INTR_CFG	0x40310240	Port interrupt configuration register
GPIO_PRT5_OUT	0x40310280	Port output data register
GPIO_PRT5_OUT_CLR	0x40310284	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT5_OUT_SET	0x40310288	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT5_OUT_INV	0x4031028C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT5_IN	0x40310290	Port input state register
GPIO_PRT5_INTR	0x40310294	Port interrupt status register
GPIO_PRT5_INTR_MASK	0x40310298	Port interrupt mask register
GPIO_PRT5_INTR_MASKED	0x4031029C	Port interrupt masked status register

Register	Address	Description
GPIO_PRT5_INTR_SET	0x403102A0	Port interrupt set register
GPIO_PRT5_INTR_CFG	0x403102C0	Port interrupt configuration register
GPIO_PRT5_CFG	0x403102C4	Port configuration register
GPIO_PRT6_IN	0x403102C8	Port input buffer configuration register
GPIO_PRT5_CFG_OUT	0x403102CC	Port output buffer configuration register
GPIO_PRT6_OUT	0x40310300	Port output data register
GPIO_PRT6_OUT_CLR	0x40310304	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT6_OUT_SET	0x40310308	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT6_OUT_INV	0x4031030C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT6_IN	0x40310310	Port input state register
GPIO_PRT6_INTR	0x40310314	Port interrupt status register
GPIO_PRT6_INTR_MASK	0x40310318	Port interrupt mask register
GPIO_PRT6_INTR_MASKED	0x4031031C	Port interrupt masked status register
GPIO_PRT6_INTR_SET	0x40310320	Port interrupt set register
GPIO_PRT6_INTR_CFG	0x40310340	Port interrupt configuration register
GPIO_PRT6_CFG	0x40310344	Port configuration register
GPIO_PRT6_CFG_IN	0x40310348	Port input buffer configuration register
GPIO_PRT6_CFG_OUT	0x4031034C	Port output buffer configuration register
GPIO_PRT7_OUT	0x40310380	Port output data register
GPIO_PRT7_OUT_CLR	0x40310384	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT7_OUT_SET	0x40310388	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT7_OUT_INV	0x4031038C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT7_IN	0x40310390	Port input state register
GPIO_PRT7_INTR	0x40310394	Port interrupt status register
GPIO_PRT7_INTR_MASK	0x40310398	Port interrupt mask register
GPIO_PRT7_INTR_MASKED	0x4031039C	Port interrupt masked status register
GPIO_PRT7_INTR_SET	0x403103A0	Port interrupt set register
GPIO_PRT7_INTR_CFG	0x403103C0	Port interrupt configuration register
GPIO_PRT7_CFG	0x403103C4	Port configuration register
GPIO_PRT7_CFG_IN	0x403103C8	Port input buffer configuration register
GPIO_PRT7_CFG_OUT	0x403103CC	Port output buffer configuration register
GPIO_PRT8_OUT	0x40310400	Port output data register. See GPIO_PRT3_OUT for the details of bit fields.
GPIO_PRT8_OUT_CLR	0x40310404	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT8_OUT_SET	0x40310408	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT8_OUT_INV	0x4031040C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT8_IN	0x40310410	Port input state register. See GPIO_PRT3_IN for the details of bit fields.
GPIO_PRT8_INTR	0x40310414	Port interrupt status register. See GPIO_PRT3_INTR for the details of bit fields.
GPIO_PRT8_INTR_MASK	0x40310418	Port interrupt mask register. See GPIO_PRT3_INTR_MASK for the details of bit fields.
GPIO_PRT8_INTR_MASKED	0x4031041C	Port interrupt masked status register. See GPIO_PRT3_INTR_MASKED for the details of bit fields.
GPIO_PRT8_INTR_SET	0x40310420	Port interrupt set register. See GPIO_PRT3_INTR_SET for the details of bit fields.
GPIO_PRT8_INTR_CFG	0x40310440	Port interrupt configuration register. See GPIO_PRT3_INTR_CFG for the details of bit fields.
GPIO_PRT8_CFG	0x40310444	Port configuration register. See GPIO_PRT3_CFG for the details of bit fields.

Register	Address	Description
GPIO_PRT8_CFG_IN	0x40310448	Port input buffer configuration register. See GPIO_PRT3_CFG_IN for the details of bit fields.
GPIO_PRT8_CFG_OUT	0x4031044C	Port output buffer configuration register. See GPIO_PRT3_CFG_OUT for the details of bit fields.
GPIO_PRT9_OUT	0x40310480	Port output data register. See GPIO_PRT0_OUT for the details of bit fields.
GPIO_PRT9_OUT_CLR	0x40310484	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT9_OUT_SET	0x40310488	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT9_OUT_INV	0x4031048C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT9_IN	0x40310490	Port input state register. See GPIO_PRT3_IN for the details of bit fields.
GPIO_PRT9_INTR	0x40310494	Port interrupt status register. See GPIO_PRT3_INTR for the details of bit fields.
GPIO_PRT9_INTR_MASK	0x40310498	Port interrupt mask register. See GPIO_PRT3_INTR_MASK for the details of bit fields.
GPIO_PRT9_INTR_MASKED	0x4031049C	Port interrupt masked status register. See GPIO_PRT3_INTR_MASKED for the details of bit fields.
GPIO_PRT9_INTR_SET	0x403104A0	Port interrupt set register. See GPIO_PRT3_INTR_SET for the details of bit fields.
GPIO_PRT9_INTR_CFG	0x403104C0	Port interrupt configuration register. See GPIO_PRT3_INTR_CFG for the details of bit fields.
GPIO_PRT9_CFG	0x403104C4	Port configuration register. See GPIO_PRT3_CFG for the details of bit fields.
GPIO_PRT9_CFG_IN	0x403104C8	Port input buffer configuration register. See GPIO_PRT3_CFG_IN for the details of bit fields.
GPIO_PRT9_CFG_OUT	0x403104CC	Port output buffer configuration register. See GPIO_PRT3_CFG_OUT for the details of bit fields.
GPIO_PRT10_OUT	0x40310500	Port output data register. See GPIO_PRT2_OUT for the details of bit fields.
GPIO_PRT10_OUT_CLR	0x40310504	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT10_OUT_SET	0x40310508	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT10_OUT_INV	0x4031050C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT10_IN	0x40310510	Port input state register. See GPIO_PRT3_IN for the details of bit fields.
GPIO_PRT10_INTR	0x40310514	Port interrupt status register. See GPIO_PRT3_INTR for the details of bit fields.
GPIO_PRT10_INTR_MASK	0x40310518	Port interrupt mask register. See GPIO_PRT3_INTR_MASK for the details of bit fields.
GPIO_PRT10_INTR_MASKED	0x4031051C	Port interrupt masked status register. See GPIO_PRT3_INTR_MASKED for the details of bit fields.
GPIO_PRT10_INTR_SET	0x40310520	Port interrupt set register. See GPIO_PRT3_INTR_SET for the details of bit fields.
GPIO_PRT10_INTR_CFG	0x40310540	Port interrupt configuration register. See GPIO_PRT3_INTR_CFG for the details of bit fields.
GPIO_PRT10_CFG	0x40310544	Port configuration register. See GPIO_PRT3_CFG for the details of bit fields.
GPIO_PRT10_CFG_IN	0x40310548	Port input buffer configuration register. See GPIO_PRT3_CFG_IN for the details of bit fields.
GPIO_PRT10_CFG_OUT	0x4031054C	Port output buffer configuration register. See GPIO_PRT3_CFG_OUT for the details of bit fields.
GPIO_PRT11_OUT	0x40310580	Port output data register
GPIO_PRT11_OUT_CLR	0x40310584	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT11_OUT_SET	0x40310588	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT11_OUT_INV	0x4031058C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT11_IN	0x40310590	Port input state register
GPIO_PRT11_INTR	0x40310594	Port interrupt status register
GPIO_PRT11_INTR_MASK	0x40310598	Port interrupt mask register
GPIO_PRT11_INTR_MASKED	0x4031059C	Port interrupt masked status register
GPIO_PRT11_INTR_SET	0x403105A0	Port interrupt set register
GPIO_PRT11_INTR_CFG	0x403105C0	Port interrupt configuration register
GPIO_PRT11_CFG	0x403105C4	Port configuration register
GPIO_PRT11_CFG_IN	0x403105C8	Port input buffer configuration register
GPIO_PRT11_CFG_OUT	0x403105CC	Port output buffer configuration register
GPIO_PRT12_OUT	0x40310600	Port output data register

Register	Address	Description
GPIO_PRT12_OUT_CLR	0x40310604	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT12_OUT_SET	0x40310608	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT12_OUT_INV	0x4031060C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT12_IN	0x40310610	Port input state register
GPIO_PRT12_INTR	0x40310614	Port interrupt status register
GPIO_PRT12_INTR_MASK	0x40310618	Port interrupt mask register
GPIO_PRT12_INTR_MASKED	0x4031061C	Port interrupt masked status register
GPIO_PRT12_INTR_SET	0x40310620	Port interrupt set register
GPIO_PRT12_INTR_CFG	0x40310640	Port interrupt configuration register
GPIO_PRT12_CFG	0x40310644	Port configuration register
GPIO_PRT12_CFG_IN	0x40310648	Port input buffer configuration register
GPIO_PRT12_CFG_OUT	0x4031064C	Port output buffer configuration register
GPIO_PRT13_OUT_CLR	0x40310684	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT13_OUT_SET	0x40310688	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT13_OUT_INV	0x4031068C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT13_IN	0x40310690	Port input state register. See GPIO_PRT4_IN for the details of bit fields.
GPIO_PRT13_INTR	0x40310694	Port interrupt status register. See GPIO_PRT4_INTR for the details of bit fields.
GPIO_PRT13_INTR_MASK	0x40310698	Port interrupt mask register. See GPIO_PRT4_INTR_MASK for the details of bit fields.
GPIO_PRT13_INTR_MASKED	0x4031069C	Port interrupt masked status register. See GPIO_PRT4_INTR_MASKED for the details of bit fields.
GPIO_PRT13_INTR_SET	0x403106A0	Port interrupt set register. See GPIO_PRT4_INTR_SET for the details of bit fields.
GPIO_PRT13_INTR_CFG	0x403106C0	Port interrupt configuration register. See GPIO_PRT4_INTR_CFG for the details of bit fields.
GPIO_PRT14_OUT	0x40310700	Port output data register. See GPIO_PRT3_OUT for the details of bit fields.
GPIO_PRT14_OUT_CLR	0x40310704	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT14_OUT_SET	0x40310708	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT14_OUT_INV	0x4031070C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT14_IN	0x40310710	Port input state register. See GPIO_PRT3_IN for the details of bit fields.
GPIO_PRT14_INTR	0x40310714	Port interrupt status register. See GPIO_PRT3_INTR for the details of bit fields.
GPIO_PRT14_INTR_MASK	0x40310718	Port interrupt mask register. See GPIO_PRT3_INTR_MASK for the details of bit fields.
GPIO_PRT14_INTR_MASKED	0x4031071C	Port interrupt masked status register. See GPIO_PRT3_INTR_MASKED for the details of bit fields.
GPIO_PRT14_INTR_SET	0x40310720	Port interrupt set register. See GPIO_PRT3_INTR_SET for the details of bit fields.
GPIO_PRT14_INTR_CFG	0x40310740	Port interrupt configuration register. See GPIO_PRT3_INTR_CFG for the details of bit fields.
GPIO_PRT14_CFG	0x40310744	Port configuration register. See GPIO_PRT3_CFG for the details of bit fields.
GPIO_INTR_CAUSE0	0x40314000	Interrupt port cause register 0
GPIO_VDD_ACTIVE	0x40314010	Extern power supply detection register
GPIO_VDD_INTR	0x40314014	Supply detection interrupt register
GPIO_VDD_INTR_MASK	0x40314018	Supply detection interrupt mask register
GPIO_VDD_INTR_MASKED	0x4031401C	Supply detection interrupt masked register
GPIO_VDD_INTR_SET	0x40314020	Supply detection interrupt set register

15.1.1 GPIO_PRT0_OUT

Port output data register

Address: 0x40310000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [7:6]		OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	OUT5	IO output data for pin 5 Default Value: 0
4	OUT4	IO output data for pin 4 Default Value: 0
3	OUT3	IO output data for pin 3 Default Value: 0
2	OUT2	IO output data for pin 2 Default Value: 0
1	OUT1	IO output data for pin 1 Default Value: 0
0	OUT0	IO output data for pin 0 '0': Output state set to '0' '1': Output state set to '1' Default Value: 0

15.1.2 GPIO_PRT0_OUT_CLR

Port output data clear register

Address: 0x40310004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	A	A	A	A	A	A	A	A
Name	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	OUT7	IO clear output for pin 7 Default Value: 0
6	OUT6	IO clear output for pin 6 Default Value: 0
5	OUT5	IO clear output for pin 5 Default Value: 0
4	OUT4	IO clear output for pin 4 Default Value: 0
3	OUT3	IO clear output for pin 3 Default Value: 0
2	OUT2	IO clear output for pin 2 Default Value: 0
1	OUT1	IO clear output for pin 1 Default Value: 0

15.1.2 GPIO_PRT0_OUT_CLR (continued)

0	OUT0	IO clear output for pin 0: '0': Output state not affected. '1': Output state set to '0'. Default Value: 0

15.1.3 GPIO_PRT0_OUT_SET

Port output data set register

Address: 0x40310008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	A	A	A	A	A	A	A	A
Name	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	OUT7	IO set output for pin 7 Default Value: 0
6	OUT6	IO set output for pin 6 Default Value: 0
5	OUT5	IO set output for pin 5 Default Value: 0
4	OUT4	IO set output for pin 4 Default Value: 0
3	OUT3	IO set output for pin 3 Default Value: 0
2	OUT2	IO set output for pin 2 Default Value: 0
1	OUT1	IO set output for pin 1 Default Value: 0

15.1.3 GPIO_PRT0_OUT_SET (continued)

0	OUT0	IO set output for pin 0: '0': Output state not affected. '1': Output state set to '1'. Default Value: 0

15.1.4 GPIO_PRT0_OUT_INV

Port output data invert register

Address: 0x4031000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	A	A	A	A	A	A	A	A
Name	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	OUT7	IO invert output for pin 7 Default Value: 0
6	OUT6	IO invert output for pin 6 Default Value: 0
5	OUT5	IO invert output for pin 5 Default Value: 0
4	OUT4	IO invert output for pin 4 Default Value: 0
3	OUT3	IO invert output for pin 3 Default Value: 0
2	OUT2	IO invert output for pin 2 Default Value: 0
1	OUT1	IO invert output for pin 1 Default Value: 0

15.1.4 GPIO_PRT0_OUT_INV (continued)

0	OUT0	IO invert output for pin 0: '0': Output state not affected. '1': Output state inverted ('0' => '1', '1' => '0'). Default Value: 0

15.1.5 GPIO_PRT0_IN

Port input state register

Address: 0x40310010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		IN5	IN4	IN3	IN2	IN1	IN0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_IN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_IN	Reads of this register return the logical state of the filtered pin as selected in the INTR_CFG.FLT_SEL register. Default Value: 0
5	IN5	IO pin state for pin 5 Default Value: 0
4	IN4	IO pin state for pin 4 Default Value: 0
3	IN3	IO pin state for pin 3 Default Value: 0
2	IN2	IO pin state for pin 2 Default Value: 0
1	IN1	IO pin state for pin 1 Default Value: 0

15.1.5 GPIO_PRT0_IN (continued)

0	IN0	IO pin state for pin 0 '0': Low logic level present on pin. '1': High logic level present on pin. On reset assertion , IN register will get reset. The Pad value takes 2 clock cycles to be reflected into IN Register. It's value then depends on the external pin value. Default Value: 0

15.1.6 GPIO_PRT0_INTR

Port interrupt status register

Address: 0x40310014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None		A	A	A	A	A	A
Name	None [7:6]		EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [23:22]		IN_IN5	IN_IN4	IN_IN3	IN_IN2	IN_IN1	IN_IN0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							FLT_IN_IN

Bits	Name	Description
24	FLT_IN_IN	Filtered pin state for pin selected by INTR_CFG.FLT_SEL Default Value: 0
21	IN_IN5	IO pin state for pin 5 Default Value: 0
20	IN_IN4	IO pin state for pin 4 Default Value: 0
19	IN_IN3	IO pin state for pin 3 Default Value: 0
18	IN_IN2	IO pin state for pin 2 Default Value: 0
17	IN_IN1	IO pin state for pin 1 Default Value: 0
16	IN_IN0	IO pin state for pin 0 Default Value: 0
8	FLT_EDGE	Edge detected on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0

15.1.6 GPIO_PRT0_INTR (continued)

5	EDGE5	Edge detect for IO pin 5 Default Value: 0
4	EDGE4	Edge detect for IO pin 4 Default Value: 0
3	EDGE3	Edge detect for IO pin 3 Default Value: 0
2	EDGE2	Edge detect for IO pin 2 Default Value: 0
1	EDGE1	Edge detect for IO pin 1 Default Value: 0
0	EDGE0	Edge detect for IO pin 0 '0': No edge was detected on pin. '1': An edge was detected on pin. Default Value: 0

15.1.7 GPIO_PRT0_INTR_MASK

Port interrupt mask register

Address: 0x40310018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Masks edge interrupt on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
5	EDGE5	Masks edge interrupt on IO pin 5 Default Value: 0
4	EDGE4	Masks edge interrupt on IO pin 4 Default Value: 0
3	EDGE3	Masks edge interrupt on IO pin 3 Default Value: 0
2	EDGE2	Masks edge interrupt on IO pin 2 Default Value: 0
1	EDGE1	Masks edge interrupt on IO pin 1 Default Value: 0
0	EDGE0	Masks edge interrupt on IO pin 0 '0': Pin interrupt forwarding disabled '1': Pin interrupt forwarding enabled Default Value: 0

15.1.8 GPIO_PRT0_INTR_MASKED

Port interrupt masked status register

Address: 0x4031001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Edge detected and masked on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
5	EDGE5	Edge detected and masked on IO pin 5 Default Value: 0
4	EDGE4	Edge detected and masked on IO pin 4 Default Value: 0
3	EDGE3	Edge detected and masked on IO pin 3 Default Value: 0
2	EDGE2	Edge detected and masked on IO pin 2 Default Value: 0
1	EDGE1	Edge detected and masked on IO pin 1 Default Value: 0
0	EDGE0	Edge detected AND masked on IO pin 0 '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU Default Value: 0

15.1.9 GPIO_PRT0_INTR_SET

Port interrupt set register

Address: 0x40310020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	None		A	A	A	A	A	A
Name	None [7:6]		EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1S
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Sets edge detect interrupt for filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
5	EDGE5	Sets edge detect interrupt for IO pin 5 Default Value: 0
4	EDGE4	Sets edge detect interrupt for IO pin 4 Default Value: 0
3	EDGE3	Sets edge detect interrupt for IO pin 3 Default Value: 0
2	EDGE2	Sets edge detect interrupt for IO pin 2 Default Value: 0
1	EDGE1	Sets edge detect interrupt for IO pin 1 Default Value: 0
0	EDGE0	Sets edge detect interrupt for IO pin 0 '0': Interrupt state not affected '1': Interrupt set Default Value: 0

15.1.10 GPIO_PRT0_INTR_CFG

Port interrupt configuration register

Address: 0x40310040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [15:12]				EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by INTR_CFG.FLT_SEL Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge

15.1.10 GPIO_PRT0_INTR_CFG (continued)

		0x3: BOTH : Both rising and falling edges
11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for IO pin 5 Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for IO pin 4 Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pin 3 Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pin 2 Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pin 1 Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pin 0 Default Value: 0
		0x0: DISABLE : Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges

15.1.11 GPIO_PRT0_CFG

Port configuration register

Address: 0x40310044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN1	DRIVE_MODE1 [6:4]			IN_EN0	DRIVE_MODE0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN3	DRIVE_MODE3 [14:12]			IN_EN2	DRIVE_MODE2 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN5	DRIVE_MODE5 [22:20]			IN_EN4	DRIVE_MODE4 [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	IN_EN5	Enables the input buffer for IO pin 5 Default Value: 0
22 : 20	DRIVE_MODE5	The GPIO drive mode for IO pin 5 Default Value: 0
19	IN_EN4	Enables the input buffer for IO pin 4 Default Value: 0
18 : 16	DRIVE_MODE4	The GPIO drive mode for IO pin4 Default Value: 0
15	IN_EN3	Enables the input buffer for IO pin 3 Default Value: 0
14 : 12	DRIVE_MODE3	The GPIO drive mode for IO pin 3 Default Value: 0
11	IN_EN2	Enables the input buffer for IO pin 2 Default Value: 0
10 : 8	DRIVE_MODE2	The GPIO drive mode for IO pin 2 Default Value: 0

15.1.11 GPIO_PRT0_CFG (continued)

7	IN_EN1	Enables the input buffer for IO pin 1 Default Value: 0
6 : 4	DRIVE_MODE1	The GPIO drive mode for IO pin 1 Default Value: 0
3	IN_EN0	Enables the input buffer for IO pin 0. This bit should be cleared when analog signals are present on the pin to avoid crowbar currents. The output buffer can be used to drive analog signals high or low without issue. '0': Input buffer disabled '1': Input buffer enabled Default Value: 0
2 : 0	DRIVE_MODE0	The GPIO drive mode for IO pin 0. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0 **0x0: HIGHZ :** Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance **0x1: RESERVED :** This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance

15.1.11 GPIO_PRT0_CFG (continued)

0x2: PULLUP :

Resistive pull up
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Weak/resistive pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull up
D_OUT = '1': Weak/resistive pull up

0x3: PULLDOWN :

Resistive pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull down

0x4: OD_DRIVESLOW :

Open drain, drives low
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': High Impedance
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

15.1.11 GPIO_PRT0_CFG (continued)

0x5: OD_DRIVESHIGH :

Open drain, drives high
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': High Impedance
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x6: STRONG :

Strong D_OUTput buffer
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x7: PULLUP_DOWN :

Pull up or pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = '0':
GPIO_DSI_OUT = '0': Weak/resistive pull down
GPIO_DSI_OUT = '1': Weak/resistive pull up
where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT.
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull up

15.1.12 GPIO_PRT0_CFG_IN

Port input buffer configuration register

Address: 0x40310048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		VTRIP_-SEL5_0	VTRIP_-SEL4_0	VTRIP_-SEL3_0	VTRIP_-SEL2_0	VTRIP_-SEL1_0	VTRIP_-SEL0_0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	VTRIP_SEL5_0	Configures the pin 5 input buffer mode (trip points and hysteresis) Default Value: 0
4	VTRIP_SEL4_0	Configures the pin 4 input buffer mode (trip points and hysteresis) Default Value: 0
3	VTRIP_SEL3_0	Configures the pin 3 input buffer mode (trip points and hysteresis) Default Value: 0
2	VTRIP_SEL2_0	Configures the pin 2 input buffer mode (trip points and hysteresis) Default Value: 0
1	VTRIP_SEL1_0	Configures the pin 1 input buffer mode (trip points and hysteresis) Default Value: 0
0	VTRIP_SEL0_0	Configures the pin 0 input buffer mode (trip points and hysteresis) Default Value: 0

15.1.12 GPIO_PRT0_CFG_IN (continued)

0x0: CMOS :

PSoC 6:: Input buffer compatible with CMOS and I2C interfaces
Traveo II: Full encoding is shown in CFG_IN_AUTOLVL.VTRIP_SEL0_1

0x1: TTL :

PSoC 6:: Input buffer compatible with TTL and MediaLB interfaces
Traveo II: full encoding is shown in CFG_IN_AUTOLVL.VTRIP_SEL0_1

15.1.13 GPIO_PRT0_CFG_OUT

Port output buffer configuration register

Address: 0x4031004C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		SLOW5	SLOW4	SLOW3	SLOW2	SLOW1	SLOW0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DRIVE_SEL3 [23:22]		DRIVE_SEL2 [21:20]		DRIVE_SEL1 [19:18]		DRIVE_SEL0 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [31:28]				DRIVE_SEL5 [27:26]		DRIVE_SEL4 [25:24]	

Bits	Name	Description
27 : 26	DRIVE_SEL5	Sets the GPIO drive strength for IO pin 5 Default Value: 0
25 : 24	DRIVE_SEL4	Sets the GPIO drive strength for IO pin 4 Default Value: 0
23 : 22	DRIVE_SEL3	Sets the GPIO drive strength for IO pin 3 Default Value: 0
21 : 20	DRIVE_SEL2	Sets the GPIO drive strength for IO pin 2 Default Value: 0
19 : 18	DRIVE_SEL1	Sets the GPIO drive strength for IO pin 1 Default Value: 0
17 : 16	DRIVE_SEL0	Documentation: Note: DRIVE_SELx are used among GPIO cells and HSIO_STD but the encoding values may differ as shown on the right side of this table Default Value: 0

15.1.13 GPIO_PRT0_CFG_OUT (continued)

0x0: DRIVE_SEL_ZERO :

Traveo II: GPIO_STD/GPIO_ENH: Full drive strengh: GPIO drives current at its max rated spec.
Traveo II:_GPIO_SMC: GPIO_SMC default mode.
Traveo II:_HSIO_STD: HSIO default mode.
PSoC 6: GPIO cells and HSIO_STD cells: Full drive strength: GPIO drives current at its max rated spec.

0x1: DRIVE_SEL_ONE :

Traveo II: GPIO_STD/GPIO_ENH: Full drive strengh: GPIO drives current at its max rated spec.
Traveo II:_GPIO_SMC: GPIO full drive strength.
Traveo II:_HSIO_STD: GPIO full drive strength.
PSoC 6: GPIO cells and HSIO_STD cells: 1/2 drive strength: GPIO drives current at 1/2 of its max rated spec

0x2: DRIVE_SEL_TWO :

Traveo II: GPIO_STD/GPIO_ENH: 1/2 drive strength: GPIO drives current at 1/2 of its max rated spec.
Traveo II:_GPIO_SMC: GPIO 1/2 drive strength.
Traveo II:_HSIO_STD: GPIO 1/2 drive strength.
PSoC 6: GPIO cells and HSIO_STD cells: 1/4 drive strength. GPIO drives current at 1/4 of its max rated spec.

0x3: DRIVE_SEL_THREE :

Traveo II: GPIO_STD/GPIO_ENH: 1/4 drive strength: GPIO drives current at 1/4 of its max rated spec.
Traveo II:_GPIO_SMC: GPIO 1/4 drive strength.
Traveo II:_HSIO_STD: GPIO 1/4 drive strength.
PSoC 6: GPIO cells and HSIO_STD cells: 1/8 drive strength. GPIO drives current at 1/8 of its max rated spec.

5	SLOW5	Enables slow slew rate for IO pin 5 Default Value: 0
4	SLOW4	Enables slow slew rate for IO pin 4 Default Value: 0
3	SLOW3	Enables slow slew rate for IO pin 3 Default Value: 0
2	SLOW2	Enables slow slew rate for IO pin 2 Default Value: 0
1	SLOW1	Enables slow slew rate for IO pin 1 Default Value: 0
0	SLOW0	Enables slow slew rate for IO pin 0 '0': Fast slew rate '1': Slow slew rate Default Value: 0

15.1.14 GPIO_PRT1_OUT

Port output data register

Address: 0x40310080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					RW	RW	RW
Name	None [7:3]					OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	OUT2	IO output data for pin 2 Default Value: 0
1	OUT1	IO output data for pin 1 Default Value: 0
0	OUT0	IO output data for pin 0 '0': Output state set to '0' '1': Output state set to '1' Default Value: 0

15.1.15 GPIO_PRT1_IN

Port input state register

Address: 0x40310090

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [7:3]					IN2	IN1	IN0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_IN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_IN	Reads of this register return the logical state of the filtered pin as selected in the INTR_CFG.FLT_SEL register. Default Value: 0
2	IN2	IO pin state for pin 2 Default Value: 0
1	IN1	IO pin state for pin 1 Default Value: 0
0	IN0	IO pin state for pin 0 '0': Low logic level present on pin. '1': High logic level present on pin. On reset assertion , IN register will get reset. The Pad value takes 2 clock cycles to be reflected into IN Register. It's value then depends on the external pin value. Default Value: 0

15.1.16 GPIO_PRT1_INTR

Port interrupt status register

Address: 0x40310094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					A	A	A
Name	None [7:3]					EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [23:19]					IN_IN2	IN_IN1	IN_IN0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							FLT_IN_IN

Bits	Name	Description
24	FLT_IN_IN	Filtered pin state for pin selected by INTR_CFG.FLT_SEL Default Value: 0
18	IN_IN2	IO pin state for pin 2 Default Value: 0
17	IN_IN1	IO pin state for pin 1 Default Value: 0
16	IN_IN0	IO pin state for pin 0 Default Value: 0
8	FLT_EDGE	Edge detected on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
2	EDGE2	Edge detect for IO pin 2 Default Value: 0
1	EDGE1	Edge detect for IO pin 1 Default Value: 0

15.1.16 GPIO_PRT1_INTR (continued)

0	EDGE0	Edge detect for IO pin 0 '0': No edge was detected on pin. '1': An edge was detected on pin. Default Value: 0

15.1.17 GPIO_PRT1_INTR_MASK

Port interrupt mask register

Address: 0x40310098

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Masks edge interrupt on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
2	EDGE2	Masks edge interrupt on IO pin 2 Default Value: 0
1	EDGE1	Masks edge interrupt on IO pin 1 Default Value: 0
0	EDGE0	Masks edge interrupt on IO pin 0 '0': Pin interrupt forwarding disabled '1': Pin interrupt forwarding enabled Default Value: 0

15.1.18 GPIO_PRT1_INTR_MASKED

Port interrupt masked status register

Address: 0x4031009C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [7:3]					EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Edge detected and masked on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
2	EDGE2	Edge detected and masked on IO pin 2 Default Value: 0
1	EDGE1	Edge detected and masked on IO pin 1 Default Value: 0
0	EDGE0	Edge detected AND masked on IO pin 0 '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU Default Value: 0

15.1.19 GPIO_PRT1_INTR_SET

Port interrupt set register

Address: 0x403100A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [7:3]					EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1S
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Sets edge detect interrupt for filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
2	EDGE2	Sets edge detect interrupt for IO pin 2 Default Value: 0
1	EDGE1	Sets edge detect interrupt for IO pin 1 Default Value: 0
0	EDGE0	Sets edge detect interrupt for IO pin 0 '0': Interrupt state not affected '1': Interrupt set Default Value: 0

15.1.20 GPIO_PRT1_INTR_CFG

Port interrupt configuration register

Address: 0x403100C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by INTR_CFG.FLT_SEL Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge

15.1.20 GPIO_PRT1_INTR_CFG (continued)

		0x3: BOTH : Both rising and falling edges
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pin 2 Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pin 1 Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pin 0 Default Value: 0
		0x0: DISABLE : Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges

15.1.21 GPIO_PRT1_CFG

Port configuration register

Address: 0x403100C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN1	DRIVE_MODE1 [6:4]			IN_EN0	DRIVE_MODE0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW		
HW Access	None				R	R		
Name	None [15:12]				IN_EN2	DRIVE_MODE2 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	IN_EN2	Enables the input buffer for IO pin 2 Default Value: 0
10 : 8	DRIVE_MODE2	The GPIO drive mode for IO pin 2 Default Value: 0
7	IN_EN1	Enables the input buffer for IO pin 1 Default Value: 0
6 : 4	DRIVE_MODE1	The GPIO drive mode for IO pin 1 Default Value: 0
3	IN_EN0	Enables the input buffer for IO pin 0. This bit should be cleared when analog signals are present on the pin to avoid crowbar currents. The output buffer can be used to drive analog signals high or low without issue. '0': Input buffer disabled '1': Input buffer enabled Default Value: 0

15.1.21 GPIO_PRT1_CFG (continued)

2 : 0	DRIVE_MODE0	The GPIO drive mode for IO pin 0. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0 **0x0: HIGHZ :** Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance **0x1: RESERVED :** This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance **0x2: PULLUP :** Resistive pull up For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Weak/resistive pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': Weak/resistive pull up D_OUT = '1': Weak/resistive pull up

15.1.21 GPIO_PRT1_CFG (continued)

0x3: PULLDOWN :

Resistive pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull down

0x4: OD_DRIVESLOW :

Open drain, drives low
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': High Impedance
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x5: OD_DRIVESHIGH :

Open drain, drives high
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': High Impedance
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

15.1.21 GPIO_PRT1_CFG (continued)

0x6: STRONG :

Strong D_OUTput buffer
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x7: PULLUP_DOWN :

Pull up or pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = '0':
GPIO_DSI_OUT = '0': Weak/resistive pull down
GPIO_DSI_OUT = '1': Weak/resistive pull up
where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT.
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull up

15.1.22 GPIO_PRT1_CFG_IN

Port input buffer configuration register

Address: 0x403100C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					VTRIP_-SEL2_0	VTRIP_-SEL1_0	VTRIP_-SEL0_0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	VTRIP_SEL2_0	Configures the pin 2 input buffer mode (trip points and hysteresis) Default Value: 0
1	VTRIP_SEL1_0	Configures the pin 1 input buffer mode (trip points and hysteresis) Default Value: 0
0	VTRIP_SEL0_0	Configures the pin 0 input buffer mode (trip points and hysteresis) Default Value: 0 **0x0: CMOS :** PSoC 6:: Input buffer compatible with CMOS and I2C interfaces Traveo II: Full encoding is shown in CFG_IN_AUTOLVL.VTRIP_SEL0_1 **0x1: TTL :** PSoC 6:: Input buffer compatible with TTL and MediaLB interfaces Traveo II: full encoding is shown in CFG_IN_AUTOLVL.VTRIP_SEL0_1

15.1.23 GPIO_PRT1_CFG_OUT

Port output buffer configuration register

Address: 0x403100CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					SLOW2	SLOW1	SLOW0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [23:22]		DRIVE_SEL2 [21:20]		DRIVE_SEL1 [19:18]		DRIVE_SEL0 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21 : 20	DRIVE_SEL2	Sets the GPIO drive strength for IO pin 2 Default Value: 0
19 : 18	DRIVE_SEL1	Sets the GPIO drive strength for IO pin 1 Default Value: 0
17 : 16	DRIVE_SEL0	Documentation: Note: DRIVE_SELx are used among GPIO cells and HSIO_STD but the encoding values may differ as shown on the right side of this table Default Value: 0 **0x0: DRIVE_SEL_ZERO :** Traveo II: GPIO_STD/GPIO_ENH: Full drive strengh: GPIO drives current at its max rated spec. Traveo II:_GPIO_SMC: GPIO_SMC default mode. Traveo II:_HSIO_STD: HSIO default mode. PSoC 6: GPIO cells and HSIO_STD cells: Full drive strength: GPIO drives current at its max rated spec.

15.1.23 GPIO_PRT1_CFG_OUT (continued)

		0x1: DRIVE_SEL_ONE : Traveo II: GPIO_STD/GPIO_ENH: Full drive strengh: GPIO drives current at its max rated spec. Traveo II:_GPIO_SMC: GPIO full drive strength. Traveo II:_HSIO_STD: GPIO full drive strength. PSoC 6: GPIO cells and HSIO_STD cells: 1/2 drive strength: GPIO drives current at 1/2 of its max rated spec **0x2: DRIVE_SEL_TWO :** Traveo II: GPIO_STD/GPIO_ENH: 1/2 drive strength: GPIO drives current at 1/2 of its max rated spec. Traveo II:_GPIO_SMC: GPIO 1/2 drive strength. Traveo II:_HSIO_STD: GPIO 1/2 drive strength. PSoC 6: GPIO cells and HSIO_STD cells: 1/4 drive strength. GPIO drives current at 1/4 of its max rated spec. **0x3: DRIVE_SEL_THREE :** Traveo II: GPIO_STD/GPIO_ENH: 1/4 drive strength: GPIO drives current at 1/4 of its max rated spec. Traveo II:_GPIO_SMC: GPIO 1/4 drive strength. Traveo II:_HSIO_STD: GPIO 1/4 drive strength. PSoC 6: GPIO cells and HSIO_STD cells: 1/8 drive strength. GPIO drives current at 1/8 of its max rated spec.
2	SLOW2	Enables slow slew rate for IO pin 2 Default Value: 0
1	SLOW1	Enables slow slew rate for IO pin 1 Default Value: 0
0	SLOW0	Enables slow slew rate for IO pin 0 '0': Fast slew rate '1': Slow slew rate Default Value: 0

15.1.24 GPIO_PRT2_OUT

Port output data register

Address: 0x40310100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	OUT7	IO output data for pin 7 Default Value: 0
6	OUT6	IO output data for pin 6 Default Value: 0
5	OUT5	IO output data for pin 5 Default Value: 0
4	OUT4	IO output data for pin 4 Default Value: 0
3	OUT3	IO output data for pin 3 Default Value: 0
2	OUT2	IO output data for pin 2 Default Value: 0
1	OUT1	IO output data for pin 1 Default Value: 0

15.1.24 GPIO_PRT2_OUT (continued)

0	OUT0	IO output data for pin 0 '0': Output state set to '0' '1': Output state set to '1' Default Value: 0

15.1.25 GPIO_PRT2_IN

Port input state register

Address: 0x40310110

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_IN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_IN	Reads of this register return the logical state of the filtered pin as selected in the INTR_CFG.FLT_SEL register. Default Value: 0
7	IN7	IO pin state for pin 7 Default Value: 0
6	IN6	IO pin state for pin 6 Default Value: 0
5	IN5	IO pin state for pin 5 Default Value: 0
4	IN4	IO pin state for pin 4 Default Value: 0
3	IN3	IO pin state for pin 3 Default Value: 0
2	IN2	IO pin state for pin 2 Default Value: 0

15.1.25 GPIO_PRT2_IN (continued)

1	IN1	IO pin state for pin 1 Default Value: 0
0	IN0	IO pin state for pin 0 '0': Low logic level present on pin. '1': High logic level present on pin. On reset assertion , IN register will get reset. The Pad value takes 2 clock cycles to be reflected into IN Register. It's value then depends on the external pin value. Default Value: 0

15.1.26 GPIO_PRT2_INTR

Port interrupt status register

Address: 0x40310114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	IN_IN7	IN_IN6	IN_IN5	IN_IN4	IN_IN3	IN_IN2	IN_IN1	IN_IN0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							FLT_IN_IN

Bits	Name	Description
24	FLT_IN_IN	Filtered pin state for pin selected by INTR_CFG.FLT_SEL Default Value: 0
23	IN_IN7	IO pin state for pin 7 Default Value: 0
22	IN_IN6	IO pin state for pin 6 Default Value: 0
21	IN_IN5	IO pin state for pin 5 Default Value: 0
20	IN_IN4	IO pin state for pin 4 Default Value: 0
19	IN_IN3	IO pin state for pin 3 Default Value: 0
18	IN_IN2	IO pin state for pin 2 Default Value: 0
17	IN_IN1	IO pin state for pin 1 Default Value: 0

15.1.26 GPIO_PRT2_INTR (continued)

16	IN_IN0	IO pin state for pin 0 Default Value: 0
8	FLT_EDGE	Edge detected on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Edge detect for IO pin 7 Default Value: 0
6	EDGE6	Edge detect for IO pin 6 Default Value: 0
5	EDGE5	Edge detect for IO pin 5 Default Value: 0
4	EDGE4	Edge detect for IO pin 4 Default Value: 0
3	EDGE3	Edge detect for IO pin 3 Default Value: 0
2	EDGE2	Edge detect for IO pin 2 Default Value: 0
1	EDGE1	Edge detect for IO pin 1 Default Value: 0
0	EDGE0	Edge detect for IO pin 0 '0': No edge was detected on pin. '1': An edge was detected on pin. Default Value: 0

15.1.27 GPIO_PRT2_INTR_MASK

Port interrupt mask register

Address: 0x40310118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Masks edge interrupt on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Masks edge interrupt on IO pin 7 Default Value: 0
6	EDGE6	Masks edge interrupt on IO pin 6 Default Value: 0
5	EDGE5	Masks edge interrupt on IO pin 5 Default Value: 0
4	EDGE4	Masks edge interrupt on IO pin 4 Default Value: 0
3	EDGE3	Masks edge interrupt on IO pin 3 Default Value: 0
2	EDGE2	Masks edge interrupt on IO pin 2 Default Value: 0
1	EDGE1	Masks edge interrupt on IO pin 1 Default Value: 0

15.1.27 GPIO_PRT2_INTR_MASK (continued)

0	EDGE0	Masks edge interrupt on IO pin 0 '0': Pin interrupt forwarding disabled '1': Pin interrupt forwarding enabled Default Value: 0

15.1.28 GPIO_PRT2_INTR_MASKED

Port interrupt masked status register

Address: 0x4031011C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Edge detected and masked on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Edge detected and masked on IO pin 7 Default Value: 0
6	EDGE6	Edge detected and masked on IO pin 6 Default Value: 0
5	EDGE5	Edge detected and masked on IO pin 5 Default Value: 0
4	EDGE4	Edge detected and masked on IO pin 4 Default Value: 0
3	EDGE3	Edge detected and masked on IO pin 3 Default Value: 0
2	EDGE2	Edge detected and masked on IO pin 2 Default Value: 0
1	EDGE1	Edge detected and masked on IO pin 1 Default Value: 0

15.1.28 GPIO_PRT2_INTR_MASKED (continued)

0	EDGE0	Edge detected AND masked on IO pin 0 '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU Default Value: 0

15.1.29 GPIO_PRT2_INTR_SET

Port interrupt set register

Address: 0x40310120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1S
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Sets edge detect interrupt for filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Sets edge detect interrupt for IO pin 7 Default Value: 0
6	EDGE6	Sets edge detect interrupt for IO pin 6 Default Value: 0
5	EDGE5	Sets edge detect interrupt for IO pin 5 Default Value: 0
4	EDGE4	Sets edge detect interrupt for IO pin 4 Default Value: 0
3	EDGE3	Sets edge detect interrupt for IO pin 3 Default Value: 0
2	EDGE2	Sets edge detect interrupt for IO pin 2 Default Value: 0
1	EDGE1	Sets edge detect interrupt for IO pin 1 Default Value: 0

15.1.29 GPIO_PRT2_INTR_SET (continued)

0	EDGE0	Sets edge detect interrupt for IO pin 0 '0': Interrupt state not affected '1': Interrupt set Default Value: 0

15.1.30 GPIO_PRT2_INTR_CFG

Port interrupt configuration register

Address: 0x40310140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by INTR_CFG.FLT_SEL Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge

15.1.30 GPIO_PRT2_INTR_CFG (continued)

		0x3: BOTH : Both rising and falling edges
15 : 14	EDGE7_SEL	Sets which edge will trigger an IRQ for IO pin 7 Default Value: 0
13 : 12	EDGE6_SEL	Sets which edge will trigger an IRQ for IO pin 6 Default Value: 0
11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for IO pin 5 Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for IO pin 4 Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pin 3 Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pin 2 Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pin 1 Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pin 0 Default Value: 0
		0x0: DISABLE : Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges

15.1.31 GPIO_PRT2_CFG

Port configuration register

Address: 0x40310144

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN1	DRIVE_MODE1 [6:4]			IN_EN0	DRIVE_MODE0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN3	DRIVE_MODE3 [14:12]			IN_EN2	DRIVE_MODE2 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN5	DRIVE_MODE5 [22:20]			IN_EN4	DRIVE_MODE4 [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN7	DRIVE_MODE7 [30:28]			IN_EN6	DRIVE_MODE6 [26:24]		

Bits	Name	Description
31	IN_EN7	Enables the input buffer for IO pin 7 Default Value: 0
30 : 28	DRIVE_MODE7	The GPIO drive mode for IO pin 7 Default Value: 0
27	IN_EN6	Enables the input buffer for IO pin 6 Default Value: 0
26 : 24	DRIVE_MODE6	The GPIO drive mode for IO pin 6 Default Value: 0
23	IN_EN5	Enables the input buffer for IO pin 5 Default Value: 0
22 : 20	DRIVE_MODE5	The GPIO drive mode for IO pin 5 Default Value: 0
19	IN_EN4	Enables the input buffer for IO pin 4 Default Value: 0
18 : 16	DRIVE_MODE4	The GPIO drive mode for IO pin4 Default Value: 0

15.1.31 GPIO_PRT2_CFG (continued)

15	IN_EN3	Enables the input buffer for IO pin 3 Default Value: 0
14 : 12	DRIVE_MODE3	The GPIO drive mode for IO pin 3 Default Value: 0
11	IN_EN2	Enables the input buffer for IO pin 2 Default Value: 0
10 : 8	DRIVE_MODE2	The GPIO drive mode for IO pin 2 Default Value: 0
7	IN_EN1	Enables the input buffer for IO pin 1 Default Value: 0
6 : 4	DRIVE_MODE1	The GPIO drive mode for IO pin 1 Default Value: 0
3	IN_EN0	Enables the input buffer for IO pin 0. This bit should be cleared when analog signals are present on the pin to avoid crowbar currents. The output buffer can be used to drive analog signals high or low without issue. '0': Input buffer disabled '1': Input buffer enabled Default Value: 0
2 : 0	DRIVE_MODE0	The GPIO drive mode for IO pin 0. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0 **0x0: HIGHZ :** Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance **0x1: RESERVED :** This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance

15.1.31 GPIO_PRT2_CFG (continued)

0x2: PULLUP :

Resistive pull up
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Weak/resistive pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull up
D_OUT = '1': Weak/resistive pull up

0x3: PULLDOWN :

Resistive pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull down

0x4: OD_DRIVESLOW :

Open drain, drives low
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': High Impedance
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

15.1.31 GPIO_PRT2_CFG (continued)

0x5: OD_DRIVESHIGH :

Open drain, drives high
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': High Impedance
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x6: STRONG :

Strong D_OUTput buffer
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x7: PULLUP_DOWN :

Pull up or pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = '0':
GPIO_DSI_OUT = '0': Weak/resistive pull down
GPIO_DSI_OUT = '1': Weak/resistive pull up
where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT.
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull up

15.1.32 GPIO_PRT2_CFG_IN

Port input buffer configuration register

Address: 0x40310148

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	VTRIP_-SEL7_0	VTRIP_-SEL6_0	VTRIP_-SEL5_0	VTRIP_-SEL4_0	VTRIP_-SEL3_0	VTRIP_-SEL2_0	VTRIP_-SEL1_0	VTRIP_-SEL0_0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	VTRIP_SEL7_0	Configures the pin 7 input buffer mode (trip points and hysteresis) Default Value: 0
6	VTRIP_SEL6_0	Configures the pin 6 input buffer mode (trip points and hysteresis) Default Value: 0
5	VTRIP_SEL5_0	Configures the pin 5 input buffer mode (trip points and hysteresis) Default Value: 0
4	VTRIP_SEL4_0	Configures the pin 4 input buffer mode (trip points and hysteresis) Default Value: 0
3	VTRIP_SEL3_0	Configures the pin 3 input buffer mode (trip points and hysteresis) Default Value: 0
2	VTRIP_SEL2_0	Configures the pin 2 input buffer mode (trip points and hysteresis) Default Value: 0
1	VTRIP_SEL1_0	Configures the pin 1 input buffer mode (trip points and hysteresis) Default Value: 0

15.1.32 GPIO_PRT2_CFG_IN (continued)

0	VTRIP_SEL0_0	Configures the pin 0 input buffer mode (trip points and hysteresis) Default Value: 0 **0x0: CMOS :** PSoC 6:: Input buffer compatible with CMOS and I2C interfaces Traveo II: Full encoding is shown in CFG_IN_AUTOLVL.VTRIP_SEL0_1 **0x1: TTL :** PSoC 6:: Input buffer compatible with TTL and MediaLB interfaces Traveo II: full encoding is shown in CFG_IN_AUTOLVL.VTRIP_SEL0_1

15.1.33 GPIO_PRT2_CFG_OUT

Port output buffer configuration register

Address: 0x4031014C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	SLOW7	SLOW6	SLOW5	SLOW4	SLOW3	SLOW2	SLOW1	SLOW0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DRIVE_SEL3 [23:22]		DRIVE_SEL2 [21:20]		DRIVE_SEL1 [19:18]		DRIVE_SEL0 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DRIVE_SEL7 [31:30]		DRIVE_SEL6 [29:28]		DRIVE_SEL5 [27:26]		DRIVE_SEL4 [25:24]	

Bits	Name	Description
31 : 30	DRIVE_SEL7	Sets the GPIO drive strength for IO pin 7 Default Value: 0
29 : 28	DRIVE_SEL6	Sets the GPIO drive strength for IO pin 6 Default Value: 0
27 : 26	DRIVE_SEL5	Sets the GPIO drive strength for IO pin 5 Default Value: 0
25 : 24	DRIVE_SEL4	Sets the GPIO drive strength for IO pin 4 Default Value: 0
23 : 22	DRIVE_SEL3	Sets the GPIO drive strength for IO pin 3 Default Value: 0
21 : 20	DRIVE_SEL2	Sets the GPIO drive strength for IO pin 2 Default Value: 0
19 : 18	DRIVE_SEL1	Sets the GPIO drive strength for IO pin 1 Default Value: 0

15.1.33 GPIO_PRT2_CFG_OUT (continued)

17 : 16	DRIVE_SEL0	Documentation: Note: DRIVE_SELx are used among GPIO cells and HSIO_STD but the encoding values may differ as shown on the right side of this table Default Value: 0 **0x0: DRIVE_SEL_ZERO :** Traveo II: GPIO_STD/GPIO_ENH: Full drive strengh: GPIO drives current at its max rated spec. Traveo II:_GPIO_SMC: GPIO_SMC default mode. Traveo II:_HSIO_STD: HSIO default mode. PSoC 6: GPIO cells and HSIO_STD cells: Full drive strength: GPIO drives current at its max rated spec. **0x1: DRIVE_SEL_ONE :** Traveo II: GPIO_STD/GPIO_ENH: Full drive strengh: GPIO drives current at its max rated spec. Traveo II:_GPIO_SMC: GPIO full drive strength. Traveo II:_HSIO_STD: GPIO full drive strength. PSoC 6: GPIO cells and HSIO_STD cells: 1/2 drive strength: GPIO drives current at 1/2 of its max rated spec **0x2: DRIVE_SEL_TWO :** Traveo II: GPIO_STD/GPIO_ENH: 1/2 drive strength: GPIO drives current at 1/2 of its max rated spec. Traveo II:_GPIO_SMC: GPIO 1/2 drive strength. Traveo II:_HSIO_STD: GPIO 1/2 drive strength. PSoC 6: GPIO cells and HSIO_STD cells: 1/4 drive strength. GPIO drives current at 1/4 of its max rated spec. **0x3: DRIVE_SEL_THREE :** Traveo II: GPIO_STD/GPIO_ENH: 1/4 drive strength: GPIO drives current at 1/4 of its max rated spec. Traveo II:_GPIO_SMC: GPIO 1/4 drive strength. Traveo II:_HSIO_STD: GPIO 1/4 drive strength. PSoC 6: GPIO cells and HSIO_STD cells: 1/8 drive strength. GPIO drives current at 1/8 of its max rated spec.
7	SLOW7	Enables slow slew rate for IO pin 7 Default Value: 0
6	SLOW6	Enables slow slew rate for IO pin 6 Default Value: 0
5	SLOW5	Enables slow slew rate for IO pin 5 Default Value: 0
4	SLOW4	Enables slow slew rate for IO pin 4 Default Value: 0
3	SLOW3	Enables slow slew rate for IO pin 3 Default Value: 0
2	SLOW2	Enables slow slew rate for IO pin 2 Default Value: 0

15.1.33 GPIO_PRT2_CFG_OUT (continued)

1	SLOW1	Enables slow slew rate for IO pin 1 Default Value: 0
0	SLOW0	Enables slow slew rate for IO pin 0 '0': Fast slew rate '1': Slow slew rate Default Value: 0

15.1.34 GPIO_PRT3_OUT

Port output data register

Address: 0x40310180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW	RW
Name	None [7:2]						OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	OUT1	IO output data for pin 1 Default Value: 0
0	OUT0	IO output data for pin 0 '0': Output state set to '0' '1': Output state set to '1' Default Value: 0

15.1.35 GPIO_PRT3_IN

Port input state register

Address: 0x40310190

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						IN1	IN0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_IN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_IN	Reads of this register return the logical state of the filtered pin as selected in the IN-TR_CFG.FLT_SEL register. Default Value: 0
1	IN1	IO pin state for pin 1 Default Value: 0
0	IN0	IO pin state for pin 0 '0': Low logic level present on pin. '1': High logic level present on pin. On reset assertion , IN register will get reset. The Pad value takes 2 clock cycles to be reflected into IN Register. It's value then depends on the external pin value. Default Value: 0

15.1.36 GPIO_PRT3_INTR

Port interrupt status register

Address: 0x40310194

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						A	A
Name	None [7:2]						EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None						R	R
HW Access	None						W	W
Name	None [23:18]						IN_IN1	IN_IN0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							FLT_IN_IN

Bits	Name	Description
24	FLT_IN_IN	Filtered pin state for pin selected by INTR_CFG.FLT_SEL Default Value: 0
17	IN_IN1	IO pin state for pin 1 Default Value: 0
16	IN_IN0	IO pin state for pin 0 Default Value: 0
8	FLT_EDGE	Edge detected on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
1	EDGE1	Edge detect for IO pin 1 Default Value: 0
0	EDGE0	Edge detect for IO pin 0 '0': No edge was detected on pin. '1': An edge was detected on pin. Default Value: 0

15.1.37 GPIO_PRT3_INTR_MASK

Port interrupt mask register

Address: 0x40310198

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Masks edge interrupt on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
1	EDGE1	Masks edge interrupt on IO pin 1 Default Value: 0
0	EDGE0	Masks edge interrupt on IO pin 0 '0': Pin interrupt forwarding disabled '1': Pin interrupt forwarding enabled Default Value: 0

15.1.38 GPIO_PRT3_INTR_MASKED

Port interrupt masked status register

Address: 0x4031019C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Edge detected and masked on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
1	EDGE1	Edge detected and masked on IO pin 1 Default Value: 0
0	EDGE0	Edge detected AND masked on IO pin 0 '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU Default Value: 0

15.1.39 GPIO_PRT3_INTR_SET

Port interrupt set register

Address: 0x403101A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1S
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Sets edge detect interrupt for filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
1	EDGE1	Sets edge detect interrupt for IO pin 1 Default Value: 0
0	EDGE0	Sets edge detect interrupt for IO pin 0 '0': Interrupt state not affected '1': Interrupt set Default Value: 0

15.1.40 GPIO_PRT3_INTR_CFG

Port interrupt configuration register

Address: 0x403101C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [7:4]				EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by INTR_CFG.FLT_SEL Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge

15.1.40 GPIO_PRT3_INTR_CFG (continued)

		0x3: BOTH : Both rising and falling edges
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pin 1 Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pin 0 Default Value: 0
		0x0: DISABLE : Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges

15.1.41 GPIO_PRT3_CFG

Port configuration register

Address: 0x403101C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN1	DRIVE_MODE1 [6:4]			IN_EN0	DRIVE_MODE0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	IN_EN1	Enables the input buffer for IO pin 1 Default Value: 0
6 : 4	DRIVE_MODE1	The GPIO drive mode for IO pin 1 Default Value: 0
3	IN_EN0	Enables the input buffer for IO pin 0. This bit should be cleared when analog signals are present on the pin to avoid crowbar currents. The output buffer can be used to drive analog signals high or low without issue. '0': Input buffer disabled '1': Input buffer enabled Default Value: 0
2 : 0	DRIVE_MODE0	The GPIO drive mode for IO pin 0. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0

15.1.41 GPIO_PRT3_CFG (continued)

0x0: HIGHZ :

Output buffer is off creating a high impedance input
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x1: RESERVED :

This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases.
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance

0x2: PULLUP :

Resistive pull up
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Weak/resistive pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull up
D_OUT = '1': Weak/resistive pull up

15.1.41 GPIO_PRT3_CFG (continued)

0x3: PULLDOWN :

Resistive pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull down

0x4: OD_DRIVESLOW :

Open drain, drives low
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': High Impedance
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x5: OD_DRIVESHIGH :

Open drain, drives high
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': High Impedance
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

15.1.41 GPIO_PRT3_CFG (continued)

0x6: STRONG :

Strong D_OUTput buffer
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x7: PULLUP_DOWN :

Pull up or pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = '0':
GPIO_DSI_OUT = '0': Weak/resistive pull down
GPIO_DSI_OUT = '1': Weak/resistive pull up
where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT.
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull up

15.1.42 GPIO_PRT3_CFG_IN

Port input buffer configuration register

Address: 0x403101C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						VTRIP_-SEL1_0	VTRIP_-SEL0_0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	VTRIP_SEL1_0	Configures the pin 1 input buffer mode (trip points and hysteresis) Default Value: 0
0	VTRIP_SEL0_0	Configures the pin 0 input buffer mode (trip points and hysteresis) Default Value: 0 **0x0: CMOS :** PSoC 6:: Input buffer compatible with CMOS and I2C interfaces Traveo II: Full encoding is shown in CFG_IN_AUTOLVL.VTRIP_SEL0_1 **0x1: TTL :** PSoC 6:: Input buffer compatible with TTL and MediaLB interfaces Traveo II: full encoding is shown in CFG_IN_AUTOLVL.VTRIP_SEL0_1

15.1.43 GPIO_PRT3_CFG_OUT

Port output buffer configuration register

Address: 0x403101CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						SLOW1	SLOW0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [23:20]				DRIVE_SEL1 [19:18]		DRIVE_SEL0 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 18	DRIVE_SEL1	Sets the GPIO drive strength for IO pin 1 Default Value: 0
17 : 16	DRIVE_SEL0	Documentation: Note: DRIVE_SELx are used among GPIO cells and HSIO_STD but the encoding values may differ as shown on the right side of this table Default Value: 0 **0x0: DRIVE_SEL_ZERO :** Traveo II: GPIO_STD/GPIO_ENH: Full drive strengh: GPIO drives current at its max rated spec. Traveo II:_GPIO_SMC: GPIO_SMC default mode. Traveo II:_HSIO_STD: HSIO default mode. PSoC 6: GPIO cells and HSIO_STD cells: Full drive strength: GPIO drives current at its max rated spec.

15.1.43 GPIO_PRT3_CFG_OUT (continued)

		0x1: DRIVE_SEL_ONE : Traveo II: GPIO_STD/GPIO_ENH: Full drive strengh: GPIO drives current at its max rated spec. Traveo II:_GPIO_SMC: GPIO full drive strength. Traveo II:_HSIO_STD: GPIO full drive strength. PSoC 6: GPIO cells and HSIO_STD cells: 1/2 drive strength: GPIO drives current at 1/2 of its max rated spec **0x2: DRIVE_SEL_TWO :** Traveo II: GPIO_STD/GPIO_ENH: 1/2 drive strength: GPIO drives current at 1/2 of its max rated spec. Traveo II:_GPIO_SMC: GPIO 1/2 drive strength. Traveo II:_HSIO_STD: GPIO 1/2 drive strength. PSoC 6: GPIO cells and HSIO_STD cells: 1/4 drive strength. GPIO drives current at 1/4 of its max rated spec. **0x3: DRIVE_SEL_THREE :** Traveo II: GPIO_STD/GPIO_ENH: 1/4 drive strength: GPIO drives current at 1/4 of its max rated spec. Traveo II:_GPIO_SMC: GPIO 1/4 drive strength. Traveo II:_HSIO_STD: GPIO 1/4 drive strength. PSoC 6: GPIO cells and HSIO_STD cells: 1/8 drive strength. GPIO drives current at 1/8 of its max rated spec.
1	SLOW1	Enables slow slew rate for IO pin 1 Default Value: 0
0	SLOW0	Enables slow slew rate for IO pin 0 '0': Fast slew rate '1': Slow slew rate Default Value: 0

15.1.44 GPIO_PRT4_IN

Port input state register

Address: 0x40310210

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_IN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_IN	Reads of this register return the logical state of the filtered pin as selected in the INTR_CFG.FLT_SEL register. Default Value: 0

15.1.45 GPIO_PRT4_INTR

Port interrupt status register

Address: 0x40310214

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							FLT_IN_IN

Bits	Name	Description
24	FLT_IN_IN	Filtered pin state for pin selected by INTR_CFG.FLT_SEL Default Value: 0
8	FLT_EDGE	Edge detected on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0

15.1.46 GPIO_PRT4_INTR_MASK

Port interrupt mask register

Address: 0x40310218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Masks edge interrupt on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0

15.1.47 GPIO_PRT4_INTR_MASKED

Port interrupt masked status register

Address: 0x4031021C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Edge detected and masked on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0

15.1.48 GPIO_PRT4_INTR_SET

Port interrupt set register

Address: 0x40310220

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1S
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Sets edge detect interrupt for filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0

15.1.49 GPIO_PRT4_INTR_CFG

Port interrupt configuration register

Address: 0x40310240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by INTR_CFG.FLT_SEL Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges

15.1.50 GPIO_PRT5_OUT (continued)

15.1.50 GPIO_PRT5_OUT

Port output data register

Address: 0x40310280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	None			RW	RW	RW
HW Access	RW	RW	None			RW	RW	RW
Name	OUT7	OUT6	None [5:3]			OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	OUT7	IO output data for pin 7 Default Value: 0
6	OUT6	IO output data for pin 6 Default Value: 0
2	OUT2	IO output data for pin 2 Default Value: 0
1	OUT1	IO output data for pin 1 Default Value: 0
0	OUT0	IO output data for pin 0 '0': Output state set to '0' '1': Output state set to '1' Default Value: 0

15.1.51 GPIO_PRT5_IN

Port input state register

Address: 0x40310290

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	None			R	R	R
HW Access	W	W	None			W	W	W
Name	IN7	IN6	None [5:3]			IN2	IN1	IN0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_IN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_IN	Reads of this register return the logical state of the filtered pin as selected in the IN-TR_CFG.FLT_SEL register. Default Value: 0
7	IN7	IO pin state for pin 7 Default Value: 0
6	IN6	IO pin state for pin 6 Default Value: 0
2	IN2	IO pin state for pin 2 Default Value: 0
1	IN1	IO pin state for pin 1 Default Value: 0
0	IN0	IO pin state for pin 0 '0': Low logic level present on pin. '1': High logic level present on pin. On reset assertion , IN register will get reset. The Pad value takes 2 clock cycles to be reflected into IN Register. It's value then depends on the external pin value. Default Value: 0

15.1.52 GPIO_PRT5_INTR

Port interrupt status register

Address: 0x40310294

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	None			RW1C	RW1C	RW1C
HW Access	A	A	None			A	A	A
Name	EDGE7	EDGE6	None [5:3]			EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	None			R	R	R
HW Access	W	W	None			W	W	W
Name	IN_IN7	IN_IN6	None [21:19]			IN_IN2	IN_IN1	IN_IN0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							FLT_IN_IN

Bits	Name	Description
24	FLT_IN_IN	Filtered pin state for pin selected by INTR_CFG.FLT_SEL Default Value: 0
23	IN_IN7	IO pin state for pin 7 Default Value: 0
22	IN_IN6	IO pin state for pin 6 Default Value: 0
18	IN_IN2	IO pin state for pin 2 Default Value: 0
17	IN_IN1	IO pin state for pin 1 Default Value: 0
16	IN_IN0	IO pin state for pin 0 Default Value: 0
8	FLT_EDGE	Edge detected on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Edge detect for IO pin 7 Default Value: 0

15.1.52 GPIO_PRT5_INTR (continued)

6	EDGE6	Edge detect for IO pin 6 Default Value: 0
2	EDGE2	Edge detect for IO pin 2 Default Value: 0
1	EDGE1	Edge detect for IO pin 1 Default Value: 0
0	EDGE0	Edge detect for IO pin 0 '0': No edge was detected on pin. '1': An edge was detected on pin. Default Value: 0

15.1.53 GPIO_PRT5_INTR_MASK (continued)

15.1.53 GPIO_PRT5_INTR_MASK

Port interrupt mask register

Address: 0x40310298

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	None			RW	RW	RW
HW Access	R	R	None			R	R	R
Name	EDGE7	EDGE6	None [5:3]			EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Masks edge interrupt on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Masks edge interrupt on IO pin 7 Default Value: 0
6	EDGE6	Masks edge interrupt on IO pin 6 Default Value: 0
2	EDGE2	Masks edge interrupt on IO pin 2 Default Value: 0
1	EDGE1	Masks edge interrupt on IO pin 1 Default Value: 0
0	EDGE0	Masks edge interrupt on IO pin 0 '0': Pin interrupt forwarding disabled '1': Pin interrupt forwarding enabled Default Value: 0

15.1.54 GPIO_PRT5_INTR_MASKED

Port interrupt masked status register

Address: 0x4031029C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	None			R	R	R
HW Access	W	W	None			W	W	W
Name	EDGE7	EDGE6	None [5:3]			EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Edge detected and masked on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Edge detected and masked on IO pin 7 Default Value: 0
6	EDGE6	Edge detected and masked on IO pin 6 Default Value: 0
2	EDGE2	Edge detected and masked on IO pin 2 Default Value: 0
1	EDGE1	Edge detected and masked on IO pin 1 Default Value: 0
0	EDGE0	Edge detected AND masked on IO pin 0 '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU Default Value: 0

15.1.55 GPIO_PRT5_INTR_SET

Port interrupt set register

Address: 0x403102A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	None			RW1S	RW1S	RW1S
HW Access	A	A	None			A	A	A
Name	EDGE7	EDGE6	None [5:3]			EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1S
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Sets edge detect interrupt for filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Sets edge detect interrupt for IO pin 7 Default Value: 0
6	EDGE6	Sets edge detect interrupt for IO pin 6 Default Value: 0
2	EDGE2	Sets edge detect interrupt for IO pin 2 Default Value: 0
1	EDGE1	Sets edge detect interrupt for IO pin 1 Default Value: 0
0	EDGE0	Sets edge detect interrupt for IO pin 0 '0': Interrupt state not affected '1': Interrupt set Default Value: 0

15.1.56 GPIO_PRT5_INTR_CFG

Port interrupt configuration register

Address: 0x403102C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		None			
HW Access	R		R		None			
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		None [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by INTR_CFG.FLT_SEL Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge

15.1.56 GPIO_PRT5_INTR_CFG (continued)

		0x3: BOTH : Both rising and falling edges
15 : 14	EDGE7_SEL	Sets which edge will trigger an IRQ for IO pin 7 Default Value: 0
13 : 12	EDGE6_SEL	Sets which edge will trigger an IRQ for IO pin 6 Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pin 2 Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pin 1 Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pin 0 Default Value: 0
		0x0: DISABLE : Disabled
		0x1: RISING : Rising edge
		0x2: FALLING : Falling edge
		0x3: BOTH : Both rising and falling edges

15.1.57 GPIO_PRT5_CFG (continued)

15.1.57 GPIO_PRT5_CFG

Port configuration register

Address: 0x403102C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN1	DRIVE_MODE1 [6:4]			IN_EN0	DRIVE_MODE0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW		
HW Access	None				R	R		
Name	None [15:12]				IN_EN2	DRIVE_MODE2 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN7	DRIVE_MODE7 [30:28]			IN_EN6	DRIVE_MODE6 [26:24]		

Bits	Name	Description
31	IN_EN7	Enables the input buffer for IO pin 7 Default Value: 0
30 : 28	DRIVE_MODE7	The GPIO drive mode for IO pin 7 Default Value: 0
27	IN_EN6	Enables the input buffer for IO pin 6 Default Value: 0
26 : 24	DRIVE_MODE6	The GPIO drive mode for IO pin 6 Default Value: 0
11	IN_EN2	Enables the input buffer for IO pin 2 Default Value: 0
10 : 8	DRIVE_MODE2	The GPIO drive mode for IO pin 2 Default Value: 0
7	IN_EN1	Enables the input buffer for IO pin 1 Default Value: 0

15.1.57 GPIO_PRT5_CFG (continued)

6 : 4	DRIVE_MODE1	The GPIO drive mode for IO pin 1 Default Value: 0
3	IN_EN0	Enables the input buffer for IO pin 0. This bit should be cleared when analog signals are present on the pin to avoid crowbar currents. The output buffer can be used to drive analog signals high or low without issue. '0': Input buffer disabled '1': Input buffer enabled Default Value: 0
2 : 0	DRIVE_MODE0	The GPIO drive mode for IO pin 0. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0 **0x0: HIGHZ :** Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance **0x1: RESERVED :** This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance

15.1.57 GPIO_PRT5_CFG (continued)

0x2: PULLUP :

Resistive pull up
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Weak/resistive pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull up
D_OUT = '1': Weak/resistive pull up

0x3: PULLDOWN :

Resistive pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull down

0x4: OD_DRIVESLOW :

Open drain, drives low
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': High Impedance
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

15.1.57 GPIO_PRT5_CFG (continued)

0x5: OD_DRIVESHIGH :

Open drain, drives high
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': High Impedance
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x6: STRONG :

Strong D_OUTput buffer
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x7: PULLUP_DOWN :

Pull up or pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = '0':
GPIO_DSI_OUT = '0': Weak/resistive pull down
GPIO_DSI_OUT = '1': Weak/resistive pull up
where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT.
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull up

15.1.58 GPIO_PRT5_CFG_IN (continued)

15.1.58 GPIO_PRT5_CFG_IN

Port input buffer configuration register

Address: 0x403102C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	None			RW	RW	RW
HW Access	R	R	None			R	R	R
Name	VTRIP_-SEL7_0	VTRIP_-SEL6_0	None [5:3]			VTRIP_-SEL2_0	VTRIP_-SEL1_0	VTRIP_-SEL0_0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	VTRIP_SEL7_0	Configures the pin 7 input buffer mode (trip points and hysteresis) Default Value: 0
6	VTRIP_SEL6_0	Configures the pin 6 input buffer mode (trip points and hysteresis) Default Value: 0
2	VTRIP_SEL2_0	Configures the pin 2 input buffer mode (trip points and hysteresis) Default Value: 0
1	VTRIP_SEL1_0	Configures the pin 1 input buffer mode (trip points and hysteresis) Default Value: 0
0	VTRIP_SEL0_0	Configures the pin 0 input buffer mode (trip points and hysteresis) Default Value: 0

0x0: CMOS :

PSoC 6:: Input buffer compatible with CMOS and I2C interfaces
Traveo II: Full encoding is shown in CFG_IN_AUTOLVL.VTRIP_SEL0_1

0x1: TTL :

PSoC 6:: Input buffer compatible with TTL and MediaLB interfaces
Traveo II: full encoding is shown in CFG_IN_AUTOLVL.VTRIP_SEL0_1

15.1.59 GPIO_PRT5_CFG_OUT (continued)

15.1.59 GPIO_PRT5_CFG_OUT

Port output buffer configuration register

Address: 0x403102CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	None			RW	RW	RW
HW Access	R	R	None			R	R	R
Name	SLOW7	SLOW6	None [5:3]			SLOW2	SLOW1	SLOW0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [23:22]		DRIVE_SEL2 [21:20]		DRIVE_SEL1 [19:18]		DRIVE_SEL0 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW		None			
HW Access	R		R		None			
Name	DRIVE_SEL7 [31:30]		DRIVE_SEL6 [29:28]		None [27:24]			

Bits	Name	Description
31 : 30	DRIVE_SEL7	Sets the GPIO drive strength for IO pin 7 Default Value: 0
29 : 28	DRIVE_SEL6	Sets the GPIO drive strength for IO pin 6 Default Value: 0
21 : 20	DRIVE_SEL2	Sets the GPIO drive strength for IO pin 2 Default Value: 0
19 : 18	DRIVE_SEL1	Sets the GPIO drive strength for IO pin 1 Default Value: 0
17 : 16	DRIVE_SEL0	Documentation: Note: DRIVE_SELx are used among GPIO cells and HSIO_STD but the encoding values may differ as shown on the right side of this table Default Value: 0

0x0: DRIVE_SEL_ZERO :

Traveo II: GPIO_STD/GPIO_ENH: Full drive strengh: GPIO drives current at its max rated spec.
Traveo II:_GPIO_SMC: GPIO_SMC default mode.
Traveo II:_HSIO_STD: HSIO default mode.
PSoC 6: GPIO cells and HSIO_STD cells: Full drive strength: GPIO drives current at its max rated spec.

0x1: DRIVE_SEL_ONE :

Traveo II: GPIO_STD/GPIO_ENH: Full drive strengh: GPIO drives current at its max rated spec.
Traveo II:_GPIO_SMC: GPIO full drive strength.
Traveo II:_HSIO_STD: GPIO full drive strength.
PSoC 6: GPIO cells and HSIO_STD cells: 1/2 drive strength: GPIO drives current at 1/2 of its max rated spec

0x2: DRIVE_SEL_TWO :

Traveo II: GPIO_STD/GPIO_ENH: 1/2 drive strength: GPIO drives current at 1/2 of its max rated spec.
Traveo II:_GPIO_SMC: GPIO 1/2 drive strength.
Traveo II:_HSIO_STD: GPIO 1/2 drive strength.
PSoC 6: GPIO cells and HSIO_STD cells: 1/4 drive strength. GPIO drives current at 1/4 of its max rated spec.

0x3: DRIVE_SEL_THREE :

Traveo II: GPIO_STD/GPIO_ENH: 1/4 drive strength: GPIO drives current at 1/4 of its max rated spec.
Traveo II:_GPIO_SMC: GPIO 1/4 drive strength.
Traveo II:_HSIO_STD: GPIO 1/4 drive strength.
PSoC 6: GPIO cells and HSIO_STD cells: 1/8 drive strength. GPIO drives current at 1/8 of its max rated spec.

7	SLOW7	Enables slow slew rate for IO pin 7 Default Value: 0
6	SLOW6	Enables slow slew rate for IO pin 6 Default Value: 0
2	SLOW2	Enables slow slew rate for IO pin 2 Default Value: 0
1	SLOW1	Enables slow slew rate for IO pin 1 Default Value: 0
0	SLOW0	Enables slow slew rate for IO pin 0 '0': Fast slew rate '1': Slow slew rate Default Value: 0

15.1.60 GPIO_PRT6_OUT

Port output data register

Address: 0x40310300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	None	
HW Access	RW	RW	RW	RW	RW	RW	None	
Name	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	OUT7	IO output data for pin 7 Default Value: 0
6	OUT6	IO output data for pin 6 Default Value: 0
5	OUT5	IO output data for pin 5 Default Value: 0
4	OUT4	IO output data for pin 4 Default Value: 0
3	OUT3	IO output data for pin 3 Default Value: 0
2	OUT2	IO output data for pin 2 Default Value: 0

15.1.61 GPIO_PRT6_IN

Port input state register

Address: 0x40310310

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	None	
HW Access	W	W	W	W	W	W	None	
Name	IN7	IN6	IN5	IN4	IN3	IN2	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_IN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_IN	Reads of this register return the logical state of the filtered pin as selected in the INTR_CFG.FLT_SEL register. Default Value: 0
7	IN7	IO pin state for pin 7 Default Value: 0
6	IN6	IO pin state for pin 6 Default Value: 0
5	IN5	IO pin state for pin 5 Default Value: 0
4	IN4	IO pin state for pin 4 Default Value: 0
3	IN3	IO pin state for pin 3 Default Value: 0
2	IN2	IO pin state for pin 2 Default Value: 0

15.1.62 GPIO_PRT6_INTR (continued)

15.1.62 GPIO_PRT6_INTR

Port interrupt status register

Address: 0x40310314

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	None	
HW Access	A	A	A	A	A	A	None	
Name	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	None	
HW Access	W	W	W	W	W	W	None	
Name	IN_IN7	IN_IN6	IN_IN5	IN_IN4	IN_IN3	IN_IN2	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							FLT_IN_IN

Bits	Name	Description
24	FLT_IN_IN	Filtered pin state for pin selected by INTR_CFG.FLT_SEL Default Value: 0
23	IN_IN7	IO pin state for pin 7 Default Value: 0
22	IN_IN6	IO pin state for pin 6 Default Value: 0
21	IN_IN5	IO pin state for pin 5 Default Value: 0
20	IN_IN4	IO pin state for pin 4 Default Value: 0
19	IN_IN3	IO pin state for pin 3 Default Value: 0
18	IN_IN2	IO pin state for pin 2 Default Value: 0

8	FLT_EDGE	Edge detected on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Edge detect for IO pin 7 Default Value: 0
6	EDGE6	Edge detect for IO pin 6 Default Value: 0
5	EDGE5	Edge detect for IO pin 5 Default Value: 0
4	EDGE4	Edge detect for IO pin 4 Default Value: 0
3	EDGE3	Edge detect for IO pin 3 Default Value: 0
2	EDGE2	Edge detect for IO pin 2 Default Value: 0

15.1.63 GPIO_PRT6_INTR_MASK (continued)

15.1.63 GPIO_PRT6_INTR_MASK

Port interrupt mask register

Address: 0x40310318

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	None	
HW Access	R	R	R	R	R	R	None	
Name	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Masks edge interrupt on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Masks edge interrupt on IO pin 7 Default Value: 0
6	EDGE6	Masks edge interrupt on IO pin 6 Default Value: 0
5	EDGE5	Masks edge interrupt on IO pin 5 Default Value: 0
4	EDGE4	Masks edge interrupt on IO pin 4 Default Value: 0
3	EDGE3	Masks edge interrupt on IO pin 3 Default Value: 0
2	EDGE2	Masks edge interrupt on IO pin 2 Default Value: 0

15.1.64 GPIO_PRT6_INTR_MASKED

Port interrupt masked status register

Address: 0x4031031C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	None	
HW Access	W	W	W	W	W	W	None	
Name	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Edge detected and masked on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Edge detected and masked on IO pin 7 Default Value: 0
6	EDGE6	Edge detected and masked on IO pin 6 Default Value: 0
5	EDGE5	Edge detected and masked on IO pin 5 Default Value: 0
4	EDGE4	Edge detected and masked on IO pin 4 Default Value: 0
3	EDGE3	Edge detected and masked on IO pin 3 Default Value: 0
2	EDGE2	Edge detected and masked on IO pin 2 Default Value: 0

15.1.65 GPIO_PRT6_INTR_SET

Port interrupt set register

Address: 0x40310320

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	None	
HW Access	A	A	A	A	A	A	None	
Name	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1S
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Sets edge detect interrupt for filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Sets edge detect interrupt for IO pin 7 Default Value: 0
6	EDGE6	Sets edge detect interrupt for IO pin 6 Default Value: 0
5	EDGE5	Sets edge detect interrupt for IO pin 5 Default Value: 0
4	EDGE4	Sets edge detect interrupt for IO pin 4 Default Value: 0
3	EDGE3	Sets edge detect interrupt for IO pin 3 Default Value: 0
2	EDGE2	Sets edge detect interrupt for IO pin 2 Default Value: 0

15.1.66 GPIO_PRT6_INTR_CFG (continued)

15.1.66 GPIO_PRT6_INTR_CFG

Port interrupt configuration register

Address: 0x40310340

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		None			
HW Access	R		R		None			
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by INTR_CFG.FLT_SEL Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge

		0x3: BOTH : Both rising and falling edges
15 : 14	EDGE7_SEL	Sets which edge will trigger an IRQ for IO pin 7 Default Value: 0
13 : 12	EDGE6_SEL	Sets which edge will trigger an IRQ for IO pin 6 Default Value: 0
11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for IO pin 5 Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for IO pin 4 Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pin 3 Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pin 2 Default Value: 0

15.1.67 GPIO_PRT6_CFG (continued)

15.1.67 GPIO_PRT6_CFG

Port configuration register

Address: 0x40310344

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN3	DRIVE_MODE3 [14:12]			IN_EN2	DRIVE_MODE2 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN5	DRIVE_MODE5 [22:20]			IN_EN4	DRIVE_MODE4 [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN7	DRIVE_MODE7 [30:28]			IN_EN6	DRIVE_MODE6 [26:24]		

Bits	Name	Description
31	IN_EN7	Enables the input buffer for IO pin 7 Default Value: 0
30 : 28	DRIVE_MODE7	The GPIO drive mode for IO pin 7 Default Value: 0
27	IN_EN6	Enables the input buffer for IO pin 6 Default Value: 0
26 : 24	DRIVE_MODE6	The GPIO drive mode for IO pin 6 Default Value: 0
23	IN_EN5	Enables the input buffer for IO pin 5 Default Value: 0
22 : 20	DRIVE_MODE5	The GPIO drive mode for IO pin 5 Default Value: 0
19	IN_EN4	Enables the input buffer for IO pin 4 Default Value: 0

18 : 16	DRIVE_MODE4	The GPIO drive mode for IO pin4 Default Value: 0
15	IN_EN3	Enables the input buffer for IO pin 3 Default Value: 0
14 : 12	DRIVE_MODE3	The GPIO drive mode for IO pin 3 Default Value: 0
11	IN_EN2	Enables the input buffer for IO pin 2 Default Value: 0
10 : 8	DRIVE_MODE2	The GPIO drive mode for IO pin 2 Default Value: 0

15.1.68 GPIO_PRT6_CFG_IN (continued)

15.1.68 GPIO_PRT6_CFG_IN

Port input buffer configuration register

Address: 0x40310348

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	None	
HW Access	R	R	R	R	R	R	None	
Name	VTRIP_-SEL7_0	VTRIP_-SEL6_0	VTRIP_-SEL5_0	VTRIP_-SEL4_0	VTRIP_-SEL3_0	VTRIP_-SEL2_0	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	VTRIP_SEL7_0	Configures the pin 7 input buffer mode (trip points and hysteresis) Default Value: 0
6	VTRIP_SEL6_0	Configures the pin 6 input buffer mode (trip points and hysteresis) Default Value: 0
5	VTRIP_SEL5_0	Configures the pin 5 input buffer mode (trip points and hysteresis) Default Value: 0
4	VTRIP_SEL4_0	Configures the pin 4 input buffer mode (trip points and hysteresis) Default Value: 0
3	VTRIP_SEL3_0	Configures the pin 3 input buffer mode (trip points and hysteresis) Default Value: 0
2	VTRIP_SEL2_0	Configures the pin 2 input buffer mode (trip points and hysteresis) Default Value: 0

15.1.69 GPIO_PRT6_CFG_OUT (continued)

15.1.69 GPIO_PRT6_CFG_OUT

Port output buffer configuration register

Address: 0x4031034C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	None	
HW Access	R	R	R	R	R	R	None	
Name	SLOW7	SLOW6	SLOW5	SLOW4	SLOW3	SLOW2	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW		None			
HW Access	R		R		None			
Name	DRIVE_SEL3 [23:22]		DRIVE_SEL2 [21:20]		None [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DRIVE_SEL7 [31:30]		DRIVE_SEL6 [29:28]		DRIVE_SEL5 [27:26]		DRIVE_SEL4 [25:24]	

Bits	Name	Description
31 : 30	DRIVE_SEL7	Sets the GPIO drive strength for IO pin 7 Default Value: 0
29 : 28	DRIVE_SEL6	Sets the GPIO drive strength for IO pin 6 Default Value: 0
27 : 26	DRIVE_SEL5	Sets the GPIO drive strength for IO pin 5 Default Value: 0
25 : 24	DRIVE_SEL4	Sets the GPIO drive strength for IO pin 4 Default Value: 0
23 : 22	DRIVE_SEL3	Sets the GPIO drive strength for IO pin 3 Default Value: 0
21 : 20	DRIVE_SEL2	Sets the GPIO drive strength for IO pin 2 Default Value: 0
7	SLOW7	Enables slow slew rate for IO pin 7 Default Value: 0

6	SLOW6	Enables slow slew rate for IO pin 6 Default Value: 0
5	SLOW5	Enables slow slew rate for IO pin 5 Default Value: 0
4	SLOW4	Enables slow slew rate for IO pin 4 Default Value: 0
3	SLOW3	Enables slow slew rate for IO pin 3 Default Value: 0
2	SLOW2	Enables slow slew rate for IO pin 2 Default Value: 0

15.1.70 GPIO_PRT7_OUT (continued)

15.1.70 GPIO_PRT7_OUT

Port output data register

Address: 0x40310380

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	None	RW	RW	RW	RW	RW	RW
HW Access	RW	None	RW	RW	RW	RW	RW	RW
Name	OUT7	None	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	OUT7	IO output data for pin 7 Default Value: 0
5	OUT5	IO output data for pin 5 Default Value: 0
4	OUT4	IO output data for pin 4 Default Value: 0
3	OUT3	IO output data for pin 3 Default Value: 0
2	OUT2	IO output data for pin 2 Default Value: 0
1	OUT1	IO output data for pin 1 Default Value: 0

15.1.70 GPIO_PRT7_OUT (continued)

0	OUT0	IO output data for pin 0 '0': Output state set to '0' '1': Output state set to '1' Default Value: 0

15.1.71 GPIO_PRT7_IN

Port input state register

Address: 0x40310390

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	None	R	R	R	R	R	R
HW Access	W	None	W	W	W	W	W	W
Name	IN7	None	IN5	IN4	IN3	IN2	IN1	IN0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_IN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_IN	Reads of this register return the logical state of the filtered pin as selected in the INTR_CFG.FLT_SEL register. Default Value: 0
7	IN7	IO pin state for pin 7 Default Value: 0
5	IN5	IO pin state for pin 5 Default Value: 0
4	IN4	IO pin state for pin 4 Default Value: 0
3	IN3	IO pin state for pin 3 Default Value: 0
2	IN2	IO pin state for pin 2 Default Value: 0
1	IN1	IO pin state for pin 1 Default Value: 0

15.1.71 GPIO_PRT7_IN (continued)

0	IN0	IO pin state for pin 0 '0': Low logic level present on pin. '1': High logic level present on pin. On reset assertion , IN register will get reset. The Pad value takes 2 clock cycles to be reflected into IN Register. It's value then depends on the external pin value. Default Value: 0

15.1.72 GPIO_PRT7_INTR

Port interrupt status register

Address: 0x40310394

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	None	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	None	A	A	A	A	A	A
Name	EDGE7	None	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	R	None	R	R	R	R	R	R
HW Access	W	None	W	W	W	W	W	W
Name	IN_IN7	None	IN_IN5	IN_IN4	IN_IN3	IN_IN2	IN_IN1	IN_IN0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							FLT_IN_IN

Bits	Name	Description
24	FLT_IN_IN	Filtered pin state for pin selected by INTR_CFG.FLT_SEL Default Value: 0
23	IN_IN7	IO pin state for pin 7 Default Value: 0
21	IN_IN5	IO pin state for pin 5 Default Value: 0
20	IN_IN4	IO pin state for pin 4 Default Value: 0
19	IN_IN3	IO pin state for pin 3 Default Value: 0
18	IN_IN2	IO pin state for pin 2 Default Value: 0
17	IN_IN1	IO pin state for pin 1 Default Value: 0
16	IN_IN0	IO pin state for pin 0 Default Value: 0

15.1.72 GPIO_PRT7_INTR (continued)

8	FLT_EDGE	Edge detected on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Edge detect for IO pin 7 Default Value: 0
5	EDGE5	Edge detect for IO pin 5 Default Value: 0
4	EDGE4	Edge detect for IO pin 4 Default Value: 0
3	EDGE3	Edge detect for IO pin 3 Default Value: 0
2	EDGE2	Edge detect for IO pin 2 Default Value: 0
1	EDGE1	Edge detect for IO pin 1 Default Value: 0
0	EDGE0	Edge detect for IO pin 0 '0': No edge was detected on pin. '1': An edge was detected on pin. Default Value: 0

15.1.73 GPIO_PRT7_INTR_MASK

Port interrupt mask register

Address: 0x40310398

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	None	RW	RW	RW	RW	RW	RW
HW Access	R	None	R	R	R	R	R	R
Name	EDGE7	None	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Masks edge interrupt on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Masks edge interrupt on IO pin 7 Default Value: 0
5	EDGE5	Masks edge interrupt on IO pin 5 Default Value: 0
4	EDGE4	Masks edge interrupt on IO pin 4 Default Value: 0
3	EDGE3	Masks edge interrupt on IO pin 3 Default Value: 0
2	EDGE2	Masks edge interrupt on IO pin 2 Default Value: 0
1	EDGE1	Masks edge interrupt on IO pin 1 Default Value: 0

15.1.73 GPIO_PRT7_INTR_MASK (continued)

0	EDGE0	Masks edge interrupt on IO pin 0 '0': Pin interrupt forwarding disabled '1': Pin interrupt forwarding enabled Default Value: 0

15.1.74 GPIO_PRT7_INTR_MASKED

Port interrupt masked status register

Address: 0x4031039C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	None	R	R	R	R	R	R
HW Access	W	None	W	W	W	W	W	W
Name	EDGE7	None	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Edge detected and masked on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Edge detected and masked on IO pin 7 Default Value: 0
5	EDGE5	Edge detected and masked on IO pin 5 Default Value: 0
4	EDGE4	Edge detected and masked on IO pin 4 Default Value: 0
3	EDGE3	Edge detected and masked on IO pin 3 Default Value: 0
2	EDGE2	Edge detected and masked on IO pin 2 Default Value: 0
1	EDGE1	Edge detected and masked on IO pin 1 Default Value: 0

15.1.74 GPIO_PRT7_INTR_MASKED (continued)

0	EDGE0	Edge detected AND masked on IO pin 0 '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU Default Value: 0

15.1.75 GPIO_PRT7_INTR_SET

Port interrupt set register

Address: 0x403103A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	None	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	None	A	A	A	A	A	A
Name	EDGE7	None	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1S
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Sets edge detect interrupt for filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Sets edge detect interrupt for IO pin 7 Default Value: 0
5	EDGE5	Sets edge detect interrupt for IO pin 5 Default Value: 0
4	EDGE4	Sets edge detect interrupt for IO pin 4 Default Value: 0
3	EDGE3	Sets edge detect interrupt for IO pin 3 Default Value: 0
2	EDGE2	Sets edge detect interrupt for IO pin 2 Default Value: 0
1	EDGE1	Sets edge detect interrupt for IO pin 1 Default Value: 0

15.1.75 GPIO_PRT7_INTR_SET (continued)

0	EDGE0	Sets edge detect interrupt for IO pin 0 '0': Interrupt state not affected '1': Interrupt set Default Value: 0

15.1.76 GPIO_PRT7_INTR_CFG

Port interrupt configuration register

Address: 0x403103C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None		RW		RW	
HW Access	R		None		R		R	
Name	EDGE7_SEL [15:14]		None [13:12]		EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by INTR_CFG.FLT_SEL Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge

15.1.76 GPIO_PRT7_INTR_CFG (continued)

		0x3: BOTH : Both rising and falling edges
15 : 14	EDGE7_SEL	Sets which edge will trigger an IRQ for IO pin 7 Default Value: 0
11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for IO pin 5 Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for IO pin 4 Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pin 3 Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pin 2 Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pin 1 Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pin 0 Default Value: 0
		0x0: DISABLE : Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges

15.1.77 GPIO_PRT7_CFG (continued)

15.1.77 GPIO_PRT7_CFG

Port configuration register

Address: 0x403103C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN1	DRIVE_MODE1 [6:4]			IN_EN0	DRIVE_MODE0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN3	DRIVE_MODE3 [14:12]			IN_EN2	DRIVE_MODE2 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN5	DRIVE_MODE5 [22:20]			IN_EN4	DRIVE_MODE4 [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW			None			
HW Access	R	R			None			
Name	IN_EN7	DRIVE_MODE7 [30:28]			None [27:24]			

Bits	Name	Description
31	IN_EN7	Enables the input buffer for IO pin 7 Default Value: 0
30 : 28	DRIVE_MODE7	The GPIO drive mode for IO pin 7 Default Value: 0
23	IN_EN5	Enables the input buffer for IO pin 5 Default Value: 0
22 : 20	DRIVE_MODE5	The GPIO drive mode for IO pin 5 Default Value: 0
19	IN_EN4	Enables the input buffer for IO pin 4 Default Value: 0
18 : 16	DRIVE_MODE4	The GPIO drive mode for IO pin4 Default Value: 0
15	IN_EN3	Enables the input buffer for IO pin 3 Default Value: 0

15.1.77 GPIO_PRT7_CFG (continued)

14 : 12	DRIVE_MODE3	The GPIO drive mode for IO pin 3 Default Value: 0
11	IN_EN2	Enables the input buffer for IO pin 2 Default Value: 0
10 : 8	DRIVE_MODE2	The GPIO drive mode for IO pin 2 Default Value: 0
7	IN_EN1	Enables the input buffer for IO pin 1 Default Value: 0
6 : 4	DRIVE_MODE1	The GPIO drive mode for IO pin 1 Default Value: 0
3	IN_EN0	Enables the input buffer for IO pin 0. This bit should be cleared when analog signals are present on the pin to avoid crowbar currents. The output buffer can be used to drive analog signals high or low without issue. '0': Input buffer disabled '1': Input buffer enabled Default Value: 0
2 : 0	DRIVE_MODE0	The GPIO drive mode for IO pin 0. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0 **0x0: HIGHZ :** Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance **0x1: RESERVED :** This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance

15.1.77 GPIO_PRT7_CFG (continued)

0x2: PULLUP :

Resistive pull up
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Weak/resistive pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull up
D_OUT = '1': Weak/resistive pull up

0x3: PULLDOWN :

Resistive pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull down

0x4: OD_DRIVESLOW :

Open drain, drives low
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': High Impedance
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

15.1.77 GPIO_PRT7_CFG (continued)

0x5: OD_DRIVESHIGH :

Open drain, drives high
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': High Impedance
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x6: STRONG :

Strong D_OUTput buffer
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x7: PULLUP_DOWN :

Pull up or pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = '0':
GPIO_DSI_OUT = '0': Weak/resistive pull down
GPIO_DSI_OUT = '1': Weak/resistive pull up
where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT.
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull up

15.1.78 GPIO_PRT7_CFG_IN

Port input buffer configuration register

Address: 0x403103C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	None	RW	RW	RW	RW	RW	RW
HW Access	R	None	R	R	R	R	R	R
Name	VTRIP_-SEL7_0	None	VTRIP_-SEL5_0	VTRIP_-SEL4_0	VTRIP_-SEL3_0	VTRIP_-SEL2_0	VTRIP_-SEL1_0	VTRIP_-SEL0_0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	VTRIP_SEL7_0	Configures the pin 7 input buffer mode (trip points and hysteresis) Default Value: 0
5	VTRIP_SEL5_0	Configures the pin 5 input buffer mode (trip points and hysteresis) Default Value: 0
4	VTRIP_SEL4_0	Configures the pin 4 input buffer mode (trip points and hysteresis) Default Value: 0
3	VTRIP_SEL3_0	Configures the pin 3 input buffer mode (trip points and hysteresis) Default Value: 0
2	VTRIP_SEL2_0	Configures the pin 2 input buffer mode (trip points and hysteresis) Default Value: 0
1	VTRIP_SEL1_0	Configures the pin 1 input buffer mode (trip points and hysteresis) Default Value: 0
0	VTRIP_SEL0_0	Configures the pin 0 input buffer mode (trip points and hysteresis) Default Value: 0

15.1.78 GPIO_PRT7_CFG_IN (continued)

0x0: CMOS :

PSoC 6:: Input buffer compatible with CMOS and I2C interfaces
Traveo II: Full encoding is shown in CFG_IN_AUTOLVL.VTRIP_SEL0_1

0x1: TTL :

PSoC 6:: Input buffer compatible with TTL and MediaLB interfaces
Traveo II: full encoding is shown in CFG_IN_AUTOLVL.VTRIP_SEL0_1

15.1.79 GPIO_PRT7_CFG_OUT

Port output buffer configuration register

Address: 0x403103CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	None	RW	RW	RW	RW	RW	RW
HW Access	R	None	R	R	R	R	R	R
Name	SLOW7	None	SLOW5	SLOW4	SLOW3	SLOW2	SLOW1	SLOW0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DRIVE_SEL3 [23:22]		DRIVE_SEL2 [21:20]		DRIVE_SEL1 [19:18]		DRIVE_SEL0 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None		RW		RW	
HW Access	R		None		R		R	
Name	DRIVE_SEL7 [31:30]		None [29:28]		DRIVE_SEL5 [27:26]		DRIVE_SEL4 [25:24]	

Bits	Name	Description
31 : 30	DRIVE_SEL7	Sets the GPIO drive strength for IO pin 7 Default Value: 0
27 : 26	DRIVE_SEL5	Sets the GPIO drive strength for IO pin 5 Default Value: 0
25 : 24	DRIVE_SEL4	Sets the GPIO drive strength for IO pin 4 Default Value: 0
23 : 22	DRIVE_SEL3	Sets the GPIO drive strength for IO pin 3 Default Value: 0
21 : 20	DRIVE_SEL2	Sets the GPIO drive strength for IO pin 2 Default Value: 0
19 : 18	DRIVE_SEL1	Sets the GPIO drive strength for IO pin 1 Default Value: 0
17 : 16	DRIVE_SEL0	Documentation: Note: DRIVE_SELx are used among GPIO cells and HSIO_STD but the encoding values may differ as shown on the right side of this table Default Value: 0

15.1.79 GPIO_PRT7_CFG_OUT (continued)

0x0: DRIVE_SEL_ZERO :

Traveo II: GPIO_STD/GPIO_ENH: Full drive strengh: GPIO drives current at its max rated spec.
Traveo II:_GPIO_SMC: GPIO_SMC default mode.
Traveo II:_HSIO_STD: HSIO default mode.
PSoC 6: GPIO cells and HSIO_STD cells: Full drive strength: GPIO drives current at its max rated spec.

0x1: DRIVE_SEL_ONE :

Traveo II: GPIO_STD/GPIO_ENH: Full drive strengh: GPIO drives current at its max rated spec.
Traveo II:_GPIO_SMC: GPIO full drive strength.
Traveo II:_HSIO_STD: GPIO full drive strength.
PSoC 6: GPIO cells and HSIO_STD cells: 1/2 drive strength: GPIO drives current at 1/2 of its max rated spec

0x2: DRIVE_SEL_TWO :

Traveo II: GPIO_STD/GPIO_ENH: 1/2 drive strength: GPIO drives current at 1/2 of its max rated spec.
Traveo II:_GPIO_SMC: GPIO 1/2 drive strength.
Traveo II:_HSIO_STD: GPIO 1/2 drive strength.
PSoC 6: GPIO cells and HSIO_STD cells: 1/4 drive strength. GPIO drives current at 1/4 of its max rated spec.

0x3: DRIVE_SEL_THREE :

Traveo II: GPIO_STD/GPIO_ENH: 1/4 drive strength: GPIO drives current at 1/4 of its max rated spec.
Traveo II:_GPIO_SMC: GPIO 1/4 drive strength.
Traveo II:_HSIO_STD: GPIO 1/4 drive strength.
PSoC 6: GPIO cells and HSIO_STD cells: 1/8 drive strength. GPIO drives current at 1/8 of its max rated spec.

7	SLOW7	Enables slow slew rate for IO pin 7 Default Value: 0
5	SLOW5	Enables slow slew rate for IO pin 5 Default Value: 0
4	SLOW4	Enables slow slew rate for IO pin 4 Default Value: 0
3	SLOW3	Enables slow slew rate for IO pin 3 Default Value: 0
2	SLOW2	Enables slow slew rate for IO pin 2 Default Value: 0
1	SLOW1	Enables slow slew rate for IO pin 1 Default Value: 0
0	SLOW0	Enables slow slew rate for IO pin 0 '0': Fast slew rate '1': Slow slew rate Default Value: 0

15.1.80 GPIO_PRT11_OUT

Port output data register

Address: 0x40310580

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	None
HW Access	RW	RW	RW	RW	RW	RW	RW	None
Name	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	OUT7	IO output data for pin 7 Default Value: 0
6	OUT6	IO output data for pin 6 Default Value: 0
5	OUT5	IO output data for pin 5 Default Value: 0
4	OUT4	IO output data for pin 4 Default Value: 0
3	OUT3	IO output data for pin 3 Default Value: 0
2	OUT2	IO output data for pin 2 Default Value: 0
1	OUT1	IO output data for pin 1 Default Value: 0

15.1.81 GPIO_PRT11_IN (continued)

15.1.81 GPIO_PRT11_IN

Port input state register

Address: 0x40310590

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	None
HW Access	W	W	W	W	W	W	W	None
Name	IN7	IN6	IN5	IN4	IN3	IN2	IN1	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_IN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_IN	Reads of this register return the logical state of the filtered pin as selected in the IN-TR_CFG.FLT_SEL register. Default Value: 0
7	IN7	IO pin state for pin 7 Default Value: 0
6	IN6	IO pin state for pin 6 Default Value: 0
5	IN5	IO pin state for pin 5 Default Value: 0
4	IN4	IO pin state for pin 4 Default Value: 0
3	IN3	IO pin state for pin 3 Default Value: 0
2	IN2	IO pin state for pin 2 Default Value: 0

15.1.81 GPIO_PRT11_IN (continued)

1	IN1	IO pin state for pin 1 Default Value: 0

15.1.82 GPIO_PRT11_INTR

Port interrupt status register

Address: 0x40310594

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	None
HW Access	A	A	A	A	A	A	A	None
Name	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	None
HW Access	W	W	W	W	W	W	W	None
Name	IN_IN7	IN_IN6	IN_IN5	IN_IN4	IN_IN3	IN_IN2	IN_IN1	None

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							FLT_IN_IN

Bits	Name	Description
24	FLT_IN_IN	Filtered pin state for pin selected by INTR_CFG.FLT_SEL Default Value: 0
23	IN_IN7	IO pin state for pin 7 Default Value: 0
22	IN_IN6	IO pin state for pin 6 Default Value: 0
21	IN_IN5	IO pin state for pin 5 Default Value: 0
20	IN_IN4	IO pin state for pin 4 Default Value: 0
19	IN_IN3	IO pin state for pin 3 Default Value: 0
18	IN_IN2	IO pin state for pin 2 Default Value: 0
17	IN_IN1	IO pin state for pin 1 Default Value: 0

15.1.82 GPIO_PRT11_INTR (continued)

8	FLT_EDGE	Edge detected on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Edge detect for IO pin 7 Default Value: 0
6	EDGE6	Edge detect for IO pin 6 Default Value: 0
5	EDGE5	Edge detect for IO pin 5 Default Value: 0
4	EDGE4	Edge detect for IO pin 4 Default Value: 0
3	EDGE3	Edge detect for IO pin 3 Default Value: 0
2	EDGE2	Edge detect for IO pin 2 Default Value: 0
1	EDGE1	Edge detect for IO pin 1 Default Value: 0

15.1.83 GPIO_PRT11_INTR_MASK

Port interrupt mask register

Address: 0x40310598

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	None
HW Access	R	R	R	R	R	R	R	None
Name	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Masks edge interrupt on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Masks edge interrupt on IO pin 7 Default Value: 0
6	EDGE6	Masks edge interrupt on IO pin 6 Default Value: 0
5	EDGE5	Masks edge interrupt on IO pin 5 Default Value: 0
4	EDGE4	Masks edge interrupt on IO pin 4 Default Value: 0
3	EDGE3	Masks edge interrupt on IO pin 3 Default Value: 0
2	EDGE2	Masks edge interrupt on IO pin 2 Default Value: 0
1	EDGE1	Masks edge interrupt on IO pin 1 Default Value: 0

15.1.84 GPIO_PRT11_INTR_MASKED (continued)

15.1.84 GPIO_PRT11_INTR_MASKED

Port interrupt masked status register

Address: 0x4031059C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	None
HW Access	W	W	W	W	W	W	W	None
Name	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Edge detected and masked on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Edge detected and masked on IO pin 7 Default Value: 0
6	EDGE6	Edge detected and masked on IO pin 6 Default Value: 0
5	EDGE5	Edge detected and masked on IO pin 5 Default Value: 0
4	EDGE4	Edge detected and masked on IO pin 4 Default Value: 0
3	EDGE3	Edge detected and masked on IO pin 3 Default Value: 0
2	EDGE2	Edge detected and masked on IO pin 2 Default Value: 0

1	EDGE1	Edge detected and masked on IO pin 1 Default Value: 0

15.1.85 GPIO_PRT11_INTR_SET (continued)

15.1.85 GPIO_PRT11_INTR_SET

Port interrupt set register

Address: 0x403105A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	None
HW Access	A	A	A	A	A	A	A	None
Name	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1S
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Sets edge detect interrupt for filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Sets edge detect interrupt for IO pin 7 Default Value: 0
6	EDGE6	Sets edge detect interrupt for IO pin 6 Default Value: 0
5	EDGE5	Sets edge detect interrupt for IO pin 5 Default Value: 0
4	EDGE4	Sets edge detect interrupt for IO pin 4 Default Value: 0
3	EDGE3	Sets edge detect interrupt for IO pin 3 Default Value: 0
2	EDGE2	Sets edge detect interrupt for IO pin 2 Default Value: 0

15.1.85 GPIO_PRT11_INTR_SET (continued)

1	EDGE1	Sets edge detect interrupt for IO pin 1 Default Value: 0

15.1.86 GPIO_PRT11_INTR_CFG

Port interrupt configuration register

Address: 0x403105C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		None	
HW Access	R		R		R		None	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by INTR_CFG.FLT_SEL Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge

15.1.86 GPIO_PRT11_INTR_CFG (continued)

		0x3: BOTH : Both rising and falling edges
15 : 14	EDGE7_SEL	Sets which edge will trigger an IRQ for IO pin 7 Default Value: 0
13 : 12	EDGE6_SEL	Sets which edge will trigger an IRQ for IO pin 6 Default Value: 0
11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for IO pin 5 Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for IO pin 4 Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pin 3 Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pin 2 Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pin 1 Default Value: 0

15.1.87 GPIO_PRT11_CFG

Port configuration register

Address: 0x403105C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			None			
HW Access	R	R			None			
Name	IN_EN1	DRIVE_MODE1 [6:4]			None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN3	DRIVE_MODE3 [14:12]			IN_EN2	DRIVE_MODE2 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN5	DRIVE_MODE5 [22:20]			IN_EN4	DRIVE_MODE4 [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN7	DRIVE_MODE7 [30:28]			IN_EN6	DRIVE_MODE6 [26:24]		

Bits	Name	Description
31	IN_EN7	Enables the input buffer for IO pin 7 Default Value: 0
30 : 28	DRIVE_MODE7	The GPIO drive mode for IO pin 7 Default Value: 0
27	IN_EN6	Enables the input buffer for IO pin 6 Default Value: 0
26 : 24	DRIVE_MODE6	The GPIO drive mode for IO pin 6 Default Value: 0
23	IN_EN5	Enables the input buffer for IO pin 5 Default Value: 0
22 : 20	DRIVE_MODE5	The GPIO drive mode for IO pin 5 Default Value: 0
19	IN_EN4	Enables the input buffer for IO pin 4 Default Value: 0
18 : 16	DRIVE_MODE4	The GPIO drive mode for IO pin4 Default Value: 0

15	IN_EN3	Enables the input buffer for IO pin 3 Default Value: 0
14 : 12	DRIVE_MODE3	The GPIO drive mode for IO pin 3 Default Value: 0
11	IN_EN2	Enables the input buffer for IO pin 2 Default Value: 0
10 : 8	DRIVE_MODE2	The GPIO drive mode for IO pin 2 Default Value: 0
7	IN_EN1	Enables the input buffer for IO pin 1 Default Value: 0
6 : 4	DRIVE_MODE1	The GPIO drive mode for IO pin 1 Default Value: 0

15.1.88 GPIO_PRT11_CFG_IN (continued)

15.1.88 GPIO_PRT11_CFG_IN

Port input buffer configuration register

Address: 0x403105C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	None
HW Access	R	R	R	R	R	R	R	None
Name	VTRIP_-SEL7_0	VTRIP_-SEL6_0	VTRIP_-SEL5_0	VTRIP_-SEL4_0	VTRIP_-SEL3_0	VTRIP_-SEL2_0	VTRIP_-SEL1_0	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	VTRIP_SEL7_0	Configures the pin 7 input buffer mode (trip points and hysteresis) Default Value: 0
6	VTRIP_SEL6_0	Configures the pin 6 input buffer mode (trip points and hysteresis) Default Value: 0
5	VTRIP_SEL5_0	Configures the pin 5 input buffer mode (trip points and hysteresis) Default Value: 0
4	VTRIP_SEL4_0	Configures the pin 4 input buffer mode (trip points and hysteresis) Default Value: 0
3	VTRIP_SEL3_0	Configures the pin 3 input buffer mode (trip points and hysteresis) Default Value: 0
2	VTRIP_SEL2_0	Configures the pin 2 input buffer mode (trip points and hysteresis) Default Value: 0
1	VTRIP_SEL1_0	Configures the pin 1 input buffer mode (trip points and hysteresis) Default Value: 0

15.1.89 GPIO_PRT11_CFG_OUT

Port output buffer configuration register

Address: 0x403105CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	None
HW Access	R	R	R	R	R	R	R	None
Name	SLOW7	SLOW6	SLOW5	SLOW4	SLOW3	SLOW2	SLOW1	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW		RW		None	
HW Access	R		R		R		None	
Name	DRIVE_SEL3 [23:22]		DRIVE_SEL2 [21:20]		DRIVE_SEL1 [19:18]		None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DRIVE_SEL7 [31:30]		DRIVE_SEL6 [29:28]		DRIVE_SEL5 [27:26]		DRIVE_SEL4 [25:24]	

Bits	Name	Description
31 : 30	DRIVE_SEL7	Sets the GPIO drive strength for IO pin 7 Default Value: 0
29 : 28	DRIVE_SEL6	Sets the GPIO drive strength for IO pin 6 Default Value: 0
27 : 26	DRIVE_SEL5	Sets the GPIO drive strength for IO pin 5 Default Value: 0
25 : 24	DRIVE_SEL4	Sets the GPIO drive strength for IO pin 4 Default Value: 0
23 : 22	DRIVE_SEL3	Sets the GPIO drive strength for IO pin 3 Default Value: 0
21 : 20	DRIVE_SEL2	Sets the GPIO drive strength for IO pin 2 Default Value: 0
19 : 18	DRIVE_SEL1	Sets the GPIO drive strength for IO pin 1 Default Value: 0
7	SLOW7	Enables slow slew rate for IO pin 7 Default Value: 0

6	SLOW6	Enables slow slew rate for IO pin 6 Default Value: 0
5	SLOW5	Enables slow slew rate for IO pin 5 Default Value: 0
4	SLOW4	Enables slow slew rate for IO pin 4 Default Value: 0
3	SLOW3	Enables slow slew rate for IO pin 3 Default Value: 0
2	SLOW2	Enables slow slew rate for IO pin 2 Default Value: 0
1	SLOW1	Enables slow slew rate for IO pin 1 Default Value: 0

15.1.90 GPIO_PRT12_OUT

Port output data register

Address: 0x40310600

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	None					
HW Access	RW	RW	None					
Name	OUT7	OUT6	None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	OUT7	IO output data for pin 7 Default Value: 0
6	OUT6	IO output data for pin 6 Default Value: 0

15.1.91 GPIO_PRT12_IN

Port input state register

Address: 0x40310610

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	None					
HW Access	W	W	None					
Name	IN7	IN6	None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_IN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_IN	Reads of this register return the logical state of the filtered pin as selected in the INTR_CFG.FLT_SEL register. Default Value: 0
7	IN7	IO pin state for pin 7 Default Value: 0
6	IN6	IO pin state for pin 6 Default Value: 0

15.1.92 GPIO_PRT12_INTR (continued)

15.1.92 GPIO_PRT12_INTR

Port interrupt status register

Address: 0x40310614

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	None					
HW Access	A	A	None					
Name	EDGE7	EDGE6	None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	None					
HW Access	W	W	None					
Name	IN_IN7	IN_IN6	None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							FLT_IN_IN

Bits	Name	Description
24	FLT_IN_IN	Filtered pin state for pin selected by INTR_CFG.FLT_SEL Default Value: 0
23	IN_IN7	IO pin state for pin 7 Default Value: 0
22	IN_IN6	IO pin state for pin 6 Default Value: 0
8	FLT_EDGE	Edge detected on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Edge detect for IO pin 7 Default Value: 0
6	EDGE6	Edge detect for IO pin 6 Default Value: 0

15.1.93 GPIO_PRT12_INTR_MASK

Port interrupt mask register

Address: 0x40310618

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	EDGE7	EDGE6	None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Masks edge interrupt on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Masks edge interrupt on IO pin 7 Default Value: 0
6	EDGE6	Masks edge interrupt on IO pin 6 Default Value: 0

15.1.94 GPIO_PRT12_INTR_MASKED

Port interrupt masked status register

Address: 0x4031061C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	None					
HW Access	W	W	None					
Name	EDGE7	EDGE6	None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Edge detected and masked on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Edge detected and masked on IO pin 7 Default Value: 0
6	EDGE6	Edge detected and masked on IO pin 6 Default Value: 0

15.1.95 GPIO_PRT12_INTR_SET (continued)

15.1.95 GPIO_PRT12_INTR_SET

Port interrupt set register

Address: 0x40310620

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	None					
HW Access	A	A	None					
Name	EDGE7	EDGE6	None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1S
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Sets edge detect interrupt for filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Sets edge detect interrupt for IO pin 7 Default Value: 0
6	EDGE6	Sets edge detect interrupt for IO pin 6 Default Value: 0

15.1.96 GPIO_PRT12_INTR_CFG

Port interrupt configuration register

Address: 0x40310640

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		None			
HW Access	R		R		None			
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		None [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by INTR_CFG.FLT_SEL Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge

		0x3: BOTH : Both rising and falling edges
15 : 14	EDGE7_SEL	Sets which edge will trigger an IRQ for IO pin 7 Default Value: 0
13 : 12	EDGE6_SEL	Sets which edge will trigger an IRQ for IO pin 6 Default Value: 0

15.1.97 GPIO_PRT12_CFG (continued)

15.1.97 GPIO_PRT12_CFG

Port configuration register

Address: 0x40310644

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN7	DRIVE_MODE7 [30:28]			IN_EN6	DRIVE_MODE6 [26:24]		

Bits	Name	Description
31	IN_EN7	Enables the input buffer for IO pin 7 Default Value: 0
30 : 28	DRIVE_MODE7	The GPIO drive mode for IO pin 7 Default Value: 0
27	IN_EN6	Enables the input buffer for IO pin 6 Default Value: 0
26 : 24	DRIVE_MODE6	The GPIO drive mode for IO pin 6 Default Value: 0

15.1.98 GPIO_PRT12_CFG_IN

Port input buffer configuration register

Address: 0x40310648

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	VTRIP_-SEL7_0	VTRIP_-SEL6_0	None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	VTRIP_SEL7_0	Configures the pin 7 input buffer mode (trip points and hysteresis) Default Value: 0
6	VTRIP_SEL6_0	Configures the pin 6 input buffer mode (trip points and hysteresis) Default Value: 0

15.1.99 GPIO_PRT12_CFG_OUT

Port output buffer configuration register

Address: 0x4031064C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	SLOW7	SLOW6	None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW		None			
HW Access	R		R		None			
Name	DRIVE_SEL7 [31:30]		DRIVE_SEL6 [29:28]		None [27:24]			

Bits	Name	Description
31 : 30	DRIVE_SEL7	Sets the GPIO drive strength for IO pin 7 Default Value: 0
29 : 28	DRIVE_SEL6	Sets the GPIO drive strength for IO pin 6 Default Value: 0
7	SLOW7	Enables slow slew rate for IO pin 7 Default Value: 0
6	SLOW6	Enables slow slew rate for IO pin 6 Default Value: 0

15.1.100 GPIO_INTR_CAUSE0 (continued)

15.1.100 GPIO_INTR_CAUSE0

Interrupt port cause register 0

Address: 0x40314000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	PORT_INT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None	R						
HW Access	None	W						
Name	None	PORT_INT [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14 : 0	PORT_INT	Each IO port has an associated bit field in this register. The bit field reflects the IO port's interrupt line (bit field i reflects "gpio_interrupts[i]" for IO port i). The register is used when the system uses a combined interrupt line "gpio_interrupt". The software ISR reads the register to determine which IO port(s) is responsible for the combined interrupt line. Once, the IO port(s) is determined, the IO port's GPIO_PRT_INTR register is read to determine the IO pin(s) in the IO port that caused the interrupt. '0': Port has no pending interrupt '1': Port has pending interrupt Default Value: 0

15.1.101 GPIO_VDD_ACTIVE

Extern power supply detection register

Address: 0x40314010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R					
HW Access	None		W					
Name	None [7:6]		VDDIO_ACTIVE [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	W	W	None					
Name	VDDD_ACTIVE	VDDA_ACTIVE	None [29:24]					

Bits	Name	Description
31	VDDD_ACTIVE	This bit indicates presence of the VDDD supply. This bit will always read-back 1. The VDDD supply has robust brown-out protection monitoring and it is not possible to read back this register without a valid supply. (This bit is used in certain test-modes to observe the brown-out detector status.) Default Value: 0
30	VDDA_ACTIVE	Same as VDDIO_ACTIVE for the analog supply VDDA. Default Value: 0

5 : 0	VDDIO_ACTIVE	Indicates presence or absence of VDDIO supplies (i.e. other than VDDD, VDDA) on the device (supplies are numbered 0..n-1). Note that VDDIO supplies have basic (crude) supply detectors only. If separate, robust, brown-out detection is desired on IO supplies, on-chip or off-chip analog resources need to provide it. For these bits to work reliable, the supply must be within valid spec range (per datasheet) or held at ground. Any in-between voltage has an undefined result. '0': Supply is not present '1': Supply is present When multiple VDDIO supplies are present, they will be assigned in alphanumeric ascending order to these bits during implementation. For example "vddusb, vddio_0, vddio_a, vbackup, vddio_r, vddio_1" are present then they will be assigned to these bits as below: 0: vbackup, 1: vddio_0, 2: vddio_1, 3: vddio_a, 4: vddio_r, 5: vddusb" Default Value: 0

15.1.102 GPIO_VDD_INTR

Supply detection interrupt register

Address: 0x40314014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1C					
HW Access	None		A					
Name	None [7:6]		VDDIO_ACTIVE [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C	RW1C	None					
HW Access	A	A	None					
Name	VDDD_ACTIVE	VDDA_ACTIVE	None [29:24]					

Bits	Name	Description
31	VDDD_ACTIVE	The VDDD supply is always present during operation so a supply transition can not occur. This bit will always read back '1'. Default Value: 0
30	VDDA_ACTIVE	Same as VDDIO_ACTIVE for the analog supply VDDA. Default Value: 0
5 : 0	VDDIO_ACTIVE	Supply state change detected. '0': No change to supply detected '1': Change to supply detected Default Value: 0

15.1.103 GPIO_VDD_INTR_MASK

Supply detection interrupt mask register

Address: 0x40314018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		VDDIO_ACTIVE [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	VDDD_ACTIVE	VDDA_ACTIVE	None [29:24]					

Bits	Name	Description
31	VDDD_ACTIVE	Same as VDDIO_ACTIVE for the digital supply VDDD. Default Value: 0
30	VDDA_ACTIVE	Same as VDDIO_ACTIVE for the analog supply VDDA. Default Value: 0
5 : 0	VDDIO_ACTIVE	Masks supply interrupt on VDDIO. '0': VDDIO interrupt forwarding disabled '1': VDDIO interrupt forwarding enabled Default Value: 0

15.1.104 GPIO_VDD_INTR_MASKED (continued)

15.1.104 GPIO_VDD_INTR_MASKED

Supply detection interrupt masked register

Address: 0x4031401C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R					
HW Access	None		W					
Name	None [7:6]		VDDIO_ACTIVE [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	W	W	None					
Name	VDDD_ACTIVE	VDDA_ACTIVE	None [29:24]					

Bits	Name	Description
31	VDDD_ACTIVE	Same as VDDIO_ACTIVE for the digital supply VDDD. Default Value: 0
30	VDDA_ACTIVE	Same as VDDIO_ACTIVE for the analog supply VDDA. Default Value: 0
5 : 0	VDDIO_ACTIVE	Supply transition detected AND masked '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU Default Value: 0

15.1.105 GPIO_VDD_INTR_SET (continued)

15.1.105 GPIO_VDD_INTR_SET

Supply detection interrupt set register

Address: 0x40314020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1S					
HW Access	None		A					
Name	None [7:6]		VDDIO_ACTIVE [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	RW1S	None					
HW Access	A	A	None					
Name	VDDD_ACTIVE	VDDA_ACTIVE	None [29:24]					

Bits	Name	Description
31	VDDD_ACTIVE	Same as VDDIO_ACTIVE for the digital supply VDDD. Default Value: 0
30	VDDA_ACTIVE	Same as VDDIO_ACTIVE for the analog supply VDDA. Default Value: 0
5 : 0	VDDIO_ACTIVE	Sets supply interrupt. '0': Interrupt state not affected '1': Interrupt set Default Value: 0

16 Smart I/O Registers

This section discusses the Smart I/O registers. It lists all the registers in mapping tables, in address order.

16.1 Register Details

Register	Address	Description
SMARTIO_PRT9_CTL	0x40320900	Control register
SMARTIO_PRT9_SYNC_CTL	0x40320910	Synchronization control register
SMARTIO_PRT9_LUT_SEL0	0x40320920	LUT component input selection
SMARTIO_PRT9_LUT_SEL1	0x40320924	LUT component input selection. See SMARTIO_PRT9_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT9_LUT_SEL2	0x40320928	LUT component input selection. See SMARTIO_PRT9_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT9_LUT_SEL3	0x4032092C	LUT component input selection. See SMARTIO_PRT9_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT9_LUT_SEL4	0x40320930	LUT component input selection. See SMARTIO_PRT9_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT9_LUT_SEL5	0x40320934	LUT component input selection. See SMARTIO_PRT9_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT9_LUT_SEL6	0x40320938	LUT component input selection. See SMARTIO_PRT9_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT9_LUT_SEL7	0x4032093C	LUT component input selection. See SMARTIO_PRT9_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT9_LUT_CTL0	0x40320940	LUT component control register
SMARTIO_PRT9_LUT_CTL1	0x40320944	LUT component control register. See SMARTIO_PRT9_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT9_LUT_CTL2	0x40320948	LUT component control register. See SMARTIO_PRT9_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT9_LUT_CTL3	0x4032094C	LUT component control register. See SMARTIO_PRT9_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT9_LUT_CTL4	0x40320950	LUT component control register. See SMARTIO_PRT9_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT9_LUT_CTL5	0x40320954	LUT component control register. See SMARTIO_PRT9_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT9_LUT_CTL6	0x40320958	LUT component control register. See SMARTIO_PRT9_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT9_LUT_CTL7	0x4032095C	LUT component control register. See SMARTIO_PRT9_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT9_DU_SEL	0x403209C0	Data unit component input selection
SMARTIO_PRT9_DU_CTL	0x403209C4	Data unit component control register
SMARTIO_PRT9_DATA	0x403209F0	Data register

16.1.1 SMARTIO_PRT9_CTL

Control register

Address: 0x40320900

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BYPASS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			CLOCK_SRC [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None					RW	RW
HW Access	R	None					R	R
Name	ENABLED	None [30:26]					PIPE-LINE_EN	HLD_OVR

Bits	Name	Description
31	ENABLED	Enable for programmable IO. Should only be set to '1' when the programmable IO is completely configured: '0': Disabled (signals are bypassed; behavior as if BYPASS is 0xFF). When disabled, the fabric (data unit and LUTs) reset is activated. If the IP is disabled: - The PIPELINE_EN register field should be set to '1', to ensure low power consumption by preventing combinatorial loops. - The CLOCK_SRC register field should be set to "20"-"30" (clock is constant '0'), to ensure low power consumption. '1': Enabled. Once enabled, it takes 3 "clk_fabric" clock cycles till the fabric reset is de-activated and the fabric becomes fully functional. This ensures that the IO pins' input synchronizer states are flushed when the fabric is fully functional. Default Value: 0
25	PIPELINE_EN	Enable for pipeline register: '0': Disabled (register is bypassed). '1': Enabled. Default Value: 1

16.1.1 SMARTIO_PRT9_CTL (continued)

24	HLD_OVR	IO cell hold override functionality. In DeepSleep power mode, the HSIOM holds the IO cell output and output enable signals if Active functionality is connected to the IO pads. This is undesirable if the SMARTIO is supposed to deliver DeepSleep output functionality on these IO pads. This field is used to control the hold override functionality from the SMARTIO: '0': The HSIOM controls the IO cell hold override functionality ("hsiom_hld_ovr"). '1': The SMARTIO controls the IO cel hold override functionality: - In bypass mode (ENABLED is '0' or BYPASS[i] is '1'), the HSIOM control is used. - In NON bypass mode (ENABLED is '1' and BYPASS[i] is '0'), the SMARTIO sets hold override to "pwr_hld_ovr_hib" to enable SMARTIO functionality in DeepSleep power mode (but disables it in Hibernate or Stop power mode). Default Value: Undefined
12 : 8	CLOCK_SRC	Clock ("clk_fabric") and reset ("rst_fabric_n") source selection: "0": io_data_in[0]/'1'. ... "7": io_data_in[7]/'1'. "8": chip_data[0]/'1'. ... "15": chip_data[7]/'1'. "16": clk_smartio/rst_sys_act_n. Used for both Active functionality synchronous logic on "clk_smartio". This selection is intended for synchronous operation on a PCLK specified clock frequency ("clock_smartio_pos_en"). Note that the fabric's clocked elements are frequency aligned, but NOT phase aligned to "clk_sys". "17": clk_smartio/rst_sys_dpslp_n. Used for both DeepSleep functionality synchronous logic on "clk_smartio" (note that "clk_smartio" is NOT available in DeepSleep and Hibernate power modes). This selection is intended for synchronous operation on a PCLK specified clock frequency ("clock_smartio_pos_en"). Note that the fabric's clocked elements are frequency aligned, but NOT phase aligned to "clk_sys". "18": Same as "17". Note that the M0S8 SMARTIO version used the Hibernate reset for this value, but the MXS40 SMARTIO version does not support Hibernate functionality. "19": clk_lf/rst_lf_dpslp_n (note that "clk_lf" is available in DeepSleep power mode). This selection is intended for synchronous operation on"clk_lf". Note that the fabric's clocked elements are frequency aligned, but NOT phase aligned to other "clk_lf" clocked elements. "20"-"30": Clock source is constant '0'. Any of these clock sources should be selected when the IP is disabled to ensure low power consumption. "31": asynchronous mode/'1'. Select this when clockless operation is configured. NOTE: Two positive edges of the selected clock are required for the block to be enabled (to deactivate reset). In asynchronous (clockless) mode clk_sys is used to enable the block, but is not available for clocking. Default Value: 0x14
7 : 0	BYPASS	Bypass of the programmable IO, one bit for each IO pin: BYPASS[i] is for IO pin i. When ENABLED is '1', this field is used. When ENABLED is '0', this field is NOT used and SMARTIO fabric is always bypassed. '0': No bypass (programmable SMARTIO fabric is exposed). '1': Bypass (programmable SMARTIOIO fabric is hidden). Default Value: Undefined

16.1.2 SMARTIO_PRT9_SYNC_CTL

Synchronization control register

Address: 0x40320910

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	IO_SYNC_EN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CHIP_SYNC_EN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	CHIP_SYNC_EN	Synchronization of the chip input signals to "clk_fabric", one bit for each input: CHIP_SYNC_EN[i] is for input i. '0': No synchronization. '1': Synchronization. Default Value: Undefined
7 : 0	IO_SYNC_EN	Synchronization of the IO pin input signals to "clk_fabric", one bit for each IO pin: IO_SYNC_EN[i] is for IO pin i. '0': No synchronization. '1': Synchronization. Default Value: Undefined

16.1.3 SMARTIO_PRT9_LUT_SEL0

LUT component input selection

Address: 0x40320920

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				LUT_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				LUT_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				LUT_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	LUT_TR2_SEL	LUT input signal "tr2_in" source selection. Encoding is the same as for LUT_TR1_SEL. Default Value: Undefined
11 : 8	LUT_TR1_SEL	LUT input signal "tr1_in" source selection: "0": LUT 0 output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

16.1.3 SMARTIO_PRT9_LUT_SEL0 (continued)

3 : 0	LUT_TR0_SEL	LUT input signal "tr0_in" source selection: "0": Data unit output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

16.1.4 SMARTIO_PRT9_LUT_CTL0

LUT component control register

Address: 0x40320940

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						LUT_OPC [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	LUT_OPC	LUT opcode specifies the LUT operation: "0": Combinatoral output, no feedback. tr_out = LUT[{tr2_in, tr1_in, tr0_in}]. "1": Combinatorial output, feedback. tr_out = LUT[{lut_reg, tr1_in, tr0_in}]. On clock: lut_reg <= tr_in2. "2": Sequential output, no feedback. temp = LUT[{tr2_in, tr1_in, tr0_in}]. tr_out = lut_reg. On clock: lut_reg <= temp. "3": Register with asynchronous set and reset. tr_out = lut_reg. enable = (tr2_in ^ LUT[4]) | LUT[5]. set = enable & (tr1_in ^ LUT[2]) & LUT[3]. clr = enable & (tr0_in ^ LUT[0]) & LUT[1]. Asynchronously (no clock required): lut_reg <= if (clr) '0' else if (set) '1' Default Value: Undefined

16.1.4 SMARTIO_PRT9_LUT_CTL0 (continued)

7 : 0	LUT	LUT configuration. Depending on the LUT opcode LUT_OPC, the internal state lut_reg (captured in a flip-flop) and the LUT input signals tr0_in, tr1_in, tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state (lut_reg). Default Value: Undefined

16.1.5 SMARTIO_PRT9_DU_SEL

Data unit component input selection

Address: 0x403209C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DU_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				DU_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				DU_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW		None		RW	
HW Access	None		R		None		R	
Name	None [31:30]		DU_DATA1_SEL [29:28]		None [27:26]		DU_DATA0_SEL [25:24]	

Bits	Name	Description
29 : 28	DU_DATA1_SEL	Data unit input data "data1_in" source selection. Encoding is the same as for DU_DATA0_SEL. Default Value: Undefined
25 : 24	DU_DATA0_SEL	Data unit input data "data0_in" source selection: "0": Constant "0". "1": chip_data[7:0]. "2": io_data_in[7:0]. "3": DATA.DATA MMIO register field. Default Value: Undefined
19 : 16	DU_TR2_SEL	Data unit input signal "tr2_in" source selection. Encoding is the same as for DU_TR0_SEL. Default Value: Undefined
11 : 8	DU_TR1_SEL	Data unit input signal "tr1_in" source selection. Encoding is the same as for DU_TR0_SEL. Default Value: Undefined

16.1.5 SMARTIO_PRT9_DU_SEL (continued)

3 : 0	DU_TR0_SEL	Data unit input signal "tr0_in" source selection: "0": Constant '0'. "1": Constant '1'. "2": Data unit output. "10-3": LUT 7 - 0 outputs. Otherwise: Undefined. Default Value: Undefined

16.1.6 SMARTIO_PRT9_DU_CTL

Data unit component control register

Address: 0x403209C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					DU_SIZE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				DU_OPC [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 8	DU_OPC	Data unit opcode specifies the data unit operation: "1": INCR "2": DECR "3": INCR_WRAP "4": DECR_WRAP "5": INCR_DECR "6": INCR_DECR_WRAP "7": ROR "8": SHR "9": AND_OR "10": SHR_MAJ3 "11": SHR_EQL. Otherwise: Undefined. Default Value: Undefined
2 : 0	DU_SIZE	Size/width of the data unit data operands (in bits) is DU_SIZE+1. E.g., if DU_SIZE is 7, the width is 8 bits. Default Value: Undefined

16.1.7 SMARTIO_PRT9_DATA

Data register

Address: 0x403209F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	Data unit input data source. Default Value: Undefined

17 Low-Power Comparator Registers

This section discusses the Low-Power Comparator (LPCOMP) registers. It lists all the registers in mapping tables, in address order.

17.1 Register Details

Register	Address	Description
LPCOMP_CONFIG	0x40350000	LPCOMP Configuration Register
LPCOMP_STATUS	0x40350004	LPCOMP Status Register
LPCOMP_INTR	0x40350010	LPCOMP Interrupt request register
LPCOMP_INTR_SET	0x40350014	LPCOMP Interrupt set register
LPCOMP_INTR_MASK	0x40350018	LPCOMP Interrupt request mask
LPCOMP_INTR_MASKED	0x4035001C	LPCOMP Interrupt request masked
LPCOMP_CMP0_CTRL	0x40350040	Comparator 0 control Register
LPCOMP_CMP0_SW	0x40350050	Comparator 0 switch control
LPCOMP_CMP0_SW_CLEAR	0x40350054	Comparator 0 switch control clear
LPCOMP_CMP1_CTRL	0x40350080	Comparator 1 control Register
LPCOMP_CMP1_SW	0x40350090	Comparator 1 switch control
LPCOMP_CMP1_SW_CLEAR	0x40350094	Comparator 1 switch control clear

17.1.1 LPCOMP_CONFIG

LPCOMP Configuration Register

Address: 0x40350000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	ENABLED	LPREF_EN	None					

Bits	Name	Description
31	ENABLED	- 0: LPCOMP disabled (puts analog in power down, opens all switches, all clocks turned off) - 1: LPCOMP enabled Default Value: 0
30	LPREF_EN	Enable the local reference generator circuit to generate the local Vref and Ibias. Ibias current is an alternative to the reference current IREF generated by SRSS. This bit must be set for System DeepSleep and System Hibernate operation. Default Value: 0

17.1.2 LPCOMP_STATUS

LPCOMP Status Register

Address: 0x40350004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							RW
Name	None [23:17]							OUT1

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	OUT1	Current output value of the comparator 1. Default Value: 0
0	OUT0	Current output value of the comparator 0. Default Value: 0

17.1.3 LPCOMP_INTR

LPCOMP Interrupt request register

Address: 0x40350010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						COMP1	COMP0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1	Comparator 1 Interrupt: hardware sets this interrupt when comparator 1 triggers. Write with '1' to clear bit. Default Value: 0
0	COMP0	Comparator 0 Interrupt: hardware sets this interrupt when comparator 0 triggers. Write with '1' to clear bit. Default Value: 0

17.1.4 LPCOMP_INTR_SET

LPCOMP Interrupt set register

Address: 0x40350014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						COMP1	COMP0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	COMP0	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

17.1.5 LPCOMP_INTR_MASK

LPCOMP Interrupt request mask

Address: 0x40350018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						COMP1_MASK	COMP0_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	COMP0_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

17.1.6 LPCOMP_INTR_MASKED

LPCOMP Interrupt request masked

Address: 0x4035001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						COMP1_MASKED	COMP0_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
0	COMP0_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

17.1.7 LPCOMP_CMP0_CTRL

Comparator 0 control Register

Address: 0x40350040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	None			RW	
HW Access	R		R	None			R	
Name	INTTYPE0 [7:6]		HYST0	None [4:2]			MODE0 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	None	
HW Access	None				R	R	None	
Name	None [15:12]				DSI_LEV-EL0	DSI_BY-PASS0	None [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	DSI_LEVEL0	Synchronous comparator output (trigger): 0=pulse 1=level Default Value: 0
10	DSI_BYPASS0	Asynchronous: bypass comparator output synchronization: 0=synchronize (level or pulse) 1=bypass (output async) Note that in System Deep Sleep mode, this bit needs to be set to observe the output on the dedicated pin. Default Value: 0
7 : 6	INTTYPE0	Sets which edge will trigger an IRQ Default Value: 0 **0x0: DISABLE :** Disabled, no interrupts will be detected

17.1.7 LPCOMP_CMP0_CTRL (continued)

		0x1: RISING : Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges
5	HYST0	Add hysteresis to the comparator 0= Disable Hysteresis 1= Enable Hysteresis Default Value: 0
1 : 0	MODE0	Operating mode for the comparator Default Value: 0 **0x0: OFF :** Off **0x1: ULP :** Ultra low power operating mode. This mode must be used for System Deep Sleep and System Hibernate operation. In this mode, local Ibias is used. **0x2: LP :** Low Power operating mode. In this mode, IREF from SRSS is used. **0x3: NORMAL :** Normal power, full speed operating mode. In this mode, IREF from SRSS is used.

17.1.8 LPCOMP_CMP0_SW

Comparator 0 switch control

Address: 0x40350050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	None	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	None	RW1C	RW1C	RW1C
Name	CMP0_VN0	CMP0_BN0	CMP0_AN0	CMP0_IN0	None	CMP0_BP0	CMP0_AP0	CMP0_IP0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	CMP0_VN0	Comparator 0 negative terminal switch to local Vref (LPREF_EN must be set) Default Value: 0
6	CMP0_BN0	Comparator 0 negative terminal switch to amuxbusB Default Value: 0
5	CMP0_AN0	Comparator 0 negative terminal switch to amuxbusA Default Value: 0
4	CMP0_IN0	Comparator 0 negative terminal isolation switch to GPIO Default Value: 0
2	CMP0_BP0	Comparator 0 positive terminal switch to amuxbusB Default Value: 0
1	CMP0_AP0	Comparator 0 positive terminal switch to amuxbusA Default Value: 0
0	CMP0_IP0	Comparator 0 positive terminal isolation switch to GPIO Default Value: 0

17.1.9 LPCOMP_CMP0_SW_CLEAR

Comparator 0 switch control clear

Address: 0x40350054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	None	RW1C	RW1C	RW1C
HW Access	A	A	A	A	None	A	A	A
Name	CMP0_VN0	CMP0_BN0	CMP0_AN0	CMP0_IN0	None	CMP0_BP0	CMP0_AP0	CMP0_IP0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	CMP0_VN0	see corresponding bit in CMP0_SW Default Value: 0
6	CMP0_BN0	see corresponding bit in CMP0_SW Default Value: 0
5	CMP0_AN0	see corresponding bit in CMP0_SW Default Value: 0
4	CMP0_IN0	see corresponding bit in CMP0_SW Default Value: 0
2	CMP0_BP0	see corresponding bit in CMP0_SW Default Value: 0
1	CMP0_AP0	see corresponding bit in CMP0_SW Default Value: 0
0	CMP0_IP0	see corresponding bit in CMP0_SW Default Value: 0

17.1.10 LPCOMP_CMP1_CTRL

Comparator 1 control Register

Address: 0x40350080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	None			RW	
HW Access	R		R	None			R	
Name	INTTYPE1 [7:6]		HYST1	None [4:2]			MODE1 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	None	
HW Access	None				R	R	None	
Name	None [15:12]				DSI_LEV-EL1	DSI_BY-PASS1	None [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	DSI_LEVEL1	Synchronous comparator output (trigger): 0=pulse 1=level Default Value: 0
10	DSI_BYPASS1	Asynchronous: bypass comparator output synchronization: 0=synchronize (level or pulse) 1=bypass (output async) Note that in System Deep Sleep mode, this bit needs to be set to observe the output on the dedicated pin. Default Value: 0
7 : 6	INTTYPE1	Sets which edge will trigger an IRQ Default Value: 0 **0x0: DISABLE :** Disabled, no interrupts will be detected

17.1.10 LPCOMP_CMP1_CTRL (continued)

		0x1: RISING : Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges
5	HYST1	Add hysteresis to the comparator 0= Disable Hysteresis 1= Enable Hysteresis Default Value: 0
1 : 0	MODE1	Operating mode for the comparator Default Value: 0 **0x0: OFF :** Off **0x1: ULP :** Ultra low power operating mode. This mode must be used for System Deep Sleep and System Hibernate operation. In this mode, local Ibias is used. **0x2: LP :** Low Power operating mode. In this mode, IREF from SRSS is used. **0x3: NORMAL :** Normal power, full speed operating mode. In this mode, IREF from SRSS is used.

17.1.11 LPCOMP_CMP1_SW

Comparator 1 switch control

Address: 0x40350090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	None	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	None	RW1C	RW1C	RW1C
Name	CMP1_VN1	CMP1_BN1	CMP1_AN1	CMP1_IN1	None	CMP1_BP1	CMP1_AP1	CMP1_IP1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	CMP1_VN1	Comparator 1 negative terminal switch to local Vref (LPREF_EN must be set) Default Value: 0
6	CMP1_BN1	Comparator 1 negative terminal switch to amuxbusB Default Value: 0
5	CMP1_AN1	Comparator 1 negative terminal switch to amuxbusA Default Value: 0
4	CMP1_IN1	Comparator 1 negative terminal isolation switch to GPIO Default Value: 0
2	CMP1_BP1	Comparator 1 positive terminal switch to amuxbusB Default Value: 0
1	CMP1_AP1	Comparator 1 positive terminal switch to amuxbusA Default Value: 0
0	CMP1_IP1	Comparator 1 positive terminal isolation switch to GPIO Default Value: 0

17.1.12 LPCOMP_CMP1_SW_CLEAR

Comparator 1 switch control clear

Address: 0x40350094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	None	RW1C	RW1C	RW1C
HW Access	A	A	A	A	None	A	A	A
Name	CMP1_VN1	CMP1_BN1	CMP1_AN1	CMP1_IN1	None	CMP1_BP1	CMP1_AP1	CMP1_IP1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	CMP1_VN1	see corresponding bit in CMP1_SW Default Value: 0
6	CMP1_BN1	see corresponding bit in CMP1_SW Default Value: 0
5	CMP1_AN1	see corresponding bit in CMP1_SW Default Value: 0
4	CMP1_IN1	see corresponding bit in CMP1_SW Default Value: 0
2	CMP1_BP1	see corresponding bit in CMP1_SW Default Value: 0
1	CMP1_AP1	see corresponding bit in CMP1_SW Default Value: 0
0	CMP1_IP1	see corresponding bit in CMP1_SW Default Value: 0

18 Timer, Counter, PWM Registers

This section discusses the Timer, Counter, PWM (TCPWM) registers. It lists all the registers in mapping tables, in address order.

TCPWM is grouped into two counter groups: TCPWM0 and TCPWM1. TCPWM0 contains 32-bit counters and TCPWM1 contains 16-bit counters.

18.1 Register Details

Register	Address	Description
TCPWM0_GRP0_CNT0_CTRL	0x40380000	Counter control register
TCPWM0_GRP0_CNT0_STATUS	0x40380004	Counter status register
TCPWM0_GRP0_CNT0_COUNTER	0x40380008	Counter count register
TCPWM0_GRP0_CNT0_CC0	0x40380010	Counter compare/capture 0 register
TCPWM0_GRP0_CNT0_CC0_BUFF	0x40380014	Counter buffered compare/capture 0 register
TCPWM0_GRP0_CNT0_PERIOD	0x40380020	Counter period register
TCPWM0_GRP0_CNT0_PERIOD_BUFF	0x40380024	Counter buffered period register
TCPWM0_GRP0_CNT0_DT	0x40380030	Counter PWM dead time register
TCPWM0_GRP0_CNT0_TR_CMD	0x40380040	Counter trigger command register
TCPWM0_GRP0_CNT0_TR_IN_SEL0	0x40380044	Counter input trigger selection register 0
TCPWM0_GRP0_CNT0_TR_IN_SEL1	0x40380048	Counter input trigger selection register 1
TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL	0x4038004C	Counter input trigger edge selection register
TCPWM0_GRP0_CNT0_TR_PWM_CTRL	0x40380050	Counter trigger PWM control register
TCPWM0_GRP0_CNT0_TR_OUT_SEL	0x40380054	Counter output trigger selection register
TCPWM0_GRP0_CNT0_INTR	0x40380070	Interrupt request register
TCPWM0_GRP0_CNT0_INTR_SET	0x40380074	Interrupt set request register
TCPWM0_GRP0_CNT0_INTR_MASK	0x40380078	Interrupt mask register
TCPWM0_GRP0_CNT0_INTR_MASKED	0x4038007C	Interrupt masked request register
TCPWM0_GRP0_CNT1_CTRL	0x40380080	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT1_STATUS	0x40380084	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT1_COUNTER	0x40380088	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT1_CC0	0x40380090	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT1_CC0_BUFF	0x40380094	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.

Register	Address	Description
TCPWM0_GRP0_CNT1_PERIOD	0x403800A0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT1_PERIOD_BUFF	0x403800A4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT1_DT	0x403800B0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT1_TR_CMD	0x403800C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT1_TR_IN_SEL0	0x403800C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT1_TR_IN_SEL1	0x403800C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT1_TR_IN_EDGE_SEL	0x403800CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT1_TR_PWM_CTRL	0x403800D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT1_TR_OUT_SEL	0x403800D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT1_INTR	0x403800F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT1_INTR_SET	0x403800F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT1_INTR_MASK	0x403800F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT1_INTR_MASKED	0x403800FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT2_CTRL	0x40380100	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT2_STATUS	0x40380104	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT2_COUNTER	0x40380108	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT2_CC0	0x40380110	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT2_CC0_BUFF	0x40380114	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT2_PERIOD	0x40380120	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT2_PERIOD_BUFF	0x40380124	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT2_DT	0x40380130	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT2_TR_CMD	0x40380140	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT2_TR_IN_SEL0	0x40380144	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT2_TR_IN_SEL1	0x40380148	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT2_TR_IN_EDGE_SEL	0x4038014C	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT2_TR_PWM_CTRL	0x40380150	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT2_TR_OUT_SEL	0x40380154	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT2_INTR	0x40380170	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT2_INTR_SET	0x40380174	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.

Register	Address	Description
TCPWM0_GRP0_CNT2_INTR_MASK	0x40380178	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT2_INTR_MASKED	0x4038017C	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP0_CNT3_CTRL	0x40380180	Counter control register. See TCPWM0_GRP0_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT3_STATUS	0x40380184	Counter status register. See TCPWM0_GRP0_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP0_CNT3_COUNTER	0x40380188	Counter count register. See TCPWM0_GRP0_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP0_CNT3_CC0	0x40380190	Counter compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP0_CNT3_CC0_BUFF	0x40380194	Counter buffered compare/capture 0 register. See TCPWM0_GRP0_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT3_PERIOD	0x403801A0	Counter period register. See TCPWM0_GRP0_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP0_CNT3_PERIOD_BUFF	0x403801A4	Counter buffered period register. See TCPWM0_GRP0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP0_CNT3_DT	0x403801B0	Counter PWM dead time register. See TCPWM0_GRP0_CNT0_DT for the details of bit fields.
TCPWM0_GRP0_CNT3_TR_CMD	0x403801C0	Counter trigger command register. See TCPWM0_GRP0_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP0_CNT3_TR_IN_SEL0	0x403801C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP0_CNT3_TR_IN_SEL1	0x403801C8	Counter input trigger selection register 1. See TCPWM0_GRP0_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP0_CNT3_TR_IN_EDGE_SEL	0x403801CC	Counter input trigger edge selection register. See TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP0_CNT3_TR_PWM_CTRL	0x403801D0	Counter trigger PWM control register. See TCPWM0_GRP0_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP0_CNT3_TR_OUT_SEL	0x403801D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP0_CNT3_INTR	0x403801F0	Interrupt request register. See TCPWM0_GRP0_CNT0_INTR for the details of bit fields.
TCPWM0_GRP0_CNT3_INTR_SET	0x403801F4	Interrupt set request register. See TCPWM0_GRP0_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP0_CNT3_INTR_MASK	0x403801F8	Interrupt mask register. See TCPWM0_GRP0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP0_CNT3_INTR_MASKED	0x403801FC	Interrupt masked request register. See TCPWM0_GRP0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT0_CTRL	0x40388000	Counter control register
TCPWM0_GRP1_CNT0_STATUS	0x40388004	Counter status register
TCPWM0_GRP1_CNT0_COUNTER	0x40388008	Counter count register
TCPWM0_GRP1_CNT0_CC0	0x40388010	Counter compare/capture 0 register
TCPWM0_GRP1_CNT0_CC0_BUFF	0x40388014	Counter buffered compare/capture 0 register
TCPWM0_GRP1_CNT0_CC1	0x40388018	Counter compare/capture 1 register
TCPWM0_GRP1_CNT0_CC1_BUFF	0x4038801C	Counter buffered compare/capture 1 register
TCPWM0_GRP1_CNT0_PERIOD	0x40388020	Counter period register
TCPWM0_GRP1_CNT0_PERIOD_BUFF	0x40388024	Counter buffered period register

Register	Address	Description
TCPWM0_GRP1_CNT0_DT	0x40388030	Counter PWM dead time register
TCPWM0_GRP1_CNT0_TR_CMD	0x40388040	Counter trigger command register
TCPWM0_GRP1_CNT0_TR_IN_SEL0	0x40388044	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT0_TR_IN_SEL1	0x40388048	Counter input trigger selection register 1
TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL	0x4038804C	Counter input trigger edge selection register
TCPWM0_GRP1_CNT0_TR_PWM_CTRL	0x40388050	Counter trigger PWM control register
TCPWM0_GRP1_CNT0_TR_OUT_SEL	0x40388054	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT0_INTR	0x40388070	Interrupt request register
TCPWM0_GRP1_CNT0_INTR_SET	0x40388074	Interrupt set request register
TCPWM0_GRP1_CNT0_INTR_MASK	0x40388078	Interrupt mask register
TCPWM0_GRP1_CNT0_INTR_MASKED	0x4038807C	Interrupt masked request register
TCPWM0_GRP1_CNT1_CTRL	0x40388080	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT1_STATUS	0x40388084	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT1_COUNTER	0x40388088	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT1_CC0	0x40388090	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT1_CC0_BUFF	0x40388094	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT1_CC1	0x40388098	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT1_CC1_BUFF	0x4038809C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT1_PERIOD	0x403880A0	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT1_PERIOD_BUFF	0x403880A4	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT1_DT	0x403880B0	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT1_TR_CMD	0x403880C0	Counter trigger command register. See TCPWM0_GRP1_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT1_TR_IN_SEL0	0x403880C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT1_TR_IN_SEL1	0x403880C8	Counter input trigger selection register 1. See TCPWM0_GRP1_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT1_TR_IN_EDGE_SEL	0x403880CC	Counter input trigger edge selection register. See TCPWM0_GRP1_CNT0_TR_IN_EDGE_-SEL for the details of bit fields.
TCPWM0_GRP1_CNT1_TR_PWM_CTRL	0x403880D0	Counter trigger PWM control register. See TCPWM0_GRP1_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT1_TR_OUT_SEL	0x403880D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT1_INTR	0x403880F0	Interrupt request register. See TCPWM0_GRP1_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT1_INTR_SET	0x403880F4	Interrupt set request register. See TCPWM0_GRP1_CNT0_INTR_SET for the details of bit fields.

Register	Address	Description
TCPWM0_GRP1_CNT1_INTR_MASK	0x403880F8	Interrupt mask register. See TCPWM0_GRP1_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT1_INTR_MASKED	0x403880FC	Interrupt masked request register. See TCPWM0_GRP1_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT2_CTRL	0x40388100	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT2_STATUS	0x40388104	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT2_COUNTER	0x40388108	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT2_CC0	0x40388110	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT2_CC0_BUFF	0x40388114	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT2_CC1	0x40388118	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT2_CC1_BUFF	0x4038811C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT2_PERIOD	0x40388120	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT2_PERIOD_BUFF	0x40388124	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT2_DT	0x40388130	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT2_TR_CMD	0x40388140	Counter trigger command register. See TCPWM0_GRP1_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT2_TR_IN_SEL0	0x40388144	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT2_TR_IN_SEL1	0x40388148	Counter input trigger selection register 1. See TCPWM0_GRP1_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT2_TR_IN_EDGE_SEL	0x4038814C	Counter input trigger edge selection register. See TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT2_TR_PWM_CTRL	0x40388150	Counter trigger PWM control register. See TCPWM0_GRP1_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT2_TR_OUT_SEL	0x40388154	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT2_INTR	0x40388170	Interrupt request register. See TCPWM0_GRP1_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT2_INTR_SET	0x40388174	Interrupt set request register. See TCPWM0_GRP1_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT2_INTR_MASK	0x40388178	Interrupt mask register. See TCPWM0_GRP1_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT2_INTR_MASKED	0x4038817C	Interrupt masked request register. See TCPWM0_GRP1_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT3_CTRL	0x40388180	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT3_STATUS	0x40388184	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT3_COUNTER	0x40388188	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT3_CC0	0x40388190	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT3_CC0_BUFF	0x40388194	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT3_CC1	0x40388198	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT3_CC1_BUFF	0x4038819C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.

Register	Address	Description
TCPWM0_GRP1_CNT3_PERIOD	0x403881A0	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT3_PERIOD_BUFF	0x403881A4	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT3_DT	0x403881B0	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT3_TR_CMD	0x403881C0	Counter trigger command register. See TCPWM0_GRP1_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT3_TR_IN_SEL0	0x403881C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT3_TR_IN_SEL1	0x403881C8	Counter input trigger selection register 1. See TCPWM0_GRP1_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT3_TR_IN_EDGE_SEL	0x403881CC	Counter input trigger edge selection register. See TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT3_TR_PWM_CTRL	0x403881D0	Counter trigger PWM control register. See TCPWM0_GRP1_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT3_TR_OUT_SEL	0x403881D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT3_INTR	0x403881F0	Interrupt request register. See TCPWM0_GRP1_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT3_INTR_SET	0x403881F4	Interrupt set request register. See TCPWM0_GRP1_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT3_INTR_MASK	0x403881F8	Interrupt mask register. See TCPWM0_GRP1_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT3_INTR_MASKED	0x403881FC	Interrupt masked request register. See TCPWM0_GRP1_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT4_CTRL	0x40388200	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT4_STATUS	0x40388204	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT4_COUNTER	0x40388208	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT4_CC0	0x40388210	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT4_CC0_BUFF	0x40388214	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT4_CC1	0x40388218	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT4_CC1_BUFF	0x4038821C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT4_PERIOD	0x40388220	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT4_PERIOD_BUFF	0x40388224	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT4_DT	0x40388230	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT4_TR_CMD	0x40388240	Counter trigger command register. See TCPWM0_GRP1_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT4_TR_IN_SEL0	0x40388244	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT4_TR_IN_SEL1	0x40388248	Counter input trigger selection register 1. See TCPWM0_GRP1_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT4_TR_IN_EDGE_SEL	0x4038824C	Counter input trigger edge selection register. See TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT4_TR_PWM_CTRL	0x40388250	Counter trigger PWM control register. See TCPWM0_GRP1_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT4_TR_OUT_SEL	0x40388254	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.

Register	Address	Description
TCPWM0_GRP1_CNT4_INTR	0x40388270	Interrupt request register. See TCPWM0_GRP1_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT4_INTR_SET	0x40388274	Interrupt set request register. See TCPWM0_GRP1_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT4_INTR_MASK	0x40388278	Interrupt mask register. See TCPWM0_GRP1_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT4_INTR_MASKED	0x4038827C	Interrupt masked request register. See TCPWM0_GRP1_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT5_CTRL	0x40388280	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT5_STATUS	0x40388284	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT5_COUNTER	0x40388288	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT5_CC0	0x40388290	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT5_CC0_BUFF	0x40388294	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT5_CC1	0x40388298	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT5_CC1_BUFF	0x4038829C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT5_PERIOD	0x403882A0	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT5_PERIOD_BUFF	0x403882A4	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT5_DT	0x403882B0	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT5_TR_CMD	0x403882C0	Counter trigger command register. See TCPWM0_GRP1_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT5_TR_IN_SEL0	0x403882C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT5_TR_IN_SEL1	0x403882C8	Counter input trigger selection register 1. See TCPWM0_GRP1_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT5_TR_IN_EDGE_SEL	0x403882CC	Counter input trigger edge selection register. See TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT5_TR_PWM_CTRL	0x403882D0	Counter trigger PWM control register. See TCPWM0_GRP1_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT5_TR_OUT_SEL	0x403882D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT5_INTR	0x403882F0	Interrupt request register. See TCPWM0_GRP1_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT5_INTR_SET	0x403882F4	Interrupt set request register. See TCPWM0_GRP1_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT5_INTR_MASK	0x403882F8	Interrupt mask register. See TCPWM0_GRP1_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT5_INTR_MASKED	0x403882FC	Interrupt masked request register. See TCPWM0_GRP1_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT6_CTRL	0x40388300	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT6_STATUS	0x40388304	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT6_COUNTER	0x40388308	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT6_CC0	0x40388310	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT6_CC0_BUFF	0x40388314	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.

Register	Address	Description
TCPWM0_GRP1_CNT6_CC1	0x40388318	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT6_CC1_BUFF	0x4038831C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT6_PERIOD	0x40388320	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT6_PERIOD_BUFF	0x40388324	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT6_DT	0x40388330	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT6_TR_CMD	0x40388340	Counter trigger command register. See TCPWM0_GRP1_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT6_TR_IN_SEL0	0x40388344	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT6_TR_IN_SEL1	0x40388348	Counter input trigger selection register 1. See TCPWM0_GRP1_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT6_TR_IN_EDGE_SEL	0x4038834C	Counter input trigger edge selection register. See TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL for the details of bit fields.
TCPWM0_GRP1_CNT6_TR_PWM_CTRL	0x40388350	Counter trigger PWM control register. See TCPWM0_GRP1_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT6_TR_OUT_SEL	0x40388354	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT6_INTR	0x40388370	Interrupt request register. See TCPWM0_GRP1_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT6_INTR_SET	0x40388374	Interrupt set request register. See TCPWM0_GRP1_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT6_INTR_MASK	0x40388378	Interrupt mask register. See TCPWM0_GRP1_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT6_INTR_MASKED	0x4038837C	Interrupt masked request register. See TCPWM0_GRP1_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_GRP1_CNT7_CTRL	0x40388380	Counter control register. See TCPWM0_GRP1_CNT0_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT7_STATUS	0x40388384	Counter status register. See TCPWM0_GRP1_CNT0_STATUS for the details of bit fields.
TCPWM0_GRP1_CNT7_COUNTER	0x40388388	Counter count register. See TCPWM0_GRP1_CNT0_COUNTER for the details of bit fields.
TCPWM0_GRP1_CNT7_CC0	0x40388390	Counter compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0 for the details of bit fields.
TCPWM0_GRP1_CNT7_CC0_BUFF	0x40388394	Counter buffered compare/capture 0 register. See TCPWM0_GRP1_CNT0_CC0_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT7_CC1	0x40388398	Counter compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1 for the details of bit fields.
TCPWM0_GRP1_CNT7_CC1_BUFF	0x4038839C	Counter buffered compare/capture 1 register. See TCPWM0_GRP1_CNT0_CC1_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT7_PERIOD	0x403883A0	Counter period register. See TCPWM0_GRP1_CNT0_PERIOD for the details of bit fields.
TCPWM0_GRP1_CNT7_PERIOD_BUFF	0x403883A4	Counter buffered period register. See TCPWM0_GRP1_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_GRP1_CNT7_DT	0x403883B0	Counter PWM dead time register. See TCPWM0_GRP1_CNT0_DT for the details of bit fields.
TCPWM0_GRP1_CNT7_TR_CMD	0x403883C0	Counter trigger command register. See TCPWM0_GRP1_CNT0_TR_CMD for the details of bit fields.
TCPWM0_GRP1_CNT7_TR_IN_SEL0	0x403883C4	Counter input trigger selection register 0. See TCPWM0_GRP0_CNT0_TR_IN_SEL0 for the details of bit fields.
TCPWM0_GRP1_CNT7_TR_IN_SEL1	0x403883C8	Counter input trigger selection register 1. See TCPWM0_GRP1_CNT0_TR_IN_SEL1 for the details of bit fields.
TCPWM0_GRP1_CNT7_TR_IN_EDGE_SEL	0x403883CC	Counter input trigger edge selection register. See TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL for the details of bit fields.

Register	Address	Description
TCPWM0_GRP1_CNT7_TR_PWM_CTRL	0x403883D0	Counter trigger PWM control register. See TCPWM0_GRP1_CNT0_TR_PWM_CTRL for the details of bit fields.
TCPWM0_GRP1_CNT7_TR_OUT_SEL	0x403883D4	Counter output trigger selection register. See TCPWM0_GRP0_CNT0_TR_OUT_SEL for the details of bit fields.
TCPWM0_GRP1_CNT7_INTR	0x403883F0	Interrupt request register. See TCPWM0_GRP1_CNT0_INTR for the details of bit fields.
TCPWM0_GRP1_CNT7_INTR_SET	0x403883F4	Interrupt set request register. See TCPWM0_GRP1_CNT0_INTR_SET for the details of bit fields.
TCPWM0_GRP1_CNT7_INTR_MASK	0x403883F8	Interrupt mask register. See TCPWM0_GRP1_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_GRP1_CNT7_INTR_MASKED	0x403883FC	Interrupt masked request register. See TCPWM0_GRP1_CNT0_INTR_MASKED for the details of bit fields.

18.1.1 TCPWM0_GRP0_CNT0_CTRL

Counter control register

Address: 0x40380000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	None	RW
HW Access	None					R	None	R
Name	None [7:3]					AUTO_RELOAD_PERIOD	None	AUTO_RELOAD_CC0

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		PWM_DISABLE_MODE [13:12]		None	PWM_SYNC_KILL	PWM_STOP_ON_KILL	PWM_IM_KILL

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		QUAD_ENCODING_MODE [21:20]		None	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None			RW		
HW Access	R	R	None			R		
Name	ENABLED	DBG_FREEZE_EN	None [29:27]			MODE [26:24]		

Bits	Name	Description
31	ENABLED	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). Default Value: 0

18.1.1 TCPWM0_GRP0_CNT0_CTRL (continued)

30	DBG_FREEZE_EN	Specifies the counter behavior in debug mode. '0': The counter operation continues in debug mode. '1': The counter operation freezes in debug mode. Default Value: 0
26 : 24	MODE	Counter mode. Default Value: 0 **0x0: TIMER :** Timer mode **0x1: Reserved1 :** This setting is reserved. Do not use. **0x2: CAPTURE :** Capture mode **0x3: QUAD :** Quadrature mode Different encoding modes can be selected by QUAD_ENCODING_MODE including up/down count functionality. Different counter range, reload value and capture behavior can be selected by QUAD_RANGE_-MODE (overloaded field UP_DOWN_MODE). **0x4: PWM :** Pulse width modulation (PWM) mode **0x5: PWM_DT :** PWM with deadtime insertion mode **0x6: PWM_PR :** Pseudo random pulse width modulation **0x7: SR :** Shift register mode.
21 : 20	QUAD_ENCODING_-MODE	In QUAD mode this field selects the quadrature encoding mode (X1/X2/X4) or the Up / Down rotary counting mode. In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_com-pl_out"; i.e. a disabled output line "dt_line_out" has the value QUAD_ENCODING_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUAD_ENCODING_MODE[1]. Default Value: 0

18.1.1 TCPWM0_GRP0_CNT0_CTRL (continued)

		0x0: X1 : X1 encoding (QUAD mode) This encoding is identical with an up / down counting functionality of the following way: Rising edges of input phiA increment or decrement the counter depending on the state of input phiB (direction input). **0x1: X2 :** X2 encoding (QUAD mode) **0x2: X4 :** X4 encoding (QUAD mode) **0x3: UP_DOWN :** Up / Down rotary counting mode. Input phiA increments the counter, input phiB decrements the counter. The trigger edge detection settings apply. **0x1: INV_OUT :** When bit 0 is '1', QUADRATURE_ENCODING_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes) **0x2: INV_COMPL_OUT :** When bit 1 is '1', QUADRATURE_ENCODING_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)
18	ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	UP_DOWN_MODE	Determines counter direction. In QUAD mode this field acts as QUAD_RANGE_MODE field selecting between different counter range, reload value and compare / capture behavior. Default Value: 0 **0x0: COUNT_UP :** Count up (to PERIOD). An overflow event is generated when the counter changes from a state in which COUNTER equals PERIOD. A terminal count event is generated when the counter changes from a state in which COUNTER equals PERIOD. **0x1: COUNT_DOWN :** Count down (to "0"). An underflow event is generated when the counter changes from a state in which COUNTER equals "0". A terminal count event is generated when the counter changes from a state in which COUNTER equals "0".

18.1.1 TCPWM0_GRP0_CNT0_CTRL (continued)

0x2: COUNT_UPDN1 :

Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter changes from a state in which COUNTER equals PERIOD. An underflow event is generated when the counter changes from a state in which COUNTER equals "0". A terminal count event is generated when the counter changes from a state in which COUNTER equals "0".

0x3: COUNT_UPDN2 :

Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter changes from a state in which COUNTER equals PERIOD. An underflow event is generated when the counter changes from a state in which COUNTER equals "0". A terminal count event is generated when the counter changes from a state in which COUNTER equals "0" AND when the counter changes from a state in which COUNTER equals PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).

0x0: QUAD_RANGE0 :

In QUAD mode this setting selects the QUAD_RANGE0 mode with the following behavior:
- COUNTER range is between 0x0000 and 0xFFFF / 0xFFFFFFFF (for GRP_CNT_WIDTH = 16 / 32)
- on reload / index event:
 - CC0 is copied to CC0_BUFF
 - COUNTER is copied to CC0
 - COUNTER is set to midpoint (0x8000 / 0x80000000)
 - tc and cc0_match events are generated
- when COUNTER is 0x0000 or 0xFFFF / 0xFFFFFFFF:
 - CC0 is copied to CC0_BUFF
 - COUNTER (0x0000 or 0xFFFF / 0xFFFFFFFF) is copied to CC0
 - COUNTER is set to midpoint (0x8000 / 0x80000000)
 - cc0_match event is generated

This mode is 100% backward compatible with previous TCPWM quadrature behavior.

18.1.1 TCPWM0_GRP0_CNT0_CTRL (continued)

0x1: QUAD_RANGE0_CMP :

In QUAD mode this setting selects the QUAD_RANGE0_CMP mode with the following behavior:
- COUNTER range is between 0x0000 and 0xFFFF / 0xFFFFFFFF (for GRP_CNT_WIDTH = 16 / 32)
- the capture0 event acts as 2nd reload / index event
- on reload / index event:
 - COUNTER is set to midpoint (0x8000 / 0x80000000)
 - when 'capture on index' is selected (AUTO_RELOAD_PERIOD=0):
 - tc event is generated
 - PERIOD is copied to PERIOD_BUFF
 - COUNTER is copied to PERIOD
- when COUNTER is 0x0000 or 0xFFFF / 0xFFFFFFFF:
 - COUNTER is set to midpoint (0x8000 / 0x80000000)
 - when 'capture on wrap-around' is selected (AUTO_RELOAD_PERIOD=1):
 - tc event is generated
 - PERIOD is copied to PERIOD_BUFF
 - COUNTER (0x0000 or 0xFFFF / 0xFFFFFFFF) is copied to PERIOD
- 1 or 2 compare functions (depending on CC1_PRESENT) available

This mode is to a certain extend backward compatible with previous TCPWM quadrature behavior but allows a compare function during quadrature decoding using the CC0/CC_BUFF registers and the cc0_match event. Because of that the PERIOD/PERIOD_BUFF registers are used instead of CC0/CC_BUFF registers to capture COUNTER at reload / index event or wrap-around.

0x2: QUAD_RANGE1_CAPT :

In QUAD mode this setting selects the QUAD_RANGE1_CAPT mode with the following behavior:
- COUNTER range is between 0x0000 and PERIOD
- on reload / index event:
 - COUNTER is set to 0x0000
 - tc event is generated
- when COUNTER is 0x0000 and decrementing:
 - COUNTER is set to PERIOD
 - tc event is generated
- when COUNTER equals PERIOD and is incrementing:
 - COUNTER is set to 0x0000
 - tc event is generated
- 1 or 2 capture functions (depending on CC1_PRESENT) available
- on capture0 / capture1 event:
 - CC0 / CC1 is copied to CC0_BUFF / CC1_BUFF
 - COUNTER value is copied to CC0

This mode is NOT backward compatible with previous TCPWM quadrature behavior. It is to a certain extend compatible with previous Traveo 1 QPRC behavior. It allows that the COUNTER register reflects the current angle position of the rotary encoder, i.e. no MOD or SUB calculations need to be done in SW on the COUNTER value to get the current angle position. This allows a DMA copy of the angle position from the COUNTER register. However, a disadvantage of this mode is that fast sequences of tc interrupts can occur (when encoder moves back and forth around start position). It is recommended to not use the tc interrupt in this mode.

0x3: QUAD_RANGE1_CMP :

In QUAD mode this setting selects the QUAD_RANGE1_CMP mode.
The behavior is the same as for QUAD_RANGE1_CAPT mode described above with the only difference that 1 or 2 compare functions (depending on CC1_PRESENT) are available instead of 1 or 2 capture functions.

18.1.1 TCPWM0_GRP0_CNT0_CTRL (continued)

13 : 12	PWM_DISABLE_MODE	Specifies the behavior of the PWM outputs "line_out" and "line_compl_out" while the TCPWM counter is disabled (CTL.ENABLED='0') or stopped. Note: The output signal of this selection can be further modified by the immediate kill logic and line_out polarity settings (CTRL.QUAD_ENCODING_MODE). Default Value: 0 **0x0: Z :** The behavior is the same is in previous mxtcpwm (version 1). When the counter is disabled the PWM outputs "line_out" and "line_compl_out" are NOT driven by the TCPWM. Instead the port default level configuration applies, e.g. "Z" (high impedance). Note: This is realized by driving the TCPWM output "line_out_en" to 0. When the counter is stopped upon a stop event the PWM outputs are deactivated (to the polarity defined by CTL.QUAD_ENCODING_MODE). **0x1: RETAIN :** When the counter is disabled the PWM outputs "line_out" and "line_compl_out" are driven by the TCPWM. When the counter is disabled or stopped upon a stop event the PWM outputs are retained (keep their previous levels). While the counter is disabled or stopped the PWM outputs can be changed via LINE_SEL (when parameter GRP_SMC_PRESENT = 1). **0x2: L :** When the counter is disabled the PWM outputs "line_out" and "line_compl_out" are driven by the TCPWM. When the counter is disabled or stopped upon a stop event the PWM output "line_out" is driven as a fixed '0' and the PWM output "line_compl_out" is driven as a fixed '1'. **0x3: H :** When the counter is disabled the PWM outputs "line_out" and "line_compl_out" are driven by the TCPWM. When the counter is disabled or stopped upon a stop event the PWM output "line_out" is driven as a fixed '1' and the PWM output "line_compl_out" is driven as a fixed '0'.
10	PWM_SYNC_KILL	Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
9	PWM_STOP_ON_KILL	Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0

18.1.1 TCPWM0_GRP0_CNT0_CTRL (continued)

8	PWM_IMM_KILL	Specifies whether the kill event immediately deactivates the "dt_line_out" and "dt_line_compl_out" signals or with the next module clock ("active count" pre-scaled "clk_counter"). '0': synchronous kill activation. Deactivates the "dt_line_out" and "dt_line_compl_out" signals with the next module clock ("active count" pre-scaled "clk_counter"). '1': immediate kill activation. Immediately deactivates the "dt_line_out" and "dt_line_compl_out" signals. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
2	AUTO_RELOAD_PERIOD	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff. Default Value: 0
0	AUTO_RELOAD_CC0	Specifies switching of the CC0 and buffered CC0 values. This field has a function in TIMER, QUAD (QUAD_RANGE0_CMP, QUAD_RANGE1_CMP range modes), SR, PWM, PWM_DT and PWM_PR modes. Timer, QUAD, SR modes: '0': never switch. '1': switch on a compare match 0 event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0

18.1.2 TCPWM0_GRP0_CNT0_STATUS

Counter status register

Address: 0x40380004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	None			R
HW Access	RW	RW	RW	RW	None			RW
Name	TR_STOP	TR_RE-LOAD	TR_COUNT	TR_CAP-TURE0	None [3:1]			DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R	None			R	R	None	R
HW Access	RW	None			RW	RW	None	RW
Name	RUNNING	None [14:12]			LINE_COM-PL_OUT	LINE_OUT	None	TR_START

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	DT_CNT_L [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	DT_CNT_L	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion (8bit dead time counter or low byte of 16-bit dead time counter). In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
15	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. This field is used to indicate that the counter is running after a start/reload event and that the counter is stopped after a stop event. When a running counter operation is paused in debug state (see CTRL.DBG_PAUSE) then the RUNNING bit is still '1'. Default Value: 0
11	LINE_COMPL_OUT	Indicates the actual level of the complementary PWM line output signal. Default Value: 0
10	LINE_OUT	Indicates the actual level of the PWM line output signal. Default Value: 0

18.1.2 TCPWM0_GRP0_CNT0_STATUS (continued)

8	TR_START	Indicates the actual level of the selected start trigger. Default Value: 0
7	TR_STOP	Indicates the actual level of the selected stop trigger. Default Value: 0
6	TR_RELOAD	Indicates the actual level of the selected reload trigger. Default Value: 0
5	TR_COUNT	Indicates the actual level of the selected count trigger. Default Value: 1
4	TR_CAPTURE0	Indicates the actual level of the selected capture 0 trigger. Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

18.1.3 TCPWM0_GRP0_CNT0_COUNTER

Counter count register

Address: 0x40380008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	COUNTER [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	COUNTER [31:24]							

Bits	Name	Description
31 : 0	COUNTER	16-bit / 32-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

18.1.4 TCPWM0_GRP0_CNT0_CC0

Counter compare/capture 0 register

Address: 0x40380010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	CC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	CC [31:24]							

Bits	Name	Description
31 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 4294967295

18.1.5 TCPWM0_GRP0_CNT0_CC0_BUFF

Counter buffered compare/capture 0 register

Address: 0x40380014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	CC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	CC [31:24]							

Bits	Name	Description
31 : 0	CC	Additional buffer for counter CC register. Default Value: 4294967295

18.1.6 TCPWM0_GRP0_CNT0_PERIOD

Counter period register

Address: 0x40380020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	PERIOD [31:24]							

Bits	Name	Description
31 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 4294967295

18.1.7 TCPWM0_GRP0_CNT0_PERIOD_BUFF

Counter buffered period register

Address: 0x40380024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	PERIOD [31:24]							

Bits	Name	Description
31 : 0	PERIOD	Additional buffer for counter PERIOD register. In PWM_PR mode PEROD_BUFF defines the LFSR polynomial. Each bit represents a tap of the shift register which can be feed back to the MSB via an XOR tree. Examples for GRP_CNT_WIDTH = 16: - Maximum length 16bit LFSR - polynomial x^16 + x^14 + x^13 + x^11 + 1 - taps 0,2,3,5 -> PERIOD = 0x002d - period is 2^16-1 = 65535 cycles - Maximum length 8bit LFSR: - polynomial x^8 + x^6 + x^5 + x^4 + 1 - taps 8,10,11,12 (realized in 8 MSBs of 16bit LFSR) - period is 2^8-1 = 255 cycles In SR mode PERIOD_BUFF defines which tap of the shift register generates the PWM output signals. For a delay of n cycles (from capture event to PWM output) the bit CNT_WIDTH-n should be set to '1'. For a shift register function only one tap should be use, i.e. a one-hot value must be written to PERIOD_BUFF. If multiple bits in PERIOD_BUFF are set then the taps are XOR combined. Default Value: 4294967295

18.1.8 TCPWM0_GRP0_CNT0_DT

Counter PWM dead time register

Address: 0x40380030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DT_LINE_OUT_L [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DT_LINE_OUT_L	In PWM_DT mode, this field is used to determine the low byte of the dead time before activating the PWM line output signal "line_out": amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Note: This field determines the low byte of the 16-bit dead time before activating "line_out" when parameter GRP_AMC_PRESENT for advanced motor control is set to 1. Otherwise the dead time is only 8 bit wide and the same dead time specified by this DT_LINE_OUT_L field is used before activating "line_out" and "line_compl_out". Default Value: 0 **0x0: DIVBY1 :** Divide by 1 (other-than-PWM_DT mode) **0x1: DIVBY2 :** Divide by 2 (other-than-PWM_DT mode)

18.1.8 TCPWM0_GRP0_CNT0_DT (continued)

0x2: DIVBY4 :

Divide by 4 (other-than-PWM_DT mode)

0x3: DIVBY8 :

Divide by 8 (other-than-PWM_DT mode)

0x4: DIVBY16 :

Divide by 16 (other-than-PWM_DT mode)

0x5: DIVBY32 :

Divide by 32 (other-than-PWM_DT mode)

0x6: DIVBY64 :

Divide by 64 (other-than-PWM_DT mode)

0x7: DIVBY128 :

Divide by 128 (other-than-PWM_DT mode)

18.1.9 TCPWM0_GRP0_CNT0_TR_CMD

Counter trigger command register

Address: 0x40380040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	RW1S	RW1S	None	RW1S
HW Access	None			RW1C	RW1C	RW1C	None	RW1C
Name	None [7:5]			START	STOP	RELOAD	None	CAPTURE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	START	SW start trigger. For HW behavior, see COUNTER_CAPTURE0 field. Default Value: 0
3	STOP	SW stop trigger. For HW behavior, see COUNTER_CAPTURE0 field. Default Value: 0
2	RELOAD	SW reload trigger. For HW behavior, see COUNTER_CAPTURE0 field. Default Value: 0
0	CAPTURE0	SW capture 0 trigger. When written with '1', a capture 0 trigger is generated and the HW sets the field to '0' when the SW trigger has taken effect. It should be noted that the HW operates on the counter frequency. If the counter is disabled through CTRL.ENABLED, the field is immediately set to '0'. Default Value: 0

18.1.10 TCPWM0_GRP0_CNT0_TR_IN_SEL0

Counter input trigger selection register 0

Address: 0x40380044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			CAPTURE0_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			COUNT_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			R				
Name	None [23:21]			RELOAD_SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			R				
Name	None [31:29]			STOP_SEL [28:24]				

Bits	Name	Description
28 : 24	STOP_SEL	Selects one of the 256 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
20 : 16	RELOAD_SEL	Selects one of the 256 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In these modes, it will update the counter with 0x8000 (counter midpoint) or 0x0000 depending on the QUAD_RANGE_MODE. Default Value: 0

18.1.10 TCPWM0_GRP0_CNT0_TR_IN_SEL0 (continued)

12 : 8	COUNT_SEL	Selects one of the 256 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Note: In the modes: TIMER, CAPTURE, PWM, PWM_DT, and SR. If the counter is externally triggered (COUNT_SEL > 1), an external trigger will be required for each TR_CMD to execute. For example, a write to TR_CMD.START will not start the counter until the trigger selected by COUNT_SEL asserts. The next trigger will increment the counter since the counter is now running. This goes for all TR_CMD fields. Default Value: 1
4 : 0	CAPTURE0_SEL	Selects one of the up to 256 input triggers as a capture0 trigger. Input trigger 0 is always '0' and input trigger 1 is always '1'. If existing, the one-to-one trigger inputs "tr_one_cnt_in" (different to each counter) are selected by setting 2 and above. The settings above are used for the general purpose trigger inputs "tr_all_cnt_in" connected to all counters selected. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0

18.1.11 TCPWM0_GRP0_CNT0_TR_IN_SEL1

Counter input trigger selection register 1

Address: 0x40380048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			START_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	START_SEL	Selects one of the 256 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0

18.1.12 TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL

Counter input trigger edge selection register

Address: 0x4038004C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE0_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	START_EDGE	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event. **0x2: ANY_EDGE :** Rising AND falling edge. Any odd amount of edges generates an event.

18.1.12 TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL (continued)

		0x3: NO_EDGE_DET : No edge detection, use trigger as is.
7 : 6	STOP_EDGE	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event. **0x2: ANY_EDGE :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.
5 : 4	RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event. **0x2: ANY_EDGE :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.
3 : 2	COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event.

18.1.12 TCPWM0_GRP0_CNT0_TR_IN_EDGE_SEL (continued)

		0x1: FALLING_EDGE : Falling edge. Any falling edge generates an event. **0x2: ANY_EDGE :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.
1 : 0	CAPTURE0_EDGE	A capture 0 event will copy the counter value into the CC0 register. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event. **0x2: ANY_EDGE :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.

18.1.13 TCPWM0_GRP0_CNT0_TR_PWM_CTRL

Counter trigger PWM control register

Address: 0x40380050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC0_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	UNDERFLOW_MODE	Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3 **0x0: SET :** Set to '1' **0x1: CLEAR :** Set to '0' **0x2: INVERT :** Invert

18.1.13 TCPWM0_GRP0_CNT0_TR_PWM_CTRL (continued)

		0x3: NO_CHANGE : No Change
3 : 2	OVERFLOW_MODE	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3 **0x0: SET :** Set to '1' **0x1: CLEAR :** Set to '0' **0x2: INVERT :** Invert **0x3: NO_CHANGE :** No Change
1 : 0	CC0_MATCH_MODE	Determines the effect of a compare match 0 event (COUNTER equals CC0 register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0%, the counter CC0 register should be set to "0". For a 100% duty cycle, the counter CC0 register should be set to larger than the counter PERIOD register. Default Value: 3 **0x0: SET :** Set to '1' **0x1: CLEAR :** Set to '0' **0x2: INVERT :** Invert **0x3: NO_CHANGE :** No Change

18.1.14 TCPWM0_GRP0_CNT0_TR_OUT_SEL

Counter output trigger selection register

Address: 0x40380054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	OUT1 [6:4]			None	OUT0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 4	OUT1	Selects one of the internal events to generate the output trigger 1. Default setting selects the compare match 0 event. Default Value: 3 **0x0: OVERFLOW :** Overflow event **0x1: UNDERFLOW :** Underflow event **0x2: TC :** Terminal count event

18.1.14 TCPWM0_GRP0_CNT0_TR_OUT_SEL (continued)

		0x3: CC0_MATCH : Compare match 0 event (default selection) **0x4: CC1_MATCH :** Compare match 1 event **0x5: LINE_OUT :** PWM output signal "line_out" **0x6: Reserved6 :** This setting is reserved. Do not use. **0x7: Disabled :** Output trigger disabled.
2 : 0	OUT0	Selects one of the internal events to generate the output trigger 0. Default setting selects the terminal count event. Default Value: 2 **0x0: OVERFLOW :** Overflow event **0x1: UNDERFLOW :** Underflow event **0x2: TC :** Terminal count event (default selection) **0x3: CC0_MATCH :** Compare match 0 event **0x4: CC1_MATCH :** Compare match 1 event **0x5: LINE_OUT :** PWM output signal "line_out" **0x6: Reserved6 :** This setting is reserved. Do not use.

18.1.14 TCPWM0_GRP0_CNT0_TR_OUT_SEL (continued)

0x7: Disabled :

Output trigger disabled.

18.1.15 TCPWM0_GRP0_CNT0_INTR

Interrupt request register

Address: 0x40380070

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						CC0_-MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC0_MATCH	Counter matches CC0 register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

18.1.16 TCPWM0_GRP0_CNT0_INTR_SET

Interrupt set request register

Address: 0x40380074

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						CC0_-MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC0_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

18.1.17 TCPWM0_GRP0_CNT0_INTR_MASK

Interrupt mask register

Address: 0x40380078

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CC0_-MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC0_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

18.1.18 TCPWM0_GRP0_CNT0_INTR_MASKED

Interrupt masked request register

Address: 0x4038007C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CC0_-MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC0_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	TC	Logical and of corresponding request and mask bits. Default Value: 0

18.1.19 TCPWM0_GRP1_CNT0_CTRL

Counter control register

Address: 0x40388000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None	RW	RW	RW
HW Access	R	R	R	R	None	R	R	R
Name	CC1_-MATCH_DOWN_EN	CC1_-MATCH_UP_EN	CC0_-MATCH_DOWN_EN	CC0_-MATCH_UP_EN	None	AUTO_RE-LOAD_PE-RIOD	AUTO_RE-LOAD_CC1	AUTO_RE-LOAD_CC0

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		PWM_DISABLE_MODE [13:12]		None	PWM_SYN-C_KILL	PW-M_STOP_ON_KILL	PWM_IM-M_KILL

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		QUAD_ENCODING_-MODE [21:20]		None	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None			RW		
HW Access	R	R	None			R		
Name	ENABLED	DBG_-FREEZE_EN	None [29:27]			MODE [26:24]		

Bits	Name	Description
31	ENABLED	Counter enable. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_IN_SEL, TR_IN_EDGE_-SEL, TR_PWM_CTRL and TR_OUT_SEL register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_out0" and tr_out1"). - the counter's line outputs ("line_out" and "line_compl_out"). Default Value: 0

18.1.19 TCPWM0_GRP1_CNT0_CTRL (continued)

30	DBG_FREEZE_EN	Specifies the counter behavior in debug mode. '0': The counter operation continues in debug mode. '1': The counter operation freezes in debug mode. Default Value: 0
26 : 24	MODE	Counter mode. Default Value: 0 **0x0: TIMER :** Timer mode **0x1: Reserved1 :** This setting is reserved. Do not use. **0x2: CAPTURE :** Capture mode **0x3: QUAD :** Quadrature mode Different encoding modes can be selected by QUAD_ENCODING_MODE including up/down count functionality. Different counter range, reload value and capture behavior can be selected by QUAD_RANGE_-MODE (overloaded field UP_DOWN_MODE). **0x4: PWM :** Pulse width modulation (PWM) mode **0x5: PWM_DT :** PWM with deadtime insertion mode **0x6: PWM_PR :** Pseudo random pulse width modulation **0x7: SR :** Shift register mode.
21 : 20	QUAD_ENCODING_-MODE	In QUAD mode this field selects the quadrature encoding mode (X1/X2/X4) or the Up / Down rotary counting mode. In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_com-pl_out"; i.e. a disabled output line "dt_line_out" has the value QUAD_ENCODING_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUAD_ENCODING_MODE[1]. Default Value: 0

18.1.19 TCPWM0_GRP1_CNT0_CTRL (continued)

0x0: X1 :

X1 encoding (QUAD mode)
This encoding is identical with an up / down counting functionality of the following way: Rising edges of input phiA increment or decrement the counter depending on the state of input phiB (direction input).

0x1: X2 :

X2 encoding (QUAD mode)

0x2: X4 :

X4 encoding (QUAD mode)

0x3: UP_DOWN :

Up / Down rotary counting mode. Input phiA increments the counter, input phiB decrements the counter. The trigger edge detection settings apply.

0x1: INV_OUT :

When bit 0 is '1', QUADRATURE_ENCODING_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes)

0x2: INV_COMPL_OUT :

When bit 1 is '1', QUADRATURE_ENCODING_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)

18	ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	UP_DOWN_MODE	Determines counter direction. In QUAD mode this field acts as QUAD_RANGE_MODE field selecting between different counter range, reload value and compare / capture behavior. Default Value: 0

0x0: COUNT_UP :

Count up (to PERIOD). An overflow event is generated when the counter changes from a state in which COUNTER equals PERIOD. A terminal count event is generated when the counter changes from a state in which COUNTER equals PERIOD.

0x1: COUNT_DOWN :

Count down (to "0"). An underflow event is generated when the counter changes from a state in which COUNTER equals "0". A terminal count event is generated when the counter changes from a state in which COUNTER equals "0".

18.1.19 TCPWM0_GRP1_CNT0_CTRL (continued)

0x2: COUNT_UPDN1 :

Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter changes from a state in which COUNTER equals PERIOD. An underflow event is generated when the counter changes from a state in which COUNTER equals "0". A terminal count event is generated when the counter changes from a state in which COUNTER equals "0".

0x3: COUNT_UPDN2 :

Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter changes from a state in which COUNTER equals PERIOD. An underflow event is generated when the counter changes from a state in which COUNTER equals "0". A terminal count event is generated when the counter changes from a state in which COUNTER equals "0" AND when the counter changes from a state in which COUNTER equals PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).

0x0: QUAD_RANGE0 :

In QUAD mode this setting selects the QUAD_RANGE0 mode with the following behavior:
- COUNTER range is between 0x0000 and 0xFFFF / 0xFFFFFFFF (for GRP_CNT_WIDTH = 16 / 32)
- on reload / index event:
 - CC0 is copied to CC0_BUFF
 - COUNTER is copied to CC0
 - COUNTER is set to midpoint (0x8000 / 0x80000000)
 - tc and cc0_match events are generated
- when COUNTER is 0x0000 or 0xFFFF / 0xFFFFFFFF:
 - CC0 is copied to CC0_BUFF
 - COUNTER (0x0000 or 0xFFFF / 0xFFFFFFFF) is copied to CC0
 - COUNTER is set to midpoint (0x8000 / 0x80000000)
 - cc0_match event is generated

This mode is 100% backward compatible with previous TCPWM quadrature behavior.

18.1.19 TCPWM0_GRP1_CNT0_CTRL (continued)

0x1: QUAD_RANGE0_CMP :

In QUAD mode this setting selects the QUAD_RANGE0_CMP mode with the following behavior:
- COUNTER range is between 0x0000 and 0xFFFF / 0xFFFFFFFF (for GRP_CNT_WIDTH = 16 / 32)
- the capture0 event acts as 2nd reload / index event
- on reload / index event:
 - COUNTER is set to midpoint (0x8000 / 0x80000000)
 - when 'capture on index' is selected (AUTO_RELOAD_PERIOD=0):
 - tc event is generated
 - PERIOD is copied to PERIOD_BUFF
 - COUNTER is copied to PERIOD
- when COUNTER is 0x0000 or 0xFFFF / 0xFFFFFFFF:
 - COUNTER is set to midpoint (0x8000 / 0x80000000)
 - when 'capture on wrap-around' is selected (AUTO_RELOAD_PERIOD=1):
 - tc event is generated
 - PERIOD is copied to PERIOD_BUFF
 - COUNTER (0x0000 or 0xFFFF / 0xFFFFFFFF) is copied to PERIOD
- 1 or 2 compare functions (depending on CC1_PRESENT) available

This mode is to a certain extend backward compatible with previous TCPWM quadrature behavior but allows a compare function during quadrature decoding using the CC0/CC_BUFF registers and the cc0_match event. Because of that the PERIOD/PERIOD_BUFF registers are used instead of CC0/CC_BUFF registers to capture COUNTER at reload / index event or wrap-around.

0x2: QUAD_RANGE1_CAPT :

In QUAD mode this setting selects the QUAD_RANGE1_CAPT mode with the following behavior:
- COUNTER range is between 0x0000 and PERIOD
- on reload / index event:
 - COUNTER is set to 0x0000
 - tc event is generated
- when COUNTER is 0x0000 and decrementing:
 - COUNTER is set to PERIOD
 - tc event is generated
- when COUNTER equals PERIOD and is incrementing:
 - COUNTER is set to 0x0000
 - tc event is generated
- 1 or 2 capture functions (depending on CC1_PRESENT) available
- on capture0 / capture1 event:
 - CC0 / CC1 is copied to CC0_BUFF / CC1_BUFF
 - COUNTER value is copied to CC0

This mode is NOT backward compatible with previous TCPWM quadrature behavior. It is to a certain extend compatible with previous Traveo 1 QPRC behavior. It allows that the COUNTER register reflects the current angle position of the rotary encoder, i.e. no MOD or SUB calculations need to be done in SW on the COUNTER value to get the current angle position. This allows a DMA copy of the angle position from the COUNTER register. However, a disadvantage of this mode is that fast sequences of tc interrupts can occur (when encoder moves back and forth around start position). It is recommended to not use the tc interrupt in this mode.

0x3: QUAD_RANGE1_CMP :

In QUAD mode this setting selects the QUAD_RANGE1_CMP mode.
The behavior is the same as for QUAD_RANGE1_CAPT mode described above with the only difference that 1 or 2 compare functions (depending on CC1_PRESENT) are available instead of 1 or 2 capture functions.

18.1.19 TCPWM0_GRP1_CNT0_CTRL (continued)

13 : 12	PWM_DISABLE_MODE	Specifies the behavior of the PWM outputs "line_out" and "line_compl_out" while the TCPWM counter is disabled (CTL.ENABLED='0') or stopped. Note: The output signal of this selection can be further modified by the immediate kill logic and line_out polarity settings (CTRL.QUAD_ENCODING_MODE). Default Value: 0 **0x0: Z :** The behavior is the same is in previous mxtcpwm (version 1). When the counter is disabled the PWM outputs "line_out" and "line_compl_out" are NOT driven by the TCPWM. Instead the port default level configuration applies, e.g. "Z" (high impedance). Note: This is realized by driving the TCPWM output "line_out_en" to 0. When the counter is stopped upon a stop event the PWM outputs are deactivated (to the polarity defined by CTL.QUAD_ENCODING_MODE). **0x1: RETAIN :** When the counter is disabled the PWM outputs "line_out" and "line_compl_out" are driven by the TCPWM. When the counter is disabled or stopped upon a stop event the PWM outputs are retained (keep their previous levels). While the counter is disabled or stopped the PWM outputs can be changed via LINE_SEL (when parameter GRP_SMC_PRESENT = 1). **0x2: L :** When the counter is disabled the PWM outputs "line_out" and "line_compl_out" are driven by the TCPWM. When the counter is disabled or stopped upon a stop event the PWM output "line_out" is driven as a fixed '0' and the PWM output "line_compl_out" is driven as a fixed '1'. **0x3: H :** When the counter is disabled the PWM outputs "line_out" and "line_compl_out" are driven by the TCPWM. When the counter is disabled or stopped upon a stop event the PWM output "line_out" is driven as a fixed '1' and the PWM output "line_compl_out" is driven as a fixed '0'.
10	PWM_SYNC_KILL	Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
9	PWM_STOP_ON_KILL	Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0

18.1.19 TCPWM0_GRP1_CNT0_CTRL (continued)

8	PWM_IMM_KILL	Specifies whether the kill event immediately deactivates the "dt_line_out" and "dt_line_compl_out" signals or with the next module clock ("active count" pre-scaled "clk_counter"). '0': synchronous kill activation. Deactivates the "dt_line_out" and "dt_line_compl_out" signals with the next module clock ("active count" pre-scaled "clk_counter"). '1': immediate kill activation. Immediately deactivates the "dt_line_out" and "dt_line_compl_out" signals. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
7	CC1_MATCH_DOWN_EN	Enables / disables the compare match 1 event generation (COUNTER equals CC0 register) when counting down (STATUS.DOWN = 1) in CNT_UPDN1/2 mode. '0': compare match 1 event generation disabled when counting down '1': compare match 1 event generation enabled when counting down This field has a function in PWM and PWM_DT modes only. Default Value: 1
6	CC1_MATCH_UP_EN	Enables / disables the compare match 1 event generation (COUNTER equals CC0 register) when counting up (STATUS.DOWN = 0) in CNT_UPDN1/2 mode. '0': compare match 1 event generation disabled when counting up '1': compare match 1 event generation enabled when counting up This field has a function in PWM and PWM_DT modes only. Default Value: 1
5	CC0_MATCH_DOWN_EN	Enables / disables the compare match 0 event generation (COUNTER equals CC0 register) when counting down (STATUS.DOWN = 1) in CNT_UPDN1/2 mode. '0': compare match 0 event generation disabled when counting down '1': compare match 0 event generation enabled when counting down This field has a function in PWM and PWM_DT modes only. Default Value: 1
4	CC0_MATCH_UP_EN	Enables / disables the compare match 0 event generation (COUNTER equals CC0 register) when counting up (STATUS.DOWN = 0) in CNT_UPDN1/2 mode. '0': compare match 0 event generation disabled when counting up '1': compare match 0 event generation enabled when counting up This field has a function in PWM and PWM_DT modes only. Default Value: 1
2	AUTO_RELOAD_PERIOD	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM and PWM_DT modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. In QUAD mode, QUAD_RANGE0_CMP range mode this field is used to select the index / wrap-around capture function. '0': Captures on index (reload) event. The counter value is copied to the PERIOD register on an index (reload) event. '1': Captures when COUNTER equals 0 or 0xffff. The counter value is copied to the PERIOD register when COUNTER equals 0 or 0xffff. Default Value: 0
1	AUTO_RELOAD_CC1	Specifies switching of the CC1 and buffered CC1 values. This field has a function in TIMER, QUAD (QUAD_RANGE0_CMP, QUAD_RANGE1_CMP range modes), SR, PWM, PWM_DT and PWM_PR modes. Timer, QUAD, SR modes: '0': never switch. '1': switch on a compare match 1 event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0

18.1.19 TCPWM0_GRP1_CNT0_CTRL (continued)

0	AUTO_RELOAD_CC0	Specifies switching of the CC0 and buffered CC0 values. This field has a function in TIMER, QUAD (QUAD_RANGE0_CMP, QUAD_RANGE1_CMP range modes), SR, PWM, PWM_DT and PWM_PR modes. Timer, QUAD, SR modes: '0': never switch. '1': switch on a compare match 0 event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0

18.1.20 TCPWM0_GRP1_CNT0_STATUS

Counter status register

Address: 0x40388004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	None			R
HW Access	RW	RW	RW	RW	None			RW
Name	TR_STOP	TR_RE-LOAD	TR_COUNT	TR_CAP-TURE0	None [3:1]			DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R	None			R	R	R	R
HW Access	RW	None			RW	RW	RW	RW
Name	RUNNING	None [14:12]			LINE_COM-PL_OUT	LINE_OUT	TR_CAP-TURE1	TR_START

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	DT_CNT_L [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	DT_CNT_H [31:24]							

Bits	Name	Description
31 : 24	DT_CNT_H	High byte of 16-bit dead time counter. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this field has no effect. Note: This field only exists when parameter GRP_AMC_PRESENT for advanced motor control is set to 1. Otherwise the dead time is only 8bit wide and the only the field DT_CNT_L is used as dead time counter. Default Value: 0
23 : 16	DT_CNT_L	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion (8bit dead time counter or low byte of 16-bit dead time counter). In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0

18.1.20 TCPWM0_GRP1_CNT0_STATUS (continued)

15	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. This field is used to indicate that the counter is running after a start/reload event and that the counter is stopped after a stop event. When a running counter operation is paused in debug state (see CTRL.DBG_PAUSE) then the RUNNING bit is still '1'. Default Value: 0
11	LINE_COMPL_OUT	Indicates the actual level of the complementary PWM line output signal. Default Value: 0
10	LINE_OUT	Indicates the actual level of the PWM line output signal. Default Value: 0
9	TR_CAPTURE1	Indicates the actual level of the selected capture 1 trigger. Default Value: 0
8	TR_START	Indicates the actual level of the selected start trigger. Default Value: 0
7	TR_STOP	Indicates the actual level of the selected stop trigger. Default Value: 0
6	TR_RELOAD	Indicates the actual level of the selected reload trigger. Default Value: 0
5	TR_COUNT	Indicates the actual level of the selected count trigger. Default Value: 1
4	TR_CAPTURE0	Indicates the actual level of the selected capture 0 trigger. Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

18.1.21 TCPWM0_GRP1_CNT0_COUNTER

Counter count register

Address: 0x40388008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	16-bit / 32-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

18.1.22 TCPWM0_GRP1_CNT0_CC0

Counter compare/capture 0 register

Address: 0x40388010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

18.1.23 TCPWM0_GRP1_CNT0_CC0_BUFF

Counter buffered compare/capture 0 register

Address: 0x40388014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC register. Default Value: 65535

18.1.24 TCPWM0_GRP1_CNT0_CC1

Counter compare/capture 1 register

Address: 0x40388018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

18.1.25 TCPWM0_GRP1_CNT0_CC1_BUFF

Counter buffered compare/capture 1 register

Address: 0x4038801C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC1 register. Default Value: 65535

18.1.26 TCPWM0_GRP1_CNT0_PERIOD

Counter period register

Address: 0x40388020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

18.1.27 TCPWM0_GRP1_CNT0_PERIOD_BUFF

Counter buffered period register

Address: 0x40388024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Additional buffer for counter PERIOD register. In PWM_PR mode PEROD_BUFF defines the LFSR polynomial. Each bit represents a tap of the shift register which can be feed back to the MSB via an XOR tree. Examples for GRP_CNT_WIDTH = 16: - Maximum length 16bit LFSR - polynomial x^16 + x^14 + x^13 + x^11 + 1 - taps 0,2,3,5 -> PERIOD = 0x002d - period is 2^16-1 = 65535 cycles - Maximum length 8bit LFSR: - polynomial x^8 + x^6 + x^5 + x^4 + 1 - taps 8,10,11,12 (realized in 8 MSBs of 16bit LFSR) - period is 2^8-1 = 255 cycles In SR mode PERIOD_BUFF defines which tap of the shift register generates the PWM output signals. For a delay of n cycles (from capture event to PWM output) the bit CNT_WIDTH-n should be set to '1'. For a shift register function only one tap should be use, i.e. a one-hot value must be written to PERIOD_BUFF. If multiple bits in PERIOD_BUFF are set then the taps are XOR combined. Default Value: 65535

18.1.28 TCPWM0_GRP1_CNT0_DT

Counter PWM dead time register

Address: 0x40388030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DT_LINE_OUT_L [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DT_LINE_OUT_H [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DT_LINE_COMPL_OUT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DT_LINE_COMPL_OUT [31:24]							

Bits	Name	Description
31 : 16	DT_LINE_COMPL_OUT	In PWM_DT mode, this field is used to determine the dead time before activating the complementary PWM line output signal "line_compl_out": amount of dead time cycles in the counter clock domain. In all other modes, this field has no effect. Note: This field only exists when parameter GRP_AMC_PRESENT for advanced motor control is set to 1. Otherwise the dead time is only 8 bit wide and the same dead time specified by field DT_LINE_OUT_L is used before activating "line_out" and "line_compl_out". Default Value: 0
15 : 8	DT_LINE_OUT_H	In PWM_DT mode, this field is used to determine the high byte of the dead time before activating the PWM line output signal "line_out": amount of dead time cycles in the counter clock domain. In all other modes, this field has no effect. Note: This field only exists when parameter GRP_AMC_PRESENT for advanced motor control is set to 1. Otherwise the dead time is only 8 bit wide and the same dead time specified by field DT_LINE_OUT_L is used before activating "line_out" and "line_compl_out". Default Value: 0

18.1.28 TCPWM0_GRP1_CNT0_DT (continued)

7 : 0	DT_LINE_OUT_L	In PWM_DT mode, this field is used to determine the low byte of the dead time before activating the PWM line output signal "line_out": amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Note: This field determines the low byte of the 16-bit dead time before activating "line_out" when parameter GRP_AMC_PRESENT for advanced motor control is set to 1. Otherwise the dead time is only 8 bit wide and the same dead time specified by this DT_LINE_OUT_L field is used before activating "line_out" and "line_compl_out". Default Value: 0 **0x0: DIVBY1 :** Divide by 1 (other-than-PWM_DT mode) **0x1: DIVBY2 :** Divide by 2 (other-than-PWM_DT mode) **0x2: DIVBY4 :** Divide by 4 (other-than-PWM_DT mode) **0x3: DIVBY8 :** Divide by 8 (other-than-PWM_DT mode) **0x4: DIVBY16 :** Divide by 16 (other-than-PWM_DT mode) **0x5: DIVBY32 :** Divide by 32 (other-than-PWM_DT mode) **0x6: DIVBY64 :** Divide by 64 (other-than-PWM_DT mode) **0x7: DIVBY128 :** Divide by 128 (other-than-PWM_DT mode)

18.1.29 TCPWM0_GRP1_CNT0_TR_CMD

Counter trigger command register

Address: 0x40388040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1S	RW1S	RW1S	RW1S	None	RW1S
HW Access	None		RW1C	RW1C	RW1C	RW1C	None	RW1C
Name	None [7:6]		CAPTURE1	START	STOP	RELOAD	None	CAPTURE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	CAPTURE1	SW capture 1 trigger. For HW behavior, see COUNTER_CAPTURE0 field. Default Value: 0
4	START	SW start trigger. For HW behavior, see COUNTER_CAPTURE0 field. Default Value: 0
3	STOP	SW stop trigger. For HW behavior, see COUNTER_CAPTURE0 field. Default Value: 0
2	RELOAD	SW reload trigger. For HW behavior, see COUNTER_CAPTURE0 field. Default Value: 0
0	CAPTURE0	SW capture 0 trigger. When written with '1', a capture 0 trigger is generated and the HW sets the field to '0' when the SW trigger has taken effect. It should be noted that the HW operates on the counter frequency. If the counter is disabled through CTRL.ENABLED, the field is immediately set to '0'. Default Value: 0

18.1.30 TCPWM0_GRP1_CNT0_TR_IN_SEL1

Counter input trigger selection register 1

Address: 0x40388048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			START_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			CAPTURE1_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12 : 8	CAPTURE1_SEL	Selects one of the 256 input triggers as a capture 1 trigger. Default Value: 0
4 : 0	START_SEL	Selects one of the 256 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0

18.1.31 TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL

Counter input trigger edge selection register

Address: 0x4038804C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE0_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [15:12]				CAPTURE1_EDGE [11:10]		START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 10	CAPTURE1_EDGE	A capture 1 event will copy the counter value into the CC1 register. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event. **0x2: ANY_EDGE :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.

18.1.31 TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL (continued)

9 : 8	START_EDGE	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event. **0x2: ANY_EDGE :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.
7 : 6	STOP_EDGE	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event. **0x2: ANY_EDGE :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.
5 : 4	RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event.

18.1.31 TCPWM0_GRP1_CNT0_TR_IN_EDGE_SEL (continued)

		0x2: ANY_EDGE : Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.
3 : 2	COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event. **0x2: ANY_EDGE :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.
1 : 0	CAPTURE0_EDGE	A capture 0 event will copy the counter value into the CC0 register. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event. **0x2: ANY_EDGE :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.

18.1.32 TCPWM0_GRP1_CNT0_TR_PWM_CTRL

Counter trigger PWM control register

Address: 0x40388050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	CC1_MATCH_MODE [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC0_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	CC1_MATCH_MODE	Determines the effect of a compare match 1 event (COUNTER equals CC1 register) on the "line_out" output signals. Default Value: 3 **0x0: SET :** Set to '1' **0x1: CLEAR :** Set to '0' **0x2: INVERT :** Invert

18.1.32 TCPWM0_GRP1_CNT0_TR_PWM_CTRL (continued)

		0x3: NO_CHANGE : No Change
5 : 4	UNDERFLOW_MODE	Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3 **0x0: SET :** Set to '1' **0x1: CLEAR :** Set to '0' **0x2: INVERT :** Invert **0x3: NO_CHANGE :** No Change
3 : 2	OVERFLOW_MODE	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3 **0x0: SET :** Set to '1' **0x1: CLEAR :** Set to '0' **0x2: INVERT :** Invert **0x3: NO_CHANGE :** No Change
1 : 0	CC0_MATCH_MODE	Determines the effect of a compare match 0 event (COUNTER equals CC0 register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0%, the counter CC0 register should be set to "0". For a 100% duty cycle, the counter CC0 register should be set to larger than the counter PERIOD register. Default Value: 3

18.1.32 TCPWM0_GRP1_CNT0_TR_PWM_CTRL (continued)

0x0: SET :

Set to '1'

0x1: CLEAR :

Set to '0'

0x2: INVERT :

Invert

0x3: NO_CHANGE :

No Change

18.1.33 TCPWM0_GRP1_CNT0_INTR

Interrupt request register

Address: 0x40388070

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [7:3]					CC1_-MATCH	CC0_-MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CC1_MATCH	Counter matches CC1 register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
1	CC0_MATCH	Counter matches CC0 register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

18.1.34 TCPWM0_GRP1_CNT0_INTR_SET

Interrupt set request register

Address: 0x40388074

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [7:3]					CC1_-MATCH	CC0_-MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CC1_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	CC0_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

18.1.35 TCPWM0_GRP1_CNT0_INTR_MASK

Interrupt mask register

Address: 0x40388078

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					CC1_-MATCH	CC0_-MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CC1_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	CC0_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

18.1.36 TCPWM0_GRP1_CNT0_INTR_MASKED

Interrupt masked request register

Address: 0x4038807C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [7:3]					CC1_-MATCH	CC0_-MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CC1_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
1	CC0_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	TC	Logical and of corresponding request and mask bits. Default Value: 0

19 Segment LCD Drive Registers

This section discusses the Segment LCD Drive registers. It lists all the registers in mapping tables, in address order.

19.1 Register Details

Register	Address	Description
LCD0_ID	0x403B0000	ID & Revision
LCD0_DIVIDER	0x403B0004	LCD Divider Register
LCD0_CONTROL	0x403B0008	LCD Configuration Register
LCD0_DATA00	0x403B0100	LCD Pin Data Registers
LCD0_DATA01	0x403B0104	LCD Pin Data Registers. See LCD0_DATA00 for the details of bit fields.
LCD0_DATA02	0x403B0108	LCD Pin Data Registers. See LCD0_DATA00 for the details of bit fields.
LCD0_DATA03	0x403B010C	LCD Pin Data Registers. See LCD0_DATA00 for the details of bit fields.
LCD0_DATA04	0x403B0110	LCD Pin Data Registers. See LCD0_DATA00 for the details of bit fields.
LCD0_DATA05	0x403B0114	LCD Pin Data Registers. See LCD0_DATA00 for the details of bit fields.
LCD0_DATA06	0x403B0118	LCD Pin Data Registers. See LCD0_DATA00 for the details of bit fields.
LCD0_DATA07	0x403B011C	LCD Pin Data Registers. See LCD0_DATA00 for the details of bit fields.
LCD0_DATA10	0x403B0200	LCD Pin Data Registers
LCD0_DATA11	0x403B0204	LCD Pin Data Registers. See LCD0_DATA10 for the details of bit fields.
LCD0_DATA12	0x403B0208	LCD Pin Data Registers. See LCD0_DATA10 for the details of bit fields.
LCD0_DATA13	0x403B020C	LCD Pin Data Registers. See LCD0_DATA10 for the details of bit fields.
LCD0_DATA14	0x403B0210	LCD Pin Data Registers. See LCD0_DATA10 for the details of bit fields.
LCD0_DATA15	0x403B0214	LCD Pin Data Registers. See LCD0_DATA10 for the details of bit fields.
LCD0_DATA16	0x403B0218	LCD Pin Data Registers. See LCD0_DATA10 for the details of bit fields.
LCD0_DATA17	0x403B021C	LCD Pin Data Registers. See LCD0_DATA10 for the details of bit fields.

19.1.1 LCD0_ID

ID & Revision

Address: 0x403B0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	REVISION [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	REVISION [31:24]							

Bits	Name	Description
31 : 16	REVISION	the version number is 0x0002 Default Value: 0X0002
15 : 0	ID	the ID of LCD controller peripheral is 0xF0F0 Default Value: 0XF0F0

19.1.2 LCD0_DIVIDER

LCD Divider Register

Address: 0x403B0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SUBFR_DIV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SUBFR_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DEAD_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DEAD_DIV [31:24]							

Bits	Name	Description
31 : 16	DEAD_DIV	Length of the dead time period in cycles. When set to zero, no dead time period exists. Default Value: 0
15 : 0	SUBFR_DIV	Input clock frequency divide value, to generate the 1/4 sub-frame period. The sub-frame period is 4*(SUBFR_DIV+1) cycles long. Default Value: 0

19.1.3 LCD0_CONTROL

LCD Configuration Register

Address: 0x403B0008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW		RW	RW	RW	RW	RW
HW Access	R	R		R	R	R	R	R
Name	CLOCK_LS_SEL	BIAS [6:5]		OP_MODE	TYPE	LCD_-MODE	HS_EN	LS_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				COM_NUM [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	LS_EN_STAT	None [30:24]						

Bits	Name	Description
31	LS_EN_STAT	LS enable status bit. This bit is a copy of LS_EN that is synchronized to the low speed clock domain and back to the system clock domain. Firmware can use this bit to observe whether LS_EN has taken effect in the low speed clock domain. Firmware should never change the configuration for the LS generator without ensuring this bit is 0. The following procedure should be followed to disable the LS generator: 1. If LS_EN=0 we are done. Exit the procedure. 2. Check that LS_EN_STAT=1. If not, wait until it is. This will catch the case of a recent enable (LS_EN=1) that has not taken effect yet. 3. Set LS_EN=0. 4. Wait until LS_EN_STAT=0. Default Value: 0

19.1.3 LCD0_CONTROL (continued)

11 : 8	COM_NUM	The number of COM connections minus 2. So: 0: 2 COM's 1: 3 COM's ... 13: 15 COM's 14: 16 COM's 15: undefined Default Value: 0
7	CLOCK_LS_SEL	Low speed (LS) generator clock source selection 1: select clk_mf 0: select clk_lf Default Value: 0
6 : 5	BIAS	PWM bias selection Default Value: 0 **0x0: HALF :** 1/2 Bias **0x1: THIRD :** 1/3 Bias **0x2: FOURTH :** 1/4 Bias **0x3: FIFTH :** 1/5 Bias
4	OP_MODE	Driving mode configuration Default Value: 0 **0x0: PWM :** PWM Mode **0x1: CORRELATION :** Digital Correlation Mode
3	TYPE	LCD driving waveform type configuration. Default Value: 0 **0x0: TYPE_A :** Type A - Each frame addresses each COM pin only once with a balanced (DC=0) waveform. **0x1: TYPE_B :** Type B - Each frame addresses each COM pin twice in sequence with a positive and negative waveform that together are balanced (DC=0).

19.1.3 LCD0_CONTROL (continued)

2	LCD_MODE	HS/LS Mode selection Default Value: 0 **0x0: LS :** Select Low Speed Generator (Works in Active, Sleep and DeepSleep power modes). Low speed clock (clk_lf) or middle speed clock (clk_mf) can be selected for Low Speed Generator. **0x1: HS :** Select High Speed (system clock) Generator (Works in Active and Sleep power modes only).
1	HS_EN	High speed (HS) generator enable 1: enable 0: disable Default Value: 0
0	LS_EN	Low speed (LS) generator enable 1: enable 0: disable Default Value: 0

19.1.4 LCD0_DATA00

LCD Pin Data Registers

Address: 0x403B0100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

19.1.5 LCD0_DATA10

LCD Pin Data Registers

Address: 0x403B0200

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 5-8 (COM5 is lsb). Default Value: 0

20 USB Registers

This section discusses the USB registers. It lists all the registers in mapping tables, in address order.

20.1 Register Details

Register	Address	Description
USBFS0_USBDEV_EP0_DR0	0x403F0000	Control End point EP0 Data Register
USBFS0_USBDEV_EP0_DR1	0x403F0004	Control End point EP0 Data Register. See USBFS0_USBDEV_EP0_DR0 for the details of bit fields.
USBFS0_USBDEV_EP0_DR2	0x403F0008	Control End point EP0 Data Register. See USBFS0_USBDEV_EP0_DR0 for the details of bit fields.
USBFS0_USBDEV_EP0_DR3	0x403F000C	Control End point EP0 Data Register. See USBFS0_USBDEV_EP0_DR0 for the details of bit fields.
USBFS0_USBDEV_EP0_DR4	0x403F0010	Control End point EP0 Data Register. See USBFS0_USBDEV_EP0_DR0 for the details of bit fields.
USBFS0_USBDEV_EP0_DR5	0x403F0014	Control End point EP0 Data Register. See USBFS0_USBDEV_EP0_DR0 for the details of bit fields.
USBFS0_USBDEV_EP0_DR6	0x403F0018	Control End point EP0 Data Register. See USBFS0_USBDEV_EP0_DR0 for the details of bit fields.
USBFS0_USBDEV_EP0_DR7	0x403F001C	Control End point EP0 Data Register. See USBFS0_USBDEV_EP0_DR0 for the details of bit fields.
USBFS0_USBDEV_CR0	0x403F0020	USB control 0 Register
USBFS0_USBDEV_CR1	0x403F0024	USB control 1 Register
USBFS0_USBDEV_SIE_EP_INT_EN	0x403F0028	USB SIE Data Endpoints Interrupt Enable Register
USBFS0_USBDEV_SIE_EP_INT_SR	0x403F002C	USB SIE Data Endpoint Interrupt Status
USBFS0_USBDEV_SIE_EP1_CNT0	0x403F0030	Non-control endpoint count register
USBFS0_USBDEV_SIE_EP1_CNT1	0x403F0034	Non-control endpoint count register
USBFS0_USBDEV_SIE_EP1_CR0	0x403F0038	Non-control endpoint's control Register
USBFS0_USBDEV_USBIO_CR0	0x403F0040	USBIO Control 0 Register
USBFS0_USBDEV_USBIO_CR2	0x403F0044	USBIO control 2 Register
USBFS0_USBDEV_USBIO_CR1	0x403F0048	USBIO control 1 Register
USBFS0_USBDEV_DYN_RECONFIG	0x403F0050	USB Dynamic reconfiguration register
USBFS0_USBDEV_SOF0	0x403F0060	Start Of Frame Register
USBFS0_USBDEV_SOF1	0x403F0064	Start Of Frame Register
USBFS0_USBDEV_SIE_EP2_CNT0	0x403F0070	Non-control endpoint count register. See USBFS0_USBDEV_SIE_EP1_CNT0 for the details of bit fields.
USBFS0_USBDEV_SIE_EP2_CNT1	0x403F0074	Non-control endpoint count register. See USBFS0_USBDEV_SIE_EP1_CNT1 for the details of bit fields.

Register	Address	Description
USBFS0_USBDEV_SIE_EP2_CR0	0x403F0078	Non-control endpoint's control Register. See USBFS0_USBDEV_SIE_EP1_CR0 for the details of bit fields.
USBFS0_USBDEV_OSCLK_DR0	0x403F0080	Oscillator lock data register 0
USBFS0_USBDEV_OSCLK_DR1	0x403F0084	Oscillator lock data register 1
USBFS0_USBDEV_EP0_CR	0x403F00A0	Endpoint0 control Register
USBFS0_USBDEV_EP0_CNT	0x403F00A4	Endpoint0 count Register
USBFS0_USBDEV_SIE_EP3_CNT0	0x403F00B0	Non-control endpoint count register. See USBFS0_USBDEV_SIE_EP1_CNT0 for the details of bit fields.
USBFS0_USBDEV_SIE_EP3_CNT1	0x403F00B4	Non-control endpoint count register. See USBFS0_USBDEV_SIE_EP1_CNT1 for the details of bit fields.
USBFS0_USBDEV_SIE_EP3_CR0	0x403F00B8	Non-control endpoint's control Register. See USBFS0_USBDEV_SIE_EP1_CR0 for the details of bit fields.
USBFS0_USBDEV_SIE_EP4_CNT0	0x403F00F0	Non-control endpoint count register. See USBFS0_USBDEV_SIE_EP1_CNT0 for the details of bit fields.
USBFS0_USBDEV_SIE_EP4_CNT1	0x403F00F4	Non-control endpoint count register. See USBFS0_USBDEV_SIE_EP1_CNT1 for the details of bit fields.
USBFS0_USBDEV_SIE_EP4_CR0	0x403F00F8	Non-control endpoint's control Register. See USBFS0_USBDEV_SIE_EP1_CR0 for the details of bit fields.
USBFS0_USBDEV_SIE_EP5_CNT0	0x403F0130	Non-control endpoint count register. See USBFS0_USBDEV_SIE_EP1_CNT0 for the details of bit fields.
USBFS0_USBDEV_SIE_EP5_CNT1	0x403F0134	Non-control endpoint count register. See USBFS0_USBDEV_SIE_EP1_CNT1 for the details of bit fields.
USBFS0_USBDEV_SIE_EP5_CR0	0x403F0138	Non-control endpoint's control Register. See USBFS0_USBDEV_SIE_EP1_CR0 for the details of bit fields.
USBFS0_USBDEV_SIE_EP6_CNT0	0x403F0170	Non-control endpoint count register. See USBFS0_USBDEV_SIE_EP1_CNT0 for the details of bit fields.
USBFS0_USBDEV_SIE_EP6_CNT1	0x403F0174	Non-control endpoint count register. See USBFS0_USBDEV_SIE_EP1_CNT1 for the details of bit fields.
USBFS0_USBDEV_SIE_EP6_CR0	0x403F0178	Non-control endpoint's control Register. See USBFS0_USBDEV_SIE_EP1_CR0 for the details of bit fields.
USBFS0_USBDEV_SIE_EP7_CNT0	0x403F01B0	Non-control endpoint count register. See USBFS0_USBDEV_SIE_EP1_CNT0 for the details of bit fields.
USBFS0_USBDEV_SIE_EP7_CNT1	0x403F01B4	Non-control endpoint count register. See USBFS0_USBDEV_SIE_EP1_CNT1 for the details of bit fields.
USBFS0_USBDEV_SIE_EP7_CR0	0x403F01B8	Non-control endpoint's control Register. See USBFS0_USBDEV_SIE_EP1_CR0 for the details of bit fields.
USBFS0_USBDEV_SIE_EP8_CNT0	0x403F01F0	Non-control endpoint count register. See USBFS0_USBDEV_SIE_EP1_CNT0 for the details of bit fields.
USBFS0_USBDEV_SIE_EP8_CNT1	0x403F01F4	Non-control endpoint count register. See USBFS0_USBDEV_SIE_EP1_CNT1 for the details of bit fields.
USBFS0_USBDEV_SIE_EP8_CR0	0x403F01F8	Non-control endpoint's control Register. See USBFS0_USBDEV_SIE_EP1_CR0 for the details of bit fields.
USBFS0_USBDEV_ARB_EP1_CFG	0x403F0200	Endpoint Configuration Register *1
USBFS0_USBDEV_ARB_EP1_INT_EN	0x403F0204	Endpoint Interrupt Enable Register *1
USBFS0_USBDEV_ARB_EP1_SR	0x403F0208	Endpoint Interrupt Enable Register *1
USBFS0_USBDEV_ARB_RW1_WA	0x403F0210	Endpoint Write Address value *1, *2
USBFS0_USBDEV_ARB_RW1_WA_MSB	0x403F0214	Endpoint Write Address value *1, *2
USBFS0_USBDEV_ARB_RW1_RA	0x403F0218	Endpoint Read Address value *1, *2
USBFS0_USBDEV_ARB_RW1_RA_MSB	0x403F021C	Endpoint Read Address value *1, *2
USBFS0_USBDEV_ARB_RW1_DR	0x403F0220	Endpoint Data Register
USBFS0_USBDEV_BUF_SIZE	0x403F0230	Dedicated Endpoint Buffer Size Register *1
USBFS0_USBDEV_EP_ACTIVE	0x403F0238	Endpoint Active Indication Register *1
USBFS0_USBDEV_EP_TYPE	0x403F023C	Endpoint Type (IN/OUT) Indication *1

Register	Address	Description
USBFS0_USBDEV_ARB_EP2_CFG	0x403F0240	Endpoint Configuration Register *1. See USBFS0_USBDEV_ARB_EP1_CFG for the details of bit fields.
USBFS0_USBDEV_ARB_EP2_INT_EN	0x403F0244	Endpoint Interrupt Enable Register *1. See USBFS0_USBDEV_ARB_EP1_INT_EN for the details of bit fields.
USBFS0_USBDEV_ARB_EP2_SR	0x403F0248	Endpoint Interrupt Enable Register *1. See USBFS0_USBDEV_ARB_EP1_SR for the details of bit fields.
USBFS0_USBDEV_ARB_RW2_WA	0x403F0250	Endpoint Write Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_WA for the details of bit fields.
USBFS0_USBDEV_ARB_RW2_WA_MSB	0x403F0254	Endpoint Write Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_WA_MSB for the details of bit fields.
USBFS0_USBDEV_ARB_RW2_RA	0x403F0258	Endpoint Read Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_RA for the details of bit fields.
USBFS0_USBDEV_ARB_RW2_RA_MSB	0x403F025C	Endpoint Read Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_RA_MSB for the details of bit fields.
USBFS0_USBDEV_ARB_RW2_DR	0x403F0260	Endpoint Data Register. See USBFS0_USBDEV_ARB_RW1_DR for the details of bit fields.
USBFS0_USBDEV_ARB_CFG	0x403F0270	Arbiter Configuration Register *1
USBFS0_USBDEV_USB_CLK_EN	0x403F0274	USB Block Clock Enable Register
USBFS0_USBDEV_ARB_INT_EN	0x403F0278	Arbiter Interrupt Enable *1
USBFS0_USBDEV_ARB_INT_SR	0x403F027C	Arbiter Interrupt Status *1
USBFS0_USBDEV_ARB_EP3_CFG	0x403F0280	Endpoint Configuration Register *1. See USBFS0_USBDEV_ARB_EP1_CFG for the details of bit fields.
USBFS0_USBDEV_ARB_EP3_INT_EN	0x403F0284	Endpoint Interrupt Enable Register *1. See USBFS0_USBDEV_ARB_EP1_INT_EN for the details of bit fields.
USBFS0_USBDEV_ARB_EP3_SR	0x403F0288	Endpoint Interrupt Enable Register *1. See USBFS0_USBDEV_ARB_EP1_SR for the details of bit fields.
USBFS0_USBDEV_ARB_RW3_WA	0x403F0290	Endpoint Write Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_WA for the details of bit fields.
USBFS0_USBDEV_ARB_RW3_WA_MSB	0x403F0294	Endpoint Write Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_WA_MSB for the details of bit fields.
USBFS0_USBDEV_ARB_RW3_RA	0x403F0298	Endpoint Read Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_RA for the details of bit fields.
USBFS0_USBDEV_ARB_RW3_RA_MSB	0x403F029C	Endpoint Read Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_RA_MSB for the details of bit fields.
USBFS0_USBDEV_ARB_RW3_DR	0x403F02A0	Endpoint Data Register. See USBFS0_USBDEV_ARB_RW1_DR for the details of bit fields.
USBFS0_USBDEV_CWA	0x403F02B0	Common Area Write Address *1
USBFS0_USBDEV_CWA_MSB	0x403F02B4	Endpoint Read Address value *1
USBFS0_USBDEV_ARB_EP4_CFG	0x403F02C0	Endpoint Configuration Register *1. See USBFS0_USBDEV_ARB_EP1_CFG for the details of bit fields.
USBFS0_USBDEV_ARB_EP4_INT_EN	0x403F02C4	Endpoint Interrupt Enable Register *1. See USBFS0_USBDEV_ARB_EP1_INT_EN for the details of bit fields.
USBFS0_USBDEV_ARB_EP4_SR	0x403F02C8	Endpoint Interrupt Enable Register *1. See USBFS0_USBDEV_ARB_EP1_SR for the details of bit fields.
USBFS0_USBDEV_ARB_RW4_WA	0x403F02D0	Endpoint Write Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_WA for the details of bit fields.
USBFS0_USBDEV_ARB_RW4_WA_MSB	0x403F02D4	Endpoint Write Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_WA_MSB for the details of bit fields.
USBFS0_USBDEV_ARB_RW4_RA	0x403F02D8	Endpoint Read Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_RA for the details of bit fields.
USBFS0_USBDEV_ARB_RW4_RA_MSB	0x403F02DC	Endpoint Read Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_RA_MSB for the details of bit fields.
USBFS0_USBDEV_ARB_RW4_DR	0x403F02E0	Endpoint Data Register. See USBFS0_USBDEV_ARB_RW1_DR for the details of bit fields.
USBFS0_USBDEV_DMA_THRES	0x403F02F0	DMA Burst / Threshold Configuration
USBFS0_USBDEV_DMA_THRES_MSB	0x403F02F4	DMA Burst / Threshold Configuration

Register	Address	Description
USBFS0_USBDEV_ARB_EP5_CFG	0x403F0300	Endpoint Configuration Register *1. See USBFS0_USBDEV_ARB_EP1_CFG for the details of bit fields.
USBFS0_USBDEV_ARB_EP5_INT_EN	0x403F0304	Endpoint Interrupt Enable Register *1. See USBFS0_USBDEV_ARB_EP1_INT_EN for the details of bit fields.
USBFS0_USBDEV_ARB_EP5_SR	0x403F0308	Endpoint Interrupt Enable Register *1. See USBFS0_USBDEV_ARB_EP1_SR for the details of bit fields.
USBFS0_USBDEV_ARB_RW5_WA	0x403F0310	Endpoint Write Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_WA for the details of bit fields.
USBFS0_USBDEV_ARB_RW5_WA_MSB	0x403F0314	Endpoint Write Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_WA_MSB for the details of bit fields.
USBFS0_USBDEV_ARB_RW5_RA	0x403F0318	Endpoint Read Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_RA for the details of bit fields.
USBFS0_USBDEV_ARB_RW5_RA_MSB	0x403F031C	Endpoint Read Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_RA_MSB for the details of bit fields.
USBFS0_USBDEV_ARB_RW5_DR	0x403F0320	Endpoint Data Register. See USBFS0_USBDEV_ARB_RW1_DR for the details of bit fields.
USBFS0_USBDEV_BUS_RST_CNT	0x403F0330	Bus Reset Count Register
USBFS0_USBDEV_ARB_EP6_CFG	0x403F0340	Endpoint Configuration Register *1. See USBFS0_USBDEV_ARB_EP1_CFG for the details of bit fields.
USBFS0_USBDEV_ARB_EP6_INT_EN	0x403F0344	Endpoint Interrupt Enable Register *1. See USBFS0_USBDEV_ARB_EP1_INT_EN for the details of bit fields.
USBFS0_USBDEV_ARB_EP6_SR	0x403F0348	Endpoint Interrupt Enable Register *1. See USBFS0_USBDEV_ARB_EP1_SR for the details of bit fields.
USBFS0_USBDEV_ARB_RW6_WA	0x403F0350	Endpoint Write Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_WA for the details of bit fields.
USBFS0_USBDEV_ARB_RW6_WA_MSB	0x403F0354	Endpoint Write Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_WA_MSB for the details of bit fields.
USBFS0_USBDEV_ARB_RW6_RA	0x403F0358	Endpoint Read Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_RA for the details of bit fields.
USBFS0_USBDEV_ARB_RW6_RA_MSB	0x403F035C	Endpoint Read Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_RA_MSB for the details of bit fields.
USBFS0_USBDEV_ARB_RW6_DR	0x403F0360	Endpoint Data Register. See USBFS0_USBDEV_ARB_RW1_DR for the details of bit fields.
USBFS0_USBDEV_ARB_EP7_CFG	0x403F0380	Endpoint Configuration Register *1. See USBFS0_USBDEV_ARB_EP1_CFG for the details of bit fields.
USBFS0_USBDEV_ARB_EP7_INT_EN	0x403F0384	Endpoint Interrupt Enable Register *1. See USBFS0_USBDEV_ARB_EP1_INT_EN for the details of bit fields.
USBFS0_USBDEV_ARB_EP7_SR	0x403F0388	Endpoint Interrupt Enable Register *1. See USBFS0_USBDEV_ARB_EP1_SR for the details of bit fields.
USBFS0_USBDEV_ARB_RW7_WA	0x403F0390	Endpoint Write Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_WA for the details of bit fields.
USBFS0_USBDEV_ARB_RW7_WA_MSB	0x403F0394	Endpoint Write Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_WA_MSB for the details of bit fields.
USBFS0_USBDEV_ARB_RW7_RA	0x403F0398	Endpoint Read Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_RA for the details of bit fields.
USBFS0_USBDEV_ARB_RW7_RA_MSB	0x403F039C	Endpoint Read Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_RA_MSB for the details of bit fields.
USBFS0_USBDEV_ARB_RW7_DR	0x403F03A0	Endpoint Data Register. See USBFS0_USBDEV_ARB_RW1_DR for the details of bit fields.
USBFS0_USBDEV_ARB_EP8_CFG	0x403F03C0	Endpoint Configuration Register *1. See USBFS0_USBDEV_ARB_EP1_CFG for the details of bit fields.
USBFS0_USBDEV_ARB_EP8_INT_EN	0x403F03C4	Endpoint Interrupt Enable Register *1. See USBFS0_USBDEV_ARB_EP1_INT_EN for the details of bit fields.
USBFS0_USBDEV_ARB_EP8_SR	0x403F03C8	Endpoint Interrupt Enable Register *1. See USBFS0_USBDEV_ARB_EP1_SR for the details of bit fields.
USBFS0_USBDEV_ARB_RW8_WA	0x403F03D0	Endpoint Write Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_WA for the details of bit fields.

Register	Address	Description
USBFS0_USBDEV_ARB_RW8_WA_MSB	0x403F03D4	Endpoint Write Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_WA_MSB for the details of bit fields.
USBFS0_USBDEV_ARB_RW8_RA	0x403F03D8	Endpoint Read Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_RA for the details of bit fields.
USBFS0_USBDEV_ARB_RW8_RA_MSB	0x403F03DC	Endpoint Read Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_RA_MSB for the details of bit fields.
USBFS0_USBDEV_ARB_RW8_DR	0x403F03E0	Endpoint Data Register. See USBFS0_USBDEV_ARB_RW1_DR for the details of bit fields.
USBFS0_USBDEV_MEM_DATA0	0x403F0400	DATA. This is the starting address of a register bank containing 512 registers (USBFS0_USBDEV_MEM_DATA0 to USBFS0_USBDEV_MEM_DATA511).
USBFS0_USBDEV_SOF16	0x403F1060	Start Of Frame Register
USBFS0_USBDEV_ARB_RW1_WA16	0x403F1080	Oscillator lock data register
USBFS0_USBDEV_OSCLK_DR16	0x403F1210	Endpoint Write Address value *3
USBFS0_USBDEV_ARB_RW1_RA16	0x403F1218	Endpoint Read Address value *3
USBFS0_USBDEV_ARB_RW1_DR16	0x403F1220	Endpoint Data Register
USBFS0_USBDEV_ARB_RW2_WA16	0x403F1250	Endpoint Write Address value *3. See USBFS0_USBDEV_ARB_RW1_WA16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW2_RA16	0x403F1258	Endpoint Read Address value *3. See USBFS0_USBDEV_ARB_RW1_RA16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW2_DR16	0x403F1260	Endpoint Data Register. See USBFS0_USBDEV_ARB_RW1_DR16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW3_WA16	0x403F1290	Endpoint Write Address value *3. See USBFS0_USBDEV_ARB_RW1_WA16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW3_RA16	0x403F1298	Endpoint Read Address value *3. See USBFS0_USBDEV_ARB_RW1_RA16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW3_DR16	0x403F12A0	Endpoint Data Register. See USBFS0_USBDEV_ARB_RW1_DR16 for the details of bit fields.
USBFS0_USBDEV_CWA16	0x403F12B0	Common Area Write Address
USBFS0_USBDEV_ARB_RW4_WA16	0x403F12D0	Endpoint Write Address value *3. See USBFS0_USBDEV_ARB_RW1_WA16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW4_RA16	0x403F12D8	Endpoint Read Address value *3. See USBFS0_USBDEV_ARB_RW1_RA16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW4_DR16	0x403F12E0	Endpoint Data Register. See USBFS0_USBDEV_ARB_RW1_DR16 for the details of bit fields.
USBFS0_USBDEV_DMA_THRES16	0x403F12F0	DMA Burst / Threshold Configuration
USBFS0_USBDEV_ARB_RW5_WA16	0x403F1310	Endpoint Write Address value *3. See USBFS0_USBDEV_ARB_RW1_WA16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW5_RA16	0x403F1318	Endpoint Read Address value *3. See USBFS0_USBDEV_ARB_RW1_RA16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW5_DR16	0x403F1320	Endpoint Data Register. See USBFS0_USBDEV_ARB_RW1_DR16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW6_WA16	0x403F1350	Endpoint Write Address value *3. See USBFS0_USBDEV_ARB_RW1_WA16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW6_RA16	0x403F1358	Endpoint Read Address value *3. See USBFS0_USBDEV_ARB_RW1_RA16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW6_DR16	0x403F1360	Endpoint Data Register. See USBFS0_USBDEV_ARB_RW1_DR16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW7_WA16	0x403F1390	Endpoint Write Address value *3. See USBFS0_USBDEV_ARB_RW1_WA16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW7_RA16	0x403F1398	Endpoint Read Address value *3. See USBFS0_USBDEV_ARB_RW1_RA16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW7_DR16	0x403F13A0	Endpoint Data Register. See USBFS0_USBDEV_ARB_RW1_DR16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW8_WA16	0x403F13D0	Endpoint Write Address value *3. See USBFS0_USBDEV_ARB_RW1_WA16 for the details of bit fields.

Register	Address	Description
USBFS0_USBDEV_ARB_RW8_RA16	0x403F13D8	Endpoint Read Address value *3. See USBFS0_USBDEV_ARB_RW1_RA16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW8_DR16	0x403F13E0	Endpoint Data Register. See USBFS0_USBDEV_ARB_RW1_DR16 for the details of bit fields.
USBFS0_USBLPM_POWER_CTL	0x403F2000	Power Control Register
USBFS0_USBLPM_USBIO_CTL	0x403F2008	USB IO Control Register
USBFS0_USBLPM_FLOW_CTL	0x403F200C	Flow Control Register
USBFS0_USBLPM_LPM_CTL	0x403F2010	LPM Control Register
USBFS0_USBLPM_LPM_STAT	0x403F2014	LPM Status register
USBFS0_USBLPM_INTR_SIE	0x403F2020	USB SOF, BUS RESET and EP0 Interrupt Status
USBFS0_USBLPM_INTR_SIE_SET	0x403F2024	USB SOF, BUS RESET and EP0 Interrupt Set
USBFS0_USBLPM_INTR_SIE_MASK	0x403F2028	USB SOF, BUS RESET and EP0 Interrupt Mask
USBFS0_USBLPM_INTR_SIE_MASKED	0x403F202C	USB SOF, BUS RESET and EP0 Interrupt Masked
USBFS0_USBLPM_INTR_LVL_SEL	0x403F2030	Select interrupt level for each interrupt source
USBFS0_USBLPM_INTR_CAUSE_HI	0x403F2034	High priority interrupt Cause register
USBFS0_USBLPM_INTR_CAUSE_MED	0x403F2038	Medium priority interrupt Cause register
USBFS0_USBLPM_INTR_CAUSE_LO	0x403F203C	Low priority interrupt Cause register
USBFS0_USBLPM_DFT_CTL	0x403F2070	DFT control
USBFS0_USBHOST_HOST_CTL0	0x403F4000	Host Control 0 Register.
USBFS0_USBHOST_HOST_CTL1	0x403F4010	Host Control 1 Register.
USBFS0_USBHOST_HOST_CTL2	0x403F4100	Host Control 2 Register.
USBFS0_USBHOST_HOST_ERR	0x403F4104	Host Error Status Register.
USBFS0_USBHOST_HOST_STATUS	0x403F4108	Host Status Register.
USBFS0_USBHOST_HOST_FCOMP	0x403F410C	Host SOF Interrupt Frame Compare Register
USBFS0_USBHOST_HOST_RTIMER	0x403F4110	Host Retry Timer Setup Register
USBFS0_USBHOST_HOST_ADDR	0x403F4114	Host Address Register
USBFS0_USBHOST_HOST_EOF	0x403F4118	Host EOF Setup Register
USBFS0_USBHOST_HOST_FRAME	0x403F411C	Host Frame Setup Register
USBFS0_USBHOST_HOST_TOKEN	0x403F4120	Host Token Endpoint Register
USBFS0_USBHOST_HOST_EP1_CTL	0x403F4400	Host Endpoint 1 Control Register
USBFS0_USBHOST_HOST_EP1_STATUS	0x403F4404	Host Endpoint 1 Status Register
USBFS0_USBHOST_HOST_EP1_RW1_DR	0x403F4408	Host Endpoint 1 Data 1-Byte Register
USBFS0_USBHOST_HOST_EP1_RW2_DR	0x403F440C	Host Endpoint 1 Data 2-Byte Register
USBFS0_USBHOST_HOST_EP2_CTL	0x403F4500	Host Endpoint 2 Control Register
USBFS0_USBHOST_HOST_EP2_STATUS	0x403F4504	Host Endpoint 2 Status Register
USBFS0_USBHOST_HOST_EP2_RW1_DR	0x403F4508	Host Endpoint 2 Data 1-Byte Register
USBFS0_USBHOST_HOST_EP2_RW2_DR	0x403F450C	Host Endpoint 2 Data 2-Byte Register
USBFS0_USBHOST_HOST_LVL1_SEL	0x403F4800	Host Interrupt Level 1 Selection Register
USBFS0_USBHOST_HOST_LVL2_SEL	0x403F4804	Host Interrupt Level 2 Selection Register
USBFS0_USBHOST_INTR_USBHOST_CAUSE_HI	0x403F4900	Interrupt USB Host Cause High Register
USBFS0_USBHOST_INTR_USBHOST_CAUSE_MED	0x403F4904	Interrupt USB Host Cause Medium Register
USBFS0_USBHOST_INTR_USBHOST_CAUSE_LO	0x403F4908	Interrupt USB Host Cause Low Register
USBFS0_USBHOST_INTR_HOST_EP_CAUSE_HI	0x403F4920	Interrupt USB Host Endpoint Cause High Register
USBFS0_USBHOST_INTR_HOST_EP_CAUSE_MED	0x403F4924	Interrupt USB Host Endpoint Cause Medium Register
USBFS0_USBHOST_INTR_HOST_EP_CAUSE_LO	0x403F4928	Interrupt USB Host Endpoint Cause Low Register

Register	Address	Description
USBFS0_USBHOST_INTR_USBHOST	0x403F4940	Interrupt USB Host Register
USBFS0_USBHOST_INTR_USBHOST_SET	0x403F4944	Interrupt USB Host Set Register
USBFS0_USBHOST_INTR_USBHOST_MASK	0x403F4948	Interrupt USB Host Mask Register
USBFS0_USBHOST_INTR_USBHOST_MASKED	0x403F494C	Interrupt USB Host Masked Register
USBFS0_USBHOST_INTR_HOST_EP	0x403F4A00	Interrupt USB Host Endpoint Register
USBFS0_USBHOST_INTR_HOST_EP_SET	0x403F4A04	Interrupt USB Host Endpoint Set Register
USBFS0_USBHOST_INTR_HOST_EP_MASK	0x403F4A08	Interrupt USB Host Endpoint Mask Register
USBFS0_USBHOST_INTR_HOST_EP_MASKED	0x403F4A0C	Interrupt USB Host Endpoint Masked Register
USBFS0_USBHOST_HOST_DMA_ENBL	0x403F4B00	Host DMA Enable Register
USBFS0_USBHOST_HOST_EP1_BLK	0x403F4B20	Host Endpoint 1 Block Register
USBFS0_USBHOST_HOST_EP2_BLK	0x403F4B30	Host Endpoint 2 Block Register

20.1.1 USBFS0_USBDEV_EP0_DR0

Control End point EP0 Data Register

Address: 0x403F0000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_BYTE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA_BYTE	This register is shared for both transmit and receive. The count in the EP0_CNT register determines the number of bytes received or to be transferred. Default Value: 0

20.1.2 USBFS0_USBDEV_CR0

USB control 0 Register

Address: 0x403F0020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW						
HW Access	RW	RW						
Name	USB_ENABLE	DEVICE_ADDRESS [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	USB_ENABLE	This bit enables the device to respond to USB traffic. If USB bus reset is detected, this bit is cleared. Note: When USB PHY is GPIO mode(USBIO_CR1.IOMODE=0), USB bus reset is detected. Therefore, when USB PHY is GPIO mode, this bit is cleared even if this bit is set to 1. If this bit is set to 1, write this bit upon USB bus reset interrupt, and do not write to this bit during initialization steps. Default Value: 0
6 : 0	DEVICE_ADDRESS	These bits specify the USB device address to which the SIE will respond. This address must be set by firmware and is specified by the USB Host with a SET ADDRESS command during USB enumeration. This value must be programmed by firmware when assigned during enumeration. It is not set automatically by the hardware. If USB bus reset is detected, these bits are initialized. Default Value: 0

20.1.3 USBFS0_USBDEV_CR1

USB control 1 Register

Address: 0x403F0024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW0C	RW	RW
HW Access	None				R	RW1S	R	R
Name	None [7:4]				RE-SERVED_3	BUS_AC-TIVITY	EN-ABLE_LOC K	REG_EN-ABLE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	RESERVED_3	Reserved Default Value: 0
2	BUS_ACTIVITY	The Bus Activity bit is a stickybit that detects any non-idle USB event that has occurred on the USB bus. Once set to High by the SIE to indicate the bus activity this bit retains its logical High value until firmware clears it. Default Value: 0
1	ENABLE_LOCK	This bit is set to turn on the automatic frequency locking of the internal oscillator to USB traffic. Unless an external clock is being provided this bit should remain set for proper USB operation. Default Value: 0
0	REG_ENABLE	This bit controls the operation of the internal USB regulator. For applications with supply voltages in the 5V range this bit is set high to enable the internal regulator. For device supply voltage in the 3.3V range this bit is cleared to connect the transceiver directly to the supply. Default Value: 0

20.1.4 USBFS0_USBDEV_SIE_EP_INT_EN

USB SIE Data Endpoints Interrupt Enable Register

Address: 0x403F0028

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	EP8_IN-TR_EN	EP7_IN-TR_EN	EP6_IN-TR_EN	EP5_IN-TR_EN	EP4_IN-TR_EN	EP3_IN-TR_EN	EP2_IN-TR_EN	EP1_IN-TR_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	EP8_INTR_EN	Enables interrupt for EP8 Default Value: 0
6	EP7_INTR_EN	Enables interrupt for EP7 Default Value: 0
5	EP6_INTR_EN	Enables interrupt for EP6 Default Value: 0
4	EP5_INTR_EN	Enables interrupt for EP5 Default Value: 0
3	EP4_INTR_EN	Enables interrupt for EP4 Default Value: 0
2	EP3_INTR_EN	Enables interrupt for EP3 Default Value: 0
1	EP2_INTR_EN	Enables interrupt for EP2 Default Value: 0

20.1.4 USBFS0_USBDEV_SIE_EP_INT_EN (continued)

0	EP1_INTR_EN	Enables interrupt for EP1 Default Value: 0

20.1.5 USBFS0_USBDEV_SIE_EP_INT_SR

USB SIE Data Endpoint Interrupt Status

Address: 0x403F002C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	EP8_INTR	EP7_INTR	EP6_INTR	EP5_INTR	EP4_INTR	EP3_INTR	EP2_INTR	EP1_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	EP8_INTR	Interrupt status for EP8 Default Value: 0
6	EP7_INTR	Interrupt status for EP7 Default Value: 0
5	EP6_INTR	Interrupt status for EP6 Default Value: 0
4	EP5_INTR	Interrupt status for EP5 Default Value: 0
3	EP4_INTR	Interrupt status for EP4 Default Value: 0
2	EP3_INTR	Interrupt status for EP3 Default Value: 0
1	EP2_INTR	Interrupt status for EP2 Default Value: 0
0	EP1_INTR	Interrupt status for EP1 Default Value: 0

20.1.6 USBFS0_USBDEV_SIE_EP1_CNT0 (continued)

20.1.6 USBFS0_USBDEV_SIE_EP1_CNT0

Non-control endpoint count register

Address: 0x403F0030

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW0C	None			RW		
HW Access	RW	RW1S	None			RW		
Name	DATA_-TOGGLE	DATA_VAL-ID	None [5:3]			DATA_COUNT_MSB [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DATA_TOGGLE	This bit selects the DATA packet's toggle state. For IN transactions firmware must set this bit to the expected state. For OUT transactions the hardware sets this bit to the state of the received Data Toggle bit. Default Value: 0
6	DATA_VALID	This bit is used for OUT transactions only and is read only. It is cleared to '0' if CRC bit stuffing errors or PID errors occur. This bit does not update for some endpoint mode settings. Default Value: 0 **0x0: DATA_ERROR :** No ACK'd transactions since bit was last cleared. **0x1: DATA_VALID :** Indicates a transaction ended with an ACK.

2 : 0	DATA_COUNT_MSB	These bits are the 3 MSb bits of an 11-bit counter. The LSb are the Data Count[7:0] bits of the CNT1 register. Refer to the CNT1 register for more information. Default Value: 0

20.1.7 USBFS0_USBDEV_SIE_EP1_CNT1 (continued)

20.1.7 USBFS0_USBDEV_SIE_EP1_CNT1

Non-control endpoint count register

Address: 0x403F0034

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA_COUNT	These bits are the 8 LSb of a 11-bit counter. The 3 MSb bits are in the CNT0 register. The 11-bit count indicates the number of data bytes in a transaction. Default Value: 0

20.1.8 USBFS0_USBDEV_SIE_EP1_CR0 (continued)

20.1.8 USBFS0_USBDEV_SIE_EP1_CR0

Non-control endpoint's control Register

Address: 0x403F0038

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RWC	RW	RWC	RW			
HW Access	R	RW1S	R	RW1S	RW			
Name	STALL	ER-R_IN_TXN	NA-K_INT_EN	ACKED_TXN	MODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	STALL	When this bit is set the SIE stalls an OUT packet if the Mode bits are set to ACK-OUT. The SIE stalls an IN packet if the mode bits are set to ACK-IN. This bit must be clear for all other modes. Default Value: 0
6	ERR_IN_TXN	The Error in transaction bit is set whenever an error is detected. For an IN transaction, this indicates a no response from HOST scenario. For an OUT transaction, this represents an RxErr (PID error/ CRC error/ bit-stuff error scenario). This bit is cleared by any writes to the register. Default Value: 0
5	NAK_INT_EN	When set this bit causes an endpoint interrupt to be generated even when a transfer completes with a NAK. Default Value: 0
4	ACKED_TXN	The ACK'd transaction bit is set whenever the SIE engages in a transaction to the register's endpoint that completes with an ACK packet. This bit is cleared by any writes to the register. Default Value: 0

20.1.8 USBFS0_USBDEV_SIE_EP1_CR0 (continued)

0x0: ACKED_NO :

No ACK'd transactions since bit was last cleared.

0x1: ACKED_YES :

Indicates a transaction ended with an ACK.

3 : 0	MODE	The mode controls how the USB SIE responds to traffic and how the USB SIE changes the mode of that endpoint as a result of host packets to the endpoint. Default Value: 0

0x0: DISABLE :

Ignore all USB traffic to this endpoint

0x1: NAK_INOUT :

SETUP: Accept
IN: NAK
OUT: NAK

0x2: STATUS_OUT_ONLY :

SETUP: Accept
IN: STALL
OUT: ACK 0B tokens, NAK others

0x3: STALL_INOUT :

SETUP: Accept
IN: STALL
OUT: STALL

0x5: ISO_OUT :

SETUP: Ignore
IN: Ignore
OUT: Accept Isochronous OUT token

0x6: STATUS_IN_ONLY :

SETUP: Accept
IN: Respond with 0B data
OUT: Stall

0x7: ISO_IN :

SETUP: Ignore
IN: Accept Isochronous IN token
OUT: Ignore

20.1.8 USBFS0_USBDEV_SIE_EP1_CR0 (continued)

0x8: NAK_OUT :

SETUP: Ignore
IN: Ignore
OUT: NAK

0x9: ACK_OUT :

SETUP: Ignore
IN: Ignore
OUT: Accept data and ACK if STALL=0, STALL otherwise.
Change to MODE=8 after one succesfull OUT token.

0xb: ACK_OUT_STATUS_IN :

SETUP: Accept
IN: Respond with 0B data
OUT: Accept data

0xc: NAK_IN :

SETUP: Ignore
IN: NAK
OUT: Ignore

0xd: ACK_IN :

SETUP: Ignore
IN: Respond to IN with data if STALL=0, STALL otherwise
OUT: Ignore

0xf: ACK_IN_STATUS_OUT :

SETUP: Accept
IN: Respond to IN with data
OUT: ACK 0B tokens, NAK others

20.1.9 USBFS0_USBDEV_USBIO_CR0 (continued)

20.1.9 USBFS0_USBDEV_USBIO_CR0

USBIO Control 0 Register

Address: 0x403F0040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	None				R
HW Access	R	R	R	None				W
Name	TEN	TSE0	TD	None [4:1]				RD

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	TEN	USB Transmit Enable. This is used to manually transmit on the D+ and D- pins. Normally this bit should be cleared to allow the internal SIE to drive the pins. The most common reason for manually transmitting is to force a resume state on the bus. Default Value: 0
6	TSE0	Transmit Single-Ended Zero. SE0: both D+ and D- low. No effect if TEN=0. Default Value: 0
5	TD	Transmit Data. Transmit a USB J or K state on the USB bus. No effect if TEN=0 or TSE0=1. Default Value: 0 **0x0: DIFF_K :** Force USB K state (D+ is low D- is high).

		0x1: DIFF_J : Force USB J state (D+ is high D- is low).
0	RD	Received Data. This read only bit gives the state of the USB differential receiver when IOMODE bit is '0' and USB doesn't transmit. This bit is valid if USB Device. If D+=D- (SE0), this value is undefined. Default Value: X **0x0: DIFF_LOW :** D+ < D- (K state) **0x1: DIFF_HIGH :** D+ > D- (J state)

20.1.10 USBFS0_USBDEV_USBIO_CR2 (continued)

20.1.10 USBFS0_USBDEV_USBIO_CR2

USBIO control 2 Register

Address: 0x403F0044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	R					
HW Access	R	R	R					
Name	RE-SERVED_7	TEST_PKT	RESERVED_5_0 [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	RESERVED_7	Reserved Default Value: 0
6	TEST_PKT	This bit enables the device to transmit a packet in response to an internally generated IN packet. When set, one packet will be generated. Default Value: 0
5 : 0	RESERVED_5_0	Reserved Default Value: 0

20.1.11 USBFS0_USBDEV_USBIO_CR1

USBIO control 1 Register

Address: 0x403F0048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	None		RW	R	R
HW Access	None		R	None		W	W	W
Name	None [7:6]		IOMODE	None [4:3]		RE-SERVED_2	DPO	DMO

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	IOMODE	This bit allows the D+ and D- pins to be configured for either USB mode or bit-banged modes. If this bit is set the DMI and DPI bits are used to drive the D- and D+ pins. Default Value: 1
2	RESERVED_2	Reserved Default Value: X
1	DPO	This read only bit gives the state of the D+ pin when IOMODE bit is '0' and USB doesn't transmit. This bit displays the output value of D+ pin when USB transmits SE0 or data. This bit is valid if USB Device. Default Value: X
0	DMO	This read only bit gives the state of the D- pin when IOMODE bit is '0' and USB doesn't transmit. This bit is '0' when USB transmits SE0, and this bit is '1' when USB transmits other than SE0. This bit is valid if USB Device. Default Value: X

20.1.12 USBFS0_USBDEV_DYN_RECONFIG

USB Dynamic reconfiguration register

Address: 0x403F0050

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	RW			RW
HW Access	None			W	R			R
Name	None [7:5]			DYN_RECONFIG_RDY_STS	DYN_RECONFIG_EPNO [3:1]			DYN_CONFIG_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	DYN_RECONFIG_RDY_STS	This bit indicates the ready status for the dynamic reconfiguration, when set to 1, indicates the block is ready for reconfiguration. Default Value: 0
3 : 1	DYN_RECONFIG_EPNO	These bits indicates the EP number for which reconfiguration is required when dyn_config_en bit is set to 1. Default Value: 0
0	DYN_CONFIG_EN	This bit is used to enable the dynamic re-configuration for the selected EP. If set to 1, indicates the reconfiguration required for selected EP. Use 0 for EP1, 1 for EP2, etc. Default Value: 0

20.1.13 USBFS0_USBDEV_SOF0

Start Of Frame Register

Address: 0x403F0060

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	FRAME_NUMBER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	FRAME_NUMBER	It has the lower 8 bits [7:0] of the SOF frame number. Default Value: 0

20.1.14 USBFS0_USBDEV_SOF1

Start Of Frame Register

Address: 0x403F0064

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R		
HW Access	None					RW		
Name	None [7:3]					FRAME_NUMBER_MSB [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	FRAME_NUMBER_MSB	It has the upper 3 bits [10:8] of the SOF frame number. Default Value: 0

20.1.15 USBFS0_USBDEV_OSCLK_DR0

Oscillator lock data register 0

Address: 0x403F0080

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADDER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	ADDER	These bits return the lower 8 bits of the oscillator locking circuits adder output. Default Value: X

20.1.16 USBFS0_USBDEV_OSCLK_DR1

Oscillator lock data register 1

Address: 0x403F0084

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R						
HW Access	None	W						
Name	None	ADDER_MSB [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 0	ADDER_MSB	These bits return the upper 7 bits of the oscillator locking circuits adder output. Default Value: X

20.1.17 USBFS0_USBDEV_EP0_CR (continued)

20.1.17 USBFS0_USBDEV_EP0_CR

Endpoint0 control Register

Address: 0x403F00A0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RWC	RWC	RWC	RWC	RW			
HW Access	RW1S	RW1S	RW1S	RW1S	RW			
Name	SET-UP_RCVD	IN_RCVD	OUT_RCVD	ACKED_TXN	MODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	SETUP_RCVD	When set this bit indicates a valid SETUP packet was received and ACKed. This bit is forced HIGH from the start of the data packet phase of the SETUP transaction until the start of the ACK packet returned by the SIE. The CPU is prevented from clearing this bit during this interval. After this interval the bit will remain set until cleared by firmware. While this bit is set to '1' the CPU cannot write to the EP0_DRx registers. This prevents firmware from overwriting an incoming SETUP transaction before firmware has a chance to read the SETUP data. This bit is cleared by any non-locked writes to the register. Default Value: 0
6	IN_RCVD	When set this bit indicates a valid IN packet has been received. This bit is updated to '1' after the host acknowledges an IN data packet. When clear this bit indicates either no IN has been received or that the host did not acknowledge the IN data by sending ACK handshake. It is cleared by any writes to the register. Default Value: 0

20.1.17 USBFS0_USBDEV_EP0_CR (continued)

5	OUT_RCVD	When set this bit indicates a valid OUT packet has been received and ACKed. This bit is updated to '1' after the last received packet in an OUT transaction. When clear this bit indicates no OUT received. It is cleared by any writes to the register. Default Value: 0
4	ACKED_TXN	The ACK'd transaction bit is set whenever the SIE engages in a transaction to the register's end-point that completes with an ACK packet. This bit is cleared by any writes to the register. Default Value: 0 **0x0: ACKED_NO :** No ACK'd transactions since bit was last cleared. **0x1: ACKED_YES :** Indicates a transaction ended with an ACK.
3 : 0	MODE	The mode controls how the USB SIE responds to traffic and how the USB SIE changes the mode of that endpoint as a result of host packets to the endpoint. Default Value: 0 **0x0: DISABLE :** Ignore all USB traffic to this endpoint **0x1: NAK_INOUT :** SETUP: Accept IN: NAK OUT: NAK **0x2: STATUS_OUT_ONLY :** SETUP: Accept IN: STALL OUT: ACK 0B tokens, NAK others **0x3: STALL_INOUT :** SETUP: Accept IN: STALL OUT: STALL **0x5: ISO_OUT :** SETUP: Ignore IN: Ignore OUT: Accept Isochronous OUT token **0x6: STATUS_IN_ONLY :** SETUP: Accept IN: Respond with 0B data OUT: Stall

20.1.17 USBFS0_USBDEV_EP0_CR (continued)

0x7: ISO_IN :

SETUP: Ignore
IN: Accept Isochronous IN token
OUT: Ignore

0x8: NAK_OUT :

SETUP: Ignore
IN: Ignore
OUT: NAK

0x9: ACK_OUT :

SETUP: Ignore
IN: Ignore
OUT: Accept data and ACK if STALL=0, STALL otherwise.
Change to MODE=8 after one succesfull OUT token.

0xb: ACK_OUT_STATUS_IN :

SETUP: Accept
IN: Respond with 0B data
OUT: Accept data

0xc: NAK_IN :

SETUP: Ignore
IN: NAK
OUT: Ignore

0xd: ACK_IN :

SETUP: Ignore
IN: Respond to IN with data if STALL=0, STALL otherwise
OUT: Ignore

0xf: ACK_IN_STATUS_OUT :

SETUP: Accept
IN: Respond to IN with data
OUT: ACK 0B tokens, NAK others

20.1.18 USBFS0_USBDEV_EP0_CNT (continued)

20.1.18 USBFS0_USBDEV_EP0_CNT

Endpoint0 count Register

Address: 0x403F00A4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW0C	None		RW			
HW Access	RW	RW1S	None		RW			
Name	DATA_-TOGGLE	DATA_VAL-ID	None [5:4]		BYTE_COUNT [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DATA_TOGGLE	This bit selects the DATA packet's toggle state. For IN transactions firmware must set this bit to the expected state. For OUT transactions the hardware sets this bit to the state of the received Data Toggle bit. Default Value: 0
6	DATA_VALID	This bit is used for OUT/SETUP transactions only and is read only. It is cleared to '0' if CRC bit stuffing errors or PID errors occur. This bit does not update for some endpoint mode settings. Default Value: 0 **0x0: DATA_ERROR :** No ACK'd transactions since bit was last cleared. **0x1: DATA_VALID :** Indicates a transaction ended with an ACK.

20.1.18 USBFS0_USBDEV_EP0_CNT (continued)

3 : 0	BYTE_COUNT	These bits indicate the number of data bytes in a transaction. For IN transactions firmware loads the count with the number of bytes to be transmitted to the host from the endpoint FIFO. Valid values are 0 to 8. For OUT or SETUP transactions the count is updated by hardware to the number of data bytes received plus two for the CRC bytes. Valid values are 2 to 10. Default Value: 0

20.1.19 USBFS0_USBDEV_ARB_EP1_CFG (continued)

20.1.19 USBFS0_USBDEV_ARB_EP1_CFG

Endpoint Configuration Register *1

Address: 0x403F0200

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				RE-SET_PTR	CRC_BY-PASS	DMA_REQ	IN_-DATA_RDY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	RESET_PTR	Configuration Setting to Reset the RA and WA Pointers to their start values at the End of Packet transaction. Default Value: 0 **0x0: RESET_KRYPTON :** Do not Reset Pointer; Krypton Backward compatibility mode **0x1: RESET_NORMAL :** Reset Pointer; recommended value for reduction of CPU Configuration Writes.
2	CRC_BYPASS	Configuration Setting to prevent CRC bytes from being written to memory and being read by firmware Default Value: 0

		0x0: CRC_NORMAL : No CRC bypass; CRC bytes will be written to memory and Termin will be generated for the CRC byte/s **0x1: CRC_BYPASS :** CRC Bypass Set; CRC bytes will not be written into memory and Termin will be generated for the last data byte/s
1	DMA_REQ	Manual DMA Request for a particular (1 to 8) endpoint; changing this field from 0 to 1 causes a DMA request to be generated. Default Value: 0
0	IN_DATA_RDY	Indication that Endpoint Packet Data is Ready in Main memory Default Value: 0

20.1.20 USBFS0_USBDEV_ARB_EP1_INT_EN (continued)

20.1.20 USBFS0_USBDEV_ARB_EP1_INT_EN

Endpoint Interrupt Enable Register *1

Address: 0x403F0204

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		DMA_TER-MIN_EN	ER-R_INT_EN	BUF_UNDER_EN	BUF_OVER_EN	DMA_GN-T_EN	IN_BUF_-FULL_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	DMA_TERMIN_EN	Endpoint DMA Terminated Enable Default Value: 0
4	ERR_INT_EN	Endpoint Error in Transaction Interrupt Enable Default Value: 0
3	BUF_UNDER_EN	Endpoint Buffer Underflow Enable Default Value: 0
2	BUF_OVER_EN	Endpoint Buffer Overflow Enable Default Value: 0
1	DMA_GNT_EN	Endpoint DMA Grant Enable Default Value: 0
0	IN_BUF_FULL_EN	IN Endpoint Local Buffer Full Enable Default Value: 0

20.1.21 USBFS0_USBDEV_ARB_EP1_SR

Endpoint Interrupt Enable Register *1

Address: 0x403F0208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1C	None	RW1C	RW1C	RW1C	RW1C
HW Access	None		RW1S	None	RW1S	RW1S	RW1S	RW1S
Name	None [7:6]		DMA_TER-MIN	None	BUF_UNDER	BUF_OVER	DMA_GNT	IN_BUF_-FULL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	DMA_TERMIN	Endpoint DMA Terminated Interrupt Default Value: 0
3	BUF_UNDER	Endpoint Buffer Underflow Interrupt Default Value: 0
2	BUF_OVER	Endpoint Buffer Overflow Interrupt Default Value: 0
1	DMA_GNT	Endpoint DMA Grant Interrupt Default Value: 0
0	IN_BUF_FULL	IN Endpoint Local Buffer Full Interrupt Default Value: 0

20.1.22 USBFS0_USBDEV_ARB_RW1_WA

Endpoint Write Address value *1, *2

Address: 0x403F0210

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	WA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	WA	Write Address for EP Default Value: 0

20.1.23 USBFS0_USBDEV_ARB_RW1_WA_MSB

Endpoint Write Address value *1, *2

Address: 0x403F0214

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							RW
Name	None [7:1]							WA_MSB

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	WA_MSB	Write Address for EP Default Value: 0

20.1.24 USBFS0_USBDEV_ARB_RW1_RA

Endpoint Read Address value *1, *2

Address: 0x403F0218

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	RA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	RA	Read Address for EP Default Value: 0

20.1.25 USBFS0_USBDEV_ARB_RW1_RA_MSB

Endpoint Read Address value *1, *2

Address: 0x403F021C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							RW
Name	None [7:1]							RA_MSB

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	RA_MSB	Read Address for EP Default Value: 0

20.1.26 USBFS0_USBDEV_ARB_RW1_DR

Endpoint Data Register

Address: 0x403F0220

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DR	Data Register for EP ; This register is linked to the memory, hence reset value is undefined Default Value: X

20.1.27 USBFS0_USBDEV_BUF_SIZE

Dedicated Endpoint Buffer Size Register *1

Address: 0x403F0230

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	OUT_BUF [7:4]				IN_BUF [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	OUT_BUF	Buffer size for OUT Endpoints. Default Value: 0
3 : 0	IN_BUF	Buffer size for IN Endpoints. Default Value: 0

20.1.28 USBFS0_USBDEV_EP_ACTIVE (continued)

20.1.28 USBFS0_USBDEV_EP_ACTIVE

Endpoint Active Indication Register *1

Address: 0x403F0238

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	EP8_ACT	EP7_ACT	EP6_ACT	EP5_ACT	EP4_ACT	EP3_ACT	EP2_ACT	EP1_ACT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	EP8_ACT	Indicates that Endpoint is currently active. Default Value: 0
6	EP7_ACT	Indicates that Endpoint is currently active. Default Value: 0
5	EP6_ACT	Indicates that Endpoint is currently active. Default Value: 0
4	EP5_ACT	Indicates that Endpoint is currently active. Default Value: 0
3	EP4_ACT	Indicates that Endpoint is currently active. Default Value: 0
2	EP3_ACT	Indicates that Endpoint is currently active. Default Value: 0
1	EP2_ACT	Indicates that Endpoint is currently active. Default Value: 0

20.1.28 USBFS0_USBDEV_EP_ACTIVE (continued)

0	EP1_ACT	Indicates that Endpoint is currently active. Default Value: 0

20.1.29 USBFS0_USBDEV_EP_TYPE (continued)

20.1.29 USBFS0_USBDEV_EP_TYPE

Endpoint Type (IN/OUT) Indication *1

Address: 0x403F023C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	EP8_TYP	EP7_TYP	EP6_TYP	EP5_TYP	EP4_TYP	EP3_TYP	EP2_TYP	EP1_TYP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	EP8_TYP	Endpoint Type Indication. Default Value: 0 **0x0: EP_IN :** IN outpoint **0x1: EP_OUT :** OUT outpoint
6	EP7_TYP	Endpoint Type Indication. Default Value: 0 **0x0: EP_IN :** IN outpoint

		0x1: EP_OUT : OUT outpoint
5	EP6_TYP	Endpoint Type Indication. Default Value: 0 **0x0: EP_IN :** IN outpoint **0x1: EP_OUT :** OUT outpoint
4	EP5_TYP	Endpoint Type Indication. Default Value: 0 **0x0: EP_IN :** IN outpoint **0x1: EP_OUT :** OUT outpoint
3	EP4_TYP	Endpoint Type Indication. Default Value: 0 **0x0: EP_IN :** IN outpoint **0x1: EP_OUT :** OUT outpoint
2	EP3_TYP	Endpoint Type Indication. Default Value: 0 **0x0: EP_IN :** IN outpoint **0x1: EP_OUT :** OUT outpoint
1	EP2_TYP	Endpoint Type Indication. Default Value: 0 **0x0: EP_IN :** IN outpoint

20.1.29 USBFS0_USBDEV_EP_TYPE (continued)

		0x1: EP_OUT : OUT outpoint
0	EP1_TYP	Endpoint Type Indication. Default Value: 0 **0x0: EP_IN :** IN outpoint **0x1: EP_OUT :** OUT outpoint

20.1.30 USBFS0_USBDEV_ARB_CFG (continued)

20.1.30 USBFS0_USBDEV_ARB_CFG

Arbiter Configuration Register *1

Address: 0x403F0270

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW		RW	None			
HW Access	R	R		R	None			
Name	CFG_CMP	DMA_CFG [6:5]		AU-TO_MEM	None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	CFG_CMP	Register Configuration Complete Indication. Posedge is detected on this bit. Hence a 0 to 1 transition is required. Default Value: 0
6 : 5	DMA_CFG	DMA Access Configuration. Default Value: 0 **0x0: DMA_NONE :** No DMA **0x1: DMA_MANUAL :** Manual DMA

		0x2: DMA_AUTO : Auto DMA
4	AUTO_MEM	Enables Auto Memory Configuration. Manual memory configuration by default. Default Value: 0

20.1.31 USBFS0_USBDEV_USB_CLK_EN (continued)

20.1.31 USBFS0_USBDEV_USB_CLK_EN

USB Block Clock Enable Register

Address: 0x403F0274

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							CSR_-CLK_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CSR_CLK_EN	Clock Enable for Core Logic clocked by AHB bus clock Default Value: 0

20.1.32 USBFS0_USBDEV_ARB_INT_EN

Arbiter Interrupt Enable *1

Address: 0x403F0278

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	EP8_IN-TR_EN	EP7_IN-TR_EN	EP6_IN-TR_EN	EP5_IN-TR_EN	EP4_IN-TR_EN	EP3_IN-TR_EN	EP2_IN-TR_EN	EP1_IN-TR_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	EP8_INTR_EN	Enables interrupt for EP8 Default Value: 0
6	EP7_INTR_EN	Enables interrupt for EP7 Default Value: 0
5	EP6_INTR_EN	Enables interrupt for EP6 Default Value: 0
4	EP5_INTR_EN	Enables interrupt for EP5 Default Value: 0
3	EP4_INTR_EN	Enables interrupt for EP4 Default Value: 0
2	EP3_INTR_EN	Enables interrupt for EP3 Default Value: 0
1	EP2_INTR_EN	Enables interrupt for EP2 Default Value: 0

0	EP1_INTR_EN	Enables interrupt for EP1 Default Value: 0

20.1.33 USBFS0_USBDEV_ARB_INT_SR (continued)

20.1.33 USBFS0_USBDEV_ARB_INT_SR

Arbiter Interrupt Status *1

Address: 0x403F027C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	EP8_INTR	EP7_INTR	EP6_INTR	EP5_INTR	EP4_INTR	EP3_INTR	EP2_INTR	EP1_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	EP8_INTR	Interrupt status for EP8 Default Value: 0
6	EP7_INTR	Interrupt status for EP7 Default Value: 0
5	EP6_INTR	Interrupt status for EP6 Default Value: 0
4	EP5_INTR	Interrupt status for EP5 Default Value: 0
3	EP4_INTR	Interrupt status for EP4 Default Value: 0
2	EP3_INTR	Interrupt status for EP3 Default Value: 0
1	EP2_INTR	Interrupt status for EP2 Default Value: 0

0	EP1_INTR	Interrupt status for EP1 Default Value: 0

20.1.34 USBFS0_USBDEV_CWA (continued)

20.1.34 USBFS0_USBDEV_CWA

Common Area Write Address *1

Address: 0x403F02B0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CWA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CWA	Write Address for Common Area Default Value: 0

20.1.35 USBFS0_USBDEV_CWA_MSB

Endpoint Read Address value *1

Address: 0x403F02B4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							RW
Name	None [7:1]							CWA_MSB

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CWA_MSB	Write Address for Common Area Default Value: 0

20.1.36 USBFS0_USBDEV_DMA_THRES

DMA Burst / Threshold Configuration

Address: 0x403F02F0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DMA_THS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DMA_THS	DMA Threshold count Default Value: 0

20.1.37 USBFS0_USBDEV_DMA_THRES_MSB

DMA Burst / Threshold Configuration

Address: 0x403F02F4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							RW
Name	None [7:1]							DMA_THS_MSB

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	DMA_THS_MSB	DMA Threshold count Default Value: 0

20.1.38 USBFS0_USBDEV_BUS_RST_CNT

Bus Reset Count Register

Address: 0x403F0330

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				bus_rst_cnt [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	bus_rst_cnt	Bus Reset Count Length Default Value: 10

20.1.39 USBFS0_USBDEV_MEM_DATA0

DATA

Address: 0x403F0400

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DR	Data Register for EP ; This register is linked to the memory, hence reset value is undefined Default Value: X

20.1.40 USBFS0_USBDEV_SOF16

Start Of Frame Register

Address: 0x403F1060

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	FRAME_NUMBER16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None					R		
HW Access	None					RW		
Name	None [15:11]					FRAME_NUMBER16 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10 : 0	FRAME_NUMBER16	The frame number (11b) Default Value: 0

20.1.41 USBFS0_USBDEV_OSCLK_DR16

Oscillator lock data register

Address: 0x403F1080

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADDER16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None	R						
HW Access	None	W						
Name	None	ADDER16 [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14 : 0	ADDER16	These bits return the oscillator locking circuits adder output. Default Value: X

20.1.42 USBFS0_USBDEV_ARB_RW1_WA16 (continued)

20.1.42 USBFS0_USBDEV_ARB_RW1_WA16

Endpoint Write Address value *3

Address: 0x403F1210

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	WA16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							RW
Name	None [15:9]							WA16

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8 : 0	WA16	Write Address for EP Default Value: 0

20.1.43 USBFS0_USBDEV_ARB_RW1_RA16

Endpoint Read Address value *3

Address: 0x403F1218

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	RA16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							RW
Name	None [15:9]							RA16

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8 : 0	RA16	Read Address for EP Default Value: 0

20.1.44 USBFS0_USBDEV_ARB_RW1_DR16

Endpoint Data Register

Address: 0x403F1220

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DR16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DR16 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DR16	Data Register for EP ; This register is linked to the memory, hence reset value is undefined Default Value: X

20.1.45 USBFS0_USBDEV_CWA16 (continued)

20.1.45 USBFS0_USBDEV_CWA16

Common Area Write Address

Address: 0x403F12B0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CWA16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							RW
Name	None [15:9]							CWA16

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8 : 0	CWA16	Write Address for Common Area Default Value: 0

20.1.46 USBFS0_USBDEV_DMA_THRES16

DMA Burst / Threshold Configuration

Address: 0x403F12F0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DMA_THS16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							RW
Name	None [15:9]							DMA_THS16

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8 : 0	DMA_THS16	DMA Threshold count Default Value: 0

20.1.47 USBFS0_USBLPM_POWER_CTL (continued)

20.1.47 USBFS0_USBLPM_POWER_CTL

Power Control Register

Address: 0x403F2000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	None	
HW Access	None					R	None	
Name	None [7:3]					SUSPEND	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [23:22]		DM_DOWN_EN	DM_BIG	DM_UP_EN	DP_DOWN_EN	DP_BIG	DP_UP_EN

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW	RW	None			
HW Access	None		R	R	None			
Name	None [31:30]		EN-ABLE_DMO	EN-ABLE_DPO	None [27:24]			

Bits	Name	Description
29	ENABLE_DMO	Enables the signle ended receiver on D-. Default Value: 0
28	ENABLE_DPO	Enables the single ended receiver on D+. Default Value: 0
21	DM_DOWN_EN	Enables the ~15k pull down on the DP. Default Value: 0
20	DM_BIG	Select the resister value if POWER_CTL.DM_EN='1'. This bit is valid in GPIO. '0' : The resister value is from 900 to1575Ohmpull up on the DM. '1' : The resister value is from 1425 to 3090Ohmpull up on the DM Default Value: 0

19	DM_UP_EN	Enables the pull up on the DM. The bit is valid in GPIO. The pull up resistor is disabled in not GPIO. '0' : Disable. '1' : Enable. Default Value: 0
18	DP_DOWN_EN	Enables the ~15k pull down on the DP. Default Value: 0
17	DP_BIG	Select the resister value if POWER_CTL.DP_EN='1'. This bit is valid in GPIO. '0' : The resister value is from 900 to1575Ohmpull up on the DP. '1' : The resister value is from 1425 to 3090Ohmpull up on the DP Default Value: 0
16	DP_UP_EN	Enables the pull up on the DP. '0' : Disable. '1' : Enable. Default Value: 0
2	SUSPEND	Put PHY into Suspend mode. If the PHY is enabled, this bit MUST be set before entering a low power mode (DeepSleep). Note: - This bit is invalid if the HOST bit of the Host Control 0 Register (HOST_CTL0) is '1'. Default Value: 0

20.1.48 USBFS0_USBLPM_USBIO_CTL (continued)

20.1.48 USBFS0_USBLPM_USBIO_CTL

USB IO Control Register

Address: 0x403F2008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW			RW		
HW Access	None		R			R		
Name	None [7:6]		DM_M [5:3]			DM_P [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 3	DM_M	The GPIO Drive Mode for DM IO pad. Default Value: 0
2 : 0	DM_P	The GPIO Drive Mode for DP IO pad. This field only applies if USBIO_CR1.IOMODE =1. Data comes from the corresponding GPIO.DR register. Default Value: 0 **0x0: OFF :** Mode 0: Output buffer off (high Z). Input buffer off. **0x1: INPUT :** Mode 1: Output buffer off (high Z). Input buffer on. Other values, not supported.

20.1.49 USBFS0_USBLPM_FLOW_CTL

Flow Control Register

Address: 0x403F200C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	EP8_ER-R_RESP	EP7_ER-R_RESP	EP6_ER-R_RESP	EP5_ER-R_RESP	EP4_ER-R_RESP	EP3_ER-R_RESP	EP2_ER-R_RESP	EP1_ER-R_RESP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	EP8_ERR_RESP	End Point 8 error response Default Value: 0
6	EP7_ERR_RESP	End Point 7 error response Default Value: 0
5	EP6_ERR_RESP	End Point 6 error response Default Value: 0
4	EP5_ERR_RESP	End Point 5 error response Default Value: 0
3	EP4_ERR_RESP	End Point 4 error response Default Value: 0
2	EP3_ERR_RESP	End Point 3 error response Default Value: 0
1	EP2_ERR_RESP	End Point 2 error response Default Value: 0

0	EP1_ERR_RESP	End Point 1 error response 0: do nothing (backward compatibility mode) 1: if this is an IN EP and an underflow occurs then cause a CRC error, if this is an OUT EP and an overflow occurs then send a NAK Default Value: 0

20.1.50 USBFS0_USBLPM_LPM_CTL (continued)

20.1.50 USBFS0_USBLPM_LPM_CTL

LPM Control Register

Address: 0x403F2010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	RW
HW Access	None			R	None	R	R	R
Name	None [7:5]			SUB_RESP	None	NYET_EN	LPM_ACK_RESP	LPM_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	SUB_RESP	Enable a STALL response for all undefined SubPIDs, i.e. other than LPM (0011b). If not enabled then there will be no response (Error) for the undefined SubPIDs. Default Value: 0
2	NYET_EN	Allow firmware to choose which response to use for an LPM token (LPM_EN=1) when the device is NOT ready to go to the requested low power mode (LPM_ACK_RESP=0). 0: a LPM token will get an NAK response (indicating a CRC error), the host is expected to repeat the LPM token. 1: a LPM token will get a NYET response Default Value: 0
1	LPM_ACK_RESP	LPM ACK response enable (if LPM_EN=1), to allow firmware to refuse a low power request 0: a LPM token will get a NYET or NAK (depending on NYET_EN bit below) response and the device will NOT go to a low power mode 1: a LPM token will get an ACK response and the device will go to the requested low power mode Default Value: 0

0	LPM_EN	LPM enable 0: Disabled, LPM token will not get a response (backward compatibility mode) 1: Enable, LPM token will get a handshake response (ACK, STALL, NYET or NAK) A STALL will be sent if the bLinkState is not 0001b A NYET, NAK or ACK response will be sent depending on the NYET_EN and LPM_ACK_RESP bits below Default Value: 0

20.1.51 USBFS0_USBLPM_LPM_STAT (continued)

20.1.51 USBFS0_USBLPM_LPM_STAT

LPM Status register

Address: 0x403F2014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	R			
HW Access	None			RW	RW			
Name	None [7:5]			LPM_REMOTEWAKE	LPM_BESL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	LPM_REMOTEWAKE	0: Device is prohibited from initiating a remote wake 1: Device is allow to wake the host Default Value: 0
3 : 0	LPM_BESL	Best Effort Service Latency This value should match either the Baseline (DeepSleep) or Deep (Hibernate) BESL in the BOS descriptor. Default Value: 0

20.1.52 USBFS0_USBLPM_INTR_SIE

USB SOF, BUS RESET and EP0 Interrupt Status

Address: 0x403F2020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None			RW1S	RW1S	RW1S	RW1S	RW1S
Name	None [7:5]			RESUME_INTR	LPM_INTR	EP0_INTR	BUS_RESET_INTR	SOF_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	RESUME_INTR	Interrupt status for Resume Default Value: 0
3	LPM_INTR	Interrupt status for LPM (Link Power Management, L1 entry) Default Value: 0
2	EP0_INTR	Interrupt status for EP0 Default Value: 0
1	BUS_RESET_INTR	Interrupt status for BUS RESET Default Value: 0
0	SOF_INTR	Interrupt status for USB SOF Default Value: 0

20.1.53 USBFS0_USBLPM_INTR_SIE_SET (continued)

20.1.53 USBFS0_USBLPM_INTR_SIE_SET

USB SOF, BUS RESET and EP0 Interrupt Set

Address: 0x403F2024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	None			A	A	A	A	A
Name	None [7:5]			RESUME_INTR_SET	LPM_INTR_SET	EP0_INTR_SET	BUS_RESET_INTR_SET	SOF_INTR_SET

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	RESUME_INTR_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	LPM_INTR_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	EP0_INTR_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	BUS_RESET_INTR_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	SOF_INTR_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

20.1.54 USBFS0_USBLPM_INTR_SIE_MASK

USB SOF, BUS RESET and EP0 Interrupt Mask

Address: 0x403F2028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			RESUME_INTR_MASK	LPM_INTR_MASK	EP0_INTR_MASK	BUS_RESET_INTR_MASK	SOF_INTR_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	RESUME_INTR_MASK	Set to 1 to enable interrupt corresponding to interrupt request register Default Value: 0
3	LPM_INTR_MASK	Set to 1 to enable interrupt corresponding to interrupt request register Default Value: 0
2	EP0_INTR_MASK	Set to 1 to enable interrupt corresponding to interrupt request register Default Value: 0
1	BUS_RESET_INTR_MASK	Set to 1 to enable interrupt corresponding to interrupt request register Default Value: 0
0	SOF_INTR_MASK	Set to 1 to enable interrupt corresponding to interrupt request register Default Value: 0

20.1.55 USBFS0_USBLPM_INTR_SIE_MASKED (continued)

20.1.55 USBFS0_USBLPM_INTR_SIE_MASKED

USB SOF, BUS RESET and EP0 Interrupt Masked

Address: 0x403F202C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	R	R	R	R
HW Access	None			W	W	W	W	W
Name	None [7:5]			RESUME_INTR_MASKED	LPM_INTR_MASKED	EP0_INTR_MASKED	BUS_RESET_INTR_MASKED	SOF_INTR_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	RESUME_INTR_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
3	LPM_INTR_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
2	EP0_INTR_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
1	BUS_RESET_INTR_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
0	SOF_INTR_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

20.1.56 USBFS0_USBLPM_INTR_LVL_SEL

Select interrupt level for each interrupt source

Address: 0x403F2030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	LPM_LVL_SEL [7:6]		EP0_LVL_SEL [5:4]		BUS_RESET_LVL_SEL [3:2]		SOF_LVL_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None				RW	
HW Access	R		None				R	
Name	ARB_EP_LVL_SEL [15:14]		None [13:10]				RESUME_LVL_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EP4_LVL_SEL [23:22]		EP3_LVL_SEL [21:20]		EP2_LVL_SEL [19:18]		EP1_LVL_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EP8_LVL_SEL [31:30]		EP7_LVL_SEL [29:28]		EP6_LVL_SEL [27:26]		EP5_LVL_SEL [25:24]	

Bits	Name	Description
31 : 30	EP8_LVL_SEL	EP8 Interrupt level select Default Value: 0
29 : 28	EP7_LVL_SEL	EP7 Interrupt level select Default Value: 0
27 : 26	EP6_LVL_SEL	EP6 Interrupt level select Default Value: 0
25 : 24	EP5_LVL_SEL	EP5 Interrupt level select Default Value: 0
23 : 22	EP4_LVL_SEL	EP4 Interrupt level select Default Value: 0
21 : 20	EP3_LVL_SEL	EP3 Interrupt level select Default Value: 0
19 : 18	EP2_LVL_SEL	EP2 Interrupt level select Default Value: 0

20.1.56 USBFS0_USBLPM_INTR_LVL_SEL (continued)

17 : 16	EP1_LVL_SEL	EP1 Interrupt level select Default Value: 0
15 : 14	ARB_EP_LVL_SEL	Arbiter Endpoint Interrupt level select Default Value: 0
9 : 8	RESUME_LVL_SEL	Resume Interrupt level select Default Value: 0
7 : 6	LPM_LVL_SEL	LPM Interrupt level select Default Value: 0
5 : 4	EP0_LVL_SEL	EP0 Interrupt level select Default Value: 0
3 : 2	BUS_RESET_LVL_SEL	BUS RESET Interrupt level select Default Value: 0
1 : 0	SOF_LVL_SEL	USB SOF Interrupt level select Default Value: 0 **0x0: HI :** High priority interrupt **0x1: MED :** Medium priority interrupt **0x2: LO :** Low priority interrupt **0x3: RESERVED :** illegal

20.1.57 USBFS0_USBLPM_INTR_CAUSE_HI (continued)

20.1.57 USBFS0_USBLPM_INTR_CAUSE_HI

High priority interrupt Cause register

Address: 0x403F2034

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	None		R	R	R	R	R
HW Access	RW	None		RW	RW	RW	RW	RW
Name	ARB_EP_INTR	None [6:5]		RESUME_INTR	LPM_INTR	EP0_INTR	BUS_RESET_INTR	SOF_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	EP8_INTR	EP7_INTR	EP6_INTR	EP5_INTR	EP4_INTR	EP3_INTR	EP2_INTR	EP1_INTR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	EP8_INTR	EP8 Interrupt Default Value: 0
14	EP7_INTR	EP7 Interrupt Default Value: 0
13	EP6_INTR	EP6 Interrupt Default Value: 0
12	EP5_INTR	EP5 Interrupt Default Value: 0
11	EP4_INTR	EP4 Interrupt Default Value: 0
10	EP3_INTR	EP3 Interrupt Default Value: 0

20.1.57 USBFS0_USBLPM_INTR_CAUSE_HI (continued)

9	EP2_INTR	EP2 Interrupt Default Value: 0
8	EP1_INTR	EP1 Interrupt Default Value: 0
7	ARB_EP_INTR	Arbiter Endpoint Interrupt Default Value: 0
4	RESUME_INTR	Resume Interrupt Default Value: 0
3	LPM_INTR	LPM Interrupt Default Value: 0
2	EP0_INTR	EP0 Interrupt Default Value: 0
1	BUS_RESET_INTR	BUS RESET Interrupt Default Value: 0
0	SOF_INTR	USB SOF Interrupt Default Value: 0

20.1.58 USBFS0_USBLPM_INTR_CAUSE_MED (continued)

20.1.58 USBFS0_USBLPM_INTR_CAUSE_MED

Medium priority interrupt Cause register

Address: 0x403F2038

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	None		R	R	R	R	R
HW Access	RW	None		RW	RW	RW	RW	RW
Name	ARB_EP_INTR	None [6:5]		RESUME_INTR	LPM_INTR	EP0_INTR	BUS_RESET_INTR	SOF_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	EP8_INTR	EP7_INTR	EP6_INTR	EP5_INTR	EP4_INTR	EP3_INTR	EP2_INTR	EP1_INTR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	EP8_INTR	EP8 Interrupt Default Value: 0
14	EP7_INTR	EP7 Interrupt Default Value: 0
13	EP6_INTR	EP6 Interrupt Default Value: 0
12	EP5_INTR	EP5 Interrupt Default Value: 0
11	EP4_INTR	EP4 Interrupt Default Value: 0
10	EP3_INTR	EP3 Interrupt Default Value: 0

9	EP2_INTR	EP2 Interrupt Default Value: 0
8	EP1_INTR	EP1 Interrupt Default Value: 0
7	ARB_EP_INTR	Arbiter Endpoint Interrupt Default Value: 0
4	RESUME_INTR	Resume Interrupt Default Value: 0
3	LPM_INTR	LPM Interrupt Default Value: 0
2	EP0_INTR	EP0 Interrupt Default Value: 0
1	BUS_RESET_INTR	BUS RESET Interrupt Default Value: 0
0	SOF_INTR	USB SOF Interrupt Default Value: 0

20.1.59 USBFS0_USBLPM_INTR_CAUSE_LO (continued)

20.1.59 USBFS0_USBLPM_INTR_CAUSE_LO

Low priority interrupt Cause register

Address: 0x403F203C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	None		R	R	R	R	R
HW Access	RW	None		RW	RW	RW	RW	RW
Name	ARB_EP_INTR	None [6:5]		RESUME_INTR	LPM_INTR	EP0_INTR	BUS_RESET_INTR	SOF_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	EP8_INTR	EP7_INTR	EP6_INTR	EP5_INTR	EP4_INTR	EP3_INTR	EP2_INTR	EP1_INTR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	EP8_INTR	EP8 Interrupt Default Value: 0
14	EP7_INTR	EP7 Interrupt Default Value: 0
13	EP6_INTR	EP6 Interrupt Default Value: 0
12	EP5_INTR	EP5 Interrupt Default Value: 0
11	EP4_INTR	EP4 Interrupt Default Value: 0
10	EP3_INTR	EP3 Interrupt Default Value: 0

9	EP2_INTR	EP2 Interrupt Default Value: 0
8	EP1_INTR	EP1 Interrupt Default Value: 0
7	ARB_EP_INTR	Arbiter Endpoint Interrupt Default Value: 0
4	RESUME_INTR	Resume Interrupt Default Value: 0
3	LPM_INTR	LPM Interrupt Default Value: 0
2	EP0_INTR	EP0 Interrupt Default Value: 0
1	BUS_RESET_INTR	BUS RESET Interrupt Default Value: 0
0	SOF_INTR	USB SOF Interrupt Default Value: 0

20.1.60 USBFS0_USBLPM_DFT_CTL (continued)

20.1.60 USBFS0_USBLPM_DFT_CTL

DFT control

Address: 0x403F2070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW		RW		
HW Access	None			R		R		
Name	None [7:5]			DDFT_IN_SEL [4:3]		DDFT_OUT_SEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 3	DDFT_IN_SEL	DDFT input select signal Default Value: 0 **0x0: OFF :** Nothing connected, output 0 **0x1: GPIO_DP_IN :** GPIO input of DP **0x2: GPIO_DM_IN :** GPIO input of DM
2 : 0	DDFT_OUT_SEL	DDFT output select signal Default Value: 0

0x0: OFF :

Nothing connected, output 0

0x1: DP_SE :

Single Ended output of DP

0x2: DM_SE :

Single Ended output of DM

0x3: TXOE :

Output Enable

0x4: RCV_DF :

Differential Receiver output

0x5: GPIO_DP_OUT :

GPIO output of DP

0x6: GPIO_DM_OUT :

GPIO output of DM

20.1.61 USBFS0_USBHOST_HOST_CTL0 (continued)

20.1.61 USBFS0_USBHOST_HOST_CTL0

Host Control 0 Register.

Address: 0x403F4000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							RW
Name	None [7:1]							HOST

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	This bit enables the operation of this IP. '0' : Disable USB Host '1' : Enable USB Host Note: - This bit doesn't affect the USB Device. Default Value: 0

20.1.61 USBFS0_USBHOST_HOST_CTL0 (continued)

0	HOST	This bit selects an operating mode of this IP. '0' : USB Device '1' : USB Host Notes: - The mode of operation mode does not transition immediately after setting this bit. Read this bit to confirm that the operation mode has changed. - This bit is reset to '0' if the ENABLE bit in this register changes from '1' to '0'. - Before changing from the USB Host to the USB Device, check that the following conditions are satisfied and also set the RST bit of the Host Control 1 Register (HOST_CTL1). to '1'. * The SOFBUSY bit of the Host Status Register (HOST_STATUS) is set to '0'. * The TKNEN bits of the Host Token Endpoint Register (HOST_TOKEN) is set to '000'. * The SUSP bit of the Host Status Register (HOST_STATUS) is set to '0'. Default Value: 0

20.1.62 USBFS0_USBHOST_HOST_CTL1 (continued)

20.1.62 USBFS0_USBHOST_HOST_CTL1

Host Control 1 Register.

Address: 0x403F4010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	None					RW	RW
HW Access	R	None					R	R
Name	RST	None [6:2]					USTP	CLKSEL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	RST	This bit resets the USB Host. '0' : Normal operating mode. '1' : USB Host is reset. Notes: - This bit is to it's default value '1' if the ENABLE bit of the Host Control 0 Register (HOST_CTL0) changes from '1' to '0'. - If this bit is set to '1', both the BFINI bits of the Host Endpoint 1 Control Register (HOST_EP1_CTL) and Host Endpoint 2 Control Register (HOST_EP2_CTL) are set to '1'. Default Value: 1
1	USTP	This bit stops the clock for the USB Host operating unit. When this bit is '1', power consumption can be reduced by configuring this bit. '0' : Normal operating mode. '1' : Stops the clock for the USB Host operating unit. Notes: - If this bit is set to '1', the function of USB Host can't be used because internal clock is stopped. - This bit is initialized if ENABLE bit of the Host Control 0 Register (HOST_CTL0) changes from '1' to '0'. Default Value: 1

20.1.62 USBFS0_USBHOST_HOST_CTL1 (continued)

0	CLKSEL	This bit selects the operating clock of USB Host. '0' : Low-speed clock '1' : Full-speed clock Notes: - This bit is set to it's default vaulue '1' if the ENABLE bit of the Host Control 0 Register (HOST_CTL0) changes from '1' to '0'. - This bit must always be set to '1' in the USB Device mode. Default Value: 1

20.1.63 USBFS0_USBHOST_HOST_CTL2 (continued)

20.1.63 USBFS0_USBHOST_HOST_CTL2

Host Control 2 Register.

Address: 0x403F4100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW	RW	RW	RW	RW
HW Access	R		R	R	R	R	R	R
Name	TTEST [7:6]		RE-SERVED_5	RE-SERVED_4	ALIVE	SOFSTEP	CANCEL	RETRY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	TTEST	Reserved. Keep this bitfield at the default value. Default Value: 0
5	RESERVED_5	Reserved. Keep this bitfield at the default value. Default Value: 0
4	RESERVED_4	Reserved. Keep this bitfield at the default value. Default Value: 0
3	ALIVE	This bit is used to specify the keep-alive function in the low-speed mode. If this bit it set to '1' while the CLKSEL bit of the Host Control 1 Register (HOST_CTL1) is '0', SE0 is output instead of SOF. This bit is only effective when the CLKSEL bit is '0'. If the CLKSEL bit is '1' (Full-Speed mode), SOF is output regardless of the setting of the ALIVE bit. '0' : SOF output. '1' : SE0 output (Keep alive) Default Value: 0

2	SOFSTEP	If this bit is set to '1', the SOF interrupt flag (INTR_USBHOST.SOFIRQ) is set to '1' each time SOF is sent. If this bit is set to '0', the set value of the Host SOF Interrupt Frame Compare Register (HOST_FCOMP) is compared with the low-order eight bits of the SOF frame number. If they match, the SOF interrupt flag (INTR_USBHOST.SOFIRQ) is set to '1'. '0' : An interrupt occurred due to the HOST_HFCOMP setting. '1' : An interrupt occurred. Notes: - If a SOF token (TKNEN='001') is sent by the setting of the Host Token Endpoint Register (HOST_TOKEN), the SOF interrupt flag (INTR_USBHOST.SOFIRQ) is not set to '1' regardless of the setting of this bit. Default Value: 0
1	CANCEL	When this bit is set to '1', if the target token is written to the Host Token Endpoint Register (HOST_TOKEN) in the EOF area (specified in the Host EOF Setup Register), its sending is canceled. When this bit is set to '0', token sending is not canceled even if the target token is written to the register. The cancellation of token sending is detected by reading the TCAN bit of the Interrupt USB Host Register (INTR_USBHOST). '0' : Continues a token. '1' : Cancels a token. Default Value: 0
0	RETRY	If this bit is set to '1', the target token is retried if a NAK or error* occurs. Retry processing is performed after the time that is specified in the Host Retry Timer Setup Register (HOST_RTIMER). * : HOST_ERR.RERR='1', HOST_ERR.TOUT='1', HOST_ERR.CRC='1', HOST_ERR.TGERR='1', HOST_ERR.STUFF='1' '0' : Doesn't retry token sending. '1' : Retries token sending Note: - This bit isn't initialized even if the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 1

20.1.64 USBFS0_USBHOST_HOST_ERR (continued)

20.1.64 USBFS0_USBHOST_HOST_ERR

Host Error Status Register.

Address: 0x403F4104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1S	
HW Access	W1S	W1S	W1S	W1S	W1S	W1S	W	
Name	LSTSOF	RERR	TOUT	CRC	TGERR	STUFF	HS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	LSTSOF	If this bit is set to '1', it means that the SOF token can't be sent in the USB Host because other token is in process. When this bit is '0', it means that SOF token was sent with no error. Write '1' to clear, a write of '0' is ignored. '0' : SOF sent without error. '1' : SOF error detected. Note: - This bit is set to the default value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 0
6	RERR	When this bit is set to '1', it means that the received data exceeds the specified maximum number of packets in the USB Host. If a receive error is detected, bit5 (TOUT) of this register is also set to '1'. When this bit is '0', it means that no error is detected. Write '1' to clear, a write of '0' is ignored. '0' : No receive error. '1' : Maximum packet receive error detected. - This bit is set to the default value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 0

5	TOUT	If this bit is set to '1', it means that no response is returned from the device within the specified time after a token has been sent in the USB Host. When this bit is '0', it means that no timeout is detected. Write '1' to clear, a write of '0' is ignored. '0' : No timeout. '1' : Timeout has detected. Note: - This bit is set to the default value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 0
4	CRC	If this bit is set to '1', it means that a CRC error is detected in the USB Host. When this bit is '0', it means that no error is detected. If a CRC error is detected, bit5 (TOUT) of this register is also set to '1'. Write '1' to clear, a write of '0' is ignored. '0' : No CRC error. '1' : CRC error detected. Note: - This bit is set to the default value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 0
3	TGERR	If this bit is set to '1', it means that the data does not match the TGGL data. When this bit is '0', it means that no error is detected. Write '1' to clear, a write of '0' is ignored. '0' : No toggle error. '1' : Toggle error detected. Note: - This bit is set to the default value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 0
2	STUFF	If this bit is set to '1', it means that a bit stuffing error has been detected. When this bit is '0', it means that no error is detected. If a stuffing error is detected, bit5 (TOUT) of this register is also set to '1'. Write '1' to clear, a write of '0' is ignored. '0' : No stuffing error. '1' : Stuffing error detected. Note: - This bit is set to the default value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 0
1 : 0	HS	These flags indicate the status of a handshake packet to be sent or received. These flags are set to 'NULL' when no handshake occurs due to an error or when a SOF token has been ended with the TKNEN bit of the Host Token Endpoint Register (HOST_TOKEN). These bits are updated when sending or receiving has been ended. Write '11' to set the status back to 'NULL", all other write values are ignored. Note: This bit is set to the default value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 3 **0x0: ACK :** Acknowledge Packet **0x1: NAK :** Non-Acknowledge Packet **0x2: STALL :** Stall Packet

20.1.64 USBFS0_USBHOST_HOST_ERR (continued)

0x3: NULL :

Null Packet

20.1.65 USBFS0_USBHOST_HOST_STATUS (continued)

20.1.65 USBFS0_USBHOST_HOST_STATUS

Host Status Register.

Address: 0x403F4108

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	RW1S	RW0C	RW	R	R
HW Access	RW	RW	RW	RW0C	RW	RW	RW	RW
Name	CLK-SEL_ST	RSTBUSY	RE-SERVED_5	URST	SOFBUSY	SUSP	TMODE	CSTAT

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							RW
Name	None [15:9]							HOST_ST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	HOST_ST	This bit shows whether the device is in USB Host mode. If the HOST bit of the Host Control Register (HOST_CTL0) is set to '1', this bit is set to '1'. '0' : USB Device '1' : USB Host Notes: - If this bit is different from the HOST bit, The execution of a token must wait these bits match. - This bit takes time to be initialized by the RST bit of the Host Control 1 Resgiter (HOST_CTL1). Read this bit to confirm the operation is complete. Default Value: 0

7	CLKSEL_ST	This bit shows whether it is full-speed or not. If the CLKSEL bit of the Host Control 1 Register (HOST_CTL1) is set to '1', this bit is set to '1'. '0' : Low speed '1' : Full speed Note: - If this bit is different from the CLKSEL bit, The execution of the token and bus reset must wait these bits match. - This bit takes time to be initialized by the RST bit of the Host Control 1 Resgiter (HOST_CTL1). Read this bit to confirm the operation is complete. Default Value: 1
6	RSTBUSY	This bit shows that USB Host is being reset internally. If the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1', this bit is set to '1'. If the RST bit of Host Control 1 Register (HOST_CTL1) is set to '0', this bit is set to '0'. '0' : USB Host isn't being reset. '1' : USB Host is being reset. Notes: - If this bit is '1', the a token must not be executed. - This bit isn't set to '0' or '1' immediately even if the RST bit of Host Control 1 Register (HOST_CTL1) is set to '0' or '1'. Read this bit to confirm the operation is complete. Default Value: 1
5	RESERVED_5	Reserved. Keep this bitfield at the default value. Default Value: 0
4	URST	When this bit is set to '1', the USB bus is reset. This bit remains a '1' during USB bus resetting, and changes to '0' when USB bus resetting is ended. If this bit is set to '0', the USB bus reset is complete Default Value: 0
3	SOFBUSY	When a SOF token is sent using the Host Token Endpoint Register (HOST_TOKEN), this bit is set to '1', which means that the SOF timer is active. When this bit is '0', it means that the SOF timer is under suspension. To stop the active SOF timer, write '0' to this bit. However, if this bit is written with '1', its value is ignored. '0' : The SOF timer is stopped. '1' : The SOF timer is active. Notes: - This bit is set to the initial value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. - This bit takes time to be initialized by the RST bit of the Host Control 1 Resgiter (HOST_CTL1). - The SOF timer does not stop immediately after this bit has been set to '0' to stop the SOF timer. To check whether or not the SOF timer is stopped, read this bit. Default Value: 0
2	SUSP	If this bit is set to '1', the USB Host is placed into the suspend state. If this bit is set to '0' while it is '1' or the USB bus is placed into the k-state mode, then suspend state is released, and the RWIRQ bit of the Interrupt USB Host Register (INTR_USBHOST) is set to '1'. Set to '1' : Suspend. Set '0' when this bit is '1' : Resume. Other conditions : Holds the status. Notes: - This bit is set to the default value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. - The transition to disconnected on RST isn't immediate. Read this bit to confirm the transition is complete. - If this bit is set to '1', this bit must not be set to '1' until the RWIRQ bit of the Interrupt USB Host Register (INTR_USBHOST) is set to '1'. - Do not set this bit to '1' while the USB is active (during USB bus resetting, data transfer, or SOF timer running). - If the value of this bit is changed, it is not immediately reflected on the state of the USB bus. To check whether or not the state is updated, read this bit. Default Value: 0

20.1.65 USBFS0_USBHOST_HOST_STATUS (continued)

1	TMODE	If this bit is '1', it means that the device is connected in the full-speed mode. When this bit is '0', it means that the device is connected in the low-speed mode. This bit is valid when the CSTAT bit of the Host Status Register (HOST_STATUS) is '1'. '0' : Low-speed. '1' : Full-speed. Notes: - This bit is set to the default value if the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. - The transition to disconnected on RST isn't immediate. Read this bit to confirm the transition is complete. Default Value: 1
0	CSTAT	When this bit is '1', it means that the device is connected. When this bit is '0', it means that the device is disconnected. '0' : Device is disconnected. '1' : Device is connected. Notes: - This bit is set to the default value if the RST bit of the Host Control 1 Register (Host_CTL1) is set to '1'. - The transition to disconnected on RST isn't immediate. Read this bit to confirm the transition is complete. Default Value: 0

20.1.66 USBFS0_USBHOST_HOST_FCOMP (continued)

20.1.66 USBFS0_USBHOST_HOST_FCOMP

Host SOF Interrupt Frame Compare Register

Address: 0x403F410C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FRAMECOMP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	FRAMECOMP	These bits are used to specify the data to be compared with the low-order eight bits of a frame number when sending a SOF token. If the SOFSTEP bit of Host Control 2 Register (HOST_CTL2) is '0', the frame number of SOF is compared with the value of this register when sending a SOF token. If they match, the SOFIRQ bit of the Interrupt USB Host Register (INTR_USBHOST) is set to '1'. The setting of this register is invalid when the SOFSTEP bit of Host Control 2 Register (HOST_CTL2) is '1'. Note: - This bit is not reset to default even if the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 0

20.1.67 USBFS0_USBHOST_HOST_RTIMER

Host Retry Timer Setup Register

Address: 0x403F4110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RTIMER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RTIMER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						RTIMER [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 0	RTIMER	These bits are used to specify the retry time in this register. The retry timer is activated when token sending starts while the RETRY bit of Host Control 2 Register (HOST_CTL2) is '1'. The retry time is then decremented by one when a 1-bit transfer clock (12 MHz in the full-speed mode) is output. When the retry timer reaches 0, the target token is sent, and processing ends. If a token retry occurs in the EOF area, the retry timer is stopped until SOF sending is ended. After SOF sending has been completed, the retry timer restarts with the value that is set when the timer stopped. Default Value: 0

20.1.68 USBFS0_USBHOST_HOST_ADDR (continued)

20.1.68 USBFS0_USBHOST_HOST_ADDR

Host Address Register

Address: 0x403F4114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	ADDRESS [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 0	ADDRESS	These bits are used to specify a token address. Note: - This bit is reset to default even if the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 0

20.1.69 USBFS0_USBHOST_HOST_EOF

Host EOF Setup Register

Address: 0x403F4118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	EOF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW					
HW Access	None		R					
Name	None [15:14]		EOF [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13 : 0	EOF	These bits are used to specify the time to disable token sending before transferring SOF. Specify the time with a margin, which is longer than the one-packet length. The time unit is the 1-bit transfer time. Setting example: MAXPKT = 64 bytes, full-speed mode (Token_length + packet_length + header + CRC)*7/6 + Turn_around_time =(34 bit + 546 bit)*7/6 + 36 bit = 712.7 bit Therefore, set 0x2C9. Note: - This bit is not reset to default even if the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 0

20.1.70 USBFS0_USBHOST_HOST_FRAME (continued)

20.1.70 USBFS0_USBHOST_HOST_FRAME

Host Frame Setup Register

Address: 0x403F411C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	FRAME [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					RW		
Name	None [15:11]					FRAME [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10 : 0	FRAME	These bits are used to specify a frame number of SOF. Notes: - This bit isn't reset to default even if the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. - Specify a frame number in this register before setting SOF in the TKNEN bit of the Host Token Endpoint Register (HOST_TOKEN). - This register cannot be written while the SOFBUSY bit of the Host Status Register (HOST_STATUS) is '1' and a SOF token is in process. Default Value: 0

20.1.71 USBFS0_USBHOST_HOST_TOKEN

Host Token Endpoint Register

Address: 0x403F4120

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			RW			
HW Access	None	RW0C			R			
Name	None	TKNEN [6:4]			ENDPT [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							TGGL

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	TGGL	This bit is used to set toggle data. Toggle data is sent depending on the setting of this bit. When receiving toggle data, received toggle data is compared with the toggle data of this bit to verify whether or not an error occurs. '0' : DATA0 '1' : DATA1 Notes: - This bit isn't reset to the default value even if the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. - Set this bit when the TKNEN bit of the Host Token Endpoint Register (HOST_TOKEN) is '000'. Default Value: 0

6 : 4	TKNEN	These bits send a token according to the current settings. After operation is complete, the TKNEN bit is set to '000', and the CMPIRQ bit of the Interrupt USB Host Register (INTR_USBHOST) is set to '1'. The settings of the TGGL and ENDPT bits are ignored when sending a SOF token. Notes: - This bit is set to the default value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. - The PRE packet isn't supported. - Do not set '100' to the TKNEN bit when the SOFBUSY bit of the Host Status Register (HOST_STATUS) is '1' - Mode should be USB Host before writing data to this bit. - When issuing a token again after the token interrupt flag (CMPIRQ) has been set to '1', wait for 3 cycles or more after a USB transfer clock (12 MHz in the full-speed mode, 1.5 MHz in the low-speed mode) was output, then write data to this bit. - Read the value of TKNEN bit if a new value is written in it .Continue writing in this bit until a retrieved value equals a new value written in. During this checking process, it is needed to prevent any interrupt. - Take the following steps when CMPIRQ bit of Interrupt USB Host Register (INTR_USBHOST) is set to '1' by finishing IN token or Isochronous IN token. 1. Read HS bit of Host Error Status Register (HOST_ERR), then set CMPIRQ bit to '0'. 2. Set EPn bit of Host DMA Enable Register (HOST_DMA_ENBL) (n=1 or 2) to '1' if HS bit of Host Error Status Register (HOST_ERR) is equal to '00' and wait until EPn bit of Host DMA Data Request Register (HOST_DMA_DREQ) changes to '1'. Finish the IN token processing if HS bit is not equal to '00'. 3. Read the received data if EPn bit of Host DMA Data Requet (HOST_DMA_DREQ) (n=1 or 2) changes to '1'. Default Value: 0 **0x0: NONE :** Sends no data. **0x1: SETUP :** Sends SETUP token. **0x2: IN :** Sends IN token. **0x3: OUT :** Sends OUT token. **0x4: SOF :** Sends SOF token. **0x5: ISO_IN :** Sends Isochronous IN. **0x6: ISO_OUT :** Sends Isochronous OUT.

20.1.71 USBFS0_USBHOST_HOST_TOKEN (continued)

		0x7: RSV : Reserved.
3 : 0	ENDPT	These bits are used to specify an endpoint to send or receive data to or from the device. Note: - This bit isn't reset to default even if the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 0

20.1.72 USBFS0_USBHOST_HOST_EP1_CTL (continued)

20.1.72 USBFS0_USBHOST_HOST_EP1_CTL

Host Endpoint 1 Control Register

Address: 0x403F4400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PKS1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	None		RW	RW	RW	None	RW
HW Access	RW1S	None		R	R	R	None	R
Name	BFINI	None [14:13]		DIR	DMAE	NULLE	None	PKS1

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	BFINI	This bit initializes the send/receive buffer of transfer data. The BFINI bit is also automatically set by setting the RST bit of the HOST Control 1 Register (HOST_CTL1). If the RST bit was used for resetting, therefore, set the RST bit to "0" before clearing the BFINI bit. '0' : Clears the initialization. '1' : Initializes the send/receive buffer Note : - The EP1 buffer has a double-buffer configuration. The BFINI bit initialization initializes the double buffers concurrently and also initializes the EP1DRQ and EP1SPK bits. Default Value: 1
12	DIR	This bit specifies the transfer direction the Endpoint support. '0' : IN Endpoint. '1' : OUT Endpoint Note: - This bit must be changed when INI_ST bit of the Host Endpoint 1 Status Register (HOST_EP1_STATUS) is '1'. Default Value: 0

11	DMAE	This bit sets a mode that uses DMA for writing or reading transfer data to/from send/receive buffer, and automatically transfers the send/receive data synchronized with an data request in the IN or OUT direction. Until the data size set in the DMA is reached, the data is transferred. '0' : Releases the packet transfer mode. '1' : Sets the packet transfer mode. Note : - The CPU must not access the send/receive buffer while the DMAE bit is set to '1'. For data transfer in the IN direction, set the DMA transfer size to the multiples of that set in PKS1 bits of the Host EP1 Control Register (HOST_EP1_CTL) and Host EP2 Control Register (HOST_EP2_CTR). Default Value: 0
10	NULLE	When a data transfer request in OUT the direction is transmitted while automatic buffer transfer mode is set (DMAE = 1), this bit sets a mode that transfers 0-byte data automatically upon the detection of the last packet transfer. '0' : Releases the NULL automatic transfer mode. '1' : Sets the NULL automatic transfer mode. Note : - For data transfer in the IN direction or when automatic buffer transfer mode is not set, the NULL bit configuration does not affect communication. Default Value: 0
8 : 0	PKS1	This bit specifies the maximum size transferred by one packet. The configurable range is from 0x001 to 0x100. - If automatic buffer transfer mode (DMAE='1') is used, Endpoint 0,1, or 2 cannot be used, Default Value: 256

20.1.73 USBFS0_USBHOST_HOST_EP1_STATUS (continued)

20.1.73 USBFS0_USBHOST_HOST_EP1_STATUS

Host Endpoint 1 Status Register

Address: 0x403F4404

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	SIZE1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							RW
Name	None [15:9]							SIZE1

Bits	23	22	21	20	19	18	17	16
SW Access	None					R	R	R
HW Access	None					RW	RW	RW
Name	None [23:19]					RE-SERVED_18	INI_ST	VAL_DATA

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
18	RESERVED_18	Reserved. Keep this bitfield at the default value. Default Value: 1
17	INI_ST	This bit shows that EP1 is initialized. If the init bit of the Host Endpoint 1 Control Register (HOST_EP1_CTL) is set to '1' and EP1 is initialized, this bit is to '1'. '0' : Not initiatialized '1' : Initialized Note: - This bit isn't set to '0' or '1' immediately even if BFINI bit of the Host Endpoint 1 Control Register (HOST_EP1_CTL) is set to '0' or '1'. Read this bit to confirm the transition. Default Value: 1
16	VAL_DATA	This bit shows that there is valid data in the EP1 buffer. '0' : Invalid data in the buffer '1' : Valid data in the buffer Default Value: 0

8 : 0	SIZE1	These bits indicate the number of data bytes written to the receive buffer when IN packet transfer of EP1 has finished. The indication range is from 0x000 to 0x100. Note : - These bits are set to the data size transferred in the IN direction and written to the buffer. Therefore, a value read during transfer in the OUT direction has no effect. Default Value: X

20.1.74 USBFS0_USBHOST_HOST_EP1_RW1_DR (continued)

20.1.74 USBFS0_USBHOST_HOST_EP1_RW1_DR

Host Endpoint 1 Data 1-Byte Register

Address: 0x403F4408

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	BFDT8 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	BFDT8	Data Register for EP1 for 1-byte data Default Value: 0

20.1.75 USBFS0_USBHOST_HOST_EP1_RW2_DR

Host Endpoint 1 Data 2-Byte Register

Address: 0x403F440C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	BFDT16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	BFDT16 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	BFDT16	Data Register for EP1 for 2-byte data Default Value: 0

20.1.76 USBFS0_USBHOST_HOST_EP2_CTL (continued)

20.1.76 USBFS0_USBHOST_HOST_EP2_CTL

Host Endpoint 2 Control Register

Address: 0x403F4500

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	PKS2 [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	RW	None		RW	RW	RW	None	
HW Access	RW1S	None		R	R	R	None	
Name	BFINI	None [14:13]		DIR	DMAE	NULLE	None [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	BFINI	This bit initializes the send/receive buffer of transfer data. The BFINI bit is also automatically set by setting the RST bit of the HOST Control 1 Register (HOST_CTL1). If the RST bit was used for resetting, therefore, set the RST bit to '0' before clearing the BFINI bit. '0' : Clears the initialization. '1' : Initializes the send/receive buffer Note : - The EP2 buffer has a double-buffer configuration. The BFINI bit initialization initializes the double buffers concurrently and also initializes the EP2DRQ and EP2SPK bits. Default Value: 1
12	DIR	This bit specifies the transfer direction the Endpoint support. '0' : IN Endpoint. '1' : OUT Endpoint Note: - This bit must be changed when INI_ST bit of the Host Endpoint 2 Status Register (HOST_EP2_STATUS) is '1'. Default Value: 0

11	DMAE	This bit sets a mode that uses DMA for writing or reading transfer data to/from send/receive buffer, and automatically transfers the send/receive data synchronized with an data request in the IN or OUT direction. Until the data size set in the DMA is reached, the data is transferred. '0' : Releases the automatic buffer transfer mode. '1' : Sets the automatic buffer transfer mode. Note : - The CPU must not access the send/receive buffer while the DMAE bit is set to '1'. For data transfer in the IN direction, set the DMA transfer size to the multiples of that set in PKS bits of the Host EP1 Control Register (HOST_EP1_CTL) and Host EP2 Control Register (HOST_EP2_CTR). Default Value: 0
10	NULLE	When a data transfer request in the OUT direction transmitted while packet transfer mode is set (DMAE = 1), this bit sets a mode that transfers 0-byte data automatically upon the detection of the last packet transfer. '0' : Releases the NULL automatic transfer mode. '1' : Sets the NULL automatic transfer mode. Note : - For data transfer in the IN direction or when automatic buffer transfer mode is not set, the NULL bit configuration does not affect communication. Default Value: 0
6 : 0	PKS2	This bit specifies the maximum size transferred by one packet. The configurable range is from 0x001 to 0x40. - If automatic buffer transfer mode (DMAE='1') is used, this Endpoint must not set from 0 to 2. Default Value: 64

20.1.77 USBFS0_USBHOST_HOST_EP2_STATUS (continued)

20.1.77 USBFS0_USBHOST_HOST_EP2_STATUS

Host Endpoint 2 Status Register

Address: 0x403F4504

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R						
HW Access	None	RW						
Name	None	SIZE2 [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					R	R	R
HW Access	None					RW	RW	RW
Name	None [23:19]					RE-SERVED_18	INI_ST	VAL_DATA

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
18	RESERVED_18	Reserved. Keep this bitfield at the default value. Default Value: 1
17	INI_ST	This bit shows that EP2 is initialized. If the BFINI bit of the Host Endpoint 2 Control Register (HOST_EP2_CTL) is set to '1' and EP2 is initialized, this bit is to '1'. '0' : Not Initialized '1' : Initialized Note: - This bit isn't set to '0' or '1' immediately evne if BFINI bit of the Host Endpoint 2 Control Register (HOST_EP2_CTL) is set to '0' or '1'. Default Value: 1
16	VAL_DATA	This bit shows that there is valid data in the EP2 buffer. '0' : Invalid data in the buffer '1' : Valid data in the buffer Default Value: 0

6 : 0	SIZE2	These bits indicate the number of data bytes written to the receive buffer when IN packet transfer of EP2 has finished. The indication range is from 0x000 to 0x40. Note : - These bits are set to the data size transferred in the IN direction and written to the buffer. Therefore, a value read during transfer in the OUT direction has no effect. Default Value: X

20.1.78 USBFS0_USBHOST_HOST_EP2_RW1_DR (continued)

20.1.78 USBFS0_USBHOST_HOST_EP2_RW1_DR

Host Endpoint 2 Data 1-Byte Register

Address: 0x403F4508

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	BFDT8 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	BFDT8	Data Register for EP2 for 1-byte data. Default Value: 0

20.1.79 USBFS0_USBHOST_HOST_EP2_RW2_DR

Host Endpoint 2 Data 2-Byte Register

Address: 0x403F450C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	BFDT16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	BFDT16 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	BFDT16	Data Register for EP2 for 2 byte data. Default Value: 0

20.1.80 USBFS0_USBHOST_HOST_LVL1_SEL (continued)

20.1.80 USBFS0_USBHOST_HOST_LVL1_SEL

Host Interrupt Level 1 Selection Register

Address: 0x403F4800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	CMPIRQ_SEL [7:6]		CNNIRQ_SEL [5:4]		DIRQ_SEL [3:2]		SOFIRQ_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	TCAN_SEL [15:14]		RESERVED_13_12 [13:12]		RWKIRQ_SEL [11:10]		URIRQ_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 14	TCAN_SEL	These bits assign TCAN interrupt flag to selected interrupt signals. Default Value: 0
13 : 12	RESERVED_13_12	Reserved. Keep this bitfield at the default value. Default Value: 0
11 : 10	RWKIRQ_SEL	These bits assign RWKIRQ interrupt flag to selected interrupt signals. Default Value: 0
9 : 8	URIRQ_SEL	These bits assign URIRQ interrupt flag to selected interrupt signals. Default Value: 0
7 : 6	CMPIRQ_SEL	These bits assign URIRQ interrupt flag to selected interrupt signals. Default Value: 0
5 : 4	CNNIRQ_SEL	These bits assign CNNIRQ interrupt flag to selected interrupt signals. Default Value: 0
3 : 2	DIRQ_SEL	These bits assign DIRQ interrupt flag to selected interrupt signals. Default Value: 0

1 : 0	SOFIRQ_SEL	These bits assign SOFIRQ interrupt flag to selected interrupt signals. Default Value: 0 **0x0: HI :** High priority interrupt **0x1: MED :** Medium priority interrupt **0x2: LO :** Low priority interrupt **0x3: RESERVED :** Reserved.

20.1.81 USBFS0_USBHOST_HOST_LVL2_SEL (continued)

20.1.81 USBFS0_USBHOST_HOST_LVL2_SEL

Host Interrupt Level 2 Selection Register

Address: 0x403F4804

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		None			
HW Access	R		R		None			
Name	EP1_SPK_SEL [7:6]		EP1_DRQ_SEL [5:4]		None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [15:12]				EP2_SPK_SEL [11:10]		EP2_DRQ_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 10	EP2_SPK_SEL	These bits assign EP2_SPK interrupt flag to selected interrupt signals. Default Value: 0
9 : 8	EP2_DRQ_SEL	These bits assign EP2_DRQ interrupt flag to selected interrupt signals. Default Value: 0
7 : 6	EP1_SPK_SEL	These bits assign EP1_SPK interrupt flag to selected interrupt signals. Default Value: 0
5 : 4	EP1_DRQ_SEL	These bits assign EP1_DRQ interrupt flag to selected interrupt signals. Default Value: 0
		0x0: HI : High priority interrupt

0x1: MED :

Medium priority interrupt

0x2: LO :

Low priority interrupt

0x3: RESERVED :

Reserved.

20.1.82 USBFS0_USBHOST_INTR_USBHOST_CAUSE_HI (continued)

20.1.82 USBFS0_USBHOST_INTR_USBHOST_CAUSE_HI

Interrupt USB Host Cause High Register

Address: 0x403F4900

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	TCAN_INT	RE-SERVED_6	RWKIRQ_INT	URIRQ_INT	CM-PIRQ_INT	CN-NIRQ_INT	DIRQ_INT	SO-FIRQ_INT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	TCAN_INT	TCAN interrupt Default Value: 0
6	RESERVED_6	Reserved. Default Value: 0
5	RWKIRQ_INT	RWKIRQ interrupt Default Value: 0
4	URIRQ_INT	URIRQ interrupt Default Value: 0
3	CMPIRQ_INT	CMPIRQ interrupt Default Value: 0
2	CNNIRQ_INT	CNNIRQ interrupt Default Value: 0
1	DIRQ_INT	DIRQ interrupt Default Value: 0

0	SOFIRQ_INT	SOFIRQ interrupt Default Value: 0

20.1.83 USBFS0_USBHOST_INTR_USBHOST_CAUSE_MED (continued)

20.1.83 USBFS0_USBHOST_INTR_USBHOST_CAUSE_MED

Interrupt USB Host Cause Medium Register

Address: 0x403F4904

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	TCAN_INT	RE-SERVED_6	RWKIRQ_INT	URIRQ_INT	CM-PIRQ_INT	CN-NIRQ_INT	DIRQ_INT	SO-FIRQ_INT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	TCAN_INT	TCAN interrupt Default Value: 0
6	RESERVED_6	Reserved. Default Value: 0
5	RWKIRQ_INT	RWKIRQ interrupt Default Value: 0
4	URIRQ_INT	URIRQ interrupt Default Value: 0
3	CMPIRQ_INT	CMPIRQ interrupt Default Value: 0
2	CNNIRQ_INT	CNNIRQ interrupt Default Value: 0
1	DIRQ_INT	DIRQ interrupt Default Value: 0

20.1.83 USBFS0_USBHOST_INTR_USBHOST_CAUSE_MED (continued)

0	SOFIRQ_INT	SOFIRQ interrupt Default Value: 0

20.1.84 USBFS0_USBHOST_INTR_USBHOST_CAUSE_LO (continued)

20.1.84 USBFS0_USBHOST_INTR_USBHOST_CAUSE_LO

Interrupt USB Host Cause Low Register

Address: 0x403F4908

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	TCAN_INT	RE-SERVED_6	RWKIRQ_INT	URIRQ_INT	CM-PIRQ_INT	CN-NIRQ_INT	DIRQ_INT	SO-FIRQ_INT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	TCAN_INT	TCAN interrupt Default Value: 0
6	RESERVED_6	Reserved. Default Value: 0
5	RWKIRQ_INT	RWKIRQ interrupt Default Value: 0
4	URIRQ_INT	URIRQ interrupt Default Value: 0
3	CMPIRQ_INT	CMPIRQ interrupt Default Value: 0
2	CNNIRQ_INT	CNNIRQ interrupt Default Value: 0
1	DIRQ_INT	DIRQ interrupt Default Value: 0

20.1.84 USBFS0_USBHOST_INTR_USBHOST_CAUSE_LO (continued)

0	SOFIRQ_INT	SOFIRQ interrupt Default Value: 0

20.1.85 USBFS0_USBHOST_INTR_HOST_EP_CAUSE_HI (continued)

20.1.85 USBFS0_USBHOST_INTR_HOST_EP_CAUSE_HI

Interrupt USB Host Endpoint Cause High Register

Address: 0x403F4920

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	None	
HW Access	None		W	W	W	W	None	
Name	None [7:6]		EP2SPK_INT	EP2DRQ_INT	EP1SPK_INT	EP1DRQ_INT	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	EP2SPK_INT	EP2SPK interrupt Default Value: 0
4	EP2DRQ_INT	EP2DRQ interrupt Default Value: 0
3	EP1SPK_INT	EP1SPK interrupt Default Value: 0
2	EP1DRQ_INT	EP1DRQ interrupt Default Value: 0

20.1.86 USBFS0_USBHOST_INTR_HOST_EP_CAUSE_MED (continued)

20.1.86 USBFS0_USBHOST_INTR_HOST_EP_CAUSE_MED

Interrupt USB Host Endpoint Cause Medium Register

Address: 0x403F4924

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	None	
HW Access	None		W	W	W	W	None	
Name	None [7:6]		EP2SPK_INT	EP2DRQ_INT	EP1SPK_INT	EP1DRQ_INT	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	EP2SPK_INT	EP2SPK interrupt Default Value: 0
4	EP2DRQ_INT	EP2DRQ interrupt Default Value: 0
3	EP1SPK_INT	EP1SPK interrupt Default Value: 0
2	EP1DRQ_INT	EP1DRQ interrupt Default Value: 0

20.1.87 USBFS0_USBHOST_INTR_HOST_EP_CAUSE_LO

Interrupt USB Host Endpoint Cause Low Register

Address: 0x403F4928

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	None	
HW Access	None		W	W	W	W	None	
Name	None [7:6]		EP2SP-K_INT	EP2DRQ_INT	EP1SP-K_INT	EP1DRQ_INT	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	EP2SPK_INT	EP2SPK interrupt Default Value: 0
4	EP2DRQ_INT	EP2DRQ interrupt Default Value: 0
3	EP1SPK_INT	EP1SPK interrupt Default Value: 0
2	EP1DRQ_INT	EP1DRQ interrupt Default Value: 0

20.1.88 USBFS0_USBHOST_INTR_USBHOST (continued)

20.1.88 USBFS0_USBHOST_INTR_USBHOST

Interrupt USB Host Register

Address: 0x403F4940

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S
Name	TCAN	RE-SERVED_6	RWKIRQ	URIRQ	CMPIRQ	CNNIRQ	DIRQ	SOFIRQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	TCAN	If this bit is set to '1', it means that token sending is canceled based on the setting of the CANCEL bit of Host Control 2 Register (HOST_CTL2). When this bit is '0', it means that token sending is not canceled. Write '1' to clear, a write of '0' is ignored. '0' : Does not cancel token sending. '1' : Cancels token sending. Note : - This bit is set to the default value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 0
6	RESERVED_6	Reserved. Default Value: 0

5	RWKIRQ	If this bit is set to '1', it means that remote Wake-up is ended. When this bit is '0', it has no meaning. Write '1' to clear, a write of '0' is ignored. '0' : Issues no interrupt request by restart. '1' : Issues an interrupt request by restart. Note : - This bit is set to the default value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 0
4	URIRQ	If this bit is set to '1', it means that USB bus resetting is ended. When this bit is '0', it has no meaning. If this bit is written with '1', it is set to '0'. However, if this bit is written with '0', its value is ignored. '0' : Issues no interrupt request by USB bus resetting. '1' : Issues an interrupt request by USB bus resetting. Note : - This bit is set to the initial value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 0
3	CMPIRQ	If this bit is set to '1', it means that a token is completed. When this bit is '0', it has no meaning. Write '1' to clear, a write of '0' is ignored. '0' : Issues no interrupt request by token completion. '1' : Issues an interrupt request by token completion. Note : - This bit is set to the initial value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. - This bit is not set to '1' even if the TCAN bit of the Interrupt USBHost Register (INTR_USBHOST) changes to '1'. - Take the following steps when this bit is set to '1' by finishing IN token or Isochronous IN token. 1. Read HS bit of Host Error Status Register (HOST_ERR), then set CMPIRQ bit to '0'. 2. Set EPn bit of Host DMA Enable Register (HOST_DMA_ENBL) (n=1 or 2) to '1' if HS bit of Host Error Status Register (HOST_ERR) is equal to '00' and wait until EPn bit of Host DMA Data Request Register (HOST_DMA_DREQ) changes to '1'. Finish the IN token processing if HS bit is not equal to '00'. 3. Read the received data if EPn bit of Host DMA Data Requet (HOST_DMA_DREQ) (n=1 or 2) changes to '1'. Default Value: 0
2	CNNIRQ	If this bit is set to '1', it means that a device connection is detected. When this bit is '0', it has no meaning. Write '1' to clear, a write of '0' is ignored. '0' : Issues no interrupt request by detecting a device connection. '1' : Issues an interrupt request by detecting a device connection. Note : - This bit is set to the default value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 0
1	DIRQ	If this bit is set to '1', it means that a device disconnection is detected. When this bit is '0', it has no meaning. Write '1' to clear, a write of '0' is ignored. '0' : Issues no interrupt request by detecting a device disconnection. '1' : Issues an interrupt request by detecting a device disconnection. Note : - This bit is set to the default value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 0

20.1.88 USBFS0_USBHOST_INTR_USBHOST (continued)

0	SOFIRQ	If this bit is set to '1', it means that SOF token sending is started. When this bit is '0', it has no meaning. Write '1' to clear, a write of '0' is ignored. '0' : Does not issue an interrupt request by starting a SOF token. '1' : Issues an interrupt request by starting a SOF token. Note : - This bit is set to the default value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 0

20.1.89 USBFS0_USBHOST_INTR_USBHOST_SET (continued)

20.1.89 USBFS0_USBHOST_INTR_USBHOST_SET

Interrupt USB Host Set Register

Address: 0x403F4944

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	TCANS	RE-SERVED_6	RWKIRQS	URIRQS	CMPIRQS	CNNIRQS	DIRQS	SOFIRQS

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	TCANS	This bit sets TCAN bit. If this bit is written to '1', TCAN is set to '1'. However, if this bit is written with '0', its value is ignored. Default Value: 0
6	RESERVED_6	Reserved. Keep this bitfield at the default value. Default Value: 0
5	RWKIRQS	This bit sets RWKIRQ bit. If this bit is written to '1', RWKIRQ is set to '1'. However, if this bit is written with '0', its value is ignored. Default Value: 0
4	URIRQS	This bit sets URIRQ bit. If this bit is written to '1', URIRQ is set to '1'. However, if this bit is written with '0', its value is ignored. Default Value: 0
3	CMPIRQS	This bit sets CMPIRQ bit. If this bit is written to '1', CMPIRQ is set to '1'. However, if this bit is written with '0', its value is ignored. Default Value: 0

20.1.89 USBFS0_USBHOST_INTR_USBHOST_SET (continued)

2	CNNIRQS	This bit sets CNNIRQ bit. If this bit is written to '1', CNNIRQ is set to '1'. However, if this bit is written with '0', its value is ignored. Default Value: 0
1	DIRQS	This bit sets DIRQ bit. If this bit is written to '1', DIRQ is set to '1'. However, if this bit is written with '0', its value is ignored. Default Value: 0
0	SOFIRQS	This bit sets SOFIRQ bit. If this bit is written to '1', SOFIRQ is set to '1'. However, if this bit is written with '0', its value is ignored. Default Value: 0

20.1.90 USBFS0_USBHOST_INTR_USBHOST_MASK (continued)

20.1.90 USBFS0_USBHOST_INTR_USBHOST_MASK

Interrupt USB Host Mask Register

Address: 0x403F4948

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	TCANM	RE-SERVED_6	RWKIRQM	URIRQM	CMPIRQM	CNNIRQM	DIRQM	SOFIRQM

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	TCANM	This bit masks the interrupt by TCAN flag. '0' : Disables '1' : Enables Default Value: 0
6	RESERVED_6	Reserved. Keep this bitfield at the default value. Default Value: 0
5	RWKIRQM	This bit masks the interrupt by RWKIRQ flag. '0' : Disables '1' : Enables Default Value: 0
4	URIRQM	This bit masks the interrupt by URIRQ flag. '0' : Disables '1' : Enables Default Value: 0

3	CMPIRQM	This bit masks the interrupt by CMPIRQ flag. '0' : Disables '1' : Enables Default Value: 0
2	CNNIRQM	This bit masks the interrupt by CNNIRQ flag. '0' : Disables '1' : Enables Default Value: 0
1	DIRQM	This bit masks the interrupt by DIRQ flag. '0' : Disables '1' : Enables Default Value: 0
0	SOFIRQM	This bit masks the interrupt by SOF flag. '0' : Disables '1' : Enables Default Value: 0

20.1.91 USBFS0_USBHOST_INTR_USBHOST_MASKED (continued)

20.1.91 USBFS0_USBHOST_INTR_USBHOST_MASKED

Interrupt USB Host Masked Register

Address: 0x403F494C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	TCANED	RE-SERVED_6	RWKIRQED	URIRQED	CMPIRQED	CNNIRQED	DIRQED	SOFIRQED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	TCANED	This bit indicates the interrupt by TCAN flag. '0' : Doesn't request the interrupt by TCAN '1' : Request the interrupt by TCAN Default Value: 0
6	RESERVED_6	Reserved. Default Value: 0
5	RWKIRQED	This bit indicates the interrupt by RWKIRQ flag. '0' : Doesn't request the interrupt by RWKIRQ '1' : Request the interrupt by RWKIRQ Default Value: 0
4	URIRQED	This bit indicates the interrupt by URIRQ flag. '0' : Doesn't request the interrupt by URIRQ '1' : Request the interrupt by URIRQ Default Value: 0

3	CMPIRQED	This bit indicates the interrupt by CMPIRQ flag. '0' : Doesn't request the interrupt by CMPIRQ '1' : Request the interrupt by CMPIRQ Default Value: 0
2	CNNIRQED	This bit indicates the interrupt by CNNIRQ flag. '0' : Doesn't request the interrupt by CNNIRQ '1' : Request the interrupt by CNNIRQ Default Value: 0
1	DIRQED	This bit indicates the interrupt by DIRQ flag. '0' : Doesn't request the interrupt by DIRQ '1' : Request the interrupt by DIRQ Default Value: 0
0	SOFIRQED	This bit indicates the interrupt by SOF flag. '0' : Doesn't request the interrupt by SOF '1' : Request the interrupt by SOF Default Value: 0

20.1.92 USBFS0_USBHOST_INTR_HOST_EP (continued)

20.1.92 USBFS0_USBHOST_INTR_HOST_EP

Interrupt USB Host Endpoint Register

Address: 0x403F4A00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1C	RW1C	RW1C	RW1C	None	
HW Access	None		W1S	W1S	W1S	W1S	None	
Name	None [7:6]		EP2SPK	EP2DRQ	EP1SPK	EP1DRQ	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	EP2SPK	This bit indicates that the data size transferred from the host does not satisfy the maximum packet size (including 0-byte) set by PKS1 in the Host Endpoint 2 Control Register (HOST_EP2_CTL) when the data has been received successfully. This bit is an interrupt cause, and writing '0' is ignored. Clear it by writing '1'. '0' : Received data size satisfies the maximum packet size '1' : Received data size does not satisfy the maximum packet size Note : - The SPK bit is not set during data transfer in the OUT direction. Default Value: 0

20.1.92 USBFS0_USBHOST_INTR_HOST_EP (continued)

4	EP2DRQ	This bit indicates that the EP2 packet transfer has normally ended, and processing of the data is required. The DRQ bit is an interrupt cause, and writing '0' is ignored. Clear the DRQ bit by writing '1'. '0' : Clears the interrupt cause '1' : Packet transfer normally ended Note : - If packet transfer mode (DMAE = '1') is not used, '1' must be written to the DRQ bit after data has been written or read to/from the send/receive buffer. Switch the access buffers once the DRQ bit is cleared. That DRQ = '0' may not be read after the DRQ bit is cleared. If the transfer direction is set to OUT, and the DRQ bit is cleared without writing buffer data while the DRQ bit is '1', it implies that 0-byte data is set. If DIR of the Host Endpoint 2 Control Register (HOST_EP2_CTL) is set to '1' at initial settings, the DRQ bit of corresponding Endpoint is set at the same time. Also while the DRQ bit is not set, '1' must not be written. Default Value: 0
3	EP1SPK	This bit indicates that the data size transferred from the host does not satisfy the maximum packet size (including 0-byte) set by PKS in the Host Endpoint 1 Control Register (HOST_EP1_CTL) when the data has been received successfully. This bit is an interrupt cause, and writing '0' is ignored. Clear it by writing '1'. '0' : Received data size satisfies the maximum packet size '1' : Received data size does not satisfy the maximum packet size Note : - The EP1SPK bit is not set during data transfer in the OUT direction. Default Value: 0
2	EP1DRQ	This bit indicates that the EP1 packet transfer has normally ended, and processing of the data is required. The DRQ bit is an interrupt cause, and writing '0' is ignored. Clear the DRQ bit by writing '1'. '0' : Clears the interrupt cause '1' : Packet transfer normally ended Note : - If automatic buffer transfer mode (DMAE = '1') is not used, '1' must be written to the DRQ bit after data has been written or read to/from the send/receive buffer. Switch the access buffers once the DRQ bit is cleared. That DRQ = '0' may not be read after the DRQ bit is cleared. If the transfer direction is set to OUT, and the DRQ bit is cleared without writing buffer data while the DRQ bit is '1', it implies that 0-byte data is set. If DIR of the Host Endpoint 1 Control Register (HOST_EP1_CTL) is set to '1' at initial settings, the DRQ bit of corresponding Endpoint is set at the same time. Also while the DRQ bit is not set, '1' must not be written. Default Value: 0

20.1.93 USBFS0_USBHOST_INTR_HOST_EP_SET (continued)

20.1.93 USBFS0_USBHOST_INTR_HOST_EP_SET

Interrupt USB Host Endpoint Set Register

Address: 0x403F4A04

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1S	RW1S	RW1S	RW1S	None	
HW Access	None		A	A	A	A	None	
Name	None [7:6]		EP2SPKS	EP2DRQS	EP1SPKS	EP1DRQS	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	EP2SPKS	This bit sets EP2SPK bit. If this bit is written to '1', EP2SPK is set to '1'. However, if this bit is written with '0', its value is ignored. Note: If BFINI bit of the Host Endpoint 2 Control Register (HOST_EP2_CTL) is '1', EP2SPK can't be set to '1'. Default Value: 0
4	EP2DRQS	This bit sets EP2DRQ bit. If this bit is written to '1', EP2DRQ is set to '1'. However, if this bit is written with '0', its value is ignored. Note: If BFINI bit of the Host Endpoint 2 Control Register (HOST_EP2_CTL) is '1', EP2DRQ can't be set to '1'. Default Value: 0

20.1.93 USBFS0_USBHOST_INTR_HOST_EP_SET (continued)

3	EP1SPKS	This bit sets EP1SPK bit. If this bit is written to '1', EP1SPK is set to '1'. However, if this bit is written with '0', its value is ignored. Note: If BFINI bit of the Host Endpoint 1 Control Register (HOST_EP1_CTL) is '1', EP1SPK can't be set to '1'. Default Value: 0
2	EP1DRQS	This bit sets EP1DRQ bit. If this bit is written to '1', EP1DRQ is set to '1'. However, if this bit is written with '0', its value is ignored. Note: If BFINI bit of the Host Endpoint 1 Control Register (HOST_EP1_CTL) is '1', EP1DRQ can't be set to '1'. Default Value: 0

20.1.94 USBFS0_USBHOST_INTR_HOST_EP_MASK (continued)

20.1.94 USBFS0_USBHOST_INTR_HOST_EP_MASK

Interrupt USB Host Endpoint Mask Register

Address: 0x403F4A08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	None	
HW Access	None		R	R	R	R	None	
Name	None [7:6]		EP2SPKM	EP2DRQM	EP1SPKM	EP1DRQM	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	EP2SPKM	This bit masks the interrupt by EP2SPK flag. '0' : Disables '1' : Enables Default Value: 0
4	EP2DRQM	This bit masks the interrupt by EP2DRQ flag. '0' : Disables '1' : Enables Default Value: 0
3	EP1SPKM	This bit masks the interrupt by EP1SPK flag. '0' : Disables '1' : Enables Default Value: 0
2	EP1DRQM	This bit masks the interrupt by EP1DRQ flag. '0' : Disables '1' : Enables Default Value: 0

20.1.95 USBFS0_USBHOST_INTR_HOST_EP_MASKED (continued)

20.1.95 USBFS0_USBHOST_INTR_HOST_EP_MASKED

Interrupt USB Host Endpoint Masked Register

Address: 0x403F4A0C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	None	
HW Access	None		RW	RW	RW	RW	None	
Name	None [7:6]		EP2SPKED	EP2DRQED	EP1SPKED	EP1DRQED	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	EP2SPKED	This bit indicates the interrupt by EP2SPK flag. '0' : Doesn't request the interrupt by EP2SPK '1' : Request the interrupt by EP2SPK Default Value: 0
4	EP2DRQED	This bit indicates the interrupt by EP2DRQ flag. '0' : Doesn't request the interrupt by EP2DRQ '1' : Request the interrupt by EP2DRQ Default Value: 0
3	EP1SPKED	This bit indicates the interrupt by EP1SPK flag. '0' : Doesn't request the interrupt by EP1SPK '1' : Request the interrupt by EP1SPK Default Value: 0
2	EP1DRQED	This bit indicates the interrupt by EP1DRQ flag. '0' : Doesn't request the interrupt by EP1DRQ '1' : Request the interrupt by EP1DRQ Default Value: 0

20.1.96 USBFS0_USBHOST_HOST_DMA_ENBL (continued)

20.1.96 USBFS0_USBHOST_HOST_DMA_ENBL

Host DMA Enable Register

Address: 0x403F4B00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	None	
HW Access	None				R	R	None	
Name	None [7:4]				DM_EP2DRQE	DM_EP1DRQE	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	DM_EP2DRQE	This bit enables DMA Request by EP2DRQ. '0' : Disable '1' : Enable Default Value: 0
2	DM_EP1DRQE	This bit enables DMA Request by EP1DRQ. '0' : Disable '1' : Enable Default Value: 0

20.1.97 USBFS0_USBHOST_HOST_EP1_BLK (continued)

20.1.97 USBFS0_USBHOST_HOST_EP1_BLK

Host Endpoint 1 Block Register

Address: 0x403F4B20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	BLK_NUM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	BLK_NUM [31:24]							

Bits	Name	Description
31 : 16	BLK_NUM	Set the total byte number for DMA transfer. If HOST_EP1_RW1_DR or HOST_EP1_RW2_DR is written, the block number counter is decremented when DMAE='1'. - Set this bits before DMA transfer is enabled (HOST_DMA_ENBL.DM_DP1DRQE='1') Default Value: 0

20.1.98 USBFS0_USBHOST_HOST_EP2_BLK (continued)

20.1.98 USBFS0_USBHOST_HOST_EP2_BLK

Host Endpoint 2 Block Register

Address: 0x403F4B30

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	BLK_NUM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	BLK_NUM [31:24]							

Bits	Name	Description
31 : 16	BLK_NUM	Set the total byte number for DMA transfer. If HOST_EP2_RW1_DR or HOST_EP2_RW2_DR is written, the block number counter is decremented when DMAE='1'. - Set this bits before DMA transfer is enabled (HOST_DMA_ENBL.DM_DP2DRQE='1') Default Value: 0

Section F: Peripheral Group 4

This section encompasses the following chapters:

- Serial Memory Interface Registers chapter on page 1591

21 Serial Memory Interface Registers

This section discusses the Serial Memory Interface (SMIF) registers. It lists all the registers in mapping tables, in address order.

21.1 Register Details

Register	Address	Description
SMIF0_CTL	0x40420000	Control
SMIF0_STATUS	0x40420004	Status
SMIF0_TX_CMD_FIFO_STATUS	0x40420044	Transmitter command FIFO status
SMIF0_TX_CMD_FIFO_WR	0x40420050	Transmitter command FIFO write
SMIF0_TX_DATA_FIFO_CTL	0x40420080	Transmitter data FIFO control
SMIF0_TX_DATA_FIFO_STATUS	0x40420084	Transmitter data FIFO status
SMIF0_TX_DATA_FIFO_WR1	0x40420090	Transmitter data FIFO write
SMIF0_TX_DATA_FIFO_WR2	0x40420094	Transmitter data FIFO write
SMIF0_TX_DATA_FIFO_WR4	0x40420098	Transmitter data FIFO write
SMIF0_RX_DATA_FIFO_CTL	0x404200C0	Receiver data FIFO control
SMIF0_RX_DATA_FIFO_STATUS	0x404200C4	Receiver data FIFO status
SMIF0_RX_DATA_FIFO_RD1	0x404200D0	Receiver data FIFO read
SMIF0_RX_DATA_FIFO_RD2	0x404200D4	Receiver data FIFO read
SMIF0_RX_DATA_FIFO_RD4	0x404200D8	Receiver data FIFO read
SMIF0_RX_DATA_FIFO_RD1_SILENT	0x404200E0	Receiver data FIFO silent read
SMIF0_SLOW_CA_CTL	0x40420100	Slow cache control
SMIF0_SLOW_CA_CMD	0x40420108	Slow cache command
SMIF0_FAST_CA_CTL	0x40420180	Fast cache control
SMIF0_FAST_CA_CMD	0x40420188	Fast cache command
SMIF0_CRYPTO_CMD	0x40420200	Cryptography Command
SMIF0_CRYPTO_INPUT0	0x40420220	Cryptography input 0
SMIF0_CRYPTO_INPUT1	0x40420224	Cryptography input 1
SMIF0_CRYPTO_INPUT2	0x40420228	Cryptography input 2
SMIF0_CRYPTO_INPUT3	0x4042022C	Cryptography input 3
SMIF0_CRYPTO_KEY0	0x40420240	Cryptography key 0
SMIF0_CRYPTO_KEY1	0x40420244	Cryptography key 1

Register	Address	Description
SMIF0_CRYPTO_KEY2	0x40420248	Cryptography key 2
SMIF0_CRYPTO_KEY3	0x4042024C	Cryptography key 3
SMIF0_CRYPTO_OUTPUT0	0x40420260	Cryptography output 0
SMIF0_CRYPTO_OUTPUT1	0x40420264	Cryptography output 1
SMIF0_CRYPTO_OUTPUT2	0x40420268	Cryptography output 2
SMIF0_CRYPTO_OUTPUT3	0x4042026C	Cryptography output 3
SMIF0_INTR	0x404207C0	Interrupt register
SMIF0_INTR_SET	0x404207C4	Interrupt set register
SMIF0_INTR_MASK	0x404207C8	Interrupt mask register
SMIF0_INTR_MASKED	0x404207CC	Interrupt masked register
SMIF0_DEVICE0_CTL	0x40420800	Control
SMIF0_DEVICE0_ADDR	0x40420808	Device region base address
SMIF0_DEVICE0_MASK	0x4042080C	Device region mask
SMIF0_DEVICE0_ADDR_CTL	0x40420820	Address control
SMIF0_DEVICE0_RD_CMD_CTL	0x40420840	Read command control
SMIF0_DEVICE0_RD_ADDR_CTL	0x40420844	Read address control
SMIF0_DEVICE0_RD_MODE_CTL	0x40420848	Read mode control
SMIF0_DEVICE0_RD_DUMMY_CTL	0x4042084C	Read dummy control
SMIF0_DEVICE0_RD_DATA_CTL	0x40420850	Read data control
SMIF0_DEVICE0_WR_CMD_CTL	0x40420860	Write command control
SMIF0_DEVICE0_WR_ADDR_CTL	0x40420864	Write address control
SMIF0_DEVICE0_WR_MODE_CTL	0x40420868	Write mode control
SMIF0_DEVICE0_WR_DUMMY_CTL	0x4042086C	Write dummy control
SMIF0_DEVICE0_WR_DATA_CTL	0x40420870	Write data control
SMIF0_DEVICE1_CTL	0x40420880	Control. See SMIF0_DEVICE0_CTL for the details of bit fields.
SMIF0_DEVICE1_ADDR	0x40420888	Device region base address. See SMIF0_DEVICE0_ADDR for the details of bit fields.
SMIF0_DEVICE1_MASK	0x4042088C	Device region mask. See SMIF0_DEVICE0_MASK for the details of bit fields.
SMIF0_DEVICE1_ADDR_CTL	0x404208A0	Address control. See SMIF0_DEVICE0_ADDR_CTL for the details of bit fields.
SMIF0_DEVICE1_RD_CMD_CTL	0x404208C0	Read command control. See SMIF0_DEVICE0_RD_CMD_CTL for the details of bit fields.
SMIF0_DEVICE1_RD_ADDR_CTL	0x404208C4	Read address control. See SMIF0_DEVICE0_RD_ADDR_CTL for the details of bit fields.
SMIF0_DEVICE1_RD_MODE_CTL	0x404208C8	Read mode control. See SMIF0_DEVICE0_RD_MODE_CTL for the details of bit fields.
SMIF0_DEVICE1_RD_DUMMY_CTL	0x404208CC	Read dummy control. See SMIF0_DEVICE0_RD_DUMMY_CTL for the details of bit fields.
SMIF0_DEVICE1_RD_DATA_CTL	0x404208D0	Read data control. See SMIF0_DEVICE0_RD_DATA_CTL for the details of bit fields.
SMIF0_DEVICE1_WR_CMD_CTL	0x404208E0	Write command control. See SMIF0_DEVICE0_WR_CMD_CTL for the details of bit fields.
SMIF0_DEVICE1_WR_ADDR_CTL	0x404208E4	Write address control. See SMIF0_DEVICE0_WR_ADDR_CTL for the details of bit fields.
SMIF0_DEVICE1_WR_MODE_CTL	0x404208E8	Write mode control. See SMIF0_DEVICE0_WR_MODE_CTL for the details of bit fields.
SMIF0_DEVICE1_WR_DUMMY_CTL	0x404208EC	Write dummy control. See SMIF0_DEVICE0_WR_DUMMY_CTL for the details of bit fields.
SMIF0_DEVICE1_WR_DATA_CTL	0x404208F0	Write data control. See SMIF0_DEVICE0_WR_DATA_CTL for the details of bit fields.
SMIF0_DEVICE2_CTL	0x40420900	Control. See SMIF0_DEVICE0_CTL for the details of bit fields.
SMIF0_DEVICE2_ADDR	0x40420908	Device region base address. See SMIF0_DEVICE0_ADDR for the details of bit fields.
SMIF0_DEVICE2_MASK	0x4042090C	Device region mask. See SMIF0_DEVICE0_MASK for the details of bit fields.
SMIF0_DEVICE2_ADDR_CTL	0x40420920	Address control. See SMIF0_DEVICE0_ADDR_CTL for the details of bit fields.

Register	Address	Description
SMIF0_DEVICE2_RD_CMD_CTL	0x40420940	Read command control. See SMIF0_DEVICE0_RD_CMD_CTL for the details of bit fields.
SMIF0_DEVICE2_RD_ADDR_CTL	0x40420944	Read address control. See SMIF0_DEVICE0_RD_ADDR_CTL for the details of bit fields.
SMIF0_DEVICE2_RD_MODE_CTL	0x40420948	Read mode control. See SMIF0_DEVICE0_RD_MODE_CTL for the details of bit fields.
SMIF0_DEVICE2_RD_DUMMY_CTL	0x4042094C	Read dummy control. See SMIF0_DEVICE0_RD_DUMMY_CTL for the details of bit fields.
SMIF0_DEVICE2_RD_DATA_CTL	0x40420950	Read data control. See SMIF0_DEVICE0_RD_DATA_CTL for the details of bit fields.
SMIF0_DEVICE2_WR_CMD_CTL	0x40420960	Write command control. See SMIF0_DEVICE0_WR_CMD_CTL for the details of bit fields.
SMIF0_DEVICE2_WR_ADDR_CTL	0x40420964	Write address control. See SMIF0_DEVICE0_WR_ADDR_CTL for the details of bit fields.
SMIF0_DEVICE2_WR_MODE_CTL	0x40420968	Write mode control. See SMIF0_DEVICE0_WR_MODE_CTL for the details of bit fields.
SMIF0_DEVICE2_WR_DUMMY_CTL	0x4042096C	Write dummy control. See SMIF0_DEVICE0_WR_DUMMY_CTL for the details of bit fields.
SMIF0_DEVICE2_WR_DATA_CTL	0x40420970	Write data control. See SMIF0_DEVICE0_WR_DATA_CTL for the details of bit fields.

21.1.1 SMIF0_CTL

Control

Address: 0x40420000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							XIP_MODE

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None			
HW Access	None		R		None			
Name	None [15:14]		CLOCK_IF_RX_SEL [13:12]		None [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					R		
Name	None [23:19]					DESELECT_DELAY [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						RW
HW Access	R	None						R
Name	ENABLED	None [30:25]						BLOCK

Bits	Name	Description
31	ENABLED	IP enable: '0': Disabled. All non-retention registers are reset to their default value when the IP is disabled. When the IP is disabled, the XIP accesses produce AHB-Lite bus errors. '1': Enabled. Note: Before disabling the IP, SW should ensure that the IP is NOT busy (STATUS.BUSY is '0'), otherwise illegal interface transfers may occur. Default Value: 0 **0x0: DISABLED :** **0x1: ENABLED :**
24	BLOCK	Specifies what happens for MMIO interface read accesses to an empty RX data FIFO or to a full TX format/data FIFO. Note: the FIFOs can only be accessed in MMIO_MODE. This field is not used for test controller accesses. Default Value: 0

21.1.1 SMIF0_CTL (continued)

0x0: BUS_ERROR :

0': Generate an AHB-Lite bus error. This option is useful when SW decides to use polling on STATUS.TR_BUSY to determine if a interface transfer is no longer busy (transfer is completed). This option adds SW complexity, but limits the number of AHB-Lite wait states (and limits ISR latency).

0x1: WAIT_STATES :

1': Introduce wait states. This setting potentially locks up the AHB-Lite infrastructure and may increase the CPU interrupt latency.This option is useful when SW performs TX/RX data FIFO accesses immediately after a command is setup using the TX format FIFO. This option has low SW complexity, but may result in a significant number of AHB-Lite wait states (and may increase ISR latency).

18 : 16	DESELECT_DELAY	Specifies the minimum duration of SPI deselection ("spi_select_out[]" is high/'1') in between SPI transfers: "0": 1 interface clock cycle. "1": 2 interface clock cycles. "2": 3 interface clock cycles. "3": 4 interface clock cycles. "4": 5 interface clock cycles. "5": 6 interface clock cycles. "6": 7 interface clock cycles. "7": 8 interface clock cycles. During SPI deselection, "spi_select_out[]" are '1'/inactive, "spi_data_out[]" are '1' and "spi_clk_out" is '0'/inactive. Default Value: 0
13 : 12	CLOCK_IF_RX_SEL	Specifies device interface receiver clock "clk_if_rx" source. MISO data is captured on the rising edge of "clk_if_rx". "0": "spi_clk_out" (internal clock) "1": !"spi_clk_out" (internal clock) "2": "spi_clk_in" (feedback clock) "3": !"spi_clk_in" (feedback clock) Note: the device interface transmitter clock "clk_if_tx" is fixed and is "spi_clk_out" MOSI data is driven on the falling edge of "clk_if_tx". Default Value: 3
0	XIP_MODE	Mode of operation. Note: this field should only be changed when the IP is disabled or when STATUS.BUSY is '0' and SW should not be executing from the XIP interface or MMIO interface. Default Value: 0

0x0: MMIO_MODE :

'0': MMIO mode. Individual MMIO accesses to TX and RX FIFOs are used to generate a sequence of SPI transfers. This mode of operation allows for large flexibility in terms of the SPI transfers that can be generated.

0x1: XIP_MODE :

1': XIP mode. eXecute-In-Place mode: incoming read and write transfers over the AHB-Lite bus infrastructure are automatically translated in SPI transfers to read data from and write data to a device. This mode of operation allow for efficient device read and write operations. This mode is only supported in SPI_MODE.

21.1.2 SMIF0_STATUS

Status

Address: 0x40420004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	BUSY	None						

Bits	Name	Description
31	BUSY	Cache, cryptography, XIP, device interface or any other logic busy in the IP: '0': not busy '1': busy When BUSY is '0', the IP can be safely disabled without: - the potential loss of transient write data. - the potential risk of aborting an inflight SPI device interface transfer. When BUSY is '0', the mode of operation (XIP_MODE or MMIO_MODE) can be safely changed. Default Value: 0

21.1.3 SMIF0_TX_CMD_FIFO_STATUS

Transmitter command FIFO status

Address: 0x40420044

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R		
HW Access	None					W		
Name	None [7:3]					USED3 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	USED3	Number of entries that are used in the TX command FIFO (available in both XIP_MODE and MMIO_MODE). Legal range: [0, 4]. Default Value: 0

21.1.4 SMIF0_TX_CMD_FIFO_WR

Transmitter command FIFO write

Address: 0x40420050

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA20 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA20 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				W			
HW Access	None				R			
Name	None [23:20]				DATA20 [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description

21.1.4 SMIF0_TX_CMD_FIFO_WR (continued)

19 : 0	DATA20	Command data. The higher two bits DATA[19:18] specify the specific command "0"/TX: A SPI transfer always start with a TX command FIFO entry of the "TX" format. - DATA[17:16] specifies the width of the data transfer: - "0": 1 bit/cycle (single data transfer). - "1": 2 bits/cycle (dual data transfer). - "2": 4 bits/cycle (quad data transfer). - "3": 8 bits/cycle (octal data transfer). - DATA[15]: specifies whether this is the last TX Byte; i.e. whether the "spi_select_out[3:0]" IO output signals are de-activated after the transfer. - DATA[11:8] specifies which of the four devices are selected. DATA[11:8] are directly mapped to "spi_select_out[3:0]". Two devices can be selected at the same time in dual-quad mode. - '0': device deselected - '1': device selected - DATA[7:0] specifies the transmitted Byte. "1"/TX_COUNT: The "TX_COUNT" command relies on the TX data FIFO to provide the transmitted bytes. The "TX_COUNT" command is ALWAYS considered to be the last command of a SPI data transfers. - DATA[17:16] specifies the width of the transfer. - DATA[15:0] specifies the number of to be transmitted Bytes (minus 1) from the TX data FIFO. "2"/RX_COUNT: The "RX_COUNT" command relies on the RX data FIFO to accept the received bytes. The "RX_COUNT" command is ALWAYS considered to be the last command of a SPI data transfers. - DATA[17:16] specifies the width of the transfer. - DATA[15:0] specifies the number of to be transmitted Bytes (minus 1) to the RX data FIFO. "3"/DUMMY_COUNT: The "DUMMY_COUNT" command conveys dummy cycles. Dummy cycles are used to implement a Turn-Around time in which the SPI master changes from a transmitter driving the data lines to a receiver receiving on the same data lines. The "DUMMY_COUNT" command is ALWAYS considered to be NOT the last command of a SPI data transfers; i.e. it needs to be followed by another command. - DATA[15:0] specifies the number of dummy cycles (minus 1). In dummy cycles, the data lines are not driven. Default Value: 0

21.1.5 SMIF0_TX_DATA_FIFO_CTL

Transmitter data FIFO control

Address: 0x40420080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					TRIGGER_LEVEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	TRIGGER_LEVEL	Determines when the TX data FIFO "tr_tx_req" trigger is activated (trigger activation requires MMIO_MODE, the trigger is NOT activated in XIP_MODE): - Trigger is active when TX_DATA_FIFO_STATUS.USED <= TRIGGER_LEVEL. Default Value: 0

21.1.6 SMIF0_TX_DATA_FIFO_STATUS

Transmitter data FIFO status

Address: 0x40420084

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				USED4 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	USED4	Number of entries that are used in the TX data FIFO (available in both XIP_MODE and MMIO_-MODE). Legal range: [0, 8]. Default Value: 0

21.1.7 SMIF0_TX_DATA_FIFO_WR1

Transmitter data FIFO write

Address: 0x40420090

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA0	TX data (written to TX data FIFO). Default Value: 0

21.1.8 SMIF0_TX_DATA_FIFO_WR2

Transmitter data FIFO write

Address: 0x40420094

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	DATA1	TX data (written to TX data FIFO, second byte). Default Value: 0
7 : 0	DATA0	TX data (written to TX data FIFO, first byte). Default Value: 0

21.1.9 SMIF0_TX_DATA_FIFO_WR4

Transmitter data FIFO write

Address: 0x40420098

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	DATA2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	DATA3 [31:24]							

Bits	Name	Description
31 : 24	DATA3	TX data (written to TX data FIFO, fourth byte). Default Value: 0
23 : 16	DATA2	TX data (written to TX data FIFO, third byte). Default Value: 0
15 : 8	DATA1	TX data (written to TX data FIFO, second byte). Default Value: 0
7 : 0	DATA0	TX data (written to TX data FIFO, first byte). Default Value: 0

21.1.10 SMIF0_RX_DATA_FIFO_CTL

Receiver data FIFO control

Address: 0x404200C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					TRIGGER_LEVEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	TRIGGER_LEVEL	Determines when RX data FIFO "tr_rx_req" trigger is activated (trigger activation requires MMIO_MODE, the trigger is NOT activated in XIP_MODE): - Trigger is active when RX_DATA_FIFO_STATUS.USED > TRIGGER_LEVEL. Default Value: 0

21.1.11 SMIF0_RX_DATA_FIFO_STATUS

Receiver data FIFO status

Address: 0x404200C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				USED4 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	USED4	Number of entries that are used in the RX data FIFO (available in both XIP_MODE and MMIO_-MODE). Legal range: [0, 8]. Default Value: 0

21.1.12 SMIF0_RX_DATA_FIFO_RD1

Receiver data FIFO read

Address: 0x404200D0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA0	RX data (read from RX data FIFO). Default Value: 0

21.1.13 SMIF0_RX_DATA_FIFO_RD2

Receiver data FIFO read

Address: 0x404200D4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	DATA1	RX data (read from RX data FIFO, second byte). Default Value: 0
7 : 0	DATA0	RX data (read from RX data FIFO, first byte). Default Value: 0

21.1.14 SMIF0_RX_DATA_FIFO_RD4

Receiver data FIFO read

Address: 0x404200D8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA3 [31:24]							

Bits	Name	Description
31 : 24	DATA3	RX data (read from RX data FIFO, fourth byte). Default Value: 0
23 : 16	DATA2	RX data (read from RX data FIFO, third byte). Default Value: 0
15 : 8	DATA1	RX data (read from RX data FIFO, second byte). Default Value: 0
7 : 0	DATA0	RX data (read from RX data FIFO, first byte). Default Value: 0

21.1.15 SMIF0_RX_DATA_FIFO_RD1_SILENT

Receiver data FIFO silent read

Address: 0x404200E0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA0	RX data (read from RX data FIFO). Default Value: 0

21.1.16 SMIF0_SLOW_CA_CTL

Slow cache control

Address: 0x40420100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						WAY [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None				RW	
HW Access	R	R	None				R	
Name	ENABLED	PREF_EN	None [29:26]				SET_ADDR [25:24]	

Bits	Name	Description
31	ENABLED	Cache enable: '0': Disabled. '1': Enabled. Default Value: 1
30	PREF_EN	Prefetch enable: '0': Disabled. '1': Enabled. Prefetching requires the cache to be enabled; i.e. ENABLED is '1'. Default Value: 1
25 : 24	SET_ADDR	this is for debug purpose only, and should be hidden to customers in technical document Default Value: 0
17 : 16	WAY	this is for debug purpose only, and should be hidden to customers in technical document Default Value: 0

21.1.17 SMIF0_SLOW_CA_CMD

Slow cache command

Address: 0x40420108

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							INV

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	INV	Cache and prefetch buffer invalidation. SW writes a '1' to clear the cache and prefetch buffer. The cache's LRU structure is also reset to its default state. Note, A write access will invalidate the prefetch buffer automatically in hardware. A write access should invalidate both fast and slow caches, by firmware. Note, firmware should invalidate the cache and prefetch buffer only when STATUS.BUSY is '0'. Default Value: 0

21.1.18 SMIF0_FAST_CA_CTL

Fast cache control

Address: 0x40420180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						WAY [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None				RW	
HW Access	R	R	None				R	
Name	ENABLED	PREF_EN	None [29:26]				SET_ADDR [25:24]	

Bits	Name	Description
31	ENABLED	See SLOW_CA_CTL.ENABLED. Default Value: 1
30	PREF_EN	See SLOW_CA_CTL.PREF_EN. Default Value: 1
25 : 24	SET_ADDR	this is for debug purpose only, and should be hidden to customers in technical document Default Value: 0
17 : 16	WAY	this is for debug purpose only, and should be hidden to customers in technical document Default Value: 0

21.1.19 SMIF0_FAST_CA_CMD

Fast cache command

Address: 0x40420188

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							INV

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	INV	See SLOW_CA_CMD.INV. Default Value: 0

21.1.20 SMIF0_CRYPTO_CMD

Cryptography Command

Address: 0x40420200

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							START

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	START	SW sets this field to '1' to start a AES-128 forward block cipher operation (on the address in CRYPTO_ADDR). HW sets this field to '0' to indicate that the operation has completed. Once completed, the result of the operation can be read from CRYPTO_RESULT0, ..., CRYPTO_RESULT3. The operation takes roughly 13 clk_hf clock cycles. Note: An operation can only be started in MMIO_MODE. Default Value: 0

21.1.21 SMIF0_CRYPTO_INPUT0

Cryptography input 0

Address: 0x40420220

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	INPUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INPUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INPUT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	INPUT [31:24]							

Bits	Name	Description
31 : 0	INPUT	Four Bytes of the plaintext PT[31:0] = CRYPTO_INPUT0.INPUT[31:0]. Default Value: Undefined

21.1.22 SMIF0_CRYPTO_INPUT1

Cryptography input 1

Address: 0x40420224

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	INPUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INPUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INPUT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	INPUT [31:24]							

Bits	Name	Description
31 : 0	INPUT	Four Bytes of the plaintext PT[63:32] = CRYPTO_INPUT1.INPUT[31:0]. Default Value: Undefined

21.1.23 SMIF0_CRYPTO_INPUT2

Cryptography input 2

Address: 0x40420228

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	INPUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INPUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INPUT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	INPUT [31:24]							

Bits	Name	Description
31 : 0	INPUT	Four Bytes of the plaintext PT[95:64] = CRYPTO_INPUT2.INPUT[31:0]. Default Value: Undefined

21.1.24 SMIF0_CRYPTO_INPUT3

Cryptography input 3

Address: 0x4042022C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	INPUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INPUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INPUT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	INPUT [31:24]							

Bits	Name	Description
31 : 0	INPUT	Four Bytes of the plaintext PT[127:96] = CRYPTO_INPUT3.INPUT[31:0]. Default Value: Undefined

21.1.25 SMIF0_CRYPTO_KEY0

Cryptography key 0

Address: 0x40420240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	KEY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	KEY [31:24]							

Bits	Name	Description
31 : 0	KEY	Four Bytes of the key KEY[31:0] = CRYPTO_KEY0.KEY[31:0]. Default Value: Undefined

21.1.26 SMIF0_CRYPTO_KEY1

Cryptography key 1

Address: 0x40420244

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	KEY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	KEY [31:24]							

Bits	Name	Description
31 : 0	KEY	Four Bytes of the key KEY[63:32] = CRYPTO_KEY1.KEY[31:0]. Default Value: Undefined

21.1.27 SMIF0_CRYPTO_KEY2

Cryptography key 2

Address: 0x40420248

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	KEY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	KEY [31:24]							

Bits	Name	Description
31 : 0	KEY	Four Bytes of the key KEY[95:64] = CRYPTO_KEY2.KEY[31:0]. Default Value: Undefined

21.1.28 SMIF0_CRYPTO_KEY3

Cryptography key 3

Address: 0x4042024C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	KEY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	KEY [31:24]							

Bits	Name	Description
31 : 0	KEY	Four Bytes of the key KEY[127:96] = CRYPTO_KEY3.KEY[31:0]. Default Value: Undefined

21.1.29 SMIF0_CRYPTO_OUTPUT0

Cryptography output 0

Address: 0x40420260

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	OUTPUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	OUTPUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	OUTPUT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	OUTPUT [31:24]							

Bits	Name	Description
31 : 0	OUTPUT	Four Bytes of the ciphertext CT[31:0] = CRYPTO_OUTPUT0.OUTPUT[31:0]. Default Value: Undefined

21.1.30 SMIF0_CRYPTO_OUTPUT1

Cryptography output 1

Address: 0x40420264

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	OUTPUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	OUTPUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	OUTPUT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	OUTPUT [31:24]							

Bits	Name	Description
31 : 0	OUTPUT	Four Bytes of the ciphertext CT[63:32] = CRYPTO_OUTPUT1.OUTPUT[31:0]. Default Value: Undefined

21.1.31 SMIF0_CRYPTO_OUTPUT2

Cryptography output 2

Address: 0x40420268

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	OUTPUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	OUTPUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	OUTPUT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	OUTPUT [31:24]							

Bits	Name	Description
31 : 0	OUTPUT	Four Bytes of the ciphertext CT[95:64] = CRYPTO_OUTPUT2.OUTPUT[31:0]. Default Value: Undefined

21.1.32 SMIF0_CRYPTO_OUTPUT3

Cryptography output 3

Address: 0x4042026C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	OUTPUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	OUTPUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	OUTPUT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	OUTPUT [31:24]							

Bits	Name	Description
31 : 0	OUTPUT	Four Bytes of the ciphertext CT[127:96] = CRYPTO_OUTPUT3.OUTPUT[31:0]. Default Value: Undefined

21.1.33 SMIF0_INTR

Interrupt register

Address: 0x404207C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None		RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	None [7:6]		RX_DATA_FIFO_UNDERFLOW	TX_DATA_FIFO_OVERFLOW	TX_CMD_FIFO_OVERFLOW	XIP_ALIGNMENT_ERROR	TR_RX_REQ	TR_TX_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	RX_DATA_FIFO_UNDERFLOW	Activated in MMIO mode, on an AHB-Lite read transfer from the RX data FIFO (RX_DATA_FIFO_RD1, RX_DATA_FIFO_RD2, RX_DATA_FIFO_RD4) with not enough entries available. Only activated for NON test bus controller transfers. Default Value: 0
4	TX_DATA_FIFO_OVERFLOW	Activated in MMIO mode, on an AHB-Lite write transfer to the TX data FIFO (TX_DATA_FIFO_WR1, TX_DATA_FIFO_WR2, TX_DATA_FIFO_WR4) with not enough free entries available. Default Value: 0
3	TX_CMD_FIFO_OVERFLOW	Activated in MMIO mode, on an AHB-Lite write transfer to the TX command FIFO (TX_CMD_FIFO_WR) with not enough free entries available. Default Value: 0

21.1.33 SMIF0_INTR (continued)

2	XIP_ALIGNMENT_ERROR	Activated in XIP mode, if: - The selected device's ADDR_CTL.DIV2 is '1' and the AHB-Lite bus transfer address is not a multiple of 2. - The selected device's ADDR_CTL.DIV2 is '1' and the XIP transfer request is NOT for a multiple of 2 Bytes. Note: In dual-quad SPI mode (ADDR_CTL.DIV is '1'), each memory device contributes a 4-bit nibble for read data or write data. This is only possible if the request address is a multiple of 2 and the number of requested Bytes is a multiple of 2. Default Value: 0
1	TR_RX_REQ	Activated in MMIO mode, when a RX data FIFO trigger "tr_rx_req" is activated. Default Value: 0
0	TR_TX_REQ	Activated in MMIO mode, when a TX data FIFO trigger "tr_tx_req" is activated. Default Value: 0

21.1.34 SMIF0_INTR_SET

Interrupt set register

Address: 0x404207C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	None		A	A	A	A	A	A
Name	None [7:6]		RX_DATA_FIFO_UNDERFLOW	TX_DATA_FIFO_OVERFLOW	TX_CMD_FIFO_OVERFLOW	XIP_ALIGNMENT_ERROR	TR_RX_REQ	TR_TX_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	RX_DATA_FIFO_UNDERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	TX_DATA_FIFO_OVERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	TX_CMD_FIFO_OVERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	XIP_ALIGNMENT_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	TR_RX_REQ	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TR_TX_REQ	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

21.1.35 SMIF0_INTR_MASK

Interrupt mask register

Address: 0x404207C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		RX_DATA_FIFO_UNDERFLOW	TX_DATA_FIFO_OVERFLOW	TX_CMD_FIFO_OVERFLOW	XIP_ALIGNMENT_ERROR	TR_RX_REQ	TR_TX_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	RX_DATA_FIFO_UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	TX_DATA_FIFO_OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	TX_CMD_FIFO_OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	XIP_ALIGNMENT_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	TR_RX_REQ	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TR_TX_REQ	Mask bit for corresponding bit in interrupt request register. Default Value: 0

21.1.36 SMIF0_INTR_MASKED

Interrupt masked register

Address: 0x404207CC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		RX_DATA_FIFO_UNDERFLOW	TX_DATA_FIFO_OVERFLOW	TX_CMD_FIFO_OVERFLOW	XIP_ALIGNMENT_ERROR	TR_RX_REQ	TR_TX_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	RX_DATA_FIFO_UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
4	TX_DATA_FIFO_OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
3	TX_CMD_FIFO_OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
2	XIP_ALIGNMENT_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
1	TR_RX_REQ	Logical and of corresponding request and mask bits. Default Value: 0
0	TR_TX_REQ	Logical and of corresponding request and mask bits. Default Value: 0

21.1.37 SMIF0_DEVICE0_CTL

Control

Address: 0x40420800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							WR_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							CRYP-TO_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						DATA_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	Device enable: '0': Disabled. '1': Enabled. Default Value: 0
17 : 16	DATA_SEL	Specifies the connection of the IP's data lines (spi_data[0], ..., spi_data[7]) to the device's data lines (SI/IO0, SO/IO1, IO2, IO3, IO4, IO5, IO6, IO7): "0": spi_data[0] = IO0, spi_data[1] = IO1, ..., spi_data[7] = IO7. This value is allowed for single, dual, quad, dual quad and octal SPI modes. This value must be used for the first device in dual quad SPI mode. This value must be used for octal SPI mode. "1": spi_data[2] = IO0, spi_data[3] = IO1. This value is only allowed for single and dual SPI modes. "2": spi_data[4] = IO0, spi_data[5] = IO1, ..., spi_data[7] = IO3. This value is only allowed for single, dual, quad and dual quad SPI modes. In dual quad SPI mode, this value must be used for the second device. "3": spi_data[6] = IO0, spi_data[7] = IO1. This value is only allowed for single and dual SPI modes. Default Value: 0

21.1.37 SMIF0_DEVICE0_CTL (continued)

8	CRYPTO_EN	Cryptography on read/write accesses: '0': disabled. '1': enabled. Default Value: 0
0	WR_EN	Write enable: '0': write transfers are not allowed to this device. An attempt to write to this device results in an AHB-Lite bus error. '1': write transfers are allowed to this device. Default Value: 0

21.1.38 SMIF0_DEVICE0_ADDR

Device region base address

Address: 0x40420808

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 8	ADDR	Specifies the base address of the device region. If the device region is 2^m Bytes, ADDR MUST be a multiple of 2^m. In dual quad SPI data transfer, the two devices should have the same ADDR and MASK register settings. The device control information (ADDR_CTL, RD_CMD_CTL, etc.) are provided by the MMIO control registers of the device with the lowest index. The most significant bit fields are constants and set based on the SMIF_XIP_ADDR parameter. The most significant bits are identified on the SMIF_XIP_MASK parameter. E.g., if SMIF_XIP_MASK is 0xff00:0000 (16 MB XIP memory region), ADDR[31:24] = SMIF_XIP_ADDR[31:24]. Default Value: Undefined

21.1.39 SMIF0_DEVICE0_MASK

Device region mask

Address: 0x4042080C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	MASK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	MASK [31:24]							

Bits	Name	Description
31 : 8	MASK	Specifies the size of the device region. All '1' bits are used to compare the incoming transfer request address A[31:0] with the address as specified in ADDR.ADDR: Address A is in the device when (A[31:8] & MASK[31:8]) == ADDR.ADDR[31:8]. The most significant bit fields are constants and set to'1'. The most significant bits are identified on the SMIF_XIP_MASK parameter. E.g., if SMIF_XIP_MASK is 0xff00:0000 (16 MB XIP memory region), MASK[31:24] = 0xff. Note: a transfer request that is not in any device region results in an AHB-Lite bus error. Default Value: Undefined

21.1.40 SMIF0_DEVICE0_ADDR_CTL

Address control

Address: 0x40420820

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						SIZE2 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							DIV2

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	DIV2	Specifies if the AHB-Lite bus transfer address is divided by 2 or not: '0': No divide by 2. '1': Divide by 2. This functionality is used for read and write operation in XIP, dual quad SPI mode; i.e. this DIV2 must be set to '1' in dual quad SPI mode. If the transfer request address is NOT a multiple of 2 or the requested number of Bytes is not a multiple of 2, the XIP_ALIGNMENT_ERROR interrupt cause is activated. Default Value: 0
1 : 0	SIZE2	Specifies the size of the XIP device address in Bytes: "0": 1 Byte address. "1": 2 Byte address. "2": 3 Byte address. "3": 4 Byte address. The lower significant address Bytes of the transfer request are used as XIP address to the external device. Note that for dual quad SPI data transfer, the transfer request address is divided by 2. Therefore, the transfer request address needs to be a multiple of 2. If the trasnfer requestaddress is NOT a multiple of 2, the XIP_ALIGNMENT_ERROR interrupt cause is activated. Default Value: 0

21.1.41 SMIF0_DEVICE0_RD_CMD_CTL

Read command control

Address: 0x40420840

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CODE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						WIDTH [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	PRESENT	None [30:24]						

Bits	Name	Description
31	PRESENT	Presence of command field: '0': not present '1': present Default Value: 0
17 : 16	WIDTH	Width of data transfer: "0": 1 bit/cycle (single data transfer). "1": 2 bits/cycle (dual data transfer). "2": 4 bits/cycle (quad data transfer). "3": 8 bits/cycle (octal data transfer). Default Value: 0
7 : 0	CODE	Command byte code. Default Value: 0

21.1.42 SMIF0_DEVICE0_RD_ADDR_CTL

Read address control

Address: 0x40420844

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						WIDTH [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 16	WIDTH	Width of transfer. Default Value: 0

21.1.43 SMIF0_DEVICE0_RD_MODE_CTL

Read mode control

Address: 0x40420848

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CODE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						WIDTH [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	PRESENT	None [30:24]						

Bits	Name	Description
31	PRESENT	Presence of mode field: '0': not present '1': present Default Value: 0
17 : 16	WIDTH	Width of transfer. Default Value: 0
7 : 0	CODE	Mode byte code. Default Value: 0

21.1.44 SMIF0_DEVICE0_RD_DUMMY_CTL

Read dummy control

Address: 0x4042084C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			SIZE5 [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	PRESENT	None [30:24]						

Bits	Name	Description
31	PRESENT	Presence of dummy cycles: '0': not present '1': present Default Value: 0
4 : 0	SIZE5	Number of dummy cycles (minus 1): "0": 1 cycles ... "31": 32 cycles. Note: this field specifies dummy cycles, not dummy Bytes! Default Value: 0

21.1.45 SMIF0_DEVICE0_RD_DATA_CTL

Read data control

Address: 0x40420850

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						WIDTH [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 16	WIDTH	Width of transfer. Default Value: 0

21.1.46 SMIF0_DEVICE0_WR_CMD_CTL

Write command control

Address: 0x40420860

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CODE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						WIDTH [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	PRESENT	None [30:24]						

Bits	Name	Description
31	PRESENT	Presence of command field: '0': not present '1': present Default Value: 0
17 : 16	WIDTH	Width of transfer. Default Value: 0
7 : 0	CODE	Command byte code. Default Value: 0

21.1.47 SMIF0_DEVICE0_WR_ADDR_CTL

Write address control

Address: 0x40420864

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						WIDTH [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 16	WIDTH	Width of transfer. Default Value: 0

21.1.48 SMIF0_DEVICE0_WR_MODE_CTL

Write mode control

Address: 0x40420868

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CODE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						WIDTH [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	PRESENT	None [30:24]						

Bits	Name	Description
31	PRESENT	Presence of mode field: '0': not present '1': present Default Value: 0
17 : 16	WIDTH	Width of transfer. Default Value: 0
7 : 0	CODE	Mode byte code. Default Value: 0

21.1.49 SMIF0_DEVICE0_WR_DUMMY_CTL

Write dummy control

Address: 0x4042086C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			SIZE5 [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	PRESENT	None [30:24]						

Bits	Name	Description
31	PRESENT	Presence of dummy cycles: '0': not present '1': present Default Value: 0
4 : 0	SIZE5	Number of dummy cycles (minus 1): "0": 1 cycles ... "31": 32 cycles. Default Value: 0

21.1.50 SMIF0_DEVICE0_WR_DATA_CTL

Write data control

Address: 0x40420870

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						WIDTH [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 16	WIDTH	Width of transfer. Default Value: 0

Section G: Peripheral Group 5

This section encompasses the following chapters:

- CAN FD Controller chapter on page 1649

22 CAN FD Controller

This section discusses the CAN FD Controller (CANFD) registers. It lists all the registers in mapping tables, in address order.

22.1 Register Details

Register	Address	Description
CANFD0_CH0_CREL	0x40520000	Core Release Register
CANFD0_CH0_ENDN	0x40520004	Endian Register
CANFD0_CH0_DBTP	0x4052000C	Data Bit Timing & Prescaler Register
CANFD0_CH0_TEST	0x40520010	Test Register
CANFD0_CH0_RWD	0x40520014	RAM Watchdog
CANFD0_CH0_CCCR	0x40520018	CC Control Register
CANFD0_CH0_NBTP	0x4052001C	Nominal Bit Timing & Prescaler Register
CANFD0_CH0_TSCC	0x40520020	Timestamp Counter Configuration
CANFD0_CH0_TSCV	0x40520024	Timestamp Counter Value
CANFD0_CH0_TOCC	0x40520028	Timeout Counter Configuration
CANFD0_CH0_TOCV	0x4052002C	Timeout Counter Value
CANFD0_CH0_ECR	0x40520040	Error Counter Register
CANFD0_CH0_PSR	0x40520044	Protocol Status Register
CANFD0_CH0_TDCR	0x40520048	Transmitter Delay Compensation Register
CANFD0_CH0_IR	0x40520050	Interrupt Register
CANFD0_CH0_IE	0x40520054	Interrupt Enable
CANFD0_CH0_ILS	0x40520058	Interrupt Line Select
CANFD0_CH0_ILE	0x4052005C	Interrupt Line Enable
CANFD0_CH0_GFC	0x40520080	Global Filter Configuration
CANFD0_CH0_SIDFC	0x40520084	Standard ID Filter Configuration
CANFD0_CH0_XIDFC	0x40520088	Extended ID Filter Configuration
CANFD0_CH0_XIDAM	0x40520090	Extended ID AND Mask
CANFD0_CH0_HPMS	0x40520094	High Priority Message Status
CANFD0_CH0_NDAT1	0x40520098	New Data 1
CANFD0_CH0_NDAT2	0x4052009C	New Data 2
CANFD0_CH0_RXF0C	0x405200A0	Rx FIFO 0 Configuration
CANFD0_CH0_RXF0S	0x405200A4	Rx FIFO 0 Status

Register	Address	Description
CANFD0_CH0_RXF0A	0x405200A8	Rx FIFO 0 Acknowledge
CANFD0_CH0_RXBC	0x405200AC	Rx Buffer Configuration
CANFD0_CH0_RXF1C	0x405200B0	Rx FIFO 1 Configuration
CANFD0_CH0_RXF1S	0x405200B4	Rx FIFO 1 Status
CANFD0_CH0_RXF1A	0x405200B8	Rx FIFO 1 Acknowledge
CANFD0_CH0_RXESC	0x405200BC	Rx Buffer / FIFO Element Size Configuration
CANFD0_CH0_TXBC	0x405200C0	Tx Buffer Configuration
CANFD0_CH0_TXFQS	0x405200C4	Tx FIFO/Queue Status
CANFD0_CH0_TXESC	0x405200C8	Tx Buffer Element Size Configuration
CANFD0_CH0_TXBRP	0x405200CC	Tx Buffer Request Pending
CANFD0_CH0_TXBAR	0x405200D0	Tx Buffer Add Request
CANFD0_CH0_TXBCR	0x405200D4	Tx Buffer Cancellation Request
CANFD0_CH0_TXBTO	0x405200D8	Tx Buffer Transmission Occurred
CANFD0_CH0_TXBCF	0x405200DC	Tx Buffer Cancellation Finished
CANFD0_CH0_TXBTIE	0x405200E0	Tx Buffer Transmission Interrupt Enable
CANFD0_CH0_TXBCIE	0x405200E4	Tx Buffer Cancellation Finished Interrupt Enable
CANFD0_CH0_TXEFC	0x405200F0	Tx Event FIFO Configuration
CANFD0_CH0_TXEFS	0x405200F4	Tx Event FIFO Status
CANFD0_CH0_TXEFA	0x405200F8	Tx Event FIFO Acknowledge
CANFD0_CH0_TTTMC	0x40520100	TT Trigger Memory Configuration
CANFD0_CH0_TTRMC	0x40520104	TT Reference Message Configuration
CANFD0_CH0_TTOCF	0x40520108	TT Operation Configuration
CANFD0_CH0_TTMLM	0x4052010C	TT Matrix Limits
CANFD0_CH0_TURCF	0x40520110	TUR Configuration
CANFD0_CH0_TTOCN	0x40520114	TT Operation Control
CANFD0_CH0_TTGTP	0x40520118	TT Global Time Preset
CANFD0_CH0_TTTMK	0x4052011C	TT Time Mark
CANFD0_CH0_TTIR	0x40520120	TT Interrupt Register
CANFD0_CH0_TTIE	0x40520124	TT Interrupt Enable
CANFD0_CH0_TTILS	0x40520128	TT Interrupt Line Select
CANFD0_CH0_TTOST	0x4052012C	TT Operation Status
CANFD0_CH0_TURNA	0x40520130	TUR Numerator Actual
CANFD0_CH0_TTLGT	0x40520134	TT Local & Global Time
CANFD0_CH0_TTCTC	0x40520138	TT Cycle Time & Count
CANFD0_CH0_TTCPT	0x4052013C	TT Capture Time
CANFD0_CH0_TTCSM	0x40520140	TT Cycle Sync Mark
CANFD0_CH0_RXFTOP_CTL	0x40520180	Receive FIFO Top control
CANFD0_CH0_RXFTOP0_STAT	0x405201A0	Receive FIFO 0 Top Status
CANFD0_CH0_RXFTOP0_DATA	0x405201A8	Receive FIFO 0 Top Data
CANFD0_CH0_RXFTOP1_STAT	0x405201B0	Receive FIFO 1 Top Status
CANFD0_CH0_RXFTOP1_DATA	0x405201B8	Receive FIFO 1 Top Data
CANFD0_CTL	0x40521000	Global CAN control register

Register	Address	Description
CANFD0_STATUS	0x40521004	Global CAN status register
CANFD0_INTR0_CAUSE	0x40521010	Consolidated interrupt0 cause register
CANFD0_INTR1_CAUSE	0x40521014	Consolidated interrupt1 cause register
CANFD0_TS_CTL	0x40521020	Time Stamp control register
CANFD0_TS_CNT	0x40521024	Time Stamp counter value

22.1.1 CANFD0_CH0_CREL

Core Release Register

Address: 0x40520000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	DAY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	MON [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access	R				R			
Name	SUBSTEP [23:20]				YEAR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R				R			
HW Access	R				R			
Name	REL [31:28]				STEP [27:24]			

Bits	Name	Description
31 : 28	REL	Core Release One digit, BCD-coded. Default Value: 0
27 : 24	STEP	Step of Core Release One digit, BCD-coded. Default Value: 0
23 : 20	SUBSTEP	Sub-step of Core Release One digit, BCD-coded. Default Value: 0
19 : 16	YEAR	Time Stamp Year One digit, BCD-coded. This field is set by generic parameter on M_TTCAN synthesis. Default Value: 0
15 : 8	MON	Time Stamp Month Two digits, BCD-coded. This field is set by generic parameter on M_TTCAN synthesis. Default Value: 0
7 : 0	DAY	Time Stamp Day Two digits, BCD-coded. This field is set by generic parameter on M_TTCAN synthesis. Default Value: 0

22.1.2 CANFD0_CH0_ENDN

Endian Register

Address: 0x40520004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	ETV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ETV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ETV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ETV [31:24]							

Bits	Name	Description
31 : 0	ETV	Endianness Test Value The endianness test value is 0x87654321. Default Value: 0x87654321

22.1.3 CANFD0_CH0_DBTP

Data Bit Timing & Prescaler Register

Address: 0x4052000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DTSEG2 [7:4]				DSJW [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			DTSEG1 [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None		RW				
HW Access	R	None		R				
Name	TDC	None [22:21]		DBRP [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	TDC	Transmitter Delay Compensation 0= Transmitter Delay Compensation disabled 1= Transmitter Delay Compensation enabled Default Value: 0
20 : 16	DBRP	Data Bit Rate Prescaler 0x00-0x1F The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Bit Rate Prescaler are 0 to 31. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Default Value: 0
12 : 8	DTSEG1	Data time segment before sample point 0x00-0x1F Valid values are 0 to 31. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Default Value: 0xA
7 : 4	DTSEG2	Data time segment after sample point 0x0-0xF Valid values are 0 to 15. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Default Value: 3

22.1.3 CANFD0_CH0_DBTP (continued)

3 : 0	DSJW	Data (Re)Synchronization Jump Width 0x0-0xF Valid values are 0 to 15. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Default Value: 3

22.1.4 CANFD0_CH0_TEST

Test Register

Address: 0x40520010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	RW		RW	RW	RW	RW	RW
HW Access	R	R		R	R	R	R	R
Name	RX	TX [6:5]		LBCK	CAT	CAM	TAT	TAM

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	RX	Receive Pin Monitors the actual value of pin m_ttcan_rx 0= The CAN bus is dominant (m_ttcan_rx = '0') 1= The CAN bus is recessive (m_ttcan_rx = '1') Default Value: Undefined
6 : 5	TX	Control of Transmit Pin 00 Reset value, m_ttcan_tx controlled by the CAN Core, updated at the end of the CAN bit time 01 Sample Point can be monitored at pin m_ttcan_tx 10 Dominant ('0') level at pin m_ttcan_tx 11 Recessive ('1') at pin m_ttcan_tx Default Value: 0
4	LBCK	Loop Back Mode 0= Reset value, Loop Back Mode is disabled 1= Loop Back Mode is enabled (see Section 3.1.9, Test Modes) Default Value: 0

22.1.4 CANFD0_CH0_TEST (continued)

3	CAT	ASC is not supported by M_TTCAN Check ASC Transmit Control Monitors level at output pin m_ttcan_asct. 0= Output pin m_ttcan_asct = '0' Default Value: 0
2	CAM	ASC is not supported by M_TTCAN Check ASC Multiplexer Control Monitors level at output pin m_ttcan_ascm. 0= Output pin m_ttcan_ascm = '0' 1= Output pin m_ttcan_ascm = '1' Default Value: 0
1	TAT	ASC is not supported by M_TTCAN Test ASC Transmit Control Controls output pin m_ttcan_asct in test mode, ORed with the signal from the FSE 0= Level at pin m_ttcan_asct controlled by FSE 1= Level at pin m_ttcan_asct = '1' Default Value: 0
0	TAM	ASC is not supported by M_TTCAN Test ASC Multiplexer Control Controls output pin m_ttcan_ascm in test mode, ORed with the signal from the FSE 0= Level at pin m_ttcan_ascm controlled by FSE 1= Level at pin m_ttcan_ascm = '1' Default Value: 0

22.1.5 CANFD0_CH0_RWD

RAM Watchdog

Address: 0x40520014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WDC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	WDV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	WDV	Watchdog Value Actual Message RAM Watchdog Counter Value. Default Value: 0
7 : 0	WDC	Watchdog Configuration Start value of the Message RAM Watchdog Counter. With the reset value of '00' the counter is disabled. Default Value: 0

22.1.6 CANFD0_CH0_CCCR

CC Control Register

Address: 0x40520018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	TEST	DAR	MON_	CSR	CSA	ASM	CCE	INIT

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	None		RW	RW
HW Access	R	R	R	R	None		R	R
Name	NISO	TXP	EFBI	PXHD	None [11:10]		BRSE	FDOE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	NISO	Non ISO Operation If this bit is set, the M_TTCAN uses the CAN FD frame format as specified by the Bosch CAN FD Specification V1.0. 0= CAN FD frame format according to ISO 11898-1:2015 1= CAN FD frame format according to Bosch CAN FD Specification V1.0 addressing the non-ISO CAN FD Default Value: 0
14	TXP	Transmit Pause If this bit is set, the M_TTCAN pauses for two CAN bit times before starting the next transmission after itself has successfully transmitted a frame (see Section 3.5). 0= Transmit pause disabled 1= Transmit pause enabled Default Value: 0
13	EFBI	Edge Filtering during Bus Integration 0= Edge filtering disabled 1= Two consecutive dominant tq required to detect an edge for hard synchronization Default Value: 0

22.1.6 CANFD0_CH0_CCCR (continued)

12	PXHD	Protocol Exception Handling Disable 0= Protocol exception handling enabled 1= Protocol exception handling disabled Default Value: 0
9	BRSE	Bit Rate Switch Enable 0= Bit rate switching for transmissions disabled 1= Bit rate switching for transmissions enabled Default Value: 0
8	FDOE	FD Operation Enable 0= FD operation disabled 1= FD operation enabled Default Value: 0
7	TEST	Test Mode Enable 0= Normal operation, register TEST holds reset values 1= Test Mode, write access to register TEST enabled Default Value: 0
6	DAR	Disable Automatic Retransmission 0= Automatic retransmission of messages not transmitted successfully enabled 1= Automatic retransmission disabled Default Value: 0
5	MON_	Bus Monitoring Mode Bit MON can only be set by the Host when both CCE and INIT are set to '1'. The bit can be reset by the Host at any time. 0= Bus Monitoring Mode is disabled 1= Bus Monitoring Mode is enabled Default Value: 0
4	CSR	Clock Stop Request, not supported by M_TTCAN use CTL.STOP_REQ at the group level instead. 0= No clock stop is requested 1= Clock stop requested. When clock stop is requested, first INIT and then CSA will be set after all pending transfer requests have been completed and the CAN bus reached idle. Default Value: 0
3	CSA	Clock Stop Acknowledge 0= No clock stop acknowledged 1= M_TTCAN may be set in power down by stopping m_ttcan_hclk and m_ttcan_cclk Default Value: 0
2	ASM	Restricted Operation Mode Bit ASM can only be set by the Host when both CCE and INIT are set to '1'. The bit can be reset by the Host at any time. For a description of the Restricted Operation Mode see Section 3.1.5. 0= Normal CAN operation 1= Restricted Operation Mode active Default Value: 0
1	CCE	Configuration Change Enable 0= The CPU has no write access to the protected configuration registers 1= The CPU has write access to the protected configuration registers (while CCCR.INIT = '1') Default Value: 0
0	INIT	Initialization 0= Normal Operation 1= Initialization is started Default Value: 1

22.1.7 CANFD0_CH0_NBTP

Nominal Bit Timing & Prescaler Register

Address: 0x4052001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	NTSEG2 [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	NTSEG1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	NBRP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							RW
HW Access	R							R
Name	NSJW [31:25]							NBRP

Bits	Name	Description
31 : 25	NSJW	Nominal (Re)Synchronization Jump Width 0x00-0x7F Valid values are 0 to 127. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Default Value: 3
24 : 16	NBRP	Nominal Bit Rate Prescaler 0x000-0x1FFThe value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Bit Rate Prescaler are 0 to 511. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Default Value: 0
15 : 8	NTSEG1	Nominal Time segment before sample point 0x01-0xFF Valid values are 1 to 255. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Default Value: 0xA
6 : 0	NTSEG2	Nominal Time segment after sample point 0x01-0x7F Valid values are 1 to 127. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Default Value: 3

22.1.8 CANFD0_CH0_TSCC

Timestamp Counter Configuration

Address: 0x40520020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						TSS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				TCP [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	TCP	Timestamp Counter Prescaler (still used for TOCC) 0x0-0xF Configures the timestamp and timeout counters time unit in multiples of CAN bit times [1...16]. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Default Value: 0
1 : 0	TSS	Timestamp Select, should always be set to external timestamp counter 00= Timestamp counter value always 0x0000 01= Timestamp counter value incremented according to TCP 10= External timestamp counter value used 11= Same as '00' Default Value: 0

22.1.9 CANFD0_CH0_TSCV

Timestamp Counter Value

Address: 0x40520024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TSC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TSC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	TSC	Timestamp Counter, not used for M_TTCAN The internal/external Timestamp Counter value is captured on start of frame (both Rx and Tx). When TSCC.TSS = '01', the Timestamp Counter is incremented in multiples of CAN bit times [1...16] depending on the configuration of TSCC.TCP. A wrap around sets interrupt flag IR.TSW. Write access resets the counter to zero. When TSCC.TSS = '10', TSC reflects the external Timestamp Counter value. A write access has no impact. Default Value: 0

22.1.10 CANFD0_CH0_TOCC

Timeout Counter Configuration

Address: 0x40520028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		RW
HW Access	None					R		R
Name	None [7:3]					TOS [2:1]		ETOC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	TOP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	TOP [31:24]							

Bits	Name	Description
31 : 16	TOP	Timeout Period Start value of the Timeout Counter (down-counter). Configures the Timeout Period. Default Value: 0xFFFF
2 : 1	TOS	Timeout Select When operating in Continuous mode, a write to TOCV presets the counter to the value configured by TOCC.TOP and continues down-counting. When the Timeout Counter is controlled by one of the FIFOs, an empty FIFO presets the counter to the value configured by TOCC.TOP. Down-counting is started when the first FIFO element is stored. 00= Continuous operation 01= Timeout controlled by Tx Event FIFO 10= Timeout controlled by Rx FIFO 0 11= Timeout controlled by Rx FIFO 1 Default Value: 0

22.1.10 CANFD0_CH0_TOCC (continued)

0	ETOC	Enable Timeout Counter 0= Timeout Counter disabled 1= Timeout Counter enabled Default Value: 0

22.1.11 CANFD0_CH0_TOCV

Timeout Counter Value

Address: 0x4052002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TOC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TOC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	TOC	Timeout Counter The Timeout Counter is decremented in multiples of CAN bit times [1...16] depending on the configuration of TSCC.TCP. When decremented to zero, interrupt flag IR.TOO is set and the Timeout Counter is stopped. Start and reset/restart conditions are configured via TOCC.TOS. Default Value: 0xFFFF

22.1.12 CANFD0_CH0_ECR

Error Counter Register

Address: 0x40520040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TEC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R	R						
HW Access	RW	RW						
Name	RP	REC [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW1C							
Name	CEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	CEL	CAN Error Logging The counter is incremented each time when a CAN protocol error causes the Transmit Error Counter or the Receive Error Counter to be incremented. It is reset by read access to CEL. The counter stops at 0xFF; the next increment of TEC or REC sets interrupt flag IR.ELO. Default Value: 0
15	RP	Receive Error Passive 0= The Receive Error Counter is below the error passive level of 128 1= The Receive Error Counter has reached the error passive level of 128 Default Value: 0
14 : 8	REC	Receive Error Counter Actual state of the Receive Error Counter, values between 0 and 127 Default Value: 0
7 : 0	TEC	Transmit Error Counter Actual state of the Transmit Error Counter, values between 0 and 255 Default Value: 0

22.1.13 CANFD0_CH0_PSR

Protocol Status Register

Address: 0x40520044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R		R		
HW Access	RW	RW	RW	RW		RW1S		
Name	BO	EW	EP	ACT [4:3]		LEC [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None	R	R	R	R	R		
HW Access	None	RW1C	RW1C	RW1C	RW1C	RW1S		
Name	None	PXE	RFDF	RBRS	RESI	DLEC [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None	R						
HW Access	None	RW						
Name	None	TDCV [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
22 : 16	TDCV	Transmitter Delay Compensation Value 0x00-0x7F Position of the secondary sample point, defined by the sum of the measured delay from m_can_tx to m_can_rx and TDCR.TDCO. The SSP position is, in the data phase, the number of mtq between the start of the transmitted bit and the secondary sample point. Valid values are 0 to 127 mtq. Default Value: 0
14	PXE	Protocol Exception Event , Reset on Read 0= No protocol exception event occurred since last read access 1= Protocol exception event occurred Default Value: 0
13	RFDF	Received a CAN FD Message , Reset on Read This bit is set independent of acceptance filtering. 0= Since this bit was reset by the CPU, no CAN FD message has been received 1= Message in CAN FD format with FDF flag set has been received Default Value: 0

22.1.13 CANFD0_CH0_PSR (continued)

12	RBRS	BRS flag of last received CAN FD Message , Reset on Read This bit is set together with RFDF, independent of acceptance filtering. 0= Last received CAN FD message did not have its BRS flag set 1= Last received CAN FD message had its BRS flag set Default Value: 0
11	RESI	ESI flag of last received CAN FD Message , Reset on Read This bit is set together with RFDF, independent of acceptance filtering. 0= Last received CAN FD message did not have its ESI flag set 1= Last received CAN FD message had its ESI flag set Default Value: 0
10 : 8	DLEC	Data Phase Last Error Code , Set on Read Type of last error that occurred in the data phase of a CAN FD format frame with its BRS flag set. Coding is the same as for LEC. This field will be cleared to zero when a CAN FD format frame with its BRS flag set has been transferred (reception or transmission) without error. Default Value: 7
7	BO	Bus_Off Status 0= The M_CAN is not Bus_Off 1= The M_CAN is in Bus_Off state Default Value: 0
6	EW	Warning Status 0= Both error counters are below the Error_Warning limit of 96 1= At least one of error counter has reached the Error_Warning limit of 96 Default Value: 0
5	EP	Error Passive 0= The M_CAN is in the Error_Active state. It normally takes part in bus communication and sends an active error flag when an error has been detected 1= The M_CAN is in the Error_Passive state Default Value: 0
4 : 3	ACT	Activity Monitors the module's CAN communication state. 00= Synchronizing - node is synchronizing on CAN communication 01= Idle - node is neither receiver nor transmitter 10= Receiver - node is operating as receiver 11= Transmitter - node is operating as transmitter Default Value: 0

22.1.13 CANFD0_CH0_PSR (continued)

2 : 0	LEC	Last Error Code, Set on Read0 The LEC indicates the type of the last error to occur on the CAN bus. This field will be cleared to '0' when a message has been transferred (reception or transmission) without error. 0= No Error: No error occurred since LEC has been reset by successful reception or transmission. 1= Stuff Error: More than 5 equal bits in a sequence have occurred in a part of a received message where this is not allowed. 2= Form Error: A fixed format part of a received frame has the wrong format. 3= AckError: The message transmitted by the M_TTCAN was not acknowledged by another node. 4= Bit1Error: During the transmission of a message (with the exception of the arbitration field), the device wanted to send a recessive level (bit of logical value '1'), but the monitored bus value was dominant. 5= Bit0Error: During the transmission of a message (or acknowledge bit, or active error flag, or overload flag), the device wanted to send a dominant level (data or identifier bit logical value 0'), but the monitored bus value was recessive. During Bus_Off recovery this status is set each time a sequence of 11 recessive bits has been monitored. This enables the CPU to monitor the proceeding of the Bus_Off recovery sequence (indicating the bus is not stuck at dominant or continuously disturbed). 6= CRCError: The CRC check sum of a received message was incorrect. The CRC of an incoming message does not match with the CRC calculated from the received data. 7= NoChange: Any read access to the Protocol Status Register re-initializes the LEC to '7'. When the LEC shows the value '7', no CAN bus event was detected since the last CPU read access to the Protocol Status Register. Default Value: 7

22.1.14 CANFD0_CH0_TDCR

Transmitter Delay Compensation Register

Address: 0x40520048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	TDCF [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW						
HW Access	None	R						
Name	None	TDCO [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14 : 8	TDCO	Transmitter Delay Compensation Offset 0x00-0x7F Offset value defining the distance between the measured delay from m_ttcan_tx to m_ttcan_rx and the secondary sample point. Valid values are 0 to 127 mtq. Default Value: 0
6 : 0	TDCF	Transmitter Delay Compensation Filter Window Length 0x00-0x7F Defines the minimum value for the SSP position, dominant edges on m_ttcan_rx that would result in an earlier SSP position are ignored for transmitter delay measurement. The feature is enabled when TDCF is configured to a value greater than TDCO. Valid values are 0 to 127 mtq Default Value: 0

22.1.15 CANFD0_CH0_IR

Interrupt Register

Address: 0x40520050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	RF1L_	RF1F	RF1W	RF1N	RF0L_	RF0F	RF0W	RF0N

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	TEFL_	TEFF	TEFW	TEFN	TFE	TCF	TC	HPM

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	EP_	ELO	BEU	BEC	DRX	TOO	MRAF	TSW

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [31:30]		ARA	PED	PEA	WDI	BO_	EW_

Bits	Name	Description
29	ARA	Access to Reserved Address 0= No access to reserved address occurred 1= Access to reserved address occurred Default Value: 0
28	PED	Protocol Error in Data Phase (Data Bit Time is used) 0= No protocol error in data phase 1= Protocol error in data phase detected (PSR.DLEC != 0,7) Default Value: 0
27	PEA	Protocol Error in Arbitration Phase (Nominal Bit Time is used) 0= No protocol error in arbitration phase 1= Protocol error in arbitration phase detected (PSR.LEC != 0,7) Default Value: 0
26	WDI	Watchdog Interrupt 0= No Message RAM Watchdog event occurred 1= Message RAM Watchdog event due to missing READY Default Value: 0

22.1.15 CANFD0_CH0_IR (continued)

25	BO_	Bus_Off Status 0= Bus_Off status unchanged 1= Bus_Off status changed Default Value: 0
24	EW_	Warning Status 0= Error_Warning status unchanged 1= Error_Warning status changed Default Value: 0
23	EP_	Error Passive 0= Error_Passive status unchanged 1= Error_Passive status changed Default Value: 0
22	ELO	Error Logging Overflow 0= CAN Error Logging Counter did not overflow 1= Overflow of CAN Error Logging Counter occurred Default Value: 0
21	BEU	Bit Error Uncorrected Message RAM bit error detected, uncorrected. Controlled by input signal m_ttcan_aeim_berr[1] generated by an optional external parity / ECC logic attached to the Message RAM. An uncorrected Message RAM bit error sets CCCR.INIT to '1'. This is done to avoid transmission of corrupted data. 0= No bit error detected when reading from Message RAM 1= Bit error detected, uncorrected (e.g. parity logic) Default Value: 0
20	BEC	M_TTCAN reports correctable ECC fault to the generic fault structure, this bit always reads as 0. Bit Error Corrected Message RAM bit error detected and corrected. Controlled by input signal m_ttcan_aeim_berr[0] generated by an optional external parity / ECC logic attached to the Message RAM. 0= No bit error detected when reading from Message RAM 1= Bit error detected and corrected (e.g. ECC) Default Value: 0
19	DRX	Message stored to Dedicated Rx Buffer The flag is set whenever a received message has been stored into a dedicated Rx Buffer. 0= No Rx Buffer updated 1= At least one received message stored into a Rx Buffer Default Value: 0
18	TOO	Timeout Occurred 0= No timeout 1= Timeout reached Default Value: 0

22.1.15 CANFD0_CH0_IR (continued)

17	MRAF	Message RAM Access Failure The flag is set, when the Rx Handler - has not completed acceptance filtering or storage of an accepted message until the arbitration field of the following message has been received. In this case acceptance filtering or message storage is aborted and the Rx Handler starts processing of the following message. - was not able to write a message to the Message RAM. In this case message storage is aborted. In both cases the FIFO put index is not updated resp. the New Data flag for a dedicated Rx Buffer is not set, a partly stored message is overwritten when the next message is stored to this location. The flag is also set when the Tx Handler was not able to read a message from the Message RAM in time. In this case message transmission is aborted. In case of a Tx Handler access failure the M_TTCAN is switched into Restricted Operation Mode (see Section 3.1.5). To leave Restricted Operation Mode, the Host CPU has to reset CCCR.ASM. 0= No Message RAM access failure occurred 1= Message RAM access failure occurred Default Value: 0
16	TSW	Timestamp Wraparound 0= No timestamp counter wrap-around 1= Timestamp counter wrapped around Default Value: 0
15	TEFL_	Tx Event FIFO Element Lost 0= No Tx Event FIFO element lost 1= Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero Default Value: 0
14	TEFF	Tx Event FIFO Full 0= Tx Event FIFO not full 1= Tx Event FIFO full Default Value: 0
13	TEFW	Tx Event FIFO Watermark Reached 0= Tx Event FIFO fill level below watermark 1= Tx Event FIFO fill level reached watermark Default Value: 0
12	TEFN	Tx Event FIFO New Entry 0= Tx Event FIFO unchanged 1= Tx Handler wrote Tx Event FIFO element Default Value: 0
11	TFE	Tx FIFO Empty 0= Tx FIFO non-empty 1= Tx FIFO empty Default Value: 0
10	TCF	Transmission Cancellation Finished 0= No transmission cancellation finished 1= Transmission cancellation finished Default Value: 0
9	TC	Transmission Completed 0= No transmission completed 1= Transmission completed Default Value: 0
8	HPM	High Priority Message 0= No high priority message received 1= High priority message received Default Value: 0

22.1.15 CANFD0_CH0_IR (continued)

7	RF1L_	Rx FIFO 1 Message Lost 0= No Rx FIFO 1 message lost 1= Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero Default Value: 0
6	RF1F	Rx FIFO 1 Full 0= Rx FIFO 1 not full 1= Rx FIFO 1 full Default Value: 0
5	RF1W	Rx FIFO 1 Watermark Reached 0= Rx FIFO 1 fill level below watermark 1= Rx FIFO 1 fill level reached watermark Default Value: 0
4	RF1N	Rx FIFO 1 New Message 0= No new message written to Rx FIFO 1 1= New message written to Rx FIFO 1 Default Value: 0
3	RF0L_	Rx FIFO 0 Message Lost 0= No Rx FIFO 0 message lost 1= Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero Default Value: 0
2	RF0F	Rx FIFO 0 Full 0= Rx FIFO 0 not full 1= Rx FIFO 0 full Default Value: 0
1	RF0W	Rx FIFO 0 Watermark Reached 0= Rx FIFO 0 fill level below watermark 1= Rx FIFO 0 fill level reached watermark Default Value: 0
0	RF0N	Rx FIFO 0 New Message 0= No new message written to Rx FIFO 0 1= New message written to Rx FIFO 0 Default Value: 0

22.1.16 CANFD0_CH0_IE

Interrupt Enable

Address: 0x40520054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	RF1LE	RF1FE	RF1WE	RF1NE	RF0LE	RF0FE	RF0WE	RF0NE

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	TEFLE	TEFFE	TEFWE	TEFNE	TFEE	TCFE	TCE	HPME

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	EPE	ELOE	BEUE	BECE	DRXE	TOOE	MRAFE	TSWE

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [31:30]		ARAE	PEDE	PEAE	WDIE	BOE	EWE

Bits	Name	Description
29	ARAE	Access to Reserved Address Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
28	PEDE	Protocol Error in Data Phase Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
27	PEAE	Protocol Error in Arbitration Phase Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
26	WDIE	Watchdog Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0

22.1.16 CANFD0_CH0_IE (continued)

25	BOE	Bus_Off Status Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
24	EWE	Warning Status Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
23	EPE	Error Passive Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
22	ELOE	Error Logging Overflow Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
21	BEUE	Bit Error Uncorrected Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
20	BECE	Bit Error Corrected Interrupt Enable (not used in M_TTCAN) 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
19	DRXE	Message stored to Dedicated Rx Buffer Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
18	TOOE	Timeout Occurred Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
17	MRAFE	Message RAM Access Failure Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
16	TSWE	Timestamp Wraparound Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
15	TEFLE	Tx Event FIFO Event Lost Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
14	TEFFE	Tx Event FIFO Full Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0

22.1.16 CANFD0_CH0_IE (continued)

13	TEFWE	Tx Event FIFO Watermark Reached Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
12	TEFNE	Tx Event FIDO New Entry Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
11	TFEE	Tx FIFO Empty Interrupt Enable 0= Interrupt Disabled 1= Interrupt EnabledTx FIFO Empty Interrupt Enable Default Value: 0
10	TCFE	Transmission Cancellation Finished Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
9	TCE	Transmission Completed Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
8	HPME	High Priority Message Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
7	RF1LE	Rx FIFO 1 Message Lost Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
6	RF1FE	Rx FIFO 1 Full Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
5	RF1WE	Rx FIFO 1 Watermark Reached Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
4	RF1NE	Rx FIFO 1 New Message Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
3	RF0LE	Rx FIFO 0 Message Lost Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
2	RF0FE	Rx FIFO 0 Full Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0

22.1.16 CANFD0_CH0_IE (continued)

1	RF0WE	Rx FIFO 0 Watermark Reached Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
0	RF0NE	Rx FIFO 0 New Message Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0

22.1.17 CANFD0_CH0_ILS

Interrupt Line Select

Address: 0x40520058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	RF1LL	RF1FL	RF1WL	RF1NL	RF0LL	RF0FL	RF0WL	RF0NL

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	TEFLL	TEFFL	TEFWL	TEFNL	TFEL	TCFL	TCL	HPML

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	EPL	ELOL	BEUL	BECL	DRXL	TOOL	MRAFL	TSWL

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [31:30]		ARAL	PEDL	PEAL	WDIL	BOL	EWL

Bits	Name	Description
29	ARAL	Access to Reserved Address Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
28	PEDL	Protocol Error in Data Phase Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
27	PEAL	Protocol Error in Arbitration Phase Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
26	WDIL	Watchdog Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0

22.1.17 CANFD0_CH0_ILS (continued)

25	BOL	Bus_Off Status Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
24	EWL	Warning Status Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
23	EPL	Error Passive Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
22	ELOL	Error Logging Overflow Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
21	BEUL	Bit Error Uncorrected Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
20	BECL	Bit Error Corrected Interrupt Select (not used in M_TTCAN) 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
19	DRXL	Message stored to Dedicated Rx Buffer Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
18	TOOL	Timeout Occurred Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
17	MRAFL	Message RAM Access Failure Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
16	TSWL	Timestamp Wraparound Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
15	TEFLL	Tx Event FIFO Event Lost Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
14	TEFFL	Tx Event FIFO Full Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0

22.1.17 CANFD0_CH0_ILS (continued)

13	TEFWL	Tx Event FIFO Watermark Reached Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
12	TEFNL	Tx Event FIFO New Entry Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
11	TFEL	Tx FIFO Empty Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
10	TCFL	Transmission Cancellation Finished Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
9	TCL	Transmission Completed Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
8	HPML	High Priority Message Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
7	RF1LL	Rx FIFO 1 Message Lost Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
6	RF1FL	Rx FIFO 1 Full Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
5	RF1WL	Rx FIFO 1 Watermark Reached Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
4	RF1NL	Rx FIFO 1 New Message Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
3	RF0LL	Rx FIFO 0 Message Lost Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
2	RF0FL	Rx FIFO 0 Full Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0

22.1.17 CANFD0_CH0_ILS (continued)

1	RF0WL	Rx FIFO 0 Watermark Reached Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
0	RF0NL	Rx FIFO 0 New Message Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0

22.1.18 CANFD0_CH0_ILE

Interrupt Line Enable

Address: 0x4052005C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						EINT1	EINT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	EINT1	Enable Interrupt Line 1 0= Interrupt line m_ttcan_int1 disabled 1= Interrupt line m_ttcan_int1 enabled Default Value: 0
0	EINT0	Enable Interrupt Line 0 0= Interrupt line m_ttcan_int0 disabled 1= Interrupt line m_ttcan_int0 enabled Default Value: 0

22.1.19 CANFD0_CH0_GFC

Global Filter Configuration

Address: 0x40520080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	RW
HW Access	None		R		R		R	R
Name	None [7:6]		ANFS [5:4]		ANFE [3:2]		RRFS	RRFE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	ANFS	Accept Non-matching Frames Standard Defines how received messages with 11-bit IDs that do not match any element of the filter list are treated. 00= Accept in Rx FIFO 0 01= Accept in Rx FIFO 1 10= Reject 11= Reject Default Value: 0
3 : 2	ANFE	Accept Non-matching Frames Extended Defines how received messages with 29-bit IDs that do not match any element of the filter list are treated. 00= Accept in Rx FIFO 0 01= Accept in Rx FIFO 1 10= Reject 11= Reject Default Value: 0

22.1.19 CANFD0_CH0_GFC (continued)

1	RRFS	Reject Remote Frames Standard 0= Filter remote frames with 11-bit standard IDs 1= Reject all remote frames with 11-bit standard IDs Default Value: 0
0	RRFE	Reject Remote Frames Extended 0= Filter remote frames with 29-bit extended IDs 1= Reject all remote frames with 29-bit extended IDs Default Value: 0

22.1.20 CANFD0_CH0_SIDFC

Standard ID Filter Configuration

Address: 0x40520084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	FLSSA [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	FLSSA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	LSS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	LSS	List Size Standard 0= No standard Message ID filter 1-128= Number of standard Message ID filter elements 128= Values greater than 128 are interpreted as 128 Default Value: 0
15 : 2	FLSSA	Filter List Standard Start Address Start address of standard Message ID filter list (32-bit word address, see Figure 2). Default Value: 0

22.1.21 CANFD0_CH0_XIDFC

Extended ID Filter Configuration

Address: 0x40520088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	FLESA [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	FLESA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	LSE [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
22 : 16	LSE	List Size Extended 0= No extended Message ID filter 1-64= Number of extended Message ID filter elements 64= Values greater than 64 are interpreted as 64 Default Value: 0
15 : 2	FLESA	Filter List Extended Start Address Start address of extended Message ID filter list (32-bit word address, see Figure 2). Default Value: 0

22.1.22 CANFD0_CH0_XIDAM

Extended ID AND Mask

Address: 0x40520090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	EIDM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	EIDM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	EIDM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			R				
Name	None [31:29]			EIDM [28:24]				

Bits	Name	Description
28 : 0	EIDM	Extended ID Mask For acceptance filtering of extended frames the Extended ID AND Mask is ANDed with the Message ID of a received frame. Intended for masking of 29-bit IDs in SAE J1939. With the reset value of all bits set to one the mask is not active. Default Value: 0x1FFFFFFF

22.1.23 CANFD0_CH0_HPMS

High Priority Message Status

Address: 0x40520094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		R					
HW Access	RW		RW					
Name	MSI [7:6]		BIDX [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R	R						
HW Access	RW	RW						
Name	FLST	FIDX [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	FLST	Filter List Indicates the filter list of the matching filter element. 0= Standard Filter List 1= Extended Filter List Default Value: 0
14 : 8	FIDX	Filter Index Index of matching filter element. Range is 0 to SIDFC.LSS - 1 resp. XIDFC.LSE - 1. Default Value: 0
7 : 6	MSI	Message Storage Indicator 00= No FIFO selected 01= FIFO message lost 10= Message stored in FIFO 0 11= Message stored in FIFO 1 Default Value: 0
5 : 0	BIDX	Buffer Index Index of Rx FIFO element to which the message was stored. Only valid when MSI[1] = '1'. Default Value: 0

22.1.24 CANFD0_CH0_NDAT1

New Data 1

Address: 0x40520098

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW							
Name	ND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW							
Name	ND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	RW							
Name	ND [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	RW							
Name	ND [31:24]							

Bits	Name	Description
31 : 0	ND	New Data The register holds the New Data flags of Rx Buffers 0 to 31. The flags are set when the respective Rx Buffer has been updated from a received frame. The flags remain set until the Host clears them. A flag is cleared by writing a '1' to the corresponding bit position. Writing a '0' has no effect. A hard reset will clear the register. 0= Rx Buffer not updated 1= Rx Buffer updated from new message Default Value: 0

22.1.25 CANFD0_CH0_NDAT2

New Data 2

Address: 0x4052009C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW							
Name	ND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW							
Name	ND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	RW							
Name	ND [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	RW							
Name	ND [31:24]							

Bits	Name	Description
31 : 0	ND	New Data The register holds the New Data flags of Rx Buffers 32 to 63. The flags are set when the respective Rx Buffer has been updated from a received frame. The flags remain set until the Host clears them. A flag is cleared by writing a '1' to the corresponding bit position. Writing a '0' has no effect. A hard reset will clear the register. 0= Rx Buffer not updated 1= Rx Buffer updated from new message Default Value: 0

22.1.26 CANFD0_CH0_RXF0C

Rx FIFO 0 Configuration

Address: 0x405200A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	F0SA [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	F0SA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	F0S [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW						
HW Access	R	R						
Name	F0OM	F0WM [30:24]						

Bits	Name	Description
31	F0OM	FIFO 0 Operation Mode FIFO 0 can be operated in blocking or in overwrite mode (see Section 3.4.2). 0= FIFO 0 blocking mode 1= FIFO 0 overwrite mode Default Value: 0
30 : 24	F0WM	Rx FIFO 0 Watermark 0= Watermark interrupt disabled 1-64= Level for Rx FIFO 0 watermark interrupt (IR.RF0W) 64= Watermark interrupt disabled Default Value: 0
22 : 16	F0S	Rx FIFO 0 Size 0= No Rx FIFO 0 1-64= Number of Rx FIFO 0 elements 64= Values greater than 64 are interpreted as 64 The Rx FIFO 0 elements are indexed from 0 to F0S-1 Default Value: 0
15 : 2	F0SA	Rx FIFO 0 Start Address Start address of Rx FIFO 0 in Message RAM (32-bit word address, see Figure 2). Default Value: 0

22.1.27 CANFD0_CH0_RXF0S

Rx FIFO 0 Status

Address: 0x405200A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R						
HW Access	None	RW						
Name	None	F0FL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None		R					
HW Access	None		RW					
Name	None [15:14]		F0GI [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None		R					
HW Access	None		RW					
Name	None [23:22]		F0PI [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	None						R	R
HW Access	None						RW	RW
Name	None [31:26]						RF0L	F0F

Bits	Name	Description
25	RF0L	Rx FIFO 0 Message Lost This bit is a copy of interrupt flag IR.RF0L. When IR.RF0L is reset, this bit is also reset. 0= No Rx FIFO 0 message lost 1= Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero Default Value: 0
24	F0F	Rx FIFO 0 Full 0= Rx FIFO 0 not full 1= Rx FIFO 0 full Default Value: 0
21 : 16	F0PI	Rx FIFO 0 Put Index Rx FIFO 0 write index pointer, range 0 to 63. Default Value: 0
13 : 8	F0GI	Rx FIFO 0 Get Index Rx FIFO 0 read index pointer, range 0 to 63. This field is updated by the software writing to RxF0A.F0AI Default Value: 0

22.1.27 CANFD0_CH0_RXF0S (continued)

6 : 0	F0FL	Rx FIFO 0 Fill Level Number of elements stored in Rx FIFO 0, range 0 to 64. Default Value: 0

22.1.28 CANFD0_CH0_RXF0A

Rx FIFO 0 Acknowledge

Address: 0x405200A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		A					
Name	None [7:6]		F0AI [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	F0AI	Rx FIFO 0 Acknowledge Index After the Host has read a message or a sequence of messages from Rx FIFO 0 it has to write the buffer index of the last element read from Rx FIFO 0 to F0AI. This will set the Rx FIFO 0 Get Index RXF0S.F0GI to F0AI + 1 and update the FIFO 0 Fill Level RXF0S.F0FL. Default Value: 0

22.1.29 CANFD0_CH0_RXBC

Rx Buffer Configuration

Address: 0x405200AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	RBSA [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RBSA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 2	RBSA	Rx Buffer Start Address Configures the start address of the Rx Buffers section in the Message RAM (32-bit word address). Also used to reference debug messages A,B,C. Default Value: 0

22.1.30 CANFD0_CH0_RXF1C

Rx FIFO 1 Configuration

Address: 0x405200B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	F1SA [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	F1SA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	F1S [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW						
HW Access	R	R						
Name	F1OM	F1WM [30:24]						

Bits	Name	Description
31	F1OM	FIFO 1 Operation Mode FIFO 1 can be operated in blocking or in overwrite mode (see Section 3.4.2). 0= FIFO 1 blocking mode 1= FIFO 1 overwrite mode Default Value: 0
30 : 24	F1WM	Rx FIFO 1 Watermark 0= Watermark interrupt disabled 1-64= Level for Rx FIFO 1 watermark interrupt (IR.RF1W) 64= Watermark interrupt disabled Default Value: 0
22 : 16	F1S	Rx FIFO 1 Size 0= No Rx FIFO 1 1-64= Number of Rx FIFO 1 elements 64= Values greater than 64 are interpreted as 64 The Rx FIFO 1 elements are indexed from 0 to F1S - 1 Default Value: 0
15 : 2	F1SA	Rx FIFO 1 Start Address Start address of Rx FIFO 1 in Message RAM (32-bit word address, see Figure 2). Default Value: 0

22.1.31 CANFD0_CH0_RXF1S

Rx FIFO 1 Status

Address: 0x405200B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R						
HW Access	None	RW						
Name	None	F1FL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None		R					
HW Access	None		RW					
Name	None [15:14]		F1GI [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None		R					
HW Access	None		RW					
Name	None [23:22]		F1PI [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	R		None				R	R
HW Access	RW		None				RW	RW
Name	DMS [31:30]		None [29:26]				RF1L	F1F

Bits	Name	Description
31 : 30	DMS	Debug Message Status 00= Idle state, wait for reception of debug messages, DMA request is cleared 01= Debug message A received 10= Debug messages A, B received 11= Debug messages A, B, C received, DMA request is set Default Value: 0
25	RF1L	Rx FIFO 1 Message Lost This bit is a copy of interrupt flag IR.RF1L. When IR.RF1L is reset, this bit is also reset. 0= No Rx FIFO 1 message lost 1= Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero Default Value: 0
24	F1F	Rx FIFO 1 Full 0= Rx FIFO 1 not full 1= Rx FIFO 1 full Default Value: 0
21 : 16	F1PI	Rx FIFO 1 Put Index Rx FIFO 1 write index pointer, range 0 to 63. Default Value: 0

22.1.31 CANFD0_CH0_RXF1S (continued)

13 : 8	F1GI	Rx FIFO 1 Get Index Rx FIFO 1 read index pointer, range 0 to 63. This field is updated by the software writing to RxF1A.FAI Default Value: 0
6 : 0	F1FL	Rx FIFO 1 Fill Level Number of elements stored in Rx FIFO 1, range 0 to 64. Default Value: 0

22.1.32 CANFD0_CH0_RXF1A

Rx FIFO 1 Acknowledge

Address: 0x405200B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		A					
Name	None [7:6]		F1AI [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	F1AI	Rx FIFO 1 Acknowledge Index After the Host has read a message or a sequence of messages from Rx FIFO 1 it has to write the buffer index of the last element read from Rx FIFO 1 to F1AI. This will set the Rx FIFO 1 Get Index RXF1S.F1GI to F1AI + 1 and update the FIFO 1 Fill Level RXF1S.F1FL. Default Value: 0

22.1.33 CANFD0_CH0_RXESC

Rx Buffer / FIFO Element Size Configuration

Address: 0x405200BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	F1DS [6:4]			None	F0DS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					R		
Name	None [15:11]					RBDS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10 : 8	RBDS	Rx Buffer Data Field Size 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field Default Value: 0
6 : 4	F1DS	Rx FIFO 1 Data Field Size 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field Default Value: 0

22.1.33 CANFD0_CH0_RXESC (continued)

2 : 0	F0DS	Rx FIFO 0 Data Field Size 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field Default Value: 0

22.1.34 CANFD0_CH0_TXBC

Tx Buffer Configuration

Address: 0x405200C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	TBSA [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TBSA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW					
HW Access	None		R					
Name	None [23:22]		NDTB [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW	RW					
HW Access	None	R	R					
Name	None	TFQM	TFQS [29:24]					

Bits	Name	Description
30	TFQM	Tx FIFO/Queue Mode 0= Tx FIFO operation 1= Tx Queue operation Default Value: 0
29 : 24	TFQS	Transmit FIFO/Queue Size 0= No Tx FIFO/Queue 1-32= Number of Tx Buffers used for Tx FIFO/Queue 32= Values greater than 32 are interpreted as 32 Default Value: 0
21 : 16	NDTB	Number of Dedicated Transmit Buffers 0= No Dedicated Tx Buffers 1-32= Number of Dedicated Tx Buffers 32= Values greater than 32 are interpreted as 32 Default Value: 0
15 : 2	TBSA	Tx Buffers Start Address Start address of Tx Buffers section in Message RAM (32-bit word address, see Figure 2). Default Value: 0

22.1.35 CANFD0_CH0_TXFQS

Tx FIFO/Queue Status

Address: 0x405200C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R					
HW Access	None		RW					
Name	None [7:6]		TFFL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None			R				
HW Access	None			RW				
Name	None [15:13]			TFGI [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None		R	R				
HW Access	None		RW	RW				
Name	None [23:22]		TFQF	TFQPI [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	TFQF	Tx FIFO/Queue Full 0= Tx FIFO/Queue not full 1= Tx FIFO/Queue full Default Value: 0
20 : 16	TFQPI	Tx FIFO/Queue Put Index Tx FIFO/Queue write index pointer, range 0 to 31. Default Value: 0
12 : 8	TFGI	Tx FIFO Get Index Tx FIFO read index pointer, range 0 to 31. Read as zero when Tx Queue operation is configured TXBC.TFQM = '1'). Default Value: 0
5 : 0	TFFL	Tx FIFO Free Level Number of consecutive free Tx FIFO elements starting from TFGI, range 0 to 32. Read as zero when Tx Queue operation is configured (TXBC.TFQM = '1') Default Value: 0

22.1.36 CANFD0_CH0_TXESC

Tx Buffer Element Size Configuration

Address: 0x405200C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					TBDS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	TBDS	Tx Buffer Data Field Size 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field Default Value: 0

22.1.37 CANFD0_CH0_TXBRP

Tx Buffer Request Pending

Address: 0x405200CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TRP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	TRP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	TRP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	TRP [31:24]							

Bits	Name	Description

22.1.37 CANFD0_CH0_TXBRP (continued)

31 : 0	TRP	Transmission Request Pending Each Tx Buffer has its own Transmission Request Pending bit. The bits are set via register TX-BAR. The bits are reset after a requested transmission has completed or has been cancelled via register TXBCR. TXBRP bits are set only for those Tx Buffers configured via TXBC. After a TXBRP bit has been set, a Tx scan (see Section 3.5, Tx Handling) is started to check for the pending Tx request with the highest priority (Tx Buffer with lowest Message ID). A cancellation request resets the corresponding transmission request pending bit of register TXBRP. In case a transmission has already been started when a cancellation is requested, this is done at the end of the transmission, regardless whether the transmission was successful or not. The cancellation request bits are reset directly after the corresponding TXBRP bit has been reset. After a cancellation has been requested, a finished cancellation is signaled via TXBCF after successful transmission together with the corresponding TXBTO bit when the transmission has not yet been started at the point of cancellation when the transmission has been aborted due to lost arbitration when an error occurred during frame transmission In DAR mode all transmissions are automatically cancelled if they are not successful. The corresponding TXBCF bit is set for all unsuccessful transmissions. 0= No transmission request pending 1= Transmission request pending Default Value: 0

22.1.38 CANFD0_CH0_TXBAR

Tx Buffer Add Request

Address: 0x405200D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	AR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	AR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	AR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	AR [31:24]							

Bits	Name	Description
31 : 0	AR	Add Request Each Tx Buffer has its own Add Request bit. Writing a '1' will set the corresponding Add Request bit; writing a '0' has no impact. This enables the Host to set transmission requests for multiple Tx Buffers with one write to TXBAR. TXBAR bits are set only for those Tx Buffers configured via TXBC. When no Tx scan is running, the bits are reset immediately, else the bits remain set until the Tx scan process has completed. 0= No transmission request added 1= Transmission requested added Default Value: 0

22.1.39 CANFD0_CH0_TXBCR

Tx Buffer Cancellation Request

Address: 0x405200D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	CR [31:24]							

Bits	Name	Description
31 : 0	CR	Cancellation Request Each Tx Buffer has its own Cancellation Request bit. Writing a '1' will set the corresponding Cancellation Request bit; writing a '0' has no impact. This enables the Host to set cancellation requests for multiple Tx Buffers with one write to TXBCR. TXBCR bits are set only for those Tx Buffers configured via TXBC. The bits remain set until the corresponding bit of TXBRP is reset. 0= No cancellation pending 1= Cancellation pending Default Value: 0

22.1.40 CANFD0_CH0_TXBTO

Tx Buffer Transmission Occurred

Address: 0x405200D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TO [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	TO [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	TO [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	TO [31:24]							

Bits	Name	Description
31 : 0	TO	Transmission Occurred Each Tx Buffer has its own Transmission Occurred bit. The bits are set when the corresponding TXBRP bit is cleared after a successful transmission. The bits are reset when a new transmission is requested by writing a '1' to the corresponding bit of register TXBAR. 0= No transmission occurred 1= Transmission occurred Default Value: 0

22.1.41 CANFD0_CH0_TXBCF

Tx Buffer Cancellation Finished

Address: 0x405200DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CF [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	CF [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	CF [31:24]							

Bits	Name	Description
31 : 0	CF	Cancellation Finished Each Tx Buffer has its own Cancellation Finished bit. The bits are set when the corresponding TXBRP bit is cleared after a cancellation was requested via TXBCR. In case the corresponding TXBRP bit was not set at the point of cancellation, CF is set immediately. The bits are reset when a new transmission is requested by writing a '1' to the corresponding bit of register TXBAR. 0= No transmit buffer cancellation 1= Transmit buffer cancellation finished Default Value: 0

22.1.42 CANFD0_CH0_TXBTIE

Tx Buffer Transmission Interrupt Enable

Address: 0x405200E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TIE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TIE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	TIE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	TIE [31:24]							

Bits	Name	Description
31 : 0	TIE	Transmission Interrupt Enable Each Tx Buffer has its own Transmission Interrupt Enable bit. 0= Transmission interrupt disabled 1= Transmission interrupt enable Default Value: 0

22.1.43 CANFD0_CH0_TXBCIE

Tx Buffer Cancellation Finished Interrupt Enable

Address: 0x405200E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CFIE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CFIE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CFIE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	CFIE [31:24]							

Bits	Name	Description
31 : 0	CFIE	Cancellation Finished Interrupt Enable Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0= Cancellation finished interrupt disabled 1= Cancellation finished interrupt enabled Default Value: 0

22.1.44 CANFD0_CH0_TXEFC

Tx Event FIFO Configuration

Address: 0x405200F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	EFSA [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	EFSA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW					
HW Access	None		R					
Name	None [23:22]		EFS [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW					
HW Access	None		R					
Name	None [31:30]		EFWM [29:24]					

Bits	Name	Description
29 : 24	EFWM	Event FIFO Watermark 0= Watermark interrupt disabled 1-32= Level for Tx Event FIFO watermark interrupt (IR.TEFW) 32= Watermark interrupt disabled Default Value: 0
21 : 16	EFS	Event FIFO Size 0= Tx Event FIFO disabled 1-32= Number of Tx Event FIFO elements 32= Values greater than 32 are interpreted as 32 The Tx Event FIFO elements are indexed from 0 to EFS-1 Default Value: 0
15 : 2	EFSA	Event FIFO Start Address Start address of Tx Event FIFO in Message RAM (32-bit word address, see Figure 2). Default Value: 0

22.1.45 CANFD0_CH0_TXEFS

Tx Event FIFO Status

Address: 0x405200F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R					
HW Access	None		RW					
Name	None [7:6]		EFFL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None			R				
HW Access	None			RW				
Name	None [15:13]			EFGI [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			R				
HW Access	None			RW				
Name	None [23:21]			EFPI [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None						R	R
HW Access	None						RW	RW
Name	None [31:26]						TEFL	EFF

Bits	Name	Description
25	TEFL	Tx Event FIFO Element Lost This bit is a copy of interrupt flag IR.TEFL. When IR.TEFL is reset, this bit is also reset. 0= No Tx Event FIFO element lost 1= Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero. Default Value: 0
24	EFF	Event FIFO Full 0= Tx Event FIFO not full 1= Tx Event FIFO full Default Value: 0
20 : 16	EFPI	Event FIFO Put Index Tx Event FIFO write index pointer, range 0 to 31. Default Value: 0
12 : 8	EFGI	Event FIFO Get Index Tx Event FIFO read index pointer, range 0 to 31. Default Value: 0
5 : 0	EFFL	Event FIFO Fill Level Number of elements stored in Tx Event FIFO, range 0 to 32. Default Value: 0

22.1.46 CANFD0_CH0_TXEFA

Tx Event FIFO Acknowledge

Address: 0x405200F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			EFAI [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	EFAI	Event FIFO Acknowledge Index After the Host has read an element or a sequence of elements from the Tx Event FIFO it has to write the index of the last element read from Tx Event FIFO to EFAI. This will set the Tx Event FIFO Get Index TXEFS.EFGI to EFAI + 1 and update the Event FIFO Fill Level TXEFS.EFFL. Default Value: 0

22.1.47 CANFD0_CH0_TTTMC

TT Trigger Memory Configuration

Address: 0x40520100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	TMSA [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TMSA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	TME [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
22 : 16	TME	Trigger Memory Elements 0= No Trigger Memory 1-64= Number of Trigger Memory elements 64= Values greater than 64 are interpreted as 64 Default Value: 0
15 : 2	TMSA	Trigger Memory Start Address Start address of Trigger Memory in Message RAM (32-bit word address, see Figure 2). Default Value: 0

22.1.48 CANFD0_CH0_TTRMC

TT Reference Message Configuration

Address: 0x40520104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None	RW				
HW Access	R	R	None	R				
Name	RMPS	XTD	None	RID [28:24]				

Bits	Name	Description
31	RMPS	Reference Message Payload Select Ignored in case of time slaves. 0= Reference message has no additional payload 1= The following elements are taken from Tx Buffer 0: Message Marker MM, Event FIFO Control EFC, Data Length Code DLC, Data Bytes DB Level 1: bytes 2-8, Level 0,2: bytes 5-8) Default Value: 0
30	XTD	Extended Identifier 0= 11-bit standard identifier 1= 29-bit extended identifier Default Value: 0
28 : 0	RID	Reference Identifier Identifier transmitted with reference message and used for reference message filtering. Standard or extended reference identifier depending on bit XTD. A standard identifier has to be written to ID[28:18]. Default Value: 0

22.1.49 CANFD0_CH0_TTOCF

TT Operation Configuration

Address: 0x40520108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW	RW	None	RW	
HW Access	R			R	R	None	R	
Name	LDSDL [7:5]			TM	GEN	None	OM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW						
HW Access	R	R						
Name	EECS	IRTO [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	AWL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [31:27]					EVTP	ECC	EGTF

Bits	Name	Description
26	EVTP	Event Trigger Polarity 0= Rising edge trigger 1= Falling edge trigger Default Value: 0
25	ECC	Enable Clock Calibration 0= Automatic clock calibration in TTCAN Level 0,2 is disabled 1= Automatic clock calibration in TTCAN Level 0,2 is enabled Default Value: 0
24	EGTF	Enable Global Time Filtering 0= Global time filtering in TTCAN Level 0,2 is disabled 1= Global time filtering in TTCAN Level 0,2 is enabled Default Value: 0
23 : 16	AWL	Application Watchdog Limit The application watchdog can be disabled by programming AWL to 0x00. 0x00-FF Maximum time after which the application has to serve the application watchdog. The application watchdog is incremented once each 256 NTUs. Default Value: 1

22.1.49 CANFD0_CH0_TTOCF (continued)

15	EECS	Enable External Clock Synchronization If enabled, TUR configuration (TURCF.NCL only) may be updated during TTCAN operation. 0= External clock synchronization in TTCAN Level 0,2 disabled 1= External clock synchronization in TTCAN Level 0,2 enabled Default Value: 0
14 : 8	IRTO	Initial Reference Trigger Offset 0x00-7F Positive offset, range from 0 to 127 Default Value: 0
7 : 5	LDSDL	LD of Synchronization Deviation Limit The Synchronization Deviation Limit SDL is configured by its dual logarithm LDSDL with SDL = 2(LDSDL + 5). It should not exceed the clock tolerance given by the CAN bit timing configuration. 0x0-7 LD of Synchronization Deviation Limit (SDL <= 32...4096) Default Value: 0
4	TM	Time Master 0= Time Master function disabled 1= Potential Time Master Default Value: 0
3	GEN	Gap Enable 0= Strictly time-triggered operation 1= External event-synchronized time-triggered operation Default Value: 0
1 : 0	OM	Operation Mode 00= Event-driven CAN communication, default 01= TTCAN level 1 10= TTCAN level 2 11= TTCAN level 0 Default Value: 0

22.1.50 CANFD0_CH0_TTMLM

TT Matrix Limits

Address: 0x4052010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW					
HW Access	R		R					
Name	CSS [7:6]		CCM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				TXEW [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ENTT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None				RW			
HW Access	None				R			
Name	None [31:28]				ENTT [27:24]			

Bits	Name	Description
27 : 16	ENTT	Expected Number of Tx Triggers 0x000-FFF Expected number of Tx Triggers in one Matrix Cycle Default Value: 0
11 : 8	TXEW	Tx Enable Window 0x0-F Length of Tx enable window, 1-16 NTU cycles Default Value: 0
7 : 6	CSS	Cycle Start Synchronization Enables sync pulse output at pin m_ttcan_soc. 00= No sync pulse 01= Sync pulse at start of basic cycle 10= Sync pulse at start of matrix cycle 11= Reserved Default Value: 0

22.1.50 CANFD0_CH0_TTMLM (continued)

5 : 0	CCM	Cycle Count Max 0x00 1 Basic Cycle per Matrix Cycle 0x01 2 Basic Cycles per Matrix Cycle 0x03 4 Basic Cycles per Matrix Cycle 0x07 8 Basic Cycles per Matrix Cycle 0x0F 16 Basic Cycles per Matrix Cycle 0x1F 32 Basic Cycles per Matrix Cycle 0x3F 64 Basic Cycles per Matrix Cycle others Reserved Default Value: 0

22.1.51 CANFD0_CH0_TURCF

TUR Configuration

Address: 0x40520110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	NCL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	NCL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None	RW					
HW Access	R	None	R					
Name	ELT	None	DC [29:24]					

Bits	Name	Description
31	ELT	Enable Local Time 0= Local time is stopped, default 1= Local time is enabled Default Value: 0
29 : 16	DC	Denominator Configuration 0x0000 Illegal value 0x0001-3FFF Denominator Configuration Default Value: 0x1000
15 : 0	NCL	Numerator Configuration Low Write access to the TUR Numerator Configuration Low is only possible during configuration with TURCF.ELT = '0' or if TTOCF.EECS (external clock synchronization enabled) is set. When a new value for NCL is written outside TT Configuration Mode, the new value takes effect when TTOST.WECS is cleared to '0'. NCL is locked TTOST.WECS is '1'. 0x0000-FFFF Numerator Configuration Low Default Value: 0

22.1.52 CANFD0_CH0_TTOCN

TT Operation Control

Address: 0x40520114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW		RW	RW	RW
HW Access	R		R	R		R	R	R
Name	TMC [7:6]		RTIE	SWS [4:3]		SWP	ECS	SGT

Bits	15	14	13	12	11	10	9	8
SW Access	R	None	RW	RW	RW	RW	RW	RW
HW Access	RW	None	R	R	R	R	R	R
Name	LCKC	None	ESCN	NIG	TMG	FGP	GCS	TTIE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	LCKC	TT Operation Control Register Locked Set by a write access to register TTOCN. Reset when the updated configuration has been synchronized into the CAN clock domain. 0= Write access to TTOCN enabled 1= Write access to TTOCN locked Default Value: 0
13	ESCN	External Synchronization Control If enabled the M_TTCAN synchronizes its cycle time phase to an external event signaled by a rising edge at pin m_ttcan_evt (see Section 4.11). 0= External synchronization disabled 1= External synchronization enabled Default Value: 0

22.1.52 CANFD0_CH0_TTOCN (continued)

12	NIG	Next is Gap This bit can only be set when the M_TTCAN is the actual Time Master and when it is configured for external event-synchronized time-triggered operation (TTOCF.GEN = '1') 0= No action, reset by reception of any reference message 1= Transmit next reference message with Next_is_Gap = '1' Default Value: 0
11	TMG	Time Mark Gap 0= Reset by each reference message 1= Next reference message started when Register Time Mark interrupt TTIR.RTMI is activated Default Value: 0
10	FGP	Finish Gap Set by the CPU, reset by each reference message 0= No reference message requested 1= Application requested start of reference message Default Value: 0
9	GCS	Gap Control Select 0= Gap control independent from m_ttcan_evt 1= Gap control by input pin m_ttcan_evt Default Value: 0
8	TTIE	Trigger Time Mark Interrupt Pulse Enable External time mark events are configured by trigger memory element TMEX (see Section 2.4.7). A trigger time mark interrupt pulse is generated when the trigger memory element becomes active, and the M_TTCAN is in synchronization state In_Schedule or In_Gap. 0= Trigger Time Mark Interrupt output m_ttcan_tmp disabled 1= Trigger Time Mark Interrupt output m_ttcan_tmp enabled Default Value: 0
7 : 6	TMC	Register Time Mark Compare 00= No Register Time Mark Interrupt generated 01= Register Time Mark Interrupt if Time Mark = cycle time 10= Register Time Mark Interrupt if Time Mark = local time 11= Register Time Mark Interrupt if Time Mark = global time Default Value: 0
5	RTIE	Register Time Mark Interrupt Pulse Enable Register time mark interrupts are configured by register TTTMK. A register time mark interrupt pulse with the length of one NTU is generated when the time referenced by TTOCN.TMC (cycle, local, or global) equals TTTMK.TM, independent of the synchronization state. 0= Register Time Mark Interrupt output m_ttcan_rtp disabled 1= Register Time Mark Interrupt output m_ttcan_rtp enabled Default Value: 0
4 : 3	SWS	Stop Watch Source 00= Stop Watch disabled 01= Actual value of cycle time is copied to TTCPT.SWV 10= Actual value of local time is copied to TTCPT.SWV 11= Actual value of global time is copied to TTCPT.SWV Default Value: 0
2	SWP	Stop Watch Polarity 0= Rising edge trigger 1= Falling edge trigger Default Value: 0

22.1.52 CANFD0_CH0_TTOCN (continued)

1	ECS	External Clock Synchronization Writing a '1' to ECS sets TTOST.WECS if the node is the actual Time Master. ECS is reset after one Host clock period. The external clock synchronization takes effect at the start of the next basic cycle. Default Value: 0
0	SGT	Set Global time Writing a '1' to SGT sets TTOST.WGDT if the node is the actual Time Master. SGT is reset after one Host clock period. The global time preset takes effect when the node transmits the next reference message with the Master_Ref_Mark modified by the preset value written to TTGTP. Default Value: 0

22.1.53 CANFD0_CH0_TTGTP

TT Global Time Preset

Address: 0x40520118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CTP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	CTP [31:24]							

Bits	Name	Description
31 : 16	CTP	Cycle Time Target Phase CTP is write-protected while TTOCN.ESCN or TTOST.SPL are set (see Section 4.11). 0x0000-FFFF Defines target value of cycle time when a rising edge of m_ttcan_evt is expected Default Value: 0
15 : 0	TP	Time Preset TP is write-protected while TTOST.WGTD is set. 0x0000-7FFF Next Master Reference Mark = Master Reference Mark + TP 0x8000 reserved 0x8001-FFFF Next Master Reference Mark = Master Reference Mark - (0x10000 - TP) Default Value: 0

22.1.54 CANFD0_CH0_TTTMK

TT Time Mark

Address: 0x4052011C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TM_ [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TM_ [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	TICC [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	LCKM	None [30:24]						

Bits	Name	Description
31	LCKM	TT Time Mark Register Locked Always set by a write access to registers TTOCN. Set by write access to register TTTMK when TTOCN.TMC != '00'. Reset when the registers have been synchronized into the CAN clock domain. 0= Write access to TTTMK enabled 1= Write access to TTTMK locked Default Value: 0
22 : 16	TICC	Time Mark Cycle Code Cycle count for which the time mark is valid. 0b000000x valid for all cycles 0b000001c valid every second cycle at cycle count mod2 = c 0b00001cc valid every fourth cycle at cycle count mod4 = cc 0b0001ccc valid every eighth cycle at cycle count mod8 = ccc 0b001cccc valid every sixteenth cycle at cycle count mod16 = cccc 0b01ccccc valid every thirty-second cycle at cycle count mod32 = ccccc 0b1cccccc valid every sixty-fourth cycle at cycle count mod64 = cccccc Default Value: 0

22.1.54 CANFD0_CH0_TTTMK (continued)

15 : 0	TM_	Time Mark 0x0000-FFFF Time Mark Default Value: 0

22.1.55 CANFD0_CH0_TTIR

TT Interrupt Register

Address: 0x40520120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	GTW	SWE	TTMI	RTMI	SOG	CSM_	SMC	SBC

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	IWT	ELC	SE2	SE1	TXO	TXU	GTE	GTD

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW	RW	RW
Name	None [23:19]					CER	AW	WT

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
18	CER	Configuration Error Trigger out of order. 0= No error found in trigger list 1= Error found in trigger list Default Value: 0
17	AW	Application Watchdog 0= Application watchdog served in time 1= Application watchdog not served in time Default Value: 0
16	WT	Watch Trigger 0= No missing reference message 1= Missing reference message (Level 0: cycle time 0xFF00) Default Value: 0
15	IWT	Initialization Watch Trigger The initialization is restarted by resetting IWT. 0= No missing reference message during system startup 1= No system startup due to missing reference message Default Value: 0

22.1.55 CANFD0_CH0_TTIR (continued)

14	ELC	Error Level Changed Not set when error level changed during initialization. 0= No change in error level 1= Error level changed Default Value: 0
13	SE2	Scheduling Error 2 0= No scheduling error 2 1= Scheduling error 2 occurred Default Value: 0
12	SE1	Scheduling Error 1 0= No scheduling error 1 1= Scheduling error 1 occurred Default Value: 0
11	TXO	Tx Count Overflow 0= Number of Tx Trigger as expected 1= More Tx trigger than expected in one matrix cycle Default Value: 0
10	TXU	Tx Count Underflow 0= Number of Tx Trigger as expected 1= Less Tx trigger than expected in one matrix cycle Default Value: 0
9	GTE	Global Time Error Synchronization deviation SD exceeds limit specified by TTOCF.LDSDL, TTCAN Level 0,2 only. 0= Synchronization deviation within limit 1= Synchronization deviation exceeded limit Default Value: 0
8	GTD	Global Time Discontinuity 0= No discontinuity of global time 1= Discontinuity of global time Default Value: 0
7	GTW	Global Time Wrap 0= No global time wrap occurred 1= Global time wrap from 0xFFFF to 0x0000 occurred Default Value: 0
6	SWE	Stop Watch Event 0= No rising/falling edge at stop watch trigger pin m_ttcan_swt detected 1= Rising/falling edge at stop watch trigger pin m_ttcan_swt detected Default Value: 0
5	TTMI	Trigger Time Mark Event Internal Internal time mark events are configured by trigger memory element TMIN (see Section 2.4.7). Set when the trigger memory element becomes active, and the M_TTCAN is in synchronization state In_Gap or In_Schedule. 0= Time mark not reached 1= Time mark reached (Level 0: cycle time TTOCF.IRTO * 0x200) Default Value: 0

22.1.55 CANFD0_CH0_TTIR (continued)

4	RTMI	Register Time Mark Interrupt Set when time referenced by TTOCN.TMC (cycle, local, or global) equals TTTMK.TM, independent of the synchronization state. 0= Time mark not reached 1= Time mark reached Default Value: 0
3	SOG	Start of Gap 0= No reference message seen with Next_is_Gap bit set 1= Reference message with Next_is_Gap bit set becomes valid Default Value: 0
2	CSM_	Change of Synchronization Mode 0= No change in master to slave relation or schedule synchronization 1= Master to slave relation or schedule synchronization changed, also set when TTOST.SPL is reset Default Value: 0
1	SMC	Start of Matrix Cycle 0= No Matrix Cycle started since bit has been reset 1= Matrix Cycle started Default Value: 0
0	SBC	Start of Basic Cycle 0= No Basic Cycle started since bit has been reset 1= Basic Cycle started Default Value: 0

22.1.56 CANFD0_CH0_TTIE

TT Interrupt Enable

Address: 0x40520124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	GTWE	SWEE	TTMIE	RTMIE	SOGE	CSME	SMCE	SBCE

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	IWTE	ELCE	SE2E	SE1E	TXOE	TXUE	GTEE	GTDE

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [23:19]					CERE	AWE_	WTE

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
18	CERE	Configuration Error Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
17	AWE_	Application Watchdog Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
16	WTE	Watch Trigger Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
15	IWTE	Initialization Watch Trigger Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0

22.1.56 CANFD0_CH0_TTIE (continued)

14	ELCE	Change Error Level Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
13	SE2E	Scheduling Error 2 Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
12	SE1E	Scheduling Error 1 Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
11	TXOE	Tx Count Overflow Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
10	TXUE	Tx Count Underflow Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
9	GTEE	Global Time Error Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
8	GTDE	Global Time Discontinuity Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
7	GTWE	Global Time Wrap Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
6	SWEE	Stop Watch Event Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
5	TTMIE	Trigger Time Mark Event Internal Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
4	RTMIE	Register Time Mark Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
3	SOGE	Start of Gap Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0

22.1.56 CANFD0_CH0_TTIE (continued)

2	CSME	Change of Synchronization Mode Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
1	SMCE	Start of Matrix Cycle Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
0	SBCE	Start of Basic Cycle Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0

22.1.57 CANFD0_CH0_TTILS

TT Interrupt Line Select

Address: 0x40520128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	GTWL	SWEL	TTMIL	RTMIL	SOGL	CSML	SMCL	SBCL

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	IWTL	ELCL	SE2L	SE1L	TXOL	TXUL	GTEL	GTDL

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [23:19]					CERL	AWL_	WTL

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
18	CERL	Configuration Error Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
17	AWL_	Application Watchdog Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
16	WTL	Watch Trigger Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
15	IWTL	Initialization Watch Trigger Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0

22.1.57 CANFD0_CH0_TTILS (continued)

14	ELCL	Change Error Level Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
13	SE2L	Scheduling Error 2 Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
12	SE1L	Scheduling Error 1 Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
11	TXOL	Tx Count Overflow Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
10	TXUL	Tx Count Underflow Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
9	GTEL	Global Time Error Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
8	GTDL	Global Time Discontinuity Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
7	GTWL	Global Time Wrap Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
6	SWEL	Stop Watch Event Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
5	TTMIL	Trigger Time Mark Event Internal Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
4	RTMIL	Register Time Mark Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
3	SOGL	Start of Gap Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0

22.1.57 CANFD0_CH0_TTILS (continued)

2	CSML	Change of Synchronization Mode Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
1	SMCL	Start of Matrix Cycle Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
0	SBCL	Start of Basic Cycle Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0

22.1.58 CANFD0_CH0_TTOST

TT Operation Status

Address: 0x4052012C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R		R		R	
HW Access	RW	RW	RW		RW		RW	
Name	QCS	QGTP	SYS [5:4]		MS [3:2]		EL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	RTO [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	None					
HW Access	RW	RW	None					
Name	GFI	WGTD	None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	R	R	R		
HW Access	RW	RW	RW	RW	RW	RW		
Name	SPL	WECS	AWE	WFE	GSI	TMP [26:24]		

Bits	Name	Description
31	SPL	Schedule Phase Lock The bit is valid only when external synchronization is enabled (TTOCN.ESCN = '1'). In this case it signals that the difference between cycle time configured by TTGTP.CTP and the cycle time at the rising edge at pin m_ttcan_evt is less or equal 9 NTU (see Section 4.11). 0= Phase outside range 1= Phase inside range Default Value: 0
30	WECS	Wait for External Clock Synchronization 0= No external clock synchronization pending 1= Node waits for external clock synchronization to take effect. The bit is reset at the start of the next basic cycle. Default Value: 0

22.1.58 CANFD0_CH0_TTOST (continued)

29	AWE	Application Watchdog Event The application watchdog is served by reading TTOST. When the watchdog is not served in time, bit AWE is set, all TTCAN communication is stopped, and the M_TTCAN is set into Bus Monitoring Mode. 0= Application Watchdog served in time 1= Failed to serve Application Watchdog in time Default Value: 0
28	WFE	Wait for Event 0= No Gap announced, reset by a reference message with Next_is_Gap = '0' 1= Reference message with Next_is_Gap = '1' received Default Value: 0
27	GSI	Gap Started Indicator 0= No Gap in schedule, reset by each reference message and for all time slaves 1= Gap time after Basic Cycle has started Default Value: 0
26 : 24	TMP	Time Master Priority 0x0-7 Priority of actual Time Master Default Value: 0
23	GFI	Gap Finished Indicator Set when the CPU writes TTOCN.FGP, or by a time mark interrupt if TMG = '1', or via input pin m_ttcan_evt if TTOCN.GCS = '1'. Not set by Ref_Trigger_Gap or when Gap is finished by another node sending a reference message. 0= Reset at the end of each reference message 1= Gap finished by M_TTCAN Default Value: 0
22	WGTD	Wait for Global Time Discontinuity 0= No global time preset pending 1= Node waits for the global time preset to take effect. The bit is reset when the node has transmitted a reference message with Disc_Bit = '1' or after it received a reference message. Default Value: 0
15 : 8	RTO	Reference Trigger Offset The Reference Trigger Offset value is a signed integer with a range from -127 (0x81) to 127 (0x7F). There is no notification when the lower limit of -127 is reached. In case the M_TTCAN becomes Time Master (MS[1:0] = '11'), the reset of RTO is delayed due to synchronization between Host and CAN clock domain. For time slaves the value configured by TTOCF.IRTO is read. 0x00-FF Actual Reference Trigger offset value Default Value: 0
7	QCS	Quality of Clock Speed Only relevant in TTCAN Level 0 and Level 2, otherwise fixed to '1'. 0= Local clock speed not synchronized to Time Master clock speed 1= Synchronization Deviation <= SDL Default Value: 0
6	QGTP	Quality of Global Time Phase Only relevant in TTCAN Level 0 and Level 2, otherwise fixed to '0'. 0= Global time not valid 1= Global time in phase with Time Master Default Value: 0

22.1.58 CANFD0_CH0_TTOST (continued)

5 : 4	SYS	Synchronization State 00= Out of Synchronization 01= Synchronizing to TTCAN communication 10= Schedule suspended by Gap (In_Gap) 11= Synchronized to schedule (In_Schedule) Default Value: 0
3 : 2	MS	Master State 00= Master_Off, no master properties relevant 01= Operating as Time Slave 10= Operating as Backup Time Master 11= Operating as current Time Master Default Value: 0
1 : 0	EL	Error Level 00= Severity 0 - No Error 01= Severity 1 - Warning 10= Severity 2 - Error 11= Severity 3 - Severe Error Default Value: 0

22.1.59 CANFD0_CH0_TURNA

TUR Numerator Actual

Address: 0x40520130

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	NAV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	NAV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						R	
HW Access	None						RW	
Name	None [23:18]						NAV [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 0	NAV	Numerator Actual Value 0x0EFFF reserved 0x0F000-20FFF Actual numerator value 0x21000 reserved Default Value: 0x10000

22.1.60 CANFD0_CH0_TTLGT

TT Local & Global Time

Address: 0x40520134

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	LT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	LT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	GT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	GT [31:24]							

Bits	Name	Description
31 : 16	GT	Global Time Non-fractional part of the sum of the node's local time and its local offset (see Section 4.5). 0x0000-FFFF Global time value of TTCAN network Default Value: 0
15 : 0	LT	Local Time Non-fractional part of local time, incremented once each local NTU (see Section 4.5). 0x0000-FFFF Local time value of TTCAN node Default Value: 0

22.1.61 CANFD0_CH0_TTCTC

TT Cycle Time & Count

Address: 0x40520138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		R					
HW Access	None		RW					
Name	None [23:22]		CC [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21 : 16	CC	Cycle Count 0x00-3F Number of actual Basic Cycle in the System Matrix Default Value: 0x3F
15 : 0	CT	Cycle Time Non-fractional part of the difference of the node's local time and Ref_Mark (see Section 4.5). 0x0000-FFFF Cycle time value of TTCAN Basic Cycle Default Value: 0

22.1.62 CANFD0_CH0_TTCPT

TT Capture Time

Address: 0x4052013C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R					
HW Access	None		RW					
Name	None [7:6]		CCV [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	SWV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	SWV [31:24]							

Bits	Name	Description
31 : 16	SWV	Stop Watch Value On a rising/falling edge (as configured via TTOCN.SWP) at the Stop Watch Trigger pin m_ttcan_swt, when TTOCN.SWS is != '00' and TTIR.SWE is '0', the actual time value as selected by TTOCN.SWS (cycle, local, global) is copied to SWV and TTIR.SWE will be set to '1'. Capturing of the next stop watch value is enabled by resetting TTIR.SWE. 0x0000-FFFF Captured Stop Watch value Default Value: 0
5 : 0	CCV	Cycle Count Value Cycle count value captured together with SWV. 0x00-3F Captured cycle count value Default Value: 0

22.1.63 CANFD0_CH0_TTCSM

TT Cycle Sync Mark

Address: 0x40520140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CSM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CSM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CSM	Cycle Sync Mark The Cycle Sync Mark is measured Default Value: 0

22.1.64 CANFD0_CH0_RXFTOP_CTL

Receive FIFO Top control

Address: 0x40520180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						F1TPE	F0TPE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	F1TPE	FIFO 1 Top Pointer Enable. Default Value: 0
0	F0TPE	FIFO 0 Top Pointer Enable. This enables the FIFO top pointer logic to set the FIFO Top Address (FnTA) and message word counter. This logic is also disabled when the IP is being reconfigured (CCCR.CCE=1). When this logic is disabled a Read from RXFTOP0_DATA is undefined. Default Value: 0

22.1.65 CANFD0_CH0_RXFTOP0_STAT

Receive FIFO 0 Top Status

Address: 0x405201A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	F0TA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	F0TA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	F0TA	Current FIFO 0 Top Address. This is a pointer to the next word in the message buffer defined by the FIFO Start Address (FnSA), Get Index (FnGI), the FIFO message size (FnDS) and the message word counter (FnMWC) FnTA = FnSA + FnGI * msg_size[FnDS] + FnMWC Default Value: 0

22.1.66 CANFD0_CH0_RXFTOP0_DATA

Receive FIFO 0 Top Data

Address: 0x405201A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	F0TD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	F0TD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	F0TD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	F0TD [31:24]							

Bits	Name	Description
31 : 0	F0TD	When enabled (F0TPE=1) read data from MRAM at location FnTA. This register can have a read side effect if the following conditions are met: - M_TTCAN not being reconfigured (CCCR.CCE=0) - FIFO Top Pointer logic is enabled (FnTPE=1) - FIFO is not empty (FnFL!=0) The read side effect is as follows: - if FnMWC pointed to the last word of the message (as indicated by FnDS) then the corresponding message index (FnGI) is automatically acknowledge by a write to FnAI - FnMWC is incremented (or restarted if FnMWC pointed to the last word of the message) - the FIFO top address FnTA is incremented (with FIFO wrap around) When this logic is disabled (F0TPE=0) a Read from this register returns undefined data. Default Value: Undefined

22.1.67 CANFD0_CH0_RXFTOP1_STAT

Receive FIFO 1 Top Status

Address: 0x405201B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	F1TA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	F1TA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	F1TA	See F0TA description Default Value: 0

22.1.68 CANFD0_CH0_RXFTOP1_DATA

Receive FIFO 1 Top Data

Address: 0x405201B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	F1TD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	F1TD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	F1TD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	F1TD [31:24]							

Bits	Name	Description
31 : 0	F1TD	See F0TD description Default Value: Undefined

22.1.69 CANFD0_CTL

Global CAN control register

Address: 0x40521000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							STOP_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	MRAM_OFF	None [30:24]						

Bits	Name	Description
31	MRAM_OFF	MRAM off 0= Default MRAM on (with MRAM retained in DeepSleep). 1= Switch MRAM off (not retained) to save power. Before setting this bit all the CAN channels have to be powered down using the STOP_REQ/ACK bits. When the MRAM is off any access attempt to it is considered an address error (as if MRAM_-SIZE=0). After switching the MRAM on again software needs to allow for a certain power up time before MRAM can be used, i.e. before STOP_REQ can be de-asserted. The power up time is equivalent to the system SRAM power up time specified in the CPUSS.RAM_PWR_DELAY_CTL register. MRAM_OFF should be set to 0 prior to transitioning to Hibernate mode. Default Value: 0
0	STOP_REQ	Clock Stop Request for each TTCAN IP . The m_ttcan_clkstop_req of each TTCAN IP is directly driven by these bits. Default Value: 0

22.1.70 CANFD0_STATUS

Global CAN status register

Address: 0x40521004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							STOP_ACK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	STOP_ACK	Clock Stop Acknowledge for each TTCAN IP. These bits are directly driven by m_ttcan_clkstop_ack of each TTCAN IP. When this bit is set the corresponding TTCAN IP clocks will be gated off, except HCLK will enabled for each AHB write Default Value: 0

22.1.71 CANFD0_INTR0_CAUSE

Consolidated interrupt0 cause register

Address: 0x40521010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							INT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	INT0	Show pending m_ttcan_int0 of each channel Default Value: 0

22.1.72 CANFD0_INTR1_CAUSE

Consolidated interrupt1 cause register

Address: 0x40521014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							INT1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	INT1	Show pending m_ttcan_int1 of each channel Default Value: 0

22.1.73 CANFD0_TS_CTL

Time Stamp control register

Address: 0x40521020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PRESCALE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PRESCALE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	Counter enable bit 0 = Count disabled. Stop counting up and keep the counter value 1 = Count enabled. Start counting up from the current value Default Value: 0
15 : 0	PRESCALE	Time Stamp counter prescale value. When enabled divide the Host clock (HCLK) by PRESCALE+1 to create Time Stamp clock ticks. Default Value: 0

22.1.74 CANFD0_TS_CNT

Time Stamp counter value

Address: 0x40521024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	VALUE	The counter value of the Time Stamp Counter. When enabled this counter will count Time Stamp clock ticks from the pre-scaler. When written this counter and the pre-scaler will reset to 0 (write data is ignored). Default Value: 0

Section H: Peripheral Group 6

This section encompasses the following chapters:

- Serial Communication Block Registers chapter on page 1760

23 Serial Communication Block Registers

This section discusses the Serial Communications Block (SCB) registers. It lists all the registers in mapping tables, in address order

23.1 Register Details

Register	Address	Description
SCB0_CTRL	0x40600000	Generic control
SCB0_SPI_CTRL	0x40600020	SPI control
SCB0_SPI_STATUS	0x40600024	SPI status
SCB0_UART_CTRL	0x40600040	UART control
SCB0_UART_TX_CTRL	0x40600044	UART transmitter control
SCB0_UART_RX_CTRL	0x40600048	UART receiver control
SCB0_UART_RX_STATUS	0x4060004C	UART receiver status
SCB0_UART_FLOW_CTRL	0x40600050	UART flow control
SCB0_I2C_CTRL	0x40600060	I2C control
SCB0_I2C_STATUS	0x40600064	I2C status
SCB0_I2C_M_CMD	0x40600068	I2C master command
SCB0_I2C_S_CMD	0x4060006C	I2C slave command
SCB0_I2C_CFG	0x40600070	I2C configuration
SCB0_TX_CTRL	0x40600200	Transmitter control
SCB0_TX_FIFO_CTRL	0x40600204	Transmitter FIFO control
SCB0_TX_FIFO_STATUS	0x40600208	Transmitter FIFO status
SCB0_TX_FIFO_WR	0x40600240	Transmitter FIFO write
SCB0_RX_CTRL	0x40600300	Receiver control
SCB0_RX_FIFO_CTRL	0x40600304	Receiver FIFO control
SCB0_RX_FIFO_STATUS	0x40600308	Receiver FIFO status
SCB0_RX_MATCH	0x40600310	Slave address and mask
SCB0_RX_FIFO_RD	0x40600340	Receiver FIFO read
SCB0_RX_FIFO_RD_SILENT	0x40600344	Receiver FIFO read silent
SCB0_EZ_DATA0	0x40600400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB0_EZ_DATA0 to SCB0_EZ_DATA255).
SCB0_INTR_CAUSE	0x40600E00	Active clocked interrupt signal
SCB0_INTR_M	0x40600F00	Master interrupt request

Register	Address	Description
SCB0_INTR_M_SET	0x40600F04	Master interrupt set request
SCB0_INTR_M_MASK	0x40600F08	Master interrupt mask
SCB0_INTR_M_MASKED	0x40600F0C	Master interrupt masked request
SCB0_INTR_S	0x40600F40	Slave interrupt request
SCB0_INTR_S_SET	0x40600F44	Slave interrupt set request
SCB0_INTR_S_MASK	0x40600F48	Slave interrupt mask
SCB0_INTR_S_MASKED	0x40600F4C	Slave interrupt masked request
SCB0_INTR_TX	0x40600F80	Transmitter interrupt request
SCB0_INTR_TX_SET	0x40600F84	Transmitter interrupt set request
SCB0_INTR_TX_MASK	0x40600F88	Transmitter interrupt mask
SCB0_INTR_TX_MASKED	0x40600F8C	Transmitter interrupt masked request
SCB0_INTR_RX	0x40600FC0	Receiver interrupt request
SCB0_INTR_RX_SET	0x40600FC4	Receiver interrupt set request
SCB0_INTR_RX_MASK	0x40600FC8	Receiver interrupt mask
SCB0_INTR_RX_MASKED	0x40600FCC	Receiver interrupt masked request
SCB1_CTRL	0x40610000	Generic control. See SCB0_CTRL for the details of bit fields.
SCB1_SPI_CTRL	0x40610020	SPI control. See SCB0_SPI_CTRL for the details of bit fields.
SCB1_SPI_STATUS	0x40610024	SPI status. See SCB0_SPI_STATUS for the details of bit fields.
SCB1_UART_CTRL	0x40610040	UART control. See SCB0_UART_CTRL for the details of bit fields.
SCB1_UART_TX_CTRL	0x40610044	UART transmitter control. See SCB0_UART_TX_CTRL for the details of bit fields.
SCB1_UART_RX_CTRL	0x40610048	UART receiver control. See SCB0_UART_RX_CTRL for the details of bit fields.
SCB1_UART_RX_STATUS	0x4061004C	UART receiver status. See SCB0_UART_RX_STATUS for the details of bit fields.
SCB1_UART_FLOW_CTRL	0x40610050	UART flow control. See SCB0_UART_FLOW_CTRL for the details of bit fields.
SCB1_I2C_CTRL	0x40610060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB1_I2C_STATUS	0x40610064	I2C status. See SCB0_I2C_STATUS for the details of bit fields.
SCB1_I2C_M_CMD	0x40610068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB1_I2C_S_CMD	0x4061006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB1_I2C_CFG	0x40610070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB1_TX_CTRL	0x40610200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB1_TX_FIFO_CTRL	0x40610204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB1_TX_FIFO_STATUS	0x40610208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB1_TX_FIFO_WR	0x40610240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB1_RX_CTRL	0x40610300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB1_RX_FIFO_CTRL	0x40610304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB1_RX_FIFO_STATUS	0x40610308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB1_RX_MATCH	0x40610310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB1_RX_FIFO_RD	0x40610340	Receiver FIFO read. See SCB0_RX_FIFO_RD for the details of bit fields.
SCB1_RX_FIFO_RD_SILENT	0x40610344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENTfor the details of bit fields.
SCB1_EZ_DATA0	0x40610400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB1_EZ_-DATA0 to SCB1_EZ_DATA255). See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_INTR_CAUSE	0x40610E00	Active clocked interrupt signal. See SCB0_INTR_CAUSE for the details of bit fields.
SCB1_INTR_M	0x40610F00	Master interrupt request. See SCB0_INTR_M for the details of bit fields.
SCB1_INTR_M_SET	0x40610F04	Master interrupt set request. See SCB0_INTR_M_SETfor the details of bit fields.

Register	Address	Description
SCB1_INTR_M_MASK	0x40610F08	Master interrupt mask. See SCB0_INTR_M_MASKfor the details of bit fields.
SCB1_INTR_M_MASKED	0x40610F0C	Master interrupt masked request. See SCB0_INTR_M_MASKED for the details of bit fields.
SCB1_INTR_S	0x40610F40	Slave interrupt request. See SCB0_INTR_S for the details of bit fields.
SCB1_INTR_S_SET	0x40610F44	Slave interrupt set request. See SCB0_INTR_S_SET for the details of bit fields.
SCB1_INTR_S_MASK	0x40610F48	Slave interrupt mask. See SCB0_INTR_S_MASK for the details of bit fields.
SCB1_INTR_S_MASKED	0x40610F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKED for the details of bit fields.
SCB1_INTR_TX	0x40610F80	Transmitter interrupt request. See SCB0_INTR_TX for the details of bit fields.
SCB1_INTR_TX_SET	0x40610F84	Transmitter interrupt set request. See SCB0_INTR_TX_SET for the details of bit fields.
SCB1_INTR_TX_MASK	0x40610F88	Transmitter interrupt mask. See SCB0_INTR_TX_MASK for the details of bit fields.
SCB1_INTR_TX_MASKED	0x40610F8C	Transmitter interrupt masked request. See SCB0_INTR_TX_MASKEDfor the details of bit fields.
SCB1_INTR_RX	0x40610FC0	Receiver interrupt request. See SCB0_INTR_RX for the details of bit fields.
SCB1_INTR_RX_SET	0x40610FC4	Receiver interrupt set request. See SCB0_INTR_RX_SET for the details of bit fields.
SCB1_INTR_RX_MASK	0x40610FC8	Receiver interrupt mask. See SCB0_INTR_RX_MASK for the details of bit fields.
SCB1_INTR_RX_MASKED	0x40610FCC	Receiver interrupt masked request. See SCB0_INTR_RX_MASKED for the details of bit fields.
SCB2_CTRL	0x40620000	Generic control. See SCB0_CTRL for the details of bit fields.
SCB2_SPI_CTRL	0x40620020	SPI control. See SCB0_SPI_CTRL for the details of bit fields.
SCB2_SPI_STATUS	0x40620024	SPI status. See SCB0_SPI_STATUS for the details of bit fields.
SCB2_UART_CTRL	0x40620040	UART control. See SCB0_UART_CTRL for the details of bit fields.
SCB2_UART_TX_CTRL	0x40620044	UART transmitter control. See SCB0_UART_TX_CTRL for the details of bit fields.
SCB2_UART_RX_CTRL	0x40620048	UART receiver control. See SCB0_UART_RX_CTRL for the details of bit fields.
SCB2_UART_RX_STATUS	0x4062004C	UART receiver status. See SCB0_UART_RX_STATUS for the details of bit fields.
SCB2_UART_FLOW_CTRL	0x40620050	UART flow control. See SCB0_UART_FLOW_CTRL for the details of bit fields.
SCB2_I2C_CTRL	0x40620060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB2_I2C_STATUS	0x40620064	I2C status. See SCB0_I2C_STATUS for the details of bit fields.
SCB2_I2C_M_CMD	0x40620068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB2_I2C_S_CMD	0x4062006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB2_I2C_CFG	0x40620070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB2_TX_CTRL	0x40620200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB2_TX_FIFO_CTRL	0x40620204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB2_TX_FIFO_STATUS	0x40620208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB2_TX_FIFO_WR	0x40620240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB2_RX_CTRL	0x40620300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB2_RX_FIFO_CTRL	0x40620304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB2_RX_FIFO_STATUS	0x40620308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB2_RX_MATCH	0x40620310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB2_RX_FIFO_RD	0x40620340	Receiver FIFO read. See SCB0_RX_FIFO_RD for the details of bit fields.
SCB2_RX_FIFO_RD_SILENT	0x40620344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB2_EZ_DATA0	0x40620400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB2_EZ_-DATA0 to SCB2_EZ_DATA255). See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_INTR_CAUSE	0x40620E00	Active clocked interrupt signal. See SCB0_INTR_CAUSE for the details of bit fields.
SCB2_INTR_M	0x40620F00	Master interrupt request. See SCB0_INTR_M for the details of bit fields.
SCB2_INTR_M_SET	0x40620F04	Master interrupt set request. See SCB0_INTR_M_SETfor the details of bit fields.
SCB2_INTR_M_MASK	0x40620F08	Master interrupt mask. See SCB0_INTR_M_MASKfor the details of bit fields.

Register	Address	Description
SCB2_INTR_M_MASKED	0x40620F0C	Master interrupt masked request. See SCB0_INTR_M_MASKED for the details of bit fields.
SCB2_INTR_S	0x40620F40	Slave interrupt request. See SCB0_INTR_S for the details of bit fields.
SCB2_INTR_S_SET	0x40620F44	Slave interrupt set request. See SCB0_INTR_S_SET for the details of bit fields.
SCB2_INTR_S_MASK	0x40620F48	Slave interrupt mask. See SCB0_INTR_S_MASK for the details of bit fields.
SCB2_INTR_S_MASKED	0x40620F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKED for the details of bit fields.
SCB2_INTR_TX	0x40620F80	Transmitter interrupt request. See SCB0_INTR_TX for the details of bit fields.
SCB2_INTR_TX_SET	0x40620F84	Transmitter interrupt set request. See SCB0_INTR_TX_SET for the details of bit fields.
SCB2_INTR_TX_MASK	0x40620F88	Transmitter interrupt mask. See SCB0_INTR_TX_MASK for the details of bit fields.
SCB2_INTR_TX_MASKED	0x40620F8C	Transmitter interrupt masked request. See SCB0_INTR_TX_MASKEDfor the details of bit fields.
SCB2_INTR_RX	0x40620FC0	Receiver interrupt request. See SCB0_INTR_RX for the details of bit fields.
SCB2_INTR_RX_SET	0x40620FC4	Receiver interrupt set request. See SCB0_INTR_RX_SET for the details of bit fields.
SCB2_INTR_RX_MASK	0x40620FC8	Receiver interrupt mask. See SCB0_INTR_RX_MASK for the details of bit fields.
SCB2_INTR_RX_MASKED	0x40620FCC	Receiver interrupt masked request. See SCB0_INTR_RX_MASKED for the details of bit fields.
SCB4_CTRL	0x40640000	Generic control. See SCB0_CTRL for the details of bit fields.
SCB4_SPI_CTRL	0x40640020	SPI control. See SCB0_SPI_CTRL for the details of bit fields.
SCB4_SPI_STATUS	0x40640024	SPI status. See SCB0_SPI_STATUS for the details of bit fields.
SCB4_UART_CTRL	0x40640040	UART control. See SCB0_UART_CTRL for the details of bit fields.
SCB4_UART_TX_CTRL	0x40640044	UART transmitter control. See SCB0_UART_TX_CTRL for the details of bit fields.
SCB4_UART_RX_CTRL	0x40640048	UART receiver control. See SCB0_UART_RX_CTRL for the details of bit fields.
SCB4_UART_RX_STATUS	0x4064004C	UART receiver status. See SCB0_UART_RX_STATUS for the details of bit fields.
SCB4_UART_FLOW_CTRL	0x40640050	UART flow control. See SCB0_UART_FLOW_CTRL for the details of bit fields.
SCB4_I2C_CTRL	0x40640060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB4_I2C_STATUS	0x40640064	I2C status. See SCB0_I2C_STATUS for the details of bit fields.
SCB4_I2C_M_CMD	0x40640068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB4_I2C_S_CMD	0x4064006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB4_I2C_CFG	0x40640070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB4_TX_CTRL	0x40640200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB4_TX_FIFO_CTRL	0x40640204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB4_TX_FIFO_STATUS	0x40640208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB4_TX_FIFO_WR	0x40640240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB4_RX_CTRL	0x40640300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB4_RX_FIFO_CTRL	0x40640304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB4_RX_FIFO_STATUS	0x40640308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB4_RX_MATCH	0x40640310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB4_RX_FIFO_RD	0x40640340	Receiver FIFO read. See SCB0_RX_FIFO_RD for the details of bit fields.
SCB4_RX_FIFO_RD_SILENT	0x40640344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB4_EZ_DATA0	0x40640400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB4_EZ_-DATA0 to SCB4_EZ_DATA255). See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_INTR_CAUSE	0x40640E00	Active clocked interrupt signal. See SCB0_INTR_CAUSE for the details of bit fields.
SCB4_INTR_M	0x40640F00	Master interrupt request. See SCB0_INTR_M for the details of bit fields.
SCB4_INTR_M_SET	0x40640F04	Master interrupt set request. See SCB0_INTR_M_SETfor the details of bit fields.
SCB4_INTR_M_MASK	0x40640F08	Master interrupt mask. See SCB0_INTR_M_MASKfor the details of bit fields.
SCB4_INTR_M_MASKED	0x40640F0C	Master interrupt masked request. See SCB0_INTR_M_MASKED for the details of bit fields.

Register	Address	Description
SCB4_INTR_S	0x40640F40	Slave interrupt request. See SCB0_INTR_S for the details of bit fields.
SCB4_INTR_S_SET	0x40640F44	Slave interrupt set request. See SCB0_INTR_S_SET for the details of bit fields.
SCB4_INTR_S_MASK	0x40640F48	Slave interrupt mask. See SCB0_INTR_S_MASK for the details of bit fields.
SCB4_INTR_S_MASKED	0x40640F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKED for the details of bit fields.
SCB4_INTR_TX	0x40640F80	Transmitter interrupt request. See SCB0_INTR_TX for the details of bit fields.
SCB4_INTR_TX_SET	0x40640F84	Transmitter interrupt set request. See SCB0_INTR_TX_SET for the details of bit fields.
SCB4_INTR_TX_MASK	0x40640F88	Transmitter interrupt mask. See SCB0_INTR_TX_MASK for the details of bit fields.
SCB4_INTR_TX_MASKED	0x40640F8C	Transmitter interrupt masked request. See SCB0_INTR_TX_MASKEDfor the details of bit fields.
SCB4_INTR_RX	0x40640FC0	Receiver interrupt request. See SCB0_INTR_RX for the details of bit fields.
SCB4_INTR_RX_SET	0x40640FC4	Receiver interrupt set request. See SCB0_INTR_RX_SET for the details of bit fields.
SCB4_INTR_RX_MASK	0x40640FC8	Receiver interrupt mask. See SCB0_INTR_RX_MASK for the details of bit fields.
SCB4_INTR_RX_MASKED	0x40640FCC	Receiver interrupt masked request. See SCB0_INTR_RX_MASKED for the details of bit fields.
SCB5_CTRL	0x40650000	Generic control. See SCB0_CTRL for the details of bit fields.
SCB5_SPI_CTRL	0x40650020	SPI control. See SCB0_SPI_CTRL for the details of bit fields.
SCB5_SPI_STATUS	0x40650024	SPI status. See SCB0_SPI_STATUS for the details of bit fields.
SCB5_UART_CTRL	0x40650040	UART control. See SCB0_UART_CTRL for the details of bit fields.
SCB5_UART_TX_CTRL	0x40650044	UART transmitter control. See SCB0_UART_TX_CTRL for the details of bit fields.
SCB5_UART_RX_CTRL	0x40650048	UART receiver control. See SCB0_UART_RX_CTRL for the details of bit fields.
SCB5_UART_RX_STATUS	0x4065004C	UART receiver status. See SCB0_UART_RX_STATUS for the details of bit fields.
SCB5_UART_FLOW_CTRL	0x40650050	UART flow control. See SCB0_UART_FLOW_CTRL for the details of bit fields.
SCB5_I2C_CTRL	0x40650060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB5_I2C_STATUS	0x40650064	I2C status. See SCB0_I2C_STATUS for the details of bit fields.
SCB5_I2C_M_CMD	0x40650068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB5_I2C_S_CMD	0x4065006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB5_I2C_CFG	0x40650070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB5_TX_CTRL	0x40650200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB5_TX_FIFO_CTRL	0x40650204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB5_TX_FIFO_STATUS	0x40650208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB5_TX_FIFO_WR	0x40650240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB5_RX_CTRL	0x40650300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB5_RX_FIFO_CTRL	0x40650304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB5_RX_FIFO_STATUS	0x40650308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB5_RX_MATCH	0x40650310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB5_RX_FIFO_RD	0x40650340	Receiver FIFO read. See SCB0_RX_FIFO_RD for the details of bit fields.
SCB5_RX_FIFO_RD_SILENT	0x40650344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB5_EZ_DATA0	0x40650400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB5_EZ_-DATA0 to SCB5_EZ_DATA255). See SCB0_EZ_DATA0 for the details of bit fields.
SCB5_INTR_CAUSE	0x40650E00	Active clocked interrupt signal. See SCB0_INTR_CAUSE for the details of bit fields.
SCB5_INTR_M	0x40650F00	Master interrupt request. See SCB0_INTR_M for the details of bit fields.
SCB5_INTR_M_SET	0x40650F04	Master interrupt set request. See SCB0_INTR_M_SETfor the details of bit fields.
SCB5_INTR_M_MASK	0x40650F08	Master interrupt mask. See SCB0_INTR_M_MASKfor the details of bit fields.
SCB5_INTR_M_MASKED	0x40650F0C	Master interrupt masked request. See SCB0_INTR_M_MASKED for the details of bit fields.

Register	Address	Description
SCB5_INTR_S	0x40650F40	Slave interrupt request. See SCB0_INTR_S for the details of bit fields.
SCB5_INTR_S_SET	0x40650F44	Slave interrupt set request. See SCB0_INTR_S_SET for the details of bit fields.
SCB5_INTR_S_MASK	0x40650F48	Slave interrupt mask. See SCB0_INTR_S_MASK for the details of bit fields.
SCB5_INTR_S_MASKED	0x40650F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKED for the details of bit fields.
SCB5_INTR_TX	0x40650F80	Transmitter interrupt request. See SCB0_INTR_TX for the details of bit fields.
SCB5_INTR_TX_SET	0x40650F84	Transmitter interrupt set request. See SCB0_INTR_TX_SET for the details of bit fields.
SCB5_INTR_TX_MASK	0x40650F88	Transmitter interrupt mask. See SCB0_INTR_TX_MASK for the details of bit fields.
SCB5_INTR_TX_MASKED	0x40650F8C	Transmitter interrupt masked request. See SCB0_INTR_TX_MASKEDfor the details of bit fields.
SCB5_INTR_RX	0x40650FC0	Receiver interrupt request. See SCB0_INTR_RX for the details of bit fields.
SCB5_INTR_RX_SET	0x40650FC4	Receiver interrupt set request. See SCB0_INTR_RX_SET for the details of bit fields.
SCB5_INTR_RX_MASK	0x40650FC8	Receiver interrupt mask. See SCB0_INTR_RX_MASK for the details of bit fields.
SCB5_INTR_RX_MASKED	0x40650FCC	Receiver interrupt masked request. See SCB0_INTR_RX_MASKED for the details of bit fields.
SCB6_CTRL	0x40660000	Generic control
SCB6_STATUS	0x40660004	Generic status
SCB6_CMD_RESP_CTRL	0x40660008	Command/response control
SCB6_CMD_RESP_STATUS	0x4066000C	Command/response status
SCB6_SPI_CTRL	0x40660020	SPI control. See SCB0_SPI_CTRL for the details of bit fields.
SCB6_SPI_STATUS	0x40660024	SPI status
SCB6_I2C_CTRL	0x40660060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB6_I2C_STATUS	0x40660064	I2C status
SCB6_I2C_M_CMD	0x40660068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB6_I2C_S_CMD	0x4066006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB6_I2C_CFG	0x40660070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB6_TX_CTRL	0x40660200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB6_TX_FIFO_CTRL	0x40660204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB6_TX_FIFO_STATUS	0x40660208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB6_TX_FIFO_WR	0x40660240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB6_RX_CTRL	0x40660300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB6_RX_FIFO_CTRL	0x40660304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB6_RX_FIFO_STATUS	0x40660308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB6_RX_MATCH	0x40660310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB6_RX_FIFO_RD	0x40660340	Receiver FIFO read. See SCB0_RX_FIFO_RD for the details of bit fields.
SCB6_RX_FIFO_RD_SILENT	0x40660344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB6_EZ_DATA0	0x40660400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB6_EZ_-DATA0 to SCB6_EZ_DATA255). See SCB0_EZ_DATA0 for the details of bit fields.
SCB6_INTR_CAUSE	0x40660E00	Active clocked interrupt signal
SCB6_INTR_I2C_EC	0x40660E80	Externally clocked I2C interrupt request
SCB6_INTR_I2C_EC_MASK	0x40660E88	Externally clocked I2C interrupt mask
SCB6_INTR_I2C_EC_MASKED	0x40660E8C	Externally clocked I2C interrupt masked
SCB6_INTR_SPI_EC	0x40660EC0	Externally clocked SPI interrupt request
SCB6_INTR_SPI_EC_MASK	0x40660EC8	Externally clocked SPI interrupt mask
SCB6_INTR_SPI_EC_MASKED	0x40660ECC	Externally clocked SPI interrupt masked
SCB6_INTR_M	0x40660F00	Master interrupt request. See SCB0_INTR_M for the details of bit fields.

Register	Address	Description
SCB6_INTR_M_SET	0x40660F04	Master interrupt set request. See SCB0_INTR_M_SET for the details of bit fields.
SCB6_INTR_M_MASK	0x40660F08	Master interrupt mask. See SCB0_INTR_M_MASK for the details of bit fields.
SCB6_INTR_M_MASKED	0x40660F0C	Master interrupt masked request. See SCB0_INTR_M_MASKED for the details of bit fields.
SCB6_INTR_S	0x40660F40	Slave interrupt request. See SCB0_INTR_S for the details of bit fields.
SCB6_INTR_S_SET	0x40660F44	Slave interrupt set request. See SCB0_INTR_S_SET for the details of bit fields.
SCB6_INTR_S_MASK	0x40660F48	Slave interrupt mask. See SCB0_INTR_S_MASK for the details of bit fields.
SCB6_INTR_S_MASKED	0x40660F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKED for the details of bit fields.
SCB6_INTR_TX	0x40660F80	Transmitter interrupt request
SCB6_INTR_TX_SET	0x40660F84	Transmitter interrupt set request
SCB6_INTR_TX_MASK	0x40660F88	Transmitter interrupt mask
SCB6_INTR_TX_MASKED	0x40660F8C	Transmitter interrupt masked request
SCB6_INTR_RX	0x40660FC0	Receiver interrupt request
SCB6_INTR_RX_SET	0x40660FC4	Receiver interrupt set request
SCB6_INTR_RX_MASK	0x40660FC8	Receiver interrupt mask
SCB6_INTR_RX_MASKED	0x40660FCC	Receiver interrupt masked request

23.1.1 SCB0_CTRL

Generic control

Address: 0x40600000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	None		
HW Access	None				R	None		
Name	None [15:12]				BYTE_-MODE	None [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							ADDR_AC-CEPT

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None					RW	
HW Access	R	None					R	
Name	ENABLED	None [30:26]					MODE [25:24]	

Bits	Name	Description
31	ENABLED	0': Block Disabled '1': Block Enabled The proper order in which to initialize the SCB is as follows: - Program protocol specific information using SPI_CTRL, UART_CTRL (and UART_TX_CTRL and UART_RX_CTRL) or I2C_CTRL. This includes selection of a submode, master/slave functionality and transmitter/receiver functionality when applicable. - Program generic transmitter (TX_CTRL) and receiver (RX_CTRL) information. This includes enabling of the transmitter and receiver functionality. - Program transmitter FIFO (TX_FIFO_CTRL) and receiver FIFO (RX_FIFO_CTRL) information. - Program CTRL to enable SCB, select the specific operation mode and oversampling factor. When the SCB is enabled, no control information should be changed. Changes must be made AFTER disabling the SCB, e.g. to modify the operation mode (from I2C to SPI) or to go from externally to internally clocked. The change takes effect after the SCB is re-enabled. Note that disabling the SCB will cause re-initialization of the design and associated state is lost (e.g. FIFO content). Default Value: 0
25 : 24	MODE	Mode of operation (3: Reserved) Default Value: 3

23.1.1 SCB0_CTRL (continued)

		0x0: I2C : Inter-Integrated Circuits (I2C) mode. **0x1: SPI :** Serial Peripheral Interface (SPI) mode. **0x2: UART :** Universal Asynchronous Receiver/Transmitter (UART) mode.
16	ADDR_ACCEPT	Determines whether a received matching address is accepted in the RX FIFO:. '0': Matching address does not go in RX FIFO '1': Match address does go in RX FIFO In I2C mode, this field is used to allow the slave to put the received slave address or general call address in the RX FIFO. Note that a received matching address is put in the RX FIFO when this bit is '1' for both I2C read and write transfers. In multi-processor UART receiver mode, this field is used to allow the receiver to put the received address in the RX FIFO. Note: non-matching addresses are never put in the RX FIFO. In SPI mode this field must be '0' Default Value: 0
11	BYTE_MODE	Determines the number of bits per FIFO data element: '0': 16-bit FIFO data elements. '1': 8-bit FIFO data elements. This mode doubles the amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 7]. Default Value: 0

23.1.1 SCB0_CTRL (continued)

3 : 0	OVS	Serial interface bit period oversampling factor expressed in clk_scb cycles. clk_scb is the peripheral clock divider connected to the SCB. Used for SPI Master and UART functionality. This field is NOT used in externally clocked mode. This filed is NOT used for SPI slave or I2C mode. OVS + 1 clk_scb cycles constitute a single serial interface clock/bit cycle. If OVS is odd, the oversampling factor is even and the low and high phase of the interface clock period are the same. If OVS is even, the oversampling factor is odd and the low and high phase can differ by 1 SCB clock period. In SPI master mode, the valid range is [3, 15]. The frequency of the SPI Clock is (frequency of clk_scb) / (OVS + 1). For example, is clk_scb is 50 MHz and OVS is 9, then the frequency of SPI Clock is 50 MHz / (9+1) = 5 MHz. If the MISO signal is not used for SPI master the valid range changes to [1,15] In SPI slave mode, the OVS field is NOT used. Refer to the architecture TRM for information on how to configure clk_scb for SPI Slave. Generally, it is recommended that clk_scb be as fast as possible for the slave. In UART standard sub mode (including LIN and Smartcard), the valid range is [7, 15]. In UART IrDA sub mode this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. For normal transmission mode, the pulse is roughly 3/16 of the bit period (for all bit rates). There is only one valid OVS value: - 0: 16 times oversampling. clk_scb frequency = 16*115.2 KHz for 115.2 Kbps. clk_scb frequency = 16*57.6 KHz for 57.6 Kbps. clk_scb frequency = 16*38.4 KHz for 38.4 Kbps. clk_scb frequency = 16*19.2 KHz for 19.2 Kbps. clk_scb frequency = 16*9.6 KHz for 9.6 Kbps. clk_scb frequency = 16*2.4 KHz for 2.4 Kbps. clk_scb frequency = 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. RX_CTRL.MEDIAN must be set to '1' for IrDA receiver functionality. UART IrDA RX Low power mode, OVS field values (with the required clk_scb frequency): - 0: 16 times oversampling. clk_scb frequency = 16*115.2 KHz for 115.2 Kbps. - 1: 32 times oversampling. clk_scb frequency = 32*57.6 KHz for 57.6 Kbps. - 2: 48 times oversampling. clk_scb frequency = 48*38.4 KHz for 38.4 Kbps. - 3: 96 times oversampling. clk_scb frequency = 96*19.2 KHz for 19.2 Kbps. - 4: 192 times oversampling. clk_scb frequency = 192*9.6 KHz for 9.6 Kbps. - 5: 768 times oversampling. clk_scb frequency = 768*2.4 KHz for 2.4 Kbps. - 6: 1536 times oversampling. clk_scb frequency = 1536*1.2 KHz for 1.2 Kbps. - all other values are not used in low power mode. In low power transmission mode, this pulse is potentially smaller (down to 1.62 us typical and 1.41 us minimal) than 3/16 of the bit period (for < 115.2 Kbps bitrates). Pulse widths greater or equal than two SCB clock cycles are guaranteed to be detected by the receiver. Pulse widths less than two SCB clock cycles and greater or equal than one SCB clock cycle may be detected by the receiver. Pulse widths less than one SCB clock cycle will not be detected by the receiver. Default Value: 15

23.1.2 SCB0_SPI_CTRL

SPI control

Address: 0x40600020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		SCLK_-CONTINU-OUS	LATE_MISO_SAMPLE	CPOL	CPHA	SE-LECT_PRE-CEDE	SSEL_-CONTINU-OUS

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SSEL_PO-LARITY3	SSEL_PO-LARITY2	SSEL_PO-LARITY1	SSEL_PO-LARITY0

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None			RW		RW	
HW Access	R	None			R		R	
Name	MASTER_-MODE	None [30:28]			SSEL [27:26]		MODE [25:24]	

Bits	Name	Description
31	MASTER_MODE	Master ('1') or slave ('0') mode. In master mode, transmission will commence on availability of data frames in the TX FIFO. In slave mode, when selected and there is no data frame in the TX FIFO, the slave will transmit all '1's. In both master and slave modes, received data frames will be lost if the RX FIFO is full. Default Value: 0
27 : 26	SSEL	Selects one of the four incoming/outgoing SPI slave select signals: - 0: Slave 0, SSEL[0]. - 1: Slave 1, SSEL[1]. - 2: Slave 2, SSEL[2]. - 3: Slave 3, SSEL[3]. The SCB should be disabled when changes are made to this field. Default Value: 0
25 : 24	MODE	Submode of SPI operation (3: Reserved). Default Value: 3

23.1.2 SCB0_SPI_CTRL (continued)

		0x0: SPI_MOTOROLA: SPI Motorola submode. **0x1: SPI_TI :** SPI Texas Instruments submode. **0x2: SPI_NS :** SPI National Semiconductors submode.
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only used in master mode. Not used in National Semiconductors submode. '0': No local loopback '1': the SPI master MISO line is connected to the SPI master MOSI line. In other words, in loopback mode the SPI master receives on MISO what it transmits on MOSI. Default Value: 0
11	SSEL_POLARITY3	Slave select polarity. Default Value: 0
10	SSEL_POLARITY2	Slave select polarity. Default Value: 0
9	SSEL_POLARITY1	Slave select polarity. Default Value: 0
8	SSEL_POLARITY0	Slave select polarity. SSEL_POLARITY0 applies to the outgoing SPI slave select signal 0 (master mode) and to the incoming SPI slave select signal (slave mode). For Motorola and National Semiconductors submodes: '0': slave select is low/'0' active. '1': slave select is high/'1' active. For Texas Instruments submode: '0': high/'1' active precede/coincide pulse. '1': low/'0' active precede/coincide pulse. Default Value: 0
5	SCLK_CONTINUOUS	Only applicable in master mode. '0': SCLK is generated, when the SPI master is enabled and data is transmitted. '1': SCLK is generated, when the SPI master is enabled. This mode is useful for slave devices that use SCLK for functional operation other than just SPI functionality. Default Value: 0
4	LATE_MISO_SAMPLE	Changes the SCLK edge on which MISO is captured. Only used in master mode. When '0', the default applies (for Motorola as determined by CPOL and CPHA, for Texas Instruments on the falling edge of SCLK and for National Semiconductors on the rising edge of SCLK). When '1', the alternate clock edge is used (which comes half a SPI SCLK period later). Late sampling addresses the round trip delay associated with transmitting SCLK from the master to the slave and transmitting MISO from the slave to the master. Default Value: 0
3	CPOL	Indicates the clock polarity. This field, together with the CPHA field, indicates when MOSI data is driven and MISO data is captured: - CPOL is '0': SCLK is '0' when not transmitting data. - CPOL is '1': SCLK is '1' when not transmitting data. Default Value: 0

23.1.2 SCB0_SPI_CTRL (continued)

2	CPHA	Indicates the clock phase. This field, together with the CPOL field, indicates when MOSI data is driven and MISO data is captured: - Motorola mode 0. CPOL is '0', CPHA is '0': MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. - Motorola mode 1. CPOL is '0', CPHA is '1': MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 2. CPOL is '1', CPHA is '0': MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 3. CPOL is '1', CPHA is '1': MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. In SPI Motorola submode, all four CPOL/CPHA modes are valid. in SPI NS submode, only CPOL=0 CPHA=0 mode is valid. in SPI TI submode, only CPOL=0 CPHA=1 mode is valid. Default Value: 0
1	SELECT_PRECEDE	Only used in SPI Texas Instruments' submode. When '1', the data frame start indication is a pulse on the Slave SELECT line that precedes the transfer of the first data frame bit. When '0', the data frame start indication is a pulse on the Slave SELECT line that coincides with the transfer of the first data frame bit. Default Value: 0
0	SSEL_CONTINUOUS	Continuous SPI data transfers enabled ('1') or not ('0'). This field is used in master mode. In slave mode, both continuous and non-continuous SPI data transfers are supported independent of this field. When continuous transfers are enabled indiviual data transfers are NOT seperated by slave select deselection as long as there is data in the TX FIFO. If the TX FIFO becomes empty then the slave select will be deselected. When continuous transfers are not enabled individual data frame transfers are always seperated by slave select deselection: independent of the availability of TX FIFO data frames. Default Value: 0

23.1.3 SCB0_SPI_STATUS

SPI status

Address: 0x40600024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	BUS_BUSY	SPI bus is busy. The bus is considered busy ('1') during an ongoing transaction. For Motorola and National submodes, the busy bit is '1', when the slave selection is activated. For TI submode, the busy bit is '1' from the time the preceding/coinciding slave select is activated for the first transmitted data frame, till the last MOSI/MISO bit of the last data frame is transmitted. Default Value: Undefined

23.1.4 SCB0_UART_CTRL

UART control

Address: 0x40600040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						MODE [25:24]	

Bits	Name	Description
25 : 24	MODE	Submode of UART operation (3: Reserved) Default Value: 3 **0x0: UART_STD :** Standard UART submode. **0x1: UART_SMARTCARD :** SmartCard (ISO7816) submode. Support for negative acknowledgement (NACK) on the receiver side and retransmission on the transmitter side. **0x2: UART_IRDA :** Infrared Data Association (IrDA) submode. Return to Zero modulation scheme.

23.1.4 SCB0_UART_CTRL (continued)

16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). 0: Loopback is not enabled 1: UART_TX is connected to UART_RX. UART_RTS is connected to UART_CTS. This allows a SCB UART transmitter to communicate with its receiver counterpart. Default Value: 0

23.1.5 SCB0_UART_TX_CTRL

UART transmitter control

Address: 0x40600044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	None	RW		
HW Access	None		R	R	None	R		
Name	None [7:6]		PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RETRY_ON_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	RETRY_ON_NACK	When '1', a data frame is retransmitted when a negative acknowledgement is received. Only applicable to the SmartCard submode. Default Value: 0
5	PARITY_ENABLED	Parity generation enabled ('1') or not ('0'). Only applicable in standard UART submodes. In SmartCard submode, parity generation is always enabled through hardware. In IrDA submode, parity generation is always disabled through hardware Default Value: 0
4	PARITY	Parity bit. When '0', the transmitter generates an even parity. When '1', the transmitter generates an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0
2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of half bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. Default Value: 2

23.1.6 SCB0_UART_RX_CTRL

UART receiver control

Address: 0x40600048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW		
HW Access	None	R	R	R	None	R		
Name	None	POLARITY	PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	None	RW	RW	RW
HW Access	None		R	R	None	R	R	R
Name	None [15:14]		SKIP_START	LIN_MODE	None	MP_MODE	DROP_ON_FRAME_ERROR	DROP_ON_PARITY_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				BREAK_WIDTH [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	BREAK_WIDTH	Break width. BREAK_WIDTH + 1 is the minimum width in bit periods of a break. During a break the transmitted/received line value is '0'. This feature is useful for standard UART submode and LIN submode ("break field" detection). Once, the break is detected, the INTR_RX.BREAK_DETECT bit is set to '1'. Note for LIN the break detection precedes baud rate detection, which is used to synchronize/refine the receiver clock to the transmitter clock. As a result, break detection operates with an unsynchronized/unrefined receiver clock. Therefore, the receiver's definition of a bit period is imprecise and the setting of this field should take this imprecision into account. The LIN standard also accounts for this imprecision: a LIN start bit followed by 8 data bits allows for up to 9 consecutive '0' bit periods during regular transmission, whereas the LIN break detection should be at least 13 consecutive '0' bit periods. This provides for a margin of 4 bit periods. Therefore, the default value of this field is set to 10, representing a minimal break field with of 10+1 = 11 bit periods; a value in between the 9 consecutive bit periods of a regular transmission and the 13 consecutive bit periods of a break field. This provides for slight imprecisions of the receiver clock wrt. the transmitter clock. There should not be a need to program this field to any value other than its default value. Default Value: 10

23.1.6 SCB0_UART_RX_CTRL (continued)

13	SKIP_START	Only applicable in standard UART submode. When '1', the receiver skips start bit detection for the first received data frame. Instead, it synchronizes on the first received data frame bit, which should be a '1'. This functionality is intended for wake up from DeepSleep when receiving a data frame. The transition from idle ('1') to START ('0') on the RX line is used to wake up the CPU. The transition detection (and the associated wake up functionality) is performed by the GPIO. The woken up CPU will enable the SCB's UART receiver functionality. Once enabled, it is assumed that the START bit is ongoing (the CPU wakeup and SCB enable time should be less than the START bit period). The SCB will then synchronize to a '0' to '1' transition, which indicates the first data frame bit is received (first data frame bit should be '1'). After synchronization to the first data frame bit, the SCB will resume normal UART functionality: subsequent data frames will be synchronized on the receipt of a START bit. Default Value: 0
12	LIN_MODE	Only applicable in standard UART submode. When '1', the receiver performs break detection and baud rate detection on the incoming data. First, break detection counts the amount of bit periods that have a line value of '0'. BREAK_WIDTH specifies the minum required amount of bit periods. Successful break detection sets the INTR_RX.BREAK_DETECT interrupt cause to '1'. Second, baud rate detection counts the amount of peripheral clock periods that are use to receive the synchronization byte (0x55; least significant bit first). The count is available through UART_RX_STATUS.BR_COUNTER. Successful baud rate detection sets the INTR_RX.BAUD_DETECT interrupt cause to '1' (BR_COUNTER is reliable). This functionality is used to synchronize/refine the receiver clock to the transmitter clock. The receiver software can use the BR_COUNTER value to set the right clk_scb to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Default Value: 0
10	MP_MODE	Multi-processor mode. When '1', multi-processor mode is enabled. In this mode, RX_CTRL.DATA_WIDTH must be 9 bits. In multi-processor mode, the 9th received bit of a data frame seperates addresses (bit is '1') from data (bit is '0'). A received address is matched with RX_MATCH.DATA and RX_MATCH.MASK. In the case of a match, subsequent received data is sent to the RX FIFO. In the case of NO match, subsequent received data is dropped. Default Value: 0
9	DROP_ON_FRAME_ERROR	Behaviour when an error is detected in a start or stop period. When '0', received data is sent to the RX FIFO. When '1', received data is dropped and lost. Default Value: 0
8	DROP_ON_PARITY_ERROR	Behavior when a parity check fails. When '0', received data is send to the RX FIFO. When '1', received data is dropped and lost. Only applicable in standard UART and SmartCard submodes (negatively acknowledged SmartCard data frames may be dropped with this field). Default Value: 0
6	POLARITY	Inverts incoming RX line signal "uart_rx_in". Inversion is after local loopback. This functionality only works for IrDA receiver functionality. Default Value: 0
5	PARITY_ENABLED	Parity checking enabled ('1') or not ('0'). Only applicable in standard UART submode. In SmartCard submode, parity checking is always enabled through hardware. In IrDA submode, parity checking is always disabled through hardware. Default Value: 0
4	PARITY	Parity bit. When '0', the receiver expects an even parity. When '1', the receiver expects an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0

23.1.6 SCB0_UART_RX_CTRL (continued)

2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of half bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. Note that in case of a stop bits error, the successive data frames may get lost as the receiver needs to resynchronize its start bit detection. The amount of lost data frames depends on both the amount of stop bits, the idle time between data frames and the data frame value. Default Value: 2

23.1.7 SCB0_UART_RX_STATUS

UART receiver status

Address: 0x4060004C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	BR_COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				BR_COUNTER [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 0	BR_COUNTER	For LIN: Amount of clk_scb periods that constitute the transmission of a 0x55 data frame (sent least signficant bit first) as determined by the receiver. BR_COUNTER / 8 is the amount of clk_scb periods that constitute a bit period. This field has valid data when INTR_RX.BAUD_DETECT is set to '1'. Default Value: Undefined

23.1.8 SCB0_UART_FLOW_CTRL

UART flow control

Address: 0x40600050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	TRIGGER_LEVEL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							RTS_POLARITY

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						CTS_ENABLED	CTS_POLARITY

Bits	Name	Description
25	CTS_ENABLED	Enable use of CTS input signal by the UART transmitter: '0': Disabled. The UART transmitter ignores the CTS input signal and transmits when a data frame is available for transmission in the TX FIFO or the TX shift register. '1': Enabled. The UART transmitter uses CTS input signal to qualify the transmission of data. It transmits when CTS input signal is active and a data frame is available for transmission in the TX FIFO or the TX shift register. If UART_CTRL.LOOPBACK is '1', the CTS input signal is driven by the RTS output signal locally in SCB (both signals are subjected to signal polarity changes as indicated by RTS_POLARITY and CTS_POLARITY). Default Value: 0
24	CTS_POLARITY	Polarity of the CTS input signal '0': CTS is active low ; '1': CTS is active high; Default Value: 0

23.1.8 SCB0_UART_FLOW_CTRL (continued)

16	RTS_POLARITY	Polarity of the RTS output signal: '0': RTS is active low; '1': RTS is active high; During SCB reset (Hibernate system power mode), RTS output signal is '1'. This represents an inactive state assuming an active low polarity. Default Value: 0
6 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has less entries than the amount of this field, a Ready To Send (RTS) output signal is activated. By setting this field to "0", flow control is disabled Default Value: 0

23.1.9 SCB0_I2C_CTRL (continued)

23.1.9 SCB0_I2C_CTRL

I2C control

Address: 0x40600060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LOW_PHASE_OVS [7:4]				HIGH_PHASE_OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	None	RW	RW
HW Access	R	R	R	R	R	None	R	R
Name	S_NOT_READY_-DATA_NACK	S_NOT_READY_AD-DR_NACK	S_READY_DATA_ACK	S_READY_ADDR_ACK	S_GENER-AL_IGNORE	None	M_NOT_READY_-DATA_NACK	M_READY_DATA_ACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	MASTER_-MODE	SLAVE_-MODE	None [29:24]					

Bits	Name	Description
31	MASTER_MODE	Master mode enabled ('1') or not ('0'). Note that both master and slave modes can be enabled at the same time. This allows the SCB to address itself. Default Value: 0
30	SLAVE_MODE	Slave mode enabled ('1') or not ('0'). Default Value: 0
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only applicable in master/slave mode. When '0', no loopback When '1', loopback is enabled internally in the peripheral, and as a result unaffected by other I2C devices. This allows a SCB I2C peripheral to address itself. Default Value: 0

23.1.9 SCB0_I2C_CTRL (continued)

15	S_NOT_READY_-DATA_NACK	Only used for FIFO mode, NOT EZ or CMD_RESP mode. Functionality is as follows: - 1: a received data element byte the slave is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). Default Value: 1
14	S_NOT_READY_AD-DR_NACK	Only used for FIFO mode, NOT EZ or CMD_RESP mode. Functionality is as follows: - 1: In Active/Sleep mode a received (matching) slave address is immediately NACK'd when the RX FIFO is full In DeepSleep power mode when EC_AM = '1' and EC_OP = '0' clk_scb is not avaliable, so the incoming address will be NACK'd until the clock is avaliable. Once clk_scb is avaliable the address ACK will follow S_READY_ADDR_ACK - 0: in Active/Sleep mode clock stretching is performed when the RX FIFO is full, the strech is released when the RX FIFO is no longer full. In DeepSleep power mode when EC_AM = '1' and EC_OP = '0' clk_scb is not avaliable, so the clocked will be streched on an incoming address until clk_scb is avaliable. After clk_scb is avalaible the address ACK will follow S_READY_ADDR_ACK Default Value: 1
13	S_READY_DATA_ACK	When '1', a received data element by the slave is immediately ACK'd when the RX FIFO is not full. In EZ and CMD_RESP mode, this field should be set to '1'. When '0' the data must be ACK/NACK'd by the CPU using I2C_S_CMD.S_ACK or I2C_S_C-MD.S_NACK Default Value: 1
12	S_READY_ADDR_ACK	When '1', a received (matching) slave address is immediately ACK'd when the RX FIFO is not full. In EZ and CMD_RESP mode, this field should be set to '1'. When '0' the address must be ACK/NACK'd by the CPU using I2C_S_CMD.S_ACK or I2C_S_C-MD.S_NACK Default Value: 1
11	S_GENERAL_IGNORE	When '1', a received general call slave address is immediately NACK'd (no ACK or clock stretching) and treated as a non matching slave address. This is useful for slaves that do not need any data supplied within the general call structure. When '0' the general call address is accepted and follows S_READY_ADDR_ACK and S_NOT_READY_ADDR_NACK Default Value: 1
9	M_NOT_READY_-DATA_NACK	When '1', a received data element by the master is immediately NACK'd when the RX FIFO is full. When '0', clock stretching is used instead (till the RX FIFO is no longer full). Default Value: 1
8	M_READY_DATA_ACK	When '1', a received data element by the master is immediately ACK'd when the RX FIFO is not full. When '0' the CPU is responsible for ACK/NACKing the received data frame using I2C_M_C-MD.M_ACK or I2C_M_CMD.M_NACK Default Value: 1
7 : 4	LOW_PHASE_OVS	Serial I2C interface low phase oversampling factor. (LOW_PHASE_OVS + 1) * clk_scb constitutes the low phase of a bit period. The valid range is [7, 15] with input signal median filtering and [6, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. See architecture TRM for information on slave data rate requirments. Default Value: 8
3 : 0	HIGH_PHASE_OVS	Serial I2C interface high phase oversampling factor. (HIGH_PHASE_OVS + 1) * clk_scb constitutes the high phase of a bit period. The valid range is [5, 15] with input signal median filtering and [4, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. See architecture TRM for information on slave data rate requirments. Default Value: 8

23.1.10 SCB0_I2C_STATUS

I2C status

Address: 0x40600064

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	None			R
HW Access	None		W	W	None			W
Name	None [7:6]		M_READ	S_READ	None [3:1]			BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	M_READ	I2C master read transfer ('1') or I2C master write transfer ('0'). When the I2C master is inactive/idle or transmitting START, REPEATED START, STOP or an address, this field is '0". Default Value: 0
4	S_READ	I2C slave read transfer ('1') or I2C slave write transfer ('0'). When the I2C slave is inactive/idle or receiving START, REPEATED START, STOP or an address, this field is '0". Default Value: 0
0	BUS_BUSY	I2C bus is busy. The bus is considered busy ('1'), from the time a START is detected or from the time the SCL line is '0'. The bus is considered idle ('0'), from the time a STOP is detected. If the SCB is disabled, BUS_BUSY is '0'. After enabling the SCB, it takes time for the BUS_BUSY to detect a busy bus. This time is the maximum high time of the SCL line. For a 100 kHz interface frequency, this maximum high time may last roughly 5 us (half a bit period). For single master systems, BUS_BUSY does not have to be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START (no bus collisions). For multi-master systems, BUS_BUSY can be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START_ON_IDLE (to prevent bus collisions). Default Value: 0

23.1.11 SCB0_I2C_M_CMD

I2C master command

Address: 0x40600068

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [7:5]			M_STOP	M_NACK	M_ACK	M_START_ ON_IDLE	M_START

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	M_STOP	When '1', attempt to transmit a STOP. When this action is performed, the hardware sets this field to '0'. I2C_M_CMD.M_START has a higher priority than this command: in situations where both a STOP and a REPEATED START could be transmitted, M_START takes precedence over M_STOP. Default Value: 0
3	M_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0
2	M_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0

23.1.11 SCB0_I2C_M_CMD (continued)

1	M_START_ON_IDLE	When '1', transmit a START as soon as the bus is idle (I2C_STATUS.BUS_BUSY is '0', note that BUSY has a default value of '0'). For bus idle detection the hardware relies on STOP detection. As a result, bus idle detection is only functional after at least one I2C bus transfer has been detected on the bus (default/reset value of BUSY is '0') . A START is only transmitted when the master state machine is in the default state. When this action is performed, the hardware sets this field to '0'. Default Value: 0
0	M_START	When '1', transmit a START or REPEATED START. Whether a START or REPEATED START is transmitted depends on the state of the master state machine. A START is only transmitted when the master state machine is in the default state. A REPEATED START is transmitted when the master state machine is not in the default state, but is working on an ongoing transaction. The REPEATED START can only be transmitted after a NACK or ACK has been received for a transmitted data element or after a NACK has been transmitted for a received data element. When this action is performed, the hardware sets this field to '0'. Default Value: 0

23.1.12 SCB0_I2C_S_CMD

I2C slave command

Address: 0x4060006C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW1C	RW1C
Name	None [7:2]						S_NACK	S_ACK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	S_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. In EZ and CMD_RESP mode, this field should be set to '0' (it is only to be used in FIFO mode). This command has a higher priority than I2C_S_CMD.S_ACK, I2C_CTRL.S_READY_ADDR_ACK or I2C_CTRL.S_READY_DATA_ACK. Default Value: 0
0	S_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. In EZ and CMD_RESP mode, this field should be set to '0' (it is only to be used in FIFO mode). Default Value: 0

23.1.13 SCB0_I2C_CFG

I2C configuration

Address: 0x40600070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [7:5]			SDA_IN_-FILT_SEL	None [3:2]		SDA_IN_FILT_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [15:13]			SCL_IN_-FILT_SEL	None [11:10]		SCL_IN_FILT_TRIM [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [23:22]		SDA_OUT_FILT2_TRIM [21:20]		SDA_OUT_FILT1_TRIM [19:18]		SDA_OUT_FILT0_TRIM [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW		None			
HW Access	None		R		None			
Name	None [31:30]		SDA_OUT_FILT_SEL [29:28]		None [27:24]			

Bits	Name	Description
29 : 28	SDA_OUT_FILT_SEL	Selection of cumulative "i2c_sda_out" filter delay: "0": 0 ns. "1": 50 ns (filter 0 enabled). "2": 100 ns (filters 0 and 1 enabled). "3": 150 ns (filters 0, 1 and 2 enabled). Default Value: 0
21 : 20	SDA_OUT_FILT2_TRIM	Trim bits for "i2c_sda_out" 50 ns filter 2. Not to be modified by the user Default Value: 2
19 : 18	SDA_OUT_FILT1_TRIM	Trim bits for "i2c_sda_out" 50 ns filter 1. Not to be modified by the user Default Value: 2
17 : 16	SDA_OUT_FILT0_TRIM	Trim bits for "i2c_sda_out" 50 ns filter 0. Not to be modified by the user Default Value: 2

23.1.13 SCB0_I2C_CFG (continued)

12	SCL_IN_FILT_SEL	Selection of "i2c_scl_in" filter delay: '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
9 : 8	SCL_IN_FILT_TRIM	Trim bits for "i2c_scl_in" 50 ns filter. Not to be modified by the user Default Value: 0
4	SDA_IN_FILT_SEL	Selection of "i2c_sda_in" filter delay: '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
1 : 0	SDA_IN_FILT_TRIM	Trim bits for "i2c_sda_in" 50 ns filter. SDA_IN_FILT_TRIM[1] is used to enable I2CS_EC or SPIS_EC access to internal EZ memory. 1: enable clk_scb 0: disable clk_scb Before going to deepsleep this field should be set to 0. It should be re-enabled once the device is awoken and clk_hf[0] is at the desired frequency. Default Value: 3

23.1.14 SCB0_TX_CTRL (continued)

23.1.14 SCB0_TX_CTRL

Transmitter control

Address: 0x40600200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							MSB_-FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							OPEN_DRAIN

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	OPEN_DRAIN	Each IO cell "xxx" has two associated SCB output signals "xxx_out_en" and "xxx_out". This field determines how the SCB controls those two signals. Consult the GPIO chapter in the architecture TRM to understand how the pin drive modes behave when connected to SCBs. '0': Normal operation mode. In this operation mode "xxx_out_en" output enable signal is typically constant '1' the "xxx_out" output is the outputted value. In other words, in normal operation mode, the "xxx_out" output is used to control the IO cell output value: "xxx_out" is '0' to drive an IO cell output value of '0' and "xxx_out" is '1' to drive an IO cell output value of '1'. '1': Open drain operation mode. In this operation mode "xxx_out_en" output controls the outputted value. Typically the "xxx_out" signal is a constant "0". Thus when "xxx_out_en" is "1" the line is driven low, but when "xxx_out_en" is "0" the output is not driven. This requires that the line is driven high by an external device or pull-up resistor The open drain mode is supported for: - I2C mode this field must be set. - UART mode use this mode when a pull-up resistor is used on the TX line. - SPI mode this field must be set if there are multiple slaves driving MISO. Default Value: 0

23.1.14 SCB0_TX_CTRL (continued)

8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. For EZ and CMD_RESP this field must be set to "1" Default Value: 1
3 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the amount of bits in a transmitted data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. In EZ and CMD_RESP mode (for both SPI and I2C), the only valid value is 7. Default Value: 7

23.1.15 SCB0_TX_FIFO_CTRL

Transmitter FIFO control

Address: 0x40600204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	TRIGGER_LEVEL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware reads from the transmitter FIFO do not remove FIFO entries. Freeze will not advance the TX FIFO read pointer. Default Value: 0
16	CLEAR	When '1', the transmitter FIFO and transmitter shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
6 : 0	TRIGGER_LEVEL	Trigger level. When the transmitter FIFO has less entries than the number of this field, a transmitter trigger event INTR_TX.TRIGGER is generated. Default Value: 0

23.1.16 SCB0_TX_FIFO_STATUS

Transmitter FIFO status

Address: 0x40600208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	USED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None	R						
HW Access	None	W						
Name	None	RD_PTR [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None	R						
HW Access	None	W						
Name	None	WR_PTR [30:24]						

Bits	Name	Description
30 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written. Default Value: 0
22 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read by the hardware. Default Value: 0
15	SR_VALID	Indicates whether the TX shift registers holds a valid data frame ('1') or not ('0'). The shift register can be considered the top of the TX FIFO (the data frame is not included in the USED field of the TX FIFO). The shift register is a working register and holds the data frame that is currently transmitted (when the protocol state machine is transmitting a data frame) or the data frame that is transmitted next (when the protocol state machine is not transmitting a data frame). Default Value: 0
7 : 0	USED	Amount of entries in the transmitter FIFO. The value of this field ranges from 0 to FF_DATA_NR (EZ_DATA_NR/2). Default Value: 0

23.1.17 SCB0_TX_FIFO_WR

Transmitter FIFO write

Address: 0x40600240

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data frame written into the transmitter FIFO. Behavior is similar to that of a PUSH operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used. A write to a full TX FIFO sets INTR_TX.OVERFLOW to '1'. Default Value: 0

23.1.18 SCB0_RX_CTRL

Receiver control

Address: 0x40600300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						MEDIAN	MSB_-FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	MEDIAN	Median filter. When '1', a digital 3 taps median filter is performed on input interface lines. This filter should reduce the susceptibility to errors. However, its requires higher oversampling values. For UART IrDA submode, this field should always be '1'. Default Value: 0
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. For EZ and CMD_RESP this field must be set to "1" Default Value: 1
3 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the expected amount of bits in received data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. In EZ mode (for both SPI and I2C), the only valid value is 7. Default Value: 7

23.1.19 SCB0_RX_FIFO_CTRL

Receiver FIFO control

Address: 0x40600304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	TRIGGER_LEVEL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware writes to the receiver FIFO have no effect. Freeze will not advance the RX FIFO write pointer. Default Value: 0
16	CLEAR	When '1', the receiver FIFO and receiver shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
6 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has more entries than the number of this field, a receiver trigger event INTR_RX.TRIGGER is generated. Default Value: 0

23.1.20 SCB0_RX_FIFO_STATUS

Receiver FIFO status

Address: 0x40600308

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	USED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None	R						
HW Access	None	W						
Name	None	RD_PTR [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None	R						
HW Access	None	W						
Name	None	WR_PTR [30:24]						

Bits	Name	Description
30 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written by the hardware. Default Value: 0
22 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read. Default Value: 0
15	SR_VALID	Indicates whether the RX shift registers holds a (partial) valid data frame ('1') or not ('0'). The shift register can be considered the bottom of the RX FIFO (the data frame is not included in the USED field of the RX FIFO). The shift register is a working register and holds the data frame that is currently being received (when the protocol state machine is receiving a data frame). Default Value: 0
7 : 0	USED	Amount of entries in the receiver FIFO. The value of this field ranges from 0 to FF_DATA_NR (EZ_DATA_NR/2). Default Value: 0

23.1.21 SCB0_RX_MATCH

Slave address and mask

Address: 0x40600310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	MASK	Slave device address mask. This field is a mask that specifies which of the ADDR field bits in the ADDR field take part in the matching of the slave address: MATCH = ((ADDR & MASK) == ("slave address" & MASK)). Default Value: 0
7 : 0	ADDR	Slave device address. In UART multi-processor mode, all 8 bits are used. In I2C slave mode, only bits 7 down to 1 are used. This reflects the organization of the first transmitted byte in a I2C transfer: the first 7 bits represent the address of the addressed slave, and the last 1 bit is a read/write indicator ('0': write, '1': read). Default Value: 0

23.1.22 SCB0_RX_FIFO_RD

Receiver FIFO read

Address: 0x40600340

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will remove the data frame from the FIFO; i.e. behavior is similar to that of a POP operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used. When in debug mode a read from this register behaves as a read from the SCB_RX_FIFO_RD_-SILENT register. That is data will not be removed from the FIFO A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. Default Value: Undefined

23.1.23 SCB0_RX_FIFO_RD_SILENT

Receiver FIFO read silent

Address: 0x40600344

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will NOT remove the data frame from the FIFO; i.e. behavior is similar to that of a PEEK operation. Note that when CTRL.BYTE_-MODE is '1', only DATA[7:0] are used. A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. Default Value: Undefined

23.1.24 SCB0_EZ_DATA0

Memory buffer

Address: 0x40600400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value, or checking the field BLOCKED of the INTR_TX and INTR_RX registers Default Value: Undefined

23.1.25 SCB0_INTR_CAUSE

Active clocked interrupt signal

Address: 0x40600E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				RX	TX	S	M

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	RX	Receiver interrupt active ("interrupt_rx"): INTR_RX_MASKED != 0. Default Value: 0
2	TX	Transmitter interrupt active ("interrupt_tx"): INTR_TX_MASKED != 0. Default Value: 0
1	S	Slave interrupt active ("interrupt_slave"): INTR_S_MASKED != 0. Default Value: 0
0	M	Master interrupt active ("interrupt_master"): INTR_M_MASKED != 0. Default Value: 0

23.1.26 SCB0_INTR_M

Master interrupt request

Address: 0x40600F00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	None	RW1C	RW1C	RW1C
HW Access	None			RW1S	None	RW1S	RW1S	RW1S
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	SPI master transfer done event: all data frames in the transmit FIFO are sent, the transmit FIFO is empty (both TX FIFO and transmit shifter register are empty), and SPI select output pin is de-selected. Default Value: 0
8	I2C_BUS_ERROR	I2C master bus error (unexpected detection of START or STOP condition). Default Value: 0
4	I2C_STOP	I2C master STOP. Set to '1', when the master has transmitted a STOP. Default Value: 0
2	I2C_ACK	I2C master acknowledgement. Set to '1', when the master receives a ACK (typically after the master transmitted the slave address or TX data). Default Value: 0
1	I2C_NACK	I2C master negative acknowledgement. Set to '1', when the master receives a NACK (typically after the master transmitted the slave address or TX data). Default Value: 0

23.1.26 SCB0_INTR_M (continued)

0	I2C_ARB_LOST	I2C master lost arbitration: the value driven by the master on the SDA line is not the same as the value observed on the SDA line. Default Value: 0

23.1.27 SCB0_INTR_M_SET (continued)

23.1.27 SCB0_INTR_M_SET

Master interrupt set request

Address: 0x40600F04

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	None	RW1S	RW1S	RW1S
HW Access	None			A	None	A	A	A
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

23.1.28 SCB0_INTR_M_MASK

Master interrupt mask

Address: 0x40600F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	RW
HW Access	None			R	None	R	R	R
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

23.1.29 SCB0_INTR_M_MASKED

Master interrupt masked request

Address: 0x40600F0C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	None	R	R	R
HW Access	None			W	None	W	W	W
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	R
HW Access	None						W	W
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

23.1.30 SCB0_INTR_S

Slave interrupt request

Address: 0x40600F40

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	SPI slave deselected at an unexpected time in the SPI transfer. Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0
10	SPI_EZ_STOP	SPI slave deselected after any EZ SPI transfer occurred. Default Value: 0
9	SPI_EZ_WRITE_STOP	SPI slave deselected after a write EZ SPI transfer occurred. Default Value: 0
8	I2C_BUS_ERROR	I2C slave bus error (unexpected detection of START or STOP condition). This should not occur, it represents erroneous I2C bus behavior. In case of a bus error, the I2C slave state machine abort the ongoing transfer. Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

23.1.30 SCB0_INTR_S (continued)

7	I2C_GENERAL	I2C slave general call address received. If CTRL.ADDR_ACCEPT is set the received address 0x00 (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
6	I2C_ADDR_MATCH	I2C slave matching address received. If CTRL.ADDR_ACCEPT, the received address (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
5	I2C_START	I2C slave START received. Set to '1', when START or REPEATED START event is detected. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') AND clock stretching is performed (till the internally clocked logic takes over) (I2C_CTRL.S_NOT_READY_ADDR_NACK is '0'), this field is NOT set. Firmware should use INTR_S_EC.WAKE_UP, INTR_S.I2C_ADDR_MATCH and INTR_S.I2C_GENERAL. Default Value: 0
4	I2C_STOP	I2C STOP event for I2C (read or write) transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. The event is detected on any I2C transfer intended for this slave. Note that a I2C address intended for the slave (address is matching) will result in a I2C_STOP event independent of whether the I2C address is ACK'd or NACK'd. Default Value: 0
3	I2C_WRITE_STOP	I2C STOP event for I2C write transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. Note that a I2C write address intended for the slave (address is matching and a it is a write transfer) will result in a I2C_WRITE_STOP event independent of whether the I2C address is ACK'd or NACK'd. In EZ mode, the event is detected only on I2C write transfers that have EZ data written to the memory structure (an I2C write transfer that only communicates an I2C address and EZ base address, will not result in this event being detected). Default Value: 0
2	I2C_ACK	I2C slave acknowledgement received. Set to '1', when the slave receives a ACK (typically after the slave transmitted TX data). Default Value: 0
1	I2C_NACK	I2C slave negative acknowledgement received. Set to '1', when the slave receives a NACK (typically after the slave transmitted TX data). Default Value: 0
0	I2C_ARB_LOST	I2C slave lost arbitration: the value driven on the SDA line is not the same as the value observed on the SDA line (while the SCL line is '1'). This should not occur, it represents erroneous I2C bus behavior. In case of lost arbitration, the I2C slave state machine aborts the ongoing transfer. SW may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

23.1.31 SCB0_INTR_S_SET (continued)

23.1.31 SCB0_INTR_S_SET

Slave interrupt set request

Address: 0x40600F44

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

23.1.31 SCB0_INTR_S_SET (continued)

5	I2C_START	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

23.1.32 SCB0_INTR_S_MASK (continued)

23.1.32 SCB0_INTR_S_MASK

Slave interrupt mask

Address: 0x40600F48

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0

23.1.32 SCB0_INTR_S_MASK (continued)

5	I2C_START	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

23.1.33 SCB0_INTR_S_MASKED (continued)

23.1.33 SCB0_INTR_S_MASKED

Slave interrupt masked request

Address: 0x40600F4C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
10	SPI_EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
9	SPI_EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	I2C_GENERAL	Logical and of corresponding request and mask bits. Default Value: 0
6	I2C_ADDR_MATCH	Logical and of corresponding request and mask bits. Default Value: 0

23.1.33 SCB0_INTR_S_MASKED (continued)

5	I2C_START	Logical and of corresponding request and mask bits. Default Value: 0
4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
3	I2C_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

23.1.34 SCB0_INTR_TX (continued)

23.1.34 SCB0_INTR_TX

Transmitter interrupt request

Address: 0x40600F80

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW1C	RW1C	RW1C	None		RW1C	RW1C
HW Access	None	RW1S	RW1S	RW1S	None		RW1S	RW1S
Name	None	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	UART lost arbitration: the value driven on the TX line is not the same as the value observed on the RX line. This condition event is usefull when transmitter and receiver share a TX/RX line. This is the case in LIN or SmartCard modes. Default Value: 0
9	UART_DONE	UART transmitter done event. This happens when the SCB is done transferring all data in the TX FIFO, and the last stop field is transmitted (both TX FIFO and transmit shifter register are empty). Default Value: 0
8	UART_NACK	UART transmitter received a negative acknowledgement in SmartCard mode. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

23.1.34 SCB0_INTR_TX (continued)

6	UNDERFLOW	Attempt to read from an empty TX FIFO. This happens when the SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full TX FIFO. Only used in FIFO mode. Default Value: 0
4	EMPTY	TX FIFO is empty; i.e. it has 0 entries. Only used in FIFO mode. Default Value: 0
1	NOT_FULL	TX FIFO is not full. Dependent on CTRL.BYTE_MODE: (FF_DATA_NR = EZ_DATA_NR/2) BYTE_MODE is '0': # entries != FF_DATA_NR/2. BYTE_MODE is '1': # entries != FF_DATA_NR. Only used in FIFO mode. Default Value: 0
0	TRIGGER	Less entries in the TX FIFO than the value specified by TX_FIFO_CTRL.TRIGGER_LEVEL. Only used in FIFO mode. Default Value: 0

23.1.35 SCB0_INTR_TX_SET (continued)

23.1.35 SCB0_INTR_TX_SET

Transmitter interrupt set request

Address: 0x40600F84

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW1S	RW1S	RW1S	None		RW1S	RW1S
HW Access	None	A	A	A	None		A	A
Name	None	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

1	NOT_FULL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

23.1.36 SCB0_INTR_TX_MASK (continued)

23.1.36 SCB0_INTR_TX_MASK

Transmitter interrupt mask

Address: 0x40600F88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None		RW	RW
HW Access	None	R	R	R	None		R	R
Name	None	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0

1	NOT_FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

23.1.37 SCB0_INTR_TX_MASKED (continued)

23.1.37 SCB0_INTR_TX_MASKED

Transmitter interrupt masked request

Address: 0x40600F8C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R	R	R	None		R	R
HW Access	None	W	W	W	None		W	W
Name	None	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0
9	UART_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	UART_NACK	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
4	EMPTY	Logical and of corresponding request and mask bits. Default Value: 0

1	NOT_FULL	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

23.1.38 SCB0_INTR_RX (continued)

23.1.38 SCB0_INTR_RX

Receiver interrupt request

Address: 0x40600FC0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW1C	RW1C	None	RW1C	RW1C	None	RW1C
HW Access	None	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
Name	None	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Break detection is successful: the line is '0' for UART_RX_CTRL.BREAK_WIDTH + 1 bit period. Can occur at any time to address unanticipated break fields; i.e. "break-in-data" is supported. This feature is supported for the UART standard and LIN submodes. For the UART standard submodes, ongoing receipt of data frames is NOT affected; i.e. Firmware is expected to take the proper action. For the LIN submode, possible ongoing receipt of a data frame is stopped and the (partially) received data frame is dropped and baud rate detection is started. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
10	BAUD_DETECT	LIN baudrate detection is completed. The receiver software uses the UART_RX_STA-TUS.BR_COUNTER value to set the clk_scb to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Default Value: 0

9	PARITY_ERROR	UART Parity error in received data frame. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '1', the received frame is dropped. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '0', the received frame is send to the RX FIFO. In SmartCard submode, negatively acknowledged data frames generate a parity error. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO. Default Value: 0
8	FRAME_ERROR	UART Frame error in received data frame. This can be either a start or stop bit(s) error: Start bit error: after the detection of the beginning of a start bit period (RX line changes from '1' to '0'), the middle of the start bit period is sampled erroneously (RX line is '1'). Note: a start bit error is detected BEFORE a data frame is received. Stop bit error: the RX line is sampled as '0', but a '1' was expected. Note: a stop bit error may result in failure to receive successive data frame(s). Note: a stop bit error is detected AFTER a data frame is received. A stop bit error is detected after a data frame is received, and the UART_RX_CTL.DROP_ON_-FRAME_ERROR field specifies whether the received frame is dropped or send to the RX FIFO. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '1', the received data frame is dropped. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '0', the received data frame is send to the RX FIFO. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO; i.e. the RX FIFO does not have error flags to tag erroneous data frames. Default Value: 0
6	UNDERFLOW	Attempt to read from an empty RX FIFO. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full RX FIFO. Note: in I2C mode, the OVERFLOW is set when a data frame is received and the RX FIFO is full, independent of whether it is ACK'd or NACK'd. Only used in FIFO mode. Default Value: 0
3	FULL	RX FIFO is full. Note that received data frames are lost when the RX FIFO is full. Dependent on CTRL.BYTE_MODE: (FF_DATA_NR = EZ_DATA_NR/2) BYTE_MODE is '0': # entries == FF_DATA_NR/2. BYTE_MODE is '1': # entries == FF_DATA_NR. Only used in FIFO mode. Default Value: 0
2	NOT_EMPTY	RX FIFO is not empty. Only used in FIFO mode. Default Value: 0
0	TRIGGER	More entries in the RX FIFO than the value specified by RX_FIFO_CTRL.TRIGGER_LEVEL. Only used in FIFO mode. Default Value: 0

23.1.39 SCB0_INTR_RX_SET (continued)

23.1.39 SCB0_INTR_RX_SET

Receiver interrupt set request

Address: 0x40600FC4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
HW Access	None	A	A	None	A	A	None	A
Name	None	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
10	BAUD_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
9	PARITY_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
8	FRAME_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0

3	FULL	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
2	NOT_EMPTY	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

23.1.40 SCB0_INTR_RX_MASK (continued)

23.1.40 SCB0_INTR_RX_MASK

Receiver interrupt mask

Address: 0x40600FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	None	RW	RW	None	RW
HW Access	None	R	R	None	R	R	None	R
Name	None	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	BAUD_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	PARITY_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	FRAME_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0

3	FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	NOT_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

23.1.41 SCB0_INTR_RX_MASKED (continued)

23.1.41 SCB0_INTR_RX_MASKED

Receiver interrupt masked request

Address: 0x40600FCC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R	R	None	R	R	None	R
HW Access	None	W	W	None	W	W	None	W
Name	None	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
10	BAUD_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
9	PARITY_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
8	FRAME_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0

3	FULL	Logical and of corresponding request and mask bits. Default Value: 0
2	NOT_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

23.1.42 SCB6_CTRL (continued)

23.1.42 SCB6_CTRL

Generic control

Address: 0x40660000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [15:13]			CMD_RE-SP_MODE	BYTE_-MODE	EZ_MODE	EC_OP_-MODE	EC_AM_-MODE

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						BLOCK	ADDR_AC-CEPT

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None					RW	
HW Access	R	None					R	
Name	ENABLED	None [30:26]					MODE [25:24]	

Bits	Name	Description
31	ENABLED	0': Block Disabled '1': Block Enabled The proper order in which to initialize the SCB is as follows: - Program protocol specific information using SPI_CTRL, UART_CTRL (and UART_TX_CTRL and UART_RX_CTRL) or I2C_CTRL. This includes selection of a submode, master/slave functionality and transmitter/receiver functionality when applicable. - Program generic transmitter (TX_CTRL) and receiver (RX_CTRL) information. This includes enabling of the transmitter and receiver functionality. - Program transmitter FIFO (TX_FIFO_CTRL) and receiver FIFO (RX_FIFO_CTRL) information. - Program CTRL to enable SCB, select the specific operation mode and oversampling factor. When the SCB is enabled, no control information should be changed. Changes must be made AFTER disabling the SCB, e.g. to modify the operation mode (from I2C to SPI) or to go from externally to internally clocked. The change takes effect after the SCB is re-enabled. Note that disabling the SCB will cause re-initialization of the design and associated state is lost (e.g. FIFO content). Default Value: 0

23.1.42 SCB6_CTRL (continued)

25 : 24	MODE	Mode of operation (3: Reserved) Default Value: 3 **0x0: I2C :** Inter-Integrated Circuits (I2C) mode. **0x1: SPI :** Serial Peripheral Interface (SPI) mode. **0x2: UART :** Universal Asynchronous Receiver/Transmitter (UART) mode.
17	BLOCK	Only used in externally clocked mode. If the externally clocked logic and the CPU access the EZ memory at the same time this bit determines whether a CPU access should block and result in bus wait states '0': Do not block, but ingore a write and return 0xffff:ffff for a read '1': Block, resulting in CPU wait states. If BLOCK is '0' and the accesses collide, CPU read operations return 0xffff:ffff and CPU write operations are ignored. Colliding accesses are registered as interrupt causes: field BLOCKED of the INTR_TX and INTR_RX registers. Default Value: 0
16	ADDR_ACCEPT	Determines whether a received matching address is accepted in the RX FIFO:. '0': Matching address does not go in RX FIFO '1': Match address does go in RX FIFO In I2C mode, this field is used to allow the slave to put the received slave address or general call address in the RX FIFO. Note that a received matching address is put in the RX FIFO when this bit is '1' for both I2C read and write transfers. In multi-processor UART receiver mode, this field is used to allow the receiver to put the received address in the RX FIFO. Note: non-matching addresses are never put in the RX FIFO. In SPI mode this field must be '0' Default Value: 0
12	CMD_RESP_MODE	Determines CMD_RESP mode of operation: '0': CMD_RESP mode disabled. '1': CMD_RESP mode enabled (also requires EC_AM_MODE and EC_OP_MODE to be set to '1'). In CMD_RESP mode, a meta protocol is applied to the serial interface protocol. This meta protocol adds meaning to the data frames transferred by the serial interface protocol: a data frame can represent a write memory data element or a read memory data element. The difference from EZ mode is that the address is written by the CPU, not the interface master. CMD_RESP mode can only be used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. The external master should use continuous data frames; i.e. data frames not seperated by slave deselection. In CMD_RESP mode, data frames should 8-bit in size and should be transmitted and received with the Most Significant Bit (MSB) first. In UART mode this field must be '0'. Default Value: 0

23.1.42 SCB6_CTRL (continued)

11	BYTE_MODE	Determines the number of bits per FIFO data element: '0': 16-bit FIFO data elements. '1': 8-bit FIFO data elements. This mode doubles the amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 7]. Default Value: 0
10	EZ_MODE	This field determines if EZ mode is enabled or disabled for the SCB block '0': EZ Mode Disabled '1': EZ Mode Enabled In EZ mode, a meta protocol is applied to the serial interface protocol. This meta protocol adds meaning to the data frames transferred by the serial interface protocol: a data frame can represent a memory address, a write memory data element or a read memory data element. EZ mode can only be used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. The external master should use continuous data frames; i.e. data frames not seperated by slave deselection. In EZ mode, data frames should 8-bit in size and should be transmitted and received with the Most Significant Bit (MSB) first. In UART mode this field must be '0'. Default Value: 0
9	EC_OP_MODE	This field specifies the clocking for the SCB block after the address phase '0': Internally clocked mode '1': externally clocked mode In internally clocked mode, the serial interface protocols run off the clk_scb. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked operation mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. In UART mode this field must be '0'. Default Value: 0
8	EC_AM_MODE	This field specifies the clocking for the address matching (I2C slave) or slave selection detection logic (SPI slave) '0': Internally clocked mode '1': Externally clocked mode In internally clocked mode the address detection(and slave selection detection) is done by clk_scb, and thus won't be done in deep sleep power mode as clk_scb isn't active. In externally clocked mode the address detection is done by the I2C/SPI interface clock. This allows for the device to be awoken on I2C salve address match and SPI slave select assertion. The clocking for the rest of the logic is determined by CTRL.EC_OP_MODE. Externally clocked mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. In UART mode this field must be '0'. Default Value: 0

3 : 0	OVS	Serial interface bit period oversampling factor expressed in clk_scb cycles. clk_scb is the peripheral clock divider connected to the SCB. Used for SPI Master and UART functionality. This field is NOT used in externally clocked mode. This filed is NOT used for SPI slave or I2C mode. OVS + 1 clk_scb cycles constitute a single serial interface clock/bit cycle. If OVS is odd, the oversampling factor is even and the low and high phase of the interface clock period are the same. If OVS is even, the oversampling factor is odd and the low and high phase can differ by 1 SCB clock period. In SPI master mode, the valid range is [3, 15]. The frequency of the SPI Clock is (frequency of clk_scb) / (OVS + 1). For example, is clk_scb is 50 MHz and OVS is 9, then the frequency of SPI Clock is 50 MHz / (9+1) = 5 MHz. If the MISO signal is not used for SPI master the valid range changes to [1,15] In SPI slave mode, the OVS field is NOT used. Refer to the architecture TRM for information on how to configure clk_scb for SPI Slave. Generally, it is recommended that clk_scb be as fast as possible for the slave. In UART standard sub mode (including LIN and Smartcard), the valid range is [7, 15]. In UART IrDA sub mode this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. For normal transmission mode, the pulse is roughly 3/16 of the bit period (for all bit rates). There is only one valid OVS value: - 0: 16 times oversampling. clk_scb frequency = 16*115.2 KHz for 115.2 Kbps. clk_scb frequency = 16*57.6 KHz for 57.6 Kbps. clk_scb frequency = 16*38.4 KHz for 38.4 Kbps. clk_scb frequency = 16*19.2 KHz for 19.2 Kbps. clk_scb frequency = 16*9.6 KHz for 9.6 Kbps. clk_scb frequency = 16*2.4 KHz for 2.4 Kbps. clk_scb frequency = 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. RX_CTRL.MEDIAN must be set to '1' for IrDA receiver functionality. UART IrDA RX Low power mode, OVS field values (with the required clk_scb frequency): - 0: 16 times oversampling. clk_scb frequency = 16*115.2 KHz for 115.2 Kbps. - 1: 32 times oversampling. clk_scb frequency = 32*57.6 KHz for 57.6 Kbps. - 2: 48 times oversampling. clk_scb frequency = 48*38.4 KHz for 38.4 Kbps. - 3: 96 times oversampling. clk_scb frequency = 96*19.2 KHz for 19.2 Kbps. - 4: 192 times oversampling. clk_scb frequency = 192*9.6 KHz for 9.6 Kbps. - 5: 768 times oversampling. clk_scb frequency = 768*2.4 KHz for 2.4 Kbps. - 6: 1536 times oversampling. clk_scb frequency = 1536*1.2 KHz for 1.2 Kbps. - all other values are not used in low power mode. In low power transmission mode, this pulse is potentially smaller (down to 1.62 us typical and 1.41 us minimal) than 3/16 of the bit period (for < 115.2 Kbps bitrates). Pulse widths greater or equal than two SCB clock cycles are guaranteed to be detected by the receiver. Pulse widths less than two SCB clock cycles and greater or equal than one SCB clock cycle may be detected by the receiver. Pulse widths less than one SCB clock cycle will not be detected by the receiver. Default Value: 15

23.1.43 SCB6_STATUS

Generic status

Address: 0x40660004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							EC_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory (this is only possible in EZ and CMD_RESP mode). This bit can be used by SW to determine whether it is safe for the CPU to access the EZ memory (without bus wait states (a blocked CPU access) or bus errors being generated). Note that the INTR_TX.BLOCKED and INTR_RX.BLOCKED interrupt causes are used to indicate whether CPU access was actually blocked by externally clocked logic. Default Value: Undefined

23.1.44 SCB6_CMD_RESP_CTRL

Command/response control

Address: 0x40660008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BASE_RD_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	BASE_WR_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_WR_ADDR	I2C/SPI write base address for CMD_RESP mode. At the start of a write transfer this BASE_WR_ADDR is copied to CMD_RESP_STATUS.CURR_WR_ADDR. This field should not be modified during ongoing bus transfers. Default Value: 0
7 : 0	BASE_RD_ADDR	I2C/SPI read base address for CMD_RESP mode. At the start of a read transfer this BASE_RD_ADDR is copied to CMD_RESP_STATUS.CURR_RD_ADDR. This field should not be modified during ongoing bus transfers. Default Value: 0

23.1.45 SCB6_CMD_RESP_STATUS (continued)

23.1.45 SCB6_CMD_RESP_STATUS

Command/response status

Address: 0x4066000C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CURR_RD_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	CURR_WR_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	W	W	None					
Name	CMD_RESP_EC_BUSY	CMD_RESP_EC_BUS_BUSY	None [29:24]					

Bits	Name	Description
31	CMD_RESP_EC_BUSY	Indicates whether the CURR_RD_ADDR and CURR_WR_ADDR fields in this register are reliable (when CMD_RESP_EC_BUSY is '0') or not reliable (when CMD_RESP_EC_BUSY is '1'). Note: - When there is no ongoing bus transfer, CMD_RESP_EC_BUSY is '0' (reliable). - When there is a ongoing bus transfer, CMD_RESP_EC_BUSY is '0' (reliable), when the CURR_RD_ADDR and CURR_WR_ADDR are not being updated by the HW. - When there is a ongoing bus transfer, CMD_RESP_EC_BUSY is '1' (not reliable), when the CURR_RD_ADDR or CURR_WR_ADDR are being updated by the HW. Note that this update lasts one I2C clock cycle, or two SPI clock cycles. Default Value: Undefined

30	CMD_RESP_EC_BUS_BUSY	Indicates whether there is an ongoing bus transfer to the SCB. '0': no ongoing bus transfer. '1': ongoing bus transfer. For SPI, the field is '1' when slave mode is selected. For I2C, the field is set to '1' at a I2C START/RESTART. In case of an address match, the field is set to '0' on a I2C STOP. In case of NO address match, the field is set to '0' after the failing address match. Default Value: Undefined
23 : 16	CURR_WR_ADDR	I2C/SPI write current address for CMD_RESP mode. HW increments the field after a write access to the memory buffer. However, when the last memory buffer address is reached, the address is NOT incremented (but remains at the maximim memory buffer address). The field is used to determine how many bytes have been written (# bytes = CURR_WR_ADDR - CMD_RESP_CTRL.BASE_WR_ADDR). This field is reliable when there is no bus transfer. This field is potentially unreliable when there is a ongoing bus transfer, i.e when CMD_RESP_EC_BUSY is '0', the field is reliable. Default Value: Undefined
7 : 0	CURR_RD_ADDR	I2C/SPI read current address for CMD_RESP mode. HW increments the field after a read access to the memory buffer. However, when the last memory buffer address is reached, the address is NOT incremented (but remains at the maximim memory buffer address). The field is used to determine how many bytes have been read (# bytes = CURR_RD_ADDR - CMD_RESP_CTRL.BASE_RD_ADDR). This field is reliable when there is no bus transfer. This field is potentially unreliable when there is a ongoing bus transfer, i.e. when CMD_RESP_EC_BUSY is '0', the field is reliable. Default Value: Undefined

23.1.46 SCB6_SPI_STATUS

SPI status

Address: 0x40660024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						SPI_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	SPI base EZ address. Address as provided by a SPI write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	SPI current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when SPI_EC_BUSY is '1'). Default Value: Undefined
1	SPI_EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ and CMD_RESP mode). This bit can be used by the CPU to determine whether BASE_ADDR and CURR_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	SPI bus is busy. The bus is considered busy ('1') during an ongoing transaction. For Motorola and National submodes, the busy bit is '1', when the slave selection is activated. For TI submode, the busy bit is '1' from the time the preceding/coinciding slave select is activated for the first transmitted data frame, till the last MOSI/MISO bit of the last data frame is transmitted. Default Value: Undefined

23.1.47 SCB6_I2C_STATUS (continued)

23.1.47 SCB6_I2C_STATUS

I2C status

Address: 0x40660064

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	None		R	R
HW Access	None		W	W	None		W	W
Name	None [7:6]		M_READ	S_READ	None [3:2]		I2C_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	I2C slave base EZ address. Address as provided by an I2C write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	I2C slave current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when I2C_EC_BUSY is '1'). Default Value: Undefined
5	M_READ	I2C master read transfer ('1') or I2C master write transfer ('0'). When the I2C master is inactive/idle or transmitting START, REPEATED START, STOP or an address, this field is '0". Default Value: 0
4	S_READ	I2C slave read transfer ('1') or I2C slave write transfer ('0'). When the I2C slave is inactive/idle or receiving START, REPEATED START, STOP or an address, this field is '0". Default Value: 0

1	I2C_EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_EZ_ADDR or CURR_EZ_ADDR (this is only possible in EZ and CMD_RESP mode). This bit can be used by the CPU to determine whether BASE_EZ_ADDR and CURR_EZ_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	I2C bus is busy. The bus is considered busy ('1'), from the time a START is detected or from the time the SCL line is '0'. The bus is considered idle ('0'), from the time a STOP is detected. If the SCB is disabled, BUS_BUSY is '0'. After enabling the SCB, it takes time for the BUS_BUSY to detect a busy bus. This time is the maximum high time of the SCL line. For a 100 kHz interface frequency, this maximum high time may last roughly 5 us (half a bit period). For single master systems, BUS_BUSY does not have to be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START (no bus collisions). For multi-master systems, BUS_BUSY can be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START_ON_IDLE (to prevent bus collisions). Default Value: 0

23.1.48 SCB6_INTR_CAUSE

Active clocked interrupt signal

Address: 0x40660E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		SPI_EC	I2C_EC	RX	TX	S	M

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	SPI_EC	Externally clocked SPI interrupt active ("interrupt_spi_ec"): INTR_SPI_EC_MASKED != 0. Default Value: 0
4	I2C_EC	Externally clock I2C interrupt active ("interrupt_i2c_ec"): INTR_I2C_EC_MASKED != 0. Default Value: 0
3	RX	Receiver interrupt active ("interrupt_rx"): INTR_RX_MASKED != 0. Default Value: 0
2	TX	Transmitter interrupt active ("interrupt_tx"): INTR_TX_MASKED != 0. Default Value: 0
1	S	Slave interrupt active ("interrupt_slave"): INTR_S_MASKED != 0. Default Value: 0
0	M	Master interrupt active ("interrupt_master"): INTR_M_MASKED != 0. Default Value: 0

23.1.49 SCB6_INTR_I2C_EC

Externally clocked I2C interrupt request

Address: 0x40660E80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (I2C STOP). This event is an indication that a buffer memory location has been read from. Only set for a slave request with an address match, in EZ and CMD_RESP modes, when EC_OP is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (I2C STOP). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only set for a slave request with an address match, in EZ and CMD_RESP modes, when EC_OP is '1'. Default Value: 0
1	EZ_STOP	STOP detection. Activated on the end of a every transfer (I2C STOP). Only set for a slave request with an address match, in EZ and CMD_RESP modes, when EC_OP is '1'. Default Value: 0
0	WAKE_UP	Wake up request. Active on incoming slave request (with address match). Only set when EC_AM is '1'. Default Value: 0

23.1.50 SCB6_INTR_I2C_EC_MASK

Externally clocked I2C interrupt mask

Address: 0x40660E88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

23.1.51 SCB6_INTR_I2C_EC_MASKED

Externally clocked I2C interrupt masked

Address: 0x40660E8C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

23.1.52 SCB6_INTR_SPI_EC

Externally clocked SPI interrupt request

Address: 0x40660EC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (SPI de-selection). This event is an indication that a buffer memory location has been read from. Only set in EZ and CMD_RESP modes and when EC_OP is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (SPI de-selection). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only set in EZ and CMD_RESP modes and when EC_OP is '1'. Default Value: 0
1	EZ_STOP	STOP detection. Activated on the end of a every transfer (SPI deselection). Only set in EZ and CMD_RESP mode and when EC_OP is '1'. Default Value: 0
0	WAKE_UP	Wake up request. Active on incoming slave request. Only set when EC_AM is '1'. Default Value: 0

23.1.53 SCB6_INTR_SPI_EC_MASK

Externally clocked SPI interrupt mask

Address: 0x40660EC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

23.1.54 SCB6_INTR_SPI_EC_MASKED

Externally clocked SPI interrupt masked

Address: 0x40660ECC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

23.1.55 SCB6_INTR_TX (continued)

23.1.55 SCB6_INTR_TX

Transmitter interrupt request

Address: 0x40660F80

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	None		RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	BLOCKED	CPU write can not get access to the EZ memory (EZ data access), due to an externally clocked EZ access. Default Value: 0
6	UNDERFLOW	Attempt to read from an empty TX FIFO. This happens when the SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full TX FIFO. Only used in FIFO mode. Default Value: 0
4	EMPTY	TX FIFO is empty; i.e. it has 0 entries. Only used in FIFO mode. Default Value: 0

1	NOT_FULL	TX FIFO is not full. Dependent on CTRL.BYTE_MODE: (FF_DATA_NR = EZ_DATA_NR/2) BYTE_MODE is '0': # entries != FF_DATA_NR/2. BYTE_MODE is '1': # entries != FF_DATA_NR. Only used in FIFO mode. Default Value: 0
0	TRIGGER	Less entries in the TX FIFO than the value specified by TX_FIFO_CTRL.TRIGGER_LEVEL. Only used in FIFO mode. Default Value: 0

23.1.56 SCB6_INTR_TX_SET

Transmitter interrupt set request

Address: 0x40660F84

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
HW Access	A	A	A	A	None		A	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	BLOCKED	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	NOT_FULL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

23.1.57 SCB6_INTR_TX_MASK

Transmitter interrupt mask

Address: 0x40660F88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None		RW	RW
HW Access	R	R	R	R	None		R	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	NOT_FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

23.1.58 SCB6_INTR_TX_MASKED

Transmitter interrupt masked request

Address: 0x40660F8C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	None		R	R
HW Access	W	W	W	W	None		W	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
4	EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
1	NOT_FULL	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

23.1.59 SCB6_INTR_RX (continued)

23.1.59 SCB6_INTR_RX

Receiver interrupt request

Address: 0x40660FC0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	None	RW1C	RW1C	None	RW1C
HW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	BLOCKED	CPU read transfer can not get access to the EZ memory (EZ_DATA accesses), due to an externally clocked EZ access. Default Value: 0
6	UNDERFLOW	Attempt to read from an empty RX FIFO. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full RX FIFO. Note: in I2C mode, the OVERFLOW is set when a data frame is received and the RX FIFO is full, independent of whether it is ACK'd or NACK'd. Only used in FIFO mode. Default Value: 0

3	FULL	RX FIFO is full. Note that received data frames are lost when the RX FIFO is full. Dependent on CTRL.BYTE_MODE: (FF_DATA_NR = EZ_DATA_NR/2) BYTE_MODE is '0': # entries == FF_DATA_NR/2. BYTE_MODE is '1': # entries == FF_DATA_NR. Only used in FIFO mode. Default Value: 0
2	NOT_EMPTY	RX FIFO is not empty. Only used in FIFO mode. Default Value: 0
0	TRIGGER	More entries in the RX FIFO than the value specified by RX_FIFO_CTRL.TRIGGER_LEVEL. Only used in FIFO mode. Default Value: 0

23.1.60 SCB6_INTR_RX_SET

Receiver interrupt set request

Address: 0x40660FC4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
HW Access	A	A	A	None	A	A	None	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	BLOCKED	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
3	FULL	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
2	NOT_EMPTY	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

23.1.61 SCB6_INTR_RX_MASK

Receiver interrupt mask

Address: 0x40660FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	None	RW	RW	None	RW
HW Access	R	R	R	None	R	R	None	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	NOT_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

23.1.62 SCB6_INTR_RX_MASKED (continued)

23.1.62 SCB6_INTR_RX_MASKED

Receiver interrupt masked request

Address: 0x40660FCC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	None	R	R	None	R
HW Access	W	W	W	None	W	W	None	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
3	FULL	Logical and of corresponding request and mask bits. Default Value: 0
2	NOT_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

Section I: Peripheral Group 9

This section encompasses the following chapters:

- Analog Reference Block Registers chapter on page 1862
- Continuous-Time Block Mini (CTBm) Registers chapter on page 1866
- Continuous-Time DAC Registers chapter on page 1896
- SAR ADC Registers chapter on page 1907
- FIFO Registers chapter on page 1966
- Timer Registers chapter on page 1979
- Low Power Oscillator Registers chapter on page 1983
- Programmable Analog Subsystem Registers chapter on page 1986

24 Analog Reference Block Registers

This section discusses the Analog Reference Block (AREF) registers. It lists all the registers in mapping tables, in address order.

24.1 Register Details

Register	Address	Description
PASS_AREFv2_AREF_CTRL	0x409F0E00	global AREF control

24.1.1 PASS_AREFv2_AREF_CTRL

global AREF control

Address: 0x409F0E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW		None	RW
HW Access	R	R			R		None	R
Name	CTB_IP-TAT_S-CALE	AREF_RMB [6:4]			AREF_BIAS_SCALE [3:2]		None	AREF_-MODE

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CTB_IPTAT_REDIRECT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		RW	None		RW
HW Access	None		R		R	None		R
Name	None [23:22]		VREF_SEL [21:20]		CLOCK_PU MP_PERI_-SEL	None [18:17]		IZTAT_SEL

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	R	R	R		None			
Name	ENABLED	DEEPS-LEEP_ON	DEEPSLEEP_MODE [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	- 0: AREF disabled - 1: AREF enabled Default Value: 0
30	DEEPSLEEP_ON	- 0: AREF disabled/off during System DeepSleep power mode - 1: AREF remains enabled during System DeepSleep power mode (if ENABLED=1) Default Value: 0
29 : 28	DEEPSLEEP_MODE	AREF System DeepSleep Operation Modes (only applies if DEEPSLEEP_ON = 1) Default Value: 0 **0x0: OFF :** All blocks "OFF" in System DeepSleep

24.1.1 PASS_AREFv2_AREF_CTRL (continued)

		0x1: IPTAT : IPTAT bias generator "ON" in System DeepSleep, but output is not available for use (used for fast AREF wakeup only) **0x2: IPTAT_IZTAT :** IPTAT bias generator and outputs "ON" in System DeepSleep (used for biasing the CTBm with a PTAT current only in System Deep Sleep) *Note that this mode also requires that the CTB_IPTAT_REDIRECT be set if the CTBm opamp is to operate in System DeepSleep **0x3: IPTAT_IZTAT_VREF :** IPTAT, VREF, and IZTAT generators "ON" in System DeepSleep. This mode provides identical AREF functionality in System DeepSleep as in the Active mode.
21 : 20	VREF_SEL	bandgap voltage select control Default Value: 0 **0x0: SRSS :** Use 0.8V Vref from SRSS **0x1: LOCAL :** Use locally generated Vref **0x2: EXTERNAL :** Use externally supplied Vref (aref_ext_vref)
19	CLOCK_PUMP_PERI_-SEL	CTBm charge pump clock source select. 0: Use the dedicated pump clock from SRSS (default) 1: Use one of the CLK_PERI dividers Default Value: 0
16	IZTAT_SEL	iztat current select control Default Value: 0 **0x0: SRSS :** Use 250nA IZTAT from SRSS **0x1: LOCAL :** Use locally generated 250nA

24.1.1 PASS_AREFv2_AREF_CTRL (continued)

15 : 8	CTB_IPTAT_REDIRECT	Re-direct the CTBm IPTAT output current. This can be used to reduce amplifier bias glitches during power mode transitions. 0: Opamp.IPTAT = AREF.IPTAT and Opamp.IZTAT= AREF.IZTAT 1: Opamp.IPTAT = HiZ and Opamp.IZTAT= AREF.IPTAT Note that in System Deep Sleep, the AREF IZTAT and/or IPTAT currents can be disabled and therefore the corresponding Opamp.IZTAT/IPTAT will be HiZ. Default Value: 0
7	CTB_IPTAT_SCALE	CTBm IPTAT current scaler. This bit must be set in order to operate the CTBm opamps in the lowest power mode. This bit is chip-wide (controls all CTBm opamps). 0: 1uA 1: 100nA Default Value: 0
6 : 4	AREF_RMB	Reserved - the 2 bits should be set to 0 Default Value: 0
3 : 2	AREF_BIAS_SCALE	Reserved. This bit field value should be set to 1. Default Value: 0
0	AREF_MODE	Control bit to trade off AREF settling and noise performance Default Value: 0 **0x0: NORMAL :** Normal startup (nominal noise) **0x1: FAST_START :** Fast startup (relatively higher noise)

25 Continuous-Time Block Mini (CTBm)

This section discusses the Continuous-Time Block Mini (CTBm) Registers. It lists all the registers in mapping tables, in address order

25.1 Register Details

Register	Address	Description
CTBM0_CTB_CTRL	0x40900000	global CTB and power control
CTBM0_OA_RES0_CTRL	0x40900004	Opamp0 and resistor0 control
CTBM0_OA_RES1_CTRL	0x40900008	Opamp1 and resistor1 control
CTBM0_COMP_STAT	0x4090000C	Comparator status
CTBM0_INTR	0x40900020	Interrupt request register
CTBM0_INTR_SET	0x40900024	Interrupt request set register
CTBM0_INTR_MASK	0x40900028	Interrupt request mask
CTBM0_INTR_MASKED	0x4090002C	Interrupt request masked
CTBM0_OA0_SW	0x40900080	Opamp0 switch control
CTBM0_OA0_SW_CLEAR	0x40900084	Opamp0 switch control clear
CTBM0_OA1_SW	0x40900088	Opamp1 switch control
CTBM0_OA1_SW_CLEAR	0x4090008C	Opamp1 switch control clear
CTBM0_CTD_SW	0x409000A0	CTDAC connection switch control
CTBM0_CTD_SW_CLEAR	0x409000A4	CTDAC connection switch control clear
CTBM0_CTB_SW_SQ_CTRL	0x409000C4	CTB bus switch Sar Sequencer control
CTBM0_CTB_SW_STATUS	0x409000C8	CTB bus switch control status
CTBM0_OA0_OFFSET_TRIM	0x40900F00	Opamp0 trim control
CTBM0_OA0_SLOPE_OFFSET_TRIM	0x40900F04	Opamp0 trim control
CTBM0_OA0_COMP_TRIM	0x40900F08	Opamp0 trim control
CTBM0_OA1_OFFSET_TRIM	0x40900F0C	Opamp1 trim control
CTBM0_OA1_SLOPE_OFFSET_TRIM	0x40900F10	Opamp1 trim control
CTBM0_OA1_COMP_TRIM	0x40900F14	Opamp1 trim control

25.1.1 CTBM0_CTB_CTRL

global CTB and power control

Address: 0x40900000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	ENABLED	DEEPS-LEEP_ON	None [29:24]					

Bits	Name	Description
31	ENABLED	- 0: CTBm disabled (put analog in power down, open all switches) - 1: CTBm enabled Default Value: 0
30	DEEPSLEEP_ON	- 0: CTBm is disabled during DeepSleep power mode - 1: CTBm remains enabled during DeepSleep power mode (if ENABLED=1) Default Value: 0

25.1.2 CTBM0_OA_RES0_CTRL

Opamp0 and resistor0 control

Address: 0x40900004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW		
HW Access	R	R	R	R	R	R		
Name	OA0_DSI_LEVEL	OA0_BYPASS_DSI_SYNC	OA0_HYST_EN	OA0_COMP_EN	OA0_DRIVE_STR_SEL	OA0_PWR_MODE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	None	RW	
HW Access	None			R	R	None	R	
Name	None [15:13]			OA0_BOOST_EN	OA0_PUMP_EN	None	OA0_COMPINT [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	OA0_BOOST_EN	Reserved Default Value: 0
11	OA0_PUMP_EN	Opamp0 pump enable Default Value: 0
9 : 8	OA0_COMPINT	Opamp comparator edge detect for interrupt and pulse mode of trigger Default Value: 0 **0x0: DISABLE :** Disabled, no interrupts will be detected **0x1: RISING :** Rising edge

25.1.2 CTBM0_OA_RES0_CTRL (continued)

		0x2: FALLING : Falling edge **0x3: BOTH :** Both rising and falling edges
7	OA0_DSI_LEVEL	Opamp comparator trigger output level : 0=pulse, each time an edge is detected (see OA0_COMPINT) a pulse is sent out on trigger 1=level, trigger output is a synchronized version of the comparator output Default Value: 0
6	OA0_BY-PASS_DSI_SYNC	Opamp bypass comparator output synchronization for trigger output: 0=synchronize (level or pulse), 1=bypass (asynchronous output). Default Value: 0
5	OA0_HYST_EN	Opamp hysteresis enable. See the device Datasheet for hysteresis specifications. Default Value: 0
4	OA0_COMP_EN	Opamp0 comparator enable Default Value: 0
3	OA0_DRIVE_STR_SEL	Opamp output drive strength: 0=1x, 1=10x. See the device Datasheet for exact current ranges and related specifications.This setting sets specific requirements for OA0_BOOST_EN and OA0_COMP_TRIM. Default Value: 0
2 : 0	OA0_PWR_MODE	Opamp power level. Reduced power levels also reduce gain-bandwidth (GBW). See the "Opamp Specifications" table in the device Datasheet for more details. Default Value: 0 **0x0: OFF :** Off **0x1: LOW :** Power setting = Low (low current consumption and GBW) **0x2: MEDIUM :** Power setting = Medium (moderate current consumption and GBW) **0x3: HIGH :** Power setting = High (high current consumption and GBW) **0x4: RESERVED :** Reserved

25.1.2 CTBM0_OA_RES0_CTRL (continued)

0x5: PS_LOW :

Power setting = Power Saver Low (works in Deep Sleep system power mode, with charge pump off, and reduced input common mode volage range)

0x6: PS_MEDIUM :

Power setting = Power Saver Medium (works in Deep Sleep system power mode, with charge pump off, and reduced input common mode volage range)

0x7: PS_HIGH :

Power setting = Power Saver High (works in Deep Sleep system power mode, with charge pump off, and reduced input common mode volage range)

25.1.3 CTBM0_OA_RES1_CTRL

Opamp1 and resistor1 control

Address: 0x40900008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW		
HW Access	R	R	R	R	R	R		
Name	OA1_DSI_LEVEL	OA1_BYPASS_DSI_SYNC	OA1_HYST_EN	OA1_COMP_EN	OA1_DRIVE_STR_SEL	OA1_PWR_MODE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	None	RW	
HW Access	None			R	R	None	R	
Name	None [15:13]			OA1_BOOST_EN	OA1_PUMP_EN	None	OA1_COMPINT [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	OA1_BOOST_EN	Reserved Default Value: 0
11	OA1_PUMP_EN	Opamp1 pump enable Default Value: 0
9 : 8	OA1_COMPINT	Opamp comparator edge detect for interrupt and pulse mode of trigger Default Value: 0 **0x0: DISABLE :** Disabled, no interrupts will be detected **0x1: RISING :** Rising edge

25.1.3 CTBM0_OA_RES1_CTRL (continued)

		0x2: FALLING : Falling edge **0x3: BOTH :** Both rising and falling edges
7	OA1_DSI_LEVEL	Opamp comparator trigger output level : 0=pulse, each time an edge is detected (see OA1_COMPINT) a pulse is sent out on trigger 1=level, trigger output is a synchronized version of the comparator output Default Value: 0
6	OA1_BY-PASS_DSI_SYNC	Opamp bypass comparator output synchronization for trigger output: 0=synchronize (level or pulse), 1=bypass (asynchronous output). Default Value: 0
5	OA1_HYST_EN	Opamp hysteresis enable. See the device Datasheet for hysteresis specifications. Default Value: 0
4	OA1_COMP_EN	Opamp1 comparator enable Default Value: 0
3	OA1_DRIVE_STR_SEL	Opamp output drive strength: 0=1x, 1=10x. See the device Datasheet for exact current ranges and related specifications.This setting sets specific requirements for OA1_BOOST_EN and OA1_COMP_TRIM Default Value: 0
2 : 0	OA1_PWR_MODE	Opamp power level. Reduced power levels also reduce gain-bandwidth (GBW). See the "Opamp Specifications" table in the device Datasheet for more details. Default Value: 0

25.1.4 CTBM0_COMP_STAT

Comparator status

Address: 0x4090000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							OA0_-COMP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							W
Name	None [23:17]							OA1_-COMP

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	OA1_COMP	Opamp1 current comparator status Default Value: 0
0	OA0_COMP	Opamp0 current comparator status Default Value: 0

25.1.5 CTBM0_INTR

Interrupt request register

Address: 0x40900020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						COMP1	COMP0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1	Comparator 1 Interrupt: hardware sets this interrupt when comparator 1 triggers. Write with '1' to clear bit. Default Value: 0
0	COMP0	Comparator 0 Interrupt: hardware sets this interrupt when comparator 0 triggers. Write with '1' to clear bit. Default Value: 0

25.1.6 CTBM0_INTR_SET

Interrupt request set register

Address: 0x40900024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						COMP1_SET	COMP0_SET

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	COMP0_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

25.1.7 CTBM0_INTR_MASK

Interrupt request mask

Address: 0x40900028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						COMP1_MASK	COMP0_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	COMP0_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.8 CTBM0_INTR_MASKED

Interrupt request masked

Address: 0x4090002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						COMP1_MASKED	COMP0_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
0	COMP0_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

25.1.9 CTBM0_OA0_SW

Opamp0 switch control

Address: 0x40900080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S	RW1S	None	RW1S
HW Access	None				RW1C	RW1C	None	RW1C
Name	None [7:4]				OA0P_A30	OA0P_A20	None	OA0P_A00

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1S	None					RW1S
HW Access	None	RW1C	None					RW1C
Name	None	OA0M_A81	None [13:9]					OA0M_A11

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1S	None		RW1S	None	
HW Access	None		RW1C	None		RW1C	None	
Name	None [23:22]		OA0O_D81	None [20:19]		OA0O_D51	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	OA0O_D81	Switch that shorts Opamp's 1x and 10x outputs. Default Value: 0
18	OA0O_D51	Switch that connects Opamp's output to SARBUS 0. Default Value: 0
14	OA0M_A81	Switch that connects Opamp's inverting terminal to Opamp's output for follower mode. Default Value: 0
8	OA0M_A11	Switch that connects Opamp's inverting terminal to pin 1 of CTBm port . Default Value: 0
3	OA0P_A30	Switch that connects Opamp's non-inverting terminal to pin 6 of CTBm port. Note that this bus can have additional connections to or from the CTDAC. See the Architecture TRM for details. Default Value: 0
2	OA0P_A20	Switch that connects Opamp's non-inverting terminal to pin 0 of CTBm port. See the device Data-sheet for the location of CTBm port. Default Value: 0
0	OA0P_A00	Switch that connects Opamp's non-inverting terminal to AMUXBUS A. Default Value: 0

25.1.10 CTBM0_OA0_SW_CLEAR

Opamp0 switch control clear

Address: 0x40900084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	None	RW1C
HW Access	None				A	A	None	A
Name	None [7:4]				OA0P_A30	OA0P_A20	None	OA0P_A00

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1C	None					RW1C
HW Access	None	A	None					A
Name	None	OA0M_A81	None [13:9]					OA0M_A11

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1C	None		RW1C	None	
HW Access	None		A	None		A	None	
Name	None [23:22]		OA0O_D81	None [20:19]		OA0O_D51	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	OA0O_D81	see corresponding bit in OA0_SW Default Value: 0
18	OA0O_D51	see corresponding bit in OA0_SW Default Value: 0
14	OA0M_A81	see corresponding bit in OA0_SW Default Value: 0
8	OA0M_A11	see corresponding bit in OA0_SW Default Value: 0
3	OA0P_A30	see corresponding bit in OA0_SW Default Value: 0
2	OA0P_A20	see corresponding bit in OA0_SW Default Value: 0
0	OA0P_A00	see corresponding bit in OA0_SW Default Value: 0

25.1.11 CTBM0_OA1_SW

Opamp1 switch control

Address: 0x40900088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	None		RW1S	None		RW1S	RW1S
HW Access	RW1C	None		RW1C	None		RW1C	RW1C
Name	OA1P_A73	None [6:5]		OA1P_A43	None [3:2]		OA1P_A13	OA1P_A03

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1S	None					RW1S
HW Access	None	RW1C	None					RW1C
Name	None	OA1M_A82	None [13:9]					OA1M_A22

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1S	None	RW1S	RW1S	None	
HW Access	None		RW1C	None	RW1C	RW1C	None	
Name	None [23:22]		OA1O_D82	None	OA1O_D62	OA1O_D52	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	OA1O_D82	Switch that shorts Opamp's 1x and 10x outputs. Default Value: 0
19	OA1O_D62	Switch that connects Opamp's output to SARBUS 1. Default Value: 0
18	OA1O_D52	Switch that connects Opamp's output to SARBUS 0. Default Value: 0
14	OA1M_A82	Switch that connects Opamp's inverting terminal to Opamp's output for follower mode. Default Value: 0
8	OA1M_A22	Switch that connects Opamp's inverting terminal to pin 4 of CTBm port. Default Value: 0
7	OA1P_A73	Switch that connects Opamp's non-inverting terminal to VREF. Default Value: 0
4	OA1P_A43	Switch that connects Opamp's non-inverting terminal to pin 7 of CTBm port. Default Value: 0

25.1.11 CTBM0_OA1_SW (continued)

1	OA1P_A13	Switch that connects Opamp's non-inverting terminal to pin 5 of CTBm port. See the device Datasheet for the location of CTBm port. Default Value: 0
0	OA1P_A03	Switch that connects Opamp's non-inverting terminal to AMUXBUS B. Default Value: 0

25.1.12 CTBM0_OA1_SW_CLEAR

Opamp1 switch control clear

Address: 0x4090008C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	None		RW1C	None		RW1C	RW1C
HW Access	A	None		A	None		A	A
Name	OA1P_A73	None [6:5]		OA1P_A43	None [3:2]		OA1P_A13	OA1P_A03

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1C	None					RW1C
HW Access	None	A	None					A
Name	None	OA1M_A82	None [13:9]					OA1M_A22

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1C	None	RW1C	RW1C	None	
HW Access	None		A	None	A	A	None	
Name	None [23:22]		OA1O_D82	None	OA1O_D62	OA1O_D52	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	OA1O_D82	see corresponding bit in OA1_SW Default Value: 0
19	OA1O_D62	see corresponding bit in OA1_SW Default Value: 0
18	OA1O_D52	see corresponding bit in OA1_SW Default Value: 0
14	OA1M_A82	see corresponding bit in OA1_SW Default Value: 0
8	OA1M_A22	see corresponding bit in OA1_SW Default Value: 0
7	OA1P_A73	see corresponding bit in OA1_SW Default Value: 0
4	OA1P_A43	see corresponding bit in OA1_SW Default Value: 0
1	OA1P_A13	see corresponding bit in OA1_SW Default Value: 0

25.1.12 CTBM0_OA1_SW_CLEAR (continued)

0	OA1P_A03	see corresponding bit in OA1_SW Default Value: 0

25.1.13 CTBM0_CTD_SW

CTDAC connection switch control

Address: 0x409000A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1S	RW1S	None		RW1S	None
HW Access	None		RW1C	RW1C	None		RW1C	None
Name	None [7:6]		CTDS_COR	CTDS_CRS	None [3:2]		CTDD_CRD	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S	RW1S	RW1S	RW1S	None	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	None	RW1C	RW1C	RW1C
Name	CTDH_ILR	CTDH_CIS	CTDH_CA0	CTDH_CHD	None	CTDH_COB	CTDO_-COS	CTDO_C6H

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	CTDH_ILR	Switch that shorts Opamp0's inverting and non-inverting inputs to reduce hold capacitor leakage. Default Value: 0
14	CTDH_CIS	Switch that isolates hold capacitor from other inputs connected to Opamp0's non-inverting input. Default Value: 0
13	CTDH_CA0	Switch that connects hold capacitor to Opamp0's non-inverting input. Default Value: 0
12	CTDH_CHD	Hold capacitor connect Default Value: 0
10	CTDH_COB	Switch that connects hold capacitor to Opamp0's output. Used during hold mode in Sample and Hold operation. Default Value: 0
9	CTDO_COS	Switch that connects ctdvout to the internal hold capacitor (Sampling Switch). Note this switch will temporarily be opened for deglitching if CTDAC.DEGLITCH_COS is set. Default Value: 0

25.1.13 CTBM0_CTD_SW (continued)

8	CTDO_C6H	Switch that connects pin 6 of the CTBm port to ctdvout (CTDAC Vout). See the device Datasheet for the location of CTBm port. Default Value: 0
5	CTDS_COR	Switch that connects Opamp1's inverting input to ctdvout (CTDAC Vout). Default Value: 0
4	CTDS_CRS	Switch that connects Opamp1's inverting input to ctdrefsense (CTDAC Reference Sense). Default Value: 0
1	CTDD_CRD	Switch that connects Opamp1's output to ctdrefdrive (CTDAC Reference Drive). Default Value: 0

25.1.14 CTBM0_CTD_SW_CLEAR

CTDAC connection switch control clear

Address: 0x409000A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1C	RW1C	None		RW1C	None
HW Access	None		A	A	None		A	None
Name	None [7:6]		CTDS_COR	CTDS_CRS	None [3:2]		CTDD_CRD	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C	RW1C	RW1C	RW1C	None	RW1C	RW1C	RW1C
HW Access	A	A	A	A	None	A	A	A
Name	CTDH_ILR	CTDH_CIS	CTDH_CA0	CTDH_CHD	None	CTDH_COB	CTDO_-COS	CTDO_C6H

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	CTDH_ILR	see corresponding bit in CTD_SW Default Value: 0
14	CTDH_CIS	see corresponding bit in CTD_SW Default Value: 0
13	CTDH_CA0	see corresponding bit in CTD_SW Default Value: 0
12	CTDH_CHD	see corresponding bit in CTD_SW Default Value: 0
10	CTDH_COB	see corresponding bit in CTD_SW Default Value: 0
9	CTDO_COS	see corresponding bit in CTD_SW Default Value: 0
8	CTDO_C6H	see corresponding bit in CTD_SW Default Value: 0

25.1.14 CTBM0_CTD_SW_CLEAR (continued)

5	CTDS_COR	see corresponding bit in CTD_SW Default Value: 0
4	CTDS_CRS	see corresponding bit in CTD_SW Default Value: 0
1	CTDD_CRD	see corresponding bit in CTD_SW Default Value: 0

25.1.15 CTBM0_CTB_SW_SQ_CTRL

CTB bus switch Sar Sequencer control

Address: 0x409000C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	None	
HW Access	None				R	R	None	
Name	None [15:12]				P3_SQ_C-TRL23	P2_SQ_C-TRL23	None [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	P3_SQ_CTRL23	for D52, D62 Default Value: 0
10	P2_SQ_CTRL23	for D51 Default Value: 0

25.1.16 CTBM0_CTB_SW_STATUS

CTB bus switch control status

Address: 0x409000C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	R	None			
HW Access	W	W	W	W	None			
Name	CTD_COS_STAT	OA1O_D62_STAT	OA1O_D52_STAT	OA0O_D51_STAT	None [27:24]			

Bits	Name	Description
31	CTD_COS_STAT	see COS bit in CTD_SW Default Value: 0
30	OA1O_D62_STAT	see OA1O_D62 bit in OA1_SW Default Value: 0
29	OA1O_D52_STAT	see OA1O_D52 bit in OA1_SW Default Value: 0
28	OA0O_D51_STAT	see OA0O_D51 bit in OA0_SW Default Value: 0

25.1.17 CTBM0_OA0_OFFSET_TRIM

Opamp0 trim control

Address: 0x40900F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OA0_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	OA0_OFFSET_TRIM	Opamp0 offset trim Default Value: 0

25.1.18 CTBM0_OA0_SLOPE_OFFSET_TRIM

Opamp0 trim control

Address: 0x40900F04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OA0_SLOPE_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	OA0_SLOPE_OFF-SET_TRIM	Opamp0 slope offset drift trim Default Value: 0

25.1.19 CTBM0_OA0_COMP_TRIM

Opamp0 trim control

Address: 0x40900F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						OA0_COMP_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	OA0_COMP_TRIM	Opamp0 Compensation Capacitor Trim. Value depends on the drive strength setting - 1x mode: set to 01; 10x mode: set to 11 Default Value: 0

25.1.20 CTBM0_OA1_OFFSET_TRIM

Opamp1 trim control

Address: 0x40900F0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OA1_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	OA1_OFFSET_TRIM	Opamp1 offset trim Default Value: 0

25.1.21 CTBM0_OA1_SLOPE_OFFSET_TRIM

Opamp1 trim control

Address: 0x40900F10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OA1_SLOPE_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	OA1_SLOPE_OFF-SET_TRIM	Opamp1 slope offset drift trim Default Value: 0

25.1.22 CTBM0_OA1_COMP_TRIM

Opamp1 trim control

Address: 0x40900F14

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						OA1_COMP_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	OA1_COMP_TRIM	Opamp1 Compensation Capacitor Trim. Value depends on the drive strength setting - 1x mode: set to 01; 10x mode: set to 11 Default Value: 0

26 Continuous-Time DAC Registers

This section discusses the Continuous-Time DAC (CTDAC) Registers. It lists all the registers in mapping tables, in address order

26.1 Register Details

Register	Address	Description
CTDAC0_CTDAC_CTRL	0x40940000	Global CTDAC control
CTDAC0_INTR	0x40940020	Interrupt request register
CTDAC0_INTR_SET	0x40940024	Interrupt request set register
CTDAC0_INTR_MASK	0x40940028	Interrupt request mask
CTDAC0_INTR_MASKED	0x4094002C	Interrupt request masked
CTDAC0_CTDAC_SW	0x409400B0	CTDAC switch control
CTDAC0_CTDAC_SW_CLEAR	0x409400B4	CTDAC switch control clear
CTDAC0_CTDAC_VAL	0x40940100	DAC Value
CTDAC0_CTDAC_VAL_NXT	0x40940104	Next DAC value (double buffering)

26.1.1 CTDAC0_CTDAC_CTRL

Global CTDAC control

Address: 0x40940000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		DEGLITCH_CNT [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						DEG-LITCH_-COS	DEG-LITCH_CO6

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	CT-DAC_RANGE	OUT_EN	None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	None	RW	
HW Access	R	R	R	R	R	None	R	
Name	ENABLED	DEEPS-LEEP_ON	DSI_STROBE_LEVEL	DSI_STROBE_EN	DIS-ABLED_-MODE	None	CTDAC_MODE [25:24]	

Bits	Name	Description
31	ENABLED	0: CTDAC IP disabled (put analog in power down, open all switches) 1: CTDAC IP enabled Default Value: 0
30	DEEPSLEEP_ON	- 0: CTDAC IP disabled off during DeepSleep power mode - 1: CTDAC IP remains enabled during DeepSleep power mode (if ENABLED=1) Default Value: 0
29	DSI_STROBE_LEVEL	Select level or edge detect for DSI strobe - 0: DSI strobe signal is a pulse input, after a positive edge is detected on the DSI strobe signal the next DAC value update is done on the next CTDAC clock - 1: DSI strobe signal is a level input, as long as the DSI strobe signal remains high the CTDAC will do a next DAC value update on each CTDAC clock. Default Value: 0

26.1.1 CTDAC0_CTDAC_CTRL (continued)

28	DSI_STROBE_EN	DSI strobe input Enable. This enables CTDAC updates to be further throttled by DSI. 0: Ignore DSI strobe input 1: Only do a CTDAC update if allowed by the DSI strobe (throttle), see below for level or edge Default Value: 0
27	DISABLED_MODE	Select the output value when the output is disabled (OUT_EN=0) (for risk mitigation) 0: Tri-state CTDAC output when disabled 1: output Vssa or Vref when disabled (see OUT_EN description) Default Value: 0
25 : 24	CTDAC_MODE	DAC mode, this determines the Value decoding Default Value: 0 **0x0: UNSIGNED12 :** Unsigned 12-bit VDAC, i.e. no value decoding. **0x1: VIRT_SIGNED12 :** Virtual signed 12-bits' VDAC. Value decoding: add 0x800 to the 12-bit Value (=invert MSB), to convert the lowest signed number 0x800 to the lowest unsigned number 0x000. This is the same as the SAR handles 12-bit 'virtual' signed numbers. **0x2: RESERVED2 :** **0x3: RESERVED3 :**
23	CTDAC_RANGE	By closing the bottom switch in the R2R network the output is lifted by one LSB, effectively adding 1 0: Range is [0, 4095] * Vref / 4096 1: Range is [1, 4096] * Vref / 4096 Default Value: 0
22	OUT_EN	Output enable, intended to be used during the Hold phase of the Sample and Hold when power cycling : 0: output disabled, the output is either: - Tri-state (DISABLED_MODE=0) - or Vssa (DISABLED_MODE=1 && CTDAC_RANGE=0) - or Vref (DISABLED_MODE=1 && CTDAC_RANGE=1) 1: output enabled, CTDAC output drives the programmed VALUE Default Value: 0
9	DEGLITCH_COS	Force CTB.COS switch open after each VALUE change for the set number of clock cycles. Default Value: 0
8	DEGLITCH_CO6	Force CTDAC.CO6 switch open after each VALUE change for the set number of clock cycles. Default Value: 0
5 : 0	DEGLITCH_CNT	To prevent glitches after VALUE changes from propagating the output switch can be opened for DEGLITCH_CNT+1 clk_peri clock cycles. Default Value: 0

26.1.2 CTDAC0_INTR

Interrupt request register

Address: 0x40940020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [7:1]							VDAC_EMPTY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	VDAC_EMPTY	VDAC Interrupt: hardware sets this interrupt when VDAC next value field is empty, i.e. was copied to the current VALUE. Write with '1' to clear bit. Default Value: 0

26.1.3 CTDAC0_INTR_SET

Interrupt request set register

Address: 0x40940024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							A
Name	None [7:1]							VDAC_EMPTY_SET

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	VDAC_EMPTY_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

26.1.4 CTDAC0_INTR_MASK

Interrupt request mask

Address: 0x40940028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							VDAC_EMPTY_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	VDAC_EMPTY_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

26.1.5 CTDAC0_INTR_MASKED

Interrupt request masked

Address: 0x4094002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							VDAC_EMPTY_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	VDAC_EMPTY_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

26.1.6 CTDAC0_CTDAC_SW

CTDAC switch control

Address: 0x409400B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							CTDD_CVD

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [15:9]							CTDO_CO6

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	CTDO_CO6	ctdvout to P6 pin. Note this switch will temporarily be opened for deglitching if DEGLITCH_CO6 is set Default Value: 0
0	CTDD_CVD	VDDA supply to ctdrefdrive Default Value: 0

26.1.7 CTDAC0_CTDAC_SW_CLEAR

CTDAC switch control clear

Address: 0x409400B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1C
HW Access	None							A
Name	None [7:1]							CTDD_CVD

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							CTDO_CO6

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	CTDO_CO6	see corresponding bit in CTD_SW Default Value: 0
0	CTDD_CVD	see corresponding bit in CTD_SW Default Value: 0

26.1.8 CTDAC0_CTDAC_VAL

DAC Value

Address: 0x40940100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				RW			
Name	None [15:12]				VALUE [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 0	VALUE	Value, in CTDAC_MODE 1 this value is decoded Default Value: 0

26.1.9 CTDAC0_CTDAC_VAL_NXT

Next DAC value (double buffering)

Address: 0x40940104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				VALUE [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 0	VALUE	Next value for CTDAC_VAL.VALUE Default Value: 0

27 SAR ADC Registers

This section discusses the SAR ADC registers. It lists all the registers in mapping tables, in address order.

27.1 Register Details

Register	Address	Description
SAR0_CTRL	0x409B0000	Analog control register.
SAR0_SAMPLE_CTRL	0x409B0004	Sample control register.
SAR0_SAMPLE_TIME01	0x409B0010	Sample time specification ST0 and ST1
SAR0_SAMPLE_TIME23	0x409B0014	Sample time specification ST2 and ST3
SAR0_RANGE_THRES	0x409B0018	Global range detect threshold register.
SAR0_RANGE_COND	0x409B001C	Global range detect mode register.
SAR0_CHAN_EN	0x409B0020	Enable bits for the channels
SAR0_START_CTRL	0x409B0024	Start control register (firmware trigger).
SAR0_CHAN_CONFIG0	0x409B0080	Channel configuration register.
SAR0_CHAN_CONFIG1	0x409B0084	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR0_CHAN_CONFIG2	0x409B0088	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR0_CHAN_CONFIG3	0x409B008C	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR0_CHAN_CONFIG4	0x409B0090	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR0_CHAN_CONFIG5	0x409B0094	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR0_CHAN_CONFIG6	0x409B0098	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR0_CHAN_CONFIG7	0x409B009C	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR0_CHAN_CONFIG8	0x409B00A0	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR0_CHAN_CONFIG9	0x409B00A4	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR0_CHAN_CONFIG10	0x409B00A8	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR0_CHAN_CONFIG11	0x409B00AC	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR0_CHAN_CONFIG12	0x409B00B0	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR0_CHAN_CONFIG13	0x409B00B4	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR0_CHAN_CONFIG14	0x409B00B8	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR0_CHAN_CONFIG15	0x409B00BC	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR0_CHAN_WORK0	0x409B0100	Channel working data register
SAR0_CHAN_WORK1	0x409B0104	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR0_CHAN_WORK2	0x409B0108	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.

Register	Address	Description
SAR0_CHAN_WORK3	0x409B010C	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR0_CHAN_WORK4	0x409B0110	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR0_CHAN_WORK5	0x409B0114	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR0_CHAN_WORK6	0x409B0118	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR0_CHAN_WORK7	0x409B011C	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR0_CHAN_WORK8	0x409B0120	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR0_CHAN_WORK9	0x409B0124	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR0_CHAN_WORK10	0x409B0128	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR0_CHAN_WORK11	0x409B012C	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR0_CHAN_WORK12	0x409B0130	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR0_CHAN_WORK13	0x409B0134	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR0_CHAN_WORK14	0x409B0138	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR0_CHAN_WORK15	0x409B013C	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR0_CHAN_RESULT0	0x409B0180	Channel result data register
SAR0_CHAN_RESULT1	0x409B0184	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR0_CHAN_RESULT2	0x409B0188	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR0_CHAN_RESULT3	0x409B018C	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR0_CHAN_RESULT4	0x409B0190	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR0_CHAN_RESULT5	0x409B0194	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR0_CHAN_RESULT6	0x409B0198	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR0_CHAN_RESULT7	0x409B019C	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR0_CHAN_RESULT8	0x409B01A0	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR0_CHAN_RESULT9	0x409B01A4	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR0_CHAN_RESULT10	0x409B01A8	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR0_CHAN_RESULT11	0x409B01AC	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR0_CHAN_RESULT12	0x409B01B0	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR0_CHAN_RESULT13	0x409B01B4	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR0_CHAN_RESULT14	0x409B01B8	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR0_CHAN_RESULT15	0x409B01BC	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR0_CHAN_WORK_UPDATED	0x409B0200	Channel working data register 'updated' bits
SAR0_CHAN_RESULT_UPDATED	0x409B0204	Channel result data register 'updated' bits
SAR0_INTR	0x409B0210	Interrupt request register.
SAR0_INTR_SET	0x409B0214	Interrupt set request register
SAR0_INTR_MASK	0x409B0218	Interrupt mask register.
SAR0_INTR_MASKED	0x409B021C	Interrupt masked request register
SAR0_SATURATE_INTR	0x409B0220	Saturate interrupt request register.
SAR0_SATURATE_INTR_SET	0x409B0224	Saturate interrupt set request register
SAR0_SATURATE_INTR_MASK	0x409B0228	Saturate interrupt mask register.
SAR0_SATURATE_INTR_MASKED	0x409B022C	Saturate interrupt masked request register
SAR0_RANGE_INTR	0x409B0230	Range detect interrupt request register.
SAR0_RANGE_INTR_SET	0x409B0234	Range detect interrupt set request register
SAR0_RANGE_INTR_MASK	0x409B0238	Range detect interrupt mask register.

Register	Address	Description
SAR0_RANGE_INTR_MASKED	0x409B023C	Range interrupt masked request register
SAR0_INTR_CAUSE	0x409B0240	Interrupt cause register
SAR0_INJ_CHAN_CONFIG	0x409B0280	Injection channel configuration register.
SAR0_INJ_RESULT	0x409B0290	Injection channel result register
SAR0_STATUS	0x409B02A0	Current status of internal SAR registers (mostly for debug)
SAR0_AVG_STAT	0x409B02A4	Current averaging status (for debug)
SAR0_MUX_SWITCH0	0x409B0300	SARMUX Firmware switch controls
SAR0_MUX_SWITCH_CLEAR0	0x409B0304	SARMUX Firmware switch control clear
SAR0_MUX_SWITCH_SQ_CTRL	0x409B0344	SARMUX switch Sar Sequencer control
SAR0_MUX_SWITCH_STATUS	0x409B0348	SARMUX switch status
SAR1_CTRL	0x409C0000	Analog control register.. See SAR0_CTRL for the details of bit fields.
SAR1_SAMPLE_CTRL	0x409C0004	Sample control register.. See SAR0_SAMPLE_CTRL for the details of bit fields.
SAR1_SAMPLE_TIME01	0x409C0010	Sample time specification ST0 and ST1. See SAR0_SAMPLE_TIME01 for the details of bit fields.
SAR1_SAMPLE_TIME23	0x409C0014	Sample time specification ST2 and ST3. See SAR0_SAMPLE_TIME23 for the details of bit fields.
SAR1_RANGE_THRES	0x409C0018	Global range detect threshold register.. See SAR0_RANGE_THRES for the details of bit fields.
SAR1_RANGE_COND	0x409C001C	Global range detect mode register.. See SAR0_RANGE_COND for the details of bit fields.
SAR1_CHAN_EN	0x409C0020	Enable bits for the channels. See SAR0_CHAN_EN for the details of bit fields.
SAR1_START_CTRL	0x409C0024	Start control register (firmware trigger).. See SAR0_START_CTRL for the details of bit fields.
SAR1_CHAN_CONFIG0	0x409C0080	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR1_CHAN_CONFIG1	0x409C0084	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR1_CHAN_CONFIG2	0x409C0088	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR1_CHAN_CONFIG3	0x409C008C	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR1_CHAN_CONFIG4	0x409C0090	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR1_CHAN_CONFIG5	0x409C0094	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR1_CHAN_CONFIG6	0x409C0098	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR1_CHAN_CONFIG7	0x409C009C	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR1_CHAN_CONFIG8	0x409C00A0	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR1_CHAN_CONFIG9	0x409C00A4	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR1_CHAN_CONFIG10	0x409C00A8	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR1_CHAN_CONFIG11	0x409C00AC	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR1_CHAN_CONFIG12	0x409C00B0	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR1_CHAN_CONFIG13	0x409C00B4	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR1_CHAN_CONFIG14	0x409C00B8	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR1_CHAN_CONFIG15	0x409C00BC	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR1_CHAN_WORK0	0x409C0100	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR1_CHAN_WORK1	0x409C0104	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR1_CHAN_WORK2	0x409C0108	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR1_CHAN_WORK3	0x409C010C	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR1_CHAN_WORK4	0x409C0110	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR1_CHAN_WORK5	0x409C0114	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR1_CHAN_WORK6	0x409C0118	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR1_CHAN_WORK7	0x409C011C	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.

Register	Address	Description
SAR1_CHAN_WORK8	0x409C0120	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR1_CHAN_WORK9	0x409C0124	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR1_CHAN_WORK10	0x409C0128	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR1_CHAN_WORK11	0x409C012C	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR1_CHAN_WORK12	0x409C0130	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR1_CHAN_WORK13	0x409C0134	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR1_CHAN_WORK14	0x409C0138	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR1_CHAN_WORK15	0x409C013C	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR1_CHAN_RESULT0	0x409C0180	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR1_CHAN_RESULT1	0x409C0184	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR1_CHAN_RESULT2	0x409C0188	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR1_CHAN_RESULT3	0x409C018C	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR1_CHAN_RESULT4	0x409C0190	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR1_CHAN_RESULT5	0x409C0194	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR1_CHAN_RESULT6	0x409C0198	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR1_CHAN_RESULT7	0x409C019C	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR1_CHAN_RESULT8	0x409C01A0	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR1_CHAN_RESULT9	0x409C01A4	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR1_CHAN_RESULT10	0x409C01A8	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR1_CHAN_RESULT11	0x409C01AC	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR1_CHAN_RESULT12	0x409C01B0	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR1_CHAN_RESULT13	0x409C01B4	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR1_CHAN_RESULT14	0x409C01B8	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR1_CHAN_RESULT15	0x409C01BC	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR1_CHAN_WORK_UPDATED	0x409C0200	Channel working data register 'updated' bits. See SAR0_CHAN_WORK_UPDATED for the details of bit fields.
SAR1_CHAN_RESULT_UPDATED	0x409C0204	Channel result data register 'updated' bits. See SAR0_CHAN_RESULT_UPDATED for the details of bit fields.
SAR1_INTR	0x409C0210	Interrupt request register.. See SAR0_INTR for the details of bit fields.
SAR1_INTR_SET	0x409C0214	Interrupt set request register. See SAR0_INTR_SET for the details of bit fields.
SAR1_INTR_MASK	0x409C0218	Interrupt mask register.. See SAR0_INTR_MASK for the details of bit fields.
SAR1_INTR_MASKED	0x409C021C	Interrupt masked request register. See SAR0_INTR_MASKEDfor the details of bit fields.
SAR1_SATURATE_INTR	0x409C0220	Saturate interrupt request register.. See SAR0_SATURATE_INTR for the details of bit fields.
SAR1_SATURATE_INTR_SET	0x409C0224	Saturate interrupt set request register. See SAR0_SATURATE_INTR_SET for the details of bit fields.
SAR1_SATURATE_INTR_MASK	0x409C0228	Saturate interrupt mask register.. See SAR0_SATURATE_INTR_MASK for the details of bit fields.
SAR1_SATURATE_INTR_MASKED	0x409C022C	Saturate interrupt masked request register. See SAR0_SATURATE_INTR_MASKED for the details of bit fields.
SAR1_RANGE_INTR	0x409C0230	Range detect interrupt request register.. See SAR0_RANGE_INTR for the details of bit fields.
SAR1_RANGE_INTR_SET	0x409C0234	Range detect interrupt set request register. See SAR0_RANGE_INTR_SET for the details of bit fields.
SAR1_RANGE_INTR_MASK	0x409C0238	Range detect interrupt mask register.. See SAR0_RANGE_INTR_MASK for the details of bit fields.
SAR1_RANGE_INTR_MASKED	0x409C023C	Range interrupt masked request register. See SAR0_RANGE_INTR_MASKED for the details of bit fields.
SAR1_INTR_CAUSE	0x409C0240	Interrupt cause register. See SAR0_INTR_CAUSE for the details of bit fields.
SAR1_INJ_CHAN_CONFIG	0x409C0280	Injection channel configuration register.. See SAR0_INJ_CHAN_CONFIG for the details of bit fields.

Register	Address	Description
SAR1_INJ_RESULT	0x409C0290	Injection channel result register. See SAR0_INJ_RESULT for the details of bit fields.
SAR1_STATUS	0x409C02A0	Current status of internal SAR registers (mostly for debug). See SAR0_STATUS for the details of bit fields.
SAR1_AVG_STAT	0x409C02A4	Current averaging status (for debug). See SAR0_AVG_STAT for the details of bit fields.
SAR1_MUX_SWITCH0	0x409C0300	SARMUX Firmware switch controls. See SAR0_MUX_SWITCH0 for the details of bit fields.
SAR1_MUX_SWITCH_CLEAR0	0x409C0304	SARMUX Firmware switch control clear. See SAR0_MUX_SWITCH_CLEAR0 for the details of bit fields.
SAR1_MUX_SWITCH_SQ_CTRL	0x409C0344	SARMUX switch SAR Sequencer control. See SAR0_MUX_SWITCH_SQ_CTRL for the details of bit fields.
SAR1_MUX_SWITCH_STATUS	0x409C0348	SARMUX switch status. See SAR0_MUX_SWITCH_STATUS for the details of bit fields.

27.1.1 SAR0_CTRL

Analog control register.

Address: 0x409B0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			None	RW		
HW Access	R	R			None	R		
Name	VREF_BY-P_CAP_EN	VREF_SEL [6:4]			None	PWR_CTRL_VREF [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW	None	RW			None
HW Access	R		R	None	R			None
Name	COMP_DLY [15:14]		SAR_HW_CTRL_NEGVREF	None	NEG_SEL [11:9]			None

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW	RW	RW			
HW Access	None		R	R	R			
Name	None [23:22]		REF-BUF_EN	BOOST-PUMP_EN	SPARE [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None		RW	RW		
HW Access	R	R	None		R	R		
Name	ENABLED	SWITCH_-DISABLE	None [29:28]		DEEPS-LEEP_ON	COMP_PWR [26:24]		

Bits	Name	Description
31	ENABLED	- 0: SAR disabled (put analog in power down and stop clocks), also can clear FW_TRIGGER on write. - 1: SAR IP enabled. Default Value: 0
30	SWITCH_DISABLE	Disable SAR sequencer from enabling routing switches - 0: Normal mode, SAR sequencer changes switches according to pin address in channel configurations - 1: Switches disabled, SAR sequencer does not enable any switches. Other methods such as firmware control can be used to set the switches to route the signal to be converted through the SARMUX Default Value: 0
27	DEEPSLEEP_ON	- 0: SARMUX disabled during System Deep Sleep power mode - 1: SARMUX remains enabled during System Deep Sleep power mode (if ENABLED=1) Default Value: 0

27.1.1 SAR0_CTRL (continued)

26 : 24	COMP_PWR	Comparator power mode. Default Value: 0 **0x0: P100 :** Reserved **0x1: P80 :** Reserved **0x2: P60 :** Power = 60%, Use this for SAR Clock Frequency greater than 1.8MHz up to 18MHz. **0x3: P50 :** Reserved **0x4: P40 :** Reserved **0x5: P30 :** Reserved **0x6: P20 :** Power = 20%, Use this for SAR Clock Frequency less than or equal to 1.8MHz **0x7: P10 :** Reserved
21	REFBUF_EN	For normal ADC operation this bit must be set, for all reference choices - internal, external or vdda based reference. Setting this bit is critical to proper function of switches inside SARREF block. Default Value: 0
20	BOOSTPUMP_EN	Reserved Default Value: 0
19 : 16	SPARE	Reserved Default Value: 0
15 : 14	COMP_DLY	Set the comparator latch delay in accordance with SAR conversion rate Default Value: 0 **0x0: D2P5 :** Reserved

27.1.1 SAR0_CTRL (continued)

		0x1: D4 : Reserved **0x2: D10 :** Reserved **0x3: D12 :** 12ns delay
13	SAR_HW_C-TRL_NEGVREF	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for VREF to NEG switch. Default Value: 0
11 : 9	NEG_SEL	SARADC internal NEG selection for Single ended conversion Default Value: 0 **0x0: VSSA_KELVIN :** NEG input of SARADC is connected to "vssa_kelvin" (providing more precision around zero) when the switches are controlled by SAR sequencer (SWITCH_DISABLE = 0). When SWITCH_-DISABLE =1, selecting this option, opens the switch that connects VREF to VNEG. **0x1: ART_VSSA :** NEG input of SARADC is connected to VSSA in AROUTE close to the SARADC **0x2: P1 :** NEG input of SARADC is connected to P1 pin of SARMUX port when the switches are controlled by SAR sequencer (SWITCH_DISABLE=0) **0x3: P3 :** NEG input of SARADC is connected to P3 pin of SARMUX port when the switches are controlled by SAR sequencer (SWITCH_DISABLE=0) **0x4: P5 :** NEG input of SARADC is connected to P5 pin of SARMUX port when the switches are controlled by SAR sequencer (SWITCH_DISABLE=0) **0x5: P7 :** NEG input of SARADC is connected to P7 pin of SARMUX port when the switches are controlled by SAR sequencer (SWITCH_DISABLE=0) **0x6: ACORE :** NEG input of SARADC is connected to an ACORE in AROUTE

27.1.1 SAR0_CTRL (continued)

		0x7: VREF : NEG input of SARADC is shorted with VREF input of SARADC.
7	VREF_BYP_CAP_EN	VREF bypass cap enable when VREF buffer is on Default Value: 0
6 : 4	VREF_SEL	SARADC internal VREF selection. Default Value: 0 **0x0: VREF0 :** VREF0 from PRB (VREF buffer on) **0x1: VREF1 :** VREF1 from PRB (VREF buffer on) **0x2: VREF2 :** VREF2 from PRB (VREF buffer on) **0x3: VREF_AROUTE :** VREF from AROUTE (VREF buffer on) **0x4: VBGR :** 1.2V from AREF (VREF buffer on) **0x5: VREF_EXT :** External precision Vref direct from a pin (low impedance path). **0x6: VDDA_DIV_2 :** Vdda/2 (VREF buffer on) **0x7: VDDA :** Vdda.
2 : 0	PWR_CTRL_VREF	VREF buffer low power mode. Default Value: 0 **0x0: PWR_100 :** Reserved **0x1: PWR_80 :** Reserved

27.1.1 SAR0_CTRL (continued)

0x2: PWR_60 :

Power = 60%, Use this for SAR Clock Frequency greater than 3.6 MHz up to 18MHz.(with by-pass cap)

0x3: PWR_50 :

Reserved

0x4: PWR_40 :

Reserved

0x5: PWR_30 :

Power = 30%, Use this for SAR Clock Frequency less than or equal to 3.6MHz (with or without bypass cap)

0x6: PWR_20 :

Reserved

0x7: PWR_10 :

Reserved

27.1.2 SAR0_SAMPLE_CTRL

Sample control register.

Address: 0x409B0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW	RW	None
HW Access	R	R			R	R	R	None
Name	AVG_SHIFT	AVG_CNT [6:4]			DIFFEREN-TIAL_-SIGNED	SIN-GLE_END-ED_SIGNE D	LEFT_ALIG N	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							AVG_-MODE

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [23:20]				DSI_SYN-C_TRIG-GER	DSI_TRIG-GER_LEV-EL	DSI_TRIG-GER_EN	CONTINU-OUS

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	EO-S_DSI_OU T_EN	None [30:24]						

Bits	Name	Description
31	EOS_DSI_OUT_EN	Enable to output EOS_INTR. When enabled each time EOS_INTR is set by the hardware also a trigger pulse is send on the tr_sar_out signal. Default Value: 0
19	DSI_SYNC_TRIGGER	- 0: bypass clock domain synchronization of the trigger signal. - 1: synchronize the trigger signal to the SAR clock domain, if needed an edge detect is done in the peripheral clock domain. Default Value: 1

27.1.2 SAR0_SAMPLE_CTRL (continued)

18	DSI_TRIGGER_LEVEL	- 0: trigger signal is a pulse input, a positive edge detected on the trigger signal triggers a new scan. - 1: trigger signal is a level input, as long as the trigger signal remains high the SAR will do continuous scans. This field cannot be set when SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
17	DSI_TRIGGER_EN	- 0: firmware trigger only: disable hardware trigger tr_sar_in. - 1: enable hardware trigger tr_sar_in (e.g. from TCPWM, GPIO etc) Default Value: 0
16	CONTINUOUS	- 0: Wait for next FW_TRIGGER (one shot) or hardware trigger (e.g. from TPWM for periodic triggering) before scanning enabled channels. - 1: Continuously scan enabled channels, ignore triggers. This field cannot be set when SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
8	AVG_MODE	Averaging mode Default Value: 0 **0x0: ACCUNDUMP :** Accumulate and Dump (1st order accumulate and dump filter): a channel will be sampled back to back and averaged **0x1: INTERLEAVED :** Interleaved: Each scan (trigger) one sample is taken per channel and averaged over several scans. Interleaved averaging cannot be set by SAR_CLOCK_SEL.CLOCK_SEL =1.
7	AVG_SHIFT	Averaging shifting: after averaging the result is shifted right to fit in 12 bits. Default Value: 0
6 : 4	AVG_CNT	Averaging Count for channels that have averaging enabled (AVG_EN). A channel will be sampled (1<<(AVG_CNT+1)) = [2..256] times. - In ACCUNDUMP mode (1st order accumulate and dump filter) a channel will be sampled back to back, the average result is calculated and stored and then the next enabled channel is sampled. If shifting is not enabled (AVG_SHIFT=0) then the result is forced to shift right so that is fits in 16 bits, so right shift is done by max(0,AVG_CNT-3). - In INTERLEAVED mode one sample is taken per triggered scan, only in the scan where the final averaging count is reached a valid average is calculated and stored in the RESULT register (by definition the same scan for all the channels that have averaging enabled). In all other scans the RESULT register for averaged channels will have an invalid result and the intermediate accumulated value is stored in the 16-bit WORK register. In this mode make sure that the averaging count is low enough to ensure that the intermediate value does not exceed 16-bits otherwise the MSBs will be lost. So for a 12-bit resolution the averaging count should be set to 16 or less (AVG_CNT=<3). Default Value: 0
3	DIFFERENTIAL_SIGNED	Output data from a differential conversion as a signed value when DIFFERENTIAL_EN or NEG_ADDR_EN is set to 1 If AVG_MODE = 1 (Interleaved averaging), then DIFFERENTIAL_SIGNED must be configured identically to SINGLE_ENDED_SIGNED. Default Value: 1 **0x0: UNSIGNED :** result data is unsigned (zero extended if needed)

27.1.2 SAR0_SAMPLE_CTRL (continued)

		0x1: SIGNED : Default: result data is signed (sign extended if needed)
2	SINGLE_ENDED_-SIGNED	Output data from a single ended conversion as a signed value If AVG_MODE = 1 (Interleaved averaging), then SINGLE_ENDED_SIGNED must be configured identically to DIFFERENTIAL_SIGNED. Default Value: 0 **0x0: UNSIGNED :** Default: result data is unsigned (zero extended if needed) **0x1: SIGNED :** result data is signed (sign extended if needed)
1	LEFT_ALIGN	Left align data in data[15:0], default data is right aligned in data[11:0], with sign extension to 16 bits if the channel is differential. Default Value: 0

27.1.3 SAR0_SAMPLE_TIME01

Sample time specification ST0 and ST1

Address: 0x409B0010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SAMPLE_TIME0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SAMPLE_TIME0 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SAMPLE_TIME1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						SAMPLE_TIME1 [25:24]	

Bits	Name	Description
25 : 16	SAMPLE_TIME1	Sample time1 Default Value: 3
9 : 0	SAMPLE_TIME0	Sample time0 (aperture) in ADC clock cycles. Note that actual sample time is one clock less than specified here. The minimum sample time is 167ns, which is 3.0 cycles (4 in this field) with an 18MHz clock. Minimum legal value in this register is 2. Default Value: 3

27.1.4 SAR0_SAMPLE_TIME23

Sample time specification ST2 and ST3

Address: 0x409B0014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SAMPLE_TIME2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SAMPLE_TIME2 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SAMPLE_TIME3 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						SAMPLE_TIME3 [25:24]	

Bits	Name	Description
25 : 16	SAMPLE_TIME3	Sample time3 Default Value: 3
9 : 0	SAMPLE_TIME2	Sample time2 Default Value: 3

27.1.5 SAR0_RANGE_THRES

Global range detect threshold register.

Address: 0x409B0018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RANGE_LOW [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RANGE_LOW [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RANGE_HIGH [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	RANGE_HIGH [31:24]							

Bits	Name	Description
31 : 16	RANGE_HIGH	High threshold for range detect. Default Value: 0
15 : 0	RANGE_LOW	Low threshold for range detect. Default Value: 0

27.1.6 SAR0_RANGE_COND

Global range detect mode register.

Address: 0x409B001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	RANGE_COND [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	RANGE_COND	Range condition select. Default Value: 0 **0x0: BELOW :** result < RANGE_LOW **0x1: INSIDE :** RANGE_LOW <= result < RANGE_HIGH **0x2: ABOVE :** RANGE_HIGH <= result **0x3: OUTSIDE :** result < RANGE_LOW || RANGE_HIGH <= result

27.1.7 SAR0_CHAN_EN

Enable bits for the channels

Address: 0x409B0020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CHAN_EN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CHAN_EN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CHAN_EN	Channel enable. - 0: the corresponding channel is disabled. - 1: the corresponding channel is enabled, it will be included in the next scan. Default Value: 0

27.1.8 SAR0_START_CTRL

Start control register (firmware trigger).

Address: 0x409B0024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							FW_TRIG-GER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	FW_TRIGGER	When firmware writes a 1 here it will trigger the next scan of enabled channels, hardware clears this bit when the scan started with this trigger is completed. If scanning continuously the trigger is ignored and hardware clears this bit after the next scan is done. This bit is also cleared when the SAR is disabled. This field cannot be set when SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: 0

27.1.9 SAR0_CHAN_CONFIG0

Channel configuration register.

Address: 0x409B0080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	POS_PORT_ADDR [6:4]			None	POS_PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	None	RW
HW Access	None		R		None	R	None	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	None	DIFFEREN-TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	NEG_PORT_ADDR [22:20]			None	NEG_PIN_ADDR [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							NEG_AD-DR_EN

Bits	Name	Description
24	NEG_ADDR_EN	1 - The NEG_PIN_ADDR and NEG_PORT_ADDR determines what drives the Vminus pin. This is a variation of differential mode with no even-odd pair limitation 0 - The NEG_SEL determines what drives the Vminus pin. Default Value: 0
22 : 20	NEG_PORT_ADDR	Address of the neg port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX :** SARMUX pins. **0x5: AROUTE_VIRT2 :** AROUTE virtual port2 (VPORT2)

27.1.9 SAR0_CHAN_CONFIG0 (continued)

		0x6: AROUTE_VIRT1 : AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT :** SARMUX virtual port (VPORT0)
18 : 16	NEG_PIN_ADDR	Address of the neg pin to be sampled by this channel. When NEG_PORT_ADDR = SARMUX, NEG_PIN_ADDR selects the pin of the SARMUX port. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
8	DIFFERENTIAL_EN	Differential enable for this channel. If NEG_ADDR_EN=0 and this bit is 1 then POS_PIN_ADDR[0] is ignored and considered to be 0, i.e. POS_PIN_ADDR points to the even pin of a pin pair. In that case the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. POS_PORT_ADDR is used to identify the port that contains the pins. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (if NEG_ADDR_EN=0 then POS_PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	POS_PORT_ADDR	Address of the port that contains the pin to be sampled by this channel (connected to Vplus) Default Value: 0 **0x0: SARMUX :** SARMUX pins. **0x1: CTB0 :** CTB0 **0x2: CTB1 :** CTB1 **0x3: CTB2 :** CTB2 **0x4: CTB3 :** CTB3

27.1.9 SAR0_CHAN_CONFIG0 (continued)

		0x5: AROUTE_VIRT2 : AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1 :** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT :** SARMUX virtual port (VPORT0)
2 : 0	POS_PIN_ADDR	Address of the pin to be sampled by this channel (connected to Vplus). When POS_PORT_ADDR = SARMUX, POS_PIN_ADDR selects the pin of the SARMUX port. When POS_PORT_ADDR is set to one of the CTBs, POS_PIN_ADDR selects particular opamp output. When POS_PORT_ADDR is set to VPORT0, POS_PIN_ADDR = 0, selects temperature sensor output, POS_PIN_ADDR = 1 selects AMUXBUS-A and POS_PIN_ADDR = 2 selects AMUX-BUS-B. Default Value: 0

27.1.10 SAR0_CHAN_WORK0

Channel working data register

Address: 0x409B0100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_UP-DAT-ED_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_UPDAT-ED_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_UPDATED register. This field cannot be read if SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. This field cannot be read if SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: Undefined

27.1.11 SAR0_CHAN_RESULT0

Channel result data register

Address: 0x409B0180

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_UPDATED_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_UPDATED_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_UPDATED register. This field cannot be read if SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register. This field cannot be read if SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register. This field cannot be read if SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. This field cannot be read if SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: Undefined

27.1.12 SAR0_CHAN_WORK_UPDATED

Channel working data register 'updated' bits

Address: 0x409B0200

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CHAN_WORK_UPDATED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CHAN_WORK_UPDATED [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CHAN_WORK_UPDATED	If set the corresponding WORK register was updated, i.e. was already sampled during the current scan and, in case of Interleaved averaging, reached the averaging count. If this bit is low then either the channel is not enabled or the averaging count is not yet reached for Interleaved averaging. This field cannot be read if SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: 0

27.1.13 SAR0_CHAN_RESULT_UPDATED

Channel result data register 'updated' bits

Address: 0x409B0204

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CHAN_RESULT_UPDATED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CHAN_RESULT_UPDATED [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CHAN_RESULT_UPDATED	If set the corresponding RESULT register was updated, i.e. was sampled during the previous scan and, in case of Interleaved averaging, reached the averaging count. If this bit is low then either the channel is not enabled or the averaging count is not yet reached for Interleaved averaging. This field cannot be read if SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: 0

27.1.14 SAR0_INTR

Interrupt request register.

Address: 0x409B0210

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	INJ_COLLI-SION_INTR	IN-J_RANGE_I NTR	INJ_SATU-RATE_INTR	IN-J_EOC_IN-TR	DSI_COLLI-SION_INTR	FW_COLLI-SION_INTR	OVER-FLOW_IN-TR	EOS_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INJ_COLLISION_INTR	Reserved - must be set to 3 Default Value: 0
6	INJ_RANGE_INTR	Reserved - must be set to 2 Default Value: 0
5	INJ_SATURATE_INTR	Reserved - must be set to 1 Default Value: 0
4	INJ_EOC_INTR	Reserved - must be set to 0 Default Value: 0
3	DSI_COLLISION_INTR	This interrupt is set when a hardware trigger signal is asserted while the SAR is BUSY. Raising this interrupt is delayed to when the scan caused by the hardware trigger has been completed, i.e. not when the preceding scan with which this trigger collided is completed. When this interrupt is set it implies that the channels were sampled later than was intended (jitter). Write with '1' to clear bit. Default Value: 0

27.1.14 SAR0_INTR (continued)

2	FW_COLLISION_INTR	Firmware Collision Interrupt: hardware sets this interrupt when FW_TRIGGER is asserted while the SAR is BUSY. Raising this interrupt is delayed to when the scan caused by the FW_TRIGGER has been completed, i.e. not when the preceding scan with which this trigger collided is completed. When this interrupt is set it implies that the channels were sampled later than was intended (jitter). Write with '1' to clear bit. This interrupt cannot be used if SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
1	OVERFLOW_INTR	Overflow Interrupt: hardware sets this interrupt when it sets a new EOS_INTR while that bit was not yet cleared by the firmware. Write with '1' to clear bit. This interrupt cannot be used if SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
0	EOS_INTR	End Of Scan Interrupt: hardware sets this interrupt after completing a scan of all the enabled channels. Write with '1' to clear bit. Default Value: 0

27.1.15 SAR0_INTR_SET

Interrupt set request register

Address: 0x409B0214

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	INJ_COLLI-SION_SET	IN-J_RANGE_SET	INJ_SATU-RATE_SET	IN-J_EOC_SET	DSI_COLLI-SION_SET	FW_COLLI-SION_SET	OVER-FLOW_SET	EOS_SET

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INJ_COLLISION_SET	Reserved Default Value: 0
6	INJ_RANGE_SET	Reserved Default Value: 0
5	INJ_SATURATE_SET	Reserved Default Value: 0
4	INJ_EOC_SET	Reserved Default Value: 0
3	DSI_COLLISION_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	FW_COLLISION_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	OVERFLOW_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

27.1.15 SAR0_INTR_SET (continued)

0	EOS_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

27.1.16 SAR0_INTR_MASK

Interrupt mask register.

Address: 0x409B0218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INJ_COLLISION_MASK	INJ_RANGE_MASK	INJ_SATURATE_MASK	INJ_EOC_MASK	DSI_COLLISION_MASK	FW_COLLISION_MASK	OVERFLOW_MASK	EOS_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INJ_COLLISION_MASK	Reserved Default Value: 0
6	INJ_RANGE_MASK	Reserved Default Value: 0
5	INJ_SATURATE_MASK	Reserved Default Value: 0
4	INJ_EOC_MASK	Reserved Default Value: 0
3	DSI_COLLISION_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	FW_COLLISION_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	OVERFLOW_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.16 SAR0_INTR_MASK (continued)

0	EOS_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.17 SAR0_INTR_MASKED

Interrupt masked request register

Address: 0x409B021C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	INJ_COLLI-SION_MASKED	IN-J_RANGE_MASKED	INJ_SATU-RATE_MASKED	IN-J_EOC_MASKED	DSI_COLLI-SION_MASKED	FW_COLLI-SION_MASKED	OVER-FLOW_MASKED	EO-S_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INJ_COLLI-SION_MASKED	Reserved Default Value: 0
6	INJ_RANGE_MASKED	Reserved Default Value: 0
5	INJ_SATU-RATE_MASKED	Reserved Default Value: 0
4	INJ_EOC_MASKED	Reserved Default Value: 0
3	DSI_COLLI-SION_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
2	FW_COLLI-SION_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
1	OVERFLOW_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

27.1.17 SAR0_INTR_MASKED (continued)

0	EOS_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

27.1.18 SAR0_SATURATE_INTR

Saturate interrupt request register.

Address: 0x409B0220

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	SATURATE_INTR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW1S							
Name	SATURATE_INTR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SATURATE_INTR	Saturate Interrupt: hardware sets this interrupt for each channel if a conversion result (before averaging) of that channel is either 0x000 or 0xFFF, this is an indication that the ADC likely saturated. Write with '1' to clear bit. Default Value: 0

27.1.19 SAR0_SATURATE_INTR_SET

Saturate interrupt set request register

Address: 0x409B0224

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	SATURATE_SET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	A							
Name	SATURATE_SET [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SATURATE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

27.1.20 SAR0_SATURATE_INTR_MASK

Saturate interrupt mask register.

Address: 0x409B0228

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SATURATE_MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SATURATE_MASK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SATURATE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.21 SAR0_SATURATE_INTR_MASKED

Saturate interrupt masked request register

Address: 0x409B022C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SATURATE_MASKED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SATURATE_MASKED [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SATURATE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

27.1.22 SAR0_RANGE_INTR

Range detect interrupt request register.

Address: 0x409B0230

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	RANGE_INTR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW1S							
Name	RANGE_INTR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RANGE_INTR	Range detect Interrupt: hardware sets this interrupt for each channel if the conversion result (after averaging) of that channel met the condition specified by the SAR_RANGE registers. Write with '1' to clear bit. Default Value: 0

27.1.23 SAR0_RANGE_INTR_SET

Range detect interrupt set request register

Address: 0x409B0234

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	RANGE_SET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	A							
Name	RANGE_SET [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RANGE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

27.1.24 SAR0_RANGE_INTR_MASK

Range detect interrupt mask register.

Address: 0x409B0238

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RANGE_MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RANGE_MASK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RANGE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.25 SAR0_RANGE_INTR_MASKED

Range interrupt masked request register

Address: 0x409B023C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RANGE_MASKED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RANGE_MASKED [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RANGE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

27.1.26 SAR0_INTR_CAUSE

Interrupt cause register

Address: 0x409B0240

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	INJ_COLLI-SION_MASKED_MIR	IN-J_RANGE_MASKED_MIR	INJ_SATU-RATE_MASKED_MIR	IN-J_EOC_MASKED_MIR	DSI_COLLI-SION_MASKED_MIR	FW_COLLI-SION_MASKED_MIR	OVER-FLOW_MASKED_MIR	EO-S_MASKED_MIR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	W	W	None					
Name	RANGE_MASKED_RED	SATU-RATE_MASKED_RED	None [29:24]					

Bits	Name	Description
31	RANGE_MASKED_RED	Reduction OR of all SAR_RANGE_INTR_MASKED bits Default Value: 0
30	SATU-RATE_MASKED_RED	Reduction OR of all SAR_SATURATION_INTR_MASKED bits Default Value: 0
7	INJ_COLLI-SION_MASKED_MIR	Reserved Default Value: 0
6	IN-J_RANGE_MASKED_MIR	Reserved Default Value: 0
5	INJ_SATU-RATE_MASKED_MIR	Reserved Default Value: 0
4	INJ_EOC_MASKED_MIR	Reserved Default Value: 0

27.1.26 SAR0_INTR_CAUSE (continued)

3	DSI_COLLI-SION_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
2	FW_COLLI-SION_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
1	OVER-FLOW_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
0	EOS_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0

27.1.27 SAR0_INJ_CHAN_CONFIG

Injection channel configuration register.

Address: 0x409B0280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	INJ_PORT_ADDR [6:4]			None	INJ_PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	None	RW
HW Access	None		R		None	R	None	R
Name	None [15:14]		INJ_SAMPLE_TIME_SEL [13:12]		None	INJ_AVG_EN	None	INJ_DIFFERENTIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	RW	None					
HW Access	RW1C	R	None					
Name	INJ_START_EN	INJ_TAILGATING	None [29:24]					

Bits	Name	Description
31	INJ_START_EN	Set by firmware to enable the injection channel. If INJ_TAILGATING is not set this bit also functions as trigger for this channel. Cleared by hardware after this channel has been sampled (i.e. this channel is always one shot even if CONTINUOUS is set). Also cleared if the SAR is disabled. This field cannot be set when SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
30	INJ_TAILGATING	Injection channel tailgating. - 0: no tailgating for this channel, SAR is immediately triggered when the INJ_START_EN bit is set if the SAR is not busy. If the SAR is busy, the INJ channel addressed pin is sampled at the end of the current scan. - 1: injection channel tailgating. The addressed pin is sampled after the next trigger and after all enabled channels have been scanned. Default Value: 0
13 : 12	INJ_SAMPLE_TIME_SEL	Injection sample time select: select which of the 4 global sample times to use for this channel Default Value: 0

27.1.27 SAR0_INJ_CHAN_CONFIG (continued)

10	INJ_AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
8	INJ_DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (INJ_PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	INJ_PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX :** SARMUX pins. **0x1: CTB0 :** CTB0 **0x2: CTB1 :** CTB1 **0x3: CTB2 :** CTB2 **0x4: CTB3 :** CTB3 **0x6: AROUTE_VIRT :** AROUTE virtual port **0x7: SARMUX_VIRT :** SARMUX virtual port
2 : 0	INJ_PIN_ADDR	Address of the pin to be sampled by this injection channel. If differential is enabled then INJ_PIN_ADDR[0] is ignored and considered to be 0, i.e. INJ_PIN_ADDR points to the even pin of a pin pair. Default Value: 0

27.1.28 SAR0_INJ_RESULT

Injection channel result register

Address: 0x409B0290

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	INJ_RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	INJ_RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	R	None			
HW Access	W	W	W	W	None			
Name	INJ_EOC_INTR_MIR	INJ_RANGE_INTR_MIR	INJ_SATURATE_INTR_MIR	INJ_COLLISION_INTR_MIR	None [27:24]			

Bits	Name	Description
31	INJ_EOC_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register. This field cannot be read if SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
30	INJ_RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register. This field cannot be read if SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
29	INJ_SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register. This field cannot be read if SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
28	INJ_COLLISION_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register. This field cannot be read if SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
15 : 0	INJ_RESULT	SAR conversion result of the channel. This field cannot be read if SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: Undefined

27.1.29 SAR0_STATUS

Current status of internal SAR registers (mostly for debug)

Address: 0x409B02A0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			W				
Name	None [7:5]			CUR_CHAN [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	W	W	None					
Name	BUSY	SW_VREF_NEG	None [29:24]					

Bits	Name	Description
31	BUSY	If high then the SAR is busy with a conversion. This bit is always high when CONTINUOUS is set. Firmware should wait for this bit to be low before putting the SAR in power down. Default Value: 0
30	SW_VREF_NEG	the current switch status, including DSI and sequencer controls, of the switch in the SARADC that shorts NEG with VREF input (see NEG_SEL). This field cannot be read if SAR_CLOCK_-SEL.CLOCK_SEL =1. Default Value: 0
4 : 0	CUR_CHAN	current channel being sampled (channel 16 indicates the injection channel), only valid if BUSY. This field cannot be read if SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: 0

27.1.30 SAR0_AVG_STAT

Current averaging status (for debug)

Address: 0x409B02A4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CUR_AVG_ACCU [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CUR_AVG_ACCU [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R	None			R			
HW Access	W	None			W			
Name	INTRLV_BUSY	None [22:20]			CUR_AVG_ACCU [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	CUR_AVG_CNT [31:24]							

Bits	Name	Description
31 : 24	CUR_AVG_CNT	the current value of the averaging counter. Note that the value shown is updated after the sampling time and therefore runs ahead of the accumulator update. This field cannot be read if SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
23	INTRLV_BUSY	If high then the SAR is in the middle of Interleaved averaging spanning several scans. While this bit is high the Firmware should not make any changes to the configuration registers otherwise some results may be incorrect. Note that the CUR_AVG_CNT status register below gives an indication how many more scans need to be done to complete the Interleaved averaging. This bit can be cleared by changing the averaging mode to ACCUNDUMP or by disabling the SAR. Default Value: 0
19 : 0	CUR_AVG_ACCU	the current value of the averaging accumulator. This field cannot be read if SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: 0

27.1.31 SAR0_MUX_SWITCH0

SARMUX Firmware switch controls

Address: 0x409B0300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	MUX_FW_P7_VPLUS	MUX_FW_P6_VPLUS	MUX_FW_P5_VPLUS	MUX_FW_P4_VPLUS	MUX_FW_P3_VPLUS	MUX_FW_P2_VPLUS	MUX_FW_P1_VPLUS	MUX_FW_P0_VPLUS

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	MUX_FW_P7_VMINUS	MUX_FW_P6_VMINUS	MUX_FW_P5_VMINUS	MUX_FW_P4_VMINUS	MUX_FW_P3_VMINUS	MUX_FW_P2_VMINUS	MUX_FW_P1_VMINUS	MUX_FW_P0_VMINUS

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	MUX_FW_SARBUS1_VPLUS	MUX_FW_SARBUS0_VPLUS	MUX_FW_AMUXBUSB_VMINUS	MUX_FW_AMUXBUSA_VMINUS	MUX_FW_AMUXBUSB_VPLUS	MUX_FW_AMUXBUSA_VPLUS	MUX_FW_TEMP_VPLUS	MUX_FW_VSSA_VMINUS

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW1S	RW1S
HW Access	None						RW1C	RW1C
Name	None [31:26]						MUX_FW_SARBUS1_VMINUS	MUX_FW_SARBUS0_VMINUS

Bits	Name	Description
25	MUX_FW_SARBUS1_VMINUS	Firmware control: 0=open, 1=close switch between sarbus1 and vminus signal. Write with '1' to set bit. Default Value: 0
24	MUX_FW_SARBUS0_VMINUS	Firmware control: 0=open, 1=close switch between sarbus0 and vminus signal. Write with '1' to set bit. Default Value: 0
23	MUX_FW_SARBUS1_VPLUS	Firmware control: 0=open, 1=close switch between sarbus1 and vplus signal. Write with '1' to set bit. Default Value: 0

27.1.31 SAR0_MUX_SWITCH0 (continued)

22	MUX_FW_SAR-BUS0_VPLUS	Firmware control: 0=open, 1=close switch between sarbus0 and vplus signal. Write with '1' to set bit. Default Value: 0
21	MUX_FW_AMUXBUS-B_VMINUS	Firmware control: 0=open, 1=close switch between amuxbusb and vminus signal. Write with '1' to set bit. Default Value: 0
20	MUX_FW_AMUX-BUSA_VMINUS	Firmware control: 0=open, 1=close switch between amuxbusa and vminus signal. Write with '1' to set bit. Default Value: 0
19	MUX_FW_AMUXBUS-B_VPLUS	Firmware control: 0=open, 1=close switch between amuxbusb and vplus signal. Write with '1' to set bit. Default Value: 0
18	MUX_FW_AMUX-BUSA_VPLUS	Firmware control: 0=open, 1=close switch between amuxbusa and vplus signal. Write with '1' to set bit. Default Value: 0
17	MUX_FW_TEMP_VPLUS	Firmware control: 0=open, 1=close switch between temperature sensor and vplus signal, (also powers on the temperature sensor if AREF_CTRL.EN=1 (active mode) and AREF_CTRL.DEEP-SLEEP=1 and AREF_CTRL.DEEPSLEEP_MODE=2 or 3 (required for deepsleep mode only). The Write with '1' to set bit. Default Value: 0
16	MUX_FW_VSSA_VMI-NUS	Firmware control: 0=open, 1=close switch between vssa_kelvin and vminus signal. Write with '1' to set bit. Default Value: 0
15	MUX_FW_P7_VMINUS	Firmware control: 0=open, 1=close switch between pin P7 and vminus signal. Write with '1' to set bit. Default Value: 0
14	MUX_FW_P6_VMINUS	Firmware control: 0=open, 1=close switch between pin P6 and vminus signal. Write with '1' to set bit. Default Value: 0
13	MUX_FW_P5_VMINUS	Firmware control: 0=open, 1=close switch between pin P5 and vminus signal. Write with '1' to set bit. Default Value: 0
12	MUX_FW_P4_VMINUS	Firmware control: 0=open, 1=close switch between pin P4 and vminus signal. Write with '1' to set bit. Default Value: 0
11	MUX_FW_P3_VMINUS	Firmware control: 0=open, 1=close switch between pin P3 and vminus signal. Write with '1' to set bit. Default Value: 0
10	MUX_FW_P2_VMINUS	Firmware control: 0=open, 1=close switch between pin P2 and vminus signal. Write with '1' to set bit. Default Value: 0
9	MUX_FW_P1_VMINUS	Firmware control: 0=open, 1=close switch between pin P1 and vminus signal. Write with '1' to set bit. Default Value: 0
8	MUX_FW_P0_VMINUS	Firmware control: 0=open, 1=close switch between pin P0 and vminus signal. Write with '1' to set bit. Default Value: 0

27.1.31 SAR0_MUX_SWITCH0 (continued)

7	MUX_FW_P7_VPLUS	Firmware control: 0=open, 1=close switch between pin P7 and vplus signal. Write with '1' to set bit. Default Value: 0
6	MUX_FW_P6_VPLUS	Firmware control: 0=open, 1=close switch between pin P6 and vplus signal. Write with '1' to set bit. Default Value: 0
5	MUX_FW_P5_VPLUS	Firmware control: 0=open, 1=close switch between pin P5 and vplus signal. Write with '1' to set bit. Default Value: 0
4	MUX_FW_P4_VPLUS	Firmware control: 0=open, 1=close switch between pin P4 and vplus signal. Write with '1' to set bit. Default Value: 0
3	MUX_FW_P3_VPLUS	Firmware control: 0=open, 1=close switch between pin P3 and vplus signal. Write with '1' to set bit. Default Value: 0
2	MUX_FW_P2_VPLUS	Firmware control: 0=open, 1=close switch between pin P2 and vplus signal. Write with '1' to set bit. Default Value: 0
1	MUX_FW_P1_VPLUS	Firmware control: 0=open, 1=close switch between pin P1 and vplus signal. Write with '1' to set bit. Default Value: 0
0	MUX_FW_P0_VPLUS	Firmware control: 0=open, 1=close switch between pin P0 and vplus signal. Write with '1' to set bit. Default Value: 0

27.1.32 SAR0_MUX_SWITCH_CLEAR0

SARMUX Firmware switch control clear

Address: 0x409B0304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	MUX_FW_P7_VPLUS	MUX_FW_P6_VPLUS	MUX_FW_P5_VPLUS	MUX_FW_P4_VPLUS	MUX_FW_P3_VPLUS	MUX_FW_P2_VPLUS	MUX_FW_P1_VPLUS	MUX_FW_P0_VPLUS

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	MUX_FW_P7_VMINUS	MUX_FW_P6_VMINUS	MUX_FW_P5_VMINUS	MUX_FW_P4_VMINUS	MUX_FW_P3_VMINUS	MUX_FW_P2_VMINUS	MUX_FW_P1_VMINUS	MUX_FW_P0_VMINUS

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	MUX_FW_SARBUS1_VPLUS	MUX_FW_SARBUS0_VPLUS	MUX_FW_AMUXBUSB_VMINUS	MUX_FW_AMUXBUSA_VMINUS	MUX_FW_AMUXBUSB_VPLUS	MUX_FW_AMUXBUSA_VPLUS	MUX_FW_TEMP_VPLUS	MUX_FW_VSSA_VMINUS

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW1C	RW1C
HW Access	None						A	A
Name	None [31:26]						MUX_FW_SARBUS1_VMINUS	MUX_FW_SARBUS0_VMINUS

Bits	Name	Description
25	MUX_FW_SARBUS1_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
24	MUX_FW_SARBUS0_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
23	MUX_FW_SARBUS1_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
22	MUX_FW_SARBUS0_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0

27.1.32 SAR0_MUX_SWITCH_CLEAR0 (continued)

21	MUX_FW_AMUXBUS-B_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
20	MUX_FW_AMUX-BUSA_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
19	MUX_FW_AMUXBUS-B_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
18	MUX_FW_AMUX-BUSA_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
17	MUX_FW_TEMP_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
16	MUX_FW_VSSA_VMI-NUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
15	MUX_FW_P7_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
14	MUX_FW_P6_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
13	MUX_FW_P5_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
12	MUX_FW_P4_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
11	MUX_FW_P3_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
10	MUX_FW_P2_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
9	MUX_FW_P1_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
8	MUX_FW_P0_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
7	MUX_FW_P7_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
6	MUX_FW_P6_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
5	MUX_FW_P5_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
4	MUX_FW_P4_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
3	MUX_FW_P3_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
2	MUX_FW_P2_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
1	MUX_FW_P1_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
0	MUX_FW_P0_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0

27.1.33 SAR0_MUX_SWITCH_SQ_CTRL

SARMUX switch Sar Sequencer control

Address: 0x409B0344

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	MUX_SQ_CTRL_P7	MUX_SQ_CTRL_P6	MUX_SQ_CTRL_P5	MUX_SQ_CTRL_P4	MUX_SQ_CTRL_P3	MUX_SQ_CTRL_P2	MUX_SQ_CTRL_P1	MUX_SQ_CTRL_P0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	None		RW	RW	RW	RW
HW Access	R	R	None		R	R	R	R
Name	MUX_SQ_CTRL_SARBUS1	MUX_SQ_CTRL_SARBUS0	None [21:20]		MUX_SQ_CTRL_AMUXBUSB	MUX_SQ_CTRL_AMUXBUSA	MUX_SQ_CTRL_TEMP	MUX_SQ_CTRL_VSSA

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	MUX_SQ_CTRL_SARBUS1	for sarbus1 switch Default Value: 0
22	MUX_SQ_CTRL_SARBUS0	for sarbus0 switch Default Value: 0
19	MUX_SQ_CTRL_AMUXBUSB	for amuxbusb switches Default Value: 0
18	MUX_SQ_CTRL_AMUXBUSA	for amuxbusa switch Default Value: 0
17	MUX_SQ_CTRL_TEMP	for temp switch Default Value: 0
16	MUX_SQ_CTRL_VSSA	for vssa switch Default Value: 0

27.1.33 SAR0_MUX_SWITCH_SQ_CTRL (continued)

7	MUX_SQ_CTRL_P7	for P7 switches Default Value: 0
6	MUX_SQ_CTRL_P6	for P6 switches Default Value: 0
5	MUX_SQ_CTRL_P5	for P5 switches Default Value: 0
4	MUX_SQ_CTRL_P4	for P4 switches Default Value: 0
3	MUX_SQ_CTRL_P3	for P3 switches Default Value: 0
2	MUX_SQ_CTRL_P2	for P2 switches Default Value: 0
1	MUX_SQ_CTRL_P1	for P1 switches Default Value: 0
0	MUX_SQ_CTRL_P0	for P0 switches Default Value: 0

27.1.34 SAR0_MUX_SWITCH_STATUS

SARMUX switch status

Address: 0x409B0348

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	MUX_FW_P7_VPLUS	MUX_FW_P6_VPLUS	MUX_FW_P5_VPLUS	MUX_FW_P4_VPLUS	MUX_FW_P3_VPLUS	MUX_FW_P2_VPLUS	MUX_FW_P1_VPLUS	MUX_FW_P0_VPLUS

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	MUX_FW_P7_VMINUS	MUX_FW_P6_VMINUS	MUX_FW_P5_VMINUS	MUX_FW_P4_VMINUS	MUX_FW_P3_VMINUS	MUX_FW_P2_VMINUS	MUX_FW_P1_VMINUS	MUX_FW_P0_VMINUS

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	MUX_FW_SARBUS1_VPLUS	MUX_FW_SARBUS0_VPLUS	MUX_FW_AMUXBUSB_VMINUS	MUX_FW_AMUXBUSA_VMINUS	MUX_FW_AMUXBUSB_VPLUS	MUX_FW_AMUXBUSA_VPLUS	MUX_FW_TEMP_VPLUS	MUX_FW_VSSA_VMINUS

Bits	31	30	29	28	27	26	25	24
SW Access	None						R	R
HW Access	None						W	W
Name	None [31:26]						MUX_FW_SARBUS1_VMINUS	MUX_FW_SARBUS0_VMINUS

Bits	Name	Description
25	MUX_FW_SARBUS1_VMINUS	switch status of corresponding bit in MUX_SWITCH0. This field cannot be read if SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
24	MUX_FW_SARBUS0_VMINUS	switch status of corresponding bit in MUX_SWITCH0. This field cannot be read if SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
23	MUX_FW_SARBUS1_VPLUS	switch status of corresponding bit in MUX_SWITCH0. This field cannot be read if SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: 0

27.1.34 SAR0_MUX_SWITCH_STATUS (continued)

22	MUX_FW_SAR-BUS0_VPLUS	switch status of corresponding bit in MUX_SWITCH0. This field cannot be read if SAR_-CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
21	MUX_FW_AMUXBUS-B_VMINUS	switch status of corresponding bit in MUX_SWITCH0. This field cannot be read if SAR_-CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
20	MUX_FW_AMUX-BUSA_VMINUS	switch status of corresponding bit in MUX_SWITCH0. This field cannot be read if SAR_-CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
19	MUX_FW_AMUXBUS-B_VPLUS	switch status of corresponding bit in MUX_SWITCH0. This field cannot be read if SAR_-CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
18	MUX_FW_AMUX-BUSA_VPLUS	switch status of corresponding bit in MUX_SWITCH0. This field cannot be read if SAR_-CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
17	MUX_FW_TEMP_VPLUS	switch status of corresponding bit in MUX_SWITCH0. This field cannot be read if SAR_-CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
16	MUX_FW_VSSA_VMI-NUS	switch status of corresponding bit in MUX_SWITCH0. This field cannot be read if SAR_-CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
15	MUX_FW_P7_VMINUS	switch status of corresponding bit in MUX_SWITCH0. This field cannot be read if SAR_-CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
14	MUX_FW_P6_VMINUS	switch status of corresponding bit in MUX_SWITCH0. This field cannot be read if SAR_-CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
13	MUX_FW_P5_VMINUS	switch status of corresponding bit in MUX_SWITCH0. This field cannot be read if SAR_-CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
12	MUX_FW_P4_VMINUS	switch status of corresponding bit in MUX_SWITCH0. This field cannot be read if SAR_-CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
11	MUX_FW_P3_VMINUS	switch status of corresponding bit in MUX_SWITCH0. This field cannot be read if SAR_-CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
10	MUX_FW_P2_VMINUS	switch status of corresponding bit in MUX_SWITCH0. This field cannot be read if SAR_-CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
9	MUX_FW_P1_VMINUS	switch status of corresponding bit in MUX_SWITCH0. This field cannot be read if SAR_-CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
8	MUX_FW_P0_VMINUS	switch status of corresponding bit in MUX_SWITCH0. This field cannot be read if SAR_-CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
7	MUX_FW_P7_VPLUS	switch status of corresponding bit in MUX_SWITCH0. This field cannot be read if SAR_-CLOCK_SEL.CLOCK_SEL =1. Default Value: 0

27.1.34 SAR0_MUX_SWITCH_STATUS (continued)

6	MUX_FW_P6_VPLUS	switch status of corresponding bit in MUX_SWITCH0. This field cannot be read if SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
5	MUX_FW_P5_VPLUS	switch status of corresponding bit in MUX_SWITCH0. This field cannot be read if SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
4	MUX_FW_P4_VPLUS	switch status of corresponding bit in MUX_SWITCH0. This field cannot be read if SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
3	MUX_FW_P3_VPLUS	switch status of corresponding bit in MUX_SWITCH0. This field cannot be read if SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
2	MUX_FW_P2_VPLUS	switch status of corresponding bit in MUX_SWITCH0. This field cannot be read if SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
1	MUX_FW_P1_VPLUS	switch status of corresponding bit in MUX_SWITCH0. This field cannot be read if SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
0	MUX_FW_P0_VPLUS	switch status of corresponding bit in MUX_SWITCH0. This field cannot be read if SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: 0

28 FIFO Registers

This section discusses the FIFO Registers. It lists all the registers in mapping tables, in address order

28.1 Register Details

Register	Address	Description
PASS_FIFO0_CTRL	0x409F0300	FIFO control register
PASS_FIFO0_CONFIG	0x409F0304	FIFO configuration register
PASS_FIFO0_CLEAR	0x409F0308	FIFO clear register
PASS_FIFO0_LEVEL	0x409F030C	FIFO level register
PASS_FIFO0_USED	0x409F0310	FIFO used register
PASS_FIFO0_STATUS	0x409F0314	FIFO status register
PASS_FIFO0_RD_DATA	0x409F0318	FIFO read data register
PASS_FIFO0_INTR	0x409F0320	Interrupt register
PASS_FIFO0_INTR_SET	0x409F0324	Interrupt set register
PASS_FIFO0_INTR_MASK	0x409F0328	Interrupt mask register
PASS_FIFO0_INTR_MASKED	0x409F032C	Interrupt masked register
PASS_FIFO1_CTRL	0x409F0400	FIFO control register. See PASS_FIFO0_CTRL for the details of bit fields.
PASS_FIFO1_CONFIG	0x409F0404	FIFO configuration register. See PASS_FIFO0_CONFIG for the details of bit fields.
PASS_FIFO1_CLEAR	0x409F0408	FIFO clear register. See PASS_FIFO0_CLEAR for the details of bit fields.
PASS_FIFO1_LEVEL	0x409F040C	FIFO level register. See PASS_FIFO0_LEVEL for the details of bit fields.
PASS_FIFO1_USED	0x409F0410	FIFO used register. See PASS_FIFO0_USED for the details of bit fields.
PASS_FIFO1_STATUS	0x409F0414	FIFO status register. See PASS_FIFO0_STATUS for the details of bit fields.
PASS_FIFO1_RD_DATA	0x409F0418	FIFO read data register. See PASS_FIFO0_RD_DATA for the details of bit fields.
PASS_FIFO1_INTR	0x409F0420	Interrupt register. See PASS_FIFO0_INTR for the details of bit fields.
PASS_FIFO1_INTR_SET	0x409F0424	Interrupt set register. See PASS_FIFO0_INTR_SETfor the details of bit fields.
PASS_FIFO1_INTR_MASK	0x409F0428	Interrupt mask register. See PASS_FIFO0_INTR_MASK for the details of bit fields.
PASS_FIFO1_INTR_MASKED	0x409F042C	Interrupt masked register. See PASS_FIFO0_INTR_MASKED for the details of bit fields.

28.1.1 PASS_FIFO0_CTRL

FIFO control register

Address: 0x409F0300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	Enable for SAR FIFO functionality. If CONFIG.CHAIN_TO_NXT is set, the ENABLED bit of the NEXT FIFO is set when FIFO[0] is enabled. - 0: FIFO disabled - 1: FIFO enabled Default Value: 0

28.1.2 PASS_FIFO0_CONFIG

FIFO configuration register

Address: 0x409F0304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					TR_INTR_-CL-R_RD_EN	CHAIN_TO_NXT	CHAN_ID_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	TR_INTR_CLR_RD_EN	Enable for FIFO read clearing the FIFO level trigger and level interrupt. - 0: Disabled, FIFO level trigger and level interrupt generation follows LEVEL.LEVEL. - 1: Enabled, after initial FIFO level trigger and level interrupt generation, subsequent FIFO level triggers and level interrupts are blocked until at least FIFO.LEVEL+1 reads have occurred. If CHAIN_TO_NXT is enabled, only FIFO[0].CONFIG. TR_CLR_RD_EN should be configured. Default Value: 0
1	CHAIN_TO_NXT	Chain FIFO to next FIFO (i.e. chain FIFO0 and FIFO1). - 0: FIFO not chained . FIFO operates independently (FIFO depth of 64) and only operates on result data from its associated SAR. - 1: FIFO chained to next FIFO. FIFO is part of a chain of FIFOs (effectively extending the FIFO depth beyond 64) and only operates on result data from SAR0. Default Value: 0

28.1.2 PASS_FIFO0_CONFIG (continued)

0	CHAN_ID_EN	channel number (ID) enable bit -0: CHAN_ID field in RD_DATA is disabled. A read from RD_DATA will result in (4'b0,16'b RESULT) -1: CHAN_ID field in RD_DATA is enabled. A read from RD_DATA will result in (4'b CHAN_ID, 16'b RESULT) If CHAIN_EN is enabled, only FIFO[0].config.chan_id_en should be configured and the other FIFOs in the chain will inherit the FIFO[0] config. Default Value: 0

28.1.3 PASS_FIFO0_CLEAR

FIFO clear register

Address: 0x409F0308

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							CLEAR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CLEAR	When firmware writes a 1 here it will trigger and clearing of the FIFO status registers (excluding interrupts), hardware clears this bit. Default Value: 0

28.1.4 PASS_FIFO0_LEVEL

FIFO level register

Address: 0x409F030C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LEVEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	LEVEL	FIFO level set. A trigger (and optional interrupt) event occurs when USED.USED = LEVEL+1. (Trigger generation is also affect by CONFIG.TR_CLR_RD_EN). If CHAIN_TO_NXT is disabled, the Max LEVEL is limited to 63. If CHAIN_TO_NXT is enabled, only FIFO[0].config.level should be configured and the Max LEVEL is set by the number of FIFOs in the chain. Default Value: 0

28.1.5 PASS_FIFO0_USED

FIFO used register

Address: 0x409F0310

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	USED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	USED	Number of used/occupied entries in the FIFO. If CONFIG.CHAIN_EN is disabled, the field value is in the range [0, 64]. When "0", the FIFO is empty. When "64", the FIFO is full. If CONFIG.CHAIN_EN is enabled, only FIFO[0].USED.USED should be read to detemine the used status. Default Value: 0

28.1.6 PASS_FIFO0_STATUS

FIFO status register

Address: 0x409F0314

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RD_PTR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	WR_PTR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	WR_PTR	FIFO write pointer: FIFO location at which a new data is written by the hardware. Note: This functionality is intended for debugging purposes. If CONFIG.CHAIN_TO_NXT is enabled, only FIFO[0].STATUS.WR_PTR should be read to determine the write pointer location of the chained FIFO. Default Value: 0
7 : 0	RD_PTR	FIFO read pointer: FIFO location from which a data is read. Note: This functionality is intended for debugging purposes. If CONFIG.CHAIN_TO_NXT is enabled, only FIFO[0].STATUS.RD_PTR should be read to determine the read pointer location of the chained FIFO. Default Value: 0

28.1.7 PASS_FIFO0_RD_DATA

FIFO read data register

Address: 0x409F0318

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				CHAN_ID [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	CHAN_ID	Channel number for a given SAR result. Requires CTRL.CHAN_ID_EN to be set. If CONFIG.CHAIN_TO_NXT is enabled, only FIFO[0].RD_DATA.CHAN_ID should be read. Default Value: 0
15 : 0	RESULT	SAR result. Results from all enabled channels are stored in the buffer. If CONFIG.CHAIN_TO_NXT is enabled, only FIFO[0].RD_DATA.RESULT should be read. Default Value: 0

28.1.8 PASS_FIFO0_INTR

Interrupt register

Address: 0x409F0320

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [7:3]					FIFO_UNDERFLOW	FIFO_OVERFLOW	FIFO_LEVEL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	FIFO_UNDERFLOW	HW sets this field to '1', when reading from an empty FIFO. HW tracks underflow after FIFO is being written to and FIFO_CTRL.ENABLE==1. If CONFIG.CHAIN_TO_NXT is enabled, only FIFO[0].INTR.FIFO_UNDERFLOW is updated by hardware. Write with '1' to clear bit. Default Value: 0
1	FIFO_OVERFLOW	HW sets this field to '1', when writing to a full FIFO (FIFO_USED.USED is "64"). If CONFIG.CHAIN_TO_NXT is enabled, only FIFO[0].INTR.FIFO_OVERFLOW is updated by hardware. Write with '1' to clear bit. Default Value: 0
0	FIFO_LEVEL	HW sets this field to '1', when USED.USED >= LEVEL.LEVEL+1 If CONFIG.CHAIN_TO_NXT is enabled, only FIFO[0].INTR.FIFO_LEVEL is updated by hardware. Write with '1' to clear bit. Default Value: 0

28.1.9 PASS_FIFO0_INTR_SET

Interrupt set register

Address: 0x409F0324

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [7:3]					FIFO_UNDERFLOW	FIFO_OVERFLOW	FIFO_LEVEL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	FIFO_UNDERFLOW	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
1	FIFO_OVERFLOW	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0
0	FIFO_LEVEL	Write this field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0

28.1.10 PASS_FIFO0_INTR_MASK

Interrupt mask register

Address: 0x409F0328

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					FIFO_UNDERFLOW	FIFO_OVERFLOW	FIFO_LEVEL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	FIFO_UNDERFLOW	Mask for corresponding field in INTR register. If CONFIG.CHAIN_TO_NXT is enabled, only FIFO[0].INTR_MASK.FIFO_UNDERFLOW should be set. Default Value: 0
1	FIFO_OVERFLOW	Mask for corresponding field in INTR register. If CONFIG.CHAIN_TO_NXT is enabled, only FIFO[0].INTR_MASK.FIFO_OVERFLOW should be set. Default Value: 0
0	FIFO_LEVEL	Mask for corresponding field in INTR register. If CONFIG.CHAIN_TO_NXT is enabled, only FIFO[0].INTR_MASK.FIFO_LEVEL should be set. Default Value: 0

28.1.11 PASS_FIFO0_INTR_MASKED

Interrupt masked register

Address: 0x409F032C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [7:3]					FIFO_UNDERFLOW	FIFO_OVERFLOW	FIFO_LEVEL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	FIFO_UNDERFLOW	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
1	FIFO_OVERFLOW	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0
0	FIFO_LEVEL	Logical AND of corresponding INTR and INTR_MASK fields. Default Value: 0

29 Timer Registers

This section discusses the Timer Registers. It lists all the registers in mapping tables, in address order

29.1 Register Details

Register	Address	Description
PASS_TIMER_CTRL	0x409F0100	Timer trigger control register
PASS_TIMER_CONFIG	0x409F0104	Timer trigger configuration register
PASS_TIMER_PERIOD	0x409F0108	Timer trigger period register

29.1.1 PASS_TIMER_CTRL

Timer trigger control register

Address: 0x409F0100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	0=disabled, 1=enabled Upon enable, the timer will immediately generate a trigger pulse (lasting for one clock cycle of the selected CONFIG.CLOCK_SEL) and will generate subsequent trigger pulses (again lasting one clock cycle) whenever the timer reaches terminal count. If PERIOD.PER_VAL is set to 0, the timer trigger output will remain high as long as the timer is enabled. Default Value: 0

29.1.2 PASS_TIMER_CONFIG

Timer trigger configuration register

Address: 0x409F0104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						CLOCK_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	CLOCK_SEL	Select Clock source of the Timer Default Value: 0 **0x0: CLK_PERI :** Timer clocked from CLK_PERI **0x1: CLK_DPSLP :** Timer clocked from CLK_DPSLP **0x2: CLK_LF :** Timer clocked from CLK_LF **0x3: TBD :**

29.1.3 PASS_TIMER_PERIOD

Timer trigger period register

Address: 0x409F0108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PER_VAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PER_VAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PER_VAL	Actual timer period is PER_VAL+1 (1 to 65536). Only non-zero PER_VAL are supported. (i.e. PER_VAL=0 is considered invalid). Default Value: 0

30 Low Power Oscillator Registers

This section discusses the Low Power Oscillator Registers (LPOSC). It lists all the registers in mapping tables, in address order

30.1 Register Details

Register	Address	Description
PASS_LPOSC_CTRL	0x409F0200	Low Power Oscillator control
PASS_LPOSC_CONFIG	0x409F0204	Low Power Oscillator configuration register

30.1.1 PASS_LPOSC_CTRL

Low Power Oscillator control

Address: 0x409F0200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	Master enable for LPOSC oscillator. This bit must be high at all times for all functions to work properly. Hardware will automatically disable the LPOSC during System Deep Sleep (unless DEEPSLEEP_MODE is set) Default Value: 1

30.1.2 PASS_LPOSC_CONFIG

Low Power Oscillator configuration register

Address: 0x409F0204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							DEEPS-LEEP_-MODE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	DEEPSLEEP_MODE	LPOSC functionality while in System Deep Sleep Default Value: 0 **0x0: DUTY CYCLED :** LPOSC enabled by TIMER trigger **0x1: ALWAYS_ON :** LPOSC always ON in System Deep Sleep

31 Programmable Analog Subsystem Registers

This section discusses the Programmable Analog Subsystem (PASS) Registers. It lists all the registers in mapping tables, in address order

31.1 Register Details

Register	Address	Description
PASS_INTR_CAUSE	0x409F0000	Interrupt cause register
PASS_DPSLP_CLOCK_SEL	0x409F0010	Deepsleep clock select
PASS_ANA_PWR_CFG	0x409F0014	Analog power configuration
PASS_CTBM_CLOCK_SEL	0x409F0020	Clock select for CTBm
PASS_SAR_DPSLP_CTRL0	0x409F0030	Deepsleep control for SARv3
PASS_SAR_DPSLP_CTRL1	0x409F0034	Deepsleep control for SARv3. See PASS_SAR_DPSLP_CTRL0 for the details of bit fields.
PASS_SAR_CLOCK_SEL0	0x409F0040	Clock select for SARv3
PASS_SAR_CLOCK_SEL1	0x409F0044	Clock select for SARv3. See PASS_SAR_CLOCK_SEL0 for the details of bit fields.
PASS_SAR_TR_SCAN_CNT_STATUS0	0x409F0050	SAR trigger scan control status
PASS_SAR_TR_SCAN_CNT_STATUS1	0x409F0054	SAR trigger scan control status. See PASS_SAR_TR_SCAN_CNT_STATUS0 for the details of bit fields.
PASS_SAR_TR_SCAN_CNT	0x409F0060	SAR trigger scan control
PASS_SAR_OVR_CTRL	0x409F0064	SAR HW trigger override
PASS_SAR_SIMULT_CTRL	0x409F0068	SAR simultaneous trigger control
PASS_SAR_SIMULT_FW_START_CTRL	0x409F006C	SAR simultaneous start control
PASS_SAR_TR_OUT_CTRL	0x409F0070	SAR trigger out control
PASS_VREF_TRIM0	0x409F0F00	VREF Trim bits
PASS_VREF_TRIM1	0x409F0F04	VREF Trim bits
PASS_VREF_TRIM2	0x409F0F08	VREF Trim bits
PASS_VREF_TRIM3	0x409F0F0C	VREF Trim bits
PASS_IZTAT_TRIM0	0x409F0F10	VREF Trim bits
PASS_IZTAT_TRIM1	0x409F0F14	IZTAT Trim bits
PASS_IPTAT_TRIM0	0x409F0F18	IPTAT Trim bits
PASS_ICTAT_TRIM0	0x409F0F1C	ICTAT Trim bits

31.1.1 PASS_INTR_CAUSE

Interrupt cause register

Address: 0x409F0000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	None			R
HW Access	None			W	None			W
Name	None [7:5]			CT-DAC0_INT	None [3:1]			CTB0_INT

Bits	15	14	13	12	11	10	9	8
SW Access	None		R	R	None		R	R
HW Access	None		W	W	None		W	W
Name	None [15:14]		FIFO1_INT	FIFO0_INT	None [11:10]		SAR1_INT	SAR0_INT

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13	FIFO1_INT	FIFO1 interrupt pending Default Value: 0
12	FIFO0_INT	FIFO0 interrupt pending Default Value: 0
9	SAR1_INT	SAR1 interrupt pending Default Value: 0
8	SAR0_INT	SAR0 interrupt pending Default Value: 0
4	CTDAC0_INT	CTDAC0 interrupt pending Default Value: 0
0	CTB0_INT	CTB0 interrupt pending Default Value: 0

31.1.2 PASS_DPSLP_CLOCK_SEL

Deepsleep clock select

Address: 0x409F0010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None			RW
HW Access	None	R			None			R
Name	None	DPSLP_CLOCK_DIV [6:4]			None [3:1]			DPSLP_-CLOCK_-SEL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 4	DPSLP_CLOCK_DIV	CLK_DPSLP divider Default Value: 2 **0x0: NO_DIV :** Transparent mode, feed through selected clock source w/o dividing. **0x1: DIV_BY_2 :** Divide selected clock source by 2 **0x2: DIV_BY_4 :** Divide selected clock source by 4

31.1.2 PASS_DPSLP_CLOCK_SEL (continued)

		0x3: DIV_BY_8 : Divide selected clock source by 8 **0x4: DIV_BY_16 :** Divide selected clock source by 16 **0x5: RESERVED_0 :** Reserved **0x6: RESERVED_1 :** Reserved **0x7: RESERVED_2 :** Reserved
0	DPSLP_CLOCK_SEL	Select source for PASS DPSLP Clock Default Value: 0 **0x0: CLK_LPOSC :** CLK_DPSLP is set to CLK_LPOSC **0x1: CLK_MF :** CLK_DPSLP is set to CLK_MF

31.1.3 PASS_ANA_PWR_CFG

Analog power configuration

Address: 0x409F0014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PWR_UP_DELAY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				DUTY_CYCLE_SAR_ACT_EN [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 8	DUTY_CYCLE_SAR_ACT_EN	Enable duty cycling the SAR resulting in power reduction. This feature works irrespective of the device power mode. To use this feature, the SAR must be configured for deepsleep clocking (SAR_CLOCK_SEL.CLOCK_SEL must be set to CLK_DPSLP), and the SAR must use Timer-based hardware triggering (either by following the guidlines in SAR_OVR_CTRL.HW_TR_TIMER_SEL or SAR_SIMULT_CTRL.SIMULT_HW_TIMER_SEL). Non-timer based hardware triggers cannot be used nor can the firmware based triggers (FW,Continuous). Furthermore, trigger collision functionality will be limited to interrupt generation only. -0: Legacy (SAR not duty cycled) -1: SAR duty cycled <0>: Duty Cycle enable for SAR0 <1>: Duty Cycle enable for SAR1 (if available) <2>: Duty Cycle enable for SAR2 (if available) <3>: Duty Cycle enable for SAR3 (if available) Default Value: 0
7 : 0	PWR_UP_DELAY	Power up time for analog blocks. Fastest power up time is achieved with a setting of 0. Additional time can be added to allow for analog settling. The power up time is in CLK_DPSLP cycles. This field is only applicable when CLK_DPSLP is selected using SAR_CLOCK_SEL register. Default Value: 0

31.1.4 PASS_CTBM_CLOCK_SEL

Clock select for CTBm

Address: 0x409F0020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							PUMP_-CLOCK_-SEL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	PUMP_CLOCK_SEL	Select source for CTBm Pump Clock. Default Value: 0 **0x0: LEGACY :** CTBm pump clock set by AREF.CTRL.CLOCK_PUMP_PERI_SEL (Legacy). When configured for legacy operation, the CTBm deeplseep functionality is determined solely by the CTRL.DEEPSLEEP_ON bit. **0x1: CLK_DPSLP :** CTBm pump clock sourced from CLK_DPSLP When configured for CLK_DPSLP operation, the CTBm deepsleep functionality is determined by the CTRL.DEEPSLEEP_ON bit AND SAR(s) operation (i.e. CTBm is duty cycled with the SAR(s)). In this mode, the CTBm should only be used as a buffer/gain stage for the SAR(s).

31.1.5 PASS_SAR_DPSLP_CTRL0

Deepsleep control for SARv3

Address: 0x409F0030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	enable for SAR deepsleep operation. SAR_CLOCK_SEL.CLOCK_SEL must be set to 1 for this field to affect SAR operation. - 0: SAR deeepsleep operation disabled - 1: SAR deepsleep operation enabled. Default Value: 0

31.1.6 PASS_SAR_CLOCK_SEL0

Clock select for SARv3

Address: 0x409F0040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW	None					
HW Access	None	R	None					
Name	None	CLOCK_-SEL	None [29:24]					

Bits	Name	Description
30	CLOCK_SEL	SAR clock select Default Value: 0 **0x0: LEGACY :** - 0: legacy: SAR clock source is CLK_PERI (SAR is only operational in chip ACTIVE mode) **0x1: CLK_DPSLP :** - 1: SAR clock source is CLK_DPSLP (SAR can be operational in both chip ACTIVE and DEEP-SLEEP modes)

31.1.7 PASS_SAR_TR_SCAN_CNT_STATUS0

SAR trigger scan control status

Address: 0x409F0050

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SCAN_CNT_STATUS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	SCAN_CNT_STATUS	A read from this register returns the current sample count (possible values are 1 through SCAN_TR_SCAN_CNT.SCAN_CNT+1). This field cannot be read if SAR_CLOCK_-SEL.CLOCK_SEL =1. Default Value: 0

31.1.8 PASS_SAR_TR_SCAN_CNT

SAR trigger scan control

Address: 0x409F0060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SCAN_CNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	SCAN_CNT	SAR trigger sample counter. This field determines the number of samples a SAR will take when triggered. The number of samples is SCAN_COUNT+1. This feature can be enabled for individual SARs by setting the appropriate bit of SAR_TR_CTRL.TR_SCAN_CNT_SEL. This feature can be enabled for simultaneously sampled SARs by setting SAR_SIMULT_TR_CTRL.SIMULT_TR_SCAN_CNT_SEL. If SAR.SAMPLE_CTRL.AVG_MODE is set to INTERLEAVED, the SCAN_CNT must be set an integer multiple of (1<_CNTR+1). Default Value: 0

31.1.9 PASS_SAR_OVR_CTRL

SAR HW trigger override

Address: 0x409F0064

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	TR_SCAN_CNT_SEL [7:4]				HW_TR_TIMER_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				EOS_INTR_SCAN_CNT_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 8	EOS_INTR_SCAN_CNT_-SEL	SAR EOS interrupt source select (one bit per SAR). This feature is not available for FW or Continuous triggering. -0: Legacy (SAR EOS is the source of the SAR EOS interrupt) -1: Enabled, SAR EOS interrupt only occurs for the EOS when sample=SAR_TR_S-CAN_CNT.SCAN_CNT. <0>: EOS interrupt sample count select for SAR0 <1>: EOS interrupt sample count select for SAR1 <2>: EOS interrupt sample count select for SAR2 <3>: EOS interrupt sample count select for SAR3 Default Value: 0

31.1.9 PASS_SAR_OVR_CTRL (continued)

7 : 4	TR_SCAN_CNT_SEL	SAR trigger sample select (one bit per SAR). -0: Disabled -1: Enabled, SAR takes SAR_TR_SCAN_CNT per trigger (valid for both Firmware and Edge Senstive Hardware triggering, but ignored for Level Sensitive Hardware triggering and CONTINUOUS triggering). This feature cannot be enabled if the SAR is configured for Non-Tailgating Injection (SAR.INJ_CHAN_CONFIG.INJ_TAILGATING=0 while SAR.INJ_CHAN_CONFIG.INJ_START_EN=1) <0>: trigger sample select for SAR0 <1>: trigger sample select for SAR1 <2>: trigger sample select for SAR2 <3>: trigger sample select for SAR3 Default Value: 0
3 : 0	HW_TR_TIMER_SEL	SAR hardware trigger source select (one bit per SAR). SAR must be configured for hardware triggering (SAR.SAMPLE_CTRL.DSI_TRIGGER_EN must be set to 1). -0: Legacy (tr_sar_in_) -1: Timer trigger <0>: HW Trigger source for SAR0 <1>: HW Trigger source for SAR1 <2>: HW Trigger source for SAR2 <3>: HW Trigger source for SAR3 Default Value: 0

31.1.10 PASS_SAR_SIMULT_CTRL

SAR simultaneous trigger control

Address: 0x409F0068

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW			
HW Access	None		R		R			
Name	None [7:6]		SIMULT_HW_TR_SRC [5:4]		SIMULT_HW_TR_EN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							SIMULT_HW_TR_TIMER_SEL

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW	RW	RW	RW	None	
HW Access	None		R	R	R	R	None	
Name	None [23:22]		SIMULT_EOS_INTR_SCAN_CNT_SEL	SIMULT_TR_SCAN_CNT_SEL	SIMULT_HW_SYNC_TR	SIMULT_HW_TR_LEVEL	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	SIMULT_EOS_INTR_SCAN_CNT_SEL	Simultaneous SAR EOS interrupt source select. This feature is not available for FW or Continuous triggering. -0: Legacy (SAR EOS is the source of the SAR EOS interrupt) -1: Enabled, SAR EOS interrupt only occurs for the EOS when sample=SAR_TR_SCAN_CNT.SCAN_CNT. Default Value: 0

31.1.10 PASS_SAR_SIMULT_CTRL (continued)

20	SIMULT_TR_S-CAN_CNT_SEL	Simultaneous trigger sample select -0: Disabled -1: Enabled, SAR takes SAR_TR_SCAN_CNT per trigger (valid for both Firmware and Edge Senstive Hardware triggering, but ignored for Level Sensitive Hardware triggering and CONTIN-UOUS triggering) This feature cannot be enabled if either SAR is configured for Non-Tailgating Injection (SAR.INJ_CHAN_CONFIG.INJ_TAILGATING=0 while SAR.INJ_CHAN_CONFIG.IN-J_START_EN=1) Default Value: 0
19	SIMULT_HW_SYNC_TR	- 0: bypass clock domain synchronization of the Simult trigger signal. - 1: synchronize the Simult trigger signal to the SAR clock domain, if needed an edge detect is done in the peripheral clock domain. Default Value: 1
18	SIMULT_HW_TR_LEVEL	- 0: trigger signal is a pulse input, a positive edge detected on the trigger signal triggers a new scan. - 1: trigger signal is a level input, as long as the trigger signal remains high the SAR will do continuous scans. This field cannot be set when SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: 0
8	SIMULT_HW_TR_TIM-ER_SEL	SAR hardware trigger source select -0: SIMULT_HW_TR_SRC -1: Timer trigger Default Value: 0
5 : 4	SIMULT_HW_TR_SRC	Source for Simult Hardware trigger Default Value: 0 **0x0: SAR_TR_IN_0 :** SAR 0 HW Trigger Input **0x1: SAR_TR_IN_1 :** SAR 1 HW Trigger Input **0x2: SAR_TR_IN_2 :** SAR 2 HW Trigger Input **0x3: SAR_TR_IN_3 :** SAR 3 HW Trigger Input
3 : 0	SIMULT_HW_TR_EN	SAR simultaneous hardware triggering enable (one bit per SAR) -0: disabled -1: SAR trigger override enabled (SAR trigger set by SAR_OVR_CTRL register) <0>: Simultaneuous sampling enable for SAR0 <1>: Simultaneuous sampling enable for SAR1 <2>: Simultaneuous sampling enable for SAR2 <3>: Simultaneuous sampling enable for SAR3 Simultaneous sampling requires at least two bits in this field to be set. If less than two bits are set, this register will not affect SAR operation. Default Value: 0

31.1.11 PASS_SAR_SIMULT_FW_START_CTRL

SAR simultaneous start control

Address: 0x409F006C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S			
HW Access	None				RW1C			
Name	None [7:4]				FW_TRIGGER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				CONTINUOUS [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	CONTINUOUS	This field is used to configure two or more SARs for continuous operation. -0: Continuous mode disabled -1: Continuously scan enabled channels, ignore triggers. <0>: Continuous Mode for SAR0 <1>: Continuous Mode for SAR1 <2>: Continuous Mode for SAR2 <3>: Continuous Mode for SAR3 If less than two bits are set, this field has no effect. This field cannot be set when SAR_CLOCK_-SEL.CLOCK_SEL =1. Default Value: 0

31.1.11 PASS_SAR_SIMULT_FW_START_CTRL (continued)

3 : 0	FW_TRIGGER	This field is used to simultaneously FW trigger two or more SARs. <0>: Firmware trigger for SAR0 <1>: Firmware trigger for SAR1 <2>: Firmware trigger for SAR2 <3>: Firmware trigger for SAR3 If less than two bits are set, this field has no effect. When firmware writes to this field it will trigger the next scan of enabled channels, hardware clears this bit when the scan started with this trigger is completed. If scanning continuously the trigger is ignored and hardware clears this bit after the next scan is done. This bit is also cleared when the SAR is disabled. This field cannot be set when SAR_CLOCK_SEL.CLOCK_SEL =1. Default Value: 0

31.1.12 PASS_SAR_TR_OUT_CTRL

SAR trigger out control

Address: 0x409F0070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				SAR3_TR_OUT_SEL	SAR2_TR_OUT_SEL	SAR1_TR_OUT_SEL	SAR0_TR_OUT_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	SAR3_TR_OUT_SEL	SAR3 Trigger Out Source Select Default Value: 0 **0x0: LEGACY :** sar output trigger is set by SAR.SAMPLE_CTRL.EOS_DSI_OUT_EN condition **0x1: BUFFER_TRIGGER_LEVEL :** sar output trigger is set by FIFO.CTRL.FIFO_LEVEL condition
2	SAR2_TR_OUT_SEL	SAR2 Trigger Out Source Select Default Value: 0 **0x0: LEGACY :** sar output trigger is set by SAR.SAMPLE_CTRL.EOS_DSI_OUT_EN condition

31.1.12 PASS_SAR_TR_OUT_CTRL (continued)

		0x1: BUFFER_TRIGGER_LEVEL : sar output trigger is set by FIFO.CTRL.FIFO_LEVEL condition
1	SAR1_TR_OUT_SEL	SAR1 Trigger Out Source Select Default Value: 0 **0x0: LEGACY :** sar output trigger is set by SAR.SAMPLE_CTRL.EOS_DSI_OUT_EN condition **0x1: BUFFER_TRIGGER_LEVEL :** sar output trigger is set by FIFO.CTRL.FIFO_LEVEL condition
0	SAR0_TR_OUT_SEL	SAR0 Trigger Out Source Select Default Value: 0 **0x0: LEGACY :** sar output trigger is set by SAR.SAMPLE_CTRL.EOS_DSI_OUT_EN condition **0x1: BUFFER_TRIGGER_LEVEL :** sar output trigger is set by FIFO.CTRL.FIFO_LEVEL condition

31.1.13 PASS_VREF_TRIM0

VREF Trim bits

Address: 0x409F0F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VREF_ABS_TRIM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	VREF_ABS_TRIM	bandgap absolute voltage output trim (in signed magnitude format) 0x00 : No Voltage Trim Adjustment 0x1F : Maximum Positive Trim Adjustment (+20mV) 0x3F : Maximum Negative Trim Adjustment (-20mV) Bits [7:6] are reserved. Default Value: 0

31.1.14 PASS_VREF_TRIM1

VREF Trim bits

Address: 0x409F0F04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VREF_TEMPCO_TRIM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	VREF_TEMPCO_TRIM	bandgap voltage temperature correction trim 0x00 : Minimum temperature correction (smallest PTAT voltage) 0x3F : Maximum temperature correction (largest PTAT voltage) Bits [7:6] are reserved. Default Value: 0

31.1.15 PASS_VREF_TRIM2

VREF Trim bits

Address: 0x409F0F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VREF_CURV_TRIM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	VREF_CURV_TRIM	bandgap voltage curvature correction trim 0x00 : No Curvature Correction 0x1F : Maximum Curvature Correction (2uA PTAT2 Current (at 125C)) Bits [7:5] are reserved. Default Value: 0

31.1.16 PASS_VREF_TRIM3

VREF Trim bits

Address: 0x409F0F0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				VREF_ATTEN_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	VREF_ATTEN_TRIM	Obsolete Default Value: 0

31.1.17 PASS_IZTAT_TRIM0

VREF Trim bits

Address: 0x409F0F10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	IZTAT_ABS_TRIM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	IZTAT_ABS_TRIM	IZTAT absolute current output trim 0x00 : Minimum IZTAT output current (~500nA) 0x3F : Maximum IZTAT output current (~1.5uA) Bits [7:6] are reserved. Default Value: 0

31.1.18 PASS_IZTAT_TRIM1

IZTAT Trim bits

Address: 0x409F0F14

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	IZTAT_TC_TRIM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	IZTAT_TC_TRIM	IZTAT temperature correction trim (RMB) 0x00 : No IZTAT temperature correction 0xFF : Maximum IZTAT temperature correction As this is a Risk Mitigation Register, it should be loaded with 0x08. Default Value: 0

31.1.19 PASS_IPTAT_TRIM0

IPTAT Trim bits

Address: 0x409F0F18

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	IPTAT_CTBM_TRIM [7:4]				IPTAT_CORE_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	IPTAT_CTBM_TRIM	CTMB PTAT Current Trim 0x0 : Minimum CTMB IPTAT Current (~875nA) 0xF : Maximum CTMB IPTAT Current (~1.1uA) Default Value: 0
3 : 0	IPTAT_CORE_TRIM	IPTAT trim 0x0 : Minimum IPTAT current (~150nA at room) 0xF : Maximum IPTAT current (~350nA at room) Default Value: 0

31.1.20 PASS_ICTAT_TRIM0

ICTAT Trim bits

Address: 0x409F0F1C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				ICTAT_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	ICTAT_TRIM	ICTAT trim 0x00 : Minimum ICTAT current (~150nA at room) 0x0F : Maximum ICTAT current (~350nA at room) Default Value: 0

Section J: System Registers

See the following documentation available at Arm® website for the details of Cortex®- M4 and Cortex®-M0+ system registers.

- Cortex®-M4 Technical Reference Manual
- Cortex®-M0+ Technical Reference Manual

Revision History

Revision History

Document Title: PSoC 6 MCU: CY8C61x4, CY8C62x4 Registers Technical Reference Manual (TRM) PSoC 61, PSoC 62 MCU Document Number: 002-30426			
Revision	**ECN#**	**Issue Date**	**Description of Change**
**	6887706	05/28/2020	Specification for new silicon.
*A	6924038	07/21/2020	Updated CPUSS, CRYPTO, FLASH, PROT, LPCOMP, GPIO, EFUSE, SRSS, SCB and USB chapters.
*B	7170156	06/25/2021	Updated all the registers.