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PSoC® 3 Registers TRM
(Technical Reference Manual)

Document No. 001-50581 Rev. *K

March 25, 2020

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709
www.cypress.com

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1.3.1361 FLSHID_CUST_TABLES_DAC0_M3 1668
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1.3.1365 FLSHID_CUST_TABLES_DAC0_M7 1672
1.3.1366 FLSHID_CUST_TABLES_DAC0_M8 1673
1.3.1367 FLSHID_CUST_TABLES_DAC2_M1 1674
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1.3.1371 FLSHID_CUST_TABLES_DAC2_M5 1678
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1.3.1377 FLSHID_CUST_TABLES_DAC1_M3 1684
1.3.1378 FLSHID_CUST_TABLES_DAC1_M4 1685
1.3.1379 FLSHID_CUST_TABLES_DAC1_M5 1686
1.3.1380 FLSHID_CUST_TABLES_DAC1_M6 1687
1.3.1381 FLSHID_CUST_TABLES_DAC1_M7 1688
1.3.1382 FLSHID_CUST_TABLES_DAC1_M8 1689
1.3.1383 FLSHID_CUST_TABLES_DAC3_M1 1690
1.3.1384 FLSHID_CUST_TABLES_DAC3_M2 1691
1.3.1385 FLSHID_CUST_TABLES_DAC3_M3 1692
1.3.1386 FLSHID_CUST_TABLES_DAC3_M4 1693
1.3.1387 FLSHID_CUST_TABLES_DAC3_M5 1694
1.3.1388 FLSHID_CUST_TABLES_DAC3_M6 1695
1.3.1389 FLSHID_CUST_TABLES_DAC3_M7 1696
1.3.1390 FLSHID_CUST_TABLES_DAC3_M8 1697
1.3.1391 FLSHID_MFG_CFG_IMO_TR1 1698
1.3.1392 FLS_DATA[0..65535] 1699
1.3.1393 EXTMEM_DATA[0..8388607] 1700

Revision History **1701**

Register Mapping

Register Mapping discusses the registers of the PSoC 3 device. It lists all the registers in mapping tables, in address order.

See the *PSoC 3, PSoC 5 Architecture TRM (Technical Reference Manual)*, 001-50235, for complete functionality.

1.1 Maneuvering Around the Registers

For ease-of-use, this chapter is formatted so that there is one register per page, although some registers use two pages. On each page, from top to bottom, there are four sections:

1. Register name and address (from lowest to highest).
2. Register table showing the bit organization, with reserved bits grayed out.
3. Written description of register specifics or links to additional register information.
4. Detailed register bit descriptions.

1.2 Register Conventions

The following table lists the register conventions.

Convention	Example	Description
'x' in a register name	ACBxxCR1	Multiple instances/address ranges of the same register
R	R : 00	Read register or bit(s)
W	W : 00	Write register or bit(s)
WOC	WOC:0	Write one to clear
WZC	WZC:0	Write zero to clear
RC	RC:0	Read to clear
WC	WC:0	Write to clear
NA	NA:000	Reserved
U	R:U	Undefined
00	RW : 00	Reset value is 0x00
XX	RW : XX	Register is not reset
Empty, grayed out table cell		Reserved bit or group of bits, unless otherwise stated. Write reserved bits to zero. Software cannot make any assumptions about return values.

1.3 PSoC 3 Register Map

The PSoC 3 device has a total register address space of 64 kbytes.

Register Name	Purpose	Address
SRAM_MAP_SYSMEM0_DATA[0..1023]	System Memory - CPU Region	[0..1023 * 0x4]
SRAM_MAP_SYSMEM1_DATA[0..1023]	System Memory - PHUB Region	0x1000 + [0..1023 * 0x4]
SRAM_MAP_TRACEMEM_DATA[0..1023]	Trace Memory	0x2000 + [0..1023 * 0x4]
CLKDIST_CR	Configuration Register CR	0x4000
CLKDIST_LD	LOAD Register	0x4001
CLKDIST_WRK0	LSB Shadow Divider Value Register	0x4002
CLKDIST_WRK1	MSB Shadow Divider Value Register	0x4003
CLKDIST_MSTR0	Master clock (clk_sync_d) Divider Value Register	0x4004
CLKDIST_MSTR1	Master (clk_sync_d) Configuration Register/CPU Divider Value	0x4005
CLKDIST_BCFG0	CLK_BUS LSB Divider Value Register	0x4006
CLKDIST_BCFG1	CLK_BUS MSB Divider Value Register	0x4007
CLKDIST_BCFG2	CLK_BUS Configuration Register	0x4008
CLKDIST_UCFG	USB Configuration Register	0x4009
CLKDIST_DLY0	Delay block Configuration Register	0x400a
CLKDIST_DLY1	Delay block Configuration Register	0x400b
CLKDIST_DMASK	Digital Clock Mask Register	0x4010
CLKDIST_AMASK	Analog Clock Mask Register	0x4014
CLKDIST_DCFG[0..7]_CFG0	LSB Divider Value Register	0x4080 + [0..7 * 0x4]
CLKDIST_DCFG[0..7]_CFG1	MSB Divider Value Register	0x4080 + [0..7 * 0x4] + 0x1
CLKDIST_DCFG[0..7]_CFG2	Configuration Register	0x4080 + [0..7 * 0x4] + 0x2
CLKDIST_ACFG[0..3]_CFG0	LSB Divider Value Register	0x4100 + [0..3 * 0x4]
CLKDIST_ACFG[0..3]_CFG1	MSB Divider Value Register	0x4100 + [0..3 * 0x4] + 0x1
CLKDIST_ACFG[0..3]_CFG2	Configuration Register	0x4100 + [0..3 * 0x4] + 0x2
CLKDIST_ACFG[0..3]_CFG3	Analog clocks Configuration Register	0x4100 + [0..3 * 0x4] + 0x3
FASTCLK_IMO_CR	Internal Main Oscillator Control Register	0x4200
FASTCLK_XMHZ_CSR	External 4-25 MHz Crystal Oscillator Status and Control Register	0x4210
FASTCLK_XMHZ_CFG0	External 4-25 MHz Crystal Oscillator Configuration Register 0	0x4212
FASTCLK_XMHZ_CFG1	External 4-25 MHz Crystal Oscillator Configuration Register 1	0x4213
FASTCLK_PLL_CFG0	PLL Configuration Register	0x4220
FASTCLK_PLL_CFG1	PLL Control Register	0x4221
FASTCLK_PLL_P	PLL P-Counter Configuration Register	0x4222
FASTCLK_PLL_Q	PLL Q-Counter Configuration Register	0x4223
FASTCLK_PLL_SR	PLL Status Register	0x4225
SLOWCLK_ILO_CR0	Internal Low-speed Oscillator Control Register 0	0x4300

Register Name	Purpose	Address
SLOWCLK_ILO_CR1	Internal Low-speed Oscillator Control Register 1	0x4301
SLOWCLK_X32_CR	External 32kHz Crystal Oscillator Control Register	0x4308
BOOST_CR0	Boost Control 0	0x4320
BOOST_CR1	Boost Control 1	0x4321
BOOST_CR2	Boost Control 2	0x4322
BOOST_CR3	Boost Control 3	0x4323
BOOST_SR	Boost Status	0x4324
BOOST_CR4	Boost Control Register 4	0x4325
BOOST_SR2	Boost Status Register 2	0x4326
PWRSYS_CR0	Power System Control Register 0	0x4330
PWRSYS_CR1	Power System Control Register 1	0x4331
PM_TW_CFG0	Timewheel Configuration Register 0	0x4380
PM_TW_CFG1	Timewheel Configuration Register 1	0x4381
PM_TW_CFG2	Timewheel Configuration Register 2	0x4382
PM_WDT_CFG	Watchdog Timer Configuration Register	0x4383
PM_WDT_CR	Watchdog Timer Control Register	0x4384
PM_INT_SR	Power Manager Interrupt Status Register	0x4390
PM_MODE_CFG0	Power Mode Configuration Register 0	0x4391
PM_MODE_CFG1	Power Mode Configuration Register 1	0x4392
PM_MODE_CSR	Power Mode Control/Status Register	0x4393
PM_USB_CR0	USB Power Mode Control Register 0	0x4394
PM_WAKEUP_CFG0	Power Mode Wakeup Mask Configuration Register 0	0x4398
PM_WAKEUP_CFG1	Power Mode Wakeup Mask Configuration Register 1	0x4399
PM_WAKEUP_CFG2	Power Mode Wakeup Mask Configuration Register 2	0x439a
PM_ACT_CFG0	Active Power Mode Configuration Register 0	0x43a0
PM_ACT_CFG1	Active Power Mode Configuration Register 1	0x43a1
PM_ACT_CFG2	Active Power Mode Configuration Register 2	0x43a2
PM_ACT_CFG3	Active Power Mode Configuration Register 3	0x43a3
PM_ACT_CFG4	Active Power Mode Configuration Register 4	0x43a4
PM_ACT_CFG5	Active Power Mode Configuration Register 5	0x43a5
PM_ACT_CFG6	Active Power Mode Configuration Register 6	0x43a6
PM_ACT_CFG7	Active Power Mode Configuration Register 7	0x43a7
PM_ACT_CFG8	Active Power Mode Configuration Register 8	0x43a8
PM_ACT_CFG9	Active Power Mode Configuration Register 9	0x43a9
PM_ACT_CFG10	Active Power Mode Configuration Register 10	0x43aa
PM_ACT_CFG11	Active Power Mode Configuration Register 11	0x43ab

Register Name	Purpose	Address
PM_ACT_CFG12	Active Power Mode Configuration Register 12	0x43ac
PM_ACT_CFG13	Active Power Mode Configuration Register 13	0x43ad
PM_STBY_CFG0	Standby Power Mode Configuration Register 0	0x43b0
PM_STBY_CFG1	Standby Power Mode Configuration Register 1	0x43b1
PM_STBY_CFG2	Standby Power Mode Configuration Register 2	0x43b2
PM_STBY_CFG3	Standby Power Mode Configuration Register 3	0x43b3
PM_STBY_CFG4	Standby Power Mode Configuration Register 4	0x43b4
PM_STBY_CFG5	Standby Power Mode Configuration Register 5	0x43b5
PM_STBY_CFG6	Standby Power Mode Configuration Register 6	0x43b6
PM_STBY_CFG7	Standby Power Mode Configuration Register 7	0x43b7
PM_STBY_CFG8	Standby Power Mode Configuration Register 8	0x43b8
PM_STBY_CFG9	Standby Power Mode Configuration Register 9	0x43b9
PM_STBY_CFG10	Standby Power Mode Configuration Register 10	0x43ba
PM_STBY_CFG11	Standby Power Mode Configuration Register 11	0x43bb
PM_STBY_CFG12	Standby Power Mode Configuration Register 12	0x43bc
PM_STBY_CFG13	Standby Power Mode Configuration Register 13	0x43bd
PM_AVAIL_CR0	Power Mode Available Subsystem Control Register 0	0x43c0
PM_AVAIL_CR1	Power Mode Available Subsystem Control Register 1	0x43c1
PM_AVAIL_CR2	Power Mode Available Subsystem Control Register 2	0x43c2
PM_AVAIL_CR3	Power Mode Available Subsystem Control Register 3	0x43c3
PM_AVAIL_CR4	Power Mode Available Subsystem Control Register 4	0x43c4
PM_AVAIL_CR5	Power Mode Available Subsystem Control Register 5	0x43c5
PM_AVAIL_CR6	Power Mode Available Subsystem Control Register 6	0x43c6
PM_AVAIL_SR0	Power Mode Available Subsystem Status Register 0	0x43d0
PM_AVAIL_SR1	Power Mode Available Subsystem Status Register 1	0x43d1
PM_AVAIL_SR2	Power Mode Available Subsystem Status Register 2	0x43d2
PM_AVAIL_SR3	Power Mode Available Subsystem Status Register 3	0x43d3
PM_AVAIL_SR4	Power Mode Available Subsystem Status Register 4	0x43d4
PM_AVAIL_SR5	Power Mode Available Subsystem Status Register 5	0x43d5
PM_AVAIL_SR6	Power Mode Available Subsystem Status Register 6	0x43d6
INTC_VECT[0..31]	Interrupt Address Vector registers	0x4400 + [0..31 * 0x2]
INTC_PRIOR[0..31]	Interrrupt Controller Priority Registers	0x4480 + [0..31 * 0x1]
INTC_SET_EN[0..3]	Interrrupt Controller Set Enable Registers	0x44c0 + [0..3 * 0x1]
INTC_CLR_EN[0..3]	Interrrupt Controller Clear Enable Registers	0x44c8 + [0..3 * 0x1]
INTC_SET_PD[0..3]	Interrrupt Controller Set Pend Registers	0x44d0 + [0..3 * 0x1]
INTC_CLR_PD[0..3]	Interrrupt Controller Clear Pend Registers	0x44d8 + [0..3 * 0x1]

Register Name	Purpose	Address
INTC_NUM_LINES	Interrrupt Controller Number Of Lines Register	0x44f0
INTC_ACT_INT_NUM	Interrrupt Controller Active Interrupt Register	0x44f1
INTC_ACT_VECT	Interrrupt Controller Active Vector Register	0x44f2
INTC_CSR_EN	Interrrupt Controller Configuration and Status Register	0x44f4
PICU[0..15]_INTTYPE[0..7]	Port Interrupt Control Type Register	(0x4500 + [0..15 * 0x8]) + [0..7 * 0x1]
PICU[0..15]_INTSTAT	Port Interrupt Control Status Register	0x4580 + [0..15 * 0x1]
PICU[0..15]_SNAP	Port Interrupt Control Snap Shot Register	0x4590 + [0..15 * 0x1]
PICU[0..15]_DISABLE_COR	Disable Status Register Clear on Read Feature	0x45a0 + [0..15 * 0x1]
DAC[0..3]_TR	DAC Block Trim Register	0x4608 + [0..3 * 0x1]
NPUMP_DSM_TR0	Delta Sigma Modulator (DSM) Negative Pump Trim Register 0	0x4610
NPUMP_SC_TR0	Switched Cap Negative Pump Trim Register 0	0x4611
NPUMP_OPAMP_TR0	Analog Linear Output Buffer (OPAMP) Negative Pump Trim Register 0	0x4612
OPAMP[0..3]_TR0	Analog Output Buffer Trim Register 0	0x4620 + [0..3 * 0x2]
OPAMP[0..3]_TR1	Analog Output Buffer Trim Register 1	0x4620 + [0..3 * 0x2] + 0x1
CMP[0..3]_TR0	Comparator Trim Register for PMOS Load	0x4630 + [0..3 * 0x2]
CMP[0..3]_TR1	Comparator Trim Register for NMOS Load	0x4630 + [0..3 * 0x2] + 0x1
PWRSYS_HIB_TR0	Hibernate Trim Register 0	0x4680
PWRSYS_HIB_TR1	Hibernate Trim Register 1	0x4681
PWRSYS_I2C_TR	I2C Regulator Trim Register 1	0x4682
PWRSYS_SLP_TR	Sleep Regulator Trim Register	0x4683
PWRSYS_BUZZ_TR	Power Mode Buzz Trim Register	0x4684
PWRSYS_WAKE_TR0	Power Mode Wakeup Trim Register 0	0x4685
PWRSYS_WAKE_TR1	Power Mode Wakeup Trim Register 1	0x4686
PWRSYS_BREF_TR	Boot Reference Trim Register	0x4687
PWRSYS_BG_TR	Bandgap Trim	0x4688
PWRSYS_WAKE_TR2	Power Mode Wakeup Trim Register 2	0x4689
PWRSYS_WAKE_TR3	Power Mode Wakeup Trim Register 3	0x468a
ILO_TR0	Internal Low-speed Oscillator Trim Register	0x4690
ILO_TR1	Internal Low-speed Oscillator Coarse Trim Register	0x4691
X32_TR	32 kHz Watch Crystal Oscillator Trim Register	0x4698
IMO_TR0	Internal Main Oscillator Trim Register 0	0x46a0
IMO_TR1	Internal Main Oscillator Trim Register 1	0x46a1
IMO_GAIN	Internal Main Oscillator Gain Trim Register	0x46a2
IMO_C36M	Internal Main Oscillator 36 MHz clock control register {INTERNAL}	0x46a3
IMO_TR2	Internal Main Oscillator Trim Register 2	0x46a4
XMHZ_TR	External 4-25 MHz Crystal Oscillator Trim Register	0x46a8

Register Name	Purpose	Address
DLY	Delay block Configuration Register	0x46c0
MLOGIC_DMPSTR	Dumpster Register	0x46e2
MLOGIC_SEG_CR	Segment Control Register	0x46e4
MLOGIC_SEG_CFG0	Segment Configuration Register	0x46e5
MLOGIC_DEBUG	MLOGIC Debug Register	0x46e8
MLOGIC_CPU_SCR_CPU_SCR	System Status and Control Register	0x46ea
RESET_IPOR_CR0	Imprecise Power On Reset Control Register 0	0x46f0
RESET_IPOR_CR1	Imprecise Power On Reset Control Register 1	0x46f1
RESET_IPOR_CR2	Imprecise Power On Reset Control Register 2	0x46f2
RESET_IPOR_CR3	Imprecise Power On Reset Control Register 3	0x46f3
RESET_CR0	LVI Set Point Control Register	0x46f4
RESET_CR1	Reset System Control Register	0x46f5
RESET_CR2	Software Reset Control Register	0x46f6
RESET_CR3	LVI Mode Control Register	0x46f7
RESET_CR4	Reset Ignore Control Register	0x46f8
RESET_CR5	Reset Ignore Control Register	0x46f9
RESET_SR0	Reset and Voltage Detection Status Register 0	0x46fa
RESET_SR1	Reset and Voltage Detection Status Register 1	0x46fb
RESET_SR2	Reset and Voltage Detection Status Register 2	0x46fc
RESET_SR3	Reset and Voltage Detection Status Register 3	0x46fd
RESET_TR	PRES Trim Register	0x46fe
SPC_FM_EE_CR	FM_EE_CR	0x4700
SPC_FM_EE_WAKE_CNT	FM_EE_WAKE_CNT	0x4701
SPC_EE_SCR	EEPROM Status & Control Register	0x4702
SPC_EE_ERR	EEPROM Error Register	0x4703
SPC_CPU_DATA	SPC CPU Data Register	0x4720
SPC_DMA_DATA	SPC DMA Data Register	0x4721
SPC_SR	SPC Status Register	0x4722
SPC_CR	SPC Control Register	0x4723
SPC_DMM_MAP_SRAM[0..127]	SPC Direct Memory Mapping	0x4780 + [0..127 * 0x1]
CACHE_CR	Cache Control Register	0x4800
CACHE_LP_MODE	LP_MODE Register	0x4801
CACHE_SR	Cache Status Register	0x4808
CACHE_TAG_SR	Tag Status Register	0x4810
CACHE_TAG[0..7]	Tag Register	0x4818 + [0..7 * 0x8]
CACHE_INT_MSK	Cache controller Interrupt Mask	0x4858

Register Name	Purpose	Address
CACHE_INT_SR	Cache controller Interrupt Status	0x4860
CACHE_INT_LOG0	Interrupt Log 0	0x4868
CACHE_INT_LOG1	Interrupt Log 1	0x4870
CACHE_INT_LOG2	Interrupt Log 2	0x4878
CACHE_INT_LOG3	Interrupt Log 3	0x4880
CACHE_INT_LOG4	Interrupt Log 4	0x4888
CACHE_INT_LOG5	Interrupt Log 5	0x4890
I2C_XCFG	I2C Extended Configuration Register	0x49c8
I2C_ADR	I2C Slave Adddress Register	0x49ca
I2C_CFG	I2C Configuration Register	0x49d6
I2C_CSR	I2C Control and Status Register	0x49d7
I2C_D	I2C Data Register	0x49d8
I2C_MCSR	I2C Master Control and Status Register	0x49d9
I2C_CLK_DIV1	I2C Clock Divide Factor Register-1	0x49db
I2C_CLK_DIV2	I2C Clock Divide Factor Register-2	0x49dc
DEC_CR	Decimator Control Register	0x4e00
DEC_SR	Decimator Status Register	0x4e01
DEC_SHIFT1	Decimator Shifter 1 (Input)	0x4e02
DEC_SHIFT2	Decimator Shifter 2 (Output)	0x4e03
DEC_DR2	Decimator Decimation Rate (2)	0x4e04
DEC_DR2H	Decimator Decimation Rate (2) and Overflow Correction	0x4e05
DEC_DR1	Decimator Decimation Rate (1) of CIC Filter	0x4e06
DEC_OCOR	Decimator Offset Correction Coefficient (Low Byte)	0x4e08
DEC_OCORM	Decimator Offset Correction Coefficient (Middle Byte)	0x4e09
DEC_OCORH	Decimator Offset Correction Coefficient (High Byte)	0x4e0a
DEC_GCOR	Decimator Gain Correction Coefficient (Low Byte)	0x4e0c
DEC_GCORH	Decimator Gain Correction Coefficient (High Byte)	0x4e0d
DEC_GVAL	Decimator Gain Correction Size Register	0x4e0e
DEC_OUTSAMP	Decimator Output Data Sample (Low Byte)	0x4e10
DEC_OUTSAMPM	Decimator Output Data Sample (Middle Byte)	0x4e11
DEC_OUTSAMPH	Decimator Output Data Sample (High Byte)	0x4e12
DEC_OUTSAMPS	Decimator Output Data Sample (Sign Extension)	0x4e13
DEC_COHER	Decimator Coherency Register	0x4e14
TMR[0..3]_CFG0	Configuration Register CFG0	0x4f00 + [0..3 * 0xc]
TMR[0..3]_CFG1	Configuration Register CFG1	0x4f00 + [0..3 * 0xc] + 0x1
TMR[0..3]_CFG2	Configuration Register CFG2	0x4f00 + [0..3 * 0xc] + 0x2

Register Name	Purpose	Address
TMR[0..3]_SR0	Status Register SR0	0x4f00 + [0..3 * 0xc] + 0x3
TMR[0..3]_PER0	Timer Period Register PER0	0x4f00 + [0..3 * 0xc] + 0x4
TMR[0..3]_PER1	Timer Period Register PER1	0x4f00 + [0..3 * 0xc] + 0x5
TMR[0..3]_CNT_CMP0	Count/Comparator value CNT/CMP0	0x4f00 + [0..3 * 0xc] + 0x6
TMR[0..3]_CNT_CMP1	Count/Comparator value CNT/CMP1	0x4f00 + [0..3 * 0xc] + 0x7
TMR[0..3]_CAP0	Capture Value CAP0	0x4f00 + [0..3 * 0xc] + 0x8
TMR[0..3]_CAP1	Capture Value CAP1	0x4f00 + [0..3 * 0xc] + 0x9
TMR[0..3]_RT0	Configuration Register RT0	0x4f00 + [0..3 * 0xc] + 0xa
TMR[0..3]_RT1	Configuration Register RT1	0x4f00 + [0..3 * 0xc] + 0xb
PRT[0..14]_PC[0..7]	Port Pin Configuration Register	(0x5000 + [0..14 * 0x8]) + [0..7 * 0x1]
IO_PC_PRT15_PC[0..5]	Port Pin Configuration Register	0x5078 + [0..5 * 0x1]
IO_PC_PRT15_7_6_PC[0..1]	Port Pin Configuration Register	0x507e + [0..1 * 0x1]
PRT[0..14]_DR_ALIAS	Aliased Port Data Output Register	0x5080 + [0..14 * 0x1]
PRT15_DR_15_ALIAS	Aliased Port Data Output Register	0x508f
PRT[0..14]_PS_ALIAS	Aliased Port Pin State Register	0x5090 + [0..14 * 0x1]
PRT15_PS15_ALIAS	Aliased Port Pin State Register	0x509f
PRT[0..11]_DR	Port Data Output Register	0x5100 + [0..11 * 0x10]
PRT[0..11]_PS	Port Pin State Register1	0x5100 + [0..11 * 0x10] + 0x1
PRT[0..11]_DM[0..2]	Port Drive Mode Register	(0x5100 + [0..11 * 0x10]) + 0x2 + [0..2 * 0x1]
PRT[0..11]_SLW	Port slew rate control	0x5100 + [0..11 * 0x10] + 0x5
PRT[0..11]_BYP	Port Bypass enable	0x5100 + [0..11 * 0x10] + 0x6
PRT[0..11]_BIE	Port Bidirectional enable	0x5100 + [0..11 * 0x10] + 0x7
PRT[0..11]_INP_DIS	Input buffer disable override	0x5100 + [0..11 * 0x10] + 0x8
PRT[0..11]_CTL	Port wide control signals	0x5100 + [0..11 * 0x10] + 0x9
PRT[0..11]_PRT	Port wide configuration register	0x5100 + [0..11 * 0x10] + 0xa
PRT[0..11]_BIT_MASK	Bit-mask for Aliased Register access	0x5100 + [0..11 * 0x10] + 0xb
PRT[0..11]_AMUX	Port Analog global mux bus enable	0x5100 + [0..11 * 0x10] + 0xc
PRT[0..11]_AG	Port Analog global enable	0x5100 + [0..11 * 0x10] + 0xd
PRT[0..11]_LCD_COM_SEG	Port LCD Com seg bits.	0x5100 + [0..11 * 0x10] + 0xe
PRT[0..11]_LCD_EN	Port LCD enable register.	0x5100 + [0..11 * 0x10] + 0xf
PRT12_DR	Port Data Output Register	0x51c0
PRT12_PS	Port Pin State Register1	0x51c1
PRT12_DM[0..2]	Port Drive Mode Register	0x51c2 + [0..2 * 0x1]
PRT12_SLW	Port slew rate control	0x51c5
PRT12_BYP	Port Bypass enable	0x51c6

Register Name	Purpose	Address
PRT12_BIE	Port Bidirectional enable	0x51c7
PRT12_INP_DIS	Input buffer disable override	0x51c8
PRT12_SIO_HYST_EN	SIO Hysteresis enable	0x51c9
PRT12_PRT	Port wide configuration register	0x51ca
PRT12_BIT_MASK	Bit-mask for Aliased Register access	0x51cb
PRT12_SIO_REG_HIFREQ	Regulated pull-up driver DC current setting	0x51cc
PRT12_AG	Port Analog global enable	0x51cd
PRT12_SIO_CFG	SIO Input Output Configuration	0x51ce
PRT12_SIO_DIFF	Differential Input Buffer reference voltage selection	0x51cf
PRT15_DR	Port Data Output Register	0x51f0
PRT15_PS	Port Pin State Register1	0x51f1
PRT15_DM0	Port Drive Mode Register	0x51f2
PRT15_DM1	Port Drive Mode Register	0x51f3
PRT15_DM2	Port Drive Mode Register	0x51f4
PRT15_SLW	Port slew rate control	0x51f5
PRT15_BYP	Port Bypass enable	0x51f6
PRT15_BIE	Port Bidirection enable	0x51f7
PRT15_INP_DIS	Input buffer disable override	0x51f8
PRT15_CTL	Port wide control signals	0x51f9
PRT15_PRT	Port wide configuration register	0x51fa
PRT15_BIT_MASK	Bit-mask for Aliased Register access	0x51fb
PRT15_AMUX	Port Analog global mux bus enable	0x51fc
PRT15_AG	Port Analog global enable	0x51fd
PRT15_LCD_COM_SEG	Port LCD Com seg bits.	0x51fe
PRT15_LCD_EN	Port LCD enable register.	0x51ff
PRT0_OUT_SEL0	Digital System Interconnect Port Pin Output Select Registers.	0x5200
PRT0_OUT_SEL1	Digital System Interconnect Port Pin Output Select Registers.	0x5201
PRT0_OE_SEL0	Dynamic Drive Stength of Port Output Enable Select registers.	0x5202
PRT0_OE_SEL1	Dynamic Drive Stength of Port Output Enable Select registers.	0x5203
PRT0_DBL_SYNC_IN	DSI double sync enable register.	0x5204
PRT0_SYNC_OUT	DSI sync out enable register.	0x5205
PRT0_CAPS_SEL	Global DSI select register.	0x5206
PRT1_OUT_SEL0	Digital System Interconnect Port Pin Output Select Registers.	0x5208
PRT1_OUT_SEL1	Digital System Interconnect Port Pin Output Select Registers.	0x5209
PRT1_OE_SEL0	Dynamic Drive Stength of Port Output Enable Select registers.	0x520a
PRT1_OE_SEL1	Dynamic Drive Stength of Port Output Enable Select registers.	0x520b

Register Name	Purpose	Address
PRT1_DBL_SYNC_IN	DSI double sync enable register.	0x520c
PRT1_SYNC_OUT	DSI sync out enable register.	0x520d
PRT1_CAPS_SEL	Global DSI select register.	0x520e
PRT2_OUT_SEL0	Digital System Interconnect Port Pin Output Select Registers.	0x5210
PRT2_OUT_SEL1	Digital System Interconnect Port Pin Output Select Registers.	0x5211
PRT2_OE_SEL0	Dynamic Drive Stength of Port Output Enable Select registers.	0x5212
PRT2_OE_SEL1	Dynamic Drive Stength of Port Output Enable Select registers.	0x5213
PRT2_DBL_SYNC_IN	DSI double sync enable register.	0x5214
PRT2_SYNC_OUT	DSI sync out enable register.	0x5215
PRT2_CAPS_SEL	Global DSI select register.	0x5216
PRT3_OUT_SEL0	Digital System Interconnect Port Pin Output Select Registers.	0x5218
PRT3_OUT_SEL1	Digital System Interconnect Port Pin Output Select Registers.	0x5219
PRT3_OE_SEL0	Dynamic Drive Stength of Port Output Enable Select registers.	0x521a
PRT3_OE_SEL1	Dynamic Drive Stength of Port Output Enable Select registers.	0x521b
PRT3_DBL_SYNC_IN	DSI double sync enable register.	0x521c
PRT3_SYNC_OUT	DSI sync out enable register.	0x521d
PRT3_CAPS_SEL	Global DSI select register.	0x521e
PRT4_OUT_SEL0	Digital System Interconnect Port Pin Output Select Registers.	0x5220
PRT4_OUT_SEL1	Digital System Interconnect Port Pin Output Select Registers.	0x5221
PRT4_OE_SEL0	Dynamic Drive Stength of Port Output Enable Select registers.	0x5222
PRT4_OE_SEL1	Dynamic Drive Stength of Port Output Enable Select registers.	0x5223
PRT4_DBL_SYNC_IN	DSI double sync enable register.	0x5224
PRT4_SYNC_OUT	DSI sync out enable register.	0x5225
PRT4_CAPS_SEL	Global DSI select register.	0x5226
PRT5_OUT_SEL0	Digital System Interconnect Port Pin Output Select Registers.	0x5228
PRT5_OUT_SEL1	Digital System Interconnect Port Pin Output Select Registers.	0x5229
PRT5_OE_SEL0	Dynamic Drive Stength of Port Output Enable Select registers.	0x522a
PRT5_OE_SEL1	Dynamic Drive Stength of Port Output Enable Select registers.	0x522b
PRT5_DBL_SYNC_IN	DSI double sync enable register.	0x522c
PRT5_SYNC_OUT	DSI sync out enable register.	0x522d
PRT5_CAPS_SEL	Global DSI select register.	0x522e
PRT6_OUT_SEL0	Digital System Interconnect Port Pin Output Select Registers.	0x5230
PRT6_OUT_SEL1	Digital System Interconnect Port Pin Output Select Registers.	0x5231
PRT6_OE_SEL0	Dynamic Drive Stength of Port Output Enable Select registers.	0x5232
PRT6_OE_SEL1	Dynamic Drive Stength of Port Output Enable Select registers.	0x5233
PRT6_DBL_SYNC_IN	DSI double sync enable register.	0x5234

Register Name	Purpose	Address
PRT6_SYNC_OUT	DSI sync out enable register.	0x5235
PRT6_CAPS_SEL	Global DSI select register.	0x5236
PRT12_OUT_SEL0	Digital System Interconnect Port Pin Output Select Registers.	0x5260
PRT12_OUT_SEL1	Digital System Interconnect Port Pin Output Select Registers.	0x5261
PRT12_OE_SEL0	Dynamic Drive Stength of Port Output Enable Select registers.	0x5262
PRT12_OE_SEL1	Dynamic Drive Stength of Port Output Enable Select registers.	0x5263
PRT12_DBL_SYNC_IN	DSI double sync enable register.	0x5264
PRT12_SYNC_OUT	DSI sync out enable register.	0x5265
PRT15_OUT_SEL0	Digital System Interconnect Port Pin Output Select Registers.	0x5278
PRT15_OUT_SEL1	Digital System Interconnect Port Pin Output Select Registers.	0x5279
PRT15_OE_SEL0	Dynamic Drive Stength of Port Output Enable Select registers.	0x527a
PRT15_OE_SEL1	Dynamic Drive Stength of Port Output Enable Select registers.	0x527b
PRT15_DBL_SYNC_IN	DSI double sync enable register.	0x527c
PRT15_SYNC_OUT	DSI sync out enable register.	0x527d
PRT15_CAPS_SEL	Global DSI select register.	0x527e
EMIF_NO_UDB	EMIF UDB/NO_UDB Mode Register	0x5400
EMIF_RP_WAIT_STATES	External Memory Interface Read Path Wait States Register	0x5401
EMIF_MEM_DWN	External Memory Power Down Register	0x5402
EMIF_MEMCLK_DIV	External Memory Clock Divider Register	0x5403
EMIF_CLOCK_EN	EMIF Clock Enable Register	0x5404
EMIF_EM_TYPE	External Memory Type Register	0x5405
EMIF_WP_WAIT_STATES	External Memory Interface Write Path Wait States Register	0x5406
SC[0..3]_CR0	Switched Capacitor Control Register 0	0x5800 + [0..3 * 0x4]
SC[0..3]_CR1	Switched Capacitor Control Register 1	0x5800 + [0..3 * 0x4] + 0x1
SC[0..3]_CR2	Switched Capacitor Control Register 2	0x5800 + [0..3 * 0x4] + 0x2
DAC[0..3]_CR0	DAC Block Control Register 0	0x5820 + [0..3 * 0x4]
DAC[0..3]_CR1	DAC Block Control Register 1	0x5820 + [0..3 * 0x4] + 0x1
CMP[0..3]_CR	Comparator Control Register	0x5840 + [0..3 * 0x1]
LUT[0..3]_CR	LUT Config Register	0x5848 + [0..3 * 0x2]
LUT[0..3]_MX	LUT Input Mux Config Register	0x5848 + [0..3 * 0x2] + 0x1
OPAMP[0..3]_CR	Analog Output Buffer Configuration Register	0x5858 + [0..3 * 0x2]
OPAMP[0..3]_RSVD	OPAMP reserved	0x5858 + [0..3 * 0x2] + 0x1
LCDDAC_CR0	LCD Control Register 0	0x5868
LCDDAC_CR1	LCDDAC Control Register 1	0x5869
LCDDRV_CR	LCD Control Register	0x586a
LCDTMR_CFG	LCD Timer Configuration Register	0x586b

Register Name	Purpose	Address
BG_CR0	Bandgap Precision Reference Control 0	0x586c
BG_RSVD	Bandgap Precision Reference Reserved Register	0x586d
CAPSL_CFG0	Capsense Reference Driver Configuration Register	0x5870
CAPSL_CFG1	Capsense IO Configuration Register	0x5871
CAPSR_CFG0	Capsense Reference Driver Configuration Register	0x5872
CAPSR_CFG1	Capsense IO Configuration Register	0x5873
PUMP_CR0	Pump Configuration Register 0	0x5876
PUMP_CR1	Pump Configuration Register 1	0x5877
LPF0_CR0	Low Pass Filter Control Register	0x5878
LPF0_RSVD	LPF Reserved	0x5879
LPF1_CR0	Low Pass Filter Control Register	0x587a
LPF1_RSVD	LPF Reserved	0x587b
ANAIF_CFG_MISC_CR0	MISC Control Register 0	0x587c
DSM[0..0]_CR0	Delta Sigma Modulator Control Register 0	0x5880
DSM[0..0]_CR1	Delta Sigma Modulator Control Register 1	0x5881
DSM[0..0]_CR2	Delta Sigma Modulator Control Register 2	0x5882
DSM[0..0]_CR3	Delta Sigma Modulator Control Register 3	0x5883
DSM[0..0]_CR4	Delta Sigma Modulator Control Register 4	0x5884
DSM[0..0]_CR5	Delta Sigma Modulator Control Register 5	0x5885
DSM[0..0]_CR6	Delta Sigma Modulator Control Register 6	0x5886
DSM[0..0]_CR7	Delta Sigma Modulator Control Register 7	0x5887
DSM[0..0]_CR8	Delta Sigma Modulator Control Register 8	0x5888
DSM[0..0]_CR9	Delta Sigma Modulator Control Register 9	0x5889
DSM[0..0]_CR10	Delta Sigma Modulator Control Register 10	0x588a
DSM[0..0]_CR11	Delta Sigma Modulator Control Register 11	0x588b
DSM[0..0]_CR12	Delta Sigma Modulator Control Register 12	0x588c
DSM[0..0]_CR13	Delta Sigma Modulator Control Register 13	0x588d
DSM[0..0]_CR14	Delta Sigma Modulator Control Register 14	0x588e
DSM[0..0]_CR15	Delta Sigma Modulator Control Register 15	0x588f
DSM[0..0]_CR16	Delta Sigma Modulator Control Register 0	0x5890
DSM[0..0]_CR17	Delta Sigma Modulator Control Register	0x5891
DSM[0..0]_REF0	Delta Sigma Modulator Reference Register 0	0x5892
DSM[0..0]_REF1	Delta Sigma Modulator Reference Register 1	0x5893
DSM[0..0]_REF2	Delta Sigma Modulator Reference Register 2	0x5894
DSM[0..0]_REF3	Delta Sigma Modulator Reference Register 1	0x5895
DSM[0..0]_DEM0	Delta Sigma Modulator Dynamic Element Matching Register 0	0x5896

Register Name	Purpose	Address
DSM[0..0]_DEM1	Delta Sigma Modulator Dynamic Element Matching Register 1	0x5897
DSM[0..0]_BUF0	Delta Sigma Modulator Buffer Register 0	0x589a
DSM[0..0]_BUF1	Delta Sigma Modulator Buffer Register 1	0x589b
DSM[0..0]_BUF2	Delta Sigma Modulator Buffer Register 2	0x589c
DSM[0..0]_BUF3	Delta Sigma Modulator Buffer Register 2	0x589d
DSM[0..0]_MISC	Delta Sigma Modulator Miscellaneous register	0x589e
DSM[0..0]_RSVD1	Delta Sigma Modulator RSVD 1	0x589f
SC0_SW0	Switched Capacitor Analog Routing Register 0	0x5a00
SC0_SW2	Switched Capacitor Analog Routing Register 2	0x5a02
SC0_SW3	Switched Capacitor Analog Routing Register 3	0x5a03
SC0_SW4	Switched Capacitor Analog Routing Register 4	0x5a04
SC0_SW6	Switched Capacitor Analog Routing Register 6	0x5a06
SC0_SW7	Switched Capacitor Analog Routing Register 7	0x5a07
SC0_SW8	Switched Capacitor Analog Routing Register 8	0x5a08
SC0_SW10	Switched Capacitor Analog Routing Register 10	0x5a0a
SC0_CLK	Switched Capacitor Clock Selection Register	0x5a0b
SC0_BST	Switched Capacitor Boost Clock Selection Register	0x5a0c
SC1_SW0	Switched Capacitor Analog Routing Register 0	0x5a10
SC1_SW2	Switched Capacitor Analog Routing Register 2	0x5a12
SC1_SW3	Switched Capacitor Analog Routing Register 3	0x5a13
SC1_SW4	Switched Capacitor Analog Routing Register 4	0x5a14
SC1_SW6	Switched Capacitor Analog Routing Register 6	0x5a16
SC1_SW7	Switched Capacitor Analog Routing Register 7	0x5a17
SC1_SW8	Switched Capacitor Analog Routing Register 8	0x5a18
SC1_SW10	Switched Capacitor Analog Routing Register 10	0x5a1a
SC1_CLK	Switched Capacitor Clock Selection Register	0x5a1b
SC1_BST	Switched Capacitor Boost Clock Selection Register	0x5a1c
SC2_SW0	Switched Capacitor Analog Routing Register 0	0x5a20
SC2_SW2	Switched Capacitor Analog Routing Register 2	0x5a22
SC2_SW3	Switched Capacitor Analog Routing Register 3	0x5a23
SC2_SW4	Switched Capacitor Analog Routing Register 4	0x5a24
SC2_SW6	Switched Capacitor Analog Routing Register 6	0x5a26
SC2_SW7	Switched Capacitor Analog Routing Register 7	0x5a27
SC2_SW8	Switched Capacitor Analog Routing Register 8	0x5a28
SC2_SW10	Switched Capacitor Analog Routing Register 10	0x5a2a
SC2_CLK	Switched Capacitor Clock Selection Register	0x5a2b

Register Name	Purpose	Address
SC2_BST	Switched Capacitor Boost Clock Selection Register	0x5a2c
SC3_SW0	Switched Capacitor Analog Routing Register 0	0x5a30
SC3_SW2	Switched Capacitor Analog Routing Register 2	0x5a32
SC3_SW3	Switched Capacitor Analog Routing Register 3	0x5a33
SC3_SW4	Switched Capacitor Analog Routing Register 4	0x5a34
SC3_SW6	Switched Capacitor Analog Routing Register 6	0x5a36
SC3_SW7	Switched Capacitor Analog Routing Register 7	0x5a37
SC3_SW8	Switched Capacitor Analog Routing Register 8	0x5a38
SC3_SW10	Switched Capacitor Analog Routing Register 10	0x5a3a
SC3_CLK	Switched Capacitor Clock Selection Register	0x5a3b
SC3_BST	Switched Capacitor Boost Clock Selection Register	0x5a3c
DAC0_SW0	DAC Analog Routing Register 0	0x5a80
DAC0_SW2	DAC Analog Routing Register 2	0x5a82
DAC0_SW3	DAC Analog Routing Register 3	0x5a83
DAC0_SW4	DAC Analog Routing Register 4	0x5a84
DAC0_STROBE	DAC Strobe Register	0x5a87
DAC1_SW0	DAC Analog Routing Register 0	0x5a88
DAC1_SW2	DAC Analog Routing Register 2	0x5a8a
DAC1_SW3	DAC Analog Routing Register 3	0x5a8b
DAC1_SW4	DAC Analog Routing Register 4	0x5a8c
DAC1_STROBE	DAC Strobe Register	0x5a8f
DAC2_SW0	DAC Analog Routing Register 0	0x5a90
DAC2_SW2	DAC Analog Routing Register 2	0x5a92
DAC2_SW3	DAC Analog Routing Register 3	0x5a93
DAC2_SW4	DAC Analog Routing Register 4	0x5a94
DAC2_STROBE	DAC Strobe Register	0x5a97
DAC3_SW0	DAC Analog Routing Register 0	0x5a98
DAC3_SW2	DAC Analog Routing Register 2	0x5a9a
DAC3_SW3	DAC Analog Routing Register 3	0x5a9b
DAC3_SW4	DAC Analog Routing Register 4	0x5a9c
DAC3_STROBE	DAC Strobe Register	0x5a9f
CMP0_SW0	Comparator Analog Routing Register 0	0x5ac0
CMP0_SW2	Comparator Analog Routing Register 2	0x5ac2
CMP0_SW3	Comparator Analog Routing Register 3	0x5ac3
CMP0_SW4	Comparator Analog Routing Register 4	0x5ac4
CMP0_SW6	Comparator Analog Routing Register 6	0x5ac6

Register Name	Purpose	Address
CMP0_CLK	Comparator Clock Control Register	0x5ac7
CMP1_SW0	Comparator Analog Routing Register 0	0x5ac8
CMP1_SW2	Comparator Analog Routing Register 2	0x5aca
CMP1_SW3	Comparator Analog Routing Register 3	0x5acb
CMP1_SW4	Comparator Analog Routing Register 4	0x5acc
CMP1_SW6	Comparator Analog Routing Register 6	0x5ace
CMP1_CLK	Comparator Clock Control Register	0x5acf
CMP2_SW0	Comparator Analog Routing Register 0	0x5ad0
CMP2_SW2	Comparator Analog Routing Register 2	0x5ad2
CMP2_SW3	Comparator Analog Routing Register 3	0x5ad3
CMP2_SW4	Comparator Analog Routing Register 4	0x5ad4
CMP2_SW6	Comparator Analog Routing Register 6	0x5ad6
CMP2_CLK	Comparator Clock Control Register	0x5ad7
CMP3_SW0	Comparator Analog Routing Register 0	0x5ad8
CMP3_SW2	Comparator Analog Routing Register 2	0x5ada
CMP3_SW3	Comparator Analog Routing Register 3	0x5adb
CMP3_SW4	Comparator Analog Routing Register 4	0x5adc
CMP3_SW6	Comparator Analog Routing Register 6	0x5ade
CMP3_CLK	Comparator Clock Control Register	0x5adf
DSM0_SW0	Delta Sigma Modulator Analog Routing Register 0	0x5b00
DSM0_SW2	Delta Sigma Modulator Analog Routing Register 2	0x5b02
DSM0_SW3	Delta Sigma Modulator Analog Routing Register 3	0x5b03
DSM0_SW4	Delta Sigma Modulator Analog Routing Register 4	0x5b04
DSM0_SW6	Delta Sigma Modulator Analog Routing Register 6	0x5b06
DSM0_CLK	Delta Sigma Modulator Clock Selection Register	0x5b07
OPAMP0_MX	Analog Buffer Input Selection Register	0x5b40
OPAMP0_SW	Analog Buffer Routing Switch Register	0x5b41
OPAMP1_MX	Analog Buffer Input Selection Register	0x5b42
OPAMP1_SW	Analog Buffer Routing Switch Register	0x5b43
OPAMP2_MX	Analog Buffer Input Selection Register	0x5b44
OPAMP2_SW	Analog Buffer Routing Switch Register	0x5b45
OPAMP3_MX	Analog Buffer Input Selection Register	0x5b46
OPAMP3_SW	Analog Buffer Routing Switch Register	0x5b47
LCDDAC_SW0	LCDDAC Switch Register 0	0x5b50
LCDDAC_SW1	LCDDAC Switch Register 1	0x5b51
LCDDAC_SW2	LCDDAC Switch Register 2	0x5b52

Register Name	Purpose	Address
LCDDAC_SW3	LCDDAC Switch Register 3	0x5b53
LCDDAC_SW4	LCDDAC Switch Register 3	0x5b54
SC_MISC	Switched Cap Miscellaneous Control Register	0x5b56
BUS_SW0	Bus Switch Register 0	0x5b58
BUS_SW2	Bus Switch Register 2	0x5b5a
BUS_SW3	Bus Switch Register 3	0x5b5b
DAC[0..3]_D	DAC Data Register	0x5b80 + [0..3 * 0x1]
DSM[0..0]_OUT0	DSM Output Register 0	0x5b88
DSM[0..0]_OUT1	DSM Output Register 1	0x5b89
LUT_SR	LUT Status Register	0x5b90
LUT_WRK1	Reserved	0x5b91
LUT_MSK	LUT Interrupt ReQuest (IRQ) Mask Register	0x5b92
LUT_CLK	LUT CLK Register	0x5b93
LUT_CPTR	LUT Capture Mode Register	0x5b94
CMP_WRK	Comparator output working register	0x5b96
SC_SR	Switched Capacitor Status Register	0x5b98
SC_WRK1	Reserved	0x5b99
SC_MSK	SC IRQ Mask Register	0x5b9a
SC_CMPINV	SC comparator inversion	0x5b9b
SC_CPTR	SC Capture Mode Register	0x5b9c
USB_EP0_DR[0..7]	Control End point EP0 Data Register	0x6000 + [0..7 * 0x1]
USB_CR0	USB control 0 Register	0x6008
USB_CR1	USB control 1 Register	0x6009
USB_SIE_EP_INT_EN	USB SIE Data Endpoints Interrupt Enable Register	0x600a
USB_SIE_EP_INT_SR	SIE Data Endpoint Interrupt Status	0x600b
USB_SIE_EP1_CNT0	Non-control endpoint count register	0x600c
USB_SIE_EP1_CNT1	Non-control endpoint count register	0x600d
USB_SIE_EP1_CR0	Non-control endpoint's control Register	0x600e
USB_USBIO_CR0	USBIO Control 0 Register	0x6010
USB_USBIO_CR1	USBIO control 1 Register	0x6012
USB_DYN_RECONFIG	USB Dynamic reconfiguration register	0x6014
USB_SOF0	Start Of Frame Register	0x6018
USB_SOF1	Start Of Frame Register	0x6019
USB_SIE_EP2_CNT0	Non-control endpoint count register	0x601c
USB_SIE_EP2_CNT1	Non-control endpoint count register	0x601d
USB_SIE_EP2_CR0	Non-control endpoint's control Register	0x601e

Register Name	Purpose	Address
USB_EP0_CR	Endpoint0 control Register	0x6028
USB_EP0_CNT	Endpoint0 count Register	0x6029
USB_SIE_EP3_CNT0	Non-control endpoint count register	0x602c
USB_SIE_EP3_CNT1	Non-control endpoint count register	0x602d
USB_SIE_EP3_CR0	Non-control endpoint's control Register	0x602e
USB_SIE_EP4_CNT0	Non-control endpoint count register	0x603c
USB_SIE_EP4_CNT1	Non-control endpoint count register	0x603d
USB_SIE_EP4_CR0	Non-control endpoint's control Register	0x603e
USB_SIE_EP5_CNT0	Non-control endpoint count register	0x604c
USB_SIE_EP5_CNT1	Non-control endpoint count register	0x604d
USB_SIE_EP5_CR0	Non-control endpoint's control Register	0x604e
USB_SIE_EP6_CNT0	Non-control endpoint count register	0x605c
USB_SIE_EP6_CNT1	Non-control endpoint count register	0x605d
USB_SIE_EP6_CR0	Non-control endpoint's control Register	0x605e
USB_SIE_EP7_CNT0	Non-control endpoint count register	0x606c
USB_SIE_EP7_CNT1	Non-control endpoint count register	0x606d
USB_SIE_EP7_CR0	Non-control endpoint's control Register	0x606e
USB_SIE_EP8_CNT0	Non-control endpoint count register	0x607c
USB_SIE_EP8_CNT1	Non-control endpoint count register	0x607d
USB_SIE_EP8_CR0	Non-control endpoint's control Register	0x607e
USB_ARB_EP1_CFG	Endpoint Configuration Register	0x6080
USB_ARB_EP1_INT_EN	Endpoint Interrupt Enable Register	0x6081
USB_ARB_EP1_SR	Endpoint Status Register	0x6082
USB_ARB_RW1_WA	Endpoint Write Address value	0x6084
USB_ARB_RW1_WA_MSB	Endpoint Write Address value	0x6085
USB_ARB_RW1_RA	Endpoint Read Address value	0x6086
USB_ARB_RW1_RA_MSB	Endpoint Read Address value	0x6087
USB_ARB_RW1_DR	Endpoint Data Register	0x6088
USB_BUF_SIZE	Dedicated Endpoint Buffer Size Register	0x608c
USB_EP_ACTIVE	Endpoint Active Indication Register	0x608e
USB_EP_TYPE	Endpoint Type (IN/OUT) Indication	0x608f
USB_ARB_EP2_CFG	Endpoint Configuration Register	0x6090
USB_ARB_EP2_INT_EN	Endpoint Interrupt Enable Register	0x6091
USB_ARB_EP2_SR	Endpoint Status Register	0x6092
USB_ARB_RW2_WA	Endpoint Write Address value	0x6094
USB_ARB_RW2_WA_MSB	Endpoint Write Address value	0x6095

Register Name	Purpose	Address
USB_ARB_RW2_RA	Endpoint Read Address value	0x6096
USB_ARB_RW2_RA_MSB	Endpoint Read Address value	0x6097
USB_ARB_RW2_DR	Endpoint Data Register	0x6098
USB_ARB_CFG	Arbiter Configuration Register	0x609c
USB_USB_CLK_EN	USB Block Clock Enable Register	0x609d
USB_ARB_INT_EN	Arbiter Interrupt Enable	0x609e
USB_ARB_INT_SR	Arbiter Interrupt Status	0x609f
USB_ARB_EP3_CFG	Endpoint Configuration Register	0x60a0
USB_ARB_EP3_INT_EN	Endpoint Interrupt Enable Register	0x60a1
USB_ARB_EP3_SR	Endpoint Status Register	0x60a2
USB_ARB_RW3_WA	Endpoint Write Address value	0x60a4
USB_ARB_RW3_WA_MSB	Endpoint Write Address value	0x60a5
USB_ARB_RW3_RA	Endpoint Read Address value	0x60a6
USB_ARB_RW3_RA_MSB	Endpoint Read Address value	0x60a7
USB_ARB_RW3_DR	Endpoint Data Register	0x60a8
USB_CWA	Common Area Write Address	0x60ac
USB_CWA_MSB	Common Area Write Address	0x60ad
USB_ARB_EP4_CFG	Endpoint Configuration Register	0x60b0
USB_ARB_EP4_INT_EN	Endpoint Interrupt Enable Register	0x60b1
USB_ARB_EP4_SR	Endpoint Status Register	0x60b2
USB_ARB_RW4_WA	Endpoint Write Address value	0x60b4
USB_ARB_RW4_WA_MSB	Endpoint Write Address value	0x60b5
USB_ARB_RW4_RA	Endpoint Read Address value	0x60b6
USB_ARB_RW4_RA_MSB	Endpoint Read Address value	0x60b7
USB_ARB_RW4_DR	Endpoint Data Register	0x60b8
USB_DMA_THRES	DMA Burst / Threshold Configuration	0x60bc
USB_DMA_THRES_MSB	DMA Burst / Threshold Configuration	0x60bd
USB_ARB_EP5_CFG	Endpoint Configuration Register	0x60c0
USB_ARB_EP5_INT_EN	Endpoint Interrupt Enable Register	0x60c1
USB_ARB_EP5_SR	Endpoint Status Register	0x60c2
USB_ARB_RW5_WA	Endpoint Write Address value	0x60c4
USB_ARB_RW5_WA_MSB	Endpoint Write Address value	0x60c5
USB_ARB_RW5_RA	Endpoint Read Address value	0x60c6
USB_ARB_RW5_RA_MSB	Endpoint Read Address value	0x60c7
USB_ARB_RW5_DR	Endpoint Data Register	0x60c8
USB_BUS_RST_CNT	Bus Reset Count Register	0x60cc

Register Name	Purpose	Address
USB_ARB_EP6_CFG	Endpoint Configuration Register	0x60d0
USB_ARB_EP6_INT_EN	Endpoint Interrupt Enable Register	0x60d1
USB_ARB_EP6_SR	Endpoint Status Register	0x60d2
USB_ARB_RW6_WA	Endpoint Write Address value	0x60d4
USB_ARB_RW6_WA_MSB	Endpoint Write Address value	0x60d5
USB_ARB_RW6_RA	Endpoint Read Address value	0x60d6
USB_ARB_RW6_RA_MSB	Endpoint Read Address value	0x60d7
USB_ARB_RW6_DR	Endpoint Data Register	0x60d8
USB_ARB_EP7_CFG	Endpoint Configuration Register	0x60e0
USB_ARB_EP7_INT_EN	Endpoint Interrupt Enable Register	0x60e1
USB_ARB_EP7_SR	Endpoint Status Register	0x60e2
USB_ARB_RW7_WA	Endpoint Write Address value	0x60e4
USB_ARB_RW7_WA_MSB	Endpoint Write Address value	0x60e5
USB_ARB_RW7_RA	Endpoint Read Address value	0x60e6
USB_ARB_RW7_RA_MSB	Endpoint Read Address value	0x60e7
USB_ARB_RW7_DR	Endpoint Data Register	0x60e8
USB_ARB_EP8_CFG	Endpoint Configuration Register	0x60f0
USB_ARB_EP8_INT_EN	Endpoint Interrupt Enable Register	0x60f1
USB_ARB_EP8_SR	Endpoint Status Register	0x60f2
USB_ARB_RW8_WA	Endpoint Write Address value	0x60f4
USB_ARB_RW8_WA_MSB	Endpoint Write Address value	0x60f5
USB_ARB_RW8_RA	Endpoint Read Address value	0x60f6
USB_ARB_RW8_RA_MSB	Endpoint Read Address value	0x60f7
USB_ARB_RW8_DR	Endpoint Data Register	0x60f8
B[0..3]_UDB00_A0	UDB00_A0	0x6400 + [0..3 * 0x100]
B[0..3]_UDB01_A0	UDB01_A0	0x6400 + [0..3 * 0x100] + 0x1
B[0..3]_UDB02_A0	UDB02_A0	0x6400 + [0..3 * 0x100] + 0x2
B[0..3]_UDB03_A0	UDB03_A0	0x6400 + [0..3 * 0x100] + 0x3
B[0..3]_UDB04_A0	UDB04_A0	0x6400 + [0..3 * 0x100] + 0x4
B[0..3]_UDB05_A0	UDB05_A0	0x6400 + [0..3 * 0x100] + 0x5
B[0..3]_UDB06_A0	UDB06_A0	0x6400 + [0..3 * 0x100] + 0x6
B[0..3]_UDB07_A0	UDB07_A0	0x6400 + [0..3 * 0x100] + 0x7
B[0..3]_UDB08_A0	UDB08_A0	0x6400 + [0..3 * 0x100] + 0x8
B[0..3]_UDB09_A0	UDB09_A0	0x6400 + [0..3 * 0x100] + 0x9
B[0..3]_UDB10_A0	UDB10_A0	0x6400 + [0..3 * 0x100] + 0xa
B[0..3]_UDB11_A0	UDB11_A0	0x6400 + [0..3 * 0x100] + 0xb

Register Name	Purpose	Address
B[0..3]_UDB12_A0	UDB12_A0	0x6400 + [0..3 * 0x100] + 0xc
B[0..3]_UDB13_A0	UDB13_A0	0x6400 + [0..3 * 0x100] + 0xd
B[0..3]_UDB14_A0	UDB14_A0	0x6400 + [0..3 * 0x100] + 0xe
B[0..3]_UDB15_A0	UDB15_A0	0x6400 + [0..3 * 0x100] + 0xf
B[0..3]_UDB00_A1	UDB00_A1	0x6400 + [0..3 * 0x100] + 0x10
B[0..3]_UDB01_A1	UDB01_A1	0x6400 + [0..3 * 0x100] + 0x11
B[0..3]_UDB02_A1	UDB02_A1	0x6400 + [0..3 * 0x100] + 0x12
B[0..3]_UDB03_A1	UDB03_A1	0x6400 + [0..3 * 0x100] + 0x13
B[0..3]_UDB04_A1	UDB04_A1	0x6400 + [0..3 * 0x100] + 0x14
B[0..3]_UDB05_A1	UDB05_A1	0x6400 + [0..3 * 0x100] + 0x15
B[0..3]_UDB06_A1	UDB06_A1	0x6400 + [0..3 * 0x100] + 0x16
B[0..3]_UDB07_A1	UDB07_A1	0x6400 + [0..3 * 0x100] + 0x17
B[0..3]_UDB08_A1	UDB08_A1	0x6400 + [0..3 * 0x100] + 0x18
B[0..3]_UDB09_A1	UDB09_A1	0x6400 + [0..3 * 0x100] + 0x19
B[0..3]_UDB10_A1	UDB10_A1	0x6400 + [0..3 * 0x100] + 0x1a
B[0..3]_UDB11_A1	UDB11_A1	0x6400 + [0..3 * 0x100] + 0x1b
B[0..3]_UDB12_A1	UDB12_A1	0x6400 + [0..3 * 0x100] + 0x1c
B[0..3]_UDB13_A1	UDB13_A1	0x6400 + [0..3 * 0x100] + 0x1d
B[0..3]_UDB14_A1	UDB14_A1	0x6400 + [0..3 * 0x100] + 0x1e
B[0..3]_UDB15_A1	UDB15_A1	0x6400 + [0..3 * 0x100] + 0x1f
B[0..3]_UDB00_D0	UDB00_D0	0x6400 + [0..3 * 0x100] + 0x20
B[0..3]_UDB01_D0	UDB01_D0	0x6400 + [0..3 * 0x100] + 0x21
B[0..3]_UDB02_D0	UDB02_D0	0x6400 + [0..3 * 0x100] + 0x22
B[0..3]_UDB03_D0	UDB03_D0	0x6400 + [0..3 * 0x100] + 0x23
B[0..3]_UDB04_D0	UDB04_D0	0x6400 + [0..3 * 0x100] + 0x24
B[0..3]_UDB05_D0	UDB05_D0	0x6400 + [0..3 * 0x100] + 0x25
B[0..3]_UDB06_D0	UDB06_D0	0x6400 + [0..3 * 0x100] + 0x26
B[0..3]_UDB07_D0	UDB07_D0	0x6400 + [0..3 * 0x100] + 0x27
B[0..3]_UDB08_D0	UDB08_D0	0x6400 + [0..3 * 0x100] + 0x28
B[0..3]_UDB09_D0	UDB09_D0	0x6400 + [0..3 * 0x100] + 0x29
B[0..3]_UDB10_D0	UDB10_D0	0x6400 + [0..3 * 0x100] + 0x2a
B[0..3]_UDB11_D0	UDB11_D0	0x6400 + [0..3 * 0x100] + 0x2b
B[0..3]_UDB12_D0	UDB12_D0	0x6400 + [0..3 * 0x100] + 0x2c
B[0..3]_UDB13_D0	UDB13_D0	0x6400 + [0..3 * 0x100] + 0x2d
B[0..3]_UDB14_D0	UDB14_D0	0x6400 + [0..3 * 0x100] + 0x2e
B[0..3]_UDB15_D0	UDB15_D0	0x6400 + [0..3 * 0x100] + 0x2f

Register Name	Purpose	Address
B[0..3]_UDB00_D1	UDB00_D1	0x6400 + [0..3 * 0x100] + 0x30
B[0..3]_UDB01_D1	UDB01_D1	0x6400 + [0..3 * 0x100] + 0x31
B[0..3]_UDB02_D1	UDB02_D1	0x6400 + [0..3 * 0x100] + 0x32
B[0..3]_UDB03_D1	UDB03_D1	0x6400 + [0..3 * 0x100] + 0x33
B[0..3]_UDB04_D1	UDB04_D1	0x6400 + [0..3 * 0x100] + 0x34
B[0..3]_UDB05_D1	UDB05_D1	0x6400 + [0..3 * 0x100] + 0x35
B[0..3]_UDB06_D1	UDB06_D1	0x6400 + [0..3 * 0x100] + 0x36
B[0..3]_UDB07_D1	UDB07_D1	0x6400 + [0..3 * 0x100] + 0x37
B[0..3]_UDB08_D1	UDB08_D1	0x6400 + [0..3 * 0x100] + 0x38
B[0..3]_UDB09_D1	UDB09_D1	0x6400 + [0..3 * 0x100] + 0x39
B[0..3]_UDB10_D1	UDB10_D1	0x6400 + [0..3 * 0x100] + 0x3a
B[0..3]_UDB11_D1	UDB11_D1	0x6400 + [0..3 * 0x100] + 0x3b
B[0..3]_UDB12_D1	UDB12_D1	0x6400 + [0..3 * 0x100] + 0x3c
B[0..3]_UDB13_D1	UDB13_D1	0x6400 + [0..3 * 0x100] + 0x3d
B[0..3]_UDB14_D1	UDB14_D1	0x6400 + [0..3 * 0x100] + 0x3e
B[0..3]_UDB15_D1	UDB15_D1	0x6400 + [0..3 * 0x100] + 0x3f
B[0..3]_UDB00_F0	UDB00_F0	0x6400 + [0..3 * 0x100] + 0x40
B[0..3]_UDB01_F0	UDB01_F0	0x6400 + [0..3 * 0x100] + 0x41
B[0..3]_UDB02_F0	UDB02_F0	0x6400 + [0..3 * 0x100] + 0x42
B[0..3]_UDB03_F0	UDB03_F0	0x6400 + [0..3 * 0x100] + 0x43
B[0..3]_UDB04_F0	UDB04_F0	0x6400 + [0..3 * 0x100] + 0x44
B[0..3]_UDB05_F0	UDB05_F0	0x6400 + [0..3 * 0x100] + 0x45
B[0..3]_UDB06_F0	UDB06_F0	0x6400 + [0..3 * 0x100] + 0x46
B[0..3]_UDB07_F0	UDB07_F0	0x6400 + [0..3 * 0x100] + 0x47
B[0..3]_UDB08_F0	UDB08_F0	0x6400 + [0..3 * 0x100] + 0x48
B[0..3]_UDB09_F0	UDB09_F0	0x6400 + [0..3 * 0x100] + 0x49
B[0..3]_UDB10_F0	UDB10_F0	0x6400 + [0..3 * 0x100] + 0x4a
B[0..3]_UDB11_F0	UDB11_F0	0x6400 + [0..3 * 0x100] + 0x4b
B[0..3]_UDB12_F0	UDB12_F0	0x6400 + [0..3 * 0x100] + 0x4c
B[0..3]_UDB13_F0	UDB13_F0	0x6400 + [0..3 * 0x100] + 0x4d
B[0..3]_UDB14_F0	UDB14_F0	0x6400 + [0..3 * 0x100] + 0x4e
B[0..3]_UDB15_F0	UDB15_F0	0x6400 + [0..3 * 0x100] + 0x4f
B[0..3]_UDB00_F1	UDB00_F1	0x6400 + [0..3 * 0x100] + 0x50
B[0..3]_UDB01_F1	UDB01_F1	0x6400 + [0..3 * 0x100] + 0x51
B[0..3]_UDB02_F1	UDB02_F1	0x6400 + [0..3 * 0x100] + 0x52
B[0..3]_UDB03_F1	UDB03_F1	0x6400 + [0..3 * 0x100] + 0x53

Register Name	Purpose	Address
B[0..3]_UDB04_F1	UDB04_F1	0x6400 + [0..3 * 0x100] + 0x54
B[0..3]_UDB05_F1	UDB05_F1	0x6400 + [0..3 * 0x100] + 0x55
B[0..3]_UDB06_F1	UDB06_F1	0x6400 + [0..3 * 0x100] + 0x56
B[0..3]_UDB07_F1	UDB07_F1	0x6400 + [0..3 * 0x100] + 0x57
B[0..3]_UDB08_F1	UDB08_F1	0x6400 + [0..3 * 0x100] + 0x58
B[0..3]_UDB09_F1	UDB09_F1	0x6400 + [0..3 * 0x100] + 0x59
B[0..3]_UDB10_F1	UDB10_F1	0x6400 + [0..3 * 0x100] + 0x5a
B[0..3]_UDB11_F1	UDB11_F1	0x6400 + [0..3 * 0x100] + 0x5b
B[0..3]_UDB12_F1	UDB12_F1	0x6400 + [0..3 * 0x100] + 0x5c
B[0..3]_UDB13_F1	UDB13_F1	0x6400 + [0..3 * 0x100] + 0x5d
B[0..3]_UDB14_F1	UDB14_F1	0x6400 + [0..3 * 0x100] + 0x5e
B[0..3]_UDB15_F1	UDB15_F1	0x6400 + [0..3 * 0x100] + 0x5f
B[0..3]_UDB00_ST	UDB00_ST	0x6400 + [0..3 * 0x100] + 0x60
B[0..3]_UDB01_ST	UDB01_ST	0x6400 + [0..3 * 0x100] + 0x61
B[0..3]_UDB02_ST	UDB02_ST	0x6400 + [0..3 * 0x100] + 0x62
B[0..3]_UDB03_ST	UDB03_ST	0x6400 + [0..3 * 0x100] + 0x63
B[0..3]_UDB04_ST	UDB04_ST	0x6400 + [0..3 * 0x100] + 0x64
B[0..3]_UDB05_ST	UDB05_ST	0x6400 + [0..3 * 0x100] + 0x65
B[0..3]_UDB06_ST	UDB06_ST	0x6400 + [0..3 * 0x100] + 0x66
B[0..3]_UDB07_ST	UDB07_ST	0x6400 + [0..3 * 0x100] + 0x67
B[0..3]_UDB08_ST	UDB08_ST	0x6400 + [0..3 * 0x100] + 0x68
B[0..3]_UDB09_ST	UDB09_ST	0x6400 + [0..3 * 0x100] + 0x69
B[0..3]_UDB10_ST	UDB10_ST	0x6400 + [0..3 * 0x100] + 0x6a
B[0..3]_UDB11_ST	UDB11_ST	0x6400 + [0..3 * 0x100] + 0x6b
B[0..3]_UDB12_ST	UDB12_ST	0x6400 + [0..3 * 0x100] + 0x6c
B[0..3]_UDB13_ST	UDB13_ST	0x6400 + [0..3 * 0x100] + 0x6d
B[0..3]_UDB14_ST	UDB14_ST	0x6400 + [0..3 * 0x100] + 0x6e
B[0..3]_UDB15_ST	UDB15_ST	0x6400 + [0..3 * 0x100] + 0x6f
B[0..3]_UDB00_CTL	UDB00_CTL	0x6400 + [0..3 * 0x100] + 0x70
B[0..3]_UDB01_CTL	UDB01_CTL	0x6400 + [0..3 * 0x100] + 0x71
B[0..3]_UDB02_CTL	UDB02_CTL	0x6400 + [0..3 * 0x100] + 0x72
B[0..3]_UDB03_CTL	UDB03_CTL	0x6400 + [0..3 * 0x100] + 0x73
B[0..3]_UDB04_CTL	UDB04_CTL	0x6400 + [0..3 * 0x100] + 0x74
B[0..3]_UDB05_CTL	UDB05_CTL	0x6400 + [0..3 * 0x100] + 0x75
B[0..3]_UDB06_CTL	UDB06_CTL	0x6400 + [0..3 * 0x100] + 0x76
B[0..3]_UDB07_CTL	UDB07_CTL	0x6400 + [0..3 * 0x100] + 0x77

Register Name	Purpose	Address
B[0..3]_UDB08_CTL	UDB08_CTL	0x6400 + [0..3 * 0x100] + 0x78
B[0..3]_UDB09_CTL	UDB09_CTL	0x6400 + [0..3 * 0x100] + 0x79
B[0..3]_UDB10_CTL	UDB10_CTL	0x6400 + [0..3 * 0x100] + 0x7a
B[0..3]_UDB11_CTL	UDB11_CTL	0x6400 + [0..3 * 0x100] + 0x7b
B[0..3]_UDB12_CTL	UDB12_CTL	0x6400 + [0..3 * 0x100] + 0x7c
B[0..3]_UDB13_CTL	UDB13_CTL	0x6400 + [0..3 * 0x100] + 0x7d
B[0..3]_UDB14_CTL	UDB14_CTL	0x6400 + [0..3 * 0x100] + 0x7e
B[0..3]_UDB15_CTL	UDB15_CTL	0x6400 + [0..3 * 0x100] + 0x7f
B[0..3]_UDB00_MSK	UDB00_MSK	0x6400 + [0..3 * 0x100] + 0x80
B[0..3]_UDB01_MSK	UDB01_MSK	0x6400 + [0..3 * 0x100] + 0x81
B[0..3]_UDB02_MSK	UDB02_MSK	0x6400 + [0..3 * 0x100] + 0x82
B[0..3]_UDB03_MSK	UDB03_MSK	0x6400 + [0..3 * 0x100] + 0x83
B[0..3]_UDB04_MSK	UDB04_MSK	0x6400 + [0..3 * 0x100] + 0x84
B[0..3]_UDB05_MSK	UDB05_MSK	0x6400 + [0..3 * 0x100] + 0x85
B[0..3]_UDB06_MSK	UDB06_MSK	0x6400 + [0..3 * 0x100] + 0x86
B[0..3]_UDB07_MSK	UDB07_MSK	0x6400 + [0..3 * 0x100] + 0x87
B[0..3]_UDB08_MSK	UDB08_MSK	0x6400 + [0..3 * 0x100] + 0x88
B[0..3]_UDB09_MSK	UDB09_MSK	0x6400 + [0..3 * 0x100] + 0x89
B[0..3]_UDB10_MSK	UDB10_MSK	0x6400 + [0..3 * 0x100] + 0x8a
B[0..3]_UDB11_MSK	UDB11_MSK	0x6400 + [0..3 * 0x100] + 0x8b
B[0..3]_UDB12_MSK	UDB12_MSK	0x6400 + [0..3 * 0x100] + 0x8c
B[0..3]_UDB13_MSK	UDB13_MSK	0x6400 + [0..3 * 0x100] + 0x8d
B[0..3]_UDB14_MSK	UDB14_MSK	0x6400 + [0..3 * 0x100] + 0x8e
B[0..3]_UDB15_MSK	UDB15_MSK	0x6400 + [0..3 * 0x100] + 0x8f
B[0..3]_UDB00_ACTL	UDB00_ACTL	0x6400 + [0..3 * 0x100] + 0x90
B[0..3]_UDB01_ACTL	UDB01_ACTL	0x6400 + [0..3 * 0x100] + 0x91
B[0..3]_UDB02_ACTL	UDB02_ACTL	0x6400 + [0..3 * 0x100] + 0x92
B[0..3]_UDB03_ACTL	UDB03_ACTL	0x6400 + [0..3 * 0x100] + 0x93
B[0..3]_UDB04_ACTL	UDB04_ACTL	0x6400 + [0..3 * 0x100] + 0x94
B[0..3]_UDB05_ACTL	UDB05_ACTL	0x6400 + [0..3 * 0x100] + 0x95
B[0..3]_UDB06_ACTL	UDB06_ACTL	0x6400 + [0..3 * 0x100] + 0x96
B[0..3]_UDB07_ACTL	UDB07_ACTL	0x6400 + [0..3 * 0x100] + 0x97
B[0..3]_UDB08_ACTL	UDB08_ACTL	0x6400 + [0..3 * 0x100] + 0x98
B[0..3]_UDB09_ACTL	UDB09_ACTL	0x6400 + [0..3 * 0x100] + 0x99
B[0..3]_UDB10_ACTL	UDB10_ACTL	0x6400 + [0..3 * 0x100] + 0x9a
B[0..3]_UDB11_ACTL	UDB11_ACTL	0x6400 + [0..3 * 0x100] + 0x9b

Register Name	Purpose	Address
B[0..3]_UDB12_ACTL	UDB12_ACTL	0x6400 + [0..3 * 0x100] + 0x9c
B[0..3]_UDB13_ACTL	UDB13_ACTL	0x6400 + [0..3 * 0x100] + 0x9d
B[0..3]_UDB14_ACTL	UDB14_ACTL	0x6400 + [0..3 * 0x100] + 0x9e
B[0..3]_UDB15_ACTL	UDB15_ACTL	0x6400 + [0..3 * 0x100] + 0x9f
B[0..3]_UDB00_MC	UDB00_MC	0x6400 + [0..3 * 0x100] + 0xa0
B[0..3]_UDB01_MC	UDB01_MC	0x6400 + [0..3 * 0x100] + 0xa1
B[0..3]_UDB02_MC	UDB02_MC	0x6400 + [0..3 * 0x100] + 0xa2
B[0..3]_UDB03_MC	UDB03_MC	0x6400 + [0..3 * 0x100] + 0xa3
B[0..3]_UDB04_MC	UDB04_MC	0x6400 + [0..3 * 0x100] + 0xa4
B[0..3]_UDB05_MC	UDB05_MC	0x6400 + [0..3 * 0x100] + 0xa5
B[0..3]_UDB06_MC	UDB06_MC	0x6400 + [0..3 * 0x100] + 0xa6
B[0..3]_UDB07_MC	UDB07_MC	0x6400 + [0..3 * 0x100] + 0xa7
B[0..3]_UDB08_MC	UDB08_MC	0x6400 + [0..3 * 0x100] + 0xa8
B[0..3]_UDB09_MC	UDB09_MC	0x6400 + [0..3 * 0x100] + 0xa9
B[0..3]_UDB10_MC	UDB10_MC	0x6400 + [0..3 * 0x100] + 0xaa
B[0..3]_UDB11_MC	UDB11_MC	0x6400 + [0..3 * 0x100] + 0xab
B[0..3]_UDB12_MC	UDB12_MC	0x6400 + [0..3 * 0x100] + 0xac
B[0..3]_UDB13_MC	UDB13_MC	0x6400 + [0..3 * 0x100] + 0xad
B[0..3]_UDB14_MC	UDB14_MC	0x6400 + [0..3 * 0x100] + 0xae
B[0..3]_UDB15_MC	UDB15_MC	0x6400 + [0..3 * 0x100] + 0xaf
B[0..3]_UDB00_01_A0	UDB00_01_A0	0x6800 + [0..3 * 0x200]
B[0..3]_UDB01_02_A0	UDB01_02_A0	0x6800 + [0..3 * 0x200] + 0x2
B[0..3]_UDB02_03_A0	UDB02_03_A0	0x6800 + [0..3 * 0x200] + 0x4
B[0..3]_UDB03_04_A0	UDB03_04_A0	0x6800 + [0..3 * 0x200] + 0x6
B[0..3]_UDB04_05_A0	UDB04_05_A0	0x6800 + [0..3 * 0x200] + 0x8
B[0..3]_UDB05_06_A0	UDB05_06_A0	0x6800 + [0..3 * 0x200] + 0xa
B[0..3]_UDB06_07_A0	UDB06_07_A0	0x6800 + [0..3 * 0x200] + 0xc
B[0..3]_UDB07_08_A0	UDB07_08_A0	0x6800 + [0..3 * 0x200] + 0xe
B[0..3]_UDB08_09_A0	UDB08_09_A0	0x6800 + [0..3 * 0x200] + 0x10
B[0..3]_UDB09_10_A0	UDB09_10_A0	0x6800 + [0..3 * 0x200] + 0x12
B[0..3]_UDB10_11_A0	UDB10_11_A0	0x6800 + [0..3 * 0x200] + 0x14
B[0..3]_UDB11_12_A0	UDB11_12_A0	0x6800 + [0..3 * 0x200] + 0x16
B[0..3]_UDB12_13_A0	UDB12_13_A0	0x6800 + [0..3 * 0x200] + 0x18
B[0..3]_UDB13_14_A0	UDB13_14_A0	0x6800 + [0..3 * 0x200] + 0x1a
B[0..3]_UDB14_15_A0	UDB14_15_A0	0x6800 + [0..3 * 0x200] + 0x1c
B[0..3]_UDB00_01_A1	UDB00_01_A1	0x6800 + [0..3 * 0x200] + 0x20

Register Name	Purpose	Address
B[0..3]_UDB01_02_A1	UDB01_02_A1	0x6800 + [0..3 * 0x200] + 0x22
B[0..3]_UDB02_03_A1	UDB02_03_A1	0x6800 + [0..3 * 0x200] + 0x24
B[0..3]_UDB03_04_A1	UDB03_04_A1	0x6800 + [0..3 * 0x200] + 0x26
B[0..3]_UDB04_05_A1	UDB04_05_A1	0x6800 + [0..3 * 0x200] + 0x28
B[0..3]_UDB05_06_A1	UDB05_06_A1	0x6800 + [0..3 * 0x200] + 0x2a
B[0..3]_UDB06_07_A1	UDB06_07_A1	0x6800 + [0..3 * 0x200] + 0x2c
B[0..3]_UDB07_08_A1	UDB07_08_A1	0x6800 + [0..3 * 0x200] + 0x2e
B[0..3]_UDB08_09_A1	UDB08_09_A1	0x6800 + [0..3 * 0x200] + 0x30
B[0..3]_UDB09_10_A1	UDB09_10_A1	0x6800 + [0..3 * 0x200] + 0x32
B[0..3]_UDB10_11_A1	UDB10_11_A1	0x6800 + [0..3 * 0x200] + 0x34
B[0..3]_UDB11_12_A1	UDB11_12_A1	0x6800 + [0..3 * 0x200] + 0x36
B[0..3]_UDB12_13_A1	UDB12_13_A1	0x6800 + [0..3 * 0x200] + 0x38
B[0..3]_UDB13_14_A1	UDB13_14_A1	0x6800 + [0..3 * 0x200] + 0x3a
B[0..3]_UDB14_15_A1	UDB14_15_A1	0x6800 + [0..3 * 0x200] + 0x3c
B[0..3]_UDB00_01_D0	UDB00_01_D0	0x6800 + [0..3 * 0x200] + 0x40
B[0..3]_UDB01_02_D0	UDB01_02_D0	0x6800 + [0..3 * 0x200] + 0x42
B[0..3]_UDB02_03_D0	UDB02_03_D0	0x6800 + [0..3 * 0x200] + 0x44
B[0..3]_UDB03_04_D0	UDB03_04_D0	0x6800 + [0..3 * 0x200] + 0x46
B[0..3]_UDB04_05_D0	UDB04_05_D0	0x6800 + [0..3 * 0x200] + 0x48
B[0..3]_UDB05_06_D0	UDB05_06_D0	0x6800 + [0..3 * 0x200] + 0x4a
B[0..3]_UDB06_07_D0	UDB06_07_D0	0x6800 + [0..3 * 0x200] + 0x4c
B[0..3]_UDB07_08_D0	UDB07_08_D0	0x6800 + [0..3 * 0x200] + 0x4e
B[0..3]_UDB08_09_D0	UDB08_09_D0	0x6800 + [0..3 * 0x200] + 0x50
B[0..3]_UDB09_10_D0	UDB09_10_D0	0x6800 + [0..3 * 0x200] + 0x52
B[0..3]_UDB10_11_D0	UDB10_11_D0	0x6800 + [0..3 * 0x200] + 0x54
B[0..3]_UDB11_12_D0	UDB11_12_D0	0x6800 + [0..3 * 0x200] + 0x56
B[0..3]_UDB12_13_D0	UDB12_13_D0	0x6800 + [0..3 * 0x200] + 0x58
B[0..3]_UDB13_14_D0	UDB13_14_D0	0x6800 + [0..3 * 0x200] + 0x5a
B[0..3]_UDB14_15_D0	UDB14_15_D0	0x6800 + [0..3 * 0x200] + 0x5c
B[0..3]_UDB00_01_D1	UDB00_01_D1	0x6800 + [0..3 * 0x200] + 0x60
B[0..3]_UDB01_02_D1	UDB01_02_D1	0x6800 + [0..3 * 0x200] + 0x62
B[0..3]_UDB02_03_D1	UDB02_03_D1	0x6800 + [0..3 * 0x200] + 0x64
B[0..3]_UDB03_04_D1	UDB03_04_D1	0x6800 + [0..3 * 0x200] + 0x66
B[0..3]_UDB04_05_D1	UDB04_05_D1	0x6800 + [0..3 * 0x200] + 0x68
B[0..3]_UDB05_06_D1	UDB05_06_D1	0x6800 + [0..3 * 0x200] + 0x6a
B[0..3]_UDB06_07_D1	UDB06_07_D1	0x6800 + [0..3 * 0x200] + 0x6c

Register Name	Purpose	Address
B[0..3]_UDB07_08_D1	UDB07_08_D1	0x6800 + [0..3 * 0x200] + 0x6e
B[0..3]_UDB08_09_D1	UDB08_09_D1	0x6800 + [0..3 * 0x200] + 0x70
B[0..3]_UDB09_10_D1	UDB09_10_D1	0x6800 + [0..3 * 0x200] + 0x72
B[0..3]_UDB10_11_D1	UDB10_11_D1	0x6800 + [0..3 * 0x200] + 0x74
B[0..3]_UDB11_12_D1	UDB11_12_D1	0x6800 + [0..3 * 0x200] + 0x76
B[0..3]_UDB12_13_D1	UDB12_13_D1	0x6800 + [0..3 * 0x200] + 0x78
B[0..3]_UDB13_14_D1	UDB13_14_D1	0x6800 + [0..3 * 0x200] + 0x7a
B[0..3]_UDB14_15_D1	UDB14_15_D1	0x6800 + [0..3 * 0x200] + 0x7c
B[0..3]_UDB00_01_F0	UDB00_01_F0	0x6800 + [0..3 * 0x200] + 0x80
B[0..3]_UDB01_02_F0	UDB01_02_F0	0x6800 + [0..3 * 0x200] + 0x82
B[0..3]_UDB02_03_F0	UDB02_03_F0	0x6800 + [0..3 * 0x200] + 0x84
B[0..3]_UDB03_04_F0	UDB03_04_F0	0x6800 + [0..3 * 0x200] + 0x86
B[0..3]_UDB04_05_F0	UDB04_05_F0	0x6800 + [0..3 * 0x200] + 0x88
B[0..3]_UDB05_06_F0	UDB05_06_F0	0x6800 + [0..3 * 0x200] + 0x8a
B[0..3]_UDB06_07_F0	UDB06_07_F0	0x6800 + [0..3 * 0x200] + 0x8c
B[0..3]_UDB07_08_F0	UDB07_08_F0	0x6800 + [0..3 * 0x200] + 0x8e
B[0..3]_UDB08_09_F0	UDB08_09_F0	0x6800 + [0..3 * 0x200] + 0x90
B[0..3]_UDB09_10_F0	UDB09_10_F0	0x6800 + [0..3 * 0x200] + 0x92
B[0..3]_UDB10_11_F0	UDB10_11_F0	0x6800 + [0..3 * 0x200] + 0x94
B[0..3]_UDB11_12_F0	UDB11_12_F0	0x6800 + [0..3 * 0x200] + 0x96
B[0..3]_UDB12_13_F0	UDB12_13_F0	0x6800 + [0..3 * 0x200] + 0x98
B[0..3]_UDB13_14_F0	UDB13_14_F0	0x6800 + [0..3 * 0x200] + 0x9a
B[0..3]_UDB14_15_F0	UDB14_15_F0	0x6800 + [0..3 * 0x200] + 0x9c
B[0..3]_UDB00_01_F1	UDB00_01_F1	0x6800 + [0..3 * 0x200] + 0xa0
B[0..3]_UDB01_02_F1	UDB01_02_F1	0x6800 + [0..3 * 0x200] + 0xa2
B[0..3]_UDB02_03_F1	UDB02_03_F1	0x6800 + [0..3 * 0x200] + 0xa4
B[0..3]_UDB03_04_F1	UDB03_04_F1	0x6800 + [0..3 * 0x200] + 0xa6
B[0..3]_UDB04_05_F1	UDB04_05_F1	0x6800 + [0..3 * 0x200] + 0xa8
B[0..3]_UDB05_06_F1	UDB05_06_F1	0x6800 + [0..3 * 0x200] + 0xaa
B[0..3]_UDB06_07_F1	UDB06_07_F1	0x6800 + [0..3 * 0x200] + 0xac
B[0..3]_UDB07_08_F1	UDB07_08_F1	0x6800 + [0..3 * 0x200] + 0xae
B[0..3]_UDB08_09_F1	UDB08_09_F1	0x6800 + [0..3 * 0x200] + 0xb0
B[0..3]_UDB09_10_F1	UDB09_10_F1	0x6800 + [0..3 * 0x200] + 0xb2
B[0..3]_UDB10_11_F1	UDB10_11_F1	0x6800 + [0..3 * 0x200] + 0xb4
B[0..3]_UDB11_12_F1	UDB11_12_F1	0x6800 + [0..3 * 0x200] + 0xb6
B[0..3]_UDB12_13_F1	UDB12_13_F1	0x6800 + [0..3 * 0x200] + 0xb8

Register Name	Purpose	Address
B[0..3]_UDB13_14_F1	UDB13_14_F1	0x6800 + [0..3 * 0x200] + 0xba
B[0..3]_UDB14_15_F1	UDB14_15_F1	0x6800 + [0..3 * 0x200] + 0xbc
B[0..3]_UDB00_01_ST	UDB00_01_ST	0x6800 + [0..3 * 0x200] + 0xc0
B[0..3]_UDB01_02_ST	UDB01_02_ST	0x6800 + [0..3 * 0x200] + 0xc2
B[0..3]_UDB02_03_ST	UDB02_03_ST	0x6800 + [0..3 * 0x200] + 0xc4
B[0..3]_UDB03_04_ST	UDB03_04_ST	0x6800 + [0..3 * 0x200] + 0xc6
B[0..3]_UDB04_05_ST	UDB04_05_ST	0x6800 + [0..3 * 0x200] + 0xc8
B[0..3]_UDB05_06_ST	UDB05_06_ST	0x6800 + [0..3 * 0x200] + 0xca
B[0..3]_UDB06_07_ST	UDB06_07_ST	0x6800 + [0..3 * 0x200] + 0xcc
B[0..3]_UDB07_08_ST	UDB07_08_ST	0x6800 + [0..3 * 0x200] + 0xce
B[0..3]_UDB08_09_ST	UDB08_09_ST	0x6800 + [0..3 * 0x200] + 0xd0
B[0..3]_UDB09_10_ST	UDB09_10_ST	0x6800 + [0..3 * 0x200] + 0xd2
B[0..3]_UDB10_11_ST	UDB10_11_ST	0x6800 + [0..3 * 0x200] + 0xd4
B[0..3]_UDB11_12_ST	UDB11_12_ST	0x6800 + [0..3 * 0x200] + 0xd6
B[0..3]_UDB12_13_ST	UDB12_13_ST	0x6800 + [0..3 * 0x200] + 0xd8
B[0..3]_UDB13_14_ST	UDB13_14_ST	0x6800 + [0..3 * 0x200] + 0xda
B[0..3]_UDB14_15_ST	UDB14_15_ST	0x6800 + [0..3 * 0x200] + 0xdc
B[0..3]_UDB00_01_CTL	UDB00_01_CTL	0x6800 + [0..3 * 0x200] + 0xe0
B[0..3]_UDB01_02_CTL	UDB01_02_CTL	0x6800 + [0..3 * 0x200] + 0xe2
B[0..3]_UDB02_03_CTL	UDB02_03_CTL	0x6800 + [0..3 * 0x200] + 0xe4
B[0..3]_UDB03_04_CTL	UDB03_04_CTL	0x6800 + [0..3 * 0x200] + 0xe6
B[0..3]_UDB04_05_CTL	UDB04_05_CTL	0x6800 + [0..3 * 0x200] + 0xe8
B[0..3]_UDB05_06_CTL	UDB05_06_CTL	0x6800 + [0..3 * 0x200] + 0xea
B[0..3]_UDB06_07_CTL	UDB06_07_CTL	0x6800 + [0..3 * 0x200] + 0xec
B[0..3]_UDB07_08_CTL	UDB07_08_CTL	0x6800 + [0..3 * 0x200] + 0xee
B[0..3]_UDB08_09_CTL	UDB08_09_CTL	0x6800 + [0..3 * 0x200] + 0xf0
B[0..3]_UDB09_10_CTL	UDB09_10_CTL	0x6800 + [0..3 * 0x200] + 0xf2
B[0..3]_UDB10_11_CTL	UDB10_11_CTL	0x6800 + [0..3 * 0x200] + 0xf4
B[0..3]_UDB11_12_CTL	UDB11_12_CTL	0x6800 + [0..3 * 0x200] + 0xf6
B[0..3]_UDB12_13_CTL	UDB12_13_CTL	0x6800 + [0..3 * 0x200] + 0xf8
B[0..3]_UDB13_14_CTL	UDB13_14_CTL	0x6800 + [0..3 * 0x200] + 0xfa
B[0..3]_UDB14_15_CTL	UDB14_15_CTL	0x6800 + [0..3 * 0x200] + 0xfc
B[0..3]_UDB00_01_MSK	UDB00_01_MSK	0x6800 + [0..3 * 0x200] + 0x100
B[0..3]_UDB01_02_MSK	UDB01_02_MSK	0x6800 + [0..3 * 0x200] + 0x102
B[0..3]_UDB02_03_MSK	UDB02_03_MSK	0x6800 + [0..3 * 0x200] + 0x104
B[0..3]_UDB03_04_MSK	UDB03_04_MSK	0x6800 + [0..3 * 0x200] + 0x106

Register Name	Purpose	Address
B[0..3]_UDB04_05_MSK	UDB04_05_MSK	0x6800 + [0..3 * 0x200] + 0x108
B[0..3]_UDB05_06_MSK	UDB05_06_MSK	0x6800 + [0..3 * 0x200] + 0x10a
B[0..3]_UDB06_07_MSK	UDB06_07_MSK	0x6800 + [0..3 * 0x200] + 0x10c
B[0..3]_UDB07_08_MSK	UDB07_08_MSK	0x6800 + [0..3 * 0x200] + 0x10e
B[0..3]_UDB08_09_MSK	UDB08_09_MSK	0x6800 + [0..3 * 0x200] + 0x110
B[0..3]_UDB09_10_MSK	UDB09_10_MSK	0x6800 + [0..3 * 0x200] + 0x112
B[0..3]_UDB10_11_MSK	UDB10_11_MSK	0x6800 + [0..3 * 0x200] + 0x114
B[0..3]_UDB11_12_MSK	UDB11_12_MSK	0x6800 + [0..3 * 0x200] + 0x116
B[0..3]_UDB12_13_MSK	UDB12_13_MSK	0x6800 + [0..3 * 0x200] + 0x118
B[0..3]_UDB13_14_MSK	UDB13_14_MSK	0x6800 + [0..3 * 0x200] + 0x11a
B[0..3]_UDB14_15_MSK	UDB14_15_MSK	0x6800 + [0..3 * 0x200] + 0x11c
B[0..3]_UDB00_01_ACTL	UDB00_01_ACTL	0x6800 + [0..3 * 0x200] + 0x120
B[0..3]_UDB01_02_ACTL	UDB01_02_ACTL	0x6800 + [0..3 * 0x200] + 0x122
B[0..3]_UDB02_03_ACTL	UDB02_03_ACTL	0x6800 + [0..3 * 0x200] + 0x124
B[0..3]_UDB03_04_ACTL	UDB03_04_ACTL	0x6800 + [0..3 * 0x200] + 0x126
B[0..3]_UDB04_05_ACTL	UDB04_05_ACTL	0x6800 + [0..3 * 0x200] + 0x128
B[0..3]_UDB05_06_ACTL	UDB05_06_ACTL	0x6800 + [0..3 * 0x200] + 0x12a
B[0..3]_UDB06_07_ACTL	UDB06_07_ACTL	0x6800 + [0..3 * 0x200] + 0x12c
B[0..3]_UDB07_08_ACTL	UDB07_08_ACTL	0x6800 + [0..3 * 0x200] + 0x12e
B[0..3]_UDB08_09_ACTL	UDB08_09_ACTL	0x6800 + [0..3 * 0x200] + 0x130
B[0..3]_UDB09_10_ACTL	UDB09_10_ACTL	0x6800 + [0..3 * 0x200] + 0x132
B[0..3]_UDB10_11_ACTL	UDB10_11_ACTL	0x6800 + [0..3 * 0x200] + 0x134
B[0..3]_UDB11_12_ACTL	UDB11_12_ACTL	0x6800 + [0..3 * 0x200] + 0x136
B[0..3]_UDB12_13_ACTL	UDB12_13_ACTL	0x6800 + [0..3 * 0x200] + 0x138
B[0..3]_UDB13_14_ACTL	UDB13_14_ACTL	0x6800 + [0..3 * 0x200] + 0x13a
B[0..3]_UDB14_15_ACTL	UDB14_15_ACTL	0x6800 + [0..3 * 0x200] + 0x13c
B[0..3]_UDB00_01_MC	UDB00_01_MC	0x6800 + [0..3 * 0x200] + 0x140
B[0..3]_UDB01_02_MC	UDB01_02_MC	0x6800 + [0..3 * 0x200] + 0x142
B[0..3]_UDB02_03_MC	UDB02_03_MC	0x6800 + [0..3 * 0x200] + 0x144
B[0..3]_UDB03_04_MC	UDB03_04_MC	0x6800 + [0..3 * 0x200] + 0x146
B[0..3]_UDB04_05_MC	UDB04_05_MC	0x6800 + [0..3 * 0x200] + 0x148
B[0..3]_UDB05_06_MC	UDB05_06_MC	0x6800 + [0..3 * 0x200] + 0x14a
B[0..3]_UDB06_07_MC	UDB06_07_MC	0x6800 + [0..3 * 0x200] + 0x14c
B[0..3]_UDB07_08_MC	UDB07_08_MC	0x6800 + [0..3 * 0x200] + 0x14e
B[0..3]_UDB08_09_MC	UDB08_09_MC	0x6800 + [0..3 * 0x200] + 0x150
B[0..3]_UDB09_10_MC	UDB09_10_MC	0x6800 + [0..3 * 0x200] + 0x152

Register Name	Purpose	Address
B[0..3]_UDB10_11_MC	UDB10_11_MC	0x6800 + [0..3 * 0x200] + 0x154
B[0..3]_UDB11_12_MC	UDB11_12_MC	0x6800 + [0..3 * 0x200] + 0x156
B[0..3]_UDB12_13_MC	UDB12_13_MC	0x6800 + [0..3 * 0x200] + 0x158
B[0..3]_UDB13_14_MC	UDB13_14_MC	0x6800 + [0..3 * 0x200] + 0x15a
B[0..3]_UDB14_15_MC	UDB14_15_MC	0x6800 + [0..3 * 0x200] + 0x15c
B[0..3]_UDB00_A0_A1	UDB00_A0_A1	0x6800 + [0..3 * 0x200]
B[0..3]_UDB01_A0_A1	UDB01_A0_A1	0x6800 + [0..3 * 0x200] + 0x2
B[0..3]_UDB02_A0_A1	UDB02_A0_A1	0x6800 + [0..3 * 0x200] + 0x4
B[0..3]_UDB03_A0_A1	UDB03_A0_A1	0x6800 + [0..3 * 0x200] + 0x6
B[0..3]_UDB04_A0_A1	UDB04_A0_A1	0x6800 + [0..3 * 0x200] + 0x8
B[0..3]_UDB05_A0_A1	UDB05_A0_A1	0x6800 + [0..3 * 0x200] + 0xa
B[0..3]_UDB06_A0_A1	UDB06_A0_A1	0x6800 + [0..3 * 0x200] + 0xc
B[0..3]_UDB07_A0_A1	UDB07_A0_A1	0x6800 + [0..3 * 0x200] + 0xe
B[0..3]_UDB08_A0_A1	UDB08_A0_A1	0x6800 + [0..3 * 0x200] + 0x10
B[0..3]_UDB09_A0_A1	UDB09_A0_A1	0x6800 + [0..3 * 0x200] + 0x12
B[0..3]_UDB10_A0_A1	UDB10_A0_A1	0x6800 + [0..3 * 0x200] + 0x14
B[0..3]_UDB11_A0_A1	UDB11_A0_A1	0x6800 + [0..3 * 0x200] + 0x16
B[0..3]_UDB12_A0_A1	UDB12_A0_A1	0x6800 + [0..3 * 0x200] + 0x18
B[0..3]_UDB13_A0_A1	UDB13_A0_A1	0x6800 + [0..3 * 0x200] + 0x1a
B[0..3]_UDB14_A0_A1	UDB14_A0_A1	0x6800 + [0..3 * 0x200] + 0x1c
B[0..3]_UDB15_A0_A1	UDB15_A0_A1	0x6800 + [0..3 * 0x200] + 0x1e
B[0..3]_UDB00_D0_D1	UDB00_D0_D1	0x6800 + [0..3 * 0x200] + 0x40
B[0..3]_UDB01_D0_D1	UDB01_D0_D1	0x6800 + [0..3 * 0x200] + 0x42
B[0..3]_UDB02_D0_D1	UDB02_D0_D1	0x6800 + [0..3 * 0x200] + 0x44
B[0..3]_UDB03_D0_D1	UDB03_D0_D1	0x6800 + [0..3 * 0x200] + 0x46
B[0..3]_UDB04_D0_D1	UDB04_D0_D1	0x6800 + [0..3 * 0x200] + 0x48
B[0..3]_UDB05_D0_D1	UDB05_D0_D1	0x6800 + [0..3 * 0x200] + 0x4a
B[0..3]_UDB06_D0_D1	UDB06_D0_D1	0x6800 + [0..3 * 0x200] + 0x4c
B[0..3]_UDB07_D0_D1	UDB07_D0_D1	0x6800 + [0..3 * 0x200] + 0x4e
B[0..3]_UDB08_D0_D1	UDB08_D0_D1	0x6800 + [0..3 * 0x200] + 0x50
B[0..3]_UDB09_D0_D1	UDB09_D0_D1	0x6800 + [0..3 * 0x200] + 0x52
B[0..3]_UDB10_D0_D1	UDB10_D0_D1	0x6800 + [0..3 * 0x200] + 0x54
B[0..3]_UDB11_D0_D1	UDB11_D0_D1	0x6800 + [0..3 * 0x200] + 0x56
B[0..3]_UDB12_D0_D1	UDB12_D0_D1	0x6800 + [0..3 * 0x200] + 0x58
B[0..3]_UDB13_D0_D1	UDB13_D0_D1	0x6800 + [0..3 * 0x200] + 0x5a
B[0..3]_UDB14_D0_D1	UDB14_D0_D1	0x6800 + [0..3 * 0x200] + 0x5c

Register Name	Purpose	Address
B[0..3]_UDB15_D0_D1	UDB15_D0_D1	0x6800 + [0..3 * 0x200] + 0x5e
B[0..3]_UDB00_F0_F1	UDB00_F0_F1	0x6800 + [0..3 * 0x200] + 0x80
B[0..3]_UDB01_F0_F1	UDB01_F0_F1	0x6800 + [0..3 * 0x200] + 0x82
B[0..3]_UDB02_F0_F1	UDB02_F0_F1	0x6800 + [0..3 * 0x200] + 0x84
B[0..3]_UDB03_F0_F1	UDB03_F0_F1	0x6800 + [0..3 * 0x200] + 0x86
B[0..3]_UDB04_F0_F1	UDB04_F0_F1	0x6800 + [0..3 * 0x200] + 0x88
B[0..3]_UDB05_F0_F1	UDB05_F0_F1	0x6800 + [0..3 * 0x200] + 0x8a
B[0..3]_UDB06_F0_F1	UDB06_F0_F1	0x6800 + [0..3 * 0x200] + 0x8c
B[0..3]_UDB07_F0_F1	UDB07_F0_F1	0x6800 + [0..3 * 0x200] + 0x8e
B[0..3]_UDB08_F0_F1	UDB08_F0_F1	0x6800 + [0..3 * 0x200] + 0x90
B[0..3]_UDB09_F0_F1	UDB09_F0_F1	0x6800 + [0..3 * 0x200] + 0x92
B[0..3]_UDB10_F0_F1	UDB10_F0_F1	0x6800 + [0..3 * 0x200] + 0x94
B[0..3]_UDB11_F0_F1	UDB11_F0_F1	0x6800 + [0..3 * 0x200] + 0x96
B[0..3]_UDB12_F0_F1	UDB12_F0_F1	0x6800 + [0..3 * 0x200] + 0x98
B[0..3]_UDB13_F0_F1	UDB13_F0_F1	0x6800 + [0..3 * 0x200] + 0x9a
B[0..3]_UDB14_F0_F1	UDB14_F0_F1	0x6800 + [0..3 * 0x200] + 0x9c
B[0..3]_UDB15_F0_F1	UDB15_F0_F1	0x6800 + [0..3 * 0x200] + 0x9e
B[0..3]_UDB00_ST_CTL	UDB00_ST_CTL	0x6800 + [0..3 * 0x200] + 0xc0
B[0..3]_UDB01_ST_CTL	UDB01_ST_CTL	0x6800 + [0..3 * 0x200] + 0xc2
B[0..3]_UDB02_ST_CTL	UDB02_ST_CTL	0x6800 + [0..3 * 0x200] + 0xc4
B[0..3]_UDB03_ST_CTL	UDB03_ST_CTL	0x6800 + [0..3 * 0x200] + 0xc6
B[0..3]_UDB04_ST_CTL	UDB04_ST_CTL	0x6800 + [0..3 * 0x200] + 0xc8
B[0..3]_UDB05_ST_CTL	UDB05_ST_CTL	0x6800 + [0..3 * 0x200] + 0xca
B[0..3]_UDB06_ST_CTL	UDB06_ST_CTL	0x6800 + [0..3 * 0x200] + 0xcc
B[0..3]_UDB07_ST_CTL	UDB07_ST_CTL	0x6800 + [0..3 * 0x200] + 0xce
B[0..3]_UDB08_ST_CTL	UDB08_ST_CTL	0x6800 + [0..3 * 0x200] + 0xd0
B[0..3]_UDB09_ST_CTL	UDB09_ST_CTL	0x6800 + [0..3 * 0x200] + 0xd2
B[0..3]_UDB10_ST_CTL	UDB10_ST_CTL	0x6800 + [0..3 * 0x200] + 0xd4
B[0..3]_UDB11_ST_CTL	UDB11_ST_CTL	0x6800 + [0..3 * 0x200] + 0xd6
B[0..3]_UDB12_ST_CTL	UDB12_ST_CTL	0x6800 + [0..3 * 0x200] + 0xd8
B[0..3]_UDB13_ST_CTL	UDB13_ST_CTL	0x6800 + [0..3 * 0x200] + 0xda
B[0..3]_UDB14_ST_CTL	UDB14_ST_CTL	0x6800 + [0..3 * 0x200] + 0xdc
B[0..3]_UDB15_ST_CTL	UDB15_ST_CTL	0x6800 + [0..3 * 0x200] + 0xde
B[0..3]_UDB00_MSK_ACTL	UDB00_MSK_ACTL	0x6800 + [0..3 * 0x200] + 0x100
B[0..3]_UDB01_MSK_ACTL	UDB01_MSK_ACTL	0x6800 + [0..3 * 0x200] + 0x102
B[0..3]_UDB02_MSK_ACTL	UDB02_MSK_ACTL	0x6800 + [0..3 * 0x200] + 0x104

Register Name	Purpose	Address
B[0..3]_UDB03_MSK_ACTL	UDB03_MSK_ACTL	0x6800 + [0..3 * 0x200] + 0x106
B[0..3]_UDB04_MSK_ACTL	UDB04_MSK_ACTL	0x6800 + [0..3 * 0x200] + 0x108
B[0..3]_UDB05_MSK_ACTL	UDB05_MSK_ACTL	0x6800 + [0..3 * 0x200] + 0x10a
B[0..3]_UDB06_MSK_ACTL	UDB06_MSK_ACTL	0x6800 + [0..3 * 0x200] + 0x10c
B[0..3]_UDB07_MSK_ACTL	UDB07_MSK_ACTL	0x6800 + [0..3 * 0x200] + 0x10e
B[0..3]_UDB08_MSK_ACTL	UDB08_MSK_ACTL	0x6800 + [0..3 * 0x200] + 0x110
B[0..3]_UDB09_MSK_ACTL	UDB09_MSK_ACTL	0x6800 + [0..3 * 0x200] + 0x112
B[0..3]_UDB10_MSK_ACTL	UDB10_MSK_ACTL	0x6800 + [0..3 * 0x200] + 0x114
B[0..3]_UDB11_MSK_ACTL	UDB11_MSK_ACTL	0x6800 + [0..3 * 0x200] + 0x116
B[0..3]_UDB12_MSK_ACTL	UDB12_MSK_ACTL	0x6800 + [0..3 * 0x200] + 0x118
B[0..3]_UDB13_MSK_ACTL	UDB13_MSK_ACTL	0x6800 + [0..3 * 0x200] + 0x11a
B[0..3]_UDB14_MSK_ACTL	UDB14_MSK_ACTL	0x6800 + [0..3 * 0x200] + 0x11c
B[0..3]_UDB15_MSK_ACTL	UDB15_MSK_ACTL	0x6800 + [0..3 * 0x200] + 0x11e
B[0..3]_UDB00_MC_00	UDB00_MC_00	0x6800 + [0..3 * 0x200] + 0x140
B[0..3]_UDB01_MC_00	UDB01_MC_00	0x6800 + [0..3 * 0x200] + 0x142
B[0..3]_UDB02_MC_00	UDB02_MC_00	0x6800 + [0..3 * 0x200] + 0x144
B[0..3]_UDB03_MC_00	UDB03_MC_00	0x6800 + [0..3 * 0x200] + 0x146
B[0..3]_UDB04_MC_00	UDB04_MC_00	0x6800 + [0..3 * 0x200] + 0x148
B[0..3]_UDB05_MC_00	UDB05_MC_00	0x6800 + [0..3 * 0x200] + 0x14a
B[0..3]_UDB06_MC_00	UDB06_MC_00	0x6800 + [0..3 * 0x200] + 0x14c
B[0..3]_UDB07_MC_00	UDB07_MC_00	0x6800 + [0..3 * 0x200] + 0x14e
B[0..3]_UDB08_MC_00	UDB08_MC_00	0x6800 + [0..3 * 0x200] + 0x150
B[0..3]_UDB09_MC_00	UDB09_MC_00	0x6800 + [0..3 * 0x200] + 0x152
B[0..3]_UDB10_MC_00	UDB10_MC_00	0x6800 + [0..3 * 0x200] + 0x154
B[0..3]_UDB11_MC_00	UDB11_MC_00	0x6800 + [0..3 * 0x200] + 0x156
B[0..3]_UDB12_MC_00	UDB12_MC_00	0x6800 + [0..3 * 0x200] + 0x158
B[0..3]_UDB13_MC_00	UDB13_MC_00	0x6800 + [0..3 * 0x200] + 0x15a
B[0..3]_UDB14_MC_00	UDB14_MC_00	0x6800 + [0..3 * 0x200] + 0x15c
B[0..3]_UDB15_MC_00	UDB15_MC_00	0x6800 + [0..3 * 0x200] + 0x15e
PHUB_CFG	PHUB Configuration	0x7000
PHUB_ERR	PHUB Error Detection	0x7004
PHUB_ERR_ADR	PHUB Error Address	0x7008
PHUB_CH[0..23]_BASIC_CFG	Channel Basic Configuration Register	0x7010 + [0..23 * 0x10]
PHUB_CH[0..23]_ACTION	Channel Action	0x7010 + [0..23 * 0x10] + 0x4
PHUB_CH[0..23]_BASIC_STATUS	Channel Basic Status Register	0x7010 + [0..23 * 0x10] + 0x8
PHUB_CFGMEM[0..23]_CFG0	PHUB Channel Configuration Register 0	0x7600 + [0..23 * 0x8]

Register Name	Purpose	Address
PHUB_CFGMEM[0..23]_CFG1	PHUB Channel Configuration Register 1	0x7600 + [0..23 * 0x8] + 0x4
PHUB_TDMEM[0..127]_ORIG_TD0	PHUB Original Transaction Descriptor 0	0x7800 + [0..127 * 0x8]
PHUB_TDMEM[0..127]_ORIG_TD1	PHUB Original Transaction Descriptor 0	0x7800 + [0..127 * 0x8] + 0x4
EE_DATA[0..2047]	EEPROM Memory	0x8000 + [0..2047 * 0x1]
CAN[0..0]_CSR_INT_SR	INT_SR	0xa000
CAN[0..0]_CSR_INT_EN	INT_EN	0xa004
CAN[0..0]_CSR_BUF_SR	BUF_SR	0xa008
CAN[0..0]_CSR_ERR_SR	ERR_SR	0xa00c
CAN[0..0]_CSR_CMD	CMD	0xa010
CAN[0..0]_CSR_CFG	CFG	0xa014
CAN[0..0]_TX[0..7]_CMD	TXCMD	0xa020 + [0..7 * 0x10]
CAN[0..0]_TX[0..7]_ID	TXID	0xa020 + [0..7 * 0x10] + 0x4
CAN[0..0]_TX[0..7]_DH	TXDH	0xa020 + [0..7 * 0x10] + 0x8
CAN[0..0]_TX[0..7]_DL	TXDL	0xa020 + [0..7 * 0x10] + 0xc
CAN[0..0]_RX[0..15]_CMD	RXCMD	0xa0a0 + [0..15 * 0x20]
CAN[0..0]_RX[0..15]_ID	RXID	0xa0a0 + [0..15 * 0x20] + 0x4
CAN[0..0]_RX[0..15]_DH	RXDH	0xa0a0 + [0..15 * 0x20] + 0x8
CAN[0..0]_RX[0..15]_DL	RXDL	0xa0a0 + [0..15 * 0x20] + 0xc
CAN[0..0]_RX[0..15]_AMR	RXAMR	0xa0a0 + [0..15 * 0x20] + 0x10
CAN[0..0]_RX[0..15]_ACR	RXACR	0xa0a0 + [0..15 * 0x20] + 0x14
CAN[0..0]_RX[0..15]_AMRD	RXAMRD	0xa0a0 + [0..15 * 0x20] + 0x18
CAN[0..0]_RX[0..15]_ACRD	RXACRD	0xa0a0 + [0..15 * 0x20] + 0x1c
DFB[0..0]_DPA_SRAM_DATA[0..127]	Data RAM A	0xc000 + [0..127 * 0x4]
DFB[0..0]_DPB_SRAM_DATA[0..127]	DFB Data RAM B	0xc200 + [0..127 * 0x4]
DFB[0..0]_CSA_SRAM_DATA[0..63]	DFB Control Store A	0xc400 + [0..63 * 0x4]
DFB[0..0]_CSB_SRAM_DATA[0..63]	DFB Control Store B	0xc500 + [0..63 * 0x4]
DFB[0..0]_FSM_SRAM_DATA[0..63]	DFB Code Store B	0xc600 + [0..63 * 0x4]
DFB[0..0]_ACU_SRAM_DATA[0..15]	DFB Address Store	0xc700 + [0..15 * 0x4]
DFB[0..0]_CR	DFB Command Register	0xc780
DFB[0..0]_SR	DFB Status Register	0xc784
DFB[0..0]_RAM_EN	DFB RAM Enable Register	0xc788
DFB[0..0]_RAM_DIR	DFB RAM Direction Register	0xc78c
DFB[0..0]_SEMA	DFB Semaphore Register	0xc790
DFB[0..0]_DSI_CTRL	DFB Global Control Register	0xc794
DFB[0..0]_INT_CTRL	DFB Interrupt Control Register	0xc798
DFB[0..0]_DMA_CTRL	DFB DMAREQ Control Register	0xc79c

Register Name	Purpose	Address
DFB[0..0]_STAGEA	DFB Low Byte Staging Register A	0xc7a0
DFB[0..0]_STAGEAM	DFB Middle Byte Staging Register A	0xc7a1
DFB[0..0]_STAGEAH	DFB High Byte Staging Register A	0xc7a2
DFB[0..0]_STAGEB	DFB Low Byte Staging Register B	0xc7a4
DFB[0..0]_STAGEBM	DFB Middle Byte Staging Register B	0xc7a5
DFB[0..0]_STAGEBH	DFB High Byte Staging Register B	0xc7a6
DFB[0..0]_HOLDA	DFB Low Byte Holding Register A	0xc7a8
DFB[0..0]_HOLDAM	DFB Middle Byte Holding Register A	0xc7a9
DFB[0..0]_HOLDAH	DFB High Byte Holding Register A	0xc7aa
DFB[0..0]_HOLDAS	DFB Holding Register A Sign Extension	0xc7ab
DFB[0..0]_HOLDB	DFB Low Byte Holding Register B	0xc7ac
DFB[0..0]_HOLDBM	DFB Middle Byte Holding Register B	0xc7ad
DFB[0..0]_HOLDBH	DFB High Byte Holding Register B	0xc7ae
DFB[0..0]_HOLDBS	DFB Holding Register B Sign Extension	0xc7af
DFB[0..0]_COHER	DFB Coherency Register	0xc7b0
DFB[0..0]_DALIGN	DFB Data Alignment Register	0xc7b4
SWV_ITM_SPR_DATA[0..31]	Stimulus Port Register	0xe000 + [0..31 * 0x4]
SWV_ITM_TER	Trace Enable Register	0xee00
SWV_ITM_TTR	Trace Triger Register	0xee20
SWV_ITM_CR	Control Register	0xee80
SWV_ITM_SCR	Synchronization Control Register	0xee90
SWV_ITM_ITTOAR	Integration Test Trigger Out Acknowledge Register	0xeee4
SWV_ITM_ITTOR	Integration Test Trigger Out Register	0xeee8
SWV_ITM_ITDR0	Integration Test ATB Data Register 0	0xeeec
SWV_ITM_ITCR2	Integration Test ATB Control Register 2	0xeef0
SWV_ITM_ITCR1	Integration Test ATB Control Register 1	0xeef4
SWV_ITM_ITCR0	Integration Test ATB Control Register 0	0xeef8
SWV_SWO_SSPS	Supported Synchronous Port Size Register	0xf000
SWV_SWO_CSPS	Current Synchronous Port Size Register	0xf004
SWV_SWO_CAOSD	Current Output Divisor Register	0xf010
SWV_SWO_SPP	Selected Pin Protocol Register	0xf0f0
SWV_SWO_STM	Supported Trigger Modes Registers	0xf100
SWV_SWO_STPM	Supported Test Pattern and Modes Registers	0xf200
SWV_SWO_FFS	Formatter and Flush Status Register	0xf300
SWV_SWO_FFC	Formatter and Flush Control Register	0xf304
SWV_SWO_ITDR0	Integration Test ATB Data Register 0	0xfeec

Register Name	Purpose	Address
SWV_SWO_ITCR2	Integration Test ATB Control Register 2	0xfef0
SWV_SWO_ITCR0	Integration Test ATB Control Register 0	0xfef8
SWV_SWO_ITMCR	Integration Mode Control Register	0xff00
SWV_SWO_CTS	Claim Tag Set Register	0xffa0
SWV_SWO_CTC	Claim Tag Clear Register	0xffa4
SWV_SWO_LA	Lock Access Register	0xffb0
SWV_SWO_LS	Lock Status Register	0xffb4
SWV_SWO_AS	Authentication Status Register	0xffb8
SWV_SWO_DID	Device ID Register	0xffc8
SWV_SWO_DTI	Device Type Identifier Register	0xffcc
B[0..3]_P[0..7]_U[0..1]_PLD_IT[0..11]	PLD_IT	(((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80]) + [0..11 * 0x4]
B[0..3]_P[0..7]_U[0..1]_PLD_ORT[0..3]	PLD_ORT	(((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80]) + 0x30 + [0..3 * 0x2]
B[0..3]_P[0..7]_U[0..1]_MC_CFG_CEN_CONST	MC_CFG_CEN_CONST	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x38
B[0..3]_P[0..7]_U[0..1]_MC_CFG_XORFB	MC_CFG_XORFB	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x3a
B[0..3]_P[0..7]_U[0..1]_MC_CFG_SET_RESET	MC_CFG_SET_RESET	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x3c
B[0..3]_P[0..7]_U[0..1]_MC_CFG_BYPASS	MC_CFG_BYPASS	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x3e
B[0..3]_P[0..7]_U[0..1]_CFG0	CFG0	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x40
B[0..3]_P[0..7]_U[0..1]_CFG1	CFG1	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x41
B[0..3]_P[0..7]_U[0..1]_CFG2	CFG2	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x42
B[0..3]_P[0..7]_U[0..1]_CFG3	CFG3	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x43
B[0..3]_P[0..7]_U[0..1]_CFG4	CFG4	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x44
B[0..3]_P[0..7]_U[0..1]_CFG5	CFG5	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x45
B[0..3]_P[0..7]_U[0..1]_CFG6	CFG6	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x46

Register Name	Purpose	Address
B[0..3]_P[0..7]_U[0..1]_CFG7	CFG7	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x47
B[0..3]_P[0..7]_U[0..1]_CFG8	CFG8	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x48
B[0..3]_P[0..7]_U[0..1]_CFG9	CFG9	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x49
B[0..3]_P[0..7]_U[0..1]_CFG10	CFG10	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x4a
B[0..3]_P[0..7]_U[0..1]_CFG11	CFG11	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x4b
B[0..3]_P[0..7]_U[0..1]_CFG12	CFG12	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x4c
B[0..3]_P[0..7]_U[0..1]_CFG13	CFG13	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x4d
B[0..3]_P[0..7]_U[0..1]_CFG14	CFG14	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x4e
B[0..3]_P[0..7]_U[0..1]_CFG15	CFG15	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x4f
B[0..3]_P[0..7]_U[0..1]_CFG16	CFG16	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x50
B[0..3]_P[0..7]_U[0..1]_CFG17	CFG17	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x51
B[0..3]_P[0..7]_U[0..1]_CFG18	CFG18	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x52
B[0..3]_P[0..7]_U[0..1]_CFG19	CFG19	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x53
B[0..3]_P[0..7]_U[0..1]_CFG20	CFG20	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x54
B[0..3]_P[0..7]_U[0..1]_CFG21	CFG21	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x55
B[0..3]_P[0..7]_U[0..1]_CFG22	CFG22	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x56
B[0..3]_P[0..7]_U[0..1]_CFG23	CFG23	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x57
B[0..3]_P[0..7]_U[0..1]_CFG24	CFG24	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x58

Register Name	Purpose	Address
B[0..3]_P[0..7]_U[0..1]_CFG25	CFG25	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x59
B[0..3]_P[0..7]_U[0..1]_CFG26	CFG26	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x5a
B[0..3]_P[0..7]_U[0..1]_CFG27	CFG27	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x5b
B[0..3]_P[0..7]_U[0..1]_CFG28	CFG28	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x5c
B[0..3]_P[0..7]_U[0..1]_CFG29	CFG29	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x5d
B[0..3]_P[0..7]_U[0..1]_CFG30	CFG30	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x5e
B[0..3]_P[0..7]_U[0..1]_CFG31	CFG31	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80] + 0x5f
B[0..3]_P[0..7]_U[0..1]_DCFG[0..7]	DCFG	(((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + [0..1 * 0x80]) + 0x60 + [0..7 * 0x2]
B[0..3]_P[0..7]_ROUTE_HC[0..127]	HC	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + 0x100 + [0..127 * 0x1]
B[0..3]_P[0..7]_ROUTE_HV_L[0..15]	HV_L	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + 0x180 + [0..15 * 0x1]
B[0..3]_P[0..7]_ROUTE_HS[0..23]	HS	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + 0x190 + [0..23 * 0x1]
B[0..3]_P[0..7]_ROUTE_HV_R[0..15]	HV_R	((0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200]) + 0x1a8 + [0..15 * 0x1]
B[0..3]_P[0..7]_ROUTE_PLD0IN0	PLD0IN0	(0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1c0
B[0..3]_P[0..7]_ROUTE_PLD0IN1	PLD0IN1	(0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1c2
B[0..3]_P[0..7]_ROUTE_PLD0IN2	PLD0IN2	(0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1c4
B[0..3]_P[0..7]_ROUTE_PLD1IN0	PLD1IN0	(0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1ca
B[0..3]_P[0..7]_ROUTE_PLD1IN1	PLD1IN1	(0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1cc
B[0..3]_P[0..7]_ROUTE_PLD1IN2	PLD1IN2	(0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1ce
B[0..3]_P[0..7]_ROUTE_DPIN0	DPIN0	(0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1d0
B[0..3]_P[0..7]_ROUTE_DPIN1	DPIN1	(0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1d2
B[0..3]_P[0..7]_ROUTE_SCIN	SCIN	(0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1d6

Register Name	Purpose	Address
B[0..3]_P[0..7]_ROUTE_SCIOIN	SCIOIN	(0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1d8
B[0..3]_P[0..7]_ROUTE_RCIN	RCIN	(0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1de
B[0..3]_P[0..7]_ROUTE_VS0	VS0	(0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1e0
B[0..3]_P[0..7]_ROUTE_VS1	VS1	(0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1e2
B[0..3]_P[0..7]_ROUTE_VS2	VS2	(0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1e4
B[0..3]_P[0..7]_ROUTE_VS3	VS3	(0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1e6
B[0..3]_P[0..7]_ROUTE_VS4	VS4	(0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1e8
B[0..3]_P[0..7]_ROUTE_VS5	VS5	(0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1ea
B[0..3]_P[0..7]_ROUTE_VS6	VS6	(0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1ec
B[0..3]_P[0..7]_ROUTE_VS7	VS7	(0x10000 + [0..3 * 0x1000]) + [0..7 * 0x200] + 0x1ee
DSI[0..15]_HC[0..127]	HC	(0x14000 + [0..15 * 0x100]) + [0..127 * 0x1]
DSI[0..15]_HV_L[0..15]	HV_L	(0x14000 + [0..15 * 0x100]) + 0x80 + [0..15 * 0x1]
DSI[0..15]_HS[0..23]	HS	(0x14000 + [0..15 * 0x100]) + 0x90 + [0..23 * 0x1]
DSI[0..15]_HV_R[0..15]	HV_R	(0x14000 + [0..15 * 0x100]) + 0xa8 + [0..15 * 0x1]
DSI[0..15]_DSIINP0	DSIINP0	0x14000 + [0..15 * 0x100] + 0xc0
DSI[0..15]_DSIINP1	DSIINP1	0x14000 + [0..15 * 0x100] + 0xc2
DSI[0..15]_DSIINP2	DSIINP2	0x14000 + [0..15 * 0x100] + 0xc4
DSI[0..15]_DSIINP3	DSIINP3	0x14000 + [0..15 * 0x100] + 0xc6
DSI[0..15]_DSIINP4	DSIINP4	0x14000 + [0..15 * 0x100] + 0xc8
DSI[0..15]_DSIINP5	DSIINP5	0x14000 + [0..15 * 0x100] + 0xca
DSI[0..15]_DSIOUTP0	DSIOUTP0	0x14000 + [0..15 * 0x100] + 0xcc
DSI[0..15]_DSIOUTP1	DSIOUTP1	0x14000 + [0..15 * 0x100] + 0xce
DSI[0..15]_DSIOUTP2	DSIOUTP2	0x14000 + [0..15 * 0x100] + 0xd0
DSI[0..15]_DSIOUTP3	DSIOUTP3	0x14000 + [0..15 * 0x100] + 0xd2
DSI[0..15]_DSIOUTT0	DSIOUTT0	0x14000 + [0..15 * 0x100] + 0xd4
DSI[0..15]_DSIOUTT1	DSIOUTT1	0x14000 + [0..15 * 0x100] + 0xd6
DSI[0..15]_DSIOUTT2	DSIOUTT2	0x14000 + [0..15 * 0x100] + 0xd8
DSI[0..15]_DSIOUTT3	DSIOUTT3	0x14000 + [0..15 * 0x100] + 0xda
DSI[0..15]_DSIOUTT4	DSIOUTT4	0x14000 + [0..15 * 0x100] + 0xdc

Register Name	Purpose	Address
DSI[0..15]_DSIOUTT5	DSIOUTT5	0x14000 + [0..15 * 0x100] + 0xde
DSI[0..15]_VS0	VS0	0x14000 + [0..15 * 0x100] + 0xe0
DSI[0..15]_VS1	VS1	0x14000 + [0..15 * 0x100] + 0xe2
DSI[0..15]_VS2	VS2	0x14000 + [0..15 * 0x100] + 0xe4
DSI[0..15]_VS3	VS3	0x14000 + [0..15 * 0x100] + 0xe6
DSI[0..15]_VS4	VS4	0x14000 + [0..15 * 0x100] + 0xe8
DSI[0..15]_VS5	VS5	0x14000 + [0..15 * 0x100] + 0xea
DSI[0..15]_VS6	VS6	0x14000 + [0..15 * 0x100] + 0xec
DSI[0..15]_VS7	VS7	0x14000 + [0..15 * 0x100] + 0xee
BCTL[0..3]_MDCLK_EN	MDCLK_EN	0x15000 + [0..3 * 0x10]
BCTL[0..3]_MBCLK_EN	MBCLK_EN	0x15000 + [0..3 * 0x10] + 0x1
BCTL[0..3]_WAIT_CFG	WAIT_CFG	0x15000 + [0..3 * 0x10] + 0x2
BCTL[0..3]_BANK_CTL	BANK_CTL	0x15000 + [0..3 * 0x10] + 0x3
BCTL[0..3]_DCLK_EN0	DCLK_EN	0x15000 + [0..3 * 0x10] + 0x8
BCTL[0..3]_BCLK_EN0	BCLK_EN	0x15000 + [0..3 * 0x10] + 0x9
BCTL[0..3]_DCLK_EN1	DCLK_EN	0x15000 + [0..3 * 0x10] + 0xa
BCTL[0..3]_BCLK_EN1	BCLK_EN	0x15000 + [0..3 * 0x10] + 0xb
BCTL[0..3]_DCLK_EN2	DCLK_EN	0x15000 + [0..3 * 0x10] + 0xc
BCTL[0..3]_BCLK_EN2	BCLK_EN	0x15000 + [0..3 * 0x10] + 0xd
BCTL[0..3]_DCLK_EN3	DCLK_EN	0x15000 + [0..3 * 0x10] + 0xe
BCTL[0..3]_BCLK_EN3	BCLK_EN	0x15000 + [0..3 * 0x10] + 0xf
IDMUX_IRQ_CTL[0..7]	Control Register IRQ_CTL	0x15100 + [0..7 * 0x1]
IDMUX_DRQ_CTL[0..5]	Configuration Register DRQ_CTL	0x15110 + [0..5 * 0x1]
IRAM_IRAM_L_DATA_RAM_L[0..127]	Internal Data RAM	0x50000 + [0..127 * 0x1]
IRAM_IRAM_H_DATA_RAM_H[0..127]	Internal Data RAM	0x50080 + [0..127 * 0x1]
SFR_REGS_SP	Stack Pointer	0x50181
SFR_REGS_DPL	Data Pointer 0 Low	0x50182
SFR_REGS_DPH	Data Pointer 0 High	0x50183
SFR_REGS_DPL1	Data Pointer 1 Low	0x50184
SFR_REGS_DPH1	Data Pointer 1 High	0x50185
SFR_REGS_DPS	Data pointer select register	0x50186
SFR_REGS_DPX	Data Pointer Extended 0 Register	0x50193
SFR_REGS_DPX1	Data Pointer Extended 1 Register	0x50195
SFR_REGS_P2	P2 read-write Register	0x501a0
SFR_REGS_IE	Interrupt Enable Register	0x501a8
SFR_REGS_PSW	Program Status Word Register	0x501d0

Register Name	Purpose	Address
SFR_REGS_ACC	Accumulator register	0x501e0
SFR_REGS_MXAX	MOVX @Ri extended Register	0x501ea
SFR_REGS_B	B Register	0x501f0
SFR_USER_GPIO0	GPIO0 Register	0x50180
SFR_USER_GPIRD0	GPIRD0 Register	0x50189
SFR_USER_GPIO0_SEL	GPIO0_SEL Register	0x5018a
SFR_USER_GPIO1	GPIO1 Register	0x50190
SFR_USER_GPIRD1	GPIRD1 Register	0x50191
SFR_USER_GPIO2	GPIO2 Register	0x50198
SFR_USER_GPIRD2	GPIRD2 Register	0x50199
SFR_USER_GPIO2_SEL	GPIO2_SEL Register	0x5019a
SFR_USER_GPIO1_SEL	GPIO1_SEL Register	0x501a2
SFR_USER_GPIO3	GPIO3 Register	0x501b0
SFR_USER_GPIRD3	GPIRD3 Register	0x501b1
SFR_USER_GPIO3_SEL	GPIO3_SEL Register	0x501b2
SFR_USER_GPIO4	GPIO4 Register	0x501c0
SFR_USER_GPIRD4	GPIRD4 Register	0x501c1
SFR_USER_GPIO4_SEL	GPIO4_SEL Register	0x501c2
SFR_USER_GPIO5	GPIO5 Register	0x501c8
SFR_USER_GPIRD5	GPIRD5 Register	0x501c9
SFR_USER_GPIO5_SEL	GPIO5_SEL Register	0x501ca
SFR_USER_GPIO6	GPIO6 Register	0x501d8
SFR_USER_GPIRD6	GPIRD6 Register	0x501d9
SFR_USER_GPIO6_SEL	GPIO6_SEL Register	0x501da
SFR_USER_GPIO12	GPIO12 Register	0x501e8
SFR_USER_GPIRD12	GPIRD12 Register	0x501e9
SFR_USER_GPIO12_SEL	GPIO12_SEL Register	0x501f2
SFR_USER_GPIO15	GPIO15 Register	0x501f8
SFR_USER_GPIRD15	GPIRD15 Register	0x501f9
SFR_USER_GPIO15_SEL	GPIO15_SEL Register	0x501fa
SFR_SPACE_RSVD[0..255]	Placeholder Memory Space	0x50100 + [0..255 * 0x1]
DOC_DBG_CTRL	Debug Control Register	0x50220
DOC_PA_BKPT0	Program Address Breakpoint Register 0	0x50224
DOC_PA_BKPT1	Program Address Breakpoint Register 1	0x50228
DOC_PA_BKPT2	Program Address Breakpoint Register 2	0x5022c
DOC_PA_BKPT3	Program Address Breakpoint Register 3	0x50230

Register Name	Purpose	Address
DOC_PA_BKPT4	Program Address Breakpoint Register 4	0x50234
DOC_PA_BKPT5	Program Address Breakpoint Register 5	0x50238
DOC_PA_BKPT6	Program Address Breakpoint Register 6	0x5023c
DOC_PA_BKPT7	Program Address Breakpoint Register 7	0x50240
DOC_MEM_BKPT	Memory Breakpoint Register	0x50244
DOC_BKPT_CFG	Breakpoint Configuration Register	0x50248
DOC_BKPTCS	Breakpoint Chain Status	0x5024a
DOC_TRC_CFG	Trace Configuration Register	0x5024c
DOC_PC	Program Counter	0x5024e
DOC_CPU_RST	CPU reset	0x50250
DOC_ENTR_TS	Entry Timestamp	0x50254
DOC_EXIT_TS	Exit Timestamp	0x50258
FLSHID_RSVD[0..127]	RSVD	0xc0000 + [0..127 * 0x1]
FLSHID_CUST_MDATA[0..127]	Customer Meta Data	0xc0080 + [0..127 * 0x1]
FLSHID_CUST_TABLES_Y_LOC	Y location	0xc0100
FLSHID_CUST_TABLES_X_LOC	X location	0xc0101
FLSHID_CUST_TABLES_WAFER_NUM	Wafer Number	0xc0102
FLSHID_CUST_TABLES_LOT_LSB	Lot Number LSB	0xc0103
FLSHID_CUST_TABLES_LOT_MSB	Lot Number MSB	0xc0104
FLSHID_CUST_TABLES_WRK_WK	Work Week	0xc0105
FLSHID_CUST_TABLES_FAB_YR	Fab/Yr	0xc0106
FLSHID_CUST_TABLES_MINOR	Minor Part Number	0xc0107
FLSHID_CUST_TABLES_IMO_3MHZ	IMO Trim - 3 MHz	0xc0108
FLSHID_CUST_TABLES_IMO_6MHZ	IMO Trim - 6 MHz	0xc0109
FLSHID_CUST_TABLES_IMO_12MHZ	IMO Trim - 12 MHz	0xc010a
FLSHID_CUST_TABLES_IMO_24MHZ	IMO Trim - 24 MHz	0xc010b
FLSHID_CUST_TABLES_IMO_67MHZ	IMO Trim - 67 MHz	0xc010c
FLSHID_CUST_TABLES_IMO_80MHZ	IMO Trim - 80 MHz	0xc010d
FLSHID_CUST_TABLES_IMO_92MHZ	IMO Trim - 92 MHz	0xc010e
FLSHID_CUST_TABLES_IMO_USB	IMO Trim - USB Mode	0xc010f
FLSHID_CUST_TABLES_CMP0_TR0_HS	CMP0_TR0 High Speed	0xc0110
FLSHID_CUST_TABLES_CMP1_TR0_HS	CMP1_TR0 High Speed	0xc0111
FLSHID_CUST_TABLES_CMP2_TR0_HS	CMP2_TR0 High Speed	0xc0112
FLSHID_CUST_TABLES_CMP3_TR0_HS	CMP3_TR0 High Speed	0xc0113
FLSHID_CUST_TABLES_CMP0_TR1_HS	CMP0_TR1 High Speed	0xc0114
FLSHID_CUST_TABLES_CMP1_TR1_HS	CMP1_TR1 High Speed	0xc0115

Register Name	Purpose	Address
FLSHID_CUST_TABLES_CMP2_TR1_HS	CMP2_TR1 High Speed	0xc0116
FLSHID_CUST_TABLES_CMP3_TR1_HS	CMP3_TR1 High Speed	0xc0117
FLSHID_CUST_TABLES_DEC_M1	Decimator Trim - Mode 1	0xc0118
FLSHID_CUST_TABLES_DEC_M2	Decimator Trim - mode 2	0xc0119
FLSHID_CUST_TABLES_DEC_M3	Decimator Trim - mode 3	0xc011a
FLSHID_CUST_TABLES_DEC_M4	Decimator Trim - mode 4	0xc011b
FLSHID_CUST_TABLES_DEC_M5	Decimator Trim - mode 5	0xc011c
FLSHID_CUST_TABLES_DEC_M6	Decimator Trim - mode 6	0xc011d
FLSHID_CUST_TABLES_DEC_M7	Decimator Trim - Mode 7	0xc011e
FLSHID_CUST_TABLES_DEC_M8	Decimator Trim - Mode 8	0xc011f
FLSHID_CUST_TABLES_DAC0_M1	DAC0_TR Trim - Mode 1	0xc0120
FLSHID_CUST_TABLES_DAC0_M2	DAC0_TR Trim - mode 2	0xc0121
FLSHID_CUST_TABLES_DAC0_M3	DAC0_TR Trim - mode 3	0xc0122
FLSHID_CUST_TABLES_DAC0_M4	DAC0_TR Trim - mode 4	0xc0123
FLSHID_CUST_TABLES_DAC0_M5	DAC0_TR Trim - mode 5	0xc0124
FLSHID_CUST_TABLES_DAC0_M6	DAC0_TR Trim - mode 6	0xc0125
FLSHID_CUST_TABLES_DAC0_M7	DAC0_TR Trim - mode 7	0xc0126
FLSHID_CUST_TABLES_DAC0_M8	DAC0_TR Trim - mode 8	0xc0127
FLSHID_CUST_TABLES_DAC2_M1	DAC2_TR Trim - Mode 1	0xc0128
FLSHID_CUST_TABLES_DAC2_M2	DAC2_TR Trim - mode 2	0xc0129
FLSHID_CUST_TABLES_DAC2_M3	DAC2_TR Trim - mode 3	0xc012a
FLSHID_CUST_TABLES_DAC2_M4	DAC2_TR Trim - mode 4	0xc012b
FLSHID_CUST_TABLES_DAC2_M5	DAC2_TR Trim - mode 5	0xc012c
FLSHID_CUST_TABLES_DAC2_M6	DAC2_TR Trim - mode 6	0xc012d
FLSHID_CUST_TABLES_DAC2_M7	DAC2_TR Trim - mode 7	0xc012e
FLSHID_CUST_TABLES_DAC2_M8	DAC2_TR Trim - mode 8	0xc012f
FLSHID_CUST_TABLES_DAC1_M1	DAC1_TR Trim - Mode 1	0xc0130
FLSHID_CUST_TABLES_DAC1_M2	DAC1_TR Trim - mode 2	0xc0131
FLSHID_CUST_TABLES_DAC1_M3	DAC1_TR Trim - mode 3	0xc0132
FLSHID_CUST_TABLES_DAC1_M4	DAC1_TR Trim - mode 4	0xc0133
FLSHID_CUST_TABLES_DAC1_M5	DAC1_TR Trim - mode 5	0xc0134
FLSHID_CUST_TABLES_DAC1_M6	DAC1_TR Trim - mode 6	0xc0135
FLSHID_CUST_TABLES_DAC1_M7	DAC1_TR Trim - mode 7	0xc0136
FLSHID_CUST_TABLES_DAC1_M8	DAC1_TR Trim - mode 8	0xc0137
FLSHID_CUST_TABLES_DAC3_M1	DAC3_TR Trim - Mode 1	0xc0138
FLSHID_CUST_TABLES_DAC3_M2	DAC3_TR Trim - mode 2	0xc0139

Register Name	Purpose	Address
FLSHID_CUST_TABLES_DAC3_M3	DAC3_TR Trim - mode 3	0xc013a
FLSHID_CUST_TABLES_DAC3_M4	DAC3_TR Trim - mode 4	0xc013b
FLSHID_CUST_TABLES_DAC3_M5	DAC3_TR Trim - mode 5	0xc013c
FLSHID_CUST_TABLES_DAC3_M6	DAC3_TR Trim - mode 6	0xc013d
FLSHID_CUST_TABLES_DAC3_M7	DAC3_TR Trim - mode 7	0xc013e
FLSHID_CUST_TABLES_DAC3_M8	DAC3_TR Trim - mode 8	0xc013f
FLSHID_MFG_CFG_IMO_TR1	IMO_TR1 Trim	0xc0188
FLS_DATA[0..65535]	FLASH Data	0x100000 + [0..65535 * 0x1]
EXTMEM_DATA[0..8388607]	DATA	0x800000 + [0..8388607 * 0x1]

1.3.1 SRAM_MAP_SYSMEM0_DATA[0..1023]

System Memory - CPU Region

Reset: N/A

Register : Address

SRAM_MAP_SYSMEM0_DATA: 0x0-0xFFF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	NA							
Retention	RET							
Name	sramdata							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	NA							
Retention	RET							
Name	sramdata							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	NA							
Retention	RET							
Name	sramdata							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	NA							
Retention	RET							
Name	sramdata							

Data Storage SRAM

Bits	Name	Description
31:0	sramdata[31:0]	(no description)

1.3.2 SRAM_MAP_SYSMEM1_DATA[0..1023]

System Memory - PHUB Region

Reset: N/A

Register : Address

SRAM_MAP_SYSMEM1_DATA: 0x1000-0x1FFF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	NA							
Retention	RET							
Name	sramdata							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	NA							
Retention	RET							
Name	sramdata							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	NA							
Retention	RET							
Name	sramdata							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	NA							
Retention	RET							
Name	sramdata							

Data Storage SRAM

Bits	Name	Description
31:0	sramdata[31:0]	(no description)

1.3.3 SRAM_MAP_TRACEMEM_DATA[0..1023]

Trace Memory

Reset: N/A

Register : Address

SRAM_MAP_TRACEMEM_DATA: 0x2000-0x2FFF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	NA							
Retention	RET							
Name	sramdata							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	NA							
Retention	RET							
Name	sramdata							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	NA							
Retention	RET							
Name	sramdata							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	NA							
Retention	RET							
Name	sramdata							

Data Storage SRAM

Bits	Name	Description
31:0	sramdata[31:0]	(no description)

1.3.4 CLKDIST_CR

Configuration Register CR

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_CR: 0x4000

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:00		R/W:00		R/W:00	
HW Access	NA	R	R		R		R	
Retention	NA	RET	RET		RET		RET	
Name	RSVD	IMO2X_SRC	IMO_OUT		ILO_OUT		PLL_SRC	

This register is used to configure the 4 main CLK sources. PLL_SRC - The source to the PLL reference clock input. ILO_OUT - ILO source to the clock distribution block. IMO_OUT - The source from IMO to clock distribution block. IMO2X_SRC - Source to IMO doubler. In the table, reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits should always be written with a value of '0'.

Bits	Name	Description
6	IMO2X_SRC	This bit selects if the external clock input (dsi) or XTAL CLK is input to the internal oscillator. The internal oscillator itself contains another mux allowing control if the dsi/XTAL clock or the internal oscillator itself is the source clock to the system clock called IMO and to the IMO frequency doubling circuit. The clock selection in the internal oscillator is controlled by FASTCLK_IMO_CR.XCLKEN. Because this bit can induce clock glitches, it should only be changed when no downstream clock tree is configured to use the IMO clock source, or FASTCLK_IMO_CR.XCLKEN is low at the time it is changed. See Table 1-2.
5:4	IMO_OUT[1:0]	Select the IMO output source to clock distribution. This clock configuration feature is primarily intended for internal use only. Changing this field can cause clock glitches. This needs either to be expected or avoided. To avoid glitches all downstream clock trees will need to be configured to a different clock source when this field is written. See Table 1-3.
3:2	ILO_OUT[1:0]	Select the ILO output source to clock distribution. Any clock tree using this clock as its source must be disabled before writing this register bit to avoid potential glitches. See Table 1-1.
1:0	PLL_SRC[1:0]	Select the PLL reference clock input. Do not change the value in this field while the PLL is the currently selected clock source for the Master Mux or USB clock (if enabled) See Table 1-4.

Table 1-1. Bit field encoding: ILO_OUTPUT_SEL_ENUM

Value	Name	Description
2'h0	ILO100K	100KHz output is selected
2'h1	ILO33K	33KHz output is selected
2'h2	ILO1K	1KHz output is selected
2'h3	RSVD	Reserved

(continued)

Table 1-2. Bit field encoding: IMO2X_INPUT_SEL_ENUM

Value	Name	Description
1'b0	DSI	Digital System Interconnect is used as a source to IMO doubler
1'b1	XTAL	External clock source is used as a source to IMO doubler

Table 1-3. Bit field encoding: IMO_OUTPUT_SEL_ENUM

Value	Name	Description
2'h0	IMO	IMO is selected
2'h1	IMO2X	IMO Doubler output is selected
2'h2	IMO36	IMO 36MHz output is selected
2'h3	RSVD	Reserved

Table 1-4. Bit field encoding: PLL_INPUT_SEL_ENUM

Value	Name	Description
2'h0	IMO	IMO is selected
2'h1	XTAL	4 to 25MHz XTAL is selected
2'h2	DSI	Digital System Interconnect is selected
2'h3	RSVD	Reserved

1.3.5 CLKDIST_LD

LOAD Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_LD: 0x4001

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	R/W:0	R/W:0
HW Access	NA					R/W	R/W	R/W
Retention	NA					RET	RET	RET
Name	RSVD					DISABLE	SYNC_EN	LOAD

This register provides control of clock parameters while the clocks are running and does so without compromising the integrity of the clocks (glitch-free). In groups defined by the DMASK and AMASK registers, clocks can be loaded with new count values or loaded with new divide counts and started aligned together using this feature. Setting the LOAD bit immediately copies the values of the WRK0 and WRK1 registers into all divider divide registers (DCFG0/1 and ACFG0/1, BCFG0/1), which are not masked off. Setting the SYNC_EN bit forces a load and restart of all the dividers which are not masked off (excluding BUS_CLK). Using SYNC_EN restarts all affected dividers phase aligned. In order for the dividers to start phase aligned all the divide values must be integer multiples of one another. Upon setting the DISABLE register bit all dividers which are not masked off are disabled (Excluding BUS_CLK). This allows for local control of the clock trees. The SYNC_EN and LOAD bits, bits 1 and 0 respectively, in this register are cleared upon completion of loading and/or restarting. When changing configuration of any of the ACLK/DCLKs a value of 0x00 needs to be written to both WRK0 and WRK1 registers. Next a value of 0x07 has to be written to this register, LD. One has to poll this register, LD, for bits 1 and 0 (SYNC_EN and LOAD) to be cleared in order to start modifying clock tree configuration. This applies to all ACLK/DCLK configuration bits. The WRK0/1 and DMASK/AMASK register can be written in any order but both must be written before LOAD or SYNC_EN are written. The DMASK/AMASK register must be written before the DISABLE bit is written.

Bits	Name	Description
2	DISABLE	Locally disable all unmasked divders (Excluding BUS_CLK). See Table 1-5.
1	SYNC_EN	Load all unmasked dividers with a common shadow divider value and restart all unmasked dividers in phase. See Table 1-7.
0	LOAD	Load all unmasked dividers with a common shadow divider value. (does not restart them in phase) See Table 1-6.

Table 1-5. Bit field encoding: DISABLE_ENUM

Value	Name	Description
1'b0	DISABLE_0	Enable
1'b1	DISABLE_1	Disable

Table 1-6. Bit field encoding: LOAD_ENUM

Value	Name	Description
1'b0	LOAD_0	Do nothing
1'b1	LOAD_1	Copy shadow value defined in CLKDIST_WRK0 and CLKDIST_WRK1 registers to all dividers selected in CLKDIST_MSK0 and CLKDIST_MSK1 registers

(continued)

Table 1-7. Bit field encoding: SYNC_SHADOW_ENUM

Value	Name	Description
1'b0	SYNC_0	Do nothing
1'b1	SYNC_1	Enable all dividers selected in CLKDIST_MSK register (Excluding BUS_CLK) to start (or restart) in phase. NOTE: does not load the WRK register values. This bit only phase aligns all the selected dividers with their existing divide values.

1.3.6 CLKDIST_WRK0

LSB Shadow Divider Value Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_WRK0: 0x4002

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	DIV_VAL							

This register is the low byte of a count value to be loaded in specified clock dividers defined by the A/DMASK registers. This register (with WRK1) holds a new count value to be atomically loaded, so that the 16 bits dividers can safely be updated dynamically. For information on how this feature is used, see the description in the LD register.

Bits	Name	Description
7:0	DIV_VAL[7:0]	Encoding including WRK1: 0x0000 source 0x0001 source / 2 0x0002 source / 3 ... ... 0xfffe source / 65535 0xffff source / 65536

1.3.7 CLKDIST_WRK1

MSB Shadow Divider Value Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_WRK1: 0x4003

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	DIV_VAL							

This register is the high byte of a count value to be loaded in specified clock dividers defined by the A/DMASK registers. This register (with WRK0) holds a new count value to be atomically loaded, so that the 16 bits dividers can safely be updated dynamically. For information on how this feature is used, see the description in the LD register.

Bits	Name	Description
7:0	DIV_VAL[7:0]	Encoding including WRK0: 0x0000 source 0x0001 source / 2 0x0002 source / 3 ... ... 0xfffe source / 65535 0xffff source / 65536

1.3.8 CLKDIST_MSTR0

Master clock (clk_sync_d) Divider Value Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_MSTR0: 0x4004

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	DIV_VAL							

This register holds the master source clock 8-bit divide value. This register can be written at any time, including while the divider is running. Due to a sampling anomaly in the HW, there is a small probability that the Master divider will divide by an incorrect value (not the past or new value) for one period before stabilizing on the divide value written. If this is undesirable, the workaround is to gray-code walk the divide value to that desired with multiple CSR writes. Also due to a defect in the HW, the Master clock divide value can not be changed from divide-by-n (n>1) to divide-by-1 when divide-by-1 produces an output frequency higher than 50MHz. If a frequency higher than 50MHz is desired a slower clock source must be configured during the switch to divide-by-1.

Bits	Name	Description
7:0	DIV_VAL[7:0]	0x00 source 0x01 source / 2 0x02 source / 3 ... ... 0xfe source / 255 0xff source / 256

1.3.9 CLKDIST_MSTR1

Master (clk_sync_d) Configuration Register/CPU Divider Value

Reset: Reset Signals Listed Below

Register : Address

CLKDIST_MSTR1: 0x4005

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0000				NA:00		R/W:00	
HW Access	R				NA		R	
Retention	RET				NA		NONRET	
Name	CPUDIV				RSVD		SRC_SEL	

This register holds the master clock source configuration and CPU clock divide value. Both fields in this register can be altered at any time without compromising clock integrity.

Bits	Name	Description
7:4	CPUDIV[3:0]	0x0 source 0x1 source / 2 0x2 source / 3 ... ... 0xe source / 15 0xf source / 16
1:0	SRC_SEL[1:0]	Master clock source selection. See Table 1-8.

Reset Table

Reset Signal	Applicable Register Bit(s)
System reset for retention flops [reset_all_retention]	CPUDIV[3:0]
Domain reset for non-retention flops [reset_all_nonretention]	SRC_SEL[1:0]

Table 1-8. Bit field encoding: MASTER_SRC_SEL_ENUM

Value	Name	Description
2'h0	IMO	imo output is selected
2'h1	PLL	pll output is selected
2'h2	XTAL	xtal_mhz output is selected
2'h3	DSI	dsi_c output is selected

1.3.10 CLKDIST_BCFG0

CLK_BUS LSB Divider Value Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_BCFG0: 0x4006

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	DIV_VAL							

This register holds the LSB of the 16-bit divide value. It should only be written when the clock tree is disabled to avoid clock glitches. If the clock divider needs changed when the clock is running, this can be accomplished using the atomic load feature described in the LD register description.

Bits	Name	Description
7:0	DIV_VAL[7:0]	Encoding including BCFG1: 0x0000 source 0x0001 source / 2 0x0002 source / 3 ... ... 0xfffe source / 65535 0xffff source / 65536

1.3.11 CLKDIST_BCFG1

CLK_BUS MSB Divider Value Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_BCFG1: 0x4007

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	DIV_VAL							

This register holds the MSB of the 16-bit divide value. It should only be written when the clock tree is disabled to avoid clock glitches. If the clock divider needs changed when the clock is running, this can be accomplished using the atomic load feature described in the LD register description.

Bits	Name	Description
7:0	DIV_VAL[7:0]	Encoding including BCFG0: 0x0000 source 0x0001 source / 2 0x0002 source / 3 ... ... 0xfffe source / 65535 0xffff source / 65536

1.3.12 CLKDIST_BCFG2

CLK_BUS Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_BCFG2: 0x4008

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	NA:000		
HW Access	R	R	R	R	R	NA		
Retention	RET	RET	RET	RET	RET	NA		
Name	MASK	SSS	EARLY	DUTY	SYNC	RSVD		

This register holds the configuraton values for the Bus Clock. The EARLY bit should never be used and should never be set HIGH. The DUTY bit should never be written when the divider is in use to avoid clock glitches. The SSS and SYNC_EN bits can only be safely written when clk_sync (output of MasterMux) is running at 12MHz or lower and a duty-cycle between 30/70 and 50/50 to avoid clock glitches. The MASK bit is used for inclusion/exclusion from atomic load operations. See the description of this feature in the LD register description. SSS takes precedence over SYNC_EN. Do not set SYNC_EN high with SSS low when the divider is dividing by 1, this halts BUSCLK and is non-recoverable. BUSCLK is phase-aligned (balanced) with the ACLKs/DCLKs only when SSS or SYNC_EN is set HIGH.

Bits	Name	Description
7	MASK	Mask bits to enable shadow loads--0 disable, 1 enable. See LD register description.
6	SSS	Sync source same as output frequency. Used to bypass synchronization with delay matched path. Set this bit high when not dividing and balanced system clocks are desired. Only change when clk_sync is below 12MHz to avoid clock glitches. See Table 1-11.
5	EARLY	RESERVED - Do not set HIGH in any application. See Table 1-10.
4	DUTY	Force duty cycle to 50%. Only change this bit when divider is not in use to avoid clock glitches. See Table 1-9.
3	SYNC	Select output synchronization to master clock. Use to balance system clocks only when the divider is dividing by 2 or higher. Do not set this bit high when the divider is set to divide by 1 if SSS is low - this will halt BUSCLK. Otherwise, to avoid clock glitches, first set the SSS bit high when making changes, then set the SSS bit low when changes are complete. (SSS takes precedence over SYNC so doing this will protect the clock from any glitches related to changing SYNC). See Table 1-12.

Table 1-9. Bit field encoding: DUTY_ENUM

Value	Name	Description
1'b0	DISABLE	Disable 50% duty cycle. Pulse train.
1'b1	ENABLE	Enable 50% duty cycle clock output

Table 1-10. Bit field encoding: EARLY_ENUM

Value	Name	Description
1'b0	DISABLE	Disable early phase mode
1'b1	ENABLE	Enable early phase mode

(continued)

Table 1-11. Bit field encoding: SSS_ENUM

Value	Name	Description
1'b0	DISABLE	Sync source not same frequency
1'b1	ENABLE	Sync source is same frequency

Table 1-12. Bit field encoding: SYNC_ENUM

Value	Name	Description
1'b0	DISABLE	Disable synchronization
1'b1	ENABLE	Enable synchronization

1.3.13 CLKDIST_UCFG

USB Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_UCFG: 0x4009

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:00	
HW Access	NA			R	R	R	R	
Retention	NA			RET	RET	RET	RET	
Name	RSVD			TMODE	GPIPE	DIV2	SRC_SEL	

This register holds the USB clock configuration parameters. Only change values in this register when the USB clock is disabled to avoid clock glitches.

Bits	Name	Description
4	TMODE	Enable monitoring of clk_usb through DSI routing See Table 1-16.
3	GPIPE	Global DSI input pipeline configuration See Table 1-13.
2	DIV2	USB clock divide source by two See Table 1-14.
1:0	SRC_SEL[1:0]	USB clock source selection. See Table 1-15.

Table 1-13. Bit field encoding: CDSI_ENUM

Value	Name	Description
1'b0	BYPASS	Bypass pipeline stages
1'b1	ENABLE	Use pipeline stages

Table 1-14. Bit field encoding: DIV2_ENUM

Value	Name	Description
1'b0	DISABLE	Disable divide by two
1'b1	ENABLE	Enable divide by two

Table 1-15. Bit field encoding: SRC_SEL_ENUM

Value	Name	Description
2'h0	IMO2X	imo2x output is selected
2'h1	IMO	imo output is selected
2'h2	PLL	pll output is selected
2'h3	DSI	dsi_glb_div output is selected

Table 1-16. Bit field encoding: TMODE_ENUM

Value	Name	Description
1'b0	DISABLE	Disable clk_usb_test output to DSI
1'b1	ENABLE	Enable clk_usb_test output to DSI

1.3.14 CLKDIST_DLY0

Delay block Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_DLY0: 0x400A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:00		R/W:00000				
HW Access	NA	R		R				
Retention	NA	RET		RET				
Name	RSVD	CTRIM		FTRIM				

This register is used to trim the delay cell tap duration. This register should only be used when the delay cell is in trim mode (see DLY1 MODE bit). This register can also be accessed via it's alias, the DLY register in the MFGCFG address space.

Bits	Name	Description
6:5	CTRIM[1:0]	Course trim bits for delay block See Table 1-17.
4:0	FTRIM[4:0]	Fine trim bits for delay block 5'b00000 Lowest bias ... ... 5'bfffff Highest bias

Table 1-17. Bit field encoding: CTRIM_ENUM

Value	Name	Description
2'b00	ZERO	Highest bias setting
2'b10	TWO	Second highest bias setting
2'b01	ONE	Third highest bias setting
2'b11	THREE	Fourth highest bias setting

1.3.15 CLKDIST_DLY1

Delay block Configuration Register

Reset: Reset Signals Listed Below

Register : Address

CLKDIST_DLY1: 0x400B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	NA:0	R/W:0
HW Access	NA					R	NA	R
Retention	NA					NONRET	NA	RET
Name	RSVD					EN	RSVD	MODE

This register holds the configuration control for the clock delay cell. This cell is used to program delays between the system bus clock and each of the 4 individual analog clocks (ACLK). This is used to unalign analog and digital domain clock edges to reduce noise when the analog domain clocks. Normally the 5 domains are phase aligned for applications that need clock-edge-aligned interfaces. If clock-edge-aligned interfaces aren't needed and system noise is an issue, clock tree domains can be programmably skewed away from each other.

Bits	Name	Description
2	EN	The clk_sync_d reference clock is sourced by the clk0 output of the delay cell. This output can either be sourced from a 10-tap delay element or muxed directly (bypassed) from the delay cell's clock input (clk_sync). When bypassed (EN=0), the bus clock and all 4 analog clocks (clk_a[]) are balanced (clock-edge-aligned) if their skew delay registers are programmed to 0x0001. (see CLKDIST_ACFGx_CFG3) If EN=1 this enables the delay element on clk0 and allows the system to program delays on clk_sync_d. The delay amount is identical to the ACLK channels but is not controlled with a register, but rather with customer controlled non-volatile bits that are loaded at system POR. In this mode the clk0 has a inherent ~4ns delay, meaning BUSCLK lags the 4 ACLKs by ~4ns when all tap are programmed to 0x0001. Thus, any values programmed into the PHASE_DLY fields of the CLKDIST_ACFGx_CFG3 registers will skew the clocks relative to this ~4ns skew, as will changing the clk0 delay via CNVL setting. Note that it is not allowed that the system be configured such that clk_sync_d lag any clk_a[] by less than ~4ns for any values of the programmable delay values. The HW will fail in these cases and SW should avoid doing this. See ACFG3 register description for further details. This bit is cleared on wakeup from low power modes(sleep, hibernate, hibernate timer modes), user is expected to configure this bit to the required state.
0	MODE	Clock mode. Used to put the delay cell in normal more or trim mode. See Table 1-19.

Reset Table

Reset Signal	Applicable Register Bit(s)
System reset for retention flops [reset_all_retention]	MODE, ISEL
Domain reset for non-retention flops [reset_all_nonretention]	EN

Table 1-18. Bit field encoding: ISEL_ENUM

Value	Name	Description
1'b0	BANDGAP	Use bandgap reference
1'b1	INTERNAL	Use internal reference, this selection is for engineering purposes only

(continued)

Table 1-19. Bit field encoding: MODE_ENUM

Value	Name	Description
1'b0	DELAY	Puts the cell in normal clock delay mode. This is mission mode and allows for programming of delays on the clock trees. See CLKDIST_ACFGx_CFG3
1'b1	RING	This mode is used only for trimming. While in this mode the output of a ring oscillator is monitored and tuned to 40MHz.

1.3.16 CLKDIST_DMASK

Digital Clock Mask Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_DMASK: 0x4010

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	DMASK							

Mask picking which digital clocks are enabled for shadow loads. See LD register description for usage information.

Bits	Name	Description
7:0	DMASK[7:0]	Mask bits to enable shadow loads -- 0 = Disabled, 1 = Enabled MSK0 = DCLK0 MSK1 = DCLK1 : MSK7 = DCLK7

1.3.17 CLKDIST_AMASK

Analog Clock Mask Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_AMASK: 0x4014

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Retention	NA				RET			
Name	RSVD				AMASK			

Mask picking which analog clocks are enabled for shadow loads. See LD register description for usage information.

Bits	Name	Description
3:0	AMASK[3:0]	Mask bits to enable shadow loads -- 0 = Disabled, 1 = Enabled MSK0 = ACLK0 : MSK3 = ACLK3

1.3.18 CLKDIST_DCFG[0..7]_CFG0

LSB Divider Value Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_DCFG0_CFG0: 0x4080
CLKDIST_DCFG1_CFG0: 0x4084
CLKDIST_DCFG2_CFG0: 0x4088
CLKDIST_DCFG3_CFG0: 0x408C
CLKDIST_DCFG4_CFG0: 0x4090
CLKDIST_DCFG5_CFG0: 0x4094
CLKDIST_DCFG6_CFG0: 0x4098
CLKDIST_DCFG7_CFG0: 0x409C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	DIV_VAL							

This register holds the LSB of the 16-bit divide value. Change this register only when the associated clock is disabled. See LD register for details.

Bits	Name	Description
7:0	DIV_VAL[7:0]	Encoding including BCFG1: 0x0000 source 0x0001 source / 2 0x0002 source / 3 ... ... 0xfffe source / 65535 0xffff source / 65536

1.3.19 CLKDIST_DCFG[0..7]_CFG1

MSB Divider Value Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_DCFG0_CFG1: 0x4081
CLKDIST_DCFG1_CFG1: 0x4085
CLKDIST_DCFG2_CFG1: 0x4089
CLKDIST_DCFG3_CFG1: 0x408D
CLKDIST_DCFG4_CFG1: 0x4091
CLKDIST_DCFG5_CFG1: 0x4095
CLKDIST_DCFG6_CFG1: 0x4099
CLKDIST_DCFG7_CFG1: 0x409D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	DIV_VAL							

This register holds the MSB of the 16-bit divide value. Change this register only when the associated clock is disabled. See LD register for details.

Bits	Name	Description
7:0	DIV_VAL[7:0]	Encoding including BCFG0: 0x0000 source 0x0001 source / 2 0x0002 source / 3 ... ... 0xfffe source / 65535 0xffff source / 65536

1.3.20 CLKDIST_DCFG[0..7]_CFG2

Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_DCFG0_CFG2: 0x4082
CLKDIST_DCFG1_CFG2: 0x4086
CLKDIST_DCFG2_CFG2: 0x408A
CLKDIST_DCFG3_CFG2: 0x408E
CLKDIST_DCFG4_CFG2: 0x4092
CLKDIST_DCFG5_CFG2: 0x4096
CLKDIST_DCFG6_CFG2: 0x409A
CLKDIST_DCFG7_CFG2: 0x409E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:000		
HW Access	R	R	R	R	R	R		
Retention	RET	RET	RET	RET	RET	RET		
Name	PIPE	SSS	EARLY	DUTY	SYNC	SRC_SEL		

This register holds the 8-bit DCLK configuraton values. Only change these values when the associated clock is disabled to avoid clock glitches (See LD register for details). Clock is phase-aligned with BUSCLK only when clk_sync_d is the source and SSS or SYNC_EN are set HIGH. SSS takes presedence over SYNC_EN. Never set SYNC_EN=1 with SSS=0 when dividing by 1, as this halts the clock.

Bits	Name	Description
7	PIPE	DSI input pipeline configuration See Table 1-22.
6	SSS	Sync source same as output frequency. Used to bypass synchronization with delay matched path. See Table 1-24.
5	EARLY	This bit in the configuration register can be used to set the early phase mode, with rising edge near the half-count of the divider. See Table 1-21.
4	DUTY	Force duty cycle to 50% See Table 1-20.
3	SYNC	Select output synchronization to master clock See Table 1-25.
2:0	SRC_SEL[2:0]	Clock source selection. See Table 1-23.

Table 1-20. Bit field encoding: DUTY_ENUM

Value	Name	Description
1'b0	DISABLE	Disable 50% duty cycle
1'b1	ENABLE	Enable 50% duty cycle clock output

Table 1-21. Bit field encoding: EARLY_ENUM

Value	Name	Description

(continued)

Table 1-21. Bit field encoding: EARLY_ENUM

1'b0	DISABLE	Disable early phase mode
1'b1	ENABLE	Enable early phase mode

Table 1-22. Bit field encoding: PIPE_ENUM

Value	Name	Description
1'b0	BYPASS	Bypass pipeline stages
1'b1	ENABLE	Use pipeline stages

Table 1-23. Bit field encoding: SRC_SEL_ENUM

Value	Name	Description
3'h0	clk_sync_d	clk_sync_d output is selected
3'h1	imo	imo output is selected
3'h2	xtal_mhz	xtal_mhz output is selected
3'h3	ilo	ilo output is selected
3'h4	pll	pll output is selected
3'h5	xtal_khz	xtal_khz output is selected
3'h6	dsi_g	dsi_global[0] output is selected
3'h7	dsi_d	dsi_d output is selected

Table 1-24. Bit field encoding: SSS_ENUM

Value	Name	Description
1'b0	DISABLE	Sync source not same frequency
1'b1	ENABLE	Sync source is same frequency

Table 1-25. Bit field encoding: SYNC_ENUM

Value	Name	Description
1'b0	DISABLE	Disable synchronization
1'b1	ENABLE	Enable synchronization

1.3.21 CLKDIST_ACFG[0..3]_CFG0

LSB Divider Value Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_ACFG0_CFG0: 0x4100 CLKDIST_ACFG1_CFG0: 0x4104

CLKDIST_ACFG2_CFG0: 0x4108 CLKDIST_ACFG3_CFG0: 0x410C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	DIV_VAL							

This register holds the LSB of the 16-bit divide value. Change this register only when the associated clock is disabled. See LD register for details.

Bits	Name	Description
7:0	DIV_VAL[7:0]	Encoding including BCFG1: 0x0000 source 0x0001 source / 2 0x0002 source / 3 ... ... 0xfffe source / 65535 0xffff source / 65536

1.3.22 CLKDIST_ACFG[0..3]_CFG1

MSB Divider Value Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_ACFG0_CFG1: 0x4101

CLKDIST_ACFG1_CFG1: 0x4105

CLKDIST_ACFG2_CFG1: 0x4109

CLKDIST_ACFG3_CFG1: 0x410D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	DIV_VAL							

This register holds the MSB of the 16-bit divide value. Change this register only when the associated clock is disabled. See LD register for details.

Bits	Name	Description
7:0	DIV_VAL[7:0]	Encoding including BCFG0: 0x0000 source 0x0001 source / 2 0x0002 source / 3 ... ... 0xfffe source / 65535 0xffff source / 65536

1.3.23 CLKDIST_ACFG[0..3]_CFG2

Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_ACFG0_CFG2: 0x4102

CLKDIST_ACFG1_CFG2: 0x4106

CLKDIST_ACFG2_CFG2: 0x410A

CLKDIST_ACFG3_CFG2: 0x410E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:000		
HW Access	R	R	R	R	R	R		
Retention	RET	RET	RET	RET	RET	RET		
Name	PIPE	SSS	EARLY	DUTY	SYNC	SRC_SEL		

This register holds the 8-bit ACLK configuraton values. Only change these values when the associated clock is disabled to avoid clock glitches (See LD register for details). Clock is phase-aligned with BUSCLK only when clk_sync_a/d is the source and SSS or SYNC_EN are set HIGH. SSS takes presedence over SYNC_EN. Never set SYNC_EN=1 when dividing by 1, this halts the clock.

Bits	Name	Description
7	PIPE	DSI input pipeline configuration See Table 1-28.
6	SSS	Sync source same as output frequency. Used to bypass synchronization with delay matched path. See Table 1-30.
5	EARLY	This bit in the configuration register can be used to set the early phase mode, with rising edge near the half-count of the divider. See Table 1-27.
4	DUTY	Force duty cycle to 50% See Table 1-26.
3	SYNC	Select output synchronization to master clock See Table 1-31.
2:0	SRC_SEL[2:0]	Clock source selection. See Table 1-29.

Table 1-26. Bit field encoding: DUTY_ENUM

Value	Name	Description
1'b0	DISABLE	Disable 50% duty cycle
1'b1	ENABLE	Enable 50% duty cycle clock output

Table 1-27. Bit field encoding: EARLY_ENUM

Value	Name	Description
1'b0	DISABLE	Disable early phase mode
1'b1	ENABLE	Enable early phase mode

(continued)

Table 1-28. Bit field encoding: PIPE_ENUM

Value	Name	Description
1'b0	BYPASS	Bypass pipeline stages
1'b1	ENABLE	Use pipeline stages

Table 1-29. Bit field encoding: SRC_SEL_ENUM

Value	Name	Description
3'h0	clk_sync_a	clk_sync_a output is selected
3'h1	imo	imo output is selected
3'h2	xtal_mhz	xtal_mhz output is selected
3'h3	ilo	ilo output is selected
3'h4	pll	pll output is selected
3'h5	xtal_khz	xtal_khz output is selected
3'h6	dsi_g	dsi_global[0] output is selected
3'h7	dsi_a	dsi_a output is selected

Table 1-30. Bit field encoding: SSS_ENUM

Value	Name	Description
1'b0	DISABLE	Sync source not same frequency
1'b1	ENABLE	Sync source is same frequency

Table 1-31. Bit field encoding: SYNC_ENUM

Value	Name	Description
1'b0	DISABLE	Disable synchronization
1'b1	ENABLE	Enable synchronization

1.3.24 CLKDIST_ACFG[0..3]_CFG3

Analog clocks Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CLKDIST_ACFG0_CFG3: 0x4103

CLKDIST_ACFG1_CFG3: 0x4107

CLKDIST_ACFG2_CFG3: 0x410B

CLKDIST_ACFG3_CFG3: 0x410F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Retention	NA				RET			
Name	RSVD				PHASE_DLY			

This register holds the analog clocks delay configuration. This register should not be written when the associated clock tree is enabled to avoid clock glitches. See DLY1 for more information how to use this register. Note that due to a clock balancing problem in the HW that some delay values can produce jitter in the ACLKs.

Bits	Name	Description
3:0	PHASE_DLY[3:0]	Phase delay selection (1.0ns increments): 0x00 Clock Disabled 0x01 0 ns delay 0x02 1 ns delay ... 0x0a 9 ns delay 0x0b 10 ns delay 0x0c Clock Disabled 0x0d Clock Disabled 0x0e Clock Disabled 0x0f Clock Disabled

1.3.25 FASTCLK_IMO_CR

Internal Main Oscillator Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FASTCLK_IMO_CR: 0x4200

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:000		
HW Access	R	R	R	R	R	R		
Retention	RET	RET	RET	RET	RET	RET		
Name	sel_fast_bias	usbclk_on	xclken	f2xon	en_fast_bias	f_range		

This register controls operation of the IMO.

Bits	Name	Description
7	sel_fast_bias	Select IMO reference source, possible frequency selections are 12,24 and 48MHz See Table 1-35.
6	usbclk_on	Configures IMO for higher precision for when the internal USB clock-locking function is being used. See Table 1-36.
5	xclken	External clock enable for the IMO and the IMO doubler. This bit selects if the Internal Oscillator or an external clock is the source of IMO and the input to the IMO Doubler. There are two choices for the external clock source, dsi and XTAL (see CLKDIST.CR.IMO2X_SRC). See Table 1-37.
4	f2xon	IMO Doubler enable See Table 1-33.
3	en_fast_bias	Enables fast wake bias circuitry. This must be set before selecting the fast wake bias as the IMO reference using sel_fast_bias. See Table 1-32.
2:0	f_range[2:0]	Frequency range setting for the IMO. Note that if sel_fast_bias and en_fast_bias are set OR the device is in boot OR wake from sleep/hibernate/hibernate-timer modes IMO will be forced to FIMO mode. During boot, device wakeup from sleep/hibernate/hibernate-timers mode frequency setting is overriden by the value in PWRSYS_WAKE_TR1.wake_imofreq. During other times if sel_fast_bias and en_fast_bias are set then IMO frequency setting is controlled by f_range configuration bits only. See PWRSYS_WAKE_TR1 for FIMO frequency table. See Table 1-34.

Table 1-32. Bit field encoding: EN_FAST_BIAS

Value	Name	Description
1'b0	EN_FAST_BIAS_DISABLE	Disable fast wake bias circuit
1'b1	EN_FAST_BIAS_ENABLE	Enable fast wake bias circuit

(continued)

Table 1-33. Bit field encoding: F2XON_ENUM

Value	Name	Description
1'b0	F2XON_0	Doubler disabled (IMOCLK2X = 0)
1'b1	F2XON_1	Doubler enabled. Note: input freq range limited to 24 MHz max.

Table 1-34. Bit field encoding: F_RANGE_ENUM

Value	Name	Description
3'h0	F_RANGE_0	12 MHz (normal)
3'h1	F_RANGE_1	6 MHz (12MHz if sel_fast_bias=1)
3'h2	F_RANGE_2	24 MHz
3'h3	F_RANGE_3	3 MHz (RESERVED in FIMO mode)
3'h4	F_RANGE_4	48 MHz
3'h5	F_RANGE_5	62 MHz center, 67 MHz peak (48MHz if sel_fast_bias=1)
3'h6	F_RANGE_6	72 MHz center, 80 Mhz peak (48MHz if sel_fast_bias=1)
3'h7	F_RANGE_7	Reserved (48MHz if sel_fast_bias=1)

Table 1-35. Bit field encoding: SEL_FAST_BIAS_ENUM

Value	Name	Description
1'b0	SEL_FAST_BIAS_NORMAL	Select LVBG as IMO reference
1'b1	SEL_FAST_BIAS_FAST	Select fast wake bias as IMO reference

Table 1-36. Bit field encoding: USBCLK_ON_ENUM

Value	Name	Description
1'b0	USBCLK_ON_0	Normally used for non-USB modes, for lower IMO power
1'b1	USBCLK_ON_1	USB clock-locking used; IMO runs at higher power for highest USB clock precision.

Table 1-37. Bit field encoding: XCLKEN_ENUM

Value	Name	Description
1'b0	XCLKEN_0	IMO doubler runs from the IMOCLK
1'b1	XCLKEN_1	IMO doubler runs from the selected 'external' clock.

1.3.26 FASTCLK_XMHZ_CSR

External 4-25 MHz Crystal Oscillator Status and Control Register

Reset: Reset Signals Listed Below

Register : Address

FASTCLK_XMHZ_CSR: 0x4210

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	RC:0	R/W:0	NA:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	W	R	NA	R	R	R	R	R
Retention	NONRET	RET	NA	RET	RET	RET	RET	RET
Name	xerr	xprot	RSVD	xstart	xpump_dis	xfb_dis	xto_dis	en

This register is used to enable and configure modes of the XMHZ oscillator, and to read error status. In the table above, reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits should always be written with a value of '0'.

Bits	Name	Description
7	xerr	High output indicates oscillator failure. Only use this after start-up interval is completed. This can be used for status and failure recovery.
6	xprot	Enable External Crystal Oscillator (XMHZ) fault recovery circuitry See Table 1-40.
4	xstart	This INTERNAL bit selects the start-up mode for the oscillator. By default, the output is pulsed to initiate start-up. If a system clock is available at approximately the same frequency as the crystal, this signal can be selected to provide a faster start-up time. See Table 1-42.
3	xpump_dis	This bit disables the crystal oscillator voltage pumps. Recommended settings: 1 when VDDA > 2*VCCD (pump disabled) 0 when VDDA <= 2*VCCD (pump enabled) See Table 1-41.
2	xfb_dis	This bit disables an amplitude monitor on the oscillator signal. If the oscillator amplitude is too low, the XERR bit will be high. See Table 1-39.
1	xto_dis	This bit disables a watchdog monitor on the oscillator signal. Error output bit is asserted immediately after the oscillator is enabled and is de-asserted as soon as the output clock toggles See Table 1-43.
0	en	This bit enables the 4 - 25 MHz crystal oscillator circuit when set high. See Table 1-38.

Reset Table

Reset Signal	Applicable Register Bit(s)
System reset for retention flops [reset_all_retention]	en, xto_dis, xfb_dis, xpump_dis, xstart, xprot
Domain reset for non-retention flops [reset_all_nonretention]	xerr

(continued)

Table 1-38. Bit field encoding: EN_ENUM

Value	Name	Description
1'b0	EN_0	disabled
1'b1	EN_1	enabled. Note that the oscillator amplitude takes time to reach stable amplitude. This can be monitored with the XERR bit.

Table 1-39. Bit field encoding: XFB_DIS_ENUM

Value	Name	Description
1'b0	XFB_DIS_0	Feedback enabled - If oscillator has insufficient amplitude, XERR bit will be high.
1'b1	XFB_DIS_1	Feedback disabled

Table 1-40. Bit field encoding: XPROT_ENUM

Value	Name	Description
1'b0	XPROT_0	Fault Recovery not enabled
1'b1	XPROT_1	Fault Recovery enabled

Table 1-41. Bit field encoding: XPUMP_DIS_ENUM

Value	Name	Description
1'b0	XPUMP_DIS_0	Pumps enabled - Use this setting if Vdd can be <3V.
1'b1	XPUMP_DIS_1	Pumps disabled - Only use this if Vdd will be >3V when oscillator is enabled.

Table 1-42. Bit field encoding: XSTART_ENUM

Value	Name	Description
1'b0	XSTART_0	Use internal single pulse
1'b1	XSTART_1	Use a clock close to the target frequency to improve start-up time.

Table 1-43. Bit field encoding: XTO_DIS_ENUM

Value	Name	Description
1'b0	XTO_DIS_0	Watchdog enabled - Oscillator must achieve proper switching within the internal time window, or XERR will be set high.
1'b1	XTO_DIS_1	Watchdog disabled

1.3.27 FASTCLK_XMHZ_CFG0

External 4-25 MHz Crystal Oscillator Configuration Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FASTCLK_XMHZ_CFG0: 0x4212

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:00000				
HW Access	NA			R/W				
Retention	NA			RET				
Name	RSVD			xcfg				

Bits	Name	Description
4:0	xcfg[4:0]	Selects amplifier transconductance setting, which impacts -R for crystal oscillator startup; Settings are based on the external crystal's parallel resonant load capacitance specification (CL) and its shunt capacitance (C0); CL >= 15pF: C0 >= 3.5pF: Frequency <= 7.3MHz : xcfg = 5'h0E 7.3MHz < Frequency <= 13.2MHz : xcfg = 5'h13 Frequency > 13.2MHz : xcfg = 5'h19 C0 < 3.5pF: Frequency <= 6.9MHz : xcfg = 5'h13 Frequency > 6.9MHz : xcfg = 5'h17 CL < 15pF: Frequency <= 7.3MHz : xcfg = 5'h0A 7.3MHz < Frequency <= 12.9MHz : xcfg = 5'h0E Frequency > 12.9MHz : xcfg = 5'h13

1.3.28 FASTCLK_XMHZ_CFG1

External 4-25 MHz Crystal Oscillator Configuration Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FASTCLK_XMHZ_CFG1: 0x4213

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:000			R/W:0000			
HW Access	NA	R/W			R/W			
Retention	NA	RET			RET			
Name	RSVD	vref_sel_wd			vref_sel_fb			

Bits	Name	Description
6:4	vref_sel_wd[2:0]	Selects reference level for watchdog (vrefout_wd); NOTE: vref_sel_fb must be greater than or equal to the binary value of vref_sel_wd. Valid settings are: 5 for XOSC freq < 16 MHz 3 for 16 MHz <= XOSC freq <= 25 MHz See Table 1-45.
3:0	vref_sel_fb[3:0]	Selects reference level for feedback (vrefout_fb); NOTE: vref_sel_fb must be greater than or equal to the binary value of vref_sel_wd See Table 1-44.

Table 1-44. Bit field encoding: VREF_SEL_FB_ENUM

Value	Name	Description
4'h0	VREF_SEL_FB_0	139 mV
4'h1	VREF_SEL_FB_1	185 mV
4'h2	VREF_SEL_FB_2	231 mV
4'h3	VREF_SEL_FB_3	277 mV
4'h4	VREF_SEL_FB_4	323 mV
4'h5	VREF_SEL_FB_5	370 mV
4'h6	VREF_SEL_FB_6	416 mV
4'h7	VREF_SEL_FB_7	462 mV
4'h8	VREF_SEL_FB_8	508 mV
4'h9	VREF_SEL_FB_9	554 mV
4'ha	VREF_SEL_FB_10	601 mV
4'hb	VREF_SEL_FB_11	647 mV
4'hc	VREF_SEL_FB_12	693 mV
4'hd	VREF_SEL_FB_13	739 mV
4'he	VREF_SEL_FB_14	786 mV
4'hf	VREF_SEL_FB_15	832 mV

Table 1-45. Bit field encoding: VREF_SEL_WD_ENUM

Value	Name	Description
3'h0	VREF_SEL_WD_0	46 mV
3'h1	VREF_SEL_WD_1	92 mV
3'h2	VREF_SEL_WD_2	139 mV
3'h3	VREF_SEL_WD_3	185 mV
3'h4	VREF_SEL_WD_4	231 mV

(continued)

Table 1-45. Bit field encoding: VREF_SEL_WD_ENUM

3'h5	VREF_SEL_WD_5	277 mV
3'h6	VREF_SEL_WD_6	323 mV
3'h7	VREF_SEL_WD_7	370 mV

1.3.29 FASTCLK_PLL_CFG0

PLL Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FASTCLK_PLL_CFG0: 0x4220

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:01		R/W:01		NA:000			R/W:0
HW Access	R		R		NA			R
Retention	RET		RET		NA			RET
Name	wait		delay		RSVD			en

This register provides status and control for the PLL.

Bits	Name	Description
7:6	wait[1:0]	Lock detect wait time before declaring lock. The PLL's high phase error indicator must remain low for this number of PFD clock periods before the raw lock detect signal asserts. The PFD clock must be within 1MHz to 3MHz, and is determined by the PLL reference clock (FREF) divided by Q. The PFD clock period TPFD is determined by the equation TPFD=Q/FREF See Table 1-48.
5:4	delay[1:0]	Lock detect delay time. This is approximate phase error time allowed before the high phase error indicator asserts and clears the raw lock detect status bit. See Table 1-46.
0	en	Enable PLL See Table 1-47.

Table 1-46. Bit field encoding: DELAY_ENUM

Value	Name	Description
2'h0	DELAY_0	19ns delay
2'h1	DELAY_1	23ns delay (default)
2'h2	DELAY_2	28ns delay
2'h3	DELAY_3	33ns delay

Table 1-47. Bit field encoding: PLL_EN_ENUM

Value	Name	Description
1'b0	PLL_EN_DISABLE	PLL Disabled
1'b1	PLL_EN_ENABLE	PLL Enabled

Table 1-48. Bit field encoding: WAIT_ENUM

Value	Name	Description
2'h0	WAIT_0	7 * TPFD
2'h1	WAIT_1	15 * TPFD (default)
2'h2	WAIT_2	23 * TPFD
2'h3	WAIT_3	31 * TPFD

1.3.30 FASTCLK_PLL_CFG1

PLL Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FASTCLK_PLL_CFG1: 0x4221

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:100			NA:00		R/W:10	
HW Access	NA	R			NA		R	
Retention	NA	RET			NA		RET	
Name	RSVD	icpsel			RSVD		vco_gain	

This register sets trim levels and test modes in the PLL.

Bits	Name	Description
6:4	icpsel[2:0]	Charge Pump current select. This bit-field should be set to 0x01 for all configurations. See Table 1-49.
1:0	vco_gain[1:0]	VCO loop gain. Gain doesn't begin effect the VCO frequency characteristics untill freq>60MHz. Effect of gain setting is provided at 25C, Vctrl=0.925V. See Table 1-50.

Table 1-49. Bit field encoding: PLL_ICPSEL_ENUM

Value	Name	Description
3'h0	PLL_ICPSEL_0	1uA
3'h1	PLL_ICPSEL_1	2uA
3'h2	PLL_ICPSEL_2	3uA
3'h3	PLL_ICPSEL_3	4uA
3'h4	PLL_ICPSEL_4	5uA
3'h5	PLL_ICPSEL_5	6uA
3'h6	PLL_ICPSEL_6	7uA
3'h7	PLL_ICPSEL_7	1uA

Table 1-50. Bit field encoding: PLL_VCO_GAIN_ENUM

Value	Name	Description
2'h0	PLL_VCO_GAIN_0	RESERVED
2'h1	PLL_VCO_GAIN_1	RESERVED
2'h2	PLL_VCO_GAIN_2	456 MHz/V
2'h3	PLL_VCO_GAIN_3	RESERVED

1.3.31 FASTCLK_PLL_P

PLL P-Counter Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FASTCLK_PLL_P: 0x4222

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000100							
HW Access	R							
Retention	RET							
Name	p							

This register sets the P-Counter value, an 8-bit feedback divider

Bits	Name	Description
7:0	p[7:0]	P-Counter divide value. Settings less than 8 do not give valid outputs. Valid range is 8 - 255, but this must still give a divided frequency of 1 - 3 MHz (PLLOUT / P); this is the limit of the implementation. Set the P-Counter to legal value before enabling PLL. f_out = f_in*(P/Q) See Table 1-51.

Table 1-51. Bit field encoding: P_ENUM

Value	Name	Description
8'h08	P_DIV8	Divide by 8 (minimum valid value)
8'h09	P_DIV9	Divide by 9
8'h0A	P_DIV10	Divide by 10
8'h0f	P_DIV15	Divide by 15
8'hfe	P_DIV254	Divide by 254
8'hff	P_DIV255	Divide by 255

1.3.32 FASTCLK_PLL_Q

PLL Q-Counter Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FASTCLK_PLL_Q: 0x4223

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0011			
HW Access	NA				R			
Retention	NA				RET			
Name	RSVD				q			

This register sets the Q-Counter value, a 4-bit divider on the input clock to the PLL.

Bits	Name	Description
3:0	q[3:0]	Q-Counter divide value. qrt-The Q divider (Reference) input Freq range is: 1-48MHz. The Q divider output Freq (and PFD input Freq) must be between 1-3MHz. f_out = f_in*(P/Q) See Table 1-52.

Table 1-52. Bit field encoding: Q_ENUM

Value	Name	Description
4'h0	Q_DIV1	Divide by 1
4'h1	Q_DIV2	Divide by 2
4'h2	Q_DIV3	Divide by 3
4'h3	Q_DIV4	Divide by 4
4'h4	Q_DIV5	Divide by 5
4'h5	Q_DIV6	Divide by 6
4'h6	Q_DIV7	Divide by 7
4'h7	Q_DIV8	Divide by 8
4'h8	Q_DIV9	Divide by 9
4'h9	Q_DIV10	Divide by 10
4'ha	Q_DIV11	Divide by 11
4'hb	Q_DIV12	Divide by 12
4'hc	Q_DIV13	Divide by 13
4'hd	Q_DIV14	Divide by 14
4'he	Q_DIV15	Divide by 15
4'hf	Q_DIV16	Divide by 16

1.3.33 FASTCLK_PLL_SR

PLL Status Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

FASTCLK_PLL_SR: 0x4225

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						NA:0	RC:0
HW Access	NA						NA	W
Retention	NA						NA	NONRET
Name	RSVD						RSVD	lockdet

Bits	Name	Description
0	lockdet	Lock Status Flag. If lock is acquired this flag will stay set (regardless of whether lock is subsequently lost) until it is read. Upon reading it will clear. If lock is still true then the bit will simply set again. If lock happens to be false when the clear on read occurs then the bit will stay cleared until the next lock event. This output is only valid if the PLL is enabled. If the PLL is disabled, this bit may be high and won't be cleared by a read. In this scenario, this bit will remain high after enabling the PLL until after the PLL clock output begins running. As a safeguard, the lock bit should not be polled for 50us after the PLL is enabled. The bit should be ignored altogether when the PLL is disabled.

1.3.34 SLOWCLK_ILO_CR0

Internal Low-speed Oscillator Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SLOWCLK_ILO_CR0: 0x4300

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:1	NA:0	R/W:1	R/W:1	NA:0
HW Access	NA		R	R	NA	R	R	NA
Retention	NA		RET	RET	NA	RET	RET	NA
Name	RSVD		div3en	pd_mode	RSVD	en_100k	en_1k	RSVD

This register controls operation of the ILO output clocks.

Bits	Name	Description
5	div3en	Divide-by-3 enable for 100 kHz output See Table 1-53.
4	pd_mode	Power down mode for ILO See Table 1-54.
2	en_100k	Enables 100kHz ILO clock output when set. When clear, clock output is low.
1	en_1k	Enables 1kHz ILO clock output when set. This bit is forced on when PM.WDT_CFG.wdr_en bit is set. When clear, clock output is low.

Table 1-53. Bit field encoding: DIV3EN_ENUM

Value	Name	Description
1'b0	DIV3EN_0	CLK33K disabled
1'b1	DIV3EN_1	CLK33K enabled, divides CLK100K by 3

Table 1-54. Bit field encoding: PD_MODE_ENUM

Value	Name	Description
1'b0	PD_MODE_0	Faster start-up, internal bias left on
1'b1	PD_MODE_1	Slower start-up, internal bias off

1.3.35 SLOWCLK_ILO_CR1

Internal Low-speed Oscillator Control Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SLOWCLK_ILO_CR1: 0x4301

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	R/W:0	R/W:0
HW Access	NA					R/W	R	R
Retention	NA					RET	RET	RET
Name	RSVD					freq_sel	bias_opt	dis_turbo

This register controls non-standard features of the ILO.

Bits	Name	Description
2	freq_sel	Frequency select for CLK100K See Table 1-57.
1	bias_opt	Alternate bias for ILO See Table 1-55.
0	dis_turbo	Start-up speed control See Table 1-56.

Table 1-55. Bit field encoding: BIAS_OPT_ENUM

Value	Name	Description
1'b0	BIAS_OPT_0	sub-threshold bias (default)
1'b1	BIAS_OPT_1	Use saturated bias

Table 1-56. Bit field encoding: DIS_TURBO_ENUM

Value	Name	Description
1'b0	DIS_TURBO_0	Turbo enabled (recommended)
1'b1	DIS_TURBO_1	Turbo disabled

Table 1-57. Bit field encoding: FREQ_SEL_ENUM

Value	Name	Description
1'b0	FREQ_SEL_0	CLK100K defaults to 100 kHz
1'b1	FREQ_SEL_1	CLK100K defaults to 32 kHz

1.3.36 SLOWCLK_X32_CR

External 32kHz Crystal Oscillator Control Register

Reset: Reset Signals Listed Below

Register : Address

SLOWCLK_X32_CR: 0x4308

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R:U	R:U	NA:0	R/W:1	R/W:0	R/W:0
HW Access	NA		W	W	NA	R	R	R
Retention	NA		NONRET	NONRET	NA	RET	RET	RET
Name	RSVD		ana_stat	dig_stat	RSVD	pdb	lpm	x32en

This register controls operation of the 32K Crystal Oscillator, and provides status on the oscillator's stability.

Bits	Name	Description
5	ana_stat	Indicates oscillator status, using internal analog measurement. See Table 1-58.
4	dig_stat	Indicates oscillator status, using test against a reference clock. The ILO's CLK33K must be enabled for this function to operate. See Table 1-59.
2	pdb	Power switch enable (active-low powerdown) for 32K crystal oscillator. When enabling the X32, it is recommended to set this bit first, then set en=1 in a separate bus cycle. The X32 is automatically powered down during hibernate modes.
1	lpm	Power setting for 32K crystal oscillator. This setting only takes effect in sleep modes. During active modes, the oscillator always runs in high power mode. See Table 1-60.
0	x32en	32K Crystal Oscillator Enable See Table 1-61.

Reset Table

Reset Signal	Applicable Register Bit(s)
N/A	dig_stat, ana_stat
System reset for retention flops [reset_all_retention]	x32en, lpm, pdb

Table 1-58. Bit field encoding: ANA_STAT_ENUM

Value	Name	Description
1'b0	ANA_STAT_0	oscillator not stable
1'b1	ANA_STAT_1	oscillator stable

Table 1-59. Bit field encoding: DIG_STAT_ENUM

Value	Name	Description
1'b0	DIG_STAT_0	oscillator not stable
1'b1	DIG_STAT_1	oscillator stable

(continued)

Table 1-60. Bit field encoding: LPM_ENUM

Value	Name	Description
1'b0	LPM_0	High Power Mode
1'b1	LPM_1	Low Power Mode (Only applies in chip sleep mode)

Table 1-61. Bit field encoding: X32EN_ENUM

Value	Name	Description
1'b0	X32_EN_0	Oscillator disabled, power down
1'b1	X32_EN_1	Oscillator enabled

1.3.37 BOOST_CR0

Boost Control 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BOOST_CR0: 0x4320

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:11		R/W:00100				
HW Access	R/W	R/W		R/W				
Retention	RET	RET		RET				
Name	thump	mode		vsel				

Boost output voltage and mode control register.

Bits	Name	Description
7	thump	Generates a 1 microsecond pulse on 0->1 transition. Must be cleared by firmware before another pulse can be generated. Used for discrete switch control in Boost Standby Mode.
6:5	mode[1:0]	Boost mode select. See Table 1-62.
4:0	vsel[4:0]	Boost voltage selection See Table 1-63.

Table 1-62. Bit field encoding: mode_enum

Value	Name	Description
2'b00	MODE_00	Standby Mode (low power state)
2'b01	MODE_01	Reserved
2'b10	MODE_10	Reserved
2'b11	MODE_11	Active Mode (regulating)

Table 1-63. Bit field encoding: vsel_enum

Value	Name	Description
5'b00000	VSEL_OFF	Off (0V)
5'b00001	VSEL_0x01	Reserved
5'b00010	VSEL_0x02	Reserved
5'b00011	VSEL_1P80V	1.80V
5'b00100	VSEL_1P90V	1.90V (Power Up Setting)
5'b00101	VSEL_2P00V	2.00V
5'b00110	VSEL_2P10V	2.10V
5'b00111	VSEL_2P20V	2.20V
5'b01000	VSEL_2P30V	2.30V
5'b01001	VSEL_2P40V	2.40V
5'b01010	VSEL_2P50V	2.50V
5'b01011	VSEL_2P60V	2.60V
5'b01100	VSEL_2P70V	2.70V
5'b01101	VSEL_2P80V	2.80V
5'b01110	VSEL_2P90V	2.90V
5'b01111	VSEL_3P00V	3.00V
5'b10000	VSEL_3P10V	3.10V
5'b10001	VSEL_3P20V	3.20V
5'b10010	VSEL_3P30V	3.30V

(continued)

Table 1-63. Bit field encoding: vsel_enum

5'b10011	VSEL_3P40V	3.40V
5'b10100	VSEL_3P50V	3.50V
5'b10101	VSEL_3P60V	3.60V
5'b10110	VSEL_4P00V	4.00V
5'b10111	VSEL_4P25V	4.25V
5'b11000	VSEL_4P50V	4.50V
5'b11001	VSEL_4P75V	4.75V
5'b11010	VSEL_5P00V	5.00V
5'b11011	VSEL_0x1B	Reserved
5'b11100	VSEL_0x1C	Reserved
5'b11101	VSEL_0x1D	Reserved
5'b11110	VSEL_0x1E	Reserved
5'b11111	VSEL_0x1F	Reserved

1.3.38 BOOST_CR1

Boost Control 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BOOST_CR1: 0x4321

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	NA:0	NA:0	NA:0	R/W:1	NA:0	R/W:01	
HW Access	NA	NA	NA	NA	R/W	NA	R/W	
Retention	NA	NA	NA	NA	RET	NA	RET	
Name	RSVD	RSVD	RSVD	RSVD	boosten	RSVD	clk	

Boost test, clock, and mode control register.

Bits	Name	Description
3	boosten	When set, enables boost operation
1:0	clk[1:0]	Boost active mode internal PWM clock frequency selection See Table 1-64.

Table 1-64. Bit field encoding: clk_enum

Value	Name	Description
2'b00	CLK_RSVD0	Reserved
2'b01	CLK_ON	PWM Clock On at 400kHz. Use this setting in Boost Active Mode. PWM is off in Boost Standby Mode.
2'b10	CLK_RSVD2	Reserved
2'b11	CLK_OFF	PWM Clock Off. Use this setting in Boost Standby Mode for lowest current, or for selecting the External Clock in Automatic Thump Mode.

1.3.39 BOOST_CR2

Boost Control 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BOOST_CR2: 0x4322

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0	R:1	R:0	R:0	R/W:0	R/W:0	NA:0	R/W:0
HW Access	R/W	R/W	R/W	R/W	R/W	R/W	NA	R/W
Retention	RET	RET	RET	RET	RET	RET	NA	RET
Name	disc	boosting	equal	limdet	erefsel	limoff	RSVD	enatm

Boost configuration and status register. The lower 4 bits are advanced configuration and the upper 4 bits are status.

Bits	Name	Description
7	disc	When set, boost converter is operating in discontinuous mode
6	boosting	When set, converter is boosting (VBOOST < vsel)
5	equal	When set, converter is bypassed (VBAT >= vsel). VBOOST shorted to VBAT.
4	limdet	When set, the IND was not fully pulled low during the full duration that the NMOS switch to ground was enabled. This is a debug flag only. The circuit takes no action based on this status bit.
3	erefsel	When set, selects external reference See Table 1-65.
2	limoff	When set, turns off skip cycle current limiter
0	enatm	When set, enables Automatic Thump Mode in Boost Standby Mode

Table 1-65. Bit field encoding: BOOST_EREFSEL_ENUM

Value	Name	Description
1'b0	BOOST_EREFSEL_INTERNAL	Select internal reference
1'b1	BOOST_EREFSEL_EXTERNAL	Select external 800mv precision reference (vref_800mv)

1.3.40 BOOST_CR3

Boost Control 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BOOST_CR3: 0x4323

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:00	
HW Access	NA						R/W	
Retention	NA						RET	
Name	RSVD						pwm	

Boost PWM value (not written during normal operation).

Bits	Name	Description
1:0	pwm[1:0]	Current state of the internal pulse width modulator. The PWM value should not be written during normal operation - it should be treated as read-only. 2'h3 means maximum duty cycle. 2'h0 means minimum duty cycle.

1.3.41 BOOST_SR

Boost Status

Reset: N/A

Register : Address

BOOST_SR: 0x4324

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:U	R:U	NA:0	R:U	R:U	R:U	R:U	R:U
HW Access	R/W	R/W	NA	R/W	R/W	R/W	R/W	R/W
Retention	RET	RET	NA	RET	RET	RET	RET	RET
Name	ready	start	RSVD	ov	vhi	vnom	vlo	uv

Boost status, including window comparator results.

Bits	Name	Description
7	ready	When set, internal circuits have been initialized
6	start	When set, converter is in startup mode
4	ov	Output above overvoltage limit when 1, below limit when 0
3	vhi	Output is above vhigh limit when 1, below limit when 0
2	vnom	Output is above nominal when 1, below nominal when 0
1	vlo	Output is above vlow limit when 1, below limit when 0
0	uv	Output is above undervoltage limit when 1, below limit when 0

1.3.42 BOOST_CR4

Boost Control Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BOOST_CR4: 0x4325

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Retention	NA							RET
Name	RSVD							boost_ie

Boost interrupt control register.

Bits	Name	Description
0	boost_ie	When set, a boost undervoltage condition is propagated to the interrupt controller via the PM interrupt line. When clear, the interrupt condition is masked.

1.3.43 BOOST_SR2

Boost Status Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BOOST_SR2: 0x4326

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							RC:0
HW Access	NA							R/W
Retention	NA							RET
Name	RSVD							boost_int

Boost interrupt status register.

Bits	Name	Description
0	boost_int	When set, a boost undervoltage event has occured. The setting of boost_ie determines whether this interrupt condition is masked or propagated to the interrupt controller. Sticky (whole field)

1.3.44 PWRSYS_CR0

Power System Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_CR0: 0x4330

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	NA:000			R/W:0
HW Access	NA		R	R	NA			R
Retention	NA		RET	RET	NA			RET
Name	RSVD		ext_vccd	ext_vcca	RSVD			rbbnw_dis

This register controls the voltage regulators.

Bits	Name	Description
5	ext_vccd	When set, the core digital (vccd) pin is driven with an externally regulated voltage. This disables the internal LDO-D regulator. If both LDO's are disabled, the BREF will be automatically disabled, too. The BREF must be manually enabled before re-enabling either LDO.
4	ext_vcca	When set, the core analog (vcca) pin is driven with an externally regulated voltage. This disables the internal LDO-A regulator. If both LDO's are disabled, the BREF will be automatically disabled, too. The BREF must be manually enabled before re-enabling either LDO.
0	rbbnw_dis	When set, disables the nwell reverse biasing during low power modes. Nwell reverse biasing is always disabled during active/standby modes.

1.3.45 PWRSYS_CR1

Power System Control Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_CR1: 0x4331

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	R/W:0	R/W:0
HW Access	NA					R	R	R
Retention	NA					RET	RET	RET
Name	RSVD					i2creg_backup	ldoa_dis	ldoa_iso

This register controls the voltage regulators.

Bits	Name	Description
2	i2creg_backup	When set, enables the I2C regulator backup. The I2C backup regulator enables the I2C logic to wake the chip from sleep mode on an I2C address match.
1	ldoa_dis	When set, disables the analog LDO regulator. This bit will not be set unless the ldoa_iso field is already set. Attempts to set this field while simultaneously clearing ldoa_iso will be ignored.
0	ldoa_iso	When set, prepares the system to disable the LDO-A. In this mode, the LV reference (bandgap) is supplied by the digital LDO. Also, outputs of vcca are isolated from the rest of the system. Note that this mode can result in degraded accuracy, as described in the Power Modes chapter. Once set, cannot be cleared unless ldoa_dis is already clear.

1.3.46 PM_TW_CFG0

Timewheel Configuration Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_TW_CFG0: 0x4380

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	ftw_interval							

This register controls settings for the fast timewheel. If using low power active (LPA) mode, the fast timewheel must be used to program the burst period.

Bits	Name	Description
7:0	ftw_interval[7:0]	Sets the fast timewheel interval. The fast timewheel is programmed using a 8-bit terminal count (N-1) and is clocked by the ILO at 100 kHz. When the terminal count is reached, the timewheel automatically resets and begins counting again. This value can only be changed when {PM.TW_CFG2}.ftw_en is clear. After enabling, the duration before the first event is between 1 and 2 additional cycles, depending on synchronization with the ILO clock. Additional events occur periodically with a period of (1+ftw_interval).

1.3.47 PM_TW_CFG1

Timewheel Configuration Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_TW_CFG1: 0x4381

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:1001			
HW Access	NA				R			
Retention	NA				RET			
Name	RSVD				ctw_interval			

This register controls settings for the central timewheel.

Bits	Name	Description
3:0	ctw_interval[3:0]	Sets the central timewheel interval. The period is based on the ILO running at 1 kHz. When the interval is reached, it is automatically restarted. The first interval can range from 1 to (period + 1) ms. Additional intervals occur at the nominal period. This value can only be changed when {TW_CFG2}.ctw_en is clear. See Table 1-66.

Table 1-66. Bit field encoding: ctw_interval_enum

Value	Name	Description
4'b0000	CTW_1_TICK	not presently supported ==> is same as CTW_2_TICKS
4'b0001	CTW_2_TICKS	2 CTW ticks ==> 2ms (nominal)
4'b0010	CTW_4_TICKS	4 CTW ticks ==> 4ms (nominal)
4'b0011	CTW_8_TICKS	8 CTW ticks ==> 8ms (nominal)
4'b0100	CTW_16_TICKS	16 CTW ticks ==> 16ms (nominal)
4'b0101	CTW_32_TICKS	32 CTW ticks ==> 32ms (nominal)
4'b0110	CTW_64_TICKS	64 CTW ticks ==> 64ms (nominal)
4'b0111	CTW_128_TICKS	128 CTW ticks ==> 128ms (nominal)
4'b1000	CTW_256_TICKS	256 CTW ticks ==> 256ms (nominal)
4'b1001	CTW_512_TICKS	512 CTW ticks ==> 512ms (nominal)
4'b1010	CTW_1024_TICKS	1024 CTW ticks ==> 1024ms (nominal)
4'b1011	CTW_2048_TICKS	2048 CTW ticks ==> 2048ms (nominal)
4'b1100	CTW_4096_TICKS	4096 CTW ticks ==> 4096ms (nominal)

1.3.48 PM_TW_CFG2

Timewheel Configuration Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_TW_CFG2: 0x4382

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R	R	R	R	R	R
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		onepps_ie	onepps_en	ctw_ie	ctw_en	ftw_ie	ftw_en

This register controls settings for the central and fast timewheels.

Bits	Name	Description
5	onepps_ie	When set and one pulse-per-second is enabled, an interrupt is issued when the pulse occurs. If onepps_en is not enabled, no interrupt is generated.
4	onepps_en	When set, the system returns to the active global power mode once every second. The 32 kHz external crystal oscillator must be enabled to use the one pulse-per-second function.
3	ctw_ie	When set and the central timewheel is enabled, an interrupt is issued when the central timewheel reaches the selected interval. If ctw_en is not enabled, no interrupt is generated.
2	ctw_en	When set, the system returns to the active global power mode when the central timewheel reaches the interval selected in {PM.TW_CFG1}.ctw_interval. The ILO 1 kHz clock source must be enabled to use the central timewheel.
1	ftw_ie	When set and the fast timewheel is enabled, an interrupt is issued when it reaches the terminal count. If ftw_en is not enabled, no interrupt is generated. This bit is ignored when LPA is enabled, and no interrupts are issued.
0	ftw_en	When set, the system returns to the active global power mode when the fast timewheel reaches the terminal count selected in {PM.TW_CFG0}.ftw_interval. This bit should be set when using Low Power Active (lpa) mode, since the fast timewheel is usually used to control the LPA burst period. The ILO 100 kHz clock source must be enabled to use the fast timewheel.

1.3.49 PM_WDT_CFG

Watchdog Timer Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_WDT_CFG: 0x4383

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:01		R/W:0	NA:00		R/W:01	
HW Access	R	R		R	NA		R	
Retention	RET	RET		RET	NA		RET	
Name	ctw_reset	wdt_lpmode		wdr_en	RSVD		wdt_interval	

This register controls the watchdog timer (WDT) settings.

Bits	Name	Description
7	ctw_reset	When a one is written to this field, the free-running central timewheel counter is reset to 0 and held there. Firmware must then write a zero to exit the reset state. Since the central timewheel is used for many timing tasks (including buzz timing and WDT), care must be taken when resetting it. It is generally recommended to reset it only once when the watchdog is enabled, to ensure that first watchdog period is full. Cannot be changed after the watchdog is enabled.
6:5	wdt_lpmode[1:0]	If the Watchdog-Timer (WDT) is enabled, these 2 bits are used to define how the WDT behaves when the part enters Sleep/Idle/Hibtimers (low power) mode. By default (wdt_lpmode is left 01), the system will automatically use the longest WDT interval when Sleep/Idle/Hibtimers mode is entered - so SW isn't burdened with waking just to feed the WDT. This is true regardless of the value programmed in the wdt_interval register. Upon wakeup, the interval will remain at the highest setting until the WDT is fed the first time by the user. A feeding at this point will cause the interval to automatically return to the normal setting (value in wdt_interval). If this field is set to NOCHANGE ('00'), the system does not change the interval and does not feed the WDT when entering Sleep/Idle/Hibtimers mode. If DISABLED (wdt_lpmode=11), the WDT is turned off when Sleep/Idle/Hibtimers mode is entered and remains disabled until the first feeding by the user after Active mode is reentered. This field cannot be changed once {PM.WDT_CFG}.wdr_en is set. See Table 1-68.
4	wdr_en	When set, enables the watchdog reset (WDR) using the current WDT settings. Once enabled, the WDT cannot be disabled except by a reset. Setting this bit automatically enables the ILO 1 kHz clock source.
1:0	wdt_interval[1:0]	Selects the central timewheel taps that control the WDT period. The accuracy of the intervals are dependent upon the accuracy of the oscillator used. A watchdog reset (WDR) may be issued at any time within the selected interval, so software should be programmed to service the WDT before the lower bound is reached (two tap periods). A WDR is always issued within three tap periods. Once {PM.WDT_CFG}.wdr_en is set, the watchdog interval cannot be changed. See Table 1-67.

Table 1-67. Bit field encoding: wdt_interval_enum

Value	Name	Description
2'b00	WDT_2_TICKS	2 CTW ticks ==> 4ms - 6ms
2'b01	WDT_16_TICKS	16 CTW ticks ==> 32ms - 48ms
2'b10	WDT_128_TICKS	128 CTW ticks ==> 256ms - 384ms
2'b11	WDT_1024_TICKS	1024 CTW ticks ==> 2.048s - 3.072s

(continued)

Table 1-68. Bit field encoding: wdt_lpmode_enum

Value	Name	Description
2'b00	WDT_LPMODE_NOCHANGE	WDT does not change behavior when Sleep/Idle Mode/Hibtimers is entered
2'b01	WDT_LPMODE_MAXINTER	WDT automatically switches to max interval when Sleep/Idle/Hibtimers Mode is entered
2'b10	WDT_LPMODE_RESERVED	Reserved (acts the same as NOCHANGE)
2'b11	WDT_LPMODE_DISABLED	WDT is disabled when Sleep/Idle/Hibtimers Mode is entered

1.3.50 PM_WDT_CR

Watchdog Timer Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_WDT_CR: 0x4384

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/WOC:00000000							
HW Access	NA							
Retention	RET							
Name	wdt_clear							

This register is used to feed the watchdog timer (WDT).

Bits	Name	Description
7:0	wdt_clear[7:0]	Any write to this field feeds the WDT. After each feeding, there are at least two entire watchdog timer tap periods before a WDR occurs. Always reads as zero.

1.3.51 PM_INT_SR

Power Manager Interrupt Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_INT_SR: 0x4390

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				RC:0	RC:0	RC:0	RC:0
HW Access	NA				R/W	R/W	R/W	R/W
Retention	NA				RET	RET	RET	RET
Name	RSVD				limact_int	onepps_int	ctw_int	ftw_int

This register indicates which interrupts occured since the last read of the register. All bits are automatically cleared on read. If an interrupt gets generated at the same time as a clear, the bit will remain set (which causes another interrupt).

Bits	Name	Description
3	limact_int	When set, a limited active ready event has occured. The setting of limact_ie determines whether this interrupt condition is masked or propagated to the interrupt controller. Sticky (whole field)
2	onepps_int	When set, a onepps event has occured. The setting of onepps_ie determines whether this interrupt condition is masked or propagated to the interrupt controller. Sticky (whole field)
1	ctw_int	When set, a central timewheel event has occured. The setting of ctw_ie determines whether this interrupt condition is masked or propagated to the interrupt controller. Sticky (whole field)
0	ftw_int	When set, a fast timewheel event has occured. The setting of ftw_ie determines whether this interrupt condition is masked or propagated to the interrupt controller. Sticky (whole field)

1.3.52 PM_MODE_CFG0

Power Mode Configuration Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_MODE_CFG0: 0x4391

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	lpa_cycles							

This register controls settings for the low power modes.

Bits	Name	Description
7:0	lpa_cycles[7:0]	A setting of N causes (N+1) cycles to execute during each burst

1.3.53 PM_MODE_CFG1

Power Mode Configuration Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_MODE_CFG1: 0x4392

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	NA:0	R/W:0	R/W:0
HW Access	NA				R	NA	R	R
Retention	NA				RET	NA	RET	RET
Name	RSVD				limact_ie	RSVD	lpa_fie	lpa_en

This register controls settings for the low power modes.

Bits	Name	Description
3	limact_ie	Setting this bit will issue an interrupt when the system can return from limited active to fully active mode. To reliably generate the interrupt, this bit should be set prior to entering idle mode.
1	lpa_fie	When clear, interrupts are held off until next burst. This increases average interrupt latency, as compared to an active mode baseline design with identical throughput. When set, interrupts return the system to active mode, the on-time counter is reset, and the system will execute at least N cycles.
0	lpa_en	When set, LPA mode is enabled. LPA mode is compatible with all global power modes. If standby mode is specified, it is interpreted as an early return to standby, and the LPA scheduler will wake the system on the original schedule. If idle, sleep, or hibernate modes are specified, LPA is temporarily paused and resumed upon wakeup. Clearing this bit immediately disables LPA.

1.3.54 PM_MODE_CSR

Power Mode Control/Status Register

Reset: Reset Signals Listed Below

Register : Address

PM_MODE_CSR: 0x4393

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/WC:1	R:0	NA:0	R/WOC:0	R:1	R/W:000		
HW Access	W	W	NA	R	W	R/W		
Retention	NONRET	RET	NA	RET	RET	RET		
Name	nonret_rst	limact_mode	RSVD	reactivate	pwrup_pulse_q	lp_mode		

This register controls settings for the global power mode.

Bits	Name	Description
7	nonret_rst	Persistent status bit that indicates a non-retention reset occured for some chip registers. This bit is preset high by any chip reset, and it is cleared whenever the register is written. When the system automatically resets non-retention registers (such as when returning from low power modes or a reactivation), this field is set high to indicate some register state has changed. Sticky (whole field)
6	limact_mode	When set, the chip is in limited active mode. Some subsystems and domains are unavailable in this mode. A reactivation is required to return the chip to active mode.
4	reactivate	Setting this bit reactivates subsystems with pending availability. This is used to transition from limited active to active mode or to initiate the delayed activation procedure after change(s) to PM_AVAIL* register(s). The reactivation process simulates a transition from sleep to active mode. During the simulated transition, user clocks are stopped. After completion, the system is in active mode regardless of the LP_MODE setting. This bit always reads as zero.
3	pwrup_pulse_q	When set, indicates that the chip is internally waiting for the hibernate/sleep regulator to stabilize. The chip will ignore LP requests for idle, sleep, and hibernate modes until the regulator is stable.
2:0	lp_mode[2:0]	Sets the global power mode. See Table 1-69.

Reset Table

Reset Signal	Applicable Register Bit(s)
System reset for retention flops [reset_all_retention]	lp_mode[2:0], pwrup_pulse_q, reactivate, test_domains, limact_mode
Domain reset for non-retention flops [reset_all_nonretention]	nonret_rst

Table 1-69. Bit field encoding: mode_enum

Value	Name	Description
3'b000	MODE_ACTIVE	Active mode
3'b001	MODE_STANDBY	Standby mode
3'b010	MODE_IDLE	Idle mode
3'b011	MODE_SLEEP	Sleep mode
3'b100	MODE_HIBERNATE	Hibernate mode
3'b110	MODE_HIBTIMERS	Hibernate+timewheels

1.3.55 PM_USB_CR0

USB Power Mode Control Register 0

Reset: Reset Signals Listed Below

Register : Address

PM_USB_CR0: 0x4394

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	R/W:1	R/W:0
HW Access	NA					R	R	R
Retention	NA					NONRET	RET	RET
Name	RSVD					fsusbio_pd_pullup_n	fsusbio_pd_n	fsusbio_ref_en

This register controls settings for USB low power mode.

Bits	Name	Description
2	fsusbio_pd_pullup_n	USB IO pad pullup enable. When set, the USBIO pad pullups can be used. When clear, the pullups are forced off. The pullups cannot be enabled until the appropriate supply is available. For example, if the USB regulator is configured, it must be stable before enabling the pullup or it may result in output glitches. The general guideline is to wait at least 2us after setting fsusbio_pd_n=1 before setting this field. This requirement is in addition to the reference settling time (if applicable).
1	fsusbio_pd_n	USB IO pad enable. When set, the USBIO pads can be used. When clear, the USBIO pads latch their previous settings and powerdown. This field must be high to use the pads for USB or GPIO modes. If USB is unavailable (wounded) the pads will ignore this setting and will remain disabled.
0	fsusbio_ref_en	USB IO pad receiver and regulator reference enable. The reference is required when using the USBIO pins for USB signaling. It is used by the differential receiver and USB regulator. The reference is NOT required when using the USBIO pins for GPIO signaling. Before enabling USB signaling in {USB_CR0}, enable this bit and allow the reference to settle. Settling time is max(1us after enabling, 40us after power restored). Power loss occurs during reset or when entering a deep low power mode (idle, sleep, or hibernate). Power is considered restored when reset deasserts or when the core supply reaches the PRES threshold after a wakeup. This field is retained so that if the core supply is kept up (eg. idle or sleep), the delay can be measured from the wakeup event.

Reset Table

Reset Signal	Applicable Register Bit(s)
System reset for retention flops [reset_all_retention]	fsusbio_ref_en, fsusbio_pd_n
Domain reset for non-retention flops [reset_all_nonretention]	fsusbio_pd_pullup_n

1.3.56 PM_WAKEUP_CFG0

Power Mode Wakeup Mask Configuration Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_WAKEUP_CFG0: 0x4398

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:1	R/W:1	R/W:1	R/W:1	R/W:1	R/W:1	R/W:1	R/W:1
HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	mask_sleep	mask_clkpm	mask_boost	mask_cpu	mask_i2c	mask_picu	mask_tc	mask_int

This register masks the power mode wakeup sources.

Bits	Name	Description
7	mask_sleep	When set, the PM CTW and PM 1PPS (RTC) can return the chip to active mode.
6	mask_clkpm	When set, the PM FTW, LVI or HVI can return the chip to active mode.
5	mask_boost	When set, boost undervoltage can return the chip to active mode.
4	mask_cpu	When set, a CPU bus transaction can return the chip to active mode.
3	mask_i2c	When set, I2C can return the chip to active mode.
2	mask_picu	When set, the PICU can return the chip to active mode.
1	mask_tc	When set, the Test Controller can return the chip to active mode.
0	mask_int	When set, on-chip interrupts can return the chip to active mode.

1.3.57 PM_WAKEUP_CFG1

Power Mode Wakeup Mask Configuration Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_WAKEUP_CFG1: 0x4399

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:1	R/W:1	R/W:1	R/W:1	R/W:1	R/W:1	R/W:1	R/W:1
HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	mask_cmp7	mask_cmp6	mask_cmp5	mask_cmp4	mask_cmp3	mask_cmp2	mask_cmp1	mask_cmp0

This register masks the power mode wakeup sources.

Bits	Name	Description
7	mask_cmp7	Reserved for comparator 7
6	mask_cmp6	Reserved for comparator 6
5	mask_cmp5	Reserved for comparator 5
4	mask_cmp4	Reserved for comparator 4
3	mask_cmp3	When set, comparator 3 can return the chip to active mode.
2	mask_cmp2	When set, comparator 2 can return the chip to active mode.
1	mask_cmp1	When set, comparator 1 can return the chip to active mode.
0	mask_cmp0	When set, comparator 0 can return the chip to active mode.

1.3.58 PM_WAKEUP_CFG2

Power Mode Wakeup Mask Configuration Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_WAKEUP_CFG2: 0x439A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:1
HW Access	NA							R
Retention	NA							RET
Name	RSVD							mask_lcd

This register masks the power mode wakeup sources.

Bits	Name	Description
0	mask_lcd	When set, LCD can return the chip to active mode.

1.3.59 PM_ACT_CFG0

Active Power Mode Configuration Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG0: 0x43A0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:1	R/W:0	R/W:1	R/W:1	R/W:1
HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	en_delay	en_udbarray	en_imo36m	en_imo	en_clk_spc	en_clk_bus	en_cpu	en_ic

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

Bits	Name	Description
7	en_delay	Global enable for clkdist delay line. For analog clocks (ACLKs) to be running this bit must be set, When this bit is LOW the ACLKs can't toggle.
6	en_udbarray	Global enable for UDB array.
5	en_imo36m	Enable IMO SPC clock source. This also internally enables the IMO, since it is required for the 36MHz IMO to function.
4	en_imo	Enable IMO clock source. Any wakeup event will set this bit.
3	en_clk_spc	Enable clk_spc. This also internally enables the 36MHz IMO (similar to en_imo36m), since this is required for the SPC to function.
2	en_clk_bus	Enable clk_bus. Any wakeup event (including bus access from the CPU) will automatically set this bit.
1	en_cpu	Enable CPU. This also enables the flash, since the CPU requires the flash to function. Any wake-up event will set this bit.
0	en_ic	Enable interrupt controller

1.3.60 PM_ACT_CFG1

Active Power Mode Configuration Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG1: 0x43A1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Retention	NA				RET			
Name	RSVD				en_clk_a			

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

Bits	Name	Description
3:0	en_clk_a[3:0]	Enable clk_a[3:0]

1.3.61 PM_ACT_CFG2

Active Power Mode Configuration Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG2: 0x43A2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	en_clk_d							

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

Bits	Name	Description
7:0	en_clk_d[7:0]	Enable clk_d[7:0]

1.3.62 PM_ACT_CFG3

Active Power Mode Configuration Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG3: 0x43A3

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Retention	NA				RET			
Name	RSVD				en_timer			

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

Bits	Name	Description
3:0	en_timer[3:0]	Enable timer/counters.

1.3.63 PM_ACT_CFG4

Active Power Mode Configuration Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG4: 0x43A4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Retention	NA				RET			
Name	RSVD				en_opamp			

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

Bits	Name	Description
3:0	en_opamp[3:0]	Enable analog linear output buffer.

1.3.64 PM_ACT_CFG5

Active Power Mode Configuration Register 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG5: 0x43A5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0
HW Access	NA	R	NA	R	NA	R	NA	R
Retention	NA	RET	NA	RET	NA	RET	NA	RET
Name	RSVD	en_emif	RSVD	en_lcd	RSVD	en_i2c	RSVD	en_fsusb

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

Bits	Name	Description
6	en_emif	Enable EMIF
4	en_lcd	Enable LCD.
2	en_i2c	Enable I2C block(s). Populated subsystems are counted from the LSB.
0	en_fsusb	Enable FS-USB.

1.3.65 PM_ACT_CFG6

Active Power Mode Configuration Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG6: 0x43A6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	NA:000			R/W:0
HW Access	NA			R	NA			R
Retention	NA			RET	NA			RET
Name	RSVD			en_dfb	RSVD			en_can

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

Bits	Name	Description
4	en_dfb	Enable DFB(s). Populated subsystems are counted from the LSB.
0	en_can	Enable CAN block(s). Populated subsystems are counted from the LSB.

1.3.66 PM_ACT_CFG7

Active Power Mode Configuration Register 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG7: 0x43A7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Retention	NA				RET			
Name	RSVD				en_cmp			

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

Bits	Name	Description
3:0	en_cmp[3:0]	Enable comparator(s). Populated subsystems are counted from the LSB, for example bit 0 corresponds to comparator 0.

1.3.67 PM_ACT_CFG8

Active Power Mode Configuration Register 8

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG8: 0x43A8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Retention	NA				RET			
Name	RSVD				en_dac			

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

Bits	Name	Description
3:0	en_dac[3:0]	Enable DAC block(s). Populated subsystems are counted from the LSB.

1.3.68 PM_ACT_CFG9

Active Power Mode Configuration Register 9

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG9: 0x43A9

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Retention	NA				RET			
Name	RSVD				en_swcap			

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

Bits	Name	Description
3:0	en_swcap[3:0]	Enable switchcap block(s). Populated subsystems are counted from the LSB, for example bit 0 corresponds to switchcap block 0.

1.3.69 PM_ACT_CFG10

Active Power Mode Configuration Register 10

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG10: 0x43AA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	NA:000			R/W:0
HW Access	NA			R	NA			R
Retention	NA			RET	NA			RET
Name	RSVD			en_dsm_channel	RSVD			en_dec

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

Bits	Name	Description
4	en_dsm_channel	Enable delta-sigma modulator ADC channel. Note: set the appropriate enables in the analog interface prior to setting this global enable for the channel.
0	en_dec	Enable decimator(s). Populated subsystems are counted from the LSB.

1.3.70 PM_ACT_CFG11

Active Power Mode Configuration Register 11

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG11: 0x43AB

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	NA:0000			
HW Access	NA		R	R	NA			
Retention	NA		RET	RET	NA			
Name	RSVD		en_refbufr	en_refbufl	RSVD			

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

Bits	Name	Description
5	en_refbufr	Enable RIGHT analog reference buffer (refbufr)
4	en_refbufl	Enable LEFT analog reference buffer (refbufl)

1.3.71 PM_ACT_CFG12

Active Power Mode Configuration Register 12

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG12: 0x43AC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	NA:000			R/W:1
HW Access	NA			R	NA			R
Retention	NA			RET	NA			RET
Name	RSVD			en_ee	RSVD			en_fm

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

Bits	Name	Description
4	en_ee	Enable EEPROM. Re-enabling an EEPROM macro takes 5us. During this time, the EE will not acknowledge a PHUB request.
0	en_fm	Enable flash. Active flash macros consume current, but re-enabling a disabled flash macro takes 5us. If the CPU attempts to fetch out of the macro during that time, it will be stalled. This bit allows the flash to be enabled even if the CPU is disabled, which allows a quicker return to code execution. To avoid a deadlock where the CPU attempts to fetch out of a disabled macro, the flash macro will ignore this bit if the CPU is enabled in user mode. During test mode, the flash CAN be turned off independently from the CPU.

1.3.72 PM_ACT_CFG13

Active Power Mode Configuration Register 13

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_ACT_CFG13: 0x43AD

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:1	R/W:1	R/W:1	R/W:1
HW Access	NA				R	R	R	R
Retention	NA				RET	RET	RET	RET
Name	RSVD				en_ports	en_picu	en_sysmem	en_anaif

This register enables subsystems during the active power mode. Attempts to enable unavailable subsystems are ignored.

Bits	Name	Description
3	en_ports	Enable ports. This must be enabled to read/write registers in the port logic.
2	en_picu	Enable PICU. This must be enabled to read/write registers in the PICU. Configured wakeups will continue to function if the PICU is disabled, but the interface must be enabled to clear the interrupt condition.
1	en_sysmem	Enable SYSMEM. This must be enabled to read/write the SYSMEM.
0	en_anaif	Enable analog interface. This must be enabled to read/write registers in the analog interface.

1.3.73 PM_STBY_CFG0

Standby Power Mode Configuration Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG0: 0x43B0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	en_delay	en_udbarray	en_imo36m	en_imo	en_clk_spc	en_clk_bus	en_cpu	en_ic

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

Bits	Name	Description
7	en_delay	Global enable for clkdist delay line. For analog clocks (ACLKs) to be running this bit must be set, When this bit is LOW the ACLKs can't toggle.
6	en_udbarray	Global enable for UDB array.
5	en_imo36m	Enable IMO SPC clock source. This also internally enables the IMO, since it is required for the 36MHz IMO to function.
4	en_imo	Enable IMO clock source. Any wakeup event will set this bit.
3	en_clk_spc	Enable clk_spc. This also internally enables the 36MHz IMO (similar to en_imo36m), since this is required for the SPC to function.
2	en_clk_bus	Enable clk_bus. Any wakeup event (including bus access from the CPU) will automatically set this bit.
1	en_cpu	Enable CPU. This also enables the flash, since the CPU requires the flash to function. Any wake-up event will set this bit.
0	en_ic	Enable interrupt controller

1.3.74 PM_STBY_CFG1

Standby Power Mode Configuration Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG1: 0x43B1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Retention	NA				RET			
Name	RSVD				en_clk_a			

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

Bits	Name	Description
3:0	en_clk_a[3:0]	Enable clk_a[3:0]

1.3.75 PM_STBY_CFG2

Standby Power Mode Configuration Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG2: 0x43B2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	en_clk_d							

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

Bits	Name	Description
7:0	en_clk_d[7:0]	Enable clk_d[7:0]

1.3.76 PM_STBY_CFG3

Standby Power Mode Configuration Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG3: 0x43B3

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Retention	NA				RET			
Name	RSVD				en_timer			

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

Bits	Name	Description
3:0	en_timer[3:0]	Enable timer/counters.

1.3.77 PM_STBY_CFG4

Standby Power Mode Configuration Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG4: 0x43B4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Retention	NA				RET			
Name	RSVD				en_opamp			

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

Bits	Name	Description
3:0	en_opamp[3:0]	Enable analog linear output buffer.

1.3.78 PM_STBY_CFG5

Standby Power Mode Configuration Register 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG5: 0x43B5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0
HW Access	NA	R	NA	R	NA	R	NA	R
Retention	NA	RET	NA	RET	NA	RET	NA	RET
Name	RSVD	en_emif	RSVD	en_lcd	RSVD	en_i2c	RSVD	en_fsusb

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

Bits	Name	Description
6	en_emif	Enable EMIF
4	en_lcd	Enable LCD.
2	en_i2c	Enable I2C block(s). Populated subsystems are counted from the LSB.
0	en_fsusb	Enable FS-USB.

1.3.79 PM_STBY_CFG6

Standby Power Mode Configuration Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG6: 0x43B6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	NA:000			R/W:0
HW Access	NA			R	NA			R
Retention	NA			RET	NA			RET
Name	RSVD			en_dfb	RSVD			en_can

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

Bits	Name	Description
4	en_dfb	Enable DFB(s). Populated subsystems are counted from the LSB.
0	en_can	Enable CAN block(s). Populated subsystems are counted from the LSB.

1.3.80 PM_STBY_CFG7

Standby Power Mode Configuration Register 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG7: 0x43B7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Retention	NA				RET			
Name	RSVD				en_cmp			

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

Bits	Name	Description
3:0	en_cmp[3:0]	Enable comparator(s). Populated subsystems are counted from the LSB, for example bit 0 corresponds to comparator 0.

1.3.81 PM_STBY_CFG8

Standby Power Mode Configuration Register 8

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG8: 0x43B8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Retention	NA				RET			
Name	RSVD				en_dac			

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

Bits	Name	Description
3:0	en_dac[3:0]	Enable DAC block(s). Populated subsystems are counted from the LSB.

1.3.82 PM_STBY_CFG9

Standby Power Mode Configuration Register 9

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG9: 0x43B9

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Retention	NA				RET			
Name	RSVD				en_swcap			

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

Bits	Name	Description
3:0	en_swcap[3:0]	Enable switchcap block(s). Populated subsystems are counted from the LSB, for example bit 0 corresponds to switchcap block 0.

1.3.83 PM_STBY_CFG10

Standby Power Mode Configuration Register 10

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG10: 0x43BA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	NA:000			R/W:0
HW Access	NA			R	NA			R
Retention	NA			RET	NA			RET
Name	RSVD			en_dsm_channel	RSVD			en_dec

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

Bits	Name	Description
4	en_dsm_channel	Enable delta-sigma modulator ADC channel. Note: set the appropriate enables in the analog interface prior to setting this global enable for the channel.
0	en_dec	Enable decimator(s). Populated subsystems are counted from the LSB.

1.3.84 PM_STBY_CFG11

Standby Power Mode Configuration Register 11

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG11: 0x43BB

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	NA:0000			
HW Access	NA		R	R	NA			
Retention	NA		RET	RET	NA			
Name	RSVD		en_refbufr	en_refbufl	RSVD			

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

Bits	Name	Description
5	en_refbufr	Enable RIGHT analog reference buffer (refbufr)
4	en_refbufl	Enable LEFT analog reference buffer (refbufl)

1.3.85 PM_STBY_CFG12

Standby Power Mode Configuration Register 12

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG12: 0x43BC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	NA:000			R/W:0
HW Access	NA			R	NA			R
Retention	NA			RET	NA			RET
Name	RSVD			en_ee	RSVD			en_fm

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

Bits	Name	Description
4	en_ee	Enable EEPROM. Re-enabling an EEPROM macro takes 5us. During this time, the EE will not acknowledge a PHUB request.
0	en_fm	Enable flash. Active flash macros consume current, but re-enabling a disabled flash macro takes 5us. If the CPU attempts to fetch out of the macro during that time, it will be stalled. This bit allows the flash to be enabled even if the CPU is disabled, which allows a quicker return to code execution. To avoid a deadlock where the CPU attempts to fetch out of a disabled macro, the flash macro will ignore this bit if the CPU is enabled in user mode. During test mode, the flash CAN be turned off independently from the CPU.

1.3.86 PM_STBY_CFG13

Standby Power Mode Configuration Register 13

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_STBY_CFG13: 0x43BD

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Retention	NA				RET	RET	RET	RET
Name	RSVD				en_ports	en_picu	en_sysmem	en_anaif

This register enables subsystems during the standby power mode. Attempts to enable unavailable subsystems are ignored.

Bits	Name	Description
3	en_ports	Enable ports. This must be enabled to read/write registers in the port logic.
2	en_picu	Enable PICU. This must be enabled to read/write registers in the PICU. Configured wakeups will continue to function if the PICU is disabled, but the interface must be enabled to clear the interrupt condition.
1	en_sysmem	Enable SYSMEM. This must be enabled to read/write the SYSMEM.
0	en_anaif	Enable analog interface. This must be enabled to read/write registers in the analog interface.

1.3.87 PM_AVAIL_CR0

Power Mode Available Subsystem Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_CR0: 0x43C0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:1
HW Access	NA							R
Retention	NA							RET
Name	RSVD							avail_fm

This register allows subsystems to be flagged as available or unavailable. Flagging a subsystem unavailable can result in lower power consumption during returns from sleep and hibernate. Some subsystems can only be flagged unavailable during test mode.

Bits	Name	Description
0	avail_fm	Each set bit requests a flash macro be available. Reactivation is delayed. Macro 0 can only be disabled during test_mode.

1.3.88 PM_AVAIL_CR1

Power Mode Available Subsystem Control Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_CR1: 0x43C1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:11	
HW Access	NA						R	
Retention	NA						RET	
Name	RSVD						avail_sysmem	

This register allows subsystems to be flagged as available or unavailable. Flagging a subsystem unavailable can result in lower power consumption during returns from sleep and hibernate. Some subsystems can only be flagged unavailable during test mode.

Bits	Name	Description
1:0	avail_sysmem[1:0]	Each set bit requests a sysmem macro be available. Reactivation is delayed. Populated subsystems are counted from the LSB.

1.3.89 PM_AVAIL_CR2

Power Mode Available Subsystem Control Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_CR2: 0x43C2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:1	NA:000			R/W:1
HW Access	NA			R	NA			R
Retention	NA			RET	NA			RET
Name	RSVD			avail_udb	RSVD			avail_ee

This register allows subsystems to be flagged as available or unavailable. Flagging a subsystem unavailable can result in lower power consumption during returns from sleep and hibernate. Some subsystems can only be flagged unavailable during test mode.

Bits	Name	Description
4	avail_udb	Each set bit requests a UDB bank be available. Reactivation is delayed. This bit should never be cleared if the the UDB is enabled. If this bit is cleared, then the application must reconfigure the UDB.
0	avail_ee	Each set bit requests a EEPROM macro be available. Reactivation is delayed.

1.3.90 PM_AVAIL_CR3

Power Mode Available Subsystem Control Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_CR3: 0x43C3

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:1	NA:000			R/W:1
HW Access	NA			R	NA			R
Retention	NA			RET	NA			RET
Name	RSVD			avail_sysmemtrace	RSVD			avail_dfb

This register allows subsystems to be flagged as available or unavailable. Flagging a subsystem unavailable can result in lower power consumption during returns from sleep and hibernate. Some subsystems can only be flagged unavailable during test mode.

Bits	Name	Description
4	avail_sysmemtrace	Each set bit requests a trace memory be available. Reactivation is delayed.
0	avail_dfb	Each set bit requests a DFB be available. Reactivation is delayed.

1.3.91 PM_AVAIL_CR4

Power Mode Available Subsystem Control Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_CR4: 0x43C4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:1	NA:0	R/W:1	NA:0	R/W:1
HW Access	NA			R	NA	R	NA	R
Retention	NA			RET	NA	RET	NA	RET
Name	RSVD			avail_i2c	RSVD	avail_main	RSVD	avail_spc

This register allows subsystems to be flagged as available or unavailable. Flagging a subsystem unavailable can result in lower power consumption during returns from sleep and hibernate. Some subsystems can only be flagged unavailable during test mode.

Bits	Name	Description
4	avail_i2c	When set, requests I2C be available. Reactivation is delayed.
2	avail_main	When set, requests main domain be available (default and necessary for most functionality). The main domain can only be disabled in test mode. There is no isolation in the UDB, DSM or the pumps, so also set avail_udb, avail_dsm_channel and avail_anapump low to avoid static current. Reactivation is delayed.
0	avail_spc	When set, requests SPC be available. Reactivation is delayed.

1.3.92 PM_AVAIL_CR5

Power Mode Available Subsystem Control Register 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_CR5: 0x43C5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:1
HW Access	NA							R
Retention	NA							RET
Name	RSVD							avail_dsm_ channel

This register allows subsystems to be flagged as available or unavailable. Flagging a subsystem unavailable can result in lower power consumption during returns from sleep and hibernate. Some subsystems can only be flagged unavailable during test mode.

Bits	Name	Description
0	avail_dsm_channel	Each set bit requests a delsig channel be available. Reactivation is immediate.

1.3.93 PM_AVAIL_CR6

Power Mode Available Subsystem Control Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_CR6: 0x43C6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:1	NA:00		R/W:1	R/W:1
HW Access	NA			R	NA		R	R
Retention	NA			RET	NA		RET	RET
Name	RSVD			avail_anamisc2	RSVD		avail_anapump	avail_anamisc

This register allows subsystems to be flagged as available or unavailable. Flagging a subsystem unavailable can result in lower power consumption during returns from sleep and hibernate. Some subsystems can only be flagged unavailable during test mode.

Bits	Name	Description
4	avail_anamisc2	When set, requests miscellaneous analog (group 2) be available. This register is a placeholder and presently has no fanout. Reactivation is immediate.
1	avail_anapump	When set, requests analog pump be available. Reactivation is immediate.
0	avail_anamisc	When set, requests miscellaneous analog be available. Reactivation is immediate.

1.3.94 PM_AVAIL_SR0

Power Mode Available Subsystem Status Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_SR0: 0x43D0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R:1
HW Access	NA							W
Retention	NA							RET
Name	RSVD							avail_fm

This register indicates whether a subsystem is available or not.

Bits	Name	Description
0	avail_fm	Each set bit indicates an available flash macro.

1.3.95 PM_AVAIL_SR1

Power Mode Available Subsystem Status Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_SR1: 0x43D1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R:11	
HW Access	NA						W	
Retention	NA						RET	
Name	RSVD						avail_sysmem	

This register indicates whether a subsystem is available or not.

Bits	Name	Description
1:0	avail_sysmem[1:0]	Each set bit requests a sysmem macro be available. Reactivation is delayed. Populated subsystems are counted from the LSB.

1.3.96 PM_AVAIL_SR2

Power Mode Available Subsystem Status Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_SR2: 0x43D2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R:1	NA:000			R:1
HW Access	NA			W	NA			W
Retention	NA			RET	NA			RET
Name	RSVD			avail_udb	RSVD			avail_ee

This register indicates whether a subsystem is available or not.

Bits	Name	Description
4	avail_udb	Each set bit indicates an available UDB bank.
0	avail_ee	Each set bit indicates an available EEPROM macro.

1.3.97 PM_AVAIL_SR3

Power Mode Available Subsystem Status Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_SR3: 0x43D3

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R:1	NA:000			R:1
HW Access	NA			W	NA			W
Retention	NA			RET	NA			RET
Name	RSVD			avail_sysmemtrace	RSVD			avail_dfb

This register indicates whether a subsystem is available or not.

Bits	Name	Description
4	avail_sysmemtrace	Each set bit indicates an available trace memory.
0	avail_dfb	Each set bit indicates an available DFB.

1.3.98 PM_AVAIL_SR4

Power Mode Available Subsystem Status Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_SR4: 0x43D4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R:1	NA:0	R:1	NA:0	R:1
HW Access	NA			W	NA	W	NA	W
Retention	NA			RET	NA	RET	NA	RET
Name	RSVD			avail_i2c	RSVD	avail_main	RSVD	avail_spc

This register indicates whether a subsystem is available or not.

Bits	Name	Description
4	avail_i2c	When set, I2C is available.
2	avail_main	When set, main domain is available.
0	avail_spc	When set, SPC is available.

1.3.99 PM_AVAIL_SR5

Power Mode Available Subsystem Status Register 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_SR5: 0x43D5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R:1
HW Access	NA							W
Retention	NA							RET
Name	RSVD							avail_dsm_ channel

This register indicates whether a subsystem is available or not.

Bits	Name	Description
0	avail_dsm_channel	Each set bit indicates an available delsig channel.

1.3.100 PM_AVAIL_SR6

Power Mode Available Subsystem Status Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PM_AVAIL_SR6: 0x43D6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R:1	NA:00		R:1	R:1
HW Access	NA			W	NA		W	W
Retention	NA			RET	NA		RET	RET
Name	RSVD			avail_anamisc2	RSVD		avail_anapump	avail_anamisc

This register indicates whether a subsystem is available or not.

Bits	Name	Description
4	avail_anamisc2	When set, miscellaneous analog (group 2) is available.
1	avail_anapump	When set, analog pump is available.
0	avail_anamisc	When set, miscellaneous analog is available.

1.3.101 INTC_VECT[0..31]

Interrupt Address Vector registers

Reset: N/A

Register : Address

INTC_VECT: 0x4400-0x443F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	IAV_LSB							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	IAV_MSB							

These registers contain the user programmed interrupt address vectors (iav[15:0]) for corresponding interrupts. S8DPARAM_RAM8x16 is used for storing the interrupt address vectors. The registers access is such that the write/read happens to/from the LSB first and then the MSB. The addresses shown below are corresponds to LSB addresses. For corresponding MSB, add 1 to corresponding LSB address. Note: On reset, these registers contain X's and need to initialize prior to use them in IC. PHUB can written/read to/from either 8-bits or 16-bits of these registers.

Bits	Name	Description
15:8	IAV_MSB[7:0]	These bits contain the Higher byte of user programmed interrupt address vector (iav[15:8])
7:0	IAV_LSB[7:0]	These bits contain the Lower byte of user programmed interrupt address vector (iav[7:0])

1.3.102 INTC_PRIOR[0..31]

Interrrupt Controller Priority Registers

Reset: System reset for retention flops [reset_all_retention]

Register : Address

INTC_PRIOR0: 0x4480	INTC_PRIOR1: 0x4481
INTC_PRIOR2: 0x4482	INTC_PRIOR3: 0x4483
INTC_PRIOR4: 0x4484	INTC_PRIOR5: 0x4485
INTC_PRIOR6: 0x4486	INTC_PRIOR7: 0x4487
INTC_PRIOR8: 0x4488	INTC_PRIOR9: 0x4489
INTC_PRIOR10: 0x448A	INTC_PRIOR11: 0x448B
INTC_PRIOR12: 0x448C	INTC_PRIOR13: 0x448D
INTC_PRIOR14: 0x448E	INTC_PRIOR15: 0x448F
INTC_PRIOR16: 0x4490	INTC_PRIOR17: 0x4491
INTC_PRIOR18: 0x4492	INTC_PRIOR19: 0x4493
INTC_PRIOR20: 0x4494	INTC_PRIOR21: 0x4495
INTC_PRIOR22: 0x4496	INTC_PRIOR23: 0x4497
INTC_PRIOR24: 0x4498	INTC_PRIOR25: 0x4499
INTC_PRIOR26: 0x449A	INTC_PRIOR27: 0x449B
INTC_PRIOR28: 0x449C	INTC_PRIOR29: 0x449D
INTC_PRIOR30: 0x449E	INTC_PRIOR31: 0x449F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:000			NA:00000				
HW Access	R/W			NA				
Retention	RET			NA				
Name	PRIOR			RSVD				

These registers assign a priority value from 0 to 7 to each of the available interrupts. The highest priority is 0 and the lowest priority is 7. The priority registers are stored with the most significant bit (MSB) first. This means that for the three bit priority scheme used in the current design, the priority value will be stored in bits [7:5], the remaining bits will always be zero's. If it is a 3 bit priority scheme, then the most significant 3 bits are used. While Reading from these registers, the most 3 bits (7:5) are valid bits. Note: While writing/reading into/from Priority registers through PHUB interface, the priority value will be expected/ available on phub_spkn_hwdat [7:5] for Byte access and phub_spkn_hwdat [15:13], phub_spkn_hwdat [7:5] for word access (16 bits).

Bits	Name	Description
7:5	PRIOR[2:0]	The priority value of corresponding interrupt input can be programmed into this register.

1.3.103 INTC_SET_EN[0..3]

Interrrupt Controller Set Enable Registers

Reset: System reset for retention flops [reset_all_retention]

Register : Address

INTC_SET_EN0: 0x44C0 INTC_SET_EN1: 0x44C1

INTC_SET_EN2: 0x44C2 INTC_SET_EN3: 0x44C3

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	SET_EN							

These registers enable and mask interrupts, and determine which interrupts are currently enabled. Each bit in the register corresponds to one of 8 among 32 interrupts. Setting a bit in the Interrupt Set-Enable Register enables the corresponding interrupt. When the enable bit of a pending interrupt is set, the interrupt controller activates the interrupt based on its priority. When the enable bit is clear, asserting its interrupt signal pends the interrupt, but it is not possible to activate the interrupt, regardless of its priority. Note: There exists only one physical flop for both INTC_SET_EN[0] and INTC_CLR_EN[0] registers. so effectively, N flops are required for both INTC_SET_EN and INTC_CL_EN registers instead of 2N where N is the No. of interrupts/8

Bits	Name	Description
7:0	SET_EN[7:0]	Interrupt set-enable bits For write operations: '1' - enable interrupt '0' - no effect For read operations: '1' - indicates that the interrupt is enabled '0' - indicates that the interrupt is disabled Writing '0' to a bit has no effect. Reading the bit, returns its current state.

1.3.104 INTC_CLR_EN[0..3]

Interrrupt Controller Clear Enable Registers

Reset: System reset for retention flops [reset_all_retention]

Register : Address

INTC_CLR_EN0: 0x44C8 INTC_CLR_EN1: 0x44C9

INTC_CLR_EN2: 0x44CA INTC_CLR_EN3: 0x44CB

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	CLR_EN							

These registers disable the interrupts and determines which interrupts are currently disabled ('0' indicates that the interrupt is disabled). Each bit in the register corresponds to one of 8 among 32 interrupts. Setting an Interrupt Clear-Enable Register bit disables the corresponding interrupt. .

Bits	Name	Description
7:0	CLR_EN[7:0]	Interrupt clear-enable bits For write operations: '1' - Disable the interrupt '0' - Nothing to do on corresponding interrupt For read operations: '1' - indicates the enabled interrupts '0' - indicates the disabled interrupts Writing '0' to a bit has no effect. Reading the bit, returns its current state.

1.3.105 INTC_SET_PD[0..3]

Interrrupt Controller Set Pend Registers

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

INTC_SET_PD0: 0x44D0

INTC_SET_PD1: 0x44D1

INTC_SET_PD2: 0x44D2

INTC_SET_PD3: 0x44D3

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	SET_PD							

These registers force the interrupts into the pending state and determines which interrupts are currently pending. Each bit in the register corresponds to one of 8 among 32 interrupts. Setting an interrupt set-pending register bit pends the corresponding interrupt, that is, it puts the corresponding interrupt in the pending state. Note: writing '0' to the interrupt set-pending register has no affect on an interrupt that is already pending or that is disabled.

Bits	Name	Description
7:0	SET_PD[7:0]	Interrupt set-pending bits For write operations: '1' - pend the corresponding interrupt '0' - not pend the corresponding interrupt For read operations: '1' - indicates that currently pended interrupts '0' - corresponding interrupt is not in pending state Writing '0' to a bit has no effect. Reading the bit returns its current state.

1.3.106 INTC_CLR_PD[0..3]

Interrrupt Controller Clear Pend Registers

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

INTC_CLR_PD0: 0x44D8 INTC_CLR_PD1: 0x44D9

INTC_CLR_PD2: 0x44DA INTC_CLR_PD3: 0x44DB

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	CLR_PD							

These registers clear the pending interrupts and determines which interrupts are currently pending. Each bit in the register corresponds to one of 8 among 32 interrupts. Setting an Interrupt clear pending register bit puts the corresponding pending interrupt in the inactive state. Note: There exists only one physical flop for both INTC_SET_PD[0] and INTC_CLR_PD[0] registers. so effectively, N flops are required for both INTC_SET_PD and INTC_CLR_PD registers instead of 2N where N is the No. of interrupts/8

Bits	Name	Description
7:0	CLR_PD[7:0]	Interrupt clear-pending bits For write operations: '1' - To clear pending interrupt '0' - Nothing to do on interrupt For read operations: '1' - indicates that currently pended interrupts '0' - corresponding interrupt is not in pend state Writing '0' to a bit has no effect. Reading the bit returns its current state.

1.3.107 INTC_NUM_LINES

Interrrupt Controller Number Of Lines Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

INTC_NUM_LINES: 0x44F0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R:011		
HW Access	NA					R		
Retention	NA					NONRET		
Name	RSVD					INT_LINES		

This register reports the number of interrupt lines that the interrupt controller supports.

Bits	Name	Description
2:0	INT_LINES[2:0]	Total number of interrupt lines with the least equal to 8. 3'b000 = up to 8 interrupts 3'b001 = up to 16 interrupts 3'b010 = up to 24 interrupts 3'b011 = up to 32 interrupts 3'b100 = up to 40 interrupts 3'b101 = up to 48 interrupts 3'b110 = up to 56 interrupts 3'b111 = up to 64 interrupts

1.3.108 INTC_ACT_INT_NUM

Interrrupt Controller Active Interrupt Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

INTC_ACT_INT_NUM: 0x44F1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R:00000				
HW Access	NA			R/W				
Retention	NA			NONRET				
Name	RSVD			ACT_INT_NUM				

This register provides information on the recently posted interrupt, that is corresponding to the interrupt for which the IRQ was sent to the 8051. The value on this register is valid for corresponding posted interrupt only between duration of irq and corresponding ira. Otherwise the value on this register is not corresponding to the posted interrupt.

Bits	Name	Description
4:0	ACT_INT_NUM[4:0]	Interrupt Number of the recently posted interrupt.

1.3.109 INTC_ACT_VECT

Interrrupt Controller Active Vector Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

INTC_ACT_VECT: 0x44F2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	NONRET							
Name	ACT_VECT_LSB							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	NONRET							
Name	ACT_VECT_MSB							

This register provides information on the interrupt address vector (iav) of the recently posted interrupt, i.e. the active interrupt. This register is read only. The value on this register is valid for corresponding posted interrupt only between irq and corresponding ira.

Bits	Name	Description
15:8	ACT_VECT_MSB[7:0]	The Higher byte of interrupt address vector (iav[15:8]) of the active interrupt is stored in this 8-bit register
7:0	ACT_VECT_LSB[7:0]	The Lower byte of interrupt address vector (iav[7:0]) of the active interrupt is stored in this 8-bit register

1.3.110 INTC_CSR_EN

Interrrupt Controller Configuration and Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

INTC_CSR_EN: 0x44F4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:0	R/W:0
HW Access	NA						R/W	R
Retention	NA						RET	RET
Name	RSVD						DISABLE_IRQ	CLOCK_EN

The register bit '0'(CLOCK_EN) is used to enable the clock signal for internal core logic. This regiter bit is used along with external input 'intc_clk_en' which is driven from Power Manager to generate the clock signal for internal core logic. This register should not be accessed through DMA. The register bit '1'(DIS_IRQ) is used to disable IRQ generation to CPU when written with 1'b1. This write is mandatory before disabling the IE bit in 8051.

Bits	Name	Description
1	DISABLE_IRQ	1'b0: Enables the IRQ generation to CPU 1'b1: Disables the IRQ generation to CPU.
0	CLOCK_EN	1'b0: Disables the clock signal for internal core logic 1'b1: Enables the clock signal for internal core logic.

1.3.111 PICU[0..15]_INTTYPE[0..7]

Port Interrupt Control Type Register

Reset: System reset for always on flops [reset_all_alwayson]

Register : Address

PICU0_INTTYPE0: 0x4500
PICU0_INTTYPE1: 0x4501
PICU0_INTTYPE2: 0x4502
PICU0_INTTYPE3: 0x4503
PICU0_INTTYPE4: 0x4504
PICU0_INTTYPE5: 0x4505
PICU0_INTTYPE6: 0x4506
PICU0_INTTYPE7: 0x4507
PICU1_INTTYPE0: 0x4508
PICU1_INTTYPE1: 0x4509
PICU1_INTTYPE2: 0x450A
PICU1_INTTYPE3: 0x450B
PICU1_INTTYPE4: 0x450C
PICU1_INTTYPE5: 0x450D
PICU1_INTTYPE6: 0x450E
PICU1_INTTYPE7: 0x450F
PICU2_INTTYPE0: 0x4510
PICU2_INTTYPE1: 0x4511
PICU2_INTTYPE2: 0x4512
PICU2_INTTYPE3: 0x4513
PICU2_INTTYPE4: 0x4514
PICU2_INTTYPE5: 0x4515
PICU2_INTTYPE6: 0x4516
PICU2_INTTYPE7: 0x4517
PICU3_INTTYPE0: 0x4518
PICU3_INTTYPE1: 0x4519
PICU3_INTTYPE2: 0x451A
PICU3_INTTYPE3: 0x451B
PICU3_INTTYPE4: 0x451C
PICU3_INTTYPE5: 0x451D
PICU3_INTTYPE6: 0x451E
PICU3_INTTYPE7: 0x451F
PICU4_INTTYPE0: 0x4520
PICU4_INTTYPE1: 0x4521
PICU4_INTTYPE2: 0x4522
PICU4_INTTYPE3: 0x4523
PICU4_INTTYPE4: 0x4524
PICU4_INTTYPE5: 0x4525
PICU4_INTTYPE6: 0x4526
PICU4_INTTYPE7: 0x4527
PICU5_INTTYPE0: 0x4528
PICU5_INTTYPE1: 0x4529
PICU5_INTTYPE2: 0x452A
PICU5_INTTYPE3: 0x452B
PICU5_INTTYPE4: 0x452C
PICU5_INTTYPE5: 0x452D
PICU5_INTTYPE6: 0x452E
PICU5_INTTYPE7: 0x452F
PICU6_INTTYPE0: 0x4530
PICU6_INTTYPE1: 0x4531
PICU6_INTTYPE2: 0x4532
PICU6_INTTYPE3: 0x4533
PICU6_INTTYPE4: 0x4534
PICU6_INTTYPE5: 0x4535
PICU6_INTTYPE6: 0x4536
PICU6_INTTYPE7: 0x4537
PICU12_INTTYPE0: 0x4560
PICU12_INTTYPE1: 0x4561
PICU12_INTTYPE2: 0x4562
PICU12_INTTYPE3: 0x4563
PICU12_INTTYPE4: 0x4564
PICU12_INTTYPE5: 0x4565
PICU12_INTTYPE6: 0x4566
PICU12_INTTYPE7: 0x4567
PICU15_INTTYPE0: 0x4578
PICU15_INTTYPE1: 0x4579

(continued)

Register : Address

PICU15_INTTYPE2: 0x457A

PICU15_INTTYPE3: 0x457B

PICU15_INTTYPE4: 0x457C

PICU15_INTTYPE5: 0x457D

PICU15_INTTYPE6: 0x457E

PICU15_INTTYPE7: 0x457F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:00	
HW Access	NA						R	
Retention	NA						RET	
Name	RSVD						INTTYPE	

This register configures the type of interrupt for a pin. In the table, reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits should always be written with a value of '0'.

Bits	Name	Description
1:0	INTTYPE[1:0]	This field configures the type of interrupt type enabled. See Table 1-70.

Table 1-70. Bit field encoding: INTTYPE_ENUM

Value	Name	Description
2'b00	DISABLE	Disable Interrupts for pin.
2'b01	RISING_EDGE	Enable Rising Edge Interrupts for pin.
2'b10	FALLING_EDGE	Enable Falling Edge Interrupts for pin.
2'b11	CHANGE_MODE	Enable Both Edge Interrupts for pin.

1.3.112 PICU[0..15]_INTSTAT

Port Interrupt Control Status Register

Reset: System reset for always on flops [reset_all_alwayson]

Register : Address

PICU0_INTSTAT: 0x4580

PICU1_INTSTAT: 0x4581

PICU2_INTSTAT: 0x4582

PICU3_INTSTAT: 0x4583

PICU4_INTSTAT: 0x4584

PICU5_INTSTAT: 0x4585

PICU6_INTSTAT: 0x4586

PICU12_INTSTAT: 0x458C

PICU15_INTSTAT: 0x458F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	RC:0	RC:0	RC:0	RC:0	RC:0	RC:0	RC:0	RC:0
HW Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	STAT7	STAT6	STAT5	STAT4	STAT3	STAT2	STAT1	STAT0

This register provides information on the recently posted interrupts.

Bits	Name	Description
7	Interrupt Status {STAT7}	Pin 7 Interrupt Status See Table 1-71.
6	Interrupt Status {STAT6}	Pin 6 Interrupt Status See Table 1-71.
5	Interrupt Status {STAT5}	Pin 5 Interrupt Status See Table 1-71.
4	Interrupt Status {STAT4}	Pin 4 Interrupt Status See Table 1-71.
3	Interrupt Status {STAT3}	Pin 3 Interrupt Status See Table 1-71.
2	Interrupt Status {STAT2}	Pin 2 Interrupt Status See Table 1-71.
1	Interrupt Status {STAT1}	Pin 1 Interrupt Status See Table 1-71.
0	Interrupt Status {STAT0}	Pin 0 Interrupt Status See Table 1-71.

Table 1-71. Bit field encoding: INTSTAT_ENUM

Value	Name	Description
1'b1	INT_PENDING	Indicates an interrupt is pending.
1'b0	NO_INT	Indicates no interrupt is pending.

1.3.113 PICU[0..15]_SNAP

Port Interrupt Control Snap Shot Register

Reset: System reset for always on flops [reset_all_alwayson]

Register : Address

PICU0_SNAP: 0x4590 | PICU1_SNAP: 0x4591 | PICU2_SNAP: 0x4592

PICU3_SNAP: 0x4593 | PICU4_SNAP: 0x4594 | PICU5_SNAP: 0x4595

PICU6_SNAP: 0x4596 | PICU12_SNAP: 0x459C | PICU15_SNAP: 0x459F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	RET							
Name	SNAPSHOT							

This register provides information on the state of input pins at recent read to Status register. An exception is this register will not be updated when status register is read with DISABLE_COR or CORD bit in MLOGIC.DEBUG register set

Bits	Name	Description
7:0	SNAPSHOT[7:0]	Contains input pin values at recent read to status register

1.3.114 PICU[0..15]_DISABLE_COR

Disable Status Register Clear on Read Feature

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

PICU0_DISABLE_COR: 0x45A0

PICU1_DISABLE_COR: 0x45A1

PICU2_DISABLE_COR: 0x45A2

PICU3_DISABLE_COR: 0x45A3

PICU4_DISABLE_COR: 0x45A4

PICU5_DISABLE_COR: 0x45A5

PICU6_DISABLE_COR: 0x45A6

PICU12_DISABLE_COR: 0x45AC

PICU15_DISABLE_COR: 0x45AF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Retention	NA							NONRET
Name	RSVD							DISABLE_COR

This register is provided to disable the clear on read feature of Status Register. Either this register bit or CORD bit in MLOGIC.DEBUG register can disable the clear on read feature of status register. The interrupt will be cleared when both DISABLE_COR is 1'b0, CORD bit in MLOGIC.DEBUG register is 1'b0 and there is a status register read. In the table, reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits should always be written with a value of '0'.

Bits	Name	Description
0	DISABLE_COR	1'b0: Status Register is Clear On Read. 1'b1: Disable the Clear on Read feature of Status Register.

1.3.115 DAC[0..3]_TR

DAC Block Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC0_TR: 0x4608 DAC1_TR: 0x4609 DAC2_TR: 0x460A

DAC3_TR: 0x460B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	tr							

Bits	Name	Description
7:0	tr[7:0]	8 Calibration bits

1.3.116 NPUMP_DSM_TR0

Delta Sigma Modulator (DSM) Negative Pump Trim Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NPUMP_DSM_TR0: 0x4610

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:00	
HW Access	NA						R	
Retention	NA						RET	
Name	RSVD						npump_dsm_trim	

Bits	Name	Description
1:0	npump_dsm_trim[1:0]	Delta Sigma Modulator (DSM) Negative Pump Trim

1.3.117 NPUMP_SC_TR0

Switched Cap Negative Pump Trim Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NPUMP_SC_TR0: 0x4611

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:00	
HW Access	NA						R	
Retention	NA						RET	
Name	RSVD						npump_sc_trim	

Bits	Name	Description
1:0	npump_sc_trim[1:0]	Switched Cap Negative Pump Trim See Table 1-72.

Table 1-72. Bit field encoding: NPUMP_SC_TR0_ENUM

Value	Name	Description
2'b00	one_sc_block	1 SC block
2'b01	two_sc_blocks	2 SC blocks
2'b10	four_sc_blocks	4 SC blocks
2'b11	turbo_mode	Turbo mode for risk mitigation, 4 SC blocks

1.3.118 NPUMP_OPAMP_TR0

Analog Linear Output Buffer (OPAMP) Negative Pump Trim Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

NPUMP_OPAMP_TR0: 0x4612

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:00	
HW Access	NA						R	
Retention	NA						RET	
Name	RSVD						npump_opamp_trim	

Bits	Name	Description
1:0	npump_opamp_trim[1:0]	Analog Linear Output Buffer (OPAMP) Negative Pump Trim

1.3.119 OPAMP[0..3]_TR0

Analog Output Buffer Trim Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

OPAMP0_TR0: 0x4620 OPAMP1_TR0: 0x4622 OPAMP2_TR0: 0x4624

OPAMP3_TR0: 0x4626

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:00000				
HW Access	NA			R				
Retention	NA			RET				
Name	RSVD			offset_trim				

Bits	Name	Description
4:0	offset_trim[4:0]	Offset Trim: 420uV typical step size; +/- 6.8mV offset trimmable range

1.3.120 OPAMP[0..3]_TR1

Analog Output Buffer Trim Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

OPAMP0_TR1: 0x4621 OPAMP1_TR1: 0x4623 OPAMP2_TR1: 0x4625

OPAMP3_TR1: 0x4627

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R							
Retention	NA							
Name	RSVD							

Bits	Name	Description
7:0	RSVD[7:0]	Reserved for OPAMP expansion

1.3.121 CMP[0..3]_TR0

Comparator Trim Register for PMOS Load

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP0_TR0: 0x4630 CMP1_TR0: 0x4632 CMP2_TR0: 0x4634

CMP3_TR0: 0x4636

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0000			
HW Access	NA			R	R			
Retention	NA			RET	RET			
Name	RSVD			trim_pmos_sel	trim_pmos_mag			

Bits	Name	Description
4	trim_pmos_sel	Selects the side of the pmos load to which the trim magnitude is applied See Table 1-74.
3:0	trim_pmos_mag[3:0]	Sets the trim magnitude of the pmos load for offset calibration See Table 1-73.

Table 1-73. Bit field encoding: TRIM_PMAG_ENUM

Value	Name	Description
4'h0	TRIM_PMAG_0	Does not add any offset.
4'h1	TRIM_PMAG_1	Adds offset of ~1mV to side selected by trim_pmos_sel bit
4'h2	TRIM_PMAG_2	Adds offset of ~2mV to side selected by trim_pmos_sel bit
4'h3	TRIM_PMAG_3	Adds offset of ~3mV to side selected by trim_pmos_sel bit
4'h4	TRIM_PMAG_4	Adds offset of ~4mV to side selected by trim_pmos_sel bit
4'h5	TRIM_PMAG_5	Adds offset of ~5mV to side selected by trim_pmos_sel bit
4'h6	TRIM_PMAG_6	Adds offset of ~6mV to side selected by trim_pmos_sel bit
4'h7	TRIM_PMAG_7	Adds offset of ~7mV to side selected by trim_pmos_sel bit
4'h8	TRIM_PMAG_8	Adds offset of ~8mV to side selected by trim_pmos_sel bit
4'h9	TRIM_PMAG_9	Adds offset of ~9mV to side selected by trim_pmos_sel bit
4'ha	TRIM_PMAG_A	Adds offset of ~10mV to side selected by trim_pmos_sel bit
4'hb	TRIM_PMAG_B	Adds offset of ~11mV to side selected by trim_pmos_sel bit
4'hc	TRIM_PMAG_C	Adds offset of ~12mV to side selected by trim_pmos_sel bit
4'hd	TRIM_PMAG_D	Adds offset of ~13mV to side selected by trim_pmos_sel bit
4'he	TRIM_PMAG_E	Adds offset of ~14mV to side selected by trim_pmos_sel bit
4'hf	TRIM_PMAG_F	Adds offset of ~15mV to side selected by trim_pmos_sel bit

Table 1-74. Bit field encoding: TRIM_PSEL_ENUM

Value	Name	Description
1'b0	TRIM_PSEL_0	Trim the positive side of the pmos load
1'b1	TRIM_PSEL_1	Trim the negative side of the pmos load

1.3.122 CMP[0..3]_TR1

Comparator Trim Register for NMOS Load

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP0_TR1: 0x4631 CMP1_TR1: 0x4633 CMP2_TR1: 0x4635

CMP3_TR1: 0x4637

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	NA:0	R/W:000		
HW Access	NA			R	NA	R		
Retention	NA			RET	NA	RET		
Name	RSVD			trim_nmos_sel	RSVD	trim_nmos_mag		

Bits	Name	Description
4	trim_nmos_sel	Selects the side of the nmos load to which the trim magnitude is applied See Table 1-76.
2:0	trim_nmos_mag[2:0]	Sets the trim magnitude of the nmos load for offset calibration See Table 1-75.

Table 1-75. Bit field encoding: TRIM_NMAG_ENUM

Value	Name	Description
3'h0	TRIM_NMAG_0	Does not add any offset.
3'h1	TRIM_NMAG_1	Adds offset of ~1mV to side selected by trim_nmos_sel bit
3'h2	TRIM_NMAG_2	Adds offset of ~2mV to side selected by trim_nmos_sel bit
3'h3	TRIM_NMAG_3	Adds offset of ~3mV to side selected by trim_nmos_sel bit
3'h4	TRIM_NMAG_4	Adds offset of ~4mV to side selected by trim_nmos_sel bit
3'h5	TRIM_NMAG_5	Adds offset of ~5mV to side selected by trim_nmos_sel bit
3'h6	TRIM_NMAG_6	Adds offset of ~6mV to side selected by trim_nmos_sel bit
3'h7	TRIM_NMAG_7	Adds offset of ~7mV to side selected by trim_nmos_sel bit

Table 1-76. Bit field encoding: TRIM_NSEL_ENUM

Value	Name	Description
1'b0	TRIM_NSEL_0	Trim the negative side of the nmos load
1'b1	TRIM_NSEL_1	Trim the positive side of the nmos load

1.3.123 PWRSYS_HIB_TR0

Hibernate Trim Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_HIB_TR0: 0x4680

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:1111				R/W:0000			
HW Access	R				R			
Retention	RET				RET			
Name	trim				biasg			

This register trims the hibernate regulator, which generates the vpwrka supply.

Bits	Name	Description
7:4	trim[3:0]	Hibernate regulator trim.
3:0	biasg[3:0]	Hibernate regulator biasg tweak trim. During powerup hib/slp holdoff specified in PWRSYS_SLP_TR, this trim is internally forced to 4'b0001 until the hib/slp powerup holdoff is finished. This register can be written and will readback normally during the force condition (ie the force condition will not be seen during readback). After the force condition ends, the contents of this register will be applied to the hib/slp regulator.

1.3.124 PWRSYS_HIB_TR1

Hibernate Trim Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_HIB_TR1: 0x4681

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:000			R/W:1011			
HW Access	R	R			R			
Retention	RET	RET			RET			
Name	dis_hibernate	rbb_trim			enleg			

This register trims the hibernate regulator and reverse body bias generator.

Bits	Name	Description
7	dis_hibernate	Setting this bit will disable hibernate mode.
6:4	rbb_trim[2:0]	Reverse body bias generator trim.
3:0	enleg[3:0]	Each set bit enables a current leg of the hibernate regulator for the keepalive supply.

1.3.125 PWRSYS_I2C_TR

I2C Regulator Trim Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_I2C_TR: 0x4682

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:000			NA:00		R/W:11	
HW Access	NA	R			NA		R	
Retention	NA	RET			NA		RET	
Name	RSVD	restrim			RSVD		trim	

This register trims the I2C regulator.

Bits	Name	Description
6:4	restrim[2:0]	I2C regulator series resistor trim.
1:0	trim[1:0]	I2C regulator trim.

1.3.126 PWRSYS_SLP_TR

Sleep Regulator Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_SLP_TR: 0x4683

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:111			R/W:0	R/W:0011			
HW Access	R			R	R			
Retention	RET			RET	RET			
Name	hibslp_holdoff			bypass	trim			

This register trims the sleep regulator.

Bits	Name	Description
7:5	hibslp_holdoff[2:0]	Number of 1kHz ILO clocks before the hibernate/sleep regulator is ready after a chip reset. Before it is ready, the system will ignore power mode requests except active and standby. It also overrides trim settings for the hibernate/sleep regulator. See Table 1-77.
4	bypass	When set, disables the sleep regulator and shorts vccd to vpwrsleep. The bypass is internally shorted until hibslp_holdoff expires.
3:0	trim[3:0]	Sleep regulator trim.

Table 1-77. Bit field encoding: holdoff_enum

Value	Name	Description
3'b000	HOLDOFF0	0 clocks => disables holdoff
3'b001	HOLDOFF1	1 clocks => 0-1ms
3'b010	HOLDOFF2	2 clocks => 1-2ms
3'b011	HOLDOFF3	3 clocks => 2-3ms
3'b100	HOLDOFF4	4 clocks => 3-4ms
3'b101	HOLDOFF5	5 clocks => 4-5ms
3'b110	HOLDOFF6	6 clocks => 5-6ms
3'b111	HOLDOFF7	7 clocks => 6-7ms

1.3.127 PWRSYS_BUZZ_TR

Power Mode Buzz Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_BUZZ_TR: 0x4684

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0011				R/W:0011			
HW Access	R				R			
Retention	RET				RET			
Name	idle_buzz				slp_buzz			

This register trims the settings for system sampling (buzzing).

Bits	Name	Description
7:4	idle_buzz[3:0]	Sets the buzz rate for digital and analog LDOs during idle mode See Table 1-78.
3:0	slp_buzz[3:0]	Sets the buzz rate for digital and analog LDOs during sleep mode See Table 1-78.

Table 1-78. Bit field encoding: psoc3pwrmgr_pwrsys_trim_buzz_enum

Value	Name	Description
4'b0000	BUZZ_2_TICKS	2 CTW ticks ==> 2ms
4'b0001	BUZZ_4_TICKS	4 CTW ticks ==> 4ms
4'b0010	BUZZ_8_TICKS	8 CTW ticks ==> 8ms
4'b0011	BUZZ_16_TICKS	16 CTW ticks ==> 16ms
4'b0100	BUZZ_32_TICKS	32 CTW ticks ==> 32ms
4'b0101	BUZZ_64_TICKS	64 CTW ticks ==> 64ms
4'b0110	BUZZ_128_TICKS	128 CTW ticks ==> 128ms
4'b0111	BUZZ_256_TICKS	256 CTW ticks ==> 256ms
4'b1000	BUZZ_512_TICKS	512 CTW ticks ==> 512ms

1.3.128 PWRSYS_WAKE_TR0

Power Mode Wakeup Trim Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_WAKE_TR0: 0x4685

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:01111111							
HW Access	R							
Retention	RET							
Name	wake_to_interval							

This register configures the settings for waking up the chip from low power modes.

Bits	Name	Description
7:0	wake_to_interval[7:0]	Sets the timeout time to wait until allowing a reset from the PRES-A or PRES-D propagates to the hard reset logic. Prior to this timeout, the power manager prevents PRES output signals from resetting the device. After this timeout, a reset indication from either PRES circuit will cause a system hard reset. The timeout time is (wake_precnt+1)*wake_to_interval IMO cycles running at wake_imofreq. To avoid reset on wake from hibernate, this register must be set to 0xFF prior to hibernate entry. The register may be restored to 0x7F upon wake from hibernate to return to the wakeup default for subsequent sleep wakeups. It is safe to leave the register at 0xFF for all wakeups, but it must be written to 0xFF prior to the first hibernate entry.

1.3.129 PWRSYS_WAKE_TR1

Power Mode Wakeup Trim Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_WAKE_TR1: 0x4686

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:1	NA:0	R/W:000			R/W:000		
HW Access	NA	NA	R			R		
Retention	NA	NA	RET			RET		
Name	RSVD	RSVD	wake_precnt			wake_imofreq		

This register configures the settings for waking up the chip from low power modes.

Bits	Name	Description
5:3	wake_precnt[2:0]	Sets the wakeup precount value for the timeout counter {PWRSYS.WAKE_TR0} and holdoff counter {PWRSYS.WAKE_TR3}. Thus precount value also scales the timing of the wakeup sequencer that enables internal power domains. Wakeup timing is specified at 12MHz. If a different wake_imofreq is used, wake_precnt is used to adjust the wakeup timing back to 12MHz. A larger precount value may also be used to allow for longer PRES timeout intervals (controlled by wake_ho_interval as well). Note that the actual precount value is wake_precnt + 1. To avoid reset on wake from hibernate, wake_precnt must be written to 4 (divide by 5) prior to hibernate entry. To preserve datasheet wakeup time from sleep, wake_precnt must be restored to the default value of 0 (divide by 1) upon wakeup from hibernate. See Table 1-80.
2:0	wake_imofreq[2:0]	Sets the IMO frequency used during chip wakeup from a low power mode. See Table 1-79.

Table 1-79. Bit field encoding: fimo_freq_enum

Value	Name	Description
3'b000	FIMO_12MHZ	12 MHz
3'b001	FIMO_RSVD001	RESERVED
3'b010	FIMO_RSVD010	RESERVED
3'b011	FIMO_RSVD011	RESERVED
3'b100	FIMO_RSVD100	RESERVED
3'b101	FIMO_RSVD101	RESERVED
3'b110	FIMO_RSVD110	RESERVED
3'b111	FIMO_RSVD111	RESERVED

Table 1-80. Bit field encoding: wake_precnt_enum

Value	Name	Description
3'b000	WPC1	Wakeup sequencer and counters run at FIMO frequency divided by 1 (sleep wakeup)
3'b001	WPC2	Wakeup sequencer and counters run at FIMO frequency divided by 2
3'b010	WPC3	Wakeup sequencer and counters run at FIMO frequency divided by 3
3'b011	WPC4	Wakeup sequencer and counters run at FIMO frequency divided by 4
3'b100	WPC5	Wakeup sequencer and counters run at FIMO frequency divided by 5 (hibernate wakeup)
3'b101	WPC6	Wakeup sequencer and counters run at FIMO frequency divided by 6
3'b110	WPC7	Wakeup sequencer and counters run at FIMO frequency divided by 7
3'b111	WPC8	Wakeup sequencer and counters run at FIMO frequency divided by 8

1.3.130 PWRSYS_BREF_TR

Boot Reference Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_BREF_TR: 0x4687

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:1	NA:00		R/W:1	R/W:0	R/W:1	R/W:1	R/W:0
HW Access	R	NA		R	R	R	R	R
Retention	RET	NA		RET	RET	RET	RET	RET
Name	bref_manual	RSVD		bref_force_turbo	bref_testmode_reg	bref_en_reg	bref_outen_reg	bref_refsw_reg

This registers configures the power system boot reference..

Bits	Name	Description
7	bref_manual	This bit must be written low in the manufacturing trim portion of the test program. When set the other fields in this register allow manual bootref control, which is for RMP and char purposes only. When clear, the power manager will automatically switch the bootref output between the bootref voltage itself and the LVBG after resets and wakeups. When clear, at power up and wakeup, the power manager forces the LDO and LPCOMP references to be the boot reference until device wakes up (meaning until CPU starts running on wakeup). bootref is disabled while device wakeup when this bit is set, the device is in externally regulated VCCA and VCCD mode, AND PWRSYS_WAKE_TR2[2] is set. At the above configuration regular LPCOMPs are used to detect power good during Hibernate and Hibernate timers mode. Since reference is disabled, device can't wakeup from hibernate and hibernate timer modes. Make sure PWRSYS_WAKE_TR2[2] is cleared during Hibertnate, Hibernate Timers mode
4	bref_force_turbo	reserved
3	bref_testmode_reg	When bref_manual is set, this puts the bootref in testmode.
2	bref_en_reg	When bref_manual is set, this fields enables the internal boot reference. This field must be set whenever either LDO is on.
1	bref_outen_reg	When bref_manual is set, this fields enables the output stage of the LDO reference selector. This field must be set prior to selecting the BREF source using bref_refsw_reg.
0	bref_refsw_reg	When bref_manual is set, this fields controls the power system reference source. Using the LVBG reference improves PSRR. See Table 1-81.

Table 1-81. Bit field encoding: bref_refsw_enum

Value	Name	Description
1'b0	BREF	BREF (boot reference)
1'b1	LVBG	LVBG (low voltage band gap)

1.3.131 PWRSYS_BG_TR

Bandgap Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_BG_TR: 0x4688

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	NA:0	R/W:00000				
HW Access	NA	R	NA	R				
Retention	NA	RET	NA	RET				
Name	RSVD	trimbuf_fine	RSVD	inl_ctl				

Bandgap Trim

Bits	Name	Description
6	trimbuf_fine	Current Bandgap - nonlinear current control (fine tuning)
4:0	inl_ctl[4:0]	Current Bandgap - nonlinear current control

1.3.132 PWRSYS_WAKE_TR2

Power Mode Wakeup Trim Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_WAKE_TR2: 0x4689

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:1	R/W:1	R/W:1	R/W:1	R/W:1	R/W:1
HW Access	NA		R	R	R	R	R	R
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		use_early_short	use_vccd_backup	use_vcca_backup	use_vccdclk_det	use_bgwkup_fast	en_buzz

This register configures the settings for waking up the chip from low power modes.

Bits	Name	Description
5	use_early_short	Enable early shorting between vccd/vnwell/vpwrao/vpwrka. When set, the shorts will be applied at the wakeup event for sleep and idle modes. If clear or a wakeup from hibernate mode, shorts will be applied at the powergood event. Note that if early shorting is used, it is critical that vccd be at a valid voltage (>1.2V) for proper logic retention. If it is not, then state loss can occur including WDT failure. If using internal regulation, it is recommended to set use_vccd_backup and use_vcca_backup to ensure that the supply is valid. This bit is in a protected register segment to avoid accidental corruption. This bit must be set to achieve the wake time specs when using internal regulation for vccd.
4	use_vccd_backup	Enable replica regulated vccd supply. When using internal regulation for vccd, this bit enables a backup regulator that keeps vccd during sleep and idle modes. When clear, buzzing should be enabled to ensure that vccd remains high enough to meet the wake time requirement. If the buzzing approach is used, it is highly recommended to use the LPCOMP powergood detection scheme (use_vccdclk_det=0), since it is robust if vccd droops. This bit must be set to achieve the wake time specs when using the internal regulation for vccd. If the chip is configured for external vccd supply using {PWRSYS_CR0}.ext_vccd, then this bit is ignored.
3	use_vcca_backup	Enable replica regulated vcca supply. When using internal regulation for vcca, this bit enables a backup regulator that keeps vcca during sleep and idle modes. When clear, buzzing should be enabled to ensure that vcca remains high enough to meet the wake time requirement. If the buzzing approach is used, it is highly recommended to use the LPCOMP powergood detection scheme (use_vccdclk_det=0), since it is robust if vcca droops. This bit must be set to achieve the wake time specs when using the internal regulation for vcca. If the chip is configured for external vcca supply using {PWRSYS_CR0}.ext_vcca, then this bit is ignored.
2	use_vccdclk_det	Enable alternate powergood detector. When set, an alternate powergood detector is used during wakeup from hibernate and sleep. When clear, the LPCOMPs are used. The alternate powergood detector relies on valid vccd and vcca supplies. It is recommended to use it with the replica regulators (use_vccd_backup and use_vcca_backup) or external supplies. The LPCOMP detector is more robust to droops on vcca and vccd. The alternate powergood detector is slower and should not be used. This bit must be cleared to achieve the wake time specs.
1	use_bgwkup_fast	Enable fast BG wakeup. This bit must be set to achieve the wake time specs.
0	en_buzz	Enable buzz wakeups. Buzzing wakes the regulators (if configured) and performs periodic voltage supervision.

1.3.133 PWRSYS_WAKE_TR3

Power Mode Wakeup Trim Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PWRSYS_WAKE_TR3: 0x468A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:01011111							
HW Access	R							
Retention	RET							
Name	wake_ho_interval							

This register configures the settings for waking up the chip from low power modes.

Bits	Name	Description
7:0	wake_ho_interval[7:0]	Sets the holdoff time to wait until sampling PRES-A/D. The holdoff time is (wake_precnt+1)*wake_ho_interval IMO cycles running at wake_imofreq.

1.3.134 ILO_TR0

Internal Low-speed Oscillator Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ILO_TR0: 0x4690

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:1000				R/W:1000			
HW Access	R				R			
Retention	RET				RET			
Name	tr_100k				tr_1k			

This register is used to trim the frequency of the ILO output clocks.

Bits	Name	Description
7:4	tr_100k[3:0]	Trim setting for 100 kHz output See Table 1-82.
3:0	tr_1k[3:0]	Trim setting for 1 kHz output See Table 1-83.

Table 1-82. Bit field encoding: TR_100K_ENUM

Value	Name	Description
4'b0000	TR_100K_MIN	Minimum Frequency
4'b1111	TR_100K_MAX	Maximum Frequency

Table 1-83. Bit field encoding: TR_1K_ENUM

Value	Name	Description
4'b0000	TR_1K_MIN	Minimum Frequency
4'b1111	TR_1K_MAX	Maximum Frequency

1.3.135 ILO_TR1

Internal Low-speed Oscillator Coarse Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ILO_TR1: 0x4691

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	R/W:10	
HW Access	NA					R	R	
Retention	NA					RET	RET	
Name	RSVD					ct_range	ctrim	

This register is used to trim the frequency of the ILO output clocks.

Bits	Name	Description
2	ct_range	Coarse Trim Range select for ILO See Table 1-85.
1:0	ctrim[1:0]	Coarse Trim Setting for ILO See Table 1-84.

Table 1-84. Bit field encoding: CTRIM_ENUM

Value	Name	Description
2'h0	CTRIM_0	Full Resistor (lowest current, lowest frequency)
2'h1	CTRIM_1	3/4 * R
2'h2	CTRIM_2	1/2 * R
2'h3	CTRIM_3	1/4 * R (highest current, highest frequency)

Table 1-85. Bit field encoding: CT_RANGE_ENUM

Value	Name	Description
1'b0	CT_RANGE_0	Normal range
1'b1	CT_RANGE_1	Lower current range

1.3.136 X32_TR

32 kHz Watch Crystal Oscillator Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

X32_TR: 0x4698

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:101		
HW Access	NA					R		
Retention	NA					RET		
Name	RSVD					xgm		

Bits	Name	Description
2:0	xgm[2:0]	Amplifier GM setting, applies to both High and Low power modes See Table 1-86.

Table 1-86. Bit field encoding: XGM_ENUM

Value	Name	Description
3'b000	XGM_MAX	Highest current setting
3'b101	XGM_DEFAULT	Default setting
3'b111	XGM_MIN	Lowest current setting

1.3.137 IMO_TR0

Internal Main Oscillator Trim Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

IMO_TR0: 0x46A0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:111			NA:00000				
HW Access	R/W			NA				
Retention	RET			NA				
Name	imo_lsb			RSVD				

This register contains the frequency trim for the IMO. For each frequency range, a separate factory trim should be loaded into this register. It is recommended that the user not change the value of this register. When changing frequency ranges, the new trim value should be applied at the lowest freqency range. For example, when switching to a high range, first apply the trim value of the higher range, then switch the IMO to that range. If switching to a lower range, change the range first and then apply the new trim value.

Bits	Name	Description
7:5	imo_lsb[2:0]	These are the 3 LSB of the IMO frequency trim. Normally these are not changed by the user, and are only modified by the hardware during USB clock-locking. These bits are locked from user write when USB Oscillator locking is enabled. See Table 1-87.

Table 1-87. Bit field encoding: IMO_LSB_ENUM

Value	Name	Description
3'b000	IMO_LSB_MIN	minimum value
3'b111	IMO_LSB_MAX	maximum value

1.3.138 IMO_TR1

Internal Main Oscillator Trim Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

IMO_TR1: 0x46A1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:10011101							
HW Access	R/W							
Retention	RET							
Name	imo_trim							

IMO Trim for 48 MHz frequency setting

Bits	Name	Description
7:0	imo_trim[7:0]	Frequency trim (8 MSbits) for the IMO. 8 MSbits of the trim. The factory trim only uses these 8 bits; the 3 LSbits (IMO_LSB[2:0]) are normally only used during USB operation. These bits are locked from user write when USB Oscillator locking is enabled. See Table 1-88.

Table 1-88. Bit field encoding: IMO_TRIM_ENUM

Value	Name	Description
8'h00	IMO_TRIM_MIN	Minimum frequency
8'hff	IMO_TRIM_MAX	Maximum frequency

1.3.139 IMO_GAIN

Internal Main Oscillator Gain Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

IMO_GAIN: 0x46A2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:001111					
HW Access	NA		R					
Retention	NA		RET					
Name	RSVD		gain					

This register contains the gain trim for the IMO. This is normally set with a factory trim and not modified by the user.

Bits	Name	Description
5:0	gain[5:0]	Gain trim for the IMO. This controls the kHz/step of the trim setting in the IMO_TR register. See Table 1-89.

Table 1-89. Bit field encoding: GAIN_ENUM

Value	Name	Description
6'h00	GAIN_MAX	Maximum Gain
6'h3F	GAIN_MIN	Minimum Gain

1.3.140 IMO_C36M

Internal Main Oscillator 36 MHz clock control register {INTERNAL}

Reset: System reset for retention flops [reset_all_retention]

Register : Address

IMO_C36M: 0x46A3

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Retention	NA				RET			
Name	RSVD				tr36			

This register controls operation of the 36 Mhz output of the IMO.

Bits	Name	Description
3:0	tr36[3:0]	Frequency trim for the 36 MHz SPC clock. This value should not be changed by the user. See Table 1-90.

Table 1-90. Bit field encoding: TR36_ENUM

Value	Name	Description
4'h0	TR36_MIN	Minimum frequency
4'hf	TR36_MAX	Maximum frequency

1.3.141 IMO_TR2

Internal Main Oscillator Trim Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

IMO_TR2: 0x46A4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:0	R/W:000110					
HW Access	R	NA	R					
Retention	RET	NA	RET					
Name	pll_trim	RSVD	fimo_trim					

This register contains the frequency trim for the IMO during fastwake mode.

Bits	Name	Description
7	pll_trim	PLL trim for VCO duty cycle. Must be set to 1'b0 in production test and firmware.
5:0	fimo_trim[5:0]	Frequency trim for the IMO in fastwake mode (FIMO). This value should not be changed by the user. Reset default value for bits 5:4 will be overwritten by NVLatch bits during boot See Table 1-91.

Table 1-91. Bit field encoding: FIMO_TRIM_ENUM

Value	Name	Description
6'h00	FIMO_TRIM_MIN	Minimum frequency
6'h3f	FIMO_TRIM_MAX	Maximum frequency

1.3.142 XMHZ_TR

External 4-25 MHz Crystal Oscillator Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

XMHZ_TR: 0x46A8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Retention	NA				RET			
Name	RSVD				iref			

Bits	Name	Description
3:0	iref[3:0]	This bit adjusts the output current of the oscillator circuit. The value is selected to match the output external crystal characteristics. See Table 1-92.

Table 1-92. Bit field encoding: IREF_ENUM

Value	Name	Description
4'h0	IREF_0	13 unit resistors
4'h1	IREF_1	14 unit resistors
4'h2	IREF_2	15 unit resistors
4'h3	IREF_3	16 unit resistors
4'h4	IREF_4	17 unit resistors
4'h5	IREF_5	18 unit resistors
4'h6	IREF_6	19 unit resistors
4'h7	IREF_7	20 unit resistors
4'h8	IREF_8	21 unit resistors
4'h9	IREF_9	22 unit resistors
4'ha	IREF_A	23 unit resistors
4'hb	IREF_B	24 unit resistors
4'hc	IREF_C	25 unit resistors
4'hd	IREF_D	26 unit resistors
4'he	IREF_E	27 unit resistors
4'hf	IREF_F	28 unit resistors

1.3.143 DLY

Delay block Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DLY: 0x46C0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:00		R/W:00000				
HW Access	NA	R		R				
Retention	NA	RET		RET				
Name	RSVD	CTRIM		FTRIM				

This register is used to trim the delay cell tap duration. This register should only be used when the delay cell is in trim mode (see CLKDIST_DLY1 MODE bit). This register can also be accessed via it's alias, the CLKDIST_DLY0 register **User Defined Properties:** unique_name_space=1

Bits	Name	Description
6:5	CTRIM[1:0]	Course trim bits for delay block See Table 1-93.
4:0	FTRIM[4:0]	Fine trim bits for delay block 5'b00000 Lowest bias ... ... 5'bfffff Highest bias

Table 1-93. Bit field encoding: CTRIM_ENUM

Value	Name	Description
2'b00	ZERO	Highest bias setting
2'b10	TWO	Second highest bias setting
2'b01	ONE	Third highest bias setting
2'b11	THREE	Fourth highest bias setting

1.3.144 MLOGIC_DMPSTR

Dumpster Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

MLOGIC_DMPSTR: 0x46E2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R							
Retention	RET							
Name	dumpster							

Bits	Name	Description
7:0	dumpster[7:0]	Dummy register used to pad the manufacturing configuration table. If the MFGCFG table has less than 63 data/address pairs, the remaining pairs write to this register to ensure nothing configured incorrectly

1.3.145 MLOGIC_SEG_CR

Segment Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

MLOGIC_SEG_CR: 0x46E4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:10110100							
HW Access	R							
Retention	RET							
Name	segment_control							

Bits	Name	Description
7:0	segment_control[7:0]	Segment Control, controls write access to the segment register. When 0xB5 is written the lock on the Segment Configuration is removed. When 0xB4 is written, the Segment Configuration bits are locked and may only be read. Writing any other value triggers a reset.

1.3.146 MLOGIC_SEG_CFG0

Segment Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

MLOGIC_SEG_CFG0: 0x46E5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/WOSET:0	R/W:0	R/WOSET:0	R/W:0	R/WOSET:0	R/W:0	R/WOSET:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	lock_protect_3	lock_3	lock_protect_2	lock_2	lock_protect_1	lock_1	lock_protect_0	lock_0

Bits	Name	Description
7	lock_protect_3	Segment Lock Protect
6	lock_3	Segment Lock
5	lock_protect_2	Segment Lock Protect
4	lock_2	Segment Lock
3	lock_protect_1	Segment Lock Protect
2	lock_1	Segment Lock
1	lock_protect_0	Segment Lock Protect
0	lock_0	Segment Lock

1.3.147 MLOGIC_DEBUG

MLOGIC Debug Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

MLOGIC_DEBUG: 0x46E8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	NA:00	
HW Access	NA			R	R	R	NA	
Retention	NA			RET	RET	RET	NA	
Name	RSVD			CORD	swv_clk_sel	swv_clk_en	RSVD	

Bits	Name	Description
4	CORD	0x0: Reading RC registers clears the values in them. 0x1: Clear on Read Disabled. Values in RC registers are not cleared when read.
3	swv_clk_sel	Serial Wire Viewer (SWV) trace clock select. When set to '0' SWD clock is used for trace clock. When set to '1' clk_cpu/2 is used for trace clock
2	swv_clk_en	Serial Wire View (SWV) clock enable. When set to '1' the clocks for SWV are enabled. This bit must be set to '1' to use SWV

1.3.148 MLOGIC_CPU_SCR_CPU_SCR

System Status and Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

MLOGIC_CPU_SCR_CPU_SCR: 0x46EA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R:0	R:1	R:0	R/W:0
HW Access	NA				R/W	R/W	R/W	R
Retention	NA				RET	RET	RET	RET
Name	RSVD				wol	boot	tmode	stop

Bits	Name	Description
3	wol	Write Once Latch Status
2	boot	Boot. Cleared by the Checksum block upon completion of the boot process. Can also be cleared in Test Mode setting the boot bit in the Test Controller CR1 register to bypass the boot process.
1	tmode	Test Mode Status
0	stop	Halt the CPU. Halts the CPU in any mode when written to. Requires a reset, DMA or DOC write to start the CPU again.

1.3.149 RESET_IPOR_CR0

Imprecise Power On Reset Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

RESET_IPOR_CR0: 0x46F0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	W:00000000							
HW Access	R							
Retention	RET							
Name	code							

The IPOR has a 32-bit internal register that disables the IPOR circuits when a certain code is written. This register is split into four 8-bit sections. None of these bits are set on power-up (they are allowed to power-up in a random state). Once the IPOR is disabled in all four registers, any invalid key write to any of the registers causes a hardware reset.

Bits	Name	Description
7:0	code[7:0]	Write 0xD4 to disable this portion of the code. Once the entire code is disabled, any invalid key write will cause a hardware reset.

1.3.150 RESET_IPOR_CR1

Imprecise Power On Reset Control Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

RESET_IPOR_CR1: 0x46F1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	W:00000000							
HW Access	R							
Retention	RET							
Name	code							

The IPOR has a 32-bit internal register that disables the IPOR circuits when a certain code is written. This register is split into four 8-bit sections. None of these bits are set on power-up (they are allowed to power-up in a random state). Once the IPOR is disabled in all four registers, any invalid key write to any of the registers causes a hardware reset.

Bits	Name	Description
7:0	code[7:0]	Write 0xAA to disable this portion of the code. Once the entire code is disabled, any invalid key write will cause a hardware reset.

1.3.151 RESET_IPOR_CR2

Imprecise Power On Reset Control Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

RESET_IPOR_CR2: 0x46F2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	W:00000000							
HW Access	R							
Retention	RET							
Name	code							

The IPOR has a 32-bit internal register that disables the IPOR circuits when a certain code is written. This register is split into four 8-bit sections. None of these bits are set on power-up (they are allowed to power-up in a random state). Once the IPOR is disabled in all four registers, any invalid key write to any of the registers causes a hardware reset.

Bits	Name	Description
7:0	code[7:0]	Write 0x56 to disable this portion of the code. Once the entire code is disabled, any invalid key write will cause a hardware reset.

1.3.152 RESET_IPOR_CR3

Imprecise Power On Reset Control Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

RESET_IPOR_CR3: 0x46F3

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	W:00000000							
HW Access	R							
Retention	RET							
Name	code							

The IPOR has a 32-bit internal register that disables the IPOR circuits when a certain code is written. This register is split into four 8-bit sections. None of these bits are set on power-up (they are allowed to power-up in a random state). Once the IPOR is disabled in all four registers, any invalid key write to any of the registers causes a hardware reset.

Bits	Name	Description
7:0	code[7:0]	Write 0xC9 to disable this portion of the code. Once the entire code is disabled, any invalid key write will cause a hardware reset.

1.3.153 RESET_CR0

LVI Set Point Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

RESET_CR0: 0x46F4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0000				R/W:0000			
HW Access	R				R			
Retention	RET				RET			
Name	lvia				lvid			

Bits	Name	Description
7:4	lvia[3:0]	When LVI-A is enabled, these 4 bits select the trip point of the detector. See Table 1-94.
3:0	lvid[3:0]	When LVI-D is enabled, these 4 bits select the trip point of the detector. See Table 1-95.

Table 1-94. Bit field encoding: lvia_sel

Value	Name	Description
4'b0000	LVIA_0	1.73V
4'b0001	LVIA_1	1.95v
4'b0010	LVIA_2	2.20V
4'b0011	LVIA_3	2.45V
4'b0100	LVIA_4	2.71V
4'b0101	LVIA_5	2.95V
4'b0110	LVIA_6	3.21V
4'b0111	LVIA_7	3.46V
4'b1000	LVIA_8	3.70V
4'b1001	LVIA_9	3.95V
4'b1010	LVIA_A	4.20V
4'b1011	LVIA_B	4.45V
4'b1100	LVIA_C	4.70V
4'b1101	LVIA_D	4.98V
4'b1110	LVIA_E	5.21V
4'b1111	LVIA_F	5.47V

Table 1-95. Bit field encoding: lvid_sel

Value	Name	Description
4'b0000	LVID_0	1.73V
4'b0001	LVID_1	1.95v
4'b0010	LVID_2	2.20V
4'b0011	LVID_3	2.45V
4'b0100	LVID_4	2.71V
4'b0101	LVID_5	2.95V
4'b0110	LVID_6	3.21V
4'b0111	LVID_7	3.46V
4'b1000	LVID_8	3.70V

(continued)

Table 1-95. Bit field encoding: lvid_sel

4'b1001	LVID_9	3.95V
4'b1010	LVID_A	4.20V
4'b1011	LVID_B	4.45V
4'b1100	LVID_C	4.70V
4'b1101	LVID_D	4.98V
4'b1110	LVID_E	5.21V
4'b1111	LVID_F	5.47V

1.3.154 RESET_CR1

Reset System Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

RESET_CR1: 0x46F5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Retention	NA				RET	RET	RET	RET
Name	RSVD				vmon_hvi_sel	en_hvia	en_lvia	en_lvid

This register enables circuits in the reset subsystem.

Bits	Name	Description
3	vmon_hvi_sel	When set to 1, this bit enables the vmon to look at the VDDD. When this bit is cleared to 0, the vmon looks at the VDDA.
2	en_hvia	When set to 1, enables the high-voltage-interrupt feature on the external analog supply. When this bit is set, there is a possible glitch on the output. To account for this glitch the user must mask the interrupt prior to setting this bit, then clear the status register immediately after this bit is set. Only then this circuit is ready for use.
1	en_lvia	Enables the low-voltage-interrupt or reset feature on the external analog supply. When this bit is set to 1 along with the en_presa bit (RESET_CR3 bit 7) set to 1, the lvia becomes an additional reset source through the presa reset path. When this bit is set to 1 along with the en_presa bit (RESET_CR3 bit 7) cleared to 0, the lvia becomes an interrupt source. When this bit is cleared to 0, the bit state (either a zero or a one) of the en_presa bit (RESET_CR3 bit 7) has no impact on the reset or interrupt functionality. When this bit is set, there is a possible glitch on the output. To account for this glitch the user must mask the interrupt prior to setting this bit, then clear the status register immediately after this bit is set. Only then this circuit is ready for use.
0	en_lvid	Enables the low-voltage-interrupt or reset feature on the external digital supply. When this bit is set to 1 along with the en_presd bit (RESET_CR3 bit 6) set to 1, the lvid becomes an additional reset source through the presd reset path. When this bit is set to 1 along with the en_presd bit (RESET_CR3 bit 6) cleared to 0, the lvid becomes an interrupt source. When this bit is cleared to 0, the bit state (either a zero or a one) of the en_presd bit (RESET_CR3 bit 6) has no impact on the reset or interrupt functionality. When this bit is set, there is a possible glitch on the output. To account for this glitch the user must mask the interrupt prior to setting this bit, then clear the status register immediately after this bit is set. Only then this circuit is ready for use.

1.3.155 RESET_CR2

Software Reset Control Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

RESET_CR2: 0x46F6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Retention	NA							NONRET
Name	RSVD							swr

This register control the software reset (SWR).

Bits	Name	Description
0	swr	Setting this bit will cause a system reset.

1.3.156 RESET_CR3

LVI Mode Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

RESET_CR3: 0x46F7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:1	R/W:1	NA:000			NA:000		
HW Access	R	R	NA			NA		
Retention	RET	RET	NA			NA		
Name	en_presa	en_presd	RSVD			RSVD		

This register controls mode settings for the LVI detector.

Bits	Name	Description
7	en_presa	When this bit is set to 1 along with the en_lvia bit (RESET_CR1 bit 1) set to 1 , the lvia becomes an additional reset source through the presa reset path. When this bit is cleared to 0 along with the en_lvia bit (RESET_CR1 bit 1) set to 1, the lvia is only used as an interrupt source. If the en_lvia bit (RESET_CR1 bit 1) is cleared to 0, the bit state (either a zero or a one) has no impact on the reset or interrupt functionality. This bit is in segment 0.
6	en_presd	When this bit is set to 1 along with the en_lvid bit (RESET_CR1 bit 0) set to 1 , the lvid becomes an additional reset source through the presd reset path. When this bit is cleared to 0 along with the en_lvid bit (RESET_CR1 bit 0) set to 1, the lvid is only used as an interrupt source. If the en_lvid bit (RESET_CR1 bit 0) is cleared to 0, the bit state (either a zero or a one) has no impact on the reset or interrupt functionality. This bit is in segment 0.

Table 1-96. Bit field encoding: tmux_sel

Value	Name	Description
3'b000	TMODE_000	Normal mode (output driven to vgnd)
3'b001	TMODE_001	PRES-D
3'b010	TMODE_010	PRES-A
3'b011	TMODE_011	LVI-D
3'b100	TMODE_100	LVI-A
3'b101	TMODE_101	HVI-A
3'b110	TMODE_110	LPCOMP-D (set => powergood)
3'b111	TMODE_111	LPCOMP-A (set => powergood)

1.3.157 RESET_CR4

Reset Ignore Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

RESET_CR4: 0x46F8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:1	R/W:1	R/W:0	R/W:0
HW Access	NA			R	R	R	R	R
Retention	NA			RET	RET	RET	RET	RET
Name	RSVD			ignore_hbr1	ignore_lpcompa1	ignore_lpcompd1	ignore_presa1	ignore_presd1

This register configures the system to ignore certain reset sources.

Bits	Name	Description
4	ignore_hbr1	When both this bit and ignore_hbr2 are set to 1, the HBR circuit is disabled.
3	ignore_lpcompa1	When both this bit and ignore_lpcompa2 are set to 1, the LPCOMP-A circuits is disabled. Before entering Low Power Modes (LPM), this bit must be high.
2	ignore_lpcompd1	When both this bit and ignore_lpcompd2 are set to 1, the LPCOMP-D circuit is disabled. Before entering Low Power Modes (LPM), this bit must be high.
1	ignore_presa1	When both this bit and ignore_presa2 are set to 1, the PRES-A circuits is disabled.
0	ignore_presd1	When both this bit and ignore_presd2 are set to 1, the PRES-D circuit is disabled.

1.3.158 RESET_CR5

Reset Ignore Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

RESET_CR5: 0x46F9

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:1	R/W:1	R/W:0	R/W:0
HW Access	NA			R	R	R	R	R
Retention	NA			RET	RET	RET	RET	RET
Name	RSVD			ignore_hbr2	ignore_lpcompa2	ignore_lpcompd2	ignore_presa2	ignore_presd2

This register configures the system to ignore certain reset sources.

Bits	Name	Description
4	ignore_hbr2	When both this bit and ignore_hbr1 are set to 1, the HBR circuit is disabled.
3	ignore_lpcompa2	When both this bit and ignore_lpcompa1 are set to 1, the LPCOMP-A circuits is disabled. Before entering Low Power Modes (LPM), this bit must be high.
2	ignore_lpcompd2	When both this bit and ignore_lpcompd1 are set to 1, the LPCOMP-D circuit is disabled. Before entering Low Power Modes (LPM), this bit must be high.
1	ignore_presa2	When both this bit and ignore_presa1 are set to 1, the PRES-A circuits is disabled.
0	ignore_presd2	When both this bit and ignore_presd1 are set to 1, the PRES-D circuit is disabled.

1.3.159 RESET_SR0

Reset and Voltage Detection Status Register 0

Reset: Reset Signals Listed Below

Register : Address

RESET_SR0: 0x46FA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00		RC:0	NA:0	RC:0	RC:0	RC:0	RC:0
HW Access	NA		R/W	NA	R/W	R/W	R/W	R/W
Retention	RET		RET	NA	RET	NONRET	NONRET	NONRET
Name	gpsw_s		swr_s	RSVD	wdr_s	hvia_s	lvia_s	lvid_s

This register gives persistent status for the reset and voltage detection systems.

Bits	Name	Description
7:6	gpsw_s[1:0]	General purpose status for user software. These bits can be set to 1 or cleared to 0 by software and only reset by hard reset sources. They can be used to hold user defined status that persists through many resets.
5	swr_s	Persistent status of the software reset. This bit will be set to 1 when a software reset occurs and will stay set to 1 until cleared to 0 by the user or reset. Sticky (whole field)
3	wdr_s	Persistent status of the watchdog reset. This bit will be set to 1 when a watchdog reset occurs and will stay set to 1 until cleared to 0 by the user or reset. Sticky (whole field)
2	hvia_s	Persistent status of analog HVI. This bit will be set to 1 when the analog supply goes below the trip point for the HVI detector and will stay set to 1 until cleared to 0 by the user or reset. Sticky (whole field)
1	lvia_s	Persistent status of analog LVI. This bit will be set to 1 when the analog supply goes below the trip point for the LVI detector and will stay set to 1 until cleared to 0 by the user or reset. Sticky (whole field)
0	lvid_s	Persistent status of digital LVI. This bit will be set to 1 when the digital supply goes below the trip point for the LVI detector and will stay set to 1 until cleared to 0 by the user or reset. Sticky (whole field)

Reset Table

Reset Signal	Applicable Register Bit(s)
IPOR/PRES/HBR for retention flops [reset_hard_retention]	wdr_s, swr_s, gpsw_s[1:0]
IPOR/PRES/HBR for non-retention flops [reset_hard_nonretention]	lvid_s, lvia_s, hvia_s

1.3.160 RESET_SR1

Reset and Voltage Detection Status Register 1

Reset: IPOR/PRES/HBR for non-retention flops [reset_hard_nonretention]

Register : Address

RESET_SR1: 0x46FB

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	RC:0	RC:0	RC:0	RC:0	NA:00		RC:0
HW Access	NA	R/W	R/W	R/W	R/W	NA		R/W
Retention	NA	NONRET	NONRET	NONRET	NONRET	NA		NONRET
Name	RSVD	lpcompa_s	lpcompd_s	presa_s	presd_s	RSVD		segr_s

This register gives persistent status for the reset and voltage detection systems.

Bits	Name	Description
6	lpcompa_s	Persistent status of analog LPCOMP. This bit will be set to 1 when the analog supply goes below the trip point for the LPCOMP circuit and will stay set to 1 until cleared to 0 by the user or reset. Note that this field is only useful during test mode when the LPCOMP-A circuit does not cause a system reset. Sticky (whole field)
5	lpcompd_s	Persistent status of digital LPCOMP. This bit will be set to 1 when the digital supply goes below the trip point for the LPCOMP circuit and will stay set to 1 until cleared to 0 by the user or reset. Note that this field is only useful during test mode when the LPCOMP-D circuit does not cause a system reset. Sticky (whole field)
4	presa_s	Persistent status of analog PRES. This bit will be set to 1 when the analog supply goes below the trip point for the PRES circuit and will stay set to 1 until cleared to 0 by the user or reset. Note that this field is only useful during test mode when the PRES-A circuit does not cause a system reset. Sticky (whole field)
3	presd_s	Persistent status of digital PRES. This bit will be set to 1 when the digital supply goes below the trip point for the PRES circuit and will stay set to 1 until cleared to 0 by the user or reset. Note that this field is only useful during test mode when the PRES-D circuit does not cause a system reset. Sticky (whole field)
0	segr_s	Persistent status of the segment reset. This bit will be set to 1 when the segment reset occurs circuit and will stay set to 1 until cleared to 0 by the user or reset. Note a segment reset occurs when a value other than 0xB4 or 0xB5 is written to the Segment Control Register. Sticky (whole field)

1.3.161 RESET_SR2

Reset and Voltage Detection Status Register 2

Reset: IPOR/PRES/HBR for non-retention flops [reset_hard_nonretention]

Register : Address

RESET_SR2: 0x46FC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0	R:0	R:0	R:0	R:0	R:0	R:0	R:0
HW Access	W	W	W	W	W	W	W	W
Retention	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET
Name	hbrs_r	lpcompa_r	lpcompd_r	presa_r	presd_r	hvia_r	lvia_r	lvid_r

This register gives real-time status for the reset and voltage detection systems.

Bits	Name	Description
7	hbrs_r	Real-time status of HBR. This is only useful when the HBR does not cause a system level reset.
6	lpcompa_r	Real-time status of analog LPCOMP. This is only useful when the LPCOMP-A output is ignored.
5	lpcompd_r	Real-time status of digital LPCOMP. This is only useful when the LPCOMP-D output is ignored.
4	presa_r	Real-time status of analog PRES. This is only useful when the PRES-A output is ignored.
3	presd_r	Real-time status of digital PRES. This is only useful when the PRES-D output is ignored.
2	hvia_r	Real-time status of analog HVI.
1	lvia_r	Real-time status of analog LVI.
0	lvid_r	Real-time status of digital LVI.

1.3.162 RESET_SR3

Reset and Voltage Detection Status Register 3

Reset: IPOR/PRES/HBR for retention flops [reset_hard_retention]

Register : Address

RESET_SR3: 0x46FD

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:1	NA:000		
HW Access	R/W				W	NA		
Retention	RET				RET	NA		
Name	cksm_fail_cnts				ipor_key_n	RSVD		

This register gives persistent status for the reset and voltage detection systems.

Bits	Name	Description
7:4	cksm_fail_cnts[3:0]	Count of the number of times the Checksum process has failed, causing a reset. These 4 bits will hold the count value and it will stay until cleared to 0 by a reset.
3	ipor_key_n	IPOR key status. When low, the IPOR key has been properly written using the IPOR_CR registers.

1.3.163 RESET_TR

PRES Trim Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

RESET_TR: 0x46FE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0111				R/W:0111			
HW Access	R				R			
Retention	RET				RET			
Name	presa				presd			

This register sets the trim for the precision voltage detectors (PRES).

Bits	Name	Description
7:4	presa[3:0]	Trim for PRES-A. Default value sets the trip to 1.6V
3:0	presd[3:0]	Trim for PRES-D. Default value sets the trip to 1.6V

1.3.164 SPC_FM_EE_CR

FM_EE_CR

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SPC_FM_EE_CR: 0x4700

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R:0	NA:000			R/W:0	R/W:0
HW Access	NA		R/W	NA			R	R
Retention	NA		RET	NA			RET	RET
Name	RSVD		EE_AWAKE	RSVD			EE_Priority	FM_Priority

This register contains control bits for the flash and eeprom arrays

Bits	Name	Description
5	EE_AWAKE	Status signal to denote that the EEPROM array is awake & powered, when set equal to 1. On reset, this value is 0. When the EEPROM is enabled, after the 5 us startup time has elapsed, the bit will be set to a 1.
1	EE_Priority	Sets priority between the PHUB and the SPC for who gets control of the EEPROM array upon simultaneous access requests. 1-> SPC has priority. 0-> PHUB has priority.
0	FM_Priority	Sets priority between the cache controller and the SPC for who gets control of the flash array upon simultaneous access requests. 1-> SPC has priority. 0-> Cache controller has priority.

1.3.165 SPC_FM_EE_WAKE_CNT

FM_EE_WAKE_CNT

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SPC_FM_EE_WAKE_CNT: 0x4701

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00011110							
HW Access	R							
Retention	RET							
Name	Wake_Count							

Flash/EEPROM Wake Count Register

Bits	Name	Description
7:0	Wake_Count[7:0]	The wake count defines the number of Bus Clock cycles it takes for the flash or eeprom to wake up from being in a put into a low power mode independent of the chip power mode (while the rest of the chip remained in active or standby). Wake up time for these blocks is 5 us. The granularity of this register is 2 Bus Clock cycles, so a value of 0x1E (30d) defines the wake up time as 60 cycles of the Bus Clock. This register needs to be written with a value dependent on the Bus Clock frequency so that the duration of the cycles is equal to or greater than the 5 us delay required. The reset value of this register (0x1E) is for a Bus Clock frequency of 12 MHz.

1.3.166 SPC_EE_SCR

EEPROM Status & Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SPC_EE_SCR: 0x4702

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R:0	R/W:0
HW Access	NA						R/W	R
Retention	NA						RET	RET
Name	RSVD						EE_AHB_ACK	AHB_EE_REQ

This register contains status and control bits for the EEPROM array.

Bits	Name	Description
1	EE_AHB_ACK	Once the AHB_EE_REQ bit is set, this bit is set high once the EEPROM is available to be read across the PHUB interface.
0	AHB_EE_REQ	This bit is set high when a read access of the EEPROM, through the PHUB interface, is desired. This is a request bit and is part of a two bit interface with the EE_AHB_ACK bit.

1.3.167 SPC_EE_ERR

EEPROM Error Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SPC_EE_ERR: 0x4703

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							RC:0
HW Access	NA							R/W
Retention	NA							RET
Name	RSVD							EEPROM_error

This register has an error bit for the EEPROM array on the chip. The error bit indicates whether or not the array has had a collision error where two masters (the SPC and the PHUB interface) attempted to access the array simultaneously. The bits are cleared upon a read of this register.

Bits	Name	Description
0	EEPROM_error	Error bit for EEPROM array 0

1.3.168 SPC_CPU_DATA

SPC CPU Data Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

SPC_CPU_DATA: 0x4720

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	CPU_Data							

This register is the command interface to the SPC that allows SPC instructions to be executed by the host CPU writing a sequential series of parameters to this location. This register is meant only for the CPU and not the DMA controller to prevent collisions between the CPU and the DMAC when both attempt to call a function in the SPC

Bits	Name	Description
7:0	CPU_Data[7:0]	CPU Data.

1.3.169 SPC_DMA_DATA

SPC DMA Data Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

SPC_DMA_DATA: 0x4721

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	DMA_Data							

This register is the command interface to the SPC that allows SPC instructions to be executed by the DMA controller writing a sequential series of parameters to this location. This register is meant only for the DMA Controller and not the CPU to prevent collisions between the CPU and the DMAC when both attempt to call a function in the SPC

Bits	Name	Description
7:0	DMA_Data[7:0]	DMA Data.

1.3.170 SPC_SR

SPC Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SPC_SR: 0x4722

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:000000						R:1	R:0
HW Access	R/W						R/W	R/W
Retention	RET						RET	RET
Name	Status_Code						SPC_Idle	Data_Ready

This register returns the current status of the SPC and the exit status of the last complete SPC instruction.

Bits	Name	Description
7:2	Status_Code[5:0]	The Status Code represents the exit status of the last executed SPC instruction. See Table 1-99.
1	SPC_Idle	This bit indicates whether or not the SPC is currently executing an instruction. The bit transitions low as soon as the 1st byte of the 2-byte command key (0xB6) is written into the SPC CPU or DMA Data Register. The bit transitions high as soon as an instruction completes or if the 2nd byte of the command key is invalid. See Table 1-98.
0	Data_Ready	This bit indicates whether or not the SPC has data that is ready to be read from the SPC CPU or DMA Data Register. See Table 1-97.

Table 1-97. Bit field encoding: DATA_RDY_ENUM

Value	Name	Description
1'h0	DATA_IS_NOT_RDY	The SPC isn't ready for the next byte to be written
1'h1	DATA_IS_RDY	The SPC is read for the next byte to be written

Table 1-98. Bit field encoding: INSTR_IDLE_ENUM

Value	Name	Description
1'h0	INSTR_IS_NOT_IDLE	SPC is currently executing an SPC instruction.
1'h1	INSTR_IS_IDLE	SPC is idle and not busy executing an instruction.

Table 1-99. Bit field encoding: SPC_SR_STATUS_CODE_ENUM

Value	Name	Description
6'h0	SPC_SR_OPERATION_SUCCESS	Operation Successful
6'h1	SPC_SR_INVALID_ARRAY_ID	Invalid Array ID for given command
6'h2	SPC_SR_INVALID_2_BYTE_KEY	Invalid 2-byte key
6'h3	SPC_SR_ADDR_ARRY_IS_ASLEEP	Addressed Array is Asleep
6'h4	SPC_SR_EXTERNAL_ACCESS_FAILURE	External Access Failure (SPC is not in external access mode)

(continued)

Table 1-99. Bit field encoding: SPC_SR_STATUS_CODE_ENUM

6'h5	SPC_SR_INVALID_N_VALUE	Invalid N Value for given command
6'h6	SPC_SR_TEST_MODE_FAILURE	Test Mode Failure (SPC is not in test mode)
6'h7	SPC_SR_SMART_WRITE_ALGO_CHKSUM	Smart Write Algorithm Checksum Failure
6'h8	SPC_SR_SMART_WRITE_PARAM_CHKSUM	Smart Write Parameter Checksum Failure
6'h9	SPC_SR_PROTECTION_CHK_FAILURE	Protection Check Failure: protection settings are in a state which prevents the given command from executing
6'hA	SPC_SR_INVALID_ADDR_PARAM	Invalid Address parameter for the given command
6'hB	SPC_SR_INVALID_CMD_CODE	Invalid Command Code
6'hC	SPC_SR_INVALID_ROW_ID	Invalid Row ID parameter for given command
6'hD	SPC_SR_INVALID_INPUT_GET_TEMP_ADC	Invalid input value for Get Temp & Get ADC commands
6'hE	SPC_SR_TMP_SENSOR_VBR_DRIVEN_EXT_DEV	Tempsensor Vbe is currently driven to an external device
6'hF	SPC_SR_INVALID_SPC_STATE	Invalid SPC state (M8G's PC value out of range. Manual SPC Reset required)
6'h10	SPC_SR_START_RANGE_SMART_WRITE	START RANGE: Smart Write return codes (only when using Smart Write algorithm) SWU-016.1 for exact definitions
6'h3F	SPC_SR_END_RANGE_SMART_WRITE	END RANGE: Smart Write return codes (only when using Smart Write algorithm) SWU-016.1 for exact definitions
6'h20	SPC_SR_PEP_PROGRAM_FAILURE	PEP Program Failure (only when using PEP algorithm): Data Verification Failure (row latch checksum != programmed row checksum)

1.3.171 SPC_CR

SPC Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SPC_CR: 0x4723

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R:0	NA:0	NA:0	R/W:0
HW Access	NA				R/W	NA	NA	R/W
Retention	NA				RET	NA	NA	RET
Name	RSVD				SPC_CTRL	RSVD	RSVD	SPC_Manual_Reset

This register contains control bits for the SPC. This register is reset upon assertion of the SPC_Manual_Reset bit.

Bits	Name	Description
3	SPC_CTRL	This is a status bit that defines which SPC data register (SPC.CPU_DATA or SPC.DMA_DATA) was or is currently being used to send a command to the SPC. When one of the two data registers has the first byte of the SPC 2-byte command key written to it, that register now has temporary control of the SPC. Upon this register write, this bit is set accordingly. All subsequent register writes to the other data register are ignored until the command completes.
0	SPC_Manual_Reset	Setting this bit manually resets the SPC. The SPC hardware automatically clears the bit after being held high for 2 cycles of the AHB Bus Clock. See Table 1-101.

Table 1-100. Bit field encoding: SPC_BUSFREQ_ENUM

Value	Name	Description
1'h0	SPC_BUSFREQ_LOW	Tells the SPC that the Bus Clock Frequency is: 50 < Frequency <= 100.
1'h1	SPC_BUSFREQ_HIGH	Tells the SPC that the Bus Clock Frequency is: Frequency <= 50.

Table 1-101. Bit field encoding: SPC_RESET_ENUM

Value	Name	Description
1'h0	SPC_RST_LOW	SPC is in normal execution mode.
1'h1	SPC_RST_HIGH	SPC is in a reset state.

1.3.172 SPC_DMM_MAP_SRAM[0..127]

SPC Direct Memory Mapping

Reset: N/A

Register : Address

SPC_DMM_MAP_SRAM: 0x4780-0x47FF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	spcsramdata							

Maps one of 5 possible 128-byte pages from the 128-Data Store SRAM or 512-byte Code Store SRAM

Bits	Name	Description
7:0	spcsramdata[7:0]	(no description)

1.3.173 CACHE_CR

Cache Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CACHE_CR: 0x4800

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:11		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R		R	R	R/W	R/W	R/W	R
Retention	RET		RET	RET	RET	RET	RET	RET
Name	FLASH_CYCLES		BFILL_EN	CACHE_EN	UNLOCK	CACHE_INV	PHUB_INV	SRAM_EN

CACHE.CR is used to configure the behavior of the cache

Bits	Name	Description
7:6	FLASH_CYCLES[1:0]	Specifies the number of clock cycles the cache will wait before it samples data coming back from Flash. 0x1: 1 cycle. -> 0-22 MHz 0x2: 2 cycles. -> >22-44 MHz 0x3: 3 cycles. -> >44-67 MHz 0x0: 4 cycles. -> RESERVED / Extra Margin (not expected to be used) If EN_CPU=0 then 'cycles' is in terms of bus clock cycles and MHz refers to bus clock frequency. If EN_CPU=1 then 'cycles' is in terms of cpu clock cycles and MHz refers to cpu clock frequency. See PM.ACT/STBY.CFG0.1 for an explanation of EN_CPU. If the cpu clock frequency is not equal to the bus clock frequency, then it's imperative to adjust FLASH_CYCLES when changing EN_CPU.
5	BFILL_EN	0x0: Disables background fill mechanism; allows for some minor power savings 0x1: Enables background fill mechanism to improve CPU performance; requires CACHE_EN=1 and SRAM_EN=1 otherwise this bit is ignored and background fill is disabled
4	CACHE_EN	0x0: Disables HW ability to write data coming from the flash to the cache SRAM. 0x1: Enables HW ability to write data coming from the flash to the cache SRAM.
3	UNLOCK	This is a 'virtual flop' that clears immediately. Reading this bit will always return 0. 0x1: 0x1: Writing 1 will cause all lock bits in the tags and itself to be cleared the following cycle.
2	CACHE_INV	This is a 'virtual flop' that clears immediately. Reading this bit will always return 0. 0x1: Writing 1 will cause all valid bits in the tags, the valid bit for the 8 byte CPU interface and itself to be cleared the following cycle.
1	PHUB_INV	This is a 'virtual flop' that clears immediately. Reading this bit will always return 0. 0x1: Writing 1 will cause the valid bit for the 8 byte PHUB interface read buffer and itself to be cleared the following cycle.
0	SRAM_EN	This bit enables the use of SRAM memory. If bit is 0, SRAM clock is gated. This SRAM clock is also used for the tag registers. Gating this clock will prevent the tag registers from being written.

1.3.174 CACHE_LP_MODE

LP_MODE Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CACHE_LP_MODE: 0x4801

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:11111111							
HW Access	R/W							
Retention	RET							
Name	LP_MODE							

CACHE.LP_MODE is used to configure the FLASH Low Power Mode feature

Bits	Name	Description
7:0	LP_MODE[7:0]	0x0 - 0xfe: Specifies the number of cache hits after which the cache controller will assert SLEEP_REQ. 0xff: Low Power Mode disabled.; this register is on segment 1 and must be unlocked before writing is allowed

1.3.175 CACHE_SR

Cache Status Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

CACHE_SR: 0x4808

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R:0	NA:0
HW Access	NA						R/W	NA
Retention	NA						NONRET	NA
Name	RSVD						FLUSH_DONE	RSVD

CACHE.SR contains the Cache status

Bits	Name	Description
1	FLUSH_DONE	0x0: Flush was not performed since the last assertion of reset, or since CACHE.CR.CACHE_EN got set. 0x1: Flush is done. This bit clears automatically when : 1. a new Flush sequence has started; test_mode signal goes from 0 to 1. 2. CACHE.CR.CACHE_EN bit is set.

1.3.176 CACHE_TAG_SR

Tag Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CACHE_TAG_SR: 0x4810

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	RET							
Name	TAG_VALID							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	RET							
Name	TAG_LOCK							

This is a virtual register that is a collection of the individual valid bits of the corresponding Tag registers.

Bits	Name	Description
15:8	TAG_LOCK[7:0]	Bit vector of lock bits from the Tag registers.
7:0	TAG_VALID[7:0]	Bit vector of valid bits from the Tag registers.

1.3.177 CACHE_TAG[0..7]

Tag Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CACHE_TAG0: 0x4818 CACHE_TAG1: 0x4820 CACHE_TAG2: 0x4828

CACHE_TAG3: 0x4830 CACHE_TAG4: 0x4838 CACHE_TAG5: 0x4840

CACHE_TAG6: 0x4848 CACHE_TAG7: 0x4850

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00		NA:0000				R/W:0	R/W:0
HW Access	R/W		NA				R/W	R/W
Retention	RET		NA				RET	RET
Name	TAG_ADDR		RSVD				TAG_LOCK	TAG_VALID

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	TAG_ADDR							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	VALID_VECTOR							

Contains Cache Line Tag information. The SRAM_EN bit must be set to write these registers in User Mode.

Bits	Name	Description
31:24	VALID_VECTOR[7:0]	Each bit corresponds to a word within the cache line. Each cache line has 8, 64-bit words. 0x0: Corresponding word is invalid. The fill state machine should attempt to fill this word if the tag is valid. 0x1: This word is valid and can be used to satisfy the cpu with a hit.
15:6	TAG_ADDR[9:0]	Tag address bits [15:6] of the requested instruction fetch.
1	TAG_LOCK	0x0: The line is not locked and may be evicted by the replacement algorithm to make room for a new line. 0x1: The line is locked into the cache and cannot be chosen for eviction.

(continued)

0	TAG_VALID	0x0: The line is invalid. All valid bits for the words within the line should be invalid as well. 0x1: The line is valid. The instruction fetch will get a hit if the corresponding word is valid as well.

1.3.178 CACHE_INT_MSK

Cache controller Interrupt Mask

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

CACHE_INT_MSK: 0x4858

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:000000					
HW Access	NA		R					
Retention	NA		NONRET					
Name	RSVD		VECTOR_MASK					

Interrupt Mask Register

Bits	Name	Description
5:0	VECTOR_MASK[5:0]	Bit vector of mask bits applied to corresponding interrupt

1.3.179 CACHE_INT_SR

Cache controller Interrupt Status

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

CACHE_INT_SR: 0x4860

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R:000000					
HW Access	NA		R/W					
Retention	NA		NONRET					
Name	RSVD		VECTOR_VALID					

Interrupt Status Register

Bits	Name	Description
5:0	VECTOR_VALID[5:0]	Bit vector of valid bits from Interrupt_log registers

1.3.180 CACHE_INT_LOG0

Interrupt Log 0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

CACHE_INT_LOG0: 0x4868

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R:000			RC:0
HW Access	NA				R/W			R/W
Retention	NA				NONRET			NONRET
Name	RSVD				INT_LINE			INT_VALID

ISR Loading Violation Interrupt

Bits	Name	Description
3:1	INT_LINE[2:0]	Cache Line number where the ISR loading violation occurred.
0	INT_VALID	0x0: Interrupt log is invalid. 0x1: Interrupt log is valid. Log will be frozen until read

1.3.181 CACHE_INT_LOG1

Interrupt Log 1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

CACHE_INT_LOG1: 0x4870

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R:000			RC:0
HW Access	NA				R/W			R/W
Retention	NA				NONRET			NONRET
Name	RSVD				INT_LINE			INT_VALID

Coherency Violation Interrupt

Bits	Name	Description
3:1	INT_LINE[2:0]	Cache Line number where the Coherency violation occurred.
0	INT_VALID	0x0: Interrupt log is invalid. 0x1: Interrupt log is valid. Log will be frozen until read

1.3.182 CACHE_INT_LOG2

Interrupt Log 2

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

CACHE_INT_LOG2: 0x4878

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00		NA:00000					RC:0
HW Access	R/W		NA					R/W
Retention	NONRET		NA					NONRET
Name	TAG_ADDR		RSVD					INT_VALID

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	NONRET							
Name	TAG_ADDR							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00		R:000			R:000		
HW Access	NA		R/W			R/W		
Retention	NA		NONRET			NONRET		
Name	RSVD		TAG_LINE2			TAG_LINE1		

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Duplicate Tag Violation Interrupt

Bits	Name	Description
21:19	TAG_LINE2[2:0]	Line number of the second tag that matched
18:16	TAG_LINE1[2:0]	Line number of the first tag that matched
15:6	TAG_ADDR[9:0]	Tag address that produced the multiple hits
0	INT_VALID	0x0: Interrupt log is invalid. 0x1: Interrupt log is valid. Log will be frozen until read

1.3.183 CACHE_INT_LOG3

Interrupt Log 3

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

CACHE_INT_LOG3: 0x4880

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000					NA:00		RC:0
HW Access	R/W					NA		R/W
Retention	NONRET					NA		NONRET
Name	FLASH_ADDR					RSVD		INT_VALID

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	NONRET							
Name	FLASH_ADDR							

ECC-Single Bit error detected and corrected

Bits	Name	Description
15:3	FLASH_ADDR[12:0]	Flash address where error was detected and corrected
0	INT_VALID	0x0: Interrupt log is invalid. 0x1: Interrupt log is valid. Log will be frozen until read

1.3.184 CACHE_INT_LOG4

Interrupt Log 4

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

CACHE_INT_LOG4: 0x4888

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000					NA:00		RC:0
HW Access	R/W					NA		R/W
Retention	NONRET					NA		NONRET
Name	FLASH_ADDR					RSVD		INT_VALID

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	NONRET							
Name	FLASH_ADDR							

ECC-Multiple Bit error detected--uncorrectable

Bits	Name	Description
15:3	FLASH_ADDR[12:0]	Flash address where error was detected; error cannot be corrected
0	INT_VALID	0x0: Interrupt log is invalid. 0x1: Interrupt log is valid. Log will be frozen until read

1.3.185 CACHE_INT_LOG5

Interrupt Log 5

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

CACHE_INT_LOG5: 0x4890

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000					NA:00		RC:0
HW Access	R/W					NA		R/W
Retention	NONRET					NA		NONRET
Name	FLASH_ADDR					RSVD		INT_VALID

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	NONRET							
Name	FLASH_ADDR							

Attempted write to Flash error

Bits	Name	Description
15:3	FLASH_ADDR[12:0]	Flash address where write was attempted
0	INT_VALID	0x0: Interrupt log is invalid. 0x1: Interrupt log is valid. Log will be frozen until read

1.3.186 I2C_XCFG

I2C Extended Configuration Register

Reset: Reset Signals Listed Below

Register : Address

I2C_XCFG: 0x49C8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R:0	R/W:0	NA:000			R/W:0
HW Access	R	R	R/W	R/W	NA			R
Retention	NONRET	NONRET	RET	RET	NA			NONRET
Name	csr_clk_en	i2c_on	ready_to_sleep	force_nack	RSVD			hw_addr_en

This register configures enhanced features. In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Always write reserved bits with a value of '0'.

Bits	Name	Description
7	csr_clk_en	This bit is used for gating system clock for the blocks core logic that is not associated with AHB interface. Clock is made available to the core logic only when this bit is set to 1 and the input pin ext_clk_en is also active. If either of them is not active, the blocks core logic does not receive the system clock. See Table 1-102.
6	i2c_on	This bit should be set by the user during initial block configuration if the user wants to use the I2C block as wake-up source. Only when this bit set along with other bits mentioned in the sleep mode section, the I2C wakes up system from sleep on address match.
5	ready_to_sleep	Once the user sets the force_nack bit, the I2C block sets this bit if I2C is not busy or it waits for ongoing transaction to be completed and then sets this bit. As long as this bit is set, the I2C block is going to nack all the transactions.Clearing force_nack bit automatically clears this bit. HW clears this bit automatically on assertion of PD (Power Down)
4	force_nack	This bit must be set by the user before putting the device to sleep and wait for ready_to_sleep status bit to be set. This can be cleared by user by writing '0' and the HW clears it automatically on assertion of PD(Power Down)
0	hw_addr_en	When hw_addr_en = 1, on addr match: interrupt is generated, CSR[3] bit is set, clk is stalled, device will ACK automatically; When hw_addr_en = 1, on addr mismatch: no interrupt is generated, CSR[3] bit is set, clk not stalled, device will NACK automatically; You must configure the compare address in the ADR register; When hw_addr_en = 0, on addr match: interrupt is generated, CSR[3] bit is set, clk is stalled; When hw_addr_en = 0, on addr mismatch: interrupt is generated, CSR[3] bit is set, clk is stalled; and the received address is available in the Data register, to enable the CPU to do a firmware address compare; The functionality of this bit is independent of the data buffering mode See Table 1-103.

Reset Table

Reset Signal	Applicable Register Bit(s)
System reset for retention flops [reset_all_retention]	force_nack, ready_to_sleep
Domain reset for non-retention flops [reset_all_nonretention]	hw_addr_en, i2c_on, csr_clk_en

(continued)

Table 1-102. Bit field encoding: csr_clk_en_enum

Value	Name	Description
1'b1	CSR_CLK_EN	CLK gating for block core logic is enabled
1'b0	CSR_CLK_DIS	CLK gating for blobk core logic is disabled

Table 1-103. Bit field encoding: hw_addr_en_enum

Value	Name	Description
1'b1	HW_ADDR_EN	HW Address comparison is enabled
1'b0	HW_ADDR_DIS	HW Address comparison is disabled

1.3.187 I2C_ADR

I2C Slave Adddress Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

I2C_ADR: 0x49CA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R						
Retention	NA	NONRET						
Name	RSVD	slave_address						

This register holds the slave's 7-bit address. When hardware address compare mode is not enabled in the XCFG register, this register is not in use. In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Always write reserved bits with a value of '0'.

Bits	Name	Description
6:0	slave_address[6:0]	These seven bits hold the slave's own device address. These bits are held zero if I2C_CFG.en_mstr and I2C_CFG.en_slave are both zero.

1.3.188 I2C_CFG

I2C Configuration Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

I2C_CFG: 0x49D6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	NA:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	NA	R	R	R
Retention	NONRET	NONRET	NONRET	NONRET	NA	NONRET	NONRET	NONRET
Name	sio_select	pselect	bus_error_ie	stop_ie	RSVD	clock_rate	en_mstr	en_slave

This register is used to set the basic operating modes, baud rate, and interrupt selection. In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Alweays write reserved bits with a value of '0'.

Bits	Name	Description
7	sio_select	I2C Pin Select for SCL/SDA lines from SIO1/SIO2, 0 = SCL and SDA lines get their inputs from SIO1 module.sclk_str1 and sda_ack1 are driven to SIO1 module and they get asserted once device wakes up from sleep. 1 = SCL and SDA lines get their inputs from SIO2 module. sclk_str2 and sda_ack2 are driven to SIO2 module and they get asserted once device wakes up from sleep. This bit is valid only when I2C.CFG[6] is asserted. See Table 1-109.
6	pselect	I2C Pin Select for SCL/SDA lines from GPIO/SIO, 0 = SCL and SDA lines get their inputs from GPIO module.sclk_str0 and sda_ack0 are driven to GPIO module and they get asserted once device wakes up from sleep. 1 = SCL and SDA lines get their inputs from one of the SIO Blocks that is chosen based on the configuration of bit I2C.CFG[7] See Table 1-108.
5	bus_error_ie	Bus Error Interrupt Enable 0 disabled 1 enabled. An interrupt is generated on the detection of a Bus error condition. See Table 1-104.
4	stop_ie	Stop Interrupt Enable 0 disabled 1 enabled. An interrupt is generated on the detection of a Stop condition. See Table 1-110.
2	clock_rate	0 Samples/bit is 16, 1 Samples/bit is 32 See Table 1-105.
1	en_mstr	0 Disabled 1 enabled See Table 1-106.
0	en_slave	0 Disabled 1 enabled See Table 1-107.

Table 1-104. Bit field encoding: bus_error_ie_enum

Value	Name	Description

(continued)

Table 1-104. Bit field encoding: bus_error_ie_enum

1'b1	BUS_ERROR_IE_EN	Bus Error Interrupt is enabled
1'b0	BUS_ERROR_IE_DIS	Bus Error Interrupt is disabled

Table 1-105. Bit field encoding: clock_rate_enum

Value	Name	Description
1'b0	RATE_1	Samples/bit is 16. For 100K Standard mode OR 400K Fast mode.
1'b1	RATE_2	Samples/bit is 32. For 50K Standard mode.

Table 1-106. Bit field encoding: en_mstr_enum

Value	Name	Description
1'b1	MASTER_EN	Master mode is enabled for the device
1'b0	MASTER_DIS	Master mode is disabled for the device

Table 1-107. Bit field encoding: en_slave_enum

Value	Name	Description
1'b1	SLAVE_EN	Slave mode is enabled for the device
1'b0	SLAVE_DIS	Slave mode is disabled for the device

Table 1-108. Bit field encoding: pselect_enum

Value	Name	Description
1'b1	PSELECT_EN	SCL/SDA lines get their inputs from SIO blocks
1'b0	PSELECT_DIS	SCL/SDA lines get their inputs from GPIO blocks

Table 1-109. Bit field encoding: sio_select_enum

Value	Name	Description
1'b1	SIO_SELECT_EN	SCL/SDA lines get their inputs from SIO2 block
1'b0	SIO_SELECT_DIS	SCL/SDA lines get their inputs from SIO1 block

Table 1-110. Bit field encoding: stop_ie_enum

Value	Name	Description
1'b1	STOP_IE_EN	Stop Interrupt is enabled
1'b0	STOP_IE_DIS	Stop Interrupt is disabled

1.3.189 I2C_CSR

I2C Control and Status Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

I2C_CSR: 0x49D7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/WZC:0	R/W:0	R/WZC:0	R/W:0	R/WZC:0	R/W:0	R/WZC:0	R/WZC:0
HW Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Retention	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET
Name	bus_error	lost_arb	stop_status	ack	address	transmit	lrb	byte_complete

This register is used by the slave to control the flow of data bytes and to keep track of the bus state during a transfer. Bits in this register are held in reset until one of the enable bits in CFG is set. In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits should always be written with a value of '0'.

Bits	Name	Description
7	bus_error	0 Status bit. It must be cleared by firmware by writing a '0' to the bit position. It is never cleared by the hardware. 1 a misplaced Start or Stop condition was detected. This bit is held zero if I2C_CFG.en_mstr and I2C_CFG.en_slave are both zero.
6	lost_arb	0 This bit is set immediately on lost arbitration; however, it does not cause an interrupt. This status may be checked after the following Byte Complete interrupt. Any Start detect or a write to the Start or Restart generate bits (MCSR register), when operating in Master mode, will also clear the bit. 1 lost Arbitration. This bit is held zero if I2C_CFG.en_mstr is zero.
5	stop_status	0 Status bit. It must be cleared by firmware with write of '0' to the bit position. It is never cleared by the hardware. 1 a Stop condition was detected. This bit is held zero if I2C_CFG.en_mstr and I2C_CFG.en_slave are both zero.
4	ack	Acknowledge Out. Bit is automatically cleared by hardware on a Byte Complete event. 0 nack the last received byte. 1 ack the last received byte
3	address	0 Status bit. It must be cleared by firmware with write of '0' to the bit position. 1 the received byte is a slave address. This bit is held zero if I2C_CFG.en_mstr and I2C_CFG.en_slave are both zero.
2	transmit	Bit is set by firmware to define the direction of the byte transfer. Any Start detect will clear the bit. 0 receive mode 1 transmit mode. This bit is held zero if I2C_CFG.en_mstr and I2C_CFG.en_slave are both zero. See Table 1-111.
1	lrb	Last Received Bit. The value of the 9th bit in a Transmit sequence, which is the acknowledge bit from the receiver. Any Start detect or a write to the Start or Restart generate bits, when operating in Master mode, will also clear the bit. 0 last transmitted byte was ACK'ed by the receiver. 1 last transmitted byte was NACK'ed by the receiver. This bit is held zero if I2C_CFG.en_mstr and I2C_CFG.en_slave are both zero.

(continued)

0	byte_complete	Transmit/Receive Mode: 0 no completed transmit/receive since last cleared by firmware. Any Start detect or a write to the start or Restart generate bits, when operating in Master mode, will also clear the bit. Transmit mode: 1 eight bits of data have been transmitted and an ACK or NACK has been received. Receive mode: 1 eight bits of data have been received. This bit is held zero if I2C_CFG.en_mstr and I2C_CFG.en_slave are both zero.

Table 1-111. Bit field encoding: transmit_enum

Value	Name	Description
1'b1	TRANSMIT_EN	Bytes are transferred from the device
1'b0	TRANSMIT_DIS	Bytes are received from the device

1.3.190 I2C_D

I2C Data Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

I2C_D: 0x49D8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	data							

This register provides read/write access to the Shift register. This register is read only for received data and write only for transmitted data.

Bits	Name	Description
7:0	data[7:0]	Read received data or write data to transmit. These bits are held zero if I2C_CFG.en_mstr and I2C_CFG.en_slave are both zero.

1.3.191 I2C_MCSR

I2C Master Control and Status Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

I2C_MCSR: 0x49D9

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R:0	R:0	R/W:0	R/W:0
HW Access	NA			R/W	R/W	R/W	R/W	R/W
Retention	NA			NONRET	NONRET	NONRET	NONRET	NONRET
Name	RSVD			stop_gen	bus_busy	master_mode	restart_gen	start_gen

This register implements I2C framing controls and provides Bus Busy status. Bits in this register are held in reset until one of the enable bits in CFG is set. In the table above, note that reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits should always be written with a value of '0'.

Bits	Name	Description
4	stop_gen	This bit is set only for master transmitter and used at the end of byte transfer. After byte complete status is set, if this bit is set followed by the Transmit bit in I2C.CSR register, Stop condition is generated after byte complete. This bit is automatically reset to 0 after the Stop, start or Restart has been generated. During data phase, if Stop Gen bit is set to 0, clearing the Transmit bit in I2C.CSR register will also generate a Stop condition. This bit is held zero if I2C_CFG.en_mstr and I2C_CFG.en_slave are both zero.
3	bus_busy	This bit is set to the following. 0 when a Stop condition is detected (from any bus master). 1 when a Start condition is detected (from any bus master). This bit is held zero if I2C_CFG.en_mstr and I2C_CFG.en_slave are both zero.
2	master_mode	This bit is set/cleared by hardware when the device is operating as a master. 0 stop condition detected, generated by this device. 1 start condition detected, generated by this device. This bit is held zero if I2C_CFG.en_mstr and I2C_CFG.en_slave are both zero.
1	restart_gen	This bit is cleared by hardware when the Restart generation is complete. 0 restart generation complete. 1 generate a Restart condition. This bit is held zero if I2C_CFG.en_mstr and I2C_CFG.en_slave are both zero.
0	start_gen	This bit is cleared by hardware when the Start generation is complete. 0 start generation complete. 1 generate a Start condition and send a byte (address) to the I2C bus, if bus is not busy. This bit is held zero if I2C_CFG.en_mstr and I2C_CFG.en_slave are both zero.

1.3.192 I2C_CLK_DIV1

I2C Clock Divide Factor Register-1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

I2C_CLK_DIV1: 0x49DB

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	divide_factor_1							

This register has the 8 LSB bits of the 10-bit Clock Divider.

Bits	Name	Description
7:0	divide_factor_1[7:0]	The configuration of this register along with that in register CLK_DIV2 defines the factor by which the SYSCLK will be divided in the I2C block. These bits are held zero if I2C_CFG.en_mstr and I2C_CFG.en_slave are both zero.

1.3.193 I2C_CLK_DIV2

I2C Clock Divide Factor Register-2

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

I2C_CLK_DIV2: 0x49DC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:00	
HW Access	NA						R	
Retention	NA						NONRET	
Name	RSVD						divide_factor_2	

This register has the 2 MSB bits of the 10-bit Clock Divider.

Bits	Name	Description
1:0	divide_factor_2[1:0]	The configuration of this register along with that in register CLK_DIV1 defines the factor by which the SYSCLK will be divided in the I2C block. These bits are held zero if I2C_CFG.en_mstr and I2C_CFG.en_slave are both zero.

1.3.194 DEC_CR

Decimator Control Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DEC_CR: 0x4E00

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:00		R/W:0	R/W:0
HW Access	R	R	R	R	R		R	R/W
Retention	NONRET	NONRET	NONRET	NONRET	NONRET		NONRET	NONRET
Name	sat_en	fir_en	ocor_en	gcor_en	conv_mode		xstart_en	start_conv

This register provides information about start, stop, mode, and feature enables. A read of this register produces the last value written to this register with the exception of bit 0. If a 1 is read from bit 0 and conv_mode doesn't = 00 this indicates the filter is running. If a 0 is read and conv_mode doesn't = 00 the block is in the standby state. If conv_mode = 00 bit 0 has no meaning and could be 1 or 0.

Bits	Name	Description
7	sat_en	Controls saturation logic in the Post Processing filter. When enabled, the resulting outputs of the Post Processing filter are held to the most positive or negative values, rather then wrapping around. Conversion results are unpredictable if this bit is changed while the Post Processing filter is running. This bit is ignored if FIR_EN, OCOR_EN and GCOR_EN are all 0. This feature is used to prevent wrap-around if the Decimator is mis-configured when using the Post Processor. NOTE: This is different from the Overflow Correction described in DR2H See Table 1-116.
6	fir_en	Controls whether or not Post Processing filter implements a FIR filter. If this bit is set it enables the Post Processing filter. Conversion results are unpredictable if this bit is changed while the filter is running. The decimation period of this filter is controlled by the DR2 bits in register DR2 and DR2H. See Table 1-113.
5	ocor_en	This bit controls the offset correction feature of the Post Processing filter. If this bit is set it enables the Post Processing filter. The offset value is programmed in the OCOR bits of registers OCOR, OCORM and OCORH. Conversion results are unpredictable if this bit is changed while the filter is running. See Table 1-115.
4	gcor_en	This bit controls the gain correction feature of the Post Processing filter. If this bit is set it enables the Post Processing filter. The gain coefficient is programmed in the GCOR bits of registers GCOR and GCORH. Which bits in this 16-bit field that are valid is set in GVAL. Conversion results are unpredictable if this bit is changed while the filter is running. When this feature is enabled, the DR1 register field must be set to a value higher than 32 (worst case) for proper operation. See the DR1 register definition of cases where values less than 32 are allowed. See Table 1-114.

(continued)

3:2	conv_mode[1:0]	The value in these two bits controls the sampling mode the Decimator runs in. Single Sample mode resets all values in the ADC path, captures one sample (4 decimation cycles) and returns to the Standby state. Fast Filter mode is a continuous running Single Sample mode - the ADC path being reset between each sample. Continuous mode resets the ADC path, generates a sample and then without resetting the ADC path, generates a new sample every decimation cycle thereafter. Fast FIR mode is the same as the Continuous mode except it resets the ADC channel and starts again at the termination of the DR2 (FIR Filter) period. If Fast FIR mode is selected and FIR Enable is not set in bit 6, Fast FIR and Continuous mode function the same. Conversion results are unpredictable if these bits are changed while the filter is running. See Table 1-112.
1	xstart_en	Controls whether DSI signal ext_start is active. If XSTART_EN is high, it allows the ext_start input to start a conversion just as START_CONV does. Regardless of the state of this bit, writing to START_CONV will start a conversion. See Table 1-118.
0	start_conv	A write of 1 to this bit starts a conversion (regardless of the state of XSTART_EN) according to the CONV_MODE set in bits 2, 3. If read, a 1 indicates the filter is running when not in Single Sample mode. If a 0 is read the block is in the standby state when not in Single Sample mode. When in Single Sample more this bit is cleared shortly after it is written and does not reflect the running state of the Decimator. If the Decimator is running in Single Sample Mode and this bit is written with a 1 the conversion start is queued, and will start then the previous one completes. If a 1 is read from this bit when in Single Sample Mode it indicates a conversion start is queued. Note that the other bits of this CSR are not queued so queued SS Mode starts must set the same bits in this register as the conversion running. If 0 is written to this bit, it forces the block into the Standby start via a soft-reset. This soft-reset works in any mode and at any time and takes a minimum of 1 and maximum of 2 adc_clk cycles to complete. If a 1 is written before the soft-reset has completed, the start is queued and the conversion will start when the soft-reset is complete. See Table 1-117.

Table 1-112. Bit field encoding: conv_modes_enum

Value	Name	Description
2'b00	SINGLE_SAMPLE	Single Sample Mode.
2'b01	FAST_FILTER	Fast Filter Mode.
2'b10	CONTINUOUS	Continuous Mode.
2'b11	FAST_FIR	Fast FIR.

Table 1-113. Bit field encoding: fir_en_enum

Value	Name	Description
1'b1	FIR_EN	FIR filter function is on.
1'b0	FIR_DIS	FIR filter function disabled.

Table 1-114. Bit field encoding: gcor_en_enum

Value	Name	Description
1'b1	GCOR_EN	Gain correction enabled.
1'b0	GCOR_DIS	Default: no gain correction.

Table 1-115. Bit field encoding: ocor_en_enum

Value	Name	Description
1'b1	OCOR_EN	Offset correction enabled.
1'b0	OCOR_DIS	No offset correction.

Table 1-116. Bit field encoding: sat_en_enum

Value	Name	Description
1'b1	SAT_EN	Saturation Control Enabled.
1'b0	SAT_DIS	No saturation control.

(continued)

Table 1-117. Bit field encoding: start_conv_enum

Value	Name	Description
1'b1	DEC_START	Initiate a conversion.
1'b0	DEC_STOP	Kill current conversion (if running) and enter Standby state (SW reset).

Table 1-118. Bit field encoding: xstart_en_enum

Value	Name	Description
1'b1	XSTART_EN	Enable the DSI input signal ext_start to start a conversion.
1'b0	XSTART_DIS	Default: DSI signal ext_start is disabled.

1.3.195 DEC_SR

Decimator Status Register

Reset: Reset Signals Listed Below

Register : Address

DEC_SR: 0x4E01

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	W:0	R/W:0	R:0
HW Access	NA		R	R	R	R	R	R/W
Retention	NA		RET	RET	RET	NONRET	RET	NONRET
Name	RSVD		coreclk_disable	intr_pulse	out_align	intr_clr	intr_mask	conv_done

This register provides information about interrupt, polling, status, and control features.

Bits	Name	Description
5	coreclk_disable	This bit when set high disables (gates off) the clock to the entire core of the block (adc_clk). This includes all FFs except those used for the AHB interface and CSRs. When disabled (set high) the AHB interface to the CSR is still fully functional. This bit is ANDed with the primary input signal cic_clk_en to control the clock gate. cic_clk_en must be high and CoreCLK_Disable must be low for the clock to run. See Table 1-120.
4	intr_pulse	This read/write bit selects if cic_intr is pulse or level sensed. If level, a sample completion sets cic_intr high where it remains until bit 2 is written, a soft-reset if performed or if OUTSAMP/M/H is read. If pulse, a single cycle (pclk) strobe is generated on cic_intr to be used as an edge sensed interrupt or a DMAREQ. Regardless of which is selected, the interrupt output is still subject to masking by bit 1. See Table 1-123.
3	out_align	This bit when set high causes a read of OUTSAMP to produce the contents of OUTSAMPM and OUTSAMPM to produce the contents of OUTSAMPH. Effectively, this is an 8-bit right shift of the result. Note that the setting of this bit does not alter the content of the OUTSAMP registers. Setting this bit simply realigns the byte lanes when the register is read. If this bit is set low, the OUTSAMP registers are read normally. This feature is added to allow the SW to read 9 to 16 bit samples from the Decimator in one cycle on bits 15:0. Note also that when using Coherency checking in conjunction with this alignment feature that the Key Coherency Byte selected in the COHER register is referenced based on the address of the register being read, not the content delivered on the bus. This means that if this bit is set high with the intent to read sample data 23:8 on 15:0 that they Key Coherency Byte should be set to either OUTSAMP or OUTSAMPM, not OUTSAMPH. See Table 1-124.
2	intr_clr	INTR_CLR is a write-only bit that clears bit0 and cic_intr. A read always produces a 0. See Table 1-121.
1	intr_mask	INTR_MASK is a RD/WR bit that controls the generation of the conversion completion interrupt. A read produces that last value written to this bit. This bit functions as a mask regardless of the value of bit 4 (INTR PULSE). See Table 1-122.

(continued)

0	conv_done	CONV_DONE is a read-only bit indicating that the most recently started conversion has completed if it has been cleared since the last sample read. This same bit is the interrupt signal cic_intr when bit 4 is low, if not masked by bit 1. This bit is intended to provide a polling mechanism should this be preferred to receiving interrupts. It is cleared by writing a 1 to bit 2, a soft-reset or a read of register OUTSAMP, OUTSAMPM or OUTSAMPH (regardless of Coherency settings). See Table 1-119.

Reset Table

Reset Signal	Applicable Register Bit(s)
System reset for retention flops [reset_all_retention]	intr_mask, out_align, intr_pulse, coreclk_disable
Domain reset for non-retention flops [reset_all_nonretention]	conv_done, intr_clr

Table 1-119. Bit field encoding: conv_done_enum

Value	Name	Description
1'b1	CONV_COMP	Most recently started conversion completed.
1'b0	CONV_NOTCOMP	Conversion not completed since last clear.

Table 1-120. Bit field encoding: coreclk_disable_enum

Value	Name	Description
1'b1	CORECLK_DISABLE_HIGH	Core Clock is Disabled
1'b0	CORECLK_DISABLE_LOW	Core Clock is Enabled

Table 1-121. Bit field encoding: intr_clr_enum

Value	Name	Description
1'b1	INTR_CLEAR	Clears CONV_DONE and the interrupt on cic_intr (if enabled).
1'b0	INTR_NOP	No affect.

Table 1-122. Bit field encoding: intr_mask_enum

Value	Name	Description
1'b1	INTR_MASKED	Masks the interrupt generation on cic_intr.
1'b0	INTR_ENABLED	Allows CONV_DONE to generate an interrupt.

Table 1-123. Bit field encoding: intr_pulse_enum

Value	Name	Description
1'b1	INTR_PULSE	Selects a pulse interrupt on cic_intr.
1'b0	INTR_LEVEL	Selects a level interrupt on cic_intr.

Table 1-124. Bit field encoding: out_align_enum

Value	Name	Description
1'b1	OUT_ALIGN_HIGH	Shifts SAMP registers right by 8-bits
1'b0	OUT_ALIGN_LOW	No affect on SAMP Registers

1.3.196 DEC_SHIFT1

Decimator Shifter 1 (Input)

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_SHIFT1: 0x4E02

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:00000				
HW Access	NA			R				
Retention	NA			RET				
Name	RSVD			shift1				

This register provides control information to the input (left) shifter. SHIFT1 is a 5-bit field that sets the amount of left shift that the Modulator input will be shifted. Disturbing this field during a conversion will disturb the output value. This register should only be updated while the CIC filter is in the Standby state. Conversion results are unpredictable if these bits are changed while the filter is running. Not all values from 0 to 31 make computational sense. A read of this register produces the last value written to this register.

Bits	Name	Description
4:0	shift1[4:0]	Value for left shift amount of modulator input data. 0 = no shift, 1 = left shift by 1 bit, ... up to the max supported 31.

1.3.197 DEC_SHIFT2

Decimator Shifter 2 (Output)

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_SHIFT2: 0x4E03

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Retention	NA				RET			
Name	RSVD				shift2			

This register provides control of the post CIC (output) shifter. This shifter sits at the input of the Post Processor and is only functional on the CIC output sample when the Post Processor is in use. SHIFT2 is a 4-bit field that sets the amount of right shift on the output of the CIC filter as it enters the Post Processor. Changing this field during a conversion will disrupt the output value. Conversion results are unpredictable if these bits are changed while the filter is running. Shift2 shifts right by the amount held in this register. Not all values from 0 to 15 make computational sense. A read of this register produces the last value written to this register.

Bits	Name	Description
3:0	shift2[3:0]	Value for the amount of right shift for the output of the CIC filter prior to entering the Post Processor. Functional values range from 0 to 15, 0 = no shift.

1.3.198 DEC_DR2

Decimator Decimation Rate (2)

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_DR2: 0x4E04

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	dr2_low							

This register provides information to the Post Processor about the decimation rate of the FIR filter. This is a 10-bit field that sets the decimation ratio in the Post Processing filter. The upper 2 bits are found in register DR2H. The decimation ratio minus 1 in binary is the number to program in this 10-bit field. Valid decimation ratios are 2 to 1024. Changing this field during a conversion will disrupt the output value. Conversion results are unpredictable if these bits are changed while the filter is running. A read of this register produces the last value written to this register.

Bits	Name	Description
7:0	dr2_low[7:0]	FIR Filter decimation ratio bits [7:0] (of [9:0]).

1.3.199 DEC_DR2H

Decimator Decimation Rate (2) and Overflow Correction

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_DR2H: 0x4E05

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000					NA:0	R/W:00	
HW Access	R					NA	R	
Retention	RET					NA	RET	
Name	of_width					RSVD	dr2_high	

This register provides information to the Post Processor about the decimation rate of the FIR filter. This is a 10-bit field that sets the decimation ratio in the Post Processing filter. The lower 8 bits are found in register DR2. The decimation ratio minus 1 in binary is the number to program in this 10-bit field. Valid decimation ratios are 2 to 1024. The OverFlow Correction Width field is used to correct for 2's compliment overflow in output results. For n bit results the CIC filter will create a maximum number of +2^n (for positive ranges) or +2^(n-1) (for signed ranges) which both need (n+1) bits to represent. When read truncated to n bits this produces errors in the output range. This field allows SW to program a reference to the size of n and where the n bits are in the output register and it controls correction HW that clamps the output value to +2^n-1 and +2^(n-1)-1, respectively. Changing either of the fields in this register during a conversion will disrupt the output value. Conversion results are unpredictable if this register is changed while the Decimator is running. A read of this register produces the last value written to this register.

Bits	Name	Description
7:3	of_width[4:0]	Occupying the top 5 bits of this register is the Overflow Correction Bit-Width field (it is unrelated to the DR2). This field both enables and sets the bit width of the Overflow Correction logic in the CIC core. With n = number of bits in the sample SW will read from OUTSAMP, the following formula gives the value to program into OF_WIDTH: OF_WIDTH = n-1+s (for signed ranges), OF_WIDTH = n+s (for positive ranges) -- where s = the number of bit positions the result field is left-shifted from the lsb of the OUTSAMP register. Examples: For an 8-bit result that is lsb aligned in OUTSAMP and is signed, n=8, s=0 so: OF_WIDTH = 8-1+0 = 7. For an 8-bit result that is lsb aligned in OUTSAMP and is a positive range: OF_WIDTH = 8+0 = 8. For a signed 12-bit result that is shifted into the high two bytes: OF_WIDTH = 12-1+8 = 19. Functional values of OF_WIDTH are 5 to 22 (6 to 23-bit numbers). Any other value in this field disables the Overflow Correction feature and data is not altered when passing through the Overflow Correction logic. Overflow Correction only works on positive numbers. Example: If OF_WIDTH is set to 7 (for an 8-bit signed value) and given a range of -144 to 144, the 144 will get truncated to 127 but the -144 will not get truncated.
1:0	dr2_high[1:0]	FIR Filter decimation ratio bits [9:8] (of [9:0]). See description in DR2 register

1.3.200 DEC_DR1

Decimator Decimation Rate (1) of CIC Filter

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_DR1: 0x4E06

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	dr1							

DR1 is an 8-bit field that sets the decimation ratio in the CIC filter. The decimation ratio minus 1 in binary is the number to program in this register. Valid decimation ratios are any value in the range 2 to 256 (program 1-255) for all modes where the Post Processor is not in use. Note this does not mean the results will be valid. For higher levels of input data (moddat), higher DR1 values will saturate the CIC filter and give meaningless results. This is true for any of the 4 modes Single Sample, Continuous, Fast Filter or Fast FIR. Because the Post Processor needs time to perform its enabled calculations, the minimum DR1 for cases where the Post Process is enabled are greater and are a function of what Post Processing features are enabled. These restrictions also apply to SS Mode if started back-to-back or queued. Minimum DR1 values for each are given as: Offset Correction: DR1 >= 4, FIR (Sync1): DR1 >= 4, Both Offset and FIR: DR1 >= 5, Gain Correction: DR1 >= GVAL + 5, Gain and Offset: DR1 >= GVAL + 6, Gain and FIR: DR1 >= GVAL + 6, Gain and Offset and FIR: DR1 >= GVAL + 7, (where GVAL is the 0-based value programmed into the register). Changing this field during a conversion will disrupt the output value. Conversion results are unpredictable if these bits are changed while the filter is running.

Bits	Name	Description
7:0	dr1[7:0]	CIC Filter decimation rate.

1.3.201 DEC_OCOR

Decimator Offset Correction Coefficient (Low Byte)

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_OCOR: 0x4E08

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	ocor_low							

OCOR / OCORM / OCORH is a 24-bit 2's compliment signed field that is the offset correction value used if the Post Processor Offset feature is enabled. The field is specified in registers OCOR, OCORM, and OCORH. This register may be written while the filter is running. OCOR, OCORM and OCORH can be coherency interlocked (selectable in the COHER register). A Key Coherency Byte can be defined in the COHER register. If any byte of the Offset field is written the field is flagged incoherent until the Key Coherency Byte is written. Once the Key Coherency Byte is written the field is flagged coherent again. When not coherent, the HW will not pass any portion of the 24-bit number to the Post Processor. When incoherent, the previous Offset value is used. A new Offset value is accepted when a write to the Key Coherency Byte is seen - as defined in the COHER register. The 3 bytes of the Offset field may be written in any order but the Key Coherency Byte must be written last.

Bits	Name	Description
7:0	ocor_low[7:0]	Offset correction coefficient bits [7:0] (of [23:0]).

1.3.202 DEC_OCORM

Decimator Offset Correction Coefficient (Middle Byte)

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_OCORM: 0x4E09

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	ocor_mid							

See descripion in OCOR register above.

Bits	Name	Description
7:0	ocor_mid[7:0]	Offset correction coefficient bits [15:8] (of [23:0]).

1.3.203 DEC_OCORH

Decimator Offset Correction Coefficient (High Byte)

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_OCORH: 0x4E0A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	ocor_high							

See description in OCOR register above.

Bits	Name	Description
7:0	ocor_high[7:0]	Offset correction coefficient bits [23:16] (of [23:0]).

1.3.204 DEC_GCOR

Decimator Gain Correction Coefficient (Low Byte)

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_GCOR: 0x4E0C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	gcor_low							

GCOR / GCORH is a 16-bit field that is the gain correction value for the Post Processor. The field is specified in registers GCOR and GCORH. This register may be written while the filter is running. If a multiply is in progress, updates to the gain correction value will be ignored until the start of the next multiply. Which bits that are valid in the 16 bit field is signified in the GVAL register. The implementation in HW is a shift_add multiply which consumes a clock cycle (adc_clk) for each valid bit in the GCOR field as defined by GVAL. GCOR, GCORH and GVAL can be coherency interlocked (selectable in the COHER register). A Key Coherency Byte can be defined in the COHER register. If any byte of the Gain/Gain_Value field is written the field is flagged incoherent until the Key Coherency Byte is written. Once the Key Coherency Byte is written the field is flagged coherent again. When not coherent, the HW will not pass any portion of the 16-bit Gain number or 8-bit Gain Value to the Post Processor. When incoherent, the previous written values are used. A new Gain/Gain_Value is accepted when a write to the Key Coherency Byte is seen - as defined in the COHER register. The 3 bytes of the Gain/Gain_Value field may be written in any order but the Key Coherency Byte must be written last. READ: A read of this register produces the last value written to this register. Reads have no affect on coherency flags.

Bits	Name	Description
7:0	gcor_low[7:0]	Gain correction coefficient bits [7:0] (of [15:0]).

1.3.205 DEC_GCORH

Decimator Gain Correction Coefficient (High Byte)

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_GCORH: 0x4E0D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	gcor_high							

Seed description of GCOR register above.

Bits	Name	Description
7:0	gcor_high[7:0]	Gain correction coefficient bits [15:8] (of [15:0]).

1.3.206 DEC_GVAL

Decimator Gain Correction Size Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_GVAL: 0x4E0E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Retention	NA				RET			
Name	RSVD				gval			

GVAL is a 4-bit field that signifies to the HW how many bits of GCOR field are valid. The number of valid bits minus one should be written (0000b = 1 bit, 1111b = all 16 bits). Updates to this register will be ignored until the start of the next multiply. This register may be written while the filter is running. The valid field is measured from LSB (bit 0) up. Note that the HW always assumes the field specified by GVAL is left justified (starts at bit 0 of GCOR) and has a binary-point after the left-most digit. For example, if GVAL is programmed with a 7d, this means there are 8 valid bits in GCOR and they have the format x.xxxxxxxb. If GCOR (GCORH, GCOR) holds the value 00000000 10100000b and GVAL is 7, only the low-order 8 bits are considered (10100000b) and the binary point is assumed after the left-most digit (1.0100000b). The multiply coefficient in the example would be 1.25d. Although a good explanation example, this isn't the most efficient way to multiply by 1.25d. Better would be GCOR (GCORH, GCOR) holds the value 00000000 00000101b and GVAL is 2, which gives (1.01b). Another example: If it is desired to multiply by a gain coefficient of 0.125d (0.001b) then GCOR would be programmed with a value of 00000001b, GCORH with 00000000b and GVAL (GVAL) with 0011b - meaning there are 4 valid bits x.xxxb. The multiplier thus has a coefficient range of 1/(2^15) to 2.0-(1/(2^15)) in steps of 1/(2^15) GCOR, GCORH and GVAL can be coherency interlocked (selectable in the COHER register). A Key Coherency Byte can be defined in the COHER register. If any byte of the Gain/Gain_Value field is written the field is flagged incoherent until the Key Coherency Byte is written. Once the Key Coherency Byte is written the field is flagged coherent again. When not coherent, the HW will not pass any portion of the 16-bit Gain number or 8-bit Gain Value to the Post Processor. When incoherent, the previous written values are used. A new Gain/Gain_Value is accepted when a write to the Key Coherency Byte is seen - as defined in the COHER register. The 3 bytes of the Gain/Gain_Value field may be written in any order but the Key Coherency Byte must be written last. READ: A read of this register produces the last value written to this register. Reads have no affect on coherency flags.

Bits	Name	Description
3:0	gval[3:0]	Number of valid bits minus one in Gain Coefficient registers GCORH and GCOR.

1.3.207 DEC_OUTSAMP

Decimator Output Data Sample (Low Byte)

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DEC_OUTSAMP: 0x4E10

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	NONRET							
Name	samp_low							

This register is read-only and contains the low order byte of the conversion result. In some configurations of the block the output results of interest are placed in bits 23:8 of the output sample field. To allow reading such values in one bus cycle an alignment feature is added to shift the result right by 8-bits. This feature is enabled by the OUTPUT_ALIGN bit of the SR register. This register can be coherency interlock protected (selectable in the COHER register). A Key Coherency Byte can be defined in the COHER register. If any byte of the OUTSAMP / OUTSAMPM / OUTSAMPH field is read the field is flagged incoherent until the Key Coherency Byte is read. Once the Key Coherency Byte is read the field is flagged coherent again. When the Decimator generates a new sample and the output sample field is coherent, the output sample field is over-written with the new value - regardless of whether it had been read prior or not. If the output sample field is flagged incoherent when the new sample is generated, the new sample is lost and the output sample field is left untouched. There is no warning given when either a new sample is lost or an unread output sample is overwritten. WRITE: This register is read-only - writes to this address complete but have no affect.

Bits	Name	Description
7:0	samp_low[7:0]	Low order byte of the filter conversion result, bits [7:0] (of [23:0]) --- Or if the out_align bit is set it contains bits [15:8] (of [23:0]).

1.3.208 DEC_OUTSAMPM

Decimator Output Data Sample (Middle Byte)

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DEC_OUTSAMPM: 0x4E11

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	NONRET							
Name	samp_middle							

This register is read-only and contains the middle order byte of the conversion result. In some configurations of the block the output results of interest are placed in bits 23:8 of the output sample field. To allow reading such values in one bus cycle an alignment feature is added to shift the result right by 8-bits. This feature is enabled by the OUTPUT_ALIGN bit of the SR register. This register can be coherency interlock protected (selectable in the COHER register). A Key Coherency Byte can be defined in the COHER register. If any byte of the OUTSAMP / OUTSAMPM / OUTSAMPH field is read the field is flagged incoherent until the Key Coherency Byte is read. Once the Key Coherency Byte is read the field is flagged coherent again. When the Decimator generates a new sample and the output sample field is coherent, the output sample field is over-written with the new value - regardless of whether it had been read prior or not. If the output sample field is flagged incoherent when the new sample is generated, the new sample is lost and the output sample field is left untouched. There is no warning given when either a new sample is lost or an unread output sample is overwritten. WRITE: This register is read-only - writes to this address complete but have no affect.

Bits	Name	Description
7:0	samp_middle[7:0]	Middle order byte of the filter conversion result, bits [15:8] (of [23:0]) --- Or if the out_align bit is set it contains bits [23:16] (of [23:0]).

1.3.209 DEC_OUTSAMPH

Decimator Output Data Sample (High Byte)

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DEC_OUTSAMPH: 0x4E12

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	NONRET							
Name	samp_high							

This register is read-only and contains the high order byte of the conversion result. This register can be coherency interlock protected (selectable in the COHER register). A Key Coherency Byte can be defined in the COHER register. If any byte of the OUTSAMP / OUTSAMPM / OUTSAMPH field is read the field is flagged incoherent until the Key Coherency Byte is read. Once the Key Coherency Byte is read the field is flagged coherent again. When the Decimator generates a new sample and the output sample field is coherent, the output sample field is over-written with the new value - regardless of whether it had been read prior or not. If the output sample field is flagged incoherent when the new sample is generated, the new sample is lost and the output sample field is left untouched. There is no warning given when either a new sample is lost or an unread output sample is overwritten. Note that even though there is no register defined for the high byte (address xx13) of this register, if this register is read as a 16-bit access the top byte will contain the sign extension. WRITE: This register is read-only - writes to this address complete but have no affect.

Bits	Name	Description
7:0	samp_high[7:0]	High order byte of the filter conversion result, bits [23:16] (of [23:0]).

1.3.210 DEC_OUTSAMPS

Decimator Output Data Sample (Sign Extension)

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DEC_OUTSAMPS: 0x4E13

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	samp_signext							

* This is a pseudo register. There are no FFs or even an address decode for this pseudo register. If read or written as a byte it acts the same as all other unused byte addresses in the block's address space - writes are ignored and reads produce 0 on the bus. However, if OUTSAMPH is read as a 16-bit value, it is sign extended onto the bus on these 8 bits. This pseudo register definition is here simply to document this sign extension functionality. WRITE: This register is read-only - writes to this address complete but have no affect. If read as a byte, it always returns 0. If read as the high byte of a 16-bit read of OUTSAMPH, it always returns the sign extension of the value in OUTSAMP/M/H.

Bits	Name	Description
7:0	samp_signext[7:0]	Sign extension of the value held in OUTSAMP.

1.3.211 DEC_COHER

Decimator Coherency Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DEC_COHER: 0x4E14

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:00		R/W:00		R/W:00	
HW Access	NA		R		R		R	
Retention	NA		RET		RET		RET	
Name	RSVD		gcor_key		ocor_key		samp_key	

The three 2-bit fields of this register are used to select which of the 3 bytes (of the OCOR, GCOR/GVAL and OUTSAMP fields) will be used as the Key Coherency Byte (KCB). Or, if no coherency checking is desired, to turn it off. The KCB selected is SW's way of tell the HW which byte of the 3-byte field it will access to signify the completion of a coherent operation. For the OCOR and GCOR/GVAL 3-byte fields, selecting the key byte tells the HW which of the bytes it will write last to note that all of the bytes it wants to update have been written. When any non-Key byte is written, the coherency HW locks the underlying ALU hardware from seeing the potentially incoherent value. While incoherent the ALU uses a shadow copy of the last coherent value received. The SW lastly writes the KCB and the HW flags the field as coherent and the next ALU operation needing that coefficient will get a copy of the newly written value. The OUTSAMP field is basically the same other than it's a read only register and the coherency protects the output sample from being overwritten by a subsequent sample if the present sample is in the process of being read (this is technically an overrun condition). If no byte of the previous sample has been read, a new sample will overwrite the last. If the previous sample is in the process of being read, a new sample will be dropped. Coherency doesn't protect againt over/under flow, it only makes sure the sample read is coherent.

Bits	Name	Description
5:4	gcor_key[1:0]	Sets the Key Coherency Byte of the GCOR/GCORH/GVAL field See Table 1-125.
3:2	ocor_key[1:0]	Sets the Key Coherency Byte of the OCOR/OCORM/OCORH field See Table 1-126.
1:0	samp_key[1:0]	Sets the Key Coherency Byte of the OUTSAMP/OUTSAMPM/OUTSAMPH field See Table 1-127.

Table 1-125. Bit field encoding: gcor_key_enum

Value	Name	Description
2'b00	GCOR_KEY_OFF	Gain Coefficient Coherency checking off.
2'b01	GCOR_KEY_LOW	Key Byte is low byte (GCOR).
2'b10	GCOR_KEY_MID	Key Byte is med byte (GCORH).
2'b11	GCOR_KEY_HIGH	Key Byte is high byte (GVAL).

Table 1-126. Bit field encoding: ocor_key_enum

Value	Name	Description
2'b00	OCOR_KEY_OFF	Offset Coefficient Coherency checking off.
2'b01	OCOR_KEY_LOW	Key Byte is low byte (OCOR).
2'b10	OCOR_KEY_MID	Key Byte is med byte (OCORM).
2'b11	OCOR_KEY_HIGH	Key Byte is high byte (OCORH).

(continued)

Table 1-127. Bit field encoding: samp_key_enum

Value	Name	Description
2'b00	SAMP_KEY_OFF	Output Sample Coherency checking off.
2'b01	SAMP_KEY_LOW	Key Byte is low byte (OUTSAMP).
2'b10	SAMP_KEY_MID	Key Byte is med byte (OUTSAMPM).
2'b11	SAMP_KEY_HIGH	Key Byte is high byte (OUTSAMPH).

1.3.212 TMR[0..3]_CFG0

Configuration Register CFG0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_CFG0: 0x4F00 TMR1_CFG0: 0x4F0C TMR2_CFG0: 0x4F18

TMR3_CFG0: 0x4F24

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R		R	R	R	R	R	R
Retention	RET		RET	RET	RET	RET	RET	RET
Name	DEADBAND_PERIOD		DB	INV	CMP_BUFF	ONESHOT	MODE	EN

This register is used to configure the timer block.

Bits	Name	Description
7:6	DEADBAND_PERIOD[1:0]	Deadband Period
5	DB	Deadband mode--Deadband phases phi1 and phi2 are outputted on CMP and TC output pins respectively. See Table 1-128.
4	INV	Invert sense of TIMEREN signal
3	CMP_BUFF	Buffer compare register. Compare register updates only on timer terminal count.
2	ONESHOT	Timer stops upon reaching stop condition defined by TMR_CFG bits. Can be restarted by asserting TIMER RESET or disabling and re-enabling block.
1	MODE	Mode. (0 = Timer; 1 = Comparator) See Table 1-129.
0	EN	Enables timer/comparator.

Table 1-128. Bit field encoding: db_enum

Value	Name	Description
1'b0	Timer	CMP and TC are output.
1'b1	Deadband	PHI1 (instead of CMP) and PHI2 (instead of TC) are output.

Table 1-129. Bit field encoding: mode_enum

Value	Name	Description
1'b0	Timer	Timer mode. CNT/CMP register holds timer count value.
1'b1	Comparator	Comparator mode. CNT/CMP register holds comparator threshold value.

1.3.213 TMR[0..3]_CFG1

Configuration Register CFG1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_CFG1: 0x4F01 TMR1_CFG1: 0x4F0D TMR2_CFG1: 0x4F19

TMR3_CFG1: 0x4F25

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:000			R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R			R	R	R	R
Retention	RET	RET			RET	RET	RET	RET
Name	BUS_CLK_SEL	CLK_BUS_EN_SEL			DBMODE	DCOR	FTC	IRQ_SEL

This register is used to configure the timer block.

Bits	Name	Description
7	BUS_CLK_SEL	Bus Clock selection. See Table 1-130.
6:4	CLK_BUS_EN_SEL[2:0]	Digital Global Clock selection. See Table 1-131.
3	DBMODE	Deadband mode (asynchronous/synchronous). CMP output pin is also affected when not in deadband mode (CFG0.DEADBAND). See Table 1-132.
2	DCOR	Disable Clear on Read (DCOR) of Status Register SR0. See Table 1-133.
1	FTC	First Terminal Count (FTC). Setting this bit forces a single pulse on the TC pin when first enabled. See Table 1-134.
0	IRQ_SEL	Irq selection. (0 = raw interrupts; 1 = status register interrupts) See Table 1-135.

Table 1-130. Bit field encoding: bus_sel_enum

Value	Name	Description
1'b0	clk_d	Use the digital clocks, clk_d[*], as system clock.
1'b1	clk_bus	Use the system bus clock, clk_bus, as system clock.

Table 1-131. Bit field encoding: clk_cfg_enum

Value	Name	Description
3'b000	clk_d0	Select digital clock 0, clk_d[0], as clock enable.
3'b001	clk_d1	Select digital clock 1, clk_d[1], as clock enable.
3'b010	clk_d2	Select digital clock 2, clk_d[2], as clock enable.
3'b011	clk_d3	Select digital clock 3, clk_d[3], as clock enable.
3'b100	clk_d4	Select digital clock 4, clk_d[4], as clock enable.
3'b101	clk_d5	Select digital clock 5, clk_d[5], as clock enable.

(continued)

Table 1-131. Bit field encoding: clk_cfg_enum

3'b110	clk_d6	Select digital clock 6, clk_d[6], as clock enable.
3'b111	clk_d7	Select digital clock 7, clk_d[7], as clock enable.

Table 1-132. Bit field encoding: dbmode_enum

Value	Name	Description
1'b0	Asynchronous	Asynchronous kill: Output is gated off immediately, and restored after a minimum of 1 application clock cycle.
1'b1	Synchronous	Synchronous kill: Output is gated of immediately, and restored after a minimum of one full counter period (at the terminal count).

Table 1-133. Bit field encoding: dcor_enum

Value	Name	Description
1'b0	Enable clear on read	Clear status register, SR0, when read.
1'b1	Disable clear on read	Do not clear status register, SR0, when read.

Table 1-134. Bit field encoding: ftc_enum

Value	Name	Description
1'b0	Disable FTC	Disable the single cycle pulse, which signifies the timer is starting.
1'b1	Enable FTC	Enable the single cycle pulse, which signifies the timer is starting.

Table 1-135. Bit field encoding: irq_sel_enum

Value	Name	Description
1'b0	Raw IRQ	IRQ from raw signals, maskable by corresponding mask bit in SR0 register.
1'b1	Status IRQ	IRQ from status signals, maskable by corresponding mask bit in SR0 register. Clear interrupt by writing '0' to corresponding status bit of SR0 register.

1.3.214 TMR[0..3]_CFG2

Configuration Register CFG2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_CFG2: 0x4F02 TMR1_CFG2: 0x4F0E TMR2_CFG2: 0x4F1A

TMR3_CFG2: 0x4F26

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:000			R/W:0	R/W:0	NA:00	
HW Access	R	R			R	R	NA	
Retention	RET	RET			RET	RET	NA	
Name	HW_EN	CMP_CFG			ROD	COD	RSVD	

This register is used to configure the timer block.

Bits	Name	Description
7	HW_EN	When set Timer Enable controls counting.
6:4	CMP_CFG[2:0]	Comparator configuration: 000 = '=='; 001 = '<'; 010 = '<=' 011 = '>'; 100 = '>=' See Table 1-136.
3	ROD	Reset On Disable (ROD). Resets internal state of output logic.
2	COD	Clear On Disable (COD). Clears or gates outputs to zero.

Table 1-136. Bit field encoding: cmp_cfg_enum

Value	Name	Description
3'b000	Equal	Compare Equal '=='
3'b001	Less than	Compare Less Than '<'.
3'b010	Less than or equal	Compare Less Than or Equal '<='.
3'b011	Greater	Compare Greater Than '>'.
3'b100	Greater than or equal	Compare Greater Than or Equal '>='.

Table 1-137. Bit field encoding: tmr_cfg_enum

Value	Name	Description
2'b00	Continuous	Timer runs while EN bit of CFG0 register is set to '1'.
2'b01	Pulsewidth	Timer runs from positive to negative edge of TIMEREN.
2'b10	Period	Timer runs from positive to positive edge of TIMEREN.
2'b11	Irq	Timer runs until IRQ.

1.3.215 TMR[0..3]_SR0

Status Register SR0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_SR0: 0x4F03 TMR1_SR0: 0x4F0F TMR2_SR0: 0x4F1B

TMR3_SR0: 0x4F27

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	RC:0	RC:0	RC:0	RC:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R/W	R/W	R/W	R/W	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	TC	CAP_CMP	TEN	TSTOP	MTC	MCAP_CMP	MTEN	MTSTOP

This register us used to configure interrupt masking and obtain status. Status bits 7-4 are cleared on read.

Bits	Name	Description
7	TC	Terminal count status. Interrupt,Sticky (individual bits)
6	CAP_CMP	Capture/Compare status (MODE = 0--Capture; MODE = 1--Compare). Interrupt,Sticky (individual bits)
5	TEN	Timer enable status. Interrupt,Sticky (individual bits)
4	TSTOP	Timer stop status. Interrupt,Sticky (individual bits)
3	MTC	Terminal count interrupt mask. (0 = Masked; 1 = Unmasked)
2	MCAP_CMP	Capture/Compare interrupt mask (MODE = 0--Capture; MODE = 1--Compare). (0 = Masked; 1 = Unmasked)
1	MTEN	Timer enable interrupt mask. (0 = Masked; 1 = Unmasked)
0	MTSTOP	Timer stop interrupt mask. (0 = Masked; 1 = Unmasked)

1.3.216 TMR[0..3]_PER0

Timer Period Register PER0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_PER0: 0x4F04 TMR1_PER0: 0x4F10 TMR2_PER0: 0x4F1C

TMR3_PER0: 0x4F28

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	TIMER_PERIOD0							

This register contains the count value the timer is loaded with. When enabled the counter down counts from the value of this register to zero. NOTE: A period of 0 is not supported.

Bits	Name	Description
7:0	TIMER_PERIOD0[7:0]	Determines the high byte of the period for the timer.

1.3.217 TMR[0..3]_PER1

Timer Period Register PER1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_PER1: 0x4F05 TMR1_PER1: 0x4F11 TMR2_PER1: 0x4F1D

TMR3_PER1: 0x4F29

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	TIMER_PERIOD1							

This register contains the count value the timer is loaded with. When enabled the counter down counts from the value of this register to zero. NOTE: A period of 0 is not supported.

Bits	Name	Description
7:0	TIMER_PERIOD1[7:0]	Determines the low byte of the period for the timer.

1.3.218 TMR[0..3]_CNT_CMP0

Count/Comparator value CNT/CMP0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_CNT_CMP0: 0x4F06

TMR1_CNT_CMP0: 0x4F12

TMR2_CNT_CMP0: 0x4F1E

TMR3_CNT_CMP0: 0x4F2A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	COUNT_COMPARE0							

This register is a shared register. Its meaning depends upon the value of the MODE bit in the CFG0 register. (MODE = 0--Count value; MODE = 1--Comparator value).

Bits	Name	Description
7:0	COUNT_COMPARE0[7:0]	MODE = 0--LSB of current count value; MODE = 1--LSB of comparator threshold.

1.3.219 TMR[0..3]_CNT_CMP1

Count/Comparator value CNT/CMP1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_CNT_CMP1: 0x4F07 TMR1_CNT_CMP1: 0x4F13

TMR2_CNT_CMP1: 0x4F1F TMR3_CNT_CMP1: 0x4F2B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	COUNT_COMPARE1							

This register is a shared register. Its meaning depends upon the value of the MODE bit in the CFG0 register. (MODE = 0--Count value; MODE = 1--Comparator value).

Bits	Name	Description
7:0	COUNT_COMPARE1[7:0]	MODE = 0--MSB of current count value; MODE = 1--MSB of comparator threshold.

1.3.220 TMR[0..3]_CAP0

Capture Value CAP0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_CAP0: 0x4F08 TMR1_CAP0: 0x4F14 TMR2_CAP0: 0x4F20

TMR3_CAP0: 0x4F2C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	RET							
Name	CAPTURE_VALUE0							

This register holds the captured LSB of the timer count value. A 16-bit read of the CNT register returns the current timer value and captures. An 8-bit LSB read of the CNT register returns the LSB and captures both the LSB and MSB. This register only has meaning when MODE = 0 and is not to be used for any purpose when MODE = 1.

Bits	Name	Description
7:0	CAPTURE_VALUE0[7:0]	Captured LSB of the timer count value.

1.3.221 TMR[0..3]_CAP1

Capture Value CAP1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_CAP1: 0x4F09 TMR1_CAP1: 0x4F15 TMR2_CAP1: 0x4F21

TMR3_CAP1: 0x4F2D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	RET							
Name	CAPTURE_VALUE1							

This register holds the captured MSB of the timer count value. A 16-bit read of the CNT register returns the current timer value and captures. An 8-bit LSB read of the CNT register returns the LSB and captures both the LSB and MSB. This register only has meaning when MODE = 0 and is not to be used for any purpose when MODE = 1.

Bits	Name	Description
7:0	CAPTURE_VALUE1[7:0]	Captured MSB of the timer count value.

1.3.222 TMR[0..3]_RT0

Configuration Register RT0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_RT0: 0x4F0A TMR1_RT0: 0x4F16 TMR2_RT0: 0x4F22

TMR3_RT0: 0x4F2E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00		R/W:00		R/W:00		R/W:00	
HW Access	R		R		R		R	
Retention	RET		RET		RET		RET	
Name	TIMER_RST_SRC_SEL		TIMER_EN_SRC_SEL		CAPTURE_SRC_SEL		KILL_SRC_SEL	

This register is used to configure the dsi input routing to the timer block.

Bits	Name	Description
7:6	TIMER_RST_SRC_SEL[1:0]	Selects the driver for the timer reset signal See Table 1-138.
5:4	TIMER_EN_SRC_SEL[1:0]	Selects the driver for the timer enable signal See Table 1-138.
3:2	CAPTURE_SRC_SEL[1:0]	Selects the driver for the capture signal See Table 1-138.
1:0	KILL_SRC_SEL[1:0]	Selects the driver for the kill signal See Table 1-138.

Table 1-138. Bit field encoding: src_enum

Value	Name	Description
2'b00	dsi_in0	dsi_in0 selected as source.
2'b01	dsi_in1	dsi_in1 selected as source.
2'b10	dsi_in2	dsi_in2 selected as source.
2'b11	dsi_in3	dsi_in3 selected as source.

1.3.223 TMR[0..3]_RT1

Configuration Register RT1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

TMR0_RT1: 0x4F0B TMR1_RT1: 0x4F17 TMR2_RT1: 0x4F23

TMR3_RT1: 0x4F2F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R	R	R	R	R	R
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		SYNCTC	SYNCCMP	SYNCDSI3	SYNCDSI2	SYNCDSI1	SYNCDSI0

This register is used to configure the dsi input routing to the timer block. Input signals, dsi_in0, dsi_in1, dsi_in2 and dsi_in3, are double synchronized to the system/bus clock. Output signals, tc and cmp, are registered on the application clock.

Bits	Name	Description
5	SYNCTC	Register TC/TC-IRQ with selected clk_bus_en (0 = not registered; 1 = registered)
4	SYNCCMP	Register CMP/CMPB output with selected clk_bus_en (0 = not registered; 1 = registered)
3	SYNCDSI3	Synchronize DSI input, dsi_in3, to clk_bus (0 = no synchronization; 1 = synchronization)
2	SYNCDSI2	Synchronize DSI input, dsi_in2, to clk_bus (0 = no synchronization; 1 = synchronization)
1	SYNCDSI1	Synchronize DSI input, dsi_in1, to clk_bus (0 = no synchronization; 1 = synchronization)
0	SYNCDSI0	Synchronize DSI input, dsi_in0, to clk_bus (0 = no synchronization; 1 = synchronization)

1.3.224 PRT[0..14]_PC[0..7]

Port Pin Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_PC0: 0x5000 PRT0_PC1: 0x5001 PRT0_PC2: 0x5002
PRT0_PC3: 0x5003 PRT0_PC4: 0x5004 PRT0_PC5: 0x5005
PRT0_PC6: 0x5006 PRT0_PC7: 0x5007 PRT1_PC0: 0x5008
PRT1_PC1: 0x5009 PRT1_PC2: 0x500A PRT1_PC3: 0x500B
PRT1_PC4: 0x500C PRT1_PC5: 0x500D PRT1_PC6: 0x500E
PRT1_PC7: 0x500F PRT2_PC0: 0x5010 PRT2_PC1: 0x5011
PRT2_PC2: 0x5012 PRT2_PC3: 0x5013 PRT2_PC4: 0x5014
PRT2_PC5: 0x5015 PRT2_PC6: 0x5016 PRT2_PC7: 0x5017
PRT3_PC0: 0x5018 PRT3_PC1: 0x5019 PRT3_PC2: 0x501A
PRT3_PC3: 0x501B PRT3_PC4: 0x501C PRT3_PC5: 0x501D
PRT3_PC6: 0x501E PRT3_PC7: 0x501F PRT4_PC0: 0x5020
PRT4_PC1: 0x5021 PRT4_PC2: 0x5022 PRT4_PC3: 0x5023
PRT4_PC4: 0x5024 PRT4_PC5: 0x5025 PRT4_PC6: 0x5026
PRT4_PC7: 0x5027 PRT5_PC0: 0x5028 PRT5_PC1: 0x5029
PRT5_PC2: 0x502A PRT5_PC3: 0x502B PRT5_PC4: 0x502C
PRT5_PC5: 0x502D PRT5_PC6: 0x502E PRT5_PC7: 0x502F
PRT6_PC0: 0x5030 PRT6_PC1: 0x5031 PRT6_PC2: 0x5032
PRT6_PC3: 0x5033 PRT6_PC4: 0x5034 PRT6_PC5: 0x5035
PRT6_PC6: 0x5036 PRT6_PC7: 0x5037 PRT12_PC0: 0x5060
PRT12_PC1: 0x5061 PRT12_PC2: 0x5062 PRT12_PC3: 0x5063
PRT12_PC4: 0x5064 PRT12_PC5: 0x5065 PRT12_PC6: 0x5066
PRT12_PC7: 0x5067

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	bypass	slew	bidirEn	pin_state	driveMode_2	driveMode_1	driveMode_0	data_out

The Port Pin Configuration Registers (PRTxPC0 through PRTxPC7) access several configuration or status bits of a single I/O port pin at once. Please reference the register description of the aliased register for detailed information the port configuration controlled by a given bit.

Bits **Name** **Description**

(continued)

7	bypass	The Bypass bit is the same as the corresponding bit in the port bypass register. See Table 1-140.
6	slew	The slew bit is the same as the corresponding bit in the port slew register.
5	bidirEn	The BiDir En bit is the same as the corresponding bit in the port bidirection enable register. See Table 1-139.
4	pin_state	The Pin State bit (read only) is the same as the corresponding bit in the port pin state register.
3	driveMode_2	The DM2 bit is the same as the corresponding bit in the drive mode 2 register. Please refer to the IO section on IO drive modes for detailed information on the 8 different drive mode configurations.
2	driveMode_1	The DM1 bit is the same as the corresponding bit in the drive mode 1 register. Please refer to the IO section on IO drive modes for detailed information on the 8 different drive mode configurations.
1	driveMode_0	The DM0 bit is the same as the corresponding bit in the drive mode 0 register. Please refer to the IO section on IO drive modes for detailed information on the 8 different drive mode configurations.
0	data_out	The data out bit is the same as the corresponding bit in the data register.

Table 1-139. Bit field encoding: bidir_en_enum

Value	Name	Description
1'b0	BIDIR_DIS	dynamic bidirectional mode disabled.
1'b1	BIDIR_EN	dynamic bidirectional mode enabled.

Table 1-140. Bit field encoding: bypass_en_enum

Value	Name	Description
1'b0	BYPASS_DIS	bypass function disabled.
1'b1	BYPASS_EN	bypass function enabled.

1.3.225 IO_PC_PRT15_PC[0..5]

Port Pin Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

IO_PC_PRT15_PC0: 0x5078

IO_PC_PRT15_PC1: 0x5079

IO_PC_PRT15_PC2: 0x507A

IO_PC_PRT15_PC3: 0x507B

IO_PC_PRT15_PC4: 0x507C

IO_PC_PRT15_PC5: 0x507D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	bypass	slew	bidirEn	pin_state	driveMode_2	driveMode_1	driveMode_0	data_out

The Port Pin Configuration Registers (PRTxPC0 through PRTxPC7) access several configuration or status bits of a single I/O port pin at once. Please reference the register description of the aliased register for detailed information the port configuration controlled by a given bit.

Bits	Name	Description
7	bypass	The Bypass bit is the same as the corresponding bit in the port bypass register. See Table 1-142.
6	slew	The slew bit is the same as the corresponding bit in the port slew register.
5	bidirEn	The BiDir En bit is the same as the corresponding bit in the port bidirection enable register. See Table 1-141.
4	pin_state	The Pin State bit (read only) is the same as the corresponding bit in the port pin state register.
3	driveMode_2	The DM2 bit is the same as the corresponding bit in the drive mode 2 register. Please refer to the IO section on IO drive modes for detailed information on the 8 different drive mode configurations.
2	driveMode_1	The DM1 bit is the same as the corresponding bit in the drive mode 1 register. Please refer to the IO section on IO drive modes for detailed information on the 8 different drive mode configurations.
1	driveMode_0	The DM0 bit is the same as the corresponding bit in the drive mode 0 register. Please refer to the IO section on IO drive modes for detailed information on the 8 different drive mode configurations.
0	data_out	The data out bit is the same as the corresponding bit in the data register.

Table 1-141. Bit field encoding: bidir_en_enum

Value	Name	Description
1'b0	BIDIR_DIS	dynamic bidirectional mode disabled.
1'b1	BIDIR_EN	dynamic bidirectional mode enabled.

Table 1-142. Bit field encoding: bypass_en_enum

Value	Name	Description
1'b0	BYPASS_DIS	bypass function disabled.

(continued)

Table 1-142. Bit field encoding: bypass_en_enum

1'b1	BYPASS_EN	bypass function enabled.

1.3.226 IO_PC_PRT15_7_6_PC[0..1]

Port Pin Configuration Register

Reset: Reset Signals Listed Below

Register : Address

IO_PC_PRT15_7_6_PC0: 0x507E IO_PC_PRT15_7_6_PC1: 0x507F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:00		R:U	NA:0	R/W:0	R/W:0	R/W:1
HW Access	R/W	NA		R/W	NA	R/W	R/W	R/W
Retention	RET	NA		NONRET	NA	RET	RET	RET
Name	bypass	RSVD		pin_state	RSVD	pullUp_en	driveMode_0	data_out

The Port Pin Configuration Registers (PRTxPC0 through PRTxPC7) access several configuration or status bits of a single I/O port pin at once. Please reference the register description of the aliased register for detailed information the port configuration controlled by a given bit.

Bits	Name	Description
7	bypass	The Bypass bit is the same as the corresponding bit in the port bypass register. See Table 1-143.
4	pin_state	The Pin State bit (read only) is the same as the corresponding bit in the port pin state register.
2	pullUp_en	The pull-up en bit is the same as the corresponding bit in the drive mode 1 register.
1	driveMode_0	The DM0 bit is the same as the corresponding bit in the drive mode 0 register.
0	data_out	The data out bit is the same as the corresponding bit in the data register.

Reset Table

Reset Signal	Applicable Register Bit(s)
N/A	pin_state
System reset for retention flops [reset_all_retention]	data_out, driveMode_0, pullUp_en, bypass

Table 1-143. Bit field encoding: bypass_en_enum

Value	Name	Description
1'b0	BYPASS_DIS	bypass function disabled.
1'b1	BYPASS_EN	bypass function enabled.

1.3.227 PRT[0..14]_DR_ALIAS

Aliased Port Data Output Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_DR_ALIAS: 0x5080

PRT1_DR_ALIAS: 0x5081

PRT2_DR_ALIAS: 0x5082

PRT3_DR_ALIAS: 0x5083

PRT4_DR_ALIAS: 0x5084

PRT5_DR_ALIAS: 0x5085

PRT6_DR_ALIAS: 0x5086

PRT12_DR_ALIAS: 0x508C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	DataReg_alias							

This register is used to set the output data output state for the corresponding GPIO port.

Bits	Name	Description
7:0	DataReg_alias[7:0]	The data written to this register specifies the high (Data=1) or low (Data=0) state for the GPIO pin at each bit location of the selected port. This register is only accessible if the PRTxBIT_MASK register bits are set.

1.3.228 PRT15_DR_15_ALIAS

Aliased Port Data Output Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_DR_15_ALIAS: 0x508F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:000000					
HW Access	R/W	R/W	R/W					
Retention	RET	RET	RET					
Name	DataReg_DM_alias	DataReg_DP_alias	DataReg_alias					

This register is used to set the output data output state for the corresponding GPIO port.

Bits	Name	Description
7	DataReg_DM_alias	The data written to this register specifies the high (Data=1) or low (Data=0) state for the GPIO pin at each bit location of the selected port. This register is only accessible if the PRTxBIT_MASK register bits are set.
6	DataReg_DP_alias	The data written to this register specifies the high (Data=1) or low (Data=0) state for the GPIO pin at each bit location of the selected port. This register is only accessible if the PRTxBIT_MASK register bits are set.
5:0	DataReg_alias[5:0]	The data written to this register specifies the high (Data=1) or low (Data=0) state for the GPIO pin at each bit location of the selected port. This register is only accessible if the PRTxBIT_MASK register bits are set.

1.3.229 PRT[0..14]_PS_ALIAS

Aliased Port Pin State Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_PS_ALIAS: 0x5090

PRT1_PS_ALIAS: 0x5091

PRT2_PS_ALIAS: 0x5092

PRT3_PS_ALIAS: 0x5093

PRT4_PS_ALIAS: 0x5094

PRT5_PS_ALIAS: 0x5095

PRT6_PS_ALIAS: 0x5096

PRT12_PS_ALIAS: 0x509C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R							
Retention	RET							
Name	PinState_alias							

The Port Pin State Registers PRTxPS read the logical pin state for the corresponding GPIO port. Writes to this register have no effect. If the drive mode for the pin is set to High-Z Analog, the state will read 0 independent of the voltage on the pin.

Bits	Name	Description
7:0	PinState_alias[7:0]	Reads of this register return the logical state of the corresponding I/O pin. The data read from this register specifies the logical state of the pin: 1 Reads HIGH if the pin voltage is above the input buffer threshold, logic high. 0 Reads LOW if the pin voltage is below that threshold, logic low.

1.3.230 PRT15_PS15_ALIAS

Aliased Port Pin State Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_PS15_ALIAS: 0x509F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0	R:0	R:000000					
HW Access	R/W	R/W	R/W					
Retention	RET	RET	RET					
Name	PinState_DM_alias	PinState_DP_alias	PinState_alias					

The Port Pin State Registers PRTxPS read the logical pin state for the corresponding GPIO port. Writes to this register have no effect. If the drive mode for the pin is set to High-Z Analog, the state will read 0 independent of the voltage on the pin.

Bits	Name	Description
7	PinState_DM_alias	Reads of this register return the logical state of the corresponding I/O pin. The data read from this register specifies the logical state of the pin: 1 Reads HIGH if the pin voltage is above the input buffer threshold, logic high. 0 Reads LOW if the pin voltage is below that threshold, logic low.
6	PinState_DP_alias	Reads of this register return the logical state of the corresponding I/O pin. The data read from this register specifies the logical state of the pin: 1 Reads HIGH if the pin voltage is above the input buffer threshold, logic high. 0 Reads LOW if the pin voltage is below that threshold, logic low.
5:0	PinState_alias[5:0]	Reads of this register return the logical state of the corresponding I/O pin. The data read from this register specifies the logical state of the pin: 1 Reads HIGH if the pin voltage is above the input buffer threshold, logic high. 0 Reads LOW if the pin voltage is below that threshold, logic low.

1.3.231 PRT[0..11]_DR

Port Data Output Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_DR: 0x5100 PRT1_DR: 0x5110 PRT2_DR: 0x5120

PRT3_DR: 0x5130 PRT4_DR: 0x5140 PRT5_DR: 0x5150

PRT6_DR: 0x5160

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	DataReg							

This register is used to set the output data state for the corresponding GPIO port.

Bits	Name	Description
7:0	DataReg[7:0]	The data written to this register specifies the high (Data=1) or low (Data=0) state for the GPIO pin at each bit location of the selected port.

1.3.232 PRT[0..11]_PS

Port Pin State Register1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_PS: 0x5101 PRT1_PS: 0x5111 PRT2_PS: 0x5121

PRT3_PS: 0x5131 PRT4_PS: 0x5141 PRT5_PS: 0x5151

PRT6_PS: 0x5161

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	RET							
Name	PinState							

The Port Pin State Registers PRTxPS read the logical pin state for the corresponding GPIO port. Writes to this register have no effect. If the drive mode for the pin is set to High-Z Analog, the state will read 0 independent of the voltage on the pin.

Bits	Name	Description
7:0	PinState[7:0]	Reads of this register return the logical state of the corresponding I/O pin. The data read from this register specifies the logical state of the pin: 1'b1 Reads HIGH if the pin voltage is above the input buffer threshold, logic high. 1'b0 Reads LOW if the pin voltage is below that threshold, logic low.

1.3.233 PRT[0..11]_DM[0..2]

Port Drive Mode Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_DM0: 0x5102	PRT0_DM1: 0x5103	PRT0_DM2: 0x5104
PRT1_DM0: 0x5112	PRT1_DM1: 0x5113	PRT1_DM2: 0x5114
PRT2_DM0: 0x5122	PRT2_DM1: 0x5123	PRT2_DM2: 0x5124
PRT3_DM0: 0x5132	PRT3_DM1: 0x5133	PRT3_DM2: 0x5134
PRT4_DM0: 0x5142	PRT4_DM1: 0x5143	PRT4_DM2: 0x5144
PRT5_DM0: 0x5152	PRT5_DM1: 0x5153	PRT5_DM2: 0x5154
PRT6_DM0: 0x5162	PRT6_DM1: 0x5163	PRT6_DM2: 0x5164

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	DriveMode							

These registers, PRTx.DM2, PRTx.DM1, and PRTx.DM0, combined value determines the unique drive mode of each bit in a GPIO port. Using a combination of the three drive mode registers available per port, there are eight possible drive modes for each port pin. The bit position of each port pin corresponds to the bit position of each of the three drive mode registers per port. The three bits from the drive mode registers grouped per pin and referred to as DM2, DM1, and DM0, or together as DM[2:0]. Please refer to the IO section on IO drive modes for detailed information on the eight different drive mode configurations.

Bits	Name	Description
7:0	DriveMode[7:0]	1'b0 Corresponding drive mode register bit asserted low. 1'b1 Corresponding drive mode register asserted high. DM [2:0] = {PRT *X* .DM2 [y] ,PRT *X* .DM1 [y] ,PRT *X* .DM0 [y] } DM [2:0] : Complete drive mode setting for pin [y] 3'b000 : Mode 0, input/output buffers disabled. 3'b001 : Mode 1, input only 3'b010 : Mode 2, weak pull-up, strong pull-down 3'b011 : Mode 3, strong pull-up, weak pull-down 3'b100 : Mode 4, open drain, strong pull-down 3'b101 : Mode 5, open drain, strong pull-up 3'b110 : Mode 6, stong pull-up, strong pull-down 3'b111 : Mode 7, weak pull-up, weak pull-down

1.3.234 PRT[0..11]_SLW

Port slew rate control

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_SLW: 0x5105 PRT1_SLW: 0x5115 PRT2_SLW: 0x5125

PRT3_SLW: 0x5135 PRT4_SLW: 0x5145 PRT5_SLW: 0x5155

PRT6_SLW: 0x5165

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	SlwCtl							

The output drive on any I/O pin can be set to a fast edge rate mode (Slew=0) or slow edge rate mode (Slew=1) The slew rate only applies to strong output drive modes, not to resistive drive modes. Slower edge rates normally reduce EMI issues and are recommended when speed is not critical.

Bits	Name	Description
7:0	SlwCtl[7:0]	Each bit controls the output edge rate of the corresponding port pin. 1'b0 Fast edge rate mode 1'b1 Slow edge rate mode

1.3.235 PRT[0..11]_BYP

Port Bypass enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_BYP: 0x5106 PRT1_BYP: 0x5116 PRT2_BYP: 0x5126

PRT3_BYP: 0x5136 PRT4_BYP: 0x5146 PRT5_BYP: 0x5156

PRT6_BYP: 0x5166

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	Bypass							

The Port Bypass Registers select output data from either the data output register or internal sources such as digital global bus.

Bits	Name	Description
7:0	Bypass[7:0]	1'b1 Selected digital system interconnect (DSI) drives the corresponding port pin. 1'b0 Port logic data register drives the corresponding port pin. *The drive mode settings must configure the port to enable the output buffer or the DSI dynamic drive control must configure the ouput enable for the pad.*

1.3.236 PRT[0..11]_BIE

Port Bidirectional enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_BIE: 0x5107 PRT1_BIE: 0x5117 PRT2_BIE: 0x5127

PRT3_BIE: 0x5137 PRT4_BIE: 0x5147 PRT5_BIE: 0x5157

PRT6_BIE: 0x5167

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	BidirectEn							

The Port Bidirectional Enable Registers are used to enable dynamic bidirectional mode at any pin.

Bits	Name	Description
7:0	BidirectEn[7:0]	Each bit controls the bidirectional mode of the corresponding port pin. 1'b0 Normal operation of pad. Drive mode setting configures output buffer 1'b1 Selected dynamic control DSI configures output buffer

1.3.237 PRT[0..11]_INP_DIS

Input buffer disable override

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_INP_DIS: 0x5108

PRT1_INP_DIS: 0x5118

PRT2_INP_DIS: 0x5128

PRT3_INP_DIS: 0x5138

PRT4_INP_DIS: 0x5148

PRT5_INP_DIS: 0x5158

PRT6_INP_DIS: 0x5168

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	Inp_dis							

The bits asserted force the input buffers off.

Bits	Name	Description
7:0	Inp_dis[7:0]	1'b1 Input buffers are disabled, overrides drive mode register settings. 1'b0 Input buffers are configured based on drive mode register settings.

1.3.238 PRT[0..11]_CTL

Port wide control signals

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_CTL: 0x5109 PRT1_CTL: 0x5119 PRT2_CTL: 0x5129

PRT3_CTL: 0x5139 PRT4_CTL: 0x5149 PRT5_CTL: 0x5159

PRT6_CTL: 0x5169

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:000			R/W:0
HW Access	NA				R			R
Retention	NA				RET			RET
Name	RSVD				portEmifCfg			vtrip_sel

The port wide vtrip select register is used to select the input buffer trip point select. The emif configuration bits are used to configure the port for external memory access.

Bits	Name	Description
3:1	portEmifCfg[2:0]	GPIO emif selection option configures the port for External memory interface. See Table 1-144.
0	vtrip_sel	The GPIO cells include a vtrip_sel signal to alter the input buffer voltage. See Table 1-145.

Table 1-144. Bit field encoding: emif_cfg_enum

Value	Name	Description
3'b000	NOT_EMIF	Port not selected for EMIF control
3'b001	LSB_ADDR	Port selected as Address LS byte range
3'b010	UPR_ADDR	Port selected as Address upper byte range
3'b011	MSB_ADDR	Port selected as Address MS byte range
3'b101	LSB_DATA	Port selected as Data lower byte range
3'b110	MSB_DATA	Port selected as Data upper byte range

Table 1-145. Bit field encoding: vtrip_sel_enum

Value	Name	Description
1'b0	VTRIP_CMOS	Input buffer functions as a CMOS input buffer.
1'b1	VTRIP_LVTTL	Input buffer functions as a LVTTL input buffer.

1.3.239 PRT[0..11]_PRT

Port wide configuration register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_PRT: 0x510A PRT1_PRT: 0x511A PRT2_PRT: 0x512A

PRT3_PRT: 0x513A PRT4_PRT: 0x514A PRT5_PRT: 0x515A

PRT6_PRT: 0x516A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	W:0	W:0	W:0	NA:0	W:0	W:0	W:0	NA:0
HW Access	R	R	R	NA	R	R	R	NA
Retention	RET	RET	RET	NA	RET	RET	RET	NA
Name	byPass	slew	bidirectEn	RSVD	driveMode2	driveMode1	driveMode0	RSVD

The Port Configuration Register accesses several available configuration registers on a port-wide basis with a single bit write.

Bits	Name	Description
7	byPass	The Bypass bit sets all the bits for the port bypass register. See Table 1-147.
6	slew	The slew bit is the same as the corresponding bit in the port slew register.
5	bidirectEn	The BiDir En bit sets all bits for the port bidirection enable register. See Table 1-146.
3	driveMode2	A write to this bit sets all bits for the corresponding drive mode register of the entire port.
2	driveMode1	A write to this bit sets all bits for the corresponding drive mode register of the entire port.
1	driveMode0	A write to this bit sets all bits for the corresponding drive mode register of the entire port.

Table 1-146. Bit field encoding: bidir_en_enum

Value	Name	Description
1'b0	BIDIR_DIS	dynamic bidirectional mode disabled.
1'b1	BIDIR_EN	dynamic bidirectional mode enabled.

Table 1-147. Bit field encoding: bypass_en_enum

Value	Name	Description
1'b0	BYPASS_DIS	bypass function disabled.
1'b1	BYPASS_EN	bypass function enabled.

1.3.240 PRT[0..11]_BIT_MASK

Bit-mask for Aliased Register access

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_BIT_MASK: 0x510B

PRT1_BIT_MASK: 0x511B

PRT2_BIT_MASK: 0x512B

PRT3_BIT_MASK: 0x513B

PRT4_BIT_MASK: 0x514B

PRT5_BIT_MASK: 0x515B

PRT6_BIT_MASK: 0x516B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	bit_mask							

The bits asserted in the bit-mask register allow direct access to the data register or pin state register via the aliased registers.

Bits	Name	Description
7:0	bit_mask[7:0]	1'b1 Allow access to data register and pin state registers via aliased register address space. 1'b0 Block access to data register and pin state registers via aliased register address space.

1.3.241 PRT[0..11]_AMUX

Port Analog global mux bus enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_AMUX: 0x510C PRT1_AMUX: 0x511C PRT2_AMUX: 0x512C

PRT3_AMUX: 0x513C PRT4_AMUX: 0x514C PRT5_AMUX: 0x515C

PRT6_AMUX: 0x516C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	Amux							

Analog global mux switch.

Bits	Name	Description
7:0	Amux[7:0]	Connects analog mux bus to the pad when asserted.

1.3.242 PRT[0..11]_AG

Port Analog global enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_AG: 0x510D PRT1_AG: 0x511D PRT2_AG: 0x512D

PRT3_AG: 0x513D PRT4_AG: 0x514D PRT5_AG: 0x515D

PRT6_AG: 0x516D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	AnalogGlobal							

Analog global switch.

Bits	Name	Description
7:0	AnalogGlobal[7:0]	Connects analog global to the pad when asserted.

1.3.243 PRT[0..11]_LCD_COM_SEG

Port LCD Com seg bits.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_LCD_COM_SEG: 0x510E

PRT1_LCD_COM_SEG: 0x511E

PRT2_LCD_COM_SEG: 0x512E

PRT3_LCD_COM_SEG: 0x513E

PRT4_LCD_COM_SEG: 0x514E

PRT5_LCD_COM_SEG: 0x515E

PRT6_LCD_COM_SEG: 0x516E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	com_seg							

Selects whether a pin is set as a common or segment drive pin.

Bits	Name	Description
7:0	com_seg[7:0]	Specify whether the pin will drive common or segment mode when LCD is enabled. 1'b0 Segment 1'b1 Common

1.3.244 PRT[0..11]_LCD_EN

Port LCD enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_LCD_EN: 0x510F

PRT1_LCD_EN: 0x511F

PRT2_LCD_EN: 0x512F

PRT3_LCD_EN: 0x513F

PRT4_LCD_EN: 0x514F

PRT5_LCD_EN: 0x515F

PRT6_LCD_EN: 0x516F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	Lcd_en							

Enables a given pin for LCD drive mode

Bits	Name	Description
7:0	Lcd_en[7:0]	Enable the pin for LCD mode. 1'b0 Disabled 1'b1 Enabled

1.3.245 PRT12_DR

Port Data Output Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_DR: 0x51C0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	DataReg							

This register is used to set the output data state for the corresponding GPIO port.

Bits	Name	Description
7:0	DataReg[7:0]	The data written to this register specifies the high (Data=1) or low (Data=0) state for the GPIO pin at each bit location of the selected port.

1.3.246 PRT12_PS

Port Pin State Register1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_PS: 0x51C1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	RET							
Name	PinState							

The Port Pin State Registers PRTxPS read the logical pin state for the corresponding GPIO port. Writes to this register have no effect. If the drive mode for the pin is set to High-Z Analog, the state will read 0 independent of the voltage on the pin.

Bits	Name	Description
7:0	PinState[7:0]	Reads of this register return the logical state of the corresponding I/O pin. The data read from this register specifies the logical state of the pin: 1'b1 Reads HIGH if the pin voltage is above the input buffer threshold, logic high. 1'b0 Reads LOW if the pin voltage is below that threshold, logic low.

1.3.247 PRT12_DM[0..2]

Port Drive Mode Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_DM0: 0x51C2 PRT12_DM1: 0x51C3 PRT12_DM2: 0x51C4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	DriveMode							

These registers, PRTx.DM2, PRTx.DM1, and PRTx.DM0, combined value determines the unique drive mode of each bit in a GPIO port. Using a combination of the three drive mode registers available per port, there are eight possible drive modes for each port pin. The bit position of each port pin corresponds to the bit position of each of the three drive mode registers per port. The three bits from the drive mode registers grouped per pin and referred to as DM2, DM1, and DM0, or together as DM[2:0]. Please refer to the IO section on IO drive modes for detailed information on the eight different drive mode configurations.

Bits	Name	Description
7:0	DriveMode[7:0]	1'b0 Corresponding drive mode register bit asserted low. 1'b1 Corresponding drive mode register asserted high.

DM [2:0] = {PRT *X* .DM2 [y] ,PRT *X* .DM1 [y] ,PRT *X* .DM0 [y] }

DM [2:0] : Complete drive mode setting for pin [y] 3'b000 : Mode 0, input/output buffers disabled. 3'b001 : Mode 1, input only 3'b010 : Mode 2, weak pull-up, strong pull-down 3'b011 : Mode 3, strong pull-up, weak pull-down 3'b100 : Mode 4, open drain, strong pull-down 3'b101 : Mode 5, open drain, strong pull-up 3'b110 : Mode 6, stong pull-up, strong pull-down 3'b111 : Mode 7, weak pull-up, weak pull-down

1.3.248 PRT12_SLW

Port slew rate control

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_SLW: 0x51C5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	SlwCtl							

The output drive on any I/O pin can be set to a fast edge rate mode (Slew=0) or slow edge rate mode (Slew=1) The slew rate only applies to strong output drive modes, not to resistive drive modes. Slower edge rates normally reduce EMI issues and are recommended when speed is not critical.

Bits	Name	Description
7:0	SlwCtl[7:0]	Each bit controls the output edge rate of the corresponding port pin. 1'b0 Fast edge rate mode 1'b1 Slow edge rate mode

1.3.249 PRT12_BYP

Port Bypass enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_BYP: 0x51C6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	Bypass							

The Port Bypass Registers select output data from either the data output register or internal sources such as digital global bus.

Bits	Name	Description
7:0	Bypass[7:0]	1'b1 Selected digital system interconnect (DSI) drives the corresponding port pin. 1'b0 Port logic data register drives the corresponding port pin. *The drive mode settings must configure the port to enable the output buffer or the DSI dynamic drive control must configure the ouput enable for the pad.*

1.3.250 PRT12_BIE

Port Bidirectional enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_BIE: 0x51C7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	BidirectEn							

The Port Bidirectional Enable Registers are used to enable dynamic bidirectional mode at any pin.

Bits	Name	Description
7:0	BidirectEn[7:0]	Each bit controls the bidirectional mode of the corresponding port pin. 1'b0 Normal operation of pad. Drive mode setting configures output buffer 1'b1 Selected dynamic control DSI configures output buffer

1.3.251 PRT12_INP_DIS

Input buffer disable override

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_INP_DIS: 0x51C8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	Inp_dis							

The bits asserted force the input buffers off.

Bits	Name	Description
7:0	Inp_dis[7:0]	1'b1 Input buffers are disabled, overrides drive mode register settings. 1'b0 Input buffers are configured based on drive mode register settings.

1.3.252 PRT12_SIO_HYST_EN

SIO Hysteresis enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_SIO_HYST_EN: 0x51C9

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	sio_diff_hyst_en							

The SIO hysteresis enable for the SIO differential input buffer.

Bits	Name	Description
7:0	sio_diff_hyst_en[7:0]	(no description)

1.3.253 PRT12_PRT

Port wide configuration register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_PRT: 0x51CA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	W:0	W:0	W:0	NA:0	W:0	W:0	W:0	NA:0
HW Access	R	R	R	NA	R	R	R	NA
Retention	RET	RET	RET	NA	RET	RET	RET	NA
Name	byPass	slew	bidirectEn	RSVD	driveMode2	driveMode1	driveMode0	RSVD

The Port Configuration Register accesses several available configuration registers on a port-wide basis with a single bit write.

Bits	Name	Description
7	byPass	The Bypass bit sets all the bits for the port bypass register. See Table 1-149.
6	slew	The slew bit is the same as the corresponding bit in the port slew register.
5	bidirectEn	The BiDir En bit sets all bits for the port bidirection enable register. See Table 1-148.
3	driveMode2	A write to this bit sets all bits for the corresponding drive mode register of the entire port.
2	driveMode1	A write to this bit sets all bits for the corresponding drive mode register of the entire port.
1	driveMode0	A write to this bit sets all bits for the corresponding drive mode register of the entire port.

Table 1-148. Bit field encoding: bidir_en_enum

Value	Name	Description
1'b0	BIDIR_DIS	dynamic bidirectional mode disabled.
1'b1	BIDIR_EN	dynamic bidirectional mode enabled.

Table 1-149. Bit field encoding: bypass_en_enum

Value	Name	Description
1'b0	BYPASS_DIS	bypass function disabled.
1'b1	BYPASS_EN	bypass function enabled.

1.3.254 PRT12_BIT_MASK

Bit-mask for Aliased Register access

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_BIT_MASK: 0x51CB

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	bit_mask							

The bits asserted in the bit-mask register allow direct access to the data register or pin state register via the aliased registers.

Bits	Name	Description
7:0	bit_mask[7:0]	1'b1 Allow access to data register and pin state registers via aliased register address space. 1'b0 Block access to data register and pin state registers via aliased register address space.

1.3.255 PRT12_SIO_REG_HIFREQ

Regulated pull-up driver DC current setting

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_SIO_REG_HIFREQ: 0x51CC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0
HW Access	R	NA	R	NA	R	NA	R	NA
Retention	RET	NA	RET	NA	RET	NA	RET	NA
Name	sio_reg_hifreq_7_6	RSVD	sio_reg_hifreq_5_4	RSVD	sio_reg_hifreq_3_2	RSVD	sio_reg_hifreq_1_0	RSVD

Sets each SIO pair's pull-up driver DC current. For output frequency <=10MHz, setting this low will lower the DC current on the SIO pin pair. For output frequency >10MHz <= 33MHz, set the bit high.

Bits	Name	Description
7	sio_reg_hifreq_7_6	pull-up driver DC current
5	sio_reg_hifreq_5_4	pull-up driver DC current
3	sio_reg_hifreq_3_2	pull-up driver DC current
1	sio_reg_hifreq_1_0	pull-up driver DC current

1.3.256 PRT12_AG

Port Analog global enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_AG: 0x51CD

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00		R/W:00		R/W:00		R/W:00	
HW Access	R		R		R		R	
Retention	RET		RET		RET		RET	
Name	AnalogGlobal_7_6		AnalogGlobal_5_4		AnalogGlobal_3_2		AnalogGlobal_1_0	

Analog global switch.

Bits	Name	Description
7:6	AnalogGlobal_7_6[1:0]	Connects analog global when asserted. See Table 1-150.
5:4	AnalogGlobal_5_4[1:0]	Connects analog global when asserted. See Table 1-150.
3:2	AnalogGlobal_3_2[1:0]	Connects analog global when asserted. See Table 1-150.
1:0	AnalogGlobal_1_0[1:0]	Connects analog global when asserted. See Table 1-150.

Table 1-150. Bit field encoding: pr12_ag_enum

Value	Name	Description
2'b00	NO_AG	No AG selected.
2'b01	AG0_SEL	low bit AG connection selected.
2'b10	AG1_SEL	high bit AG connection selected.
2'b11	VCCD_SEL	VCCD connection selected.

1.3.257 PRT12_SIO_CFG

SIO Input Output Configuration

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_SIO_CFG: 0x51CE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	ibuf_sel_7_6	vreg_en_7_6	ibuf_sel_5_4	vreg_en_5_4	ibuf_sel_3_2	vreg_en_3_2	ibuf_sel_1_0	vreg_en_1_0

Sets each SIO pair's input output Configuration. vreg_en=0 & ibuf_sel=0 sets the mode to Single Ended Input Buffer, Non-regulated Output Buffer. vreg_en=0 & ibuf_sel=1 sets the mode to Differential Input Buffer, Non-regulated Output Buffer. vreg_en=1 & ibuf_sel=0 sets the mode to Single Ended Input Buffer, Regulated Output Buffer. vreg_en=1 & ibuf_sel=1 sets the mode to Differential Input Buffer, Regulated Output Buffer.

Bits	Name	Description
7	ibuf_sel_7_6	sets the ibuf_sel for the corresponding SIO pair
6	vreg_en_7_6	sets the vreg_en for the corresponding SIO pair
5	ibuf_sel_5_4	sets the ibuf_sel for the corresponding SIO pair
4	vreg_en_5_4	sets the vreg_en for the corresponding SIO pair
3	ibuf_sel_3_2	sets the ibuf_sel for the corresponding SIO pair
2	vreg_en_3_2	sets the vreg_en for the corresponding SIO pair
1	ibuf_sel_1_0	sets the ibuf_sel for the corresponding SIO pair
0	vreg_en_1_0	sets the vreg_en for the corresponding SIO pair

1.3.258 PRT12_SIO_DIFF

Differential Input Buffer reference voltage selection

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_SIO_DIFF: 0x51CF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	vref_sel_7_6	vtrip_sel_7_6	vref_sel_5_4	vtrip_sel_5_4	vref_sel_3_2	vtrip_sel_3_2	vref_sel_1_0	vtrip_sel_1_0

Sets each SIO pair's input buffer switching threshold. If ibuf_sel=0, vref_sel has no impact as the single-ended receiver is used. In this case: vtrip_sel=0 sets the single-ended input buffer threshold to CMOS levels. vtrip_sel=1 sets the single-ended input buffer threshold to LVTTL levels. If ibuf_sel=1, the differential receiver is used and vref_sel does have functional impact. In this case: vref_sel=0 & vtrip_sel=0 sets the differential input buffer threshold to 0.5*vio. vref_sel=0 & vtrip_sel=1 sets the differential input buffer threshold to 0.4*vio. vref_sel=1 & vtrip_sel=0 sets the differential input buffer threshold to 0.5*vohref. vref_sel=1 & vtrip_sel=1 sets the differential input buffer threshold to vohref.

Bits	Name	Description
7	vref_sel_7_6	sets the vref_sel for the corresponding SIO pair
6	vtrip_sel_7_6	sets the vtrip_sel for the corresponding SIO pair
5	vref_sel_5_4	sets the vref_sel for the corresponding SIO pair
4	vtrip_sel_5_4	sets the vtrip_sel for the corresponding SIO pair
3	vref_sel_3_2	sets the vref_sel for the corresponding SIO pair
2	vtrip_sel_3_2	sets the vtrip_sel for the corresponding SIO pair
1	vref_sel_1_0	sets the vref_sel for the corresponding SIO pair
0	vtrip_sel_1_0	sets the vtrip_sel for the corresponding SIO pair

1.3.259 PRT15_DR

Port Data Output Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_DR: 0x51F0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:1	R/W:1	R/W:000000					
HW Access	R	R	R					
Retention	RET	RET	RET					
Name	DataReg_DM	DataReg_DP	DataReg					

This register is used to set the output data state for the corresponding GPIO port.

Bits	Name	Description
7	DataReg_DM	The data written to this register specifies the high (Data=1) or low (Data=0) state for the corresponding USB pin when GPIO mode is enabled by setting the USB.USBIO_CR1 iomode bit.
6	DataReg_DP	The data written to this register specifies the high (Data=1) or low (Data=0) state for the corresponding USB pin when GPIO mode is enabled by setting the USB.USBIO_CR1 iomode bit.
5:0	DataReg[5:0]	The data written to this register specifies the high (Data=1) or low (Data=0) state for the GPIO pin at each bit location of the selected port.

1.3.260 PRT15_PS

Port Pin State Register1

Reset: Reset Signals Listed Below

Register : Address

PRT15_PS: 0x51F1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:U	R:U	R:000000					
HW Access	R/W	R/W	R/W					
Retention	NONRET	NONRET	RET					
Name	PinState_DM	PinState_DP	PinState					

The Port Pin State Registers PRTxPS read the logical pin state for the corresponding GPIO port. Writes to this register have no effect. If the drive mode for the pin is set to High-Z Analog, the state will read 0 independent of the voltage on the pin.

Bits	Name	Description
7	PinState_DM	Reads of this register return the logical state of the corresponding I/O pin. The data read from this register specifies the logical state of the pin: 1'b1 Reads HIGH if the pin voltage is above the input buffer threshold, logic high. 1'b0 Reads LOW if the pin voltage is below that threshold, logic low.
6	PinState_DP	Reads of this register return the logical state of the corresponding I/O pin. The data read from this register specifies the logical state of the pin: 1'b1 Reads HIGH if the pin voltage is above the input buffer threshold, logic high. 1'b0 Reads LOW if the pin voltage is below that threshold, logic low.
5:0	PinState[5:0]	Reads of this register return the logical state of the corresponding I/O pin. The data read from this register specifies the logical state of the pin: 1'b1 Reads HIGH if the pin voltage is above the input buffer threshold, logic high. 1'b0 Reads LOW if the pin voltage is below that threshold, logic low.

Reset Table

Reset Signal	Applicable Register Bit(s)
N/A	PinState_DP, PinState_DM
System reset for retention flops [reset_all_retention]	PinState[5:0]

1.3.261 PRT15_DM0

Port Drive Mode Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_DM0: 0x51F2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:000000					
HW Access	R	R	R					
Retention	RET	RET	RET					
Name	DriveMode_DM	DriveMode_DP	DriveMode					

These registers, PRTx.DM2, PRTx.DM1, and PRTx.DM0, combined value determines the unique drive mode of each bit in a GPIO port. Using a combination of the three drive mode registers available per port, there are eight possible drive modes for each port pin. The bit position of each port pin corresponds to the bit position of each of the three drive mode registers per port. The three bits from the drive mode registers grouped per pin and referred to as DM2, DM1, and DM0, or together as DM[2:0]. Please refer to the IO section on IO drive modes for detailed information on the eight different drive mode configurations. The PRTx.DM0[7:6] select the drive mode setting for the limited GPIO functionality of the USBIO.

Bits	Name	Description
7	DriveMode_DM	If iomode is set to GPIO mode in USB_USBIO_CR1, driveMode_DM configures the D- pin drive mode. If IOMode is set to USB mode, driveMode_DM is ignored by the D-. 1'b0: open drain mode. If dmi is high, DM is open drain, if dmi is low, DM forced low. 1'b1: drive out. The pin follows the Datareg_DM value
6	DriveMode_DP	Pull-up enable control for USBIO D+ pin. If iomode is set to GPIO mode in USB_USBIO_CR1, driveMode_DP configures the D+ pin drive mode. If IOMode is set to USB mode, driveMode_DP is ignored by the D+. 1'b0: open drain mode. If dpi is high, DP is open drain, if dpi is low, DP forced low. 1'b1: drive out. The pin follows the Datareg_DP value
5:0	DriveMode[5:0]	1'b0 Corresponding drive mode register bit asserted low. 1'b1 Corresponding drive mode register asserted high. DM [2:0] = {PRT *X* .DM2 [y] ,PRT *X* .DM1 [y] ,PRT *X* .DM0 [y] } DM [2:0] : Complete drive mode setting for pin [y] 3'b000 : Mode 0, input/output buffers disabled. 3'b001 : Mode 1, input only 3'b010 : Mode 2, weak pull-up, strong pull-down 3'b011 : Mode 3, strong pull-up, weak pull-down 3'b100 : Mode 4, open drain, strong pull-down 3'b101 : Mode 5, open drain, strong pull-up 3'b110 : Mode 6, stong pull-up, strong pull-down 3'b111 : Mode 7, weak pull-up, weak pull-down

1.3.262 PRT15_DM1

Port Drive Mode Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_DM1: 0x51F3

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:000000					
HW Access	R	R	R					
Retention	RET	RET	RET					
Name	PullUp_en_DM	PullUp_en_DP	DriveMode					

These registers, PRTx.DM2, PRTx.DM1, and PRTx.DM0, combined value determines the unique drive mode of each bit in a GPIO port. Using a combination of the three drive mode registers available per port, there are eight possible drive modes for each port pin. The bit position of each port pin corresponds to the bit position of each of the three drive mode registers per port. The three bits from the drive mode registers grouped per pin and referred to as DM2, DM1, and DM0, or together as DM[2:0]. Please refer to the IO section on IO drive modes for detailed information on the eight different drive mode configurations. The PRTx.DM1[7:6] enable the 5 kOhm pull-ups on the limited GPIO functionality USBIO pins.

Bits	Name	Description
7	PullUp_en_DM	Pull-up enable control for USBIO D- pin. If iomode is set to GPIO mode in USB_USBIO_CR1, pullUp_en_DM configures the D- 5kOhm pull-up resistor. If IOMode is set to USB mode, pullUp_en_DM is ignored by the D-. 1'b1: 5kOhm pull-up enabled on D- 1'b0: no pull-up
6	PullUp_en_DP	If iomode is set to GPIO mode in USB_USBIO_CR1, pullUp_en_DP configures the D+ 5kOhm pull-up resistor. If IOMode is set to USB mode, pullUp_en_DP is ignored by the D+. 1'b1: 5kOhm pull-up enabled on D+ 1'b0: no pull-up
5:0	DriveMode[5:0]	1'b0 Corresponding drive mode register bit asserted low. 1'b1 Corresponding drive mode register asserted high. DM [2:0] = {PRT *X* .DM2 [y] ,PRT *X* .DM1 [y] ,PRT *X* .DM0 [y] } DM [2:0] : Complete drive mode setting for pin [y] 3'b000 : Mode 0, input/output buffers disabled. 3'b001 : Mode 1, input only 3'b010 : Mode 2, weak pull-up, strong pull-down 3'b011 : Mode 3, strong pull-up, weak pull-down 3'b100 : Mode 4, open drain, strong pull-down 3'b101 : Mode 5, open drain, strong pull-up 3'b110 : Mode 6, stong pull-up, strong pull-down 3'b111 : Mode 7, weak pull-up, weak pull-down

1.3.263 PRT15_DM2

Port Drive Mode Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_DM2: 0x51F4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:000000					
HW Access	NA		R					
Retention	NA		RET					
Name	RSVD		DriveMode					

These registers, PRTx.DM2, PRTx.DM1, and PRTx.DM0, combined value determines the unique drive mode of each bit in a GPIO port. Using a combination of the three drive mode registers available per port, there are eight possible drive modes for each port pin. The bit position of each port pin corresponds to the bit position of each of the three drive mode registers per port. The three bits from the drive mode registers grouped per pin and referred to as DM2, DM1, and DM0, or together as DM[2:0]. Please refer to the IO section on IO drive modes for detailed information on the eight different drive mode configurations.

Bits	Name	Description
5:0	DriveMode[5:0]	1'b0 Corresponding drive mode register bit asserted low. 1'b1 Corresponding drive mode register asserted high. DM [2:0] = {PRT *X* .DM2 [y] ,PRT *X* .DM1 [y] ,PRT *X* .DM0 [y] } DM [2:0] : Complete drive mode setting for pin [y] 3'b000 : Mode 0, input/output buffers disabled. 3'b001 : Mode 1, input only 3'b010 : Mode 2, weak pull-up, strong pull-down 3'b011 : Mode 3, strong pull-up, weak pull-down 3'b100 : Mode 4, open drain, strong pull-down 3'b101 : Mode 5, open drain, strong pull-up 3'b110 : Mode 6, stong pull-up, strong pull-down 3'b111 : Mode 7, weak pull-up, weak pull-down

1.3.264 PRT15_SLW

Port slew rate control

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_SLW: 0x51F5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:000000					
HW Access	NA		R					
Retention	NA		RET					
Name	RSVD		SlwCtl					

The output drive on any I/O pin can be set to a fast edge rate mode (Slew=0) or slow edge rate mode (Slew=1) The slew rate only applies to strong output drive modes, not to resistive drive modes. Slower edge rates normally reduce EMI issues and are recommended when speed is not critical.

Bits	Name	Description
5:0	SlwCtl[5:0]	Each bit controls the output edge rate of the corresponding port pin. 1'b0 Fast edge rate mode 1'b1 Slow edge rate mode

1.3.265 PRT15_BYP

Port Bypass enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_BYP: 0x51F6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00		R/W:000000					
HW Access	R		R					
Retention	RET		RET					
Name	Bypass_usb		Bypass					

The Port Bypass Registers select output data from either the data output register or internal sources such as digital global bus. Shared USB pins must be set to GPIO mode.

Bits	Name	Description
7:6	Bypass_usb[1:0]	1'b1 Selected digital system interconnect (DSI) drives the corresponding port pin. 1'b0 DMI/DPI outputs from USB drives the corresponding port pin configured in IO mode. *GPIO mode must be enabled in order to bypass the shared function USB/IO pins.*
5:0	Bypass[5:0]	1'b1 Selected digital system interconnect (DSI) drives the corresponding port pin. 1'b0 Port logic data register drives the corresponding port pin. *The drive mode settings must configure the port to enable the output buffer or the DSI dynamic drive control must configure the ouput enable for the pad.*

1.3.266 PRT15_BIE

Port Bidirection enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_BIE: 0x51F7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:000000					
HW Access	NA		R					
Retention	NA		RET					
Name	RSVD		BidirectEn					

The Port Bidirectional Enable Registers are used to enable dynamic bidirectional mode at any pin.

Bits	Name	Description
5:0	BidirectEn[5:0]	Each bit controls the bidirectional mode of the corresponding port pin. 1'b0 Normal operation of pad. Drive mode setting configures output buffer 1'b1 Selected dynamic control DSI configures output buffer

1.3.267 PRT15_INP_DIS

Input buffer disable override

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_INP_DIS: 0x51F8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:1	R/W:1	R/W:000000					
HW Access	R	R	R					
Retention	RET	RET	RET					
Name	seinput_dis_dm	seinput_dis_dp	Inp_dis					

The bits asserted force the input buffers off.

Bits	Name	Description
7	seinput_dis_dm	1'b1 Single ended input disabled, IO mode disabled for USBIO. 1'b0 Single ended input enabled.
6	seinput_dis_dp	1'b1 Single ended input disabled, IO mode disabled for USBIO. 1'b0 Single ended input enabled.
5:0	Inp_dis[5:0]	1'b1 Input buffers are disabled, overrides drive mode register settings. 1'b0 Input buffers are configured based on drive mode register settings.

1.3.268 PRT15_CTL

Port wide control signals

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_CTL: 0x51F9

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Retention	NA							RET
Name	RSVD							vtrip_sel

The port wide vtrip select register is used to select the input buffer trip point select

Bits	Name	Description
0	vtrip_sel	The GPIO cells include a vtrip_sel signal to alter the input buffer voltage. See Table 1-151.

Table 1-151. Bit field encoding: vtrip_sel_enum

Value	Name	Description
1'b0	VTRIP_CMOS	Input buffer functions as a CMOS input buffer.
1'b1	VTRIP_LVTTL	Input buffer functions as a LVTTL input buffer.

1.3.269 PRT15_PRT

Port wide configuration register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_PRT: 0x51FA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	W:0	W:0	W:0	NA:0	W:0	W:0	W:0	NA:0
HW Access	R	R	R	NA	R	R	R	NA
Retention	RET	RET	RET	NA	RET	RET	RET	NA
Name	byPass	slew	bidirectEn	RSVD	driveMode2	driveMode1	driveMode0	RSVD

The Port Configuration Register accesses several available configuration registers on a port-wide basis with a single bit write. The write will have no effect on reserved register bits. Please reference the aplicable registers definitions.

Bits	Name	Description
7	byPass	The Bypass bit sets all the bits for the port bypass register. See Table 1-153.
6	slew	The slew bit is the same as the corresponding bit in the port slew register.
5	bidirectEn	The BiDir En bit sets all bits for the port bidirection enable register. See Table 1-152.
3	driveMode2	A write to this bit sets all bits for the corresponding drive mode register of the entire port.
2	driveMode1	A write to this bit sets all bits for the corresponding drive mode register of the entire port.
1	driveMode0	A write to this bit sets all bits for the corresponding drive mode register of the entire port.

Table 1-152. Bit field encoding: bidir_en_enum

Value	Name	Description
1'b0	BIDIR_DIS	dynamic bidirectional mode disabled.
1'b1	BIDIR_EN	dynamic bidirectional mode enabled.

Table 1-153. Bit field encoding: bypass_en_enum

Value	Name	Description
1'b0	BYPASS_DIS	bypass function disabled.
1'b1	BYPASS_EN	bypass function enabled.

1.3.270 PRT15_BIT_MASK

Bit-mask for Aliased Register access

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_BIT_MASK: 0x51FB

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:000000					
HW Access	R	R	R					
Retention	RET	RET	RET					
Name	bit_mask_dm	bit_mask_dp	bit_mask					

The bits asserted in the bit-mask register allow direct access to the data register or pin state register via the aliased registers.

Bits	Name	Description
7	bit_mask_dm	Aliased register access of port 15[7:6] is for USB pins when configured to GPIO mode. 1'b1 Allow access to data register and pin state registers via aliased register address space. 1'b0 Block access to data register and pin state registers via aliased register address space.
6	bit_mask_dp	Aliased register access of port 15[7:6] is for USB pins when configured to GPIO mode. 1'b1 Allow access to data register and pin state registers via aliased register address space. 1'b0 Block access to data register and pin state registers via aliased register address space.
5:0	bit_mask[5:0]	1'b1 Allow access to data register and pin state registers via aliased register address space. 1'b0 Block access to data register and pin state registers via aliased register address space.

1.3.271 PRT15_AMUX

Port Analog global mux bus enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_AMUX: 0x51FC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:000000					
HW Access	NA		R					
Retention	NA		RET					
Name	RSVD		Amux					

Analog global mux switch.

Bits	Name	Description
5:0	Amux[5:0]	Connects analog mux bus to the pad when asserted.

1.3.272 PRT15_AG

Port Analog global enable

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_AG: 0x51FD

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:000000					
HW Access	NA		R					
Retention	NA		RET					
Name	RSVD		AnalogGlobal					

Analog global switch.

Bits	Name	Description
5:0	AnalogGlobal[5:0]	Connects analog global to the pad when asserted.

1.3.273 PRT15_LCD_COM_SEG

Port LCD Com seg bits.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_LCD_COM_SEG: 0x51FE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:000000					
HW Access	NA		R					
Retention	NA		RET					
Name	RSVD		com_seg					

Selects whether a pin is set as a common or segment drive pin.

Bits	Name	Description
5:0	com_seg[5:0]	Specify whether the pin will drive common or segment mode when LCD is enabled. 1'b0 Segment 1'b1 Common

1.3.274 PRT15_LCD_EN

Port LCD enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_LCD_EN: 0x51FF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:000000					
HW Access	NA		R					
Retention	NA		RET					
Name	RSVD		Lcd_en					

Enables a given pin for LCD drive mode

Bits	Name	Description
5:0	Lcd_en[5:0]	Enable the pin for LCD mode. 1'b0 Disabled 1'b1 Enabled

1.3.275 PRT0_OUT_SEL0

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_OUT_SEL0: 0x5200

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.276 PRT0_OUT_SEL1

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_OUT_SEL1: 0x5201

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.277 PRT0_OE_SEL0

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_OE_SEL0: 0x5202

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOEsel							

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
7:0	portOEsel[7:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.278 PRT0_OE_SEL1

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_OE_SEL1: 0x5203

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOEsel							

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
7:0	portOEsel[7:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.279 PRT0_DBL_SYNC_IN

DSI double sync enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_DBL_SYNC_IN: 0x5204

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	dbl_sync_in							

The port double sync register selects to synchronize the data in from the port before driving the digital system interconnect (DSI) signals to the UDB.

Bits	Name	Description
7:0	dbl_sync_in[7:0]	When asserted selects to synchronize the data in from the corresponding pad.

1.3.280 PRT0_SYNC_OUT

DSI sync out enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_SYNC_OUT: 0x5205

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	sync_out							

The port sync register selects to synchronize the data driving the pad using the existing port data register.

Bits	Name	Description
7:0	sync_out[7:0]	When asserted selects to synchronize the data from the DSI driving the corresponding pad.

1.3.281 PRT0_CAPS_SEL

Global DSI select register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT0_CAPS_SEL: 0x5206

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	caps_sel							

The global DSI select register. When enabled, the global DSI dynamic control is selected to drive the dig_glbl_ctl.

Bits	Name	Description
7:0	caps_sel[7:0]	When asserted selects the global DSI to drive dig_glbl_ctl on the pad.

1.3.282 PRT1_OUT_SEL0

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT1_OUT_SEL0: 0x5208

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.283 PRT1_OUT_SEL1

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT1_OUT_SEL1: 0x5209

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.284 PRT1_OE_SEL0

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT1_OE_SEL0: 0x520A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOEsel							

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
7:0	portOEsel[7:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.285 PRT1_OE_SEL1

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT1_OE_SEL1: 0x520B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOEsel							

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
7:0	portOEsel[7:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.286 PRT1_DBL_SYNC_IN

DSI double sync enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT1_DBL_SYNC_IN: 0x520C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	dbl_sync_in							

The port double sync register selects to synchronize the data in from the port before driving the digital system interconnect (DSI) signals to the UDB.

Bits	Name	Description
7:0	dbl_sync_in[7:0]	When asserted selects to synchronize the data in from the corresponding pad.

1.3.287 PRT1_SYNC_OUT

DSI sync out enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT1_SYNC_OUT: 0x520D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	sync_out							

The port sync register selects to synchronize the data driving the pad using the existing port data register.

Bits	Name	Description
7:0	sync_out[7:0]	When asserted selects to synchronize the data from the DSI driving the corresponding pad.

1.3.288 PRT1_CAPS_SEL

Global DSI select register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT1_CAPS_SEL: 0x520E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	caps_sel							

The global DSI select register. When enabled, the global DSI dynamic control is selected to drive the dig_glbl_ctl.

Bits	Name	Description
7:0	caps_sel[7:0]	When asserted selects the global DSI to drive dig_glbl_ctl on the pad.

1.3.289 PRT2_OUT_SEL0

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT2_OUT_SEL0: 0x5210

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.290 PRT2_OUT_SEL1

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT2_OUT_SEL1: 0x5211

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.291 PRT2_OE_SEL0

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT2_OE_SEL0: 0x5212

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOEsel							

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
7:0	portOEsel[7:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.292 PRT2_OE_SEL1

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT2_OE_SEL1: 0x5213

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOEsel							

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
7:0	portOEsel[7:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.293 PRT2_DBL_SYNC_IN

DSI double sync enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT2_DBL_SYNC_IN: 0x5214

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	dbl_sync_in							

The port double sync register selects to synchronize the data in from the port before driving the digital system interconnect (DSI) signals to the UDB.

Bits	Name	Description
7:0	dbl_sync_in[7:0]	When asserted selects to synchronize the data in from the corresponding pad.

1.3.294 PRT2_SYNC_OUT

DSI sync out enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT2_SYNC_OUT: 0x5215

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	sync_out							

The port sync register selects to synchronize the data driving the pad using the existing port data register.

Bits	Name	Description
7:0	sync_out[7:0]	When asserted selects to synchronize the data from the DSI driving the corresponding pad.

1.3.295 PRT2_CAPS_SEL

Global DSI select register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT2_CAPS_SEL: 0x5216

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	caps_sel							

The global DSI select register. When enabled, the global DSI dynamic control is selected to drive the dig_glbl_ctl.

Bits	Name	Description
7:0	caps_sel[7:0]	When asserted selects the global DSI to drive dig_glbl_ctl on the pad.

1.3.296 PRT3_OUT_SEL0

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT3_OUT_SEL0: 0x5218

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.297 PRT3_OUT_SEL1

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT3_OUT_SEL1: 0x5219

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.298 PRT3_OE_SEL0

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT3_OE_SEL0: 0x521A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOEsel							

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
7:0	portOEsel[7:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.299 PRT3_OE_SEL1

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT3_OE_SEL1: 0x521B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOEsel							

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
7:0	portOEsel[7:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.300 PRT3_DBL_SYNC_IN

DSI double sync enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT3_DBL_SYNC_IN: 0x521C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	dbl_sync_in							

The port double sync register selects to synchronize the data in from the port before driving the digital system interconnect (DSI) signals to the UDB.

Bits	Name	Description
7:0	dbl_sync_in[7:0]	When asserted selects to synchronize the data in from the corresponding pad.

1.3.301 PRT3_SYNC_OUT

DSI sync out enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT3_SYNC_OUT: 0x521D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	sync_out							

The port sync register selects to synchronize the data driving the pad using the existing port data register.

Bits	Name	Description
7:0	sync_out[7:0]	When asserted selects to synchronize the data from the DSI driving the corresponding pad.

1.3.302 PRT3_CAPS_SEL

Global DSI select register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT3_CAPS_SEL: 0x521E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	caps_sel							

The global DSI select register. When enabled, the global DSI dynamic control is selected to drive the dig_glbl_ctl.

Bits	Name	Description
7:0	caps_sel[7:0]	When asserted selects the global DSI to drive dig_glbl_ctl on the pad.

1.3.303 PRT4_OUT_SEL0

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT4_OUT_SEL0: 0x5220

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.304 PRT4_OUT_SEL1

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT4_OUT_SEL1: 0x5221

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.305 PRT4_OE_SEL0

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT4_OE_SEL0: 0x5222

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOEsel							

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
7:0	portOEsel[7:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.306 PRT4_OE_SEL1

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT4_OE_SEL1: 0x5223

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOEsel							

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
7:0	portOEsel[7:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.307 PRT4_DBL_SYNC_IN

DSI double sync enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT4_DBL_SYNC_IN: 0x5224

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	dbl_sync_in							

The port double sync register selects to synchronize the data in from the port before driving the digital system interconnect (DSI) signals to the UDB.

Bits	Name	Description
7:0	dbl_sync_in[7:0]	When asserted selects to synchronize the data in from the corresponding pad.

1.3.308 PRT4_SYNC_OUT

DSI sync out enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT4_SYNC_OUT: 0x5225

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	sync_out							

The port sync register selects to synchronize the data driving the pad using the existing port data register.

Bits	Name	Description
7:0	sync_out[7:0]	When asserted selects to synchronize the data from the DSI driving the corresponding pad.

1.3.309 PRT4_CAPS_SEL

Global DSI select register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT4_CAPS_SEL: 0x5226

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	caps_sel							

The global DSI select register. When enabled, the global DSI dynamic control is selected to drive the dig_glbl_ctl.

Bits	Name	Description
7:0	caps_sel[7:0]	When asserted selects the global DSI to drive dig_glbl_ctl on the pad.

1.3.310 PRT5_OUT_SEL0

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT5_OUT_SEL0: 0x5228

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.311 PRT5_OUT_SEL1

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT5_OUT_SEL1: 0x5229

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.312 PRT5_OE_SEL0

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT5_OE_SEL0: 0x522A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOEsel							

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
7:0	portOEsel[7:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.313 PRT5_OE_SEL1

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT5_OE_SEL1: 0x522B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOEsel							

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
7:0	portOEsel[7:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.314 PRT5_DBL_SYNC_IN

DSI double sync enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT5_DBL_SYNC_IN: 0x522C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	dbl_sync_in							

The port double sync register selects to synchronize the data in from the port before driving the digital system interconnect (DSI) signals to the UDB.

Bits	Name	Description
7:0	dbl_sync_in[7:0]	When asserted selects to synchronize the data in from the corresponding pad.

1.3.315 PRT5_SYNC_OUT

DSI sync out enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT5_SYNC_OUT: 0x522D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	sync_out							

The port sync register selects to synchronize the data driving the pad using the existing port data register.

Bits	Name	Description
7:0	sync_out[7:0]	When asserted selects to synchronize the data from the DSI driving the corresponding pad.

1.3.316 PRT5_CAPS_SEL

Global DSI select register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT5_CAPS_SEL: 0x522E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	caps_sel							

The global DSI select register. When enabled, the global DSI dynamic control is selected to drive the dig_glbl_ctl.

Bits	Name	Description
7:0	caps_sel[7:0]	When asserted selects the global DSI to drive dig_glbl_ctl on the pad.

1.3.317 PRT6_OUT_SEL0

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT6_OUT_SEL0: 0x5230

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.318 PRT6_OUT_SEL1

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT6_OUT_SEL1: 0x5231

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.319 PRT6_OE_SEL0

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT6_OE_SEL0: 0x5232

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOEsel							

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
7:0	portOEsel[7:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.320 PRT6_OE_SEL1

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT6_OE_SEL1: 0x5233

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOEsel							

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
7:0	portOEsel[7:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.321 PRT6_DBL_SYNC_IN

DSI double sync enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT6_DBL_SYNC_IN: 0x5234

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	dbl_sync_in							

The port double sync register selects to synchronize the data in from the port before driving the digital system interconnect (DSI) signals to the UDB.

Bits	Name	Description
7:0	dbl_sync_in[7:0]	When asserted selects to synchronize the data in from the corresponding pad.

1.3.322 PRT6_SYNC_OUT

DSI sync out enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT6_SYNC_OUT: 0x5235

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	sync_out							

The port sync register selects to synchronize the data driving the pad using the existing port data register.

Bits	Name	Description
7:0	sync_out[7:0]	When asserted selects to synchronize the data from the DSI driving the corresponding pad.

1.3.323 PRT6_CAPS_SEL

Global DSI select register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT6_CAPS_SEL: 0x5236

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	caps_sel							

The global DSI select register. When enabled, the global DSI dynamic control is selected to drive the dig_glbl_ctl.

Bits	Name	Description
7:0	caps_sel[7:0]	When asserted selects the global DSI to drive dig_glbl_ctl on the pad.

1.3.324 PRT12_OUT_SEL0

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_OUT_SEL0: 0x5260

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.325 PRT12_OUT_SEL1

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_OUT_SEL1: 0x5261

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.326 PRT12_OE_SEL0

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_OE_SEL0: 0x5262

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOEsel							

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
7:0	portOEsel[7:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.327 PRT12_OE_SEL1

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_OE_SEL1: 0x5263

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOEsel							

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
7:0	portOEsel[7:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.328 PRT12_DBL_SYNC_IN

DSI double sync enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_DBL_SYNC_IN: 0x5264

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	dbl_sync_in							

The port double sync register selects to synchronize the data in from the port before driving the digital system interconnect (DSI) signals to the UDB.

Bits	Name	Description
7:0	dbl_sync_in[7:0]	When asserted selects to synchronize the data in from the corresponding pad.

1.3.329 PRT12_SYNC_OUT

DSI sync out enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT12_SYNC_OUT: 0x5265

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	sync_out							

The port sync register selects to synchronize the data driving the pad using the existing port data register.

Bits	Name	Description
7:0	sync_out[7:0]	When asserted selects to synchronize the data from the DSI driving the corresponding pad.

1.3.330 PRT15_OUT_SEL0

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_OUT_SEL0: 0x5278

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.331 PRT15_OUT_SEL1

Digital System Interconnect Port Pin Output Select Registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_OUT_SEL1: 0x5279

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	portOutsel							

The corresponding bits for each pad of Output select register 1 and register 0 together select the DSI net driving the corresponding output port pin for each bit of the port. This is implemented with a 4-to-1 multiplexer for each port pin output. This allows each pin to be driven by four of the eight available DSI connections to the port.

For port *x* pin *y* , the TAP selects from the dsi to pad 3 through 0 for pads 3 through 0 **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 0 TAP == 01 Select DSI 1 TAP == 10 Select DSI 2 TAP == 11 Select DSI 3

For port *x* pin *y* , the TAP selects from the dsi to pad 7 through 4 for pads 7 through 4. **TAP == {PRT [*x*] OUT_SEL1 [*y*] , PRT [*x*] OUT_SEL0 [*y*] }** TAP == 00 Select DSI 4 TAP == 01 Select DSI 5 TAP == 10 Select DSI 6 TAP == 11 Select DSI 7

Bits	Name	Description
7:0	portOutsel[7:0]	Selects which of the available taps are selected for the given I/O pin output.

1.3.332 PRT15_OE_SEL0

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_OE_SEL0: 0x527A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:000000					
HW Access	NA		R					
Retention	NA		RET					
Name	RSVD		portOEsel					

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
5:0	portOEsel[5:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.333 PRT15_OE_SEL1

Dynamic Drive Stength of Port Output Enable Select registers.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_OE_SEL1: 0x527B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:000000					
HW Access	NA		R					
Retention	NA		RET					
Name	RSVD		portOEsel					

The dynamic output enable select registers 1 and register 0 together select the DSI dynamic control bits for each port pin, the corresponding bit from each register is selects the DSI for each pad. This is implemented with a 4-to-1 multiplexr for each port pin output enable.

TAP == {PRT [*x*] OE_SEL1 [*y*] , PRT [*x*] OE_SEL0 [*y*] } TAP == 00 Select DSI dynamic oe 0 TAP == 01 Select DSI dynamic oe 1 TAP == 10 Select DSI dynamic oe 2 TAP == 11 Select DSI dynamic oe 3

Bits	Name	Description
5:0	portOEsel[5:0]	Selects which of the available taps are selected for the given I/O pin.

1.3.334 PRT15_DBL_SYNC_IN

DSI double sync enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_DBL_SYNC_IN: 0x527C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	dbl_sync_in							

The port double sync register selects to synchronize the data in from the port before driving the digital system interconnect (DSI) signals to the UDB.

Bits	Name	Description
7:0	dbl_sync_in[7:0]	When asserted selects to synchronize the data in from the corresponding pad.

1.3.335 PRT15_SYNC_OUT

DSI sync out enable register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_SYNC_OUT: 0x527D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	sync_out							

The port sync register selects to synchronize the data driving the pad using the existing port data register.

Bits	Name	Description
7:0	sync_out[7:0]	When asserted selects to synchronize the data from the DSI driving the corresponding pad.

1.3.336 PRT15_CAPS_SEL

Global DSI select register.

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PRT15_CAPS_SEL: 0x527E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:000000					
HW Access	NA		R					
Retention	NA		RET					
Name	RSVD		sync_out					

The global DSI select register. When enabled, the global DSI dynamic control is selected to drive the dig_glbl_ctl.

Bits	Name	Description
5:0	sync_out[5:0]	When asserted selects the global DSI to drive dig_glbl_ctl on the pad.

1.3.337 EMIF_NO_UDB

EMIF UDB/NO_UDB Mode Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

EMIF_NO_UDB: 0x5400

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Retention	NA							RET
Name	RSVD							no_udb

This register indicates whether UDBs are generating external memory control signals or to enable EMIF to generate them for Flow Through Sync SRAM or Asynchronous SRAM. In the table, reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits should always be written with a value of '0'.

Bits	Name	Description
0	no_udb	1'b0: UDB Mode. In this mode EMIF bypasses the external memory transfer request to UDBs and UDBs should be configured to generate the control signals for external memory. 1`b1: NO_UDB Mode. In this mode, the EMIF generates the control signals for Flow through Sync SRAM or Async SRAM

1.3.338 EMIF_RP_WAIT_STATES

External Memory Interface Read Path Wait States Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

EMIF_RP_WAIT_STATES: 0x5401

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:000		
HW Access	NA					R		
Retention	NA					RET		
Name	RSVD					rp_wait_states		

This register configures the additional wait states for read operation. In the table, reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits should always be written with a value of '0'.

Bits	Name	Description
2:0	rp_wait_states[2:0]	In NO_UDB mode the following table determines the minimum number of additional clock cycles (wait states) required to complete the external read operation (this table assumes EMIF_MEMCLK_DIV is programmed correctly relative to f(HCLK)): 0 <= f(HCLK) <= 19: RP_WAIT_STATES can be 0 or more 19 < f(HCLK) <= 33: RP_WAIT_STATES must be >= 1 33 < f(HCLK) <= 41: RP_WAIT_STATES can be 0 or more 41 < f(HCLK) <= 54: RP_WAIT_STATES must be >= 1 54 < f(HCLK) <= 67: RP_WAIT_STATES must be >= 2 67 < f(HCLK) <= 82: RP_WAIT_STATES must be >= 2 82 < f(HCLK) <= 95: RP_WAIT_STATES must be >= 3 95 < f(HCLK) <= 99: RP_WAIT_STATES must be >= 4

1.3.339 EMIF_MEM_DWN

External Memory Power Down Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

EMIF_MEM_DWN: 0x5402

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Retention	NA							RET
Name	RSVD							mem_pd

This register puts the external memory into power down mode. This register is active only for Sync SRAM in NO_UDB mode. In the table, reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits should always be written with a value of '0'.

Bits	Name	Description
0	mem_pd	1`b1: External Memory power down. 1`b0: External memory power up

1.3.340 EMIF_MEMCLK_DIV

External Memory Clock Divider Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

EMIF_MEMCLK_DIV: 0x5403

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:00	
HW Access	NA						R	
Retention	NA						RET	
Name	RSVD						memclk_div	

This register sets the divider value for external memory clock frequency. In the table, reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits should always be written with a value of '0'.

Bits	Name	Description
1:0	memclk_div[1:0]	2'b00: f(EM_clock) = f(HCLK), when f(HCLK) <= 33MHz. 2'b01: f(EM_clock) = 1/2f(HCLK), when 33MHz <= f(HCLK) <= 67MHz. 2'b10: f(EM_clock) = 1/3f(HCLK), when 67MHz <= f(HCLK) <= 99MHz. 2'b11: f(EM_clock) = 1/4f(HCLK), Backup configuration.

1.3.341 EMIF_CLOCK_EN

EMIF Clock Enable Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

EMIF_CLOCK_EN: 0x5404

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Retention	NA							RET
Name	RSVD							clock_en

This register enables the clock for EMIF core logic.

Bits	Name	Description
0	clock_en	1'b0: Disable Clock for EMIF core logic. 1'b1: Enable Clock for EMIF core. Along with this bit, the input 'emif_clk_en' to EMIF block should also be 1'b1 to enable the clock. This input can be made 1'b1 by setting corresponding bit in PM.ACT.CFG5 register in Power Manager.

1.3.342 EMIF_EM_TYPE

External Memory Type Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

EMIF_EM_TYPE: 0x5405

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Retention	NA							RET
Name	RSVD							em_type

This register indicates whether to generate control signals for Sync or Async SRAM in NO_UDB mode

Bits	Name	Description
0	em_type	1'b0: Generate control signals for Flow through Sync SRAM (CY7C1324H). 1'b1: Generate control signals for Async SRAM (CY7C1041D).

1.3.343 EMIF_WP_WAIT_STATES

External Memory Interface Write Path Wait States Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

EMIF_WP_WAIT_STATES: 0x5406

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:000		
HW Access	NA					R		
Retention	NA					RET		
Name	RSVD					wp_wait_states		

This register configures the additional wait states for write operation. In the table, reserved bits are grayed table cells and are not described in the bit description section below. Reserved bits should always be written with a value of '0'.

Bits	Name	Description
2:0	wp_wait_states[2:0]	In NO_UDB mode the following table determines the minimum number of additional clock cycles (wait states) required to complete the external write operation (this table assumes EMIF_MEMCLK_DIV is programmed correctly relative to f(HCLK)): 0 <= f(HCLK) <= 28: WP_WAIT_STATES can be 0 or more 28 < f(HCLK) <= 33: WP_WAIT_STATES must be >= 1 33 < f(HCLK) <= 61: WP_WAIT_STATES can be 0 or more 61 < f(HCLK) <= 67: WP_WAIT_STATES must be >= 1 67 < f(HCLK) <= 81: WP_WAIT_STATES can be 0 or more 81 < f(HCLK) <= 99: WP_WAIT_STATES must be >= 1

1.3.344 SC[0..3]_CR0

Switched Capacitor Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_CR0: 0x5800 SC1_CR0: 0x5804 SC2_CR0: 0x5808

SC3_CR0: 0x580C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		NA:00		R/W:000			NA:0
HW Access	NA		NA		R			NA
Retention	NA		NA		RET			NA
Name	RSVD		R		mode			RSVD

Bits	Name	Description
3:1	mode[2:0]	Configuration select for the SC block See Table 1-154.

Table 1-154. Bit field encoding: SC_MODE_ENUM

Value	Name	Description
3'b000	SC_MODE_NAKED_OPAMP	Naked Op-Amp
3'b001	SC_MODE_TIA	Transimpedance Amplifier (TIA)
3'b010	SC_MODE_CTMIXER	Continuous Time Mixer
3'b011	SC_MODE_NRZ_SH	Discrete Time Mixer - NRZ S/H
3'b100	SC_MODE_UNITY	Unity Gain Buffer
3'b101	SC_MODE_1ST_MOD	First Order Modulator
3'b110	SC_MODE_PGA	Programmable Gain Amplifier (PGA)
3'b111	SC_MODE_TRACKANDHOLD	Track and Hold

1.3.345 SC[0..3]_CR1

Switched Capacitor Control Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_CR1: 0x5801 SC1_CR1: 0x5805 SC2_CR1: 0x5809

SC3_CR1: 0x580D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:00		R/W:00	
HW Access	NA		R	R	R		R	
Retention	NA		RET	RET	RET		RET	
Name	RSVD		gain	div2	comp		drive	

Bits	Name	Description
5	gain	Controls the ratio of the feedback cap for S/H Mixer mode and PGA mode See Table 1-158.
4	div2	When 0, the sample clock only needs to be half the desired sample frequency for S/H Mixer mode See Table 1-156.
3:2	comp[1:0]	Selects between various compensation capacitor sizes See Table 1-155.
1:0	drive[1:0]	Selects between current settings (I_Load (uA)) in the output buffer See Table 1-157.

Table 1-155. Bit field encoding: SC_COMP_ENUM

Value	Name	Description
2'b00	SC_COMP_3P0PF	3.0pF
2'b01	SC_COMP_3P6PF	3.6pF
2'b10	SC_COMP_4P35PF	4.35pF
2'b11	SC_COMP_5P1PF	5.1pF

Table 1-156. Bit field encoding: SC_DIV2_ENUM

Value	Name	Description
1'b0	SC_DIV2_DISABLE	no frequency division
1'b1	SC_DIV2_ENABLE	SC CLK is divided by two

Table 1-157. Bit field encoding: SC_DRIVE_ENUM

Value	Name	Description
2'b00	I_LOAD_175UA	175 uA
2'b01	I_LOAD_260UA	260 uA
2'b10	I_LOAD_330UA	330 uA
2'b11	I_LOAD_400UA	400 uA

Table 1-158. Bit field encoding: SC_GAIN_ENUM

Value	Name	Description

(continued)

Table 1-158. Bit field encoding: SC_GAIN_ENUM

1'b0	GAIN_0DB	0 dB
1'b1	GAIN_6DB	6 dB

1.3.346 SC[0..3]_CR2

Switched Capacitor Control Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_CR2: 0x5802 SC1_CR2: 0x5806 SC2_CR2: 0x580A

SC3_CR2: 0x580E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:000			R/W:00		R/W:0	R/W:0
HW Access	R	R			R		R	R
Retention	RET	RET			RET		RET	RET
Name	pga_gndvref	rval			redc		r20_40b	bias_ctrl

Bits	Name	Description
7	pga_gndvref	Programmable Gain Amplifier Application - Ground VREF See Table 1-160.
6:4	rval[2:0]	Programmable Gain Amplifier (PGA) and Transimpedance Amplifier (TIA): Feedback resistor (Rfb) See Table 1-163.
3:2	redc[1:0]	Another stability control setting. Adjusts capactiance between amplifier output and first stage See Table 1-162.
1	r20_40b	PGA Mode: input impedance (Rin), Mixer Mode: input and feedback impedance (Rmix) See Table 1-161.
0	bias_ctrl	Toggles the bias current in the amplifier between normal and 1/2 See Table 1-159.

Table 1-159. Bit field encoding: SC_BIAS_CONTROL_ENUM

Value	Name	Description
1'b0	BIAS_1X	1x current reference reduces bandwidth to increase stability
1'b1	BIAS_2X	normal operation - 2x current reference to increase bandwidth

Table 1-160. Bit field encoding: SC_PGA_GNDVREF_ENUM

Value	Name	Description
1'b0	SC_PGA_GNDVREF_DIS	VREF not grounded
1'b1	SC_PGA_GNDVREF_EN	VREF grounded

Table 1-161. Bit field encoding: SC_R20_40B_ENUM

Value	Name	Description
1'b0	SC_R20_40B_40K	40kOhm
1'b1	SC_R20_40B_20K	20kOhm

(continued)

Table 1-162. Bit field encoding: SC_REDC_ENUM

Value	Name	Description
2'b00	SC_REDC_00	Varies depending on mode. See Switched Cap documentation
2'b01	SC_REDC_01	Varies depending on mode. See Switched Cap documentation
2'b10	SC_REDC_10	Varies depending on mode. See Switched Cap documentation
2'b11	SC_REDC_11	Varies depending on mode. See Switched Cap documentation

Table 1-163. Bit field encoding: SC_RVAL_ENUM

Value	Name	Description
3'b000	SC_RVAL_20	20 kOhm
3'b001	SC_RVAL_30	30 kOhm
3'b010	SC_RVAL_40	40 kOhm
3'b011	SC_RVAL_80	80 kOhm
3'b100	SC_RVAL_120	120 kOhm
3'b101	SC_RVAL_250	250 kOhm
3'b110	SC_RVAL_500	500 kOhm
3'b111	SC_RVAL_1000	1 MegaOhm

1.3.347 DAC[0..3]_CR0

DAC Block Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC0_CR0: 0x5820 DAC1_CR0: 0x5824 DAC2_CR0: 0x5828

DAC3_CR0: 0x582C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:00		R/W:0	NA:0
HW Access	NA			R	R		R	NA
Retention	NA			RET	RET		RET	NA
Name	RSVD			mode	range		hs	RSVD

Bits	Name	Description
4	mode	Mode Bit See Table 1-165.
3:2	range[1:0]	Ranges for mode=0 (VDAC) and mode=1 (IDAC) See Table 1-166.
1	hs	High Speed Bit See Table 1-164.

Table 1-164. Bit field encoding: DAC_HS_ENUM

Value	Name	Description
1'b0	DAC_HS_LOWPOWER	regular (low power)
1'b1	DAC_HS_HIGHSPEED	high speed (higher power)

Table 1-165. Bit field encoding: DAC_MODE_ENUM

Value	Name	Description
1'b0	DAC_MODE_V	voltage DAC
1'b1	DAC_MODE_I	current DAC

Table 1-166. Bit field encoding: DAC_RANGE_ENUM

Value	Name	Description
2'b00	DAC_RANGE_0	x0=0V to 4*vref (1.024V); 0 to 31.875uA
2'b01	DAC_RANGE_1	x1=0V to 16*vref (4.096V); 0 to 255uA
2'b10	DAC_RANGE_2	x0=0V to 4*vref (1.024V); 0 to 2.040mA
2'b11	DAC_RANGE_3	x1=0V to 16*vref (4.096V); not used

1.3.348 DAC[0..3]_CR1

DAC Block Control Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC0_CR1: 0x5821 DAC1_CR1: 0x5825 DAC2_CR1: 0x5829

DAC3_CR1: 0x582D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R	R	R	R	R	R
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		mx_data	reset_udb_en	mx_idir	idirbit	mx_ioff	ioffbit

Bits	Name	Description
5	mx_data	Select DATA source See Table 1-168.
4	reset_udb_en	DAC reset enable See Table 1-171.
3	mx_idir	Mux selection for DAC current direction control See Table 1-169.
2	idirbit	register source for DAC current direction See Table 1-167.
1	mx_ioff	Mux selection for DAC current off control See Table 1-170.
0	ioffbit	register source for DAC current off

Table 1-167. Bit field encoding: IDIRBIT_ENUM

Value	Name	Description
1'b1	IDIR_SNK	Current sink
1'b0	IDIR_SRC	Current source

Table 1-168. Bit field encoding: MX_DATA_ENUM

Value	Name	Description
1'b0	MX_DATA_REG	Select register source (DACxn_D)
1'b1	MX_DATA_UDB	Select UDB source

Table 1-169. Bit field encoding: MX_IDIR_ENUM

Value	Name	Description
1'b0	MX_IDIR_REG	Register source idirbit selected
1'b1	MX_IDIR_UDB	UDB ictrl selected

(continued)

Table 1-170. Bit field encoding: MX_IOFF_ENUM

Value	Name	Description
1'b0	MX_IOFF_REG	Register source ioffbit selected
1'b1	MX_IOFF_UDB	UDB ictrl selected

Table 1-171. Bit field encoding: RESET_UDB_EN_ENUM

Value	Name	Description
1'b0	RESET_UDB_EN_DISABLE	Disable DAC Reset Source from UDB (System reset always resets)
1'b1	RESET_UDB_EN_ENABLE	Enable DAC Reset Source from UDB

1.3.349 CMP[0..3]_CR

Comparator Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP0_CR: 0x5840 CMP1_CR: 0x5841 CMP2_CR: 0x5842

CMP3_CR: 0x5843

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:00	
HW Access	NA	R	R	R	R	R	R	
Retention	NA	RET	RET	RET	RET	RET	RET	
Name	RSVD	filt	hyst	cal_en	mx_ao	pd_override	sel	

Bits	Name	Description
6	filt	enables a glitch filter at the output of the comparator See Table 1-173.
5	hyst	enables a hysteresis of 10mV typ. See Table 1-174.
4	cal_en	enables shorting of the two comparator inputs for trim calibration purposes See Table 1-172.
3	mx_ao	comparator sleep always-on logic mux control See Table 1-175.
2	pd_override	Power down override to allow comparator to continue operating during sleep. Note: if chip wants to wakeup using p3comp resource, this bit must be set to 1. See Table 1-176.
1:0	sel[1:0]	Selects the mode of operation of the comparator See Table 1-177.

Table 1-172. Bit field encoding: CMP_CAL_EN_ENUM

Value	Name	Description
1'b0	CMP_CAL_EN_DISABLE	Disable calibration
1'b1	CMP_CAL_EN_ENABLE	Enable calibration

Table 1-173. Bit field encoding: CMP_FILT_ENUM

Value	Name	Description
1'b0	CMP_FILT_DISABLE	Disable glitch filter
1'b1	CMP_FILT_ENABLE	Enable glitch filter

Table 1-174. Bit field encoding: CMP_HYST_ENUM

Value	Name	Description
1'b1	CMP_HYST_DISABLE	Disable hysteresis

(continued)

Table 1-174. Bit field encoding: CMP_HYST_ENUM

1'b0	CMP_HYST_ENABLE	Enable hysteresis

Table 1-175. Bit field encoding: CMP_MX_AO_ENUM

Value	Name	Description
1'b0	CMP_MX_AO_BYPASS	Bypass comparator sleep always-on logic
1'b1	CMP_MX_AO_ENABLE	Enable comparator sleep always-on logic

Table 1-176. Bit field encoding: CMP_PD_OVERRIDE_ENUM

Value	Name	Description
1'b0	CMP_PD_OVERRIDE_DISABLE	Don't override power down
1'b1	CMP_PD_OVERRIDE_ENABLE	Override power down

Table 1-177. Bit field encoding: SEL_ENUM

Value	Name	Description
2'b00	SEL_SLOW	slow mode
2'b01	SEL_FAST	fast mode
2'b10	SEL_LP	ultra low power mode. Note: if chip wants to wakeup using p3comp resource, p3comp shall be in ultra low power mode and pd_override bit must be set to 1
2'b11	SEL_ILLEGAL	Illegal Mode

1.3.350 LUT[0..3]_CR

LUT Config Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LUT0_CR: 0x5848 LUT1_CR: 0x584A LUT2_CR: 0x584C

LUT3_CR: 0x584E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Retention	NA				RET			
Name	RSVD				q			

Bits	Name	Description
3:0	q[3:0]	LUT function See Table 1-178.

Table 1-178. Bit field encoding: LUT_Q_ENUM

Value	Name	Description
4'h0	LUT_Q_0	FALSE (0)
4'h1	LUT_Q_A_AND_B	A AND B
4'h2	LUT_Q_A_AND_NOTB	A AND !B
4'h3	LUT_Q_A	A
4'h4	LUT_Q_NOTA_AND_B	!A AND B
4'h5	LUT_Q_B	B
4'h6	LUT_Q_A_XOR_B	A XOR B
4'h7	LUT_Q_A_OR_B	A OR B
4'h8	LUT_Q_A_NOR_B	A NOR B
4'h9	LUT_Q_A_XNOR_B	A XNOR B
4'ha	LUT_Q_NOTB	!B
4'hb	LUT_Q_A_OR_NOTB	A OR !B
4'hc	LUT_Q_NOTA	!A
4'hd	LUT_Q_NOTA_OR_B	!A OR B
4'he	LUT_Q_A_NAND_B	A NAND B
4'hf	LUT_Q_1	TRUE (1)

1.3.351 LUT[0..3]_MX

LUT Input Mux Config Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LUT0_MX: 0x5849 LUT1_MX: 0x584B LUT2_MX: 0x584D

LUT3_MX: 0x584F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:00		NA:00		R/W:00	
HW Access	NA		R		NA		R	
Retention	NA		RET		NA		RET	
Name	RSVD		mx_b		RSVD		mx_a	

Bits	Name	Description
5:4	mx_b[1:0]	Mux Select for LUT Input B See Table 1-179.
1:0	mx_a[1:0]	Mux Select for LUT Input A See Table 1-179.

Table 1-179. Bit field encoding: LUT_MUX_ENUM

Value	Name	Description
2'h0	LUT_MUX_0	CMP0 output selected
2'h1	LUT_MUX_1	CMP1 output selected
2'h2	LUT_MUX_2	CMP2 output selected
2'h3	LUT_MUX_3	CMP3 output selected

1.3.352 OPAMP[0..3]_CR

Analog Output Buffer Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

OPAMP0_CR: 0x5858 OPAMP1_CR: 0x585A OPAMP2_CR: 0x585C

OPAMP3_CR: 0x585E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:00	
HW Access	NA						R	
Retention	NA						RET	
Name	RSVD						pwr_mode	

Bits	Name	Description
1:0	pwr_mode[1:0]	Power Mode See Table 1-180.

Table 1-180. Bit field encoding: OPAMP_PWR_MODE_ENUM

Value	Name	Description
2'h0	OPAMP_PWR_MODE_TIA	TIA (default)
2'h1	OPAMP_PWR_MODE_SLOW	Slow
2'h2	OPAMP_PWR_MODE_MEDIUM	Medium
2'h3	OPAMP_PWR_MODE_FAST	Fast

1.3.353 OPAMP[0..3]_RSVD

OPAMP reserved

Reset: System reset for retention flops [reset_all_retention]

Register : Address

OPAMP0_RSVD: 0x5859 OPAMP1_RSVD: 0x585B

OPAMP2_RSVD: 0x585D OPAMP3_RSVD: 0x585F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R							
Retention	NA							
Name	RSVD							

Bits	Name	Description
7:0	RSVD[7:0]	Reserved for OPAMP expansion

1.3.354 LCDDAC_CR0

LCD Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LCDDAC_CR0: 0x5868

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:000			R/W:0	NA:0	R/W:00	
HW Access	R	NA			R	NA	R	
Retention	RET	NA			RET	NA	RET	
Name	lp_en	RSVD			continous_drive	RSVD	bias_sel	

Bits	Name	Description
7	lp_en	Setting this bit allows the UDB to gate the Low Power Ack for the LCD Subsystem (lcd_lp_ack_n); When set to 0, the LCD subsystem LP ack is directly driven by the lpreq from the power manager See Table 1-183.
3	continous_drive	This bit allows the LCDDAC to remain active when the chip goes to sleep. In this mode, the LCDDAC drives the LCD pins while the LCD Driver is in bypass mode See Table 1-182.
1:0	bias_sel[1:0]	Selects the LCD bias/multiplex ratio See Table 1-181.

Table 1-181. Bit field encoding: LCDDAC_BIAS_SELECT_ENUM

Value	Name	Description
2'b00	LCDDAC_BIAS_SELECT_1DIV3	v0=2.0-supply; v1=0.666*v0; v2=0.333*v0; v3=0.666*v0; v4=0.333*v0; Multiplex ratios=2:1,3:1,4:1
2'b01	LCDDAC_BIAS_SELECT_1DIV4	v0=2.0-supply; v1=0.750*v0; v2=0.500*v0; v3=0.500*v0; v4=0.250*v0; Multiplex ratio=8:1
2'b10	LCDDAC_BIAS_SELECT_1DIV5	v0=2.0-supply; v1=0.800*v0; v2=0.600*v0; v3=0.400*v0; v4=0.200*v0; Multiplex ratio=16:1
2'b11	LCDDAC_BIAS_SELECT_1DIV5_ALSO	v0=2.0-supply; v1=0.800*v0; v2=0.600*v0; v3=0.400*v0; v4=0.200*v0; Multiplex ratio=16:1

Table 1-182. Bit field encoding: LCDDAC_CONTINUOUS_DRIVE_ENUM

Value	Name	Description
1'b0	LCDDAC_CONTINUOUS_DRIVE_CANCATCHZZZ	LCDDAC is powered down when the chip is in sleep
1'b1	LCDDAC_CONTINUOUS_DRIVE_LIVINGDEAD	LCDDAC is active when the chip is in sleep

Table 1-183. Bit field encoding: LCD_LP_EN_ENUM

Value	Name	Description
1'b0	LCD_LP_EN_DISABLED	LCD UDB LP Ack Disabled

(continued)

Table 1-183. Bit field encoding: LCD_LP_EN_ENUM

1'b1	LCD_LP_EN_ENABLED	LCD UDB LP Ack Enabled

1.3.355 LCDDAC_CR1

LCDDAC Control Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LCDDAC_CR1: 0x5869

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:000000					
HW Access	NA	R	R					
Retention	NA	RET	RET					
Name	RSVD	nc	contrast_ctl					

Bits	Name	Description
6	nc	Not connected
5:0	contrast_ctl[5:0]	LCD Contrast control setting. Bit6 Not Connected; Step size is 27.3 mV @ 3.0 V supply and 50 mV @ 5.5 V supply; Min V0 should be 2 V. To achieve this, use code value 6'h00 for 5.5 V supply and 6'h21 for 3 V supply. Max V0 is equal to supply level for code value 6'h3f See Table 1-184.

Table 1-184. Bit field encoding: LCDDAC_D_ENUM

Value	Name	Description
6'h0	LCDDAC_D_MIN	Minimum
6'h3f	LCDDAC_D_MAX	Max

1.3.356 LCDDRV_CR

LCD Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LCDDRV_CR: 0x586A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA			R	R	R	R	R
Retention	NA			RET	RET	RET	RET	RET
Name	RSVD			bypass_en	pts	invert	mode_0	dispblnk

Bits	Name	Description
4	bypass_en	This bit enables bypassing the LCD Driver, so that the LCDDAC is driving the LCD glass. The LCDDAC continuous_drive bit is also set to allow the LCDDAC to remain active when the chip goes to sleep. See Table 1-185.
3	pts	pts (pull-to-supply) signal enables the LCD Driver to be able to drive to supply level. In normal operation, the ouput of the LCD Driver is limited to VIO-0.5V whereas when the pts mode is enabled, the output can reach to VIO. See Table 1-189.
2	invert	Invert LCD Display (invert display data on all pins configured as segments) See Table 1-187.
1	mode_0	LCD Driver mode[0]; mode[2:1] come from DSI HiDrive modes: HiDrive mode is used to refresh or to write new data to the LCD glass. Reason for different drive strengths is to save power and reduce AC coupling. There are cases where common drivers face more load then segment drivers. For these cases stronger commons should be selected. Also, to reduce AC coupling, the common drivers should be stronger than segment drivers (assuming number of common pins are less than segment pins). For cases where there is a big glass with number of common pins is close to or equal to segment pins, com=4x and seg=4x should be used to reduce charge times LoDrive modes: The purpose of this mode is to sustain the voltage on the LCD in the case of a leakage. In the case of higher leakage due to glass type, glass size or environment temperature; stronger LoDrive mode can be used. Control Bits Mode Drive Strength mode[2:0] 000 HiDrive seg=1x, com=1x 001 HiDrive seg=1x, com=2x 010 HiDrive seg=1x, com=4x 011 HiDrive seg=2x, com=2x 100 HiDrive seg=2x, com=4x 101 HiDrive seg=4x, com=4x 110 LoDrive seg=1x, com=1x 111 LoDrive seg=2x, com=2x See Table 1-188.

(continued)

0	dispblnk	LCD Display Blank See Table 1-186.

Table 1-185. Bit field encoding: LCD_BYPASS_EN_ENUM

Value	Name	Description
1'b0	LCD_BYPASS_EN_LCDDRV_DRIVES_GLASS	Normal mode
1'b1	LCD_BYPASS_EN_LCDDAC_DRIVES_GLASS	Bypass mode

Table 1-186. Bit field encoding: LCD_DISPBLNK_ENUM

Value	Name	Description
1'b0	LCD_DISPBLNK_HIZ	When in a low power mode, set output buffer in LCD Drivers to hi impedance. This leaves intact the last image driven to the LCD display (charge will slowly leak off and the image will fade unless updated).
1'b1	LCD_DISPBLNK_BLANK	When in a low power mode, set output buffer in LCD Drivers to ground. Blanks the LCD display.

Table 1-187. Bit field encoding: LCD_INVERT_ENUM

Value	Name	Description
1'b0	LCD_INVERT_DISABLED	Normal display
1'b1	LCD_INVERT_ENABLED	Inverted display

Table 1-188. Bit field encoding: LCD_MODE_0_ENUM

Value	Name	Description
1'b0	LCD_MODE_0_0	Depends on other signals
1'b1	LCD_MODE_0_1	Depends on other signals

Table 1-189. Bit field encoding: LCD_PTS_ENUM

Value	Name	Description
1'b0	LCD_PTS_0	normal operation, VOUT = VIO-0.5V
1'b1	LCD_PTS_1	pts mode enabled, VOUT = VIO

1.3.357 LCDTMR_CFG

LCD Timer Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LCDTMR_CFG: 0x586B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:000000						R/W:0	R/W:0
HW Access	R						R	R
Retention	RET						RET	RET
Name	period						clk_sel	en_timer

Bits	Name	Description
7:2	period[5:0]	LCD timer period / lcd_int period; change only when LCD timer is disabled
1	clk_sel	LCD timer clock source selection bit; change only when LCD timer is disabled See Table 1-190.
0	en_timer	LCD timer enable bit See Table 1-191.

Table 1-190. Bit field encoding: LCD_CLK_SEL_ENUM

Value	Name	Description
1'b0	LCD_CLK_SEL_ILO_1KHZ	ILO 1kHz
1'b1	LCD_CLK_SEL_ECO_8KHZ	8kHz Tap of ONEPPS (One Pulse Per Second) from 32kHz External Watch Crystal Oscillator

Table 1-191. Bit field encoding: LCD_EN_TIMER_ENUM

Value	Name	Description
1'b0	LCD_EN_TIMER_DISABLED	LCD Timer is disabled
1'b1	LCD_EN_TIMER_ENABLED	LCD Timer is enabled

1.3.358 BG_CR0

Bandgap Precision Reference Control 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BG_CR0: 0x586C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:00	
HW Access	NA				R	R	R	
Retention	NA				RET	RET	RET	
Name	RSVD				bg_vda_res_en	bg_vda_swabusl0	cmp_mxvn	

Bits	Name	Description
3	bg_vda_res_en	Bandgap VDA See Table 1-192.
2	bg_vda_swabusl0	Switch Control for VDA Bandgap output to abusl0 connection See Table 1-193.
1:0	cmp_mxvn[1:0]	Mux for comparator reference cmp1_vref See Table 1-194.

Table 1-192. Bit field encoding: BG_VDA_RES_EN_ENUM

Value	Name	Description
1'h0	BG_VDA_RES_EN_VDA	VDA
1'h1	BG_VDA_RES_EN_HALFVDA	VDA/2

Table 1-193. Bit field encoding: BG_VDA_SWABUSL0_ENUM

Value	Name	Description
1'h0	BG_VDA_SWABUSL0_DISCONNECT	not connected
1'h1	BG_VDA_SWABUSL0_CONNECT	Connect VDA Bandgap output to abusl0

Table 1-194. Bit field encoding: CMP_MXVN_ENUM

Value	Name	Description
2'h0	CMP_MXVN_NC	not connected (NC)
2'h1	CMP_MXVN_VDA	Bandgap VREF_VDA output selected
2'h2	CMP_MXVN_CMP1	Bandgap VREF_CMP1 output selected
2'h2	CMP_MXVN_RSVD	Reserved

1.3.359 BG_RSVD

Bandgap Precision Reference Reserved Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BG_RSVD: 0x586D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R							
Retention	NA							
Name	RSVD							

Bits	Name	Description
7:0	RSVD[7:0]	Reserved

1.3.360 CAPSL_CFG0

Capsense Reference Driver Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CAPSL_CFG0: 0x5870

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:00		R/W:0	R/W:00		R/W:0	R/W:0
HW Access	R	NA		R	R		R	R
Retention	RET	NA		RET	RET		RET	RET
Name	mxcmp	RSVD		ch_cont	refsel		boost	out_en

Bits	Name	Description
7	mxcmp	Reference Buffer channel to comparator vp mux select See Table 1-197.
4	ch_cont	Reference Buffer Channel Selection Control See Table 1-196.
3:2	refsel[1:0]	Reference Selection See Table 1-199.
1	boost	High power mode See Table 1-195.
0	out_en	Reference Buffer Output enable See Table 1-198.

Table 1-195. Bit field encoding: CS_BOOST_ENUM

Value	Name	Description
1'b0	CS_BOOST_NORMAL	Normal Drive (typically 10-60pF)
1'b1	CS_BOOST_HIGH	High Drive (typical load = 0.1 to 20nF)

Table 1-196. Bit field encoding: CS_CH_CONT_ENUM

Value	Name	Description
1'b0	CS_CH_CONT_VS	Ch2: Vssa path
1'b1	CS_CH_CONT_AG	Ch1: Analog Global Path

Table 1-197. Bit field encoding: CS_MXCMP_ENUM

Value	Name	Description
1'b0	CS_MXCMP_AG	Analog Global path connected to comparator vp mux (ch1)
1'b1	CS_MXCMP_VS	Vssa path connected to comparator vp mux (ch2)

Table 1-198. Bit field encoding: CS_OUT_EN_ENUM

Value	Name	Description
1'b0	CS_OUT_EN_HIZ	tristate
1'b1	CS_OUT_EN_ON	connected

(continued)

Table 1-199. Bit field encoding: CS_REFSEL_ENUM

Value	Name	Description
2'h0	CS_REFSEL_1P024	1.024 V Bandgap Reference
2'h1	CS_REFSEL_1P2	1.2 V Bandgap Reference
2'h2	CS_REFSEL_TREFSEL1	dac2_vout (left CapSense); dac3_vout (right CapSense)
2'h3	CS_REFSEL_TREFSEL1_ALSO	dac2_vout (left CapSense); dac3_vout (right CapSense)

1.3.361 CAPSL_CFG1

Capsense IO Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CAPSL_CFG1: 0x5871

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:00	
HW Access	NA						R	
Retention	NA						RET	
Name	RSVD						io_ctrl	

Bits	Name	Description
1:0	io_ctrl[1:0]	Capsense Pull-up/Pull-down control See Table 1-200.

Table 1-200. Bit field encoding: CS_IO_CTRL

Value	Name	Description
2'h0	CS_IO_CTRL_DEFAULT	Neither pull-up or pull-down (default)
2'h1	CS_IO_CTRL_PU	Capsense Pull-up mode
2'h2	CS_IO_CTRL_NONE	Neither pull-up or pull-down
2'h3	CS_IO_CTRL_PD	Capsense Pull-down mode

1.3.362 CAPSR_CFG0

Capsense Reference Driver Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CAPSR_CFG0: 0x5872

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:00		R/W:0	R/W:00		R/W:0	R/W:0
HW Access	R	NA		R	R		R	R
Retention	RET	NA		RET	RET		RET	RET
Name	mxcmp	RSVD		ch_cont	refsel		boost	out_en

Bits	Name	Description
7	mxcmp	Reference Buffer channel to comparator vp mux select See Table 1-203.
4	ch_cont	Reference Buffer Channel Selection Control See Table 1-202.
3:2	refsel[1:0]	Reference Selection See Table 1-205.
1	boost	High power mode See Table 1-201.
0	out_en	Reference Buffer Output enable See Table 1-204.

Table 1-201. Bit field encoding: CS_BOOST_ENUM

Value	Name	Description
1'b0	CS_BOOST_NORMAL	Normal Drive (typically 10-60pF)
1'b1	CS_BOOST_HIGH	High Drive (typical load = 0.1 to 20nF)

Table 1-202. Bit field encoding: CS_CH_CONT_ENUM

Value	Name	Description
1'b0	CS_CH_CONT_VS	Ch2: Vssa path
1'b1	CS_CH_CONT_AG	Ch1: Analog Global Path

Table 1-203. Bit field encoding: CS_MXCMP_ENUM

Value	Name	Description
1'b0	CS_MXCMP_AG	Analog Global path connected to comparator vp mux (ch1)
1'b1	CS_MXCMP_VS	Vssa path connected to comparator vp mux (ch2)

Table 1-204. Bit field encoding: CS_OUT_EN_ENUM

Value	Name	Description
1'b0	CS_OUT_EN_HIZ	tristate
1'b1	CS_OUT_EN_ON	connected

(continued)

Table 1-205. Bit field encoding: CS_REFSEL_ENUM

Value	Name	Description
2'h0	CS_REFSEL_1P024	1.024 V Bandgap Reference
2'h1	CS_REFSEL_1P2	1.2 V Bandgap Reference
2'h2	CS_REFSEL_TREFSEL1	dac2_vout (left CapSense); dac3_vout (right CapSense)
2'h3	CS_REFSEL_TREFSEL1_ALSO	dac2_vout (left CapSense); dac3_vout (right CapSense)

1.3.363 CAPSR_CFG1

Capsense IO Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CAPSR_CFG1: 0x5873

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:00	
HW Access	NA						R	
Retention	NA						RET	
Name	RSVD						io_ctrl	

Bits	Name	Description
1:0	io_ctrl[1:0]	Capsense Pull-up/Pull-down control See Table 1-206.

Table 1-206. Bit field encoding: CS_IO_CTRL

Value	Name	Description
2'h0	CS_IO_CTRL_DEFAULT	Neither pull-up or pull-down (default)
2'h1	CS_IO_CTRL_PU	Capsense Pull-up mode
2'h2	CS_IO_CTRL_NONE	Neither pull-up or pull-down
2'h3	CS_IO_CTRL_PD	Capsense Pull-down mode

1.3.364 PUMP_CR0

Pump Configuration Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PUMP_CR0: 0x5876

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:0	R/W:0	NA:0	R/W:0	R/W:0	R/W:0
HW Access	NA	R	R	R	NA	R	R	R
Retention	NA	RET	RET	RET	NA	RET	RET	RET
Name	RSVD	pump_amx_selclk	pump_amx_force	pump_amx_auto	RSVD	pump_ag_selclk	pump_ag_force	pump_ag_auto

Bits	Name	Description
6	pump_amx_selclk	Analog Mux Bus Pump Clock Selection See Table 1-208.
5	pump_amx_force	force pumping - if block enabled enable pump regardless of voltage state
4	pump_amx_auto	enable autopumping - if block enabled pump when low voltage detected
2	pump_ag_selclk	Analog Global Pump Clock Selection See Table 1-207.
1	pump_ag_force	force pumping - if block enabled enable pump regardless of voltage state
0	pump_ag_auto	enable autopumping - if block enabled pump when low voltage detected

Table 1-207. Bit field encoding: PUMP_AG_SELCLK_ENUM

Value	Name	Description
1'b0	PUMP_AG_SELCLK_EXTERNAL	External (DSI) clock selected
1'b1	PUMP_AG_SELCLK_INTERNAL	Pump internal clock selected

Table 1-208. Bit field encoding: PUMP_AMX_SELCLK_ENUM

Value	Name	Description
1'b0	PUMP_AMX_SELCLK_EXTERNAL	External (DSI) clock selected
1'b1	PUMP_AMX_SELCLK_INTERNAL	Pump internal clock selected

1.3.365 PUMP_CR1

Pump Configuration Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PUMP_CR1: 0x5877

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	NA:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	NA	R	R	R
Retention	RET	RET	RET	RET	NA	RET	RET	RET
Name	npump_sc_selclk	npump_opamp_selclk	npump_opamp_force	npump_opamp_auto	RSVD	npump_dsm_selclk	npump_dsm_force	npump_dsm_auto

Bits	Name	Description
7	npump_sc_selclk	Switched Cap Negative Pump Clock Selection See Table 1-211.
6	npump_opamp_selclk	Opamp Negative Pump Clock Selection See Table 1-210.
5	npump_opamp_force	force pumping - if block enabled enable pump regardless of voltage state
4	npump_opamp_auto	enable autopumping - if block enabled pump when low voltage detected
2	npump_dsm_selclk	DSM Negative Pump Clock Selection See Table 1-209.
1	npump_dsm_force	force pumping - if block enabled enable pump regardless of voltage state
0	npump_dsm_auto	enable autopumping - if block enabled pump when low voltage detected

Table 1-209. Bit field encoding: NPUMP_DSM_SELCLK_ENUM

Value	Name	Description
1'b0	NPUMP_DSM_SELCLK_EXTERNAL	External (DSI) clock selected
1'b1	NPUMP_DSM_SELCLK_INTERNAL	Negative pump internal clock selected

Table 1-210. Bit field encoding: NPUMP_OPAMP_SELCLK_ENUM

Value	Name	Description
1'b0	NPUMP_OPAMP_SELCLK_EXTERNAL	External (DSI) clock selected
1'b1	NPUMP_OPAMP_SELCLK_INTERNAL	Negative pump internal clock selected

Table 1-211. Bit field encoding: NPUMP_SC_SELCLK_ENUM

Value	Name	Description
1'b0	NPUMP_SC_SELCLK_EXTERNAL	External (DSI) clock selected

(continued)

Table 1-211. Bit field encoding: NPUMP_SC_SELCLK_ENUM

1'b1	NPUMP_SC_SELCLK_INTERNAL	Negative pump internal clock selected

1.3.366 LPF0_CR0

Low Pass Filter Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LPF0_CR0: 0x5878

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	NA:0	R/W:0	R/W:00	
HW Access	NA		R	R	NA	R	R	
Retention	NA		RET	RET	NA	RET	RET	
Name	RSVD		csel	rsel	RSVD	swout	swin	

Bits	Name	Description
5	csel	Capacitance Selection See Table 1-212.
4	rsel	Resistance Selection See Table 1-213.
2	swout	Output Switch Control See Table 1-215.
1:0	swin[1:0]	Input Switch Control See Table 1-214.

Table 1-212. Bit field encoding: LPF_CSEL_ENUM

Value	Name	Description
1'b0	LPF_CSEL_1X	5pF
1'b1	LPF_CSEL_2X	10pF

Table 1-213. Bit field encoding: LPF_RSEL_ENUM

Value	Name	Description
1'b0	LPF_RSEL_1X	1x; 7 units; 7*29778.62ohms = 0.208 MOhm
1'b1	LPF_RSEL_5X	5x; 35 units; 35*29778.62ohms = 1.04 MOhm

Table 1-214. Bit field encoding: LPF_SWIN_ENUM

Value	Name	Description
2'h0	LPF_SWIN_NC	inputs not connected
2'h1	LPF_SWIN_AG0	Analog Global 0 connected LPF0 (left): AGL0 LPF1 (right): AGR0
2'h2	LPF_SWIN_AMX	Analog Muxbus connected LPF0 (left): AMUXBUSL LPF1 (right): AMUXBUSR
2'h3	LPF_SWIN_BOTH	Both Analog Global and Analog Mux Bus connected (other end of the wire can be disconnected through the port control)

(continued)

Table 1-215. Bit field encoding: LPF_SWOUT_ENUM

Value	Name	Description
1'h0	LPF_SWOUT_NC	LPF output not connected
1'h1	LPF_SWOUT_ABUS0	LPF output connected to Analog local bus 0 LPF0 (left): ABUSL0 LPF1 (right): ABUSR0

1.3.367 LPF0_RSVD

LPF Reserved

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LPF0_RSVD: 0x5879

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R							
Retention	NA							
Name	RSVD							

Bits	Name	Description
7:0	RSVD[7:0]	Reserved

1.3.368 LPF1_CR0

Low Pass Filter Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LPF1_CR0: 0x587A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	NA:0	R/W:0	R/W:00	
HW Access	NA		R	R	NA	R	R	
Retention	NA		RET	RET	NA	RET	RET	
Name	RSVD		csel	rsel	RSVD	swout	swin	

Bits	Name	Description
5	csel	Capacitance Selection See Table 1-216.
4	rsel	Resistance Selection See Table 1-217.
2	swout	Output Switch Control See Table 1-219.
1:0	swin[1:0]	Input Switch Control See Table 1-218.

Table 1-216. Bit field encoding: LPF_CSEL_ENUM

Value	Name	Description
1'b0	LPF_CSEL_1X	5pF
1'b1	LPF_CSEL_2X	10pF

Table 1-217. Bit field encoding: LPF_RSEL_ENUM

Value	Name	Description
1'b0	LPF_RSEL_1X	1x; 7 units; 7*29778.62ohms = 0.208 MOhm
1'b1	LPF_RSEL_5X	5x; 35 units; 35*29778.62ohms = 1.04 MOhm

Table 1-218. Bit field encoding: LPF_SWIN_ENUM

Value	Name	Description
2'h0	LPF_SWIN_NC	inputs not connected
2'h1	LPF_SWIN_AG0	Analog Global 0 connected LPF0 (left): AGL0 LPF1 (right): AGR0
2'h2	LPF_SWIN_AMX	Analog Muxbus connected LPF0 (left): AMUXBUSL LPF1 (right): AMUXBUSR
2'h3	LPF_SWIN_BOTH	Both Analog Global and Analog Mux Bus connected (other end of the wire can be disconnected through the port control)

(continued)

Table 1-219. Bit field encoding: LPF_SWOUT_ENUM

Value	Name	Description
1'h0	LPF_SWOUT_NC	LPF output not connected
1'h1	LPF_SWOUT_ABUS0	LPF output connected to Analog local bus 0 LPF0 (left): ABUSL0 LPF1 (right): ABUSR0

1.3.369 LPF1_RSVD

LPF Reserved

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LPF1_RSVD: 0x587B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R							
Retention	NA							
Name	RSVD							

Bits	Name	Description
7:0	RSVD[7:0]	Reserved

1.3.370 ANAIF_CFG_MISC_CR0

MISC Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

ANAIF_CFG_MISC_CR0: 0x587C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Retention	NA							RET
Name	RSVD							enpdb

Bits	Name	Description
0	enpdb	Analog Switch Enable Pull Down Bar (active low enable) - if enabled, all unused/opened analog routing switches will have their center nodes pulled down See Table 1-220.

Table 1-220. Bit field encoding: ENPDB_ENUM

Value	Name	Description
1'b0	ENPDB_ENABLE	Enable analog switch pulldown
1'b1	ENPDB_DISABLE	Disable analog switch pulldown

1.3.371 DSM[0..0]_CR0

Delta Sigma Modulator Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR0: 0x5880

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:00		R/W:00	
HW Access	NA				R		R	
Retention	NA				RET		RET	
Name	RSVD				nonov		qlev	

Bits	Name	Description
3:2	nonov[1:0]	Non overlap delay of clock phases See Table 1-221.
1:0	qlev[1:0]	Quantization Level choice for modulator See Table 1-222.

Table 1-221. Bit field encoding: NONOV_ENUM

Value	Name	Description
2'h0	NONOV_LOW	low (1.57ns, typ)
2'h1	NONOV_MEDIUM	medium (3.54ns, typ)
2'h2	NONOV_HIGH	high (6.47ns, typ)
2'h3	NONOV_VERYHIGH	very high (9.91ns, typ)

Table 1-222. Bit field encoding: QLEV_ENUM

Value	Name	Description
2'b00	QLEV_2	2 level quantization
2'b01	QLEV_3	3 level quantization
2'b10	QLEV_9	9 level quantization
2'b11	QLEV_9_ALSO	9 level quantization

1.3.372 DSM[0..0]_CR1

Delta Sigma Modulator Control Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR1: 0x5881

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:0	R/W:00000				
HW Access	NA	R	R	R				
Retention	NA	RET	RET	RET				
Name	RSVD	dpmode	oden	odet_th				

Bits	Name	Description
6	dpmode	Datapath mode See Table 1-223.
5	oden	Overload detect scheme enable
4:0	odet_th[4:0]	Overload detection threshold. If the number of continuous 1s or 0s coming out of quantizer exceeds this number overload detection flag is set

Table 1-223. Bit field encoding: DPMODE_ENUM

Value	Name	Description
1'h0	DPMODE_NORMAL	normal
1'h1	DPMODE_LOWOFFSET	low offset

1.3.373 DSM[0..0]_CR2

Delta Sigma Modulator Control Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR2: 0x5882

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:000		
HW Access	R	R	R	R	R	R		
Retention	RET	RET	RET	RET	RET	RET		
Name	mx_reset	reset3_en	reset2_en	reset1_en	mod_chop_en	fchop		

Bits	Name	Description
7	mx_reset	select DSM reset source See Table 1-225.
6	reset3_en	allow third stage integrating capacitance to be reset See Table 1-228.
5	reset2_en	allow second stage integrating capacitance to be reset See Table 1-227.
4	reset1_en	Allow first stage integrating capacitance to be reset See Table 1-226.
3	mod_chop_en	Enable Modulator Chopping
2:0	fchop[2:0]	Chopping Frequency Selection. The Fclock is samply frequency clock See Table 1-224.

Table 1-224. Bit field encoding: FCHOP_ENUM

Value	Name	Description
3'h0	FCHOP_DIV2	Fclock/2
3'h1	FCHOP_DIV4	Fclock/4
3'h2	FCHOP_DIV8	Fclock/8
3'h3	FCHOP_DIV16	Fclock/16
3'h4	FCHOP_DIV32	Fclock/32
3'h5	FCHOP_DIV64	Fclock/64
3'h6	FCHOP_DIV128	Fclock/128
3'h7	FCHOP_DIV256	Fclock/256

Table 1-225. Bit field encoding: MXSELRESET_ENUM

Value	Name	Description
1'b0	MXSELRESET_0	Select Decimator for reset source
1'b1	MXSELRESET_1	Select UDB for reset source

(continued)

Table 1-226. Bit field encoding: RESET1_EN_ENUM

Value	Name	Description
1'b0	RESET1_EN_DISABLE	First stage integrating capacitance cannot be reset (use when in overload, to allow for first order operation)
1'b1	RESET1_EN_ENABLE	First stage integrating capacitance can be reset

Table 1-227. Bit field encoding: RESET2_EN_ENUM

Value	Name	Description
1'b0	RESET2_EN_DISABLE	second stage integrating capacitance cannot be reset (use when in overload, to allow for second order operation, assuming the reset1_en bit is also cleared
1'b1	RESET2_EN_ENABLE	second stage integrating capacitance can be reset

Table 1-228. Bit field encoding: RESET3_EN_ENUM

Value	Name	Description
1'b0	RESET3_EN_DISABLE	third stage integrating capacitance cannot be reset (use only for debug purposes)
1'b1	RESET3_EN_ENABLE	third stage integrating capacitance can be reset

1.3.374 DSM[0..0]_CR3

Delta Sigma Modulator Control Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR3: 0x5883

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:0	R/W:0	R/W:0	R/W:0000			
HW Access	R	NA	R	R	R			
Retention	RET	NA	RET	RET	RET			
Name	sign	RSVD	mx_dout	modbitin_en	mx_modbitin			

Bits	Name	Description
7	sign	Invert sign of input See Table 1-232.
5	mx_dout	Select DSM dout routed to UDB See Table 1-230.
4	modbitin_en	modbitin enable See Table 1-229.
3:0	mx_modbitin[3:0]	Select modbitin input See Table 1-231.

Table 1-229. Bit field encoding: MODBITIN_EN_ENUM

Value	Name	Description
1'b0	MODBITIN_EN_DISABLE	Do not allow modbit input to be mixed with modulator input
1'b1	MODBITIN_EN_ENABLE	Allow modbit input to be mixed with modulator input

Table 1-230. Bit field encoding: MX_DOUT_ENUM

Value	Name	Description
1'b0	MX_DOUT_8BIT	Select reg OUT0=dout[7:0] (synced; w/o post processing)
1'b1	MX_DOUT_2SCOMP	Select reg OUT1={2'b0,ovdcause,ovdflag,dout2scomp} (synced; overload cause, overload flag, dout 2s complement

Table 1-231. Bit field encoding: MX_MODBITIN_ENUM

Value	Name	Description
4'h0	MX_MODBITIN_LUT0	lut0_out
4'h1	MX_MODBITIN_LUT1	lut1_out
4'h2	MX_MODBITIN_LUT2	lut2_out
4'h3	MX_MODBITIN_LUT3	lut3_out
4'h4	MX_MODBITIN_LUT4	lut4_out (doesn't exist on Leopard, tied to 0)
4'h5	MX_MODBITIN_LUT5	lut5_out (doesn't exist on Leopard, tied to 0)
4'h6	MX_MODBITIN_LUT6	lut6_out (doesn't exist on Leopard, tied to 0)
4'h7	MX_MODBITIN_LUT7	lut7_out (doesn't exist on Leopard, tied to 0)

(continued)

Table 1-231. Bit field encoding: MX_MODBITIN_ENUM

4'h8	MX_MODBITIN_UDB	UDB
4'h9	MX_MODBITIN_CONST 1	constant 1
4'ha	MX_MODBITIN_CONST 0	constant 0
4'hb	MX_MODBITIN_0xB_RSVD	Reserved
4'hc	MX_MODBITIN_0xC_RSVD	Reserved
4'hd	MX_MODBITIN_0xD_RSVD	Reserved
4'he	MX_MODBITIN_0xE_RSVD	Reserved
4'hf	MX_MODBITIN_0xF_RSVD	Reserved

Table 1-232. Bit field encoding: SIGN_ENUM

Value	Name	Description
1'b0	SIGN_NONINVERT	keep original polarity for the input
1'b1	SIGN_INVERT	Invert sign of input (use when trying to chop once and then average the offset value out)

1.3.375 DSM[0..0]_CR4

Delta Sigma Modulator Control Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR4: 0x5884

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0000000						
HW Access	R	R						
Retention	RET	RET						
Name	fcap1_en	fcap1						

Bits	Name	Description
7	fcap1_en	Enable/Disable Capacitance path meant for DFT (Design for Testability) of the first integrator's integrating capacitance path See Table 1-234.
6:0	fcap1[6:0]	binary weighted first stage integrating capacitance See Table 1-233.

Table 1-233. Bit field encoding: FCAP1_ENUM

Value	Name	Description
7'b0	FCAP1_MIN	0 fF
7'b1111111	FCAP1_MAX	Max Value = 12.7 pF
7'b0000001	FCAP1_BIT0	fcap[0] set -> +100 fF
7'b0000010	FCAP1_BIT1	fcap[1] set -> +200 fF
7'b0000100	FCAP1_BIT2	fcap[2] set -> +400 fF
7'b0001000	FCAP1_BIT3	fcap[3] set -> +800 fF
7'b0010000	FCAP1_BIT4	fcap[4] set -> +1600 fF
7'b0100000	FCAP1_BIT5	fcap[5] set -> +3200 fF
7'b1000000	FCAP1_BIT6	fcap[6] set -> +6400 fF

Table 1-234. Bit field encoding: FCAP1_EN_ENUM

Value	Name	Description
1'h0	FCAP1_EN_DISABLE	Disable the DFT 100fF capacitance path
1'h1	FCAP1_EN_ENABLE	Enable the DFT 100fF capacitance path

1.3.376 DSM[0..0]_CR5

Delta Sigma Modulator Control Register 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR5: 0x5885

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0000000						
HW Access	R	R						
Retention	RET	RET						
Name	ipcap1_en	ipcap1						

Bits	Name	Description
7	ipcap1_en	Enable/Disable Capacitance path meant for DFT (Design for Testability) of the first integrator's input sampling path See Table 1-236.
6:0	ipcap1[6:0]	Binary weighted first stage integrating capacitance See Table 1-235.

Table 1-235. Bit field encoding: IPCAP1_ENUM

Value	Name	Description
7'b0	IPCAP1_MIN	0 fF
7'b1111111	IPCAP1_MAX	Max Value = 12.688 pF
7'b0000001	IPCAP1_BIT0	ipcap1[0] set -> +96 fF
7'b0000010	IPCAP1_BIT1	ipcap1[1] set -> +192 fF
7'b0000100	IPCAP1_BIT2	ipcap1[2] set -> +400 fF
7'b0001000	IPCAP1_BIT3	ipcap1[3] set -> +800 fF
7'b0010000	IPCAP1_BIT4	ipcap1[4] set -> +1600 fF
7'b0100000	IPCAP1_BIT5	ipcap1[5] set -> +3200 fF
7'b1000000	IPCAP1_BIT6	ipcap1[6] set -> +6400 fF

Table 1-236. Bit field encoding: IPCAP1_EN_ENUM

Value	Name	Description
1'h0	IPCAP1_EN_DISABLE	Disable the DFT 96fF capacitance path
1'h1	IPCAP1_EN_ENABLE	Enable the DFT 96fF capacitance path

1.3.377 DSM[0..0]_CR6

Delta Sigma Modulator Control Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR6: 0x5886

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:000000					
HW Access	NA	R	R					
Retention	NA	RET	RET					
Name	RSVD	daccap_en	daccap					

Bits	Name	Description
6	daccap_en	Enable/Disable Capacitance path meant for DFT (Design for Testability) of the DAC Reference sampling path See Table 1-238.
5:0	daccap[5:0]	Binary weighted first stage DAC capacitance See Table 1-237.

Table 1-237. Bit field encoding: DACCAP_ENUM

Value	Name	Description
6'b000001	DACCAP_BIT0	daccap[0] set -> add 12*8= +96 fF
6'b000010	DACCAP_BIT1	daccap[1] set -> add 24*8= +192 fF
6'b000100	DACCAP_BIT2	daccap[2] set -> add 50*8= +400 fF
6'b001000	DACCAP_BIT3	daccap[3] set -> add 100*8= +800 fF
6'b010000	DACCAP_BIT4	daccap[4] set -> add 200*8= +1600 fF
6'b100000	DACCAP_BIT5	daccap[5] set -> add 400*8= +3200 fF

Table 1-238. Bit field encoding: DACCAP_EN_ENUM

Value	Name	Description
1'h0	DACCAP_EN_DISABLE	Disable the DFT 12fF capacitance path
1'h1	DACCAP_EN_ENABLE	Enable the DFT 12fF capacitance path

1.3.378 DSM[0..0]_CR7

Delta Sigma Modulator Control Register 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR7: 0x5887

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	NA:0	NA:000		
HW Access	R	R	R	R	NA	NA		
Retention	RET	RET	RET	RET	NA	NA		
Name	fcap2_en	fcap3_en	ipcap1offset	fcap1offset	RSVD	RSVD		

Bits	Name	Description
7	fcap2_en	Enable/Disable additional 50fF capacitance path in the second integrators integrating capacitance path See Table 1-240.
6	fcap3_en	Enable/Disable additonal capacitance path in the third integrator's integrating capacitance path See Table 1-241.
5	ipcap1offset	Offset capacitance for the input sampling capacitance in the first stage integrator See Table 1-242.
4	fcap1offset	Offset Capacitance for the integrating capacitance in the first stage integrator See Table 1-239.

Table 1-239. Bit field encoding: FCAP1OFFSET_ENUM

Value	Name	Description
1'b0	FCAP1OFFSET_0	Don't add offset capacitance
1'b1	FCAP1OFFSET_1	Add offset capacitance of 3.4 pF

Table 1-240. Bit field encoding: FCAP2_EN_ENUM

Value	Name	Description
1'h0	FCAP2_EN_DISABLE	Disable the additonal 50fF capacitance path
1'h1	FCAP2_EN_ENABLE	Enable the additonal 50fF capacitance path

Table 1-241. Bit field encoding: FCAP3_EN_ENUM

Value	Name	Description
1'h0	FCAP3_EN_DISABLE	Disable the additonal 100fF capacitance path
1'h1	FCAP3_EN_ENABLE	Enable the 100fF capacitance path

Table 1-242. Bit field encoding: IPCAP1OFFSET_ENUM

Value	Name	Description
1'b0	IPCAP1OFFSET_0	Don't add offset capacitance
1'b1	IPCAP1OFFSET_1	Add offset capacitance of 4.8 pF

1.3.379 DSM[0..0]_CR8

Delta Sigma Modulator Control Register 8

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR8: 0x5888

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:000			R/W:0000			
HW Access	R	R			R			
Retention	RET	RET			RET			
Name	ipcap2_en	ipcap2			fcap2			

Bits	Name	Description
7	ipcap2_en	Enable/Disable additional 50fF capacitance path in the second integrator's input sampling path See Table 1-245.
6:4	ipcap2[2:0]	The second integrator's input sampling capacitance (0-350fF, 50fF step) See Table 1-244.
3:0	fcap2[3:0]	The second stage integrating capacitance (0-750fF, 50fF step) See Table 1-243.

Table 1-243. Bit field encoding: FCAP2_ENUM

Value	Name	Description
4'h0	FCAP2_0FEMPTO	0fF
4'h1	FCAP2_50FEMPTO	50fF
4'h2	FCAP2_100FEMPTO	100fF
4'h3	FCAP2_150FEMPTO	150fF
4'h4	FCAP2_200FEMPTO	200fF
4'h5	FCAP2_250FEMPTO	250fF
4'h6	FCAP2_300FEMPTO	300fF
4'h7	FCAP2_350FEMPTO	350fF
4'h8	FCAP2_400FEMPTO	400fF
4'h9	FCAP2_450FEMPTO	450fF
4'ha	FCAP2_500FEMPTO	500fF
4'hb	FCAP2_550FEMPTO	550fF
4'hc	FCAP2_600FEMPTO	600fF
4'hd	FCAP2_650FEMPTO	650fF
4'he	FCAP2_700FEMPTO	700fF
4'hf	FCAP2_750FEMPTO	750fF

Table 1-244. Bit field encoding: IPCAP2_ENUM

Value	Name	Description
3'h0	IPCAP2_0FEMPTO	0fF
3'h1	IPCAP2_50FEMPTO	50fF
3'h2	IPCAP2_100FEMPTO	100fF
3'h3	IPCAP2_150FEMPTO	150fF
3'h4	IPCAP2_200FEMPTO	200fF
3'h5	IPCAP2_250FEMPTO	250fF

(continued)

Table 1-244. Bit field encoding: IPCAP2_ENUM

3'h6	IPCAP2_300FEMPTO	300fF
3'h7	IPCAP2_350FEMPTO	350fF

Table 1-245. Bit field encoding: IPCAP2_EN_ENUM

Value	Name	Description
1'h0	IPCAP2_EN_DISABLE	Disable the additonal 50fF capacitance path
1'h1	IPCAP2_EN_ENABLE	Enable the additonal 50fF capacitance path

1.3.380 DSM[0..0]_CR9

Delta Sigma Modulator Control Register 9

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR9: 0x5889

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:000			R/W:0000			
HW Access	R	R			R			
Retention	RET	RET			RET			
Name	ipcap3_en	ipcap3			fcap3			

Bits	Name	Description
7	ipcap3_en	Enable/Disable additional 50fF capacitance path in the third integrator's input sampling path See Table 1-248.
6:4	ipcap3[2:0]	The third integrator's input sampling capacitance (0-350fF in 50fF step) See Table 1-247.
3:0	fcap3[3:0]	The third stage integrating capacitance (0-750fF, 50fF step) See Table 1-246.

Table 1-246. Bit field encoding: FCAP3_ENUM

Value	Name	Description
4'h0	FCAP3_0FEMPTO	0fF
4'h1	FCAP3_100FEMPTO	100fF
4'h2	FCAP3_200FEMPTO	200fF
4'h3	FCAP3_300FEMPTO	300fF
4'h4	FCAP3_400FEMPTO	400fF
4'h5	FCAP3_500FEMPTO	500fF
4'h6	FCAP3_600FEMPTO	600fF
4'h7	FCAP3_700FEMPTO	700fF
4'h8	FCAP3_800FEMPTO	800fF
4'h9	FCAP3_900FEMPTO	900fF
4'ha	FCAP3_1000FEMPTO	1000fF
4'hb	FCAP3_1100FEMPTO	1100fF
4'hc	FCAP3_1200FEMPTO	1200fF
4'hd	FCAP3_1300FEMPTO	1300fF
4'he	FCAP3_1400FEMPTO	1400fF
4'hf	FCAP3_1500FEMPTO	1500fF

Table 1-247. Bit field encoding: IPCAP3_ENUM

Value	Name	Description
3'h0	IPCAP3_0FEMPTO	0fF
3'h1	IPCAP3_50FEMPTO	50fF
3'h2	IPCAP3_100FEMPTO	100fF
3'h3	IPCAP3_150FEMPTO	150fF
3'h4	IPCAP3_200FEMPTO	200fF
3'h5	IPCAP3_250FEMPTO	250fF

(continued)

Table 1-247. Bit field encoding: IPCAP3_ENUM

3'h6	IPCAP3_300FEMPTO	300fF
3'h7	IPCAP3_350FEMPTO	350fF

Table 1-248. Bit field encoding: IPCAP3_EN_ENUM

Value	Name	Description
1'h0	IPCAP3_EN_DISABLE	Disable the additonal 50fF capacitance path
1'h1	IPCAP3_EN_ENABLE	Enable the additonal 50fF capacitance path

1.3.381 DSM[0..0]_CR10

Delta Sigma Modulator Control Register 10

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR10: 0x588A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:000			R/W:0	R/W:000		
HW Access	R	R			R	R		
Retention	RET	RET			RET	RET		
Name	sumcap1_en	sumcap1			sumcap2_en	sumcap2		

Bits	Name	Description
7	sumcap1_en	Enabling/Disabling the the additional 50fF capacitance path that lies between first integrator output and summer input (feed-forward) path See Table 1-250.
6:4	sumcap1[2:0]	The summer capacitance that lies on the feed-forward path from the first integrator output (0fF to 350fF in 50fF step) See Table 1-249.
3	sumcap2_en	Enabling/Disabling the additional 50fF capacitance path that lies between the second integrator output and summer input (feed-forward) path See Table 1-252.
2:0	sumcap2[2:0]	The summer capacitance that lies on the feed-forward path from the second integrator output (0fF to 350fF in 50fF step See Table 1-251.

Table 1-249. Bit field encoding: SUMCAP1_ENUM

Value	Name	Description
3'h0	SUMCAP1_0FEMPTO	0fF
3'h1	SUMCAP1_50FEMPTO	50fF
3'h2	SUMCAP1_100FEMPTO	100fF
3'h3	SUMCAP1_150FEMPTO	150fF
3'h4	SUMCAP1_200FEMPTO	200fF
3'h5	SUMCAP1_250FEMPTO	250fF
3'h6	SUMCAP1_300FEMPTO	300fF
3'h7	SUMCAP1_350FEMPTO	350fF

(continued)

Table 1-250. Bit field encoding: SUMCAP1_EN_ENUM

Value	Name	Description
1'h0	SUMCAP1_EN_DISABLE	Disable the additonal 50fF capacitance path
1'h1	SUMCAP1_EN_ENABLE	Enable the additonal 50fF capacitance path

Table 1-251. Bit field encoding: SUMCAP2_ENUM

Value	Name	Description
3'h0	SUMCAP2_0FEMPTO	0fF
3'h1	SUMCAP2_50FEMPTO	50fF
3'h2	SUMCAP2_100FEMPTO	100fF
3'h3	SUMCAP2_150FEMPTO	150fF
3'h4	SUMCAP2_200FEMPTO	200fF
3'h5	SUMCAP2_250FEMPTO	250fF
3'h6	SUMCAP2_300FEMPTO	300fF
3'h7	SUMCAP2_350FEMPTO	350fF

Table 1-252. Bit field encoding: SUMCAP2_EN_ENUM

Value	Name	Description
1'h0	SUMCAP2_EN_DISABLE	Disable the additonal 50fF capacitance path
1'h1	SUMCAP2_EN_ENABLE	Enable the additonal 50fF capacitance path

1.3.382 DSM[0..0]_CR11

Delta Sigma Modulator Control Register 11

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR11: 0x588B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:000			R/W:0000			
HW Access	R	R			R			
Retention	RET	RET			RET			
Name	sumcap3_en	sumcap3			sumcapfb			

Bits	Name	Description
7	sumcap3_en	Enabling/Disabling the additional 50fF path that lies between the third integrator output and summer input (feed-forward) path See Table 1-254.
6:4	sumcap3[2:0]	The summer capacitance that lies on the feed-forward path from the third integrator output (0fF to 350fF in 50fF step See Table 1-253.
3:0	sumcapfb[3:0]	The summer feedback capacitance (0fF to 750F in 50fF step) See Table 1-255.

Table 1-253. Bit field encoding: SUMCAP3_ENUM

Value	Name	Description
3'h0	SUMCAP3_0FEMPTO	0fF
3'h1	SUMCAP3_50FEMPTO	50fF
3'h2	SUMCAP3_100FEMPTO	100fF
3'h3	SUMCAP3_150FEMPTO	150fF
3'h4	SUMCAP3_200FEMPTO	200fF
3'h5	SUMCAP3_250FEMPTO	250fF
3'h6	SUMCAP3_300FEMPTO	300fF
3'h7	SUMCAP3_350FEMPTO	350fF

Table 1-254. Bit field encoding: SUMCAP3_EN_ENUM

Value	Name	Description
1'h0	SUMCAP3_EN_DISABLE	Disable the additional 50fF capacitance path
1'h1	SUMCAP3_EN_ENABLE	Enable the additonal 50fF capacitance path

(continued)

Table 1-255. Bit field encoding: SUMCAPFB_ENUM

Value	Name	Description
4'h0	SUMCAPFB_0FEMPTO	0fF
4'h1	SUMCAPFB_50FEMPTO	50fF
4'h2	SUMCAPFB_100FEMPTO	100fF
4'h3	SUMCAPFB_150FEMPTO	150fF
4'h4	SUMCAPFB_200FEMPTO	200fF
4'h5	SUMCAPFB_250FEMPTO	250fF
4'h6	SUMCAPFB_300FEMPTO	300fF
4'h7	SUMCAPFB_350FEMPTO	350fF
4'h8	SUMCAPFB_400FEMPTO	400fF
4'h9	SUMCAPFB_450FEMPTO	450fF
4'ha	SUMCAPFB_500FEMPTO	500fF
4'hb	SUMCAPFB_550FEMPTO	550fF
4'hc	SUMCAPFB_600FEMPTO	600fF
4'hd	SUMCAPFB_650FEMPTO	650fF
4'he	SUMCAPFB_700FEMPTO	700fF
4'hf	SUMCAPFB_750FEMPTO	750fF

1.3.383 DSM[0..0]_CR12

Delta Sigma Modulator Control Register 12

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR12: 0x588C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:0	R/W:00000				
HW Access	NA	R	R	R				
Retention	NA	RET	RET	RET				
Name	RSVD	sumcapfb_en	sumcapin_en	sumcapin				

Bits	Name	Description
6	sumcapfb_en	Enabling/Disabling the DFT path that lies on the feedback path of the active summer See Table 1-256.
5	sumcapin_en	Enabling/Disabling the DFT path that lies between input of the sigma delta modulator and the summer input. See Table 1-258.
4:0	sumcapin[4:0]	The summer capacitance that lies on the path where the input signal is summed (50fF to 1.6pF in 50fF step) See Table 1-257.

Table 1-256. Bit field encoding: SUMCAPFB_EN_ENUM

Value	Name	Description
1'h0	SUMCAPFB_EN_DISABLE	Disable the DFT 50fF capacitance path
1'h1	SUMCAPFB_EN_ENABLE	Enable the DFT 50fF capacitance path

Table 1-257. Bit field encoding: SUMCAPIN_ENUM

Value	Name	Description
5'h00	SUMCAPIN_0FEMPTO	0fF
5'h01	SUMCAPIN_50FEMPTO	50fF
5'h02	SUMCAPIN_100FEMPTO	100fF
5'h03	SUMCAPIN_150FEMPTO	150fF
5'h04	SUMCAPIN_200FEMPTO	200fF
5'h05	SUMCAPIN_250FEMPTO	250fF
5'h06	SUMCAPIN_300FEMPTO	300fF
5'h07	SUMCAPIN_350FEMPTO	350fF

(continued)

Table 1-257. Bit field encoding: SUMCAPIN_ENUM

5'h08	SUMCAPIN_400FEMPTO	400fF
5'h09	SUMCAPIN_450FEMPTO	450fF
5'h0a	SUMCAPIN_500FEMPTO	500fF
5'h0b	SUMCAPIN_550FEMPTO	550fF
5'h0c	SUMCAPIN_600FEMPTO	600fF
5'h0d	SUMCAPIN_650FEMPTO	650fF
5'h0e	SUMCAPIN_700FEMPTO	700fF
5'h0f	SUMCAPIN_750FEMPTO	750fF
5'h10	SUMCAPIN_800FEMPTO	800fF
5'h11	SUMCAPIN_850FEMPTO	850fF
5'h12	SUMCAPIN_900FEMPTO	900fF
5'h13	SUMCAPIN_950FEMPTO	950fF
5'h14	SUMCAPIN_1000FEMPTO	1000fF
5'h15	SUMCAPIN_1050FEMPTO	1050fF
5'h16	SUMCAPIN_1100FEMPTO	1100fF
5'h17	SUMCAPIN_1150FEMPTO	1150fF
5'h18	SUMCAPIN_1200FEMPTO	1200fF
5'h19	SUMCAPIN_1250FEMPTO	1250fF
5'h1a	SUMCAPIN_1300FEMPTO	1300fF
5'h1b	SUMCAPIN_1350FEMPTO	1350fF
5'h1c	SUMCAPIN_1400FEMPTO	1400fF
5'h1d	SUMCAPIN_1450FEMPTO	1450fF
5'h1e	SUMCAPIN_1500FEMPTO	1500fF
5'h1f	SUMCAPIN_1550FEMPTO	1550fF

Table 1-258. Bit field encoding: SUMCAPIN_EN_ENUM

Value	Name	Description
1'h0	SUMCAPIN_EN_DISABLE	Disable the DFT 50fF capacitance path
1'h1	SUMCAPIN_EN_ENABLE	Enable the DFT 50fF capacitance path

1.3.384 DSM[0..0]_CR13

Delta Sigma Modulator Control Register 13

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR13: 0x588D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R							
Retention	NA							
Name	RSVD							

Bits	Name	Description
7:0	RSVD[7:0]	Reserved

1.3.385 DSM[0..0]_CR14

Delta Sigma Modulator Control Register 14

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR14: 0x588E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0000				NA:0	R/W:000		
HW Access	R				NA	R		
Retention	RET				NA	RET		
Name	opamp1_bw				RSVD	power1		

Bits	Name	Description
7:4	opamp1_bw[3:0]	First Stage Opamp Bandwidth Control (Risk Mitigation not for User control). Table gives value for Modulator input bw[3:0] See Table 1-259.
2:0	power1[2:0]	First Stage Opamp Power level control See Table 1-260.

Table 1-259. Bit field encoding: OPAMP1_BW_ENUM

Value	Name	Description
4'h0	OPAMP1_BW_0x0	(default)
4'h1	OPAMP1_BW_0x1	(used with 1.5X power)
4'h2	OPAMP1_BW_0x2	reserved
4'h3	OPAMP1_BW_0x3	(used with 2X power)
4'h4	OPAMP1_BW_0x4	reserved
4'h5	OPAMP1_BW_0x5	reserved
4'h6	OPAMP1_BW_0x6	reserved
4'h7	OPAMP1_BW_0x7	(used with 2.5X power)
4'h8	OPAMP1_BW_0x8	(higher BW, 1.25X power)
4'h9	OPAMP1_BW_0x9	(lower noise)
4'ha	OPAMP1_BW_0xA	reserved
4'hb	OPAMP1_BW_0xB	reserved
4'hc	OPAMP1_BW_0xC	reserved
4'hd	OPAMP1_BW_0xD	reserved
4'he	OPAMP1_BW_0xE	reserved
4'hf	OPAMP1_BW_0xF	reserved

Table 1-260. Bit field encoding: POWER1_ENUM

Value	Name	Description
3'h0	POWER1_0	Low (44uA)
3'h1	POWER1_1	Medium (123uA)
3'h2	POWER1_2	High (492uA)
3'h3	POWER1_3	1.5X (750uA)
3'h4	POWER1_4	2X (1mA)
3'h5	POWER1_5	C/2 @ 3MSPS (277uA)
3'h6	POWER1_6	C/4 @ 3MSPS (185uA)
3'h7	POWER1_7	2.5X (1.5mA)

1.3.386 DSM[0..0]_CR15

Delta Sigma Modulator Control Register 15

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR15: 0x588F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:00		NA:0	R/W:000		
HW Access	NA		R		NA	R		
Retention	NA		RET		NA	RET		
Name	RSVD		power_comp		RSVD	power2_3		

Bits	Name	Description
5:4	power_comp[1:0]	The power control for the quantizer block See Table 1-262.
2:0	power2_3[2:0]	The power control for the second and third integrator stages See Table 1-261.

Table 1-261. Bit field encoding: POWER2_3_ENUM

Value	Name	Description
3'h0	POWER2_3_LOW	LOW (4uA)
3'h1	POWER2_3_MEDIUM	MEDIUM (17uA)
3'h2	POWER2_3_HIGH	HIGH (68uA)
3'h3	POWER2_3_1P5X	1.5X (100uA)
3'h4	POWER2_3_2X	2X (135uA)
3'h5	POWER2_3_HIGH_5	HIGH (68uA)
3'h6	POWER2_3_HIGH_6	HIGH (68uA)
3'h7	POWER2_3_HIGH_7	HIGH (68uA)

Table 1-262. Bit field encoding: POWER_COMP_ENUM

Value	Name	Description
2'h0	POWER_COMP_VERYLOW	very low (2.2uA)
2'h1	POWER_COMP_NORMAL	Normal (8.6uA)
2'h2	POWER_COMP_6MHZ	6MHz (17uA)
2'h3	POWER_COMP_12MHZ	12MHz (35uA)

1.3.387 DSM[0..0]_CR16

Delta Sigma Modulator Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR16: 0x5890

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:000			R/W:0	R/W:000		
HW Access	NA	R			R	R		
Retention	NA	RET			RET	RET		
Name	RSVD	power_sum			en_cp	cp_pwrctl		

Bits	Name	Description
6:4	power_sum[2:0]	The power control for the summer block See Table 1-264.
3	en_cp	Enable charge pump
2:0	cp_pwrctl[2:0]	Charge Pump Power Control Modes See Table 1-263.

Table 1-263. Bit field encoding: CP_PWRCTL_ENUM

Value	Name	Description
3'h0	CP_PWRCTL_TURBO	Charge pump operating in Turbo Power (560uA) mode
3'h1	CP_PWRCTL_2X	Charge pump operating in 6MHz (300uA) mode
3'h2	CP_PWRCTL_HIGH	Charge pump operating in High power (170uA) mode
3'h3	CP_PWRCTL_MEDIUM	Charge pump operating in Medium power (70uA) mode
3'h4	CP_PWRCTL_LOW	Charge pump operating in Low Power (30uA) mode
3'h5	CP_PWRCTL_5	Reserved
3'h6	CP_PWRCTL_6	Reserved
3'h7	CP_PWRCTL_7	Reserved

Table 1-264. Bit field encoding: POWER_SUM_ENUM

Value	Name	Description
3'h0	POWER_SUM_LOW	LOW (4uA)
3'h1	POWER_SUM_MEDIUM	MEDIUM (17uA)
3'h2	POWER_SUM_HIGH	HIGH (68uA)
3'h3	POWER_SUM_1P5X	1.5X (100uA)
3'h4	POWER_SUM_2X	2X (135uA)
3'h5	POWER_SUM_HIGH_5	HIGH (68uA)
3'h6	POWER_SUM_HIGH_6	HIGH (68uA)
3'h7	POWER_SUM_HIGH_7	HIGH (68uA)

1.3.388 DSM[0..0]_CR17

Delta Sigma Modulator Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CR17: 0x5891

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00		R/W:00		R/W:00		R/W:0	R/W:0
HW Access	R		R		R		R	R
Retention	RET		RET		RET		RET	RET
Name	pwr_ctrl_vref_inn		pwr_ctrl_vcm		pwr_ctrl_vref		en_buf_vcm	en_buf_vref

Bits	Name	Description
7:6	pwr_ctrl_vref_inn[1:0]	Power control modes for REFBUF1 (the reference buffer that connects ADC reference to the negative input MUX of the channel) See Table 1-269.
5:4	pwr_ctrl_vcm[1:0]	Power Control for the Voltage Common Mode Buffer for the Sigma Delta ADC See Table 1-267.
3:2	pwr_ctrl_vref[1:0]	Power Control for the Voltage Reference Buffer for the Sigma Delta ADC See Table 1-268.
1	en_buf_vcm	Enable/Disable control for ADC (Internal)Reference Buffer See Table 1-265.
0	en_buf_vref	Enable/Disable control for ADC (Internal)Reference Buffer See Table 1-266.

Table 1-265. Bit field encoding: EN_BUF_VCM_ENUM

Value	Name	Description
1'h0	EN_BUF_VCM_0	The ADC Output common mode (VCM) voltage buffer is powered down
1'h1	EN_BUF_VCM_1	The ADC Output common mode (VCM) voltage buffer is NOT powered down

Table 1-266. Bit field encoding: EN_BUF_VREF_ENUM

Value	Name	Description
1'h0	EN_BUF_VREF_0	The Internal Reference Voltage Buffer is powered down
1'h1	EN_BUF_VREF_1	The Internal Reference Voltage Buffer is NOT powered down

Table 1-267. Bit field encoding: PWR_CTRL_VCM_ENUM

Value	Name	Description
2'h0	PWR_CTRL_VCM_0	VCM Buffer is operating in Low Power (18 uA) mode
2'h1	PWR_CTRL_VCM_1	VCM Buffer is operating in Medium Power (28 uA) mode
2'h2	PWR_CTRL_VCM_2	VCM Buffer is operating in High Power (55 uA) mode
2'h3	PWR_CTRL_VCM_3	VCM Buffer is operating in Turbo Power (114 uA) mode

Table 1-268. Bit field encoding: PWR_CTRL_VREF_ENUM

Value	Name	Description

(continued)

Table 1-268. Bit field encoding: PWR_CTRL_VREF_ENUM

2'h0	PWR_CTRL_VREF_0	VREF Buffer is operating in Low Power (26 uA) mode
2'h1	PWR_CTRL_VREF_1	VREF Buffer is operating in Medium Power (32 uA) mode
2'h2	PWR_CTRL_VREF_2	VREF Buffer is operating in High Power (118 uA) mode
2'h3	PWR_CTRL_VREF_3	VREF Buffer is operating in Turbo Power (232 uA) mode

Table 1-269. Bit field encoding: PWR_CTRL_VREF_INN_ENUM

Value	Name	Description
2'h0	PWR_CTRL_VREF_INN_LOW	VREF Buffer (Input mux path) is operating in Low Power (26uA) mode
2'h1	PWR_CTRL_VREF_INN_MEDIUM	VREF Buffer (Input mux path) is operating in Medium Power (32uA) mode
2'h2	PWR_CTRL_VREF_INN_HIGH	VREF Buffer (Input mux path) is operating in High Power (118uA) mode
2'h3	PWR_CTRL_VREF_INN_TURBO	VREF Buffer (Input mux path) is operating in Turbo Power (232uA) mode

1.3.389 DSM[0..0]_REF0

Delta Sigma Modulator Reference Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_REF0: 0x5892

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00		NA:0	R/W:0	R/W:0	R/W:000		
HW Access	R		NA	R	R	R		
Retention	RET		NA	RET	RET	RET		
Name	vcmsel		RSVD	vref_res_div_en	en_buf_vref_inn	refmux		

Bits	Name	Description
7:6	vcmsel[1:0]	Output common mode selection for modulator See Table 1-271.
4	vref_res_div_en	If enabled it allows the resistor divided value of (VDDA/3 or VDDA/4) to a selectable voltage for the RefMux
3	en_buf_vref_inn	Enable/Disable control for ADC (internal) REFBUF1 Buffer; This buffers the ADC reference before being sent to INN Mux; See DSM chapter
2:0	refmux[2:0]	Mux control that allows for selecting one among the various available internal reference values See Table 1-270.

Table 1-270. Bit field encoding: REFMUX_ENUM

Value	Name	Description
3'h0	REFMUX_0	No Selection made for VCM
3'h1	REFMUX_1	VDAC0 output is the reference for the DSM
3'h2	REFMUX_2	VDDA/4 is selected as the reference for the DSM (VDDA is the external voltage supply)
3'h3	REFMUX_3	VDDA/3 is selected as the reference for the DSM (VDDA is the external voltage supply)
3'h4	REFMUX_4	internal precision bandgap reference of 1.024 (typ) is selected as the DSM reference
3'h5	REFMUX_5	internal precision bandgap reference of 1.2V (typ) is selected as the DSM reference
3'h6	REFMUX_6	N/A
3'h7	REFMUX_7	N/A

Table 1-271. Bit field encoding: VCMSEL_ENUM

Value	Name	Description
2'h0	VCMSEL_0	No selection is made for VCM
2'h1	VCMSEL_1	0.8V from bandgap trim buffer is being selected as VCM (output common mode) for the DSM opamps
2'h2	VCMSEL_2	0.7V from bandgap trim buffer is being selected as VCM (output common mode)
2'h3	VCMSEL_3	Vssd being selected as VCM (output common mode) for the DSM opamps

1.3.390 DSM[0..0]_REF1

Delta Sigma Modulator Reference Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_REF1: 0x5893

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Retention	NA							RET
Name	RSVD							dac_gnd_sel

Bits	Name	Description
0	dac_gnd_sel	Selects DSM Reference DAC Capacitor Ground See Table 1-272.

Table 1-272. Bit field encoding: DSM_DAC_GND_SEL_ENUM

Value	Name	Description
1'b0	DSM_DAC_GND_SEL_INT	select DSM internal vssa
1'b1	DSM_DAC_GND_SEL_EXT	select external ground (AGL6)

1.3.391 DSM[0..0]_REF2

Delta Sigma Modulator Reference Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_REF2: 0x5894

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	s7_en	s6_en	s5_en	s4_en	s3_en	s2_en	s1_en	s0_en

Bits	Name	Description
7	s7_en	If Set, closes the S7 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel
6	s6_en	If Set, closes the S6 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel
5	s5_en	If Set, closes the S5 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel
4	s4_en	If Set, closes the S4 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel
3	s3_en	If Set, closes the S3 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel
2	s2_en	If Set, closes the S2 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel
1	s1_en	If Set, closes the S1 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel
0	s0_en	If Set, closes the S0 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel

1.3.392 DSM[0..0]_REF3

Delta Sigma Modulator Reference Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_REF3: 0x5895

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R	R	R	R	R	R
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		s13_en	s12_en	s11_en	s10_en	s9_en	s8_en

Bits	Name	Description
5	s13_en	If Set, closes the S13 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel
4	s12_en	If Set, closes the S12 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel
3	s11_en	If Set, closes the S11 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel
2	s10_en	If Set, closes the S10 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel
1	s9_en	If Set, closes the S9 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel
0	s8_en	If Set, closes the S8 switch in figure Sigma Delta Channel Analog Reference Selection in the DSM chapter; See sub-section Analog Reference Options for the Sigma Delta Channel

1.3.393 DSM[0..0]_DEM0

Delta Sigma Modulator Dynamic Element Matching Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_DEM0: 0x5896

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA			R	R	R	R	R
Retention	NA			RET	RET	RET	RET	RET
Name	RSVD			demtest_src	adc_test_en	en_dem	en_scrambler1	en_scrambler0

Bits	Name	Description
4	demtest_src	Select demtest source See Table 1-274.
3	adc_test_en	Enable/Disable All test modes in Sigma Delta Channel See Table 1-273.
2	en_dem	Enable DEM See Table 1-275.
1	en_scrambler1	Enable Scrambler 1 See Table 1-277.
0	en_scrambler0	Enable Scrambler 0 See Table 1-276.

Table 1-273. Bit field encoding: ADC_TEST_EN_ENUM

Value	Name	Description
1'h0	ADC_TEST_EN_0	Disable all test modes for the sigma delta channel
1'h1	ADC_TEST_EN_1	Enable all test modes for the sigma delta channel

Table 1-274. Bit field encoding: DEMTEST_SRC_ENUM

Value	Name	Description
1'h0	DEMTEST_SRC_REG	ANAIF register source selected - DSM#_DEM1.demtest[7:0]
1'h1	DEMTEST_SRC_UDB	UDB array source selected - dsi_anaif_dft[7:0]

Table 1-275. Bit field encoding: EN_DEM_ENUM

Value	Name	Description
1'h0	EN_DEM_DISABLE	Disable DEM
1'h1	EN_DEM_ENABLE	Enable DEM

Table 1-276. Bit field encoding: EN_SCRAMBLER0_ENUM

Value	Name	Description
1'h0	EN_SCRAMBLER0_DISABLE	Disable Scrambler 0

(continued)

Table 1-276. Bit field encoding: EN_SCRAMBLER0_ENUM

1'h1	EN_SCRAMBLER0_ENABLE	Enable Scrambler 0

Table 1-277. Bit field encoding: EN_SCRAMBLER1_ENUM

Value	Name	Description
1'h0	EN_SCRAMBLER1_DISABLE	Disable Scrambler 1
1'h1	EN_SCRAMBLER1_ENABLE	Enable Scrambler 1

1.3.394 DSM[0..0]_DEM1

Delta Sigma Modulator Dynamic Element Matching Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_DEM1: 0x5897

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	demtest							

Bits	Name	Description
7:0	demtest[7:0]	Register control for the DAC unit elements inside the first integrator. This can be used when bit DSM.DEM0[3], adc_test_en, is set. If the adc_test_en is not set the the control logic inside the modulator determines how the DAC unit elements are controlled. This is meant for static testing purposes

1.3.395 DSM[0..0]_BUF0

Delta Sigma Modulator Buffer Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_BUF0: 0x589A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	R/W:0	R/W:0
HW Access	NA					R	R	R
Retention	NA					RET	RET	RET
Name	RSVD					rail_rail_en	bypass_p	enable_p

Bits	Name	Description
2	rail_rail_en	Selects Rail-to-Rail Mode See Table 1-280.
1	bypass_p	Remove positive half of the buffer from signal path See Table 1-278.
0	enable_p	Buffer Positive Half Enable See Table 1-279.

Table 1-278. Bit field encoding: BYPASS_P_ENUM

Value	Name	Description
1'b0	BYPASS_P_0	The buffer in the positive half remains on the signal path (Refer Fig 33-2)
1'b1	BYPASS_P_1	bypass the buffer on the positive half of the signal path (Refer Fig 33-2)

Table 1-279. Bit field encoding: ENABLE_P_ENUM

Value	Name	Description
1'b0	ENABLE_P_0	power down buffer in positive half
1'b1	ENABLE_P_1	enable positive half of buffer

Table 1-280. Bit field encoding: RAIL_RAIL_EN_ENUM

Value	Name	Description
1'h0	RAIL_RAIL_EN_DISABLE	Level shifted mode
1'h1	RAIL_RAIL_EN_ENABLE	Rail-to-Rail mode

1.3.396 DSM[0..0]_BUF1

Delta Sigma Modulator Buffer Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_BUF1: 0x589B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:00		R/W:0	R/W:0
HW Access	NA				R		R	R
Retention	NA				RET		RET	RET
Name	RSVD				gain		bypass_n	enable_n

Bits	Name	Description
3:2	gain[1:0]	Gain settings of 1,2,4,8 are supported See Table 1-283.
1	bypass_n	Remove negative half of the buffer from signal path See Table 1-281.
0	enable_n	Buffer Negative Half Enable See Table 1-282.

Table 1-281. Bit field encoding: BYPASS_N_ENUM

Value	Name	Description
1'b0	BYPASS_N_DISABLE_BYPASS	The buffer in the negative half remains on the signal path (Refer Fig 33-2)
1'b1	BYPASS_N_ENABLE_BYPASS	bypass the buffer on the negative half of the signal path (Refer Fig 33-2)

Table 1-282. Bit field encoding: ENABLE_N_ENUM

Value	Name	Description
1'b0	ENABLE_N_0	power down buffer in negative half
1'b1	ENABLE_P_1	enable negative half of buffer

Table 1-283. Bit field encoding: GAIN_ENUM

Value	Name	Description
2'h0	GAIN_1X	1x
2'h1	GAIN_2X	2x
2'h2	GAIN_4X	4x
2'h3	GAIN_8X	8x

1.3.397 DSM[0..0]_BUF2

Delta Sigma Modulator Buffer Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_BUF2: 0x589C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:0	R/W:0
HW Access	NA						R	R
Retention	NA						RET	RET
Name	RSVD						add_extra_rc	lowpower_en

Bits	Name	Description
1	add_extra_rc	If enabled an additional RC is included at the output of the buffer differentially, to lower noise at the expense of settling else normal settling.
0	lowpower_en	Enables the lower power mode of operation. The normal power mode implies 600uA typical current consumption per opamp in the buffer. See Table 1-284.

Table 1-284. Bit field encoding: LOWPOWER_EN_ENUM

Value	Name	Description
1'h0	LOWPOWER_EN_NORMAL	Input buffer operated in normal power mode
1'h1	LOWPOWER_EN_LOW	Input buffer operated in low (1/4th of normal power) power mode

1.3.398 DSM[0..0]_BUF3

Delta Sigma Modulator Buffer Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_BUF3: 0x589D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:000		
HW Access	NA				R	R		
Retention	NA				RET	RET		
Name	RSVD				buf_chop_en	buf_fchop		

Bits	Name	Description
3	buf_chop_en	Enable/ Disable Chopping of the input buffer (TYPE A or B as selected in DSM_BUF0 register) See Table 1-285.
2:0	buf_fchop[2:0]	Input Buffer Chopping frequency control See Table 1-286.

Table 1-285. Bit field encoding: BUF_CHOP_EN_ENUM

Value	Name	Description
1'b0	BUF_CHOP_EN_0	Disable Chopping of the input buffer (type is as determined by
1'b1	BUF_CHOP_EN_1	Enable Chopping of the input buffer

Table 1-286. Bit field encoding: BUF_FCHOP_ENUM

Value	Name	Description
3'h0	BUF_FCHOP_0	chopping frequency is fs/2
3'h1	BUF_FCHOP_1	chopping frequency is fs/4
3'h2	BUF_FCHOP_2	chopping frequency is fs/8
3'h3	BUF_FCHOP_3	chopping frequency is fs/16
3'h4	BUF_FCHOP_4	chopping frequency is fs/32
3'h5	BUF_FCHOP_5	chopping frequency is fs/64
3'h6	BUF_FCHOP_6	chopping frequency is fs/128
3'h7	BUF_FCHOP_7	chopping frequency is fs/256

1.3.399 DSM[0..0]_MISC

Delta Sigma Modulator Miscellaneous register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_MISC: 0x589E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	NA:0	R/W:0
HW Access	NA				R	R	NA	R
Retention	NA				RET	RET	NA	RET
Name	RSVD				swvn_src	swvp_src	RSVD	sel_iclk_cp

Bits	Name	Description
3	swvn_src	negative input routing control source See Table 1-287.
2	swvp_src	positive input routing control source See Table 1-288.
0	sel_iclk_cp	Select Charge Pump Internal Clock See Table 1-289.

Table 1-287. Bit field encoding: DSM_SWVN_SRC_ENUM

Value	Name	Description
1'b0	DSM_SWVN_SRC_REG	ANAIF DSM routing registers
1'b1	DSM_SWVN_SRC_UDB	UDB

Table 1-288. Bit field encoding: DSM_SWVP_SRC_ENUM

Value	Name	Description
1'b0	DSM_SWVP_SRC_REG	ANAIF DSM routing registers
1'b1	DSM_SWVP_SRC_UDB	UDB

Table 1-289. Bit field encoding: SEL_ICLK_CP_ENUM

Value	Name	Description
1'b0	SEL_ICLK_CP_EXTERNAL	External (DSI) Charge Pump Clock selected
1'b1	SEL_ICLK_CP_INTERNAL	Internal Charge Pump Clock selected

1.3.400 DSM[0..0]_RSVD1

Delta Sigma Modulator RSVD 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_RSVD1: 0x589F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R							
Retention	NA							
Name	RSVD							

Bits	Name	Description
7:0	RSVD[7:0]	Reserved

1.3.401 SC0_SW0

Switched Capacitor Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_SW0: 0x5A00

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	vin_ag7	vin_ag6	vin_ag5	vin_ag4	vin_ag3	vin_ag2	vin_ag1	vin_ag0

Bits	Name	Description
7	vin_ag7	Connect SC signal input VIN to analog global of same side See Table 1-290.
6	vin_ag6	Connect SC signal input VIN to analog global of same side See Table 1-290.
5	vin_ag5	Connect SC signal input VIN to analog global of same side See Table 1-290.
4	vin_ag4	Connect SC signal input VIN to analog global of same side See Table 1-290.
3	vin_ag3	Connect SC signal input VIN to analog global of same side See Table 1-290.
2	vin_ag2	Connect SC signal input VIN to analog global of same side See Table 1-290.
1	vin_ag1	Connect SC signal input VIN to analog global of same side See Table 1-290.
0	vin_ag0	Connect SC signal input VIN to analog global of same side See Table 1-290.

Table 1-290. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.402 SC0_SW2

Switched Capacitor Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_SW2: 0x5A02

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	NA:0	R/W:0
HW Access	NA				R	R	NA	R
Retention	NA				RET	RET	NA	RET
Name	RSVD				vin_abus3	vin_abus2	RSVD	vin_abus0

Bits	Name	Description
3	vin_abus3	Connect SC signal input VIN to analog (local) bus of the same side See Table 1-291.
2	vin_abus2	Connect SC signal input VIN to analog (local) bus of the same side See Table 1-291.
0	vin_abus0	Connect SC signal input VIN to analog (local) bus of the same side See Table 1-291.

Table 1-291. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.403 SC0_SW3

Switched Capacitor Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_SW3: 0x5A03

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	NA:000			R/W:0	R/W:0
HW Access	NA		R	NA			R	R
Retention	NA		RET	NA			RET	RET
Name	RSVD		vref_bgvref	RSVD			vin_bgvref	vin_amx

Bits	Name	Description
5	vref_bgvref	Connect SC signal input VREF to Bandgap Voltage Reference See Table 1-293.
1	vin_bgvref	Connect SC signal input VIN to Bandgap Voltage Reference See Table 1-293.
0	vin_amx	Connect SC signal input VIN to Analog Mux Bus See Table 1-292.

Table 1-292. Bit field encoding: AMX_ENUM

Value	Name	Description
1'b0	AMX_NC	not connected
1'b1	AMX_CONNECTED	Connect to AMUXBUS

Table 1-293. Bit field encoding: VREF_ENUM

Value	Name	Description
1'b0	VREF_NC	not connected
1'b1	VREF_CONNECTED	Connect to Voltage Reference

1.3.404 SC0_SW4

Switched Capacitor Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_SW4: 0x5A04

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0
HW Access	NA	R	NA	R	NA	R	NA	R
Retention	NA	RET	NA	RET	NA	RET	NA	RET
Name	RSVD	vref_ag6	RSVD	vref_ag4	RSVD	vref_ag2	RSVD	vref_ag0

Bits	Name	Description
6	vref_ag6	Connect SC signal input VREF to analog global of same side See Table 1-294.
4	vref_ag4	Connect SC signal input VREF to analog global of same side See Table 1-294.
2	vref_ag2	Connect SC signal input VREF to analog global of same side See Table 1-294.
0	vref_ag0	Connect SC signal input VREF to analog global of same side See Table 1-294.

Table 1-294. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.405 SC0_SW6

Switched Capacitor Analog Routing Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_SW6: 0x5A06

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Retention	NA							RET
Name	RSVD							vref_abus0

Bits	Name	Description
0	vref_abus0	Connect SC signal input VREF to analog (local) bus of the same side See Table 1-295.

Table 1-295. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.406 SC0_SW7

Switched Capacitor Analog Routing Register 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_SW7: 0x5A07

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	NA:00	
HW Access	NA					R/W	NA	
Retention	NA					RET	NA	
Name	RSVD					vin_vo	RSVD	

Bits	Name	Description
2	vin_vo	Connect SC signal input VIN to VO of opposite SC See Table 1-296.

Table 1-296. Bit field encoding: VIN_VO_ENUM

Value	Name	Description
1'b0	VIN_VO_0	not connected
1'b1	VIN_VO_1	Connect VIN to VO of opposite SC

1.3.407 SC0_SW8

Switched Capacitor Analog Routing Register 8

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_SW8: 0x5A08

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0
HW Access	R	NA	R	NA	R	NA	R	NA
Retention	RET	NA	RET	NA	RET	NA	RET	NA
Name	vo_ag7	RSVD	vo_ag5	RSVD	vo_ag3	RSVD	vo_ag1	RSVD

Bits	Name	Description
7	vo_ag7	Connect voltage output to analog global of same side (see field instance name) See Table 1-297.
5	vo_ag5	Connect voltage output to analog global of same side (see field instance name) See Table 1-297.
3	vo_ag3	Connect voltage output to analog global of same side (see field instance name) See Table 1-297.
1	vo_ag1	Connect voltage output to analog global of same side (see field instance name) See Table 1-297.

Table 1-297. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.408 SC0_SW10

Switched Capacitor Analog Routing Register 10

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_SW10: 0x5A0A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	NA:0	R/W:0	NA:0
HW Access	NA				R	NA	R	NA
Retention	NA				RET	NA	RET	NA
Name	RSVD				vo_abus3	RSVD	vo_abus1	RSVD

Bits	Name	Description
3	vo_abus3	Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-298.
1	vo_abus1	Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-298.

Table 1-298. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.409 SC0_CLK

Switched Capacitor Clock Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_CLK: 0x5A0B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:000		
HW Access	NA		R/W	R	R	R		
Retention	NA		RET	RET	RET	RET		
Name	RSVD		dyn_cntl_en	bypass_sync	clk_en	mx_clk		

Bits	Name	Description
5	dyn_cntl_en	Enable Dynamic Control (UDB generated clock source drives dynamic control) See Table 1-301.
4	bypass_sync	Bypass Synchronization See Table 1-299.
3	clk_en	Clock gating control See Table 1-300.
2:0	mx_clk[2:0]	Clock Selection See Table 1-302.

Table 1-299. Bit field encoding: BYPASS_SYNC_ENUM

Value	Name	Description
1'b0	BYPASS_SYNC_0	Synchronization not bypassed (Synchronization enabled)
1'b1	BYPASS_SYNC_1	Synchronization bypassed (Synchronization disabled)

Table 1-300. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	CLK_EN_0	disable clock
1'b1	CLK_EN_1	enable clock

Table 1-301. Bit field encoding: DYN_CNTL_ENUM

Value	Name	Description
1'b0	DYN_CNTL_DIS	Dynamic Control Disabled
1'b1	DYN_CNTL_EN	Dynamic Control Enabled

Table 1-302. Bit field encoding: MX_CLK_ENUM

Value	Name	Description
3'h0	MX_CLK_0	Select clk_a0 and clk_a0_dig
3'h1	MX_CLK_1	Select clk_a1 and clk_a1_dig
3'h2	MX_CLK_2	Select clk_a2 and clk_a2_dig
3'h3	MX_CLK_3	Select clk_a3 and clk_a3_dig
3'h4	MX_CLK_4	Select UDB generated clock

(continued)

Table 1-302. Bit field encoding: MX_CLK_ENUM

3'h5	MX_CLK_5	Reserved
3'h6	MX_CLK_6	Reserved
3'h7	MX_CLK_7	Reserved

1.3.410 SC0_BST

Switched Capacitor Boost Clock Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC0_BST: 0x5A0C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:000		
HW Access	NA				R	R		
Retention	NA				RET	RET		
Name	RSVD				bst_clk_en	mx_bst_clk		

Bits	Name	Description
3	bst_clk_en	Clock gating control See Table 1-303.
2:0	mx_bst_clk[2:0]	Clock Selection See Table 1-304.

Table 1-303. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	CLK_EN_0	disable clock
1'b1	CLK_EN_1	enable clock

Table 1-304. Bit field encoding: MX_CLK_ENUM

Value	Name	Description
3'h0	MX_CLK_0	Select clk_a0 and clk_a0_dig
3'h1	MX_CLK_1	Select clk_a1 and clk_a1_dig
3'h2	MX_CLK_2	Select clk_a2 and clk_a2_dig
3'h3	MX_CLK_3	Select clk_a3 and clk_a3_dig
3'h4	MX_CLK_4	Select UDB generated clock
3'h5	MX_CLK_5	Reserved
3'h6	MX_CLK_6	Reserved
3'h7	MX_CLK_7	Reserved

1.3.411 SC1_SW0

Switched Capacitor Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC1_SW0: 0x5A10

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	vin_ag7	vin_ag6	vin_ag5	vin_ag4	vin_ag3	vin_ag2	vin_ag1	vin_ag0

Bits	Name	Description
7	vin_ag7	Connect SC signal input VIN to analog global of same side See Table 1-305.
6	vin_ag6	Connect SC signal input VIN to analog global of same side See Table 1-305.
5	vin_ag5	Connect SC signal input VIN to analog global of same side See Table 1-305.
4	vin_ag4	Connect SC signal input VIN to analog global of same side See Table 1-305.
3	vin_ag3	Connect SC signal input VIN to analog global of same side See Table 1-305.
2	vin_ag2	Connect SC signal input VIN to analog global of same side See Table 1-305.
1	vin_ag1	Connect SC signal input VIN to analog global of same side See Table 1-305.
0	vin_ag0	Connect SC signal input VIN to analog global of same side See Table 1-305.

Table 1-305. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.412 SC1_SW2

Switched Capacitor Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC1_SW2: 0x5A12

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	NA:0	R/W:0
HW Access	NA				R	R	NA	R
Retention	NA				RET	RET	NA	RET
Name	RSVD				vin_abus3	vin_abus2	RSVD	vin_abus0

Bits	Name	Description
3	vin_abus3	Connect SC signal input VIN to analog (local) bus of the same side See Table 1-306.
2	vin_abus2	Connect SC signal input VIN to analog (local) bus of the same side See Table 1-306.
0	vin_abus0	Connect SC signal input VIN to analog (local) bus of the same side See Table 1-306.

Table 1-306. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.413 SC1_SW3

Switched Capacitor Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC1_SW3: 0x5A13

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	NA:000			R/W:0	R/W:0
HW Access	NA		R	NA			R	R
Retention	NA		RET	NA			RET	RET
Name	RSVD		vref_bgvref	RSVD			vin_bgvref	vin_amx

Bits	Name	Description
5	vref_bgvref	Connect SC signal input VREF to Bandgap Voltage Reference See Table 1-308.
1	vin_bgvref	Connect SC signal input VIN to Bandgap Voltage Reference See Table 1-308.
0	vin_amx	Connect SC signal input VIN to Analog Mux Bus See Table 1-307.

Table 1-307. Bit field encoding: AMX_ENUM

Value	Name	Description
1'b0	AMX_NC	not connected
1'b1	AMX_CONNECTED	Connect to AMUXBUS

Table 1-308. Bit field encoding: VREF_ENUM

Value	Name	Description
1'b0	VREF_NC	not connected
1'b1	VREF_CONNECTED	Connect to Voltage Reference

1.3.414 SC1_SW4

Switched Capacitor Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC1_SW4: 0x5A14

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0
HW Access	NA	R	NA	R	NA	R	NA	R
Retention	NA	RET	NA	RET	NA	RET	NA	RET
Name	RSVD	vref_ag6	RSVD	vref_ag4	RSVD	vref_ag2	RSVD	vref_ag0

Bits	Name	Description
6	vref_ag6	Connect SC signal input VREF to analog global of same side See Table 1-309.
4	vref_ag4	Connect SC signal input VREF to analog global of same side See Table 1-309.
2	vref_ag2	Connect SC signal input VREF to analog global of same side See Table 1-309.
0	vref_ag0	Connect SC signal input VREF to analog global of same side See Table 1-309.

Table 1-309. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.415 SC1_SW6

Switched Capacitor Analog Routing Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC1_SW6: 0x5A16

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Retention	NA							RET
Name	RSVD							vref_abus0

Bits	Name	Description
0	vref_abus0	Connect SC signal input VREF to analog (local) bus of the same side See Table 1-310.

Table 1-310. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.416 SC1_SW7

Switched Capacitor Analog Routing Register 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC1_SW7: 0x5A17

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	NA:00	
HW Access	NA					R/W	NA	
Retention	NA					RET	NA	
Name	RSVD					vin_vo	RSVD	

Bits	Name	Description
2	vin_vo	Connect SC signal input VIN to VO of opposite SC See Table 1-311.

Table 1-311. Bit field encoding: VIN_VO_ENUM

Value	Name	Description
1'b0	VIN_VO_0	not connected
1'b1	VIN_VO_1	Connect VIN to VO of opposite SC

1.3.417 SC1_SW8

Switched Capacitor Analog Routing Register 8

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC1_SW8: 0x5A18

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0
HW Access	R	NA	R	NA	R	NA	R	NA
Retention	RET	NA	RET	NA	RET	NA	RET	NA
Name	vo_ag7	RSVD	vo_ag5	RSVD	vo_ag3	RSVD	vo_ag1	RSVD

Bits	Name	Description
7	vo_ag7	Connect voltage output to analog global of same side (see field instance name) See Table 1-312.
5	vo_ag5	Connect voltage output to analog global of same side (see field instance name) See Table 1-312.
3	vo_ag3	Connect voltage output to analog global of same side (see field instance name) See Table 1-312.
1	vo_ag1	Connect voltage output to analog global of same side (see field instance name) See Table 1-312.

Table 1-312. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.418 SC1_SW10

Switched Capacitor Analog Routing Register 10

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC1_SW10: 0x5A1A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	NA:0	R/W:0	NA:0
HW Access	NA				R	NA	R	NA
Retention	NA				RET	NA	RET	NA
Name	RSVD				vo_abus3	RSVD	vo_abus1	RSVD

Bits	Name	Description
3	vo_abus3	Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-313.
1	vo_abus1	Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-313.

Table 1-313. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.419 SC1_CLK

Switched Capacitor Clock Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC1_CLK: 0x5A1B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:000		
HW Access	NA		R/W	R	R	R		
Retention	NA		RET	RET	RET	RET		
Name	RSVD		dyn_cntl_en	bypass_sync	clk_en	mx_clk		

Bits	Name	Description
5	dyn_cntl_en	Enable Dynamic Control (UDB generated clock source drives dynamic control) See Table 1-316.
4	bypass_sync	Bypass Synchronization See Table 1-314.
3	clk_en	Clock gating control See Table 1-315.
2:0	mx_clk[2:0]	Clock Selection See Table 1-317.

Table 1-314. Bit field encoding: BYPASS_SYNC_ENUM

Value	Name	Description
1'b0	BYPASS_SYNC_0	Synchronization not bypassed (Synchronization enabled)
1'b1	BYPASS_SYNC_1	Synchronization bypassed (Synchronization disabled)

Table 1-315. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	CLK_EN_0	disable clock
1'b1	CLK_EN_1	enable clock

Table 1-316. Bit field encoding: DYN_CNTL_ENUM

Value	Name	Description
1'b0	DYN_CNTL_DIS	Dynamic Control Disabled
1'b1	DYN_CNTL_EN	Dynamic Control Enabled

Table 1-317. Bit field encoding: MX_CLK_ENUM

Value	Name	Description
3'h0	MX_CLK_0	Select clk_a0 and clk_a0_dig
3'h1	MX_CLK_1	Select clk_a1 and clk_a1_dig
3'h2	MX_CLK_2	Select clk_a2 and clk_a2_dig
3'h3	MX_CLK_3	Select clk_a3 and clk_a3_dig
3'h4	MX_CLK_4	Select UDB generated clock

(continued)

Table 1-317. Bit field encoding: MX_CLK_ENUM

3'h5	MX_CLK_5	Reserved
3'h6	MX_CLK_6	Reserved
3'h7	MX_CLK_7	Reserved

1.3.420 SC1_BST

Switched Capacitor Boost Clock Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC1_BST: 0x5A1C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:000		
HW Access	NA				R	R		
Retention	NA				RET	RET		
Name	RSVD				bst_clk_en	mx_bst_clk		

Bits	Name	Description
3	bst_clk_en	Clock gating control See Table 1-318.
2:0	mx_bst_clk[2:0]	Clock Selection See Table 1-319.

Table 1-318. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	CLK_EN_0	disable clock
1'b1	CLK_EN_1	enable clock

Table 1-319. Bit field encoding: MX_CLK_ENUM

Value	Name	Description
3'h0	MX_CLK_0	Select clk_a0 and clk_a0_dig
3'h1	MX_CLK_1	Select clk_a1 and clk_a1_dig
3'h2	MX_CLK_2	Select clk_a2 and clk_a2_dig
3'h3	MX_CLK_3	Select clk_a3 and clk_a3_dig
3'h4	MX_CLK_4	Select UDB generated clock
3'h5	MX_CLK_5	Reserved
3'h6	MX_CLK_6	Reserved
3'h7	MX_CLK_7	Reserved

1.3.421 SC2_SW0

Switched Capacitor Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC2_SW0: 0x5A20

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	vin_ag7	vin_ag6	vin_ag5	vin_ag4	vin_ag3	vin_ag2	vin_ag1	vin_ag0

Bits	Name	Description
7	vin_ag7	Connect SC signal input VIN to analog global of same side See Table 1-320.
6	vin_ag6	Connect SC signal input VIN to analog global of same side See Table 1-320.
5	vin_ag5	Connect SC signal input VIN to analog global of same side See Table 1-320.
4	vin_ag4	Connect SC signal input VIN to analog global of same side See Table 1-320.
3	vin_ag3	Connect SC signal input VIN to analog global of same side See Table 1-320.
2	vin_ag2	Connect SC signal input VIN to analog global of same side See Table 1-320.
1	vin_ag1	Connect SC signal input VIN to analog global of same side See Table 1-320.
0	vin_ag0	Connect SC signal input VIN to analog global of same side See Table 1-320.

Table 1-320. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.422 SC2_SW2

Switched Capacitor Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC2_SW2: 0x5A22

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	NA:0
HW Access	NA				R	R	R	NA
Retention	NA				RET	RET	RET	NA
Name	RSVD				vin_abus3	vin_abus2	vin_abus1	RSVD

Bits	Name	Description
3	vin_abus3	Connect SC signal input VIN to analog (local) bus of the same side See Table 1-321.
2	vin_abus2	Connect SC signal input VIN to analog (local) bus of the same side See Table 1-321.
1	vin_abus1	Connect SC signal input VIN to analog (local) bus of the same side See Table 1-321.

Table 1-321. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.423 SC2_SW3

Switched Capacitor Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC2_SW3: 0x5A23

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	NA:000			R/W:0	R/W:0
HW Access	NA		R	NA			R	R
Retention	NA		RET	NA			RET	RET
Name	RSVD		vref_bgvref	RSVD			vin_bgvref	vin_amx

Bits	Name	Description
5	vref_bgvref	Connect SC signal input VREF to Bandgap Voltage Reference See Table 1-323.
1	vin_bgvref	Connect SC signal input VIN to Bandgap Voltage Reference See Table 1-323.
0	vin_amx	Connect SC signal input VIN to Analog Mux Bus See Table 1-322.

Table 1-322. Bit field encoding: AMX_ENUM

Value	Name	Description
1'b0	AMX_NC	not connected
1'b1	AMX_CONNECTED	Connect to AMUXBUS

Table 1-323. Bit field encoding: VREF_ENUM

Value	Name	Description
1'b0	VREF_NC	not connected
1'b1	VREF_CONNECTED	Connect to Voltage Reference

1.3.424 SC2_SW4

Switched Capacitor Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC2_SW4: 0x5A24

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0
HW Access	R	NA	R	NA	R	NA	R	NA
Retention	RET	NA	RET	NA	RET	NA	RET	NA
Name	vref_ag7	RSVD	vref_ag5	RSVD	vref_ag3	RSVD	vref_ag1	RSVD

Bits	Name	Description
7	vref_ag7	Connect SC signal input VREF to analog global of same side See Table 1-324.
5	vref_ag5	Connect SC signal input VREF to analog global of same side See Table 1-324.
3	vref_ag3	Connect SC signal input VREF to analog global of same side See Table 1-324.
1	vref_ag1	Connect SC signal input VREF to analog global of same side See Table 1-324.

Table 1-324. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.425 SC2_SW6

Switched Capacitor Analog Routing Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC2_SW6: 0x5A26

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:0	NA:0
HW Access	NA						R	NA
Retention	NA						RET	NA
Name	RSVD						vref_abus1	RSVD

Bits	Name	Description
1	vref_abus1	Connect SC signal input VREF to analog (local) bus of the same side See Table 1-325.

Table 1-325. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.426 SC2_SW7

Switched Capacitor Analog Routing Register 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC2_SW7: 0x5A27

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	NA:00	
HW Access	NA					R/W	NA	
Retention	NA					RET	NA	
Name	RSVD					vin_vo	RSVD	

Bits	Name	Description
2	vin_vo	Connect SC signal input VIN to VO of opposite SC See Table 1-326.

Table 1-326. Bit field encoding: VIN_VO_ENUM

Value	Name	Description
1'b0	VIN_VO_0	not connected
1'b1	VIN_VO_1	Connect VIN to VO of opposite SC

1.3.427 SC2_SW8

Switched Capacitor Analog Routing Register 8

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC2_SW8: 0x5A28

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0
HW Access	NA	R	NA	R	NA	R	NA	R
Retention	NA	RET	NA	RET	NA	RET	NA	RET
Name	RSVD	vo_ag6	RSVD	vo_ag4	RSVD	vo_ag2	RSVD	vo_ag0

Bits	Name	Description
6	vo_ag6	Connect voltage output to analog global of same side (see field instance name) See Table 1-327.
4	vo_ag4	Connect voltage output to analog global of same side (see field instance name) See Table 1-327.
2	vo_ag2	Connect voltage output to analog global of same side (see field instance name) See Table 1-327.
0	vo_ag0	Connect voltage output to analog global of same side (see field instance name) See Table 1-327.

Table 1-327. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.428 SC2_SW10

Switched Capacitor Analog Routing Register 10

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC2_SW10: 0x5A2A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	NA:0	R/W:0
HW Access	NA					R	NA	R
Retention	NA					RET	NA	RET
Name	RSVD					vo_abus2	RSVD	vo_abus0

Bits	Name	Description
2	vo_abus2	Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-328.
0	vo_abus0	Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-328.

Table 1-328. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.429 SC2_CLK

Switched Capacitor Clock Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC2_CLK: 0x5A2B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:000		
HW Access	NA		R/W	R	R	R		
Retention	NA		RET	RET	RET	RET		
Name	RSVD		dyn_cntl_en	bypass_sync	clk_en	mx_clk		

Bits	Name	Description
5	dyn_cntl_en	Enable Dynamic Control (UDB generated clock source drives dynamic control) See Table 1-331.
4	bypass_sync	Bypass Synchronization See Table 1-329.
3	clk_en	Clock gating control See Table 1-330.
2:0	mx_clk[2:0]	Clock Selection See Table 1-332.

Table 1-329. Bit field encoding: BYPASS_SYNC_ENUM

Value	Name	Description
1'b0	BYPASS_SYNC_0	Synchronization not bypassed (Synchronization enabled)
1'b1	BYPASS_SYNC_1	Synchronization bypassed (Synchronization disabled)

Table 1-330. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	CLK_EN_0	disable clock
1'b1	CLK_EN_1	enable clock

Table 1-331. Bit field encoding: DYN_CNTL_ENUM

Value	Name	Description
1'b0	DYN_CNTL_DIS	Dynamic Control Disabled
1'b1	DYN_CNTL_EN	Dynamic Control Enabled

Table 1-332. Bit field encoding: MX_CLK_ENUM

Value	Name	Description
3'h0	MX_CLK_0	Select clk_a0 and clk_a0_dig
3'h1	MX_CLK_1	Select clk_a1 and clk_a1_dig
3'h2	MX_CLK_2	Select clk_a2 and clk_a2_dig
3'h3	MX_CLK_3	Select clk_a3 and clk_a3_dig
3'h4	MX_CLK_4	Select UDB generated clock

(continued)

Table 1-332. Bit field encoding: MX_CLK_ENUM

3'h5	MX_CLK_5	Reserved
3'h6	MX_CLK_6	Reserved
3'h7	MX_CLK_7	Reserved

1.3.430 SC2_BST

Switched Capacitor Boost Clock Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC2_BST: 0x5A2C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:000		
HW Access	NA				R	R		
Retention	NA				RET	RET		
Name	RSVD				bst_clk_en	mx_bst_clk		

Bits	Name	Description
3	bst_clk_en	Clock gating control See Table 1-333.
2:0	mx_bst_clk[2:0]	Clock Selection See Table 1-334.

Table 1-333. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	CLK_EN_0	disable clock
1'b1	CLK_EN_1	enable clock

Table 1-334. Bit field encoding: MX_CLK_ENUM

Value	Name	Description
3'h0	MX_CLK_0	Select clk_a0 and clk_a0_dig
3'h1	MX_CLK_1	Select clk_a1 and clk_a1_dig
3'h2	MX_CLK_2	Select clk_a2 and clk_a2_dig
3'h3	MX_CLK_3	Select clk_a3 and clk_a3_dig
3'h4	MX_CLK_4	Select UDB generated clock
3'h5	MX_CLK_5	Reserved
3'h6	MX_CLK_6	Reserved
3'h7	MX_CLK_7	Reserved

1.3.431 SC3_SW0

Switched Capacitor Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC3_SW0: 0x5A30

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	vin_ag7	vin_ag6	vin_ag5	vin_ag4	vin_ag3	vin_ag2	vin_ag1	vin_ag0

Bits	Name	Description
7	vin_ag7	Connect SC signal input VIN to analog global of same side See Table 1-335.
6	vin_ag6	Connect SC signal input VIN to analog global of same side See Table 1-335.
5	vin_ag5	Connect SC signal input VIN to analog global of same side See Table 1-335.
4	vin_ag4	Connect SC signal input VIN to analog global of same side See Table 1-335.
3	vin_ag3	Connect SC signal input VIN to analog global of same side See Table 1-335.
2	vin_ag2	Connect SC signal input VIN to analog global of same side See Table 1-335.
1	vin_ag1	Connect SC signal input VIN to analog global of same side See Table 1-335.
0	vin_ag0	Connect SC signal input VIN to analog global of same side See Table 1-335.

Table 1-335. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.432 SC3_SW2

Switched Capacitor Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC3_SW2: 0x5A32

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	NA:0
HW Access	NA				R	R	R	NA
Retention	NA				RET	RET	RET	NA
Name	RSVD				vin_abus3	vin_abus2	vin_abus1	RSVD

Bits	Name	Description
3	vin_abus3	Connect SC signal input VIN to analog (local) bus of the same side See Table 1-336.
2	vin_abus2	Connect SC signal input VIN to analog (local) bus of the same side See Table 1-336.
1	vin_abus1	Connect SC signal input VIN to analog (local) bus of the same side See Table 1-336.

Table 1-336. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.433 SC3_SW3

Switched Capacitor Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC3_SW3: 0x5A33

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	NA:000			R/W:0	R/W:0
HW Access	NA		R	NA			R	R
Retention	NA		RET	NA			RET	RET
Name	RSVD		vref_bgvref	RSVD			vin_bgvref	vin_amx

Bits	Name	Description
5	vref_bgvref	Connect SC signal input VREF to Bandgap Voltage Reference See Table 1-338.
1	vin_bgvref	Connect SC signal input VIN to Bandgap Voltage Reference See Table 1-338.
0	vin_amx	Connect SC signal input VIN to Analog Mux Bus See Table 1-337.

Table 1-337. Bit field encoding: AMX_ENUM

Value	Name	Description
1'b0	AMX_NC	not connected
1'b1	AMX_CONNECTED	Connect to AMUXBUS

Table 1-338. Bit field encoding: VREF_ENUM

Value	Name	Description
1'b0	VREF_NC	not connected
1'b1	VREF_CONNECTED	Connect to Voltage Reference

1.3.434 SC3_SW4

Switched Capacitor Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC3_SW4: 0x5A34

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0
HW Access	R	NA	R	NA	R	NA	R	NA
Retention	RET	NA	RET	NA	RET	NA	RET	NA
Name	vref_ag7	RSVD	vref_ag5	RSVD	vref_ag3	RSVD	vref_ag1	RSVD

Bits	Name	Description
7	vref_ag7	Connect SC signal input VREF to analog global of same side See Table 1-339.
5	vref_ag5	Connect SC signal input VREF to analog global of same side See Table 1-339.
3	vref_ag3	Connect SC signal input VREF to analog global of same side See Table 1-339.
1	vref_ag1	Connect SC signal input VREF to analog global of same side See Table 1-339.

Table 1-339. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.435 SC3_SW6

Switched Capacitor Analog Routing Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC3_SW6: 0x5A36

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:0	NA:0
HW Access	NA						R	NA
Retention	NA						RET	NA
Name	RSVD						vref_abus1	RSVD

Bits	Name	Description
1	vref_abus1	Connect SC signal input VREF to analog (local) bus of the same side See Table 1-340.

Table 1-340. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.436 SC3_SW7

Switched Capacitor Analog Routing Register 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC3_SW7: 0x5A37

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	NA:00	
HW Access	NA					R/W	NA	
Retention	NA					RET	NA	
Name	RSVD					vin_vo	RSVD	

Bits	Name	Description
2	vin_vo	Connect SC signal input VIN to VO of opposite SC See Table 1-341.

Table 1-341. Bit field encoding: VIN_VO_ENUM

Value	Name	Description
1'b0	VIN_VO_0	not connected
1'b1	VIN_VO_1	Connect VIN to VO of opposite SC

1.3.437 SC3_SW8

Switched Capacitor Analog Routing Register 8

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC3_SW8: 0x5A38

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0
HW Access	NA	R	NA	R	NA	R	NA	R
Retention	NA	RET	NA	RET	NA	RET	NA	RET
Name	RSVD	vo_ag6	RSVD	vo_ag4	RSVD	vo_ag2	RSVD	vo_ag0

Bits	Name	Description
6	vo_ag6	Connect voltage output to analog global of same side (see field instance name) See Table 1-342.
4	vo_ag4	Connect voltage output to analog global of same side (see field instance name) See Table 1-342.
2	vo_ag2	Connect voltage output to analog global of same side (see field instance name) See Table 1-342.
0	vo_ag0	Connect voltage output to analog global of same side (see field instance name) See Table 1-342.

Table 1-342. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.438 SC3_SW10

Switched Capacitor Analog Routing Register 10

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC3_SW10: 0x5A3A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	NA:0	R/W:0
HW Access	NA					R	NA	R
Retention	NA					RET	NA	RET
Name	RSVD					vo_abus2	RSVD	vo_abus0

Bits	Name	Description
2	vo_abus2	Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-343.
0	vo_abus0	Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-343.

Table 1-343. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.439 SC3_CLK

Switched Capacitor Clock Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC3_CLK: 0x5A3B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:000		
HW Access	NA		R/W	R	R	R		
Retention	NA		RET	RET	RET	RET		
Name	RSVD		dyn_cntl_en	bypass_sync	clk_en	mx_clk		

Bits	Name	Description
5	dyn_cntl_en	Enable Dynamic Control (UDB generated clock source drives dynamic control) See Table 1-346.
4	bypass_sync	Bypass Synchronization See Table 1-344.
3	clk_en	Clock gating control See Table 1-345.
2:0	mx_clk[2:0]	Clock Selection See Table 1-347.

Table 1-344. Bit field encoding: BYPASS_SYNC_ENUM

Value	Name	Description
1'b0	BYPASS_SYNC_0	Synchronization not bypassed (Synchronization enabled)
1'b1	BYPASS_SYNC_1	Synchronization bypassed (Synchronization disabled)

Table 1-345. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	CLK_EN_0	disable clock
1'b1	CLK_EN_1	enable clock

Table 1-346. Bit field encoding: DYN_CNTL_ENUM

Value	Name	Description
1'b0	DYN_CNTL_DIS	Dynamic Control Disabled
1'b1	DYN_CNTL_EN	Dynamic Control Enabled

Table 1-347. Bit field encoding: MX_CLK_ENUM

Value	Name	Description
3'h0	MX_CLK_0	Select clk_a0 and clk_a0_dig
3'h1	MX_CLK_1	Select clk_a1 and clk_a1_dig
3'h2	MX_CLK_2	Select clk_a2 and clk_a2_dig
3'h3	MX_CLK_3	Select clk_a3 and clk_a3_dig
3'h4	MX_CLK_4	Select UDB generated clock

(continued)

Table 1-347. Bit field encoding: MX_CLK_ENUM

3'h5	MX_CLK_5	Reserved
3'h6	MX_CLK_6	Reserved
3'h7	MX_CLK_7	Reserved

1.3.440 SC3_BST

Switched Capacitor Boost Clock Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC3_BST: 0x5A3C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:000		
HW Access	NA				R	R		
Retention	NA				RET	RET		
Name	RSVD				bst_clk_en	mx_bst_clk		

Bits	Name	Description
3	bst_clk_en	Clock gating control See Table 1-348.
2:0	mx_bst_clk[2:0]	Clock Selection See Table 1-349.

Table 1-348. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	CLK_EN_0	disable clock
1'b1	CLK_EN_1	enable clock

Table 1-349. Bit field encoding: MX_CLK_ENUM

Value	Name	Description
3'h0	MX_CLK_0	Select clk_a0 and clk_a0_dig
3'h1	MX_CLK_1	Select clk_a1 and clk_a1_dig
3'h2	MX_CLK_2	Select clk_a2 and clk_a2_dig
3'h3	MX_CLK_3	Select clk_a3 and clk_a3_dig
3'h4	MX_CLK_4	Select UDB generated clock
3'h5	MX_CLK_5	Reserved
3'h6	MX_CLK_6	Reserved
3'h7	MX_CLK_7	Reserved

1.3.441 DAC0_SW0

DAC Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC0_SW0: 0x5A80

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:0	R/W:0
HW Access	NA						R	R
Retention	NA						RET	RET
Name	RSVD						v_ag1	v_ag0

Bits	Name	Description
1	v_ag1	Connect voltage output to analog global of same side (see field instance name) See Table 1-350.
0	v_ag0	Connect voltage output to analog global of same side (see field instance name) See Table 1-350.

Table 1-350. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.442 DAC0_SW2

DAC Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC0_SW2: 0x5A82

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	NA:0	R/W:0	NA:0
HW Access	NA				R	NA	R	NA
Retention	NA				RET	NA	RET	NA
Name	RSVD				v_abus3	RSVD	v_abus1	RSVD

Bits	Name	Description
3	v_abus3	Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-351.
1	v_abus1	Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-351.

Table 1-351. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.443 DAC0_SW3

DAC Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC0_SW3: 0x5A83

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:00		R/W:0	NA:000			R/W:0
HW Access	R	NA		R	NA			R
Retention	RET	NA		RET	NA			RET
Name	iout	RSVD		i_amx	RSVD			v_amx

Bits	Name	Description
7	iout	Connect current output to pad See Table 1-353.
4	i_amx	Connect current output to Analog Mux Bus See Table 1-352.
0	v_amx	Connect voltage output to Analog Mux Bus See Table 1-352.

Table 1-352. Bit field encoding: AMX_ENUM

Value	Name	Description
1'b0	AMX_NC	not connected
1'b1	AMX_CONNECTED	Connect to AMUXBUS

Table 1-353. Bit field encoding: IOUT_ENUM

Value	Name	Description
1'b0	IOUT_NC	not connected
1'b1	IOUT_CONNECT	Connect to pad (see routing diagram)

1.3.444 DAC0_SW4

DAC Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC0_SW4: 0x5A84

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:0	R/W:0
HW Access	NA						R	R
Retention	NA						RET	RET
Name	RSVD						i_ag1	i_ag0

Bits	Name	Description
1	i_ag1	Connect current output to analog global of same side (see field instance name) See Table 1-354.
0	i_ag0	Connect current output to analog global of same side (see field instance name) See Table 1-354.

Table 1-354. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.445 DAC0_STROBE

DAC Strobe Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC0_STROBE: 0x5A87

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:000		
HW Access	NA				R	R		
Retention	NA				RET	RET		
Name	RSVD				strobe_en	mx_strobe		

Bits	Name	Description
3	strobe_en	Strobe gating control (See mx_strobe==3'h0) See Table 1-356.
2:0	mx_strobe[2:0]	Strobe source selection See Table 1-355.

Table 1-355. Bit field encoding: MX_STROBE_ENUM

Value	Name	Description
3'h0	MX_STROBE_BUSWRITE	Select bus write strobe source (Enable gater regardless of strobe_en setting)
3'h1	MX_STROBE_UDB_SRC	Select UDB strobe source
3'h2	MX_STROBE_NC_2	NC
3'h3	MX_STROBE_NC_3	NC
3'h4	MX_STROBE_CLK_A0_DIG	Select clk_a0_dig
3'h5	MX_STROBE_CLK_A1_DIG	Select clk_a1_dig
3'h6	MX_STROBE_CLK_A2_DIG	Select clk_a2_dig
3'h7	MX_STROBE_CLK_A3_DIG	Select clk_a3_dig

Table 1-356. Bit field encoding: STROBE_EN_ENUM

Value	Name	Description
1'b0	STROBE_EN_0	disable strobe
1'b1	STROBE_EN_1	enable strobe

1.3.446 DAC1_SW0

DAC Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC1_SW0: 0x5A88

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:0	R/W:0
HW Access	NA						R	R
Retention	NA						RET	RET
Name	RSVD						v_ag1	v_ag0

Bits	Name	Description
1	v_ag1	Connect voltage output to analog global of same side (see field instance name) See Table 1-357.
0	v_ag0	Connect voltage output to analog global of same side (see field instance name) See Table 1-357.

Table 1-357. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.447 DAC1_SW2

DAC Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC1_SW2: 0x5A8A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	NA:0	R/W:0	NA:0
HW Access	NA				R	NA	R	NA
Retention	NA				RET	NA	RET	NA
Name	RSVD				v_abus3	RSVD	v_abus1	RSVD

Bits	Name	Description
3	v_abus3	Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-358.
1	v_abus1	Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-358.

Table 1-358. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.448 DAC1_SW3

DAC Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC1_SW3: 0x5A8B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:00		R/W:0	NA:000			R/W:0
HW Access	R	NA		R	NA			R
Retention	RET	NA		RET	NA			RET
Name	iout	RSVD		i_amx	RSVD			v_amx

Bits	Name	Description
7	iout	Connect current output to pad See Table 1-360.
4	i_amx	Connect current output to Analog Mux Bus See Table 1-359.
0	v_amx	Connect voltage output to Analog Mux Bus See Table 1-359.

Table 1-359. Bit field encoding: AMX_ENUM

Value	Name	Description
1'b0	AMX_NC	not connected
1'b1	AMX_CONNECTED	Connect to AMUXBUS

Table 1-360. Bit field encoding: IOUT_ENUM

Value	Name	Description
1'b0	IOUT_NC	not connected
1'b1	IOUT_CONNECT	Connect to pad (see routing diagram)

1.3.449 DAC1_SW4

DAC Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC1_SW4: 0x5A8C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:0	R/W:0
HW Access	NA						R	R
Retention	NA						RET	RET
Name	RSVD						i_ag1	i_ag0

Bits	Name	Description
1	i_ag1	Connect current output to analog global of same side (see field instance name) See Table 1-361.
0	i_ag0	Connect current output to analog global of same side (see field instance name) See Table 1-361.

Table 1-361. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.450 DAC1_STROBE

DAC Strobe Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC1_STROBE: 0x5A8F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:000		
HW Access	NA				R	R		
Retention	NA				RET	RET		
Name	RSVD				strobe_en	mx_strobe		

Bits	Name	Description
3	strobe_en	Strobe gating control (See mx_strobe==3'h0) See Table 1-363.
2:0	mx_strobe[2:0]	Strobe source selection See Table 1-362.

Table 1-362. Bit field encoding: MX_STROBE_ENUM

Value	Name	Description
3'h0	MX_STROBE_BUSWRITE	Select bus write strobe source (Enable gater regardless of strobe_en setting)
3'h1	MX_STROBE_UDB_SRC	Select UDB strobe source
3'h2	MX_STROBE_NC_2	NC
3'h3	MX_STROBE_NC_3	NC
3'h4	MX_STROBE_CLK_A0_DIG	Select clk_a0_dig
3'h5	MX_STROBE_CLK_A1_DIG	Select clk_a1_dig
3'h6	MX_STROBE_CLK_A2_DIG	Select clk_a2_dig
3'h7	MX_STROBE_CLK_A3_DIG	Select clk_a3_dig

Table 1-363. Bit field encoding: STROBE_EN_ENUM

Value	Name	Description
1'b0	STROBE_EN_0	disable strobe
1'b1	STROBE_EN_1	enable strobe

1.3.451 DAC2_SW0

DAC Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC2_SW0: 0x5A90

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	NA:0000			
HW Access	NA		R	R	NA			
Retention	NA		RET	RET	NA			
Name	RSVD		v_ag5	v_ag4	RSVD			

Bits	Name	Description
5	v_ag5	Connect voltage output to analog global of same side (see field instance name) See Table 1-364.
4	v_ag4	Connect voltage output to analog global of same side (see field instance name) See Table 1-364.

Table 1-364. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.452 DAC2_SW2

DAC Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC2_SW2: 0x5A92

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	NA:0	R/W:0
HW Access	NA					R	NA	R
Retention	NA					RET	NA	RET
Name	RSVD					v_abus2	RSVD	v_abus0

Bits	Name	Description
2	v_abus2	Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-365.
0	v_abus0	Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-365.

Table 1-365. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.453 DAC2_SW3

DAC Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC2_SW3: 0x5A93

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:00		R/W:0	NA:000			R/W:0
HW Access	R	NA		R	NA			R
Retention	RET	NA		RET	NA			RET
Name	iout	RSVD		i_amx	RSVD			v_amx

Bits	Name	Description
7	iout	Connect current output to pad See Table 1-367.
4	i_amx	Connect current output to Analog Mux Bus See Table 1-366.
0	v_amx	Connect voltage output to Analog Mux Bus See Table 1-366.

Table 1-366. Bit field encoding: AMX_ENUM

Value	Name	Description
1'b0	AMX_NC	not connected
1'b1	AMX_CONNECTED	Connect to AMUXBUS

Table 1-367. Bit field encoding: IOUT_ENUM

Value	Name	Description
1'b0	IOUT_NC	not connected
1'b1	IOUT_CONNECT	Connect to pad (see routing diagram)

1.3.454 DAC2_SW4

DAC Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC2_SW4: 0x5A94

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	NA:0000			
HW Access	NA		R	R	NA			
Retention	NA		RET	RET	NA			
Name	RSVD		i_ag5	i_ag4	RSVD			

Bits	Name	Description
5	i_ag5	Connect current output to analog global of same side (see field instance name) See Table 1-368.
4	i_ag4	Connect current output to analog global of same side (see field instance name) See Table 1-368.

Table 1-368. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.455 DAC2_STROBE

DAC Strobe Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC2_STROBE: 0x5A97

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:000		
HW Access	NA				R	R		
Retention	NA				RET	RET		
Name	RSVD				strobe_en	mx_strobe		

Bits	Name	Description
3	strobe_en	Strobe gating control (See mx_strobe==3'h0) See Table 1-370.
2:0	mx_strobe[2:0]	Strobe source selection See Table 1-369.

Table 1-369. Bit field encoding: MX_STROBE_ENUM

Value	Name	Description
3'h0	MX_STROBE_BUSWRITE	Select bus write strobe source (Enable gater regardless of strobe_en setting)
3'h1	MX_STROBE_UDB_SRC	Select UDB strobe source
3'h2	MX_STROBE_NC_2	NC
3'h3	MX_STROBE_NC_3	NC
3'h4	MX_STROBE_CLK_A0_DIG	Select clk_a0_dig
3'h5	MX_STROBE_CLK_A1_DIG	Select clk_a1_dig
3'h6	MX_STROBE_CLK_A2_DIG	Select clk_a2_dig
3'h7	MX_STROBE_CLK_A3_DIG	Select clk_a3_dig

Table 1-370. Bit field encoding: STROBE_EN_ENUM

Value	Name	Description
1'b0	STROBE_EN_0	disable strobe
1'b1	STROBE_EN_1	enable strobe

1.3.456 DAC3_SW0

DAC Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC3_SW0: 0x5A98

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	NA:0000			
HW Access	NA		R	R	NA			
Retention	NA		RET	RET	NA			
Name	RSVD		v_ag5	v_ag4	RSVD			

Bits	Name	Description
5	v_ag5	Connect voltage output to analog global of same side (see field instance name) See Table 1-371.
4	v_ag4	Connect voltage output to analog global of same side (see field instance name) See Table 1-371.

Table 1-371. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.457 DAC3_SW2

DAC Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC3_SW2: 0x5A9A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	NA:0	R/W:0
HW Access	NA					R	NA	R
Retention	NA					RET	NA	RET
Name	RSVD					v_abus2	RSVD	v_abus0

Bits	Name	Description
2	v_abus2	Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-372.
0	v_abus0	Connect voltage output to analog (local) bus of the same side (see field instance name) See Table 1-372.

Table 1-372. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.458 DAC3_SW3

DAC Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC3_SW3: 0x5A9B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:00		R/W:0	NA:000			R/W:0
HW Access	R	NA		R	NA			R
Retention	RET	NA		RET	NA			RET
Name	iout	RSVD		i_amx	RSVD			v_amx

Bits	Name	Description
7	iout	Connect current output to pad See Table 1-374.
4	i_amx	Connect current output to Analog Mux Bus See Table 1-373.
0	v_amx	Connect voltage output to Analog Mux Bus See Table 1-373.

Table 1-373. Bit field encoding: AMX_ENUM

Value	Name	Description
1'b0	AMX_NC	not connected
1'b1	AMX_CONNECTED	Connect to AMUXBUS

Table 1-374. Bit field encoding: IOUT_ENUM

Value	Name	Description
1'b0	IOUT_NC	not connected
1'b1	IOUT_CONNECT	Connect to pad (see routing diagram)

1.3.459 DAC3_SW4

DAC Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC3_SW4: 0x5A9C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	NA:0000			
HW Access	NA		R	R	NA			
Retention	NA		RET	RET	NA			
Name	RSVD		i_ag5	i_ag4	RSVD			

Bits	Name	Description
5	i_ag5	Connect current output to analog global of same side (see field instance name) See Table 1-375.
4	i_ag4	Connect current output to analog global of same side (see field instance name) See Table 1-375.

Table 1-375. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.460 DAC3_STROBE

DAC Strobe Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC3_STROBE: 0x5A9F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:000		
HW Access	NA				R	R		
Retention	NA				RET	RET		
Name	RSVD				strobe_en	mx_strobe		

Bits	Name	Description
3	strobe_en	Strobe gating control (See mx_strobe==3'h0) See Table 1-377.
2:0	mx_strobe[2:0]	Strobe source selection See Table 1-376.

Table 1-376. Bit field encoding: MX_STROBE_ENUM

Value	Name	Description
3'h0	MX_STROBE_BUSWRITE	Select bus write strobe source (Enable gater regardless of strobe_en setting)
3'h1	MX_STROBE_UDB_SRC	Select UDB strobe source
3'h2	MX_STROBE_NC_2	NC
3'h3	MX_STROBE_NC_3	NC
3'h4	MX_STROBE_CLK_A0_DIG	Select clk_a0_dig
3'h5	MX_STROBE_CLK_A1_DIG	Select clk_a1_dig
3'h6	MX_STROBE_CLK_A2_DIG	Select clk_a2_dig
3'h7	MX_STROBE_CLK_A3_DIG	Select clk_a3_dig

Table 1-377. Bit field encoding: STROBE_EN_ENUM

Value	Name	Description
1'b0	STROBE_EN_0	disable strobe
1'b1	STROBE_EN_1	enable strobe

1.3.461 CMP0_SW0

Comparator Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP0_SW0: 0x5AC0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	vp_ag7	vp_ag6	vp_ag5	vp_ag4	vp_ag3	vp_ag2	vp_ag1	vp_ag0

Bits	Name	Description
7	vp_ag7	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-378.
6	vp_ag6	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-378.
5	vp_ag5	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-378.
4	vp_ag4	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-378.
3	vp_ag3	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-378.
2	vp_ag2	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-378.
1	vp_ag1	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-378.
0	vp_ag0	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-378.

Table 1-378. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.462 CMP0_SW2

Comparator Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP0_SW2: 0x5AC2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:0	R/W:0
HW Access	NA						R	R
Retention	NA						RET	RET
Name	RSVD						vp_abus1	vp_abus0

Bits	Name	Description
1	vp_abus1	Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-379.
0	vp_abus0	Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-379.

Table 1-379. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.463 CMP0_SW3

Comparator Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP0_SW3: 0x5AC3

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:0	R/W:0	R/W:0	NA:00		R/W:0
HW Access	NA	R	R	R	R	NA		R
Retention	NA	RET	RET	RET	RET	NA		RET
Name	RSVD	vn_vref1	vn_vref0	vn_amx	vp_refbuf	RSVD		vp_amx

Bits	Name	Description
6	vn_vref1	Connect negative voltage input to Voltage Reference 1 See Table 1-382.
5	vn_vref0	Connect negative voltage input to Voltage Reference 0 See Table 1-382.
4	vn_amx	Connect negative voltage input to Analog Mux Bus See Table 1-380.
3	vp_refbuf	Connect positive voltage input to CapSense reference buffer channel See Table 1-381.
0	vp_amx	Connect positive voltage input to Analog Mux Bus See Table 1-380.

Table 1-380. Bit field encoding: AMX_ENUM

Value	Name	Description
1'b0	AMX_NC	not connected
1'b1	AMX_CONNECTED	Connect to AMUXBUS

Table 1-381. Bit field encoding: VP_REFBUF_ENUM

Value	Name	Description
1'b0	VP_REFBUF_ENABLED	disable
1'b1	VP_REFBUF_DISABLED	enable

Table 1-382. Bit field encoding: VREF_ENUM

Value	Name	Description
1'b0	VREF_NC	not connected
1'b1	VREF_CONNECTED	Connect to Voltage Reference

1.3.464 CMP0_SW4

Comparator Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP0_SW4: 0x5AC4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0
HW Access	NA	R	NA	R	NA	R	NA	R
Retention	NA	RET	NA	RET	NA	RET	NA	RET
Name	RSVD	vn_ag6	RSVD	vn_ag4	RSVD	vn_ag2	RSVD	vn_ag0

Bits	Name	Description
6	vn_ag6	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-383.
4	vn_ag4	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-383.
2	vn_ag2	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-383.
0	vn_ag0	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-383.

Table 1-383. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.465 CMP0_SW6

Comparator Analog Routing Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP0_SW6: 0x5AC6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	NA:00	
HW Access	NA				R	R	NA	
Retention	NA				RET	RET	NA	
Name	RSVD				vn_abus3	vn_abus2	RSVD	

Bits	Name	Description
3	vn_abus3	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-384.
2	vn_abus2	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-384.

Table 1-384. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.466 CMP0_CLK

Comparator Clock Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP0_CLK: 0x5AC7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:000		
HW Access	NA			R	R	R		
Retention	NA			RET	RET	RET		
Name	RSVD			bypass_sync	clk_en	mx_clk		

Bits	Name	Description
4	bypass_sync	Bypass Synchronization See Table 1-385.
3	clk_en	Clock gating control See Table 1-386.
2:0	mx_clk[2:0]	Clock Selection See Table 1-387.

Table 1-385. Bit field encoding: BYPASS_SYNC_ENUM

Value	Name	Description
1'b0	BYPASS_SYNC_0	Synchronization not bypassed (Synchronization enabled)
1'b1	BYPASS_SYNC_1	Synchronization bypassed (Synchronization disabled)

Table 1-386. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	CLK_EN_0	disable clock
1'b1	CLK_EN_1	enable clock

Table 1-387. Bit field encoding: MX_CLK_ENUM

Value	Name	Description
3'h0	MX_CLK_0	Select clk_a0 and clk_a0_dig
3'h1	MX_CLK_1	Select clk_a1 and clk_a1_dig
3'h2	MX_CLK_2	Select clk_a2 and clk_a2_dig
3'h3	MX_CLK_3	Select clk_a3 and clk_a3_dig
3'h4	MX_CLK_4	Select UDB generated clock
3'h5	MX_CLK_5	Reserved
3'h6	MX_CLK_6	Reserved
3'h7	MX_CLK_7	Reserved

1.3.467 CMP1_SW0

Comparator Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP1_SW0: 0x5AC8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	vp_ag7	vp_ag6	vp_ag5	vp_ag4	vp_ag3	vp_ag2	vp_ag1	vp_ag0

Bits	Name	Description
7	vp_ag7	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-388.
6	vp_ag6	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-388.
5	vp_ag5	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-388.
4	vp_ag4	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-388.
3	vp_ag3	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-388.
2	vp_ag2	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-388.
1	vp_ag1	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-388.
0	vp_ag0	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-388.

Table 1-388. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.468 CMP1_SW2

Comparator Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP1_SW2: 0x5ACA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:0	R/W:0
HW Access	NA						R	R
Retention	NA						RET	RET
Name	RSVD						vp_abus1	vp_abus0

Bits	Name	Description
1	vp_abus1	Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-389.
0	vp_abus0	Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-389.

Table 1-389. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.469 CMP1_SW3

Comparator Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP1_SW3: 0x5ACB

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:0	R/W:0	R/W:0	NA:00		R/W:0
HW Access	NA	R	R	R	R	NA		R
Retention	NA	RET	RET	RET	RET	NA		RET
Name	RSVD	vn_vref1	vn_vref0	vn_amx	vp_refbuf	RSVD		vp_amx

Bits	Name	Description
6	vn_vref1	Connect negative voltage input to Voltage Reference 1 See Table 1-392.
5	vn_vref0	Connect negative voltage input to Voltage Reference 0 See Table 1-392.
4	vn_amx	Connect negative voltage input to Analog Mux Bus See Table 1-390.
3	vp_refbuf	Connect positive voltage input to CapSense reference buffer channel See Table 1-391.
0	vp_amx	Connect positive voltage input to Analog Mux Bus See Table 1-390.

Table 1-390. Bit field encoding: AMX_ENUM

Value	Name	Description
1'b0	AMX_NC	not connected
1'b1	AMX_CONNECTED	Connect to AMUXBUS

Table 1-391. Bit field encoding: VP_REFBUF_ENUM

Value	Name	Description
1'b0	VP_REFBUF_ENABLED	disable
1'b1	VP_REFBUF_DISABLED	enable

Table 1-392. Bit field encoding: VREF_ENUM

Value	Name	Description
1'b0	VREF_NC	not connected
1'b1	VREF_CONNECTED	Connect to Voltage Reference

1.3.470 CMP1_SW4

Comparator Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP1_SW4: 0x5ACC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0
HW Access	NA	R	NA	R	NA	R	NA	R
Retention	NA	RET	NA	RET	NA	RET	NA	RET
Name	RSVD	vn_ag6	RSVD	vn_ag4	RSVD	vn_ag2	RSVD	vn_ag0

Bits	Name	Description
6	vn_ag6	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-393.
4	vn_ag4	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-393.
2	vn_ag2	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-393.
0	vn_ag0	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-393.

Table 1-393. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.471 CMP1_SW6

Comparator Analog Routing Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP1_SW6: 0x5ACE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	NA:00	
HW Access	NA				R	R	NA	
Retention	NA				RET	RET	NA	
Name	RSVD				vn_abus3	vn_abus2	RSVD	

Bits	Name	Description
3	vn_abus3	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-394.
2	vn_abus2	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-394.

Table 1-394. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.472 CMP1_CLK

Comparator Clock Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP1_CLK: 0x5ACF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:000		
HW Access	NA			R	R	R		
Retention	NA			RET	RET	RET		
Name	RSVD			bypass_sync	clk_en	mx_clk		

Bits	Name	Description
4	bypass_sync	Bypass Synchronization See Table 1-395.
3	clk_en	Clock gating control See Table 1-396.
2:0	mx_clk[2:0]	Clock Selection See Table 1-397.

Table 1-395. Bit field encoding: BYPASS_SYNC_ENUM

Value	Name	Description
1'b0	BYPASS_SYNC_0	Synchronization not bypassed (Synchronization enabled)
1'b1	BYPASS_SYNC_1	Synchronization bypassed (Synchronization disabled)

Table 1-396. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	CLK_EN_0	disable clock
1'b1	CLK_EN_1	enable clock

Table 1-397. Bit field encoding: MX_CLK_ENUM

Value	Name	Description
3'h0	MX_CLK_0	Select clk_a0 and clk_a0_dig
3'h1	MX_CLK_1	Select clk_a1 and clk_a1_dig
3'h2	MX_CLK_2	Select clk_a2 and clk_a2_dig
3'h3	MX_CLK_3	Select clk_a3 and clk_a3_dig
3'h4	MX_CLK_4	Select UDB generated clock
3'h5	MX_CLK_5	Reserved
3'h6	MX_CLK_6	Reserved
3'h7	MX_CLK_7	Reserved

1.3.473 CMP2_SW0

Comparator Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP2_SW0: 0x5AD0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	vp_ag7	vp_ag6	vp_ag5	vp_ag4	vp_ag3	vp_ag2	vp_ag1	vp_ag0

Bits	Name	Description
7	vp_ag7	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-398.
6	vp_ag6	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-398.
5	vp_ag5	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-398.
4	vp_ag4	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-398.
3	vp_ag3	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-398.
2	vp_ag2	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-398.
1	vp_ag1	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-398.
0	vp_ag0	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-398.

Table 1-398. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.474 CMP2_SW2

Comparator Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP2_SW2: 0x5AD2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:0	R/W:0
HW Access	NA						R	R
Retention	NA						RET	RET
Name	RSVD						vp_abus1	vp_abus0

Bits	Name	Description
1	vp_abus1	Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-399.
0	vp_abus0	Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-399.

Table 1-399. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.475 CMP2_SW3

Comparator Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP2_SW3: 0x5AD3

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:0	R/W:0	R/W:0	NA:00		R/W:0
HW Access	NA	R	R	R	R	NA		R
Retention	NA	RET	RET	RET	RET	NA		RET
Name	RSVD	vn_vref1	vn_vref0	vn_amx	vp_refbuf	RSVD		vp_amx

Bits	Name	Description
6	vn_vref1	Connect negative voltage input to Voltage Reference 1 See Table 1-402.
5	vn_vref0	Connect negative voltage input to Voltage Reference 0 See Table 1-402.
4	vn_amx	Connect negative voltage input to Analog Mux Bus See Table 1-400.
3	vp_refbuf	Connect positive voltage input to CapSense reference buffer channel See Table 1-401.
0	vp_amx	Connect positive voltage input to Analog Mux Bus See Table 1-400.

Table 1-400. Bit field encoding: AMX_ENUM

Value	Name	Description
1'b0	AMX_NC	not connected
1'b1	AMX_CONNECTED	Connect to AMUXBUS

Table 1-401. Bit field encoding: VP_REFBUF_ENUM

Value	Name	Description
1'b0	VP_REFBUF_ENABLED	disable
1'b1	VP_REFBUF_DISABLED	enable

Table 1-402. Bit field encoding: VREF_ENUM

Value	Name	Description
1'b0	VREF_NC	not connected
1'b1	VREF_CONNECTED	Connect to Voltage Reference

1.3.476 CMP2_SW4

Comparator Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP2_SW4: 0x5AD4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0
HW Access	R	NA	R	NA	R	NA	R	NA
Retention	RET	NA	RET	NA	RET	NA	RET	NA
Name	vn_ag7	RSVD	vn_ag5	RSVD	vn_ag3	RSVD	vn_ag1	RSVD

Bits	Name	Description
7	vn_ag7	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-403.
5	vn_ag5	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-403.
3	vn_ag3	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-403.
1	vn_ag1	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-403.

Table 1-403. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.477 CMP2_SW6

Comparator Analog Routing Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP2_SW6: 0x5AD6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	NA:00	
HW Access	NA				R	R	NA	
Retention	NA				RET	RET	NA	
Name	RSVD				vn_abus3	vn_abus2	RSVD	

Bits	Name	Description
3	vn_abus3	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-404.
2	vn_abus2	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-404.

Table 1-404. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.478 CMP2_CLK

Comparator Clock Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP2_CLK: 0x5AD7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:000		
HW Access	NA			R	R	R		
Retention	NA			RET	RET	RET		
Name	RSVD			bypass_sync	clk_en	mx_clk		

Bits	Name	Description
4	bypass_sync	Bypass Synchronization See Table 1-405.
3	clk_en	Clock gating control See Table 1-406.
2:0	mx_clk[2:0]	Clock Selection See Table 1-407.

Table 1-405. Bit field encoding: BYPASS_SYNC_ENUM

Value	Name	Description
1'b0	BYPASS_SYNC_0	Synchronization not bypassed (Synchronization enabled)
1'b1	BYPASS_SYNC_1	Synchronization bypassed (Synchronization disabled)

Table 1-406. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	CLK_EN_0	disable clock
1'b1	CLK_EN_1	enable clock

Table 1-407. Bit field encoding: MX_CLK_ENUM

Value	Name	Description
3'h0	MX_CLK_0	Select clk_a0 and clk_a0_dig
3'h1	MX_CLK_1	Select clk_a1 and clk_a1_dig
3'h2	MX_CLK_2	Select clk_a2 and clk_a2_dig
3'h3	MX_CLK_3	Select clk_a3 and clk_a3_dig
3'h4	MX_CLK_4	Select UDB generated clock
3'h5	MX_CLK_5	Reserved
3'h6	MX_CLK_6	Reserved
3'h7	MX_CLK_7	Reserved

1.3.479 CMP3_SW0

Comparator Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP3_SW0: 0x5AD8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	vp_ag7	vp_ag6	vp_ag5	vp_ag4	vp_ag3	vp_ag2	vp_ag1	vp_ag0

Bits	Name	Description
7	vp_ag7	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-408.
6	vp_ag6	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-408.
5	vp_ag5	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-408.
4	vp_ag4	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-408.
3	vp_ag3	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-408.
2	vp_ag2	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-408.
1	vp_ag1	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-408.
0	vp_ag0	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-408.

Table 1-408. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.480 CMP3_SW2

Comparator Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP3_SW2: 0x5ADA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:0	R/W:0
HW Access	NA						R	R
Retention	NA						RET	RET
Name	RSVD						vp_abus1	vp_abus0

Bits	Name	Description
1	vp_abus1	Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-409.
0	vp_abus0	Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-409.

Table 1-409. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.481 CMP3_SW3

Comparator Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP3_SW3: 0x5ADB

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:0	R/W:0	R/W:0	NA:00		R/W:0
HW Access	NA	R	R	R	R	NA		R
Retention	NA	RET	RET	RET	RET	NA		RET
Name	RSVD	vn_vref1	vn_vref0	vn_amx	vp_refbuf	RSVD		vp_amx

Bits	Name	Description
6	vn_vref1	Connect negative voltage input to Voltage Reference 1 See Table 1-412.
5	vn_vref0	Connect negative voltage input to Voltage Reference 0 See Table 1-412.
4	vn_amx	Connect negative voltage input to Analog Mux Bus See Table 1-410.
3	vp_refbuf	Connect positive voltage input to CapSense reference buffer channel See Table 1-411.
0	vp_amx	Connect positive voltage input to Analog Mux Bus See Table 1-410.

Table 1-410. Bit field encoding: AMX_ENUM

Value	Name	Description
1'b0	AMX_NC	not connected
1'b1	AMX_CONNECTED	Connect to AMUXBUS

Table 1-411. Bit field encoding: VP_REFBUF_ENUM

Value	Name	Description
1'b0	VP_REFBUF_ENABLED	disable
1'b1	VP_REFBUF_DISABLED	enable

Table 1-412. Bit field encoding: VREF_ENUM

Value	Name	Description
1'b0	VREF_NC	not connected
1'b1	VREF_CONNECTED	Connect to Voltage Reference

1.3.482 CMP3_SW4

Comparator Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP3_SW4: 0x5ADC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0
HW Access	R	NA	R	NA	R	NA	R	NA
Retention	RET	NA	RET	NA	RET	NA	RET	NA
Name	vn_ag7	RSVD	vn_ag5	RSVD	vn_ag3	RSVD	vn_ag1	RSVD

Bits	Name	Description
7	vn_ag7	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-413.
5	vn_ag5	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-413.
3	vn_ag3	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-413.
1	vn_ag1	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-413.

Table 1-413. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.483 CMP3_SW6

Comparator Analog Routing Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP3_SW6: 0x5ADE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	NA:00	
HW Access	NA				R	R	NA	
Retention	NA				RET	RET	NA	
Name	RSVD				vn_abus3	vn_abus2	RSVD	

Bits	Name	Description
3	vn_abus3	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-414.
2	vn_abus2	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-414.

Table 1-414. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.484 CMP3_CLK

Comparator Clock Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

CMP3_CLK: 0x5ADF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:000		
HW Access	NA			R	R	R		
Retention	NA			RET	RET	RET		
Name	RSVD			bypass_sync	clk_en	mx_clk		

Bits	Name	Description
4	bypass_sync	Bypass Synchronization See Table 1-415.
3	clk_en	Clock gating control See Table 1-416.
2:0	mx_clk[2:0]	Clock Selection See Table 1-417.

Table 1-415. Bit field encoding: BYPASS_SYNC_ENUM

Value	Name	Description
1'b0	BYPASS_SYNC_0	Synchronization not bypassed (Synchronization enabled)
1'b1	BYPASS_SYNC_1	Synchronization bypassed (Synchronization disabled)

Table 1-416. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	CLK_EN_0	disable clock
1'b1	CLK_EN_1	enable clock

Table 1-417. Bit field encoding: MX_CLK_ENUM

Value	Name	Description
3'h0	MX_CLK_0	Select clk_a0 and clk_a0_dig
3'h1	MX_CLK_1	Select clk_a1 and clk_a1_dig
3'h2	MX_CLK_2	Select clk_a2 and clk_a2_dig
3'h3	MX_CLK_3	Select clk_a3 and clk_a3_dig
3'h4	MX_CLK_4	Select UDB generated clock
3'h5	MX_CLK_5	Reserved
3'h6	MX_CLK_6	Reserved
3'h7	MX_CLK_7	Reserved

1.3.485 DSM0_SW0

Delta Sigma Modulator Analog Routing Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_SW0: 0x5B00

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	vp_ag7	vp_ag6	vp_ag5	vp_ag4	vp_ag3	vp_ag2	vp_ag1	vp_ag0

Bits	Name	Description
7	vp_ag7	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-418.
6	vp_ag6	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-418.
5	vp_ag5	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-418.
4	vp_ag4	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-418.
3	vp_ag3	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-418.
2	vp_ag2	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-418.
1	vp_ag1	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-418.
0	vp_ag0	Connect positive voltage input to analog global of same side (see field instance name) See Table 1-418.

Table 1-418. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.486 DSM0_SW2

Delta Sigma Modulator Analog Routing Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_SW2: 0x5B02

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	NA:0	R/W:0
HW Access	NA					R	NA	R
Retention	NA					RET	NA	RET
Name	RSVD					vp_abus2	RSVD	vp_abus0

Bits	Name	Description
2	vp_abus2	Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-419.
0	vp_abus0	Connect positive voltage input to analog (local) bus of the same side (see field instance name) See Table 1-419.

Table 1-419. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.487 DSM0_SW3

Delta Sigma Modulator Analog Routing Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_SW3: 0x5B03

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:0	NA:00		R/W:0	NA:0	R/W:0
HW Access	NA	R	R	NA		R	NA	R
Retention	NA	RET	RET	NA		RET	NA	RET
Name	RSVD	vn_vssa	vn_vref	RSVD		vp_vssa	RSVD	vp_amx

Bits	Name	Description
6	vn_vssa	Connect negative voltage input to vssa See Table 1-422.
5	vn_vref	Connect negative voltage input to Voltage Reference See Table 1-421.
2	vp_vssa	Connect positive voltage input to vssa See Table 1-422.
0	vp_amx	Connect positive voltage input to Analog Mux Bus See Table 1-420.

Table 1-420. Bit field encoding: AMX_ENUM

Value	Name	Description
1'b0	AMX_NC	not connected
1'b1	AMX_CONNECTED	Connect to AMUXBUS

Table 1-421. Bit field encoding: VREF_ENUM

Value	Name	Description
1'b0	VREF_NC	not connected
1'b1	VREF_CONNECTED	Connect to Voltage Reference

Table 1-422. Bit field encoding: VSSA_ENUM

Value	Name	Description
1'b0	VSSA_NC	not connected
1'b1	VSSA_CONNECTED	Connect to vssa

1.3.488 DSM0_SW4

Delta Sigma Modulator Analog Routing Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_SW4: 0x5B04

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0	R/W:0	NA:0
HW Access	R	NA	R	NA	R	NA	R	NA
Retention	RET	NA	RET	NA	RET	NA	RET	NA
Name	vn_ag7	RSVD	vn_ag5	RSVD	vn_ag3	RSVD	vn_ag1	RSVD

Bits	Name	Description
7	vn_ag7	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-423.
5	vn_ag5	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-423.
3	vn_ag3	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-423.
1	vn_ag1	Connect negative voltage input to analog global of same side (see field instance name) See Table 1-423.

Table 1-423. Bit field encoding: AG_ENUM

Value	Name	Description
1'b0	AG_NC	not connected
1'b1	AG_CONNECTED	Connect to Analog Global

1.3.489 DSM0_SW6

Delta Sigma Modulator Analog Routing Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_SW6: 0x5B06

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	NA:0	R/W:0	NA:0
HW Access	NA				R	NA	R	NA
Retention	NA				RET	NA	RET	NA
Name	RSVD				vn_abus3	RSVD	vn_abus1	RSVD

Bits	Name	Description
3	vn_abus3	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-424.
1	vn_abus1	Connect negative voltage input to analog (local) bus of the same side (see field instance name) See Table 1-424.

Table 1-424. Bit field encoding: ABUS_ENUM

Value	Name	Description
1'b0	ABUS_NC	not connected
1'b1	ABUS_CONNECTED	Connect to Analog (local) Bus

1.3.490 DSM0_CLK

Delta Sigma Modulator Clock Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DSM0_CLK: 0x5B07

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:000		
HW Access	NA			R	R	R		
Retention	NA			RET	RET	RET		
Name	RSVD			bypass_sync	clk_en	mx_clk		

Bits	Name	Description
4	bypass_sync	Bypass Synchronization See Table 1-425.
3	clk_en	Clock gating control See Table 1-426.
2:0	mx_clk[2:0]	Clock Selection See Table 1-427.

Table 1-425. Bit field encoding: BYPASS_SYNC_ENUM

Value	Name	Description
1'b0	BYPASS_SYNC_0	Synchronization not bypassed (Synchronization enabled)
1'b1	BYPASS_SYNC_1	Synchronization bypassed (Synchronization disabled)

Table 1-426. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	CLK_EN_0	disable clock
1'b1	CLK_EN_1	enable clock

Table 1-427. Bit field encoding: MX_CLK_ENUM

Value	Name	Description
3'h0	MX_CLK_0	Select clk_a0 and clk_a0_dig
3'h1	MX_CLK_1	Select clk_a1 and clk_a1_dig
3'h2	MX_CLK_2	Select clk_a2 and clk_a2_dig
3'h3	MX_CLK_3	Select clk_a3 and clk_a3_dig
3'h4	MX_CLK_4	Select UDB generated clock
3'h5	MX_CLK_5	Reserved
3'h6	MX_CLK_6	Reserved
3'h7	MX_CLK_7	Reserved

1.3.491 OPAMP0_MX

Analog Buffer Input Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

OPAMP0_MX: 0x5B40

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:00		R/W:0000			
HW Access	NA		R		R			
Retention	NA		RET		RET			
Name	RSVD		mx_vn		mx_vp			

Bits	Name	Description
5:4	mx_vn[1:0]	Mux Select VN See Table 1-428.
3:0	mx_vp[3:0]	Mux Select VP See Table 1-429.

Table 1-428. Bit field encoding: OPAMP0_MX_VN_ENUM

Value	Name	Description
2'h0	OPAMP0_MX_VN_DEFAULT	Default - Not Connected (NC)
2'h1	OPAMP0_MX_VN_AG4	Mux Selection AGL[4]
2'h2	OPAMP0_MX_VN_AG6	Mux Selection AGL[6]
2'h3	OPAMP0_MX_VN_0x3	Reserved (NC)

Table 1-429. Bit field encoding: OPAMP0_MX_VP_ENUM

Value	Name	Description
4'h0	OPAMP0_MX_VP_DEFAULT	Default - Not Connected (NC)
4'h1	OPAMP0_MX_VP_AG4	Mux Selection: AGL[4]
4'h2	OPAMP0_MX_VP_AG5	Mux Selection: AGL[5]
4'h3	OPAMP0_MX_VP_AG6	Mux Selection: AGL[6]
4'h4	OPAMP0_MX_VP_AG7	Mux Selection: AGL[7]
4'h5	OPAMP0_MX_VP_ABUS0	Mux Selection: ABUSL[0]
4'h6	OPAMP0_MX_VP_ABUS1	Mux Selection: ABUSL[1]
4'h7	OPAMP0_MX_VP_ABUS2	Mux Selection: ABUSL[2]
4'h8	OPAMP0_MX_VP_ABUS3	Mux Selection: ABUSL[3]
4'h9	OPAMP0_MX_VP_VREF	Mux Selection: OPAMP Voltage Reference
4'ha	OPAMP0_MX_VP_H_0xA	Reserved (NC)
4'hb	OPAMP0_MX_VP_H_0xB	Reserved (NC)

(continued)

Table 1-429. Bit field encoding: OPAMP0_MX_VP_ENUM

4'hc	OPAMP0_MX_VP_H_0xC	Reserved (NC)
4'hd	OPAMP0_MX_VP_H_0xD	Reserved (NC)
4'he	OPAMP0_MX_VP_H_0xE	Reserved (NC)
4'hf	OPAMP0_MX_VP_H_0xF	Reserved (NC)

1.3.492 OPAMP0_SW

Analog Buffer Routing Switch Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

OPAMP0_SW: 0x5B41

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	R/W:0	R/W:0
HW Access	NA					R	R	R
Retention	NA					RET	RET	RET
Name	RSVD					swinp	swinn	swfol

Bits	Name	Description
2	swinp	Switch Enable Positive Input
1	swinn	Switch Enable Negative Input
0	swfol	Switch Enable Follow

1.3.493 OPAMP1_MX

Analog Buffer Input Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

OPAMP1_MX: 0x5B42

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:00		R/W:0000			
HW Access	NA		R		R			
Retention	NA		RET		RET			
Name	RSVD		mx_vn		mx_vp			

Bits	Name	Description
5:4	mx_vn[1:0]	Mux Select VN See Table 1-430.
3:0	mx_vp[3:0]	Mux Select VP See Table 1-431.

Table 1-430. Bit field encoding: OPAMP1_MX_VN_ENUM

Value	Name	Description
2'h0	OPAMP1_MX_VN_DEFAULT	Default - Not Connected (NC)
2'h1	OPAMP1_MX_VN_AG4	Mux Selection AGR[4]
2'h2	OPAMP1_MX_VN_AG6	Mux Selection AGR[6]
2'h3	OPAMP1_MX_VN_0x3	Reserved (NC)

Table 1-431. Bit field encoding: OPAMP1_MX_VP_ENUM

Value	Name	Description
4'h0	OPAMP1_MX_VP_DEFAULT	Default - Not Connected (NC)
4'h1	OPAMP1_MX_VP_AG4	Mux Selection: AGR[4]
4'h2	OPAMP1_MX_VP_AG5	Mux Selection: AGR[5]
4'h3	OPAMP1_MX_VP_AG6	Mux Selection: AGR[6]
4'h4	OPAMP1_MX_VP_AG7	Mux Selection: AGR[7]
4'h5	OPAMP1_MX_VP_ABUS0	Mux Selection: ABUSR[0]
4'h6	OPAMP1_MX_VP_ABUS1	Mux Selection: ABUSR[1]
4'h7	OPAMP1_MX_VP_ABUS2	Mux Selection: ABUSR[2]
4'h8	OPAMP1_MX_VP_ABUS3	Mux Selection: ABUSR[3]
4'h9	OPAMP1_MX_VP_VREF	Mux Selection: OPAMP Voltage Reference
4'ha	OPAMP1_MX_VP_H_0xA	Reserved (NC)
4'hb	OPAMP1_MX_VP_H_0xB	Reserved (NC)

(continued)

Table 1-431. Bit field encoding: OPAMP1_MX_VP_ENUM

4'hc	OPAMP1_MX_VP_H_0xC	Reserved (NC)
4'hd	OPAMP1_MX_VP_H_0xD	Reserved (NC)
4'he	OPAMP1_MX_VP_H_0xE	Reserved (NC)
4'hf	OPAMP1_MX_VP_H_0xF	Reserved (NC)

1.3.494 OPAMP1_SW

Analog Buffer Routing Switch Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

OPAMP1_SW: 0x5B43

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	R/W:0	R/W:0
HW Access	NA					R	R	R
Retention	NA					RET	RET	RET
Name	RSVD					swinp	swinn	swfol

Bits	Name	Description
2	swinp	Switch Enable Positive Input
1	swinn	Switch Enable Negative Input
0	swfol	Switch Enable Follow

1.3.495 OPAMP2_MX

Analog Buffer Input Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

OPAMP2_MX: 0x5B44

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:00		R/W:0000			
HW Access	NA		R		R			
Retention	NA		RET		RET			
Name	RSVD		mx_vn		mx_vp			

Bits	Name	Description
5:4	mx_vn[1:0]	Mux Select VN See Table 1-432.
3:0	mx_vp[3:0]	Mux Select VP See Table 1-433.

Table 1-432. Bit field encoding: OPAMP2_MX_VN_ENUM

Value	Name	Description
2'h0	OPAMP2_MX_VN_DEFAULT	Default - Not Connected (NC)
2'h1	OPAMP2_MX_VN_AG5	Mux Selection AGL[5]
2'h2	OPAMP2_MX_VN_AG7	Mux Selection AGL[7]
2'h3	OPAMP2_MX_VN_0x3	Reserved (NC)

Table 1-433. Bit field encoding: OPAMP2_MX_VP_ENUM

Value	Name	Description
4'h0	OPAMP2_MX_VP_DEFAULT	Default - Not Connected (NC)
4'h1	OPAMP2_MX_VP_AG4	Mux Selection: AGL[4]
4'h2	OPAMP2_MX_VP_AG5	Mux Selection: AGL[5]
4'h3	OPAMP2_MX_VP_AG6	Mux Selection: AGL[6]
4'h4	OPAMP2_MX_VP_AG7	Mux Selection: AGL[7]
4'h5	OPAMP2_MX_VP_ABUS0	Mux Selection: ABUSL[0]
4'h6	OPAMP2_MX_VP_ABUS1	Mux Selection: ABUSL[1]
4'h7	OPAMP2_MX_VP_ABUS2	Mux Selection: ABUSL[2]
4'h8	OPAMP2_MX_VP_ABUS3	Mux Selection: ABUSL[3]
4'h9	OPAMP2_MX_VP_VREF	Mux Selection: OPAMP Voltage Reference
4'ha	OPAMP2_MX_VP_H_0xA	Reserved (NC)
4'hb	OPAMP2_MX_VP_H_0xB	Reserved (NC)

(continued)

Table 1-433. Bit field encoding: OPAMP2_MX_VP_ENUM

4'hc	OPAMP2_MX_VP_H_0xC	Reserved (NC)
4'hd	OPAMP2_MX_VP_H_0xD	Reserved (NC)
4'he	OPAMP2_MX_VP_H_0xE	Reserved (NC)
4'hf	OPAMP2_MX_VP_H_0xF	Reserved (NC)

1.3.496 OPAMP2_SW

Analog Buffer Routing Switch Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

OPAMP2_SW: 0x5B45

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	R/W:0	R/W:0
HW Access	NA					R	R	R
Retention	NA					RET	RET	RET
Name	RSVD					swinp	swinn	swfol

Bits	Name	Description
2	swinp	Switch Enable Positive Input
1	swinn	Switch Enable Negative Input
0	swfol	Switch Enable Follow

1.3.497 OPAMP3_MX

Analog Buffer Input Selection Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

OPAMP3_MX: 0x5B46

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:00		R/W:0000			
HW Access	NA		R		R			
Retention	NA		RET		RET			
Name	RSVD		mx_vn		mx_vp			

Bits	Name	Description
5:4	mx_vn[1:0]	Mux Select VN See Table 1-434.
3:0	mx_vp[3:0]	Mux Select VP See Table 1-435.

Table 1-434. Bit field encoding: OPAMP3_MX_VN_ENUM

Value	Name	Description
2'h0	OPAMP3_MX_VN_DEFAULT	Default - Not Connected (NC)
2'h1	OPAMP3_MX_VN_AG5	Mux Selection AGR[5]
2'h2	OPAMP3_MX_VN_AG7	Mux Selection AGR[7]
2'h3	OPAMP3_MX_VN_0x3	Reserved (NC)

Table 1-435. Bit field encoding: OPAMP3_MX_VP_ENUM

Value	Name	Description
4'h0	OPAMP3_MX_VP_DEFAULT	Default - Not Connected (NC)
4'h1	OPAMP3_MX_VP_AG4	Mux Selection: AGR[4]
4'h2	OPAMP3_MX_VP_AG5	Mux Selection: AGR[5]
4'h3	OPAMP3_MX_VP_AG6	Mux Selection: AGR[6]
4'h4	OPAMP3_MX_VP_AG7	Mux Selection: AGR[7]
4'h5	OPAMP3_MX_VP_ABUS0	Mux Selection: ABUSR[0]
4'h6	OPAMP3_MX_VP_ABUS1	Mux Selection: ABUSR[1]
4'h7	OPAMP3_MX_VP_ABUS2	Mux Selection: ABUSR[2]
4'h8	OPAMP3_MX_VP_ABUS3	Mux Selection: ABUSR[3]
4'h9	OPAMP3_MX_VP_VREF	Mux Selection: OPAMP Voltage Reference
4'ha	OPAMP3_MX_VP_H_0xA	Reserved (NC)
4'hb	OPAMP3_MX_VP_H_0xB	Reserved (NC)

(continued)

Table 1-435. Bit field encoding: OPAMP3_MX_VP_ENUM

4'hc	OPAMP3_MX_VP_H_0xC	Reserved (NC)
4'hd	OPAMP3_MX_VP_H_0xD	Reserved (NC)
4'he	OPAMP3_MX_VP_H_0xE	Reserved (NC)
4'hf	OPAMP3_MX_VP_H_0xF	Reserved (NC)

1.3.498 OPAMP3_SW

Analog Buffer Routing Switch Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

OPAMP3_SW: 0x5B47

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	R/W:0	R/W:0
HW Access	NA					R	R	R
Retention	NA					RET	RET	RET
Name	RSVD					swinp	swinn	swfol

Bits	Name	Description
2	swinp	Switch Enable Positive Input
1	swinn	Switch Enable Negative Input
0	swfol	Switch Enable Follow

1.3.499 LCDDAC_SW0

LCDDAC Switch Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LCDDAC_SW0: 0x5B50

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:000		
HW Access	NA					R		
Retention	NA					RET		
Name	RSVD					sw0		

Bits	Name	Description
2:0	sw0[2:0]	Switch Control for LCD_BIAS_BUS[0] See Table 1-436.

Table 1-436. Bit field encoding: LCDDAC_SW0_ENUM

Value	Name	Description
3'h0	LCDDAC_SW0_NC	NC
3'h1	LCDDAC_SW0_LCDDAC_V0	LCDDAC_V0 connected to LCD_BIAS_BUS[0]
3'h2	LCDDAC_SW0_ABUSR0	ABUSR[0] connected to LCD_BIAS_BUS[0]
3'h3	LCDDAC_SW0_3	LCDDAC_V0 and ABUSR[0] connected to LCD_BIAS_BUS[0]
3'h4	LCDDAC_SW0_ABUSR1	ABUSR[1] connected to LCD_BIAS_BUS[0]
3'h5	LCDDAC_SW0_5	LCDDAC_V0 and ABUSR[1] connected to LCD_BIAS_BUS[0]
3'h6	LCDDAC_SW0_6	ABUSR[0] and ABUSR[1] connected to LCD_BIAS_BUS[0]
3'h7	LCDDAC_SW0_7	LCDDAC_V0 and ABUSR[0] and ABUSR[1] connected to LCD_BIAS_BUS[0]

1.3.500 LCDDAC_SW1

LCDDAC Switch Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LCDDAC_SW1: 0x5B51

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:000		
HW Access	NA					R		
Retention	NA					RET		
Name	RSVD					sw1		

Bits	Name	Description
2:0	sw1[2:0]	Switch Control for LCD_BIAS_BUS[1] See Table 1-437.

Table 1-437. Bit field encoding: LCDDAC_SW1_ENUM

Value	Name	Description
3'h0	LCDDAC_SW1_NC	NC
3'h1	LCDDAC_SW1_LCDDAC_V1	LCDDAC_V1 connected to LCD_BIAS_BUS[1]
3'h2	LCDDAC_SW1_ABUSL0	ABUSL[0] connected to LCD_BIAS_BUS[1]
3'h3	LCDDAC_SW1_3	LCDDAC_V1 and ABUSL[0] connected to LCD_BIAS_BUS[1]
3'h4	LCDDAC_SW1_ABUSL1	ABUSL[1] connected to LCD_BIAS_BUS[1]
3'h5	LCDDAC_SW1_5	LCDDAC_V1 and ABUSL[1] connected to LCD_BIAS_BUS[1]
3'h6	LCDDAC_SW1_6	ABUSL[0] and ABUSL[1] connected to LCD_BIAS_BUS[1]
3'h7	LCDDAC_SW1_7	LCDDAC_V1 and ABUSL[0] and ABUSL[1] connected to LCD_BIAS_BUS[1]

1.3.501 LCDDAC_SW2

LCDDAC Switch Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LCDDAC_SW2: 0x5B52

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:000		
HW Access	NA					R		
Retention	NA					RET		
Name	RSVD					sw2		

Bits	Name	Description
2:0	sw2[2:0]	Switch Control for LCD_BIAS_BUS[2] See Table 1-438.

Table 1-438. Bit field encoding: LCDDAC_SW2_ENUM

Value	Name	Description
3'h0	LCDDAC_SW2_NC	NC
3'h1	LCDDAC_SW2_LCDDAC_V2	LCDDAC_V2 connected to LCD_BIAS_BUS[2]
3'h2	LCDDAC_SW2_ABUSR2	ABUSR[2] connected to LCD_BIAS_BUS[2]
3'h3	LCDDAC_SW2_3	LCDDAC_V2 and ABUSR[2] connected to LCD_BIAS_BUS[2]
3'h4	LCDDAC_SW2_ABUSR3	ABUSR[3] connected to LCD_BIAS_BUS[2]
3'h5	LCDDAC_SW2_5	LCDDAC_V2 and ABUSR[3] connected to LCD_BIAS_BUS[2]
3'h6	LCDDAC_SW2_6	ABUSR[2] and ABUSR[3] connected to LCD_BIAS_BUS[2]
3'h7	LCDDAC_SW2_7	LCDDAC_V2 and ABUSR[2] and ABUSR[3] connected to LCD_BIAS_BUS[2]

1.3.502 LCDDAC_SW3

LCDDAC Switch Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LCDDAC_SW3: 0x5B53

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:000		
HW Access	NA					R		
Retention	NA					RET		
Name	RSVD					sw3		

Bits	Name	Description
2:0	sw3[2:0]	Switch Control for LCD_BIAS_BUS[3] See Table 1-439.

Table 1-439. Bit field encoding: LCDDAC_SW3_ENUM

Value	Name	Description
3'h0	LCDDAC_SW3_NC	NC
3'h1	LCDDAC_SW3_LCDDAC_V3	LCDDAC_V3 connected to LCD_BIAS_BUS[3]
3'h2	LCDDAC_SW3_ABUSL2	ABUSL[2] connected to LCD_BIAS_BUS[3]
3'h3	LCDDAC_SW3_3	LCDDAC_V3 and ABUSL[2] connected to LCD_BIAS_BUS[3]
3'h4	LCDDAC_SW3_ABUSL3	ABUSL[3] connected to LCD_BIAS_BUS[3]
3'h5	LCDDAC_SW3_5	LCDDAC_V3 and ABUSL[3] connected to LCD_BIAS_BUS[3]
3'h6	LCDDAC_SW3_6	ABUSL[2] and ABUSL[3] connected to LCD_BIAS_BUS[3]
3'h7	LCDDAC_SW3_7	LCDDAC_V3 and ABUSL[2] and ABUSL[3] connected to LCD_BIAS_BUS[3]

1.3.503 LCDDAC_SW4

LCDDAC Switch Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LCDDAC_SW4: 0x5B54

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:000		
HW Access	NA					R		
Retention	NA					RET		
Name	RSVD					sw4		

Bits	Name	Description
2:0	sw4[2:0]	Switch Control for LCD_BIAS_BUS[4] See Table 1-440.

Table 1-440. Bit field encoding: LCDDAC_SW4_ENUM

Value	Name	Description
3'h0	LCDDAC_SW4_NC	NC
3'h1	LCDDAC_SW4_LCDDAC_V4	LCDDAC_V4 connected to LCD_BIAS_BUS[4]
3'h2	LCDDAC_SW4_AMUXBUSR	AMUXBUSR connected to LCD_BIAS_BUS[4]
3'h3	LCDDAC_SW4_3	LCDDAC_V4 and AMUXBUSR connected to LCD_BIAS_BUS[4]
3'h4	LCDDAC_SW4_AMUXBUSL	AMUXBUSL connected to LCD_BIAS_BUS[4]
3'h5	LCDDAC_SW4_5	LCDDAC_V4 and AMUXBUSL connected to LCD_BIAS_BUS[4]
3'h6	LCDDAC_SW4_6	AMUXBUSR and AMUXBUSL connected to LCD_BIAS_BUS[4]
3'h7	LCDDAC_SW4_7	LCDDAC_V4 and AMUXBUSR and AMUXBUSL connected to LCD_BIAS_BUS[4]

1.3.504 SC_MISC

Switched Cap Miscellaneous Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC_MISC: 0x5B56

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	NA:00		R/W:0	R/W:0
HW Access	NA		R	R	NA		R	R
Retention	NA		RET	RET	NA		RET	RET
Name	RSVD		sc_pump_force	sc_pump_auto	RSVD		diff_pga_1_3	diff_pga_0_2

Bits	Name	Description
5	sc_pump_force	force pumping - if block enabled enable pump regardless of voltage state
4	sc_pump_auto	enable autopumping - if block enabled pump when low voltage detected
1	diff_pga_1_3	Switched Cap Pair Connect for Differential Amplifier Applications See Table 1-441.
0	diff_pga_0_2	Switched Cap Pair Connect for Differential Amplifier Applications See Table 1-441.

Table 1-441. Bit field encoding: SC_DIFF_PGA_ENUM

Value	Name	Description
1'h0	SC_DIFF_PGA_DISABLED	Differential PGA pair connect disabled
1'h1	SC_DIFF_PGA_ENABLED	Differential PGA pair connect enabled

1.3.505 BUS_SW0

Bus Switch Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BUS_SW0: 0x5B58

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	ag7	ag6	ag5	ag4	ag3	ag2	ag1	ag0

Bits	Name	Description
7	ag7	Connect Left and Right Analog Globals See Table 1-449.
6	ag6	Connect Left and Right Analog Globals See Table 1-448.
5	ag5	Connect Left and Right Analog Globals See Table 1-447.
4	ag4	Connect Left and Right Analog Globals See Table 1-446.
3	ag3	Connect Left and Right Analog Globals See Table 1-445.
2	ag2	Connect Left and Right Analog Globals See Table 1-444.
1	ag1	Connect Left and Right Analog Globals See Table 1-443.
0	ag0	Connect Left and Right Analog Globals See Table 1-442.

Table 1-442. Bit field encoding: AG0_ENUM

Value	Name	Description
1'b0	AG0_NC	Disconnect AGL[0] and AGR[0]
1'b1	AG0_CONNECT	Connect AGL[0] and AGR[0]

Table 1-443. Bit field encoding: AG1_ENUM

Value	Name	Description
1'b0	AG1_NC	Disconnect AGL[1] and AGR[1]
1'b1	AG1_CONNECT	Connect AGL[1] and AGR[1]

(continued)

Table 1-444. Bit field encoding: AG2_ENUM

Value	Name	Description
1'b0	AG2_NC	Disconnect AGL[2] and AGR[2]
1'b1	AG2_CONNECT	Connect AGL[2] and AGR[2]

Table 1-445. Bit field encoding: AG3_ENUM

Value	Name	Description
1'b0	AG3_NC	Disconnect AGL[3] and AGR[3]
1'b1	AG3_CONNECT	Connect AGL[3] and AGR[3]

Table 1-446. Bit field encoding: AG4_ENUM

Value	Name	Description
1'b0	AG4_NC	Disconnect AGL[4] and AGR[4]
1'b1	AG4_CONNECT	Connect AGL[4] and AGR[4]

Table 1-447. Bit field encoding: AG5_ENUM

Value	Name	Description
1'b0	AG5_NC	Disconnect AGL[5] and AGR[5]
1'b1	AG5_CONNECT	Connect AGL[5] and AGR[5]

Table 1-448. Bit field encoding: AG6_ENUM

Value	Name	Description
1'b0	AG6_NC	Disconnect AGL[6] and AGR[6]
1'b1	AG6_CONNECT	Connect AGL[6] and AGR[6]

Table 1-449. Bit field encoding: AG7_ENUM

Value	Name	Description
1'b0	AG7_NC	Disconnect AGL[7] and AGR[7]
1'b1	AG7_CONNECT	Connect AGL[7] and AGR[7]

1.3.506 BUS_SW2

Bus Switch Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BUS_SW2: 0x5B5A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Retention	NA				RET	RET	RET	RET
Name	RSVD				abus3	abus2	abus1	abus0

Bits	Name	Description
3	abus3	Connect Left and Right Analog (local) Buses See Table 1-453.
2	abus2	Connect Left and Right Analog (local) Buses See Table 1-452.
1	abus1	Connect Left and Right Analog (local) Buses See Table 1-451.
0	abus0	Connect Left and Right Analog (local) Buses See Table 1-450.

Table 1-450. Bit field encoding: ABUS0_ENUM

Value	Name	Description
1'b0	ABUS0_NC	Disconnect ABUSL[0] and ABUSR[0]
1'b1	ABUS0_CONNECT	Connect ABUSL[0] and ABUSR[0]

Table 1-451. Bit field encoding: ABUS1_ENUM

Value	Name	Description
1'b0	ABUS1_NC	Disconnect ABUSL[1] and ABUSR[1]
1'b1	ABUS1_CONNECT	Connect ABUSL[1] and ABUSR[1]

Table 1-452. Bit field encoding: ABUS2_ENUM

Value	Name	Description
1'b0	ABUS2_NC	Disconnect ABUSL[2] and ABUSR[2]
1'b1	ABUS2_CONNECT	Connect ABUSL[2] and ABUSR[2]

Table 1-453. Bit field encoding: ABUS3_ENUM

Value	Name	Description
1'b0	ABUS3_NC	Disconnect ABUSL[3] and ABUSR[3]
1'b1	ABUS3_CONNECT	Connect ABUSL[3] and ABUSR[3]

1.3.507 BUS_SW3

Bus Switch Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BUS_SW3: 0x5B5B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:00		NA:0	R/W:0
HW Access	NA				R		NA	R
Retention	NA				RET		NA	RET
Name	RSVD				power2ag_sel		RSVD	amx

Bits	Name	Description
3:2	power2ag_sel[1:0]	Connect power pins to Analog Global See Table 1-455.
0	amx	Connect Left and Rigth Analog Mux Bus See Table 1-454.

Table 1-454. Bit field encoding: AMX_ENUM

Value	Name	Description
1'b0	AMX_NC	Disconnect AMXL and AMXR
1'b1	AMX_CONNECT	Connect AMXL and AMXR

Table 1-455. Bit field encoding: POWER2AG_SEL_ENUM

Value	Name	Description
2'h0	POWER2AG_SEL_NC	AGL[3] not connected to power pins
2'h1	POWER2AG_SEL_VDDA	AGL[3] connected to vdda
2'h2	POWER2AG_SEL_VDDD	AGL[3] connected to vddd
2'h3	POWER2AG_SEL_VBAT	AGL[3] connected to vbat (RC filtered)

1.3.508 DAC[0..3]_D

DAC Data Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DAC0_D: 0x5B80 DAC1_D: 0x5B81 DAC2_D: 0x5B82 DAC3_D: 0x5B83

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	data							

This register stores the DAC output data. This register is retained during low power modes, however the internal registers inside the DAC are not. To drive out DAC data upon return from low power modes, this register must be rewritten or the DAC must be strobed once.

Bits	Name	Description
7:0	data[7:0]	8 DAC data bits. These bits are retained in low power modes, but internal DAC state is not. To drive DAC data out upon return from lower power modes, this register must be rewritten or a DAC strobe supplied.

1.3.509 DSM[0..0]_OUT0

DSM Output Register 0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DSM0_OUT0: 0x5B88

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	dout							

Bits	Name	Description
7:0	dout[7:0]	DSM output

1.3.510 DSM[0..0]_OUT1

DSM Output Register 1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DSM0_OUT1: 0x5B89

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R:0	R:0	R:0000			
HW Access	NA		W	W	W			
Retention	NA		NONRET	NONRET	NONRET			
Name	RSVD		ovdcause	ovdflag	dout2scomp			

Bits	Name	Description
5	ovdcause	Overload Cause See Table 1-457.
4	ovdflag	Overload detected
3:0	dout2scomp[3:0]	DSM Output Register 1 See Table 1-456.

Table 1-456. Bit field encoding: DSM_DOUT2SCOMP_ENUM

Value	Name	Description
4'h0	DSM_DOUT2SCOMP_0	NA (qlev=00); 0 (qlev=01); 0 (qlev=10)
4'h1	DSM_DOUT2SCOMP_1	+1 (qlev=00); +1 (qlev=01); +1 (qlev=10)
4'h2	DSM_DOUT2SCOMP_2	NA (qlev=00); NA (qlev=01); +2 (qlev=10)
4'h3	DSM_DOUT2SCOMP_3	NA (qlev=00); NA (qlev=01); +3 (qlev=10)
4'h4	DSM_DOUT2SCOMP_4	NA (qlev=00); NA (qlev=01); +4 (qlev=10)
4'h5	DSM_DOUT2SCOMP_5	NA (qlev=00); NA (qlev=01); NA (qlev=10)
4'h6	DSM_DOUT2SCOMP_6	NA (qlev=00); NA (qlev=01); NA (qlev=10)
4'h7	DSM_DOUT2SCOMP_7	NA (qlev=00); NA (qlev=01); NA (qlev=10)
4'h8	DSM_DOUT2SCOMP_8	NA (qlev=00); NA (qlev=01); NA (qlev=10)
4'h9	DSM_DOUT2SCOMP_9	NA (qlev=00); NA (qlev=01); NA (qlev=10)
4'ha	DSM_DOUT2SCOMP_10	NA (qlev=00); NA (qlev=01); NA (qlev=10)
4'hb	DSM_DOUT2SCOMP_11	NA (qlev=00); NA (qlev=01); NA (qlev=10)
4'hc	DSM_DOUT2SCOMP_12	NA (qlev=00); NA (qlev=01); -4 (qlev=10)
4'hd	DSM_DOUT2SCOMP_13	NA (qlev=00); NA (qlev=01); -3 (qlev=10)
4'he	DSM_DOUT2SCOMP_14	NA (qlev=00); NA (qlev=01); -2 (qlev=10)
4'hf	DSM_DOUT2SCOMP_15	-1 (qlev=00); -1 (qlev=01); -1 (qlev=10)

Table 1-457. Bit field encoding: OVDCAUSE_ENUM

Value	Name	Description
1'b0	OVDCAUSE_0	0s overload
1'b1	OVDCAUSE_1	1s overload

1.3.511 LUT_SR

LUT Status Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

LUT_SR: 0x5B90

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				RC:0	RC:0	RC:0	RC:0
HW Access	NA				R/W	R/W	R/W	R/W
Retention	NA				NONRET	NONRET	NONRET	NONRET
Name	RSVD				lut3_out	lut2_out	lut1_out	lut0_out

Clear-on-read sticky status register

Bits	Name	Description
3	lut3_out	LUT output
2	lut2_out	LUT output
1	lut1_out	LUT output
0	lut0_out	LUT output

1.3.512 LUT_WRK1

Reserved

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LUT_WRK1: 0x5B91

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NA							
Name	RSVD							

Bits	Name	Description
7:0	RSVD[7:0]	Reserved

1.3.513 LUT_MSK

LUT Interrupt ReQuest (IRQ) Mask Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LUT_MSK: 0x5B92

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Retention	NA				RET	RET	RET	RET
Name	RSVD				lut3_msk	lut2_msk	lut1_msk	lut0_msk

Bits	Name	Description
3	lut3_msk	Enable LUT IRQ See Table 1-458.
2	lut2_msk	Enable LUT IRQ See Table 1-458.
1	lut1_msk	Enable LUT IRQ See Table 1-458.
0	lut0_msk	Enable LUT IRQ See Table 1-458.

Table 1-458. Bit field encoding: LUT_MSK_ENUM

Value	Name	Description
1'b1	LUT_MSK_ENABLE	enable LUT IRQ
1'b0	LUT_MSK_DISABLE	disable LUT IRQ

1.3.514 LUT_CLK

LUT CLK Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LUT_CLK: 0x5B93

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Retention	NA				RET	RET	RET	RET
Name	RSVD				lut3_en_clk	lut2_en_clk	lut1_en_clk	lut0_en_clk

LUT status clk gater control

Bits	Name	Description
3	lut3_en_clk	LUT status clock gater control See Table 1-459.
2	lut2_en_clk	LUT status clock gater control See Table 1-459.
1	lut1_en_clk	LUT status clock gater control See Table 1-459.
0	lut0_en_clk	LUT status clock gater control See Table 1-459.

Table 1-459. Bit field encoding: LUT_EN_CLK_ENUM

Value	Name	Description
1'b0	LUT_EN_CLK_DISABLE	LUT status clock disabled
1'b1	LUT_EN_CLK_ENABLE	LUT status clock enabled (must set this bit for LUT interrupts)

1.3.515 LUT_CPTR

LUT Capture Mode Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

LUT_CPTR: 0x5B94

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Retention	NA				RET	RET	RET	RET
Name	RSVD				lut3_capture_mode	lut2_capture_mode	lut1_capture_mode	lut0_capture_mode

LUT status capture mode

Bits	Name	Description
3	lut3_capture_mode	LUT status capture mode See Table 1-460.
2	lut2_capture_mode	LUT status capture mode See Table 1-460.
1	lut1_capture_mode	LUT status capture mode See Table 1-460.
0	lut0_capture_mode	LUT status capture mode See Table 1-460.

Table 1-460. Bit field encoding: LUT_CAPTURE_MODE_ENUM

Value	Name	Description
1'b0	LUT_CAPTURE_MODE_EDGE	LUT status edge capture mode
1'b1	LUT_CAPTURE_MODE_LEVEL	LUT status level capture mode

1.3.516 CMP_WRK

Comparator output working register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

CMP_WRK: 0x5B96

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R:0	R:0	R:0	R:0
HW Access	NA				W	W	W	W
Retention	NA				NONRET	NONRET	NONRET	NONRET
Name	RSVD				cmp3_out	cmp2_out	cmp1_out	cmp0_out

Bits	Name	Description
3	cmp3_out	Comparator Output
2	cmp2_out	Comparator Output
1	cmp1_out	Comparator Output
0	cmp0_out	Comparator Output

1.3.517 SC_SR

Switched Capacitor Status Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

SC_SR: 0x5B98

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				RC:0	RC:0	RC:0	RC:0
HW Access	NA				W	W	W	W
Retention	NA				NONRET	NONRET	NONRET	NONRET
Name	RSVD				sc3_modout	sc2_modout	sc1_modout	sc0_modout

Bits	Name	Description
3	sc3_modout	Switched Cap block modulator output
2	sc2_modout	Switched Cap block modulator output
1	sc1_modout	Switched Cap block modulator output
0	sc0_modout	Switched Cap block modulator output

1.3.518 SC_WRK1

Reserved

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC_WRK1: 0x5B99

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NA							
Name	RSVD							

Bits	Name	Description
7:0	RSVD[7:0]	Reserved

1.3.519 SC_MSK

SC IRQ Mask Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC_MSK: 0x5B9A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Retention	NA				RET	RET	RET	RET
Name	RSVD				sc3_msk	sc2_msk	sc1_msk	sc0_msk

Bits	Name	Description
3	sc3_msk	Enable SC IRQ See Table 1-461.
2	sc2_msk	Enable SC IRQ See Table 1-461.
1	sc1_msk	Enable SC IRQ See Table 1-461.
0	sc0_msk	Enable SC IRQ See Table 1-461.

Table 1-461. Bit field encoding: SC_MSK_ENUM

Value	Name	Description
1'b1	SC_MSK_ENABLE	enable SC IRQ
1'b0	SC_MSK_DISABLE	disable SC IRQ

1.3.520 SC_CMPINV

SC comparator inversion

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC_CMPINV: 0x5B9B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Retention	NA				RET	RET	RET	RET
Name	RSVD				sc3_cmpinv	sc2_cmpinv	sc1_cmpinv	sc0_cmpinv

Bits	Name	Description
3	sc3_cmpinv	Switched Cap modulator comparator output inversion control See Table 1-462.
2	sc2_cmpinv	Switched Cap modulator comparator output inversion control See Table 1-462.
1	sc1_cmpinv	Switched Cap modulator comparator output inversion control See Table 1-462.
0	sc0_cmpinv	Switched Cap modulator comparator output inversion control See Table 1-462.

Table 1-462. Bit field encoding: SC_CMPINV_ENUM

Value	Name	Description
1'b0	SC_CMPINV_DISABLE	Switched Cap modulator comparator output not inverted
1'b1	SC_CMPINV_ENABLE	Switched Cap modulator comparator output inverted

1.3.521 SC_CPTR

SC Capture Mode Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SC_CPTR: 0x5B9C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Retention	NA				RET	RET	RET	RET
Name	RSVD				sc3_capture_mode	sc2_capture_mode	sc1_capture_mode	sc0_capture_mode

SC status capture mode

Bits	Name	Description
3	sc3_capture_mode	SC status capture mode See Table 1-463.
2	sc2_capture_mode	SC status capture mode See Table 1-463.
1	sc1_capture_mode	SC status capture mode See Table 1-463.
0	sc0_capture_mode	SC status capture mode See Table 1-463.

Table 1-463. Bit field encoding: SC_CAPTURE_MODE_ENUM

Value	Name	Description
1'b0	SC_CAPTURE_MODE_EDGE	SC status edge capture mode
1'b1	SC_CAPTURE_MODE_LEVEL	SC status level capture mode

1.3.522 USB_EP0_DR[0..7]

Control End point EP0 Data Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_EP0_DR0: 0x6000 USB_EP0_DR1: 0x6001

USB_EP0_DR2: 0x6002 USB_EP0_DR3: 0x6003

USB_EP0_DR4: 0x6004 USB_EP0_DR5: 0x6005

USB_EP0_DR6: 0x6006 USB_EP0_DR7: 0x6007

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	data_byte							

The Endpoint 0 Data Register (EP0_DR) is used to read and write data to the USB control endpoint. The EP0_DR register has a hardware-locking feature that prevents the CPU write when SETUP is active. The registers are locked as soon as the SETUP token is decoded and remain locked throughout the SETUP transaction and until the EP0_CR register have been read. This is to prevent over-writing new SETUP data before firmware knows it has arrived. All other endpoint data buffers do not have this locking feature. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7:0	data_byte[7:0]	This register is shared for both transmit and receive. The count in the EP0_CNT register determines the number of bytes received or to be transferred.

1.3.523 USB_CR0

USB control 0 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_CR0: 0x6008

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0000000						
HW Access	R	R						
Retention	RET	RET						
Name	usb_enable	device_address						

The USB Control Register 0 (CR0) is used to set the PSoC3's USB address and enable the USB system resource. All bits in this register are reset to zero when a USB bus reset interrupt occurs. The IMO frequency should be set to 24MHz before USB is enabled. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	usb_enable	This bit enables the PSoC device to respond to USB traffic. 0 - USB disabled. 1 - USB enabled.
6:0	device_address[6:0]	These bits specify the USB device address to which the SIE will respond. This address must be set by firmware and is specified by the USB Host with a SET ADDRESS command during USB enumeration. This value must be programmed by firmware when assigned during enumeration. It is not set automatically by the hardware.

1.3.524 USB_CR1

USB control 1 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

USB_CR1: 0x6009

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/WZC:0	R/W:0	R/W:0
HW Access	NA				R	W	R	R
Retention	NA				RET	RET	RET	RET
Name	RSVD				trim_offset_msb	bus_activity	enable_lock	reg_enable

The USB Control Register 1 (CR1) is used to configure the internal regulator and the oscillator tuning capability. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
3	trim_offset_msb	This bit is enabled/disabled for using trim bit[7]. 0-enabled. 1-disabled.
2	bus_activity	The Bus Activity bit is a stickybit that detects any non-idle USB event that has occurred on the USB bus. Once set to High by the SIE to indicate the bus activity this bit retains its logical High value until firmware clears it. Writing a '0' to this bit clears it; writing a '1' preserves its value. 0 No activity. 1 Non-idle activity (D+ = Low) was detected since the last time the bit was cleared. Sticky (individual bits)
1	enable_lock	This bit is set to turn on the automatic frequency locking of the internal oscillator to USB traffic. Unless an external clock is being provided this bit should remain set for proper USB operation. 0 Locking disabled. 1 Locking enabled.
0	reg_enable	This bit controls the operation of the internal USB regulator. For applications with PSoC supply voltages in the 5V range this bit is set high to enable the internal regulator. For device supply voltage in the 3.3V range this bit is cleared to connect the transceiver directly to the supply. 0- Pass-through mode. Use for Vdd = 3.3V range. 1- Regulating mode. Use for Vdd = 5V range.

1.3.525 USB_SIE_EP_INT_EN

USB SIE Data Endpoints Interrupt Enable Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP_INT_EN: 0x600A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Retention	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET
Name	ep8_intr_en	ep7_intr_en	ep6_intr_en	ep5_intr_en	ep4_intr_en	ep3_intr_en	ep2_intr_en	ep1_intr_en

The USB SIE Data Endpoints Interrupt Enable Register (SIE_EP_INT_EN) is used to enable/ mask the Data Endpoint Interrupts This register is clocked with the AHB Bus Clock

Bits	Name	Description
7	ep8_intr_en	EP8 Interrupt Enable. 0: Do not raise EP8 Interrupt. 1: Raise EP8 Interrupt
6	ep7_intr_en	EP7 Interrupt Enable. 0: Do not raise EP7 Interrupt. 1: Raise EP7 Interrupt
5	ep6_intr_en	EP6 Interrupt Enable. 0: Do not raise EP6 Interrupt. 1: Raise EP6 Interrupt
4	ep5_intr_en	EP5 Interrupt Enable. 0: Do not raise EP5 Interrupt. 1: Raise EP5 Interrupt
3	ep4_intr_en	EP4 Interrupt Enable. 0: Do not raise EP4 Interrupt. 1: Raise EP4 Interrupt
2	ep3_intr_en	EP3 Interrupt Enable. 0: Do not raise EP3 Interrupt. 1: Raise EP3 Interrupt
1	ep2_intr_en	EP2 Interrupt Enable. 0: Do not raise EP2 Interrupt. 1: Raise EP2 Interrupt
0	ep1_intr_en	EP1 Interrupt Enable. 0: Do not raise EP1 Interrupt. 1: Raise EP1 Interrupt

1.3.526 USB_SIE_EP_INT_SR

SIE Data Endpoint Interrupt Status

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP_INT_SR: 0x600B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0
HW Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Retention	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET
Name	ep8_intr	ep7_intr	ep6_intr	ep5_intr	ep4_intr	ep3_intr	ep2_intr	ep1_intr

SIE Data Endpoint Status Register. This is an Interrupt Status Register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7	ep8_intr	EP8 Interrupt Status. 0: EP8 Interrupt not raised. 1: EP8 Interrupt Present
6	ep7_intr	EP7 Interrupt Status. 0: EP7 Interrupt not raised. 1: EP7 Interrupt Present
5	ep6_intr	EP6 Interrupt Status. 0: EP6 Interrupt not raised. 1: EP6 Interrupt Present
4	ep5_intr	EP5 Interrupt Status. 0: EP5 Interrupt not raised. 1: EP5 Interrupt Present
3	ep4_intr	EP4 Interrupt Status. 0: EP4 Interrupt not raised. 1: EP4 Interrupt Present
2	ep3_intr	EP3 Interrupt Status. 0: EP3 Interrupt not raised. 1: EP3 Interrupt Present
1	ep2_intr	EP2 Interrupt Status. 0: EP2 Interrupt not raised. 1: EP2 Interrupt Present
0	ep1_intr	EP1 Interrupt Status. 0: EP1 Interrupt not raised. 1: EP1 Interrupt Present

1.3.527 USB_SIE_EP1_CNT0

Non-control endpoint count register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP1_CNT0: 0x600C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/WZC:0	NA:000			R/W:000		
HW Access	R/W	W	NA			R/W		
Retention	NONRET	NONRET	NA			NONRET		
Name	data_toggle	data_valid	RSVD			data_count_msb		

The Endpoint Count Register 0 (CNT0) is used for configuring endpoints one through eight. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	data_toggle	This bit selects the DATA packet's toggle state. For IN transactions firmware must set this bit to the expected state. For OUT transactions the hardware sets this bit to the state of the received Data Toggle bit. 0- DATA0. 1- DATA1
6	data_valid	This bit is used for OUT transactions only and is read only. It is cleared to '0' if CRC bit stuffing errors or PID errors occur. This bit does not update for some endpoint mode settings. 0- Error in data received. 1- No Errors Sticky (individual bits)
2:0	data_count_msb[2:0]	These bits are the 3 MSb bits of a 11-bit counter. The LSb are the Data Count[7:0] bits of the CNT1 register. Refer to the CNT1 register for more information.

1.3.528 USB_SIE_EP1_CNT1

Non-control endpoint count register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP1_CNT1: 0x600D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	data_count							

The Endpoint Count Register 1 (CNT1) sets or reports the number of bytes in a USB data transfer to the non-control endpoints. For IN transactions firmware loads the count with the number of data bytes to transmit to the host. Valid values for MODE 1 and MODE 2 are 0 to 514 and for MODE 3 it is 0 to 1025. The 11-bit count also sets the limit for the number of bytes that are received for an OUT transaction. Before an OUT transaction is received for an endpoint set this count value to the maximum number of allowable data bytes. If this count value is set to a value greater then the number of bytes (Data + CRC) received both the data from the USB packet and the 2-byte CRC are written to the USB's dedicated SRAM. If the number of Data Bytes received is exactly same as the 11-bit count then only the Data is updated into the USB SRAM and the CRC is discarded but the OUT transaction is completed according to the Modebits of the EP Control Register. If the number of Data Bytes received is more than the 11-bit count then the OUT transaction is ignored. Once the OUT transaction is complete the full 11-bit count is updated by the SIE to the actual number of data bytes received by the SIE plus two for the packet's CRC. Valid values for MODE 1 and MODE 2 are 2 to 514 and for MODE 3 it is 2 to 1025. To get the actual number of bytes received firmware needs to decrement the 11-bit count by two. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7:0	data_count[7:0]	These bits are the 8 LSb of a 11-bit counter.The 3 MSb bits are the Count MSbbit of the CNT0 register. The 11-bit count indicates the number of data bytes in a transaction.

1.3.529 USB_SIE_EP1_CR0

Non-control endpoint's control Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP1_CR0: 0x600E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/WC:0	R/W:0	R/WC:0	R/W:0000			
HW Access	R	W	R	W	R/W			
Retention	NONRET	NONRET	NONRET	NONRET	NONRET			
Name	stall	err_in_txn	nak_int_en	acked_txn	mode			

The Endpoint Control Register 0 (CR0) is used for status and configuration of the non-control endpoints . This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	stall	When this bit is set the SIE stalls an OUT packet if the Mode bits are set to ACK-OUT. The SIE stalls an IN packet if the mode bits are set to ACK-IN. This bit must be clear for all other modes. 0- Do not issue a stall. 1- Stall an OUT packet if mode bits are set to ACK-OUT or Stall an IN packet if mode bits are set to ACK-IN.
6	err_in_txn	The Error in transaction bit is set whenever an error is detected. For an IN transaction, this indicates a no response from HOST scenario. For an OUT transaction, this represents an RxErr (PID error/ CRC error/ bit-stuff error scenario). This bit is cleared by any writes to the register. 0- No errored transactions since bit was last cleared. 1- Indicates a transaction ended with an error. Sticky (individual bits)
5	nak_int_en	When set this bit causes an endpoint interrupt to be generated even when a transfer completes with a NAK. 0- Do not issue an interrupt after completing the transaction by sending NAK. 1-Interrupt after transaction is complete by sending NAK.
4	acked_txn	The ACK'd transaction bit is set whenever the SIE engages in a transaction to the register's endpoint that completes with an ACK packet. This bit is cleared by any writes to the register. 0- No ACK'd transactions since bit was last cleared. 1- Indicates a transaction ended with an ACK. Sticky (individual bits)
3:0	mode[3:0]	The mode controls how the USB SIE responds to traffic and how the USB SIE changes the mode of that endpoint as a result of host packets to the endpoint.

1.3.530 USB_USBIO_CR0

USBIO Control 0 Register

Reset: Reset Signals Listed Below

Register : Address

USB_USBIO_CR0: 0x6010

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	NA:0000				R:U
HW Access	R	R	R	NA				W
Retention	RET	RET	RET	NA				NONRET
Name	ten	tse0	td	RSVD				rd

The USB IO Control Register 0 (USBIO_CR0) is used for manually transmitting on the USB D+ and D- pins or reading the differential receiver. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	ten	USB Transmit Enable. This is used to manually transmit on the D+ and D- pins. Normally this bit should be cleared to allow the internal SIE to drive the pins. The most common reason for manually transmitting is to force a resume state on the bus. 0- Manual Transmission Off (TSE0 and TD have no effect). 1- Manual Transmission Enabled (TSE0 and TD determine the state of the D+ and Dpins).
6	tse0	Transmit Single-Ended Zero. SE0: both D+ and D- low. No effect if TEN=0. 0- Do not force SE0. 1- Force SE0 on D+ and D-.
5	td	Transmit Data. Transmit a USB J or K state on the USB bus. No effect if TEN=0 or TSE0=1. 0- Force USB K state (D+ is low D- is high). 1- Force USB J state (D+ is high D- is low)
0	rd	Received Data. This read only bit gives the state of the USB differential receiver. 0- D+ < D- or D+ = D- = 0.

Reset Table

Reset Signal	Applicable Register Bit(s)
N/A	rd
System reset for retention flops [reset_all_retention]	td, tse0, ten

1.3.531 USB_USBIO_CR1

USBIO control 1 Register

Reset: Reset Signals Listed Below

Register : Address

USB_USBIO_CR1: 0x6012

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:1	NA:00		R/W:0	R:U	R:U
HW Access	NA		R	NA		R	W	W
Retention	NA		RET	NA		RET	NONRET	NONRET
Name	RSVD		iomode	RSVD		usbpuen	dpo	dmo

The USB IO Control Register 1 (USBIO_CR1) is used to manually read or write the D+ and D- pins and to configure internal pull-up resistors on those pins. This register is clocked with AHB (BUS) Clock

Bits	Name	Description
5	iomode	This bit allows the D+ and D- pins to be configured for either USB mode or bit banged modes. If this bit is set the DMI and DPI bits are used to drive the D- and D+ pins. 0- USB Mode. Drive Mode has no effect. 1- Drive Mode DMI and DPI determine state of the D+ and D- pins.
2	usbpuen	This bit controls the connection of the internal 1.5 k pull up resistor on the D+ pin. 0- No effect. 1- Apply internal USB pull-up resistor to D+ pad.
1	dpo	This read only bit gives the state of the D+ pin.
0	dmo	This read only bit gives the state of the D- pin.

Reset Table

Reset Signal	Applicable Register Bit(s)
N/A	dmo, dpo
System reset for retention flops [reset_all_retention]	usbpuen, iomode

1.3.532 USB_DYN_RECONFIG

USB Dynamic reconfiguration register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_DYN_RECONFIG: 0x6014

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R:0	R/W:000			R/W:0
HW Access	NA			W	R			R
Retention	NA			NONRET	NONRET			NONRET
Name	RSVD			dyn_reconfig_rdy_sts	dyn_reconfig_epno			dyn_config_en

This regsiter is used for dynamically configuring the data EPs. This register is clocked with AHB Clock

Bits	Name	Description
4	dyn_reconfig_rdy_sts	This bit indicates the ready status for the dynamic reconfiguration, when set to 1 , indicates the block is ready for reconfiguration .
3:1	dyn_reconfig_epno[2:0]	These bits indicates the EP number for which reconfiguration is required when dyn_config_en bit is set to 1.
0	dyn_config_en	This bit is used to enable the dynamic re-configuration for the selected EP. If set to 1 , indicates the reconfiguration required for selected EP.

1.3.533 USB_SOF0

Start Of Frame Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SOF0: 0x6018

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	NONRET							
Name	frame_number							

The USB Start of Frame Registers (SOF0 and SOF1) provide access to the 11-bit SOF frame number. Start of frame packets are sent from the host every one ms. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7:0	frame_number[7:0]	It has the lower 8 bits [7:0] of the SOF frame number.

1.3.534 USB_SOF1

Start Of Frame Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SOF1: 0x6019

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R:000		
HW Access	NA					R/W		
Retention	NA					NONRET		
Name	RSVD					frame_number		

The USB Start of Frame Registers (SOF0 and SOF1) provide access to the 11-bit SOF frame number. Start of frame packets are sent from the host every one ms. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
2:0	frame_number[2:0]	It has the upper 3 bits [10:8] of the SOF frame number.

1.3.535 USB_SIE_EP2_CNT0

Non-control endpoint count register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP2_CNT0: 0x601C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/WZC:0	NA:000			R/W:000		
HW Access	R/W	W	NA			R/W		
Retention	NONRET	NONRET	NA			NONRET		
Name	data_toggle	data_valid	RSVD			data_count_msb		

The Endpoint Count Register 0 (CNT0) is used for configuring endpoints one through eight. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	data_toggle	This bit selects the DATA packet's toggle state. For IN transactions firmware must set this bit to the expected state. For OUT transactions the hardware sets this bit to the state of the received Data Toggle bit. 0- DATA0. 1- DATA1
6	data_valid	This bit is used for OUT transactions only and is read only. It is cleared to '0' if CRC bit stuffing errors or PID errors occur. This bit does not update for some endpoint mode settings. 0- Error in data received. 1- No Errors Sticky (individual bits)
2:0	data_count_msb[2:0]	These bits are the 3 MSb bits of a 11-bit counter. The LSb are the Data Count[7:0] bits of the CNT1 register. Refer to the CNT1 register for more information.

1.3.536 USB_SIE_EP2_CNT1

Non-control endpoint count register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP2_CNT1: 0x601D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	data_count							

The Endpoint Count Register 1 (CNT1) sets or reports the number of bytes in a USB data transfer to the non-control endpoints. For IN transactions firmware loads the count with the number of data bytes to transmit to the host. Valid values for MODE 1 and MODE 2 are 0 to 514 and for MODE 3 it is 0 to 1025. The 11-bit count also sets the limit for the number of bytes that are received for an OUT transaction. Before an OUT transaction is received for an endpoint set this count value to the maximum number of allowable data bytes. If this count value is set to a value greater then the number of bytes (Data + CRC) received both the data from the USB packet and the 2-byte CRC are written to the USB's dedicated SRAM. If the number of Data Bytes received is exactly same as the 11-bit count then only the Data is updated into the USB SRAM and the CRC is discarded but the OUT transaction is completed according to the Modebits of the EP Control Register. If the number of Data Bytes received is more than the 11-bit count then the OUT transaction is ignored. Once the OUT transaction is complete the full 11-bit count is updated by the SIE to the actual number of data bytes received by the SIE plus two for the packet's CRC. Valid values for MODE 1 and MODE 2 are 2 to 514 and for MODE 3 it is 2 to 1025. To get the actual number of bytes received firmware needs to decrement the 11-bit count by two. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7:0	data_count[7:0]	These bits are the 8 LSb of a 11-bit counter.The 3 MSb bits are the Count MSbbit of the CNT0 register. The 11-bit count indicates the number of data bytes in a transaction.

1.3.537 USB_SIE_EP2_CR0

Non-control endpoint's control Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP2_CR0: 0x601E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/WC:0	R/W:0	R/WC:0	R/W:0000			
HW Access	R	W	R	W	R/W			
Retention	NONRET	NONRET	NONRET	NONRET	NONRET			
Name	stall	err_in_txn	nak_int_en	acked_txn	mode			

The Endpoint Control Register 0 (CR0) is used for status and configuration of the non-control endpoints . This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	stall	When this bit is set the SIE stalls an OUT packet if the Mode bits are set to ACK-OUT. The SIE stalls an IN packet if the mode bits are set to ACK-IN. This bit must be clear for all other modes. 0- Do not issue a stall. 1- Stall an OUT packet if mode bits are set to ACK-OUT or Stall an IN packet if mode bits are set to ACK-IN.
6	err_in_txn	The Error in transaction bit is set whenever an error is detected. For an IN transaction, this indicates a no response from HOST scenario. For an OUT transaction, this represents an RxErr (PID error/ CRC error/ bit-stuff error scenario). This bit is cleared by any writes to the register. 0- No errored transactions since bit was last cleared. 1- Indicates a transaction ended with an error. Sticky (individual bits)
5	nak_int_en	When set this bit causes an endpoint interrupt to be generated even when a transfer completes with a NAK. 0- Do not issue an interrupt after completing the transaction by sending NAK. 1-Interrupt after transaction is complete by sending NAK.
4	acked_txn	The ACK'd transaction bit is set whenever the SIE engages in a transaction to the register's endpoint that completes with an ACK packet. This bit is cleared by any writes to the register. 0- No ACK'd transactions since bit was last cleared. 1- Indicates a transaction ended with an ACK. Sticky (individual bits)
3:0	mode[3:0]	The mode controls how the USB SIE responds to traffic and how the USB SIE changes the mode of that endpoint as a result of host packets to the endpoint.

1.3.538 USB_EP0_CR

Endpoint0 control Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_EP0_CR: 0x6028

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/WC:0	R/WC:0	R/WC:0	R/WC:0	R/W:0000			
HW Access	W	W	W	W	R/W			
Retention	NONRET	NONRET	NONRET	NONRET	NONRET			
Name	setup_rcvd	in_rcvd	out_rcvd	acked_txn	mode			

The Endpoint Control Register (EP0_CR) is used to configure endpoint 0. Because both firmware and the SIE are allowed to write to the Endpoint 0 Control and Count registers the SIE provides an interlocking mechanism to prevent accidental overwriting of data. When the SIE writes to these registers they are locked and the processor cannot write to them until after reading the EP0_CR register. Writing to this register clears the upper four bits regardless of the value written. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	setup_rcvd	When set this bit indicates a valid SETUP packet was received and ACKed. This bit is forced HIGH from the start of the data packet phase of the SETUP transaction until the start of the ACK packet returned by the SIE. The CPU is prevented from clearing this bit during this interval. After this interval the bit will remain set until cleared by firmware. While this bit is set to '1' the CPU cannot write to the EP0_DRx registers. This prevents firmware from overwriting an incoming SETUP transaction before firmware has a chance to read the SETUP data. This bit is cleared by any non-locked writes to the register. Sticky (individual bits)
6	in_rcvd	When set this bit indicates a valid IN packet has been received. This bit is updated to '1' after the host acknowledges an IN data packet. When clear this bit indicates either no IN has been received or that the host did not acknowledge the IN data by sending ACK handshake. It is cleared by any non-locked writes to the register. Sticky (individual bits)
5	out_rcvd	When set this bit indicates a valid OUT packet has been received and ACKed. This bit is updated to '1' after the last received packet in an OUT transaction. When clear this bit indicates no OUT received. It is cleared by any non-locked writes to the register. Sticky (individual bits)
4	acked_txn	This bit is set whenever the SIE engages in a transaction to the register's endpoint that completes with a ACK packet. This bit is cleared by any nonlocked writes to the register. Sticky (individual bits)
3:0	mode[3:0]	The mode bits control how the USB SIE responds to traffic and how the USB SIE will change the mode of that endpoint as a result of host packets to the endpoint.

1.3.539 USB_EP0_CNT

Endpoint0 count Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_EP0_CNT: 0x6029

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/WZC:0	NA:00		R/W:0000			
HW Access	R/W	W	NA		R/W			
Retention	NONRET	NONRET	NA		NONRET			
Name	data_toggle	data_valid	RSVD		byte_count			

The Endpoint 0 Count Register (EP0_CNT) is used to configure endpoint 0. Whenever the count updates from a SETUP or OUT transaction this register locks and can not be written by the CPU. Reading the EP0_CR register unlocks this register. This prevents firmware from overwriting a status update on incoming SETUP or OUT transactions before firmware has a chance to read the data. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	data_toggle	This bit selects the DATA packet's toggle state. For IN transactions firmware must set this bit. For OUT or SETUP transactions the SIE hardware sets this bit to the state of the received Data Toggle bit. 0- DATA0. 1- DATA1
6	data_valid	This bit indicates whether there were errors in OUT or SETUP transactions. It is cleared to '0' if CRC bit stuff or PID errors have occurred. This bit does not update for some endpoint mode settings. This bit may be cleared by writing a zero to it when the register is not locked. 0- Error in data received. 1- No Errors Sticky (individual bits)
3:0	byte_count[3:0]	These bits indicate the number of data bytes in a transaction. For IN transactions firmware loads the count with the number of bytes to be transmitted to the host from the endpoint FIFO. Valid values are 0 to 8. For OUT or SETUP transactions the count is updated by hardware to the number of data bytes received plus two for the CRC bytes. Valid values are 2 to 10.

1.3.540 USB_SIE_EP3_CNT0

Non-control endpoint count register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP3_CNT0: 0x602C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/WZC:0	NA:000			R/W:000		
HW Access	R/W	W	NA			R/W		
Retention	NONRET	NONRET	NA			NONRET		
Name	data_toggle	data_valid	RSVD			data_count_msb		

The Endpoint Count Register 0 (CNT0) is used for configuring endpoints one through eight. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	data_toggle	This bit selects the DATA packet's toggle state. For IN transactions firmware must set this bit to the expected state. For OUT transactions the hardware sets this bit to the state of the received Data Toggle bit. 0- DATA0. 1- DATA1
6	data_valid	This bit is used for OUT transactions only and is read only. It is cleared to '0' if CRC bit stuffing errors or PID errors occur. This bit does not update for some endpoint mode settings. 0- Error in data received. 1- No Errors Sticky (individual bits)
2:0	data_count_msb[2:0]	These bits are the 3 MSb bits of a 11-bit counter. The LSb are the Data Count[7:0] bits of the CNT1 register. Refer to the CNT1 register for more information.

1.3.541 USB_SIE_EP3_CNT1

Non-control endpoint count register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP3_CNT1: 0x602D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	data_count							

The Endpoint Count Register 1 (CNT1) sets or reports the number of bytes in a USB data transfer to the non-control endpoints. For IN transactions firmware loads the count with the number of data bytes to transmit to the host. Valid values for MODE 1 and MODE 2 are 0 to 514 and for MODE 3 it is 0 to 1025. The 11-bit count also sets the limit for the number of bytes that are received for an OUT transaction. Before an OUT transaction is received for an endpoint set this count value to the maximum number of allowable data bytes. If this count value is set to a value greater then the number of bytes (Data + CRC) received both the data from the USB packet and the 2-byte CRC are written to the USB's dedicated SRAM. If the number of Data Bytes received is exactly same as the 11-bit count then only the Data is updated into the USB SRAM and the CRC is discarded but the OUT transaction is completed according to the Modebits of the EP Control Register. If the number of Data Bytes received is more than the 11-bit count then the OUT transaction is ignored. Once the OUT transaction is complete the full 11-bit count is updated by the SIE to the actual number of data bytes received by the SIE plus two for the packet's CRC. Valid values for MODE 1 and MODE 2 are 2 to 514 and for MODE 3 it is 2 to 1025. To get the actual number of bytes received firmware needs to decrement the 11-bit count by two. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7:0	data_count[7:0]	These bits are the 8 LSb of a 11-bit counter.The 3 MSb bits are the Count MSbbit of the CNT0 register. The 11-bit count indicates the number of data bytes in a transaction.

1.3.542 USB_SIE_EP3_CR0

Non-control endpoint's control Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP3_CR0: 0x602E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/WC:0	R/W:0	R/WC:0	R/W:0000			
HW Access	R	W	R	W	R/W			
Retention	NONRET	NONRET	NONRET	NONRET	NONRET			
Name	stall	err_in_txn	nak_int_en	acked_txn	mode			

The Endpoint Control Register 0 (CR0) is used for status and configuration of the non-control endpoints . This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	stall	When this bit is set the SIE stalls an OUT packet if the Mode bits are set to ACK-OUT. The SIE stalls an IN packet if the mode bits are set to ACK-IN. This bit must be clear for all other modes. 0- Do not issue a stall. 1- Stall an OUT packet if mode bits are set to ACK-OUT or Stall an IN packet if mode bits are set to ACK-IN.
6	err_in_txn	The Error in transaction bit is set whenever an error is detected. For an IN transaction, this indicates a no response from HOST scenario. For an OUT transaction, this represents an RxErr (PID error/ CRC error/ bit-stuff error scenario). This bit is cleared by any writes to the register. 0- No errored transactions since bit was last cleared. 1- Indicates a transaction ended with an error. Sticky (individual bits)
5	nak_int_en	When set this bit causes an endpoint interrupt to be generated even when a transfer completes with a NAK. 0- Do not issue an interrupt after completing the transaction by sending NAK. 1-Interrupt after transaction is complete by sending NAK.
4	acked_txn	The ACK'd transaction bit is set whenever the SIE engages in a transaction to the register's endpoint that completes with an ACK packet. This bit is cleared by any writes to the register. 0- No ACK'd transactions since bit was last cleared. 1- Indicates a transaction ended with an ACK. Sticky (individual bits)
3:0	mode[3:0]	The mode controls how the USB SIE responds to traffic and how the USB SIE changes the mode of that endpoint as a result of host packets to the endpoint.

1.3.543 USB_SIE_EP4_CNT0

Non-control endpoint count register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP4_CNT0: 0x603C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/WZC:0	NA:000			R/W:000		
HW Access	R/W	W	NA			R/W		
Retention	NONRET	NONRET	NA			NONRET		
Name	data_toggle	data_valid	RSVD			data_count_msb		

The Endpoint Count Register 0 (CNT0) is used for configuring endpoints one through eight. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	data_toggle	This bit selects the DATA packet's toggle state. For IN transactions firmware must set this bit to the expected state. For OUT transactions the hardware sets this bit to the state of the received Data Toggle bit. 0- DATA0. 1- DATA1
6	data_valid	This bit is used for OUT transactions only and is read only. It is cleared to '0' if CRC bit stuffing errors or PID errors occur. This bit does not update for some endpoint mode settings. 0- Error in data received. 1- No Errors Sticky (individual bits)
2:0	data_count_msb[2:0]	These bits are the 3 MSb bits of a 11-bit counter. The LSb are the Data Count[7:0] bits of the CNT1 register. Refer to the CNT1 register for more information.

1.3.544 USB_SIE_EP4_CNT1

Non-control endpoint count register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP4_CNT1: 0x603D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	data_count							

The Endpoint Count Register 1 (CNT1) sets or reports the number of bytes in a USB data transfer to the non-control endpoints. For IN transactions firmware loads the count with the number of data bytes to transmit to the host. Valid values for MODE 1 and MODE 2 are 0 to 514 and for MODE 3 it is 0 to 1025. The 11-bit count also sets the limit for the number of bytes that are received for an OUT transaction. Before an OUT transaction is received for an endpoint set this count value to the maximum number of allowable data bytes. If this count value is set to a value greater then the number of bytes (Data + CRC) received both the data from the USB packet and the 2-byte CRC are written to the USB's dedicated SRAM. If the number of Data Bytes received is exactly same as the 11-bit count then only the Data is updated into the USB SRAM and the CRC is discarded but the OUT transaction is completed according to the Modebits of the EP Control Register. If the number of Data Bytes received is more than the 11-bit count then the OUT transaction is ignored. Once the OUT transaction is complete the full 11-bit count is updated by the SIE to the actual number of data bytes received by the SIE plus two for the packet's CRC. Valid values for MODE 1 and MODE 2 are 2 to 514 and for MODE 3 it is 2 to 1025. To get the actual number of bytes received firmware needs to decrement the 11-bit count by two. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7:0	data_count[7:0]	These bits are the 8 LSb of a 11-bit counter.The 3 MSb bits are the Count MSbbit of the CNT0 register. The 11-bit count indicates the number of data bytes in a transaction.

1.3.545 USB_SIE_EP4_CR0

Non-control endpoint's control Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP4_CR0: 0x603E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/WC:0	R/W:0	R/WC:0	R/W:0000			
HW Access	R	W	R	W	R/W			
Retention	NONRET	NONRET	NONRET	NONRET	NONRET			
Name	stall	err_in_txn	nak_int_en	acked_txn	mode			

The Endpoint Control Register 0 (CR0) is used for status and configuration of the non-control endpoints . This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	stall	When this bit is set the SIE stalls an OUT packet if the Mode bits are set to ACK-OUT. The SIE stalls an IN packet if the mode bits are set to ACK-IN. This bit must be clear for all other modes. 0- Do not issue a stall. 1- Stall an OUT packet if mode bits are set to ACK-OUT or Stall an IN packet if mode bits are set to ACK-IN.
6	err_in_txn	The Error in transaction bit is set whenever an error is detected. For an IN transaction, this indicates a no response from HOST scenario. For an OUT transaction, this represents an RxErr (PID error/ CRC error/ bit-stuff error scenario). This bit is cleared by any writes to the register. 0- No errored transactions since bit was last cleared. 1- Indicates a transaction ended with an error. Sticky (individual bits)
5	nak_int_en	When set this bit causes an endpoint interrupt to be generated even when a transfer completes with a NAK. 0- Do not issue an interrupt after completing the transaction by sending NAK. 1-Interrupt after transaction is complete by sending NAK.
4	acked_txn	The ACK'd transaction bit is set whenever the SIE engages in a transaction to the register's endpoint that completes with an ACK packet. This bit is cleared by any writes to the register. 0- No ACK'd transactions since bit was last cleared. 1- Indicates a transaction ended with an ACK. Sticky (individual bits)
3:0	mode[3:0]	The mode controls how the USB SIE responds to traffic and how the USB SIE changes the mode of that endpoint as a result of host packets to the endpoint.

1.3.546 USB_SIE_EP5_CNT0

Non-control endpoint count register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP5_CNT0: 0x604C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/WZC:0	NA:000			R/W:000		
HW Access	R/W	W	NA			R/W		
Retention	NONRET	NONRET	NA			NONRET		
Name	data_toggle	data_valid	RSVD			data_count_msb		

The Endpoint Count Register 0 (CNT0) is used for configuring endpoints one through eight. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	data_toggle	This bit selects the DATA packet's toggle state. For IN transactions firmware must set this bit to the expected state. For OUT transactions the hardware sets this bit to the state of the received Data Toggle bit. 0- DATA0. 1- DATA1
6	data_valid	This bit is used for OUT transactions only and is read only. It is cleared to '0' if CRC bit stuffing errors or PID errors occur. This bit does not update for some endpoint mode settings. 0- Error in data received. 1- No Errors Sticky (individual bits)
2:0	data_count_msb[2:0]	These bits are the 3 MSb bits of a 11-bit counter. The LSb are the Data Count[7:0] bits of the CNT1 register. Refer to the CNT1 register for more information.

1.3.547 USB_SIE_EP5_CNT1

Non-control endpoint count register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP5_CNT1: 0x604D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	data_count							

The Endpoint Count Register 1 (CNT1) sets or reports the number of bytes in a USB data transfer to the non-control endpoints. For IN transactions firmware loads the count with the number of data bytes to transmit to the host. Valid values for MODE 1 and MODE 2 are 0 to 514 and for MODE 3 it is 0 to 1025. The 11-bit count also sets the limit for the number of bytes that are received for an OUT transaction. Before an OUT transaction is received for an endpoint set this count value to the maximum number of allowable data bytes. If this count value is set to a value greater then the number of bytes (Data + CRC) received both the data from the USB packet and the 2-byte CRC are written to the USB's dedicated SRAM. If the number of Data Bytes received is exactly same as the 11-bit count then only the Data is updated into the USB SRAM and the CRC is discarded but the OUT transaction is completed according to the Modebits of the EP Control Register. If the number of Data Bytes received is more than the 11-bit count then the OUT transaction is ignored. Once the OUT transaction is complete the full 11-bit count is updated by the SIE to the actual number of data bytes received by the SIE plus two for the packet's CRC. Valid values for MODE 1 and MODE 2 are 2 to 514 and for MODE 3 it is 2 to 1025. To get the actual number of bytes received firmware needs to decrement the 11-bit count by two. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7:0	data_count[7:0]	These bits are the 8 LSb of a 11-bit counter.The 3 MSb bits are the Count MSbbit of the CNT0 register. The 11-bit count indicates the number of data bytes in a transaction.

1.3.548 USB_SIE_EP5_CR0

Non-control endpoint's control Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP5_CR0: 0x604E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/WC:0	R/W:0	R/WC:0	R/W:0000			
HW Access	R	W	R	W	R/W			
Retention	NONRET	NONRET	NONRET	NONRET	NONRET			
Name	stall	err_in_txn	nak_int_en	acked_txn	mode			

The Endpoint Control Register 0 (CR0) is used for status and configuration of the non-control endpoints . This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	stall	When this bit is set the SIE stalls an OUT packet if the Mode bits are set to ACK-OUT. The SIE stalls an IN packet if the mode bits are set to ACK-IN. This bit must be clear for all other modes. 0- Do not issue a stall. 1- Stall an OUT packet if mode bits are set to ACK-OUT or Stall an IN packet if mode bits are set to ACK-IN.
6	err_in_txn	The Error in transaction bit is set whenever an error is detected. For an IN transaction, this indicates a no response from HOST scenario. For an OUT transaction, this represents an RxErr (PID error/ CRC error/ bit-stuff error scenario). This bit is cleared by any writes to the register. 0- No errored transactions since bit was last cleared. 1- Indicates a transaction ended with an error. Sticky (individual bits)
5	nak_int_en	When set this bit causes an endpoint interrupt to be generated even when a transfer completes with a NAK. 0- Do not issue an interrupt after completing the transaction by sending NAK. 1-Interrupt after transaction is complete by sending NAK.
4	acked_txn	The ACK'd transaction bit is set whenever the SIE engages in a transaction to the register's endpoint that completes with an ACK packet. This bit is cleared by any writes to the register. 0- No ACK'd transactions since bit was last cleared. 1- Indicates a transaction ended with an ACK. Sticky (individual bits)
3:0	mode[3:0]	The mode controls how the USB SIE responds to traffic and how the USB SIE changes the mode of that endpoint as a result of host packets to the endpoint.

1.3.549 USB_SIE_EP6_CNT0

Non-control endpoint count register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP6_CNT0: 0x605C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/WZC:0	NA:000			R/W:000		
HW Access	R/W	W	NA			R/W		
Retention	NONRET	NONRET	NA			NONRET		
Name	data_toggle	data_valid	RSVD			data_count_msb		

The Endpoint Count Register 0 (CNT0) is used for configuring endpoints one through eight. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	data_toggle	This bit selects the DATA packet's toggle state. For IN transactions firmware must set this bit to the expected state. For OUT transactions the hardware sets this bit to the state of the received Data Toggle bit. 0- DATA0. 1- DATA1
6	data_valid	This bit is used for OUT transactions only and is read only. It is cleared to '0' if CRC bit stuffing errors or PID errors occur. This bit does not update for some endpoint mode settings. 0- Error in data received. 1- No Errors Sticky (individual bits)
2:0	data_count_msb[2:0]	These bits are the 3 MSb bits of a 11-bit counter. The LSb are the Data Count[7:0] bits of the CNT1 register. Refer to the CNT1 register for more information.

1.3.550 USB_SIE_EP6_CNT1

Non-control endpoint count register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP6_CNT1: 0x605D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	data_count							

The Endpoint Count Register 1 (CNT1) sets or reports the number of bytes in a USB data transfer to the non-control endpoints. For IN transactions firmware loads the count with the number of data bytes to transmit to the host. Valid values for MODE 1 and MODE 2 are 0 to 514 and for MODE 3 it is 0 to 1025. The 11-bit count also sets the limit for the number of bytes that are received for an OUT transaction. Before an OUT transaction is received for an endpoint set this count value to the maximum number of allowable data bytes. If this count value is set to a value greater then the number of bytes (Data + CRC) received both the data from the USB packet and the 2-byte CRC are written to the USB's dedicated SRAM. If the number of Data Bytes received is exactly same as the 11-bit count then only the Data is updated into the USB SRAM and the CRC is discarded but the OUT transaction is completed according to the Modebits of the EP Control Register. If the number of Data Bytes received is more than the 11-bit count then the OUT transaction is ignored. Once the OUT transaction is complete the full 11-bit count is updated by the SIE to the actual number of data bytes received by the SIE plus two for the packet's CRC. Valid values for MODE 1 and MODE 2 are 2 to 514 and for MODE 3 it is 2 to 1025. To get the actual number of bytes received firmware needs to decrement the 11-bit count by two. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7:0	data_count[7:0]	These bits are the 8 LSb of a 11-bit counter.The 3 MSb bits are the Count MSbbit of the CNT0 register. The 11-bit count indicates the number of data bytes in a transaction.

1.3.551 USB_SIE_EP6_CR0

Non-control endpoint's control Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP6_CR0: 0x605E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/WC:0	R/W:0	R/WC:0	R/W:0000			
HW Access	R	W	R	W	R/W			
Retention	NONRET	NONRET	NONRET	NONRET	NONRET			
Name	stall	err_in_txn	nak_int_en	acked_txn	mode			

The Endpoint Control Register 0 (CR0) is used for status and configuration of the non-control endpoints . This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	stall	When this bit is set the SIE stalls an OUT packet if the Mode bits are set to ACK-OUT. The SIE stalls an IN packet if the mode bits are set to ACK-IN. This bit must be clear for all other modes. 0- Do not issue a stall. 1- Stall an OUT packet if mode bits are set to ACK-OUT or Stall an IN packet if mode bits are set to ACK-IN.
6	err_in_txn	The Error in transaction bit is set whenever an error is detected. For an IN transaction, this indicates a no response from HOST scenario. For an OUT transaction, this represents an RxErr (PID error/ CRC error/ bit-stuff error scenario). This bit is cleared by any writes to the register. 0- No errored transactions since bit was last cleared. 1- Indicates a transaction ended with an error. Sticky (individual bits)
5	nak_int_en	When set this bit causes an endpoint interrupt to be generated even when a transfer completes with a NAK. 0- Do not issue an interrupt after completing the transaction by sending NAK. 1-Interrupt after transaction is complete by sending NAK.
4	acked_txn	The ACK'd transaction bit is set whenever the SIE engages in a transaction to the register's endpoint that completes with an ACK packet. This bit is cleared by any writes to the register. 0- No ACK'd transactions since bit was last cleared. 1- Indicates a transaction ended with an ACK. Sticky (individual bits)
3:0	mode[3:0]	The mode controls how the USB SIE responds to traffic and how the USB SIE changes the mode of that endpoint as a result of host packets to the endpoint.

1.3.552 USB_SIE_EP7_CNT0

Non-control endpoint count register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP7_CNT0: 0x606C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/WZC:0	NA:000			R/W:000		
HW Access	R/W	W	NA			R/W		
Retention	NONRET	NONRET	NA			NONRET		
Name	data_toggle	data_valid	RSVD			data_count_msb		

The Endpoint Count Register 0 (CNT0) is used for configuring endpoints one through eight. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	data_toggle	This bit selects the DATA packet's toggle state. For IN transactions firmware must set this bit to the expected state. For OUT transactions the hardware sets this bit to the state of the received Data Toggle bit. 0- DATA0. 1- DATA1
6	data_valid	This bit is used for OUT transactions only and is read only. It is cleared to '0' if CRC bit stuffing errors or PID errors occur. This bit does not update for some endpoint mode settings. 0- Error in data received. 1- No Errors Sticky (individual bits)
2:0	data_count_msb[2:0]	These bits are the 3 MSb bits of a 11-bit counter. The LSb are the Data Count[7:0] bits of the CNT1 register. Refer to the CNT1 register for more information.

1.3.553 USB_SIE_EP7_CNT1

Non-control endpoint count register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP7_CNT1: 0x606D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	data_count							

The Endpoint Count Register 1 (CNT1) sets or reports the number of bytes in a USB data transfer to the non-control endpoints. For IN transactions firmware loads the count with the number of data bytes to transmit to the host. Valid values for MODE 1 and MODE 2 are 0 to 514 and for MODE 3 it is 0 to 1025. The 11-bit count also sets the limit for the number of bytes that are received for an OUT transaction. Before an OUT transaction is received for an endpoint set this count value to the maximum number of allowable data bytes. If this count value is set to a value greater then the number of bytes (Data + CRC) received both the data from the USB packet and the 2-byte CRC are written to the USB's dedicated SRAM. If the number of Data Bytes received is exactly same as the 11-bit count then only the Data is updated into the USB SRAM and the CRC is discarded but the OUT transaction is completed according to the Modebits of the EP Control Register. If the number of Data Bytes received is more than the 11-bit count then the OUT transaction is ignored. Once the OUT transaction is complete the full 11-bit count is updated by the SIE to the actual number of data bytes received by the SIE plus two for the packet's CRC. Valid values for MODE 1 and MODE 2 are 2 to 514 and for MODE 3 it is 2 to 1025. To get the actual number of bytes received firmware needs to decrement the 11-bit count by two. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7:0	data_count[7:0]	These bits are the 8 LSb of a 11-bit counter.The 3 MSb bits are the Count MSbbit of the CNT0 register. The 11-bit count indicates the number of data bytes in a transaction.

1.3.554 USB_SIE_EP7_CR0

Non-control endpoint's control Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP7_CR0: 0x606E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/WC:0	R/W:0	R/WC:0	R/W:0000			
HW Access	R	W	R	W	R/W			
Retention	NONRET	NONRET	NONRET	NONRET	NONRET			
Name	stall	err_in_txn	nak_int_en	acked_txn	mode			

The Endpoint Control Register 0 (CR0) is used for status and configuration of the non-control endpoints . This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	stall	When this bit is set the SIE stalls an OUT packet if the Mode bits are set to ACK-OUT. The SIE stalls an IN packet if the mode bits are set to ACK-IN. This bit must be clear for all other modes. 0- Do not issue a stall. 1- Stall an OUT packet if mode bits are set to ACK-OUT or Stall an IN packet if mode bits are set to ACK-IN.
6	err_in_txn	The Error in transaction bit is set whenever an error is detected. For an IN transaction, this indicates a no response from HOST scenario. For an OUT transaction, this represents an RxErr (PID error/ CRC error/ bit-stuff error scenario). This bit is cleared by any writes to the register. 0- No errored transactions since bit was last cleared. 1- Indicates a transaction ended with an error. Sticky (individual bits)
5	nak_int_en	When set this bit causes an endpoint interrupt to be generated even when a transfer completes with a NAK. 0- Do not issue an interrupt after completing the transaction by sending NAK. 1-Interrupt after transaction is complete by sending NAK.
4	acked_txn	The ACK'd transaction bit is set whenever the SIE engages in a transaction to the register's endpoint that completes with an ACK packet. This bit is cleared by any writes to the register. 0- No ACK'd transactions since bit was last cleared. 1- Indicates a transaction ended with an ACK. Sticky (individual bits)
3:0	mode[3:0]	The mode controls how the USB SIE responds to traffic and how the USB SIE changes the mode of that endpoint as a result of host packets to the endpoint.

1.3.555 USB_SIE_EP8_CNT0

Non-control endpoint count register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP8_CNT0: 0x607C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/WZC:0	NA:000			R/W:000		
HW Access	R/W	W	NA			R/W		
Retention	NONRET	NONRET	NA			NONRET		
Name	data_toggle	data_valid	RSVD			data_count_msb		

The Endpoint Count Register 0 (CNT0) is used for configuring endpoints one through eight. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	data_toggle	This bit selects the DATA packet's toggle state. For IN transactions firmware must set this bit to the expected state. For OUT transactions the hardware sets this bit to the state of the received Data Toggle bit. 0- DATA0. 1- DATA1
6	data_valid	This bit is used for OUT transactions only and is read only. It is cleared to '0' if CRC bit stuffing errors or PID errors occur. This bit does not update for some endpoint mode settings. 0- Error in data received. 1- No Errors Sticky (individual bits)
2:0	data_count_msb[2:0]	These bits are the 3 MSb bits of a 11-bit counter. The LSb are the Data Count[7:0] bits of the CNT1 register. Refer to the CNT1 register for more information.

1.3.556 USB_SIE_EP8_CNT1

Non-control endpoint count register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP8_CNT1: 0x607D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	data_count							

The Endpoint Count Register 1 (CNT1) sets or reports the number of bytes in a USB data transfer to the non-control endpoints. For IN transactions firmware loads the count with the number of data bytes to transmit to the host. Valid values for MODE 1 and MODE 2 are 0 to 514 and for MODE 3 it is 0 to 1025. The 11-bit count also sets the limit for the number of bytes that are received for an OUT transaction. Before an OUT transaction is received for an endpoint set this count value to the maximum number of allowable data bytes. If this count value is set to a value greater then the number of bytes (Data + CRC) received both the data from the USB packet and the 2-byte CRC are written to the USB's dedicated SRAM. If the number of Data Bytes received is exactly same as the 11-bit count then only the Data is updated into the USB SRAM and the CRC is discarded but the OUT transaction is completed according to the Modebits of the EP Control Register. If the number of Data Bytes received is more than the 11-bit count then the OUT transaction is ignored. Once the OUT transaction is complete the full 11-bit count is updated by the SIE to the actual number of data bytes received by the SIE plus two for the packet's CRC. Valid values for MODE 1 and MODE 2 are 2 to 514 and for MODE 3 it is 2 to 1025. To get the actual number of bytes received firmware needs to decrement the 11-bit count by two. This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7:0	data_count[7:0]	These bits are the 8 LSb of a 11-bit counter.The 3 MSb bits are the Count MSbbit of the CNT0 register. The 11-bit count indicates the number of data bytes in a transaction.

1.3.557 USB_SIE_EP8_CR0

Non-control endpoint's control Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_SIE_EP8_CR0: 0x607E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/WC:0	R/W:0	R/WC:0	R/W:0000			
HW Access	R	W	R	W	R/W			
Retention	NONRET	NONRET	NONRET	NONRET	NONRET			
Name	stall	err_in_txn	nak_int_en	acked_txn	mode			

The Endpoint Control Register 0 (CR0) is used for status and configuration of the non-control endpoints . This register is clocked with 48 MHz USB Clock

Bits	Name	Description
7	stall	When this bit is set the SIE stalls an OUT packet if the Mode bits are set to ACK-OUT. The SIE stalls an IN packet if the mode bits are set to ACK-IN. This bit must be clear for all other modes. 0- Do not issue a stall. 1- Stall an OUT packet if mode bits are set to ACK-OUT or Stall an IN packet if mode bits are set to ACK-IN.
6	err_in_txn	The Error in transaction bit is set whenever an error is detected. For an IN transaction, this indicates a no response from HOST scenario. For an OUT transaction, this represents an RxErr (PID error/ CRC error/ bit-stuff error scenario). This bit is cleared by any writes to the register. 0- No errored transactions since bit was last cleared. 1- Indicates a transaction ended with an error. Sticky (individual bits)
5	nak_int_en	When set this bit causes an endpoint interrupt to be generated even when a transfer completes with a NAK. 0- Do not issue an interrupt after completing the transaction by sending NAK. 1-Interrupt after transaction is complete by sending NAK.
4	acked_txn	The ACK'd transaction bit is set whenever the SIE engages in a transaction to the register's endpoint that completes with an ACK packet. This bit is cleared by any writes to the register. 0- No ACK'd transactions since bit was last cleared. 1- Indicates a transaction ended with an ACK. Sticky (individual bits)
3:0	mode[3:0]	The mode controls how the USB SIE responds to traffic and how the USB SIE changes the mode of that endpoint as a result of host packets to the endpoint.

1.3.558 USB_ARB_EP1_CFG

Endpoint Configuration Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP1_CFG: 0x6080

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Retention	NA				NONRET	NONRET	NONRET	NONRET
Name	RSVD				reset_ptr	crc_bypass	dma_req	in_data_rdy

Endpoint Configuration Register This register is clocked with AHB Bus Clock

Bits	Name	Description
3	reset_ptr	Configuration Setting to Reset the RA and WA Pointers to their start values at the End of Packet transaction. 0: Do not Reset Pointer; Krypton Backward compatibility mode; 1: Reset Pointer; recommended value for reduction of CPU Configuration Writes.
2	crc_bypass	Configuration Setting to prevent CRC bytes from being written to memory and being read by firmware 0: No CRC bypass; CRC bytes will be written to memory and Termin will be generated for the CRC byte/s 1: CRC Bypass Set; CRC bytes will not be written into memory and Termin will be generated for the last data byte/s
1	dma_req	Manual DMA Request for a particular (1 to 8) endpoint; 0 to 1 Transition detected => Edge Sensitive. 0: No DMA Request. 1: Raise DMA Request
0	in_data_rdy	Indication that Endpoint Packet Data is Ready in Main memory; Level Sensitive.

1.3.559 USB_ARB_EP1_INT_EN

Endpoint Interrupt Enable Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP1_INT_EN: 0x6081

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA			R	R	R	R	R
Retention	NA			NONRET	NONRET	NONRET	NONRET	NONRET
Name	RSVD			err_int_en	buf_under_en	buf_over_en	dma_gnt_en	in_buf_full_en

Endpoint Interrupt Enable Register This register is clocked with AHB Bus Clock

Bits	Name	Description
4	err_int_en	Endpoint Error in Transaction Interrupt Enable
3	buf_under_en	Endpoint Buffer Underflow Enable
2	buf_over_en	Endpoint Buffer Overflow Enable
1	dma_gnt_en	Endpoint DMA Grant Enable
0	in_buf_full_en	IN Endpoint Local Buffer Full Enable

1.3.560 USB_ARB_EP1_SR

Endpoint Status Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP1_SR: 0x6082

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0
HW Access	NA				R/W	R/W	R/W	R/W
Retention	NA				NONRET	NONRET	NONRET	NONRET
Name	RSVD				buf_under	buf_over	dma_gnt	in_buf_full

Endpoint Status Register This register is clocked with AHB Bus Clock

Bits	Name	Description
3	buf_under	Endpoint Buffer Underflow Indication
2	buf_over	Endpoint Buffer Overflow Indication
1	dma_gnt	Endpoint DMA Grant Indication
0	in_buf_full	IN Endpoint Local Buffer Full Indication

1.3.561 USB_ARB_RW1_WA

Endpoint Write Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW1_WA: 0x6084

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	wa							

Write Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	wa[7:0]	Write Address for EP

1.3.562 USB_ARB_RW1_WA_MSB

Endpoint Write Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW1_WA_MSB: 0x6085

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Retention	NA							NONRET
Name	RSVD							wa_msb

Write Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	wa_msb	Write Address for EP

1.3.563 USB_ARB_RW1_RA

Endpoint Read Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW1_RA: 0x6086

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	ra							

Read Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	ra[7:0]	Read Address for EP

1.3.564 USB_ARB_RW1_RA_MSB

Endpoint Read Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW1_RA_MSB: 0x6087

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Retention	NA							NONRET
Name	RSVD							ra_msb

Read Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	ra_msb	Read Address for EP

1.3.565 USB_ARB_RW1_DR

Endpoint Data Register

Reset: N/A

Register : Address

USB_ARB_RW1_DR: 0x6088

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	dr							

Data Register for Endpoint ; This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	dr[7:0]	Data Register for EP ; This register is linked to the memory, hence reset value is undefined.

1.3.566 USB_BUF_SIZE

Dedicated Endpoint Buffer Size Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_BUF_SIZE: 0x608C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0000				R/W:0000			
HW Access	R				R			
Retention	NONRET				NONRET			
Name	out_buf				in_buf			

Dedicated buffer size for IN and OUT type Endpoints; Encoded power of 2 value; Eg: 1 => 2 bytes; 2 => 4 bytes; 9 => 512 bytes This register is clocked with AHB Bus Clock

Bits	Name	Description
7:4	out_buf[3:0]	Buffer size for OUT Endpoints.
3:0	in_buf[3:0]	Buffer size for IN Endpoints.

1.3.567 USB_EP_ACTIVE

Endpoint Active Indication Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_EP_ACTIVE: 0x608E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Retention	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET
Name	ep8_act	ep7_act	ep6_act	ep5_act	ep4_act	ep3_act	ep2_act	ep1_act

Endpoint Active Register; Indicates if an Endpoint is active or not; Required to be programmed only in the case of Automatic Memory Management mode of operation. This register is clocked with AHB Bus Clock

Bits	Name	Description
7	ep8_act	Endpoint 8 Active Indication. 0: Inactive. 1: Active
6	ep7_act	Endpoint 7 Active Indication. 0: Inactive. 1: Active
5	ep6_act	Endpoint 6 Active Indication. 0: Inactive. 1: Active
4	ep5_act	Endpoint 5 Active Indication. 0: Inactive. 1: Active
3	ep4_act	Endpoint 4 Active Indication. 0: Inactive. 1: Active
2	ep3_act	Endpoint 3 Active Indication. 0: Inactive. 1: Active
1	ep2_act	Endpoint 2 Active Indication. 0: Inactive. 1: Active
0	ep1_act	Endpoint 1 Active Indication. 0: Inactive. 1: Active

1.3.568 USB_EP_TYPE

Endpoint Type (IN/OUT) Indication

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_EP_TYPE: 0x608F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Retention	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET
Name	ep8_typ	ep7_typ	ep6_typ	ep5_typ	ep4_typ	ep3_typ	ep2_typ	ep1_typ

Endpoint Type Register; Indicates the Endpoint Type as IN / OUT. Value is valid if EP_ACTIVE bit is set for the corresponding Endpoint. This register is clocked with AHB Bus Clock

Bits	Name	Description
7	ep8_typ	Endpoint 8 Type Indication. 0: IN. 1: OUT
6	ep7_typ	Endpoint 7 Type Indication. 0: IN. 1: OUT
5	ep6_typ	Endpoint 6 Type Indication. 0: IN. 1: OUT
4	ep5_typ	Endpoint 5 Type Indication. 0: IN. 1: OUT
3	ep4_typ	Endpoint 4 Type Indication. 0: IN. 1: OUT
2	ep3_typ	Endpoint 3 Type Indication. 0: IN. 1: OUT
1	ep2_typ	Endpoint 2 Type Indication. 0: IN. 1: OUT
0	ep1_typ	Endpoint 1 Type Indication. 0: IN. 1: OUT

1.3.569 USB_ARB_EP2_CFG

Endpoint Configuration Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP2_CFG: 0x6090

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Retention	NA				NONRET	NONRET	NONRET	NONRET
Name	RSVD				reset_ptr	crc_bypass	dma_req	in_data_rdy

Endpoint Configuration Register This register is clocked with AHB Bus Clock

Bits	Name	Description
3	reset_ptr	Configuration Setting to Reset the RA and WA Pointers to their start values at the End of Packet transaction. 0: Do not Reset Pointer; Krypton Backward compatibility mode; 1: Reset Pointer; recommended value for reduction of CPU Configuration Writes.
2	crc_bypass	Configuration Setting to prevent CRC bytes from being written to memory and being read by firmware 0: No CRC bypass; CRC bytes will be written to memory and Termin will be generated for the CRC byte/s 1: CRC Bypass Set; CRC bytes will not be written into memory and Termin will be generated for the last data byte/s
1	dma_req	Manual DMA Request for a particular (1 to 8) endpoint; 0 to 1 Transition detected => Edge Sensitive. 0: No DMA Request. 1: Raise DMA Request
0	in_data_rdy	Indication that Endpoint Packet Data is Ready in Main memory; Level Sensitive.

1.3.570 USB_ARB_EP2_INT_EN

Endpoint Interrupt Enable Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP2_INT_EN: 0x6091

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA			R	R	R	R	R
Retention	NA			NONRET	NONRET	NONRET	NONRET	NONRET
Name	RSVD			err_int_en	buf_under_en	buf_over_en	dma_gnt_en	in_buf_full_en

Endpoint Interrupt Enable Register This register is clocked with AHB Bus Clock

Bits	Name	Description
4	err_int_en	Endpoint Error in Transaction Interrupt Enable
3	buf_under_en	Endpoint Buffer Underflow Enable
2	buf_over_en	Endpoint Buffer Overflow Enable
1	dma_gnt_en	Endpoint DMA Grant Enable
0	in_buf_full_en	IN Endpoint Local Buffer Full Enable

1.3.571 USB_ARB_EP2_SR

Endpoint Status Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP2_SR: 0x6092

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0
HW Access	NA				R/W	R/W	R/W	R/W
Retention	NA				NONRET	NONRET	NONRET	NONRET
Name	RSVD				buf_under	buf_over	dma_gnt	in_buf_full

Endpoint Status Register This register is clocked with AHB Bus Clock

Bits	Name	Description
3	buf_under	Endpoint Buffer Underflow Indication
2	buf_over	Endpoint Buffer Overflow Indication
1	dma_gnt	Endpoint DMA Grant Indication
0	in_buf_full	IN Endpoint Local Buffer Full Indication

1.3.572 USB_ARB_RW2_WA

Endpoint Write Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW2_WA: 0x6094

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	wa							

Write Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	wa[7:0]	Write Address for EP

1.3.573 USB_ARB_RW2_WA_MSB

Endpoint Write Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW2_WA_MSB: 0x6095

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Retention	NA							NONRET
Name	RSVD							wa_msb

Write Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	wa_msb	Write Address for EP

1.3.574 USB_ARB_RW2_RA

Endpoint Read Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW2_RA: 0x6096

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	ra							

Read Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	ra[7:0]	Read Address for EP

1.3.575 USB_ARB_RW2_RA_MSB

Endpoint Read Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW2_RA_MSB: 0x6097

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Retention	NA							NONRET
Name	RSVD							ra_msb

Read Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	ra_msb	Read Address for EP

1.3.576 USB_ARB_RW2_DR

Endpoint Data Register

Reset: N/A

Register : Address

USB_ARB_RW2_DR: 0x6098

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	dr							

Data Register for Endpoint ; This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	dr[7:0]	Data Register for EP ; This register is linked to the memory, hence reset value is undefined.

1.3.577 USB_ARB_CFG

Arbiter Configuration Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_CFG: 0x609C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:00		R/W:0	NA:0000			
HW Access	R	R		R	NA			
Retention	NONRET	NONRET		NONRET	NA			
Name	cfg_cmp	dma_cfg		auto_mem	RSVD			

Arbiter Configuration Register. For MODE I Operation: This register can be left in its default state. For MODE II and MODE III Operation: This register should be programmed. Cfg_cmp bit set to 0 during configuration of PFSUSB Registers. Cfg_cmp bit set to 1 once configuration is complete. This should then be held at 1 during functional mode. Similarly auto_mem and dma_cfg settings are static and should not be modified during block operation. This register is clocked with AHB Bus Clock

Bits	Name	Description
7	cfg_cmp	Register Configuration Complete Indication. Posedge is detected on this bit. Hence a 0 to 1 transition is required. 0: Configuration in progress. 1: Configuration complete.
6:5	dma_cfg[1:0]	DMA Access Configuration. 00: No DMA. 01: Manual DMA. 10: Auto DMA and Manual DMA. 11: Reserved.
4	auto_mem	Auto / Manual Memory Configuration. 0: Manual Memory Config (CPU). 1: Auto Memory Configl

1.3.578 USB_USB_CLK_EN

USB Block Clock Enable Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_USB_CLK_EN: 0x609D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Retention	NA							NONRET
Name	RSVD							csr_clk_en

USB Block Clock Enable Register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	csr_clk_en	Clock Enable for Core Logic clocked by AHB bus clock

1.3.579 USB_ARB_INT_EN

Arbiter Interrupt Enable

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_INT_EN: 0x609E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Retention	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET
Name	ep8_intr_en	ep7_intr_en	ep6_intr_en	ep5_intr_en	ep4_intr_en	ep3_intr_en	ep2_intr_en	ep1_intr_en

Arbiter Interrupt Enable Register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7	ep8_intr_en	EP8 Interrupt Enable. 0: Do not raise EP8 Interrupt. 1: Raise EP8 Interrupt
6	ep7_intr_en	EP7 Interrupt Enable. 0: Do not raise EP7 Interrupt. 1: Raise EP7 Interrupt
5	ep6_intr_en	EP6 Interrupt Enable. 0: Do not raise EP6 Interrupt. 1: Raise EP6 Interrupt
4	ep5_intr_en	EP5 Interrupt Enable. 0: Do not raise EP5 Interrupt. 1: Raise EP5 Interrupt
3	ep4_intr_en	EP4 Interrupt Enable. 0: Do not raise EP4 Interrupt. 1: Raise EP4 Interrupt
2	ep3_intr_en	EP3 Interrupt Enable. 0: Do not raise EP3 Interrupt. 1: Raise EP3 Interrupt
1	ep2_intr_en	EP2 Interrupt Enable. 0: Do not raise EP2 Interrupt. 1: Raise EP2 Interrupt
0	ep1_intr_en	EP1 Interrupt Enable. 0: Do not raise EP1 Interrupt. 1: Raise EP1 Interrupt

1.3.580 USB_ARB_INT_SR

Arbiter Interrupt Status

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_INT_SR: 0x609F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0	R:0	R:0	R:0	R:0	R:0	R:0	R:0
HW Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Retention	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET
Name	ep8_intr	ep7_intr	ep6_intr	ep5_intr	ep4_intr	ep3_intr	ep2_intr	ep1_intr

Arbiter Status Register. This is an Interrupt Status Register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7	ep8_intr	EP8 Interrupt Status. 0: EP8 Interrupt not raised. 1: EP8 Interrupt Present
6	ep7_intr	EP7 Interrupt Status. 0: EP7 Interrupt not raised. 1: EP7 Interrupt Present
5	ep6_intr	EP6 Interrupt Status. 0: EP6 Interrupt not raised. 1: EP6 Interrupt Present
4	ep5_intr	EP5 Interrupt Status. 0: EP5 Interrupt not raised. 1: EP5 Interrupt Present
3	ep4_intr	EP4 Interrupt Status. 0: EP4 Interrupt not raised. 1: EP4 Interrupt Present
2	ep3_intr	EP3 Interrupt Status. 0: EP3 Interrupt not raised. 1: EP3 Interrupt Present
1	ep2_intr	EP2 Interrupt Status. 0: EP2 Interrupt not raised. 1: EP2 Interrupt Present
0	ep1_intr	EP1 Interrupt Status. 0: EP1 Interrupt not raised. 1: EP1 Interrupt Present

1.3.581 USB_ARB_EP3_CFG

Endpoint Configuration Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP3_CFG: 0x60A0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Retention	NA				NONRET	NONRET	NONRET	NONRET
Name	RSVD				reset_ptr	crc_bypass	dma_req	in_data_rdy

Endpoint Configuration Register This register is clocked with AHB Bus Clock

Bits	Name	Description
3	reset_ptr	Configuration Setting to Reset the RA and WA Pointers to their start values at the End of Packet transaction. 0: Do not Reset Pointer; Krypton Backward compatibility mode; 1: Reset Pointer; recommended value for reduction of CPU Configuration Writes.
2	crc_bypass	Configuration Setting to prevent CRC bytes from being written to memory and being read by firmware 0: No CRC bypass; CRC bytes will be written to memory and Termin will be generated for the CRC byte/s 1: CRC Bypass Set; CRC bytes will not be written into memory and Termin will be generated for the last data byte/s
1	dma_req	Manual DMA Request for a particular (1 to 8) endpoint; 0 to 1 Transition detected => Edge Sensitive. 0: No DMA Request. 1: Raise DMA Request
0	in_data_rdy	Indication that Endpoint Packet Data is Ready in Main memory; Level Sensitive.

1.3.582 USB_ARB_EP3_INT_EN

Endpoint Interrupt Enable Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP3_INT_EN: 0x60A1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA			R	R	R	R	R
Retention	NA			NONRET	NONRET	NONRET	NONRET	NONRET
Name	RSVD			err_int_en	buf_under_en	buf_over_en	dma_gnt_en	in_buf_full_en

Endpoint Interrupt Enable Register This register is clocked with AHB Bus Clock

Bits	Name	Description
4	err_int_en	Endpoint Error in Transaction Interrupt Enable
3	buf_under_en	Endpoint Buffer Underflow Enable
2	buf_over_en	Endpoint Buffer Overflow Enable
1	dma_gnt_en	Endpoint DMA Grant Enable
0	in_buf_full_en	IN Endpoint Local Buffer Full Enable

1.3.583 USB_ARB_EP3_SR

Endpoint Status Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP3_SR: 0x60A2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0
HW Access	NA				R/W	R/W	R/W	R/W
Retention	NA				NONRET	NONRET	NONRET	NONRET
Name	RSVD				buf_under	buf_over	dma_gnt	in_buf_full

Endpoint Status Register This register is clocked with AHB Bus Clock

Bits	Name	Description
3	buf_under	Endpoint Buffer Underflow Indication
2	buf_over	Endpoint Buffer Overflow Indication
1	dma_gnt	Endpoint DMA Grant Indication
0	in_buf_full	IN Endpoint Local Buffer Full Indication

1.3.584 USB_ARB_RW3_WA

Endpoint Write Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW3_WA: 0x60A4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	wa							

Write Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	wa[7:0]	Write Address for EP

1.3.585 USB_ARB_RW3_WA_MSB

Endpoint Write Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW3_WA_MSB: 0x60A5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Retention	NA							NONRET
Name	RSVD							wa_msb

Write Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	wa_msb	Write Address for EP

1.3.586 USB_ARB_RW3_RA

Endpoint Read Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW3_RA: 0x60A6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	ra							

Read Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	ra[7:0]	Read Address for EP

1.3.587 USB_ARB_RW3_RA_MSB

Endpoint Read Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW3_RA_MSB: 0x60A7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Retention	NA							NONRET
Name	RSVD							ra_msb

Read Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	ra_msb	Read Address for EP

1.3.588 USB_ARB_RW3_DR

Endpoint Data Register

Reset: N/A

Register : Address

USB_ARB_RW3_DR: 0x60A8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	dr							

Data Register for Endpoint ; This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	dr[7:0]	Data Register for EP ; This register is linked to the memory, hence reset value is undefined.

1.3.589 USB_CWA

Common Area Write Address

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_CWA: 0x60AC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	cwa							

Write Address Pointer for Common Area; LSB 8 bits of the 9 bit pointer are stored in this register. This register is only valid in Mode3 operation. Although it is R/W register for CPU, all intended updates are performed by the block and CPU can access the value for debug purposes. This register will indicate the Common Area location in memory. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	cwa[7:0]	Write Address for Common Area

1.3.590 USB_CWA_MSB

Common Area Write Address

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_CWA_MSB: 0x60AD

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Retention	NA							NONRET
Name	RSVD							cwa_msb

Write Address Pointer for Common Area; MSB of the 9 bit pointer are stored in this register. This register is only valid in Mode3 operation. Although it is R/W register for CPU, all intended updates are performed by the block and CPU can access the value for debug purposes. This register will indicate the Common Area location in memory. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	cwa_msb	Write Address for Common Area

1.3.591 USB_ARB_EP4_CFG

Endpoint Configuration Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP4_CFG: 0x60B0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Retention	NA				NONRET	NONRET	NONRET	NONRET
Name	RSVD				reset_ptr	crc_bypass	dma_req	in_data_rdy

Endpoint Configuration Register This register is clocked with AHB Bus Clock

Bits	Name	Description
3	reset_ptr	Configuration Setting to Reset the RA and WA Pointers to their start values at the End of Packet transaction. 0: Do not Reset Pointer; Krypton Backward compatibility mode; 1: Reset Pointer; recommended value for reduction of CPU Configuration Writes.
2	crc_bypass	Configuration Setting to prevent CRC bytes from being written to memory and being read by firmware 0: No CRC bypass; CRC bytes will be written to memory and Termin will be generated for the CRC byte/s 1: CRC Bypass Set; CRC bytes will not be written into memory and Termin will be generated for the last data byte/s
1	dma_req	Manual DMA Request for a particular (1 to 8) endpoint; 0 to 1 Transition detected => Edge Sensitive. 0: No DMA Request. 1: Raise DMA Request
0	in_data_rdy	Indication that Endpoint Packet Data is Ready in Main memory; Level Sensitive.

1.3.592 USB_ARB_EP4_INT_EN

Endpoint Interrupt Enable Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP4_INT_EN: 0x60B1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA			R	R	R	R	R
Retention	NA			NONRET	NONRET	NONRET	NONRET	NONRET
Name	RSVD			err_int_en	buf_under_en	buf_over_en	dma_gnt_en	in_buf_full_en

Endpoint Interrupt Enable Register This register is clocked with AHB Bus Clock

Bits	Name	Description
4	err_int_en	Endpoint Error in Transaction Interrupt Enable
3	buf_under_en	Endpoint Buffer Underflow Enable
2	buf_over_en	Endpoint Buffer Overflow Enable
1	dma_gnt_en	Endpoint DMA Grant Enable
0	in_buf_full_en	IN Endpoint Local Buffer Full Enable

1.3.593 USB_ARB_EP4_SR

Endpoint Status Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP4_SR: 0x60B2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0
HW Access	NA				R/W	R/W	R/W	R/W
Retention	NA				NONRET	NONRET	NONRET	NONRET
Name	RSVD				buf_under	buf_over	dma_gnt	in_buf_full

Endpoint Status Register This register is clocked with AHB Bus Clock

Bits	Name	Description
3	buf_under	Endpoint Buffer Underflow Indication
2	buf_over	Endpoint Buffer Overflow Indication
1	dma_gnt	Endpoint DMA Grant Indication
0	in_buf_full	IN Endpoint Local Buffer Full Indication

1.3.594 USB_ARB_RW4_WA

Endpoint Write Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW4_WA: 0x60B4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	wa							

Write Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	wa[7:0]	Write Address for EP

1.3.595 USB_ARB_RW4_WA_MSB

Endpoint Write Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW4_WA_MSB: 0x60B5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Retention	NA							NONRET
Name	RSVD							wa_msb

Write Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	wa_msb	Write Address for EP

1.3.596 USB_ARB_RW4_RA

Endpoint Read Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW4_RA: 0x60B6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	ra							

Read Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	ra[7:0]	Read Address for EP

1.3.597 USB_ARB_RW4_RA_MSB

Endpoint Read Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW4_RA_MSB: 0x60B7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Retention	NA							NONRET
Name	RSVD							ra_msb

Read Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	ra_msb	Read Address for EP

1.3.598 USB_ARB_RW4_DR

Endpoint Data Register

Reset: N/A

Register : Address

USB_ARB_RW4_DR: 0x60B8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	dr							

Data Register for Endpoint ; This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	dr[7:0]	Data Register for EP ; This register is linked to the memory, hence reset value is undefined.

1.3.599 USB_DMA_THRES

DMA Burst / Threshold Configuration

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_DMA_THRES: 0x60BC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	dma_ths							

It contains 8 LSB bits of DMA Threshold Register This register is only valid in Mode3 operation. This register should be programmed to the same value as the DMA Burst Count programmed in the corresponding Channel Basic Config Register in PHUB. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	dma_ths[7:0]	8 Lsb bits of 9 bit DMA Threshold count.

1.3.600 USB_DMA_THRES_MSB

DMA Burst / Threshold Configuration

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_DMA_THRES_MSB: 0x60BD

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Retention	NA							NONRET
Name	RSVD							dma_ths_msb

It contains the MSB bit of DMA Threshold Register This register is clocked with AHB Bus Clock

Bits	Name	Description
0	dma_ths_msb	Msb bit of 9 bit DMA Threshold count.

1.3.601 USB_ARB_EP5_CFG

Endpoint Configuration Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP5_CFG: 0x60C0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Retention	NA				NONRET	NONRET	NONRET	NONRET
Name	RSVD				reset_ptr	crc_bypass	dma_req	in_data_rdy

Endpoint Configuration Register This register is clocked with AHB Bus Clock

Bits	Name	Description
3	reset_ptr	Configuration Setting to Reset the RA and WA Pointers to their start values at the End of Packet transaction. 0: Do not Reset Pointer; Krypton Backward compatibility mode; 1: Reset Pointer; recommended value for reduction of CPU Configuration Writes.
2	crc_bypass	Configuration Setting to prevent CRC bytes from being written to memory and being read by firmware 0: No CRC bypass; CRC bytes will be written to memory and Termin will be generated for the CRC byte/s 1: CRC Bypass Set; CRC bytes will not be written into memory and Termin will be generated for the last data byte/s
1	dma_req	Manual DMA Request for a particular (1 to 8) endpoint; 0 to 1 Transition detected => Edge Sensitive. 0: No DMA Request. 1: Raise DMA Request
0	in_data_rdy	Indication that Endpoint Packet Data is Ready in Main memory; Level Sensitive.

1.3.602 USB_ARB_EP5_INT_EN

Endpoint Interrupt Enable Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP5_INT_EN: 0x60C1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA			R	R	R	R	R
Retention	NA			NONRET	NONRET	NONRET	NONRET	NONRET
Name	RSVD			err_int_en	buf_under_en	buf_over_en	dma_gnt_en	in_buf_full_en

Endpoint Interrupt Enable Register This register is clocked with AHB Bus Clock

Bits	Name	Description
4	err_int_en	Endpoint Error in Transaction Interrupt Enable
3	buf_under_en	Endpoint Buffer Underflow Enable
2	buf_over_en	Endpoint Buffer Overflow Enable
1	dma_gnt_en	Endpoint DMA Grant Enable
0	in_buf_full_en	IN Endpoint Local Buffer Full Enable

1.3.603 USB_ARB_EP5_SR

Endpoint Status Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP5_SR: 0x60C2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0
HW Access	NA				R/W	R/W	R/W	R/W
Retention	NA				NONRET	NONRET	NONRET	NONRET
Name	RSVD				buf_under	buf_over	dma_gnt	in_buf_full

Endpoint Status Register This register is clocked with AHB Bus Clock

Bits	Name	Description
3	buf_under	Endpoint Buffer Underflow Indication
2	buf_over	Endpoint Buffer Overflow Indication
1	dma_gnt	Endpoint DMA Grant Indication
0	in_buf_full	IN Endpoint Local Buffer Full Indication

1.3.604 USB_ARB_RW5_WA

Endpoint Write Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW5_WA: 0x60C4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	wa							

Write Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	wa[7:0]	Write Address for EP

1.3.605 USB_ARB_RW5_WA_MSB

Endpoint Write Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW5_WA_MSB: 0x60C5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Retention	NA							NONRET
Name	RSVD							wa_msb

Write Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	wa_msb	Write Address for EP

1.3.606 USB_ARB_RW5_RA

Endpoint Read Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW5_RA: 0x60C6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	ra							

Read Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	ra[7:0]	Read Address for EP

1.3.607 USB_ARB_RW5_RA_MSB

Endpoint Read Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW5_RA_MSB: 0x60C7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Retention	NA							NONRET
Name	RSVD							ra_msb

Read Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	ra_msb	Read Address for EP

1.3.608 USB_ARB_RW5_DR

Endpoint Data Register

Reset: N/A

Register : Address

USB_ARB_RW5_DR: 0x60C8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	dr							

Data Register for Endpoint ; This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	dr[7:0]	Data Register for EP ; This register is linked to the memory, hence reset value is undefined.

1.3.609 USB_BUS_RST_CNT

Bus Reset Count Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_BUS_RST_CNT: 0x60CC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:1010			
HW Access	NA				R			
Retention	NA				NONRET			
Name	RSVD				bus_rst_cnt			

Bus Reset Count register ; For USB bus reset length; The value in this register determines the no. of pulses of the low freq. clock which will be counted to determine if an SE0 condition has been held for long enough to declare a USB Bus reset condition. In krypton, 3 pulses of a 32 KHz clock were counted to declare a usb bus reset condition. In leopard, a 100 KHz clock is used. Recommended is to count 10 pulses of this clock to remain equivalent to Krypton. This register is clocked with AHB Bus Clock

Bits	Name	Description
3:0	bus_rst_cnt[3:0]	Bus Reset Count Length

1.3.610 USB_ARB_EP6_CFG

Endpoint Configuration Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP6_CFG: 0x60D0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Retention	NA				NONRET	NONRET	NONRET	NONRET
Name	RSVD				reset_ptr	crc_bypass	dma_req	in_data_rdy

Endpoint Configuration Register This register is clocked with AHB Bus Clock

Bits	Name	Description
3	reset_ptr	Configuration Setting to Reset the RA and WA Pointers to their start values at the End of Packet transaction. 0: Do not Reset Pointer; Krypton Backward compatibility mode; 1: Reset Pointer; recommended value for reduction of CPU Configuration Writes.
2	crc_bypass	Configuration Setting to prevent CRC bytes from being written to memory and being read by firmware 0: No CRC bypass; CRC bytes will be written to memory and Termin will be generated for the CRC byte/s 1: CRC Bypass Set; CRC bytes will not be written into memory and Termin will be generated for the last data byte/s
1	dma_req	Manual DMA Request for a particular (1 to 8) endpoint; 0 to 1 Transition detected => Edge Sensitive. 0: No DMA Request. 1: Raise DMA Request
0	in_data_rdy	Indication that Endpoint Packet Data is Ready in Main memory; Level Sensitive.

1.3.611 USB_ARB_EP6_INT_EN

Endpoint Interrupt Enable Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP6_INT_EN: 0x60D1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA			R	R	R	R	R
Retention	NA			NONRET	NONRET	NONRET	NONRET	NONRET
Name	RSVD			err_int_en	buf_under_en	buf_over_en	dma_gnt_en	in_buf_full_en

Endpoint Interrupt Enable Register This register is clocked with AHB Bus Clock

Bits	Name	Description
4	err_int_en	Endpoint Error in Transaction Interrupt Enable
3	buf_under_en	Endpoint Buffer Underflow Enable
2	buf_over_en	Endpoint Buffer Overflow Enable
1	dma_gnt_en	Endpoint DMA Grant Enable
0	in_buf_full_en	IN Endpoint Local Buffer Full Enable

1.3.612 USB_ARB_EP6_SR

Endpoint Status Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP6_SR: 0x60D2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0
HW Access	NA				R/W	R/W	R/W	R/W
Retention	NA				NONRET	NONRET	NONRET	NONRET
Name	RSVD				buf_under	buf_over	dma_gnt	in_buf_full

Endpoint Status Register This register is clocked with AHB Bus Clock

Bits	Name	Description
3	buf_under	Endpoint Buffer Underflow Indication
2	buf_over	Endpoint Buffer Overflow Indication
1	dma_gnt	Endpoint DMA Grant Indication
0	in_buf_full	IN Endpoint Local Buffer Full Indication

1.3.613 USB_ARB_RW6_WA

Endpoint Write Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW6_WA: 0x60D4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	wa							

Write Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	wa[7:0]	Write Address for EP

1.3.614 USB_ARB_RW6_WA_MSB

Endpoint Write Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW6_WA_MSB: 0x60D5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Retention	NA							NONRET
Name	RSVD							wa_msb

Write Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	wa_msb	Write Address for EP

1.3.615 USB_ARB_RW6_RA

Endpoint Read Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW6_RA: 0x60D6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	ra							

Read Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	ra[7:0]	Read Address for EP

1.3.616 USB_ARB_RW6_RA_MSB

Endpoint Read Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW6_RA_MSB: 0x60D7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Retention	NA							NONRET
Name	RSVD							ra_msb

Read Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	ra_msb	Read Address for EP

1.3.617 USB_ARB_RW6_DR

Endpoint Data Register

Reset: N/A

Register : Address

USB_ARB_RW6_DR: 0x60D8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	dr							

Data Register for Endpoint ; This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	dr[7:0]	Data Register for EP ; This register is linked to the memory, hence reset value is undefined.

1.3.618 USB_ARB_EP7_CFG

Endpoint Configuration Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP7_CFG: 0x60E0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Retention	NA				NONRET	NONRET	NONRET	NONRET
Name	RSVD				reset_ptr	crc_bypass	dma_req	in_data_rdy

Endpoint Configuration Register This register is clocked with AHB Bus Clock

Bits	Name	Description
3	reset_ptr	Configuration Setting to Reset the RA and WA Pointers to their start values at the End of Packet transaction. 0: Do not Reset Pointer; Krypton Backward compatibility mode; 1: Reset Pointer; recommended value for reduction of CPU Configuration Writes.
2	crc_bypass	Configuration Setting to prevent CRC bytes from being written to memory and being read by firmware 0: No CRC bypass; CRC bytes will be written to memory and Termin will be generated for the CRC byte/s 1: CRC Bypass Set; CRC bytes will not be written into memory and Termin will be generated for the last data byte/s
1	dma_req	Manual DMA Request for a particular (1 to 8) endpoint; 0 to 1 Transition detected => Edge Sensitive. 0: No DMA Request. 1: Raise DMA Request
0	in_data_rdy	Indication that Endpoint Packet Data is Ready in Main memory; Level Sensitive.

1.3.619 USB_ARB_EP7_INT_EN

Endpoint Interrupt Enable Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP7_INT_EN: 0x60E1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA			R	R	R	R	R
Retention	NA			NONRET	NONRET	NONRET	NONRET	NONRET
Name	RSVD			err_int_en	buf_under_en	buf_over_en	dma_gnt_en	in_buf_full_en

Endpoint Interrupt Enable Register This register is clocked with AHB Bus Clock

Bits	Name	Description
4	err_int_en	Endpoint Error in Transaction Interrupt Enable
3	buf_under_en	Endpoint Buffer Underflow Enable
2	buf_over_en	Endpoint Buffer Overflow Enable
1	dma_gnt_en	Endpoint DMA Grant Enable
0	in_buf_full_en	IN Endpoint Local Buffer Full Enable

1.3.620 USB_ARB_EP7_SR

Endpoint Status Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP7_SR: 0x60E2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0
HW Access	NA				R/W	R/W	R/W	R/W
Retention	NA				NONRET	NONRET	NONRET	NONRET
Name	RSVD				buf_under	buf_over	dma_gnt	in_buf_full

Endpoint Status Register This register is clocked with AHB Bus Clock

Bits	Name	Description
3	buf_under	Endpoint Buffer Underflow Indication
2	buf_over	Endpoint Buffer Overflow Indication
1	dma_gnt	Endpoint DMA Grant Indication
0	in_buf_full	IN Endpoint Local Buffer Full Indication

1.3.621 USB_ARB_RW7_WA

Endpoint Write Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW7_WA: 0x60E4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	wa							

Write Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	wa[7:0]	Write Address for EP

1.3.622 USB_ARB_RW7_WA_MSB

Endpoint Write Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW7_WA_MSB: 0x60E5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Retention	NA							NONRET
Name	RSVD							wa_msb

Write Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	wa_msb	Write Address for EP

1.3.623 USB_ARB_RW7_RA

Endpoint Read Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW7_RA: 0x60E6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	ra							

Read Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	ra[7:0]	Read Address for EP

1.3.624 USB_ARB_RW7_RA_MSB

Endpoint Read Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW7_RA_MSB: 0x60E7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Retention	NA							NONRET
Name	RSVD							ra_msb

Read Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	ra_msb	Read Address for EP

1.3.625 USB_ARB_RW7_DR

Endpoint Data Register

Reset: N/A

Register : Address

USB_ARB_RW7_DR: 0x60E8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	dr							

Data Register for Endpoint ; This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	dr[7:0]	Data Register for EP ; This register is linked to the memory, hence reset value is undefined.

1.3.626 USB_ARB_EP8_CFG

Endpoint Configuration Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP8_CFG: 0x60F0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Retention	NA				NONRET	NONRET	NONRET	NONRET
Name	RSVD				reset_ptr	crc_bypass	dma_req	in_data_rdy

Endpoint Configuration Register This register is clocked with AHB Bus Clock

Bits	Name	Description
3	reset_ptr	Configuration Setting to Reset the RA and WA Pointers to their start values at the End of Packet transaction. 0: Do not Reset Pointer; Krypton Backward compatibility mode; 1: Reset Pointer; recommended value for reduction of CPU Configuration Writes.
2	crc_bypass	Configuration Setting to prevent CRC bytes from being written to memory and being read by firmware 0: No CRC bypass; CRC bytes will be written to memory and Termin will be generated for the CRC byte/s 1: CRC Bypass Set; CRC bytes will not be written into memory and Termin will be generated for the last data byte/s
1	dma_req	Manual DMA Request for a particular (1 to 8) endpoint; 0 to 1 Transition detected => Edge Sensitive. 0: No DMA Request. 1: Raise DMA Request
0	in_data_rdy	Indication that Endpoint Packet Data is Ready in Main memory; Level Sensitive.

1.3.627 USB_ARB_EP8_INT_EN

Endpoint Interrupt Enable Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP8_INT_EN: 0x60F1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA			R	R	R	R	R
Retention	NA			NONRET	NONRET	NONRET	NONRET	NONRET
Name	RSVD			err_int_en	buf_under_en	buf_over_en	dma_gnt_en	in_buf_full_en

Endpoint Interrupt Enable Register This register is clocked with AHB Bus Clock

Bits	Name	Description
4	err_int_en	Endpoint Error in Transaction Interrupt Enable
3	buf_under_en	Endpoint Buffer Underflow Enable
2	buf_over_en	Endpoint Buffer Overflow Enable
1	dma_gnt_en	Endpoint DMA Grant Enable
0	in_buf_full_en	IN Endpoint Local Buffer Full Enable

1.3.628 USB_ARB_EP8_SR

Endpoint Status Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_EP8_SR: 0x60F2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0
HW Access	NA				R/W	R/W	R/W	R/W
Retention	NA				NONRET	NONRET	NONRET	NONRET
Name	RSVD				buf_under	buf_over	dma_gnt	in_buf_full

Endpoint Status Register This register is clocked with AHB Bus Clock

Bits	Name	Description
3	buf_under	Endpoint Buffer Underflow Indication
2	buf_over	Endpoint Buffer Overflow Indication
1	dma_gnt	Endpoint DMA Grant Indication
0	in_buf_full	IN Endpoint Local Buffer Full Indication

1.3.629 USB_ARB_RW8_WA

Endpoint Write Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW8_WA: 0x60F4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	wa							

Write Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	wa[7:0]	Write Address for EP

1.3.630 USB_ARB_RW8_WA_MSB

Endpoint Write Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW8_WA_MSB: 0x60F5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Retention	NA							NONRET
Name	RSVD							wa_msb

Write Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	wa_msb	Write Address for EP

1.3.631 USB_ARB_RW8_RA

Endpoint Read Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW8_RA: 0x60F6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	ra							

Read Address Pointer for Endpoint ; LSB 8 bits of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	ra[7:0]	Read Address for EP

1.3.632 USB_ARB_RW8_RA_MSB

Endpoint Read Address value

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

USB_ARB_RW8_RA_MSB: 0x60F7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Retention	NA							NONRET
Name	RSVD							ra_msb

Read Address Pointer for Endpoint ; MSB 1 bit of the 9 bit pointer are stored in this register. This register is clocked with AHB Bus Clock

Bits	Name	Description
0	ra_msb	Read Address for EP

1.3.633 USB_ARB_RW8_DR

Endpoint Data Register

Reset: N/A

Register : Address

USB_ARB_RW8_DR: 0x60F8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	dr							

Data Register for Endpoint ; This register is clocked with AHB Bus Clock

Bits	Name	Description
7:0	dr[7:0]	Data Register for EP ; This register is linked to the memory, hence reset value is undefined.

1.3.634 B[0..3]_UDB00_A0

UDB00_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_A0: 0x6400

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0							

Accumulator 0

Bits	Name	Description
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.635 B[0..3]_UDB01_A0

UDB01_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_A0: 0x6401

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0							

Accumulator 0

Bits	Name	Description
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.636 B[0..3]_UDB02_A0

UDB02_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_A0: 0x6402

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0							

Accumulator 0

Bits	Name	Description
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.637 B[0..3]_UDB03_A0

UDB03_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_A0: 0x6403

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0							

Accumulator 0

Bits	Name	Description
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.638 B[0..3]_UDB04_A0

UDB04_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_A0: 0x6404 B1_UDB04_A0: 0x6504

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0							

Accumulator 0

Bits	Name	Description
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.639 B[0..3]_UDB05_A0

UDB05_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_A0: 0x6405 B1_UDB05_A0: 0x6505

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0							

Accumulator 0

Bits	Name	Description
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.640 B[0..3]_UDB06_A0

UDB06_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_A0: 0x6406 B1_UDB06_A0: 0x6506

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0							

Accumulator 0

Bits	Name	Description
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.641 B[0..3]_UDB07_A0

UDB07_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_A0: 0x6407 B1_UDB07_A0: 0x6507

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0							

Accumulator 0

Bits	Name	Description
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.642 B[0..3]_UDB08_A0

UDB08_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_A0: 0x6408 B1_UDB08_A0: 0x6508

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0							

Accumulator 0

Bits	Name	Description
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.643 B[0..3]_UDB09_A0

UDB09_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_A0: 0x6409 B1_UDB09_A0: 0x6509

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0							

Accumulator 0

Bits	Name	Description
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.644 B[0..3]_UDB10_A0

UDB10_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_A0: 0x640A B1_UDB10_A0: 0x650A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0							

Accumulator 0

Bits	Name	Description
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.645 B[0..3]_UDB11_A0

UDB11_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_A0: 0x640B B1_UDB11_A0: 0x650B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0							

Accumulator 0

Bits	Name	Description
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.646 B[0..3]_UDB12_A0

UDB12_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_A0: 0x640C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0							

Accumulator 0

Bits	Name	Description
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.647 B[0..3]_UDB13_A0

UDB13_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_A0: 0x640D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0							

Accumulator 0

Bits	Name	Description
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.648 B[0..3]_UDB14_A0

UDB14_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_A0: 0x640E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0							

Accumulator 0

Bits	Name	Description
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.649 B[0..3]_UDB15_A0

UDB15_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB15_A0: 0x640F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0							

Accumulator 0

Bits	Name	Description
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.650 B[0..3]_UDB00_A1

UDB00_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_A1: 0x6410

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1							

Accumulator 1

Bits	Name	Description
7:0	A1[7:0]	Generic field for 8 bit working registers

1.3.651 B[0..3]_UDB01_A1

UDB01_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_A1: 0x6411

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1							

Accumulator 1

Bits	Name	Description
7:0	A1[7:0]	Generic field for 8 bit working registers

1.3.652 B[0..3]_UDB02_A1

UDB02_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_A1: 0x6412

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1							

Accumulator 1

Bits	Name	Description
7:0	A1[7:0]	Generic field for 8 bit working registers

1.3.653 B[0..3]_UDB03_A1

UDB03_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_A1: 0x6413

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1							

Accumulator 1

Bits	Name	Description
7:0	A1[7:0]	Generic field for 8 bit working registers

1.3.654 B[0..3]_UDB04_A1

UDB04_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_A1: 0x6414 B1_UDB04_A1: 0x6514

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1							

Accumulator 1

Bits	Name	Description
7:0	A1[7:0]	Generic field for 8 bit working registers

1.3.655 B[0..3]_UDB05_A1

UDB05_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_A1: 0x6415 B1_UDB05_A1: 0x6515

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1							

Accumulator 1

Bits	Name	Description
7:0	A1[7:0]	Generic field for 8 bit working registers

1.3.656 B[0..3]_UDB06_A1

UDB06_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_A1: 0x6416 B1_UDB06_A1: 0x6516

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1							

Accumulator 1

Bits	Name	Description
7:0	A1[7:0]	Generic field for 8 bit working registers

1.3.657 B[0..3]_UDB07_A1

UDB07_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_A1: 0x6417 B1_UDB07_A1: 0x6517

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1							

Accumulator 1

Bits	Name	Description
7:0	A1[7:0]	Generic field for 8 bit working registers

1.3.658 B[0..3]_UDB08_A1

UDB08_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_A1: 0x6418 B1_UDB08_A1: 0x6518

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1							

Accumulator 1

Bits	Name	Description
7:0	A1[7:0]	Generic field for 8 bit working registers

1.3.659 B[0..3]_UDB09_A1

UDB09_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_A1: 0x6419 B1_UDB09_A1: 0x6519

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1							

Accumulator 1

Bits	Name	Description
7:0	A1[7:0]	Generic field for 8 bit working registers

1.3.660 B[0..3]_UDB10_A1

UDB10_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_A1: 0x641A B1_UDB10_A1: 0x651A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1							

Accumulator 1

Bits	Name	Description
7:0	A1[7:0]	Generic field for 8 bit working registers

1.3.661 B[0..3]_UDB11_A1

UDB11_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_A1: 0x641B B1_UDB11_A1: 0x651B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1							

Accumulator 1

Bits	Name	Description
7:0	A1[7:0]	Generic field for 8 bit working registers

1.3.662 B[0..3]_UDB12_A1

UDB12_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_A1: 0x641C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1							

Accumulator 1

Bits	Name	Description
7:0	A1[7:0]	Generic field for 8 bit working registers

1.3.663 B[0..3]_UDB13_A1

UDB13_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_A1: 0x641D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1							

Accumulator 1

Bits	Name	Description
7:0	A1[7:0]	Generic field for 8 bit working registers

1.3.664 B[0..3]_UDB14_A1

UDB14_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_A1: 0x641E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1							

Accumulator 1

Bits	Name	Description
7:0	A1[7:0]	Generic field for 8 bit working registers

1.3.665 B[0..3]_UDB15_A1

UDB15_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB15_A1: 0x641F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1							

Accumulator 1

Bits	Name	Description
7:0	A1[7:0]	Generic field for 8 bit working registers

1.3.666 B[0..3]_UDB00_D0

UDB00_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB00_D0: 0x6420

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0							

Data 0

Bits	Name	Description
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.667 B[0..3]_UDB01_D0

UDB01_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB01_D0: 0x6421

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0							

Data 0

Bits	Name	Description
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.668 B[0..3]_UDB02_D0

UDB02_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB02_D0: 0x6422

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0							

Data 0

Bits	Name	Description
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.669 B[0..3]_UDB03_D0

UDB03_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB03_D0: 0x6423

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0							

Data 0

Bits	Name	Description
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.670 B[0..3]_UDB04_D0

UDB04_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB04_D0: 0x6424 B1_UDB04_D0: 0x6524

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0							

Data 0

Bits	Name	Description
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.671 B[0..3]_UDB05_D0

UDB05_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB05_D0: 0x6425 B1_UDB05_D0: 0x6525

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0							

Data 0

Bits	Name	Description
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.672 B[0..3]_UDB06_D0

UDB06_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB06_D0: 0x6426 B1_UDB06_D0: 0x6526

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0							

Data 0

Bits	Name	Description
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.673 B[0..3]_UDB07_D0

UDB07_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB07_D0: 0x6427 B1_UDB07_D0: 0x6527

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0							

Data 0

Bits	Name	Description
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.674 B[0..3]_UDB08_D0

UDB08_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB08_D0: 0x6428 B1_UDB08_D0: 0x6528

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0							

Data 0

Bits	Name	Description
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.675 B[0..3]_UDB09_D0

UDB09_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB09_D0: 0x6429 B1_UDB09_D0: 0x6529

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0							

Data 0

Bits	Name	Description
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.676 B[0..3]_UDB10_D0

UDB10_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB10_D0: 0x642A B1_UDB10_D0: 0x652A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0							

Data 0

Bits	Name	Description
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.677 B[0..3]_UDB11_D0

UDB11_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB11_D0: 0x642B

B1_UDB11_D0: 0x652B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0							

Data 0

Bits	Name	Description
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.678 B[0..3]_UDB12_D0

UDB12_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB12_D0: 0x642C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0							

Data 0

Bits	Name	Description
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.679 B[0..3]_UDB13_D0

UDB13_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB13_D0: 0x642D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0							

Data 0

Bits	Name	Description
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.680 B[0..3]_UDB14_D0

UDB14_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB14_D0: 0x642E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0							

Data 0

Bits	Name	Description
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.681 B[0..3]_UDB15_D0

UDB15_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB15_D0: 0x642F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0							

Data 0

Bits	Name	Description
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.682 B[0..3]_UDB00_D1

UDB00_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB00_D1: 0x6430

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1							

Data 1

Bits	Name	Description
7:0	D1[7:0]	Generic field for 8 bit working registers

1.3.683 B[0..3]_UDB01_D1

UDB01_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB01_D1: 0x6431

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1							

Data 1

Bits	Name	Description
7:0	D1[7:0]	Generic field for 8 bit working registers

1.3.684 B[0..3]_UDB02_D1

UDB02_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB02_D1: 0x6432

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1							

Data 1

Bits	Name	Description
7:0	D1[7:0]	Generic field for 8 bit working registers

1.3.685 B[0..3]_UDB03_D1

UDB03_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB03_D1: 0x6433

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1							

Data 1

Bits	Name	Description
7:0	D1[7:0]	Generic field for 8 bit working registers

1.3.686 B[0..3]_UDB04_D1

UDB04_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB04_D1: 0x6434 B1_UDB04_D1: 0x6534

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1							

Data 1

Bits	Name	Description
7:0	D1[7:0]	Generic field for 8 bit working registers

1.3.687 B[0..3]_UDB05_D1

UDB05_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB05_D1: 0x6435 B1_UDB05_D1: 0x6535

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1							

Data 1

Bits	Name	Description
7:0	D1[7:0]	Generic field for 8 bit working registers

1.3.688 B[0..3]_UDB06_D1

UDB06_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB06_D1: 0x6436 B1_UDB06_D1: 0x6536

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1							

Data 1

Bits	Name	Description
7:0	D1[7:0]	Generic field for 8 bit working registers

1.3.689 B[0..3]_UDB07_D1

UDB07_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB07_D1: 0x6437 B1_UDB07_D1: 0x6537

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1							

Data 1

Bits	Name	Description
7:0	D1[7:0]	Generic field for 8 bit working registers

1.3.690 B[0..3]_UDB08_D1

UDB08_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB08_D1: 0x6438 B1_UDB08_D1: 0x6538

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1							

Data 1

Bits	Name	Description
7:0	D1[7:0]	Generic field for 8 bit working registers

1.3.691 B[0..3]_UDB09_D1

UDB09_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB09_D1: 0x6439 B1_UDB09_D1: 0x6539

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1							

Data 1

Bits	Name	Description
7:0	D1[7:0]	Generic field for 8 bit working registers

1.3.692 B[0..3]_UDB10_D1

UDB10_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB10_D1: 0x643A B1_UDB10_D1: 0x653A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1							

Data 1

Bits	Name	Description
7:0	D1[7:0]	Generic field for 8 bit working registers

1.3.693 B[0..3]_UDB11_D1

UDB11_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB11_D1: 0x643B B1_UDB11_D1: 0x653B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1							

Data 1

Bits	Name	Description
7:0	D1[7:0]	Generic field for 8 bit working registers

1.3.694 B[0..3]_UDB12_D1

UDB12_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB12_D1: 0x643C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1							

Data 1

Bits	Name	Description
7:0	D1[7:0]	Generic field for 8 bit working registers

1.3.695 B[0..3]_UDB13_D1

UDB13_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB13_D1: 0x643D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1							

Data 1

Bits	Name	Description
7:0	D1[7:0]	Generic field for 8 bit working registers

1.3.696 B[0..3]_UDB14_D1

UDB14_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB14_D1: 0x643E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1							

Data 1

Bits	Name	Description
7:0	D1[7:0]	Generic field for 8 bit working registers

1.3.697 B[0..3]_UDB15_D1

UDB15_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB15_D1: 0x643F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1							

Data 1

Bits	Name	Description
7:0	D1[7:0]	Generic field for 8 bit working registers

1.3.698 B[0..3]_UDB00_F0

UDB00_F0

Reset: N/A

Register : Address

B0_UDB00_F0: 0x6440

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0							

FIFO 0

Bits	Name	Description
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.699 B[0..3]_UDB01_F0

UDB01_F0

Reset: N/A

Register : Address

B0_UDB01_F0: 0x6441

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0							

FIFO 0

Bits	Name	Description
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.700 B[0..3]_UDB02_F0

UDB02_F0

Reset: N/A

Register : Address

B0_UDB02_F0: 0x6442

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0							

FIFO 0

Bits	Name	Description
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.701 B[0..3]_UDB03_F0

UDB03_F0

Reset: N/A

Register : Address

B0_UDB03_F0: 0x6443

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0							

FIFO 0

Bits	Name	Description
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.702 B[0..3]_UDB04_F0

UDB04_F0

Reset: N/A

Register : Address

B0_UDB04_F0: 0x6444 B1_UDB04_F0: 0x6544

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0							

FIFO 0

Bits	Name	Description
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.703 B[0..3]_UDB05_F0

UDB05_F0

Reset: N/A

Register : Address

B0_UDB05_F0: 0x6445 B1_UDB05_F0: 0x6545

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0							

FIFO 0

Bits	Name	Description
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.704 B[0..3]_UDB06_F0

UDB06_F0

Reset: N/A

Register : Address

B0_UDB06_F0: 0x6446 B1_UDB06_F0: 0x6546

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0							

FIFO 0

Bits	Name	Description
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.705 B[0..3]_UDB07_F0

UDB07_F0

Reset: N/A

Register : Address

B0_UDB07_F0: 0x6447 B1_UDB07_F0: 0x6547

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0							

FIFO 0

Bits	Name	Description
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.706 B[0..3]_UDB08_F0

UDB08_F0

Reset: N/A

Register : Address

B0_UDB08_F0: 0x6448 B1_UDB08_F0: 0x6548

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0							

FIFO 0

Bits	Name	Description
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.707 B[0..3]_UDB09_F0

UDB09_F0

Reset: N/A

Register : Address

B0_UDB09_F0: 0x6449 B1_UDB09_F0: 0x6549

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0							

FIFO 0

Bits	Name	Description
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.708 B[0..3]_UDB10_F0

UDB10_F0

Reset: N/A

Register : Address

B0_UDB10_F0: 0x644A B1_UDB10_F0: 0x654A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0							

FIFO 0

Bits	Name	Description
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.709 B[0..3]_UDB11_F0

UDB11_F0

Reset: N/A

Register : Address

B0_UDB11_F0: 0x644B

B1_UDB11_F0: 0x654B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0							

FIFO 0

Bits	Name	Description
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.710 B[0..3]_UDB12_F0

UDB12_F0

Reset: N/A

Register : Address

B0_UDB12_F0: 0x644C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0							

FIFO 0

Bits	Name	Description
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.711 B[0..3]_UDB13_F0

UDB13_F0

Reset: N/A

Register : Address

B0_UDB13_F0: 0x644D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0							

FIFO 0

Bits	Name	Description
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.712 B[0..3]_UDB14_F0

UDB14_F0

Reset: N/A

Register : Address

B0_UDB14_F0: 0x644E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0							

FIFO 0

Bits	Name	Description
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.713 B[0..3]_UDB15_F0

UDB15_F0

Reset: N/A

Register : Address

B0_UDB15_F0: 0x644F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0							

FIFO 0

Bits	Name	Description
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.714 B[0..3]_UDB00_F1

UDB00_F1

Reset: N/A

Register : Address

B0_UDB00_F1: 0x6450

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1							

FIFO 1

Bits	Name	Description
7:0	F1[7:0]	Generic field for 8 bit working registers

1.3.715 B[0..3]_UDB01_F1

UDB01_F1

Reset: N/A

Register : Address

B0_UDB01_F1: 0x6451

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1							

FIFO 1

Bits	Name	Description
7:0	F1[7:0]	Generic field for 8 bit working registers

1.3.716 B[0..3]_UDB02_F1

UDB02_F1

Reset: N/A

Register : Address

B0_UDB02_F1: 0x6452

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1							

FIFO 1

Bits	Name	Description
7:0	F1[7:0]	Generic field for 8 bit working registers

1.3.717 B[0..3]_UDB03_F1

UDB03_F1

Reset: N/A

Register : Address

B0_UDB03_F1: 0x6453

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1							

FIFO 1

Bits	Name	Description
7:0	F1[7:0]	Generic field for 8 bit working registers

1.3.718 B[0..3]_UDB04_F1

UDB04_F1

Reset: N/A

Register : Address

B0_UDB04_F1: 0x6454 B1_UDB04_F1: 0x6554

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1							

FIFO 1

Bits	Name	Description
7:0	F1[7:0]	Generic field for 8 bit working registers

1.3.719 B[0..3]_UDB05_F1

UDB05_F1

Reset: N/A

Register : Address

B0_UDB05_F1: 0x6455 B1_UDB05_F1: 0x6555

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1							

FIFO 1

Bits	Name	Description
7:0	F1[7:0]	Generic field for 8 bit working registers

1.3.720 B[0..3]_UDB06_F1

UDB06_F1

Reset: N/A

Register : Address

B0_UDB06_F1: 0x6456 B1_UDB06_F1: 0x6556

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1							

FIFO 1

Bits	Name	Description
7:0	F1[7:0]	Generic field for 8 bit working registers

1.3.721 B[0..3]_UDB07_F1

UDB07_F1

Reset: N/A

Register : Address

B0_UDB07_F1: 0x6457 B1_UDB07_F1: 0x6557

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1							

FIFO 1

Bits	Name	Description
7:0	F1[7:0]	Generic field for 8 bit working registers

1.3.722 B[0..3]_UDB08_F1

UDB08_F1

Reset: N/A

Register : Address

B0_UDB08_F1: 0x6458 B1_UDB08_F1: 0x6558

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1							

FIFO 1

Bits	Name	Description
7:0	F1[7:0]	Generic field for 8 bit working registers

1.3.723 B[0..3]_UDB09_F1

UDB09_F1

Reset: N/A

Register : Address

B0_UDB09_F1: 0x6459 B1_UDB09_F1: 0x6559

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1							

FIFO 1

Bits	Name	Description
7:0	F1[7:0]	Generic field for 8 bit working registers

1.3.724 B[0..3]_UDB10_F1

UDB10_F1

Reset: N/A

Register : Address

B0_UDB10_F1: 0x645A B1_UDB10_F1: 0x655A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1							

FIFO 1

Bits	Name	Description
7:0	F1[7:0]	Generic field for 8 bit working registers

1.3.725 B[0..3]_UDB11_F1

UDB11_F1

Reset: N/A

Register : Address

B0_UDB11_F1: 0x645B

B1_UDB11_F1: 0x655B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1							

FIFO 1

Bits	Name	Description
7:0	F1[7:0]	Generic field for 8 bit working registers

1.3.726 B[0..3]_UDB12_F1

UDB12_F1

Reset: N/A

Register : Address

B0_UDB12_F1: 0x645C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1							

FIFO 1

Bits	Name	Description
7:0	F1[7:0]	Generic field for 8 bit working registers

1.3.727 B[0..3]_UDB13_F1

UDB13_F1

Reset: N/A

Register : Address

B0_UDB13_F1: 0x645D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1							

FIFO 1

Bits	Name	Description
7:0	F1[7:0]	Generic field for 8 bit working registers

1.3.728 B[0..3]_UDB14_F1

UDB14_F1

Reset: N/A

Register : Address

B0_UDB14_F1: 0x645E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1							

FIFO 1

Bits	Name	Description
7:0	F1[7:0]	Generic field for 8 bit working registers

1.3.729 B[0..3]_UDB15_F1

UDB15_F1

Reset: N/A

Register : Address

B0_UDB15_F1: 0x645F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1							

FIFO 1

Bits	Name	Description
7:0	F1[7:0]	Generic field for 8 bit working registers

1.3.730 B[0..3]_UDB00_ST

UDB00_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_ST: 0x6460

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST							

Status Register

Bits	Name	Description
7:0	ST[7:0]	Status register

1.3.731 B[0..3]_UDB01_ST

UDB01_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_ST: 0x6461

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST							

Status Register

Bits	Name	Description
7:0	ST[7:0]	Status register

1.3.732 B[0..3]_UDB02_ST

UDB02_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_ST: 0x6462

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST							

Status Register

Bits	Name	Description
7:0	ST[7:0]	Status register

1.3.733 B[0..3]_UDB03_ST

UDB03_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_ST: 0x6463

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST							

Status Register

Bits	Name	Description
7:0	ST[7:0]	Status register

1.3.734 B[0..3]_UDB04_ST

UDB04_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_ST: 0x6464 B1_UDB04_ST: 0x6564

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST							

Status Register

Bits	Name	Description
7:0	ST[7:0]	Status register

1.3.735 B[0..3]_UDB05_ST

UDB05_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_ST: 0x6465 B1_UDB05_ST: 0x6565

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST							

Status Register

Bits	Name	Description
7:0	ST[7:0]	Status register

1.3.736 B[0..3]_UDB06_ST

UDB06_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_ST: 0x6466 B1_UDB06_ST: 0x6566

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST							

Status Register

Bits	Name	Description
7:0	ST[7:0]	Status register

1.3.737 B[0..3]_UDB07_ST

UDB07_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_ST: 0x6467 B1_UDB07_ST: 0x6567

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST							

Status Register

Bits	Name	Description
7:0	ST[7:0]	Status register

1.3.738 B[0..3]_UDB08_ST

UDB08_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_ST: 0x6468 B1_UDB08_ST: 0x6568

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST							

Status Register

Bits	Name	Description
7:0	ST[7:0]	Status register

1.3.739 B[0..3]_UDB09_ST

UDB09_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_ST: 0x6469 B1_UDB09_ST: 0x6569

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST							

Status Register

Bits	Name	Description
7:0	ST[7:0]	Status register

1.3.740 B[0..3]_UDB10_ST

UDB10_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_ST: 0x646A B1_UDB10_ST: 0x656A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST							

Status Register

Bits	Name	Description
7:0	ST[7:0]	Status register

1.3.741 B[0..3]_UDB11_ST

UDB11_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_ST: 0x646B B1_UDB11_ST: 0x656B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST							

Status Register

Bits	Name	Description
7:0	ST[7:0]	Status register

1.3.742 B[0..3]_UDB12_ST

UDB12_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_ST: 0x646C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST							

Status Register

Bits	Name	Description
7:0	ST[7:0]	Status register

1.3.743 B[0..3]_UDB13_ST

UDB13_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_ST: 0x646D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST							

Status Register

Bits	Name	Description
7:0	ST[7:0]	Status register

1.3.744 B[0..3]_UDB14_ST

UDB14_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_ST: 0x646E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST							

Status Register

Bits	Name	Description
7:0	ST[7:0]	Status register

1.3.745 B[0..3]_UDB15_ST

UDB15_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB15_ST: 0x646F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST							

Status Register

Bits	Name	Description
7:0	ST[7:0]	Status register

1.3.746 B[0..3]_UDB00_CTL

UDB00_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_CTL: 0x6470

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL							

Control Register

Bits	Name	Description
7:0	CTL[7:0]	Control register

1.3.747 B[0..3]_UDB01_CTL

UDB01_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_CTL: 0x6471

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL							

Control Register

Bits	Name	Description
7:0	CTL[7:0]	Control register

1.3.748 B[0..3]_UDB02_CTL

UDB02_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_CTL: 0x6472

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL							

Control Register

Bits	Name	Description
7:0	CTL[7:0]	Control register

1.3.749 B[0..3]_UDB03_CTL

UDB03_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_CTL: 0x6473

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL							

Control Register

Bits	Name	Description
7:0	CTL[7:0]	Control register

1.3.750 B[0..3]_UDB04_CTL

UDB04_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_CTL: 0x6474 B1_UDB04_CTL: 0x6574

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL							

Control Register

Bits	Name	Description
7:0	CTL[7:0]	Control register

1.3.751 B[0..3]_UDB05_CTL

UDB05_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_CTL: 0x6475 B1_UDB05_CTL: 0x6575

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL							

Control Register

Bits	Name	Description
7:0	CTL[7:0]	Control register

1.3.752 B[0..3]_UDB06_CTL

UDB06_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_CTL: 0x6476 B1_UDB06_CTL: 0x6576

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL							

Control Register

Bits	Name	Description
7:0	CTL[7:0]	Control register

1.3.753 B[0..3]_UDB07_CTL

UDB07_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_CTL: 0x6477 B1_UDB07_CTL: 0x6577

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL							

Control Register

Bits	Name	Description
7:0	CTL[7:0]	Control register

1.3.754 B[0..3]_UDB08_CTL

UDB08_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_CTL: 0x6478 B1_UDB08_CTL: 0x6578

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL							

Control Register

Bits	Name	Description
7:0	CTL[7:0]	Control register

1.3.755 B[0..3]_UDB09_CTL

UDB09_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_CTL: 0x6479 B1_UDB09_CTL: 0x6579

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL							

Control Register

Bits	Name	Description
7:0	CTL[7:0]	Control register

1.3.756 B[0..3]_UDB10_CTL

UDB10_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_CTL: 0x647A B1_UDB10_CTL: 0x657A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL							

Control Register

Bits	Name	Description
7:0	CTL[7:0]	Control register

1.3.757 B[0..3]_UDB11_CTL

UDB11_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_CTL: 0x647B B1_UDB11_CTL: 0x657B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL							

Control Register

Bits	Name	Description
7:0	CTL[7:0]	Control register

1.3.758 B[0..3]_UDB12_CTL

UDB12_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_CTL: 0x647C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL							

Control Register

Bits	Name	Description
7:0	CTL[7:0]	Control register

1.3.759 B[0..3]_UDB13_CTL

UDB13_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_CTL: 0x647D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL							

Control Register

Bits	Name	Description
7:0	CTL[7:0]	Control register

1.3.760 B[0..3]_UDB14_CTL

UDB14_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_CTL: 0x647E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL							

Control Register

Bits	Name	Description
7:0	CTL[7:0]	Control register

1.3.761 B[0..3]_UDB15_CTL

UDB15_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB15_CTL: 0x647F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL							

Control Register

Bits	Name	Description
7:0	CTL[7:0]	Control register

1.3.762 B[0..3]_UDB00_MSK

UDB00_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB00_MSK: 0x6480

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK						

Interrupt Mask

Bits	Name	Description
6:0	MSK[6:0]	Generic field for 7 bit working registers

1.3.763 B[0..3]_UDB01_MSK

UDB01_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB01_MSK: 0x6481

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK						

Interrupt Mask

Bits	Name	Description
6:0	MSK[6:0]	Generic field for 7 bit working registers

1.3.764 B[0..3]_UDB02_MSK

UDB02_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB02_MSK: 0x6482

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK						

Interrupt Mask

Bits	Name	Description
6:0	MSK[6:0]	Generic field for 7 bit working registers

1.3.765 B[0..3]_UDB03_MSK

UDB03_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB03_MSK: 0x6483

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK						

Interrupt Mask

Bits	Name	Description
6:0	MSK[6:0]	Generic field for 7 bit working registers

1.3.766 B[0..3]_UDB04_MSK

UDB04_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB04_MSK: 0x6484 B1_UDB04_MSK: 0x6584

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK						

Interrupt Mask

Bits	Name	Description
6:0	MSK[6:0]	Generic field for 7 bit working registers

1.3.767 B[0..3]_UDB05_MSK

UDB05_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB05_MSK: 0x6485 B1_UDB05_MSK: 0x6585

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK						

Interrupt Mask

Bits	Name	Description
6:0	MSK[6:0]	Generic field for 7 bit working registers

1.3.768 B[0..3]_UDB06_MSK

UDB06_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB06_MSK: 0x6486 B1_UDB06_MSK: 0x6586

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK						

Interrupt Mask

Bits	Name	Description
6:0	MSK[6:0]	Generic field for 7 bit working registers

1.3.769 B[0..3]_UDB07_MSK

UDB07_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB07_MSK: 0x6487 B1_UDB07_MSK: 0x6587

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK						

Interrupt Mask

Bits	Name	Description
6:0	MSK[6:0]	Generic field for 7 bit working registers

1.3.770 B[0..3]_UDB08_MSK

UDB08_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB08_MSK: 0x6488 B1_UDB08_MSK: 0x6588

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK						

Interrupt Mask

Bits	Name	Description
6:0	MSK[6:0]	Generic field for 7 bit working registers

1.3.771 B[0..3]_UDB09_MSK

UDB09_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB09_MSK: 0x6489 B1_UDB09_MSK: 0x6589

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK						

Interrupt Mask

Bits	Name	Description
6:0	MSK[6:0]	Generic field for 7 bit working registers

1.3.772 B[0..3]_UDB10_MSK

UDB10_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB10_MSK: 0x648A B1_UDB10_MSK: 0x658A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK						

Interrupt Mask

Bits	Name	Description
6:0	MSK[6:0]	Generic field for 7 bit working registers

1.3.773 B[0..3]_UDB11_MSK

UDB11_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB11_MSK: 0x648B B1_UDB11_MSK: 0x658B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK						

Interrupt Mask

Bits	Name	Description
6:0	MSK[6:0]	Generic field for 7 bit working registers

1.3.774 B[0..3]_UDB12_MSK

UDB12_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB12_MSK: 0x648C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK						

Interrupt Mask

Bits	Name	Description
6:0	MSK[6:0]	Generic field for 7 bit working registers

1.3.775 B[0..3]_UDB13_MSK

UDB13_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB13_MSK: 0x648D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK						

Interrupt Mask

Bits	Name	Description
6:0	MSK[6:0]	Generic field for 7 bit working registers

1.3.776 B[0..3]_UDB14_MSK

UDB14_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB14_MSK: 0x648E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK						

Interrupt Mask

Bits	Name	Description
6:0	MSK[6:0]	Generic field for 7 bit working registers

1.3.777 B[0..3]_UDB15_MSK

UDB15_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB15_MSK: 0x648F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK						

Interrupt Mask

Bits	Name	Description
6:0	MSK[6:0]	Generic field for 7 bit working registers

1.3.778 B[0..3]_UDB00_ACTL

UDB00_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB00_ACTL: 0x6490

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Auxiliary Control

Bits	Name	Description
5	CNT_START	FIFO0 clear See Table 1-464.
4	INT_EN	(no description) See Table 1-467.
3	FIFO1_LVL	FIFO level See Table 1-466.
2	FIFO0_LVL	FIFO level See Table 1-466.
1	FIFO1_CLR	FIFO clear See Table 1-465.
0	FIFO0_CLR	FIFO clear See Table 1-465.

Table 1-464. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-465. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-466. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

(continued)

Table 1-467. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.779 B[0..3]_UDB01_ACTL

UDB01_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB01_ACTL: 0x6491

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Auxiliary Control

Bits	Name	Description
5	CNT_START	FIFO0 clear See Table 1-468.
4	INT_EN	(no description) See Table 1-471.
3	FIFO1_LVL	FIFO level See Table 1-470.
2	FIFO0_LVL	FIFO level See Table 1-470.
1	FIFO1_CLR	FIFO clear See Table 1-469.
0	FIFO0_CLR	FIFO clear See Table 1-469.

Table 1-468. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-469. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-470. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

(continued)

Table 1-471. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.780 B[0..3]_UDB02_ACTL

UDB02_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB02_ACTL: 0x6492

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Auxiliary Control

Bits	Name	Description
5	CNT_START	FIFO0 clear See Table 1-472.
4	INT_EN	(no description) See Table 1-475.
3	FIFO1_LVL	FIFO level See Table 1-474.
2	FIFO0_LVL	FIFO level See Table 1-474.
1	FIFO1_CLR	FIFO clear See Table 1-473.
0	FIFO0_CLR	FIFO clear See Table 1-473.

Table 1-472. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-473. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-474. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

(continued)

Table 1-475. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.781 B[0..3]_UDB03_ACTL

UDB03_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB03_ACTL: 0x6493

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Auxiliary Control

Bits	Name	Description
5	CNT_START	FIFO0 clear See Table 1-476.
4	INT_EN	(no description) See Table 1-479.
3	FIFO1_LVL	FIFO level See Table 1-478.
2	FIFO0_LVL	FIFO level See Table 1-478.
1	FIFO1_CLR	FIFO clear See Table 1-477.
0	FIFO0_CLR	FIFO clear See Table 1-477.

Table 1-476. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-477. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-478. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

(continued)

Table 1-479. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.782 B[0..3]_UDB04_ACTL

UDB04_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB04_ACTL: 0x6494 B1_UDB04_ACTL: 0x6594

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Auxiliary Control

Bits	Name	Description
5	CNT_START	FIFO0 clear See Table 1-480.
4	INT_EN	(no description) See Table 1-483.
3	FIFO1_LVL	FIFO level See Table 1-482.
2	FIFO0_LVL	FIFO level See Table 1-482.
1	FIFO1_CLR	FIFO clear See Table 1-481.
0	FIFO0_CLR	FIFO clear See Table 1-481.

Table 1-480. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-481. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-482. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

(continued)

Table 1-483. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.783 B[0..3]_UDB05_ACTL

UDB05_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB05_ACTL: 0x6495 B1_UDB05_ACTL: 0x6595

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Auxiliary Control

Bits	Name	Description
5	CNT_START	FIFO0 clear See Table 1-484.
4	INT_EN	(no description) See Table 1-487.
3	FIFO1_LVL	FIFO level See Table 1-486.
2	FIFO0_LVL	FIFO level See Table 1-486.
1	FIFO1_CLR	FIFO clear See Table 1-485.
0	FIFO0_CLR	FIFO clear See Table 1-485.

Table 1-484. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-485. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-486. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

(continued)

Table 1-487. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.784 B[0..3]_UDB06_ACTL

UDB06_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB06_ACTL: 0x6496 B1_UDB06_ACTL: 0x6596

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Auxiliary Control

Bits	Name	Description
5	CNT_START	FIFO0 clear See Table 1-488.
4	INT_EN	(no description) See Table 1-491.
3	FIFO1_LVL	FIFO level See Table 1-490.
2	FIFO0_LVL	FIFO level See Table 1-490.
1	FIFO1_CLR	FIFO clear See Table 1-489.
0	FIFO0_CLR	FIFO clear See Table 1-489.

Table 1-488. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-489. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-490. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

(continued)

Table 1-491. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.785 B[0..3]_UDB07_ACTL

UDB07_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB07_ACTL: 0x6497 B1_UDB07_ACTL: 0x6597

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Auxiliary Control

Bits	Name	Description
5	CNT_START	FIFO0 clear See Table 1-492.
4	INT_EN	(no description) See Table 1-495.
3	FIFO1_LVL	FIFO level See Table 1-494.
2	FIFO0_LVL	FIFO level See Table 1-494.
1	FIFO1_CLR	FIFO clear See Table 1-493.
0	FIFO0_CLR	FIFO clear See Table 1-493.

Table 1-492. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-493. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-494. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

(continued)

Table 1-495. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.786 B[0..3]_UDB08_ACTL

UDB08_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB08_ACTL: 0x6498 B1_UDB08_ACTL: 0x6598

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Auxiliary Control

Bits	Name	Description
5	CNT_START	FIFO0 clear See Table 1-496.
4	INT_EN	(no description) See Table 1-499.
3	FIFO1_LVL	FIFO level See Table 1-498.
2	FIFO0_LVL	FIFO level See Table 1-498.
1	FIFO1_CLR	FIFO clear See Table 1-497.
0	FIFO0_CLR	FIFO clear See Table 1-497.

Table 1-496. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-497. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-498. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

(continued)

Table 1-499. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.787 B[0..3]_UDB09_ACTL

UDB09_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB09_ACTL: 0x6499 B1_UDB09_ACTL: 0x6599

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Auxiliary Control

Bits	Name	Description
5	CNT_START	FIFO0 clear See Table 1-500.
4	INT_EN	(no description) See Table 1-503.
3	FIFO1_LVL	FIFO level See Table 1-502.
2	FIFO0_LVL	FIFO level See Table 1-502.
1	FIFO1_CLR	FIFO clear See Table 1-501.
0	FIFO0_CLR	FIFO clear See Table 1-501.

Table 1-500. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-501. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-502. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

(continued)

Table 1-503. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.788 B[0..3]_UDB10_ACTL

UDB10_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB10_ACTL: 0x649A B1_UDB10_ACTL: 0x659A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Auxiliary Control

Bits	Name	Description
5	CNT_START	FIFO0 clear See Table 1-504.
4	INT_EN	(no description) See Table 1-507.
3	FIFO1_LVL	FIFO level See Table 1-506.
2	FIFO0_LVL	FIFO level See Table 1-506.
1	FIFO1_CLR	FIFO clear See Table 1-505.
0	FIFO0_CLR	FIFO clear See Table 1-505.

Table 1-504. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-505. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-506. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

(continued)

Table 1-507. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.789 B[0..3]_UDB11_ACTL

UDB11_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB11_ACTL: 0x649B B1_UDB11_ACTL: 0x659B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Auxiliary Control

Bits	Name	Description
5	CNT_START	FIFO0 clear See Table 1-508.
4	INT_EN	(no description) See Table 1-511.
3	FIFO1_LVL	FIFO level See Table 1-510.
2	FIFO0_LVL	FIFO level See Table 1-510.
1	FIFO1_CLR	FIFO clear See Table 1-509.
0	FIFO0_CLR	FIFO clear See Table 1-509.

Table 1-508. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-509. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-510. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

(continued)

Table 1-511. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.790 B[0..3]_UDB12_ACTL

UDB12_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB12_ACTL: 0x649C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Auxiliary Control

Bits	Name	Description
5	CNT_START	FIFO0 clear See Table 1-512.
4	INT_EN	(no description) See Table 1-515.
3	FIFO1_LVL	FIFO level See Table 1-514.
2	FIFO0_LVL	FIFO level See Table 1-514.
1	FIFO1_CLR	FIFO clear See Table 1-513.
0	FIFO0_CLR	FIFO clear See Table 1-513.

Table 1-512. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-513. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-514. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

(continued)

Table 1-515. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.791 B[0..3]_UDB13_ACTL

UDB13_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB13_ACTL: 0x649D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Auxiliary Control

Bits	Name	Description
5	CNT_START	FIFO0 clear See Table 1-516.
4	INT_EN	(no description) See Table 1-519.
3	FIFO1_LVL	FIFO level See Table 1-518.
2	FIFO0_LVL	FIFO level See Table 1-518.
1	FIFO1_CLR	FIFO clear See Table 1-517.
0	FIFO0_CLR	FIFO clear See Table 1-517.

Table 1-516. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-517. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-518. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

(continued)

Table 1-519. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.792 B[0..3]_UDB14_ACTL

UDB14_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB14_ACTL: 0x649E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Auxiliary Control

Bits	Name	Description
5	CNT_START	FIFO0 clear See Table 1-520.
4	INT_EN	(no description) See Table 1-523.
3	FIFO1_LVL	FIFO level See Table 1-522.
2	FIFO0_LVL	FIFO level See Table 1-522.
1	FIFO1_CLR	FIFO clear See Table 1-521.
0	FIFO0_CLR	FIFO clear See Table 1-521.

Table 1-520. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-521. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-522. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

(continued)

Table 1-523. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.793 B[0..3]_UDB15_ACTL

UDB15_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB15_ACTL: 0x649F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Auxiliary Control

Bits	Name	Description
5	CNT_START	FIFO0 clear See Table 1-524.
4	INT_EN	(no description) See Table 1-527.
3	FIFO1_LVL	FIFO level See Table 1-526.
2	FIFO0_LVL	FIFO level See Table 1-526.
1	FIFO1_CLR	FIFO clear See Table 1-525.
0	FIFO0_CLR	FIFO clear See Table 1-525.

Table 1-524. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-525. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-526. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

(continued)

Table 1-527. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.794 B[0..3]_UDB00_MC

UDB00_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_MC: 0x64A0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC				PLD0_MC			

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC[3:0]	Read Macrocell
3:0	PLD0_MC[3:0]	Read Macrocell

1.3.795 B[0..3]_UDB01_MC

UDB01_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_MC: 0x64A1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC				PLD0_MC			

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC[3:0]	Read Macrocell
3:0	PLD0_MC[3:0]	Read Macrocell

1.3.796 B[0..3]_UDB02_MC

UDB02_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_MC: 0x64A2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC				PLD0_MC			

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC[3:0]	Read Macrocell
3:0	PLD0_MC[3:0]	Read Macrocell

1.3.797 B[0..3]_UDB03_MC

UDB03_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_MC: 0x64A3

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC				PLD0_MC			

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC[3:0]	Read Macrocell
3:0	PLD0_MC[3:0]	Read Macrocell

1.3.798 B[0..3]_UDB04_MC

UDB04_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_MC: 0x64A4 B1_UDB04_MC: 0x65A4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC				PLD0_MC			

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC[3:0]	Read Macrocell
3:0	PLD0_MC[3:0]	Read Macrocell

1.3.799 B[0..3]_UDB05_MC

UDB05_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_MC: 0x64A5 B1_UDB05_MC: 0x65A5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC				PLD0_MC			

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC[3:0]	Read Macrocell
3:0	PLD0_MC[3:0]	Read Macrocell

1.3.800 B[0..3]_UDB06_MC

UDB06_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_MC: 0x64A6 B1_UDB06_MC: 0x65A6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC				PLD0_MC			

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC[3:0]	Read Macrocell
3:0	PLD0_MC[3:0]	Read Macrocell

1.3.801 B[0..3]_UDB07_MC

UDB07_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_MC: 0x64A7 B1_UDB07_MC: 0x65A7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC				PLD0_MC			

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC[3:0]	Read Macrocell
3:0	PLD0_MC[3:0]	Read Macrocell

1.3.802 B[0..3]_UDB08_MC

UDB08_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_MC: 0x64A8 B1_UDB08_MC: 0x65A8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC				PLD0_MC			

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC[3:0]	Read Macrocell
3:0	PLD0_MC[3:0]	Read Macrocell

1.3.803 B[0..3]_UDB09_MC

UDB09_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_MC: 0x64A9 B1_UDB09_MC: 0x65A9

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC				PLD0_MC			

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC[3:0]	Read Macrocell
3:0	PLD0_MC[3:0]	Read Macrocell

1.3.804 B[0..3]_UDB10_MC

UDB10_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_MC: 0x64AA B1_UDB10_MC: 0x65AA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC				PLD0_MC			

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC[3:0]	Read Macrocell
3:0	PLD0_MC[3:0]	Read Macrocell

1.3.805 B[0..3]_UDB11_MC

UDB11_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_MC: 0x64AB B1_UDB11_MC: 0x65AB

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC				PLD0_MC			

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC[3:0]	Read Macrocell
3:0	PLD0_MC[3:0]	Read Macrocell

1.3.806 B[0..3]_UDB12_MC

UDB12_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_MC: 0x64AC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC				PLD0_MC			

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC[3:0]	Read Macrocell
3:0	PLD0_MC[3:0]	Read Macrocell

1.3.807 B[0..3]_UDB13_MC

UDB13_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_MC: 0x64AD

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC				PLD0_MC			

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC[3:0]	Read Macrocell
3:0	PLD0_MC[3:0]	Read Macrocell

1.3.808 B[0..3]_UDB14_MC

UDB14_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_MC: 0x64AE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC				PLD0_MC			

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC[3:0]	Read Macrocell
3:0	PLD0_MC[3:0]	Read Macrocell

1.3.809 B[0..3]_UDB15_MC

UDB15_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB15_MC: 0x64AF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC				PLD0_MC			

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC[3:0]	Read Macrocell
3:0	PLD0_MC[3:0]	Read Macrocell

1.3.810 B[0..3]_UDB00_01_A0

UDB00_01_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_01_A0: 0x6800

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0_MS							

Accumulator 0

Bits	Name	Description
15:8	A0_MS[7:0]	Generic field for 8 bit working registers
7:0	A0_LS[7:0]	Generic field for 8 bit working registers

1.3.811 B[0..3]_UDB01_02_A0

UDB01_02_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_02_A0: 0x6802

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0_MS							

Accumulator 0

Bits	Name	Description
15:8	A0_MS[7:0]	Generic field for 8 bit working registers
7:0	A0_LS[7:0]	Generic field for 8 bit working registers

1.3.812 B[0..3]_UDB02_03_A0

UDB02_03_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_03_A0: 0x6804

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0_MS							

Accumulator 0

Bits	Name	Description
15:8	A0_MS[7:0]	Generic field for 8 bit working registers
7:0	A0_LS[7:0]	Generic field for 8 bit working registers

1.3.813 B[0..3]_UDB03_04_A0

UDB03_04_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_04_A0: 0x6806

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0_MS							

Accumulator 0

Bits	Name	Description
15:8	A0_MS[7:0]	Generic field for 8 bit working registers
7:0	A0_LS[7:0]	Generic field for 8 bit working registers

1.3.814 B[0..3]_UDB04_05_A0

UDB04_05_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_05_A0: 0x6808 B1_UDB04_05_A0: 0x6A08

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0_MS							

Accumulator 0

Bits	Name	Description
15:8	A0_MS[7:0]	Generic field for 8 bit working registers
7:0	A0_LS[7:0]	Generic field for 8 bit working registers

1.3.815 B[0..3]_UDB05_06_A0

UDB05_06_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_06_A0: 0x680A B1_UDB05_06_A0: 0x6A0A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0_MS							

Accumulator 0

Bits	Name	Description
15:8	A0_MS[7:0]	Generic field for 8 bit working registers
7:0	A0_LS[7:0]	Generic field for 8 bit working registers

1.3.816 B[0..3]_UDB06_07_A0

UDB06_07_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_07_A0: 0x680C B1_UDB06_07_A0: 0x6A0C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0_MS							

Accumulator 0

Bits	Name	Description
15:8	A0_MS[7:0]	Generic field for 8 bit working registers
7:0	A0_LS[7:0]	Generic field for 8 bit working registers

1.3.817 B[0..3]_UDB07_08_A0

UDB07_08_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_08_A0: 0x680E B1_UDB07_08_A0: 0x6A0E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0_MS							

Accumulator 0

Bits	Name	Description
15:8	A0_MS[7:0]	Generic field for 8 bit working registers
7:0	A0_LS[7:0]	Generic field for 8 bit working registers

1.3.818 B[0..3]_UDB08_09_A0

UDB08_09_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_09_A0: 0x6810 B1_UDB08_09_A0: 0x6A10

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0_MS							

Accumulator 0

Bits	Name	Description
15:8	A0_MS[7:0]	Generic field for 8 bit working registers
7:0	A0_LS[7:0]	Generic field for 8 bit working registers

1.3.819 B[0..3]_UDB09_10_A0

UDB09_10_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_10_A0: 0x6812 B1_UDB09_10_A0: 0x6A12

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0_MS							

Accumulator 0

Bits	Name	Description
15:8	A0_MS[7:0]	Generic field for 8 bit working registers
7:0	A0_LS[7:0]	Generic field for 8 bit working registers

1.3.820 B[0..3]_UDB10_11_A0

UDB10_11_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_11_A0: 0x6814 B1_UDB10_11_A0: 0x6A14

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0_MS							

Accumulator 0

Bits	Name	Description
15:8	A0_MS[7:0]	Generic field for 8 bit working registers
7:0	A0_LS[7:0]	Generic field for 8 bit working registers

1.3.821 B[0..3]_UDB11_12_A0

UDB11_12_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_12_A0: 0x6816 B1_UDB11_12_A0: 0x6A16

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0_MS							

Accumulator 0

Bits	Name	Description
15:8	A0_MS[7:0]	Generic field for 8 bit working registers
7:0	A0_LS[7:0]	Generic field for 8 bit working registers

1.3.822 B[0..3]_UDB12_13_A0

UDB12_13_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_13_A0: 0x6818

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0_MS							

Accumulator 0

Bits	Name	Description
15:8	A0_MS[7:0]	Generic field for 8 bit working registers
7:0	A0_LS[7:0]	Generic field for 8 bit working registers

1.3.823 B[0..3]_UDB13_14_A0

UDB13_14_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_14_A0: 0x681A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0_MS							

Accumulator 0

Bits	Name	Description
15:8	A0_MS[7:0]	Generic field for 8 bit working registers
7:0	A0_LS[7:0]	Generic field for 8 bit working registers

1.3.824 B[0..3]_UDB14_15_A0

UDB14_15_A0

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_15_A0: 0x681C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0_MS							

Accumulator 0

Bits	Name	Description
15:8	A0_MS[7:0]	Generic field for 8 bit working registers
7:0	A0_LS[7:0]	Generic field for 8 bit working registers

1.3.825 B[0..3]_UDB00_01_A1

UDB00_01_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_01_A1: 0x6820

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1_MS							

Accumulator 1

Bits	Name	Description
15:8	A1_MS[7:0]	Generic field for 8 bit working registers
7:0	A1_LS[7:0]	Generic field for 8 bit working registers

1.3.826 B[0..3]_UDB01_02_A1

UDB01_02_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_02_A1: 0x6822

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1_MS							

Accumulator 1

Bits	Name	Description
15:8	A1_MS[7:0]	Generic field for 8 bit working registers
7:0	A1_LS[7:0]	Generic field for 8 bit working registers

1.3.827 B[0..3]_UDB02_03_A1

UDB02_03_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_03_A1: 0x6824

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1_MS							

Accumulator 1

Bits	Name	Description
15:8	A1_MS[7:0]	Generic field for 8 bit working registers
7:0	A1_LS[7:0]	Generic field for 8 bit working registers

1.3.828 B[0..3]_UDB03_04_A1

UDB03_04_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_04_A1: 0x6826

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1_MS							

Accumulator 1

Bits	Name	Description
15:8	A1_MS[7:0]	Generic field for 8 bit working registers
7:0	A1_LS[7:0]	Generic field for 8 bit working registers

1.3.829 B[0..3]_UDB04_05_A1

UDB04_05_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_05_A1: 0x6828 B1_UDB04_05_A1: 0x6A28

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1_MS							

Accumulator 1

Bits	Name	Description
15:8	A1_MS[7:0]	Generic field for 8 bit working registers
7:0	A1_LS[7:0]	Generic field for 8 bit working registers

1.3.830 B[0..3]_UDB05_06_A1

UDB05_06_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_06_A1: 0x682A B1_UDB05_06_A1: 0x6A2A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1_MS							

Accumulator 1

Bits	Name	Description
15:8	A1_MS[7:0]	Generic field for 8 bit working registers
7:0	A1_LS[7:0]	Generic field for 8 bit working registers

1.3.831 B[0..3]_UDB06_07_A1

UDB06_07_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_07_A1: 0x682C B1_UDB06_07_A1: 0x6A2C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1_MS							

Accumulator 1

Bits	Name	Description
15:8	A1_MS[7:0]	Generic field for 8 bit working registers
7:0	A1_LS[7:0]	Generic field for 8 bit working registers

1.3.832 B[0..3]_UDB07_08_A1

UDB07_08_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_08_A1: 0x682E B1_UDB07_08_A1: 0x6A2E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1_MS							

Accumulator 1

Bits	Name	Description
15:8	A1_MS[7:0]	Generic field for 8 bit working registers
7:0	A1_LS[7:0]	Generic field for 8 bit working registers

1.3.833 B[0..3]_UDB08_09_A1

UDB08_09_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_09_A1: 0x6830 B1_UDB08_09_A1: 0x6A30

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1_MS							

Accumulator 1

Bits	Name	Description
15:8	A1_MS[7:0]	Generic field for 8 bit working registers
7:0	A1_LS[7:0]	Generic field for 8 bit working registers

1.3.834 B[0..3]_UDB09_10_A1

UDB09_10_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_10_A1: 0x6832 B1_UDB09_10_A1: 0x6A32

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1_MS							

Accumulator 1

Bits	Name	Description
15:8	A1_MS[7:0]	Generic field for 8 bit working registers
7:0	A1_LS[7:0]	Generic field for 8 bit working registers

1.3.835 B[0..3]_UDB10_11_A1

UDB10_11_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_11_A1: 0x6834 B1_UDB10_11_A1: 0x6A34

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1_MS							

Accumulator 1

Bits	Name	Description
15:8	A1_MS[7:0]	Generic field for 8 bit working registers
7:0	A1_LS[7:0]	Generic field for 8 bit working registers

1.3.836 B[0..3]_UDB11_12_A1

UDB11_12_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_12_A1: 0x6836 B1_UDB11_12_A1: 0x6A36

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1_MS							

Accumulator 1

Bits	Name	Description
15:8	A1_MS[7:0]	Generic field for 8 bit working registers
7:0	A1_LS[7:0]	Generic field for 8 bit working registers

1.3.837 B[0..3]_UDB12_13_A1

UDB12_13_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_13_A1: 0x6838

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1_MS							

Accumulator 1

Bits	Name	Description
15:8	A1_MS[7:0]	Generic field for 8 bit working registers
7:0	A1_LS[7:0]	Generic field for 8 bit working registers

1.3.838 B[0..3]_UDB13_14_A1

UDB13_14_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_14_A1: 0x683A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1_MS							

Accumulator 1

Bits	Name	Description
15:8	A1_MS[7:0]	Generic field for 8 bit working registers
7:0	A1_LS[7:0]	Generic field for 8 bit working registers

1.3.839 B[0..3]_UDB14_15_A1

UDB14_15_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_15_A1: 0x683C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1_MS							

Accumulator 1

Bits	Name	Description
15:8	A1_MS[7:0]	Generic field for 8 bit working registers
7:0	A1_LS[7:0]	Generic field for 8 bit working registers

1.3.840 B[0..3]_UDB00_01_D0

UDB00_01_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB00_01_D0: 0x6840

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0_MS							

Data 0

Bits	Name	Description
15:8	D0_MS[7:0]	Generic field for 8 bit working registers
7:0	D0_LS[7:0]	Generic field for 8 bit working registers

1.3.841 B[0..3]_UDB01_02_D0

UDB01_02_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB01_02_D0: 0x6842

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0_MS							

Data 0

Bits	Name	Description
15:8	D0_MS[7:0]	Generic field for 8 bit working registers
7:0	D0_LS[7:0]	Generic field for 8 bit working registers

1.3.842 B[0..3]_UDB02_03_D0

UDB02_03_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB02_03_D0: 0x6844

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0_MS							

Data 0

Bits	Name	Description
15:8	D0_MS[7:0]	Generic field for 8 bit working registers
7:0	D0_LS[7:0]	Generic field for 8 bit working registers

1.3.843 B[0..3]_UDB03_04_D0

UDB03_04_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB03_04_D0: 0x6846

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0_MS							

Data 0

Bits	Name	Description
15:8	D0_MS[7:0]	Generic field for 8 bit working registers
7:0	D0_LS[7:0]	Generic field for 8 bit working registers

1.3.844 B[0..3]_UDB04_05_D0

UDB04_05_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB04_05_D0: 0x6848 B1_UDB04_05_D0: 0x6A48

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0_MS							

Data 0

Bits	Name	Description
15:8	D0_MS[7:0]	Generic field for 8 bit working registers
7:0	D0_LS[7:0]	Generic field for 8 bit working registers

1.3.845 B[0..3]_UDB05_06_D0

UDB05_06_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB05_06_D0: 0x684A

B1_UDB05_06_D0: 0x6A4A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0_MS							

Data 0

Bits	Name	Description
15:8	D0_MS[7:0]	Generic field for 8 bit working registers
7:0	D0_LS[7:0]	Generic field for 8 bit working registers

1.3.846 B[0..3]_UDB06_07_D0

UDB06_07_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB06_07_D0: 0x684C B1_UDB06_07_D0: 0x6A4C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0_MS							

Data 0

Bits	Name	Description
15:8	D0_MS[7:0]	Generic field for 8 bit working registers
7:0	D0_LS[7:0]	Generic field for 8 bit working registers

1.3.847 B[0..3]_UDB07_08_D0

UDB07_08_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB07_08_D0: 0x684E

B1_UDB07_08_D0: 0x6A4E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0_MS							

Data 0

Bits	Name	Description
15:8	D0_MS[7:0]	Generic field for 8 bit working registers
7:0	D0_LS[7:0]	Generic field for 8 bit working registers

1.3.848 B[0..3]_UDB08_09_D0

UDB08_09_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB08_09_D0: 0x6850 B1_UDB08_09_D0: 0x6A50

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0_MS							

Data 0

Bits	Name	Description
15:8	D0_MS[7:0]	Generic field for 8 bit working registers
7:0	D0_LS[7:0]	Generic field for 8 bit working registers

1.3.849 B[0..3]_UDB09_10_D0

UDB09_10_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB09_10_D0: 0x6852 B1_UDB09_10_D0: 0x6A52

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0_MS							

Data 0

Bits	Name	Description
15:8	D0_MS[7:0]	Generic field for 8 bit working registers
7:0	D0_LS[7:0]	Generic field for 8 bit working registers

1.3.850 B[0..3]_UDB10_11_D0

UDB10_11_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB10_11_D0: 0x6854 B1_UDB10_11_D0: 0x6A54

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0_MS							

Data 0

Bits	Name	Description
15:8	D0_MS[7:0]	Generic field for 8 bit working registers
7:0	D0_LS[7:0]	Generic field for 8 bit working registers

1.3.851 B[0..3]_UDB11_12_D0

UDB11_12_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB11_12_D0: 0x6856 B1_UDB11_12_D0: 0x6A56

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0_MS							

Data 0

Bits	Name	Description
15:8	D0_MS[7:0]	Generic field for 8 bit working registers
7:0	D0_LS[7:0]	Generic field for 8 bit working registers

1.3.852 B[0..3]_UDB12_13_D0

UDB12_13_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB12_13_D0: 0x6858

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0_MS							

Data 0

Bits	Name	Description
15:8	D0_MS[7:0]	Generic field for 8 bit working registers
7:0	D0_LS[7:0]	Generic field for 8 bit working registers

1.3.853 B[0..3]_UDB13_14_D0

UDB13_14_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB13_14_D0: 0x685A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0_MS							

Data 0

Bits	Name	Description
15:8	D0_MS[7:0]	Generic field for 8 bit working registers
7:0	D0_LS[7:0]	Generic field for 8 bit working registers

1.3.854 B[0..3]_UDB14_15_D0

UDB14_15_D0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB14_15_D0: 0x685C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0_MS							

Data 0

Bits	Name	Description
15:8	D0_MS[7:0]	Generic field for 8 bit working registers
7:0	D0_LS[7:0]	Generic field for 8 bit working registers

1.3.855 B[0..3]_UDB00_01_D1

UDB00_01_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB00_01_D1: 0x6860

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1_MS							

Data 1

Bits	Name	Description
15:8	D1_MS[7:0]	Generic field for 8 bit working registers
7:0	D1_LS[7:0]	Generic field for 8 bit working registers

1.3.856 B[0..3]_UDB01_02_D1

UDB01_02_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB01_02_D1: 0x6862

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1_MS							

Data 1

Bits	Name	Description
15:8	D1_MS[7:0]	Generic field for 8 bit working registers
7:0	D1_LS[7:0]	Generic field for 8 bit working registers

1.3.857 B[0..3]_UDB02_03_D1

UDB02_03_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB02_03_D1: 0x6864

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1_MS							

Data 1

Bits	Name	Description
15:8	D1_MS[7:0]	Generic field for 8 bit working registers
7:0	D1_LS[7:0]	Generic field for 8 bit working registers

1.3.858 B[0..3]_UDB03_04_D1

UDB03_04_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB03_04_D1: 0x6866

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1_MS							

Data 1

Bits	Name	Description
15:8	D1_MS[7:0]	Generic field for 8 bit working registers
7:0	D1_LS[7:0]	Generic field for 8 bit working registers

1.3.859 B[0..3]_UDB04_05_D1

UDB04_05_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB04_05_D1: 0x6868 B1_UDB04_05_D1: 0x6A68

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1_MS							

Data 1

Bits	Name	Description
15:8	D1_MS[7:0]	Generic field for 8 bit working registers
7:0	D1_LS[7:0]	Generic field for 8 bit working registers

1.3.860 B[0..3]_UDB05_06_D1

UDB05_06_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB05_06_D1: 0x686A B1_UDB05_06_D1: 0x6A6A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1_MS							

Data 1

Bits	Name	Description
15:8	D1_MS[7:0]	Generic field for 8 bit working registers
7:0	D1_LS[7:0]	Generic field for 8 bit working registers

1.3.861 B[0..3]_UDB06_07_D1

UDB06_07_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB06_07_D1: 0x686C

B1_UDB06_07_D1: 0x6A6C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1_MS							

Data 1

Bits	Name	Description
15:8	D1_MS[7:0]	Generic field for 8 bit working registers
7:0	D1_LS[7:0]	Generic field for 8 bit working registers

1.3.862 B[0..3]_UDB07_08_D1

UDB07_08_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB07_08_D1: 0x686E B1_UDB07_08_D1: 0x6A6E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1_MS							

Data 1

Bits	Name	Description
15:8	D1_MS[7:0]	Generic field for 8 bit working registers
7:0	D1_LS[7:0]	Generic field for 8 bit working registers

1.3.863 B[0..3]_UDB08_09_D1

UDB08_09_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB08_09_D1: 0x6870 B1_UDB08_09_D1: 0x6A70

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1_MS							

Data 1

Bits	Name	Description
15:8	D1_MS[7:0]	Generic field for 8 bit working registers
7:0	D1_LS[7:0]	Generic field for 8 bit working registers

1.3.864 B[0..3]_UDB09_10_D1

UDB09_10_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB09_10_D1: 0x6872 B1_UDB09_10_D1: 0x6A72

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1_MS							

Data 1

Bits	Name	Description
15:8	D1_MS[7:0]	Generic field for 8 bit working registers
7:0	D1_LS[7:0]	Generic field for 8 bit working registers

1.3.865 B[0..3]_UDB10_11_D1

UDB10_11_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB10_11_D1: 0x6874 B1_UDB10_11_D1: 0x6A74

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1_MS							

Data 1

Bits	Name	Description
15:8	D1_MS[7:0]	Generic field for 8 bit working registers
7:0	D1_LS[7:0]	Generic field for 8 bit working registers

1.3.866 B[0..3]_UDB11_12_D1

UDB11_12_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB11_12_D1: 0x6876 B1_UDB11_12_D1: 0x6A76

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1_MS							

Data 1

Bits	Name	Description
15:8	D1_MS[7:0]	Generic field for 8 bit working registers
7:0	D1_LS[7:0]	Generic field for 8 bit working registers

1.3.867 B[0..3]_UDB12_13_D1

UDB12_13_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB12_13_D1: 0x6878

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1_MS							

Data 1

Bits	Name	Description
15:8	D1_MS[7:0]	Generic field for 8 bit working registers
7:0	D1_LS[7:0]	Generic field for 8 bit working registers

1.3.868 B[0..3]_UDB13_14_D1

UDB13_14_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB13_14_D1: 0x687A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1_MS							

Data 1

Bits	Name	Description
15:8	D1_MS[7:0]	Generic field for 8 bit working registers
7:0	D1_LS[7:0]	Generic field for 8 bit working registers

1.3.869 B[0..3]_UDB14_15_D1

UDB14_15_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB14_15_D1: 0x687C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1_MS							

Data 1

Bits	Name	Description
15:8	D1_MS[7:0]	Generic field for 8 bit working registers
7:0	D1_LS[7:0]	Generic field for 8 bit working registers

1.3.870 B[0..3]_UDB00_01_F0

UDB00_01_F0

Reset: N/A

Register : Address

B0_UDB00_01_F0: 0x6880

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0_MS							

FIFO 0

Bits	Name	Description
15:8	F0_MS[7:0]	Generic field for 8 bit working registers
7:0	F0_LS[7:0]	Generic field for 8 bit working registers

1.3.871 B[0..3]_UDB01_02_F0

UDB01_02_F0

Reset: N/A

Register : Address

B0_UDB01_02_F0: 0x6882

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0_MS							

FIFO 0

Bits	Name	Description
15:8	F0_MS[7:0]	Generic field for 8 bit working registers
7:0	F0_LS[7:0]	Generic field for 8 bit working registers

1.3.872 B[0..3]_UDB02_03_F0

UDB02_03_F0

Reset: N/A

Register : Address

B0_UDB02_03_F0: 0x6884

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0_MS							

FIFO 0

Bits	Name	Description
15:8	F0_MS[7:0]	Generic field for 8 bit working registers
7:0	F0_LS[7:0]	Generic field for 8 bit working registers

1.3.873 B[0..3]_UDB03_04_F0

UDB03_04_F0

Reset: N/A

Register : Address

B0_UDB03_04_F0: 0x6886

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0_MS							

FIFO 0

Bits	Name	Description
15:8	F0_MS[7:0]	Generic field for 8 bit working registers
7:0	F0_LS[7:0]	Generic field for 8 bit working registers

1.3.874 B[0..3]_UDB04_05_F0

UDB04_05_F0

Reset: N/A

Register : Address

B0_UDB04_05_F0: 0x6888 B1_UDB04_05_F0: 0x6A88

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0_MS							

FIFO 0

Bits	Name	Description
15:8	F0_MS[7:0]	Generic field for 8 bit working registers
7:0	F0_LS[7:0]	Generic field for 8 bit working registers

1.3.875 B[0..3]_UDB05_06_F0

UDB05_06_F0

Reset: N/A

Register : Address

B0_UDB05_06_F0: 0x688A

B1_UDB05_06_F0: 0x6A8A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0_MS							

FIFO 0

Bits	Name	Description
15:8	F0_MS[7:0]	Generic field for 8 bit working registers
7:0	F0_LS[7:0]	Generic field for 8 bit working registers

1.3.876 B[0..3]_UDB06_07_F0

UDB06_07_F0

Reset: N/A

Register : Address

B0_UDB06_07_F0: 0x688C

B1_UDB06_07_F0: 0x6A8C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0_MS							

FIFO 0

Bits	Name	Description
15:8	F0_MS[7:0]	Generic field for 8 bit working registers
7:0	F0_LS[7:0]	Generic field for 8 bit working registers

1.3.877 B[0..3]_UDB07_08_F0

UDB07_08_F0

Reset: N/A

Register : Address

B0_UDB07_08_F0: 0x688E

B1_UDB07_08_F0: 0x6A8E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0_MS							

FIFO 0

Bits	Name	Description
15:8	F0_MS[7:0]	Generic field for 8 bit working registers
7:0	F0_LS[7:0]	Generic field for 8 bit working registers

1.3.878 B[0..3]_UDB08_09_F0

UDB08_09_F0

Reset: N/A

Register : Address

B0_UDB08_09_F0: 0x6890 B1_UDB08_09_F0: 0x6A90

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0_MS							

FIFO 0

Bits	Name	Description
15:8	F0_MS[7:0]	Generic field for 8 bit working registers
7:0	F0_LS[7:0]	Generic field for 8 bit working registers

1.3.879 B[0..3]_UDB09_10_F0

UDB09_10_F0

Reset: N/A

Register : Address

B0_UDB09_10_F0: 0x6892 B1_UDB09_10_F0: 0x6A92

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0_MS							

FIFO 0

Bits	Name	Description
15:8	F0_MS[7:0]	Generic field for 8 bit working registers
7:0	F0_LS[7:0]	Generic field for 8 bit working registers

1.3.880 B[0..3]_UDB10_11_F0

UDB10_11_F0

Reset: N/A

Register : Address

B0_UDB10_11_F0: 0x6894 B1_UDB10_11_F0: 0x6A94

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0_MS							

FIFO 0

Bits	Name	Description
15:8	F0_MS[7:0]	Generic field for 8 bit working registers
7:0	F0_LS[7:0]	Generic field for 8 bit working registers

1.3.881 B[0..3]_UDB11_12_F0

UDB11_12_F0

Reset: N/A

Register : Address

B0_UDB11_12_F0: 0x6896 B1_UDB11_12_F0: 0x6A96

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0_MS							

FIFO 0

Bits	Name	Description
15:8	F0_MS[7:0]	Generic field for 8 bit working registers
7:0	F0_LS[7:0]	Generic field for 8 bit working registers

1.3.882 B[0..3]_UDB12_13_F0

UDB12_13_F0

Reset: N/A

Register : Address

B0_UDB12_13_F0: 0x6898

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0_MS							

FIFO 0

Bits	Name	Description
15:8	F0_MS[7:0]	Generic field for 8 bit working registers
7:0	F0_LS[7:0]	Generic field for 8 bit working registers

1.3.883 B[0..3]_UDB13_14_F0

UDB13_14_F0

Reset: N/A

Register : Address

B0_UDB13_14_F0: 0x689A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0_MS							

FIFO 0

Bits	Name	Description
15:8	F0_MS[7:0]	Generic field for 8 bit working registers
7:0	F0_LS[7:0]	Generic field for 8 bit working registers

1.3.884 B[0..3]_UDB14_15_F0

UDB14_15_F0

Reset: N/A

Register : Address

B0_UDB14_15_F0: 0x689C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0_MS							

FIFO 0

Bits	Name	Description
15:8	F0_MS[7:0]	Generic field for 8 bit working registers
7:0	F0_LS[7:0]	Generic field for 8 bit working registers

1.3.885 B[0..3]_UDB00_01_F1

UDB00_01_F1

Reset: N/A

Register : Address

B0_UDB00_01_F1: 0x68A0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1_MS							

FIFO 1

Bits	Name	Description
15:8	F1_MS[7:0]	Generic field for 8 bit working registers
7:0	F1_LS[7:0]	Generic field for 8 bit working registers

1.3.886 B[0..3]_UDB01_02_F1

UDB01_02_F1

Reset: N/A

Register : Address

B0_UDB01_02_F1: 0x68A2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1_MS							

FIFO 1

Bits	Name	Description
15:8	F1_MS[7:0]	Generic field for 8 bit working registers
7:0	F1_LS[7:0]	Generic field for 8 bit working registers

1.3.887 B[0..3]_UDB02_03_F1

UDB02_03_F1

Reset: N/A

Register : Address

B0_UDB02_03_F1: 0x68A4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1_MS							

FIFO 1

Bits	Name	Description
15:8	F1_MS[7:0]	Generic field for 8 bit working registers
7:0	F1_LS[7:0]	Generic field for 8 bit working registers

1.3.888 B[0..3]_UDB03_04_F1

UDB03_04_F1

Reset: N/A

Register : Address

B0_UDB03_04_F1: 0x68A6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1_MS							

FIFO 1

Bits	Name	Description
15:8	F1_MS[7:0]	Generic field for 8 bit working registers
7:0	F1_LS[7:0]	Generic field for 8 bit working registers

1.3.889 B[0..3]_UDB04_05_F1

UDB04_05_F1

Reset: N/A

Register : Address

B0_UDB04_05_F1: 0x68A8 B1_UDB04_05_F1: 0x6AA8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1_MS							

FIFO 1

Bits	Name	Description
15:8	F1_MS[7:0]	Generic field for 8 bit working registers
7:0	F1_LS[7:0]	Generic field for 8 bit working registers

1.3.890 B[0..3]_UDB05_06_F1

UDB05_06_F1

Reset: N/A

Register : Address

B0_UDB05_06_F1: 0x68AA

B1_UDB05_06_F1: 0x6AAA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1_MS							

FIFO 1

Bits	Name	Description
15:8	F1_MS[7:0]	Generic field for 8 bit working registers
7:0	F1_LS[7:0]	Generic field for 8 bit working registers

1.3.891 B[0..3]_UDB06_07_F1

UDB06_07_F1

Reset: N/A

Register : Address

B0_UDB06_07_F1: 0x68AC

B1_UDB06_07_F1: 0x6AAC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1_MS							

FIFO 1

Bits	Name	Description
15:8	F1_MS[7:0]	Generic field for 8 bit working registers
7:0	F1_LS[7:0]	Generic field for 8 bit working registers

1.3.892 B[0..3]_UDB07_08_F1

UDB07_08_F1

Reset: N/A

Register : Address

B0_UDB07_08_F1: 0x68AE

B1_UDB07_08_F1: 0x6AAE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1_MS							

FIFO 1

Bits	Name	Description
15:8	F1_MS[7:0]	Generic field for 8 bit working registers
7:0	F1_LS[7:0]	Generic field for 8 bit working registers

1.3.893 B[0..3]_UDB08_09_F1

UDB08_09_F1

Reset: N/A

Register : Address

B0_UDB08_09_F1: 0x68B0 B1_UDB08_09_F1: 0x6AB0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1_MS							

FIFO 1

Bits	Name	Description
15:8	F1_MS[7:0]	Generic field for 8 bit working registers
7:0	F1_LS[7:0]	Generic field for 8 bit working registers

1.3.894 B[0..3]_UDB09_10_F1

UDB09_10_F1

Reset: N/A

Register : Address

B0_UDB09_10_F1: 0x68B2 B1_UDB09_10_F1: 0x6AB2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1_MS							

FIFO 1

Bits	Name	Description
15:8	F1_MS[7:0]	Generic field for 8 bit working registers
7:0	F1_LS[7:0]	Generic field for 8 bit working registers

1.3.895 B[0..3]_UDB10_11_F1

UDB10_11_F1

Reset: N/A

Register : Address

B0_UDB10_11_F1: 0x68B4 B1_UDB10_11_F1: 0x6AB4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1_MS							

FIFO 1

Bits	Name	Description
15:8	F1_MS[7:0]	Generic field for 8 bit working registers
7:0	F1_LS[7:0]	Generic field for 8 bit working registers

1.3.896 B[0..3]_UDB11_12_F1

UDB11_12_F1

Reset: N/A

Register : Address

B0_UDB11_12_F1: 0x68B6 B1_UDB11_12_F1: 0x6AB6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1_MS							

FIFO 1

Bits	Name	Description
15:8	F1_MS[7:0]	Generic field for 8 bit working registers
7:0	F1_LS[7:0]	Generic field for 8 bit working registers

1.3.897 B[0..3]_UDB12_13_F1

UDB12_13_F1

Reset: N/A

Register : Address

B0_UDB12_13_F1: 0x68B8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1_MS							

FIFO 1

Bits	Name	Description
15:8	F1_MS[7:0]	Generic field for 8 bit working registers
7:0	F1_LS[7:0]	Generic field for 8 bit working registers

1.3.898 B[0..3]_UDB13_14_F1

UDB13_14_F1

Reset: N/A

Register : Address

B0_UDB13_14_F1: 0x68BA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1_MS							

FIFO 1

Bits	Name	Description
15:8	F1_MS[7:0]	Generic field for 8 bit working registers
7:0	F1_LS[7:0]	Generic field for 8 bit working registers

1.3.899 B[0..3]_UDB14_15_F1

UDB14_15_F1

Reset: N/A

Register : Address

B0_UDB14_15_F1: 0x68BC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1_MS							

FIFO 1

Bits	Name	Description
15:8	F1_MS[7:0]	Generic field for 8 bit working registers
7:0	F1_LS[7:0]	Generic field for 8 bit working registers

1.3.900 B[0..3]_UDB00_01_ST

UDB00_01_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_01_ST: 0x68C0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST_MS							

Status Register

Bits	Name	Description
15:8	ST_MS[7:0]	Status register
7:0	ST_LS[7:0]	Status register

1.3.901 B[0..3]_UDB01_02_ST

UDB01_02_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_02_ST: 0x68C2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST_MS							

Status Register

Bits	Name	Description
15:8	ST_MS[7:0]	Status register
7:0	ST_LS[7:0]	Status register

1.3.902 B[0..3]_UDB02_03_ST

UDB02_03_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_03_ST: 0x68C4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST_MS							

Status Register

Bits	Name	Description
15:8	ST_MS[7:0]	Status register
7:0	ST_LS[7:0]	Status register

1.3.903 B[0..3]_UDB03_04_ST

UDB03_04_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_04_ST: 0x68C6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST_MS							

Status Register

Bits	Name	Description
15:8	ST_MS[7:0]	Status register
7:0	ST_LS[7:0]	Status register

1.3.904 B[0..3]_UDB04_05_ST

UDB04_05_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_05_ST: 0x68C8 B1_UDB04_05_ST: 0x6AC8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST_MS							

Status Register

Bits	Name	Description
15:8	ST_MS[7:0]	Status register
7:0	ST_LS[7:0]	Status register

1.3.905 B[0..3]_UDB05_06_ST

UDB05_06_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_06_ST: 0x68CA B1_UDB05_06_ST: 0x6ACA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST_MS							

Status Register

Bits	Name	Description
15:8	ST_MS[7:0]	Status register
7:0	ST_LS[7:0]	Status register

1.3.906 B[0..3]_UDB06_07_ST

UDB06_07_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_07_ST: 0x68CC B1_UDB06_07_ST: 0x6ACC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST_MS							

Status Register

Bits	Name	Description
15:8	ST_MS[7:0]	Status register
7:0	ST_LS[7:0]	Status register

1.3.907 B[0..3]_UDB07_08_ST

UDB07_08_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_08_ST: 0x68CE B1_UDB07_08_ST: 0x6ACE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST_MS							

Status Register

Bits	Name	Description
15:8	ST_MS[7:0]	Status register
7:0	ST_LS[7:0]	Status register

1.3.908 B[0..3]_UDB08_09_ST

UDB08_09_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_09_ST: 0x68D0 B1_UDB08_09_ST: 0x6AD0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST_MS							

Status Register

Bits	Name	Description
15:8	ST_MS[7:0]	Status register
7:0	ST_LS[7:0]	Status register

1.3.909 B[0..3]_UDB09_10_ST

UDB09_10_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_10_ST: 0x68D2 B1_UDB09_10_ST: 0x6AD2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST_MS							

Status Register

Bits	Name	Description
15:8	ST_MS[7:0]	Status register
7:0	ST_LS[7:0]	Status register

1.3.910 B[0..3]_UDB10_11_ST

UDB10_11_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_11_ST: 0x68D4 B1_UDB10_11_ST: 0x6AD4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST_MS							

Status Register

Bits	Name	Description
15:8	ST_MS[7:0]	Status register
7:0	ST_LS[7:0]	Status register

1.3.911 B[0..3]_UDB11_12_ST

UDB11_12_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_12_ST: 0x68D6 B1_UDB11_12_ST: 0x6AD6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST_MS							

Status Register

Bits	Name	Description
15:8	ST_MS[7:0]	Status register
7:0	ST_LS[7:0]	Status register

1.3.912 B[0..3]_UDB12_13_ST

UDB12_13_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_13_ST: 0x68D8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST_MS							

Status Register

Bits	Name	Description
15:8	ST_MS[7:0]	Status register
7:0	ST_LS[7:0]	Status register

1.3.913 B[0..3]_UDB13_14_ST

UDB13_14_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_14_ST: 0x68DA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST_MS							

Status Register

Bits	Name	Description
15:8	ST_MS[7:0]	Status register
7:0	ST_LS[7:0]	Status register

1.3.914 B[0..3]_UDB14_15_ST

UDB14_15_ST

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_15_ST: 0x68DC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST_MS							

Status Register

Bits	Name	Description
15:8	ST_MS[7:0]	Status register
7:0	ST_LS[7:0]	Status register

1.3.915 B[0..3]_UDB00_01_CTL

UDB00_01_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_01_CTL: 0x68E0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL_MS							

Control Register

Bits	Name	Description
15:8	CTL_MS[7:0]	Control register
7:0	CTL_LS[7:0]	Control register

1.3.916 B[0..3]_UDB01_02_CTL

UDB01_02_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_02_CTL: 0x68E2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL_MS							

Control Register

Bits	Name	Description
15:8	CTL_MS[7:0]	Control register
7:0	CTL_LS[7:0]	Control register

1.3.917 B[0..3]_UDB02_03_CTL

UDB02_03_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_03_CTL: 0x68E4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL_MS							

Control Register

Bits	Name	Description
15:8	CTL_MS[7:0]	Control register
7:0	CTL_LS[7:0]	Control register

1.3.918 B[0..3]_UDB03_04_CTL

UDB03_04_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_04_CTL: 0x68E6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL_MS							

Control Register

Bits	Name	Description
15:8	CTL_MS[7:0]	Control register
7:0	CTL_LS[7:0]	Control register

1.3.919 B[0..3]_UDB04_05_CTL

UDB04_05_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_05_CTL: 0x68E8 B1_UDB04_05_CTL: 0x6AE8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL_MS							

Control Register

Bits	Name	Description
15:8	CTL_MS[7:0]	Control register
7:0	CTL_LS[7:0]	Control register

1.3.920 B[0..3]_UDB05_06_CTL

UDB05_06_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_06_CTL: 0x68EA B1_UDB05_06_CTL: 0x6AEA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL_MS							

Control Register

Bits	Name	Description
15:8	CTL_MS[7:0]	Control register
7:0	CTL_LS[7:0]	Control register

1.3.921 B[0..3]_UDB06_07_CTL

UDB06_07_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_07_CTL: 0x68EC B1_UDB06_07_CTL: 0x6AEC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL_MS							

Control Register

Bits	Name	Description
15:8	CTL_MS[7:0]	Control register
7:0	CTL_LS[7:0]	Control register

1.3.922 B[0..3]_UDB07_08_CTL

UDB07_08_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_08_CTL: 0x68EE B1_UDB07_08_CTL: 0x6AEE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL_MS							

Control Register

Bits	Name	Description
15:8	CTL_MS[7:0]	Control register
7:0	CTL_LS[7:0]	Control register

1.3.923 B[0..3]_UDB08_09_CTL

UDB08_09_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_09_CTL: 0x68F0 B1_UDB08_09_CTL: 0x6AF0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL_MS							

Control Register

Bits	Name	Description
15:8	CTL_MS[7:0]	Control register
7:0	CTL_LS[7:0]	Control register

1.3.924 B[0..3]_UDB09_10_CTL

UDB09_10_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_10_CTL: 0x68F2 B1_UDB09_10_CTL: 0x6AF2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL_MS							

Control Register

Bits	Name	Description
15:8	CTL_MS[7:0]	Control register
7:0	CTL_LS[7:0]	Control register

1.3.925 B[0..3]_UDB10_11_CTL

UDB10_11_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_11_CTL: 0x68F4 B1_UDB10_11_CTL: 0x6AF4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL_MS							

Control Register

Bits	Name	Description
15:8	CTL_MS[7:0]	Control register
7:0	CTL_LS[7:0]	Control register

1.3.926 B[0..3]_UDB11_12_CTL

UDB11_12_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_12_CTL: 0x68F6 B1_UDB11_12_CTL: 0x6AF6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL_MS							

Control Register

Bits	Name	Description
15:8	CTL_MS[7:0]	Control register
7:0	CTL_LS[7:0]	Control register

1.3.927 B[0..3]_UDB12_13_CTL

UDB12_13_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_13_CTL: 0x68F8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL_MS							

Control Register

Bits	Name	Description
15:8	CTL_MS[7:0]	Control register
7:0	CTL_LS[7:0]	Control register

1.3.928 B[0..3]_UDB13_14_CTL

UDB13_14_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_14_CTL: 0x68FA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL_MS							

Control Register

Bits	Name	Description
15:8	CTL_MS[7:0]	Control register
7:0	CTL_LS[7:0]	Control register

1.3.929 B[0..3]_UDB14_15_CTL

UDB14_15_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_15_CTL: 0x68FC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL_LS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL_MS							

Control Register

Bits	Name	Description
15:8	CTL_MS[7:0]	Control register
7:0	CTL_LS[7:0]	Control register

1.3.930 B[0..3]_UDB00_01_MSK

UDB00_01_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB00_01_MSK: 0x6900

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK_LS						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK_MS						

Interrupt Mask

Bits	Name	Description
14:8	MSK_MS[6:0]	Generic field for 7 bit working registers
6:0	MSK_LS[6:0]	Generic field for 7 bit working registers

1.3.931 B[0..3]_UDB01_02_MSK

UDB01_02_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB01_02_MSK: 0x6902

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK_LS						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK_MS						

Interrupt Mask

Bits	Name	Description
14:8	MSK_MS[6:0]	Generic field for 7 bit working registers
6:0	MSK_LS[6:0]	Generic field for 7 bit working registers

1.3.932 B[0..3]_UDB02_03_MSK

UDB02_03_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB02_03_MSK: 0x6904

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK_LS						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK_MS						

Interrupt Mask

Bits	Name	Description
14:8	MSK_MS[6:0]	Generic field for 7 bit working registers
6:0	MSK_LS[6:0]	Generic field for 7 bit working registers

1.3.933 B[0..3]_UDB03_04_MSK

UDB03_04_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB03_04_MSK: 0x6906

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK_LS						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK_MS						

Interrupt Mask

Bits	Name	Description
14:8	MSK_MS[6:0]	Generic field for 7 bit working registers
6:0	MSK_LS[6:0]	Generic field for 7 bit working registers

1.3.934 B[0..3]_UDB04_05_MSK

UDB04_05_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB04_05_MSK: 0x6908 B1_UDB04_05_MSK: 0x6B08

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK_LS						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK_MS						

Interrupt Mask

Bits	Name	Description
14:8	MSK_MS[6:0]	Generic field for 7 bit working registers
6:0	MSK_LS[6:0]	Generic field for 7 bit working registers

1.3.935 B[0..3]_UDB05_06_MSK

UDB05_06_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB05_06_MSK: 0x690A B1_UDB05_06_MSK: 0x6B0A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK_LS						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK_MS						

Interrupt Mask

Bits	Name	Description
14:8	MSK_MS[6:0]	Generic field for 7 bit working registers
6:0	MSK_LS[6:0]	Generic field for 7 bit working registers

1.3.936 B[0..3]_UDB06_07_MSK

UDB06_07_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB06_07_MSK: 0x690C B1_UDB06_07_MSK: 0x6B0C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK_LS						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK_MS						

Interrupt Mask

Bits	Name	Description
14:8	MSK_MS[6:0]	Generic field for 7 bit working registers
6:0	MSK_LS[6:0]	Generic field for 7 bit working registers

1.3.937 B[0..3]_UDB07_08_MSK

UDB07_08_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB07_08_MSK: 0x690E B1_UDB07_08_MSK: 0x6B0E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK_LS						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK_MS						

Interrupt Mask

Bits	Name	Description
14:8	MSK_MS[6:0]	Generic field for 7 bit working registers
6:0	MSK_LS[6:0]	Generic field for 7 bit working registers

1.3.938 B[0..3]_UDB08_09_MSK

UDB08_09_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB08_09_MSK: 0x6910 B1_UDB08_09_MSK: 0x6B10

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK_LS						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK_MS						

Interrupt Mask

Bits	Name	Description
14:8	MSK_MS[6:0]	Generic field for 7 bit working registers
6:0	MSK_LS[6:0]	Generic field for 7 bit working registers

1.3.939 B[0..3]_UDB09_10_MSK

UDB09_10_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB09_10_MSK: 0x6912 B1_UDB09_10_MSK: 0x6B12

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK_LS						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK_MS						

Interrupt Mask

Bits	Name	Description
14:8	MSK_MS[6:0]	Generic field for 7 bit working registers
6:0	MSK_LS[6:0]	Generic field for 7 bit working registers

1.3.940 B[0..3]_UDB10_11_MSK

UDB10_11_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB10_11_MSK: 0x6914 B1_UDB10_11_MSK: 0x6B14

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK_LS						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK_MS						

Interrupt Mask

Bits	Name	Description
14:8	MSK_MS[6:0]	Generic field for 7 bit working registers
6:0	MSK_LS[6:0]	Generic field for 7 bit working registers

1.3.941 B[0..3]_UDB11_12_MSK

UDB11_12_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB11_12_MSK: 0x6916 B1_UDB11_12_MSK: 0x6B16

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK_LS						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK_MS						

Interrupt Mask

Bits	Name	Description
14:8	MSK_MS[6:0]	Generic field for 7 bit working registers
6:0	MSK_LS[6:0]	Generic field for 7 bit working registers

1.3.942 B[0..3]_UDB12_13_MSK

UDB12_13_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB12_13_MSK: 0x6918

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK_LS						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK_MS						

Interrupt Mask

Bits	Name	Description
14:8	MSK_MS[6:0]	Generic field for 7 bit working registers
6:0	MSK_LS[6:0]	Generic field for 7 bit working registers

1.3.943 B[0..3]_UDB13_14_MSK

UDB13_14_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB13_14_MSK: 0x691A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK_LS						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK_MS						

Interrupt Mask

Bits	Name	Description
14:8	MSK_MS[6:0]	Generic field for 7 bit working registers
6:0	MSK_LS[6:0]	Generic field for 7 bit working registers

1.3.944 B[0..3]_UDB14_15_MSK

UDB14_15_MSK

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB14_15_MSK: 0x691C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK_LS						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK_MS						

Interrupt Mask

Bits	Name	Description
14:8	MSK_MS[6:0]	Generic field for 7 bit working registers
6:0	MSK_LS[6:0]	Generic field for 7 bit working registers

1.3.945 B[0..3]_UDB00_01_ACTL

UDB00_01_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB00_01_ACTL: 0x6920

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Auxiliary Control

Bits	Name	Description
13	CNT_START_MS	FIFO0 clear See Table 1-528.
12	INT_EN_MS	(no description) See Table 1-531.
11	FIFO1_LVL_MS	FIFO level See Table 1-530.
10	FIFO0_LVL_MS	FIFO level See Table 1-530.
9	FIFO1_CLR_MS	FIFO clear See Table 1-529.
8	FIFO0_CLR_MS	FIFO clear See Table 1-529.
5	CNT_START_LS	FIFO0 clear See Table 1-528.
4	INT_EN_LS	(no description) See Table 1-531.

(continued)

3	FIFO1_LVL_LS	FIFO level See Table 1-530.
2	FIFO0_LVL_LS	FIFO level See Table 1-530.
1	FIFO1_CLR_LS	FIFO clear See Table 1-529.
0	FIFO0_CLR_LS	FIFO clear See Table 1-529.

Table 1-528. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-529. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-530. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-531. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.946 B[0..3]_UDB01_02_ACTL

UDB01_02_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB01_02_ACTL: 0x6922

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Auxiliary Control

Bits	Name	Description
13	CNT_START_MS	FIFO0 clear See Table 1-532.
12	INT_EN_MS	(no description) See Table 1-535.
11	FIFO1_LVL_MS	FIFO level See Table 1-534.
10	FIFO0_LVL_MS	FIFO level See Table 1-534.
9	FIFO1_CLR_MS	FIFO clear See Table 1-533.
8	FIFO0_CLR_MS	FIFO clear See Table 1-533.
5	CNT_START_LS	FIFO0 clear See Table 1-532.
4	INT_EN_LS	(no description) See Table 1-535.

(continued)

3	FIFO1_LVL_LS	FIFO level See Table 1-534.
2	FIFO0_LVL_LS	FIFO level See Table 1-534.
1	FIFO1_CLR_LS	FIFO clear See Table 1-533.
0	FIFO0_CLR_LS	FIFO clear See Table 1-533.

Table 1-532. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-533. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-534. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-535. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.947 B[0..3]_UDB02_03_ACTL

UDB02_03_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB02_03_ACTL: 0x6924

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Auxiliary Control

Bits	Name	Description
13	CNT_START_MS	FIFO0 clear See Table 1-536.
12	INT_EN_MS	(no description) See Table 1-539.
11	FIFO1_LVL_MS	FIFO level See Table 1-538.
10	FIFO0_LVL_MS	FIFO level See Table 1-538.
9	FIFO1_CLR_MS	FIFO clear See Table 1-537.
8	FIFO0_CLR_MS	FIFO clear See Table 1-537.
5	CNT_START_LS	FIFO0 clear See Table 1-536.
4	INT_EN_LS	(no description) See Table 1-539.

(continued)

3	FIFO1_LVL_LS	FIFO level See Table 1-538.
2	FIFO0_LVL_LS	FIFO level See Table 1-538.
1	FIFO1_CLR_LS	FIFO clear See Table 1-537.
0	FIFO0_CLR_LS	FIFO clear See Table 1-537.

Table 1-536. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-537. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-538. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-539. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.948 B[0..3]_UDB03_04_ACTL

UDB03_04_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB03_04_ACTL: 0x6926

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Auxiliary Control

Bits	Name	Description
13	CNT_START_MS	FIFO0 clear See Table 1-540.
12	INT_EN_MS	(no description) See Table 1-543.
11	FIFO1_LVL_MS	FIFO level See Table 1-542.
10	FIFO0_LVL_MS	FIFO level See Table 1-542.
9	FIFO1_CLR_MS	FIFO clear See Table 1-541.
8	FIFO0_CLR_MS	FIFO clear See Table 1-541.
5	CNT_START_LS	FIFO0 clear See Table 1-540.
4	INT_EN_LS	(no description) See Table 1-543.

(continued)

3	FIFO1_LVL_LS	FIFO level See Table 1-542.
2	FIFO0_LVL_LS	FIFO level See Table 1-542.
1	FIFO1_CLR_LS	FIFO clear See Table 1-541.
0	FIFO0_CLR_LS	FIFO clear See Table 1-541.

Table 1-540. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-541. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-542. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-543. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.949 B[0..3]_UDB04_05_ACTL

UDB04_05_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB04_05_ACTL: 0x6928 B1_UDB04_05_ACTL: 0x6B28

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Auxiliary Control

Bits	Name	Description
13	CNT_START_MS	FIFO0 clear See Table 1-544.
12	INT_EN_MS	(no description) See Table 1-547.
11	FIFO1_LVL_MS	FIFO level See Table 1-546.
10	FIFO0_LVL_MS	FIFO level See Table 1-546.
9	FIFO1_CLR_MS	FIFO clear See Table 1-545.
8	FIFO0_CLR_MS	FIFO clear See Table 1-545.
5	CNT_START_LS	FIFO0 clear See Table 1-544.
4	INT_EN_LS	(no description) See Table 1-547.

(continued)

3	FIFO1_LVL_LS	FIFO level See Table 1-546.
2	FIFO0_LVL_LS	FIFO level See Table 1-546.
1	FIFO1_CLR_LS	FIFO clear See Table 1-545.
0	FIFO0_CLR_LS	FIFO clear See Table 1-545.

Table 1-544. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-545. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-546. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-547. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.950 B[0..3]_UDB05_06_ACTL

UDB05_06_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB05_06_ACTL: 0x692A B1_UDB05_06_ACTL: 0x6B2A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Auxiliary Control

Bits	Name	Description
13	CNT_START_MS	FIFO0 clear See Table 1-548.
12	INT_EN_MS	(no description) See Table 1-551.
11	FIFO1_LVL_MS	FIFO level See Table 1-550.
10	FIFO0_LVL_MS	FIFO level See Table 1-550.
9	FIFO1_CLR_MS	FIFO clear See Table 1-549.
8	FIFO0_CLR_MS	FIFO clear See Table 1-549.
5	CNT_START_LS	FIFO0 clear See Table 1-548.
4	INT_EN_LS	(no description) See Table 1-551.

(continued)

3	FIFO1_LVL_LS	FIFO level See Table 1-550.
2	FIFO0_LVL_LS	FIFO level See Table 1-550.
1	FIFO1_CLR_LS	FIFO clear See Table 1-549.
0	FIFO0_CLR_LS	FIFO clear See Table 1-549.

Table 1-548. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-549. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-550. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-551. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.951 B[0..3]_UDB06_07_ACTL

UDB06_07_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB06_07_ACTL: 0x692C B1_UDB06_07_ACTL: 0x6B2C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Auxiliary Control

Bits	Name	Description
13	CNT_START_MS	FIFO0 clear See Table 1-552.
12	INT_EN_MS	(no description) See Table 1-555.
11	FIFO1_LVL_MS	FIFO level See Table 1-554.
10	FIFO0_LVL_MS	FIFO level See Table 1-554.
9	FIFO1_CLR_MS	FIFO clear See Table 1-553.
8	FIFO0_CLR_MS	FIFO clear See Table 1-553.
5	CNT_START_LS	FIFO0 clear See Table 1-552.
4	INT_EN_LS	(no description) See Table 1-555.

(continued)

3	FIFO1_LVL_LS	FIFO level See Table 1-554.
2	FIFO0_LVL_LS	FIFO level See Table 1-554.
1	FIFO1_CLR_LS	FIFO clear See Table 1-553.
0	FIFO0_CLR_LS	FIFO clear See Table 1-553.

Table 1-552. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-553. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-554. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-555. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.952 B[0..3]_UDB07_08_ACTL

UDB07_08_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB07_08_ACTL: 0x692E B1_UDB07_08_ACTL: 0x6B2E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Auxiliary Control

Bits	Name	Description
13	CNT_START_MS	FIFO0 clear See Table 1-556.
12	INT_EN_MS	(no description) See Table 1-559.
11	FIFO1_LVL_MS	FIFO level See Table 1-558.
10	FIFO0_LVL_MS	FIFO level See Table 1-558.
9	FIFO1_CLR_MS	FIFO clear See Table 1-557.
8	FIFO0_CLR_MS	FIFO clear See Table 1-557.
5	CNT_START_LS	FIFO0 clear See Table 1-556.
4	INT_EN_LS	(no description) See Table 1-559.

(continued)

3	FIFO1_LVL_LS	FIFO level See Table 1-558.
2	FIFO0_LVL_LS	FIFO level See Table 1-558.
1	FIFO1_CLR_LS	FIFO clear See Table 1-557.
0	FIFO0_CLR_LS	FIFO clear See Table 1-557.

Table 1-556. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-557. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-558. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-559. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.953 B[0..3]_UDB08_09_ACTL

UDB08_09_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB08_09_ACTL: 0x6930 B1_UDB08_09_ACTL: 0x6B30

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Auxiliary Control

Bits	Name	Description
13	CNT_START_MS	FIFO0 clear See Table 1-560.
12	INT_EN_MS	(no description) See Table 1-563.
11	FIFO1_LVL_MS	FIFO level See Table 1-562.
10	FIFO0_LVL_MS	FIFO level See Table 1-562.
9	FIFO1_CLR_MS	FIFO clear See Table 1-561.
8	FIFO0_CLR_MS	FIFO clear See Table 1-561.
5	CNT_START_LS	FIFO0 clear See Table 1-560.
4	INT_EN_LS	(no description) See Table 1-563.

(continued)

3	FIFO1_LVL_LS	FIFO level See Table 1-562.
2	FIFO0_LVL_LS	FIFO level See Table 1-562.
1	FIFO1_CLR_LS	FIFO clear See Table 1-561.
0	FIFO0_CLR_LS	FIFO clear See Table 1-561.

Table 1-560. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-561. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-562. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-563. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.954 B[0..3]_UDB09_10_ACTL

UDB09_10_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB09_10_ACTL: 0x6932 B1_UDB09_10_ACTL: 0x6B32

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Auxiliary Control

Bits	Name	Description
13	CNT_START_MS	FIFO0 clear See Table 1-564.
12	INT_EN_MS	(no description) See Table 1-567.
11	FIFO1_LVL_MS	FIFO level See Table 1-566.
10	FIFO0_LVL_MS	FIFO level See Table 1-566.
9	FIFO1_CLR_MS	FIFO clear See Table 1-565.
8	FIFO0_CLR_MS	FIFO clear See Table 1-565.
5	CNT_START_LS	FIFO0 clear See Table 1-564.
4	INT_EN_LS	(no description) See Table 1-567.

(continued)

3	FIFO1_LVL_LS	FIFO level See Table 1-566.
2	FIFO0_LVL_LS	FIFO level See Table 1-566.
1	FIFO1_CLR_LS	FIFO clear See Table 1-565.
0	FIFO0_CLR_LS	FIFO clear See Table 1-565.

Table 1-564. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-565. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-566. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-567. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.955 B[0..3]_UDB10_11_ACTL

UDB10_11_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB10_11_ACTL: 0x6934 B1_UDB10_11_ACTL: 0x6B34

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Auxiliary Control

Bits	Name	Description
13	CNT_START_MS	FIFO0 clear See Table 1-568.
12	INT_EN_MS	(no description) See Table 1-571.
11	FIFO1_LVL_MS	FIFO level See Table 1-570.
10	FIFO0_LVL_MS	FIFO level See Table 1-570.
9	FIFO1_CLR_MS	FIFO clear See Table 1-569.
8	FIFO0_CLR_MS	FIFO clear See Table 1-569.
5	CNT_START_LS	FIFO0 clear See Table 1-568.
4	INT_EN_LS	(no description) See Table 1-571.

(continued)

3	FIFO1_LVL_LS	FIFO level See Table 1-570.
2	FIFO0_LVL_LS	FIFO level See Table 1-570.
1	FIFO1_CLR_LS	FIFO clear See Table 1-569.
0	FIFO0_CLR_LS	FIFO clear See Table 1-569.

Table 1-568. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-569. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-570. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-571. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.956 B[0..3]_UDB11_12_ACTL

UDB11_12_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB11_12_ACTL: 0x6936 B1_UDB11_12_ACTL: 0x6B36

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Auxiliary Control

Bits	Name	Description
13	CNT_START_MS	FIFO0 clear See Table 1-572.
12	INT_EN_MS	(no description) See Table 1-575.
11	FIFO1_LVL_MS	FIFO level See Table 1-574.
10	FIFO0_LVL_MS	FIFO level See Table 1-574.
9	FIFO1_CLR_MS	FIFO clear See Table 1-573.
8	FIFO0_CLR_MS	FIFO clear See Table 1-573.
5	CNT_START_LS	FIFO0 clear See Table 1-572.
4	INT_EN_LS	(no description) See Table 1-575.

(continued)

3	FIFO1_LVL_LS	FIFO level See Table 1-574.
2	FIFO0_LVL_LS	FIFO level See Table 1-574.
1	FIFO1_CLR_LS	FIFO clear See Table 1-573.
0	FIFO0_CLR_LS	FIFO clear See Table 1-573.

Table 1-572. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-573. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-574. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-575. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.957 B[0..3]_UDB12_13_ACTL

UDB12_13_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB12_13_ACTL: 0x6938

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Auxiliary Control

Bits	Name	Description
13	CNT_START_MS	FIFO0 clear See Table 1-576.
12	INT_EN_MS	(no description) See Table 1-579.
11	FIFO1_LVL_MS	FIFO level See Table 1-578.
10	FIFO0_LVL_MS	FIFO level See Table 1-578.
9	FIFO1_CLR_MS	FIFO clear See Table 1-577.
8	FIFO0_CLR_MS	FIFO clear See Table 1-577.
5	CNT_START_LS	FIFO0 clear See Table 1-576.
4	INT_EN_LS	(no description) See Table 1-579.

(continued)

3	FIFO1_LVL_LS	FIFO level See Table 1-578.
2	FIFO0_LVL_LS	FIFO level See Table 1-578.
1	FIFO1_CLR_LS	FIFO clear See Table 1-577.
0	FIFO0_CLR_LS	FIFO clear See Table 1-577.

Table 1-576. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-577. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-578. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-579. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.958 B[0..3]_UDB13_14_ACTL

UDB13_14_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB13_14_ACTL: 0x693A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Auxiliary Control

Bits	Name	Description
13	CNT_START_MS	FIFO0 clear See Table 1-580.
12	INT_EN_MS	(no description) See Table 1-583.
11	FIFO1_LVL_MS	FIFO level See Table 1-582.
10	FIFO0_LVL_MS	FIFO level See Table 1-582.
9	FIFO1_CLR_MS	FIFO clear See Table 1-581.
8	FIFO0_CLR_MS	FIFO clear See Table 1-581.
5	CNT_START_LS	FIFO0 clear See Table 1-580.
4	INT_EN_LS	(no description) See Table 1-583.

(continued)

3	FIFO1_LVL_LS	FIFO level See Table 1-582.
2	FIFO0_LVL_LS	FIFO level See Table 1-582.
1	FIFO1_CLR_LS	FIFO clear See Table 1-581.
0	FIFO0_CLR_LS	FIFO clear See Table 1-581.

Table 1-580. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-581. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-582. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-583. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.959 B[0..3]_UDB14_15_ACTL

UDB14_15_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB14_15_ACTL: 0x693C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Auxiliary Control

Bits	Name	Description
13	CNT_START_MS	FIFO0 clear See Table 1-584.
12	INT_EN_MS	(no description) See Table 1-587.
11	FIFO1_LVL_MS	FIFO level See Table 1-586.
10	FIFO0_LVL_MS	FIFO level See Table 1-586.
9	FIFO1_CLR_MS	FIFO clear See Table 1-585.
8	FIFO0_CLR_MS	FIFO clear See Table 1-585.
5	CNT_START_LS	FIFO0 clear See Table 1-584.
4	INT_EN_LS	(no description) See Table 1-587.

(continued)

3	FIFO1_LVL_LS	FIFO level See Table 1-586.
2	FIFO0_LVL_LS	FIFO level See Table 1-586.
1	FIFO1_CLR_LS	FIFO clear See Table 1-585.
0	FIFO0_CLR_LS	FIFO clear See Table 1-585.

Table 1-584. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

Table 1-585. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-586. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-587. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.960 B[0..3]_UDB00_01_MC

UDB00_01_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_01_MC: 0x6940

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_MS				PLD0_MC_MS			

PLD Macrocell reading

Bits	Name	Description
15:12	PLD1_MC_MS[3:0]	Read Macrocell
11:8	PLD0_MC_MS[3:0]	Read Macrocell
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.961 B[0..3]_UDB01_02_MC

UDB01_02_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_02_MC: 0x6942

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_MS				PLD0_MC_MS			

PLD Macrocell reading

Bits	Name	Description
15:12	PLD1_MC_MS[3:0]	Read Macrocell
11:8	PLD0_MC_MS[3:0]	Read Macrocell
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.962 B[0..3]_UDB02_03_MC

UDB02_03_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_03_MC: 0x6944

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_MS				PLD0_MC_MS			

PLD Macrocell reading

Bits	Name	Description
15:12	PLD1_MC_MS[3:0]	Read Macrocell
11:8	PLD0_MC_MS[3:0]	Read Macrocell
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.963 B[0..3]_UDB03_04_MC

UDB03_04_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_04_MC: 0x6946

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_MS				PLD0_MC_MS			

PLD Macrocell reading

Bits	Name	Description
15:12	PLD1_MC_MS[3:0]	Read Macrocell
11:8	PLD0_MC_MS[3:0]	Read Macrocell
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.964 B[0..3]_UDB04_05_MC

UDB04_05_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_05_MC: 0x6948 B1_UDB04_05_MC: 0x6B48

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_MS				PLD0_MC_MS			

PLD Macrocell reading

Bits	Name	Description
15:12	PLD1_MC_MS[3:0]	Read Macrocell
11:8	PLD0_MC_MS[3:0]	Read Macrocell
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.965 B[0..3]_UDB05_06_MC

UDB05_06_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_06_MC: 0x694A B1_UDB05_06_MC: 0x6B4A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_MS				PLD0_MC_MS			

PLD Macrocell reading

Bits	Name	Description
15:12	PLD1_MC_MS[3:0]	Read Macrocell
11:8	PLD0_MC_MS[3:0]	Read Macrocell
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.966 B[0..3]_UDB06_07_MC

UDB06_07_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_07_MC: 0x694C B1_UDB06_07_MC: 0x6B4C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_MS				PLD0_MC_MS			

PLD Macrocell reading

Bits	Name	Description
15:12	PLD1_MC_MS[3:0]	Read Macrocell
11:8	PLD0_MC_MS[3:0]	Read Macrocell
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.967 B[0..3]_UDB07_08_MC

UDB07_08_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_08_MC: 0x694E B1_UDB07_08_MC: 0x6B4E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_MS				PLD0_MC_MS			

PLD Macrocell reading

Bits	Name	Description
15:12	PLD1_MC_MS[3:0]	Read Macrocell
11:8	PLD0_MC_MS[3:0]	Read Macrocell
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.968 B[0..3]_UDB08_09_MC

UDB08_09_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_09_MC: 0x6950 B1_UDB08_09_MC: 0x6B50

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_MS				PLD0_MC_MS			

PLD Macrocell reading

Bits	Name	Description
15:12	PLD1_MC_MS[3:0]	Read Macrocell
11:8	PLD0_MC_MS[3:0]	Read Macrocell
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.969 B[0..3]_UDB09_10_MC

UDB09_10_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_10_MC: 0x6952 B1_UDB09_10_MC: 0x6B52

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_MS				PLD0_MC_MS			

PLD Macrocell reading

Bits	Name	Description
15:12	PLD1_MC_MS[3:0]	Read Macrocell
11:8	PLD0_MC_MS[3:0]	Read Macrocell
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.970 B[0..3]_UDB10_11_MC

UDB10_11_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_11_MC: 0x6954 B1_UDB10_11_MC: 0x6B54

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_MS				PLD0_MC_MS			

PLD Macrocell reading

Bits	Name	Description
15:12	PLD1_MC_MS[3:0]	Read Macrocell
11:8	PLD0_MC_MS[3:0]	Read Macrocell
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.971 B[0..3]_UDB11_12_MC

UDB11_12_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_12_MC: 0x6956 B1_UDB11_12_MC: 0x6B56

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_MS				PLD0_MC_MS			

PLD Macrocell reading

Bits	Name	Description
15:12	PLD1_MC_MS[3:0]	Read Macrocell
11:8	PLD0_MC_MS[3:0]	Read Macrocell
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.972 B[0..3]_UDB12_13_MC

UDB12_13_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_13_MC: 0x6958

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_MS				PLD0_MC_MS			

PLD Macrocell reading

Bits	Name	Description
15:12	PLD1_MC_MS[3:0]	Read Macrocell
11:8	PLD0_MC_MS[3:0]	Read Macrocell
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.973 B[0..3]_UDB13_14_MC

UDB13_14_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_14_MC: 0x695A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_MS				PLD0_MC_MS			

PLD Macrocell reading

Bits	Name	Description
15:12	PLD1_MC_MS[3:0]	Read Macrocell
11:8	PLD0_MC_MS[3:0]	Read Macrocell
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.974 B[0..3]_UDB14_15_MC

UDB14_15_MC

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_15_MC: 0x695C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_MS				PLD0_MC_MS			

PLD Macrocell reading

Bits	Name	Description
15:12	PLD1_MC_MS[3:0]	Read Macrocell
11:8	PLD0_MC_MS[3:0]	Read Macrocell
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.975 B[0..3]_UDB00_A0_A1

UDB00_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_A0_A1: 0x6800

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1							

Accumulator 0 and 1

Bits	Name	Description
15:8	A1[7:0]	Generic field for 8 bit working registers
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.976 B[0..3]_UDB01_A0_A1

UDB01_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_A0_A1: 0x6802

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1							

Accumulator 0 and 1

Bits	Name	Description
15:8	A1[7:0]	Generic field for 8 bit working registers
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.977 B[0..3]_UDB02_A0_A1

UDB02_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_A0_A1: 0x6804

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1							

Accumulator 0 and 1

Bits	Name	Description
15:8	A1[7:0]	Generic field for 8 bit working registers
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.978 B[0..3]_UDB03_A0_A1

UDB03_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_A0_A1: 0x6806

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1							

Accumulator 0 and 1

Bits	Name	Description
15:8	A1[7:0]	Generic field for 8 bit working registers
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.979 B[0..3]_UDB04_A0_A1

UDB04_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_A0_A1: 0x6808 B1_UDB04_A0_A1: 0x6A08

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1							

Accumulator 0 and 1

Bits	Name	Description
15:8	A1[7:0]	Generic field for 8 bit working registers
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.980 B[0..3]_UDB05_A0_A1

UDB05_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_A0_A1: 0x680A

B1_UDB05_A0_A1: 0x6A0A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1							

Accumulator 0 and 1

Bits	Name	Description
15:8	A1[7:0]	Generic field for 8 bit working registers
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.981 B[0..3]_UDB06_A0_A1

UDB06_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_A0_A1: 0x680C B1_UDB06_A0_A1: 0x6A0C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1							

Accumulator 0 and 1

Bits	Name	Description
15:8	A1[7:0]	Generic field for 8 bit working registers
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.982 B[0..3]_UDB07_A0_A1

UDB07_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_A0_A1: 0x680E B1_UDB07_A0_A1: 0x6A0E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1							

Accumulator 0 and 1

Bits	Name	Description
15:8	A1[7:0]	Generic field for 8 bit working registers
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.983 B[0..3]_UDB08_A0_A1

UDB08_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_A0_A1: 0x6810 B1_UDB08_A0_A1: 0x6A10

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1							

Accumulator 0 and 1

Bits	Name	Description
15:8	A1[7:0]	Generic field for 8 bit working registers
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.984 B[0..3]_UDB09_A0_A1

UDB09_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_A0_A1: 0x6812 B1_UDB09_A0_A1: 0x6A12

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1							

Accumulator 0 and 1

Bits	Name	Description
15:8	A1[7:0]	Generic field for 8 bit working registers
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.985 B[0..3]_UDB10_A0_A1

UDB10_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_A0_A1: 0x6814 B1_UDB10_A0_A1: 0x6A14

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1							

Accumulator 0 and 1

Bits	Name	Description
15:8	A1[7:0]	Generic field for 8 bit working registers
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.986 B[0..3]_UDB11_A0_A1

UDB11_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_A0_A1: 0x6816 B1_UDB11_A0_A1: 0x6A16

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1							

Accumulator 0 and 1

Bits	Name	Description
15:8	A1[7:0]	Generic field for 8 bit working registers
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.987 B[0..3]_UDB12_A0_A1

UDB12_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_A0_A1: 0x6818

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1							

Accumulator 0 and 1

Bits	Name	Description
15:8	A1[7:0]	Generic field for 8 bit working registers
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.988 B[0..3]_UDB13_A0_A1

UDB13_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_A0_A1: 0x681A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1							

Accumulator 0 and 1

Bits	Name	Description
15:8	A1[7:0]	Generic field for 8 bit working registers
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.989 B[0..3]_UDB14_A0_A1

UDB14_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_A0_A1: 0x681C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1							

Accumulator 0 and 1

Bits	Name	Description
15:8	A1[7:0]	Generic field for 8 bit working registers
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.990 B[0..3]_UDB15_A0_A1

UDB15_A0_A1

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB15_A0_A1: 0x681E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	A1							

Accumulator 0 and 1

Bits	Name	Description
15:8	A1[7:0]	Generic field for 8 bit working registers
7:0	A0[7:0]	Generic field for 8 bit working registers

1.3.991 B[0..3]_UDB00_D0_D1

UDB00_D0_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB00_D0_D1: 0x6840

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1							

Data 0 and 1

Bits	Name	Description
15:8	D1[7:0]	Generic field for 8 bit working registers
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.992 B[0..3]_UDB01_D0_D1

UDB01_D0_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB01_D0_D1: 0x6842

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1							

Data 0 and 1

Bits	Name	Description
15:8	D1[7:0]	Generic field for 8 bit working registers
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.993 B[0..3]_UDB02_D0_D1

UDB02_D0_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB02_D0_D1: 0x6844

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1							

Data 0 and 1

Bits	Name	Description
15:8	D1[7:0]	Generic field for 8 bit working registers
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.994 B[0..3]_UDB03_D0_D1

UDB03_D0_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB03_D0_D1: 0x6846

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1							

Data 0 and 1

Bits	Name	Description
15:8	D1[7:0]	Generic field for 8 bit working registers
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.995 B[0..3]_UDB04_D0_D1

UDB04_D0_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB04_D0_D1: 0x6848 B1_UDB04_D0_D1: 0x6A48

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1							

Data 0 and 1

Bits	Name	Description
15:8	D1[7:0]	Generic field for 8 bit working registers
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.996 B[0..3]_UDB05_D0_D1

UDB05_D0_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB05_D0_D1: 0x684A

B1_UDB05_D0_D1: 0x6A4A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1							

Data 0 and 1

Bits	Name	Description
15:8	D1[7:0]	Generic field for 8 bit working registers
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.997 B[0..3]_UDB06_D0_D1

UDB06_D0_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB06_D0_D1: 0x684C B1_UDB06_D0_D1: 0x6A4C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1							

Data 0 and 1

Bits	Name	Description
15:8	D1[7:0]	Generic field for 8 bit working registers
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.998 B[0..3]_UDB07_D0_D1

UDB07_D0_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB07_D0_D1: 0x684E

B1_UDB07_D0_D1: 0x6A4E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1							

Data 0 and 1

Bits	Name	Description
15:8	D1[7:0]	Generic field for 8 bit working registers
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.999 B[0..3]_UDB08_D0_D1

UDB08_D0_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB08_D0_D1: 0x6850 B1_UDB08_D0_D1: 0x6A50

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1							

Data 0 and 1

Bits	Name	Description
15:8	D1[7:0]	Generic field for 8 bit working registers
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.1000 B[0..3]_UDB09_D0_D1

UDB09_D0_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB09_D0_D1: 0x6852 B1_UDB09_D0_D1: 0x6A52

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1							

Data 0 and 1

Bits	Name	Description
15:8	D1[7:0]	Generic field for 8 bit working registers
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.1001 B[0..3]_UDB10_D0_D1

UDB10_D0_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB10_D0_D1: 0x6854 B1_UDB10_D0_D1: 0x6A54

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1							

Data 0 and 1

Bits	Name	Description
15:8	D1[7:0]	Generic field for 8 bit working registers
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.1002 B[0..3]_UDB11_D0_D1

UDB11_D0_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB11_D0_D1: 0x6856 B1_UDB11_D0_D1: 0x6A56

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1							

Data 0 and 1

Bits	Name	Description
15:8	D1[7:0]	Generic field for 8 bit working registers
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.1003 B[0..3]_UDB12_D0_D1

UDB12_D0_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB12_D0_D1: 0x6858

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1							

Data 0 and 1

Bits	Name	Description
15:8	D1[7:0]	Generic field for 8 bit working registers
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.1004 B[0..3]_UDB13_D0_D1

UDB13_D0_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB13_D0_D1: 0x685A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1							

Data 0 and 1

Bits	Name	Description
15:8	D1[7:0]	Generic field for 8 bit working registers
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.1005 B[0..3]_UDB14_D0_D1

UDB14_D0_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB14_D0_D1: 0x685C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1							

Data 0 and 1

Bits	Name	Description
15:8	D1[7:0]	Generic field for 8 bit working registers
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.1006 B[0..3]_UDB15_D0_D1

UDB15_D0_D1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB15_D0_D1: 0x685E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	D1							

Data 0 and 1

Bits	Name	Description
15:8	D1[7:0]	Generic field for 8 bit working registers
7:0	D0[7:0]	Generic field for 8 bit working registers

1.3.1007 B[0..3]_UDB00_F0_F1

UDB00_F0_F1

Reset: N/A

Register : Address

B0_UDB00_F0_F1: 0x6880

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1							

FIFO 0 and 1

Bits	Name	Description
15:8	F1[7:0]	Generic field for 8 bit working registers
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.1008 B[0..3]_UDB01_F0_F1

UDB01_F0_F1

Reset: N/A

Register : Address

B0_UDB01_F0_F1: 0x6882

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1							

FIFO 0 and 1

Bits	Name	Description
15:8	F1[7:0]	Generic field for 8 bit working registers
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.1009 B[0..3]_UDB02_F0_F1

UDB02_F0_F1

Reset: N/A

Register : Address

B0_UDB02_F0_F1: 0x6884

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1							

FIFO 0 and 1

Bits	Name	Description
15:8	F1[7:0]	Generic field for 8 bit working registers
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.1010 B[0..3]_UDB03_F0_F1

UDB03_F0_F1

Reset: N/A

Register : Address

B0_UDB03_F0_F1: 0x6886

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1							

FIFO 0 and 1

Bits	Name	Description
15:8	F1[7:0]	Generic field for 8 bit working registers
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.1011 B[0..3]_UDB04_F0_F1

UDB04_F0_F1

Reset: N/A

Register : Address

B0_UDB04_F0_F1: 0x6888 B1_UDB04_F0_F1: 0x6A88

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1							

FIFO 0 and 1

Bits	Name	Description
15:8	F1[7:0]	Generic field for 8 bit working registers
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.1012 B[0..3]_UDB05_F0_F1

UDB05_F0_F1

Reset: N/A

Register : Address

B0_UDB05_F0_F1: 0x688A

B1_UDB05_F0_F1: 0x6A8A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1							

FIFO 0 and 1

Bits	Name	Description
15:8	F1[7:0]	Generic field for 8 bit working registers
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.1013 B[0..3]_UDB06_F0_F1

UDB06_F0_F1

Reset: N/A

Register : Address

B0_UDB06_F0_F1: 0x688C B1_UDB06_F0_F1: 0x6A8C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1							

FIFO 0 and 1

Bits	Name	Description
15:8	F1[7:0]	Generic field for 8 bit working registers
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.1014 B[0..3]_UDB07_F0_F1

UDB07_F0_F1

Reset: N/A

Register : Address

B0_UDB07_F0_F1: 0x688E

B1_UDB07_F0_F1: 0x6A8E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1							

FIFO 0 and 1

Bits	Name	Description
15:8	F1[7:0]	Generic field for 8 bit working registers
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.1015 B[0..3]_UDB08_F0_F1

UDB08_F0_F1

Reset: N/A

Register : Address

B0_UDB08_F0_F1: 0x6890 B1_UDB08_F0_F1: 0x6A90

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1							

FIFO 0 and 1

Bits	Name	Description
15:8	F1[7:0]	Generic field for 8 bit working registers
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.1016 B[0..3]_UDB09_F0_F1

UDB09_F0_F1

Reset: N/A

Register : Address

B0_UDB09_F0_F1: 0x6892 B1_UDB09_F0_F1: 0x6A92

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1							

FIFO 0 and 1

Bits	Name	Description
15:8	F1[7:0]	Generic field for 8 bit working registers
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.1017 B[0..3]_UDB10_F0_F1

UDB10_F0_F1

Reset: N/A

Register : Address

B0_UDB10_F0_F1: 0x6894 B1_UDB10_F0_F1: 0x6A94

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1							

FIFO 0 and 1

Bits	Name	Description
15:8	F1[7:0]	Generic field for 8 bit working registers
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.1018 B[0..3]_UDB11_F0_F1

UDB11_F0_F1

Reset: N/A

Register : Address

B0_UDB11_F0_F1: 0x6896 B1_UDB11_F0_F1: 0x6A96

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1							

FIFO 0 and 1

Bits	Name	Description
15:8	F1[7:0]	Generic field for 8 bit working registers
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.1019 B[0..3]_UDB12_F0_F1

UDB12_F0_F1

Reset: N/A

Register : Address

B0_UDB12_F0_F1: 0x6898

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1							

FIFO 0 and 1

Bits	Name	Description
15:8	F1[7:0]	Generic field for 8 bit working registers
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.1020 B[0..3]_UDB13_F0_F1

UDB13_F0_F1

Reset: N/A

Register : Address

B0_UDB13_F0_F1: 0x689A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1							

FIFO 0 and 1

Bits	Name	Description
15:8	F1[7:0]	Generic field for 8 bit working registers
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.1021 B[0..3]_UDB14_F0_F1

UDB14_F0_F1

Reset: N/A

Register : Address

B0_UDB14_F0_F1: 0x689C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1							

FIFO 0 and 1

Bits	Name	Description
15:8	F1[7:0]	Generic field for 8 bit working registers
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.1022 B[0..3]_UDB15_F0_F1

UDB15_F0_F1

Reset: N/A

Register : Address

B0_UDB15_F0_F1: 0x689E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F0							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	F1							

FIFO 0 and 1

Bits	Name	Description
15:8	F1[7:0]	Generic field for 8 bit working registers
7:0	F0[7:0]	Generic field for 8 bit working registers

1.3.1023 B[0..3]_UDB00_ST_CTL

UDB00_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_ST_CTL: 0x68C0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL							

My Status and Control Register

Bits	Name	Description
15:8	CTL[7:0]	My Control register
7:0	ST[7:0]	My Status register

1.3.1024 B[0..3]_UDB01_ST_CTL

UDB01_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_ST_CTL: 0x68C2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL							

My Status and Control Register

Bits	Name	Description
15:8	CTL[7:0]	My Control register
7:0	ST[7:0]	My Status register

1.3.1025 B[0..3]_UDB02_ST_CTL

UDB02_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_ST_CTL: 0x68C4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL							

My Status and Control Register

Bits	Name	Description
15:8	CTL[7:0]	My Control register
7:0	ST[7:0]	My Status register

1.3.1026 B[0..3]_UDB03_ST_CTL

UDB03_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_ST_CTL: 0x68C6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL							

My Status and Control Register

Bits	Name	Description
15:8	CTL[7:0]	My Control register
7:0	ST[7:0]	My Status register

1.3.1027 B[0..3]_UDB04_ST_CTL

UDB04_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_ST_CTL: 0x68C8 B1_UDB04_ST_CTL: 0x6AC8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL							

My Status and Control Register

Bits	Name	Description
15:8	CTL[7:0]	My Control register
7:0	ST[7:0]	My Status register

1.3.1028 B[0..3]_UDB05_ST_CTL

UDB05_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_ST_CTL: 0x68CA B1_UDB05_ST_CTL: 0x6ACA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL							

My Status and Control Register

Bits	Name	Description
15:8	CTL[7:0]	My Control register
7:0	ST[7:0]	My Status register

1.3.1029 B[0..3]_UDB06_ST_CTL

UDB06_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_ST_CTL: 0x68CC B1_UDB06_ST_CTL: 0x6ACC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL							

My Status and Control Register

Bits	Name	Description
15:8	CTL[7:0]	My Control register
7:0	ST[7:0]	My Status register

1.3.1030 B[0..3]_UDB07_ST_CTL

UDB07_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_ST_CTL: 0x68CE B1_UDB07_ST_CTL: 0x6ACE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL							

My Status and Control Register

Bits	Name	Description
15:8	CTL[7:0]	My Control register
7:0	ST[7:0]	My Status register

1.3.1031 B[0..3]_UDB08_ST_CTL

UDB08_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_ST_CTL: 0x68D0 B1_UDB08_ST_CTL: 0x6AD0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL							

My Status and Control Register

Bits	Name	Description
15:8	CTL[7:0]	My Control register
7:0	ST[7:0]	My Status register

1.3.1032 B[0..3]_UDB09_ST_CTL

UDB09_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_ST_CTL: 0x68D2 B1_UDB09_ST_CTL: 0x6AD2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL							

My Status and Control Register

Bits	Name	Description
15:8	CTL[7:0]	My Control register
7:0	ST[7:0]	My Status register

1.3.1033 B[0..3]_UDB10_ST_CTL

UDB10_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_ST_CTL: 0x68D4 B1_UDB10_ST_CTL: 0x6AD4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL							

My Status and Control Register

Bits	Name	Description
15:8	CTL[7:0]	My Control register
7:0	ST[7:0]	My Status register

1.3.1034 B[0..3]_UDB11_ST_CTL

UDB11_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_ST_CTL: 0x68D6 B1_UDB11_ST_CTL: 0x6AD6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL							

My Status and Control Register

Bits	Name	Description
15:8	CTL[7:0]	My Control register
7:0	ST[7:0]	My Status register

1.3.1035 B[0..3]_UDB12_ST_CTL

UDB12_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_ST_CTL: 0x68D8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL							

My Status and Control Register

Bits	Name	Description
15:8	CTL[7:0]	My Control register
7:0	ST[7:0]	My Status register

1.3.1036 B[0..3]_UDB13_ST_CTL

UDB13_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_ST_CTL: 0x68DA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL							

My Status and Control Register

Bits	Name	Description
15:8	CTL[7:0]	My Control register
7:0	ST[7:0]	My Status register

1.3.1037 B[0..3]_UDB14_ST_CTL

UDB14_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_ST_CTL: 0x68DC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL							

My Status and Control Register

Bits	Name	Description
15:8	CTL[7:0]	My Control register
7:0	ST[7:0]	My Status register

1.3.1038 B[0..3]_UDB15_ST_CTL

UDB15_ST_CTL

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB15_ST_CTL: 0x68DE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	ST							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	CTL							

My Status and Control Register

Bits	Name	Description
15:8	CTL[7:0]	My Control register
7:0	ST[7:0]	My Status register

1.3.1039 B[0..3]_UDB00_MSK_ACTL

UDB00_MSK_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB00_MSK_ACTL: 0x6900

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Interrupt Mask and Auxiliary Control

Bits	Name	Description
13	CNT_START	FIFO0 clear See Table 1-588.
12	INT_EN	(no description) See Table 1-591.
11	FIFO1_LVL	FIFO level See Table 1-590.
10	FIFO0_LVL	FIFO level See Table 1-590.
9	FIFO1_CLR	FIFO clear See Table 1-589.
8	FIFO0_CLR	FIFO clear See Table 1-589.
6:0	MSK[6:0]	Generic field for 7 bit working registers

Table 1-588. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

(continued)

Table 1-589. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-590. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-591. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.1040 B[0..3]_UDB01_MSK_ACTL

UDB01_MSK_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB01_MSK_ACTL: 0x6902

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Interrupt Mask and Auxiliary Control

Bits	Name	Description
13	CNT_START	FIFO0 clear See Table 1-592.
12	INT_EN	(no description) See Table 1-595.
11	FIFO1_LVL	FIFO level See Table 1-594.
10	FIFO0_LVL	FIFO level See Table 1-594.
9	FIFO1_CLR	FIFO clear See Table 1-593.
8	FIFO0_CLR	FIFO clear See Table 1-593.
6:0	MSK[6:0]	Generic field for 7 bit working registers

Table 1-592. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

(continued)

Table 1-593. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-594. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-595. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.1041 B[0..3]_UDB02_MSK_ACTL

UDB02_MSK_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB02_MSK_ACTL: 0x6904

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Interrupt Mask and Auxiliary Control

Bits	Name	Description
13	CNT_START	FIFO0 clear See Table 1-596.
12	INT_EN	(no description) See Table 1-599.
11	FIFO1_LVL	FIFO level See Table 1-598.
10	FIFO0_LVL	FIFO level See Table 1-598.
9	FIFO1_CLR	FIFO clear See Table 1-597.
8	FIFO0_CLR	FIFO clear See Table 1-597.
6:0	MSK[6:0]	Generic field for 7 bit working registers

Table 1-596. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

(continued)

Table 1-597. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-598. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-599. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.1042 B[0..3]_UDB03_MSK_ACTL

UDB03_MSK_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB03_MSK_ACTL: 0x6906

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Interrupt Mask and Auxiliary Control

Bits	Name	Description
13	CNT_START	FIFO0 clear See Table 1-600.
12	INT_EN	(no description) See Table 1-603.
11	FIFO1_LVL	FIFO level See Table 1-602.
10	FIFO0_LVL	FIFO level See Table 1-602.
9	FIFO1_CLR	FIFO clear See Table 1-601.
8	FIFO0_CLR	FIFO clear See Table 1-601.
6:0	MSK[6:0]	Generic field for 7 bit working registers

Table 1-600. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

(continued)

Table 1-601. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-602. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-603. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.1043 B[0..3]_UDB04_MSK_ACTL

UDB04_MSK_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB04_MSK_ACTL: 0x6908 B1_UDB04_MSK_ACTL: 0x6B08

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Interrupt Mask and Auxiliary Control

Bits	Name	Description
13	CNT_START	FIFO0 clear See Table 1-604.
12	INT_EN	(no description) See Table 1-607.
11	FIFO1_LVL	FIFO level See Table 1-606.
10	FIFO0_LVL	FIFO level See Table 1-606.
9	FIFO1_CLR	FIFO clear See Table 1-605.
8	FIFO0_CLR	FIFO clear See Table 1-605.
6:0	MSK[6:0]	Generic field for 7 bit working registers

Table 1-604. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

(continued)

Table 1-605. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-606. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-607. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.1044 B[0..3]_UDB05_MSK_ACTL

UDB05_MSK_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB05_MSK_ACTL: 0x690A B1_UDB05_MSK_ACTL: 0x6B0A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Interrupt Mask and Auxiliary Control

Bits	Name	Description
13	CNT_START	FIFO0 clear See Table 1-608.
12	INT_EN	(no description) See Table 1-611.
11	FIFO1_LVL	FIFO level See Table 1-610.
10	FIFO0_LVL	FIFO level See Table 1-610.
9	FIFO1_CLR	FIFO clear See Table 1-609.
8	FIFO0_CLR	FIFO clear See Table 1-609.
6:0	MSK[6:0]	Generic field for 7 bit working registers

Table 1-608. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

(continued)

Table 1-609. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-610. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-611. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.1045 B[0..3]_UDB06_MSK_ACTL

UDB06_MSK_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB06_MSK_ACTL: 0x690C B1_UDB06_MSK_ACTL: 0x6B0C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Interrupt Mask and Auxiliary Control

Bits	Name	Description
13	CNT_START	FIFO0 clear See Table 1-612.
12	INT_EN	(no description) See Table 1-615.
11	FIFO1_LVL	FIFO level See Table 1-614.
10	FIFO0_LVL	FIFO level See Table 1-614.
9	FIFO1_CLR	FIFO clear See Table 1-613.
8	FIFO0_CLR	FIFO clear See Table 1-613.
6:0	MSK[6:0]	Generic field for 7 bit working registers

Table 1-612. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

(continued)

Table 1-613. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-614. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-615. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.1046 B[0..3]_UDB07_MSK_ACTL

UDB07_MSK_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB07_MSK_ACTL: 0x690E B1_UDB07_MSK_ACTL: 0x6B0E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Interrupt Mask and Auxiliary Control

Bits	Name	Description
13	CNT_START	FIFO0 clear See Table 1-616.
12	INT_EN	(no description) See Table 1-619.
11	FIFO1_LVL	FIFO level See Table 1-618.
10	FIFO0_LVL	FIFO level See Table 1-618.
9	FIFO1_CLR	FIFO clear See Table 1-617.
8	FIFO0_CLR	FIFO clear See Table 1-617.
6:0	MSK[6:0]	Generic field for 7 bit working registers

Table 1-616. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

(continued)

Table 1-617. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-618. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-619. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.1047 B[0..3]_UDB08_MSK_ACTL

UDB08_MSK_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB08_MSK_ACTL: 0x6910 B1_UDB08_MSK_ACTL: 0x6B10

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Interrupt Mask and Auxiliary Control

Bits	Name	Description
13	CNT_START	FIFO0 clear See Table 1-620.
12	INT_EN	(no description) See Table 1-623.
11	FIFO1_LVL	FIFO level See Table 1-622.
10	FIFO0_LVL	FIFO level See Table 1-622.
9	FIFO1_CLR	FIFO clear See Table 1-621.
8	FIFO0_CLR	FIFO clear See Table 1-621.
6:0	MSK[6:0]	Generic field for 7 bit working registers

Table 1-620. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

(continued)

Table 1-621. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-622. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-623. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.1048 B[0..3]_UDB09_MSK_ACTL

UDB09_MSK_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB09_MSK_ACTL: 0x6912 B1_UDB09_MSK_ACTL: 0x6B12

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Interrupt Mask and Auxiliary Control

Bits	Name	Description
13	CNT_START	FIFO0 clear See Table 1-624.
12	INT_EN	(no description) See Table 1-627.
11	FIFO1_LVL	FIFO level See Table 1-626.
10	FIFO0_LVL	FIFO level See Table 1-626.
9	FIFO1_CLR	FIFO clear See Table 1-625.
8	FIFO0_CLR	FIFO clear See Table 1-625.
6:0	MSK[6:0]	Generic field for 7 bit working registers

Table 1-624. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

(continued)

Table 1-625. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-626. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-627. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.1049 B[0..3]_UDB10_MSK_ACTL

UDB10_MSK_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB10_MSK_ACTL: 0x6914 B1_UDB10_MSK_ACTL: 0x6B14

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Interrupt Mask and Auxiliary Control

Bits	Name	Description
13	CNT_START	FIFO0 clear See Table 1-628.
12	INT_EN	(no description) See Table 1-631.
11	FIFO1_LVL	FIFO level See Table 1-630.
10	FIFO0_LVL	FIFO level See Table 1-630.
9	FIFO1_CLR	FIFO clear See Table 1-629.
8	FIFO0_CLR	FIFO clear See Table 1-629.
6:0	MSK[6:0]	Generic field for 7 bit working registers

Table 1-628. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

(continued)

Table 1-629. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-630. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-631. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.1050 B[0..3]_UDB11_MSK_ACTL

UDB11_MSK_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB11_MSK_ACTL: 0x6916 B1_UDB11_MSK_ACTL: 0x6B16

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Interrupt Mask and Auxiliary Control

Bits	Name	Description
13	CNT_START	FIFO0 clear See Table 1-632.
12	INT_EN	(no description) See Table 1-635.
11	FIFO1_LVL	FIFO level See Table 1-634.
10	FIFO0_LVL	FIFO level See Table 1-634.
9	FIFO1_CLR	FIFO clear See Table 1-633.
8	FIFO0_CLR	FIFO clear See Table 1-633.
6:0	MSK[6:0]	Generic field for 7 bit working registers

Table 1-632. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

(continued)

Table 1-633. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-634. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-635. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.1051 B[0..3]_UDB12_MSK_ACTL

UDB12_MSK_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB12_MSK_ACTL: 0x6918

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Interrupt Mask and Auxiliary Control

Bits	Name	Description
13	CNT_START	FIFO0 clear See Table 1-636.
12	INT_EN	(no description) See Table 1-639.
11	FIFO1_LVL	FIFO level See Table 1-638.
10	FIFO0_LVL	FIFO level See Table 1-638.
9	FIFO1_CLR	FIFO clear See Table 1-637.
8	FIFO0_CLR	FIFO clear See Table 1-637.
6:0	MSK[6:0]	Generic field for 7 bit working registers

Table 1-636. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

(continued)

Table 1-637. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-638. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-639. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.1052 B[0..3]_UDB13_MSK_ACTL

UDB13_MSK_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB13_MSK_ACTL: 0x691A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Interrupt Mask and Auxiliary Control

Bits	Name	Description
13	CNT_START	FIFO0 clear See Table 1-640.
12	INT_EN	(no description) See Table 1-643.
11	FIFO1_LVL	FIFO level See Table 1-642.
10	FIFO0_LVL	FIFO level See Table 1-642.
9	FIFO1_CLR	FIFO clear See Table 1-641.
8	FIFO0_CLR	FIFO clear See Table 1-641.
6:0	MSK[6:0]	Generic field for 7 bit working registers

Table 1-640. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

(continued)

Table 1-641. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-642. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-643. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.1053 B[0..3]_UDB14_MSK_ACTL

UDB14_MSK_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB14_MSK_ACTL: 0x691C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Interrupt Mask and Auxiliary Control

Bits	Name	Description
13	CNT_START	FIFO0 clear See Table 1-644.
12	INT_EN	(no description) See Table 1-647.
11	FIFO1_LVL	FIFO level See Table 1-646.
10	FIFO0_LVL	FIFO level See Table 1-646.
9	FIFO1_CLR	FIFO clear See Table 1-645.
8	FIFO0_CLR	FIFO clear See Table 1-645.
6:0	MSK[6:0]	Generic field for 7 bit working registers

Table 1-644. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

(continued)

Table 1-645. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-646. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-647. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.1054 B[0..3]_UDB15_MSK_ACTL

UDB15_MSK_ACTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_UDB15_MSK_ACTL: 0x691E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R/W						
Retention	NA	RET						
Name	RSVD	MSK						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA		R/W	R/W	R/W	R/W	R/W	R/W
Retention	NA		RET	RET	RET	RET	RET	RET
Name	RSVD		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Interrupt Mask and Auxiliary Control

Bits	Name	Description
13	CNT_START	FIFO0 clear See Table 1-648.
12	INT_EN	(no description) See Table 1-651.
11	FIFO1_LVL	FIFO level See Table 1-650.
10	FIFO0_LVL	FIFO level See Table 1-650.
9	FIFO1_CLR	FIFO clear See Table 1-649.
8	FIFO0_CLR	FIFO clear See Table 1-649.
6:0	MSK[6:0]	Generic field for 7 bit working registers

Table 1-648. Bit field encoding: E_CNT_START

Value	Name	Description
1'b0	E_CNT_START0	Disable counter
1'b1	E_CNT_START1	Enable counter

(continued)

Table 1-649. Bit field encoding: E_FIFO_CLR

Value	Name	Description
1'b0	E_FIFO_CLR_0	Normal FIFO operation
1'b1	E_FIFO_CLR_1	Clear FIFO state

Table 1-650. Bit field encoding: E_FIFO_LVL

Value	Name	Description
1'b0	E_FIFO_LVL_0	FIFO LVL: input mode: FIFO not full; output mode: FIFO not empty
1'b1	E_FIFO_LVL_1	FIFO LVL: input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

Table 1-651. Bit field encoding: E_INT_EN

Value	Name	Description
1'b0	E_INT_EN0	Interrupt disabled
1'b1	E_INT_EN1	Interrupt enabled

1.3.1055 B[0..3]_UDB00_MC_00

UDB00_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB00_MC_00: 0x6940

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.1056 B[0..3]_UDB01_MC_00

UDB01_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB01_MC_00: 0x6942

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.1057 B[0..3]_UDB02_MC_00

UDB02_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB02_MC_00: 0x6944

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.1058 B[0..3]_UDB03_MC_00

UDB03_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB03_MC_00: 0x6946

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.1059 B[0..3]_UDB04_MC_00

UDB04_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB04_MC_00: 0x6948 B1_UDB04_MC_00: 0x6B48

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.1060 B[0..3]_UDB05_MC_00

UDB05_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB05_MC_00: 0x694A B1_UDB05_MC_00: 0x6B4A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.1061 B[0..3]_UDB06_MC_00

UDB06_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB06_MC_00: 0x694C B1_UDB06_MC_00: 0x6B4C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.1062 B[0..3]_UDB07_MC_00

UDB07_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB07_MC_00: 0x694E B1_UDB07_MC_00: 0x6B4E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.1063 B[0..3]_UDB08_MC_00

UDB08_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB08_MC_00: 0x6950 B1_UDB08_MC_00: 0x6B50

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.1064 B[0..3]_UDB09_MC_00

UDB09_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB09_MC_00: 0x6952 B1_UDB09_MC_00: 0x6B52

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.1065 B[0..3]_UDB10_MC_00

UDB10_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB10_MC_00: 0x6954 B1_UDB10_MC_00: 0x6B54

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.1066 B[0..3]_UDB11_MC_00

UDB11_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB11_MC_00: 0x6956 B1_UDB11_MC_00: 0x6B56

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.1067 B[0..3]_UDB12_MC_00

UDB12_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB12_MC_00: 0x6958

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.1068 B[0..3]_UDB13_MC_00

UDB13_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB13_MC_00: 0x695A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.1069 B[0..3]_UDB14_MC_00

UDB14_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB14_MC_00: 0x695C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.1070 B[0..3]_UDB15_MC_00

UDB15_MC_00

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

B0_UDB15_MC_00: 0x695E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	NONRET				NONRET			
Name	PLD1_MC_LS				PLD0_MC_LS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

PLD Macrocell reading

Bits	Name	Description
7:4	PLD1_MC_LS[3:0]	Read Macrocell
3:0	PLD0_MC_LS[3:0]	Read Macrocell

1.3.1071 PHUB_CFG

PHUB Configuration

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PHUB_CFG: 0x7000

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:1111111							R/W:0
HW Access	R							R
Retention	RET							RET
Name	spk_cpu_pri							cpu_clkdif

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:UUUUUUUU							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:0	R/W:0000000						
HW Access	R	R						
Retention	RET	RET						
Name	simple_pri	pri_int_en						

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:UUU			R:1	R/W:1	R/W:111		
HW Access	NA			R/W	R	R		
Retention	NA			RET	RET	RET		
Name	RSVD			dmac_idle	dmac_en	bus_timeout		

This is the general configuration register for the PHUB

Bits	Name	Description
28	dmac_idle	Indicates whether the DMAC is currently IDLE or not
27	dmac_en	Global DMAC enable
26:24	bus_timeout[2:0]	Specifies the number of wait states (!HREADY responses by an accessed peripheral) PHUB will allow before timing out the AHB transaction. On a bus timeout PHUB will act as if it received a positive HREADY from the peripheral then move onto the next natural transaction as it would normally. The BUS_TIMEOUT bit of the ERR register will be set upon detecting the timeout. See Table 1-652.
23	simple_pri	0: Grant allocation fairness algorithm enabled 1: Grant allocation fairness algorithm disabled; simple priority utilized

(continued)

22:16	pri_int_en[6:0]	0: Priority can not interrupt lower priority channels 1: Priority can interrupt lower priority channels Bits 22:16 correspond to priorities 6:0. Priority 7 is the lowest priority and thus can not interrupt yet lower priorities and therefore there is no bit for it.
7:1	spk_cpu_pri[6:0]	0: DMA priority spoke 1: CPU priority spoke Bits 15:1 correspond to spokes 15:1 respectively. SPK0 is not accessible by the CPU and thus no bit exists for it. The number of valid SPKxx_CPU_PRI bits is determined by the cfg_num_of_spk[4:0] input to PHUB; non-configured bits are hardwired to 0.
0	cpu_clkdif	0: CPU_CLOCK_EN assumed tied to 1; Performance Mode 1: CPU_CLOCK_EN assumed to modulate; Mixed Frequency Mode

Table 1-652. Bit field encoding: BUS_TIMEOUT_ENUM

Value	Name	Description
3'b000	Timeout_0	Disable bus timeout detection
3'b001	Timeout_1	8 wait states
3'b010	Timeout_2	16 wait states
3'b011	Timeout_3	32 wait states
3'b100	Timeout_4	64 wait states
3'b101	Timeout_5	128 wait states
3'b110	Timeout_6	256 wait states
3'b111	Timeout_7	511 wait states (default)

1.3.1072 PHUB_ERR

PHUB Error Detection

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

PHUB_ERR: 0x7004

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:UUUU				R/WOC:0	R/WOC:0	R/WOC:0	NA:U
HW Access	NA				R/W	R/W	R/W	NA
Retention	NA				NONRET	NONRET	NONRET	NA
Name	RSVD				periph_err	unpop_acc	bus_timeout	RSVD

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:UUUUUUUU							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:UUUUUUUU							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:UUUUUUUU							
HW Access	NA							
Retention	NA							
Name	RSVD							

PHUB detects the following errors: 1. Bus Timeout 2. Unpopulated address access 3. Peripheral AHB ERROR response If the error was detected as a result of a CPU access then PHUB will send an AHB ERROR response to the CPU. If the error was detected as a result of either a CPU or DMA access then PHUB will set the corresponding bit in the following ERR register.

Bits	Name	Description
3	periph_err	Set to 1 when a peripheral responds to a bus transaction with an AHB ERROR response. Cleared by writing a 1.
2	unpop_acc	Set to 1 when an access is attempted to an address that does not decode to any spoke HSEL. Cleared by writing a 1.
1	bus_timeout	Set to 1 when a bus timeout occurs. Cleared by writing a 1. Timeout values are determined by the BUS_TIMEOUT field in the PHUBCFG register.

1.3.1073 PHUB_ERR_ADR

PHUB Error Address

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

PHUB_ERR_ADR: 0x7008

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	NONRET							
Name	err_adr							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	NONRET							
Name	err_adr							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	NONRET							
Name	err_adr							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	NONRET							
Name	err_adr							

Contains the address that caused an error to trigger

Bits	Name	Description
31:0	err_adr[31:0]	Contains the value of the address that caused the error (limited to the BUS_TIMEOUT, UNPOP_ACC and PERIPH_ERR errors). If there are a succession of errors that occur before the CPU is able to clear the ERR register to all zeros, ERR_ADR will latch the address of the first error only.

1.3.1074 PHUB_CH[0..23]_BASIC_CFG

Channel Basic Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PHUB_CH0_BASIC_CFG: 0x7010
PHUB_CH1_BASIC_CFG: 0x7020
PHUB_CH2_BASIC_CFG: 0x7030
PHUB_CH3_BASIC_CFG: 0x7040
PHUB_CH4_BASIC_CFG: 0x7050
PHUB_CH5_BASIC_CFG: 0x7060
PHUB_CH6_BASIC_CFG: 0x7070
PHUB_CH7_BASIC_CFG: 0x7080
PHUB_CH8_BASIC_CFG: 0x7090
PHUB_CH9_BASIC_CFG: 0x70A0
PHUB_CH10_BASIC_CFG: 0x70B0
PHUB_CH11_BASIC_CFG: 0x70C0
PHUB_CH12_BASIC_CFG: 0x70D0
PHUB_CH13_BASIC_CFG: 0x70E0
PHUB_CH14_BASIC_CFG: 0x70F0
PHUB_CH15_BASIC_CFG: 0x7100
PHUB_CH16_BASIC_CFG: 0x7110
PHUB_CH17_BASIC_CFG: 0x7120
PHUB_CH18_BASIC_CFG: 0x7130
PHUB_CH19_BASIC_CFG: 0x7140
PHUB_CH20_BASIC_CFG: 0x7150
PHUB_CH21_BASIC_CFG: 0x7160
PHUB_CH22_BASIC_CFG: 0x7170
PHUB_CH23_BASIC_CFG: 0x7180

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:UU		R/W:0	R/W:0	R/W:000			R/W:0
HW Access	NA		R	R	R			R
Retention	NA		RET	RET	RET			RET
Name	RSVD		work_sep	rr_en	pri			en

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:UUUUUUUU							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:UUUUUUUU							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:UUUUUUUU							
HW Access	NA							
Retention	NA							

(continued)

Name	RSVD

Each channel will have the following basic configuration stored in gates inside PHUB.

Bits	Name	Description
5	work_sep	If a TD requires multiple bursts DMAC must remember where it left off between bursts while allowing interleaving other channels' bus access. It can either store the intermediate TD states on top of the current CHn_ORIG_TD0/1 of the TD chain, OR it can store it separately in a working area called CHn_SEP_TD0/1. The latter allows the original TD chain to be preserved. 0: Store the intermediate and final TD states on top of the original TD chain. Intermediate state storage allows the CPU to gauge progress of a particular TD. Final state storage allows the CPU to 'walk the chain' later and see what the final completion state of each TD was. 1: Store the intermediate TD states separately in CHn_SEP_TD0/1 to preserve the original TD chain. Intermediate state storage allows the CPU to gauge progress of a particular TD. Note the final state of each TD is not stored anywhere in this case. CHn_SEP_TD0/1 is stored in TDMEM and the address is: {00, CH_NUM[5:0], 000} In other words the slot in TDMEM that equals the channel number becomes reserved for DMAC's private use. Instead of processing the original TDs in place, DMAC will copy the original TDs to this separate working area and process them there. Because of this the separate working area is considered reserved and no real TDs should be stored there.
4	rr_en	Round-Robin enable RR_EN is only valid if the cfg_ch_recent_cnt_size[2:0] input to PHUB is not zero; otherwise RR_EN is hardwired to zero.
3:1	pri[2:0]	Channel priority; see DMA Arbiter section for description of channel priorities
0	en	0: Channel is disabled from accepting requests. This is the default state of the channel and allows the channel to be fully configured before enabling. This can also be used to stall a chain. If TD_ACTIVE=0 then clearing this bit will prevent any further DMA requests from being accepted by the channel until ENABLE is set again. If TD_ACTIVE=1 then DMAC will allow the current burst to finish naturally. Then when DMAC returns to the IDLE state it will prevent any further DMA requests from being accepted by the channel until ENABLE is set again. If a TD chain finishes due to NEXT_TD_PTR=0xFE then the ENABLE bit will be cleared automatically (this is not the case if the TD chain finishes due to NEXT_TD_PTR=0xFF). 1: Channel is enabled and will accept DMA requests for it. While the channel is enabled any other configuration information for the channel should NOT be altered to ensure graceful operation. This includes the channel's BASIC_CFG, BASIC_STATUS, CFG0/1, and associated TDs.

1.3.1075 PHUB_CH[0..23]_ACTION

Channel Action

Reset: System reset for retention flops [reset_all_retention]

Register : Address

PHUB_CH0_ACTION: 0x7014
PHUB_CH1_ACTION: 0x7024
PHUB_CH2_ACTION: 0x7034
PHUB_CH3_ACTION: 0x7044
PHUB_CH4_ACTION: 0x7054
PHUB_CH5_ACTION: 0x7064
PHUB_CH6_ACTION: 0x7074
PHUB_CH7_ACTION: 0x7084
PHUB_CH8_ACTION: 0x7094
PHUB_CH9_ACTION: 0x70A4
PHUB_CH10_ACTION: 0x70B4
PHUB_CH11_ACTION: 0x70C4
PHUB_CH12_ACTION: 0x70D4
PHUB_CH13_ACTION: 0x70E4
PHUB_CH14_ACTION: 0x70F4
PHUB_CH15_ACTION: 0x7104
PHUB_CH16_ACTION: 0x7114
PHUB_CH17_ACTION: 0x7124
PHUB_CH18_ACTION: 0x7134
PHUB_CH19_ACTION: 0x7144
PHUB_CH20_ACTION: 0x7154
PHUB_CH21_ACTION: 0x7164
PHUB_CH22_ACTION: 0x7174
PHUB_CH23_ACTION: 0x7184

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:UUUUU					R/WOSET:0	R/WOSET:0	R/WOSET:0
HW Access	NA					R/W	R/W	R/W
Retention	NA					RET	RET	RET
Name	RSVD					cpu_term_chain	cpu_term_td	cpu_req

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:UUUUUUUU							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:UUUUUUUU							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:UUUUUUUU							
HW Access	NA							

(continued)

Retention	NA
Name	RSVD

Each channel will have the following action register associated with it:

Bits	Name	Description
2	cpu_term_chain	Setting this bit causes the TD chain to terminate and the channel's ENABLE and CHAIN_ACTIVE bits to clear. If TD_ACTIVE=0 setting this bit will effectively create a request for the channel. When the request wins the DMAC will do some housekeeping associated with terminating a chain which includes clearing the channel's ENABLE, CHAIN_ACTIVE and CPU_TERM_CHAIN bits. If TD_ACTIVE=1 then DMAC will terminate the current burst as soon as any outstanding AHB requests are completed. The channel's ENABLE, CHAIN_ACTIVE and CPU_TERM_CHAIN bits will be cleared when the DMAC returns to the IDLE state.
1	cpu_term_td	Setting this bit causes the current TD to terminate regardless of the status of the XFRCNT associated with the TD. If TD_ACTIVE=0 the CPU_TERM_TD bit will just wait in the background. When the channel is eventually requested and serviced by DMAC the data burst will be preempted and the TD will complete just as if XFRCNT had expired. When the DMAC FSM returns to the IDLE state it will clear the CPU_TERM_TD bit. If TD_ACTIVE=1 then DMAC will terminate the current burst as soon as any outstanding AHB requests are completed. The TD will them complete just as if XFRCNT had expired. When the DMAC FSM returns to the IDLE state it will clear the CPU_TERM_TD bit.
0	cpu_req	Setting this bit creates a direct DMA request for the channel. If TD_ACTIVE=0 CPU_REQ will remain set until the request wins arbitration and is accepted by DMAC. This bit is cleared upon triggering the DMAC FSM from the IDLE state. If TD_ACTIVE=1 CPU_REQ will remain set and will apply to the next burst for the channel. The bit will essentially be ignored by DMAC and will be left alone so that it can trigger the next burst for the channel.

1.3.1076 PHUB_CH[0..23]_BASIC_STATUS

Channel Basic Status Register

Reset: Reset Signals Listed Below

Register : Address

PHUB_CH0_BASIC_STATUS: 0x7018

PHUB_CH1_BASIC_STATUS: 0x7028

PHUB_CH2_BASIC_STATUS: 0x7038

PHUB_CH3_BASIC_STATUS: 0x7048

PHUB_CH4_BASIC_STATUS: 0x7058

PHUB_CH5_BASIC_STATUS: 0x7068

PHUB_CH6_BASIC_STATUS: 0x7078

PHUB_CH7_BASIC_STATUS: 0x7088

PHUB_CH8_BASIC_STATUS: 0x7098

PHUB_CH9_BASIC_STATUS: 0x70A8

PHUB_CH10_BASIC_STATUS: 0x70B8

PHUB_CH11_BASIC_STATUS: 0x70C8

PHUB_CH12_BASIC_STATUS: 0x70D8

PHUB_CH13_BASIC_STATUS: 0x70E8

PHUB_CH14_BASIC_STATUS: 0x70F8

PHUB_CH15_BASIC_STATUS: 0x7108

PHUB_CH16_BASIC_STATUS: 0x7118

PHUB_CH17_BASIC_STATUS: 0x7128

PHUB_CH18_BASIC_STATUS: 0x7138

PHUB_CH19_BASIC_STATUS: 0x7148

PHUB_CH20_BASIC_STATUS: 0x7158

PHUB_CH21_BASIC_STATUS: 0x7168

PHUB_CH22_BASIC_STATUS: 0x7178

PHUB_CH23_BASIC_STATUS: 0x7188

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:1111				NA:UU		R:0	R:0
HW Access	R/W				NA		R/W	R/W
Retention	RET				NA		RET	RET
Name	rr_cnt				RSVD		td_active	chain_active

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:U	R/W:UUUUUUU						

(continued)

HW Access	NA	R/W
Retention	NA	RET
Name	RSVD	td_ptr

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:UUUUUUUU							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:UUUUUUUU							
HW Access	NA							
Retention	NA							
Name	RSVD							

Each channel will have the following status information stored in gates inside PHUB

Bits	Name	Description
14:8	td_ptr[6:0]	Address pointer to the current CHn_ORIG_TD0/1 in the chain. The CPU initializes this to the location of the first TD in the chain before enabling the channel. DMAC updates TD_PTR with NEXT_TD when it completes the current TD. This gives status to the CPU of how far along the chain is and where it is. The CHn_ORIG_TD0/1 chain is stored in TDMEM and DMAC accesses the current TD at: {TD_PTR[7:0], 000} The number of valid TD_PTR bits is determined by the cfg_ch_td_ptr_size[3:0] input to PHUB; non-configured bits are hardwired to 0. br] TD_PTR resets to the same value as the channel number.
7:4	rr_cnt[3:0]	Current state of the channel's Round-Robin counter. The lower the value the more recently the channel has won a DMA grant with zero meaning it won the last grant. 0: RR_CNT will be frozen on the terminal count (all ones) and therefore it will look as if the channel has never received a DMA grant which will give it an advantage over channels that do support Round-Robin. Put another way, when RR_EN=0 the channel is not subject to Round-Robin rules. 1: RR_CNT will reset each time the channel wins a DMA grant. It will increment each time any other channel wins a DMA grant. It will stop incrementing when it hits the terminal count (all ones). The number of valid RR_CNT bits is determined by the cfg_ch_recent_cnt_size[2:0] input to PHUB; non-configured bits are hardwired to 0.
1	td_active	0: channel is not currently being serviced by DMAC 1: channel is currently being serviced by DMAC
0	chain_active	0: TD chain is inactive; either no DMA requests have triggered a new chain or the previous chain has completed. 1: TD chain has been triggered by a DMA request

Reset Table

Reset Signal	Applicable Register Bit(s)
N/A	td_ptr[6:0]

(continued)

Reset Table

System reset for retention flops [reset_all_retention]	chain_active, td_active, rr_cnt[3:0]

1.3.1077 PHUB_CFGMEM[0..23]_CFG0

PHUB Channel Configuration Register 0

Reset: N/A

Register : Address

PHUB_CFGMEM0_CFG0: 0x7600
PHUB_CFGMEM1_CFG0: 0x7608
PHUB_CFGMEM2_CFG0: 0x7610
PHUB_CFGMEM3_CFG0: 0x7618
PHUB_CFGMEM4_CFG0: 0x7620
PHUB_CFGMEM5_CFG0: 0x7628
PHUB_CFGMEM6_CFG0: 0x7630
PHUB_CFGMEM7_CFG0: 0x7638
PHUB_CFGMEM8_CFG0: 0x7640
PHUB_CFGMEM9_CFG0: 0x7648
PHUB_CFGMEM10_CFG0: 0x7650
PHUB_CFGMEM11_CFG0: 0x7658
PHUB_CFGMEM12_CFG0: 0x7660
PHUB_CFGMEM13_CFG0: 0x7668
PHUB_CFGMEM14_CFG0: 0x7670
PHUB_CFGMEM15_CFG0: 0x7678
PHUB_CFGMEM16_CFG0: 0x7680
PHUB_CFGMEM17_CFG0: 0x7688
PHUB_CFGMEM18_CFG0: 0x7690
PHUB_CFGMEM19_CFG0: 0x7698
PHUB_CFGMEM20_CFG0: 0x76A0
PHUB_CFGMEM21_CFG0: 0x76A8
PHUB_CFGMEM22_CFG0: 0x76B0
PHUB_CFGMEM23_CFG0: 0x76B8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:U	R/W:UUUUUUU						
HW Access	R	R						
Retention	RET	RET						
Name	req_per_burst	burstcnt						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	termout1_sel				termout0_sel			

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:UUUU				R/W:UUUU			
HW Access	NA				R			
Retention	NA				RET			
Name	RSVD				termin_sel			

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUU							NA:U
HW Access	R							NA

(continued)

Retention	RET	NA
Name	burstcount_remain	RSVD

Each channel will have some configuration information stored in RAM, and this configuration information is called CHn_CFG0/1. CHn_CFG0/1 are stored in CFGMEM at {CH_NUM[5:0], 000}. Chn_CFG0/1 are described in detail below.

Bits	Name	Description
31:25	burstcount_remain[6:0]	These bits are reserved for use by the DMAC in storing the intermediate state of BURSTCNT in the event that the channel is interrupted mid-burst by a higher priority channel. These bits need to be preserved by SW only if the channel is active and interrupt-able. Otherwise SW can over-write these bits without concern, for instance when initially setting up the configuration for the channel.
19:16	termin_sel[3:0]	Selects 1 of the 16 TERMIN[15:0] inputs to PHUB for use in terminating a TD. Any active high strobe on the TERMIN signal will be positive edge detected and will cause the TD to terminate if TERMIN_EN is set in the TD. The TD will complete just as if XFRCNT expired.
15:12	termout1_sel[3:0]	Selects 1 of the 16 TERMOUT1[15:0] outputs from PHUB to be toggled upon completion of the current TD if TERMOUT1_EN is set in the TD. Because the frequency of the receiving logic for the TERMOUT1 signal is unknown by PHUB the signal is simply toggled and the receiving logic should be capable of detecting either a positive or negative edge on the TERMOUT1 signal and interpret either as the completion of the current TD.
11:8	termout0_sel[3:0]	Selects 1 of the 16 TERMOUT0[15:0] outputs from PHUB to be toggled upon completion of the current TD if TERMOUT0_EN is set in the TD. Because the frequency of the receiving logic for the TERMOUT0 signal is unknown by PHUB the signal is simply toggled and the receiving logic should be capable of detecting either a positive or negative edge on the TERMOUT0 signal and interpret either as the completion of the current TD.
7	req_per_burst	0: A DMA request is required to activate each TD in the chain. If the TD requires multiple bursts to complete then all subsequent bursts after the first burst will be automatically requested and carried out. DMAC will set the AUTO_BURST_WHOLE_TD request after completing each burst except the last. 1: A DMA request is required to activate each TD in the chain. If the TD requires multiple bursts to complete then all subsequent bursts after the first burst must also be individually requested.
6:0	burstcnt[6:0]	The data block moved by a TD can be broken up into small bursts. BURSTCNT[6:0] specifies the length of the small burst from 1 to 127 bytes. If BURSTCNT=0 this means do not break the data block into small bursts and instead burst the whole XFRCNT in one burst. The number of valid BURSTCNT bits is determined by the cfg_burstcnt_size[2:0] input to PHUB; non-configured bits are ignored by the DMAC.

1.3.1078 PHUB_CFGMEM[0..23]_CFG1

PHUB Channel Configuration Register 1

Reset: N/A

Register : Address

PHUB_CFGMEM0_CFG1: 0x7604
PHUB_CFGMEM1_CFG1: 0x760C
PHUB_CFGMEM2_CFG1: 0x7614
PHUB_CFGMEM3_CFG1: 0x761C
PHUB_CFGMEM4_CFG1: 0x7624
PHUB_CFGMEM5_CFG1: 0x762C
PHUB_CFGMEM6_CFG1: 0x7634
PHUB_CFGMEM7_CFG1: 0x763C
PHUB_CFGMEM8_CFG1: 0x7644
PHUB_CFGMEM9_CFG1: 0x764C
PHUB_CFGMEM10_CFG1: 0x7654
PHUB_CFGMEM11_CFG1: 0x765C
PHUB_CFGMEM12_CFG1: 0x7664
PHUB_CFGMEM13_CFG1: 0x766C
PHUB_CFGMEM14_CFG1: 0x7674
PHUB_CFGMEM15_CFG1: 0x767C
PHUB_CFGMEM16_CFG1: 0x7684
PHUB_CFGMEM17_CFG1: 0x768C
PHUB_CFGMEM18_CFG1: 0x7694
PHUB_CFGMEM19_CFG1: 0x769C
PHUB_CFGMEM20_CFG1: 0x76A4
PHUB_CFGMEM21_CFG1: 0x76AC
PHUB_CFGMEM22_CFG1: 0x76B4
PHUB_CFGMEM23_CFG1: 0x76BC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	RET							
Name	src_base_adr							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	RET							
Name	src_base_adr							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	RET							
Name	dst_base_adr							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	RET							

(continued)

Name	dst_base_adr

Each channel will have some configuration information stored in RAM, and this configuration information is called CHn_CFG0/1. CHn_CFG0/1 are stored in CFGMEM at {CH_NUM[5:0], 000}. Chn_CFG0/1 are described in detail below.

Bits	Name	Description
31:16	dst_base_adr[15:0]	Base address used for the destination address. Concatenates with DST_ADR[15:0] from the TD to form the full address.
15:0	src_base_adr[15:0]	Base address used for the source address. Concatenates with SRC_ADR[15:0] from the TD to form the full source address.

1.3.1079 PHUB_TDMEM[0..127]_ORIG_TD0

PHUB Original Transaction Descriptor 0

Reset: N/A

Register : Address

PHUB_TDMEM0_ORIG_TD0: 0x7800

PHUB_TDMEM1_ORIG_TD0: 0x7808

PHUB_TDMEM2_ORIG_TD0: 0x7810

PHUB_TDMEM3_ORIG_TD0: 0x7818

PHUB_TDMEM4_ORIG_TD0: 0x7820

PHUB_TDMEM5_ORIG_TD0: 0x7828

PHUB_TDMEM6_ORIG_TD0: 0x7830

PHUB_TDMEM7_ORIG_TD0: 0x7838

PHUB_TDMEM8_ORIG_TD0: 0x7840

PHUB_TDMEM9_ORIG_TD0: 0x7848

PHUB_TDMEM10_ORIG_TD0: 0x7850

PHUB_TDMEM11_ORIG_TD0: 0x7858

PHUB_TDMEM12_ORIG_TD0: 0x7860

PHUB_TDMEM13_ORIG_TD0: 0x7868

PHUB_TDMEM14_ORIG_TD0: 0x7870

PHUB_TDMEM15_ORIG_TD0: 0x7878

PHUB_TDMEM16_ORIG_TD0: 0x7880

PHUB_TDMEM17_ORIG_TD0: 0x7888

PHUB_TDMEM18_ORIG_TD0: 0x7890

PHUB_TDMEM19_ORIG_TD0: 0x7898

PHUB_TDMEM20_ORIG_TD0: 0x78A0

PHUB_TDMEM21_ORIG_TD0: 0x78A8

PHUB_TDMEM22_ORIG_TD0: 0x78B0

PHUB_TDMEM23_ORIG_TD0: 0x78B8

PHUB_TDMEM24_ORIG_TD0: 0x78C0

PHUB_TDMEM25_ORIG_TD0: 0x78C8

PHUB_TDMEM26_ORIG_TD0: 0x78D0

PHUB_TDMEM27_ORIG_TD0: 0x78D8

PHUB_TDMEM28_ORIG_TD0: 0x78E0

PHUB_TDMEM29_ORIG_TD0: 0x78E8

PHUB_TDMEM30_ORIG_TD0: 0x78F0

PHUB_TDMEM31_ORIG_TD0: 0x78F8

PHUB_TDMEM32_ORIG_TD0: 0x7900

(continued)

Register : Address

PHUB_TDMEM33_ORIG_TD0: 0x7908

PHUB_TDMEM34_ORIG_TD0: 0x7910

PHUB_TDMEM35_ORIG_TD0: 0x7918

PHUB_TDMEM36_ORIG_TD0: 0x7920

PHUB_TDMEM37_ORIG_TD0: 0x7928

PHUB_TDMEM38_ORIG_TD0: 0x7930

PHUB_TDMEM39_ORIG_TD0: 0x7938

PHUB_TDMEM40_ORIG_TD0: 0x7940

PHUB_TDMEM41_ORIG_TD0: 0x7948

PHUB_TDMEM42_ORIG_TD0: 0x7950

PHUB_TDMEM43_ORIG_TD0: 0x7958

PHUB_TDMEM44_ORIG_TD0: 0x7960

PHUB_TDMEM45_ORIG_TD0: 0x7968

PHUB_TDMEM46_ORIG_TD0: 0x7970

PHUB_TDMEM47_ORIG_TD0: 0x7978

PHUB_TDMEM48_ORIG_TD0: 0x7980

PHUB_TDMEM49_ORIG_TD0: 0x7988

PHUB_TDMEM50_ORIG_TD0: 0x7990

PHUB_TDMEM51_ORIG_TD0: 0x7998

PHUB_TDMEM52_ORIG_TD0: 0x79A0

PHUB_TDMEM53_ORIG_TD0: 0x79A8

PHUB_TDMEM54_ORIG_TD0: 0x79B0

PHUB_TDMEM55_ORIG_TD0: 0x79B8

PHUB_TDMEM56_ORIG_TD0: 0x79C0

PHUB_TDMEM57_ORIG_TD0: 0x79C8

PHUB_TDMEM58_ORIG_TD0: 0x79D0

PHUB_TDMEM59_ORIG_TD0: 0x79D8

PHUB_TDMEM60_ORIG_TD0: 0x79E0

PHUB_TDMEM61_ORIG_TD0: 0x79E8

PHUB_TDMEM62_ORIG_TD0: 0x79F0

PHUB_TDMEM63_ORIG_TD0: 0x79F8

PHUB_TDMEM64_ORIG_TD0: 0x7A00

PHUB_TDMEM65_ORIG_TD0: 0x7A08

PHUB_TDMEM66_ORIG_TD0: 0x7A10

PHUB_TDMEM67_ORIG_TD0: 0x7A18

PHUB_TDMEM68_ORIG_TD0: 0x7A20

(continued)

Register : Address

PHUB_TDMEM69_ORIG_TD0: 0x7A28
PHUB_TDMEM70_ORIG_TD0: 0x7A30
PHUB_TDMEM71_ORIG_TD0: 0x7A38
PHUB_TDMEM72_ORIG_TD0: 0x7A40
PHUB_TDMEM73_ORIG_TD0: 0x7A48
PHUB_TDMEM74_ORIG_TD0: 0x7A50
PHUB_TDMEM75_ORIG_TD0: 0x7A58
PHUB_TDMEM76_ORIG_TD0: 0x7A60
PHUB_TDMEM77_ORIG_TD0: 0x7A68
PHUB_TDMEM78_ORIG_TD0: 0x7A70
PHUB_TDMEM79_ORIG_TD0: 0x7A78
PHUB_TDMEM80_ORIG_TD0: 0x7A80
PHUB_TDMEM81_ORIG_TD0: 0x7A88
PHUB_TDMEM82_ORIG_TD0: 0x7A90
PHUB_TDMEM83_ORIG_TD0: 0x7A98
PHUB_TDMEM84_ORIG_TD0: 0x7AA0
PHUB_TDMEM85_ORIG_TD0: 0x7AA8
PHUB_TDMEM86_ORIG_TD0: 0x7AB0
PHUB_TDMEM87_ORIG_TD0: 0x7AB8
PHUB_TDMEM88_ORIG_TD0: 0x7AC0
PHUB_TDMEM89_ORIG_TD0: 0x7AC8
PHUB_TDMEM90_ORIG_TD0: 0x7AD0
PHUB_TDMEM91_ORIG_TD0: 0x7AD8
PHUB_TDMEM92_ORIG_TD0: 0x7AE0
PHUB_TDMEM93_ORIG_TD0: 0x7AE8
PHUB_TDMEM94_ORIG_TD0: 0x7AF0
PHUB_TDMEM95_ORIG_TD0: 0x7AF8
PHUB_TDMEM96_ORIG_TD0: 0x7B00
PHUB_TDMEM97_ORIG_TD0: 0x7B08
PHUB_TDMEM98_ORIG_TD0: 0x7B10
PHUB_TDMEM99_ORIG_TD0: 0x7B18
PHUB_TDMEM100_ORIG_TD0: 0x7B20
PHUB_TDMEM101_ORIG_TD0: 0x7B28
PHUB_TDMEM102_ORIG_TD0: 0x7B30
PHUB_TDMEM103_ORIG_TD0: 0x7B38
PHUB_TDMEM104_ORIG_TD0: 0x7B40

(continued)

Register : Address

PHUB_TDMEM105_ORIG_TD0: 0x7B48

PHUB_TDMEM106_ORIG_TD0: 0x7B50

PHUB_TDMEM107_ORIG_TD0: 0x7B58

PHUB_TDMEM108_ORIG_TD0: 0x7B60

PHUB_TDMEM109_ORIG_TD0: 0x7B68

PHUB_TDMEM110_ORIG_TD0: 0x7B70

PHUB_TDMEM111_ORIG_TD0: 0x7B78

PHUB_TDMEM112_ORIG_TD0: 0x7B80

PHUB_TDMEM113_ORIG_TD0: 0x7B88

PHUB_TDMEM114_ORIG_TD0: 0x7B90

PHUB_TDMEM115_ORIG_TD0: 0x7B98

PHUB_TDMEM116_ORIG_TD0: 0x7BA0

PHUB_TDMEM117_ORIG_TD0: 0x7BA8

PHUB_TDMEM118_ORIG_TD0: 0x7BB0

PHUB_TDMEM119_ORIG_TD0: 0x7BB8

PHUB_TDMEM120_ORIG_TD0: 0x7BC0

PHUB_TDMEM121_ORIG_TD0: 0x7BC8

PHUB_TDMEM122_ORIG_TD0: 0x7BD0

PHUB_TDMEM123_ORIG_TD0: 0x7BD8

PHUB_TDMEM124_ORIG_TD0: 0x7BE0

PHUB_TDMEM125_ORIG_TD0: 0x7BE8

PHUB_TDMEM126_ORIG_TD0: 0x7BF0

PHUB_TDMEM127_ORIG_TD0: 0x7BF8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	xfrcnt							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:UUUU				R/W:UUUU			
HW Access	NA				R/W			
Retention	NA				RET			
Name	RSVD				xfrcnt			

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							

(continued)

HW Access	R
Retention	RET
Name	next_td_ptr

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U
HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	swap_en	swap_size	auto_exec_next	termin_en	termout1_en	termout0_en	inc_dst_adr	inc_src_adr

Each channel will have a TD chain (as short as one TD in length) that provides instructions to the DMAC for carrying out a DMA sequence for the channel. This is described in greater detail in the 'TD Chains' section to follow. The TD chain is comprised of one or more CHn_ORIG_TD0/1 TDs. DMAC accesses the CHn_ORIG_TD0/1 chain from TDMEM and the address in TDMEM of the current TD in the chain is {TD_PTR[7:0], 000}. TD_PTR for the first TD in a chain is initialized by the CPU. As the chain progresses through TDs the TD_PTR will be automatically updated by DMAC to reflect the current TD being accessed in the chain. CHn_ORIG_TD0/1 are described in detail below.

Bits	Name	Description
31	swap_en	0: Do not perform endian swap 1: Perform endian swap. BURSTCNT and XFRCNT must be an integer multiple of SWAP_SIZE.
30	swap_size	Only valid if SWAP_EN=1. 0: Swap size = 2 bytes, meaning every 2 bytes are endian swapped during the DMA transfer. 1: Swap size = 4 bytes, meaning every 4 bytes are endian swapped during the DMA transfer.
29	auto_exec_next	0: The next TD in the chain requires a CPU_REQ or peripheral request in order to trigger 1: The next TD in the chain will trigger automatically when the current TD completes. The DMAC will create an AUTO_EXEC_NEXT_TD request for the channel when it completes the current TD.
28	termin_en	0: Do not terminate this TD based on a TERMIN signal. 1: Terminate this TD if a positive edge on the TERMIN signal selected by TERMIN_SEL is detected. Any ongoing burst will terminate as soon as any outstanding AHB requests have been completed. The TD will then complete just as if XFRCNT expired.
27	termout1_en	0: Do not toggle a TERMOUT1 signal when this TD completes 1: When this TD completes the TERMOUT1 signal selected by TERMOUT1_SEL will toggle. Because the frequency of the receiving logic for the TERMOUT1 signal is unknown by PHUB the signal is simply toggled and the receiving logic should be capable of detecting either a positive or negative edge on the TERMOUT1 signal and interpret either as the completion of the current TD.
26	termout0_en	0: Do not toggle a TERMOUT0 signal when the TD completes 1: When this TD completes the TERMOUT0 signal selected by TERMOUT0_SEL will toggle. Because the frequency of the receiving logic for the TERMOUT0 signal is unknown by PHUB the signal is simply toggled and the receiving logic should be capable of detecting either a positive or negative edge on the TERMOUT0 signal and interpret either as the completion of the current TD.
25	inc_dst_adr	0: Freeze DST_ADR throughout the burst 1: Increment DST_ADR according to the size of each data transaction in the burst
24	inc_src_adr	0: Freeze SRC_ADR throughout the burst 1: Increment SRC_ADR according to the size of each data transaction in the burst

(continued)

23:16	next_td_ptr[7:0]	Specifies the next TD to be executed in the chain when this TD completes. When this TD completes the value of NEXT_TD_PTR is copied into the TD_PTR status register to allow the CPU to see where in the chain the channel is. If NEXT_TD_PTR=0xFE or 0xFF then this is the last TD in the chain. When the last TD in a chain completes DMAC will clear CHAIN_ACTIVE and if NEXT_TD_PTR=0xFE then ENABLE will clear as well.
11:0	xfrcnt[11:0]	Transfer count in bytes from 1 to 4KB-1, or indefinite transfer count if set to 0. 1. Setting XFRCNT to 0: This means transfer count is not used to terminate the TD. An indefinite amount of data can be transferred in this mode. The TD must be terminated either by TERMIN, CPU_TERM_TD or CPU_TERM_CHAIN. Data movement is broken into bursts according to BURSTCNT. Note in the special case where both XFRCNT and BURSTCNT are 0 data will be transferred indefinitely and without interruption. 2. Setting XFRCNT to non-0: This means the XFRCNT is used to determine how much data will be transferred (1 to 4KB-1). If BURSTCNT=0 then DMAC will transfer the entire XFRCNT worth of data in one burst. If BURSTCNT is not 0 and BURSTCNT represents a value that is greater than or equal to XFRCNT then DMAC will transfer the entire XFRCNT worth of data in one burst. If BURSTCNT is not 0 and BURSTCNT represents a value that is less than XFRCNT then DMAC will break the data movement into multiple bursts as dictated by BURSTCNT. See the description for the REQ_PER_BURST bit for how subsequent bursts are triggered. At any point the TD can terminate before exhausting the XFRCNT due to TERMIN, CPU_TERM_TD or CPU_TERM_CHAIN. When DMAC updates the TD (whether it's the CHn_ORIG_TD0/1 or CHn_SEP_TD0/1) at the end of a burst it will update the XFRCNT to reflect the newly decremented value based on the number of bytes that were transferred in the burst. The number of valid XFRCNT bits is determined by the cfg_xfrcnt_size[4:0] input to PHUB; non-configured bits are ignored by the DMAC.

1.3.1080 PHUB_TDMEM[0..127]_ORIG_TD1

PHUB Original Transaction Descriptor 0

Reset: N/A

Register : Address

PHUB_TDMEM0_ORIG_TD1: 0x7804

PHUB_TDMEM1_ORIG_TD1: 0x780C

PHUB_TDMEM2_ORIG_TD1: 0x7814

PHUB_TDMEM3_ORIG_TD1: 0x781C

PHUB_TDMEM4_ORIG_TD1: 0x7824

PHUB_TDMEM5_ORIG_TD1: 0x782C

PHUB_TDMEM6_ORIG_TD1: 0x7834

PHUB_TDMEM7_ORIG_TD1: 0x783C

PHUB_TDMEM8_ORIG_TD1: 0x7844

PHUB_TDMEM9_ORIG_TD1: 0x784C

PHUB_TDMEM10_ORIG_TD1: 0x7854

PHUB_TDMEM11_ORIG_TD1: 0x785C

PHUB_TDMEM12_ORIG_TD1: 0x7864

PHUB_TDMEM13_ORIG_TD1: 0x786C

PHUB_TDMEM14_ORIG_TD1: 0x7874

PHUB_TDMEM15_ORIG_TD1: 0x787C

PHUB_TDMEM16_ORIG_TD1: 0x7884

PHUB_TDMEM17_ORIG_TD1: 0x788C

PHUB_TDMEM18_ORIG_TD1: 0x7894

PHUB_TDMEM19_ORIG_TD1: 0x789C

PHUB_TDMEM20_ORIG_TD1: 0x78A4

PHUB_TDMEM21_ORIG_TD1: 0x78AC

PHUB_TDMEM22_ORIG_TD1: 0x78B4

PHUB_TDMEM23_ORIG_TD1: 0x78BC

PHUB_TDMEM24_ORIG_TD1: 0x78C4

PHUB_TDMEM25_ORIG_TD1: 0x78CC

PHUB_TDMEM26_ORIG_TD1: 0x78D4

PHUB_TDMEM27_ORIG_TD1: 0x78DC

PHUB_TDMEM28_ORIG_TD1: 0x78E4

PHUB_TDMEM29_ORIG_TD1: 0x78EC

PHUB_TDMEM30_ORIG_TD1: 0x78F4

PHUB_TDMEM31_ORIG_TD1: 0x78FC

PHUB_TDMEM32_ORIG_TD1: 0x7904

(continued)

Register : Address

PHUB_TDMEM33_ORIG_TD1: 0x790C
PHUB_TDMEM34_ORIG_TD1: 0x7914
PHUB_TDMEM35_ORIG_TD1: 0x791C
PHUB_TDMEM36_ORIG_TD1: 0x7924
PHUB_TDMEM37_ORIG_TD1: 0x792C
PHUB_TDMEM38_ORIG_TD1: 0x7934
PHUB_TDMEM39_ORIG_TD1: 0x793C
PHUB_TDMEM40_ORIG_TD1: 0x7944
PHUB_TDMEM41_ORIG_TD1: 0x794C
PHUB_TDMEM42_ORIG_TD1: 0x7954
PHUB_TDMEM43_ORIG_TD1: 0x795C
PHUB_TDMEM44_ORIG_TD1: 0x7964
PHUB_TDMEM45_ORIG_TD1: 0x796C
PHUB_TDMEM46_ORIG_TD1: 0x7974
PHUB_TDMEM47_ORIG_TD1: 0x797C
PHUB_TDMEM48_ORIG_TD1: 0x7984
PHUB_TDMEM49_ORIG_TD1: 0x798C
PHUB_TDMEM50_ORIG_TD1: 0x7994
PHUB_TDMEM51_ORIG_TD1: 0x799C
PHUB_TDMEM52_ORIG_TD1: 0x79A4
PHUB_TDMEM53_ORIG_TD1: 0x79AC
PHUB_TDMEM54_ORIG_TD1: 0x79B4
PHUB_TDMEM55_ORIG_TD1: 0x79BC
PHUB_TDMEM56_ORIG_TD1: 0x79C4
PHUB_TDMEM57_ORIG_TD1: 0x79CC
PHUB_TDMEM58_ORIG_TD1: 0x79D4
PHUB_TDMEM59_ORIG_TD1: 0x79DC
PHUB_TDMEM60_ORIG_TD1: 0x79E4
PHUB_TDMEM61_ORIG_TD1: 0x79EC
PHUB_TDMEM62_ORIG_TD1: 0x79F4
PHUB_TDMEM63_ORIG_TD1: 0x79FC
PHUB_TDMEM64_ORIG_TD1: 0x7A04
PHUB_TDMEM65_ORIG_TD1: 0x7A0C
PHUB_TDMEM66_ORIG_TD1: 0x7A14
PHUB_TDMEM67_ORIG_TD1: 0x7A1C
PHUB_TDMEM68_ORIG_TD1: 0x7A24

(continued)

Register : Address

PHUB_TDMEM69_ORIG_TD1: 0x7A2C
PHUB_TDMEM70_ORIG_TD1: 0x7A34
PHUB_TDMEM71_ORIG_TD1: 0x7A3C
PHUB_TDMEM72_ORIG_TD1: 0x7A44
PHUB_TDMEM73_ORIG_TD1: 0x7A4C
PHUB_TDMEM74_ORIG_TD1: 0x7A54
PHUB_TDMEM75_ORIG_TD1: 0x7A5C
PHUB_TDMEM76_ORIG_TD1: 0x7A64
PHUB_TDMEM77_ORIG_TD1: 0x7A6C
PHUB_TDMEM78_ORIG_TD1: 0x7A74
PHUB_TDMEM79_ORIG_TD1: 0x7A7C
PHUB_TDMEM80_ORIG_TD1: 0x7A84
PHUB_TDMEM81_ORIG_TD1: 0x7A8C
PHUB_TDMEM82_ORIG_TD1: 0x7A94
PHUB_TDMEM83_ORIG_TD1: 0x7A9C
PHUB_TDMEM84_ORIG_TD1: 0x7AA4
PHUB_TDMEM85_ORIG_TD1: 0x7AAC
PHUB_TDMEM86_ORIG_TD1: 0x7AB4
PHUB_TDMEM87_ORIG_TD1: 0x7ABC
PHUB_TDMEM88_ORIG_TD1: 0x7AC4
PHUB_TDMEM89_ORIG_TD1: 0x7ACC
PHUB_TDMEM90_ORIG_TD1: 0x7AD4
PHUB_TDMEM91_ORIG_TD1: 0x7ADC
PHUB_TDMEM92_ORIG_TD1: 0x7AE4
PHUB_TDMEM93_ORIG_TD1: 0x7AEC
PHUB_TDMEM94_ORIG_TD1: 0x7AF4
PHUB_TDMEM95_ORIG_TD1: 0x7AFC
PHUB_TDMEM96_ORIG_TD1: 0x7B04
PHUB_TDMEM97_ORIG_TD1: 0x7B0C
PHUB_TDMEM98_ORIG_TD1: 0x7B14
PHUB_TDMEM99_ORIG_TD1: 0x7B1C
PHUB_TDMEM100_ORIG_TD1: 0x7B24
PHUB_TDMEM101_ORIG_TD1: 0x7B2C
PHUB_TDMEM102_ORIG_TD1: 0x7B34
PHUB_TDMEM103_ORIG_TD1: 0x7B3C
PHUB_TDMEM104_ORIG_TD1: 0x7B44

(continued)

Register : Address

PHUB_TDMEM105_ORIG_TD1: 0x7B4C

PHUB_TDMEM106_ORIG_TD1: 0x7B54

PHUB_TDMEM107_ORIG_TD1: 0x7B5C

PHUB_TDMEM108_ORIG_TD1: 0x7B64

PHUB_TDMEM109_ORIG_TD1: 0x7B6C

PHUB_TDMEM110_ORIG_TD1: 0x7B74

PHUB_TDMEM111_ORIG_TD1: 0x7B7C

PHUB_TDMEM112_ORIG_TD1: 0x7B84

PHUB_TDMEM113_ORIG_TD1: 0x7B8C

PHUB_TDMEM114_ORIG_TD1: 0x7B94

PHUB_TDMEM115_ORIG_TD1: 0x7B9C

PHUB_TDMEM116_ORIG_TD1: 0x7BA4

PHUB_TDMEM117_ORIG_TD1: 0x7BAC

PHUB_TDMEM118_ORIG_TD1: 0x7BB4

PHUB_TDMEM119_ORIG_TD1: 0x7BBC

PHUB_TDMEM120_ORIG_TD1: 0x7BC4

PHUB_TDMEM121_ORIG_TD1: 0x7BCC

PHUB_TDMEM122_ORIG_TD1: 0x7BD4

PHUB_TDMEM123_ORIG_TD1: 0x7BDC

PHUB_TDMEM124_ORIG_TD1: 0x7BE4

PHUB_TDMEM125_ORIG_TD1: 0x7BEC

PHUB_TDMEM126_ORIG_TD1: 0x7BF4

PHUB_TDMEM127_ORIG_TD1: 0x7BFC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	src_adr							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	src_adr							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							

(continued)

HW Access	R/W
Retention	RET
Name	dst_adr

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dst_adr							

Each channel will have a TD chain (as short as one TD in length) that provides instructions to the DMAC for carrying out a DMA sequence for the channel. This is described in greater detail in the 'TD Chains' section to follow. The TD chain is comprised of one or more CHn_ORIG_TD0/1 TDs. DMAC accesses the CHn_ORIG_TD0/1 chain from TDMEM and the address in TDMEM of the current TD in the chain is {TD_PTR[7:0], 000}. TD_PTR for the first TD in a chain is initialized by the CPU. As the chain progresses through TDs the TD_PTR will be automatically updated by DMAC to reflect the current TD being accessed in the chain. CHn_ORIG_TD0/1 are described in detail below.

Bits	Name	Description
31:16	dst_adr[15:0]	Specifies the lower portion of the full destination address by concatenating with DST_BASE_ADR from CHn_CFG1. Can be incremented or not depending on the setting of INC_DST_ADR. Only DST_ADR will increment; DST_BASE_ADR will remain static. Therefore, separate TDs should be used to cross 64KB address boundaries. If INC_DST_ADR=1 then when DMAC updates the TD (whether it's the CHn_ORIG_TD0/1 or CHn_SEP_TD0/1) at the end of a burst it will update DST_ADR to reflect the newly incremented value based on the number of bytes that were transferred to the destination during the burst.
15:0	src_adr[15:0]	Specifies the lower portion of the full source address by concatenating with SRC_BASE_ADR from CHn_CFG1. Can be incremented or not depending on the setting of INC_SRC_ADR. Only SRC_ADR will increment; SRC_BASE_ADR will remain static. Therefore, separate TDs should be used to cross 64KB address boundaries. If INC_SRC_ADR=1 then when DMAC updates the TD (whether it's the CHn_ORIG_TD0/1 or CHn_SEP_TD0/1) at the end of a burst it will update SRC_ADR to reflect the newly incremented value based on the number of bytes that were transferred from the source during the burst.

1.3.1081 EE_DATA[0..2047]

EEPROM Memory

Reset: N/A

Register : Address

EE_DATA: 0x8000-0x87FF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	data							

Bits	Name	Description
7:0	data[7:0]	(no description)

1.3.1082 CAN[0..0]_CSR_INT_SR

INT_SR

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

CAN0_CSR_INT_SR: 0xA000

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0	NA:00	
HW Access	R/W	R/W	R/W	R/W	R/W	R/W	NA	
Retention	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET	NA	
Name	form_err	ack_err	stuff_err	bit_err	ovr_load	arb_loss	RSVD	

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:000			R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0
HW Access	NA			R/W	R/W	R/W	R/W	R/W
Retention	NA			NONRET	NONRET	NONRET	NONRET	NONRET
Name	RSVD			rx_msg	tx_msg	rx_msg_loss	bus_off	crc_err

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

The interrupt status register stores internal interrupt events. Once a bit is set it remains set until it is cleared by writing a '1' to it. The interrupt enable register has no effect on the interrupt status register. A pending interrupt occurs when the flag is set to '1'. To acknowledge an interrupt, set the flag to '1'

Bits	Name	Description
12	rx_msg	Msg Recieved
11	tx_msg	Tx msg Sent
10	rx_msg_loss	Rx msg loss Interrupt
9	bus_off	Bus Off State
8	crc_err	CRC Error Interrupt

(continued)

7	form_err	Form Error Interrupt
6	ack_err	Ack Error Interrupt
5	stuff_err	Stuff Error Interrupt
4	bit_err	Bit Error Interrupt
3	ovr_load	Overload Interrupt
2	arb_loss	Arbitration Loss

1.3.1083 CAN[0..0]_CSR_INT_EN

INT_EN

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

CAN0_CSR_INT_EN: 0xA004

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	NA:0	R/W:0
HW Access	R	R	R	R	R	R	NA	R
Retention	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET	NA	NONRET
Name	form_err	ack_err	stuff_err	bit_err	ovr_load	arb_loss	RSVD	int_ebl

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA			R	R	R	R	R
Retention	NA			NONRET	NONRET	NONRET	NONRET	NONRET
Name	RSVD			rx_msg	tx_msg	rx_msg_loss	bus_off	crc_err

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

A particular interrupt source is enabled by setting its respective flag to 1

Bits	Name	Description
12	rx_msg	Msg Recived
11	tx_msg	Tx Msg sent Interrupt
10	rx_msg_loss	Rx Msg Loss Interrupt Enable
9	bus_off	Busoff State Interrupt Enable
8	crc_err	CRC Error Interrupt Enable
7	form_err	Form Error Interrupt Enable
6	ack_err	Ack Error Interrupt Enable

(continued)

5	stuff_err	Stuff Error Interrupt Enable
4	bit_err	Bit Error Interrupt Enable
3	ovr_load	Overload Interrupt Enable
2	arb_loss	Arbitration Loss Interrupt Enable
0	int_ebl	Global Interrupt enable Flag

1.3.1084 CAN[0..0]_CSR_BUF_SR

BUF_SR

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

CAN0_CSR_BUF_SR: 0xA008

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0	R:0	R:0	R:0	R:0	R:0	R:0	R:0
HW Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Retention	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET
Name	rx_msg7	rx_msg6	rx_msg5	rx_msg4	rx_msg3	rx_msg2	rx_msg1	rx_msg0

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:0	R:0	R:0	R:0	R:0	R:0	R:0	R:0
HW Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Retention	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET
Name	rx_msg15	rx_msg14	rx_msg13	rx_msg12	rx_msg11	rx_msg10	rx_msg9	rx_msg8

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:0	R:0	R:0	R:0	R:0	R:0	R:0	R:0
HW Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Retention	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET
Name	tx_msg7	tx_msg6	tx_msg5	tx_msg4	tx_msg3	tx_msg2	tx_msg1	tx_msg0

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

These status indicators bundle the respective flags from all RxMessage and TxMessage buffers. Note All flags are read only. To acknowledge a MsgAv flag, the CPU must write to the respective RxMessage buffer.

Bits	Name	Description
23	tx_msg7	Tx req Pending for Tx Msg7
22	tx_msg6	Tx req Pending for Tx Msg6
21	tx_msg5	Tx req Pending for Tx Msg5
20	tx_msg4	Tx req Pending for Tx Msg4
19	tx_msg3	Tx req Pending for Tx Msg3
18	tx_msg2	Tx req Pending for Tx Msg2
17	tx_msg1	Tx req Pending for Tx Msg1

(continued)

16	tx_msg0	Tx req Pending for Tx Msg0
15	rx_msg15	Rx Msg15 Available
14	rx_msg14	Rx Msg14 Available
13	rx_msg13	Rx Msg13 Available
12	rx_msg12	Rx Msg12 Available
11	rx_msg11	Rx Msg11 Available
10	rx_msg10	Rx Msg10 Available
9	rx_msg9	Rx Msg9 Available
8	rx_msg8	Rx Msg8 Available
7	rx_msg7	Rx Msg7 Available
6	rx_msg6	Rx Msg6 Available
5	rx_msg5	Rx Msg5 Available
4	rx_msg4	Rx Msg4 Available
3	rx_msg3	Rx Msg3 Available
2	rx_msg2	Rx Msg2 Available
1	rx_msg1	Rx Msg1 Available
0	rx_msg0	Rx Msg0 Available

1.3.1085 CAN[0..0]_CSR_ERR_SR

ERR_SR

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

CAN0_CSR_ERR_SR: 0xA00C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	NONRET							
Name	tx_err_cnt							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	NONRET							
Name	rx_err_cnt							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:0000				R:0	R:0	R:00	
HW Access	NA				R/W	R/W	R/W	
Retention	NA				NONRET	NONRET	NONRET	
Name	RSVD				rxgte96	txgte96	err_state	

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Status indicators are provided to report the CAN controller error state, receive error count, and transmit error count. Special flags report error counter values equal to or in excess of 96 errors are available to indicate heavily disturbed bus situations. The transmitter error counter according to the CAN standard. When it is greater than 255 Decomal, it is fixed at 255 Decimal.

Bits	Name	Description
19	rxgte96	Rx Error Count is greater or equal to 96 Decimal
18	txgte96	Tx Error Count is greater or equal to 96 Decimal
17:16	err_state[1:0]	Error State of CAN node, 00 error active, 01 error passive, 1x bus off
15:8	rx_err_cnt[7:0]	Rx error Count. When in bus-off state,this counter is used to count 128 groups of 11 recessive bits
7:0	tx_err_cnt[7:0]	Tx error Count

1.3.1086 CAN[0..0]_CSR_CMD

CMD

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

CAN0_CSR_CMD: 0xA010

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	NA:0	R/W:0	R/W:0
HW Access	NA				R	NA	R	R/W
Retention	NA				NONRET	NA	NONRET	NONRET
Name	RSVD				sram_test	RSVD	listen	run_stop

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

The CAN can be used in different operating mode,by disabling transmitting data,it is possible to use the CAN in listen only mode,enabling feature such as automatic bit rate detection,SRAM Test Mode

Bits	Name	Description
3	sram_test	SRAM test Mode. 0 Normal operation, 1 Enable SRAM test mode
1	listen	Listen only mode. 0 Active, 1 CAN listen only
0	run_stop	Run/Stop mode. 0 Sets the CAN controller to stop mode. Returns '1' when stopped, 1 Sets the CAN controller to run mode. Returns '1' when running

1.3.1087 CAN[0..0]_CSR_CFG

CFG

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

CAN0_CSR_CFG: 0xA014

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:000			R/W:0	R/W:00		R/W:0	R/W:0
HW Access	R			R	R		R	R
Retention	NONRET			NONRET	NONRET		NONRET	NONRET
Name	cfg_tseg2			auto_rst	cfg_sjw		sampling_mode	edge_mode

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:000			R/W:0	R/W:0000			
HW Access	NA			R	R			
Retention	NA			NONRET	NONRET			
Name	RSVD			cfg_arbiter	cfg_tseg1			

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	cfg_bitrate							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:0	R/W:0000000						
HW Access	NA	R						
Retention	NA	NONRET						
Name	RSVD	cfg_bitrate						

CAN module has to be configured prior to use,this register define the effective CAN data rate,CAN data synchronization,message buffer arbitration

Bits	Name	Description
30:16	cfg_bitrate[14:0]	CAN configuration Bit rate. 0 equals 1 clock cycle, 1 equals 2 clock cycles, ..., 32767 equals 32768 clock cycles
12	cfg_arbiter	Tx buffer Arbiter. 0 Round robin arbitration, 1 Fixed priority arbitration
11:8	cfg_tseg1[3:0]	Length of time segment1
7:5	cfg_tseg2[2:0]	Length of time segment2
4	auto_rst	auto_restart. 0 After bus-off, the CAN must be restarted 'by hand'. This is the recommended setting, 1 After bus-off, the CAN is restarting automatically after 128 groups of 11 recessive bits

(continued)

3:2	cfg_sjw[1:0]	Synchronization Jump Width
1	sampling_mode	CAN bus Bit sampling. 0 One sampling point is used in the receiver path, 1 Three sampling points with majority decision are used
0	edge_mode	CAN bus synchronization logic. 0 Edge from 'R' to 'D' is used for synchronization, 1 Both edges are used

1.3.1088 CAN[0..0]_TX[0..7]_CMD

TXCMD

Reset: N/A

Register : Address

CAN0_TX0_CMD: 0xA020

CAN0_TX1_CMD: 0xA030

CAN0_TX2_CMD: 0xA040

CAN0_TX3_CMD: 0xA050

CAN0_TX4_CMD: 0xA060

CAN0_TX5_CMD: 0xA070

CAN0_TX6_CMD: 0xA080

CAN0_TX7_CMD: 0xA090

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				W:U	R:U	R:U	R:U
HW Access	NA				R	R/W	R/W	R/W
Retention	NA				NONRET	NONRET	NONRET	NONRET
Name	RSVD				wpn1	txint_ebl	txabort	txreq

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NA							
Name	RSVD0							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	W:U	R/W:U	R/W:U	R/W:U	R/W:UUUU			
HW Access	R	R/W	R	R	R			
Retention	NONRET	NA	NONRET	NONRET	NONRET			
Name	wpn2	RSVD1	rtr	ide	dlc			

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NA							
Name	RSVD2							

This is the Interrupt Enable bit. 0 interrupt disabled. 1 interrupt enables, successful message transmission sets the TxMsg flag in the Interrupt Controller.

Bits	Name	Description
31:24	RSVD2[7:0]	Reserved bits. Since data read from these bits is from memory, the value at reset is undefined
23	wpn2	Write protection for bits [21:16]. 0 = Bits [21:16] are write protected. 1 = Bits [21:16] are modified by writes. The wpn2 bit must always be set in the same write that is modifying bits [21:16] as these bit's states are not preserved. The readback value of the wpn2 bit is undefined.

(continued)

22	RSVD1	Reserved bits. Since data read from these bits is from memory, the value at reset is undefined
21	rtr	RTR Remote bit. 0 Standard message, 1 RTR message
20	ide	Extended identifier. 0 Standard format message, 1 Extended format message
19:16	dlc[3:0]	Data Length of the Tx Msg. Invalid values are transmitted as they are, but the number of data bytes is limited to eight. 0 Message has 0 data byte, data[63:0] is not used, 1 Message has 1 data byte, data[63:56] is used, ..., 8 Message has 8 data bytes, data [63:0] is used, 9-15 Message has 8 data bytes
15:8	RSVD0[7:0]	Reserved bits. Since data read from these bits is from memory, the value at reset is undefined
3	wpn1	Write protection for bit [2]. 0 = Bit [2] is write protected. 1 = Bit [2] is modified by writes. The wpn1 bit must always be set in the same write that is modifying bit [2] as this bit's state is not preserved. The wpn1 bit is always zero for readback.
2	txint_ebl	Transmit Interrupt Enable. 0 Interrupt disabled, 1 Interrupt enabled, succesful message transmission setst the TxMsg flag in the interrupt controller
1	txabort	Transmit Abort Request. 0 idle, 1 Requests removal of a pending message. The message is removed the next time an arbitration loss happened. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time
0	txreq	Transmit Request. For Write: 0 Idle, 1 Message Transmit request. For Read: 0 TxReq completed, 1 TxReq pending

1.3.1089 CAN[0..0]_TX[0..7]_ID

TXID

Reset: N/A

Register : Address

CAN0_TX0_ID: 0xA024 CAN0_TX1_ID: 0xA034

CAN0_TX2_ID: 0xA044 CAN0_TX3_ID: 0xA054

CAN0_TX4_ID: 0xA064 CAN0_TX5_ID: 0xA074

CAN0_TX6_ID: 0xA084 CAN0_TX7_ID: 0xA094

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUU					NA:000		
HW Access	R					NA		
Retention	NONRET					NA		
Name	id					RSVD		

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	NONRET							
Name	id							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	NONRET							
Name	id							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	NONRET							
Name	id							

CAN Tx Msg Identifier

Bits	Name	Description
31:3	id[28:0]	Tx Msg Indentifier

1.3.1090 CAN[0..0]_TX[0..7]_DH

TXDH

Reset: N/A

Register : Address

CAN0_TX0_DH: 0xA028

CAN0_TX1_DH: 0xA038

CAN0_TX2_DH: 0xA048

CAN0_TX3_DH: 0xA058

CAN0_TX4_DH: 0xA068

CAN0_TX5_DH: 0xA078

CAN0_TX6_DH: 0xA088

CAN0_TX7_DH: 0xA098

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	NONRET							
Name	data_high							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	NONRET							
Name	data_high							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	NONRET							
Name	data_high							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	NONRET							
Name	data_high							

CAN Tx Msg Upper Data Bytes

Bits	Name	Description
31:0	data_high[31:0]	Upper Data Bytes

1.3.1091 CAN[0..0]_TX[0..7]_DL

TXDL

Reset: N/A

Register : Address

CAN0_TX0_DL: 0xA02C

CAN0_TX1_DL: 0xA03C

CAN0_TX2_DL: 0xA04C

CAN0_TX3_DL: 0xA05C

CAN0_TX4_DL: 0xA06C

CAN0_TX5_DL: 0xA07C

CAN0_TX6_DL: 0xA08C

CAN0_TX7_DL: 0xA09C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	NONRET							
Name	data_low							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	NONRET							
Name	data_low							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	NONRET							
Name	data_low							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	NONRET							
Name	data_low							

CAN Tx Msg Lower Data Bytes

Bits	Name	Description
31:0	data_low[31:0]	Lower Data Bytes

1.3.1092 CAN[0..0]_RX[0..15]_CMD

RXCMD

Reset: N/A

Register : Address

CAN0_RX0_CMD: 0xA0A0
CAN0_RX1_CMD: 0xA0C0
CAN0_RX2_CMD: 0xA0E0
CAN0_RX3_CMD: 0xA100
CAN0_RX4_CMD: 0xA120
CAN0_RX5_CMD: 0xA140
CAN0_RX6_CMD: 0xA160
CAN0_RX7_CMD: 0xA180
CAN0_RX8_CMD: 0xA1A0
CAN0_RX9_CMD: 0xA1C0
CAN0_RX10_CMD: 0xA1E0
CAN0_RX11_CMD: 0xA200
CAN0_RX12_CMD: 0xA220
CAN0_RX13_CMD: 0xA240
CAN0_RX14_CMD: 0xA260
CAN0_RX15_CMD: 0xA280

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U
HW Access	R	R	R	R	R	R	R	R
Retention	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET
Name	wpnl	lk_flg	rx_int_ebl	rtr_rply	buf_ebl	rtr_abort	rtr_rpy_pnd	msg_av

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NA							
Name	RSVD0							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	W:U	R/W:U	R/W:U	R/W:U	R/W:UUUU			
HW Access	R	R/W	R	R	R			
Retention	NONRET	NA	NONRET	NONRET	NONRET			
Name	wpnh	RSVD1	rtr	ide	dlc			

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NA							
Name	RSVD2							

Rx Msg Control register have recieve interrupt enable,buffer enable,link flag,identifier

Bits	Name	Description

(continued)

31:24	RSVD2[7:0]	Reserved bits. Since data read from these bits is from memory, the value at reset is undefined
23	wpnh	Write protection for bits [21:16]. 0 = Bits [21:16] are write protected. 1 = Bits [21:16] are modified by writes. The wpnh bit must always be set in the same write that is modifying bits [21:16] as these bit's states are not preserved. The readback value of the wpnh bit is undefined.
22	RSVD1	Reserved bits. Since data read from these bits is from memory, the value at reset is undefined
21	rtr	RTR Remote Bit.0 This is a regular message, 1 This is an RTR message
20	ide	Extended Identifier Bit. 0 This is a standard format message, 1 This is an extended format message
19:16	dlc[3:0]	Data Length Code. 0 Message has 0 data bytes, data[63:0] is not valid, 1 Message has 1 data byte, data[63:56] is valid, ..., 8 Message has 8 data bytes, data [63:0] is valid, 9-15 Message has 8 data bytes
15:8	RSVD0[7:0]	Reserved bits. Since data read from these bits is from memory, the value at reset is undefined
7	wpnl	Write protection for bits [6:3]. 0 = Bits [6:3] are write protected. 1 = Bits [6:3] are modified by writes. The wpnl bit must always be set in the same write that is modifying bits [6:3] as these bit's states are not preserved. The wpnl bit is always zero for readback.
6	lk_flg	Link Flag used to link the Rx Buffer. 0 This buffer is not linked to the next, 1 This biffer is linked with the next buffer
5	rx_int_ebl	Recieve Interrupt Enable. 0 Interrupt generation is disabled, 1 Interrupt generation is enabled
4	rtr_rply	Automatic RTR Message Handling. 0 Automatic RTR message handling disabled, 1 Automatic RTR message handling enabled
3	buf_ebl	Buffer Enable. 0 Buffer is disabled, 1 Buffer is enabled
2	rtr_abort	RTR Abort Request. 0 Idle, 1 Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time.
1	rtr_rpy_pnd	RTR Reply request Pending. 0 No RTR reply request pending, 1 RTR reply request pending
0	msg_av	Message Available. For Read: 0 No new message available, 1 New message available. For Write: 0 Idle, 1 Acknowledges receipt of new message

1.3.1093 CAN[0..0]_RX[0..15]_ID

RXID

Reset: N/A

Register : Address

CAN0_RX0_ID: 0xA0A4
CAN0_RX1_ID: 0xA0C4
CAN0_RX2_ID: 0xA0E4
CAN0_RX3_ID: 0xA104
CAN0_RX4_ID: 0xA124
CAN0_RX5_ID: 0xA144
CAN0_RX6_ID: 0xA164
CAN0_RX7_ID: 0xA184
CAN0_RX8_ID: 0xA1A4
CAN0_RX9_ID: 0xA1C4
CAN0_RX10_ID: 0xA1E4
CAN0_RX11_ID: 0xA204
CAN0_RX12_ID: 0xA224
CAN0_RX13_ID: 0xA244
CAN0_RX14_ID: 0xA264
CAN0_RX15_ID: 0xA284

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUU					R/W:UUU		
HW Access	R					R		
Retention	NONRET					NONRET		
Name	id					zeroes		

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	NONRET							
Name	id							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	NONRET							
Name	id							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	NONRET							
Name	id							

The register contains Rx Msg Identifier

Bits	Name	Description

(continued)

31:3	id[28:0]	Rx Msg Identifier
2:0	zeroes[2:0]	zeros

1.3.1094 CAN[0..0]_RX[0..15]_DH

RXDH

Reset: N/A

Register : Address

CAN0_RX0_DH: 0xA0A8
CAN0_RX1_DH: 0xA0C8
CAN0_RX2_DH: 0xA0E8
CAN0_RX3_DH: 0xA108
CAN0_RX4_DH: 0xA128
CAN0_RX5_DH: 0xA148
CAN0_RX6_DH: 0xA168
CAN0_RX7_DH: 0xA188
CAN0_RX8_DH: 0xA1A8
CAN0_RX9_DH: 0xA1C8
CAN0_RX10_DH: 0xA1E8
CAN0_RX11_DH: 0xA208
CAN0_RX12_DH: 0xA228
CAN0_RX13_DH: 0xA248
CAN0_RX14_DH: 0xA268
CAN0_RX15_DH: 0xA288

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	NONRET							
Name	data_high							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	NONRET							
Name	data_high							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	NONRET							
Name	data_high							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	NONRET							
Name	data_high							

The register contains the Upper Data Bytes

Bits	Name	Description

(continued)

31:0	data_high[31:0]	Upper Data bytes

1.3.1095 CAN[0..0]_RX[0..15]_DL

RXDL

Reset: N/A

Register : Address

CAN0_RX0_DL: 0xA0AC
CAN0_RX1_DL: 0xA0CC
CAN0_RX2_DL: 0xA0EC
CAN0_RX3_DL: 0xA10C
CAN0_RX4_DL: 0xA12C
CAN0_RX5_DL: 0xA14C
CAN0_RX6_DL: 0xA16C
CAN0_RX7_DL: 0xA18C
CAN0_RX8_DL: 0xA1AC
CAN0_RX9_DL: 0xA1CC
CAN0_RX10_DL: 0xA1EC
CAN0_RX11_DL: 0xA20C
CAN0_RX12_DL: 0xA22C
CAN0_RX13_DL: 0xA24C
CAN0_RX14_DL: 0xA26C
CAN0_RX15_DL: 0xA28C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	NONRET							
Name	data							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	NONRET							
Name	data							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	NONRET							
Name	data							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	NONRET							
Name	data							

The Register Contains the Lower data bytes

Bits	Name	Description

(continued)

31:0	data[31:0]	Lower Data bytes

1.3.1096 CAN[0..0]_RX[0..15]_AMR

RXAMR

Reset: N/A

Register : Address

CAN0_RX0_AMR: 0xA0B0
CAN0_RX1_AMR: 0xA0D0
CAN0_RX2_AMR: 0xA0F0
CAN0_RX3_AMR: 0xA110
CAN0_RX4_AMR: 0xA130
CAN0_RX5_AMR: 0xA150
CAN0_RX6_AMR: 0xA170
CAN0_RX7_AMR: 0xA190
CAN0_RX8_AMR: 0xA1B0
CAN0_RX9_AMR: 0xA1D0
CAN0_RX10_AMR: 0xA1F0
CAN0_RX11_AMR: 0xA210
CAN0_RX12_AMR: 0xA230
CAN0_RX13_AMR: 0xA250
CAN0_RX14_AMR: 0xA270
CAN0_RX15_AMR: 0xA290

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUU					R/W:U	R/W:U	NA:0
HW Access	R					R	R	NA
Retention	NONRET					NONRET	NONRET	NA
Name	id					ide	rtr	RSVD

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	NONRET							
Name	id							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	NONRET							
Name	id							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	NONRET							
Name	id							

The Register contains the Acceptance mask value

Bits	Name	Description

(continued)

31:3	id[28:0]	Identifier
2	ide	Extended Identifier
1	rtr	RTR Bit

1.3.1097 CAN[0..0]_RX[0..15]_ACR

RXACR

Reset: N/A

Register : Address

CAN0_RX0_ACR: 0xA0B4
CAN0_RX1_ACR: 0xA0D4
CAN0_RX2_ACR: 0xA0F4
CAN0_RX3_ACR: 0xA114
CAN0_RX4_ACR: 0xA134
CAN0_RX5_ACR: 0xA154
CAN0_RX6_ACR: 0xA174
CAN0_RX7_ACR: 0xA194
CAN0_RX8_ACR: 0xA1B4
CAN0_RX9_ACR: 0xA1D4
CAN0_RX10_ACR: 0xA1F4
CAN0_RX11_ACR: 0xA214
CAN0_RX12_ACR: 0xA234
CAN0_RX13_ACR: 0xA254
CAN0_RX14_ACR: 0xA274
CAN0_RX15_ACR: 0xA294

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUU					R/W:U	R/W:U	NA:0
HW Access	R					R	R	NA
Retention	NONRET					NONRET	NONRET	NA
Name	id					ide	rtr	RSVD

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	NONRET							
Name	id							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	NONRET							
Name	id							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	NONRET							
Name	id							

The Register contains the Acceptance Code value

Bits	Name	Description

(continued)

31:3	id[28:0]	Identifier
2	ide	Extended Identifier
1	rtr	RTR Bit

1.3.1098 CAN[0..0]_RX[0..15]_AMRD

RXAMRD

Reset: N/A

Register : Address

CAN0_RX0_AMRD: 0xA0B8
CAN0_RX1_AMRD: 0xA0D8
CAN0_RX2_AMRD: 0xA0F8
CAN0_RX3_AMRD: 0xA118
CAN0_RX4_AMRD: 0xA138
CAN0_RX5_AMRD: 0xA158
CAN0_RX6_AMRD: 0xA178
CAN0_RX7_AMRD: 0xA198
CAN0_RX8_AMRD: 0xA1B8
CAN0_RX9_AMRD: 0xA1D8
CAN0_RX10_AMRD: 0xA1F8
CAN0_RX11_AMRD: 0xA218
CAN0_RX12_AMRD: 0xA238
CAN0_RX13_AMRD: 0xA258
CAN0_RX14_AMRD: 0xA278
CAN0_RX15_AMRD: 0xA298

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	NONRET							
Name	data_lsb							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	NONRET							
Name	data_lsb							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

The register conatins the Acceptance mask data

Bits	Name	Description

(continued)

15:0	data_lsb[15:0]	Upper 2 Bytes of Data

1.3.1099 CAN[0..0]_RX[0..15]_ACRD

RXACRD

Reset: N/A

Register : Address

CAN0_RX0_ACRD: 0xA0BC
CAN0_RX1_ACRD: 0xA0DC
CAN0_RX2_ACRD: 0xA0FC
CAN0_RX3_ACRD: 0xA11C
CAN0_RX4_ACRD: 0xA13C
CAN0_RX5_ACRD: 0xA15C
CAN0_RX6_ACRD: 0xA17C
CAN0_RX7_ACRD: 0xA19C
CAN0_RX8_ACRD: 0xA1BC
CAN0_RX9_ACRD: 0xA1DC
CAN0_RX10_ACRD: 0xA1FC
CAN0_RX11_ACRD: 0xA21C
CAN0_RX12_ACRD: 0xA23C
CAN0_RX13_ACRD: 0xA25C
CAN0_RX14_ACRD: 0xA27C
CAN0_RX15_ACRD: 0xA29C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	NONRET							
Name	data_lsb							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	NONRET							
Name	data_lsb							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

The register conatins the Acceptance code data

Bits	Name	Description

(continued)

15:0	data_lsb[15:0]	Upper 2 Bytes of Data

1.3.1100 DFB[0..0]_DPA_SRAM_DATA[0..127]

Data RAM A

Reset: N/A

Register : Address

DFB_DPA_SRAM_DATA: 0xC000-0xC1FF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	sramdata							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	sramdata							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	sramdata							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Data Storage SRAM

Bits	Name	Description
23:0	sramdata[23:0]	(no description)

1.3.1101 DFB[0..0]_DPB_SRAM_DATA[0..127]

DFB Data RAM B

Reset: N/A

Register : Address

DFB_DPB_SRAM_DATA: 0xC200-0xC3FF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	sramdata							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	sramdata							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	sramdata							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Data Storage SRAM

Bits	Name	Description
23:0	sramdata[23:0]	(no description)

1.3.1102 DFB[0..0]_CSA_SRAM_DATA[0..63]

DFB Control Store A

Reset: N/A

Register : Address

DFB_CSA_SRAM_DATA: 0xC400-0xC4FF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	sramdata							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	sramdata							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	sramdata							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	sramdata							

Control Storage SRAM

Bits	Name	Description
31:0	sramdata[31:0]	(no description)

1.3.1103 DFB[0..0]_CSB_SRAM_DATA[0..63]

DFB Control Store B

Reset: N/A

Register : Address

DFB_CSB_SRAM_DATA: 0xC500-0xC5FF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	sramdata							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	sramdata							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	sramdata							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	sramdata							

Control Storage SRAM

Bits	Name	Description
31:0	sramdata[31:0]	(no description)

1.3.1104 DFB[0..0]_FSM_SRAM_DATA[0..63]

DFB Code Store B

Reset: N/A

Register : Address

DFB_FSM_SRAM_DATA: 0xC600-0xC6FF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	sramdata							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	sramdata							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	sramdata							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	sramdata							

Code Storage SRAM

Bits	Name	Description
31:0	sramdata[31:0]	(no description)

1.3.1105 DFB[0..0]_ACU_SRAM_DATA[0..15]

DFB Address Store

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB_ACU_SRAM_DATA: 0xC700-0xC73F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	NONRET							
Name	sramdata							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00		R/W:000000					
HW Access	NA		R/W					
Retention	NA		NONRET					
Name	RSVD		sramdata					

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Address Storage Memory

Bits	Name	Description
13:0	sramdata[13:0]	(no description)

1.3.1106 DFB[0..0]_CR

DFB Command Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_CR: 0xC780

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:0	R/W:0	R/W:0
HW Access	NA					R	R	R
Retention	NA					NONRET	NONRET	NONRET
Name	RSVD					CORECLK_ DISABLE	ADDR6	RUN

This register enables/disables DFB operation and sets FSM memory bank. Also, the internal core clock gater is controlled. A read of this register produces the last value written to this register.

Bits	Name	Description
2	CORECLK_DISABLE	This bit when set high disables (gates off) the clock to the entire core of the block. This includes all FFs except those used for the AHB interface and CSRs and all 6 RAMs. When disabled (set high) the AHB interface to the CSR is still fully functional. This bit is ANDed with the primary input signal dfb_clk_en to control the clock gate. dfb_clk_en must be high and CoreCLK_Disable must be low for the clock to run. See Table 1-654.
1	ADDR6	This bit is literally address bit 5 (6th bit) of the FSM RAM when addressed by the DFB Controller. It has no affect on the FSM RAM when addressed on the AHB interface. It controls the Banking feature of the FSM. See Table 1-653.
0	RUN	Setting this bit to 1 enables the DFB to run. Setting it to 0 forces the next state address of the FSM to zero of the active Bank, reinitializes the ACU's and PC's and clears the round flag, saturation flag, saturation detect flag and all 6 extended Enables in the Controller. See Table 1-655.

Table 1-653. Bit field encoding: addr6_enum

Value	Name	Description
1'b1	ADDR6_HIGH	ADDR6 is High
1'b0	ADDR6_LOW	ADDR6 is Low

Table 1-654. Bit field encoding: coreclk_disable_enum

Value	Name	Description
1'b1	CORECLK_DISABLE_HIGH	Core Clock is Disabled (gated)
1'b0	CORECLK_DISABLE_LOW	Core Clock is Enabled

Table 1-655. Bit field encoding: run_bit_enum

Value	Name	Description
1'b1	RUN_EN	DFB is enabled to operate.
1'b0	RUN_DIS	DFB operation is halted.

1.3.1107 DFB[0..0]_SR

DFB Status Register

Reset: Reset Signals Listed Below

Register : Address

DFB0_SR: 0xC784

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0	R/WOC:0	R:U	R:U	R:U
HW Access	W	W	W	W	W	W	W	W
Retention	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET	NONRET
Name	INTR_SEM2	INTR_SEM1	INTR_SEM0	INTR_HOLDB	INTR_HOLDA	RND_MODE	SAT_MODE	RAM_SEL

This register contains 5 bits indicating the status of block generated interrupts and 3 bits of status from the Datapath unit. Of the 5 sources of interrupts, only those configured in INT_CTRL are activated. If not activated in INT_CTRL they will never assert in this register. If an interrupt source bit (7:3) is set this indicates it is at least one of the sources of the currently driven interrupt on dfb_intr. More than one of the 5 could be asserted. Note that if the system SW wishes to poll for an event and not have an interrupt generated, the interrupt must be enabled in the INT_CTRL register so that it can be polled here and then disable the interrupt in the Interrupt Controller or not connect the dfb_intr signal to the Interrupt Controller at all by not configuring the DSI path. Bits 2:0 are read-only - writes to these bits have no affect. Writes to bits 7:3 of '1' clear the bit, writes of 0 have no affect.

Bits	Name	Description
7	INTR_SEM2	If this bit is high, semaphore register bit 2 is a source of the current interrupt. Write a '1' to this bit to clear it. See Table 1-660.
6	INTR_SEM1	If this bit is high, semaphore register bit 1 is a source of the current interrupt. Write a '1' to this bit to clear it. See Table 1-659.
5	INTR_SEM0	If this bit is high, semaphore register bit 0 is a source of the current interrupt. Write a '1' to this bit to clear it. See Table 1-658.
4	INTR_HOLDB	If this bit is high, Holding register B is a source of the current interrupt. Write a '1' to this bit to clear it. Reading the Holding register B also clears this bit. See Table 1-657.
3	INTR_HOLDA	If this bit is high, Holding register A is a source of the current interrupt. Write a '1' to this bit to clear it. Reading the Holding register A also clears this bit. See Table 1-656.
2	RND_MODE	Indicates that the DP is in Round mode - meaning that any result passing out of the DP unit is being rounded to a 16-bit value. See Table 1-662.

(continued)

1	SAT_MODE	Indicates that the DP unit is in Saturation mode - meaning that any mathematic operation executed that produces a number outside the range of a 24-bit 2's compliment number is clamped to the mode positive or negative number allowed. Saturation mode is set/unset under Assembly control in the DFB Controller. See Table 1-663.
0	RAM_SEL	This bit indicates which Control Store memory is in use, RAM A or RAM B. See Table 1-661.

Reset Table

Reset Signal	Applicable Register Bit(s)
N/A	RAM_SEL, SAT_MODE, RND_MODE
Domain reset for non-retention flops [reset_all_nonretention]	INTR_HOLDA, INTR_HOLDB, INTR_SEM0, INTR_SEM1, INTR_SEM2

Table 1-656. Bit field encoding: intr_holda_enum

Value	Name	Description
1'b0	HOLDA_OFF	Indicates no pending Holding A Register Interrupt.
1'b1	HOLDA_ON	Indicates a pending Holding A Register Interrupt.

Table 1-657. Bit field encoding: intr_holdb_enum

Value	Name	Description
1'b0	HOLDB_OFF	Indicates no pending Holding B Register Interrupt.
1'b1	HOLDB_ON	Indicates a pending Holding B Register Interrupt.

Table 1-658. Bit field encoding: intr_sem0_enum

Value	Name	Description
1'b0	SEM0_OFF	Indicates no pending Semaphore 0 Interrupt.
1'b1	SEM0_ON	Indicates a pending Semaphore 0 Interrupt.

Table 1-659. Bit field encoding: intr_sem1_enum

Value	Name	Description
1'b0	SEM1_OFF	Indicates no pending Semaphore 1 Interrupt.
1'b1	SEM1_ON	Indicates a pending Semaphore 1 Interrupt.

Table 1-660. Bit field encoding: intr_sem2_enum

Value	Name	Description
1'b0	SEM2_OFF	Indicates no pending Semaphore 2 Interrupt.
1'b1	SEM2_ON	Indicates a pending Semaphore 2 Interrupt.

Table 1-661. Bit field encoding: ram_select_bit_enum

Value	Name	Description
1'b0	RAMSEL_LOW	Control Store memory A is in use.
1'b1	RAMSEL_HIGH	Control Store memory B is in use.

Table 1-662. Bit field encoding: rnd_mode_enum

Value	Name	Description
1'b0	RND_OFF	Indicates Round Mode is off.
1'b1	RND_ON	Indicates Round Mode is on.

Table 1-663. Bit field encoding: sat_mode_enum

Value	Name	Description
1'b0	SAT_OFF	Indicates Saturation mode is off.
1'b1	SAT_ON	Indicates Saturation mode is on.

1.3.1108 DFB[0..0]_RAM_EN

DFB RAM Enable Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DFB0_RAM_EN: 0xC788

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00		R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R		R	R	R	R	R	R
Retention	RET		RET	RET	RET	RET	RET	RET
Name	RAMWR_ADDRING		DPB_EN	DPA_EN	ACU_EN	CSB_EN	CSA_EN	FSM_EN

This register controls the DFB memory enables. These bits are tied directly to the enable pins of the RAMs in this block and should be used by System SW to power-down RAMs not in use. A read of this register produces the last value written to this register. The high two bits control the RAM overlay addressing.

Bits	Name	Description
7:6	RAMWR_ADDRING[1:0]	These two bits control the write addressing of the 4 largest RAMs embedded in the DFB (CS-A, CS-B, Data-A, Data-B). The setting of these bits allows overlaid writes to occur to these memories when it is desired to fill them with like data. This feature is primarily intended to enhance SW BIST test time but may also have functional uses as well like filling both CS RAMs concurrently as they typically hold identical data. Setting these bits to 01, for example, configures the HW to write to both CS-A and CS-B for any write to the address space of either CS-A or CS-B. Reads are not affected by these bits. See Table 1-665.
5	DPB_EN	Datapath RAM B RAM enable / disable. See Table 1-664.
4	DPA_EN	Datapath RAM A RAM enable / disable. See Table 1-664.
3	ACU_EN	ACU RAM RAM enable / disable. See Table 1-664.
2	CSB_EN	Control Store RAM B RAM enable / disable. See Table 1-664.
1	CSA_EN	Control Store RAM A RAM enable / disable. See Table 1-664.
0	FSM_EN	FSM RAM RAM enable / disable. See Table 1-664.

Table 1-664. Bit field encoding: ram_enable_bit_enum

Value	Name	Description
1'b1	RAM_EN	RAM is enabled.
1'b0	RAM_DIS	RAM is disabled.

(continued)

Table 1-665. Bit field encoding: ram_write_addressing_bits_enum

Value	Name	Description
2'b00	NO_OVERLAY	No overlay mapping.
2'b11	OVERLAY_CS_A_CS_B	Overlay CS A with CS B.
2'b10	OVERLAY_DATA_A_DATA_B	Overlay Data A with Data B.
2'b11	OVERLAY_CS_AB_DATA_AB	Overlay CS A/B with Data A with DATA B.

1.3.1109 DFB[0..0]_RAM_DIR

DFB RAM Direction Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DFB0_RAM_DIR: 0xC78C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:1	R/W:1	R/W:1	R/W:1	R/W:1	R/W:1
HW Access	NA	R	R	R	R	R	R	R
Retention	NA	RET	RET	RET	RET	RET	RET	RET
Name	RSVD	SNP_DABLE	DPB_DIR	DPA_DIR	ACU_DIR	CSB_DIR	CSA_DIR	FSM_DIR

This register controls the DFB memory direction. These bits control if each RAM of this block is embedded to the DFB function or mapped in the system address space on the AHB bus. Mapping to the bus facilitates SW BIST, Configuration filling, and Block Mode transfers. A read to this register returns what was last written. When programming code into the CSA/B and FSM RAMs the RAM_DIR bits should be set and unset together. When in normal operating mode and the CSA/B, ACU and FSM are being filled with assembly code/data, it is high recommended that all four RAMs DIR bits be set and cleared together.

Bits	Name	Description
6	SNP_DABLE	The CS and DP RAMs (optionally the FSM) have address snooping logic that watches for redundant back-to-back RD cycles and disables the RAM to conserve power. Writing a 1 to this bit disables this logic for all RAMs. See Table 1-667.
5	DPB_DIR	Datapath RAM B RAM Direction. See Table 1-666.
4	DPA_DIR	Datapath RAM A RAM Direction. See Table 1-666.
3	ACU_DIR	ACU RAM RAM Direction. See Table 1-666.
2	CSB_DIR	Control Store RAM B RAM Direction. See Table 1-666.
1	CSA_DIR	Control Store RAM A RAM Direction. See Table 1-666.
0	FSM_DIR	FSM RAM RAM Direction. See Table 1-666.

Table 1-666. Bit field encoding: ram_direction_bit_enum

Value	Name	Description
1'b1	RAM_AHB	System Bus
1'b0	RAM_DFB	DFB

(continued)

Table 1-667. Bit field encoding: snoop_disable_bit_enum

Value	Name	Description
1'b1	SNP_DISABLE	Disabled
1'b0	SNP_ENABLE	Enabled

1.3.1110 DFB[0..0]_SEMA

DFB Semaphore Register

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_SEMA: 0xC790

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	W:000			NA:0	R/W:000		
HW Access	NA	R			NA	R		
Retention	NA	NONRET			NA	NONRET		
Name	RSVD	SEMA_MASK			RSVD	SEMA		

This register controls the DFB Semaphore register. These bits are used to pass semaphores between the DFB Controller and the System SW. Their use and purpose is user defined. A read to this register returns what was last written by either System SW or the DFB Controller.

Bits	Name	Description
6:4	SEMA_MASK[2:0]	These bits are used to mask writes to bits 2-0. They are write-only. If bit 4 is a 1 then the value on bit 0 will be written to SEM0, otherwise SEM0 will not be altered. Likewise for MASK1 and SEM1, and MASK2 and SEM2.
2:0	SEMA[2:0]	These bits are used to pass semaphores between the DFB Controller and the System SW. Their definition is user defined. There is no HW implementing an arbitration methodology should both the System and Control access the same SEM bit at the same time. Coherency of the SEM bits is the responsibility of the SW running on the Controller and the System CPU. If the same SEM bit is written by the Controller and the System in the exact same cycle (a collision), the System write takes precedence over the Controller. In this manner, each of the 3 bits are treated individually.

1.3.1111 DFB[0..0]_DSI_CTRL

DFB Global Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DFB0_DSI_CTRL: 0xC794

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:00		R/W:00	
HW Access	NA				R		R	
Retention	NA				RET		RET	
Name	RSVD				GBL2_OUT		GBL1_OUT	

This register controls what internal signals are mapped to the two primary output global signals dfb_globalo1 and dfb_globalo2. A read of this register produces the last value written to this register. These two outputs are registered (pclk rising) just before leaving the block - giving them a 1 cycle delay and a full clock cycle to propagate to their DSI destinations.

Bits	Name	Description
3:2	GBL2_OUT[1:0]	These bits are used to control what internal signals are mapped to the primary output signal dfb_globalo2. See Table 1-669.
1:0	GBL1_OUT[1:0]	These bits are used to control what internal signals are mapped to the primary output signal dfb_globalo1. See Table 1-668.

Table 1-668. Bit field encoding: global_output_1_encoding_bits_enum

Value	Name	Description
2'b00	DFB_RUN	DFB RUN Bit. This is the same bit as the RUN bit in the DFB0_CR register.
2'b01	SEM0	Semaphore Bit 0. This is the same signal described in the DFB0_SEMA CSR.
2'b10	SEM1	Semaphore Bit 1. This is the same signal described in the DFB0_SEMA CSR.
2'b11	DFB_INTR	DFB Interrupt. This is the same signal as the primary dfb_intr output signal.

Table 1-669. Bit field encoding: global_output_2_encoding_bits_enum

Value	Name	Description
2'b00	SEM2	Semaphore Bit 2. This is the same signal described in the DFB0_SEMA CSR.
2'b01	DPSIGN	Datapath Sign. This signal asserts anytime the output of the ALU in the Datapath unit is negative. It will remain high for each cycle this condition is true.
2'b10	DPTHREASH	Datapath Threashold Crossed. This signal asserts anytime the threashold of 0 is crossed in the ALU when one of the following instructions is executing: TDECA, TSUBA, TSUBB, TADDABSA, TADDABSB. It will remain high for each cycle this condition is true.
2'b11	DPEQ	Datapath ALU=0. This signal asserts high when the output of the ALU in the Datapath unit equals 0 and one of the following ALU commands is executing: TDECA, TSUBA, TSUBB, TADDABSA, TADDABSB. It will remain high for each cycle this condition is true.

1.3.1112 DFB[0..0]_INT_CTRL

DFB Interrupt Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DFB0_INT_CTRL: 0xC798

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA			R	R	R	R	R
Retention	NA			RET	RET	RET	RET	RET
Name	RSVD			SEMA2_EN	SEMA1_EN	SEMA0_EN	HOLDB_EN	HOLDA_EN

This register allows control of what events generate an interrupt. Each of the events enabled by the bits in this register are ORed together to produce the dfb_intr signal. A read to this register returns what was last written. System SW should see that a semaphore is never configured as both a DMA request and an interrupt (see DMA_CTRL).

Bits	Name	Description
4	SEMA2_EN	If this bit is set high, an interrupt is generated each time a 1 is written into the semaphore register bit 2. See Table 1-671.
3	SEMA1_EN	If this bit is set high, an interrupt is generated each time a 1 is written into the semaphore register bit 1. See Table 1-671.
2	SEMA0_EN	If this bit is set high, an interrupt is generated each time a 1 is written into the semaphore register bit 0. See Table 1-671.
1	HOLDB_EN	If this bit is set high, an interrupt is generated each time new valid data is written into the output Holding register B. See Table 1-670.
0	HOLDA_EN	If this bit is set high, an interrupt is generated each time new valid data is written into the output Holding register A. See Table 1-670.

Table 1-670. Bit field encoding: enable_holding_reg_bit_enum

Value	Name	Description
1'b1	ENABLE_HOLDING_IRQ_EN	Interrupt is generated each time new valid data is written inot the output Holding register.
1'b0	ENABLE_HOLDING_IRQ_DIS	Holding register interrupt masked.

Table 1-671. Bit field encoding: enable_semaphore_bit_enum

Value	Name	Description
1'b1	ENABLE_SEMAPHORE_IRQ_EN	Interrupt is generated each time a 1 is written to the semaphore register.
1'b0	ENABLE_SEMAPHORE_IRQ_DIS	Semaphore register interrupt masked.

1.3.1113 DFB[0..0]_DMA_CTRL

DFB DMAREQ Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DFB0_DMA_CTRL: 0xC79C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:00		R/W:00	
HW Access	NA				R		R	
Retention	NA				RET		RET	
Name	RSVD				DMAREQ2		DMAREQ1	

This register allows control of what events generate DMAREQ events. Each field allows the user to configure what event drives each of the two DMAREQ primary output signals. Note that if a semaphore is configured as the DMAREQ the HW automatically clears the appropriate semaphore register after one pclk cycle - creating a single cycle pulse on the dmareq output as is required. Otherwise, the semaphores are sticky. If a Holding register is programmed as a DMAREQ, the DMAREQ is level sensed, instead of a pulse. The DMAREQ in this case will stay asserted until the Holding register is read. Level sensed is the preferred method of PHUB even though a strobe will work. System SW should see that a semaphore is never configured as both a DMA request and an interrupt (see INT_CTRL). A read of this register returns the last value written.

Bits	Name	Description
3:2	DMAREQ2[1:0]	The value in these two bits selects which event drives dma_req2. See Table 1-673.
1:0	DMAREQ1[1:0]	The value in these two bits selects which event drives dma_req1. See Table 1-672.

Table 1-672. Bit field encoding: dma_req_1_source_bits_enum

Value	Name	Description
2'b00	DMAREQ1_DISABLED	Disabled
2'b01	DMAREQ1_HOLDING_REG_A	New data in Holding Register A.
2'b10	DMAREQ1_SEMAPHORE_0	Semaphore 0.
2'b11	DMAREQ1_SEMAPHORE_1	Semaphore 1.

Table 1-673. Bit field encoding: dma_req_2_source_bits_enum

Value	Name	Description
2'b00	DMAREQ2_DISABLED	Disabled
2'b01	DMAREQ2_HOLDING_REG_B	New data in Holding Register B.
2'b10	DMAREQ2_SEMAPHORE_0	Semaphore 0.
2'b11	DMAREQ2_SEMAPHORE_1	Semaphore 1.

1.3.1114 DFB[0..0]_STAGEA

DFB Low Byte Staging Register A

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_STAGEA: 0xC7A0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	STGA_LOW							

This is the low byte of the Streaming input Staging Register - Port A. If the Staging A Data Alignment bit is set in the DALIGN register then data written to this address will be written into bits 15:8 instead. Although the Staging A/B registers are shown here as 3 byte-wide registers, it is primarily intended that they be treated as 24-bit registers at a 32-bit offset. Due to the architecture of the DFB, any value written to the Staging A or B registers that is less than 24 bits in size must be msb aligned. For example, a 16-bit value written to the Staging A register must be written to STAGExM and STAGExH with STAGEx set to 0. The Staging registers support byte and half-word accesses as well. However, if byte and half-word accesses are used then the Key Coherency Byte feature must be used. Also see the COHER register description below. In some use models it is desirous to write 16-bit values on bus bits 15:0 and have them actually writing to bits 23:8 of the register. A System SW convenience feature to accomplish this is provided. If the Data Alignment bit for these registers is set in the DALIGN register the byte written is shifted up (left) to the next byte position. This is only true of the two lower bytes. READ: AHB: What was last written. The DFB Controller reads this register (and the other 2 bytes) by asserting busrd and setting the low-order ACU RAM address bit low. WRITE: Writes the low byte of the input Staging Register for Port A or the middle byte if the Data Alignment bit is set in the DALIGN register.

Bits	Name	Description
7:0	STGA_LOW[7:0]	A write to this register sets the low byte of the input Staging Register for Port A.

1.3.1115 DFB[0..0]_STAGEAM

DFB Middle Byte Staging Register A

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_STAGEAM: 0xC7A1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	STGA_MID							

This is the middle byte of the Streaming input Staging Register - Port A. If the Staging A Data Alignment bit is set in the DALIGN register then data written to this address will be written into bits 23:16 instead. See usage notes in STAGEA register description above.

Bits	Name	Description
7:0	STGA_MID[7:0]	A write to this register sets the middle byte of the input Staging Register for Port A.

1.3.1116 DFB[0..0]_STAGEAH

DFB High Byte Staging Register A

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_STAGEAH: 0xC7A2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	STGA_HIGH							

This is the high byte of the Streaming input Staging Register - Port A. See usage notes in STAGEA register description above.

Bits	Name	Description
7:0	STGA_HIGH[7:0]	A write to this register sets the high byte of the input Staging Register for Port A.

1.3.1117 DFB[0..0]_STAGEB

DFB Low Byte Staging Register B

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_STAGEB: 0xC7A4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	STGB_LOW							

This is the low byte of the Streaming input Staging Register - Port B. If the Staging B Data Alignment bit is set in the DALIGN register then data written to this address will be written into bits 15:8 instead. See usage notes in STAGEA register description above.

Bits	Name	Description
7:0	STGB_LOW[7:0]	A write to this register sets the low byte of the input Staging Register for Port B.

1.3.1118 DFB[0..0]_STAGEBM

DFB Middle Byte Staging Register B

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_STAGEBM: 0xC7A5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	STGB_MID							

This is the middle byte of the Streaming input Staging Register - Port B. If the Staging B Data Alignment bit is set in the DALIGN register then data written to this address will be written into bits 23:16 instead. See usage notes in STAGEA register description above.

Bits	Name	Description
7:0	STGB_MID[7:0]	A write to this register sets the middle byte of the input Staging Register for Port B.

1.3.1119 DFB[0..0]_STAGEBH

DFB High Byte Staging Register B

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_STAGEBH: 0xC7A6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	NONRET							
Name	STGB_HIGH							

This is the high byte of the Streaming input Staging Register - Port B. See usage notes in STAGEA register description above.

Bits	Name	Description
7:0	STGB_HIGH[7:0]	A write to this register sets the high byte of the input Staging Register for Port B.

1.3.1120 DFB[0..0]_HOLDA

DFB Low Byte Holding Register A

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_HOLDA: 0xC7A8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	HOLDA_LOW							

This is the low byte of the output Holding Register - Port A. If the Holding A Data Alignment bit is set in the DALIGN register then data read from this address will be bits 15:8 instead. Although the Holding A/B registers are shown here as 3 byte-wide registers, it is primarily intended that they be treated as 24-bit registers at a 32-bit offset. Due to the architecture of the DFB, any value read from the Holding A or B registers will be msb aligned unless shifted otherwise by the Datapath shifter. For example, if the resultant output samples are 16-bit values, a read of a Holding register will produce that data on bits 23:8, or HOLDxH and HOLDxM. The Holding registers support byte and half-word accesses as well. However, if byte and half-word accesses are used then the Key Coherency Byte feature must be used. Also see the COHER register description below. In some use models it is desirous to read 16-bit values on bus bits 15:0 and have them actually source from bits 23:8 of the register. A System SW convenience feature to accomplish this is provided. If the Data Alignment bit for these registers is set in the DALIGN register the byte read is shifted down (right) to the next byte position. This is only true of the two upper bytes. Also as a System SW convenience, reads of the Holding registers are sign extended up to bit 31 of the bus even though the top byte is not documented or implemented as a real register. If the DFB is configured (see INT_CTRL) to generate an interrupt based on valid data in the Holding register, the interrupt status bit in the SR register will be cleared when any portion (byte, 16-bit or full 32-bit read) of the Holding register is read, by the CPU or the DMA Controller. READ: What was last written by the DFB Controller. WRITE: Read-only by AHB, DFB Controller writes to this register (including the other 2 bytes) with a buswr command and the low-order ACU RAM address bit set low.

Bits	Name	Description
7:0	HOLDA_LOW[7:0]	Low byte of the output Holding Register, Port A.

1.3.1121 DFB[0..0]_HOLDAM

DFB Middle Byte Holding Register A

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_HOLDAM: 0xC7A9

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	HOLDA_MID							

This is the middle byte of the output Holding Register - Port A. If the Holding A Data Alignment bit is set in the DALIGN register then data read from this address will be bits 23:16 instead. See usage notes in HOLDA register description above.

Bits	Name	Description
7:0	HOLDA_MID[7:0]	Middle byte of the output Holding Register, Port A.

1.3.1122 DFB[0..0]_HOLDAH

DFB High Byte Holding Register A

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_HOLDAH: 0xC7AA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	HOLDA_HIGH							

This is the high byte of the output Holding Register - Port A. See usage notes in HOLDA register description above.

Bits	Name	Description
7:0	HOLDA_HIGH[7:0]	High byte of the output Holding Register, Port A.

1.3.1123 DFB[0..0]_HOLDAS

DFB Holding Register A Sign Extension

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_HOLDAS: 0xC7AB

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	HOLDA_SIGNEXT							

* This is a pseudo register. There are no FFs or even an address decode for this pseudo register. If read or written as a byte it acts the same as all other unused byte addresses in the block's address space - writes are ignored and reads produce 0 on the bus. However, if HOLDA is read as a 32-bit value or HOLDAH is read as a 16-bit value, the sign is extended onto this byte lane. This pseudo register definition is here simply to document this sign extension functionality. See usage notes in HOLDA register description above. READ: Always 0 if read as a byte. Always the sign extension if HOLDA is read as a 32-bit value or HOLDAH is read as a 16-bit value. WRITE: Ignored.

Bits	Name	Description
7:0	HOLDA_SIGNEXT[7:0]	Output Holding Register Sign Extension, Port A.

1.3.1124 DFB[0..0]_HOLDB

DFB Low Byte Holding Register B

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_HOLDB: 0xC7AC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	HOLDB_LOW							

This is the low byte of the output Holding Register - Port B. If the Holding B Data Alignment bit is set in the DALIGN register then data read from this address will be bits 15:8 instead. See usage notes in HOLDA register description above.

Bits	Name	Description
7:0	HOLDB_LOW[7:0]	Low byte of the output Holding Register, Port B.

1.3.1125 DFB[0..0]_HOLDBM

DFB Middle Byte Holding Register B

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_HOLDBM: 0xC7AD

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	HOLDB_MID							

This is the middle byte of the output Holding Register - Port B. If the Holding B Data Alignment bit is set in the DALIGN register then data read from this address will be bits 23:16 instead. See usage notes in HOLDA register description above.

Bits	Name	Description
7:0	HOLDB_MID[7:0]	Middle byte of the output Holding Register, Port B.

1.3.1126 DFB[0..0]_HOLDBH

DFB High Byte Holding Register B

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_HOLDBH: 0xC7AE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	HOLDB_HIGH							

This is the high byte of the output Holding Register - Port B. See usage notes in HOLDA register description above.

Bits	Name	Description
7:0	HOLDB_HIGH[7:0]	High byte of the output Holding Register, Port B.

1.3.1127 DFB[0..0]_HOLDBS

DFB Holding Register B Sign Extension

Reset: Domain reset for non-retention flops [reset_all_nonretention]

Register : Address

DFB0_HOLDBS: 0xC7AF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	W							
Retention	NONRET							
Name	HOLDB_SIGNEXT							

* This is a pseudo register. There are no FFs or even an address decode for this pseudo register. If read or written as a byte it acts the same as all other unused byte addresses in the block's address space - writes are ignored and reads produce 0 on the bus. However, if HOLDB is read as a 32-bit value or HOLDBH is read as a 16-bit value, the sign is extended onto this byte lane. This pseudo register definition is here simply to document this sign extension functionality. See usage notes in HOLDA register description above. READ: Always 0 if read as a byte. Always the sign extension if HOLDB is read as a 32-bit value or HOLDBH is read as a 16-bit value. WRITE: Ignored.

Bits	Name	Description
7:0	HOLDB_SIGNEXT[7:0]	Output Holding Register Sign Extension, Port B.

1.3.1128 DFB[0..0]_COHER

DFB Coherency Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DFB0_COHER: 0xC7B0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:10		R/W:10		R/W:10		R/W:10	
HW Access	R		R		R		R	
Retention	RET		RET		RET		RET	
Name	holdb_key		holda_key		stgb_key		stga_key	

The 4 2-bit fields of this register are used to select which of the 3 bytes of each of the STAGEA, STAGEB, HOLDA and HOLDB will be used as the Key Coherency Byte. Coherency refers to the HW added to this block to protect against malfunctions of the block in cases where register fields are wider than the bus access, leaving intervals in time when fields are partially written/read (incoherent). The Key Coherency Byte is the SW's way of telling the HW which byte of the field will be written/read last when an update to the field is desired. When the Key byte is written/read, the field is flagged coherent. If any other byte is written/read, the field is flagged incoherent.

Bits	Name	Description
7:6	holdb_key[1:0]	Sets the Key Coherency Byte of the Holding B register See Table 1-675.
5:4	holda_key[1:0]	Sets the Key Coherency Byte of the Holding A register See Table 1-674.
3:2	stgb_key[1:0]	Sets the Key Coherency Byte of the Staging B register See Table 1-677.
1:0	stga_key[1:0]	Sets the Key Coherency Byte of the Staging A register See Table 1-676.

Table 1-674. Bit field encoding: holda_key_enum

Value	Name	Description
2'b00	HOLDA_KEY_LOW	Key Byte is low byte.
2'b01	HOLDA_KEY_MID	Key Byte is med byte.
2'b10	HOLDA_KEY_HIGH	Key Byte is high byte.

Table 1-675. Bit field encoding: holdb_key_enum

Value	Name	Description
2'b00	HOLDB_KEY_LOW	Key Byte is low byte.
2'b01	HOLDB_KEY_MID	Key Byte is med byte.
2'b10	HOLDB_KEY_HIGH	Key Byte is high byte.

Table 1-676. Bit field encoding: stga_key_enum

Value	Name	Description
2'b00	STGA_KEY_LOW	Key Byte is low byte.
2'b01	STGA_KEY_MID	Key Byte is med byte.
2'b10	STGA_KEY_HIGH	Key Byte is high byte.

(continued)

Table 1-677. Bit field encoding: stgb_key_enum

Value	Name	Description
2'b00	STGB_KEY_LOW	Key Byte is low byte.
2'b01	STGB_KEY_MID	Key Byte is med byte.
2'b10	STGB_KEY_HIGH	Key Byte is high byte.

1.3.1129 DFB[0..0]_DALIGN

DFB Data Alignment Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DFB0_DALIGN: 0xC7B4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Retention	NA				RET	RET	RET	RET
Name	RSVD				holdb_dalign	holda_dalign	stgb_dalign	stga_dalign

These bits when set high causes an 8-bit shift in the data to all access of the corresponding Staging and Holding registers. The purpose of this feature is to allow 9 to 16 bit input and output samples to travel as 16-bit values on the AHB bus. Because the DFB datapath is inherently msb aligned, it is convenient to the System SW to align values on bits 23:8 of the Staging and Holding register to bits 15:0 of the bus. A read of this register produces the last value written to this register.

Bits	Name	Description
3	holdb_dalign	Shifts the read right by a byte. See Table 1-679.
2	holda_dalign	Shifts the read right by a byte. See Table 1-678.
1	stgb_dalign	Shifts the write left by a byte. See Table 1-681.
0	stga_dalign	Shifts the write left by a byte. See Table 1-680.

Table 1-678. Bit field encoding: holda_dalign_enum

Value	Name	Description
1'b0	HOLDA_DALIGN_LOW	Reads normally.
1'b1	HOLDA_DALIGN_HIGH	Reads shifted right by 8-bits.

Table 1-679. Bit field encoding: holdb_dalign_enum

Value	Name	Description
1'b0	HOLDB_DALIGN_LOW	Reads normally.
1'b1	HOLDB_DALIGN_HIGH	Reads shifted right by 8-bits.

Table 1-680. Bit field encoding: stga_dalign_enum

Value	Name	Description
1'b0	STGA_DALIGN_LOW	Writes normally.
1'b1	STGA_DALIGN_HIGH	Writes shifted left by 8-bits.

Table 1-681. Bit field encoding: stgb_dalign_enum

Value	Name	Description
1'b0	STGB_DALIGN_LOW	Writes normally.
1'b1	STGB_DALIGN_HIGH	Writes shifted left by 8-bits.

1.3.1130 SWV_ITM_SPR_DATA[0..31]

Stimulus Port Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SWV_ITM_SPR_DATA0: 0xE000
SWV_ITM_SPR_DATA1: 0xE004
SWV_ITM_SPR_DATA2: 0xE008
SWV_ITM_SPR_DATA3: 0xE00C
SWV_ITM_SPR_DATA4: 0xE010
SWV_ITM_SPR_DATA5: 0xE014
SWV_ITM_SPR_DATA6: 0xE018
SWV_ITM_SPR_DATA7: 0xE01C
SWV_ITM_SPR_DATA8: 0xE020
SWV_ITM_SPR_DATA9: 0xE024
SWV_ITM_SPR_DATA10: 0xE028
SWV_ITM_SPR_DATA11: 0xE02C
SWV_ITM_SPR_DATA12: 0xE030
SWV_ITM_SPR_DATA13: 0xE034
SWV_ITM_SPR_DATA14: 0xE038
SWV_ITM_SPR_DATA15: 0xE03C
SWV_ITM_SPR_DATA16: 0xE040
SWV_ITM_SPR_DATA17: 0xE044
SWV_ITM_SPR_DATA18: 0xE048
SWV_ITM_SPR_DATA19: 0xE04C
SWV_ITM_SPR_DATA20: 0xE050
SWV_ITM_SPR_DATA21: 0xE054
SWV_ITM_SPR_DATA22: 0xE058
SWV_ITM_SPR_DATA23: 0xE05C
SWV_ITM_SPR_DATA24: 0xE060
SWV_ITM_SPR_DATA25: 0xE064
SWV_ITM_SPR_DATA26: 0xE068
SWV_ITM_SPR_DATA27: 0xE06C
SWV_ITM_SPR_DATA28: 0xE070
SWV_ITM_SPR_DATA29: 0xE074
SWV_ITM_SPR_DATA30: 0xE078
SWV_ITM_SPR_DATA31: 0xE07C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	SPR_BIT							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	SPR_BIT							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	SPR_BIT							

(continued)

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	SPR_BIT							

Each of the 32 stimulus ports is represented by a virtual address. A write to one of these locations causes data to be written into the FIFO if the corresponding bit in the Trace Enable Register is set and ITM is enabled. Reading from any of the stimulus ports returns the FIFO status (notFull(1) / Full(0)) only if the ITM is enabled.

Bits	Name	Description
31:0	SPR_BIT[31:0]	(no description)

1.3.1131 SWV_ITM_TER

Trace Enable Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SWV_ITM_TER: 0xEE00

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	TER_BIT							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	TER_BIT							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	TER_BIT							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	TER_BIT							

Bit mask to enable tracing on ITM stimulus ports. Each bit location corresponds to a virtual stimulus register; when a bit is set, a write to the appropriate stimulus location results in a packet being generated, except when the FIFO is full. Reset to disable all locations is 0x00000000. The setting of the bits [31:16] is ignored if secure trace is disabled. Stimulus ports 16-31 are disabled when the ability to perform secure non-invasive debug is removed. The setting of the bits [31:0] is ignored if non-secure trace is disabled. Stimulus ports 0-31 are disabled when the ability to perform non-secure non-invasive debug is removed.

Bits	Name	Description
31:0	TER_BIT[31:0]	(no description)

1.3.1132 SWV_ITM_TTR

Trace Triger Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SWV_ITM_TTR: 0xEE20

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	TER_BIT							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	TER_BIT							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	TER_BIT							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	TER_BIT							

Bit mask to enable trigger generation, TRIGOUT, on selected writes to the Stimulus Registers. Each bit in the register represents one of the virtual stimulus registers. When the bit is set, a pulse is sent on TRIGOUT when writing to the corresponding Stimulus Register. The pulse is held until TRIGOUTACK is returned, which can result in masking of multiple triggers with one acknowledgement. Triggers are not generated if trace is disabled. When secure non-invasive debug, or secure trace, is disabled, no triggers are generated for Stimulus Registers 16 to 31. If non-secure non-invasive debug, or trace, is disabled, no triggers are generated. The register is zero on reset, and the default is no triggers generated.

Bits	Name	Description
31:0	TER_BIT[31:0]	(no description)

1.3.1133 SWV_ITM_CR

Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SWV_ITM_CR: 0xEE80

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:1	R/W:0	R/W:0
HW Access	NA				R	R	R	R
Retention	NA				RET	RET	RET	RET
Name	RSVD				DWTEn	SYNCEn	TSSEn	ITMEn

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:000000						R/W:00	
HW Access	NA						R	
Retention	NA						RET	
Name	RSVD						TSPrescale	

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:0	R/W:0000000						
HW Access	R	R						
Retention	RET	RET						
Name	ITMBusy	TraceID						

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

This is the control word used to configure and control transfers through the APB interface.

Bits	Name	Description
23	ITMBusy	ITM is transmitting trace and FIFO is not empty See Table 1-683.
22:16	TraceID[6:0]	ATIDM[6:0] value See Table 1-686.
9:8	TSPrescale[1:0]	Timestamp Prescaler divide value See Table 1-687.

(continued)

3	DWTEn	Enable DWT input port See Table 1-682.
2	SYNCEn	Enable sync packets The SYNCEn bit is always 0x1 and is enabled. See Table 1-685.
1	TSSEn	Enable timestamps, delta See Table 1-688.
0	ITMEn	Enable ITM stimulus, also acts as a global enable It is recommended that the ITMEn bit is cleared and waits for the ITMBusy bit to be cleared, before changing any fields in the Control Register, otherwise the behavior can be unpredictable. See Overflow packet on page 13-4 for information about disabling the ITM overflow packets. See Table 1-684.

Table 1-682. Bit field encoding: DWT_ENUM

Value	Name	Description
1'd1	DWT_EN	Enable DWT input port Data Watchpoint and Trace (DWT) is not used in the CoreSight ITM, so the DWTEn bit is always 0x0.

Table 1-683. Bit field encoding: ITMBUSY_ENUM

Value	Name	Description
1'b1	ITMBUSY	ITM is transmitting trace and FIFO is not empty

Table 1-684. Bit field encoding: ITM_ENUM

Value	Name	Description
1'd1	ITM_EN	Enable ITM stimulus, also acts as a global enable

Table 1-685. Bit field encoding: SYNC_ENUM

Value	Name	Description
1'd1	SYNC_EN	Enable sync packets

Table 1-686. Bit field encoding: TRACEID_ENUM

Value	Name	Description
7'h0	TCID	ATIDM[6:0] value

Table 1-687. Bit field encoding: TSPRESCALE_ENUM

Value	Name	Description
2'h0	TSP_1	Timestamp Prescaler divide by 1
2'd1	TSP_4	Timestamp Prescaler divide by 4
2'd2	TSP_16	Timestamp Prescaler divide by 16
2'd3	TSP_64	Timestamp Prescaler divide by 64

Table 1-688. Bit field encoding: TSS_ENUM

Value	Name	Description
1'd1	TSS_EN	Enable timestamps, delta

1.3.1134 SWV_ITM_SCR

Synchronization Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SWV_ITM_SCR: 0xEE90

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	SyncCount							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0000				R/W:0100			
HW Access	NA				R			
Retention	NA				RET			
Name	RSVD				SyncCount			

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Synchronization packets must be output on a regular basis to provide decompression tools markers in the trace stream. The first synchronization packet is output when the ITM is enabled by setting bit [0] in the Control Register. Subsequent packets are output when the counter reaches zero, that is, decrement on data entered into the FIFO. The Synchronization Control Register represents the reloaded count value when the counter reaches zero, not the current count. This register must only be changed when the ITM is disabled.

Bits	Name	Description
11:0	SyncCount[11:0]	Counter value for time between synchronization markers See Table 1-689.

Table 1-689. Bit field encoding: SC_ENUM

Value	Name	Description
12'h400	SYNC_COUNT	Counter value for time between synchronization markers

1.3.1135 SWV_ITM_ITTOAR

Integration Test Trigger Out Acknowledge Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SWV_ITM_ITTOAR: 0xEEE4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R:0
HW Access	NA							R
Retention	NA							RET
Name	RSVD							IT-TRIGOUTACK

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	Name	Description
0	ITTRIGOUTACK	Read the value of TRIGOUTACK See Table 1-690.

Table 1-690. Bit field encoding: ITTOAR_ENUM

Value	Name	Description
1'b1	ITTRIGOUTACK	Read the value of TRIGOUTACK

1.3.1136 SWV_ITM_ITTOR

Integration Test Trigger Out Register

Reset: N/A

Register : Address

SWV_ITM_ITTOR: 0xEEE8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							W:U
HW Access	NA							R
Retention	NA							NONRET
Name	RSVD							ITTRIGOUT

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	Name	Description
0	ITTRIGOUT	Set the value of TRIGOUT See Table 1-691.

Table 1-691. Bit field encoding: ITTOR_ENUM

Value	Name	Description
1'b1	ITTRIGOUT	Set the value of TRIGOUT

1.3.1137 SWV_ITM_ITDR0

Integration Test ATB Data Register 0

Reset: N/A

Register : Address

SWV_ITM_ITDR0: 0xEEEC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						W:UU	
HW Access	NA						R	
Retention	NA						NONRET	
Name	RSVD						ITDR0	

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	Name	Description
1:0	ITDR0[1:0]	(no description) See Table 1-692.

Table 1-692. Bit field encoding: ITDR0_ENUM

Value	Name	Description
2'b01	ITATDATAM0	Set the value of ATDATAM[0]
2'b10	ITATDATAM7	Set the value of ATDATAM[7]

1.3.1138 SWV_ITM_ITCR2

Integration Test ATB Control Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SWV_ITM_ITCR2: 0xEEF0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R:1
HW Access	NA							R
Retention	NA							RET
Name	RSVD							ITCR2

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	Name	Description
0	ITCR2	Read the value of ATREADYM See Table 1-693.

Table 1-693. Bit field encoding: ITCR2_ENUM

Value	Name	Description
1'b0	ITATDATAM0	Read the value of ATREADYM

1.3.1139 SWV_ITM_ITCR1

Integration Test ATB Control Register 1

Reset: N/A

Register : Address

SWV_ITM_ITCR1: 0xEEF4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	W:UUUUUUU						
HW Access	NA	R						
Retention	NA	NONRET						
Name	RSVD	ITCR1						

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	Name	Description
6:0	ITCR1[6:0]	(no description) See Table 1-694.

Table 1-694. Bit field encoding: ITCR1_ENUM

Value	Name	Description
7'b0	ITATIDM	Set the value of ATIDM[6:0]

1.3.1140 SWV_ITM_ITCR0

Integration Test ATB Control Register 0

Reset: N/A

Register : Address

SWV_ITM_ITCR0: 0xEEF8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						W:UU	
HW Access	NA						R	
Retention	NA						NONRET	
Name	RSVD						ITCR0	

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	Name	Description
1:0	ITCR0[1:0]	(no description) See Table 1-695.

Table 1-695. Bit field encoding: ITCR0_ENUM

Value	Name	Description
2'b01	ITATVALIDM	Set the value of ITATVALIDM
2'b10	ATREADY	Set the value of ATREADY

1.3.1141 SWV_SWO_SSPS

Supported Synchronous Port Size Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SWV_SWO_SSPS: 0xF000

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R							
Retention	RET							
Name	SSPS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	R							
Retention	RET							
Name	SSPS							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:00000000							
HW Access	R							
Retention	RET							
Name	SSPS							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R:00000000							
HW Access	R							
Retention	RET							
Name	SSPS							

This register is only for implementations that implement a synchronous trace port, TRACEDATA or TRACECLK. The SWO does not support synchronous mode, so this register reads as zero.

Bits	Name	Description
31:0	SSPS[31:0]	(no description) See Table 1-696.

Table 1-696. Bit field encoding: SSPS_ENUM

Value	Name	Description
32'h0	SSPS	(no description)

1.3.1142 SWV_SWO_CSPS

Current Synchronous Port Size Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SWV_SWO_CSPS: 0xF004

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R							
Retention	RET							
Name	CSPS							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	R							
Retention	RET							
Name	CSPS							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:00000000							
HW Access	R							
Retention	RET							
Name	CSPS							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R:00000000							
HW Access	R							
Retention	RET							
Name	CSPS							

The SWO does not support synchronous mode, so this register reads as zero.

Bits	Name	Description
31:0	CSPS[31:0]	(no description) See Table 1-697.

Table 1-697. Bit field encoding: CSPS_ENUM

Value	Name	Description
32'h0	CSPS	(no description)

1.3.1143 SWV_SWO_CAOSD

Current Output Divisor Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SWV_SWO_CAOSD: 0xF010

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	CASOD							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:000			R/W:00000				
HW Access	NA			R				
Retention	NA			RET				
Name	RSVD			CASOD				

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

With this register it is possible to scale the baud rate of the SWO output. It divides TRACECLKIN, enabling it when the counter reaches the programmed value and thus reducing the baud rate of the TRACESWO pin.

Bits	Name	Description
12:0	CASOD[12:0]	Prescaler See Table 1-698.

Table 1-698. Bit field encoding: CAOSD_ENUM

Value	Name	Description
13'h0	CAOSD	13 bit prescale counter.

1.3.1144 SWV_SWO_SPP

Selected Pin Protocol Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SWV_SWO_SPP: 0xF0F0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:01	
HW Access	NA						R	
Retention	NA						RET	
Name	RSVD						SPP	

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

This register selects which protocol to use for trace outputting. The register is defined in Table 12-9 on page 12-13, and the supported values allowed in the register are determined by bits [11:9] of the Device ID Register, Table 12-7 on page 12-9. When only one protocol is supported on a component, this device is read only and set as the appropriate protocol.

Bits	Name	Description
1:0	SPP[1:0]	Select the pin protocol where multiple types are supported. The selection of unsupported protocols can result in unpredictable behavior. See Table 1-699.

Table 1-699. Bit field encoding: SPP_ENUM

Value	Name	Description
2'h01	Manchester	Single Wire Output (Manchester). This is the reset value.
2'h10	NRZ	Single Wire Output (NRZ).

1.3.1145 SWV_SWO_STM

Supported Trigger Modes Registers

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SWV_SWO_STM: 0xF100

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R:00000				
HW Access	NA			R				
Retention	NA			RET				
Name	RSVD			Multipliers				

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0000000							R:0
HW Access	NA							R
Retention	NA							RET
Name	RSVD							TCount8

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:000000						R:0	R:0
HW Access	NA						R	R
Retention	NA						RET	RET
Name	RSVD						TrgRun	Triggered

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

This register indicates the implemented Trigger Counter multipliers and other supported features of the trigger system. Because no trigger options are implemented in the SWO, this register must read as zero.

Bits	Name	Description
17	TrgRun	Trigger Counter running. A trigger has occurred but the counter is not at zero. See Table 1-701.
16	Triggered	A trigger has occurred and the counter has reached zero where implemented. See Table 1-701.
8	TCount8	8-bit wide counter register implemented. See Table 1-701.

(continued)

4:0	Multipliers[4:0]	(no description) See Table 1-700.

Table 1-700. Bit field encoding: MULT_ENUM

Value	Name	Description
5'h1	Mult2	Multiply the Trigger Counter by 2 supported.
5'h1	Mult4	Multiply the Trigger Counter by 4 supported.
5'h1	Mult16	Multiply the Trigger Counter by 16 supported.
5'h1	Mult256	Multiply the Trigger Counter by 256 supported.
5'h1	Mult64k	Multiply the Trigger Counter by 65536 supported.

Table 1-701. Bit field encoding: STM_ENUM

Value	Name	Description
1'h1	TrgRun	(no description)

1.3.1146 SWV_SWO_STPM

Supported Test Pattern and Modes Registers

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SWV_SWO_STPM: 0xF200

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R:0000			
HW Access	NA				R			
Retention	NA				RET			
Name	RSVD				Pattern			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0000000							R:0
HW Access	NA							R
Retention	NA							RET
Name	RSVD							PPat8

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:000000						R:00	
HW Access	NA						R	
Retention	NA						RET	
Name	RSVD						Mode	

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	Name	Description
17:16	Mode[1:0]	(no description) See Table 1-702.
8	PPat8	(no description) See Table 1-704.
3:0	Pattern[3:0]	(no description) See Table 1-703.

(continued)

Table 1-702. Bit field encoding: STPMM_ENUM

Value	Name	Description
2'h2	PContEn	Continuous Mode
2'h1	PtimeEn	Timed Mode

Table 1-703. Bit field encoding: STPMP_ENUM

Value	Name	Description
4'h8	FPatF0	FF/00 Pattern.
4'h4	FPatA5	AA/55 Pattern.
4'h2	FPatW1	Walking 0's Pattern.
4'h1	FPatW0	Walking 1's Pattern

Table 1-704. Bit field encoding: STPPP_ENUM

Value	Name	Description
1'h1	PPat8	8-bit Programmable Test Pattern

1.3.1147 SWV_SWO_FFS

Formatter and Flush Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SWV_SWO_FFS: 0xF300

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R:1000			
HW Access	NA				R			
Retention	NA				RET			
Name	RSVD				FFS			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	Name	Description
3:0	FFS[3:0]	(no description) See Table 1-705.

Table 1-705. Bit field encoding: FFS_ENUM

Value	Name	Description
4'h8	FtNonStop	Formatter cannot be stopped. Settings can be altered without the requirement to stop the formatter, therefore this bit remains HIGH.
4'h4	TCPresent	TRACECTL is not present, therefore this bit is tied off to 0.
4'h2	FtStopped	Formatter stopped. Because the formatter is not present, this bit always reads 0.
4'h1	FlInProg	Flush In Progress. Because flushing is not supported, this bit always reads 0.

1.3.1148 SWV_SWO_FFC

Formatter and Flush Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SWV_SWO_FFC: 0xF304

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R:000			NA:00		R:00	
HW Access	NA	R			NA		R	
Retention	NA	RET			NA		RET	
Name	RSVD	FON			RSVD		ENF	

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R:000			NA:0	R:000		
HW Access	NA	R			NA	R		
Retention	NA	RET			NA	RET		
Name	RSVD	STOP			RSVD	TRIG		

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	Name	Description
14:12	STOP[2:0]	Stop events See Table 1-708.
10:8	TRIG[2:0]	Trigger mark See Table 1-709.
6:4	FON[2:0]	FOn events See Table 1-707.

(continued)

1:0	ENF[1:0]	EnF events See Table 1-706.

Table 1-706. Bit field encoding: ENF_ENUM

Value	Name	Description
2'h2	EnFCont	Continuous Formatting, that is, data is always present. Embed in trigger packets and indicate null cycles using sync packets.
2'h1	EnFTC	Enable Formatting. Do not embed triggers into the formatted stream. Trace disable cycles and triggers are indicated where possible in the selected pin protocol.

Table 1-707. Bit field encoding: FON_ENUM

Value	Name	Description
3'h4	FOnMan	Manually generates a flush of the system. Setting this bit causes a flush to be generated. This is cleared when this flush has been serviced. This bit is clear on reset.
3'h2	FOnTrig	Generates flush using a trigger event. Set this bit to cause a flush of data in the system when a trigger event occurs.
3'h1	FOnFlIn	Generate Flush using the FLUSHIN interface. Set this bit to enable use of the FLUSHIN connection.

Table 1-708. Bit field encoding: ST_ENUM

Value	Name	Description
3'h4	StopMan	Manually stop the output of trace.
3'h2	StopTrig	Stop the formatter when a Trigger Event is observed.
3'h1	StopFl	Stop the formatter when a flush has completed, that is, return of AFREADY. This forces the FIFO to drain of any part completed packets.

Table 1-709. Bit field encoding: TRIG_ENUM

Value	Name	Description
3'h4	TrigFl	Indicate a trigger on Flush completion, that is, AFREADY is returned.
3'h2	TrigEvt	Indicates a trigger on a Trigger Event.
3'h1	TrigIn	Indicates a trigger on TRIGIN being asserted.

1.3.1149 SWV_SWO_ITDR0

Integration Test ATB Data Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SWV_SWO_ITDR0: 0xFEEC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R:00	
HW Access	NA						R	
Retention	NA						RET	
Name	RSVD						ATDATA	

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	Name	Description
1:0	ATDATA[1:0]	(no description) See Table 1-710.

Table 1-710. Bit field encoding: ATDATA_ENUM

Value	Name	Description
2'h2	ATDATA7	Reads the value of ATDATAS[7]
2'h1	ATDATA0	Reads the value of ATDATAS[0]

1.3.1150 SWV_SWO_ITCR2

Integration Test ATB Control Register 2

Reset: N/A

Register : Address

SWV_SWO_ITCR2: 0xFEF0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							W:U
HW Access	NA							R
Retention	NA							NONRET
Name	RSVD							ATREADY-DATA

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	Name	Description
0	ATREADYDATA	(no description) See Table 1-711.

Table 1-711. Bit field encoding: ATREADY_ENUM

Value	Name	Description
1'h1	ATREADY	Sets the value of ATREADYS. Topology detection register, always present

1.3.1151 SWV_SWO_ITCR0

Integration Test ATB Control Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SWV_SWO_ITCR0: 0xFEF8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R:0
HW Access	NA							R
Retention	NA							RET
Name	RSVD							ATVALID

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	Name	Description
0	ATVALID	(no description) See Table 1-712.

Table 1-712. Bit field encoding: ATVALID_ENUM

Value	Name	Description
1'h1	ATVALID	Reads the value of ATVALIDS. Topology detection register, always present

1.3.1152 SWV_SWO_ITMCR

Integration Mode Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SWV_SWO_ITMCR: 0xFF00

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Retention	NA							RET
Name	RSVD							ITCTRL

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

This register enables the component to switch from a functional mode, the default behavior, to integration mode. The ITM must be disabled and be in the idle state before setting the Integration Mode.

Bits	Name	Description
0	ITCTRL	(no description) See Table 1-713.

Table 1-713. Bit field encoding: ITCTRL_ENUM

Value	Name	Description
1'h1	ITCTRL	If set, the component reverts to an integration mode to enable topology detection or to enable integration testing. When no integration functionality has been put into a component, because it is not required, writing a HIGH to this location must be ignored and must return a LOW on read. At reset integration functionality is disabled.

1.3.1153 SWV_SWO_CTS

Claim Tag Set Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SWV_SWO_CTS: 0xFFA0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R:1111			
HW Access	NA				R			
Retention	NA				RET			
Name	RSVD				CLAIMTAG			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

The Claim Tag Set Register is used with the Claim Tag Clear Register. This register returns the number of bits that can be set on a read, and enables individual bits to be set on a write. All CoreSight components implement a minimum of a 4-bit claim tag (n=4). CoreSight ETMs implement an 8-bit claim tag field.

Bits	Name	Description
3:0	CLAIMTAG[3:0]	A bit-programmable register bank that reads the Claim Tag Value (CTV) Reads: A read returns 32'h000000FF indicating that this claim tag is eight bits wide. 32'h0000000F indicates that this claim tag is four bits wide. Logic 1 indicates that this bit can be set. Logic 0 indicates that this bit is unimplemented, that is, it cannot be set. See Table 1-714.

Table 1-714. Bit field encoding: CLAIMTAG_ENUM

Value	Name	Description
4'hF	CLAIMTAG	(no description)

1.3.1154 SWV_SWO_CTC

Claim Tag Clear Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SWV_SWO_CTC: 0xFFA4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0000			
HW Access	NA				R			
Retention	NA				RET			
Name	RSVD				CLAIMTAG			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

The Claim Tag Clear Register is used in conjunction with the Claim Tag Set Register. See Claim Tag Set Register

Bits	Name	Description
3:0	CLAIMTAG[3:0]	A bit-programmable register bank that sets the CTV. Reads: A read returns a value indicating the current claim value. This is 0 on reset. See Table 1-715.

Table 1-715. Bit field encoding: CLAIMTAGC_ENUM

Value	Name	Description
4'h0	CLAIMTAGCLEAR	(no description)

1.3.1155 SWV_SWO_LA

Lock Access Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SWV_SWO_LA: 0xFFB0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	W:00000000							
HW Access	R							
Retention	RET							
Name	LA							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	W:00000000							
HW Access	R							
Retention	RET							
Name	LA							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	W:00000000							
HW Access	R							
Retention	RET							
Name	LA							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	W:00000000							
HW Access	R							
Retention	RET							
Name	LA							

The Lock Access Register enables a write access to component registers.

Bits	Name	Description
31:0	LA[31:0]	Write Access Code. A write of 0xC5ACCE55 enables further write access to this component. An invalid write has the effect of removing write access. See Table 1-716.

Table 1-716. Bit field encoding: LA_ENUM

Value	Name	Description
32'h0	LA	(no description)

1.3.1156 SWV_SWO_LS

Lock Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SWV_SWO_LS: 0xFFB4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R:0	R:0	R:0
HW Access	NA					R	R	R
Retention	NA					RET	RET	RET
Name	RSVD					Bit	STATUS	IMP

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

The Lock Status Register indicates the status of the lock control mechanism. The Lock Status Register is used with the Lock Access Register.

Bits	Name	Description
2	Bit	Lock Register Width See Table 1-719.
1	STATUS	Device Write Access Selection See Table 1-718.
0	IMP	Lock Mechanism Selection See Table 1-717.

(continued)

Table 1-717. Bit field encoding: IMP_ENUM

Value	Name	Description
1'h0	IMP_DS	lock mechanism is not implemented.
1'h1	IMP_EN	lock mechanism is implemented.

Table 1-718. Bit field encoding: STATUS_ENUM

Value	Name	Description
1'h0	STATUS_G	device write access is granted.
1'h1	STATUS_L	device write access is locked.

Table 1-719. Bit field encoding: WD_ENUM

Value	Name	Description
1'h0	WD_32	device implements a 32-bit lock register.
1'h1	WD_8	device implements a 8-bit lock register..

1.3.1157 SWV_SWO_AS

Authentication Status Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SWV_SWO_AS: 0xFFB8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00		R:00		R:00		R:00	
HW Access	R		R		R		R	
Retention	RET		RET		RET		RET	
Name	SNDS		SIDS		NNDS		NIDS	

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

The Authentication Status Register reports the required security level and current status of the security enable bit pairs. Where functionality changes on a given security level, this change is reported in this register.

Bits	Name	Description
7:6	SNDS[1:0]	Secure noninvasive debug status See Table 1-720.
5:4	SIDS[1:0]	Secure invasive debug status See Table 1-720.
3:2	NNDS[1:0]	Nonsecure noninvasive debug status See Table 1-720.

(continued)

1:0	NIDS[1:0]	Nonsecure invasive debug status See Table 1-720.

Table 1-720. Bit field encoding: AS_ENUM

Value	Name	Description
2'h0	FUNC_N	Functionality not implemented or controlled elsewhere.
2'h2	FUNC_DS	Functionality disabled.
2'h3	FUNC_EN	Functionality enabled.

1.3.1158 SWV_SWO_DID

Device ID Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SWV_SWO_DID: 0xFFC8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:10		R:1	R/W:0	R:0000			
HW Access	R		R	R/W	R			
Retention	RET		RET	RET	RET			
Name	DID3		DID2	DID1	DID0			

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:000			R:0	R:1	R:1	R:1	R:0
HW Access	NA			R	R	R	R	R
Retention	NA			RET	RET	RET	RET	RET
Name	RSVD			DID7	DID6	DID5	DID4	DID3

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

This register indicates the capabilities of the device.

Bits	Name	Description
12	DID7	STP fitted. SWO does not support this.
11	DID6	UART NRZ Serial Wire Output support. SWO supports this mode.
10	DID5	Manchester Serial Wire Output support. SWO supports this mode.
9	DID4	Synchronous trace port not supported. SWO does not support synchronous trace port.
8:6	DID3[2:0]	FIFO Size (Power of 2).
5	DID2	Indicates the relationship between ATCLK and TRACECLKIN. The SWO always assumes the relationship is asynchronous. See Table 1-721.

(continued)

4	DID1	Enables Manual selection, so that bits [3:0] indicate the number of selectable inputs selectable on EXTCLKOUT[3:0]
3:0	DID0[3:0]	Hidden Level of input multiplexing.When non-zero this value indicates the type/number of ATB multiplexing present on the input to the ATB. This value is used to assist topology detection of the ATB structure. See Table 1-722.

Table 1-721. Bit field encoding: ASYNCATTRCLK_ENUM

Value	Name	Description
1'b1	ASYNC	ATCLK and TRACECLKIN are asynchronous clocks
1'b0	SYNC	ATCLK and TRACECLKIN are synchronous clocks

Table 1-722. Bit field encoding: HLIPMUX_ENUM

Value	Name	Description
4'b0001	FIXP	Fixed priority done by port number, bit[4] must be 0
4'b0000	NIPMP	No invisibe port multiplexing present, bit [4] must be 0

1.3.1159 SWV_SWO_DTI

Device Type Identifier Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SWV_SWO_DTI: 0xFFCC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00010001							
HW Access	R							
Retention	RET							
Name	TYPE							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

The Device Type Identifier Register enables devices to be identified by their CoreSight Class. The classifications are defined to enable any interrogating tools to obtain more information about the device in the absence of understanding the Part Number field. This information can then be reported back to the user of the debugger.

Bits	Name	Description
7:0	Device Type {TYPE[7:0]}	Bits [7:4] are assigned to Main type/class. Bits[3:0] are assigned as Sub type, for trace sources this is broken down into cores, DSPs or buses. See Table 1-723.

Table 1-723. Bit field encoding: MAINSUB_ENUM

Value	Name	Description
8'h14	MAINSUB1	Main class= Debug Control, Sub type = Cross Trigger Matrix, CTI

(continued)

Table 1-723. Bit field encoding: MAINSUB_ENUM

8'h13	MAINSUB2	Main class= Trace Source, Sub type = ETM, associated with processor or core
8'h43	MAINSUB3	Main class= Trace Source, Sub type = HTM, stimulus from bus activity
8'h12	MAINSUB4	Main class= Trace Link, Sub type = Trace Funnel
8'h21	MAINSUB5	Main class= Trace Sink, Sub type = ETB
8'h11	MAINSUB6	Main class= Trace Sink, Sub type = TPIU

1.3.1160 B[0..3]_P[0..7]_U[0..1]_PLD_IT[0..11]

PLD_IT

Reset: N/A

Register : Address

B0_P0_U0_PLD_IT0: 0x10000
B0_P0_U0_PLD_IT1: 0x10004
B0_P0_U0_PLD_IT2: 0x10008
B0_P0_U0_PLD_IT3: 0x1000C
B0_P0_U0_PLD_IT4: 0x10010
B0_P0_U0_PLD_IT5: 0x10014
B0_P0_U0_PLD_IT6: 0x10018
B0_P0_U0_PLD_IT7: 0x1001C
B0_P0_U0_PLD_IT8: 0x10020
B0_P0_U0_PLD_IT9: 0x10024
B0_P0_U0_PLD_IT10: 0x10028
B0_P0_U0_PLD_IT11: 0x1002C
B0_P0_U1_PLD_IT0: 0x10080
B0_P0_U1_PLD_IT1: 0x10084
B0_P0_U1_PLD_IT2: 0x10088
B0_P0_U1_PLD_IT3: 0x1008C
B0_P0_U1_PLD_IT4: 0x10090
B0_P0_U1_PLD_IT5: 0x10094
B0_P0_U1_PLD_IT6: 0x10098
B0_P0_U1_PLD_IT7: 0x1009C
B0_P0_U1_PLD_IT8: 0x100A0
B0_P0_U1_PLD_IT9: 0x100A4
B0_P0_U1_PLD_IT10: 0x100A8
B0_P0_U1_PLD_IT11: 0x100AC
B0_P1_U0_PLD_IT0: 0x10200
B0_P1_U0_PLD_IT1: 0x10204
B0_P1_U0_PLD_IT2: 0x10208
B0_P1_U0_PLD_IT3: 0x1020C
B0_P1_U0_PLD_IT4: 0x10210
B0_P1_U0_PLD_IT5: 0x10214
B0_P1_U0_PLD_IT6: 0x10218
B0_P1_U0_PLD_IT7: 0x1021C
B0_P1_U0_PLD_IT8: 0x10220
B0_P1_U0_PLD_IT9: 0x10224
B0_P1_U0_PLD_IT10: 0x10228
B0_P1_U0_PLD_IT11: 0x1022C
B0_P1_U1_PLD_IT0: 0x10280
B0_P1_U1_PLD_IT1: 0x10284
B0_P1_U1_PLD_IT2: 0x10288
B0_P1_U1_PLD_IT3: 0x1028C
B0_P1_U1_PLD_IT4: 0x10290
B0_P1_U1_PLD_IT5: 0x10294
B0_P1_U1_PLD_IT6: 0x10298
B0_P1_U1_PLD_IT7: 0x1029C
B0_P1_U1_PLD_IT8: 0x102A0
B0_P1_U1_PLD_IT9: 0x102A4
B0_P1_U1_PLD_IT10: 0x102A8
B0_P1_U1_PLD_IT11: 0x102AC
B0_P2_U0_PLD_IT0: 0x10400
B0_P2_U0_PLD_IT1: 0x10404
B0_P2_U0_PLD_IT2: 0x10408
B0_P2_U0_PLD_IT3: 0x1040C
B0_P2_U0_PLD_IT4: 0x10410
B0_P2_U0_PLD_IT5: 0x10414
B0_P2_U0_PLD_IT6: 0x10418
B0_P2_U0_PLD_IT7: 0x1041C
B0_P2_U0_PLD_IT8: 0x10420
B0_P2_U0_PLD_IT9: 0x10424
B0_P2_U0_PLD_IT10: 0x10428
B0_P2_U0_PLD_IT11: 0x1042C
B0_P2_U1_PLD_IT0: 0x10480
B0_P2_U1_PLD_IT1: 0x10484
B0_P2_U1_PLD_IT2: 0x10488
B0_P2_U1_PLD_IT3: 0x1048C
B0_P2_U1_PLD_IT4: 0x10490
B0_P2_U1_PLD_IT5: 0x10494

(continued)

Register : Address	
B0_P2_U1_PLD_IT6: 0x10498	B0_P2_U1_PLD_IT7: 0x1049C
B0_P2_U1_PLD_IT8: 0x104A0	B0_P2_U1_PLD_IT9: 0x104A4
B0_P2_U1_PLD_IT10: 0x104A8	B0_P2_U1_PLD_IT11: 0x104AC
B0_P3_U0_PLD_IT0: 0x10600	B0_P3_U0_PLD_IT1: 0x10604
B0_P3_U0_PLD_IT2: 0x10608	B0_P3_U0_PLD_IT3: 0x1060C
B0_P3_U0_PLD_IT4: 0x10610	B0_P3_U0_PLD_IT5: 0x10614
B0_P3_U0_PLD_IT6: 0x10618	B0_P3_U0_PLD_IT7: 0x1061C
B0_P3_U0_PLD_IT8: 0x10620	B0_P3_U0_PLD_IT9: 0x10624
B0_P3_U0_PLD_IT10: 0x10628	B0_P3_U0_PLD_IT11: 0x1062C
B0_P3_U1_PLD_IT0: 0x10680	B0_P3_U1_PLD_IT1: 0x10684
B0_P3_U1_PLD_IT2: 0x10688	B0_P3_U1_PLD_IT3: 0x1068C
B0_P3_U1_PLD_IT4: 0x10690	B0_P3_U1_PLD_IT5: 0x10694
B0_P3_U1_PLD_IT6: 0x10698	B0_P3_U1_PLD_IT7: 0x1069C
B0_P3_U1_PLD_IT8: 0x106A0	B0_P3_U1_PLD_IT9: 0x106A4
B0_P3_U1_PLD_IT10: 0x106A8	B0_P3_U1_PLD_IT11: 0x106AC
B0_P4_U0_PLD_IT0: 0x10800	B0_P4_U0_PLD_IT1: 0x10804
B0_P4_U0_PLD_IT2: 0x10808	B0_P4_U0_PLD_IT3: 0x1080C
B0_P4_U0_PLD_IT4: 0x10810	B0_P4_U0_PLD_IT5: 0x10814
B0_P4_U0_PLD_IT6: 0x10818	B0_P4_U0_PLD_IT7: 0x1081C
B0_P4_U0_PLD_IT8: 0x10820	B0_P4_U0_PLD_IT9: 0x10824
B0_P4_U0_PLD_IT10: 0x10828	B0_P4_U0_PLD_IT11: 0x1082C
B0_P4_U1_PLD_IT0: 0x10880	B0_P4_U1_PLD_IT1: 0x10884
B0_P4_U1_PLD_IT2: 0x10888	B0_P4_U1_PLD_IT3: 0x1088C
B0_P4_U1_PLD_IT4: 0x10890	B0_P4_U1_PLD_IT5: 0x10894
B0_P4_U1_PLD_IT6: 0x10898	B0_P4_U1_PLD_IT7: 0x1089C
B0_P4_U1_PLD_IT8: 0x108A0	B0_P4_U1_PLD_IT9: 0x108A4
B0_P4_U1_PLD_IT10: 0x108A8	B0_P4_U1_PLD_IT11: 0x108AC
B0_P5_U0_PLD_IT0: 0x10A00	B0_P5_U0_PLD_IT1: 0x10A04
B0_P5_U0_PLD_IT2: 0x10A08	B0_P5_U0_PLD_IT3: 0x10A0C
B0_P5_U0_PLD_IT4: 0x10A10	B0_P5_U0_PLD_IT5: 0x10A14
B0_P5_U0_PLD_IT6: 0x10A18	B0_P5_U0_PLD_IT7: 0x10A1C
B0_P5_U0_PLD_IT8: 0x10A20	B0_P5_U0_PLD_IT9: 0x10A24
B0_P5_U0_PLD_IT10: 0x10A28	B0_P5_U0_PLD_IT11: 0x10A2C
B0_P5_U1_PLD_IT0: 0x10A80	B0_P5_U1_PLD_IT1: 0x10A84
B0_P5_U1_PLD_IT2: 0x10A88	B0_P5_U1_PLD_IT3: 0x10A8C
B0_P5_U1_PLD_IT4: 0x10A90	B0_P5_U1_PLD_IT5: 0x10A94

(continued)

Register : Address

B0_P5_U1_PLD_IT6: 0x10A98
B0_P5_U1_PLD_IT7: 0x10A9C
B0_P5_U1_PLD_IT8: 0x10AA0
B0_P5_U1_PLD_IT9: 0x10AA4
B0_P5_U1_PLD_IT10: 0x10AA8
B0_P5_U1_PLD_IT11: 0x10AAC
B0_P6_U0_PLD_IT0: 0x10C00
B0_P6_U0_PLD_IT1: 0x10C04
B0_P6_U0_PLD_IT2: 0x10C08
B0_P6_U0_PLD_IT3: 0x10C0C
B0_P6_U0_PLD_IT4: 0x10C10
B0_P6_U0_PLD_IT5: 0x10C14
B0_P6_U0_PLD_IT6: 0x10C18
B0_P6_U0_PLD_IT7: 0x10C1C
B0_P6_U0_PLD_IT8: 0x10C20
B0_P6_U0_PLD_IT9: 0x10C24
B0_P6_U0_PLD_IT10: 0x10C28
B0_P6_U0_PLD_IT11: 0x10C2C
B0_P6_U1_PLD_IT0: 0x10C80
B0_P6_U1_PLD_IT1: 0x10C84
B0_P6_U1_PLD_IT2: 0x10C88
B0_P6_U1_PLD_IT3: 0x10C8C
B0_P6_U1_PLD_IT4: 0x10C90
B0_P6_U1_PLD_IT5: 0x10C94
B0_P6_U1_PLD_IT6: 0x10C98
B0_P6_U1_PLD_IT7: 0x10C9C
B0_P6_U1_PLD_IT8: 0x10CA0
B0_P6_U1_PLD_IT9: 0x10CA4
B0_P6_U1_PLD_IT10: 0x10CA8
B0_P6_U1_PLD_IT11: 0x10CAC
B0_P7_U0_PLD_IT0: 0x10E00
B0_P7_U0_PLD_IT1: 0x10E04
B0_P7_U0_PLD_IT2: 0x10E08
B0_P7_U0_PLD_IT3: 0x10E0C
B0_P7_U0_PLD_IT4: 0x10E10
B0_P7_U0_PLD_IT5: 0x10E14
B0_P7_U0_PLD_IT6: 0x10E18
B0_P7_U0_PLD_IT7: 0x10E1C
B0_P7_U0_PLD_IT8: 0x10E20
B0_P7_U0_PLD_IT9: 0x10E24
B0_P7_U0_PLD_IT10: 0x10E28
B0_P7_U0_PLD_IT11: 0x10E2C
B0_P7_U1_PLD_IT0: 0x10E80
B0_P7_U1_PLD_IT1: 0x10E84
B0_P7_U1_PLD_IT2: 0x10E88
B0_P7_U1_PLD_IT3: 0x10E8C
B0_P7_U1_PLD_IT4: 0x10E90
B0_P7_U1_PLD_IT5: 0x10E94
B0_P7_U1_PLD_IT6: 0x10E98
B0_P7_U1_PLD_IT7: 0x10E9C
B0_P7_U1_PLD_IT8: 0x10EA0
B0_P7_U1_PLD_IT9: 0x10EA4
B0_P7_U1_PLD_IT10: 0x10EA8
B0_P7_U1_PLD_IT11: 0x10EAC
B1_P2_U0_PLD_IT0: 0x11400
B1_P2_U0_PLD_IT1: 0x11404
B1_P2_U0_PLD_IT2: 0x11408
B1_P2_U0_PLD_IT3: 0x1140C
B1_P2_U0_PLD_IT4: 0x11410
B1_P2_U0_PLD_IT5: 0x11414
B1_P2_U0_PLD_IT6: 0x11418
B1_P2_U0_PLD_IT7: 0x1141C
B1_P2_U0_PLD_IT8: 0x11420
B1_P2_U0_PLD_IT9: 0x11424
B1_P2_U0_PLD_IT10: 0x11428
B1_P2_U0_PLD_IT11: 0x1142C
B1_P2_U1_PLD_IT0: 0x11480
B1_P2_U1_PLD_IT1: 0x11484
B1_P2_U1_PLD_IT2: 0x11488
B1_P2_U1_PLD_IT3: 0x1148C
B1_P2_U1_PLD_IT4: 0x11490
B1_P2_U1_PLD_IT5: 0x11494

(continued)

Register : Address	
B1_P2_U1_PLD_IT6: 0x11498	B1_P2_U1_PLD_IT7: 0x1149C
B1_P2_U1_PLD_IT8: 0x114A0	B1_P2_U1_PLD_IT9: 0x114A4
B1_P2_U1_PLD_IT10: 0x114A8	B1_P2_U1_PLD_IT11: 0x114AC
B1_P3_U0_PLD_IT0: 0x11600	B1_P3_U0_PLD_IT1: 0x11604
B1_P3_U0_PLD_IT2: 0x11608	B1_P3_U0_PLD_IT3: 0x1160C
B1_P3_U0_PLD_IT4: 0x11610	B1_P3_U0_PLD_IT5: 0x11614
B1_P3_U0_PLD_IT6: 0x11618	B1_P3_U0_PLD_IT7: 0x1161C
B1_P3_U0_PLD_IT8: 0x11620	B1_P3_U0_PLD_IT9: 0x11624
B1_P3_U0_PLD_IT10: 0x11628	B1_P3_U0_PLD_IT11: 0x1162C
B1_P3_U1_PLD_IT0: 0x11680	B1_P3_U1_PLD_IT1: 0x11684
B1_P3_U1_PLD_IT2: 0x11688	B1_P3_U1_PLD_IT3: 0x1168C
B1_P3_U1_PLD_IT4: 0x11690	B1_P3_U1_PLD_IT5: 0x11694
B1_P3_U1_PLD_IT6: 0x11698	B1_P3_U1_PLD_IT7: 0x1169C
B1_P3_U1_PLD_IT8: 0x116A0	B1_P3_U1_PLD_IT9: 0x116A4
B1_P3_U1_PLD_IT10: 0x116A8	B1_P3_U1_PLD_IT11: 0x116AC
B1_P4_U0_PLD_IT0: 0x11800	B1_P4_U0_PLD_IT1: 0x11804
B1_P4_U0_PLD_IT2: 0x11808	B1_P4_U0_PLD_IT3: 0x1180C
B1_P4_U0_PLD_IT4: 0x11810	B1_P4_U0_PLD_IT5: 0x11814
B1_P4_U0_PLD_IT6: 0x11818	B1_P4_U0_PLD_IT7: 0x1181C
B1_P4_U0_PLD_IT8: 0x11820	B1_P4_U0_PLD_IT9: 0x11824
B1_P4_U0_PLD_IT10: 0x11828	B1_P4_U0_PLD_IT11: 0x1182C
B1_P4_U1_PLD_IT0: 0x11880	B1_P4_U1_PLD_IT1: 0x11884
B1_P4_U1_PLD_IT2: 0x11888	B1_P4_U1_PLD_IT3: 0x1188C
B1_P4_U1_PLD_IT4: 0x11890	B1_P4_U1_PLD_IT5: 0x11894
B1_P4_U1_PLD_IT6: 0x11898	B1_P4_U1_PLD_IT7: 0x1189C
B1_P4_U1_PLD_IT8: 0x118A0	B1_P4_U1_PLD_IT9: 0x118A4
B1_P4_U1_PLD_IT10: 0x118A8	B1_P4_U1_PLD_IT11: 0x118AC
B1_P5_U0_PLD_IT0: 0x11A00	B1_P5_U0_PLD_IT1: 0x11A04
B1_P5_U0_PLD_IT2: 0x11A08	B1_P5_U0_PLD_IT3: 0x11A0C
B1_P5_U0_PLD_IT4: 0x11A10	B1_P5_U0_PLD_IT5: 0x11A14
B1_P5_U0_PLD_IT6: 0x11A18	B1_P5_U0_PLD_IT7: 0x11A1C
B1_P5_U0_PLD_IT8: 0x11A20	B1_P5_U0_PLD_IT9: 0x11A24
B1_P5_U0_PLD_IT10: 0x11A28	B1_P5_U0_PLD_IT11: 0x11A2C
B1_P5_U1_PLD_IT0: 0x11A80	B1_P5_U1_PLD_IT1: 0x11A84
B1_P5_U1_PLD_IT2: 0x11A88	B1_P5_U1_PLD_IT3: 0x11A8C
B1_P5_U1_PLD_IT4: 0x11A90	B1_P5_U1_PLD_IT5: 0x11A94

(continued)

Register : Address

B1_P5_U1_PLD_IT6: 0x11A98

B1_P5_U1_PLD_IT7: 0x11A9C

B1_P5_U1_PLD_IT8: 0x11AA0

B1_P5_U1_PLD_IT9: 0x11AA4

B1_P5_U1_PLD_IT10: 0x11AA8

B1_P5_U1_PLD_IT11: 0x11AAC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U
HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U
HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U
HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U
HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Complement input term byte

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term.
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term.
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term.
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term.
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term.
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term.

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term.
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term.
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term.
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term.
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term.
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term.
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term.
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term.
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term.
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term.
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term
3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term

1.3.1161 B[0..3]_P[0..7]_U[0..1]_PLD_ORT[0..3]

PLD_ORT

Reset: N/A

Register : Address

B0_P0_U0_PLD_ORT0: 0x10030
B0_P0_U0_PLD_ORT1: 0x10032
B0_P0_U0_PLD_ORT2: 0x10034
B0_P0_U0_PLD_ORT3: 0x10036
B0_P0_U1_PLD_ORT0: 0x100B0
B0_P0_U1_PLD_ORT1: 0x100B2
B0_P0_U1_PLD_ORT2: 0x100B4
B0_P0_U1_PLD_ORT3: 0x100B6
B0_P1_U0_PLD_ORT0: 0x10230
B0_P1_U0_PLD_ORT1: 0x10232
B0_P1_U0_PLD_ORT2: 0x10234
B0_P1_U0_PLD_ORT3: 0x10236
B0_P1_U1_PLD_ORT0: 0x102B0
B0_P1_U1_PLD_ORT1: 0x102B2
B0_P1_U1_PLD_ORT2: 0x102B4
B0_P1_U1_PLD_ORT3: 0x102B6
B0_P2_U0_PLD_ORT0: 0x10430
B0_P2_U0_PLD_ORT1: 0x10432
B0_P2_U0_PLD_ORT2: 0x10434
B0_P2_U0_PLD_ORT3: 0x10436
B0_P2_U1_PLD_ORT0: 0x104B0
B0_P2_U1_PLD_ORT1: 0x104B2
B0_P2_U1_PLD_ORT2: 0x104B4
B0_P2_U1_PLD_ORT3: 0x104B6
B0_P3_U0_PLD_ORT0: 0x10630
B0_P3_U0_PLD_ORT1: 0x10632
B0_P3_U0_PLD_ORT2: 0x10634
B0_P3_U0_PLD_ORT3: 0x10636
B0_P3_U1_PLD_ORT0: 0x106B0
B0_P3_U1_PLD_ORT1: 0x106B2
B0_P3_U1_PLD_ORT2: 0x106B4
B0_P3_U1_PLD_ORT3: 0x106B6
B0_P4_U0_PLD_ORT0: 0x10830
B0_P4_U0_PLD_ORT1: 0x10832
B0_P4_U0_PLD_ORT2: 0x10834
B0_P4_U0_PLD_ORT3: 0x10836
B0_P4_U1_PLD_ORT0: 0x108B0
B0_P4_U1_PLD_ORT1: 0x108B2
B0_P4_U1_PLD_ORT2: 0x108B4
B0_P4_U1_PLD_ORT3: 0x108B6
B0_P5_U0_PLD_ORT0: 0x10A30
B0_P5_U0_PLD_ORT1: 0x10A32
B0_P5_U0_PLD_ORT2: 0x10A34
B0_P5_U0_PLD_ORT3: 0x10A36
B0_P5_U1_PLD_ORT0: 0x10AB0
B0_P5_U1_PLD_ORT1: 0x10AB2
B0_P5_U1_PLD_ORT2: 0x10AB4
B0_P5_U1_PLD_ORT3: 0x10AB6
B0_P6_U0_PLD_ORT0: 0x10C30
B0_P6_U0_PLD_ORT1: 0x10C32
B0_P6_U0_PLD_ORT2: 0x10C34
B0_P6_U0_PLD_ORT3: 0x10C36
B0_P6_U1_PLD_ORT0: 0x10CB0
B0_P6_U1_PLD_ORT1: 0x10CB2
B0_P6_U1_PLD_ORT2: 0x10CB4
B0_P6_U1_PLD_ORT3: 0x10CB6
B0_P7_U0_PLD_ORT0: 0x10E30
B0_P7_U0_PLD_ORT1: 0x10E32
B0_P7_U0_PLD_ORT2: 0x10E34
B0_P7_U0_PLD_ORT3: 0x10E36
B0_P7_U1_PLD_ORT0: 0x10EB0
B0_P7_U1_PLD_ORT1: 0x10EB2
B0_P7_U1_PLD_ORT2: 0x10EB4
B0_P7_U1_PLD_ORT3: 0x10EB6
B1_P2_U0_PLD_ORT0: 0x11430
B1_P2_U0_PLD_ORT1: 0x11432

(continued)

Register : Address

B1_P2_U0_PLD_ORT2: 0x11434
B1_P2_U0_PLD_ORT3: 0x11436
B1_P2_U1_PLD_ORT0: 0x114B0
B1_P2_U1_PLD_ORT1: 0x114B2
B1_P2_U1_PLD_ORT2: 0x114B4
B1_P2_U1_PLD_ORT3: 0x114B6
B1_P3_U0_PLD_ORT0: 0x11630
B1_P3_U0_PLD_ORT1: 0x11632
B1_P3_U0_PLD_ORT2: 0x11634
B1_P3_U0_PLD_ORT3: 0x11636
B1_P3_U1_PLD_ORT0: 0x116B0
B1_P3_U1_PLD_ORT1: 0x116B2
B1_P3_U1_PLD_ORT2: 0x116B4
B1_P3_U1_PLD_ORT3: 0x116B6
B1_P4_U0_PLD_ORT0: 0x11830
B1_P4_U0_PLD_ORT1: 0x11832
B1_P4_U0_PLD_ORT2: 0x11834
B1_P4_U0_PLD_ORT3: 0x11836
B1_P4_U1_PLD_ORT0: 0x118B0
B1_P4_U1_PLD_ORT1: 0x118B2
B1_P4_U1_PLD_ORT2: 0x118B4
B1_P4_U1_PLD_ORT3: 0x118B6
B1_P5_U0_PLD_ORT0: 0x11A30
B1_P5_U0_PLD_ORT1: 0x11A32
B1_P5_U0_PLD_ORT2: 0x11A34
B1_P5_U0_PLD_ORT3: 0x11A36
B1_P5_U1_PLD_ORT0: 0x11AB0
B1_P5_U1_PLD_ORT1: 0x11AB2
B1_P5_U1_PLD_ORT2: 0x11AB4
B1_P5_U1_PLD_ORT3: 0x11AB6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U
HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	PLD0_ORT_PTx_7	PLD0_ORT_PTx_6	PLD0_ORT_PTx_5	PLD0_ORT_PTx_4	PLD0_ORT_PTx_3	PLD0_ORT_PTx_2	PLD0_ORT_PTx_1	PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U
HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	PLD1_ORT_PTx_7	PLD1_ORT_PTx_6	PLD1_ORT_PTx_5	PLD1_ORT_PTx_4	PLD1_ORT_PTx_3	PLD1_ORT_PTx_2	PLD1_ORT_PTx_1	PLD1_ORT_PTx_0

OR term byte

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term.
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term.
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term.
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term.
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term.
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term.

(continued)

9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term.
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term.
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term.
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term.
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term.
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term.
3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term.
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term.
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term.
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term.

1.3.1162 B[0..3]_P[0..7]_U[0..1]_MC_CFG_CEN_CONST

MC_CFG_CEN_CONST

Reset: N/A

Register : Address

B0_P0_U0_MC_CFG_CEN_CONST: 0x10038

B0_P0_U1_MC_CFG_CEN_CONST: 0x100B8

B0_P1_U0_MC_CFG_CEN_CONST: 0x10238

B0_P1_U1_MC_CFG_CEN_CONST: 0x102B8

B0_P2_U0_MC_CFG_CEN_CONST: 0x10438

B0_P2_U1_MC_CFG_CEN_CONST: 0x104B8

B0_P3_U0_MC_CFG_CEN_CONST: 0x10638

B0_P3_U1_MC_CFG_CEN_CONST: 0x106B8

B0_P4_U0_MC_CFG_CEN_CONST: 0x10838

B0_P4_U1_MC_CFG_CEN_CONST: 0x108B8

B0_P5_U0_MC_CFG_CEN_CONST: 0x10A38

B0_P5_U1_MC_CFG_CEN_CONST: 0x10AB8

B0_P6_U0_MC_CFG_CEN_CONST: 0x10C38

B0_P6_U1_MC_CFG_CEN_CONST: 0x10CB8

B0_P7_U0_MC_CFG_CEN_CONST: 0x10E38

B0_P7_U1_MC_CFG_CEN_CONST: 0x10EB8

B1_P2_U0_MC_CFG_CEN_CONST: 0x11438

B1_P2_U1_MC_CFG_CEN_CONST: 0x114B8

B1_P3_U0_MC_CFG_CEN_CONST: 0x11638

B1_P3_U1_MC_CFG_CEN_CONST: 0x116B8

B1_P4_U0_MC_CFG_CEN_CONST: 0x11838

B1_P4_U1_MC_CFG_CEN_CONST: 0x118B8

B1_P5_U0_MC_CFG_CEN_CONST: 0x11A38

B1_P5_U1_MC_CFG_CEN_CONST: 0x11AB8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U
HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	PLD0_MC3_DFF_C	PLD0_MC3_CEN	PLD0_MC2_DFF_C	PLD0_MC2_CEN	PLD0_MC1_DFF_C	PLD0_MC1_CEN	PLD0_MC0_DFF_C	PLD0_MC0_CEN

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U

(continued)

HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	PLD1_MC3_DFF_C	PLD1_MC3_CEN	PLD1_MC2_DFF_C	PLD1_MC2_CEN	PLD1_MC1_DFF_C	PLD1_MC1_CEN	PLD1_MC0_DFF_C	PLD1_MC0_CEN

Macrocell configuration for Carry Enable and Constant

Bits	Name	Description
15	PLD1_MC3_DFF_C	DFF Constant See Table 1-725.
14	PLD1_MC3_CEN	Carry enable See Table 1-724.
13	PLD1_MC2_DFF_C	DFF Constant See Table 1-725.
12	PLD1_MC2_CEN	Carry enable See Table 1-724.
11	PLD1_MC1_DFF_C	DFF Constant See Table 1-725.
10	PLD1_MC1_CEN	Carry enable See Table 1-724.
9	PLD1_MC0_DFF_C	DFF Constant See Table 1-725.
8	PLD1_MC0_CEN	Carry enable See Table 1-724.
7	PLD0_MC3_DFF_C	DFF Constant See Table 1-725.
6	PLD0_MC3_CEN	Carry enable See Table 1-724.
5	PLD0_MC2_DFF_C	DFF Constant See Table 1-725.
4	PLD0_MC2_CEN	Carry enable See Table 1-724.
3	PLD0_MC1_DFF_C	DFF Constant See Table 1-725.
2	PLD0_MC1_CEN	Carry enable See Table 1-724.
1	PLD0_MC0_DFF_C	DFF Constant See Table 1-725.

(continued)

0	PLD0_MC0_CEN	Carry enable See Table 1-724.

Table 1-724. Bit field encoding: CEN_ENUM

Value	Name	Description
1'b0	DISABLE	Disabled
1'b1	ENABLE	Enabled

Table 1-725. Bit field encoding: DFF_ENUM

Value	Name	Description
1'b0	TRUE	DFF non-inverted
1'b1	INVERTED	DFF inverted

1.3.1163 B[0..3]_P[0..7]_U[0..1]_MC_CFG_XORFB

MC_CFG_XORFB

Reset: N/A

Register : Address

B0_P0_U0_MC_CFG_XORFB: 0x1003A

B0_P0_U1_MC_CFG_XORFB: 0x100BA

B0_P1_U0_MC_CFG_XORFB: 0x1023A

B0_P1_U1_MC_CFG_XORFB: 0x102BA

B0_P2_U0_MC_CFG_XORFB: 0x1043A

B0_P2_U1_MC_CFG_XORFB: 0x104BA

B0_P3_U0_MC_CFG_XORFB: 0x1063A

B0_P3_U1_MC_CFG_XORFB: 0x106BA

B0_P4_U0_MC_CFG_XORFB: 0x1083A

B0_P4_U1_MC_CFG_XORFB: 0x108BA

B0_P5_U0_MC_CFG_XORFB: 0x10A3A

B0_P5_U1_MC_CFG_XORFB: 0x10ABA

B0_P6_U0_MC_CFG_XORFB: 0x10C3A

B0_P6_U1_MC_CFG_XORFB: 0x10CBA

B0_P7_U0_MC_CFG_XORFB: 0x10E3A

B0_P7_U1_MC_CFG_XORFB: 0x10EBA

B1_P2_U0_MC_CFG_XORFB: 0x1143A

B1_P2_U1_MC_CFG_XORFB: 0x114BA

B1_P3_U0_MC_CFG_XORFB: 0x1163A

B1_P3_U1_MC_CFG_XORFB: 0x116BA

B1_P4_U0_MC_CFG_XORFB: 0x1183A

B1_P4_U1_MC_CFG_XORFB: 0x118BA

B1_P5_U0_MC_CFG_XORFB: 0x11A3A

B1_P5_U1_MC_CFG_XORFB: 0x11ABA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UU		R/W:UU		R/W:UU		R/W:UU	
HW Access	R		R		R		R	
Retention	RET		RET		RET		RET	
Name	PLD0_MC3_XORFB		PLD0_MC2_XORFB		PLD0_MC1_XORFB		PLD0_MC0_XORFB	

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UU		R/W:UU		R/W:UU		R/W:UU	
HW Access	R		R		R		R	

(continued)

Retention	RET	RET	RET	RET
Name	PLD1_MC3_XORFB	PLD1_MC2_XORFB	PLD1_MC1_XORFB	PLD1_MC0_XORFB

Macrocell configuration for XOR feedback

Bits	Name	Description
15:14	PLD1_MC3_XORFB[1:0]	XOR feedback See Table 1-726.
13:12	PLD1_MC2_XORFB[1:0]	XOR feedback See Table 1-726.
11:10	PLD1_MC1_XORFB[1:0]	XOR feedback See Table 1-726.
9:8	PLD1_MC0_XORFB[1:0]	XOR feedback See Table 1-726.
7:6	PLD0_MC3_XORFB[1:0]	XOR feedback See Table 1-726.
5:4	PLD0_MC2_XORFB[1:0]	XOR feedback See Table 1-726.
3:2	PLD0_MC1_XORFB[1:0]	XOR feedback See Table 1-726.
1:0	PLD0_MC0_XORFB[1:0]	XOR feedback See Table 1-726.

Table 1-726. Bit field encoding: XORFB_ENUM

Value	Name	Description
2'b00	DFF	DFF
2'b01	CARRY	Carry
2'b10	TFF_H	TFF on high
2'b11	TFF_L	TFF on low

1.3.1164 B[0..3]_P[0..7]_U[0..1]_MC_CFG_SET_RESET

MC_CFG_SET_RESET

Reset: N/A

Register : Address

B0_P0_U0_MC_CFG_SET_RESET: 0x1003C

B0_P0_U1_MC_CFG_SET_RESET: 0x100BC

B0_P1_U0_MC_CFG_SET_RESET: 0x1023C

B0_P1_U1_MC_CFG_SET_RESET: 0x102BC

B0_P2_U0_MC_CFG_SET_RESET: 0x1043C

B0_P2_U1_MC_CFG_SET_RESET: 0x104BC

B0_P3_U0_MC_CFG_SET_RESET: 0x1063C

B0_P3_U1_MC_CFG_SET_RESET: 0x106BC

B0_P4_U0_MC_CFG_SET_RESET: 0x1083C

B0_P4_U1_MC_CFG_SET_RESET: 0x108BC

B0_P5_U0_MC_CFG_SET_RESET: 0x10A3C

B0_P5_U1_MC_CFG_SET_RESET: 0x10ABC

B0_P6_U0_MC_CFG_SET_RESET: 0x10C3C

B0_P6_U1_MC_CFG_SET_RESET: 0x10CBC

B0_P7_U0_MC_CFG_SET_RESET: 0x10E3C

B0_P7_U1_MC_CFG_SET_RESET: 0x10EBC

B1_P2_U0_MC_CFG_SET_RESET: 0x1143C

B1_P2_U1_MC_CFG_SET_RESET: 0x114BC

B1_P3_U0_MC_CFG_SET_RESET: 0x1163C

B1_P3_U1_MC_CFG_SET_RESET: 0x116BC

B1_P4_U0_MC_CFG_SET_RESET: 0x1183C

B1_P4_U1_MC_CFG_SET_RESET: 0x118BC

B1_P5_U0_MC_CFG_SET_RESET: 0x11A3C

B1_P5_U1_MC_CFG_SET_RESET: 0x11ABC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U
HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	PLD0_MC3_RESET_SEL	PLD0_MC3_SET_SEL	PLD0_MC2_RESET_SEL	PLD0_MC2_SET_SEL	PLD0_MC1_RESET_SEL	PLD0_MC1_SET_SEL	PLD0_MC0_RESET_SEL	PLD0_MC0_SET_SEL

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U	R/W:U

(continued)

HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	PLD1_MC3_RESET_SEL	PLD1_MC3_SET_SEL	PLD1_MC2_RESET_SEL	PLD1_MC2_SET_SEL	PLD1_MC1_RESET_SEL	PLD1_MC1_SET_SEL	PLD1_MC0_RESET_SEL	PLD1_MC0_SET_SEL

Macrocell configuration for set and reset

Bits	Name	Description
15	PLD1_MC3_RESET_SEL	Reset select enable See Table 1-727.
14	PLD1_MC3_SET_SEL	Set select enable See Table 1-728.
13	PLD1_MC2_RESET_SEL	Reset select enable See Table 1-727.
12	PLD1_MC2_SET_SEL	Set select enable See Table 1-728.
11	PLD1_MC1_RESET_SEL	Reset select enable See Table 1-727.
10	PLD1_MC1_SET_SEL	Set select enable See Table 1-728.
9	PLD1_MC0_RESET_SEL	Reset select enable See Table 1-727.
8	PLD1_MC0_SET_SEL	Set select enable See Table 1-728.
7	PLD0_MC3_RESET_SEL	Reset select enable See Table 1-727.
6	PLD0_MC3_SET_SEL	Set select enable See Table 1-728.
5	PLD0_MC2_RESET_SEL	Reset select enable See Table 1-727.
4	PLD0_MC2_SET_SEL	Set select enable See Table 1-728.
3	PLD0_MC1_RESET_SEL	Reset select enable See Table 1-727.
2	PLD0_MC1_SET_SEL	Set select enable See Table 1-728.

(continued)

1	PLD0_MC0_RESET_SEL	Reset select enable See Table 1-727.
0	PLD0_MC0_SET_SEL	Set select enable See Table 1-728.

Table 1-727. Bit field encoding: RESET_SEL_ENUM

Value	Name	Description
1'b0	DISABLE	Reset not used
1'b1	ENABLE	Reset enabled

Table 1-728. Bit field encoding: SET_SEL_ENUM

Value	Name	Description
1'b0	DISABLE	Set not used
1'b1	ENABLE	Set reset enabled

1.3.1165 B[0..3]_P[0..7]_U[0..1]_MC_CFG_BYPASS

MC_CFG_BYPASS

Reset: N/A

Register : Address

B0_P0_U0_MC_CFG_BYPASS: 0x1003E

B0_P0_U1_MC_CFG_BYPASS: 0x100BE

B0_P1_U0_MC_CFG_BYPASS: 0x1023E

B0_P1_U1_MC_CFG_BYPASS: 0x102BE

B0_P2_U0_MC_CFG_BYPASS: 0x1043E

B0_P2_U1_MC_CFG_BYPASS: 0x104BE

B0_P3_U0_MC_CFG_BYPASS: 0x1063E

B0_P3_U1_MC_CFG_BYPASS: 0x106BE

B0_P4_U0_MC_CFG_BYPASS: 0x1083E

B0_P4_U1_MC_CFG_BYPASS: 0x108BE

B0_P5_U0_MC_CFG_BYPASS: 0x10A3E

B0_P5_U1_MC_CFG_BYPASS: 0x10ABE

B0_P6_U0_MC_CFG_BYPASS: 0x10C3E

B0_P6_U1_MC_CFG_BYPASS: 0x10CBE

B0_P7_U0_MC_CFG_BYPASS: 0x10E3E

B0_P7_U1_MC_CFG_BYPASS: 0x10EBE

B1_P2_U0_MC_CFG_BYPASS: 0x1143E

B1_P2_U1_MC_CFG_BYPASS: 0x114BE

B1_P3_U0_MC_CFG_BYPASS: 0x1163E

B1_P3_U1_MC_CFG_BYPASS: 0x116BE

B1_P4_U0_MC_CFG_BYPASS: 0x1183E

B1_P4_U1_MC_CFG_BYPASS: 0x118BE

B1_P5_U0_MC_CFG_BYPASS: 0x11A3E

B1_P5_U1_MC_CFG_BYPASS: 0x11ABE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:U	NA:0	R/W:U	NA:0	R/W:U	NA:0	R/W:U
HW Access	NA	R	NA	R	NA	R	NA	R
Retention	NA	RET	NA	RET	NA	RET	NA	RET
Name	RSVD	PLD0_MC3_BYPASS	RSVD	PLD0_MC2_BYPASS	RSVD	PLD0_MC1_BYPASS	RSVD	PLD0_MC0_BYPASS

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0	R/W:U	NA:0	R/W:U	NA:0	R/W:U	NA:0	R/W:U

(continued)

HW Access	NA	R	NA	R	NA	R	NA	R
Retention	NA	RET	NA	RET	NA	RET	NA	RET
Name	RSVD	PLD1_MC3 _BYPASS	RSVD	PLD1_MC2 _BYPASS	RSVD	PLD1_MC1 _BYPASS	RSVD	PLD1_MC0 _BYPASS

Macrocell configuration for bypass

Bits	Name	Description
14	PLD1_MC3_BYPASS	Bypass selection See Table 1-729.
12	PLD1_MC2_BYPASS	Bypass selection See Table 1-729.
10	PLD1_MC1_BYPASS	Bypass selection See Table 1-729.
8	PLD1_MC0_BYPASS	Bypass selection See Table 1-729.
6	PLD0_MC3_BYPASS	Bypass selection See Table 1-729.
4	PLD0_MC2_BYPASS	Bypass selection See Table 1-729.
2	PLD0_MC1_BYPASS	Bypass selection See Table 1-729.
0	PLD0_MC0_BYPASS	Bypass selection See Table 1-729.

Table 1-729. Bit field encoding: BYPASS_ENUM

Value	Name	Description
1'b0	REGISTER	Registered output
1'b1	COMBINATIONAL	Combinational output

1.3.1166 B[0..3]_P[0..7]_U[0..1]_CFG0

CFG0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG0: 0x10040
B0_P1_U0_CFG0: 0x10240
B0_P2_U0_CFG0: 0x10440
B0_P3_U0_CFG0: 0x10640
B0_P4_U0_CFG0: 0x10840
B0_P5_U0_CFG0: 0x10A40
B0_P6_U0_CFG0: 0x10C40
B0_P7_U0_CFG0: 0x10E40
B1_P2_U0_CFG0: 0x11440
B1_P3_U0_CFG0: 0x11640
B1_P4_U0_CFG0: 0x11840
B1_P5_U0_CFG0: 0x11A40
B0_P0_U1_CFG0: 0x100C0
B0_P1_U1_CFG0: 0x102C0
B0_P2_U1_CFG0: 0x104C0
B0_P3_U1_CFG0: 0x106C0
B0_P4_U1_CFG0: 0x108C0
B0_P5_U1_CFG0: 0x10AC0
B0_P6_U1_CFG0: 0x10CC0
B0_P7_U1_CFG0: 0x10EC0
B1_P2_U1_CFG0: 0x114C0
B1_P3_U1_CFG0: 0x116C0
B1_P4_U1_CFG0: 0x118C0
B1_P5_U1_CFG0: 0x11AC0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:000			NA:0	R/W:000		
HW Access	NA	R			NA	R		
Retention	NA	RET			NA	RET		
Name	RSVD	RAD1			RSVD	RAD0		

Datapath Input Selection - RAD1 RAD0. Address bits 0 and 1 to the dynamic configuration RAM

Bits	Name	Description
6:4	RAD1[2:0]	Datapath Permutable Input Mux See Table 1-730.
2:0	RAD0[2:0]	Datapath Permutable Input Mux See Table 1-730.

Table 1-730. Bit field encoding: DP_INPUT_MUX_ENUM

Value	Name	Description
3'b000	OFF	Input off
3'b001	DP_IN0	Set to dp_in[0]
3'b010	DP_IN1	Set to dp_in[1]
3'b011	DP_IN2	Set to dp_in[2]
3'b100	DP_IN3	Set to dp_in[3]
3'b101	DP_IN4	Set to dp_in[4]
3'b110	DP_IN5	Set to dp_in[5]
3'b111	RESERVED	Reserved

1.3.1167 B[0..3]_P[0..7]_U[0..1]_CFG1

CFG1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG1: 0x10041
B0_P1_U0_CFG1: 0x10241
B0_P2_U0_CFG1: 0x10441
B0_P3_U0_CFG1: 0x10641
B0_P4_U0_CFG1: 0x10841
B0_P5_U0_CFG1: 0x10A41
B0_P6_U0_CFG1: 0x10C41
B0_P7_U0_CFG1: 0x10E41
B1_P2_U0_CFG1: 0x11441
B1_P3_U0_CFG1: 0x11641
B1_P4_U0_CFG1: 0x11841
B1_P5_U0_CFG1: 0x11A41
B0_P0_U1_CFG1: 0x100C1
B0_P1_U1_CFG1: 0x102C1
B0_P2_U1_CFG1: 0x104C1
B0_P3_U1_CFG1: 0x106C1
B0_P4_U1_CFG1: 0x108C1
B0_P5_U1_CFG1: 0x10AC1
B0_P6_U1_CFG1: 0x10CC1
B0_P7_U1_CFG1: 0x10EC1
B1_P2_U1_CFG1: 0x114C1
B1_P3_U1_CFG1: 0x116C1
B1_P4_U1_CFG1: 0x118C1
B1_P5_U1_CFG1: 0x11AC1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00000					R/W:000		
HW Access	NA					R		
Retention	NA					RET		
Name	RSVD					RAD2		

Datapath Input Selection - RAD2. Address bit 2 to the dynamic configuration RAM

Bits	Name	Description
2:0	RAD2[2:0]	Datapath Permutable Input Mux See Table 1-731.

Table 1-731. Bit field encoding: DP_INPUT_MUX_ENUM

Value	Name	Description
3'b000	OFF	Input off
3'b001	DP_IN0	Set to dp_in[0]
3'b010	DP_IN1	Set to dp_in[1]
3'b011	DP_IN2	Set to dp_in[2]
3'b100	DP_IN3	Set to dp_in[3]
3'b101	DP_IN4	Set to dp_in[4]
3'b110	DP_IN5	Set to dp_in[5]
3'b111	RESERVED	Reserved

1.3.1168 B[0..3]_P[0..7]_U[0..1]_CFG2

CFG2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG2: 0x10042
B0_P1_U0_CFG2: 0x10242
B0_P2_U0_CFG2: 0x10442
B0_P3_U0_CFG2: 0x10642
B0_P4_U0_CFG2: 0x10842
B0_P5_U0_CFG2: 0x10A42
B0_P6_U0_CFG2: 0x10C42
B0_P7_U0_CFG2: 0x10E42
B1_P2_U0_CFG2: 0x11442
B1_P3_U0_CFG2: 0x11642
B1_P4_U0_CFG2: 0x11842
B1_P5_U0_CFG2: 0x11A42
B0_P0_U1_CFG2: 0x100C2
B0_P1_U1_CFG2: 0x102C2
B0_P2_U1_CFG2: 0x104C2
B0_P3_U1_CFG2: 0x106C2
B0_P4_U1_CFG2: 0x108C2
B0_P5_U1_CFG2: 0x10AC2
B0_P6_U1_CFG2: 0x10CC2
B0_P7_U1_CFG2: 0x10EC2
B1_P2_U1_CFG2: 0x114C2
B1_P3_U1_CFG2: 0x116C2
B1_P4_U1_CFG2: 0x118C2
B1_P5_U1_CFG2: 0x11AC2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:000			NA:0	R/W:000		
HW Access	NA	R			NA	R		
Retention	NA	RET			NA	RET		
Name	RSVD	F1_LD			RSVD	F0_LD		

Datapath Input Selection - F1_LD F0_LD. FIFO load strobes. When in input mode, the FIFO loads from the system bus. When in output mode, the FIFOs load from either the A0, A1 or the ALU

Bits	Name	Description
6:4	F1_LD[2:0]	Datapath Permutable Input Mux See Table 1-732.
2:0	F0_LD[2:0]	Datapath Permutable Input Mux See Table 1-732.

Table 1-732. Bit field encoding: DP_INPUT_MUX_ENUM

Value	Name	Description
3'b000	OFF	Input off
3'b001	DP_IN0	Set to dp_in[0]
3'b010	DP_IN1	Set to dp_in[1]
3'b011	DP_IN2	Set to dp_in[2]
3'b100	DP_IN3	Set to dp_in[3]
3'b101	DP_IN4	Set to dp_in[4]
3'b110	DP_IN5	Set to dp_in[5]
3'b111	RESERVED	Reserved

1.3.1169 B[0..3]_P[0..7]_U[0..1]_CFG3

CFG3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG3: 0x10043
B0_P1_U0_CFG3: 0x10243
B0_P2_U0_CFG3: 0x10443
B0_P3_U0_CFG3: 0x10643
B0_P4_U0_CFG3: 0x10843
B0_P5_U0_CFG3: 0x10A43
B0_P6_U0_CFG3: 0x10C43
B0_P7_U0_CFG3: 0x10E43
B1_P2_U0_CFG3: 0x11443
B1_P3_U0_CFG3: 0x11643
B1_P4_U0_CFG3: 0x11843
B1_P5_U0_CFG3: 0x11A43
B0_P0_U1_CFG3: 0x100C3
B0_P1_U1_CFG3: 0x102C3
B0_P2_U1_CFG3: 0x104C3
B0_P3_U1_CFG3: 0x106C3
B0_P4_U1_CFG3: 0x108C3
B0_P5_U1_CFG3: 0x10AC3
B0_P6_U1_CFG3: 0x10CC3
B0_P7_U1_CFG3: 0x10EC3
B1_P2_U1_CFG3: 0x114C3
B1_P3_U1_CFG3: 0x116C3
B1_P4_U1_CFG3: 0x118C3
B1_P5_U1_CFG3: 0x11AC3

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:000			NA:0	R/W:000		
HW Access	NA	R			NA	R		
Retention	NA	RET			NA	RET		
Name	RSVD	D1_LD			RSVD	D0_LD		

Datapath Input Selection - D1_LD D0_LD. Data Register load strobes. These are edge sensitive signals. On the positive edge, a byte is transferred from the associated FIFO to the Data Register.

Bits	Name	Description
6:4	D1_LD[2:0]	Datapath Permutable Input Mux See Table 1-733.
2:0	D0_LD[2:0]	Datapath Permutable Input Mux See Table 1-733.

Table 1-733. Bit field encoding: DP_INPUT_MUX_ENUM

Value	Name	Description
3'b000	OFF	Input off
3'b001	DP_IN0	Set to dp_in[0]
3'b010	DP_IN1	Set to dp_in[1]
3'b011	DP_IN2	Set to dp_in[2]
3'b100	DP_IN3	Set to dp_in[3]
3'b101	DP_IN4	Set to dp_in[4]
3'b110	DP_IN5	Set to dp_in[5]
3'b111	RESERVED	Reserved

1.3.1170 B[0..3]_P[0..7]_U[0..1]_CFG4

CFG4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG4: 0x10044
B0_P1_U0_CFG4: 0x10244
B0_P2_U0_CFG4: 0x10444
B0_P3_U0_CFG4: 0x10644
B0_P4_U0_CFG4: 0x10844
B0_P5_U0_CFG4: 0x10A44
B0_P6_U0_CFG4: 0x10C44
B0_P7_U0_CFG4: 0x10E44
B1_P2_U0_CFG4: 0x11444
B1_P3_U0_CFG4: 0x11644
B1_P4_U0_CFG4: 0x11844
B1_P5_U0_CFG4: 0x11A44

B0_P0_U1_CFG4: 0x100C4
B0_P1_U1_CFG4: 0x102C4
B0_P2_U1_CFG4: 0x104C4
B0_P3_U1_CFG4: 0x106C4
B0_P4_U1_CFG4: 0x108C4
B0_P5_U1_CFG4: 0x10AC4
B0_P6_U1_CFG4: 0x10CC4
B0_P7_U1_CFG4: 0x10EC4
B1_P2_U1_CFG4: 0x114C4
B1_P3_U1_CFG4: 0x116C4
B1_P4_U1_CFG4: 0x118C4
B1_P5_U1_CFG4: 0x11AC4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:000			NA:0	R/W:000		
HW Access	NA	R			NA	R		
Retention	NA	RET			NA	RET		
Name	RSVD	CI_MUX			RSVD	SI_MUX		

Datapath Input Selection - CI_MUX SI_MUX. Carry In data and Shift In data from routing

Bits	Name	Description
6:4	CI_MUX[2:0]	Datapath Permutable Input Mux See Table 1-734.
2:0	SI_MUX[2:0]	Datapath Permutable Input Mux See Table 1-734.

Table 1-734. Bit field encoding: DP_INPUT_MUX_ENUM

Value	Name	Description
3'b000	OFF	Input off
3'b001	DP_IN0	Set to dp_in[0]
3'b010	DP_IN1	Set to dp_in[1]
3'b011	DP_IN2	Set to dp_in[2]
3'b100	DP_IN3	Set to dp_in[3]
3'b101	DP_IN4	Set to dp_in[4]
3'b110	DP_IN5	Set to dp_in[5]
3'b111	RESERVED	Reserved

1.3.1171 B[0..3]_P[0..7]_U[0..1]_CFG5

CFG5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG5: 0x10045
B0_P1_U0_CFG5: 0x10245
B0_P2_U0_CFG5: 0x10445
B0_P3_U0_CFG5: 0x10645
B0_P4_U0_CFG5: 0x10845
B0_P5_U0_CFG5: 0x10A45
B0_P6_U0_CFG5: 0x10C45
B0_P7_U0_CFG5: 0x10E45
B1_P2_U0_CFG5: 0x11445
B1_P3_U0_CFG5: 0x11645
B1_P4_U0_CFG5: 0x11845
B1_P5_U0_CFG5: 0x11A45

B0_P0_U1_CFG5: 0x100C5
B0_P1_U1_CFG5: 0x102C5
B0_P2_U1_CFG5: 0x104C5
B0_P3_U1_CFG5: 0x106C5
B0_P4_U1_CFG5: 0x108C5
B0_P5_U1_CFG5: 0x10AC5
B0_P6_U1_CFG5: 0x10CC5
B0_P7_U1_CFG5: 0x10EC5
B1_P2_U1_CFG5: 0x114C5
B1_P3_U1_CFG5: 0x116C5
B1_P4_U1_CFG5: 0x118C5
B1_P5_U1_CFG5: 0x11AC5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0000				R/W:0000			
HW Access	R				R			
Retention	RET				RET			
Name	OUT1				OUT0			

Datapath Output Selection for OUT1 OUT0, a 1 of 16 select

Bits	Name	Description
7:4	OUT1[3:0]	Datapath Permutable Ouput Mux See Table 1-735.
3:0	OUT0[3:0]	Datapath Permutable Ouput Mux See Table 1-735.

Table 1-735. Bit field encoding: DP_OUTPUT_MUX_ENUM

Value	Name	Description
4'b0000	CE0	Comparator 0 equal
4'b0001	CL0	Comparator 0 less than
4'b0010	Z0	Accumulator 0 zero detect
4'b0011	FF0	Accumulator 0 ones detect
4'b0100	CE1	Comparator 1 equal
4'b0101	CL1	Comparator 1 less than
4'b0110	Z1	Accumulator 1 zero detect
4'b0111	FF1	Accumulator 1 ones detect
4'b1000	OV_MSB	Overflow of MSB
4'b1001	CO_MSB	Carry out of MSB
4'b1010	CMSBO	CRC MSB

(continued)

Table 1-735. Bit field encoding: DP_OUTPUT_MUX_ENUM

4'b1011	SO	Shift out
4'b1100	F0_BLK_STAT	FIFO 0 block status defined by direction
4'b1101	F1_BLK_STAT	FIFO 1 block status defined by direction
4'b1110	F0_BUS_STAT	FIFO 0 bus status defined by direction and level
4'b1111	F1_BUS_STAT	FIFO 1 bus status defined by direction and level

1.3.1172 B[0..3]_P[0..7]_U[0..1]_CFG6

CFG6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG6: 0x10046
B0_P1_U0_CFG6: 0x10246
B0_P2_U0_CFG6: 0x10446
B0_P3_U0_CFG6: 0x10646
B0_P4_U0_CFG6: 0x10846
B0_P5_U0_CFG6: 0x10A46
B0_P6_U0_CFG6: 0x10C46
B0_P7_U0_CFG6: 0x10E46
B1_P2_U0_CFG6: 0x11446
B1_P3_U0_CFG6: 0x11646
B1_P4_U0_CFG6: 0x11846
B1_P5_U0_CFG6: 0x11A46

B0_P0_U1_CFG6: 0x100C6
B0_P1_U1_CFG6: 0x102C6
B0_P2_U1_CFG6: 0x104C6
B0_P3_U1_CFG6: 0x106C6
B0_P4_U1_CFG6: 0x108C6
B0_P5_U1_CFG6: 0x10AC6
B0_P6_U1_CFG6: 0x10CC6
B0_P7_U1_CFG6: 0x10EC6
B1_P2_U1_CFG6: 0x114C6
B1_P3_U1_CFG6: 0x116C6
B1_P4_U1_CFG6: 0x118C6
B1_P5_U1_CFG6: 0x11AC6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0000				R/W:0000			
HW Access	R				R			
Retention	RET				RET			
Name	OUT3				OUT2			

Datapath Output Selection for OUT3 OUT2, a 1 of 16 select

Bits	Name	Description
7:4	OUT3[3:0]	Datapath Permutable Ouput Mux See Table 1-736.
3:0	OUT2[3:0]	Datapath Permutable Ouput Mux See Table 1-736.

Table 1-736. Bit field encoding: DP_OUTPUT_MUX_ENUM

Value	Name	Description
4'b0000	CE0	Comparator 0 equal
4'b0001	CL0	Comparator 0 less than
4'b0010	Z0	Accumulator 0 zero detect
4'b0011	FF0	Accumulator 0 ones detect
4'b0100	CE1	Comparator 1 equal
4'b0101	CL1	Comparator 1 less than
4'b0110	Z1	Accumulator 1 zero detect
4'b0111	FF1	Accumulator 1 ones detect
4'b1000	OV_MSB	Overflow of MSB
4'b1001	CO_MSB	Carry out of MSB
4'b1010	CMSBO	CRC MSB

(continued)

Table 1-736. Bit field encoding: DP_OUTPUT_MUX_ENUM

4'b1011	SO	Shift out
4'b1100	F0_BLK_STAT	FIFO 0 block status defined by direction
4'b1101	F1_BLK_STAT	FIFO 1 block status defined by direction
4'b1110	F0_BUS_STAT	FIFO 0 bus status defined by direction and level
4'b1111	F1_BUS_STAT	FIFO 1 bus status defined by direction and level

1.3.1173 B[0..3]_P[0..7]_U[0..1]_CFG7

CFG7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG7: 0x10047
B0_P1_U0_CFG7: 0x10247
B0_P2_U0_CFG7: 0x10447
B0_P3_U0_CFG7: 0x10647
B0_P4_U0_CFG7: 0x10847
B0_P5_U0_CFG7: 0x10A47
B0_P6_U0_CFG7: 0x10C47
B0_P7_U0_CFG7: 0x10E47
B1_P2_U0_CFG7: 0x11447
B1_P3_U0_CFG7: 0x11647
B1_P4_U0_CFG7: 0x11847
B1_P5_U0_CFG7: 0x11A47

B0_P0_U1_CFG7: 0x100C7
B0_P1_U1_CFG7: 0x102C7
B0_P2_U1_CFG7: 0x104C7
B0_P3_U1_CFG7: 0x106C7
B0_P4_U1_CFG7: 0x108C7
B0_P5_U1_CFG7: 0x10AC7
B0_P6_U1_CFG7: 0x10CC7
B0_P7_U1_CFG7: 0x10EC7
B1_P2_U1_CFG7: 0x114C7
B1_P3_U1_CFG7: 0x116C7
B1_P4_U1_CFG7: 0x118C7
B1_P5_U1_CFG7: 0x11AC7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0000				R/W:0000			
HW Access	R				R			
Retention	RET				RET			
Name	OUT5				OUT4			

Datapath Output Selection for OUT5 OUT4, a 1 of 16 select

Bits	Name	Description
7:4	OUT5[3:0]	Datapath Permutable Ouput Mux See Table 1-737.
3:0	OUT4[3:0]	Datapath Permutable Ouput Mux See Table 1-737.

Table 1-737. Bit field encoding: DP_OUTPUT_MUX_ENUM

Value	Name	Description
4'b0000	CE0	Comparator 0 equal
4'b0001	CL0	Comparator 0 less than
4'b0010	Z0	Accumulator 0 zero detect
4'b0011	FF0	Accumulator 0 ones detect
4'b0100	CE1	Comparator 1 equal
4'b0101	CL1	Comparator 1 less than
4'b0110	Z1	Accumulator 1 zero detect
4'b0111	FF1	Accumulator 1 ones detect
4'b1000	OV_MSB	Overflow of MSB
4'b1001	CO_MSB	Carry out of MSB
4'b1010	CMSBO	CRC MSB

(continued)

Table 1-737. Bit field encoding: DP_OUTPUT_MUX_ENUM

4'b1011	SO	Shift out
4'b1100	F0_BLK_STAT	FIFO 0 block status defined by direction
4'b1101	F1_BLK_STAT	FIFO 1 block status defined by direction
4'b1110	F0_BUS_STAT	FIFO 0 bus status defined by direction and level
4'b1111	F1_BUS_STAT	FIFO 1 bus status defined by direction and level

1.3.1174 B[0..3]_P[0..7]_U[0..1]_CFG8

CFG8

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG8: 0x10048
B0_P1_U0_CFG8: 0x10248
B0_P2_U0_CFG8: 0x10448
B0_P3_U0_CFG8: 0x10648
B0_P4_U0_CFG8: 0x10848
B0_P5_U0_CFG8: 0x10A48
B0_P6_U0_CFG8: 0x10C48
B0_P7_U0_CFG8: 0x10E48
B1_P2_U0_CFG8: 0x11448
B1_P3_U0_CFG8: 0x11648
B1_P4_U0_CFG8: 0x11848
B1_P5_U0_CFG8: 0x11A48
B0_P0_U1_CFG8: 0x100C8
B0_P1_U1_CFG8: 0x102C8
B0_P2_U1_CFG8: 0x104C8
B0_P3_U1_CFG8: 0x106C8
B0_P4_U1_CFG8: 0x108C8
B0_P5_U1_CFG8: 0x10AC8
B0_P6_U1_CFG8: 0x10CC8
B0_P7_U1_CFG8: 0x10EC8
B1_P2_U1_CFG8: 0x114C8
B1_P3_U1_CFG8: 0x116C8
B1_P4_U1_CFG8: 0x118C8
B1_P5_U1_CFG8: 0x11AC8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:000000					
HW Access	NA		R					
Retention	NA		RET					
Name	RSVD		OUT_SYNC					

Datapath Output Synchronization Option

Bits	Name	Description
5:0	OUT_SYNC[5:0]	Datapath Output Synchronization. Each datapath output can be registered (default,0), or combinational (1)

1.3.1175 B[0..3]_P[0..7]_U[0..1]_CFG9

CFG9

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG9: 0x10049
B0_P0_U1_CFG9: 0x100C9
B0_P1_U0_CFG9: 0x10249
B0_P1_U1_CFG9: 0x102C9
B0_P2_U0_CFG9: 0x10449
B0_P2_U1_CFG9: 0x104C9
B0_P3_U0_CFG9: 0x10649
B0_P3_U1_CFG9: 0x106C9
B0_P4_U0_CFG9: 0x10849
B0_P4_U1_CFG9: 0x108C9
B0_P5_U0_CFG9: 0x10A49
B0_P5_U1_CFG9: 0x10AC9
B0_P6_U0_CFG9: 0x10C49
B0_P6_U1_CFG9: 0x10CC9
B0_P7_U0_CFG9: 0x10E49
B0_P7_U1_CFG9: 0x10EC9
B1_P2_U0_CFG9: 0x11449
B1_P2_U1_CFG9: 0x114C9
B1_P3_U0_CFG9: 0x11649
B1_P3_U1_CFG9: 0x116C9
B1_P4_U0_CFG9: 0x11849
B1_P4_U1_CFG9: 0x118C9
B1_P5_U0_CFG9: 0x11A49
B1_P5_U1_CFG9: 0x11AC9

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	AMASK							

Datapath ALU Mask

Bits	Name	Description
7:0	AMASK[7:0]	Datapath ALU Mask. The mask value in this register is applied to the output of the Datapath ALU result before the result is stored. The AMASK_EN bit (CFG12) must be set for the mask to be operational.

1.3.1176 B[0..3]_P[0..7]_U[0..1]_CFG10

CFG10

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG10: 0x1004A
B0_P0_U1_CFG10: 0x100CA
B0_P1_U0_CFG10: 0x1024A
B0_P1_U1_CFG10: 0x102CA
B0_P2_U0_CFG10: 0x1044A
B0_P2_U1_CFG10: 0x104CA
B0_P3_U0_CFG10: 0x1064A
B0_P3_U1_CFG10: 0x106CA
B0_P4_U0_CFG10: 0x1084A
B0_P4_U1_CFG10: 0x108CA
B0_P5_U0_CFG10: 0x10A4A
B0_P5_U1_CFG10: 0x10ACA
B0_P6_U0_CFG10: 0x10C4A
B0_P6_U1_CFG10: 0x10CCA
B0_P7_U0_CFG10: 0x10E4A
B0_P7_U1_CFG10: 0x10ECA
B1_P2_U0_CFG10: 0x1144A
B1_P2_U1_CFG10: 0x114CA
B1_P3_U0_CFG10: 0x1164A
B1_P3_U1_CFG10: 0x116CA
B1_P4_U0_CFG10: 0x1184A
B1_P4_U1_CFG10: 0x118CA
B1_P5_U0_CFG10: 0x11A4A
B1_P5_U1_CFG10: 0x11ACA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	CMASK0							

Datapath Compare 0 Mask

Bits	Name	Description
7:0	CMASK0[7:0]	Datapath Compare 0 Mask. The mask value in this register is applied to the output of the Accumulator 0 before it is used for comparison in Compare block 0. The CMASK0_EN bit (CFG12) must be set for the mask to be operational.

1.3.1177 B[0..3]_P[0..7]_U[0..1]_CFG11

CFG11

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG11: 0x1004B
B0_P0_U1_CFG11: 0x100CB
B0_P1_U0_CFG11: 0x1024B
B0_P1_U1_CFG11: 0x102CB
B0_P2_U0_CFG11: 0x1044B
B0_P2_U1_CFG11: 0x104CB
B0_P3_U0_CFG11: 0x1064B
B0_P3_U1_CFG11: 0x106CB
B0_P4_U0_CFG11: 0x1084B
B0_P4_U1_CFG11: 0x108CB
B0_P5_U0_CFG11: 0x10A4B
B0_P5_U1_CFG11: 0x10ACB
B0_P6_U0_CFG11: 0x10C4B
B0_P6_U1_CFG11: 0x10CCB
B0_P7_U0_CFG11: 0x10E4B
B0_P7_U1_CFG11: 0x10ECB
B1_P2_U0_CFG11: 0x1144B
B1_P2_U1_CFG11: 0x114CB
B1_P3_U0_CFG11: 0x1164B
B1_P3_U1_CFG11: 0x116CB
B1_P4_U0_CFG11: 0x1184B
B1_P4_U1_CFG11: 0x118CB
B1_P5_U0_CFG11: 0x11A4B
B1_P5_U1_CFG11: 0x11ACB

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	CMASK1							

Datapath Compare 1 Mask

Bits	Name	Description
7:0	CMASK1[7:0]	Datapath Compare 1 Mask. The mask value in this register is applied to the selected Compare 1 block input (Accumulator 0 or Accumulator 1) before it is used for comparison. The CMASK1_EN bit (CFG12) must be set for the mask to be operational.

1.3.1178 B[0..3]_P[0..7]_U[0..1]_CFG12

CFG12

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG12: 0x1004C
B0_P0_U1_CFG12: 0x100CC
B0_P1_U0_CFG12: 0x1024C
B0_P1_U1_CFG12: 0x102CC
B0_P2_U0_CFG12: 0x1044C
B0_P2_U1_CFG12: 0x104CC
B0_P3_U0_CFG12: 0x1064C
B0_P3_U1_CFG12: 0x106CC
B0_P4_U0_CFG12: 0x1084C
B0_P4_U1_CFG12: 0x108CC
B0_P5_U0_CFG12: 0x10A4C
B0_P5_U1_CFG12: 0x10ACC
B0_P6_U0_CFG12: 0x10C4C
B0_P6_U1_CFG12: 0x10CCC
B0_P7_U0_CFG12: 0x10E4C
B0_P7_U1_CFG12: 0x10ECC
B1_P2_U0_CFG12: 0x1144C
B1_P2_U1_CFG12: 0x114CC
B1_P3_U0_CFG12: 0x1164C
B1_P3_U1_CFG12: 0x116CC
B1_P4_U0_CFG12: 0x1184C
B1_P4_U1_CFG12: 0x118CC
B1_P5_U0_CFG12: 0x11A4C
B1_P5_U1_CFG12: 0x11ACC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:00		R/W:00	
HW Access	R	R	R	R	R		R	
Retention	RET	RET	RET	RET	RET		RET	
Name	CMASK1_EN	CMASK0_EN	AMASK_EN	DEF_SI	SI_SELB		SI_SELA	

Datapath mask enables and shift in configuration

Bits	Name	Description
7	CMASK1_EN	Datapath mask enable See Table 1-739.
6	CMASK0_EN	Datapath mask enable See Table 1-739.
5	AMASK_EN	Datapath mask enable See Table 1-739.
4	DEF_SI	Datapath default shift value See Table 1-738.
3:2	SI_SELB[1:0]	Datapath shift in source select See Table 1-740.

(continued)

1:0	SI_SELA[1:0]	Datapath shift in source select See Table 1-740.

Table 1-738. Bit field encoding: DEF_SHIFT_ENUM

Value	Name	Description
1'b0	DEFAULT_0	Default shift is 0
1'b1	DEFAULT_1	Default shift is 1

Table 1-739. Bit field encoding: MASK_ENABLE_ENUM

Value	Name	Description
1'b0	DISABLE	Masking disabled
1'b1	ENABLE	Masking enabled

Table 1-740. Bit field encoding: SI_SEL_ENUM

Value	Name	Description
2'b00	DEFAULT	Default value specified in default shift field
2'b01	REGISTERED	Shift in is the shift out registered from previous cycle
2'b10	ROUTE	Shift in is selected from datapath routing input
2'b11	CHAIN	Shift in is chained from the previous datapath

1.3.1179 B[0..3]_P[0..7]_U[0..1]_CFG13

CFG13

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG13: 0x1004D
B0_P0_U1_CFG13: 0x100CD
B0_P1_U0_CFG13: 0x1024D
B0_P1_U1_CFG13: 0x102CD
B0_P2_U0_CFG13: 0x1044D
B0_P2_U1_CFG13: 0x104CD
B0_P3_U0_CFG13: 0x1064D
B0_P3_U1_CFG13: 0x106CD
B0_P4_U0_CFG13: 0x1084D
B0_P4_U1_CFG13: 0x108CD
B0_P5_U0_CFG13: 0x10A4D
B0_P5_U1_CFG13: 0x10ACD
B0_P6_U0_CFG13: 0x10C4D
B0_P6_U1_CFG13: 0x10CCD
B0_P7_U0_CFG13: 0x10E4D
B0_P7_U1_CFG13: 0x10ECD
B1_P2_U0_CFG13: 0x1144D
B1_P2_U1_CFG13: 0x114CD
B1_P3_U0_CFG13: 0x1164D
B1_P3_U1_CFG13: 0x116CD
B1_P4_U0_CFG13: 0x1184D
B1_P4_U1_CFG13: 0x118CD
B1_P5_U0_CFG13: 0x11A4D
B1_P5_U1_CFG13: 0x11ACD

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00		R/W:00		R/W:00		R/W:00	
HW Access	R		R		R		R	
Retention	RET		RET		RET		RET	
Name	CMP_SELB		CMP_SELA		CI_SELB		CI_SELA	

Datapath carry in and compare configuration

Bits	Name	Description
7:6	CMP_SELB[1:0]	Datapath compare select See Table 1-742.
5:4	CMP_SELA[1:0]	Datapath compare select See Table 1-742.
3:2	CI_SELB[1:0]	Datapath carry in source select See Table 1-741.
1:0	CI_SELA[1:0]	Datapath carry in source select See Table 1-741.

Table 1-741. Bit field encoding: CI_SEL_ENUM

Value	Name	Description
2'b00	DEFAULT	Default arithmetic mode
2'b01	REGISTERED	Carry in is the carry out registered from previous cycle
2'b10	ROUTE	Carry in is selected from datapath routing input
2'b11	CHAIN	Carry in is chained from the previous datapath

(continued)

Table 1-742. Bit field encoding: CMP_SEL_ENUM

Value	Name	Description
2'b00	A1_D1	Compare A1 to D1
2'b01	A1_A0	Compare A1 to A0
2'b10	A0_D1	Compare A0 to D1
2'b11	A0_A0	Compare A0 to A0

1.3.1180 B[0..3]_P[0..7]_U[0..1]_CFG14

CFG14

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG14: 0x1004E
B0_P0_U1_CFG14: 0x100CE
B0_P1_U0_CFG14: 0x1024E
B0_P1_U1_CFG14: 0x102CE
B0_P2_U0_CFG14: 0x1044E
B0_P2_U1_CFG14: 0x104CE
B0_P3_U0_CFG14: 0x1064E
B0_P3_U1_CFG14: 0x106CE
B0_P4_U0_CFG14: 0x1084E
B0_P4_U1_CFG14: 0x108CE
B0_P5_U0_CFG14: 0x10A4E
B0_P5_U1_CFG14: 0x10ACE
B0_P6_U0_CFG14: 0x10C4E
B0_P6_U1_CFG14: 0x10CCE
B0_P7_U0_CFG14: 0x10E4E
B0_P7_U1_CFG14: 0x10ECE
B1_P2_U0_CFG14: 0x1144E
B1_P2_U1_CFG14: 0x114CE
B1_P3_U0_CFG14: 0x1164E
B1_P3_U1_CFG14: 0x116CE
B1_P4_U0_CFG14: 0x1184E
B1_P4_U1_CFG14: 0x118CE
B1_P5_U0_CFG14: 0x11A4E
B1_P5_U1_CFG14: 0x11ACE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:000			R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R			R	R	R	R
Retention	RET	RET			RET	RET	RET	RET
Name	MSB_EN	MSB_SEL			CHAIN_CMSB	CHAIN_FB	CHAIN1	CHAIN0

Datapath chaining and MSB configuration

Bits	Name	Description
7	MSB_EN	Datapath MSB selection enable See Table 1-746.
6:4	MSB_SEL[2:0]	Datapath MSB Selection See Table 1-747.
3	CHAIN_CMSB	Datapath CRC MSB chaining enable See Table 1-743.
2	CHAIN_FB	Datapath CRC feedback chaining enable See Table 1-745.
1	CHAIN1	Datapath condition chaining enable See Table 1-744.

(continued)

0	CHAIN0	Datapath condition chaining enable See Table 1-744.

Table 1-743. Bit field encoding: CHAIN_CMSB_ENUM

Value	Name	Description
1'b0	DISABLE	CRC MSB is not chained
1'b1	ENABLE	CRC MSB is chained from the next (MSB) datapath

Table 1-744. Bit field encoding: CHAIN_EN_ENUM

Value	Name	Description
1'b0	DISABLE	Conditions are not chained
1'b1	ENABLE	Conditions are chained from the previous (LSB) datapath

Table 1-745. Bit field encoding: CHAIN_FB_ENUM

Value	Name	Description
1'b0	DISABLE	CRC feedback is not chained
1'b1	ENABLE	CRC feedback is chained from the previous (LSB) datapath

Table 1-746. Bit field encoding: MSB_EN_ENUM

Value	Name	Description
1'b0	DISABLE	MSB selection is disabled, MSB is bit 7
1'b1	ENABLE	MSB selection is controlled by MSB_SEL

Table 1-747. Bit field encoding: MSB_SEL_ENUM

Value	Name	Description
3'b000	BIT0	MSB is bit 0
3'b001	BIT1	MSB is bit 1
3'b010	BIT2	MSB is bit 2
3'b011	BIT3	MSB is bit 3
3'b100	BIT4	MSB is bit 4
3'b101	BIT5	MSB is bit 5
3'b110	BIT6	MSB is bit 6
3'b111	BIT7	MSB is bit 7 - equivalent to MSB EN = 0

1.3.1181 B[0..3]_P[0..7]_U[0..1]_CFG15

CFG15

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG15: 0x1004F
B0_P0_U1_CFG15: 0x100CF
B0_P1_U0_CFG15: 0x1024F
B0_P1_U1_CFG15: 0x102CF
B0_P2_U0_CFG15: 0x1044F
B0_P2_U1_CFG15: 0x104CF
B0_P3_U0_CFG15: 0x1064F
B0_P3_U1_CFG15: 0x106CF
B0_P4_U0_CFG15: 0x1084F
B0_P4_U1_CFG15: 0x108CF
B0_P5_U0_CFG15: 0x10A4F
B0_P5_U1_CFG15: 0x10ACF
B0_P6_U0_CFG15: 0x10C4F
B0_P6_U1_CFG15: 0x10CCF
B0_P7_U0_CFG15: 0x10E4F
B0_P7_U1_CFG15: 0x10ECF
B1_P2_U0_CFG15: 0x1144F
B1_P2_U1_CFG15: 0x114CF
B1_P3_U0_CFG15: 0x1164F
B1_P3_U1_CFG15: 0x116CF
B1_P4_U0_CFG15: 0x1184F
B1_P4_U1_CFG15: 0x118CF
B1_P5_U0_CFG15: 0x11A4F
B1_P5_U1_CFG15: 0x11ACF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:00		R/W:00	
HW Access	R	R	R	R	R		R	
Retention	RET	RET	RET	RET	RET		RET	
Name	PI_SEL	SHIFT_SEL	PI_DYN	MSB_SI	F1_INSEL		F0_INSEL	

Datapath FIFO, shift and parallel input control

Bits	Name	Description
7	PI_SEL	Datapath parallel input selection See Table 1-751.
6	SHIFT_SEL	Datapath shift out selection See Table 1-752.
5	PI_DYN	Enable for dynamic control of parallel data input (PI) mux. See Table 1-750.
4	MSB_SI	Arithmetic shift right operation shift in selection See Table 1-749.
3:2	F1_INSEL[1:0]	Datapath FIFO Configuration See Table 1-748.
1:0	F0_INSEL[1:0]	Datapath FIFO Configuration See Table 1-748.

(continued)

Table 1-748. Bit field encoding: FIFO_CFG_ENUM

Value	Name	Description
2'b00	INPUT	Input Mode: Write source is the system bus; read destination is corresponding data register or accumulator
2'b01	OUTPUT_A0	Output Mode: Write source is A0, read destination is the system bus
2'b10	OUTPUT_A1	Output Mode: Write source is A1, read destination is the system bus
2'b11	OUTPUT_ALU	Output Mode: Write source is the ALU output, read destination is the system bus

Table 1-749. Bit field encoding: MSB_SI_ENUM

Value	Name	Description
1'b0	DEFAULT	Shift in default value (when SI_SELA and/or SI_SELB == 0)
1'b1	MSB	Override default and shift in MSB value

Table 1-750. Bit field encoding: PI_DYN_ENUM

Value	Name	Description
1'b0	DISABLED	Parallel input mux select is only controlled by static configuration (PI_SEL).
1'b1	ENABLED	Parallel input mux to the Datapath is controlled by CFB_EN field in Datapath Dynamic RAM. When this mode is enabled, the CFB_EN usage for CRC/PRS functionality is disabled.

Table 1-751. Bit field encoding: PI_SEL_ENUM

Value	Name	Description
1'b0	NORMAL	Normal operation, ALU source is from accumulator selection
1'b1	PARALLEL	ALU source A input is from the parallel data input

Table 1-752. Bit field encoding: SHIFT_SEL_ENUM

Value	Name	Description
1'b0	SOL_MSB	Routed shift out is shift out left (sol_msb)
1'b1	SOR	Routed shift out is shift out right (sor)

1.3.1182 B[0..3]_P[0..7]_U[0..1]_CFG16

CFG16

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG16: 0x10050
B0_P1_U0_CFG16: 0x10250
B0_P2_U0_CFG16: 0x10450
B0_P3_U0_CFG16: 0x10650
B0_P4_U0_CFG16: 0x10850
B0_P5_U0_CFG16: 0x10A50
B0_P6_U0_CFG16: 0x10C50
B0_P7_U0_CFG16: 0x10E50
B1_P2_U0_CFG16: 0x11450
B1_P3_U0_CFG16: 0x11650
B1_P4_U0_CFG16: 0x11850
B1_P5_U0_CFG16: 0x11A50
B0_P0_U1_CFG16: 0x100D0
B0_P1_U1_CFG16: 0x102D0
B0_P2_U1_CFG16: 0x104D0
B0_P3_U1_CFG16: 0x106D0
B0_P4_U1_CFG16: 0x108D0
B0_P5_U1_CFG16: 0x10AD0
B0_P6_U1_CFG16: 0x10CD0
B0_P7_U1_CFG16: 0x10ED0
B1_P2_U1_CFG16: 0x114D0
B1_P3_U1_CFG16: 0x116D0
B1_P4_U1_CFG16: 0x118D0
B1_P5_U1_CFG16: 0x11AD0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	F1_CK_INV	F0_CK_INV	FIFO_FAST	FIFO_CAP	FIFO_EDGE	FIFO_ASYNC	EXT_CRCPRS	WRK16_CONCAT

Datapath FIFO and register access configuration control

Bits	Name	Description
7	F1_CK_INV	FIFO Clock Invert. When this bit is set, the polarity of the clock for the given FIFO will be inverted, with respect to the polarity of the selected Datapath clock. See Table 1-756.
6	F0_CK_INV	FIFO Clock Invert. When this bit is set, the polarity of the clock for the given FIFO will be inverted, with respect to the polarity of the selected Datapath clock. See Table 1-756.
5	FIFO_FAST	FIFO Fast Mode. When this bit is set, the FIFO write logic is clocked by the application bus clock. Lowers the latency of capture timing, at the expense of additional power. See Table 1-758.
4	FIFO_CAP	FIFO Software Capture Mode. When this bit is set, a read of A0 or A1 triggers a capture into F0 or F1 respectively. This function follows the chaining configuration. All accumulators in the chain from a given block to the MS block in the chain are captured. Captured data may be read immediately from the FIFO. Only applies to FIFOs configured in output mode. See Table 1-755.

(continued)

3	FIFO_EDGE	Edge/level sensitive FIFO write control (Fx_LD). Only applies to FIFO configured in output mode See Table 1-757.
2	FIFO_ASYNC	Asynchronous FIFO clocking support See Table 1-754.
1	EXT_CRCPRS	External CRC/PRS mode See Table 1-753.
0	WRK16_CONCAT	Datapath register access mode See Table 1-759.

Table 1-753. Bit field encoding: EXT_CRCPRS_ENUM

Value	Name	Description
1'b0	INTERNAL	Internal CRC/PRS routing
1'b1	EXTERNAL	External CRC/PRS routing

Table 1-754. Bit field encoding: FIFO_ASYNC_ENUM

Value	Name	Description
1'b0	DISABLED	FIFO clocks are synchronous
1'b1	ENABLED	FIFO clocks are asynchronous

Table 1-755. Bit field encoding: FIFO_CAP_ENUM

Value	Name	Description
1'b0	DISABLED	FIFO capture is disabled.
1'b1	ENABLED	FIFO capture is enabled (FIFO must be in output mode). A read of A0 or A1 will write into F0 or F1.

Table 1-756. Bit field encoding: FIFO_CK_INV_ENUM

Value	Name	Description
1'b0	NORMAL	FIFO clock is the same polarity as the Datapath clock.
1'b1	INVERTED	FIFO clock is inverted with respect to the Datapath clock.

Table 1-757. Bit field encoding: FIFO_EDGE_ENUM

Value	Name	Description
1'b0	LEVEL	FIFO write from accumulators/ALU is level sensitive. FIFO write occurs on a clock edge whenever the write control is sampled high on that edge.
1'b1	EDGE	FIFO write from accumulators/ALU is edge sensitive. FIFO write occurs on a clock edge folloing a 0 to 1 transition on the write control. The write control must be negated for at least one full cycle of the FIFO clock for a subsequent transition to be detected.

Table 1-758. Bit field encoding: FIFO_FAST_ENUM

Value	Name	Description
1'b0	DISABLED	FIFO is clocked with selected Datapath clock.
1'b1	ENABLED	FIFO is clocked with application bus clock. Master and quadrant bus clock gating must be enabled.

Table 1-759. Bit field encoding: WRK16_SEL_ENUM

Value	Name	Description
1'b0	DEFAULT	16-bit default access mode: selects registers in two consecutive UDBs in chaining order
1'b1	CONCATENATE	16-bit concat access mode: selects concatenated registers in a single UDB

1.3.1183 B[0..3]_P[0..7]_U[0..1]_CFG17

CFG17

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG17: 0x10051
B0_P0_U1_CFG17: 0x100D1
B0_P1_U0_CFG17: 0x10251
B0_P1_U1_CFG17: 0x102D1
B0_P2_U0_CFG17: 0x10451
B0_P2_U1_CFG17: 0x104D1
B0_P3_U0_CFG17: 0x10651
B0_P3_U1_CFG17: 0x106D1
B0_P4_U0_CFG17: 0x10851
B0_P4_U1_CFG17: 0x108D1
B0_P5_U0_CFG17: 0x10A51
B0_P5_U1_CFG17: 0x10AD1
B0_P6_U0_CFG17: 0x10C51
B0_P6_U1_CFG17: 0x10CD1
B0_P7_U0_CFG17: 0x10E51
B0_P7_U1_CFG17: 0x10ED1
B1_P2_U0_CFG17: 0x11451
B1_P2_U1_CFG17: 0x114D1
B1_P3_U0_CFG17: 0x11651
B1_P3_U1_CFG17: 0x116D1
B1_P4_U0_CFG17: 0x11851
B1_P4_U1_CFG17: 0x118D1
B1_P5_U0_CFG17: 0x11A51
B1_P5_U1_CFG17: 0x11AD1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA			R	R	R	R	R
Retention	NA			RET	RET	RET	RET	RET
Name	RSVD			FIFO_ADD_SYNC	NC1	NC0	F1_DYN	F0_DYN

Datapath FIFO control

Bits	Name	Description
4	FIFO_ADD_SYNC	Adds an additional sync flip-flop to FIFO block status. See Table 1-760.
3	NC1	Spare register bit
2	NC0	Spare register bit
1	F1_DYN	When this bit is set, the associated FIFO configuration may be dynamically controlled. See Table 1-761.
0	F0_DYN	When this bit is set, the associated FIFO configuration may be dynamically controlled. See Table 1-761.

Table 1-760. Bit field encoding: FIFO_ADD_SYNC_ENUM

Value	Name	Description
1'b0	DISABLED	Compatible Mode: FIFO block status sync configuration is 'none' (FIFO_ASYNC = 0) and 1 sync flip-flop (FIFO_ASYNC = 1)

(continued)

Table 1-760. Bit field encoding: FIFO_ADD_SYNC_ENUM

1'b1	ENABLED	Add Sync Mode: FIFO block status sync configuration 1 sync flip-flop (FIFO_ASYNC = 0) and 2 sync flip-flops (FIFO_ASYNC = 1)

Table 1-761. Bit field encoding: FIFO_DYN_ENUM

Value	Name	Description
1'b0	STATIC	Default. FIFO direction is static and controlled by the associated Fx_INSEL bits (CFG15).
1'b1	DYNAMIC	The associated FIFO direction is dynamically controlled by the associated 'dx_load' Datapath input signal. When the 'dx_load' signal is '0', the access is internal, where the FIFO is both a source for the Datapath, and a destination for the Datapath (destination path from Fx_INSEL bits). When the 'dx_load' signal is '1', the access is external, where the CPU can both write and read the FIFO. When dynamic mode is activated, the dx_load signals are disabled for use as Data Register load signals.

1.3.1184 B[0..3]_P[0..7]_U[0..1]_CFG18

CFG18

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG18: 0x10052
B0_P1_U0_CFG18: 0x10252
B0_P2_U0_CFG18: 0x10452
B0_P3_U0_CFG18: 0x10652
B0_P4_U0_CFG18: 0x10852
B0_P5_U0_CFG18: 0x10A52
B0_P6_U0_CFG18: 0x10C52
B0_P7_U0_CFG18: 0x10E52
B1_P2_U0_CFG18: 0x11452
B1_P3_U0_CFG18: 0x11652
B1_P4_U0_CFG18: 0x11852
B1_P5_U0_CFG18: 0x11A52
B0_P0_U1_CFG18: 0x100D2
B0_P1_U1_CFG18: 0x102D2
B0_P2_U1_CFG18: 0x104D2
B0_P3_U1_CFG18: 0x106D2
B0_P4_U1_CFG18: 0x108D2
B0_P5_U1_CFG18: 0x10AD2
B0_P6_U1_CFG18: 0x10CD2
B0_P7_U1_CFG18: 0x10ED2
B1_P2_U1_CFG18: 0x114D2
B1_P3_U1_CFG18: 0x116D2
B1_P4_U1_CFG18: 0x118D2
B1_P5_U1_CFG18: 0x11AD2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	CTL_MD0							

Control Register Mode 0 (used in conjunction with Control Register Mode 1)

Bits	Name	Description
7:0	CTL_MD0[7:0]	CTL_MD1 and CTL_MD0 are concatenated to form an encoding for the mode of each control bit in the control register. Value '00' is Direct Mode, where the value written to that bit drives directly in the the routing. Value '01' is Sync Mode, where the control bit input is resampled by the selected SC clock before it is driven into the routing. Value '11' is Pulse Mode. Similar to Sync Mode, the control bit is resampled, then driven into the routing for a duration of 1 SC clock period. In addition, the control bit accessible by the CPU is reset at the end of the pulse period. The control bit can be polled for feedback with regard to this timing.

1.3.1185 B[0..3]_P[0..7]_U[0..1]_CFG19

CFG19

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG19: 0x10053
B0_P0_U1_CFG19: 0x100D3
B0_P1_U0_CFG19: 0x10253
B0_P1_U1_CFG19: 0x102D3
B0_P2_U0_CFG19: 0x10453
B0_P2_U1_CFG19: 0x104D3
B0_P3_U0_CFG19: 0x10653
B0_P3_U1_CFG19: 0x106D3
B0_P4_U0_CFG19: 0x10853
B0_P4_U1_CFG19: 0x108D3
B0_P5_U0_CFG19: 0x10A53
B0_P5_U1_CFG19: 0x10AD3
B0_P6_U0_CFG19: 0x10C53
B0_P6_U1_CFG19: 0x10CD3
B0_P7_U0_CFG19: 0x10E53
B0_P7_U1_CFG19: 0x10ED3
B1_P2_U0_CFG19: 0x11453
B1_P2_U1_CFG19: 0x114D3
B1_P3_U0_CFG19: 0x11653
B1_P3_U1_CFG19: 0x116D3
B1_P4_U0_CFG19: 0x11853
B1_P4_U1_CFG19: 0x118D3
B1_P5_U0_CFG19: 0x11A53
B1_P5_U1_CFG19: 0x11AD3

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	CTL_MD1							

Control Register Mode 1 (used in conjunction with Control Register Mode 0)

Bits	Name	Description
7:0	CTL_MD1[7:0]	CTL_MD1 and CTL_MD0 are concatenated to form an encoding for the mode of each control bit in the control register. Value '00' is Direct Mode, where the value written to that bit drives directly in the the routing. Value '01' is Sync Mode, where the control bit input is resampled by the selected SC clock before it is driven into the routing. Value '11' is Pulse Mode. Similar to Sync Mode, the control bit is resampled, then driven into the routing for a duration of 1 SC clock period. In addition, the control bit accessible by the CPU is reset at the end of the pulse period. The control bit can be polled for feedback with regard to this timing.

1.3.1186 B[0..3]_P[0..7]_U[0..1]_CFG20

CFG20

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG20: 0x10054
B0_P0_U1_CFG20: 0x100D4
B0_P1_U0_CFG20: 0x10254
B0_P1_U1_CFG20: 0x102D4
B0_P2_U0_CFG20: 0x10454
B0_P2_U1_CFG20: 0x104D4
B0_P3_U0_CFG20: 0x10654
B0_P3_U1_CFG20: 0x106D4
B0_P4_U0_CFG20: 0x10854
B0_P4_U1_CFG20: 0x108D4
B0_P5_U0_CFG20: 0x10A54
B0_P5_U1_CFG20: 0x10AD4
B0_P6_U0_CFG20: 0x10C54
B0_P6_U1_CFG20: 0x10CD4
B0_P7_U0_CFG20: 0x10E54
B0_P7_U1_CFG20: 0x10ED4
B1_P2_U0_CFG20: 0x11454
B1_P2_U1_CFG20: 0x114D4
B1_P3_U0_CFG20: 0x11654
B1_P3_U1_CFG20: 0x116D4
B1_P4_U0_CFG20: 0x11854
B1_P4_U1_CFG20: 0x118D4
B1_P5_U0_CFG20: 0x11A54
B1_P5_U1_CFG20: 0x11AD4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	STAT_MD							

Status Register input mode selection

Bits	Name	Description
7:0	STAT_MD[7:0]	Mode selection for each bit of the status register. A '0' is transparent mode, where internal routing is read directly by CPU firmware. A '1' is sticky-clear-on-read mode, where once the given bit is set, it will stay set until the CPU reads the bit.

1.3.1187 B[0..3]_P[0..7]_U[0..1]_CFG21

CFG21

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG21: 0x10055
B0_P1_U0_CFG21: 0x10255
B0_P2_U0_CFG21: 0x10455
B0_P3_U0_CFG21: 0x10655
B0_P4_U0_CFG21: 0x10855
B0_P5_U0_CFG21: 0x10A55
B0_P6_U0_CFG21: 0x10C55
B0_P7_U0_CFG21: 0x10E55
B1_P2_U0_CFG21: 0x11455
B1_P3_U0_CFG21: 0x11655
B1_P4_U0_CFG21: 0x11855
B1_P5_U0_CFG21: 0x11A55
B0_P0_U1_CFG21: 0x100D5
B0_P1_U1_CFG21: 0x102D5
B0_P2_U1_CFG21: 0x104D5
B0_P3_U1_CFG21: 0x106D5
B0_P4_U1_CFG21: 0x108D5
B0_P5_U1_CFG21: 0x10AD5
B0_P6_U1_CFG21: 0x10CD5
B0_P7_U1_CFG21: 0x10ED5
B1_P2_U1_CFG21: 0x114D5
B1_P3_U1_CFG21: 0x116D5
B1_P4_U1_CFG21: 0x118D5
B1_P5_U1_CFG21: 0x11AD5

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000000						R/W:0	R/W:0
HW Access	NA						R	R
Retention	NA						RET	RET
Name	RSVD						NC1	NC0

Spare register bits

Bits	Name	Description
1	NC1	Spare register bit
0	NC0	Spare register bit

1.3.1188 B[0..3]_P[0..7]_U[0..1]_CFG22

CFG22

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG22: 0x10056
B0_P1_U0_CFG22: 0x10256
B0_P2_U0_CFG22: 0x10456
B0_P3_U0_CFG22: 0x10656
B0_P4_U0_CFG22: 0x10856
B0_P5_U0_CFG22: 0x10A56
B0_P6_U0_CFG22: 0x10C56
B0_P7_U0_CFG22: 0x10E56
B1_P2_U0_CFG22: 0x11456
B1_P3_U0_CFG22: 0x11656
B1_P4_U0_CFG22: 0x11856
B1_P5_U0_CFG22: 0x11A56

B0_P0_U1_CFG22: 0x100D6
B0_P1_U1_CFG22: 0x102D6
B0_P2_U1_CFG22: 0x104D6
B0_P3_U1_CFG22: 0x106D6
B0_P4_U1_CFG22: 0x108D6
B0_P5_U1_CFG22: 0x10AD6
B0_P6_U1_CFG22: 0x10CD6
B0_P7_U1_CFG22: 0x10ED6
B1_P2_U1_CFG22: 0x114D6
B1_P3_U1_CFG22: 0x116D6
B1_P4_U1_CFG22: 0x118D6
B1_P5_U1_CFG22: 0x11AD6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:000			R/W:0	R/W:0	R/W:0	R/W:00	
HW Access	NA			R	R	R	R	
Retention	NA			RET	RET	RET	RET	
Name	RSVD			SC_EXT_RES	SC_SYNC_MD	SC_INT_MD	SC_OUT_CTL	

SC block configuration control

Bits	Name	Description
4	SC_EXT_RES	Control register external reset operation. This bit supports autonomous usage of the control register, where a routed reset should clear the writable input registers. By default this is off because the CPU writable register can be cleared in firmware. In other usage models, such as DMA data writing, an asynchronous routed reset may be needed. See Table 1-763.
3	SC_SYNC_MD	SC Sync Mode - controls when the status register operates as a 4-bit double synchronizer module See Table 1-765.
2	SC_INT_MD	SC Interrupt Mode - controls when the UDB driving an interrupt generated from the masked OR reduction of status bits 6 to 0 See Table 1-764.
1:0	SC_OUT_CTL[1:0]	Selects the output source for the Status and Control routing connections See Table 1-762.

(continued)

Table 1-762. Bit field encoding: OUT_CTL_ENUM

Value	Name	Description
2'b00	CONTROL	Control out, 8-bits of control are driven to the routing connections
2'b01	PARALLEL	Datapath parallel output, 8-bits of datapath parallel output data are driven to the routing connections
2'b10	COUNTER	Counter out, 7-bits of count and 1 bit (MSB) of terminal count are driven to the routing connections
2'b11	RESERVED	Reserved

Table 1-763. Bit field encoding: SC_EXT_RES_ENUM

Value	Name	Description
1'b0	DISABLED	When a routed reset is applied to the control register, only embedded state (sampling registers) are cleared
1'b1	ENABLED	When a routed reset is applied to the control register, all state is cleared, including the CPU writable control bits.

Table 1-764. Bit field encoding: SC_INT_MD_ENUM

Value	Name	Description
1'b0	NORMAL	Normal Mode - Routing connection sc_io[3] is a normal input to the status register
1'b1	INT_MODE	Interrupt Mode - Routing connection sc_io[3] operates as the UDB interrupt output

Table 1-765. Bit field encoding: SC_SYNC_MD_ENUM

Value	Name	Description
1'b0	NORMAL	Normal Mode - Status register operation
1'b1	SYNC_MODE	Sync Mode - Routing inputs sc_in[3:0] are the 4 sync inputs, and connections sc_io[3:0] operate as the sync outputs

1.3.1189 B[0..3]_P[0..7]_U[0..1]_CFG23

CFG23

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG23: 0x10057
B0_P1_U0_CFG23: 0x10257
B0_P2_U0_CFG23: 0x10457
B0_P3_U0_CFG23: 0x10657
B0_P4_U0_CFG23: 0x10857
B0_P5_U0_CFG23: 0x10A57
B0_P6_U0_CFG23: 0x10C57
B0_P7_U0_CFG23: 0x10E57
B1_P2_U0_CFG23: 0x11457
B1_P3_U0_CFG23: 0x11657
B1_P4_U0_CFG23: 0x11857
B1_P5_U0_CFG23: 0x11A57

B0_P0_U1_CFG23: 0x100D7
B0_P1_U1_CFG23: 0x102D7
B0_P2_U1_CFG23: 0x104D7
B0_P3_U1_CFG23: 0x106D7
B0_P4_U1_CFG23: 0x108D7
B0_P5_U1_CFG23: 0x10AD7
B0_P6_U1_CFG23: 0x10CD7
B0_P7_U1_CFG23: 0x10ED7
B1_P2_U1_CFG23: 0x114D7
B1_P3_U1_CFG23: 0x116D7
B1_P4_U1_CFG23: 0x118D7
B1_P5_U1_CFG23: 0x11AD7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:0	R/W:0	R/W:00		R/W:00	
HW Access	NA	R	R	R	R		R	
Retention	NA	RET	RET	RET	RET		RET	
Name	RSVD	ALT_CNT	ROUTE_EN	ROUTE_LD	CNT_EN_SEL		CNT_LD_SEL	

Counter Control

Bits	Name	Description
6	ALT_CNT	Configure the alternate operating mode of the counter See Table 1-766.
5	ROUTE_EN	Configure the counter enable signal for routing input See Table 1-769.
4	ROUTE_LD	Configure the counter load signal for routing input See Table 1-770.
3:2	CNT_EN_SEL[1:0]	Selects the routing inputs for the counter enable signal See Table 1-767.
1:0	CNT_LD_SEL[1:0]	Selects the routing inputs for the counter load signal See Table 1-768.

Table 1-766. Bit field encoding: SC_ALT_CNT_ENUM

Value	Name	Description
1'b0	DEFAULT_MODE	Default counter operating mode

(continued)

Table 1-766. Bit field encoding: SC_ALT_CNT_ENUM

1'b1	ALT_MODE	Alternate counter operating mode

Table 1-767. Bit field encoding: SC_CNT_EN_ENUM

Value	Name	Description
2'b00	SC_IN4	sc_in[4]
2'b01	SC_IN5	sc_in[5]
2'b10	SC_IN6	sc_in[6]
2'b11	SC_IO	sc_io, (SC_IO_CTL must be set to Input Mode)

Table 1-768. Bit field encoding: SC_CNT_LD_ENUM

Value	Name	Description
2'b00	SC_IN0	sc_in[0]
2'b01	SC_IN1	sc_in[1]
2'b10	SC_IN2	sc_in[2]
2'b11	SC_IN3	sc_in[3]

Table 1-769. Bit field encoding: SC_ROUTE_EN_ENUM

Value	Name	Description
1'b0	DISABLE	Routed EN signal is not used. EN signal is only controlled by firmware CNT START (ACTL register)
1'b1	ROUTED	Routed EN signal is used, CNT START must be set

Table 1-770. Bit field encoding: SC_ROUTE_LD_ENUM

Value	Name	Description
1'b0	DISABLE	Routed LD signal is not used
1'b1	ROUTED	Routed LD signal is used

1.3.1190 B[0..3]_P[0..7]_U[0..1]_CFG24

CFG24

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG24: 0x10058
B0_P1_U0_CFG24: 0x10258
B0_P2_U0_CFG24: 0x10458
B0_P3_U0_CFG24: 0x10658
B0_P4_U0_CFG24: 0x10858
B0_P5_U0_CFG24: 0x10A58
B0_P6_U0_CFG24: 0x10C58
B0_P7_U0_CFG24: 0x10E58
B1_P2_U0_CFG24: 0x11458
B1_P3_U0_CFG24: 0x11658
B1_P4_U0_CFG24: 0x11858
B1_P5_U0_CFG24: 0x11A58
B0_P0_U1_CFG24: 0x100D8
B0_P1_U1_CFG24: 0x102D8
B0_P2_U1_CFG24: 0x104D8
B0_P3_U1_CFG24: 0x106D8
B0_P4_U1_CFG24: 0x108D8
B0_P5_U1_CFG24: 0x10AD8
B0_P6_U1_CFG24: 0x10CD8
B0_P7_U1_CFG24: 0x10ED8
B1_P2_U1_CFG24: 0x114D8
B1_P3_U1_CFG24: 0x116D8
B1_P4_U1_CFG24: 0x118D8
B1_P5_U1_CFG24: 0x11AD8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:00		R/W:00	
HW Access	R	R	R	R	R		R	
Retention	RET	RET	RET	RET	RET		RET	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE		RC_EN_SEL	

PLD0 Clock and Reset control

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3]
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3]
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. See Table 1-774.

(continued)

4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. See Table 1-771.
3:2	RC_EN_MODE[1:0]	Selects the operating mode for the clock to the associated UDB component block. See Table 1-772.
1:0	RC_EN_SEL[1:0]	Selects channel route for enable control to the associated UDB component block See Table 1-773.

Table 1-771. Bit field encoding: RC_EN_INV_ENUM

Value	Name	Description
1'b0	TRUE	Non-inverted
1'b1	INVERTED	Inverted

Table 1-772. Bit field encoding: RC_EN_MODE_ENUM

Value	Name	Description
2'b00	OFF	Always off
2'b01	ON	Always on
2'b10	POSEDGE	Positive edge
2'b11	LEVEL	Level sensitive

Table 1-773. Bit field encoding: RC_EN_SEL_ENUM

Value	Name	Description
2'b00	RC_IN0	rc_in[0]
2'b01	RC_IN1	rc_in[1]
2'b10	RC_IN2	rc_in[2]
2'b11	RC_IN3	rc_in[3]

Table 1-774. Bit field encoding: RC_INV_ENUM

Value	Name	Description
1'b0	TRUE	Non-inverted
1'b1	INVERTED	Inverted

1.3.1191 B[0..3]_P[0..7]_U[0..1]_CFG25

CFG25

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG25: 0x10059
B0_P1_U0_CFG25: 0x10259
B0_P2_U0_CFG25: 0x10459
B0_P3_U0_CFG25: 0x10659
B0_P4_U0_CFG25: 0x10859
B0_P5_U0_CFG25: 0x10A59
B0_P6_U0_CFG25: 0x10C59
B0_P7_U0_CFG25: 0x10E59
B1_P2_U0_CFG25: 0x11459
B1_P3_U0_CFG25: 0x11659
B1_P4_U0_CFG25: 0x11859
B1_P5_U0_CFG25: 0x11A59

B0_P0_U1_CFG25: 0x100D9
B0_P1_U1_CFG25: 0x102D9
B0_P2_U1_CFG25: 0x104D9
B0_P3_U1_CFG25: 0x106D9
B0_P4_U1_CFG25: 0x108D9
B0_P5_U1_CFG25: 0x10AD9
B0_P6_U1_CFG25: 0x10CD9
B0_P7_U1_CFG25: 0x10ED9
B1_P2_U1_CFG25: 0x114D9
B1_P3_U1_CFG25: 0x116D9
B1_P4_U1_CFG25: 0x118D9
B1_P5_U1_CFG25: 0x11AD9

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:00		R/W:00	
HW Access	R	R	R	R	R		R	
Retention	RET	RET	RET	RET	RET		RET	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE		RC_EN_SEL	

PLD1 Clock and Reset control. Note: In alternate reset mode (ALT RES = 1), The PLD0 routed reset selection controls both PLD0 and PLD1, therefore the RC_SEL bits for PLD1 are not used.

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3]
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3]
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. See Table 1-778.

(continued)

4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. See Table 1-775.
3:2	RC_EN_MODE[1:0]	Selects the operating mode for the clock to the associated UDB component block. See Table 1-776.
1:0	RC_EN_SEL[1:0]	Selects channel route for enable control to the associated UDB component block See Table 1-777.

Table 1-775. Bit field encoding: RC_EN_INV_ENUM

Value	Name	Description
1'b0	TRUE	Non-inverted
1'b1	INVERTED	Inverted

Table 1-776. Bit field encoding: RC_EN_MODE_ENUM

Value	Name	Description
2'b00	OFF	Always off
2'b01	ON	Always on
2'b10	POSEDGE	Positive edge
2'b11	LEVEL	Level sensitive

Table 1-777. Bit field encoding: RC_EN_SEL_ENUM

Value	Name	Description
2'b00	RC_IN0	rc_in[0]
2'b01	RC_IN1	rc_in[1]
2'b10	RC_IN2	rc_in[2]
2'b11	RC_IN3	rc_in[3]

Table 1-778. Bit field encoding: RC_INV_ENUM

Value	Name	Description
1'b0	TRUE	Non-inverted
1'b1	INVERTED	Inverted

1.3.1192 B[0..3]_P[0..7]_U[0..1]_CFG26

CFG26

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG26: 0x1005A
B0_P0_U1_CFG26: 0x100DA
B0_P1_U0_CFG26: 0x1025A
B0_P1_U1_CFG26: 0x102DA
B0_P2_U0_CFG26: 0x1045A
B0_P2_U1_CFG26: 0x104DA
B0_P3_U0_CFG26: 0x1065A
B0_P3_U1_CFG26: 0x106DA
B0_P4_U0_CFG26: 0x1085A
B0_P4_U1_CFG26: 0x108DA
B0_P5_U0_CFG26: 0x10A5A
B0_P5_U1_CFG26: 0x10ADA
B0_P6_U0_CFG26: 0x10C5A
B0_P6_U1_CFG26: 0x10CDA
B0_P7_U0_CFG26: 0x10E5A
B0_P7_U1_CFG26: 0x10EDA
B1_P2_U0_CFG26: 0x1145A
B1_P2_U1_CFG26: 0x114DA
B1_P3_U0_CFG26: 0x1165A
B1_P3_U1_CFG26: 0x116DA
B1_P4_U0_CFG26: 0x1185A
B1_P4_U1_CFG26: 0x118DA
B1_P5_U0_CFG26: 0x11A5A
B1_P5_U1_CFG26: 0x11ADA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:00		R/W:00	
HW Access	R	R	R	R	R		R	
Retention	RET	RET	RET	RET	RET		RET	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE		RC_EN_SEL	

Datapath Clock and Reset control

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3]
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3]
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. See Table 1-782.

(continued)

4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. See Table 1-779.
3:2	RC_EN_MODE[1:0]	Selects the operating mode for the clock to the associated UDB component block. See Table 1-780.
1:0	RC_EN_SEL[1:0]	Selects channel route for enable control to the associated UDB component block See Table 1-781.

Table 1-779. Bit field encoding: RC_EN_INV_ENUM

Value	Name	Description
1'b0	TRUE	Non-inverted
1'b1	INVERTED	Inverted

Table 1-780. Bit field encoding: RC_EN_MODE_ENUM

Value	Name	Description
2'b00	OFF	Always off
2'b01	ON	Always on
2'b10	POSEDGE	Positive edge
2'b11	LEVEL	Level sensitive

Table 1-781. Bit field encoding: RC_EN_SEL_ENUM

Value	Name	Description
2'b00	RC_IN0	rc_in[0]
2'b01	RC_IN1	rc_in[1]
2'b10	RC_IN2	rc_in[2]
2'b11	RC_IN3	rc_in[3]

Table 1-782. Bit field encoding: RC_INV_ENUM

Value	Name	Description
1'b0	TRUE	Non-inverted
1'b1	INVERTED	Inverted

1.3.1193 B[0..3]_P[0..7]_U[0..1]_CFG27

CFG27

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG27: 0x1005B
B0_P0_U1_CFG27: 0x100DB
B0_P1_U0_CFG27: 0x1025B
B0_P1_U1_CFG27: 0x102DB
B0_P2_U0_CFG27: 0x1045B
B0_P2_U1_CFG27: 0x104DB
B0_P3_U0_CFG27: 0x1065B
B0_P3_U1_CFG27: 0x106DB
B0_P4_U0_CFG27: 0x1085B
B0_P4_U1_CFG27: 0x108DB
B0_P5_U0_CFG27: 0x10A5B
B0_P5_U1_CFG27: 0x10ADB
B0_P6_U0_CFG27: 0x10C5B
B0_P6_U1_CFG27: 0x10CDB
B0_P7_U0_CFG27: 0x10E5B
B0_P7_U1_CFG27: 0x10EDB
B1_P2_U0_CFG27: 0x1145B
B1_P2_U1_CFG27: 0x114DB
B1_P3_U0_CFG27: 0x1165B
B1_P3_U1_CFG27: 0x116DB
B1_P4_U0_CFG27: 0x1185B
B1_P4_U1_CFG27: 0x118DB
B1_P5_U0_CFG27: 0x11A5B
B1_P5_U1_CFG27: 0x11ADB

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:00		R/W:00	
HW Access	R	R	R	R	R		R	
Retention	RET	RET	RET	RET	RET		RET	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE		RC_EN_SEL	

Status/Control Clock and Reset control

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3]
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3]
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. See Table 1-786.

(continued)

4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. See Table 1-783.
3:2	RC_EN_MODE[1:0]	Selects the operating mode for the clock to the associated UDB component block. See Table 1-784.
1:0	RC_EN_SEL[1:0]	Selects channel route for enable control to the associated UDB component block See Table 1-785.

Table 1-783. Bit field encoding: RC_EN_INV_ENUM

Value	Name	Description
1'b0	TRUE	Non-inverted
1'b1	INVERTED	Inverted

Table 1-784. Bit field encoding: RC_EN_MODE_ENUM

Value	Name	Description
2'b00	OFF	Always off
2'b01	ON	Always on
2'b10	POSEDGE	Positive edge
2'b11	LEVEL	Level sensitive

Table 1-785. Bit field encoding: RC_EN_SEL_ENUM

Value	Name	Description
2'b00	RC_IN0	rc_in[0]
2'b01	RC_IN1	rc_in[1]
2'b10	RC_IN2	rc_in[2]
2'b11	RC_IN3	rc_in[3]

Table 1-786. Bit field encoding: RC_INV_ENUM

Value	Name	Description
1'b0	TRUE	Non-inverted
1'b1	INVERTED	Inverted

1.3.1194 B[0..3]_P[0..7]_U[0..1]_CFG28

CFG28

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG28: 0x1005C
B0_P0_U1_CFG28: 0x100DC
B0_P1_U0_CFG28: 0x1025C
B0_P1_U1_CFG28: 0x102DC
B0_P2_U0_CFG28: 0x1045C
B0_P2_U1_CFG28: 0x104DC
B0_P3_U0_CFG28: 0x1065C
B0_P3_U1_CFG28: 0x106DC
B0_P4_U0_CFG28: 0x1085C
B0_P4_U1_CFG28: 0x108DC
B0_P5_U0_CFG28: 0x10A5C
B0_P5_U1_CFG28: 0x10ADC
B0_P6_U0_CFG28: 0x10C5C
B0_P6_U1_CFG28: 0x10CDC
B0_P7_U0_CFG28: 0x10E5C
B0_P7_U1_CFG28: 0x10EDC
B1_P2_U0_CFG28: 0x1145C
B1_P2_U1_CFG28: 0x114DC
B1_P3_U0_CFG28: 0x1165C
B1_P3_U1_CFG28: 0x116DC
B1_P4_U0_CFG28: 0x1185C
B1_P4_U1_CFG28: 0x118DC
B1_P5_U0_CFG28: 0x11A5C
B1_P5_U1_CFG28: 0x11ADC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0000				R/W:0000			
HW Access	R				R			
Retention	RET				RET			
Name	PLD1_CK_SEL				PLD0_CK_SEL			

Clock Selection for PLD1 and PLD0

Bits	Name	Description
7:4	PLD1_CK_SEL[3:0]	Clock selection registers See Table 1-787.
3:0	PLD0_CK_SEL[3:0]	Clock selection registers See Table 1-787.

Table 1-787. Bit field encoding: RC_CK_SEL_ENUM

Value	Name	Description
4'b0000	GCLK0	gclk[0]
4'b0001	GCLK1	gclk[1]
4'b0010	GCLK2	gclk[2]
4'b0011	GCLK3	gclk[3]
4'b0100	GCLK4	gclk[4]
4'b0101	GCLK5	gclk[5]
4'b0110	GCLK6	gclk[6]
4'b0111	GCLK7	gclk[7]
4'b1000	EXT_CLK	ext_clk
4'b1001	SYSCLK	sysclk

1.3.1195 B[0..3]_P[0..7]_U[0..1]_CFG29

CFG29

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG29: 0x1005D
B0_P1_U0_CFG29: 0x1025D
B0_P2_U0_CFG29: 0x1045D
B0_P3_U0_CFG29: 0x1065D
B0_P4_U0_CFG29: 0x1085D
B0_P5_U0_CFG29: 0x10A5D
B0_P6_U0_CFG29: 0x10C5D
B0_P7_U0_CFG29: 0x10E5D
B1_P2_U0_CFG29: 0x1145D
B1_P3_U0_CFG29: 0x1165D
B1_P4_U0_CFG29: 0x1185D
B1_P5_U0_CFG29: 0x11A5D

B0_P0_U1_CFG29: 0x100DD
B0_P1_U1_CFG29: 0x102DD
B0_P2_U1_CFG29: 0x104DD
B0_P3_U1_CFG29: 0x106DD
B0_P4_U1_CFG29: 0x108DD
B0_P5_U1_CFG29: 0x10ADD
B0_P6_U1_CFG29: 0x10CDD
B0_P7_U1_CFG29: 0x10EDD
B1_P2_U1_CFG29: 0x114DD
B1_P3_U1_CFG29: 0x116DD
B1_P4_U1_CFG29: 0x118DD
B1_P5_U1_CFG29: 0x11ADD

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0000				R/W:0000			
HW Access	R				R			
Retention	RET				RET			
Name	SC_CK_SEL				DP_CK_SEL			

Clock Selection for Datapath, Status and Control

Bits	Name	Description
7:4	SC_CK_SEL[3:0]	Clock selection registers See Table 1-788.
3:0	DP_CK_SEL[3:0]	Clock selection registers See Table 1-788.

Table 1-788. Bit field encoding: RC_CK_SEL_ENUM

Value	Name	Description
4'b0000	GCLK0	gclk[0]
4'b0001	GCLK1	gclk[1]
4'b0010	GCLK2	gclk[2]
4'b0011	GCLK3	gclk[3]
4'b0100	GCLK4	gclk[4]
4'b0101	GCLK5	gclk[5]
4'b0110	GCLK6	gclk[6]
4'b0111	GCLK7	gclk[7]
4'b1000	EXT_CLK	ext_clk
4'b1001	SYSCLK	sysclk

1.3.1196 B[0..3]_P[0..7]_U[0..1]_CFG30

CFG30

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG30: 0x1005E
B0_P0_U1_CFG30: 0x100DE
B0_P1_U0_CFG30: 0x1025E
B0_P1_U1_CFG30: 0x102DE
B0_P2_U0_CFG30: 0x1045E
B0_P2_U1_CFG30: 0x104DE
B0_P3_U0_CFG30: 0x1065E
B0_P3_U1_CFG30: 0x106DE
B0_P4_U0_CFG30: 0x1085E
B0_P4_U1_CFG30: 0x108DE
B0_P5_U0_CFG30: 0x10A5E
B0_P5_U1_CFG30: 0x10ADE
B0_P6_U0_CFG30: 0x10C5E
B0_P6_U1_CFG30: 0x10CDE
B0_P7_U0_CFG30: 0x10E5E
B0_P7_U1_CFG30: 0x10EDE
B1_P2_U0_CFG30: 0x1145E
B1_P2_U1_CFG30: 0x114DE
B1_P3_U0_CFG30: 0x1165E
B1_P3_U1_CFG30: 0x116DE
B1_P4_U0_CFG30: 0x1185E
B1_P4_U1_CFG30: 0x118DE
B1_P5_U0_CFG30: 0x11A5E
B1_P5_U1_CFG30: 0x11ADE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	NA:0	R/W:0	R/W:0	R/W:0	R/W:00	
HW Access	R	R	NA	R	R	R	R	
Retention	RET	RET	NA	RET	RET	RET	RET	
Name	SC_RES_POL	DP_RES_POL	RSVD	GUDB_WR	EN_RES_CNTCTL	RES_POL	RES_SEL	

Reset control

Bits	Name	Description
7	SC_RES_POL	Only valid when ALT RES (CFG31) is '1'. This bit controls the polarity of the selected SC routed reset. See Table 1-794.
6	DP_RES_POL	Only valid when ALT RES (CFG31) is '1'. This bit controls the polarity of the selected Datapath routed reset. See Table 1-789.
4	GUDB_WR	Enable global write operation for the configuration and working registers in this UDB. When this bit is set, the UDB ID select decoding is bypassed. See Table 1-791.
3	EN_RES_CNTCTL	This bit gates the routed reset to the counter/control register. By default, the operation is compatible, i.e., it only applies to the counter. However, if the updated control regisiter modes are used (sync mode, pulse mode, or the ext res bit) then the routed reset applies to the control register also. See Table 1-790.

(continued)

2	RES_POL	The meaning of this bit depends on the value of the ALT RES bit in CFG31. When ALT RES is '0' (compatible mode), this bit sets the polarity of the routed reset. When ALT RES is '1', this bit is unused. See Table 1-792.
1:0	RES_SEL[1:0]	The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES is '0' (compatible mode), this 2 bit field selects the RC routing input for the compatible reset scheme. When the ALT RES bit is '1', these bits are not used. See Table 1-793.

Table 1-789. Bit field encoding: RC_DP_RES_POL_ENUM

Value	Name	Description
1'b0	TRUE	Routed reset to the Datapath block is true polarity.
1'b1	INVERTED	Routed reset to the Datapath block is inverted polarity.

Table 1-790. Bit field encoding: RC_EN_RES_CNTCTL_ENUM

Value	Name	Description
1'b0	DISABLE	Routed reset is not applied to counter/control register
1'b1	ENABLE	Routed reset is applied to the counter/control register

Table 1-791. Bit field encoding: RC_GUDB_WR_ENUM

Value	Name	Description
1'b0	DISABLE	Global UDB configuration/working register write is disabled
1'b1	ENABLE	Global UDB configuration/working register write is enabled

Table 1-792. Bit field encoding: RC_RES_POL_ENUM

Value	Name	Description
1'b0	NEGATED	Polarity of the routed reset is true.
1'b1	ASSERTED	Polarity of the routed reset is inverted.

Table 1-793. Bit field encoding: RC_RES_SEL_ENUM

Value	Name	Description
2'b00	RC_IN0	rc_in[0]
2'b01	RC_IN1	rc_in[1]
2'b10	RC_IN2	rc_in[2]
2'b11	RC_IN3	rc_in[3]

Table 1-794. Bit field encoding: RC_SC_RES_POL_ENUM

Value	Name	Description
1'b0	TRUE	Routed reset to the Status and Control block is true polarity.
1'b1	INVERTED	Routed reset to the Status and Control block is inverted polarity.

1.3.1197 B[0..3]_P[0..7]_U[0..1]_CFG31

CFG31

Reset: System reset for retention flops [reset_all_retention]

Register : Address

B0_P0_U0_CFG31: 0x1005F
B0_P0_U1_CFG31: 0x100DF
B0_P1_U0_CFG31: 0x1025F
B0_P1_U1_CFG31: 0x102DF
B0_P2_U0_CFG31: 0x1045F
B0_P2_U1_CFG31: 0x104DF
B0_P3_U0_CFG31: 0x1065F
B0_P3_U1_CFG31: 0x106DF
B0_P4_U0_CFG31: 0x1085F
B0_P4_U1_CFG31: 0x108DF
B0_P5_U0_CFG31: 0x10A5F
B0_P5_U1_CFG31: 0x10ADF
B0_P6_U0_CFG31: 0x10C5F
B0_P6_U1_CFG31: 0x10CDF
B0_P7_U0_CFG31: 0x10E5F
B0_P7_U1_CFG31: 0x10EDF
B1_P2_U0_CFG31: 0x1145F
B1_P2_U1_CFG31: 0x114DF
B1_P3_U0_CFG31: 0x1165F
B1_P3_U1_CFG31: 0x116DF
B1_P4_U0_CFG31: 0x1185F
B1_P4_U1_CFG31: 0x118DF
B1_P5_U0_CFG31: 0x11A5F
B1_P5_U1_CFG31: 0x11ADF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:00		R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R		R	R	R	R
Retention	RET	RET	RET		RET	RET	RET	RET
Name	PLD1_RES_POL	PLD0_RES_POL	EXT_CK_SEL		EN_RES_DP	EN_RES_STAT	EXT_SYNC	ALT_RES

Reset control

Bits	Name	Description
7	PLD1_RES_POL	Not connected. NOTE: There is only one routed reset available to both PLDs in the UDB. When ALT RES is '1', PLD0 RES SEL controls the polarity of the routed reset for both PLDs. See Table 1-801.
6	PLD0_RES_POL	The meaning of this bit depends on the value of ALT RES. When ALT RES (CFG31) is '1', this bit controls the polarity of the selected PLD0 routed reset. NOTE: There is only one routed reset available in the PLD block for both PLDs, therefore this bit controls the reset polarity to both PLD0 and PLD1. When ALT RES is '0' this bit is not used. See Table 1-800.
5:4	EXT_CK_SEL[1:0]	External clock selection See Table 1-798.
3	EN_RES_DP	Only valid when ALT RES (CFG31) is '1'. This bit gates the routed reset to the Datapath block. See Table 1-796.

(continued)

2	EN_RES_STAT	Only valid when ALT RES (CFG31) is '1'. This bit gates the routed reset to the status register. See Table 1-797.
1	EXT_SYNC	Enable synchronization of selected external clock See Table 1-799.
0	ALT_RES	This bit toggles between two reset configurations. When this bit is '0', one routed reset is shared by all components in this UDB (compatible mode). When this bit is a 1, each block can select a unique routed reset from the available RC inputs.; See Table 1-795.

Table 1-795. Bit field encoding: RC_ALT_RES_ENUM

Value	Name	Description
1'b0	COMPATIBLE	All UDB blocks share a common routed reset.
1'b1	ALTERNAT	Each UDB component block can select and control it's individual routed reset.

Table 1-796. Bit field encoding: RC_EN_RES_DP_ENUM

Value	Name	Description
1'b0	DISABLE	Routed reset to the Datapath block is gated off.
1'b1	ENABLE	Routed reset to the Datapath block is on. ALT RES must be '1' and routed reset must be selected in CFG26

Table 1-797. Bit field encoding: RC_EN_RES_STAT_ENUM

Value	Name	Description
1'b0	NEGATED	Status register routed reset is gated off
1'b1	ASSERTED	Status register routed reset is on

Table 1-798. Bit field encoding: RC_EXT_CK_SEL_ENUM

Value	Name	Description
2'b00	RC_IN0	rc_in[0]
2'b01	RC_IN1	rc_in[1]
2'b10	RC_IN2	rc_in[2]
2'b11	RC_IN3	rc_in[3]

Table 1-799. Bit field encoding: RC_EXT_SYNC_ENUM

Value	Name	Description
1'b0	DISABLE	Selected external clock input is not synchronized
1'b1	ENABLE	Selected external clock input is synchronized

Table 1-800. Bit field encoding: RC_PLD0_RES_POL_ENUM

Value	Name	Description
1'b0	TRUE	Routed reset to the PLD0/PLD1 block is true polarity.
1'b1	INVERTED	Routed reset to the PLD0/PLD1 block is inverted polarity.

Table 1-801. Bit field encoding: RC_PLD1_RES_POL_ENUM

Value	Name	Description
1'b0	TRUE	NU
1'b1	INVERTED	NU

1.3.1198 B[0..3]_P[0..7]_U[0..1]_DCFG[0..7]

DCFG

Reset: N/A

Register : Address

B0_P0_U0_DCFG0: 0x10060
B0_P0_U0_DCFG1: 0x10062
B0_P0_U0_DCFG2: 0x10064
B0_P0_U0_DCFG3: 0x10066
B0_P0_U0_DCFG4: 0x10068
B0_P0_U0_DCFG5: 0x1006A
B0_P0_U0_DCFG6: 0x1006C
B0_P0_U0_DCFG7: 0x1006E
B0_P0_U1_DCFG0: 0x100E0
B0_P0_U1_DCFG1: 0x100E2
B0_P0_U1_DCFG2: 0x100E4
B0_P0_U1_DCFG3: 0x100E6
B0_P0_U1_DCFG4: 0x100E8
B0_P0_U1_DCFG5: 0x100EA
B0_P0_U1_DCFG6: 0x100EC
B0_P0_U1_DCFG7: 0x100EE
B0_P1_U0_DCFG0: 0x10260
B0_P1_U0_DCFG1: 0x10262
B0_P1_U0_DCFG2: 0x10264
B0_P1_U0_DCFG3: 0x10266
B0_P1_U0_DCFG4: 0x10268
B0_P1_U0_DCFG5: 0x1026A
B0_P1_U0_DCFG6: 0x1026C
B0_P1_U0_DCFG7: 0x1026E
B0_P1_U1_DCFG0: 0x102E0
B0_P1_U1_DCFG1: 0x102E2
B0_P1_U1_DCFG2: 0x102E4
B0_P1_U1_DCFG3: 0x102E6
B0_P1_U1_DCFG4: 0x102E8
B0_P1_U1_DCFG5: 0x102EA
B0_P1_U1_DCFG6: 0x102EC
B0_P1_U1_DCFG7: 0x102EE
B0_P2_U0_DCFG0: 0x10460
B0_P2_U0_DCFG1: 0x10462
B0_P2_U0_DCFG2: 0x10464
B0_P2_U0_DCFG3: 0x10466
B0_P2_U0_DCFG4: 0x10468
B0_P2_U0_DCFG5: 0x1046A
B0_P2_U0_DCFG6: 0x1046C
B0_P2_U0_DCFG7: 0x1046E
B0_P2_U1_DCFG0: 0x104E0
B0_P2_U1_DCFG1: 0x104E2
B0_P2_U1_DCFG2: 0x104E4
B0_P2_U1_DCFG3: 0x104E6
B0_P2_U1_DCFG4: 0x104E8
B0_P2_U1_DCFG5: 0x104EA
B0_P2_U1_DCFG6: 0x104EC
B0_P2_U1_DCFG7: 0x104EE
B0_P3_U0_DCFG0: 0x10660
B0_P3_U0_DCFG1: 0x10662
B0_P3_U0_DCFG2: 0x10664
B0_P3_U0_DCFG3: 0x10666
B0_P3_U0_DCFG4: 0x10668
B0_P3_U0_DCFG5: 0x1066A
B0_P3_U0_DCFG6: 0x1066C
B0_P3_U0_DCFG7: 0x1066E
B0_P3_U1_DCFG0: 0x106E0
B0_P3_U1_DCFG1: 0x106E2
B0_P3_U1_DCFG2: 0x106E4
B0_P3_U1_DCFG3: 0x106E6
B0_P3_U1_DCFG4: 0x106E8
B0_P3_U1_DCFG5: 0x106EA
B0_P3_U1_DCFG6: 0x106EC
B0_P3_U1_DCFG7: 0x106EE
B0_P4_U0_DCFG0: 0x10860
B0_P4_U0_DCFG1: 0x10862

(continued)

Register : Address	
B0_P4_U0_DCFG2: 0x10864	B0_P4_U0_DCFG3: 0x10866
B0_P4_U0_DCFG4: 0x10868	B0_P4_U0_DCFG5: 0x1086A
B0_P4_U0_DCFG6: 0x1086C	B0_P4_U0_DCFG7: 0x1086E
B0_P4_U1_DCFG0: 0x108E0	B0_P4_U1_DCFG1: 0x108E2
B0_P4_U1_DCFG2: 0x108E4	B0_P4_U1_DCFG3: 0x108E6
B0_P4_U1_DCFG4: 0x108E8	B0_P4_U1_DCFG5: 0x108EA
B0_P4_U1_DCFG6: 0x108EC	B0_P4_U1_DCFG7: 0x108EE
B0_P5_U0_DCFG0: 0x10A60	B0_P5_U0_DCFG1: 0x10A62
B0_P5_U0_DCFG2: 0x10A64	B0_P5_U0_DCFG3: 0x10A66
B0_P5_U0_DCFG4: 0x10A68	B0_P5_U0_DCFG5: 0x10A6A
B0_P5_U0_DCFG6: 0x10A6C	B0_P5_U0_DCFG7: 0x10A6E
B0_P5_U1_DCFG0: 0x10AE0	B0_P5_U1_DCFG1: 0x10AE2
B0_P5_U1_DCFG2: 0x10AE4	B0_P5_U1_DCFG3: 0x10AE6
B0_P5_U1_DCFG4: 0x10AE8	B0_P5_U1_DCFG5: 0x10AEA
B0_P5_U1_DCFG6: 0x10AEC	B0_P5_U1_DCFG7: 0x10AEE
B0_P6_U0_DCFG0: 0x10C60	B0_P6_U0_DCFG1: 0x10C62
B0_P6_U0_DCFG2: 0x10C64	B0_P6_U0_DCFG3: 0x10C66
B0_P6_U0_DCFG4: 0x10C68	B0_P6_U0_DCFG5: 0x10C6A
B0_P6_U0_DCFG6: 0x10C6C	B0_P6_U0_DCFG7: 0x10C6E
B0_P6_U1_DCFG0: 0x10CE0	B0_P6_U1_DCFG1: 0x10CE2
B0_P6_U1_DCFG2: 0x10CE4	B0_P6_U1_DCFG3: 0x10CE6
B0_P6_U1_DCFG4: 0x10CE8	B0_P6_U1_DCFG5: 0x10CEA
B0_P6_U1_DCFG6: 0x10CEC	B0_P6_U1_DCFG7: 0x10CEE
B0_P7_U0_DCFG0: 0x10E60	B0_P7_U0_DCFG1: 0x10E62
B0_P7_U0_DCFG2: 0x10E64	B0_P7_U0_DCFG3: 0x10E66
B0_P7_U0_DCFG4: 0x10E68	B0_P7_U0_DCFG5: 0x10E6A
B0_P7_U0_DCFG6: 0x10E6C	B0_P7_U0_DCFG7: 0x10E6E
B0_P7_U1_DCFG0: 0x10EE0	B0_P7_U1_DCFG1: 0x10EE2
B0_P7_U1_DCFG2: 0x10EE4	B0_P7_U1_DCFG3: 0x10EE6
B0_P7_U1_DCFG4: 0x10EE8	B0_P7_U1_DCFG5: 0x10EEA
B0_P7_U1_DCFG6: 0x10EEC	B0_P7_U1_DCFG7: 0x10EEE
B1_P2_U0_DCFG0: 0x11460	B1_P2_U0_DCFG1: 0x11462
B1_P2_U0_DCFG2: 0x11464	B1_P2_U0_DCFG3: 0x11466
B1_P2_U0_DCFG4: 0x11468	B1_P2_U0_DCFG5: 0x1146A
B1_P2_U0_DCFG6: 0x1146C	B1_P2_U0_DCFG7: 0x1146E
B1_P2_U1_DCFG0: 0x114E0	B1_P2_U1_DCFG1: 0x114E2

(continued)

Register : Address

B1_P2_U1_DCFG2: 0x114E4
B1_P2_U1_DCFG3: 0x114E6
B1_P2_U1_DCFG4: 0x114E8
B1_P2_U1_DCFG5: 0x114EA
B1_P2_U1_DCFG6: 0x114EC
B1_P2_U1_DCFG7: 0x114EE
B1_P3_U0_DCFG0: 0x11660
B1_P3_U0_DCFG1: 0x11662
B1_P3_U0_DCFG2: 0x11664
B1_P3_U0_DCFG3: 0x11666
B1_P3_U0_DCFG4: 0x11668
B1_P3_U0_DCFG5: 0x1166A
B1_P3_U0_DCFG6: 0x1166C
B1_P3_U0_DCFG7: 0x1166E
B1_P3_U1_DCFG0: 0x116E0
B1_P3_U1_DCFG1: 0x116E2
B1_P3_U1_DCFG2: 0x116E4
B1_P3_U1_DCFG3: 0x116E6
B1_P3_U1_DCFG4: 0x116E8
B1_P3_U1_DCFG5: 0x116EA
B1_P3_U1_DCFG6: 0x116EC
B1_P3_U1_DCFG7: 0x116EE
B1_P4_U0_DCFG0: 0x11860
B1_P4_U0_DCFG1: 0x11862
B1_P4_U0_DCFG2: 0x11864
B1_P4_U0_DCFG3: 0x11866
B1_P4_U0_DCFG4: 0x11868
B1_P4_U0_DCFG5: 0x1186A
B1_P4_U0_DCFG6: 0x1186C
B1_P4_U0_DCFG7: 0x1186E
B1_P4_U1_DCFG0: 0x118E0
B1_P4_U1_DCFG1: 0x118E2
B1_P4_U1_DCFG2: 0x118E4
B1_P4_U1_DCFG3: 0x118E6
B1_P4_U1_DCFG4: 0x118E8
B1_P4_U1_DCFG5: 0x118EA
B1_P4_U1_DCFG6: 0x118EC
B1_P4_U1_DCFG7: 0x118EE
B1_P5_U0_DCFG0: 0x11A60
B1_P5_U0_DCFG1: 0x11A62
B1_P5_U0_DCFG2: 0x11A64
B1_P5_U0_DCFG3: 0x11A66
B1_P5_U0_DCFG4: 0x11A68
B1_P5_U0_DCFG5: 0x11A6A
B1_P5_U0_DCFG6: 0x11A6C
B1_P5_U0_DCFG7: 0x11A6E
B1_P5_U1_DCFG0: 0x11AE0
B1_P5_U1_DCFG1: 0x11AE2
B1_P5_U1_DCFG2: 0x11AE4
B1_P5_U1_DCFG3: 0x11AE6
B1_P5_U1_DCFG4: 0x11AE8
B1_P5_U1_DCFG5: 0x11AEA
B1_P5_U1_DCFG6: 0x11AEC
B1_P5_U1_DCFG7: 0x11AEE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UU		R/W:UU		R/W:U	R/W:U	R/W:U	R/W:U
HW Access	R		R		R	R	R	R
Retention	RET		RET		RET	RET	RET	RET
Name	A0_WR_SRC		A1_WR_SRC		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:UUU			R/W:U	R/W:UU		R/W:UU	
HW Access	R			R	R		R	

(continued)

Retention	RET	RET	RET	RET
Name	FUNC	SRC_A	SRC_B	SHIFT

Dynamic Configuration RAM

Bits	Name	Description
15:13	FUNC[2:0]	Dynamic ALU function selection See Table 1-807.
12	SRC_A	Dynamic ALU source A selection See Table 1-810.
11:10	SRC_B[1:0]	Dynamic ALU source B selection See Table 1-811.
9:8	SHIFT[1:0]	Dynamic shift selection See Table 1-808.
7:6	A0_WR_SRC[1:0]	Dynamic A0 write source selection See Table 1-802.
5:4	A1_WR_SRC[1:0]	Dynamic A1 write source selection See Table 1-803.
3	CFB_EN	Dynamic CRC feedback selection See Table 1-804.
2	CI_SEL	Dynamic carry in selection See Table 1-805.
1	SI_SEL	Dynamic shift in selection See Table 1-809.
0	CMP_SEL	Dynamic compare selection See Table 1-806.

Table 1-802. Bit field encoding: A0_WR_SRC_ENUM

Value	Name	Description
2'b00	NOWRITE	no value written to A0
2'b01	ALU	ALU output written to A0
2'b10	D0	D0 value written to A0
2'b11	F0	F0 value written to A0

Table 1-803. Bit field encoding: A1_WR_SRC_ENUM

Value	Name	Description
2'b00	NOWRITE	no value written to A1
2'b01	ALU	ALU output written to A1
2'b10	D1	D1 value written to A1
2'b11	F1	F1 value written to A1

Table 1-804. Bit field encoding: CFB_EN_ENUM

Value	Name	Description
1'b0	DISABLE	CRC feedback disabled

(continued)

Table 1-804. Bit field encoding: CFB_EN_ENUM

1'b1	ENABLE	CRC feedback enabled

Table 1-805. Bit field encoding: CI_SEL_ENUM

Value	Name	Description
1'b0	CFG_A	Configuration A
1'b1	CFG_B	Configuration B

Table 1-806. Bit field encoding: CMP_SEL_ENUM

Value	Name	Description
1'b0	CFG_A	Configuration A
1'b1	CFG_B	Configuration B

Table 1-807. Bit field encoding: FUNC_ENUM

Value	Name	Description
3'b000	PASS	Pass
3'b001	INC_A	Increment source A
3'b010	DEC_A	Decrement source A
3'b011	ADD	Add
3'b100	SUB	Subtract
3'b101	XOR	Bitwise XOR
3'b110	AND	Bitwise AND
3'b111	OR	Bitwise OR

Table 1-808. Bit field encoding: SHIFT_ENUM

Value	Name	Description
2'b00	NOSHIFT	No shift
2'b01	LEFT	Left shift
2'b10	RIGHT	Right shift
2'b11	SWAP	Nibble swap

Table 1-809. Bit field encoding: SI_SEL_ENUM

Value	Name	Description
1'b0	CFG_A	Configuration A
1'b1	CFG_B	Configuration B

Table 1-810. Bit field encoding: SRC_A_ENUM

Value	Name	Description
1'b0	A0	ALU source A is A0
1'b1	A1	ALU source A is A1

Table 1-811. Bit field encoding: SRC_B_ENUM

Value	Name	Description
2'b00	D0	ALU source B is D0
2'b01	D1	ALU source B is D1
2'b10	A0	ALU source B is A0
2'b11	A1	ALU source B is A1

1.3.1199 B[0..3]_P[0..7]_ROUTE_HC[0..127]

HC

Reset: N/A

Register : Address

B0_P0_ROUTE_HC0: 0x10100
B0_P0_ROUTE_HC1: 0x10101
B0_P0_ROUTE_HC2: 0x10102
B0_P0_ROUTE_HC3: 0x10103
B0_P0_ROUTE_HC4: 0x10104
B0_P0_ROUTE_HC5: 0x10105
B0_P0_ROUTE_HC6: 0x10106
B0_P0_ROUTE_HC7: 0x10107
B0_P0_ROUTE_HC8: 0x10108
B0_P0_ROUTE_HC9: 0x10109
B0_P0_ROUTE_HC10: 0x1010A
B0_P0_ROUTE_HC11: 0x1010B
B0_P0_ROUTE_HC12: 0x1010C
B0_P0_ROUTE_HC13: 0x1010D
B0_P0_ROUTE_HC14: 0x1010E
B0_P0_ROUTE_HC15: 0x1010F
B0_P0_ROUTE_HC16: 0x10110
B0_P0_ROUTE_HC17: 0x10111
B0_P0_ROUTE_HC18: 0x10112
B0_P0_ROUTE_HC19: 0x10113
B0_P0_ROUTE_HC20: 0x10114
B0_P0_ROUTE_HC21: 0x10115
B0_P0_ROUTE_HC22: 0x10116
B0_P0_ROUTE_HC23: 0x10117
B0_P0_ROUTE_HC24: 0x10118
B0_P0_ROUTE_HC25: 0x10119
B0_P0_ROUTE_HC26: 0x1011A
B0_P0_ROUTE_HC27: 0x1011B
B0_P0_ROUTE_HC28: 0x1011C
B0_P0_ROUTE_HC29: 0x1011D
B0_P0_ROUTE_HC30: 0x1011E
B0_P0_ROUTE_HC31: 0x1011F
B0_P0_ROUTE_HC32: 0x10120
B0_P0_ROUTE_HC33: 0x10121
B0_P0_ROUTE_HC34: 0x10122
B0_P0_ROUTE_HC35: 0x10123
B0_P0_ROUTE_HC36: 0x10124
B0_P0_ROUTE_HC37: 0x10125
B0_P0_ROUTE_HC38: 0x10126
B0_P0_ROUTE_HC39: 0x10127
B0_P0_ROUTE_HC40: 0x10128
B0_P0_ROUTE_HC41: 0x10129
B0_P0_ROUTE_HC42: 0x1012A
B0_P0_ROUTE_HC43: 0x1012B
B0_P0_ROUTE_HC44: 0x1012C
B0_P0_ROUTE_HC45: 0x1012D
B0_P0_ROUTE_HC46: 0x1012E
B0_P0_ROUTE_HC47: 0x1012F
B0_P0_ROUTE_HC48: 0x10130
B0_P0_ROUTE_HC49: 0x10131
B0_P0_ROUTE_HC50: 0x10132
B0_P0_ROUTE_HC51: 0x10133
B0_P0_ROUTE_HC52: 0x10134
B0_P0_ROUTE_HC53: 0x10135
B0_P0_ROUTE_HC54: 0x10136
B0_P0_ROUTE_HC55: 0x10137
B0_P0_ROUTE_HC56: 0x10138
B0_P0_ROUTE_HC57: 0x10139
B0_P0_ROUTE_HC58: 0x1013A
B0_P0_ROUTE_HC59: 0x1013B
B0_P0_ROUTE_HC60: 0x1013C
B0_P0_ROUTE_HC61: 0x1013D
B0_P0_ROUTE_HC62: 0x1013E
B0_P0_ROUTE_HC63: 0x1013F
B0_P0_ROUTE_HC64: 0x10140
B0_P0_ROUTE_HC65: 0x10141

(continued)

Register : Address	
B0_P0_ROUTE_HC66: 0x10142	B0_P0_ROUTE_HC67: 0x10143
B0_P0_ROUTE_HC68: 0x10144	B0_P0_ROUTE_HC69: 0x10145
B0_P0_ROUTE_HC70: 0x10146	B0_P0_ROUTE_HC71: 0x10147
B0_P0_ROUTE_HC72: 0x10148	B0_P0_ROUTE_HC73: 0x10149
B0_P0_ROUTE_HC74: 0x1014A	B0_P0_ROUTE_HC75: 0x1014B
B0_P0_ROUTE_HC76: 0x1014C	B0_P0_ROUTE_HC77: 0x1014D
B0_P0_ROUTE_HC78: 0x1014E	B0_P0_ROUTE_HC79: 0x1014F
B0_P0_ROUTE_HC80: 0x10150	B0_P0_ROUTE_HC81: 0x10151
B0_P0_ROUTE_HC82: 0x10152	B0_P0_ROUTE_HC83: 0x10153
B0_P0_ROUTE_HC84: 0x10154	B0_P0_ROUTE_HC85: 0x10155
B0_P0_ROUTE_HC86: 0x10156	B0_P0_ROUTE_HC87: 0x10157
B0_P0_ROUTE_HC88: 0x10158	B0_P0_ROUTE_HC89: 0x10159
B0_P0_ROUTE_HC90: 0x1015A	B0_P0_ROUTE_HC91: 0x1015B
B0_P0_ROUTE_HC92: 0x1015C	B0_P0_ROUTE_HC93: 0x1015D
B0_P0_ROUTE_HC94: 0x1015E	B0_P0_ROUTE_HC95: 0x1015F
B0_P0_ROUTE_HC96: 0x10160	B0_P0_ROUTE_HC97: 0x10161
B0_P0_ROUTE_HC98: 0x10162	B0_P0_ROUTE_HC99: 0x10163
B0_P0_ROUTE_HC100: 0x10164	B0_P0_ROUTE_HC101: 0x10165
B0_P0_ROUTE_HC102: 0x10166	B0_P0_ROUTE_HC103: 0x10167
B0_P0_ROUTE_HC104: 0x10168	B0_P0_ROUTE_HC105: 0x10169
B0_P0_ROUTE_HC106: 0x1016A	B0_P0_ROUTE_HC107: 0x1016B
B0_P0_ROUTE_HC108: 0x1016C	B0_P0_ROUTE_HC109: 0x1016D
B0_P0_ROUTE_HC110: 0x1016E	B0_P0_ROUTE_HC111: 0x1016F
B0_P0_ROUTE_HC112: 0x10170	B0_P0_ROUTE_HC113: 0x10171
B0_P0_ROUTE_HC114: 0x10172	B0_P0_ROUTE_HC115: 0x10173
B0_P0_ROUTE_HC116: 0x10174	B0_P0_ROUTE_HC117: 0x10175
B0_P0_ROUTE_HC118: 0x10176	B0_P0_ROUTE_HC119: 0x10177
B0_P0_ROUTE_HC120: 0x10178	B0_P0_ROUTE_HC121: 0x10179
B0_P0_ROUTE_HC122: 0x1017A	B0_P0_ROUTE_HC123: 0x1017B
B0_P0_ROUTE_HC124: 0x1017C	B0_P0_ROUTE_HC125: 0x1017D
B0_P0_ROUTE_HC126: 0x1017E	B0_P0_ROUTE_HC127: 0x1017F
B0_P1_ROUTE_HC0: 0x10300	B0_P1_ROUTE_HC1: 0x10301
B0_P1_ROUTE_HC2: 0x10302	B0_P1_ROUTE_HC3: 0x10303
B0_P1_ROUTE_HC4: 0x10304	B0_P1_ROUTE_HC5: 0x10305
B0_P1_ROUTE_HC6: 0x10306	B0_P1_ROUTE_HC7: 0x10307
B0_P1_ROUTE_HC8: 0x10308	B0_P1_ROUTE_HC9: 0x10309

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Register : Address	
B0_P1_ROUTE_HC10: 0x1030A	B0_P1_ROUTE_HC11: 0x1030B
B0_P1_ROUTE_HC12: 0x1030C	B0_P1_ROUTE_HC13: 0x1030D
B0_P1_ROUTE_HC14: 0x1030E	B0_P1_ROUTE_HC15: 0x1030F
B0_P1_ROUTE_HC16: 0x10310	B0_P1_ROUTE_HC17: 0x10311
B0_P1_ROUTE_HC18: 0x10312	B0_P1_ROUTE_HC19: 0x10313
B0_P1_ROUTE_HC20: 0x10314	B0_P1_ROUTE_HC21: 0x10315
B0_P1_ROUTE_HC22: 0x10316	B0_P1_ROUTE_HC23: 0x10317
B0_P1_ROUTE_HC24: 0x10318	B0_P1_ROUTE_HC25: 0x10319
B0_P1_ROUTE_HC26: 0x1031A	B0_P1_ROUTE_HC27: 0x1031B
B0_P1_ROUTE_HC28: 0x1031C	B0_P1_ROUTE_HC29: 0x1031D
B0_P1_ROUTE_HC30: 0x1031E	B0_P1_ROUTE_HC31: 0x1031F
B0_P1_ROUTE_HC32: 0x10320	B0_P1_ROUTE_HC33: 0x10321
B0_P1_ROUTE_HC34: 0x10322	B0_P1_ROUTE_HC35: 0x10323
B0_P1_ROUTE_HC36: 0x10324	B0_P1_ROUTE_HC37: 0x10325
B0_P1_ROUTE_HC38: 0x10326	B0_P1_ROUTE_HC39: 0x10327
B0_P1_ROUTE_HC40: 0x10328	B0_P1_ROUTE_HC41: 0x10329
B0_P1_ROUTE_HC42: 0x1032A	B0_P1_ROUTE_HC43: 0x1032B
B0_P1_ROUTE_HC44: 0x1032C	B0_P1_ROUTE_HC45: 0x1032D
B0_P1_ROUTE_HC46: 0x1032E	B0_P1_ROUTE_HC47: 0x1032F
B0_P1_ROUTE_HC48: 0x10330	B0_P1_ROUTE_HC49: 0x10331
B0_P1_ROUTE_HC50: 0x10332	B0_P1_ROUTE_HC51: 0x10333
B0_P1_ROUTE_HC52: 0x10334	B0_P1_ROUTE_HC53: 0x10335
B0_P1_ROUTE_HC54: 0x10336	B0_P1_ROUTE_HC55: 0x10337
B0_P1_ROUTE_HC56: 0x10338	B0_P1_ROUTE_HC57: 0x10339
B0_P1_ROUTE_HC58: 0x1033A	B0_P1_ROUTE_HC59: 0x1033B
B0_P1_ROUTE_HC60: 0x1033C	B0_P1_ROUTE_HC61: 0x1033D
B0_P1_ROUTE_HC62: 0x1033E	B0_P1_ROUTE_HC63: 0x1033F
B0_P1_ROUTE_HC64: 0x10340	B0_P1_ROUTE_HC65: 0x10341
B0_P1_ROUTE_HC66: 0x10342	B0_P1_ROUTE_HC67: 0x10343
B0_P1_ROUTE_HC68: 0x10344	B0_P1_ROUTE_HC69: 0x10345
B0_P1_ROUTE_HC70: 0x10346	B0_P1_ROUTE_HC71: 0x10347
B0_P1_ROUTE_HC72: 0x10348	B0_P1_ROUTE_HC73: 0x10349
B0_P1_ROUTE_HC74: 0x1034A	B0_P1_ROUTE_HC75: 0x1034B
B0_P1_ROUTE_HC76: 0x1034C	B0_P1_ROUTE_HC77: 0x1034D
B0_P1_ROUTE_HC78: 0x1034E	B0_P1_ROUTE_HC79: 0x1034F
B0_P1_ROUTE_HC80: 0x10350	B0_P1_ROUTE_HC81: 0x10351

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Register : Address	
B0_P1_ROUTE_HC82: 0x10352	B0_P1_ROUTE_HC83: 0x10353
B0_P1_ROUTE_HC84: 0x10354	B0_P1_ROUTE_HC85: 0x10355
B0_P1_ROUTE_HC86: 0x10356	B0_P1_ROUTE_HC87: 0x10357
B0_P1_ROUTE_HC88: 0x10358	B0_P1_ROUTE_HC89: 0x10359
B0_P1_ROUTE_HC90: 0x1035A	B0_P1_ROUTE_HC91: 0x1035B
B0_P1_ROUTE_HC92: 0x1035C	B0_P1_ROUTE_HC93: 0x1035D
B0_P1_ROUTE_HC94: 0x1035E	B0_P1_ROUTE_HC95: 0x1035F
B0_P1_ROUTE_HC96: 0x10360	B0_P1_ROUTE_HC97: 0x10361
B0_P1_ROUTE_HC98: 0x10362	B0_P1_ROUTE_HC99: 0x10363
B0_P1_ROUTE_HC100: 0x10364	B0_P1_ROUTE_HC101: 0x10365
B0_P1_ROUTE_HC102: 0x10366	B0_P1_ROUTE_HC103: 0x10367
B0_P1_ROUTE_HC104: 0x10368	B0_P1_ROUTE_HC105: 0x10369
B0_P1_ROUTE_HC106: 0x1036A	B0_P1_ROUTE_HC107: 0x1036B
B0_P1_ROUTE_HC108: 0x1036C	B0_P1_ROUTE_HC109: 0x1036D
B0_P1_ROUTE_HC110: 0x1036E	B0_P1_ROUTE_HC111: 0x1036F
B0_P1_ROUTE_HC112: 0x10370	B0_P1_ROUTE_HC113: 0x10371
B0_P1_ROUTE_HC114: 0x10372	B0_P1_ROUTE_HC115: 0x10373
B0_P1_ROUTE_HC116: 0x10374	B0_P1_ROUTE_HC117: 0x10375
B0_P1_ROUTE_HC118: 0x10376	B0_P1_ROUTE_HC119: 0x10377
B0_P1_ROUTE_HC120: 0x10378	B0_P1_ROUTE_HC121: 0x10379
B0_P1_ROUTE_HC122: 0x1037A	B0_P1_ROUTE_HC123: 0x1037B
B0_P1_ROUTE_HC124: 0x1037C	B0_P1_ROUTE_HC125: 0x1037D
B0_P1_ROUTE_HC126: 0x1037E	B0_P1_ROUTE_HC127: 0x1037F
B0_P2_ROUTE_HC0: 0x10500	B0_P2_ROUTE_HC1: 0x10501
B0_P2_ROUTE_HC2: 0x10502	B0_P2_ROUTE_HC3: 0x10503
B0_P2_ROUTE_HC4: 0x10504	B0_P2_ROUTE_HC5: 0x10505
B0_P2_ROUTE_HC6: 0x10506	B0_P2_ROUTE_HC7: 0x10507
B0_P2_ROUTE_HC8: 0x10508	B0_P2_ROUTE_HC9: 0x10509
B0_P2_ROUTE_HC10: 0x1050A	B0_P2_ROUTE_HC11: 0x1050B
B0_P2_ROUTE_HC12: 0x1050C	B0_P2_ROUTE_HC13: 0x1050D
B0_P2_ROUTE_HC14: 0x1050E	B0_P2_ROUTE_HC15: 0x1050F
B0_P2_ROUTE_HC16: 0x10510	B0_P2_ROUTE_HC17: 0x10511
B0_P2_ROUTE_HC18: 0x10512	B0_P2_ROUTE_HC19: 0x10513
B0_P2_ROUTE_HC20: 0x10514	B0_P2_ROUTE_HC21: 0x10515
B0_P2_ROUTE_HC22: 0x10516	B0_P2_ROUTE_HC23: 0x10517
B0_P2_ROUTE_HC24: 0x10518	B0_P2_ROUTE_HC25: 0x10519

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Register : Address	
B0_P2_ROUTE_HC26: 0x1051A	B0_P2_ROUTE_HC27: 0x1051B
B0_P2_ROUTE_HC28: 0x1051C	B0_P2_ROUTE_HC29: 0x1051D
B0_P2_ROUTE_HC30: 0x1051E	B0_P2_ROUTE_HC31: 0x1051F
B0_P2_ROUTE_HC32: 0x10520	B0_P2_ROUTE_HC33: 0x10521
B0_P2_ROUTE_HC34: 0x10522	B0_P2_ROUTE_HC35: 0x10523
B0_P2_ROUTE_HC36: 0x10524	B0_P2_ROUTE_HC37: 0x10525
B0_P2_ROUTE_HC38: 0x10526	B0_P2_ROUTE_HC39: 0x10527
B0_P2_ROUTE_HC40: 0x10528	B0_P2_ROUTE_HC41: 0x10529
B0_P2_ROUTE_HC42: 0x1052A	B0_P2_ROUTE_HC43: 0x1052B
B0_P2_ROUTE_HC44: 0x1052C	B0_P2_ROUTE_HC45: 0x1052D
B0_P2_ROUTE_HC46: 0x1052E	B0_P2_ROUTE_HC47: 0x1052F
B0_P2_ROUTE_HC48: 0x10530	B0_P2_ROUTE_HC49: 0x10531
B0_P2_ROUTE_HC50: 0x10532	B0_P2_ROUTE_HC51: 0x10533
B0_P2_ROUTE_HC52: 0x10534	B0_P2_ROUTE_HC53: 0x10535
B0_P2_ROUTE_HC54: 0x10536	B0_P2_ROUTE_HC55: 0x10537
B0_P2_ROUTE_HC56: 0x10538	B0_P2_ROUTE_HC57: 0x10539
B0_P2_ROUTE_HC58: 0x1053A	B0_P2_ROUTE_HC59: 0x1053B
B0_P2_ROUTE_HC60: 0x1053C	B0_P2_ROUTE_HC61: 0x1053D
B0_P2_ROUTE_HC62: 0x1053E	B0_P2_ROUTE_HC63: 0x1053F
B0_P2_ROUTE_HC64: 0x10540	B0_P2_ROUTE_HC65: 0x10541
B0_P2_ROUTE_HC66: 0x10542	B0_P2_ROUTE_HC67: 0x10543
B0_P2_ROUTE_HC68: 0x10544	B0_P2_ROUTE_HC69: 0x10545
B0_P2_ROUTE_HC70: 0x10546	B0_P2_ROUTE_HC71: 0x10547
B0_P2_ROUTE_HC72: 0x10548	B0_P2_ROUTE_HC73: 0x10549
B0_P2_ROUTE_HC74: 0x1054A	B0_P2_ROUTE_HC75: 0x1054B
B0_P2_ROUTE_HC76: 0x1054C	B0_P2_ROUTE_HC77: 0x1054D
B0_P2_ROUTE_HC78: 0x1054E	B0_P2_ROUTE_HC79: 0x1054F
B0_P2_ROUTE_HC80: 0x10550	B0_P2_ROUTE_HC81: 0x10551
B0_P2_ROUTE_HC82: 0x10552	B0_P2_ROUTE_HC83: 0x10553
B0_P2_ROUTE_HC84: 0x10554	B0_P2_ROUTE_HC85: 0x10555
B0_P2_ROUTE_HC86: 0x10556	B0_P2_ROUTE_HC87: 0x10557
B0_P2_ROUTE_HC88: 0x10558	B0_P2_ROUTE_HC89: 0x10559
B0_P2_ROUTE_HC90: 0x1055A	B0_P2_ROUTE_HC91: 0x1055B
B0_P2_ROUTE_HC92: 0x1055C	B0_P2_ROUTE_HC93: 0x1055D
B0_P2_ROUTE_HC94: 0x1055E	B0_P2_ROUTE_HC95: 0x1055F
B0_P2_ROUTE_HC96: 0x10560	B0_P2_ROUTE_HC97: 0x10561

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Register : Address	
B0_P2_ROUTE_HC98: 0x10562	B0_P2_ROUTE_HC99: 0x10563
B0_P2_ROUTE_HC100: 0x10564	B0_P2_ROUTE_HC101: 0x10565
B0_P2_ROUTE_HC102: 0x10566	B0_P2_ROUTE_HC103: 0x10567
B0_P2_ROUTE_HC104: 0x10568	B0_P2_ROUTE_HC105: 0x10569
B0_P2_ROUTE_HC106: 0x1056A	B0_P2_ROUTE_HC107: 0x1056B
B0_P2_ROUTE_HC108: 0x1056C	B0_P2_ROUTE_HC109: 0x1056D
B0_P2_ROUTE_HC110: 0x1056E	B0_P2_ROUTE_HC111: 0x1056F
B0_P2_ROUTE_HC112: 0x10570	B0_P2_ROUTE_HC113: 0x10571
B0_P2_ROUTE_HC114: 0x10572	B0_P2_ROUTE_HC115: 0x10573
B0_P2_ROUTE_HC116: 0x10574	B0_P2_ROUTE_HC117: 0x10575
B0_P2_ROUTE_HC118: 0x10576	B0_P2_ROUTE_HC119: 0x10577
B0_P2_ROUTE_HC120: 0x10578	B0_P2_ROUTE_HC121: 0x10579
B0_P2_ROUTE_HC122: 0x1057A	B0_P2_ROUTE_HC123: 0x1057B
B0_P2_ROUTE_HC124: 0x1057C	B0_P2_ROUTE_HC125: 0x1057D
B0_P2_ROUTE_HC126: 0x1057E	B0_P2_ROUTE_HC127: 0x1057F
B0_P3_ROUTE_HC0: 0x10700	B0_P3_ROUTE_HC1: 0x10701
B0_P3_ROUTE_HC2: 0x10702	B0_P3_ROUTE_HC3: 0x10703
B0_P3_ROUTE_HC4: 0x10704	B0_P3_ROUTE_HC5: 0x10705
B0_P3_ROUTE_HC6: 0x10706	B0_P3_ROUTE_HC7: 0x10707
B0_P3_ROUTE_HC8: 0x10708	B0_P3_ROUTE_HC9: 0x10709
B0_P3_ROUTE_HC10: 0x1070A	B0_P3_ROUTE_HC11: 0x1070B
B0_P3_ROUTE_HC12: 0x1070C	B0_P3_ROUTE_HC13: 0x1070D
B0_P3_ROUTE_HC14: 0x1070E	B0_P3_ROUTE_HC15: 0x1070F
B0_P3_ROUTE_HC16: 0x10710	B0_P3_ROUTE_HC17: 0x10711
B0_P3_ROUTE_HC18: 0x10712	B0_P3_ROUTE_HC19: 0x10713
B0_P3_ROUTE_HC20: 0x10714	B0_P3_ROUTE_HC21: 0x10715
B0_P3_ROUTE_HC22: 0x10716	B0_P3_ROUTE_HC23: 0x10717
B0_P3_ROUTE_HC24: 0x10718	B0_P3_ROUTE_HC25: 0x10719
B0_P3_ROUTE_HC26: 0x1071A	B0_P3_ROUTE_HC27: 0x1071B
B0_P3_ROUTE_HC28: 0x1071C	B0_P3_ROUTE_HC29: 0x1071D
B0_P3_ROUTE_HC30: 0x1071E	B0_P3_ROUTE_HC31: 0x1071F
B0_P3_ROUTE_HC32: 0x10720	B0_P3_ROUTE_HC33: 0x10721
B0_P3_ROUTE_HC34: 0x10722	B0_P3_ROUTE_HC35: 0x10723
B0_P3_ROUTE_HC36: 0x10724	B0_P3_ROUTE_HC37: 0x10725
B0_P3_ROUTE_HC38: 0x10726	B0_P3_ROUTE_HC39: 0x10727
B0_P3_ROUTE_HC40: 0x10728	B0_P3_ROUTE_HC41: 0x10729

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Register : Address	
B0_P3_ROUTE_HC42: 0x1072A	B0_P3_ROUTE_HC43: 0x1072B
B0_P3_ROUTE_HC44: 0x1072C	B0_P3_ROUTE_HC45: 0x1072D
B0_P3_ROUTE_HC46: 0x1072E	B0_P3_ROUTE_HC47: 0x1072F
B0_P3_ROUTE_HC48: 0x10730	B0_P3_ROUTE_HC49: 0x10731
B0_P3_ROUTE_HC50: 0x10732	B0_P3_ROUTE_HC51: 0x10733
B0_P3_ROUTE_HC52: 0x10734	B0_P3_ROUTE_HC53: 0x10735
B0_P3_ROUTE_HC54: 0x10736	B0_P3_ROUTE_HC55: 0x10737
B0_P3_ROUTE_HC56: 0x10738	B0_P3_ROUTE_HC57: 0x10739
B0_P3_ROUTE_HC58: 0x1073A	B0_P3_ROUTE_HC59: 0x1073B
B0_P3_ROUTE_HC60: 0x1073C	B0_P3_ROUTE_HC61: 0x1073D
B0_P3_ROUTE_HC62: 0x1073E	B0_P3_ROUTE_HC63: 0x1073F
B0_P3_ROUTE_HC64: 0x10740	B0_P3_ROUTE_HC65: 0x10741
B0_P3_ROUTE_HC66: 0x10742	B0_P3_ROUTE_HC67: 0x10743
B0_P3_ROUTE_HC68: 0x10744	B0_P3_ROUTE_HC69: 0x10745
B0_P3_ROUTE_HC70: 0x10746	B0_P3_ROUTE_HC71: 0x10747
B0_P3_ROUTE_HC72: 0x10748	B0_P3_ROUTE_HC73: 0x10749
B0_P3_ROUTE_HC74: 0x1074A	B0_P3_ROUTE_HC75: 0x1074B
B0_P3_ROUTE_HC76: 0x1074C	B0_P3_ROUTE_HC77: 0x1074D
B0_P3_ROUTE_HC78: 0x1074E	B0_P3_ROUTE_HC79: 0x1074F
B0_P3_ROUTE_HC80: 0x10750	B0_P3_ROUTE_HC81: 0x10751
B0_P3_ROUTE_HC82: 0x10752	B0_P3_ROUTE_HC83: 0x10753
B0_P3_ROUTE_HC84: 0x10754	B0_P3_ROUTE_HC85: 0x10755
B0_P3_ROUTE_HC86: 0x10756	B0_P3_ROUTE_HC87: 0x10757
B0_P3_ROUTE_HC88: 0x10758	B0_P3_ROUTE_HC89: 0x10759
B0_P3_ROUTE_HC90: 0x1075A	B0_P3_ROUTE_HC91: 0x1075B
B0_P3_ROUTE_HC92: 0x1075C	B0_P3_ROUTE_HC93: 0x1075D
B0_P3_ROUTE_HC94: 0x1075E	B0_P3_ROUTE_HC95: 0x1075F
B0_P3_ROUTE_HC96: 0x10760	B0_P3_ROUTE_HC97: 0x10761
B0_P3_ROUTE_HC98: 0x10762	B0_P3_ROUTE_HC99: 0x10763
B0_P3_ROUTE_HC100: 0x10764	B0_P3_ROUTE_HC101: 0x10765
B0_P3_ROUTE_HC102: 0x10766	B0_P3_ROUTE_HC103: 0x10767
B0_P3_ROUTE_HC104: 0x10768	B0_P3_ROUTE_HC105: 0x10769
B0_P3_ROUTE_HC106: 0x1076A	B0_P3_ROUTE_HC107: 0x1076B
B0_P3_ROUTE_HC108: 0x1076C	B0_P3_ROUTE_HC109: 0x1076D
B0_P3_ROUTE_HC110: 0x1076E	B0_P3_ROUTE_HC111: 0x1076F
B0_P3_ROUTE_HC112: 0x10770	B0_P3_ROUTE_HC113: 0x10771

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Register : Address	
B0_P3_ROUTE_HC114: 0x10772	B0_P3_ROUTE_HC115: 0x10773
B0_P3_ROUTE_HC116: 0x10774	B0_P3_ROUTE_HC117: 0x10775
B0_P3_ROUTE_HC118: 0x10776	B0_P3_ROUTE_HC119: 0x10777
B0_P3_ROUTE_HC120: 0x10778	B0_P3_ROUTE_HC121: 0x10779
B0_P3_ROUTE_HC122: 0x1077A	B0_P3_ROUTE_HC123: 0x1077B
B0_P3_ROUTE_HC124: 0x1077C	B0_P3_ROUTE_HC125: 0x1077D
B0_P3_ROUTE_HC126: 0x1077E	B0_P3_ROUTE_HC127: 0x1077F
B0_P4_ROUTE_HC0: 0x10900	B0_P4_ROUTE_HC1: 0x10901
B0_P4_ROUTE_HC2: 0x10902	B0_P4_ROUTE_HC3: 0x10903
B0_P4_ROUTE_HC4: 0x10904	B0_P4_ROUTE_HC5: 0x10905
B0_P4_ROUTE_HC6: 0x10906	B0_P4_ROUTE_HC7: 0x10907
B0_P4_ROUTE_HC8: 0x10908	B0_P4_ROUTE_HC9: 0x10909
B0_P4_ROUTE_HC10: 0x1090A	B0_P4_ROUTE_HC11: 0x1090B
B0_P4_ROUTE_HC12: 0x1090C	B0_P4_ROUTE_HC13: 0x1090D
B0_P4_ROUTE_HC14: 0x1090E	B0_P4_ROUTE_HC15: 0x1090F
B0_P4_ROUTE_HC16: 0x10910	B0_P4_ROUTE_HC17: 0x10911
B0_P4_ROUTE_HC18: 0x10912	B0_P4_ROUTE_HC19: 0x10913
B0_P4_ROUTE_HC20: 0x10914	B0_P4_ROUTE_HC21: 0x10915
B0_P4_ROUTE_HC22: 0x10916	B0_P4_ROUTE_HC23: 0x10917
B0_P4_ROUTE_HC24: 0x10918	B0_P4_ROUTE_HC25: 0x10919
B0_P4_ROUTE_HC26: 0x1091A	B0_P4_ROUTE_HC27: 0x1091B
B0_P4_ROUTE_HC28: 0x1091C	B0_P4_ROUTE_HC29: 0x1091D
B0_P4_ROUTE_HC30: 0x1091E	B0_P4_ROUTE_HC31: 0x1091F
B0_P4_ROUTE_HC32: 0x10920	B0_P4_ROUTE_HC33: 0x10921
B0_P4_ROUTE_HC34: 0x10922	B0_P4_ROUTE_HC35: 0x10923
B0_P4_ROUTE_HC36: 0x10924	B0_P4_ROUTE_HC37: 0x10925
B0_P4_ROUTE_HC38: 0x10926	B0_P4_ROUTE_HC39: 0x10927
B0_P4_ROUTE_HC40: 0x10928	B0_P4_ROUTE_HC41: 0x10929
B0_P4_ROUTE_HC42: 0x1092A	B0_P4_ROUTE_HC43: 0x1092B
B0_P4_ROUTE_HC44: 0x1092C	B0_P4_ROUTE_HC45: 0x1092D
B0_P4_ROUTE_HC46: 0x1092E	B0_P4_ROUTE_HC47: 0x1092F
B0_P4_ROUTE_HC48: 0x10930	B0_P4_ROUTE_HC49: 0x10931
B0_P4_ROUTE_HC50: 0x10932	B0_P4_ROUTE_HC51: 0x10933
B0_P4_ROUTE_HC52: 0x10934	B0_P4_ROUTE_HC53: 0x10935
B0_P4_ROUTE_HC54: 0x10936	B0_P4_ROUTE_HC55: 0x10937
B0_P4_ROUTE_HC56: 0x10938	B0_P4_ROUTE_HC57: 0x10939

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Register : Address	
B0_P4_ROUTE_HC58: 0x1093A	B0_P4_ROUTE_HC59: 0x1093B
B0_P4_ROUTE_HC60: 0x1093C	B0_P4_ROUTE_HC61: 0x1093D
B0_P4_ROUTE_HC62: 0x1093E	B0_P4_ROUTE_HC63: 0x1093F
B0_P4_ROUTE_HC64: 0x10940	B0_P4_ROUTE_HC65: 0x10941
B0_P4_ROUTE_HC66: 0x10942	B0_P4_ROUTE_HC67: 0x10943
B0_P4_ROUTE_HC68: 0x10944	B0_P4_ROUTE_HC69: 0x10945
B0_P4_ROUTE_HC70: 0x10946	B0_P4_ROUTE_HC71: 0x10947
B0_P4_ROUTE_HC72: 0x10948	B0_P4_ROUTE_HC73: 0x10949
B0_P4_ROUTE_HC74: 0x1094A	B0_P4_ROUTE_HC75: 0x1094B
B0_P4_ROUTE_HC76: 0x1094C	B0_P4_ROUTE_HC77: 0x1094D
B0_P4_ROUTE_HC78: 0x1094E	B0_P4_ROUTE_HC79: 0x1094F
B0_P4_ROUTE_HC80: 0x10950	B0_P4_ROUTE_HC81: 0x10951
B0_P4_ROUTE_HC82: 0x10952	B0_P4_ROUTE_HC83: 0x10953
B0_P4_ROUTE_HC84: 0x10954	B0_P4_ROUTE_HC85: 0x10955
B0_P4_ROUTE_HC86: 0x10956	B0_P4_ROUTE_HC87: 0x10957
B0_P4_ROUTE_HC88: 0x10958	B0_P4_ROUTE_HC89: 0x10959
B0_P4_ROUTE_HC90: 0x1095A	B0_P4_ROUTE_HC91: 0x1095B
B0_P4_ROUTE_HC92: 0x1095C	B0_P4_ROUTE_HC93: 0x1095D
B0_P4_ROUTE_HC94: 0x1095E	B0_P4_ROUTE_HC95: 0x1095F
B0_P4_ROUTE_HC96: 0x10960	B0_P4_ROUTE_HC97: 0x10961
B0_P4_ROUTE_HC98: 0x10962	B0_P4_ROUTE_HC99: 0x10963
B0_P4_ROUTE_HC100: 0x10964	B0_P4_ROUTE_HC101: 0x10965
B0_P4_ROUTE_HC102: 0x10966	B0_P4_ROUTE_HC103: 0x10967
B0_P4_ROUTE_HC104: 0x10968	B0_P4_ROUTE_HC105: 0x10969
B0_P4_ROUTE_HC106: 0x1096A	B0_P4_ROUTE_HC107: 0x1096B
B0_P4_ROUTE_HC108: 0x1096C	B0_P4_ROUTE_HC109: 0x1096D
B0_P4_ROUTE_HC110: 0x1096E	B0_P4_ROUTE_HC111: 0x1096F
B0_P4_ROUTE_HC112: 0x10970	B0_P4_ROUTE_HC113: 0x10971
B0_P4_ROUTE_HC114: 0x10972	B0_P4_ROUTE_HC115: 0x10973
B0_P4_ROUTE_HC116: 0x10974	B0_P4_ROUTE_HC117: 0x10975
B0_P4_ROUTE_HC118: 0x10976	B0_P4_ROUTE_HC119: 0x10977
B0_P4_ROUTE_HC120: 0x10978	B0_P4_ROUTE_HC121: 0x10979
B0_P4_ROUTE_HC122: 0x1097A	B0_P4_ROUTE_HC123: 0x1097B
B0_P4_ROUTE_HC124: 0x1097C	B0_P4_ROUTE_HC125: 0x1097D
B0_P4_ROUTE_HC126: 0x1097E	B0_P4_ROUTE_HC127: 0x1097F
B0_P5_ROUTE_HC0: 0x10B00	B0_P5_ROUTE_HC1: 0x10B01

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Register : Address	
B0_P5_ROUTE_HC2: 0x10B02	B0_P5_ROUTE_HC3: 0x10B03
B0_P5_ROUTE_HC4: 0x10B04	B0_P5_ROUTE_HC5: 0x10B05
B0_P5_ROUTE_HC6: 0x10B06	B0_P5_ROUTE_HC7: 0x10B07
B0_P5_ROUTE_HC8: 0x10B08	B0_P5_ROUTE_HC9: 0x10B09
B0_P5_ROUTE_HC10: 0x10B0A	B0_P5_ROUTE_HC11: 0x10B0B
B0_P5_ROUTE_HC12: 0x10B0C	B0_P5_ROUTE_HC13: 0x10B0D
B0_P5_ROUTE_HC14: 0x10B0E	B0_P5_ROUTE_HC15: 0x10B0F
B0_P5_ROUTE_HC16: 0x10B10	B0_P5_ROUTE_HC17: 0x10B11
B0_P5_ROUTE_HC18: 0x10B12	B0_P5_ROUTE_HC19: 0x10B13
B0_P5_ROUTE_HC20: 0x10B14	B0_P5_ROUTE_HC21: 0x10B15
B0_P5_ROUTE_HC22: 0x10B16	B0_P5_ROUTE_HC23: 0x10B17
B0_P5_ROUTE_HC24: 0x10B18	B0_P5_ROUTE_HC25: 0x10B19
B0_P5_ROUTE_HC26: 0x10B1A	B0_P5_ROUTE_HC27: 0x10B1B
B0_P5_ROUTE_HC28: 0x10B1C	B0_P5_ROUTE_HC29: 0x10B1D
B0_P5_ROUTE_HC30: 0x10B1E	B0_P5_ROUTE_HC31: 0x10B1F
B0_P5_ROUTE_HC32: 0x10B20	B0_P5_ROUTE_HC33: 0x10B21
B0_P5_ROUTE_HC34: 0x10B22	B0_P5_ROUTE_HC35: 0x10B23
B0_P5_ROUTE_HC36: 0x10B24	B0_P5_ROUTE_HC37: 0x10B25
B0_P5_ROUTE_HC38: 0x10B26	B0_P5_ROUTE_HC39: 0x10B27
B0_P5_ROUTE_HC40: 0x10B28	B0_P5_ROUTE_HC41: 0x10B29
B0_P5_ROUTE_HC42: 0x10B2A	B0_P5_ROUTE_HC43: 0x10B2B
B0_P5_ROUTE_HC44: 0x10B2C	B0_P5_ROUTE_HC45: 0x10B2D
B0_P5_ROUTE_HC46: 0x10B2E	B0_P5_ROUTE_HC47: 0x10B2F
B0_P5_ROUTE_HC48: 0x10B30	B0_P5_ROUTE_HC49: 0x10B31
B0_P5_ROUTE_HC50: 0x10B32	B0_P5_ROUTE_HC51: 0x10B33
B0_P5_ROUTE_HC52: 0x10B34	B0_P5_ROUTE_HC53: 0x10B35
B0_P5_ROUTE_HC54: 0x10B36	B0_P5_ROUTE_HC55: 0x10B37
B0_P5_ROUTE_HC56: 0x10B38	B0_P5_ROUTE_HC57: 0x10B39
B0_P5_ROUTE_HC58: 0x10B3A	B0_P5_ROUTE_HC59: 0x10B3B
B0_P5_ROUTE_HC60: 0x10B3C	B0_P5_ROUTE_HC61: 0x10B3D
B0_P5_ROUTE_HC62: 0x10B3E	B0_P5_ROUTE_HC63: 0x10B3F
B0_P5_ROUTE_HC64: 0x10B40	B0_P5_ROUTE_HC65: 0x10B41
B0_P5_ROUTE_HC66: 0x10B42	B0_P5_ROUTE_HC67: 0x10B43
B0_P5_ROUTE_HC68: 0x10B44	B0_P5_ROUTE_HC69: 0x10B45
B0_P5_ROUTE_HC70: 0x10B46	B0_P5_ROUTE_HC71: 0x10B47
B0_P5_ROUTE_HC72: 0x10B48	B0_P5_ROUTE_HC73: 0x10B49

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Register : Address	
B0_P5_ROUTE_HC74: 0x10B4A	B0_P5_ROUTE_HC75: 0x10B4B
B0_P5_ROUTE_HC76: 0x10B4C	B0_P5_ROUTE_HC77: 0x10B4D
B0_P5_ROUTE_HC78: 0x10B4E	B0_P5_ROUTE_HC79: 0x10B4F
B0_P5_ROUTE_HC80: 0x10B50	B0_P5_ROUTE_HC81: 0x10B51
B0_P5_ROUTE_HC82: 0x10B52	B0_P5_ROUTE_HC83: 0x10B53
B0_P5_ROUTE_HC84: 0x10B54	B0_P5_ROUTE_HC85: 0x10B55
B0_P5_ROUTE_HC86: 0x10B56	B0_P5_ROUTE_HC87: 0x10B57
B0_P5_ROUTE_HC88: 0x10B58	B0_P5_ROUTE_HC89: 0x10B59
B0_P5_ROUTE_HC90: 0x10B5A	B0_P5_ROUTE_HC91: 0x10B5B
B0_P5_ROUTE_HC92: 0x10B5C	B0_P5_ROUTE_HC93: 0x10B5D
B0_P5_ROUTE_HC94: 0x10B5E	B0_P5_ROUTE_HC95: 0x10B5F
B0_P5_ROUTE_HC96: 0x10B60	B0_P5_ROUTE_HC97: 0x10B61
B0_P5_ROUTE_HC98: 0x10B62	B0_P5_ROUTE_HC99: 0x10B63
B0_P5_ROUTE_HC100: 0x10B64	B0_P5_ROUTE_HC101: 0x10B65
B0_P5_ROUTE_HC102: 0x10B66	B0_P5_ROUTE_HC103: 0x10B67
B0_P5_ROUTE_HC104: 0x10B68	B0_P5_ROUTE_HC105: 0x10B69
B0_P5_ROUTE_HC106: 0x10B6A	B0_P5_ROUTE_HC107: 0x10B6B
B0_P5_ROUTE_HC108: 0x10B6C	B0_P5_ROUTE_HC109: 0x10B6D
B0_P5_ROUTE_HC110: 0x10B6E	B0_P5_ROUTE_HC111: 0x10B6F
B0_P5_ROUTE_HC112: 0x10B70	B0_P5_ROUTE_HC113: 0x10B71
B0_P5_ROUTE_HC114: 0x10B72	B0_P5_ROUTE_HC115: 0x10B73
B0_P5_ROUTE_HC116: 0x10B74	B0_P5_ROUTE_HC117: 0x10B75
B0_P5_ROUTE_HC118: 0x10B76	B0_P5_ROUTE_HC119: 0x10B77
B0_P5_ROUTE_HC120: 0x10B78	B0_P5_ROUTE_HC121: 0x10B79
B0_P5_ROUTE_HC122: 0x10B7A	B0_P5_ROUTE_HC123: 0x10B7B
B0_P5_ROUTE_HC124: 0x10B7C	B0_P5_ROUTE_HC125: 0x10B7D
B0_P5_ROUTE_HC126: 0x10B7E	B0_P5_ROUTE_HC127: 0x10B7F
B0_P6_ROUTE_HC0: 0x10D00	B0_P6_ROUTE_HC1: 0x10D01
B0_P6_ROUTE_HC2: 0x10D02	B0_P6_ROUTE_HC3: 0x10D03
B0_P6_ROUTE_HC4: 0x10D04	B0_P6_ROUTE_HC5: 0x10D05
B0_P6_ROUTE_HC6: 0x10D06	B0_P6_ROUTE_HC7: 0x10D07
B0_P6_ROUTE_HC8: 0x10D08	B0_P6_ROUTE_HC9: 0x10D09
B0_P6_ROUTE_HC10: 0x10D0A	B0_P6_ROUTE_HC11: 0x10D0B
B0_P6_ROUTE_HC12: 0x10D0C	B0_P6_ROUTE_HC13: 0x10D0D
B0_P6_ROUTE_HC14: 0x10D0E	B0_P6_ROUTE_HC15: 0x10D0F
B0_P6_ROUTE_HC16: 0x10D10	B0_P6_ROUTE_HC17: 0x10D11

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Register : Address	
B0_P6_ROUTE_HC18: 0x10D12	B0_P6_ROUTE_HC19: 0x10D13
B0_P6_ROUTE_HC20: 0x10D14	B0_P6_ROUTE_HC21: 0x10D15
B0_P6_ROUTE_HC22: 0x10D16	B0_P6_ROUTE_HC23: 0x10D17
B0_P6_ROUTE_HC24: 0x10D18	B0_P6_ROUTE_HC25: 0x10D19
B0_P6_ROUTE_HC26: 0x10D1A	B0_P6_ROUTE_HC27: 0x10D1B
B0_P6_ROUTE_HC28: 0x10D1C	B0_P6_ROUTE_HC29: 0x10D1D
B0_P6_ROUTE_HC30: 0x10D1E	B0_P6_ROUTE_HC31: 0x10D1F
B0_P6_ROUTE_HC32: 0x10D20	B0_P6_ROUTE_HC33: 0x10D21
B0_P6_ROUTE_HC34: 0x10D22	B0_P6_ROUTE_HC35: 0x10D23
B0_P6_ROUTE_HC36: 0x10D24	B0_P6_ROUTE_HC37: 0x10D25
B0_P6_ROUTE_HC38: 0x10D26	B0_P6_ROUTE_HC39: 0x10D27
B0_P6_ROUTE_HC40: 0x10D28	B0_P6_ROUTE_HC41: 0x10D29
B0_P6_ROUTE_HC42: 0x10D2A	B0_P6_ROUTE_HC43: 0x10D2B
B0_P6_ROUTE_HC44: 0x10D2C	B0_P6_ROUTE_HC45: 0x10D2D
B0_P6_ROUTE_HC46: 0x10D2E	B0_P6_ROUTE_HC47: 0x10D2F
B0_P6_ROUTE_HC48: 0x10D30	B0_P6_ROUTE_HC49: 0x10D31
B0_P6_ROUTE_HC50: 0x10D32	B0_P6_ROUTE_HC51: 0x10D33
B0_P6_ROUTE_HC52: 0x10D34	B0_P6_ROUTE_HC53: 0x10D35
B0_P6_ROUTE_HC54: 0x10D36	B0_P6_ROUTE_HC55: 0x10D37
B0_P6_ROUTE_HC56: 0x10D38	B0_P6_ROUTE_HC57: 0x10D39
B0_P6_ROUTE_HC58: 0x10D3A	B0_P6_ROUTE_HC59: 0x10D3B
B0_P6_ROUTE_HC60: 0x10D3C	B0_P6_ROUTE_HC61: 0x10D3D
B0_P6_ROUTE_HC62: 0x10D3E	B0_P6_ROUTE_HC63: 0x10D3F
B0_P6_ROUTE_HC64: 0x10D40	B0_P6_ROUTE_HC65: 0x10D41
B0_P6_ROUTE_HC66: 0x10D42	B0_P6_ROUTE_HC67: 0x10D43
B0_P6_ROUTE_HC68: 0x10D44	B0_P6_ROUTE_HC69: 0x10D45
B0_P6_ROUTE_HC70: 0x10D46	B0_P6_ROUTE_HC71: 0x10D47
B0_P6_ROUTE_HC72: 0x10D48	B0_P6_ROUTE_HC73: 0x10D49
B0_P6_ROUTE_HC74: 0x10D4A	B0_P6_ROUTE_HC75: 0x10D4B
B0_P6_ROUTE_HC76: 0x10D4C	B0_P6_ROUTE_HC77: 0x10D4D
B0_P6_ROUTE_HC78: 0x10D4E	B0_P6_ROUTE_HC79: 0x10D4F
B0_P6_ROUTE_HC80: 0x10D50	B0_P6_ROUTE_HC81: 0x10D51
B0_P6_ROUTE_HC82: 0x10D52	B0_P6_ROUTE_HC83: 0x10D53
B0_P6_ROUTE_HC84: 0x10D54	B0_P6_ROUTE_HC85: 0x10D55
B0_P6_ROUTE_HC86: 0x10D56	B0_P6_ROUTE_HC87: 0x10D57
B0_P6_ROUTE_HC88: 0x10D58	B0_P6_ROUTE_HC89: 0x10D59

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Register : Address	
B0_P6_ROUTE_HC90: 0x10D5A	B0_P6_ROUTE_HC91: 0x10D5B
B0_P6_ROUTE_HC92: 0x10D5C	B0_P6_ROUTE_HC93: 0x10D5D
B0_P6_ROUTE_HC94: 0x10D5E	B0_P6_ROUTE_HC95: 0x10D5F
B0_P6_ROUTE_HC96: 0x10D60	B0_P6_ROUTE_HC97: 0x10D61
B0_P6_ROUTE_HC98: 0x10D62	B0_P6_ROUTE_HC99: 0x10D63
B0_P6_ROUTE_HC100: 0x10D64	B0_P6_ROUTE_HC101: 0x10D65
B0_P6_ROUTE_HC102: 0x10D66	B0_P6_ROUTE_HC103: 0x10D67
B0_P6_ROUTE_HC104: 0x10D68	B0_P6_ROUTE_HC105: 0x10D69
B0_P6_ROUTE_HC106: 0x10D6A	B0_P6_ROUTE_HC107: 0x10D6B
B0_P6_ROUTE_HC108: 0x10D6C	B0_P6_ROUTE_HC109: 0x10D6D
B0_P6_ROUTE_HC110: 0x10D6E	B0_P6_ROUTE_HC111: 0x10D6F
B0_P6_ROUTE_HC112: 0x10D70	B0_P6_ROUTE_HC113: 0x10D71
B0_P6_ROUTE_HC114: 0x10D72	B0_P6_ROUTE_HC115: 0x10D73
B0_P6_ROUTE_HC116: 0x10D74	B0_P6_ROUTE_HC117: 0x10D75
B0_P6_ROUTE_HC118: 0x10D76	B0_P6_ROUTE_HC119: 0x10D77
B0_P6_ROUTE_HC120: 0x10D78	B0_P6_ROUTE_HC121: 0x10D79
B0_P6_ROUTE_HC122: 0x10D7A	B0_P6_ROUTE_HC123: 0x10D7B
B0_P6_ROUTE_HC124: 0x10D7C	B0_P6_ROUTE_HC125: 0x10D7D
B0_P6_ROUTE_HC126: 0x10D7E	B0_P6_ROUTE_HC127: 0x10D7F
B0_P7_ROUTE_HC0: 0x10F00	B0_P7_ROUTE_HC1: 0x10F01
B0_P7_ROUTE_HC2: 0x10F02	B0_P7_ROUTE_HC3: 0x10F03
B0_P7_ROUTE_HC4: 0x10F04	B0_P7_ROUTE_HC5: 0x10F05
B0_P7_ROUTE_HC6: 0x10F06	B0_P7_ROUTE_HC7: 0x10F07
B0_P7_ROUTE_HC8: 0x10F08	B0_P7_ROUTE_HC9: 0x10F09
B0_P7_ROUTE_HC10: 0x10F0A	B0_P7_ROUTE_HC11: 0x10F0B
B0_P7_ROUTE_HC12: 0x10F0C	B0_P7_ROUTE_HC13: 0x10F0D
B0_P7_ROUTE_HC14: 0x10F0E	B0_P7_ROUTE_HC15: 0x10F0F
B0_P7_ROUTE_HC16: 0x10F10	B0_P7_ROUTE_HC17: 0x10F11
B0_P7_ROUTE_HC18: 0x10F12	B0_P7_ROUTE_HC19: 0x10F13
B0_P7_ROUTE_HC20: 0x10F14	B0_P7_ROUTE_HC21: 0x10F15
B0_P7_ROUTE_HC22: 0x10F16	B0_P7_ROUTE_HC23: 0x10F17
B0_P7_ROUTE_HC24: 0x10F18	B0_P7_ROUTE_HC25: 0x10F19
B0_P7_ROUTE_HC26: 0x10F1A	B0_P7_ROUTE_HC27: 0x10F1B
B0_P7_ROUTE_HC28: 0x10F1C	B0_P7_ROUTE_HC29: 0x10F1D
B0_P7_ROUTE_HC30: 0x10F1E	B0_P7_ROUTE_HC31: 0x10F1F
B0_P7_ROUTE_HC32: 0x10F20	B0_P7_ROUTE_HC33: 0x10F21

(continued)

Register : Address	
B0_P7_ROUTE_HC34: 0x10F22	B0_P7_ROUTE_HC35: 0x10F23
B0_P7_ROUTE_HC36: 0x10F24	B0_P7_ROUTE_HC37: 0x10F25
B0_P7_ROUTE_HC38: 0x10F26	B0_P7_ROUTE_HC39: 0x10F27
B0_P7_ROUTE_HC40: 0x10F28	B0_P7_ROUTE_HC41: 0x10F29
B0_P7_ROUTE_HC42: 0x10F2A	B0_P7_ROUTE_HC43: 0x10F2B
B0_P7_ROUTE_HC44: 0x10F2C	B0_P7_ROUTE_HC45: 0x10F2D
B0_P7_ROUTE_HC46: 0x10F2E	B0_P7_ROUTE_HC47: 0x10F2F
B0_P7_ROUTE_HC48: 0x10F30	B0_P7_ROUTE_HC49: 0x10F31
B0_P7_ROUTE_HC50: 0x10F32	B0_P7_ROUTE_HC51: 0x10F33
B0_P7_ROUTE_HC52: 0x10F34	B0_P7_ROUTE_HC53: 0x10F35
B0_P7_ROUTE_HC54: 0x10F36	B0_P7_ROUTE_HC55: 0x10F37
B0_P7_ROUTE_HC56: 0x10F38	B0_P7_ROUTE_HC57: 0x10F39
B0_P7_ROUTE_HC58: 0x10F3A	B0_P7_ROUTE_HC59: 0x10F3B
B0_P7_ROUTE_HC60: 0x10F3C	B0_P7_ROUTE_HC61: 0x10F3D
B0_P7_ROUTE_HC62: 0x10F3E	B0_P7_ROUTE_HC63: 0x10F3F
B0_P7_ROUTE_HC64: 0x10F40	B0_P7_ROUTE_HC65: 0x10F41
B0_P7_ROUTE_HC66: 0x10F42	B0_P7_ROUTE_HC67: 0x10F43
B0_P7_ROUTE_HC68: 0x10F44	B0_P7_ROUTE_HC69: 0x10F45
B0_P7_ROUTE_HC70: 0x10F46	B0_P7_ROUTE_HC71: 0x10F47
B0_P7_ROUTE_HC72: 0x10F48	B0_P7_ROUTE_HC73: 0x10F49
B0_P7_ROUTE_HC74: 0x10F4A	B0_P7_ROUTE_HC75: 0x10F4B
B0_P7_ROUTE_HC76: 0x10F4C	B0_P7_ROUTE_HC77: 0x10F4D
B0_P7_ROUTE_HC78: 0x10F4E	B0_P7_ROUTE_HC79: 0x10F4F
B0_P7_ROUTE_HC80: 0x10F50	B0_P7_ROUTE_HC81: 0x10F51
B0_P7_ROUTE_HC82: 0x10F52	B0_P7_ROUTE_HC83: 0x10F53
B0_P7_ROUTE_HC84: 0x10F54	B0_P7_ROUTE_HC85: 0x10F55
B0_P7_ROUTE_HC86: 0x10F56	B0_P7_ROUTE_HC87: 0x10F57
B0_P7_ROUTE_HC88: 0x10F58	B0_P7_ROUTE_HC89: 0x10F59
B0_P7_ROUTE_HC90: 0x10F5A	B0_P7_ROUTE_HC91: 0x10F5B
B0_P7_ROUTE_HC92: 0x10F5C	B0_P7_ROUTE_HC93: 0x10F5D
B0_P7_ROUTE_HC94: 0x10F5E	B0_P7_ROUTE_HC95: 0x10F5F
B0_P7_ROUTE_HC96: 0x10F60	B0_P7_ROUTE_HC97: 0x10F61
B0_P7_ROUTE_HC98: 0x10F62	B0_P7_ROUTE_HC99: 0x10F63
B0_P7_ROUTE_HC100: 0x10F64	B0_P7_ROUTE_HC101: 0x10F65
B0_P7_ROUTE_HC102: 0x10F66	B0_P7_ROUTE_HC103: 0x10F67
B0_P7_ROUTE_HC104: 0x10F68	B0_P7_ROUTE_HC105: 0x10F69

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Register : Address	
B0_P7_ROUTE_HC106: 0x10F6A	B0_P7_ROUTE_HC107: 0x10F6B
B0_P7_ROUTE_HC108: 0x10F6C	B0_P7_ROUTE_HC109: 0x10F6D
B0_P7_ROUTE_HC110: 0x10F6E	B0_P7_ROUTE_HC111: 0x10F6F
B0_P7_ROUTE_HC112: 0x10F70	B0_P7_ROUTE_HC113: 0x10F71
B0_P7_ROUTE_HC114: 0x10F72	B0_P7_ROUTE_HC115: 0x10F73
B0_P7_ROUTE_HC116: 0x10F74	B0_P7_ROUTE_HC117: 0x10F75
B0_P7_ROUTE_HC118: 0x10F76	B0_P7_ROUTE_HC119: 0x10F77
B0_P7_ROUTE_HC120: 0x10F78	B0_P7_ROUTE_HC121: 0x10F79
B0_P7_ROUTE_HC122: 0x10F7A	B0_P7_ROUTE_HC123: 0x10F7B
B0_P7_ROUTE_HC124: 0x10F7C	B0_P7_ROUTE_HC125: 0x10F7D
B0_P7_ROUTE_HC126: 0x10F7E	B0_P7_ROUTE_HC127: 0x10F7F
B1_P2_ROUTE_HC0: 0x11500	B1_P2_ROUTE_HC1: 0x11501
B1_P2_ROUTE_HC2: 0x11502	B1_P2_ROUTE_HC3: 0x11503
B1_P2_ROUTE_HC4: 0x11504	B1_P2_ROUTE_HC5: 0x11505
B1_P2_ROUTE_HC6: 0x11506	B1_P2_ROUTE_HC7: 0x11507
B1_P2_ROUTE_HC8: 0x11508	B1_P2_ROUTE_HC9: 0x11509
B1_P2_ROUTE_HC10: 0x1150A	B1_P2_ROUTE_HC11: 0x1150B
B1_P2_ROUTE_HC12: 0x1150C	B1_P2_ROUTE_HC13: 0x1150D
B1_P2_ROUTE_HC14: 0x1150E	B1_P2_ROUTE_HC15: 0x1150F
B1_P2_ROUTE_HC16: 0x11510	B1_P2_ROUTE_HC17: 0x11511
B1_P2_ROUTE_HC18: 0x11512	B1_P2_ROUTE_HC19: 0x11513
B1_P2_ROUTE_HC20: 0x11514	B1_P2_ROUTE_HC21: 0x11515
B1_P2_ROUTE_HC22: 0x11516	B1_P2_ROUTE_HC23: 0x11517
B1_P2_ROUTE_HC24: 0x11518	B1_P2_ROUTE_HC25: 0x11519
B1_P2_ROUTE_HC26: 0x1151A	B1_P2_ROUTE_HC27: 0x1151B
B1_P2_ROUTE_HC28: 0x1151C	B1_P2_ROUTE_HC29: 0x1151D
B1_P2_ROUTE_HC30: 0x1151E	B1_P2_ROUTE_HC31: 0x1151F
B1_P2_ROUTE_HC32: 0x11520	B1_P2_ROUTE_HC33: 0x11521
B1_P2_ROUTE_HC34: 0x11522	B1_P2_ROUTE_HC35: 0x11523
B1_P2_ROUTE_HC36: 0x11524	B1_P2_ROUTE_HC37: 0x11525
B1_P2_ROUTE_HC38: 0x11526	B1_P2_ROUTE_HC39: 0x11527
B1_P2_ROUTE_HC40: 0x11528	B1_P2_ROUTE_HC41: 0x11529
B1_P2_ROUTE_HC42: 0x1152A	B1_P2_ROUTE_HC43: 0x1152B
B1_P2_ROUTE_HC44: 0x1152C	B1_P2_ROUTE_HC45: 0x1152D
B1_P2_ROUTE_HC46: 0x1152E	B1_P2_ROUTE_HC47: 0x1152F
B1_P2_ROUTE_HC48: 0x11530	B1_P2_ROUTE_HC49: 0x11531

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Register : Address

B1_P2_ROUTE_HC50: 0x11532
B1_P2_ROUTE_HC51: 0x11533
B1_P2_ROUTE_HC52: 0x11534
B1_P2_ROUTE_HC53: 0x11535
B1_P2_ROUTE_HC54: 0x11536
B1_P2_ROUTE_HC55: 0x11537
B1_P2_ROUTE_HC56: 0x11538
B1_P2_ROUTE_HC57: 0x11539
B1_P2_ROUTE_HC58: 0x1153A
B1_P2_ROUTE_HC59: 0x1153B
B1_P2_ROUTE_HC60: 0x1153C
B1_P2_ROUTE_HC61: 0x1153D
B1_P2_ROUTE_HC62: 0x1153E
B1_P2_ROUTE_HC63: 0x1153F
B1_P2_ROUTE_HC64: 0x11540
B1_P2_ROUTE_HC65: 0x11541
B1_P2_ROUTE_HC66: 0x11542
B1_P2_ROUTE_HC67: 0x11543
B1_P2_ROUTE_HC68: 0x11544
B1_P2_ROUTE_HC69: 0x11545
B1_P2_ROUTE_HC70: 0x11546
B1_P2_ROUTE_HC71: 0x11547
B1_P2_ROUTE_HC72: 0x11548
B1_P2_ROUTE_HC73: 0x11549
B1_P2_ROUTE_HC74: 0x1154A
B1_P2_ROUTE_HC75: 0x1154B
B1_P2_ROUTE_HC76: 0x1154C
B1_P2_ROUTE_HC77: 0x1154D
B1_P2_ROUTE_HC78: 0x1154E
B1_P2_ROUTE_HC79: 0x1154F
B1_P2_ROUTE_HC80: 0x11550
B1_P2_ROUTE_HC81: 0x11551
B1_P2_ROUTE_HC82: 0x11552
B1_P2_ROUTE_HC83: 0x11553
B1_P2_ROUTE_HC84: 0x11554
B1_P2_ROUTE_HC85: 0x11555
B1_P2_ROUTE_HC86: 0x11556
B1_P2_ROUTE_HC87: 0x11557
B1_P2_ROUTE_HC88: 0x11558
B1_P2_ROUTE_HC89: 0x11559
B1_P2_ROUTE_HC90: 0x1155A
B1_P2_ROUTE_HC91: 0x1155B
B1_P2_ROUTE_HC92: 0x1155C
B1_P2_ROUTE_HC93: 0x1155D
B1_P2_ROUTE_HC94: 0x1155E
B1_P2_ROUTE_HC95: 0x1155F
B1_P2_ROUTE_HC96: 0x11560
B1_P2_ROUTE_HC97: 0x11561
B1_P2_ROUTE_HC98: 0x11562
B1_P2_ROUTE_HC99: 0x11563
B1_P2_ROUTE_HC100: 0x11564
B1_P2_ROUTE_HC101: 0x11565
B1_P2_ROUTE_HC102: 0x11566
B1_P2_ROUTE_HC103: 0x11567
B1_P2_ROUTE_HC104: 0x11568
B1_P2_ROUTE_HC105: 0x11569
B1_P2_ROUTE_HC106: 0x1156A
B1_P2_ROUTE_HC107: 0x1156B
B1_P2_ROUTE_HC108: 0x1156C
B1_P2_ROUTE_HC109: 0x1156D
B1_P2_ROUTE_HC110: 0x1156E
B1_P2_ROUTE_HC111: 0x1156F
B1_P2_ROUTE_HC112: 0x11570
B1_P2_ROUTE_HC113: 0x11571
B1_P2_ROUTE_HC114: 0x11572
B1_P2_ROUTE_HC115: 0x11573
B1_P2_ROUTE_HC116: 0x11574
B1_P2_ROUTE_HC117: 0x11575
B1_P2_ROUTE_HC118: 0x11576
B1_P2_ROUTE_HC119: 0x11577
B1_P2_ROUTE_HC120: 0x11578
B1_P2_ROUTE_HC121: 0x11579

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Register : Address

B1_P2_ROUTE_HC122: 0x1157A
B1_P2_ROUTE_HC123: 0x1157B
B1_P2_ROUTE_HC124: 0x1157C
B1_P2_ROUTE_HC125: 0x1157D
B1_P2_ROUTE_HC126: 0x1157E
B1_P2_ROUTE_HC127: 0x1157F
B1_P3_ROUTE_HC0: 0x11700
B1_P3_ROUTE_HC1: 0x11701
B1_P3_ROUTE_HC2: 0x11702
B1_P3_ROUTE_HC3: 0x11703
B1_P3_ROUTE_HC4: 0x11704
B1_P3_ROUTE_HC5: 0x11705
B1_P3_ROUTE_HC6: 0x11706
B1_P3_ROUTE_HC7: 0x11707
B1_P3_ROUTE_HC8: 0x11708
B1_P3_ROUTE_HC9: 0x11709
B1_P3_ROUTE_HC10: 0x1170A
B1_P3_ROUTE_HC11: 0x1170B
B1_P3_ROUTE_HC12: 0x1170C
B1_P3_ROUTE_HC13: 0x1170D
B1_P3_ROUTE_HC14: 0x1170E
B1_P3_ROUTE_HC15: 0x1170F
B1_P3_ROUTE_HC16: 0x11710
B1_P3_ROUTE_HC17: 0x11711
B1_P3_ROUTE_HC18: 0x11712
B1_P3_ROUTE_HC19: 0x11713
B1_P3_ROUTE_HC20: 0x11714
B1_P3_ROUTE_HC21: 0x11715
B1_P3_ROUTE_HC22: 0x11716
B1_P3_ROUTE_HC23: 0x11717
B1_P3_ROUTE_HC24: 0x11718
B1_P3_ROUTE_HC25: 0x11719
B1_P3_ROUTE_HC26: 0x1171A
B1_P3_ROUTE_HC27: 0x1171B
B1_P3_ROUTE_HC28: 0x1171C
B1_P3_ROUTE_HC29: 0x1171D
B1_P3_ROUTE_HC30: 0x1171E
B1_P3_ROUTE_HC31: 0x1171F
B1_P3_ROUTE_HC32: 0x11720
B1_P3_ROUTE_HC33: 0x11721
B1_P3_ROUTE_HC34: 0x11722
B1_P3_ROUTE_HC35: 0x11723
B1_P3_ROUTE_HC36: 0x11724
B1_P3_ROUTE_HC37: 0x11725
B1_P3_ROUTE_HC38: 0x11726
B1_P3_ROUTE_HC39: 0x11727
B1_P3_ROUTE_HC40: 0x11728
B1_P3_ROUTE_HC41: 0x11729
B1_P3_ROUTE_HC42: 0x1172A
B1_P3_ROUTE_HC43: 0x1172B
B1_P3_ROUTE_HC44: 0x1172C
B1_P3_ROUTE_HC45: 0x1172D
B1_P3_ROUTE_HC46: 0x1172E
B1_P3_ROUTE_HC47: 0x1172F
B1_P3_ROUTE_HC48: 0x11730
B1_P3_ROUTE_HC49: 0x11731
B1_P3_ROUTE_HC50: 0x11732
B1_P3_ROUTE_HC51: 0x11733
B1_P3_ROUTE_HC52: 0x11734
B1_P3_ROUTE_HC53: 0x11735
B1_P3_ROUTE_HC54: 0x11736
B1_P3_ROUTE_HC55: 0x11737
B1_P3_ROUTE_HC56: 0x11738
B1_P3_ROUTE_HC57: 0x11739
B1_P3_ROUTE_HC58: 0x1173A
B1_P3_ROUTE_HC59: 0x1173B
B1_P3_ROUTE_HC60: 0x1173C
B1_P3_ROUTE_HC61: 0x1173D
B1_P3_ROUTE_HC62: 0x1173E
B1_P3_ROUTE_HC63: 0x1173F
B1_P3_ROUTE_HC64: 0x11740
B1_P3_ROUTE_HC65: 0x11741

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Register : Address	
B1_P3_ROUTE_HC66: 0x11742	B1_P3_ROUTE_HC67: 0x11743
B1_P3_ROUTE_HC68: 0x11744	B1_P3_ROUTE_HC69: 0x11745
B1_P3_ROUTE_HC70: 0x11746	B1_P3_ROUTE_HC71: 0x11747
B1_P3_ROUTE_HC72: 0x11748	B1_P3_ROUTE_HC73: 0x11749
B1_P3_ROUTE_HC74: 0x1174A	B1_P3_ROUTE_HC75: 0x1174B
B1_P3_ROUTE_HC76: 0x1174C	B1_P3_ROUTE_HC77: 0x1174D
B1_P3_ROUTE_HC78: 0x1174E	B1_P3_ROUTE_HC79: 0x1174F
B1_P3_ROUTE_HC80: 0x11750	B1_P3_ROUTE_HC81: 0x11751
B1_P3_ROUTE_HC82: 0x11752	B1_P3_ROUTE_HC83: 0x11753
B1_P3_ROUTE_HC84: 0x11754	B1_P3_ROUTE_HC85: 0x11755
B1_P3_ROUTE_HC86: 0x11756	B1_P3_ROUTE_HC87: 0x11757
B1_P3_ROUTE_HC88: 0x11758	B1_P3_ROUTE_HC89: 0x11759
B1_P3_ROUTE_HC90: 0x1175A	B1_P3_ROUTE_HC91: 0x1175B
B1_P3_ROUTE_HC92: 0x1175C	B1_P3_ROUTE_HC93: 0x1175D
B1_P3_ROUTE_HC94: 0x1175E	B1_P3_ROUTE_HC95: 0x1175F
B1_P3_ROUTE_HC96: 0x11760	B1_P3_ROUTE_HC97: 0x11761
B1_P3_ROUTE_HC98: 0x11762	B1_P3_ROUTE_HC99: 0x11763
B1_P3_ROUTE_HC100: 0x11764	B1_P3_ROUTE_HC101: 0x11765
B1_P3_ROUTE_HC102: 0x11766	B1_P3_ROUTE_HC103: 0x11767
B1_P3_ROUTE_HC104: 0x11768	B1_P3_ROUTE_HC105: 0x11769
B1_P3_ROUTE_HC106: 0x1176A	B1_P3_ROUTE_HC107: 0x1176B
B1_P3_ROUTE_HC108: 0x1176C	B1_P3_ROUTE_HC109: 0x1176D
B1_P3_ROUTE_HC110: 0x1176E	B1_P3_ROUTE_HC111: 0x1176F
B1_P3_ROUTE_HC112: 0x11770	B1_P3_ROUTE_HC113: 0x11771
B1_P3_ROUTE_HC114: 0x11772	B1_P3_ROUTE_HC115: 0x11773
B1_P3_ROUTE_HC116: 0x11774	B1_P3_ROUTE_HC117: 0x11775
B1_P3_ROUTE_HC118: 0x11776	B1_P3_ROUTE_HC119: 0x11777
B1_P3_ROUTE_HC120: 0x11778	B1_P3_ROUTE_HC121: 0x11779
B1_P3_ROUTE_HC122: 0x1177A	B1_P3_ROUTE_HC123: 0x1177B
B1_P3_ROUTE_HC124: 0x1177C	B1_P3_ROUTE_HC125: 0x1177D
B1_P3_ROUTE_HC126: 0x1177E	B1_P3_ROUTE_HC127: 0x1177F
B1_P4_ROUTE_HC0: 0x11900	B1_P4_ROUTE_HC1: 0x11901
B1_P4_ROUTE_HC2: 0x11902	B1_P4_ROUTE_HC3: 0x11903
B1_P4_ROUTE_HC4: 0x11904	B1_P4_ROUTE_HC5: 0x11905
B1_P4_ROUTE_HC6: 0x11906	B1_P4_ROUTE_HC7: 0x11907
B1_P4_ROUTE_HC8: 0x11908	B1_P4_ROUTE_HC9: 0x11909

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Register : Address	
B1_P4_ROUTE_HC10: 0x1190A	B1_P4_ROUTE_HC11: 0x1190B
B1_P4_ROUTE_HC12: 0x1190C	B1_P4_ROUTE_HC13: 0x1190D
B1_P4_ROUTE_HC14: 0x1190E	B1_P4_ROUTE_HC15: 0x1190F
B1_P4_ROUTE_HC16: 0x11910	B1_P4_ROUTE_HC17: 0x11911
B1_P4_ROUTE_HC18: 0x11912	B1_P4_ROUTE_HC19: 0x11913
B1_P4_ROUTE_HC20: 0x11914	B1_P4_ROUTE_HC21: 0x11915
B1_P4_ROUTE_HC22: 0x11916	B1_P4_ROUTE_HC23: 0x11917
B1_P4_ROUTE_HC24: 0x11918	B1_P4_ROUTE_HC25: 0x11919
B1_P4_ROUTE_HC26: 0x1191A	B1_P4_ROUTE_HC27: 0x1191B
B1_P4_ROUTE_HC28: 0x1191C	B1_P4_ROUTE_HC29: 0x1191D
B1_P4_ROUTE_HC30: 0x1191E	B1_P4_ROUTE_HC31: 0x1191F
B1_P4_ROUTE_HC32: 0x11920	B1_P4_ROUTE_HC33: 0x11921
B1_P4_ROUTE_HC34: 0x11922	B1_P4_ROUTE_HC35: 0x11923
B1_P4_ROUTE_HC36: 0x11924	B1_P4_ROUTE_HC37: 0x11925
B1_P4_ROUTE_HC38: 0x11926	B1_P4_ROUTE_HC39: 0x11927
B1_P4_ROUTE_HC40: 0x11928	B1_P4_ROUTE_HC41: 0x11929
B1_P4_ROUTE_HC42: 0x1192A	B1_P4_ROUTE_HC43: 0x1192B
B1_P4_ROUTE_HC44: 0x1192C	B1_P4_ROUTE_HC45: 0x1192D
B1_P4_ROUTE_HC46: 0x1192E	B1_P4_ROUTE_HC47: 0x1192F
B1_P4_ROUTE_HC48: 0x11930	B1_P4_ROUTE_HC49: 0x11931
B1_P4_ROUTE_HC50: 0x11932	B1_P4_ROUTE_HC51: 0x11933
B1_P4_ROUTE_HC52: 0x11934	B1_P4_ROUTE_HC53: 0x11935
B1_P4_ROUTE_HC54: 0x11936	B1_P4_ROUTE_HC55: 0x11937
B1_P4_ROUTE_HC56: 0x11938	B1_P4_ROUTE_HC57: 0x11939
B1_P4_ROUTE_HC58: 0x1193A	B1_P4_ROUTE_HC59: 0x1193B
B1_P4_ROUTE_HC60: 0x1193C	B1_P4_ROUTE_HC61: 0x1193D
B1_P4_ROUTE_HC62: 0x1193E	B1_P4_ROUTE_HC63: 0x1193F
B1_P4_ROUTE_HC64: 0x11940	B1_P4_ROUTE_HC65: 0x11941
B1_P4_ROUTE_HC66: 0x11942	B1_P4_ROUTE_HC67: 0x11943
B1_P4_ROUTE_HC68: 0x11944	B1_P4_ROUTE_HC69: 0x11945
B1_P4_ROUTE_HC70: 0x11946	B1_P4_ROUTE_HC71: 0x11947
B1_P4_ROUTE_HC72: 0x11948	B1_P4_ROUTE_HC73: 0x11949
B1_P4_ROUTE_HC74: 0x1194A	B1_P4_ROUTE_HC75: 0x1194B
B1_P4_ROUTE_HC76: 0x1194C	B1_P4_ROUTE_HC77: 0x1194D
B1_P4_ROUTE_HC78: 0x1194E	B1_P4_ROUTE_HC79: 0x1194F
B1_P4_ROUTE_HC80: 0x11950	B1_P4_ROUTE_HC81: 0x11951

(continued)

Register : Address	
B1_P4_ROUTE_HC82: 0x11952	B1_P4_ROUTE_HC83: 0x11953
B1_P4_ROUTE_HC84: 0x11954	B1_P4_ROUTE_HC85: 0x11955
B1_P4_ROUTE_HC86: 0x11956	B1_P4_ROUTE_HC87: 0x11957
B1_P4_ROUTE_HC88: 0x11958	B1_P4_ROUTE_HC89: 0x11959
B1_P4_ROUTE_HC90: 0x1195A	B1_P4_ROUTE_HC91: 0x1195B
B1_P4_ROUTE_HC92: 0x1195C	B1_P4_ROUTE_HC93: 0x1195D
B1_P4_ROUTE_HC94: 0x1195E	B1_P4_ROUTE_HC95: 0x1195F
B1_P4_ROUTE_HC96: 0x11960	B1_P4_ROUTE_HC97: 0x11961
B1_P4_ROUTE_HC98: 0x11962	B1_P4_ROUTE_HC99: 0x11963
B1_P4_ROUTE_HC100: 0x11964	B1_P4_ROUTE_HC101: 0x11965
B1_P4_ROUTE_HC102: 0x11966	B1_P4_ROUTE_HC103: 0x11967
B1_P4_ROUTE_HC104: 0x11968	B1_P4_ROUTE_HC105: 0x11969
B1_P4_ROUTE_HC106: 0x1196A	B1_P4_ROUTE_HC107: 0x1196B
B1_P4_ROUTE_HC108: 0x1196C	B1_P4_ROUTE_HC109: 0x1196D
B1_P4_ROUTE_HC110: 0x1196E	B1_P4_ROUTE_HC111: 0x1196F
B1_P4_ROUTE_HC112: 0x11970	B1_P4_ROUTE_HC113: 0x11971
B1_P4_ROUTE_HC114: 0x11972	B1_P4_ROUTE_HC115: 0x11973
B1_P4_ROUTE_HC116: 0x11974	B1_P4_ROUTE_HC117: 0x11975
B1_P4_ROUTE_HC118: 0x11976	B1_P4_ROUTE_HC119: 0x11977
B1_P4_ROUTE_HC120: 0x11978	B1_P4_ROUTE_HC121: 0x11979
B1_P4_ROUTE_HC122: 0x1197A	B1_P4_ROUTE_HC123: 0x1197B
B1_P4_ROUTE_HC124: 0x1197C	B1_P4_ROUTE_HC125: 0x1197D
B1_P4_ROUTE_HC126: 0x1197E	B1_P4_ROUTE_HC127: 0x1197F
B1_P5_ROUTE_HC0: 0x11B00	B1_P5_ROUTE_HC1: 0x11B01
B1_P5_ROUTE_HC2: 0x11B02	B1_P5_ROUTE_HC3: 0x11B03
B1_P5_ROUTE_HC4: 0x11B04	B1_P5_ROUTE_HC5: 0x11B05
B1_P5_ROUTE_HC6: 0x11B06	B1_P5_ROUTE_HC7: 0x11B07
B1_P5_ROUTE_HC8: 0x11B08	B1_P5_ROUTE_HC9: 0x11B09
B1_P5_ROUTE_HC10: 0x11B0A	B1_P5_ROUTE_HC11: 0x11B0B
B1_P5_ROUTE_HC12: 0x11B0C	B1_P5_ROUTE_HC13: 0x11B0D
B1_P5_ROUTE_HC14: 0x11B0E	B1_P5_ROUTE_HC15: 0x11B0F
B1_P5_ROUTE_HC16: 0x11B10	B1_P5_ROUTE_HC17: 0x11B11
B1_P5_ROUTE_HC18: 0x11B12	B1_P5_ROUTE_HC19: 0x11B13
B1_P5_ROUTE_HC20: 0x11B14	B1_P5_ROUTE_HC21: 0x11B15
B1_P5_ROUTE_HC22: 0x11B16	B1_P5_ROUTE_HC23: 0x11B17
B1_P5_ROUTE_HC24: 0x11B18	B1_P5_ROUTE_HC25: 0x11B19

(continued)

Register : Address	
B1_P5_ROUTE_HC26: 0x11B1A	B1_P5_ROUTE_HC27: 0x11B1B
B1_P5_ROUTE_HC28: 0x11B1C	B1_P5_ROUTE_HC29: 0x11B1D
B1_P5_ROUTE_HC30: 0x11B1E	B1_P5_ROUTE_HC31: 0x11B1F
B1_P5_ROUTE_HC32: 0x11B20	B1_P5_ROUTE_HC33: 0x11B21
B1_P5_ROUTE_HC34: 0x11B22	B1_P5_ROUTE_HC35: 0x11B23
B1_P5_ROUTE_HC36: 0x11B24	B1_P5_ROUTE_HC37: 0x11B25
B1_P5_ROUTE_HC38: 0x11B26	B1_P5_ROUTE_HC39: 0x11B27
B1_P5_ROUTE_HC40: 0x11B28	B1_P5_ROUTE_HC41: 0x11B29
B1_P5_ROUTE_HC42: 0x11B2A	B1_P5_ROUTE_HC43: 0x11B2B
B1_P5_ROUTE_HC44: 0x11B2C	B1_P5_ROUTE_HC45: 0x11B2D
B1_P5_ROUTE_HC46: 0x11B2E	B1_P5_ROUTE_HC47: 0x11B2F
B1_P5_ROUTE_HC48: 0x11B30	B1_P5_ROUTE_HC49: 0x11B31
B1_P5_ROUTE_HC50: 0x11B32	B1_P5_ROUTE_HC51: 0x11B33
B1_P5_ROUTE_HC52: 0x11B34	B1_P5_ROUTE_HC53: 0x11B35
B1_P5_ROUTE_HC54: 0x11B36	B1_P5_ROUTE_HC55: 0x11B37
B1_P5_ROUTE_HC56: 0x11B38	B1_P5_ROUTE_HC57: 0x11B39
B1_P5_ROUTE_HC58: 0x11B3A	B1_P5_ROUTE_HC59: 0x11B3B
B1_P5_ROUTE_HC60: 0x11B3C	B1_P5_ROUTE_HC61: 0x11B3D
B1_P5_ROUTE_HC62: 0x11B3E	B1_P5_ROUTE_HC63: 0x11B3F
B1_P5_ROUTE_HC64: 0x11B40	B1_P5_ROUTE_HC65: 0x11B41
B1_P5_ROUTE_HC66: 0x11B42	B1_P5_ROUTE_HC67: 0x11B43
B1_P5_ROUTE_HC68: 0x11B44	B1_P5_ROUTE_HC69: 0x11B45
B1_P5_ROUTE_HC70: 0x11B46	B1_P5_ROUTE_HC71: 0x11B47
B1_P5_ROUTE_HC72: 0x11B48	B1_P5_ROUTE_HC73: 0x11B49
B1_P5_ROUTE_HC74: 0x11B4A	B1_P5_ROUTE_HC75: 0x11B4B
B1_P5_ROUTE_HC76: 0x11B4C	B1_P5_ROUTE_HC77: 0x11B4D
B1_P5_ROUTE_HC78: 0x11B4E	B1_P5_ROUTE_HC79: 0x11B4F
B1_P5_ROUTE_HC80: 0x11B50	B1_P5_ROUTE_HC81: 0x11B51
B1_P5_ROUTE_HC82: 0x11B52	B1_P5_ROUTE_HC83: 0x11B53
B1_P5_ROUTE_HC84: 0x11B54	B1_P5_ROUTE_HC85: 0x11B55
B1_P5_ROUTE_HC86: 0x11B56	B1_P5_ROUTE_HC87: 0x11B57
B1_P5_ROUTE_HC88: 0x11B58	B1_P5_ROUTE_HC89: 0x11B59
B1_P5_ROUTE_HC90: 0x11B5A	B1_P5_ROUTE_HC91: 0x11B5B
B1_P5_ROUTE_HC92: 0x11B5C	B1_P5_ROUTE_HC93: 0x11B5D
B1_P5_ROUTE_HC94: 0x11B5E	B1_P5_ROUTE_HC95: 0x11B5F
B1_P5_ROUTE_HC96: 0x11B60	B1_P5_ROUTE_HC97: 0x11B61

(continued)

Register : Address

B1_P5_ROUTE_HC98: 0x11B62	B1_P5_ROUTE_HC99: 0x11B63
B1_P5_ROUTE_HC100: 0x11B64	B1_P5_ROUTE_HC101: 0x11B65
B1_P5_ROUTE_HC102: 0x11B66	B1_P5_ROUTE_HC103: 0x11B67
B1_P5_ROUTE_HC104: 0x11B68	B1_P5_ROUTE_HC105: 0x11B69
B1_P5_ROUTE_HC106: 0x11B6A	B1_P5_ROUTE_HC107: 0x11B6B
B1_P5_ROUTE_HC108: 0x11B6C	B1_P5_ROUTE_HC109: 0x11B6D
B1_P5_ROUTE_HC110: 0x11B6E	B1_P5_ROUTE_HC111: 0x11B6F
B1_P5_ROUTE_HC112: 0x11B70	B1_P5_ROUTE_HC113: 0x11B71
B1_P5_ROUTE_HC114: 0x11B72	B1_P5_ROUTE_HC115: 0x11B73
B1_P5_ROUTE_HC116: 0x11B74	B1_P5_ROUTE_HC117: 0x11B75
B1_P5_ROUTE_HC118: 0x11B76	B1_P5_ROUTE_HC119: 0x11B77
B1_P5_ROUTE_HC120: 0x11B78	B1_P5_ROUTE_HC121: 0x11B79
B1_P5_ROUTE_HC122: 0x11B7A	B1_P5_ROUTE_HC123: 0x11B7B
B1_P5_ROUTE_HC124: 0x11B7C	B1_P5_ROUTE_HC125: 0x11B7D
B1_P5_ROUTE_HC126: 0x11B7E	B1_P5_ROUTE_HC127: 0x11B7F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	RET							
Name	hc_byte							

UDB Channel HC Tile Configuration

Bits	Name	Description
7:0	hc_byte[7:0]	RAM configuration bytes for channel

1.3.1200 B[0..3]_P[0..7]_ROUTE_HV_L[0..15]

HV_L

Reset: N/A

Register : Address

B0_P0_ROUTE_HV_L0: 0x10180
B0_P0_ROUTE_HV_L1: 0x10181
B0_P0_ROUTE_HV_L2: 0x10182
B0_P0_ROUTE_HV_L3: 0x10183
B0_P0_ROUTE_HV_L4: 0x10184
B0_P0_ROUTE_HV_L5: 0x10185
B0_P0_ROUTE_HV_L6: 0x10186
B0_P0_ROUTE_HV_L7: 0x10187
B0_P0_ROUTE_HV_L8: 0x10188
B0_P0_ROUTE_HV_L9: 0x10189
B0_P0_ROUTE_HV_L10: 0x1018A
B0_P0_ROUTE_HV_L11: 0x1018B
B0_P0_ROUTE_HV_L12: 0x1018C
B0_P0_ROUTE_HV_L13: 0x1018D
B0_P0_ROUTE_HV_L14: 0x1018E
B0_P0_ROUTE_HV_L15: 0x1018F
B0_P1_ROUTE_HV_L0: 0x10380
B0_P1_ROUTE_HV_L1: 0x10381
B0_P1_ROUTE_HV_L2: 0x10382
B0_P1_ROUTE_HV_L3: 0x10383
B0_P1_ROUTE_HV_L4: 0x10384
B0_P1_ROUTE_HV_L5: 0x10385
B0_P1_ROUTE_HV_L6: 0x10386
B0_P1_ROUTE_HV_L7: 0x10387
B0_P1_ROUTE_HV_L8: 0x10388
B0_P1_ROUTE_HV_L9: 0x10389
B0_P1_ROUTE_HV_L10: 0x1038A
B0_P1_ROUTE_HV_L11: 0x1038B
B0_P1_ROUTE_HV_L12: 0x1038C
B0_P1_ROUTE_HV_L13: 0x1038D
B0_P1_ROUTE_HV_L14: 0x1038E
B0_P1_ROUTE_HV_L15: 0x1038F
B0_P2_ROUTE_HV_L0: 0x10580
B0_P2_ROUTE_HV_L1: 0x10581
B0_P2_ROUTE_HV_L2: 0x10582
B0_P2_ROUTE_HV_L3: 0x10583
B0_P2_ROUTE_HV_L4: 0x10584
B0_P2_ROUTE_HV_L5: 0x10585
B0_P2_ROUTE_HV_L6: 0x10586
B0_P2_ROUTE_HV_L7: 0x10587
B0_P2_ROUTE_HV_L8: 0x10588
B0_P2_ROUTE_HV_L9: 0x10589
B0_P2_ROUTE_HV_L10: 0x1058A
B0_P2_ROUTE_HV_L11: 0x1058B
B0_P2_ROUTE_HV_L12: 0x1058C
B0_P2_ROUTE_HV_L13: 0x1058D
B0_P2_ROUTE_HV_L14: 0x1058E
B0_P2_ROUTE_HV_L15: 0x1058F
B0_P3_ROUTE_HV_L0: 0x10780
B0_P3_ROUTE_HV_L1: 0x10781
B0_P3_ROUTE_HV_L2: 0x10782
B0_P3_ROUTE_HV_L3: 0x10783
B0_P3_ROUTE_HV_L4: 0x10784
B0_P3_ROUTE_HV_L5: 0x10785
B0_P3_ROUTE_HV_L6: 0x10786
B0_P3_ROUTE_HV_L7: 0x10787
B0_P3_ROUTE_HV_L8: 0x10788
B0_P3_ROUTE_HV_L9: 0x10789
B0_P3_ROUTE_HV_L10: 0x1078A
B0_P3_ROUTE_HV_L11: 0x1078B
B0_P3_ROUTE_HV_L12: 0x1078C
B0_P3_ROUTE_HV_L13: 0x1078D
B0_P3_ROUTE_HV_L14: 0x1078E
B0_P3_ROUTE_HV_L15: 0x1078F
B0_P4_ROUTE_HV_L0: 0x10980
B0_P4_ROUTE_HV_L1: 0x10981

(continued)

Register : Address	
B0_P4_ROUTE_HV_L2: 0x10982	B0_P4_ROUTE_HV_L3: 0x10983
B0_P4_ROUTE_HV_L4: 0x10984	B0_P4_ROUTE_HV_L5: 0x10985
B0_P4_ROUTE_HV_L6: 0x10986	B0_P4_ROUTE_HV_L7: 0x10987
B0_P4_ROUTE_HV_L8: 0x10988	B0_P4_ROUTE_HV_L9: 0x10989
B0_P4_ROUTE_HV_L10: 0x1098A	B0_P4_ROUTE_HV_L11: 0x1098B
B0_P4_ROUTE_HV_L12: 0x1098C	B0_P4_ROUTE_HV_L13: 0x1098D
B0_P4_ROUTE_HV_L14: 0x1098E	B0_P4_ROUTE_HV_L15: 0x1098F
B0_P5_ROUTE_HV_L0: 0x10B80	B0_P5_ROUTE_HV_L1: 0x10B81
B0_P5_ROUTE_HV_L2: 0x10B82	B0_P5_ROUTE_HV_L3: 0x10B83
B0_P5_ROUTE_HV_L4: 0x10B84	B0_P5_ROUTE_HV_L5: 0x10B85
B0_P5_ROUTE_HV_L6: 0x10B86	B0_P5_ROUTE_HV_L7: 0x10B87
B0_P5_ROUTE_HV_L8: 0x10B88	B0_P5_ROUTE_HV_L9: 0x10B89
B0_P5_ROUTE_HV_L10: 0x10B8A	B0_P5_ROUTE_HV_L11: 0x10B8B
B0_P5_ROUTE_HV_L12: 0x10B8C	B0_P5_ROUTE_HV_L13: 0x10B8D
B0_P5_ROUTE_HV_L14: 0x10B8E	B0_P5_ROUTE_HV_L15: 0x10B8F
B0_P6_ROUTE_HV_L0: 0x10D80	B0_P6_ROUTE_HV_L1: 0x10D81
B0_P6_ROUTE_HV_L2: 0x10D82	B0_P6_ROUTE_HV_L3: 0x10D83
B0_P6_ROUTE_HV_L4: 0x10D84	B0_P6_ROUTE_HV_L5: 0x10D85
B0_P6_ROUTE_HV_L6: 0x10D86	B0_P6_ROUTE_HV_L7: 0x10D87
B0_P6_ROUTE_HV_L8: 0x10D88	B0_P6_ROUTE_HV_L9: 0x10D89
B0_P6_ROUTE_HV_L10: 0x10D8A	B0_P6_ROUTE_HV_L11: 0x10D8B
B0_P6_ROUTE_HV_L12: 0x10D8C	B0_P6_ROUTE_HV_L13: 0x10D8D
B0_P6_ROUTE_HV_L14: 0x10D8E	B0_P6_ROUTE_HV_L15: 0x10D8F
B0_P7_ROUTE_HV_L0: 0x10F80	B0_P7_ROUTE_HV_L1: 0x10F81
B0_P7_ROUTE_HV_L2: 0x10F82	B0_P7_ROUTE_HV_L3: 0x10F83
B0_P7_ROUTE_HV_L4: 0x10F84	B0_P7_ROUTE_HV_L5: 0x10F85
B0_P7_ROUTE_HV_L6: 0x10F86	B0_P7_ROUTE_HV_L7: 0x10F87
B0_P7_ROUTE_HV_L8: 0x10F88	B0_P7_ROUTE_HV_L9: 0x10F89
B0_P7_ROUTE_HV_L10: 0x10F8A	B0_P7_ROUTE_HV_L11: 0x10F8B
B0_P7_ROUTE_HV_L12: 0x10F8C	B0_P7_ROUTE_HV_L13: 0x10F8D
B0_P7_ROUTE_HV_L14: 0x10F8E	B0_P7_ROUTE_HV_L15: 0x10F8F
B1_P2_ROUTE_HV_L0: 0x11580	B1_P2_ROUTE_HV_L1: 0x11581
B1_P2_ROUTE_HV_L2: 0x11582	B1_P2_ROUTE_HV_L3: 0x11583
B1_P2_ROUTE_HV_L4: 0x11584	B1_P2_ROUTE_HV_L5: 0x11585
B1_P2_ROUTE_HV_L6: 0x11586	B1_P2_ROUTE_HV_L7: 0x11587
B1_P2_ROUTE_HV_L8: 0x11588	B1_P2_ROUTE_HV_L9: 0x11589

(continued)

Register : Address

B1_P2_ROUTE_HV_L10: 0x1158A
B1_P2_ROUTE_HV_L11: 0x1158B
B1_P2_ROUTE_HV_L12: 0x1158C
B1_P2_ROUTE_HV_L13: 0x1158D
B1_P2_ROUTE_HV_L14: 0x1158E
B1_P2_ROUTE_HV_L15: 0x1158F
B1_P3_ROUTE_HV_L0: 0x11780
B1_P3_ROUTE_HV_L1: 0x11781
B1_P3_ROUTE_HV_L2: 0x11782
B1_P3_ROUTE_HV_L3: 0x11783
B1_P3_ROUTE_HV_L4: 0x11784
B1_P3_ROUTE_HV_L5: 0x11785
B1_P3_ROUTE_HV_L6: 0x11786
B1_P3_ROUTE_HV_L7: 0x11787
B1_P3_ROUTE_HV_L8: 0x11788
B1_P3_ROUTE_HV_L9: 0x11789
B1_P3_ROUTE_HV_L10: 0x1178A
B1_P3_ROUTE_HV_L11: 0x1178B
B1_P3_ROUTE_HV_L12: 0x1178C
B1_P3_ROUTE_HV_L13: 0x1178D
B1_P3_ROUTE_HV_L14: 0x1178E
B1_P3_ROUTE_HV_L15: 0x1178F
B1_P4_ROUTE_HV_L0: 0x11980
B1_P4_ROUTE_HV_L1: 0x11981
B1_P4_ROUTE_HV_L2: 0x11982
B1_P4_ROUTE_HV_L3: 0x11983
B1_P4_ROUTE_HV_L4: 0x11984
B1_P4_ROUTE_HV_L5: 0x11985
B1_P4_ROUTE_HV_L6: 0x11986
B1_P4_ROUTE_HV_L7: 0x11987
B1_P4_ROUTE_HV_L8: 0x11988
B1_P4_ROUTE_HV_L9: 0x11989
B1_P4_ROUTE_HV_L10: 0x1198A
B1_P4_ROUTE_HV_L11: 0x1198B
B1_P4_ROUTE_HV_L12: 0x1198C
B1_P4_ROUTE_HV_L13: 0x1198D
B1_P4_ROUTE_HV_L14: 0x1198E
B1_P4_ROUTE_HV_L15: 0x1198F
B1_P5_ROUTE_HV_L0: 0x11B80
B1_P5_ROUTE_HV_L1: 0x11B81
B1_P5_ROUTE_HV_L2: 0x11B82
B1_P5_ROUTE_HV_L3: 0x11B83
B1_P5_ROUTE_HV_L4: 0x11B84
B1_P5_ROUTE_HV_L5: 0x11B85
B1_P5_ROUTE_HV_L6: 0x11B86
B1_P5_ROUTE_HV_L7: 0x11B87
B1_P5_ROUTE_HV_L8: 0x11B88
B1_P5_ROUTE_HV_L9: 0x11B89
B1_P5_ROUTE_HV_L10: 0x11B8A
B1_P5_ROUTE_HV_L11: 0x11B8B
B1_P5_ROUTE_HV_L12: 0x11B8C
B1_P5_ROUTE_HV_L13: 0x11B8D
B1_P5_ROUTE_HV_L14: 0x11B8E
B1_P5_ROUTE_HV_L15: 0x11B8F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	RET							
Name	hv_byte							

UDB Channel HV Tile Configuration

Bits	Name	Description
7:0	hv_byte[7:0]	RAM configuration bytes for channel

1.3.1201 B[0..3]_P[0..7]_ROUTE_HS[0..23]

HS

Reset: N/A

Register : Address

B0_P0_ROUTE_HS0: 0x10190
B0_P0_ROUTE_HS1: 0x10191
B0_P0_ROUTE_HS2: 0x10192
B0_P0_ROUTE_HS3: 0x10193
B0_P0_ROUTE_HS4: 0x10194
B0_P0_ROUTE_HS5: 0x10195
B0_P0_ROUTE_HS6: 0x10196
B0_P0_ROUTE_HS7: 0x10197
B0_P0_ROUTE_HS8: 0x10198
B0_P0_ROUTE_HS9: 0x10199
B0_P0_ROUTE_HS10: 0x1019A
B0_P0_ROUTE_HS11: 0x1019B
B0_P0_ROUTE_HS12: 0x1019C
B0_P0_ROUTE_HS13: 0x1019D
B0_P0_ROUTE_HS14: 0x1019E
B0_P0_ROUTE_HS15: 0x1019F
B0_P0_ROUTE_HS16: 0x101A0
B0_P0_ROUTE_HS17: 0x101A1
B0_P0_ROUTE_HS18: 0x101A2
B0_P0_ROUTE_HS19: 0x101A3
B0_P0_ROUTE_HS20: 0x101A4
B0_P0_ROUTE_HS21: 0x101A5
B0_P0_ROUTE_HS22: 0x101A6
B0_P0_ROUTE_HS23: 0x101A7
B0_P1_ROUTE_HS0: 0x10390
B0_P1_ROUTE_HS1: 0x10391
B0_P1_ROUTE_HS2: 0x10392
B0_P1_ROUTE_HS3: 0x10393
B0_P1_ROUTE_HS4: 0x10394
B0_P1_ROUTE_HS5: 0x10395
B0_P1_ROUTE_HS6: 0x10396
B0_P1_ROUTE_HS7: 0x10397
B0_P1_ROUTE_HS8: 0x10398
B0_P1_ROUTE_HS9: 0x10399
B0_P1_ROUTE_HS10: 0x1039A
B0_P1_ROUTE_HS11: 0x1039B
B0_P1_ROUTE_HS12: 0x1039C
B0_P1_ROUTE_HS13: 0x1039D
B0_P1_ROUTE_HS14: 0x1039E
B0_P1_ROUTE_HS15: 0x1039F
B0_P1_ROUTE_HS16: 0x103A0
B0_P1_ROUTE_HS17: 0x103A1
B0_P1_ROUTE_HS18: 0x103A2
B0_P1_ROUTE_HS19: 0x103A3
B0_P1_ROUTE_HS20: 0x103A4
B0_P1_ROUTE_HS21: 0x103A5
B0_P1_ROUTE_HS22: 0x103A6
B0_P1_ROUTE_HS23: 0x103A7
B0_P2_ROUTE_HS0: 0x10590
B0_P2_ROUTE_HS1: 0x10591
B0_P2_ROUTE_HS2: 0x10592
B0_P2_ROUTE_HS3: 0x10593
B0_P2_ROUTE_HS4: 0x10594
B0_P2_ROUTE_HS5: 0x10595
B0_P2_ROUTE_HS6: 0x10596
B0_P2_ROUTE_HS7: 0x10597
B0_P2_ROUTE_HS8: 0x10598
B0_P2_ROUTE_HS9: 0x10599
B0_P2_ROUTE_HS10: 0x1059A
B0_P2_ROUTE_HS11: 0x1059B
B0_P2_ROUTE_HS12: 0x1059C
B0_P2_ROUTE_HS13: 0x1059D
B0_P2_ROUTE_HS14: 0x1059E
B0_P2_ROUTE_HS15: 0x1059F
B0_P2_ROUTE_HS16: 0x105A0
B0_P2_ROUTE_HS17: 0x105A1

(continued)

Register : Address	
B0_P2_ROUTE_HS18: 0x105A2	B0_P2_ROUTE_HS19: 0x105A3
B0_P2_ROUTE_HS20: 0x105A4	B0_P2_ROUTE_HS21: 0x105A5
B0_P2_ROUTE_HS22: 0x105A6	B0_P2_ROUTE_HS23: 0x105A7
B0_P3_ROUTE_HS0: 0x10790	B0_P3_ROUTE_HS1: 0x10791
B0_P3_ROUTE_HS2: 0x10792	B0_P3_ROUTE_HS3: 0x10793
B0_P3_ROUTE_HS4: 0x10794	B0_P3_ROUTE_HS5: 0x10795
B0_P3_ROUTE_HS6: 0x10796	B0_P3_ROUTE_HS7: 0x10797
B0_P3_ROUTE_HS8: 0x10798	B0_P3_ROUTE_HS9: 0x10799
B0_P3_ROUTE_HS10: 0x1079A	B0_P3_ROUTE_HS11: 0x1079B
B0_P3_ROUTE_HS12: 0x1079C	B0_P3_ROUTE_HS13: 0x1079D
B0_P3_ROUTE_HS14: 0x1079E	B0_P3_ROUTE_HS15: 0x1079F
B0_P3_ROUTE_HS16: 0x107A0	B0_P3_ROUTE_HS17: 0x107A1
B0_P3_ROUTE_HS18: 0x107A2	B0_P3_ROUTE_HS19: 0x107A3
B0_P3_ROUTE_HS20: 0x107A4	B0_P3_ROUTE_HS21: 0x107A5
B0_P3_ROUTE_HS22: 0x107A6	B0_P3_ROUTE_HS23: 0x107A7
B0_P4_ROUTE_HS0: 0x10990	B0_P4_ROUTE_HS1: 0x10991
B0_P4_ROUTE_HS2: 0x10992	B0_P4_ROUTE_HS3: 0x10993
B0_P4_ROUTE_HS4: 0x10994	B0_P4_ROUTE_HS5: 0x10995
B0_P4_ROUTE_HS6: 0x10996	B0_P4_ROUTE_HS7: 0x10997
B0_P4_ROUTE_HS8: 0x10998	B0_P4_ROUTE_HS9: 0x10999
B0_P4_ROUTE_HS10: 0x1099A	B0_P4_ROUTE_HS11: 0x1099B
B0_P4_ROUTE_HS12: 0x1099C	B0_P4_ROUTE_HS13: 0x1099D
B0_P4_ROUTE_HS14: 0x1099E	B0_P4_ROUTE_HS15: 0x1099F
B0_P4_ROUTE_HS16: 0x109A0	B0_P4_ROUTE_HS17: 0x109A1
B0_P4_ROUTE_HS18: 0x109A2	B0_P4_ROUTE_HS19: 0x109A3
B0_P4_ROUTE_HS20: 0x109A4	B0_P4_ROUTE_HS21: 0x109A5
B0_P4_ROUTE_HS22: 0x109A6	B0_P4_ROUTE_HS23: 0x109A7
B0_P5_ROUTE_HS0: 0x10B90	B0_P5_ROUTE_HS1: 0x10B91
B0_P5_ROUTE_HS2: 0x10B92	B0_P5_ROUTE_HS3: 0x10B93
B0_P5_ROUTE_HS4: 0x10B94	B0_P5_ROUTE_HS5: 0x10B95
B0_P5_ROUTE_HS6: 0x10B96	B0_P5_ROUTE_HS7: 0x10B97
B0_P5_ROUTE_HS8: 0x10B98	B0_P5_ROUTE_HS9: 0x10B99
B0_P5_ROUTE_HS10: 0x10B9A	B0_P5_ROUTE_HS11: 0x10B9B
B0_P5_ROUTE_HS12: 0x10B9C	B0_P5_ROUTE_HS13: 0x10B9D
B0_P5_ROUTE_HS14: 0x10B9E	B0_P5_ROUTE_HS15: 0x10B9F
B0_P5_ROUTE_HS16: 0x10BA0	B0_P5_ROUTE_HS17: 0x10BA1

(continued)

Register : Address	
B0_P5_ROUTE_HS18: 0x10BA2	B0_P5_ROUTE_HS19: 0x10BA3
B0_P5_ROUTE_HS20: 0x10BA4	B0_P5_ROUTE_HS21: 0x10BA5
B0_P5_ROUTE_HS22: 0x10BA6	B0_P5_ROUTE_HS23: 0x10BA7
B0_P6_ROUTE_HS0: 0x10D90	B0_P6_ROUTE_HS1: 0x10D91
B0_P6_ROUTE_HS2: 0x10D92	B0_P6_ROUTE_HS3: 0x10D93
B0_P6_ROUTE_HS4: 0x10D94	B0_P6_ROUTE_HS5: 0x10D95
B0_P6_ROUTE_HS6: 0x10D96	B0_P6_ROUTE_HS7: 0x10D97
B0_P6_ROUTE_HS8: 0x10D98	B0_P6_ROUTE_HS9: 0x10D99
B0_P6_ROUTE_HS10: 0x10D9A	B0_P6_ROUTE_HS11: 0x10D9B
B0_P6_ROUTE_HS12: 0x10D9C	B0_P6_ROUTE_HS13: 0x10D9D
B0_P6_ROUTE_HS14: 0x10D9E	B0_P6_ROUTE_HS15: 0x10D9F
B0_P6_ROUTE_HS16: 0x10DA0	B0_P6_ROUTE_HS17: 0x10DA1
B0_P6_ROUTE_HS18: 0x10DA2	B0_P6_ROUTE_HS19: 0x10DA3
B0_P6_ROUTE_HS20: 0x10DA4	B0_P6_ROUTE_HS21: 0x10DA5
B0_P6_ROUTE_HS22: 0x10DA6	B0_P6_ROUTE_HS23: 0x10DA7
B0_P7_ROUTE_HS0: 0x10F90	B0_P7_ROUTE_HS1: 0x10F91
B0_P7_ROUTE_HS2: 0x10F92	B0_P7_ROUTE_HS3: 0x10F93
B0_P7_ROUTE_HS4: 0x10F94	B0_P7_ROUTE_HS5: 0x10F95
B0_P7_ROUTE_HS6: 0x10F96	B0_P7_ROUTE_HS7: 0x10F97
B0_P7_ROUTE_HS8: 0x10F98	B0_P7_ROUTE_HS9: 0x10F99
B0_P7_ROUTE_HS10: 0x10F9A	B0_P7_ROUTE_HS11: 0x10F9B
B0_P7_ROUTE_HS12: 0x10F9C	B0_P7_ROUTE_HS13: 0x10F9D
B0_P7_ROUTE_HS14: 0x10F9E	B0_P7_ROUTE_HS15: 0x10F9F
B0_P7_ROUTE_HS16: 0x10FA0	B0_P7_ROUTE_HS17: 0x10FA1
B0_P7_ROUTE_HS18: 0x10FA2	B0_P7_ROUTE_HS19: 0x10FA3
B0_P7_ROUTE_HS20: 0x10FA4	B0_P7_ROUTE_HS21: 0x10FA5
B0_P7_ROUTE_HS22: 0x10FA6	B0_P7_ROUTE_HS23: 0x10FA7
B1_P2_ROUTE_HS0: 0x11590	B1_P2_ROUTE_HS1: 0x11591
B1_P2_ROUTE_HS2: 0x11592	B1_P2_ROUTE_HS3: 0x11593
B1_P2_ROUTE_HS4: 0x11594	B1_P2_ROUTE_HS5: 0x11595
B1_P2_ROUTE_HS6: 0x11596	B1_P2_ROUTE_HS7: 0x11597
B1_P2_ROUTE_HS8: 0x11598	B1_P2_ROUTE_HS9: 0x11599
B1_P2_ROUTE_HS10: 0x1159A	B1_P2_ROUTE_HS11: 0x1159B
B1_P2_ROUTE_HS12: 0x1159C	B1_P2_ROUTE_HS13: 0x1159D
B1_P2_ROUTE_HS14: 0x1159E	B1_P2_ROUTE_HS15: 0x1159F
B1_P2_ROUTE_HS16: 0x115A0	B1_P2_ROUTE_HS17: 0x115A1

(continued)

Register : Address	
B1_P2_ROUTE_HS18: 0x115A2	B1_P2_ROUTE_HS19: 0x115A3
B1_P2_ROUTE_HS20: 0x115A4	B1_P2_ROUTE_HS21: 0x115A5
B1_P2_ROUTE_HS22: 0x115A6	B1_P2_ROUTE_HS23: 0x115A7
B1_P3_ROUTE_HS0: 0x11790	B1_P3_ROUTE_HS1: 0x11791
B1_P3_ROUTE_HS2: 0x11792	B1_P3_ROUTE_HS3: 0x11793
B1_P3_ROUTE_HS4: 0x11794	B1_P3_ROUTE_HS5: 0x11795
B1_P3_ROUTE_HS6: 0x11796	B1_P3_ROUTE_HS7: 0x11797
B1_P3_ROUTE_HS8: 0x11798	B1_P3_ROUTE_HS9: 0x11799
B1_P3_ROUTE_HS10: 0x1179A	B1_P3_ROUTE_HS11: 0x1179B
B1_P3_ROUTE_HS12: 0x1179C	B1_P3_ROUTE_HS13: 0x1179D
B1_P3_ROUTE_HS14: 0x1179E	B1_P3_ROUTE_HS15: 0x1179F
B1_P3_ROUTE_HS16: 0x117A0	B1_P3_ROUTE_HS17: 0x117A1
B1_P3_ROUTE_HS18: 0x117A2	B1_P3_ROUTE_HS19: 0x117A3
B1_P3_ROUTE_HS20: 0x117A4	B1_P3_ROUTE_HS21: 0x117A5
B1_P3_ROUTE_HS22: 0x117A6	B1_P3_ROUTE_HS23: 0x117A7
B1_P4_ROUTE_HS0: 0x11990	B1_P4_ROUTE_HS1: 0x11991
B1_P4_ROUTE_HS2: 0x11992	B1_P4_ROUTE_HS3: 0x11993
B1_P4_ROUTE_HS4: 0x11994	B1_P4_ROUTE_HS5: 0x11995
B1_P4_ROUTE_HS6: 0x11996	B1_P4_ROUTE_HS7: 0x11997
B1_P4_ROUTE_HS8: 0x11998	B1_P4_ROUTE_HS9: 0x11999
B1_P4_ROUTE_HS10: 0x1199A	B1_P4_ROUTE_HS11: 0x1199B
B1_P4_ROUTE_HS12: 0x1199C	B1_P4_ROUTE_HS13: 0x1199D
B1_P4_ROUTE_HS14: 0x1199E	B1_P4_ROUTE_HS15: 0x1199F
B1_P4_ROUTE_HS16: 0x119A0	B1_P4_ROUTE_HS17: 0x119A1
B1_P4_ROUTE_HS18: 0x119A2	B1_P4_ROUTE_HS19: 0x119A3
B1_P4_ROUTE_HS20: 0x119A4	B1_P4_ROUTE_HS21: 0x119A5
B1_P4_ROUTE_HS22: 0x119A6	B1_P4_ROUTE_HS23: 0x119A7
B1_P5_ROUTE_HS0: 0x11B90	B1_P5_ROUTE_HS1: 0x11B91
B1_P5_ROUTE_HS2: 0x11B92	B1_P5_ROUTE_HS3: 0x11B93
B1_P5_ROUTE_HS4: 0x11B94	B1_P5_ROUTE_HS5: 0x11B95
B1_P5_ROUTE_HS6: 0x11B96	B1_P5_ROUTE_HS7: 0x11B97
B1_P5_ROUTE_HS8: 0x11B98	B1_P5_ROUTE_HS9: 0x11B99
B1_P5_ROUTE_HS10: 0x11B9A	B1_P5_ROUTE_HS11: 0x11B9B
B1_P5_ROUTE_HS12: 0x11B9C	B1_P5_ROUTE_HS13: 0x11B9D
B1_P5_ROUTE_HS14: 0x11B9E	B1_P5_ROUTE_HS15: 0x11B9F
B1_P5_ROUTE_HS16: 0x11BA0	B1_P5_ROUTE_HS17: 0x11BA1

(continued)

Register : Address

B1_P5_ROUTE_HS18: 0x11BA2 B1_P5_ROUTE_HS19: 0x11BA3

B1_P5_ROUTE_HS20: 0x11BA4 B1_P5_ROUTE_HS21: 0x11BA5

B1_P5_ROUTE_HS22: 0x11BA6 B1_P5_ROUTE_HS23: 0x11BA7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	RET							
Name	hs_byte							

UDB Channel HS Tile Configuration

Bits	Name	Description
7:0	hs_byte[7:0]	RAM configuration bytes for channel

1.3.1202 B[0..3]_P[0..7]_ROUTE_HV_R[0..15]

HV_R

Reset: N/A

Register : Address

B0_P0_ROUTE_HV_R0: 0x101A8
B0_P0_ROUTE_HV_R1: 0x101A9
B0_P0_ROUTE_HV_R2: 0x101AA
B0_P0_ROUTE_HV_R3: 0x101AB
B0_P0_ROUTE_HV_R4: 0x101AC
B0_P0_ROUTE_HV_R5: 0x101AD
B0_P0_ROUTE_HV_R6: 0x101AE
B0_P0_ROUTE_HV_R7: 0x101AF
B0_P0_ROUTE_HV_R8: 0x101B0
B0_P0_ROUTE_HV_R9: 0x101B1
B0_P0_ROUTE_HV_R10: 0x101B2
B0_P0_ROUTE_HV_R11: 0x101B3
B0_P0_ROUTE_HV_R12: 0x101B4
B0_P0_ROUTE_HV_R13: 0x101B5
B0_P0_ROUTE_HV_R14: 0x101B6
B0_P0_ROUTE_HV_R15: 0x101B7
B0_P1_ROUTE_HV_R0: 0x103A8
B0_P1_ROUTE_HV_R1: 0x103A9
B0_P1_ROUTE_HV_R2: 0x103AA
B0_P1_ROUTE_HV_R3: 0x103AB
B0_P1_ROUTE_HV_R4: 0x103AC
B0_P1_ROUTE_HV_R5: 0x103AD
B0_P1_ROUTE_HV_R6: 0x103AE
B0_P1_ROUTE_HV_R7: 0x103AF
B0_P1_ROUTE_HV_R8: 0x103B0
B0_P1_ROUTE_HV_R9: 0x103B1
B0_P1_ROUTE_HV_R10: 0x103B2
B0_P1_ROUTE_HV_R11: 0x103B3
B0_P1_ROUTE_HV_R12: 0x103B4
B0_P1_ROUTE_HV_R13: 0x103B5
B0_P1_ROUTE_HV_R14: 0x103B6
B0_P1_ROUTE_HV_R15: 0x103B7
B0_P2_ROUTE_HV_R0: 0x105A8
B0_P2_ROUTE_HV_R1: 0x105A9
B0_P2_ROUTE_HV_R2: 0x105AA
B0_P2_ROUTE_HV_R3: 0x105AB
B0_P2_ROUTE_HV_R4: 0x105AC
B0_P2_ROUTE_HV_R5: 0x105AD
B0_P2_ROUTE_HV_R6: 0x105AE
B0_P2_ROUTE_HV_R7: 0x105AF
B0_P2_ROUTE_HV_R8: 0x105B0
B0_P2_ROUTE_HV_R9: 0x105B1
B0_P2_ROUTE_HV_R10: 0x105B2
B0_P2_ROUTE_HV_R11: 0x105B3
B0_P2_ROUTE_HV_R12: 0x105B4
B0_P2_ROUTE_HV_R13: 0x105B5
B0_P2_ROUTE_HV_R14: 0x105B6
B0_P2_ROUTE_HV_R15: 0x105B7
B0_P3_ROUTE_HV_R0: 0x107A8
B0_P3_ROUTE_HV_R1: 0x107A9
B0_P3_ROUTE_HV_R2: 0x107AA
B0_P3_ROUTE_HV_R3: 0x107AB
B0_P3_ROUTE_HV_R4: 0x107AC
B0_P3_ROUTE_HV_R5: 0x107AD
B0_P3_ROUTE_HV_R6: 0x107AE
B0_P3_ROUTE_HV_R7: 0x107AF
B0_P3_ROUTE_HV_R8: 0x107B0
B0_P3_ROUTE_HV_R9: 0x107B1
B0_P3_ROUTE_HV_R10: 0x107B2
B0_P3_ROUTE_HV_R11: 0x107B3
B0_P3_ROUTE_HV_R12: 0x107B4
B0_P3_ROUTE_HV_R13: 0x107B5
B0_P3_ROUTE_HV_R14: 0x107B6
B0_P3_ROUTE_HV_R15: 0x107B7
B0_P4_ROUTE_HV_R0: 0x109A8
B0_P4_ROUTE_HV_R1: 0x109A9

(continued)

Register : Address	
B0_P4_ROUTE_HV_R2: 0x109AA	B0_P4_ROUTE_HV_R3: 0x109AB
B0_P4_ROUTE_HV_R4: 0x109AC	B0_P4_ROUTE_HV_R5: 0x109AD
B0_P4_ROUTE_HV_R6: 0x109AE	B0_P4_ROUTE_HV_R7: 0x109AF
B0_P4_ROUTE_HV_R8: 0x109B0	B0_P4_ROUTE_HV_R9: 0x109B1
B0_P4_ROUTE_HV_R10: 0x109B2	B0_P4_ROUTE_HV_R11: 0x109B3
B0_P4_ROUTE_HV_R12: 0x109B4	B0_P4_ROUTE_HV_R13: 0x109B5
B0_P4_ROUTE_HV_R14: 0x109B6	B0_P4_ROUTE_HV_R15: 0x109B7
B0_P5_ROUTE_HV_R0: 0x10BA8	B0_P5_ROUTE_HV_R1: 0x10BA9
B0_P5_ROUTE_HV_R2: 0x10BAA	B0_P5_ROUTE_HV_R3: 0x10BAB
B0_P5_ROUTE_HV_R4: 0x10BAC	B0_P5_ROUTE_HV_R5: 0x10BAD
B0_P5_ROUTE_HV_R6: 0x10BAE	B0_P5_ROUTE_HV_R7: 0x10BAF
B0_P5_ROUTE_HV_R8: 0x10BB0	B0_P5_ROUTE_HV_R9: 0x10BB1
B0_P5_ROUTE_HV_R10: 0x10BB2	B0_P5_ROUTE_HV_R11: 0x10BB3
B0_P5_ROUTE_HV_R12: 0x10BB4	B0_P5_ROUTE_HV_R13: 0x10BB5
B0_P5_ROUTE_HV_R14: 0x10BB6	B0_P5_ROUTE_HV_R15: 0x10BB7
B0_P6_ROUTE_HV_R0: 0x10DA8	B0_P6_ROUTE_HV_R1: 0x10DA9
B0_P6_ROUTE_HV_R2: 0x10DAA	B0_P6_ROUTE_HV_R3: 0x10DAB
B0_P6_ROUTE_HV_R4: 0x10DAC	B0_P6_ROUTE_HV_R5: 0x10DAD
B0_P6_ROUTE_HV_R6: 0x10DAE	B0_P6_ROUTE_HV_R7: 0x10DAF
B0_P6_ROUTE_HV_R8: 0x10DB0	B0_P6_ROUTE_HV_R9: 0x10DB1
B0_P6_ROUTE_HV_R10: 0x10DB2	B0_P6_ROUTE_HV_R11: 0x10DB3
B0_P6_ROUTE_HV_R12: 0x10DB4	B0_P6_ROUTE_HV_R13: 0x10DB5
B0_P6_ROUTE_HV_R14: 0x10DB6	B0_P6_ROUTE_HV_R15: 0x10DB7
B0_P7_ROUTE_HV_R0: 0x10FA8	B0_P7_ROUTE_HV_R1: 0x10FA9
B0_P7_ROUTE_HV_R2: 0x10FAA	B0_P7_ROUTE_HV_R3: 0x10FAB
B0_P7_ROUTE_HV_R4: 0x10FAC	B0_P7_ROUTE_HV_R5: 0x10FAD
B0_P7_ROUTE_HV_R6: 0x10FAE	B0_P7_ROUTE_HV_R7: 0x10FAF
B0_P7_ROUTE_HV_R8: 0x10FB0	B0_P7_ROUTE_HV_R9: 0x10FB1
B0_P7_ROUTE_HV_R10: 0x10FB2	B0_P7_ROUTE_HV_R11: 0x10FB3
B0_P7_ROUTE_HV_R12: 0x10FB4	B0_P7_ROUTE_HV_R13: 0x10FB5
B0_P7_ROUTE_HV_R14: 0x10FB6	B0_P7_ROUTE_HV_R15: 0x10FB7
B1_P2_ROUTE_HV_R0: 0x115A8	B1_P2_ROUTE_HV_R1: 0x115A9
B1_P2_ROUTE_HV_R2: 0x115AA	B1_P2_ROUTE_HV_R3: 0x115AB
B1_P2_ROUTE_HV_R4: 0x115AC	B1_P2_ROUTE_HV_R5: 0x115AD
B1_P2_ROUTE_HV_R6: 0x115AE	B1_P2_ROUTE_HV_R7: 0x115AF
B1_P2_ROUTE_HV_R8: 0x115B0	B1_P2_ROUTE_HV_R9: 0x115B1

(continued)

Register : Address

B1_P2_ROUTE_HV_R10: 0x115B2
B1_P2_ROUTE_HV_R11: 0x115B3
B1_P2_ROUTE_HV_R12: 0x115B4
B1_P2_ROUTE_HV_R13: 0x115B5
B1_P2_ROUTE_HV_R14: 0x115B6
B1_P2_ROUTE_HV_R15: 0x115B7
B1_P3_ROUTE_HV_R0: 0x117A8
B1_P3_ROUTE_HV_R1: 0x117A9
B1_P3_ROUTE_HV_R2: 0x117AA
B1_P3_ROUTE_HV_R3: 0x117AB
B1_P3_ROUTE_HV_R4: 0x117AC
B1_P3_ROUTE_HV_R5: 0x117AD
B1_P3_ROUTE_HV_R6: 0x117AE
B1_P3_ROUTE_HV_R7: 0x117AF
B1_P3_ROUTE_HV_R8: 0x117B0
B1_P3_ROUTE_HV_R9: 0x117B1
B1_P3_ROUTE_HV_R10: 0x117B2
B1_P3_ROUTE_HV_R11: 0x117B3
B1_P3_ROUTE_HV_R12: 0x117B4
B1_P3_ROUTE_HV_R13: 0x117B5
B1_P3_ROUTE_HV_R14: 0x117B6
B1_P3_ROUTE_HV_R15: 0x117B7
B1_P4_ROUTE_HV_R0: 0x119A8
B1_P4_ROUTE_HV_R1: 0x119A9
B1_P4_ROUTE_HV_R2: 0x119AA
B1_P4_ROUTE_HV_R3: 0x119AB
B1_P4_ROUTE_HV_R4: 0x119AC
B1_P4_ROUTE_HV_R5: 0x119AD
B1_P4_ROUTE_HV_R6: 0x119AE
B1_P4_ROUTE_HV_R7: 0x119AF
B1_P4_ROUTE_HV_R8: 0x119B0
B1_P4_ROUTE_HV_R9: 0x119B1
B1_P4_ROUTE_HV_R10: 0x119B2
B1_P4_ROUTE_HV_R11: 0x119B3
B1_P4_ROUTE_HV_R12: 0x119B4
B1_P4_ROUTE_HV_R13: 0x119B5
B1_P4_ROUTE_HV_R14: 0x119B6
B1_P4_ROUTE_HV_R15: 0x119B7
B1_P5_ROUTE_HV_R0: 0x11BA8
B1_P5_ROUTE_HV_R1: 0x11BA9
B1_P5_ROUTE_HV_R2: 0x11BAA
B1_P5_ROUTE_HV_R3: 0x11BAB
B1_P5_ROUTE_HV_R4: 0x11BAC
B1_P5_ROUTE_HV_R5: 0x11BAD
B1_P5_ROUTE_HV_R6: 0x11BAE
B1_P5_ROUTE_HV_R7: 0x11BAF
B1_P5_ROUTE_HV_R8: 0x11BB0
B1_P5_ROUTE_HV_R9: 0x11BB1
B1_P5_ROUTE_HV_R10: 0x11BB2
B1_P5_ROUTE_HV_R11: 0x11BB3
B1_P5_ROUTE_HV_R12: 0x11BB4
B1_P5_ROUTE_HV_R13: 0x11BB5
B1_P5_ROUTE_HV_R14: 0x11BB6
B1_P5_ROUTE_HV_R15: 0x11BB7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	RET							
Name	hv_byte							

UDB Channel HV Tile Configuration

Bits	Name	Description
7:0	hv_byte[7:0]	RAM configuration bytes for channel

1.3.1203 B[0..3]_P[0..7]_ROUTE_PLD0IN0

PLD0IN0

Reset: N/A

Register : Address

B0_P0_ROUTE_PLD0IN0: 0x101C0

B0_P1_ROUTE_PLD0IN0: 0x103C0

B0_P2_ROUTE_PLD0IN0: 0x105C0

B0_P3_ROUTE_PLD0IN0: 0x107C0

B0_P4_ROUTE_PLD0IN0: 0x109C0

B0_P5_ROUTE_PLD0IN0: 0x10BC0

B0_P6_ROUTE_PLD0IN0: 0x10DC0

B0_P7_ROUTE_PLD0IN0: 0x10FC0

B1_P2_ROUTE_PLD0IN0: 0x115C0

B1_P3_ROUTE_PLD0IN0: 0x117C0

B1_P4_ROUTE_PLD0IN0: 0x119C0

B1_P5_ROUTE_PLD0IN0: 0x11BC0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	pi_bot				pi_top			

UDB Channel PI Tile Configuration

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration nibble for BOTTOM UDB port interface configuration
3:0	pi_top[3:0]	RAM configuration nibble for TOP UDB port interface configuration

1.3.1204 B[0..3]_P[0..7]_ROUTE_PLD0IN1

PLD0IN1

Reset: N/A

Register : Address

B0_P0_ROUTE_PLD0IN1: 0x101C2

B0_P1_ROUTE_PLD0IN1: 0x103C2

B0_P2_ROUTE_PLD0IN1: 0x105C2

B0_P3_ROUTE_PLD0IN1: 0x107C2

B0_P4_ROUTE_PLD0IN1: 0x109C2

B0_P5_ROUTE_PLD0IN1: 0x10BC2

B0_P6_ROUTE_PLD0IN1: 0x10DC2

B0_P7_ROUTE_PLD0IN1: 0x10FC2

B1_P2_ROUTE_PLD0IN1: 0x115C2

B1_P3_ROUTE_PLD0IN1: 0x117C2

B1_P4_ROUTE_PLD0IN1: 0x119C2

B1_P5_ROUTE_PLD0IN1: 0x11BC2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	pi_bot				pi_top			

UDB Channel PI Tile Configuration

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration nibble for BOTTOM UDB port interface configuration
3:0	pi_top[3:0]	RAM configuration nibble for TOP UDB port interface configuration

1.3.1205 B[0..3]_P[0..7]_ROUTE_PLD0IN2

PLD0IN2

Reset: N/A

Register : Address

B0_P0_ROUTE_PLD0IN2: 0x101C4

B0_P1_ROUTE_PLD0IN2: 0x103C4

B0_P2_ROUTE_PLD0IN2: 0x105C4

B0_P3_ROUTE_PLD0IN2: 0x107C4

B0_P4_ROUTE_PLD0IN2: 0x109C4

B0_P5_ROUTE_PLD0IN2: 0x10BC4

B0_P6_ROUTE_PLD0IN2: 0x10DC4

B0_P7_ROUTE_PLD0IN2: 0x10FC4

B1_P2_ROUTE_PLD0IN2: 0x115C4

B1_P3_ROUTE_PLD0IN2: 0x117C4

B1_P4_ROUTE_PLD0IN2: 0x119C4

B1_P5_ROUTE_PLD0IN2: 0x11BC4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	pi_bot				pi_top			

UDB Channel PI Tile Configuration

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration nibble for BOTTOM UDB port interface configuration
3:0	pi_top[3:0]	RAM configuration nibble for TOP UDB port interface configuration

1.3.1206 B[0..3]_P[0..7]_ROUTE_PLD1IN0

PLD1IN0

Reset: N/A

Register : Address

B0_P0_ROUTE_PLD1IN0: 0x101CA

B0_P1_ROUTE_PLD1IN0: 0x103CA

B0_P2_ROUTE_PLD1IN0: 0x105CA

B0_P3_ROUTE_PLD1IN0: 0x107CA

B0_P4_ROUTE_PLD1IN0: 0x109CA

B0_P5_ROUTE_PLD1IN0: 0x10BCA

B0_P6_ROUTE_PLD1IN0: 0x10DCA

B0_P7_ROUTE_PLD1IN0: 0x10FCA

B1_P2_ROUTE_PLD1IN0: 0x115CA

B1_P3_ROUTE_PLD1IN0: 0x117CA

B1_P4_ROUTE_PLD1IN0: 0x119CA

B1_P5_ROUTE_PLD1IN0: 0x11BCA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	pi_bot				pi_top			

UDB Channel PI Tile Configuration

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration nibble for BOTTOM UDB port interface configuration
3:0	pi_top[3:0]	RAM configuration nibble for TOP UDB port interface configuration

1.3.1207 B[0..3]_P[0..7]_ROUTE_PLD1IN1

PLD1IN1

Reset: N/A

Register : Address

B0_P0_ROUTE_PLD1IN1: 0x101CC

B0_P1_ROUTE_PLD1IN1: 0x103CC

B0_P2_ROUTE_PLD1IN1: 0x105CC

B0_P3_ROUTE_PLD1IN1: 0x107CC

B0_P4_ROUTE_PLD1IN1: 0x109CC

B0_P5_ROUTE_PLD1IN1: 0x10BCC

B0_P6_ROUTE_PLD1IN1: 0x10DCC

B0_P7_ROUTE_PLD1IN1: 0x10FCC

B1_P2_ROUTE_PLD1IN1: 0x115CC

B1_P3_ROUTE_PLD1IN1: 0x117CC

B1_P4_ROUTE_PLD1IN1: 0x119CC

B1_P5_ROUTE_PLD1IN1: 0x11BCC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	pi_bot				pi_top			

UDB Channel PI Tile Configuration

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration nibble for BOTTOM UDB port interface configuration
3:0	pi_top[3:0]	RAM configuration nibble for TOP UDB port interface configuration

1.3.1208 B[0..3]_P[0..7]_ROUTE_PLD1IN2

PLD1IN2

Reset: N/A

Register : Address

B0_P0_ROUTE_PLD1IN2: 0x101CE

B0_P1_ROUTE_PLD1IN2: 0x103CE

B0_P2_ROUTE_PLD1IN2: 0x105CE

B0_P3_ROUTE_PLD1IN2: 0x107CE

B0_P4_ROUTE_PLD1IN2: 0x109CE

B0_P5_ROUTE_PLD1IN2: 0x10BCE

B0_P6_ROUTE_PLD1IN2: 0x10DCE

B0_P7_ROUTE_PLD1IN2: 0x10FCE

B1_P2_ROUTE_PLD1IN2: 0x115CE

B1_P3_ROUTE_PLD1IN2: 0x117CE

B1_P4_ROUTE_PLD1IN2: 0x119CE

B1_P5_ROUTE_PLD1IN2: 0x11BCE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	pi_bot				pi_top			

UDB Channel PI Tile Configuration

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration nibble for BOTTOM UDB port interface configuration
3:0	pi_top[3:0]	RAM configuration nibble for TOP UDB port interface configuration

1.3.1209 B[0..3]_P[0..7]_ROUTE_DPIN0

DPIN0

Reset: N/A

Register : Address

B0_P0_ROUTE_DPIN0: 0x101D0
B0_P1_ROUTE_DPIN0: 0x103D0
B0_P2_ROUTE_DPIN0: 0x105D0
B0_P3_ROUTE_DPIN0: 0x107D0
B0_P4_ROUTE_DPIN0: 0x109D0
B0_P5_ROUTE_DPIN0: 0x10BD0
B0_P6_ROUTE_DPIN0: 0x10DD0
B0_P7_ROUTE_DPIN0: 0x10FD0
B1_P2_ROUTE_DPIN0: 0x115D0
B1_P3_ROUTE_DPIN0: 0x117D0
B1_P4_ROUTE_DPIN0: 0x119D0
B1_P5_ROUTE_DPIN0: 0x11BD0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	pi_bot				pi_top			

UDB Channel PI Tile Configuration

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration nibble for BOTTOM UDB port interface configuration
3:0	pi_top[3:0]	RAM configuration nibble for TOP UDB port interface configuration

1.3.1210 B[0..3]_P[0..7]_ROUTE_DPIN1

DPIN1

Reset: N/A

Register : Address

B0_P0_ROUTE_DPIN1: 0x101D2
B0_P1_ROUTE_DPIN1: 0x103D2
B0_P2_ROUTE_DPIN1: 0x105D2
B0_P3_ROUTE_DPIN1: 0x107D2
B0_P4_ROUTE_DPIN1: 0x109D2
B0_P5_ROUTE_DPIN1: 0x10BD2
B0_P6_ROUTE_DPIN1: 0x10DD2
B0_P7_ROUTE_DPIN1: 0x10FD2
B1_P2_ROUTE_DPIN1: 0x115D2
B1_P3_ROUTE_DPIN1: 0x117D2
B1_P4_ROUTE_DPIN1: 0x119D2
B1_P5_ROUTE_DPIN1: 0x11BD2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:00		R/W:UU		R/W:UU		NA:00	
HW Access	NA		R		R		NA	
Retention	NA		RET		RET		NA	
Name	RSVD		pi_bot		pi_top		RSVD	

UDB Channel PI Tile Configuration (half populated)

Bits	Name	Description
5:4	pi_bot[1:0]	RAM configuration bits (2) for BOTTOM UDB port interface configuration
3:2	pi_top[1:0]	RAM configuration bits (2) for TOP UDB port interface configuration

1.3.1211 B[0..3]_P[0..7]_ROUTE_SCIN

SCIN

Reset: N/A

Register : Address

B0_P0_ROUTE_SCIN: 0x101D6
B0_P1_ROUTE_SCIN: 0x103D6
B0_P2_ROUTE_SCIN: 0x105D6
B0_P3_ROUTE_SCIN: 0x107D6
B0_P4_ROUTE_SCIN: 0x109D6
B0_P5_ROUTE_SCIN: 0x10BD6
B0_P6_ROUTE_SCIN: 0x10DD6
B0_P7_ROUTE_SCIN: 0x10FD6
B1_P2_ROUTE_SCIN: 0x115D6
B1_P3_ROUTE_SCIN: 0x117D6
B1_P4_ROUTE_SCIN: 0x119D6
B1_P5_ROUTE_SCIN: 0x11BD6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	pi_bot				pi_top			

UDB Channel PI Tile Configuration

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration nibble for BOTTOM UDB port interface configuration
3:0	pi_top[3:0]	RAM configuration nibble for TOP UDB port interface configuration

1.3.1212 B[0..3]_P[0..7]_ROUTE_SCIOIN

SCIOIN

Reset: N/A

Register : Address

B0_P0_ROUTE_SCIOIN: 0x101D8
B0_P1_ROUTE_SCIOIN: 0x103D8
B0_P2_ROUTE_SCIOIN: 0x105D8
B0_P3_ROUTE_SCIOIN: 0x107D8
B0_P4_ROUTE_SCIOIN: 0x109D8
B0_P5_ROUTE_SCIOIN: 0x10BD8
B0_P6_ROUTE_SCIOIN: 0x10DD8
B0_P7_ROUTE_SCIOIN: 0x10FD8
B1_P2_ROUTE_SCIOIN: 0x115D8
B1_P3_ROUTE_SCIOIN: 0x117D8
B1_P4_ROUTE_SCIOIN: 0x119D8
B1_P5_ROUTE_SCIOIN: 0x11BD8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	pi_bot				pi_top			

UDB Channel PI Tile Configuration

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration nibble for BOTTOM UDB port interface configuration
3:0	pi_top[3:0]	RAM configuration nibble for TOP UDB port interface configuration

1.3.1213 B[0..3]_P[0..7]_ROUTE_RCIN

RCIN

Reset: N/A

Register : Address

B0_P0_ROUTE_RCIN: 0x101DE
B0_P1_ROUTE_RCIN: 0x103DE
B0_P2_ROUTE_RCIN: 0x105DE
B0_P3_ROUTE_RCIN: 0x107DE
B0_P4_ROUTE_RCIN: 0x109DE
B0_P5_ROUTE_RCIN: 0x10BDE
B0_P6_ROUTE_RCIN: 0x10DDE
B0_P7_ROUTE_RCIN: 0x10FDE
B1_P2_ROUTE_RCIN: 0x115DE
B1_P3_ROUTE_RCIN: 0x117DE
B1_P4_ROUTE_RCIN: 0x119DE
B1_P5_ROUTE_RCIN: 0x11BDE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	pi_bot				pi_top			

UDB Channel PI Tile Configuration

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration nibble for BOTTOM UDB port interface configuration
3:0	pi_top[3:0]	RAM configuration nibble for TOP UDB port interface configuration

1.3.1214 B[0..3]_P[0..7]_ROUTE_VS0

VS0

Reset: N/A

Register : Address

B0_P0_ROUTE_VS0: 0x101E0
B0_P1_ROUTE_VS0: 0x103E0
B0_P2_ROUTE_VS0: 0x105E0
B0_P3_ROUTE_VS0: 0x107E0
B0_P4_ROUTE_VS0: 0x109E0
B0_P5_ROUTE_VS0: 0x10BE0
B0_P6_ROUTE_VS0: 0x10DE0
B0_P7_ROUTE_VS0: 0x10FE0
B1_P2_ROUTE_VS0: 0x115E0
B1_P3_ROUTE_VS0: 0x117E0
B1_P4_ROUTE_VS0: 0x119E0
B1_P5_ROUTE_VS0: 0x11BE0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	vs_bot				vs_top			

UDB Channel VS Tile Configuration

Bits	Name	Description
7:4	vs_bot[3:0]	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration
3:0	vs_top[3:0]	RAM configuration nibble for TOP UDB vertical segmentation configuration

1.3.1215 B[0..3]_P[0..7]_ROUTE_VS1

VS1

Reset: N/A

Register : Address

B0_P0_ROUTE_VS1: 0x101E2
B0_P1_ROUTE_VS1: 0x103E2
B0_P2_ROUTE_VS1: 0x105E2
B0_P3_ROUTE_VS1: 0x107E2
B0_P4_ROUTE_VS1: 0x109E2
B0_P5_ROUTE_VS1: 0x10BE2
B0_P6_ROUTE_VS1: 0x10DE2
B0_P7_ROUTE_VS1: 0x10FE2
B1_P2_ROUTE_VS1: 0x115E2
B1_P3_ROUTE_VS1: 0x117E2
B1_P4_ROUTE_VS1: 0x119E2
B1_P5_ROUTE_VS1: 0x11BE2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	vs_bot				vs_top			

UDB Channel VS Tile Configuration

Bits	Name	Description
7:4	vs_bot[3:0]	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration
3:0	vs_top[3:0]	RAM configuration nibble for TOP UDB vertical segmentation configuration

1.3.1216 B[0..3]_P[0..7]_ROUTE_VS2

VS2

Reset: N/A

Register : Address

B0_P0_ROUTE_VS2: 0x101E4
B0_P1_ROUTE_VS2: 0x103E4
B0_P2_ROUTE_VS2: 0x105E4
B0_P3_ROUTE_VS2: 0x107E4
B0_P4_ROUTE_VS2: 0x109E4
B0_P5_ROUTE_VS2: 0x10BE4
B0_P6_ROUTE_VS2: 0x10DE4
B0_P7_ROUTE_VS2: 0x10FE4
B1_P2_ROUTE_VS2: 0x115E4
B1_P3_ROUTE_VS2: 0x117E4
B1_P4_ROUTE_VS2: 0x119E4
B1_P5_ROUTE_VS2: 0x11BE4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	vs_bot				vs_top			

UDB Channel VS Tile Configuration

Bits	Name	Description
7:4	vs_bot[3:0]	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration
3:0	vs_top[3:0]	RAM configuration nibble for TOP UDB vertical segmentation configuration

1.3.1217 B[0..3]_P[0..7]_ROUTE_VS3

VS3

Reset: N/A

Register : Address

B0_P0_ROUTE_VS3: 0x101E6
B0_P1_ROUTE_VS3: 0x103E6
B0_P2_ROUTE_VS3: 0x105E6
B0_P3_ROUTE_VS3: 0x107E6
B0_P4_ROUTE_VS3: 0x109E6
B0_P5_ROUTE_VS3: 0x10BE6
B0_P6_ROUTE_VS3: 0x10DE6
B0_P7_ROUTE_VS3: 0x10FE6
B1_P2_ROUTE_VS3: 0x115E6
B1_P3_ROUTE_VS3: 0x117E6
B1_P4_ROUTE_VS3: 0x119E6
B1_P5_ROUTE_VS3: 0x11BE6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	vs_bot				vs_top			

UDB Channel VS Tile Configuration

Bits	Name	Description
7:4	vs_bot[3:0]	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration
3:0	vs_top[3:0]	RAM configuration nibble for TOP UDB vertical segmentation configuration

1.3.1218 B[0..3]_P[0..7]_ROUTE_VS4

VS4

Reset: N/A

Register : Address

B0_P0_ROUTE_VS4: 0x101E8
B0_P1_ROUTE_VS4: 0x103E8
B0_P2_ROUTE_VS4: 0x105E8
B0_P3_ROUTE_VS4: 0x107E8
B0_P4_ROUTE_VS4: 0x109E8
B0_P5_ROUTE_VS4: 0x10BE8
B0_P6_ROUTE_VS4: 0x10DE8
B0_P7_ROUTE_VS4: 0x10FE8
B1_P2_ROUTE_VS4: 0x115E8
B1_P3_ROUTE_VS4: 0x117E8
B1_P4_ROUTE_VS4: 0x119E8
B1_P5_ROUTE_VS4: 0x11BE8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	vs_bot				vs_top			

UDB Channel VS Tile Configuration

Bits	Name	Description
7:4	vs_bot[3:0]	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration
3:0	vs_top[3:0]	RAM configuration nibble for TOP UDB vertical segmentation configuration

1.3.1219 B[0..3]_P[0..7]_ROUTE_VS5

VS5

Reset: N/A

Register : Address

B0_P0_ROUTE_VS5: 0x101EA
B0_P1_ROUTE_VS5: 0x103EA
B0_P2_ROUTE_VS5: 0x105EA
B0_P3_ROUTE_VS5: 0x107EA
B0_P4_ROUTE_VS5: 0x109EA
B0_P5_ROUTE_VS5: 0x10BEA
B0_P6_ROUTE_VS5: 0x10DEA
B0_P7_ROUTE_VS5: 0x10FEA
B1_P2_ROUTE_VS5: 0x115EA
B1_P3_ROUTE_VS5: 0x117EA
B1_P4_ROUTE_VS5: 0x119EA
B1_P5_ROUTE_VS5: 0x11BEA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	vs_bot				vs_top			

UDB Channel VS Tile Configuration

Bits	Name	Description
7:4	vs_bot[3:0]	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration
3:0	vs_top[3:0]	RAM configuration nibble for TOP UDB vertical segmentation configuration

1.3.1220 B[0..3]_P[0..7]_ROUTE_VS6

VS6

Reset: N/A

Register : Address

B0_P0_ROUTE_VS6: 0x101EC
B0_P1_ROUTE_VS6: 0x103EC
B0_P2_ROUTE_VS6: 0x105EC
B0_P3_ROUTE_VS6: 0x107EC
B0_P4_ROUTE_VS6: 0x109EC
B0_P5_ROUTE_VS6: 0x10BEC
B0_P6_ROUTE_VS6: 0x10DEC
B0_P7_ROUTE_VS6: 0x10FEC
B1_P2_ROUTE_VS6: 0x115EC
B1_P3_ROUTE_VS6: 0x117EC
B1_P4_ROUTE_VS6: 0x119EC
B1_P5_ROUTE_VS6: 0x11BEC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	vs_bot				vs_top			

UDB Channel VS Tile Configuration

Bits	Name	Description
7:4	vs_bot[3:0]	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration
3:0	vs_top[3:0]	RAM configuration nibble for TOP UDB vertical segmentation configuration

1.3.1221 B[0..3]_P[0..7]_ROUTE_VS7

VS7

Reset: N/A

Register : Address

B0_P0_ROUTE_VS7: 0x101EE
B0_P1_ROUTE_VS7: 0x103EE
B0_P2_ROUTE_VS7: 0x105EE
B0_P3_ROUTE_VS7: 0x107EE
B0_P4_ROUTE_VS7: 0x109EE
B0_P5_ROUTE_VS7: 0x10BEE
B0_P6_ROUTE_VS7: 0x10DEE
B0_P7_ROUTE_VS7: 0x10FEE
B1_P2_ROUTE_VS7: 0x115EE
B1_P3_ROUTE_VS7: 0x117EE
B1_P4_ROUTE_VS7: 0x119EE
B1_P5_ROUTE_VS7: 0x11BEE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	vs_bot				vs_top			

UDB Channel VS Tile Configuration

Bits	Name	Description
7:4	vs_bot[3:0]	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration
3:0	vs_top[3:0]	RAM configuration nibble for TOP UDB vertical segmentation configuration

1.3.1222 DSI[0..15]_HC[0..127]

HC

Reset: N/A

Register : Address

DSI0_HC0: 0x14000	DSI0_HC1: 0x14001	DSI0_HC2: 0x14002
DSI0_HC3: 0x14003	DSI0_HC4: 0x14004	DSI0_HC5: 0x14005
DSI0_HC6: 0x14006	DSI0_HC7: 0x14007	DSI0_HC8: 0x14008
DSI0_HC9: 0x14009	DSI0_HC10: 0x1400A	DSI0_HC11: 0x1400B
DSI0_HC12: 0x1400C	DSI0_HC13: 0x1400D	DSI0_HC14: 0x1400E
DSI0_HC15: 0x1400F	DSI0_HC16: 0x14010	DSI0_HC17: 0x14011
DSI0_HC18: 0x14012	DSI0_HC19: 0x14013	DSI0_HC20: 0x14014
DSI0_HC21: 0x14015	DSI0_HC22: 0x14016	DSI0_HC23: 0x14017
DSI0_HC24: 0x14018	DSI0_HC25: 0x14019	DSI0_HC26: 0x1401A
DSI0_HC27: 0x1401B	DSI0_HC28: 0x1401C	DSI0_HC29: 0x1401D
DSI0_HC30: 0x1401E	DSI0_HC31: 0x1401F	DSI0_HC32: 0x14020
DSI0_HC33: 0x14021	DSI0_HC34: 0x14022	DSI0_HC35: 0x14023
DSI0_HC36: 0x14024	DSI0_HC37: 0x14025	DSI0_HC38: 0x14026
DSI0_HC39: 0x14027	DSI0_HC40: 0x14028	DSI0_HC41: 0x14029
DSI0_HC42: 0x1402A	DSI0_HC43: 0x1402B	DSI0_HC44: 0x1402C
DSI0_HC45: 0x1402D	DSI0_HC46: 0x1402E	DSI0_HC47: 0x1402F
DSI0_HC48: 0x14030	DSI0_HC49: 0x14031	DSI0_HC50: 0x14032
DSI0_HC51: 0x14033	DSI0_HC52: 0x14034	DSI0_HC53: 0x14035
DSI0_HC54: 0x14036	DSI0_HC55: 0x14037	DSI0_HC56: 0x14038
DSI0_HC57: 0x14039	DSI0_HC58: 0x1403A	DSI0_HC59: 0x1403B
DSI0_HC60: 0x1403C	DSI0_HC61: 0x1403D	DSI0_HC62: 0x1403E
DSI0_HC63: 0x1403F	DSI0_HC64: 0x14040	DSI0_HC65: 0x14041
DSI0_HC66: 0x14042	DSI0_HC67: 0x14043	DSI0_HC68: 0x14044
DSI0_HC69: 0x14045	DSI0_HC70: 0x14046	DSI0_HC71: 0x14047
DSI0_HC72: 0x14048	DSI0_HC73: 0x14049	DSI0_HC74: 0x1404A
DSI0_HC75: 0x1404B	DSI0_HC76: 0x1404C	DSI0_HC77: 0x1404D
DSI0_HC78: 0x1404E	DSI0_HC79: 0x1404F	DSI0_HC80: 0x14050
DSI0_HC81: 0x14051	DSI0_HC82: 0x14052	DSI0_HC83: 0x14053
DSI0_HC84: 0x14054	DSI0_HC85: 0x14055	DSI0_HC86: 0x14056
DSI0_HC87: 0x14057	DSI0_HC88: 0x14058	DSI0_HC89: 0x14059
DSI0_HC90: 0x1405A	DSI0_HC91: 0x1405B	DSI0_HC92: 0x1405C
DSI0_HC93: 0x1405D	DSI0_HC94: 0x1405E	DSI0_HC95: 0x1405F
DSI0_HC96: 0x14060	DSI0_HC97: 0x14061	DSI0_HC98: 0x14062

(continued)

Register : Address		
DSI0_HC99: 0x14063	DSI0_HC100: 0x14064	DSI0_HC101: 0x14065
DSI0_HC102: 0x14066	DSI0_HC103: 0x14067	DSI0_HC104: 0x14068
DSI0_HC105: 0x14069	DSI0_HC106: 0x1406A	DSI0_HC107: 0x1406B
DSI0_HC108: 0x1406C	DSI0_HC109: 0x1406D	DSI0_HC110: 0x1406E
DSI0_HC111: 0x1406F	DSI0_HC112: 0x14070	DSI0_HC113: 0x14071
DSI0_HC114: 0x14072	DSI0_HC115: 0x14073	DSI0_HC116: 0x14074
DSI0_HC117: 0x14075	DSI0_HC118: 0x14076	DSI0_HC119: 0x14077
DSI0_HC120: 0x14078	DSI0_HC121: 0x14079	DSI0_HC122: 0x1407A
DSI0_HC123: 0x1407B	DSI0_HC124: 0x1407C	DSI0_HC125: 0x1407D
DSI0_HC126: 0x1407E	DSI0_HC127: 0x1407F	DSI1_HC0: 0x14100
DSI1_HC1: 0x14101	DSI1_HC2: 0x14102	DSI1_HC3: 0x14103
DSI1_HC4: 0x14104	DSI1_HC5: 0x14105	DSI1_HC6: 0x14106
DSI1_HC7: 0x14107	DSI1_HC8: 0x14108	DSI1_HC9: 0x14109
DSI1_HC10: 0x1410A	DSI1_HC11: 0x1410B	DSI1_HC12: 0x1410C
DSI1_HC13: 0x1410D	DSI1_HC14: 0x1410E	DSI1_HC15: 0x1410F
DSI1_HC16: 0x14110	DSI1_HC17: 0x14111	DSI1_HC18: 0x14112
DSI1_HC19: 0x14113	DSI1_HC20: 0x14114	DSI1_HC21: 0x14115
DSI1_HC22: 0x14116	DSI1_HC23: 0x14117	DSI1_HC24: 0x14118
DSI1_HC25: 0x14119	DSI1_HC26: 0x1411A	DSI1_HC27: 0x1411B
DSI1_HC28: 0x1411C	DSI1_HC29: 0x1411D	DSI1_HC30: 0x1411E
DSI1_HC31: 0x1411F	DSI1_HC32: 0x14120	DSI1_HC33: 0x14121
DSI1_HC34: 0x14122	DSI1_HC35: 0x14123	DSI1_HC36: 0x14124
DSI1_HC37: 0x14125	DSI1_HC38: 0x14126	DSI1_HC39: 0x14127
DSI1_HC40: 0x14128	DSI1_HC41: 0x14129	DSI1_HC42: 0x1412A
DSI1_HC43: 0x1412B	DSI1_HC44: 0x1412C	DSI1_HC45: 0x1412D
DSI1_HC46: 0x1412E	DSI1_HC47: 0x1412F	DSI1_HC48: 0x14130
DSI1_HC49: 0x14131	DSI1_HC50: 0x14132	DSI1_HC51: 0x14133
DSI1_HC52: 0x14134	DSI1_HC53: 0x14135	DSI1_HC54: 0x14136
DSI1_HC55: 0x14137	DSI1_HC56: 0x14138	DSI1_HC57: 0x14139
DSI1_HC58: 0x1413A	DSI1_HC59: 0x1413B	DSI1_HC60: 0x1413C
DSI1_HC61: 0x1413D	DSI1_HC62: 0x1413E	DSI1_HC63: 0x1413F
DSI1_HC64: 0x14140	DSI1_HC65: 0x14141	DSI1_HC66: 0x14142
DSI1_HC67: 0x14143	DSI1_HC68: 0x14144	DSI1_HC69: 0x14145
DSI1_HC70: 0x14146	DSI1_HC71: 0x14147	DSI1_HC72: 0x14148
DSI1_HC73: 0x14149	DSI1_HC74: 0x1414A	DSI1_HC75: 0x1414B
DSI1_HC76: 0x1414C	DSI1_HC77: 0x1414D	DSI1_HC78: 0x1414E

(continued)

Register : Address		
DSI1_HC79: 0x1414F	DSI1_HC80: 0x14150	DSI1_HC81: 0x14151
DSI1_HC82: 0x14152	DSI1_HC83: 0x14153	DSI1_HC84: 0x14154
DSI1_HC85: 0x14155	DSI1_HC86: 0x14156	DSI1_HC87: 0x14157
DSI1_HC88: 0x14158	DSI1_HC89: 0x14159	DSI1_HC90: 0x1415A
DSI1_HC91: 0x1415B	DSI1_HC92: 0x1415C	DSI1_HC93: 0x1415D
DSI1_HC94: 0x1415E	DSI1_HC95: 0x1415F	DSI1_HC96: 0x14160
DSI1_HC97: 0x14161	DSI1_HC98: 0x14162	DSI1_HC99: 0x14163
DSI1_HC100: 0x14164	DSI1_HC101: 0x14165	DSI1_HC102: 0x14166
DSI1_HC103: 0x14167	DSI1_HC104: 0x14168	DSI1_HC105: 0x14169
DSI1_HC106: 0x1416A	DSI1_HC107: 0x1416B	DSI1_HC108: 0x1416C
DSI1_HC109: 0x1416D	DSI1_HC110: 0x1416E	DSI1_HC111: 0x1416F
DSI1_HC112: 0x14170	DSI1_HC113: 0x14171	DSI1_HC114: 0x14172
DSI1_HC115: 0x14173	DSI1_HC116: 0x14174	DSI1_HC117: 0x14175
DSI1_HC118: 0x14176	DSI1_HC119: 0x14177	DSI1_HC120: 0x14178
DSI1_HC121: 0x14179	DSI1_HC122: 0x1417A	DSI1_HC123: 0x1417B
DSI1_HC124: 0x1417C	DSI1_HC125: 0x1417D	DSI1_HC126: 0x1417E
DSI1_HC127: 0x1417F	DSI2_HC0: 0x14200	DSI2_HC1: 0x14201
DSI2_HC2: 0x14202	DSI2_HC3: 0x14203	DSI2_HC4: 0x14204
DSI2_HC5: 0x14205	DSI2_HC6: 0x14206	DSI2_HC7: 0x14207
DSI2_HC8: 0x14208	DSI2_HC9: 0x14209	DSI2_HC10: 0x1420A
DSI2_HC11: 0x1420B	DSI2_HC12: 0x1420C	DSI2_HC13: 0x1420D
DSI2_HC14: 0x1420E	DSI2_HC15: 0x1420F	DSI2_HC16: 0x14210
DSI2_HC17: 0x14211	DSI2_HC18: 0x14212	DSI2_HC19: 0x14213
DSI2_HC20: 0x14214	DSI2_HC21: 0x14215	DSI2_HC22: 0x14216
DSI2_HC23: 0x14217	DSI2_HC24: 0x14218	DSI2_HC25: 0x14219
DSI2_HC26: 0x1421A	DSI2_HC27: 0x1421B	DSI2_HC28: 0x1421C
DSI2_HC29: 0x1421D	DSI2_HC30: 0x1421E	DSI2_HC31: 0x1421F
DSI2_HC32: 0x14220	DSI2_HC33: 0x14221	DSI2_HC34: 0x14222
DSI2_HC35: 0x14223	DSI2_HC36: 0x14224	DSI2_HC37: 0x14225
DSI2_HC38: 0x14226	DSI2_HC39: 0x14227	DSI2_HC40: 0x14228
DSI2_HC41: 0x14229	DSI2_HC42: 0x1422A	DSI2_HC43: 0x1422B
DSI2_HC44: 0x1422C	DSI2_HC45: 0x1422D	DSI2_HC46: 0x1422E
DSI2_HC47: 0x1422F	DSI2_HC48: 0x14230	DSI2_HC49: 0x14231
DSI2_HC50: 0x14232	DSI2_HC51: 0x14233	DSI2_HC52: 0x14234
DSI2_HC53: 0x14235	DSI2_HC54: 0x14236	DSI2_HC55: 0x14237
DSI2_HC56: 0x14238	DSI2_HC57: 0x14239	DSI2_HC58: 0x1423A

(continued)

Register : Address		
DSI2_HC59: 0x1423B	DSI2_HC60: 0x1423C	DSI2_HC61: 0x1423D
DSI2_HC62: 0x1423E	DSI2_HC63: 0x1423F	DSI2_HC64: 0x14240
DSI2_HC65: 0x14241	DSI2_HC66: 0x14242	DSI2_HC67: 0x14243
DSI2_HC68: 0x14244	DSI2_HC69: 0x14245	DSI2_HC70: 0x14246
DSI2_HC71: 0x14247	DSI2_HC72: 0x14248	DSI2_HC73: 0x14249
DSI2_HC74: 0x1424A	DSI2_HC75: 0x1424B	DSI2_HC76: 0x1424C
DSI2_HC77: 0x1424D	DSI2_HC78: 0x1424E	DSI2_HC79: 0x1424F
DSI2_HC80: 0x14250	DSI2_HC81: 0x14251	DSI2_HC82: 0x14252
DSI2_HC83: 0x14253	DSI2_HC84: 0x14254	DSI2_HC85: 0x14255
DSI2_HC86: 0x14256	DSI2_HC87: 0x14257	DSI2_HC88: 0x14258
DSI2_HC89: 0x14259	DSI2_HC90: 0x1425A	DSI2_HC91: 0x1425B
DSI2_HC92: 0x1425C	DSI2_HC93: 0x1425D	DSI2_HC94: 0x1425E
DSI2_HC95: 0x1425F	DSI2_HC96: 0x14260	DSI2_HC97: 0x14261
DSI2_HC98: 0x14262	DSI2_HC99: 0x14263	DSI2_HC100: 0x14264
DSI2_HC101: 0x14265	DSI2_HC102: 0x14266	DSI2_HC103: 0x14267
DSI2_HC104: 0x14268	DSI2_HC105: 0x14269	DSI2_HC106: 0x1426A
DSI2_HC107: 0x1426B	DSI2_HC108: 0x1426C	DSI2_HC109: 0x1426D
DSI2_HC110: 0x1426E	DSI2_HC111: 0x1426F	DSI2_HC112: 0x14270
DSI2_HC113: 0x14271	DSI2_HC114: 0x14272	DSI2_HC115: 0x14273
DSI2_HC116: 0x14274	DSI2_HC117: 0x14275	DSI2_HC118: 0x14276
DSI2_HC119: 0x14277	DSI2_HC120: 0x14278	DSI2_HC121: 0x14279
DSI2_HC122: 0x1427A	DSI2_HC123: 0x1427B	DSI2_HC124: 0x1427C
DSI2_HC125: 0x1427D	DSI2_HC126: 0x1427E	DSI2_HC127: 0x1427F
DSI3_HC0: 0x14300	DSI3_HC1: 0x14301	DSI3_HC2: 0x14302
DSI3_HC3: 0x14303	DSI3_HC4: 0x14304	DSI3_HC5: 0x14305
DSI3_HC6: 0x14306	DSI3_HC7: 0x14307	DSI3_HC8: 0x14308
DSI3_HC9: 0x14309	DSI3_HC10: 0x1430A	DSI3_HC11: 0x1430B
DSI3_HC12: 0x1430C	DSI3_HC13: 0x1430D	DSI3_HC14: 0x1430E
DSI3_HC15: 0x1430F	DSI3_HC16: 0x14310	DSI3_HC17: 0x14311
DSI3_HC18: 0x14312	DSI3_HC19: 0x14313	DSI3_HC20: 0x14314
DSI3_HC21: 0x14315	DSI3_HC22: 0x14316	DSI3_HC23: 0x14317
DSI3_HC24: 0x14318	DSI3_HC25: 0x14319	DSI3_HC26: 0x1431A
DSI3_HC27: 0x1431B	DSI3_HC28: 0x1431C	DSI3_HC29: 0x1431D
DSI3_HC30: 0x1431E	DSI3_HC31: 0x1431F	DSI3_HC32: 0x14320
DSI3_HC33: 0x14321	DSI3_HC34: 0x14322	DSI3_HC35: 0x14323
DSI3_HC36: 0x14324	DSI3_HC37: 0x14325	DSI3_HC38: 0x14326

(continued)

Register : Address		
DSI3_HC39: 0x14327	DSI3_HC40: 0x14328	DSI3_HC41: 0x14329
DSI3_HC42: 0x1432A	DSI3_HC43: 0x1432B	DSI3_HC44: 0x1432C
DSI3_HC45: 0x1432D	DSI3_HC46: 0x1432E	DSI3_HC47: 0x1432F
DSI3_HC48: 0x14330	DSI3_HC49: 0x14331	DSI3_HC50: 0x14332
DSI3_HC51: 0x14333	DSI3_HC52: 0x14334	DSI3_HC53: 0x14335
DSI3_HC54: 0x14336	DSI3_HC55: 0x14337	DSI3_HC56: 0x14338
DSI3_HC57: 0x14339	DSI3_HC58: 0x1433A	DSI3_HC59: 0x1433B
DSI3_HC60: 0x1433C	DSI3_HC61: 0x1433D	DSI3_HC62: 0x1433E
DSI3_HC63: 0x1433F	DSI3_HC64: 0x14340	DSI3_HC65: 0x14341
DSI3_HC66: 0x14342	DSI3_HC67: 0x14343	DSI3_HC68: 0x14344
DSI3_HC69: 0x14345	DSI3_HC70: 0x14346	DSI3_HC71: 0x14347
DSI3_HC72: 0x14348	DSI3_HC73: 0x14349	DSI3_HC74: 0x1434A
DSI3_HC75: 0x1434B	DSI3_HC76: 0x1434C	DSI3_HC77: 0x1434D
DSI3_HC78: 0x1434E	DSI3_HC79: 0x1434F	DSI3_HC80: 0x14350
DSI3_HC81: 0x14351	DSI3_HC82: 0x14352	DSI3_HC83: 0x14353
DSI3_HC84: 0x14354	DSI3_HC85: 0x14355	DSI3_HC86: 0x14356
DSI3_HC87: 0x14357	DSI3_HC88: 0x14358	DSI3_HC89: 0x14359
DSI3_HC90: 0x1435A	DSI3_HC91: 0x1435B	DSI3_HC92: 0x1435C
DSI3_HC93: 0x1435D	DSI3_HC94: 0x1435E	DSI3_HC95: 0x1435F
DSI3_HC96: 0x14360	DSI3_HC97: 0x14361	DSI3_HC98: 0x14362
DSI3_HC99: 0x14363	DSI3_HC100: 0x14364	DSI3_HC101: 0x14365
DSI3_HC102: 0x14366	DSI3_HC103: 0x14367	DSI3_HC104: 0x14368
DSI3_HC105: 0x14369	DSI3_HC106: 0x1436A	DSI3_HC107: 0x1436B
DSI3_HC108: 0x1436C	DSI3_HC109: 0x1436D	DSI3_HC110: 0x1436E
DSI3_HC111: 0x1436F	DSI3_HC112: 0x14370	DSI3_HC113: 0x14371
DSI3_HC114: 0x14372	DSI3_HC115: 0x14373	DSI3_HC116: 0x14374
DSI3_HC117: 0x14375	DSI3_HC118: 0x14376	DSI3_HC119: 0x14377
DSI3_HC120: 0x14378	DSI3_HC121: 0x14379	DSI3_HC122: 0x1437A
DSI3_HC123: 0x1437B	DSI3_HC124: 0x1437C	DSI3_HC125: 0x1437D
DSI3_HC126: 0x1437E	DSI3_HC127: 0x1437F	DSI4_HC0: 0x14400
DSI4_HC1: 0x14401	DSI4_HC2: 0x14402	DSI4_HC3: 0x14403
DSI4_HC4: 0x14404	DSI4_HC5: 0x14405	DSI4_HC6: 0x14406
DSI4_HC7: 0x14407	DSI4_HC8: 0x14408	DSI4_HC9: 0x14409
DSI4_HC10: 0x1440A	DSI4_HC11: 0x1440B	DSI4_HC12: 0x1440C
DSI4_HC13: 0x1440D	DSI4_HC14: 0x1440E	DSI4_HC15: 0x1440F
DSI4_HC16: 0x14410	DSI4_HC17: 0x14411	DSI4_HC18: 0x14412

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Register : Address		
DSI4_HC19: 0x14413	DSI4_HC20: 0x14414	DSI4_HC21: 0x14415
DSI4_HC22: 0x14416	DSI4_HC23: 0x14417	DSI4_HC24: 0x14418
DSI4_HC25: 0x14419	DSI4_HC26: 0x1441A	DSI4_HC27: 0x1441B
DSI4_HC28: 0x1441C	DSI4_HC29: 0x1441D	DSI4_HC30: 0x1441E
DSI4_HC31: 0x1441F	DSI4_HC32: 0x14420	DSI4_HC33: 0x14421
DSI4_HC34: 0x14422	DSI4_HC35: 0x14423	DSI4_HC36: 0x14424
DSI4_HC37: 0x14425	DSI4_HC38: 0x14426	DSI4_HC39: 0x14427
DSI4_HC40: 0x14428	DSI4_HC41: 0x14429	DSI4_HC42: 0x1442A
DSI4_HC43: 0x1442B	DSI4_HC44: 0x1442C	DSI4_HC45: 0x1442D
DSI4_HC46: 0x1442E	DSI4_HC47: 0x1442F	DSI4_HC48: 0x14430
DSI4_HC49: 0x14431	DSI4_HC50: 0x14432	DSI4_HC51: 0x14433
DSI4_HC52: 0x14434	DSI4_HC53: 0x14435	DSI4_HC54: 0x14436
DSI4_HC55: 0x14437	DSI4_HC56: 0x14438	DSI4_HC57: 0x14439
DSI4_HC58: 0x1443A	DSI4_HC59: 0x1443B	DSI4_HC60: 0x1443C
DSI4_HC61: 0x1443D	DSI4_HC62: 0x1443E	DSI4_HC63: 0x1443F
DSI4_HC64: 0x14440	DSI4_HC65: 0x14441	DSI4_HC66: 0x14442
DSI4_HC67: 0x14443	DSI4_HC68: 0x14444	DSI4_HC69: 0x14445
DSI4_HC70: 0x14446	DSI4_HC71: 0x14447	DSI4_HC72: 0x14448
DSI4_HC73: 0x14449	DSI4_HC74: 0x1444A	DSI4_HC75: 0x1444B
DSI4_HC76: 0x1444C	DSI4_HC77: 0x1444D	DSI4_HC78: 0x1444E
DSI4_HC79: 0x1444F	DSI4_HC80: 0x14450	DSI4_HC81: 0x14451
DSI4_HC82: 0x14452	DSI4_HC83: 0x14453	DSI4_HC84: 0x14454
DSI4_HC85: 0x14455	DSI4_HC86: 0x14456	DSI4_HC87: 0x14457
DSI4_HC88: 0x14458	DSI4_HC89: 0x14459	DSI4_HC90: 0x1445A
DSI4_HC91: 0x1445B	DSI4_HC92: 0x1445C	DSI4_HC93: 0x1445D
DSI4_HC94: 0x1445E	DSI4_HC95: 0x1445F	DSI4_HC96: 0x14460
DSI4_HC97: 0x14461	DSI4_HC98: 0x14462	DSI4_HC99: 0x14463
DSI4_HC100: 0x14464	DSI4_HC101: 0x14465	DSI4_HC102: 0x14466
DSI4_HC103: 0x14467	DSI4_HC104: 0x14468	DSI4_HC105: 0x14469
DSI4_HC106: 0x1446A	DSI4_HC107: 0x1446B	DSI4_HC108: 0x1446C
DSI4_HC109: 0x1446D	DSI4_HC110: 0x1446E	DSI4_HC111: 0x1446F
DSI4_HC112: 0x14470	DSI4_HC113: 0x14471	DSI4_HC114: 0x14472
DSI4_HC115: 0x14473	DSI4_HC116: 0x14474	DSI4_HC117: 0x14475
DSI4_HC118: 0x14476	DSI4_HC119: 0x14477	DSI4_HC120: 0x14478
DSI4_HC121: 0x14479	DSI4_HC122: 0x1447A	DSI4_HC123: 0x1447B
DSI4_HC124: 0x1447C	DSI4_HC125: 0x1447D	DSI4_HC126: 0x1447E

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Register : Address		
DSI4_HC127: 0x1447F	DSI5_HC0: 0x14500	DSI5_HC1: 0x14501
DSI5_HC2: 0x14502	DSI5_HC3: 0x14503	DSI5_HC4: 0x14504
DSI5_HC5: 0x14505	DSI5_HC6: 0x14506	DSI5_HC7: 0x14507
DSI5_HC8: 0x14508	DSI5_HC9: 0x14509	DSI5_HC10: 0x1450A
DSI5_HC11: 0x1450B	DSI5_HC12: 0x1450C	DSI5_HC13: 0x1450D
DSI5_HC14: 0x1450E	DSI5_HC15: 0x1450F	DSI5_HC16: 0x14510
DSI5_HC17: 0x14511	DSI5_HC18: 0x14512	DSI5_HC19: 0x14513
DSI5_HC20: 0x14514	DSI5_HC21: 0x14515	DSI5_HC22: 0x14516
DSI5_HC23: 0x14517	DSI5_HC24: 0x14518	DSI5_HC25: 0x14519
DSI5_HC26: 0x1451A	DSI5_HC27: 0x1451B	DSI5_HC28: 0x1451C
DSI5_HC29: 0x1451D	DSI5_HC30: 0x1451E	DSI5_HC31: 0x1451F
DSI5_HC32: 0x14520	DSI5_HC33: 0x14521	DSI5_HC34: 0x14522
DSI5_HC35: 0x14523	DSI5_HC36: 0x14524	DSI5_HC37: 0x14525
DSI5_HC38: 0x14526	DSI5_HC39: 0x14527	DSI5_HC40: 0x14528
DSI5_HC41: 0x14529	DSI5_HC42: 0x1452A	DSI5_HC43: 0x1452B
DSI5_HC44: 0x1452C	DSI5_HC45: 0x1452D	DSI5_HC46: 0x1452E
DSI5_HC47: 0x1452F	DSI5_HC48: 0x14530	DSI5_HC49: 0x14531
DSI5_HC50: 0x14532	DSI5_HC51: 0x14533	DSI5_HC52: 0x14534
DSI5_HC53: 0x14535	DSI5_HC54: 0x14536	DSI5_HC55: 0x14537
DSI5_HC56: 0x14538	DSI5_HC57: 0x14539	DSI5_HC58: 0x1453A
DSI5_HC59: 0x1453B	DSI5_HC60: 0x1453C	DSI5_HC61: 0x1453D
DSI5_HC62: 0x1453E	DSI5_HC63: 0x1453F	DSI5_HC64: 0x14540
DSI5_HC65: 0x14541	DSI5_HC66: 0x14542	DSI5_HC67: 0x14543
DSI5_HC68: 0x14544	DSI5_HC69: 0x14545	DSI5_HC70: 0x14546
DSI5_HC71: 0x14547	DSI5_HC72: 0x14548	DSI5_HC73: 0x14549
DSI5_HC74: 0x1454A	DSI5_HC75: 0x1454B	DSI5_HC76: 0x1454C
DSI5_HC77: 0x1454D	DSI5_HC78: 0x1454E	DSI5_HC79: 0x1454F
DSI5_HC80: 0x14550	DSI5_HC81: 0x14551	DSI5_HC82: 0x14552
DSI5_HC83: 0x14553	DSI5_HC84: 0x14554	DSI5_HC85: 0x14555
DSI5_HC86: 0x14556	DSI5_HC87: 0x14557	DSI5_HC88: 0x14558
DSI5_HC89: 0x14559	DSI5_HC90: 0x1455A	DSI5_HC91: 0x1455B
DSI5_HC92: 0x1455C	DSI5_HC93: 0x1455D	DSI5_HC94: 0x1455E
DSI5_HC95: 0x1455F	DSI5_HC96: 0x14560	DSI5_HC97: 0x14561
DSI5_HC98: 0x14562	DSI5_HC99: 0x14563	DSI5_HC100: 0x14564
DSI5_HC101: 0x14565	DSI5_HC102: 0x14566	DSI5_HC103: 0x14567
DSI5_HC104: 0x14568	DSI5_HC105: 0x14569	DSI5_HC106: 0x1456A

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Register : Address		
DSI5_HC107: 0x1456B	DSI5_HC108: 0x1456C	DSI5_HC109: 0x1456D
DSI5_HC110: 0x1456E	DSI5_HC111: 0x1456F	DSI5_HC112: 0x14570
DSI5_HC113: 0x14571	DSI5_HC114: 0x14572	DSI5_HC115: 0x14573
DSI5_HC116: 0x14574	DSI5_HC117: 0x14575	DSI5_HC118: 0x14576
DSI5_HC119: 0x14577	DSI5_HC120: 0x14578	DSI5_HC121: 0x14579
DSI5_HC122: 0x1457A	DSI5_HC123: 0x1457B	DSI5_HC124: 0x1457C
DSI5_HC125: 0x1457D	DSI5_HC126: 0x1457E	DSI5_HC127: 0x1457F
DSI6_HC0: 0x14600	DSI6_HC1: 0x14601	DSI6_HC2: 0x14602
DSI6_HC3: 0x14603	DSI6_HC4: 0x14604	DSI6_HC5: 0x14605
DSI6_HC6: 0x14606	DSI6_HC7: 0x14607	DSI6_HC8: 0x14608
DSI6_HC9: 0x14609	DSI6_HC10: 0x1460A	DSI6_HC11: 0x1460B
DSI6_HC12: 0x1460C	DSI6_HC13: 0x1460D	DSI6_HC14: 0x1460E
DSI6_HC15: 0x1460F	DSI6_HC16: 0x14610	DSI6_HC17: 0x14611
DSI6_HC18: 0x14612	DSI6_HC19: 0x14613	DSI6_HC20: 0x14614
DSI6_HC21: 0x14615	DSI6_HC22: 0x14616	DSI6_HC23: 0x14617
DSI6_HC24: 0x14618	DSI6_HC25: 0x14619	DSI6_HC26: 0x1461A
DSI6_HC27: 0x1461B	DSI6_HC28: 0x1461C	DSI6_HC29: 0x1461D
DSI6_HC30: 0x1461E	DSI6_HC31: 0x1461F	DSI6_HC32: 0x14620
DSI6_HC33: 0x14621	DSI6_HC34: 0x14622	DSI6_HC35: 0x14623
DSI6_HC36: 0x14624	DSI6_HC37: 0x14625	DSI6_HC38: 0x14626
DSI6_HC39: 0x14627	DSI6_HC40: 0x14628	DSI6_HC41: 0x14629
DSI6_HC42: 0x1462A	DSI6_HC43: 0x1462B	DSI6_HC44: 0x1462C
DSI6_HC45: 0x1462D	DSI6_HC46: 0x1462E	DSI6_HC47: 0x1462F
DSI6_HC48: 0x14630	DSI6_HC49: 0x14631	DSI6_HC50: 0x14632
DSI6_HC51: 0x14633	DSI6_HC52: 0x14634	DSI6_HC53: 0x14635
DSI6_HC54: 0x14636	DSI6_HC55: 0x14637	DSI6_HC56: 0x14638
DSI6_HC57: 0x14639	DSI6_HC58: 0x1463A	DSI6_HC59: 0x1463B
DSI6_HC60: 0x1463C	DSI6_HC61: 0x1463D	DSI6_HC62: 0x1463E
DSI6_HC63: 0x1463F	DSI6_HC64: 0x14640	DSI6_HC65: 0x14641
DSI6_HC66: 0x14642	DSI6_HC67: 0x14643	DSI6_HC68: 0x14644
DSI6_HC69: 0x14645	DSI6_HC70: 0x14646	DSI6_HC71: 0x14647
DSI6_HC72: 0x14648	DSI6_HC73: 0x14649	DSI6_HC74: 0x1464A
DSI6_HC75: 0x1464B	DSI6_HC76: 0x1464C	DSI6_HC77: 0x1464D
DSI6_HC78: 0x1464E	DSI6_HC79: 0x1464F	DSI6_HC80: 0x14650
DSI6_HC81: 0x14651	DSI6_HC82: 0x14652	DSI6_HC83: 0x14653
DSI6_HC84: 0x14654	DSI6_HC85: 0x14655	DSI6_HC86: 0x14656

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Register : Address		
DSI6_HC87: 0x14657	DSI6_HC88: 0x14658	DSI6_HC89: 0x14659
DSI6_HC90: 0x1465A	DSI6_HC91: 0x1465B	DSI6_HC92: 0x1465C
DSI6_HC93: 0x1465D	DSI6_HC94: 0x1465E	DSI6_HC95: 0x1465F
DSI6_HC96: 0x14660	DSI6_HC97: 0x14661	DSI6_HC98: 0x14662
DSI6_HC99: 0x14663	DSI6_HC100: 0x14664	DSI6_HC101: 0x14665
DSI6_HC102: 0x14666	DSI6_HC103: 0x14667	DSI6_HC104: 0x14668
DSI6_HC105: 0x14669	DSI6_HC106: 0x1466A	DSI6_HC107: 0x1466B
DSI6_HC108: 0x1466C	DSI6_HC109: 0x1466D	DSI6_HC110: 0x1466E
DSI6_HC111: 0x1466F	DSI6_HC112: 0x14670	DSI6_HC113: 0x14671
DSI6_HC114: 0x14672	DSI6_HC115: 0x14673	DSI6_HC116: 0x14674
DSI6_HC117: 0x14675	DSI6_HC118: 0x14676	DSI6_HC119: 0x14677
DSI6_HC120: 0x14678	DSI6_HC121: 0x14679	DSI6_HC122: 0x1467A
DSI6_HC123: 0x1467B	DSI6_HC124: 0x1467C	DSI6_HC125: 0x1467D
DSI6_HC126: 0x1467E	DSI6_HC127: 0x1467F	DSI7_HC0: 0x14700
DSI7_HC1: 0x14701	DSI7_HC2: 0x14702	DSI7_HC3: 0x14703
DSI7_HC4: 0x14704	DSI7_HC5: 0x14705	DSI7_HC6: 0x14706
DSI7_HC7: 0x14707	DSI7_HC8: 0x14708	DSI7_HC9: 0x14709
DSI7_HC10: 0x1470A	DSI7_HC11: 0x1470B	DSI7_HC12: 0x1470C
DSI7_HC13: 0x1470D	DSI7_HC14: 0x1470E	DSI7_HC15: 0x1470F
DSI7_HC16: 0x14710	DSI7_HC17: 0x14711	DSI7_HC18: 0x14712
DSI7_HC19: 0x14713	DSI7_HC20: 0x14714	DSI7_HC21: 0x14715
DSI7_HC22: 0x14716	DSI7_HC23: 0x14717	DSI7_HC24: 0x14718
DSI7_HC25: 0x14719	DSI7_HC26: 0x1471A	DSI7_HC27: 0x1471B
DSI7_HC28: 0x1471C	DSI7_HC29: 0x1471D	DSI7_HC30: 0x1471E
DSI7_HC31: 0x1471F	DSI7_HC32: 0x14720	DSI7_HC33: 0x14721
DSI7_HC34: 0x14722	DSI7_HC35: 0x14723	DSI7_HC36: 0x14724
DSI7_HC37: 0x14725	DSI7_HC38: 0x14726	DSI7_HC39: 0x14727
DSI7_HC40: 0x14728	DSI7_HC41: 0x14729	DSI7_HC42: 0x1472A
DSI7_HC43: 0x1472B	DSI7_HC44: 0x1472C	DSI7_HC45: 0x1472D
DSI7_HC46: 0x1472E	DSI7_HC47: 0x1472F	DSI7_HC48: 0x14730
DSI7_HC49: 0x14731	DSI7_HC50: 0x14732	DSI7_HC51: 0x14733
DSI7_HC52: 0x14734	DSI7_HC53: 0x14735	DSI7_HC54: 0x14736
DSI7_HC55: 0x14737	DSI7_HC56: 0x14738	DSI7_HC57: 0x14739
DSI7_HC58: 0x1473A	DSI7_HC59: 0x1473B	DSI7_HC60: 0x1473C
DSI7_HC61: 0x1473D	DSI7_HC62: 0x1473E	DSI7_HC63: 0x1473F
DSI7_HC64: 0x14740	DSI7_HC65: 0x14741	DSI7_HC66: 0x14742

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Register : Address		
DSI7_HC67: 0x14743	DSI7_HC68: 0x14744	DSI7_HC69: 0x14745
DSI7_HC70: 0x14746	DSI7_HC71: 0x14747	DSI7_HC72: 0x14748
DSI7_HC73: 0x14749	DSI7_HC74: 0x1474A	DSI7_HC75: 0x1474B
DSI7_HC76: 0x1474C	DSI7_HC77: 0x1474D	DSI7_HC78: 0x1474E
DSI7_HC79: 0x1474F	DSI7_HC80: 0x14750	DSI7_HC81: 0x14751
DSI7_HC82: 0x14752	DSI7_HC83: 0x14753	DSI7_HC84: 0x14754
DSI7_HC85: 0x14755	DSI7_HC86: 0x14756	DSI7_HC87: 0x14757
DSI7_HC88: 0x14758	DSI7_HC89: 0x14759	DSI7_HC90: 0x1475A
DSI7_HC91: 0x1475B	DSI7_HC92: 0x1475C	DSI7_HC93: 0x1475D
DSI7_HC94: 0x1475E	DSI7_HC95: 0x1475F	DSI7_HC96: 0x14760
DSI7_HC97: 0x14761	DSI7_HC98: 0x14762	DSI7_HC99: 0x14763
DSI7_HC100: 0x14764	DSI7_HC101: 0x14765	DSI7_HC102: 0x14766
DSI7_HC103: 0x14767	DSI7_HC104: 0x14768	DSI7_HC105: 0x14769
DSI7_HC106: 0x1476A	DSI7_HC107: 0x1476B	DSI7_HC108: 0x1476C
DSI7_HC109: 0x1476D	DSI7_HC110: 0x1476E	DSI7_HC111: 0x1476F
DSI7_HC112: 0x14770	DSI7_HC113: 0x14771	DSI7_HC114: 0x14772
DSI7_HC115: 0x14773	DSI7_HC116: 0x14774	DSI7_HC117: 0x14775
DSI7_HC118: 0x14776	DSI7_HC119: 0x14777	DSI7_HC120: 0x14778
DSI7_HC121: 0x14779	DSI7_HC122: 0x1477A	DSI7_HC123: 0x1477B
DSI7_HC124: 0x1477C	DSI7_HC125: 0x1477D	DSI7_HC126: 0x1477E
DSI7_HC127: 0x1477F	DSI8_HC0: 0x14800	DSI8_HC1: 0x14801
DSI8_HC2: 0x14802	DSI8_HC3: 0x14803	DSI8_HC4: 0x14804
DSI8_HC5: 0x14805	DSI8_HC6: 0x14806	DSI8_HC7: 0x14807
DSI8_HC8: 0x14808	DSI8_HC9: 0x14809	DSI8_HC10: 0x1480A
DSI8_HC11: 0x1480B	DSI8_HC12: 0x1480C	DSI8_HC13: 0x1480D
DSI8_HC14: 0x1480E	DSI8_HC15: 0x1480F	DSI8_HC16: 0x14810
DSI8_HC17: 0x14811	DSI8_HC18: 0x14812	DSI8_HC19: 0x14813
DSI8_HC20: 0x14814	DSI8_HC21: 0x14815	DSI8_HC22: 0x14816
DSI8_HC23: 0x14817	DSI8_HC24: 0x14818	DSI8_HC25: 0x14819
DSI8_HC26: 0x1481A	DSI8_HC27: 0x1481B	DSI8_HC28: 0x1481C
DSI8_HC29: 0x1481D	DSI8_HC30: 0x1481E	DSI8_HC31: 0x1481F
DSI8_HC32: 0x14820	DSI8_HC33: 0x14821	DSI8_HC34: 0x14822
DSI8_HC35: 0x14823	DSI8_HC36: 0x14824	DSI8_HC37: 0x14825
DSI8_HC38: 0x14826	DSI8_HC39: 0x14827	DSI8_HC40: 0x14828
DSI8_HC41: 0x14829	DSI8_HC42: 0x1482A	DSI8_HC43: 0x1482B
DSI8_HC44: 0x1482C	DSI8_HC45: 0x1482D	DSI8_HC46: 0x1482E

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Register : Address		
DSI8_HC47: 0x1482F	DSI8_HC48: 0x14830	DSI8_HC49: 0x14831
DSI8_HC50: 0x14832	DSI8_HC51: 0x14833	DSI8_HC52: 0x14834
DSI8_HC53: 0x14835	DSI8_HC54: 0x14836	DSI8_HC55: 0x14837
DSI8_HC56: 0x14838	DSI8_HC57: 0x14839	DSI8_HC58: 0x1483A
DSI8_HC59: 0x1483B	DSI8_HC60: 0x1483C	DSI8_HC61: 0x1483D
DSI8_HC62: 0x1483E	DSI8_HC63: 0x1483F	DSI8_HC64: 0x14840
DSI8_HC65: 0x14841	DSI8_HC66: 0x14842	DSI8_HC67: 0x14843
DSI8_HC68: 0x14844	DSI8_HC69: 0x14845	DSI8_HC70: 0x14846
DSI8_HC71: 0x14847	DSI8_HC72: 0x14848	DSI8_HC73: 0x14849
DSI8_HC74: 0x1484A	DSI8_HC75: 0x1484B	DSI8_HC76: 0x1484C
DSI8_HC77: 0x1484D	DSI8_HC78: 0x1484E	DSI8_HC79: 0x1484F
DSI8_HC80: 0x14850	DSI8_HC81: 0x14851	DSI8_HC82: 0x14852
DSI8_HC83: 0x14853	DSI8_HC84: 0x14854	DSI8_HC85: 0x14855
DSI8_HC86: 0x14856	DSI8_HC87: 0x14857	DSI8_HC88: 0x14858
DSI8_HC89: 0x14859	DSI8_HC90: 0x1485A	DSI8_HC91: 0x1485B
DSI8_HC92: 0x1485C	DSI8_HC93: 0x1485D	DSI8_HC94: 0x1485E
DSI8_HC95: 0x1485F	DSI8_HC96: 0x14860	DSI8_HC97: 0x14861
DSI8_HC98: 0x14862	DSI8_HC99: 0x14863	DSI8_HC100: 0x14864
DSI8_HC101: 0x14865	DSI8_HC102: 0x14866	DSI8_HC103: 0x14867
DSI8_HC104: 0x14868	DSI8_HC105: 0x14869	DSI8_HC106: 0x1486A
DSI8_HC107: 0x1486B	DSI8_HC108: 0x1486C	DSI8_HC109: 0x1486D
DSI8_HC110: 0x1486E	DSI8_HC111: 0x1486F	DSI8_HC112: 0x14870
DSI8_HC113: 0x14871	DSI8_HC114: 0x14872	DSI8_HC115: 0x14873
DSI8_HC116: 0x14874	DSI8_HC117: 0x14875	DSI8_HC118: 0x14876
DSI8_HC119: 0x14877	DSI8_HC120: 0x14878	DSI8_HC121: 0x14879
DSI8_HC122: 0x1487A	DSI8_HC123: 0x1487B	DSI8_HC124: 0x1487C
DSI8_HC125: 0x1487D	DSI8_HC126: 0x1487E	DSI8_HC127: 0x1487F
DSI9_HC0: 0x14900	DSI9_HC1: 0x14901	DSI9_HC2: 0x14902
DSI9_HC3: 0x14903	DSI9_HC4: 0x14904	DSI9_HC5: 0x14905
DSI9_HC6: 0x14906	DSI9_HC7: 0x14907	DSI9_HC8: 0x14908
DSI9_HC9: 0x14909	DSI9_HC10: 0x1490A	DSI9_HC11: 0x1490B
DSI9_HC12: 0x1490C	DSI9_HC13: 0x1490D	DSI9_HC14: 0x1490E
DSI9_HC15: 0x1490F	DSI9_HC16: 0x14910	DSI9_HC17: 0x14911
DSI9_HC18: 0x14912	DSI9_HC19: 0x14913	DSI9_HC20: 0x14914
DSI9_HC21: 0x14915	DSI9_HC22: 0x14916	DSI9_HC23: 0x14917
DSI9_HC24: 0x14918	DSI9_HC25: 0x14919	DSI9_HC26: 0x1491A

(continued)

Register : Address		
DSI9_HC27: 0x1491B	DSI9_HC28: 0x1491C	DSI9_HC29: 0x1491D
DSI9_HC30: 0x1491E	DSI9_HC31: 0x1491F	DSI9_HC32: 0x14920
DSI9_HC33: 0x14921	DSI9_HC34: 0x14922	DSI9_HC35: 0x14923
DSI9_HC36: 0x14924	DSI9_HC37: 0x14925	DSI9_HC38: 0x14926
DSI9_HC39: 0x14927	DSI9_HC40: 0x14928	DSI9_HC41: 0x14929
DSI9_HC42: 0x1492A	DSI9_HC43: 0x1492B	DSI9_HC44: 0x1492C
DSI9_HC45: 0x1492D	DSI9_HC46: 0x1492E	DSI9_HC47: 0x1492F
DSI9_HC48: 0x14930	DSI9_HC49: 0x14931	DSI9_HC50: 0x14932
DSI9_HC51: 0x14933	DSI9_HC52: 0x14934	DSI9_HC53: 0x14935
DSI9_HC54: 0x14936	DSI9_HC55: 0x14937	DSI9_HC56: 0x14938
DSI9_HC57: 0x14939	DSI9_HC58: 0x1493A	DSI9_HC59: 0x1493B
DSI9_HC60: 0x1493C	DSI9_HC61: 0x1493D	DSI9_HC62: 0x1493E
DSI9_HC63: 0x1493F	DSI9_HC64: 0x14940	DSI9_HC65: 0x14941
DSI9_HC66: 0x14942	DSI9_HC67: 0x14943	DSI9_HC68: 0x14944
DSI9_HC69: 0x14945	DSI9_HC70: 0x14946	DSI9_HC71: 0x14947
DSI9_HC72: 0x14948	DSI9_HC73: 0x14949	DSI9_HC74: 0x1494A
DSI9_HC75: 0x1494B	DSI9_HC76: 0x1494C	DSI9_HC77: 0x1494D
DSI9_HC78: 0x1494E	DSI9_HC79: 0x1494F	DSI9_HC80: 0x14950
DSI9_HC81: 0x14951	DSI9_HC82: 0x14952	DSI9_HC83: 0x14953
DSI9_HC84: 0x14954	DSI9_HC85: 0x14955	DSI9_HC86: 0x14956
DSI9_HC87: 0x14957	DSI9_HC88: 0x14958	DSI9_HC89: 0x14959
DSI9_HC90: 0x1495A	DSI9_HC91: 0x1495B	DSI9_HC92: 0x1495C
DSI9_HC93: 0x1495D	DSI9_HC94: 0x1495E	DSI9_HC95: 0x1495F
DSI9_HC96: 0x14960	DSI9_HC97: 0x14961	DSI9_HC98: 0x14962
DSI9_HC99: 0x14963	DSI9_HC100: 0x14964	DSI9_HC101: 0x14965
DSI9_HC102: 0x14966	DSI9_HC103: 0x14967	DSI9_HC104: 0x14968
DSI9_HC105: 0x14969	DSI9_HC106: 0x1496A	DSI9_HC107: 0x1496B
DSI9_HC108: 0x1496C	DSI9_HC109: 0x1496D	DSI9_HC110: 0x1496E
DSI9_HC111: 0x1496F	DSI9_HC112: 0x14970	DSI9_HC113: 0x14971
DSI9_HC114: 0x14972	DSI9_HC115: 0x14973	DSI9_HC116: 0x14974
DSI9_HC117: 0x14975	DSI9_HC118: 0x14976	DSI9_HC119: 0x14977
DSI9_HC120: 0x14978	DSI9_HC121: 0x14979	DSI9_HC122: 0x1497A
DSI9_HC123: 0x1497B	DSI9_HC124: 0x1497C	DSI9_HC125: 0x1497D
DSI9_HC126: 0x1497E	DSI9_HC127: 0x1497F	DSI12_HC0: 0x14C00
DSI12_HC1: 0x14C01	DSI12_HC2: 0x14C02	DSI12_HC3: 0x14C03
DSI12_HC4: 0x14C04	DSI12_HC5: 0x14C05	DSI12_HC6: 0x14C06

(continued)

Register : Address		
DSI12_HC7: 0x14C07	DSI12_HC8: 0x14C08	DSI12_HC9: 0x14C09
DSI12_HC10: 0x14C0A	DSI12_HC11: 0x14C0B	DSI12_HC12: 0x14C0C
DSI12_HC13: 0x14C0D	DSI12_HC14: 0x14C0E	DSI12_HC15: 0x14C0F
DSI12_HC16: 0x14C10	DSI12_HC17: 0x14C11	DSI12_HC18: 0x14C12
DSI12_HC19: 0x14C13	DSI12_HC20: 0x14C14	DSI12_HC21: 0x14C15
DSI12_HC22: 0x14C16	DSI12_HC23: 0x14C17	DSI12_HC24: 0x14C18
DSI12_HC25: 0x14C19	DSI12_HC26: 0x14C1A	DSI12_HC27: 0x14C1B
DSI12_HC28: 0x14C1C	DSI12_HC29: 0x14C1D	DSI12_HC30: 0x14C1E
DSI12_HC31: 0x14C1F	DSI12_HC32: 0x14C20	DSI12_HC33: 0x14C21
DSI12_HC34: 0x14C22	DSI12_HC35: 0x14C23	DSI12_HC36: 0x14C24
DSI12_HC37: 0x14C25	DSI12_HC38: 0x14C26	DSI12_HC39: 0x14C27
DSI12_HC40: 0x14C28	DSI12_HC41: 0x14C29	DSI12_HC42: 0x14C2A
DSI12_HC43: 0x14C2B	DSI12_HC44: 0x14C2C	DSI12_HC45: 0x14C2D
DSI12_HC46: 0x14C2E	DSI12_HC47: 0x14C2F	DSI12_HC48: 0x14C30
DSI12_HC49: 0x14C31	DSI12_HC50: 0x14C32	DSI12_HC51: 0x14C33
DSI12_HC52: 0x14C34	DSI12_HC53: 0x14C35	DSI12_HC54: 0x14C36
DSI12_HC55: 0x14C37	DSI12_HC56: 0x14C38	DSI12_HC57: 0x14C39
DSI12_HC58: 0x14C3A	DSI12_HC59: 0x14C3B	DSI12_HC60: 0x14C3C
DSI12_HC61: 0x14C3D	DSI12_HC62: 0x14C3E	DSI12_HC63: 0x14C3F
DSI12_HC64: 0x14C40	DSI12_HC65: 0x14C41	DSI12_HC66: 0x14C42
DSI12_HC67: 0x14C43	DSI12_HC68: 0x14C44	DSI12_HC69: 0x14C45
DSI12_HC70: 0x14C46	DSI12_HC71: 0x14C47	DSI12_HC72: 0x14C48
DSI12_HC73: 0x14C49	DSI12_HC74: 0x14C4A	DSI12_HC75: 0x14C4B
DSI12_HC76: 0x14C4C	DSI12_HC77: 0x14C4D	DSI12_HC78: 0x14C4E
DSI12_HC79: 0x14C4F	DSI12_HC80: 0x14C50	DSI12_HC81: 0x14C51
DSI12_HC82: 0x14C52	DSI12_HC83: 0x14C53	DSI12_HC84: 0x14C54
DSI12_HC85: 0x14C55	DSI12_HC86: 0x14C56	DSI12_HC87: 0x14C57
DSI12_HC88: 0x14C58	DSI12_HC89: 0x14C59	DSI12_HC90: 0x14C5A
DSI12_HC91: 0x14C5B	DSI12_HC92: 0x14C5C	DSI12_HC93: 0x14C5D
DSI12_HC94: 0x14C5E	DSI12_HC95: 0x14C5F	DSI12_HC96: 0x14C60
DSI12_HC97: 0x14C61	DSI12_HC98: 0x14C62	DSI12_HC99: 0x14C63
DSI12_HC100: 0x14C64	DSI12_HC101: 0x14C65	DSI12_HC102: 0x14C66
DSI12_HC103: 0x14C67	DSI12_HC104: 0x14C68	DSI12_HC105: 0x14C69
DSI12_HC106: 0x14C6A	DSI12_HC107: 0x14C6B	DSI12_HC108: 0x14C6C
DSI12_HC109: 0x14C6D	DSI12_HC110: 0x14C6E	DSI12_HC111: 0x14C6F
DSI12_HC112: 0x14C70	DSI12_HC113: 0x14C71	DSI12_HC114: 0x14C72

(continued)

Register : Address		
DSI12_HC115: 0x14C73	DSI12_HC116: 0x14C74	DSI12_HC117: 0x14C75
DSI12_HC118: 0x14C76	DSI12_HC119: 0x14C77	DSI12_HC120: 0x14C78
DSI12_HC121: 0x14C79	DSI12_HC122: 0x14C7A	DSI12_HC123: 0x14C7B
DSI12_HC124: 0x14C7C	DSI12_HC125: 0x14C7D	DSI12_HC126: 0x14C7E
DSI12_HC127: 0x14C7F	DSI13_HC0: 0x14D00	DSI13_HC1: 0x14D01
DSI13_HC2: 0x14D02	DSI13_HC3: 0x14D03	DSI13_HC4: 0x14D04
DSI13_HC5: 0x14D05	DSI13_HC6: 0x14D06	DSI13_HC7: 0x14D07
DSI13_HC8: 0x14D08	DSI13_HC9: 0x14D09	DSI13_HC10: 0x14D0A
DSI13_HC11: 0x14D0B	DSI13_HC12: 0x14D0C	DSI13_HC13: 0x14D0D
DSI13_HC14: 0x14D0E	DSI13_HC15: 0x14D0F	DSI13_HC16: 0x14D10
DSI13_HC17: 0x14D11	DSI13_HC18: 0x14D12	DSI13_HC19: 0x14D13
DSI13_HC20: 0x14D14	DSI13_HC21: 0x14D15	DSI13_HC22: 0x14D16
DSI13_HC23: 0x14D17	DSI13_HC24: 0x14D18	DSI13_HC25: 0x14D19
DSI13_HC26: 0x14D1A	DSI13_HC27: 0x14D1B	DSI13_HC28: 0x14D1C
DSI13_HC29: 0x14D1D	DSI13_HC30: 0x14D1E	DSI13_HC31: 0x14D1F
DSI13_HC32: 0x14D20	DSI13_HC33: 0x14D21	DSI13_HC34: 0x14D22
DSI13_HC35: 0x14D23	DSI13_HC36: 0x14D24	DSI13_HC37: 0x14D25
DSI13_HC38: 0x14D26	DSI13_HC39: 0x14D27	DSI13_HC40: 0x14D28
DSI13_HC41: 0x14D29	DSI13_HC42: 0x14D2A	DSI13_HC43: 0x14D2B
DSI13_HC44: 0x14D2C	DSI13_HC45: 0x14D2D	DSI13_HC46: 0x14D2E
DSI13_HC47: 0x14D2F	DSI13_HC48: 0x14D30	DSI13_HC49: 0x14D31
DSI13_HC50: 0x14D32	DSI13_HC51: 0x14D33	DSI13_HC52: 0x14D34
DSI13_HC53: 0x14D35	DSI13_HC54: 0x14D36	DSI13_HC55: 0x14D37
DSI13_HC56: 0x14D38	DSI13_HC57: 0x14D39	DSI13_HC58: 0x14D3A
DSI13_HC59: 0x14D3B	DSI13_HC60: 0x14D3C	DSI13_HC61: 0x14D3D
DSI13_HC62: 0x14D3E	DSI13_HC63: 0x14D3F	DSI13_HC64: 0x14D40
DSI13_HC65: 0x14D41	DSI13_HC66: 0x14D42	DSI13_HC67: 0x14D43
DSI13_HC68: 0x14D44	DSI13_HC69: 0x14D45	DSI13_HC70: 0x14D46
DSI13_HC71: 0x14D47	DSI13_HC72: 0x14D48	DSI13_HC73: 0x14D49
DSI13_HC74: 0x14D4A	DSI13_HC75: 0x14D4B	DSI13_HC76: 0x14D4C
DSI13_HC77: 0x14D4D	DSI13_HC78: 0x14D4E	DSI13_HC79: 0x14D4F
DSI13_HC80: 0x14D50	DSI13_HC81: 0x14D51	DSI13_HC82: 0x14D52
DSI13_HC83: 0x14D53	DSI13_HC84: 0x14D54	DSI13_HC85: 0x14D55
DSI13_HC86: 0x14D56	DSI13_HC87: 0x14D57	DSI13_HC88: 0x14D58
DSI13_HC89: 0x14D59	DSI13_HC90: 0x14D5A	DSI13_HC91: 0x14D5B
DSI13_HC92: 0x14D5C	DSI13_HC93: 0x14D5D	DSI13_HC94: 0x14D5E

(continued)

Register : Address		
DSI13_HC95: 0x14D5F	DSI13_HC96: 0x14D60	DSI13_HC97: 0x14D61
DSI13_HC98: 0x14D62	DSI13_HC99: 0x14D63	DSI13_HC100: 0x14D64
DSI13_HC101: 0x14D65	DSI13_HC102: 0x14D66	DSI13_HC103: 0x14D67
DSI13_HC104: 0x14D68	DSI13_HC105: 0x14D69	DSI13_HC106: 0x14D6A
DSI13_HC107: 0x14D6B	DSI13_HC108: 0x14D6C	DSI13_HC109: 0x14D6D
DSI13_HC110: 0x14D6E	DSI13_HC111: 0x14D6F	DSI13_HC112: 0x14D70
DSI13_HC113: 0x14D71	DSI13_HC114: 0x14D72	DSI13_HC115: 0x14D73
DSI13_HC116: 0x14D74	DSI13_HC117: 0x14D75	DSI13_HC118: 0x14D76
DSI13_HC119: 0x14D77	DSI13_HC120: 0x14D78	DSI13_HC121: 0x14D79
DSI13_HC122: 0x14D7A	DSI13_HC123: 0x14D7B	DSI13_HC124: 0x14D7C
DSI13_HC125: 0x14D7D	DSI13_HC126: 0x14D7E	DSI13_HC127: 0x14D7F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	RET							
Name	hc_byte							

DSI HC Tile Configuration

Bits	Name	Description
7:0	hc_byte[7:0]	RAM configuration for DSI channel bytes

1.3.1223 DSI[0..15]_HV_L[0..15]

HV_L

Reset: N/A

Register : Address

DSI0_HV_L0: 0x14080
DSI0_HV_L1: 0x14081
DSI0_HV_L2: 0x14082
DSI0_HV_L3: 0x14083
DSI0_HV_L4: 0x14084
DSI0_HV_L5: 0x14085
DSI0_HV_L6: 0x14086
DSI0_HV_L7: 0x14087
DSI0_HV_L8: 0x14088
DSI0_HV_L9: 0x14089
DSI0_HV_L10: 0x1408A
DSI0_HV_L11: 0x1408B
DSI0_HV_L12: 0x1408C
DSI0_HV_L13: 0x1408D
DSI0_HV_L14: 0x1408E
DSI0_HV_L15: 0x1408F
DSI1_HV_L0: 0x14180
DSI1_HV_L1: 0x14181
DSI1_HV_L2: 0x14182
DSI1_HV_L3: 0x14183
DSI1_HV_L4: 0x14184
DSI1_HV_L5: 0x14185
DSI1_HV_L6: 0x14186
DSI1_HV_L7: 0x14187
DSI1_HV_L8: 0x14188
DSI1_HV_L9: 0x14189
DSI1_HV_L10: 0x1418A
DSI1_HV_L11: 0x1418B
DSI1_HV_L12: 0x1418C
DSI1_HV_L13: 0x1418D
DSI1_HV_L14: 0x1418E
DSI1_HV_L15: 0x1418F
DSI2_HV_L0: 0x14280
DSI2_HV_L1: 0x14281
DSI2_HV_L2: 0x14282
DSI2_HV_L3: 0x14283
DSI2_HV_L4: 0x14284
DSI2_HV_L5: 0x14285
DSI2_HV_L6: 0x14286
DSI2_HV_L7: 0x14287
DSI2_HV_L8: 0x14288
DSI2_HV_L9: 0x14289
DSI2_HV_L10: 0x1428A
DSI2_HV_L11: 0x1428B
DSI2_HV_L12: 0x1428C
DSI2_HV_L13: 0x1428D
DSI2_HV_L14: 0x1428E
DSI2_HV_L15: 0x1428F
DSI3_HV_L0: 0x14380
DSI3_HV_L1: 0x14381
DSI3_HV_L2: 0x14382
DSI3_HV_L3: 0x14383
DSI3_HV_L4: 0x14384
DSI3_HV_L5: 0x14385
DSI3_HV_L6: 0x14386
DSI3_HV_L7: 0x14387
DSI3_HV_L8: 0x14388
DSI3_HV_L9: 0x14389
DSI3_HV_L10: 0x1438A
DSI3_HV_L11: 0x1438B
DSI3_HV_L12: 0x1438C
DSI3_HV_L13: 0x1438D
DSI3_HV_L14: 0x1438E
DSI3_HV_L15: 0x1438F
DSI4_HV_L0: 0x14480
DSI4_HV_L1: 0x14481

(continued)

Register : Address

DSI4_HV_L2: 0x14482
DSI4_HV_L3: 0x14483
DSI4_HV_L4: 0x14484
DSI4_HV_L5: 0x14485
DSI4_HV_L6: 0x14486
DSI4_HV_L7: 0x14487
DSI4_HV_L8: 0x14488
DSI4_HV_L9: 0x14489
DSI4_HV_L10: 0x1448A
DSI4_HV_L11: 0x1448B
DSI4_HV_L12: 0x1448C
DSI4_HV_L13: 0x1448D
DSI4_HV_L14: 0x1448E
DSI4_HV_L15: 0x1448F
DSI5_HV_L0: 0x14580
DSI5_HV_L1: 0x14581
DSI5_HV_L2: 0x14582
DSI5_HV_L3: 0x14583
DSI5_HV_L4: 0x14584
DSI5_HV_L5: 0x14585
DSI5_HV_L6: 0x14586
DSI5_HV_L7: 0x14587
DSI5_HV_L8: 0x14588
DSI5_HV_L9: 0x14589
DSI5_HV_L10: 0x1458A
DSI5_HV_L11: 0x1458B
DSI5_HV_L12: 0x1458C
DSI5_HV_L13: 0x1458D
DSI5_HV_L14: 0x1458E
DSI5_HV_L15: 0x1458F
DSI6_HV_L0: 0x14680
DSI6_HV_L1: 0x14681
DSI6_HV_L2: 0x14682
DSI6_HV_L3: 0x14683
DSI6_HV_L4: 0x14684
DSI6_HV_L5: 0x14685
DSI6_HV_L6: 0x14686
DSI6_HV_L7: 0x14687
DSI6_HV_L8: 0x14688
DSI6_HV_L9: 0x14689
DSI6_HV_L10: 0x1468A
DSI6_HV_L11: 0x1468B
DSI6_HV_L12: 0x1468C
DSI6_HV_L13: 0x1468D
DSI6_HV_L14: 0x1468E
DSI6_HV_L15: 0x1468F
DSI7_HV_L0: 0x14780
DSI7_HV_L1: 0x14781
DSI7_HV_L2: 0x14782
DSI7_HV_L3: 0x14783
DSI7_HV_L4: 0x14784
DSI7_HV_L5: 0x14785
DSI7_HV_L6: 0x14786
DSI7_HV_L7: 0x14787
DSI7_HV_L8: 0x14788
DSI7_HV_L9: 0x14789
DSI7_HV_L10: 0x1478A
DSI7_HV_L11: 0x1478B
DSI7_HV_L12: 0x1478C
DSI7_HV_L13: 0x1478D
DSI7_HV_L14: 0x1478E
DSI7_HV_L15: 0x1478F
DSI8_HV_L0: 0x14880
DSI8_HV_L1: 0x14881
DSI8_HV_L2: 0x14882
DSI8_HV_L3: 0x14883
DSI8_HV_L4: 0x14884
DSI8_HV_L5: 0x14885
DSI8_HV_L6: 0x14886
DSI8_HV_L7: 0x14887
DSI8_HV_L8: 0x14888
DSI8_HV_L9: 0x14889

(continued)

Register : Address

DSI8_HV_L10: 0x1488A
DSI8_HV_L11: 0x1488B
DSI8_HV_L12: 0x1488C
DSI8_HV_L13: 0x1488D
DSI8_HV_L14: 0x1488E
DSI8_HV_L15: 0x1488F
DSI9_HV_L0: 0x14980
DSI9_HV_L1: 0x14981
DSI9_HV_L2: 0x14982
DSI9_HV_L3: 0x14983
DSI9_HV_L4: 0x14984
DSI9_HV_L5: 0x14985
DSI9_HV_L6: 0x14986
DSI9_HV_L7: 0x14987
DSI9_HV_L8: 0x14988
DSI9_HV_L9: 0x14989
DSI9_HV_L10: 0x1498A
DSI9_HV_L11: 0x1498B
DSI9_HV_L12: 0x1498C
DSI9_HV_L13: 0x1498D
DSI9_HV_L14: 0x1498E
DSI9_HV_L15: 0x1498F
DSI12_HV_L0: 0x14C80
DSI12_HV_L1: 0x14C81
DSI12_HV_L2: 0x14C82
DSI12_HV_L3: 0x14C83
DSI12_HV_L4: 0x14C84
DSI12_HV_L5: 0x14C85
DSI12_HV_L6: 0x14C86
DSI12_HV_L7: 0x14C87
DSI12_HV_L8: 0x14C88
DSI12_HV_L9: 0x14C89
DSI12_HV_L10: 0x14C8A
DSI12_HV_L11: 0x14C8B
DSI12_HV_L12: 0x14C8C
DSI12_HV_L13: 0x14C8D
DSI12_HV_L14: 0x14C8E
DSI12_HV_L15: 0x14C8F
DSI13_HV_L0: 0x14D80
DSI13_HV_L1: 0x14D81
DSI13_HV_L2: 0x14D82
DSI13_HV_L3: 0x14D83
DSI13_HV_L4: 0x14D84
DSI13_HV_L5: 0x14D85
DSI13_HV_L6: 0x14D86
DSI13_HV_L7: 0x14D87
DSI13_HV_L8: 0x14D88
DSI13_HV_L9: 0x14D89
DSI13_HV_L10: 0x14D8A
DSI13_HV_L11: 0x14D8B
DSI13_HV_L12: 0x14D8C
DSI13_HV_L13: 0x14D8D
DSI13_HV_L14: 0x14D8E
DSI13_HV_L15: 0x14D8F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	RET							
Name	hv_byte							

DSI HV Tile Configuration

Bits	Name	Description
7:0	hv_byte[7:0]	RAM configuration for DSI channel bytes

1.3.1224 DSI[0..15]_HS[0..23]

HS

Reset: N/A

Register : Address

DSI0_HS0: 0x14090
DSI0_HS1: 0x14091
DSI0_HS2: 0x14092
DSI0_HS3: 0x14093
DSI0_HS4: 0x14094
DSI0_HS5: 0x14095
DSI0_HS6: 0x14096
DSI0_HS7: 0x14097
DSI0_HS8: 0x14098
DSI0_HS9: 0x14099
DSI0_HS10: 0x1409A
DSI0_HS11: 0x1409B
DSI0_HS12: 0x1409C
DSI0_HS13: 0x1409D
DSI0_HS14: 0x1409E
DSI0_HS15: 0x1409F
DSI0_HS16: 0x140A0
DSI0_HS17: 0x140A1
DSI0_HS18: 0x140A2
DSI0_HS19: 0x140A3
DSI0_HS20: 0x140A4
DSI0_HS21: 0x140A5
DSI0_HS22: 0x140A6
DSI0_HS23: 0x140A7
DSI1_HS0: 0x14190
DSI1_HS1: 0x14191
DSI1_HS2: 0x14192
DSI1_HS3: 0x14193
DSI1_HS4: 0x14194
DSI1_HS5: 0x14195
DSI1_HS6: 0x14196
DSI1_HS7: 0x14197
DSI1_HS8: 0x14198
DSI1_HS9: 0x14199
DSI1_HS10: 0x1419A
DSI1_HS11: 0x1419B
DSI1_HS12: 0x1419C
DSI1_HS13: 0x1419D
DSI1_HS14: 0x1419E
DSI1_HS15: 0x1419F
DSI1_HS16: 0x141A0
DSI1_HS17: 0x141A1
DSI1_HS18: 0x141A2
DSI1_HS19: 0x141A3
DSI1_HS20: 0x141A4
DSI1_HS21: 0x141A5
DSI1_HS22: 0x141A6
DSI1_HS23: 0x141A7
DSI2_HS0: 0x14290
DSI2_HS1: 0x14291
DSI2_HS2: 0x14292
DSI2_HS3: 0x14293
DSI2_HS4: 0x14294
DSI2_HS5: 0x14295
DSI2_HS6: 0x14296
DSI2_HS7: 0x14297
DSI2_HS8: 0x14298
DSI2_HS9: 0x14299
DSI2_HS10: 0x1429A
DSI2_HS11: 0x1429B
DSI2_HS12: 0x1429C
DSI2_HS13: 0x1429D
DSI2_HS14: 0x1429E
DSI2_HS15: 0x1429F
DSI2_HS16: 0x142A0
DSI2_HS17: 0x142A1
DSI2_HS18: 0x142A2
DSI2_HS19: 0x142A3
DSI2_HS20: 0x142A4
DSI2_HS21: 0x142A5
DSI2_HS22: 0x142A6
DSI2_HS23: 0x142A7
DSI3_HS0: 0x14390
DSI3_HS1: 0x14391
DSI3_HS2: 0x14392
DSI3_HS3: 0x14393
DSI3_HS4: 0x14394
DSI3_HS5: 0x14395
DSI3_HS6: 0x14396
DSI3_HS7: 0x14397
DSI3_HS8: 0x14398
DSI3_HS9: 0x14399
DSI3_HS10: 0x1439A
DSI3_HS11: 0x1439B
DSI3_HS12: 0x1439C
DSI3_HS13: 0x1439D
DSI3_HS14: 0x1439E
DSI3_HS15: 0x1439F
DSI3_HS16: 0x143A0
DSI3_HS17: 0x143A1
DSI3_HS18: 0x143A2
DSI3_HS19: 0x143A3
DSI3_HS20: 0x143A4
DSI3_HS21: 0x143A5
DSI3_HS22: 0x143A6
DSI3_HS23: 0x143A7
DSI4_HS0: 0x14490
DSI4_HS1: 0x14491
DSI4_HS2: 0x14492

(continued)

Register : Address		
DSI4_HS3: 0x14493	DSI4_HS4: 0x14494	DSI4_HS5: 0x14495
DSI4_HS6: 0x14496	DSI4_HS7: 0x14497	DSI4_HS8: 0x14498
DSI4_HS9: 0x14499	DSI4_HS10: 0x1449A	DSI4_HS11: 0x1449B
DSI4_HS12: 0x1449C	DSI4_HS13: 0x1449D	DSI4_HS14: 0x1449E
DSI4_HS15: 0x1449F	DSI4_HS16: 0x144A0	DSI4_HS17: 0x144A1
DSI4_HS18: 0x144A2	DSI4_HS19: 0x144A3	DSI4_HS20: 0x144A4
DSI4_HS21: 0x144A5	DSI4_HS22: 0x144A6	DSI4_HS23: 0x144A7
DSI5_HS0: 0x14590	DSI5_HS1: 0x14591	DSI5_HS2: 0x14592
DSI5_HS3: 0x14593	DSI5_HS4: 0x14594	DSI5_HS5: 0x14595
DSI5_HS6: 0x14596	DSI5_HS7: 0x14597	DSI5_HS8: 0x14598
DSI5_HS9: 0x14599	DSI5_HS10: 0x1459A	DSI5_HS11: 0x1459B
DSI5_HS12: 0x1459C	DSI5_HS13: 0x1459D	DSI5_HS14: 0x1459E
DSI5_HS15: 0x1459F	DSI5_HS16: 0x145A0	DSI5_HS17: 0x145A1
DSI5_HS18: 0x145A2	DSI5_HS19: 0x145A3	DSI5_HS20: 0x145A4
DSI5_HS21: 0x145A5	DSI5_HS22: 0x145A6	DSI5_HS23: 0x145A7
DSI6_HS0: 0x14690	DSI6_HS1: 0x14691	DSI6_HS2: 0x14692
DSI6_HS3: 0x14693	DSI6_HS4: 0x14694	DSI6_HS5: 0x14695
DSI6_HS6: 0x14696	DSI6_HS7: 0x14697	DSI6_HS8: 0x14698
DSI6_HS9: 0x14699	DSI6_HS10: 0x1469A	DSI6_HS11: 0x1469B
DSI6_HS12: 0x1469C	DSI6_HS13: 0x1469D	DSI6_HS14: 0x1469E
DSI6_HS15: 0x1469F	DSI6_HS16: 0x146A0	DSI6_HS17: 0x146A1
DSI6_HS18: 0x146A2	DSI6_HS19: 0x146A3	DSI6_HS20: 0x146A4
DSI6_HS21: 0x146A5	DSI6_HS22: 0x146A6	DSI6_HS23: 0x146A7
DSI7_HS0: 0x14790	DSI7_HS1: 0x14791	DSI7_HS2: 0x14792
DSI7_HS3: 0x14793	DSI7_HS4: 0x14794	DSI7_HS5: 0x14795
DSI7_HS6: 0x14796	DSI7_HS7: 0x14797	DSI7_HS8: 0x14798
DSI7_HS9: 0x14799	DSI7_HS10: 0x1479A	DSI7_HS11: 0x1479B
DSI7_HS12: 0x1479C	DSI7_HS13: 0x1479D	DSI7_HS14: 0x1479E
DSI7_HS15: 0x1479F	DSI7_HS16: 0x147A0	DSI7_HS17: 0x147A1
DSI7_HS18: 0x147A2	DSI7_HS19: 0x147A3	DSI7_HS20: 0x147A4
DSI7_HS21: 0x147A5	DSI7_HS22: 0x147A6	DSI7_HS23: 0x147A7
DSI8_HS0: 0x14890	DSI8_HS1: 0x14891	DSI8_HS2: 0x14892
DSI8_HS3: 0x14893	DSI8_HS4: 0x14894	DSI8_HS5: 0x14895
DSI8_HS6: 0x14896	DSI8_HS7: 0x14897	DSI8_HS8: 0x14898
DSI8_HS9: 0x14899	DSI8_HS10: 0x1489A	DSI8_HS11: 0x1489B
DSI8_HS12: 0x1489C	DSI8_HS13: 0x1489D	DSI8_HS14: 0x1489E

(continued)

Register : Address		
DSI8_HS15: 0x1489F	DSI8_HS16: 0x148A0	DSI8_HS17: 0x148A1
DSI8_HS18: 0x148A2	DSI8_HS19: 0x148A3	DSI8_HS20: 0x148A4
DSI8_HS21: 0x148A5	DSI8_HS22: 0x148A6	DSI8_HS23: 0x148A7
DSI9_HS0: 0x14990	DSI9_HS1: 0x14991	DSI9_HS2: 0x14992
DSI9_HS3: 0x14993	DSI9_HS4: 0x14994	DSI9_HS5: 0x14995
DSI9_HS6: 0x14996	DSI9_HS7: 0x14997	DSI9_HS8: 0x14998
DSI9_HS9: 0x14999	DSI9_HS10: 0x1499A	DSI9_HS11: 0x1499B
DSI9_HS12: 0x1499C	DSI9_HS13: 0x1499D	DSI9_HS14: 0x1499E
DSI9_HS15: 0x1499F	DSI9_HS16: 0x149A0	DSI9_HS17: 0x149A1
DSI9_HS18: 0x149A2	DSI9_HS19: 0x149A3	DSI9_HS20: 0x149A4
DSI9_HS21: 0x149A5	DSI9_HS22: 0x149A6	DSI9_HS23: 0x149A7
DSI12_HS0: 0x14C90	DSI12_HS1: 0x14C91	DSI12_HS2: 0x14C92
DSI12_HS3: 0x14C93	DSI12_HS4: 0x14C94	DSI12_HS5: 0x14C95
DSI12_HS6: 0x14C96	DSI12_HS7: 0x14C97	DSI12_HS8: 0x14C98
DSI12_HS9: 0x14C99	DSI12_HS10: 0x14C9A	DSI12_HS11: 0x14C9B
DSI12_HS12: 0x14C9C	DSI12_HS13: 0x14C9D	DSI12_HS14: 0x14C9E
DSI12_HS15: 0x14C9F	DSI12_HS16: 0x14CA0	DSI12_HS17: 0x14CA1
DSI12_HS18: 0x14CA2	DSI12_HS19: 0x14CA3	DSI12_HS20: 0x14CA4
DSI12_HS21: 0x14CA5	DSI12_HS22: 0x14CA6	DSI12_HS23: 0x14CA7
DSI13_HS0: 0x14D90	DSI13_HS1: 0x14D91	DSI13_HS2: 0x14D92
DSI13_HS3: 0x14D93	DSI13_HS4: 0x14D94	DSI13_HS5: 0x14D95
DSI13_HS6: 0x14D96	DSI13_HS7: 0x14D97	DSI13_HS8: 0x14D98
DSI13_HS9: 0x14D99	DSI13_HS10: 0x14D9A	DSI13_HS11: 0x14D9B
DSI13_HS12: 0x14D9C	DSI13_HS13: 0x14D9D	DSI13_HS14: 0x14D9E
DSI13_HS15: 0x14D9F	DSI13_HS16: 0x14DA0	DSI13_HS17: 0x14DA1
DSI13_HS18: 0x14DA2	DSI13_HS19: 0x14DA3	DSI13_HS20: 0x14DA4
DSI13_HS21: 0x14DA5	DSI13_HS22: 0x14DA6	DSI13_HS23: 0x14DA7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	RET							
Name	hs_byte							

DSI HS Tile Configuration

Bits	Name	Description
7:0	hs_byte[7:0]	RAM configuration for DSI channel bytes

1.3.1225 DSI[0..15]_HV_R[0..15]

HV_R

Reset: N/A

Register : Address

DSI0_HV_R0: 0x140A8
DSI0_HV_R1: 0x140A9
DSI0_HV_R2: 0x140AA
DSI0_HV_R3: 0x140AB
DSI0_HV_R4: 0x140AC
DSI0_HV_R5: 0x140AD
DSI0_HV_R6: 0x140AE
DSI0_HV_R7: 0x140AF
DSI0_HV_R8: 0x140B0
DSI0_HV_R9: 0x140B1
DSI0_HV_R10: 0x140B2
DSI0_HV_R11: 0x140B3
DSI0_HV_R12: 0x140B4
DSI0_HV_R13: 0x140B5
DSI0_HV_R14: 0x140B6
DSI0_HV_R15: 0x140B7
DSI1_HV_R0: 0x141A8
DSI1_HV_R1: 0x141A9
DSI1_HV_R2: 0x141AA
DSI1_HV_R3: 0x141AB
DSI1_HV_R4: 0x141AC
DSI1_HV_R5: 0x141AD
DSI1_HV_R6: 0x141AE
DSI1_HV_R7: 0x141AF
DSI1_HV_R8: 0x141B0
DSI1_HV_R9: 0x141B1
DSI1_HV_R10: 0x141B2
DSI1_HV_R11: 0x141B3
DSI1_HV_R12: 0x141B4
DSI1_HV_R13: 0x141B5
DSI1_HV_R14: 0x141B6
DSI1_HV_R15: 0x141B7
DSI2_HV_R0: 0x142A8
DSI2_HV_R1: 0x142A9
DSI2_HV_R2: 0x142AA
DSI2_HV_R3: 0x142AB
DSI2_HV_R4: 0x142AC
DSI2_HV_R5: 0x142AD
DSI2_HV_R6: 0x142AE
DSI2_HV_R7: 0x142AF
DSI2_HV_R8: 0x142B0
DSI2_HV_R9: 0x142B1
DSI2_HV_R10: 0x142B2
DSI2_HV_R11: 0x142B3
DSI2_HV_R12: 0x142B4
DSI2_HV_R13: 0x142B5
DSI2_HV_R14: 0x142B6
DSI2_HV_R15: 0x142B7
DSI3_HV_R0: 0x143A8
DSI3_HV_R1: 0x143A9
DSI3_HV_R2: 0x143AA
DSI3_HV_R3: 0x143AB
DSI3_HV_R4: 0x143AC
DSI3_HV_R5: 0x143AD
DSI3_HV_R6: 0x143AE
DSI3_HV_R7: 0x143AF
DSI3_HV_R8: 0x143B0
DSI3_HV_R9: 0x143B1
DSI3_HV_R10: 0x143B2
DSI3_HV_R11: 0x143B3
DSI3_HV_R12: 0x143B4
DSI3_HV_R13: 0x143B5
DSI3_HV_R14: 0x143B6
DSI3_HV_R15: 0x143B7
DSI4_HV_R0: 0x144A8
DSI4_HV_R1: 0x144A9

(continued)

Register : Address	
DSI4_HV_R2: 0x144AA	DSI4_HV_R3: 0x144AB
DSI4_HV_R4: 0x144AC	DSI4_HV_R5: 0x144AD
DSI4_HV_R6: 0x144AE	DSI4_HV_R7: 0x144AF
DSI4_HV_R8: 0x144B0	DSI4_HV_R9: 0x144B1
DSI4_HV_R10: 0x144B2	DSI4_HV_R11: 0x144B3
DSI4_HV_R12: 0x144B4	DSI4_HV_R13: 0x144B5
DSI4_HV_R14: 0x144B6	DSI4_HV_R15: 0x144B7
DSI5_HV_R0: 0x145A8	DSI5_HV_R1: 0x145A9
DSI5_HV_R2: 0x145AA	DSI5_HV_R3: 0x145AB
DSI5_HV_R4: 0x145AC	DSI5_HV_R5: 0x145AD
DSI5_HV_R6: 0x145AE	DSI5_HV_R7: 0x145AF
DSI5_HV_R8: 0x145B0	DSI5_HV_R9: 0x145B1
DSI5_HV_R10: 0x145B2	DSI5_HV_R11: 0x145B3
DSI5_HV_R12: 0x145B4	DSI5_HV_R13: 0x145B5
DSI5_HV_R14: 0x145B6	DSI5_HV_R15: 0x145B7
DSI6_HV_R0: 0x146A8	DSI6_HV_R1: 0x146A9
DSI6_HV_R2: 0x146AA	DSI6_HV_R3: 0x146AB
DSI6_HV_R4: 0x146AC	DSI6_HV_R5: 0x146AD
DSI6_HV_R6: 0x146AE	DSI6_HV_R7: 0x146AF
DSI6_HV_R8: 0x146B0	DSI6_HV_R9: 0x146B1
DSI6_HV_R10: 0x146B2	DSI6_HV_R11: 0x146B3
DSI6_HV_R12: 0x146B4	DSI6_HV_R13: 0x146B5
DSI6_HV_R14: 0x146B6	DSI6_HV_R15: 0x146B7
DSI7_HV_R0: 0x147A8	DSI7_HV_R1: 0x147A9
DSI7_HV_R2: 0x147AA	DSI7_HV_R3: 0x147AB
DSI7_HV_R4: 0x147AC	DSI7_HV_R5: 0x147AD
DSI7_HV_R6: 0x147AE	DSI7_HV_R7: 0x147AF
DSI7_HV_R8: 0x147B0	DSI7_HV_R9: 0x147B1
DSI7_HV_R10: 0x147B2	DSI7_HV_R11: 0x147B3
DSI7_HV_R12: 0x147B4	DSI7_HV_R13: 0x147B5
DSI7_HV_R14: 0x147B6	DSI7_HV_R15: 0x147B7
DSI8_HV_R0: 0x148A8	DSI8_HV_R1: 0x148A9
DSI8_HV_R2: 0x148AA	DSI8_HV_R3: 0x148AB
DSI8_HV_R4: 0x148AC	DSI8_HV_R5: 0x148AD
DSI8_HV_R6: 0x148AE	DSI8_HV_R7: 0x148AF
DSI8_HV_R8: 0x148B0	DSI8_HV_R9: 0x148B1

(continued)

Register : Address

DSI8_HV_R10: 0x148B2
DSI8_HV_R11: 0x148B3
DSI8_HV_R12: 0x148B4
DSI8_HV_R13: 0x148B5
DSI8_HV_R14: 0x148B6
DSI8_HV_R15: 0x148B7
DSI9_HV_R0: 0x149A8
DSI9_HV_R1: 0x149A9
DSI9_HV_R2: 0x149AA
DSI9_HV_R3: 0x149AB
DSI9_HV_R4: 0x149AC
DSI9_HV_R5: 0x149AD
DSI9_HV_R6: 0x149AE
DSI9_HV_R7: 0x149AF
DSI9_HV_R8: 0x149B0
DSI9_HV_R9: 0x149B1
DSI9_HV_R10: 0x149B2
DSI9_HV_R11: 0x149B3
DSI9_HV_R12: 0x149B4
DSI9_HV_R13: 0x149B5
DSI9_HV_R14: 0x149B6
DSI9_HV_R15: 0x149B7
DSI12_HV_R0: 0x14CA8
DSI12_HV_R1: 0x14CA9
DSI12_HV_R2: 0x14CAA
DSI12_HV_R3: 0x14CAB
DSI12_HV_R4: 0x14CAC
DSI12_HV_R5: 0x14CAD
DSI12_HV_R6: 0x14CAE
DSI12_HV_R7: 0x14CAF
DSI12_HV_R8: 0x14CB0
DSI12_HV_R9: 0x14CB1
DSI12_HV_R10: 0x14CB2
DSI12_HV_R11: 0x14CB3
DSI12_HV_R12: 0x14CB4
DSI12_HV_R13: 0x14CB5
DSI12_HV_R14: 0x14CB6
DSI12_HV_R15: 0x14CB7
DSI13_HV_R0: 0x14DA8
DSI13_HV_R1: 0x14DA9
DSI13_HV_R2: 0x14DAA
DSI13_HV_R3: 0x14DAB
DSI13_HV_R4: 0x14DAC
DSI13_HV_R5: 0x14DAD
DSI13_HV_R6: 0x14DAE
DSI13_HV_R7: 0x14DAF
DSI13_HV_R8: 0x14DB0
DSI13_HV_R9: 0x14DB1
DSI13_HV_R10: 0x14DB2
DSI13_HV_R11: 0x14DB3
DSI13_HV_R12: 0x14DB4
DSI13_HV_R13: 0x14DB5
DSI13_HV_R14: 0x14DB6
DSI13_HV_R15: 0x14DB7

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R							
Retention	RET							
Name	hv_byte							

DSI HV Tile Configuration

Bits	Name	Description
7:0	hv_byte[7:0]	RAM configuration for DSI channel bytes

1.3.1226 DSI[0..15]_DSIINP0

DSIINP0

Reset: N/A

Register : Address

DSI0_DSIINP0: 0x140C0 | DSI1_DSIINP0: 0x141C0

DSI2_DSIINP0: 0x142C0 | DSI3_DSIINP0: 0x143C0

DSI4_DSIINP0: 0x144C0 | DSI5_DSIINP0: 0x145C0

DSI6_DSIINP0: 0x146C0 | DSI7_DSIINP0: 0x147C0

DSI8_DSIINP0: 0x148C0 | DSI9_DSIINP0: 0x149C0

DSI12_DSIINP0: 0x14CC0 | DSI13_DSIINP0: 0x14DC0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	pi_bot				pi_top			

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks
3:0	pi_top[3:0]	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks

1.3.1227 DSI[0..15]_DSIINP1

DSIINP1

Reset: N/A

Register : Address

DSI0_DSIINP1: 0x140C2
DSI1_DSIINP1: 0x141C2
DSI2_DSIINP1: 0x142C2
DSI3_DSIINP1: 0x143C2
DSI4_DSIINP1: 0x144C2
DSI5_DSIINP1: 0x145C2
DSI6_DSIINP1: 0x146C2
DSI7_DSIINP1: 0x147C2
DSI8_DSIINP1: 0x148C2
DSI9_DSIINP1: 0x149C2
DSI12_DSIINP1: 0x14CC2
DSI13_DSIINP1: 0x14DC2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	pi_bot				pi_top			

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks
3:0	pi_top[3:0]	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks

1.3.1228 DSI[0..15]_DSIINP2

DSIINP2

Reset: N/A

Register : Address

DSI0_DSIINP2: 0x140C4
DSI1_DSIINP2: 0x141C4
DSI2_DSIINP2: 0x142C4
DSI3_DSIINP2: 0x143C4
DSI4_DSIINP2: 0x144C4
DSI5_DSIINP2: 0x145C4
DSI6_DSIINP2: 0x146C4
DSI7_DSIINP2: 0x147C4
DSI8_DSIINP2: 0x148C4
DSI9_DSIINP2: 0x149C4
DSI12_DSIINP2: 0x14CC4
DSI13_DSIINP2: 0x14DC4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	pi_bot				pi_top			

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks
3:0	pi_top[3:0]	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks

1.3.1229 DSI[0..15]_DSIINP3

DSIINP3

Reset: N/A

Register : Address

DSI0_DSIINP3: 0x140C6

DSI1_DSIINP3: 0x141C6

DSI2_DSIINP3: 0x142C6

DSI3_DSIINP3: 0x143C6

DSI4_DSIINP3: 0x144C6

DSI5_DSIINP3: 0x145C6

DSI6_DSIINP3: 0x146C6

DSI7_DSIINP3: 0x147C6

DSI8_DSIINP3: 0x148C6

DSI9_DSIINP3: 0x149C6

DSI12_DSIINP3: 0x14CC6

DSI13_DSIINP3: 0x14DC6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	pi_bot				pi_top			

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks
3:0	pi_top[3:0]	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks

1.3.1230 DSI[0..15]_DSIINP4

DSIINP4

Reset: N/A

Register : Address

DSI0_DSIINP4: 0x140C8

DSI1_DSIINP4: 0x141C8

DSI2_DSIINP4: 0x142C8

DSI3_DSIINP4: 0x143C8

DSI4_DSIINP4: 0x144C8

DSI5_DSIINP4: 0x145C8

DSI6_DSIINP4: 0x146C8

DSI7_DSIINP4: 0x147C8

DSI8_DSIINP4: 0x148C8

DSI9_DSIINP4: 0x149C8

DSI12_DSIINP4: 0x14CC8

DSI13_DSIINP4: 0x14DC8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	pi_bot				pi_top			

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks
3:0	pi_top[3:0]	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks

1.3.1231 DSI[0..15]_DSIINP5

DSIINP5

Reset: N/A

Register : Address

DSI0_DSIINP5: 0x140CA

DSI1_DSIINP5: 0x141CA

DSI2_DSIINP5: 0x142CA

DSI3_DSIINP5: 0x143CA

DSI4_DSIINP5: 0x144CA

DSI5_DSIINP5: 0x145CA

DSI6_DSIINP5: 0x146CA

DSI7_DSIINP5: 0x147CA

DSI8_DSIINP5: 0x148CA

DSI9_DSIINP5: 0x149CA

DSI12_DSIINP5: 0x14CCA

DSI13_DSIINP5: 0x14DCA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	pi_bot				pi_top			

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks
3:0	pi_top[3:0]	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks

1.3.1232 DSI[0..15]_DSIOUTP0

DSIOUTP0

Reset: N/A

Register : Address

DSI0_DSIOUTP0: 0x140CC

DSI1_DSIOUTP0: 0x141CC

DSI2_DSIOUTP0: 0x142CC

DSI3_DSIOUTP0: 0x143CC

DSI4_DSIOUTP0: 0x144CC

DSI5_DSIOUTP0: 0x145CC

DSI6_DSIOUTP0: 0x146CC

DSI7_DSIOUTP0: 0x147CC

DSI8_DSIOUTP0: 0x148CC

DSI9_DSIOUTP0: 0x149CC

DSI12_DSIOUTP0: 0x14CCC

DSI13_DSIOUTP0: 0x14DCC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	pi_bot				pi_top			

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks
3:0	pi_top[3:0]	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks

1.3.1233 DSI[0..15]_DSIOUTP1

DSIOUTP1

Reset: N/A

Register : Address

DSI0_DSIOUTP1: 0x140CE

DSI1_DSIOUTP1: 0x141CE

DSI2_DSIOUTP1: 0x142CE

DSI3_DSIOUTP1: 0x143CE

DSI4_DSIOUTP1: 0x144CE

DSI5_DSIOUTP1: 0x145CE

DSI6_DSIOUTP1: 0x146CE

DSI7_DSIOUTP1: 0x147CE

DSI8_DSIOUTP1: 0x148CE

DSI9_DSIOUTP1: 0x149CE

DSI12_DSIOUTP1: 0x14CCE

DSI13_DSIOUTP1: 0x14DCE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	pi_bot				pi_top			

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks
3:0	pi_top[3:0]	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks

1.3.1234 DSI[0..15]_DSIOUTP2

DSIOUTP2

Reset: N/A

Register : Address

DSI0_DSIOUTP2: 0x140D0 | DSI1_DSIOUTP2: 0x141D0

DSI2_DSIOUTP2: 0x142D0 | DSI3_DSIOUTP2: 0x143D0

DSI4_DSIOUTP2: 0x144D0 | DSI5_DSIOUTP2: 0x145D0

DSI6_DSIOUTP2: 0x146D0 | DSI7_DSIOUTP2: 0x147D0

DSI8_DSIOUTP2: 0x148D0 | DSI9_DSIOUTP2: 0x149D0

DSI12_DSIOUTP2: 0x14CD0 | DSI13_DSIOUTP2: 0x14DD0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	pi_bot				pi_top			

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks
3:0	pi_top[3:0]	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks

1.3.1235 DSI[0..15]_DSIOUTP3

DSIOUTP3

Reset: N/A

Register : Address

DSI0_DSIOUTP3: 0x140D2

DSI1_DSIOUTP3: 0x141D2

DSI2_DSIOUTP3: 0x142D2

DSI3_DSIOUTP3: 0x143D2

DSI4_DSIOUTP3: 0x144D2

DSI5_DSIOUTP3: 0x145D2

DSI6_DSIOUTP3: 0x146D2

DSI7_DSIOUTP3: 0x147D2

DSI8_DSIOUTP3: 0x148D2

DSI9_DSIOUTP3: 0x149D2

DSI12_DSIOUTP3: 0x14CD2

DSI13_DSIOUTP3: 0x14DD2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	pi_bot				pi_top			

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks
3:0	pi_top[3:0]	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks

1.3.1236 DSI[0..15]_DSIOUTT0

DSIOUTT0

Reset: N/A

Register : Address

DSI0_DSIOUTT0: 0x140D4

DSI1_DSIOUTT0: 0x141D4

DSI2_DSIOUTT0: 0x142D4

DSI3_DSIOUTT0: 0x143D4

DSI4_DSIOUTT0: 0x144D4

DSI5_DSIOUTT0: 0x145D4

DSI6_DSIOUTT0: 0x146D4

DSI7_DSIOUTT0: 0x147D4

DSI8_DSIOUTT0: 0x148D4

DSI9_DSIOUTT0: 0x149D4

DSI12_DSIOUTT0: 0x14CD4

DSI13_DSIOUTT0: 0x14DD4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	pi_bot				pi_top			

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks
3:0	pi_top[3:0]	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks

1.3.1237 DSI[0..15]_DSIOUTT1

DSIOUTT1

Reset: N/A

Register : Address

DSI0_DSIOUTT1: 0x140D6

DSI1_DSIOUTT1: 0x141D6

DSI2_DSIOUTT1: 0x142D6

DSI3_DSIOUTT1: 0x143D6

DSI4_DSIOUTT1: 0x144D6

DSI5_DSIOUTT1: 0x145D6

DSI6_DSIOUTT1: 0x146D6

DSI7_DSIOUTT1: 0x147D6

DSI8_DSIOUTT1: 0x148D6

DSI9_DSIOUTT1: 0x149D6

DSI12_DSIOUTT1: 0x14CD6

DSI13_DSIOUTT1: 0x14DD6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	pi_bot				pi_top			

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks
3:0	pi_top[3:0]	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks

1.3.1238 DSI[0..15]_DSIOUTT2

DSIOUTT2

Reset: N/A

Register : Address

DSI0_DSIOUTT2: 0x140D8

DSI1_DSIOUTT2: 0x141D8

DSI2_DSIOUTT2: 0x142D8

DSI3_DSIOUTT2: 0x143D8

DSI4_DSIOUTT2: 0x144D8

DSI5_DSIOUTT2: 0x145D8

DSI6_DSIOUTT2: 0x146D8

DSI7_DSIOUTT2: 0x147D8

DSI8_DSIOUTT2: 0x148D8

DSI9_DSIOUTT2: 0x149D8

DSI12_DSIOUTT2: 0x14CD8

DSI13_DSIOUTT2: 0x14DD8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	pi_bot				pi_top			

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks
3:0	pi_top[3:0]	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks

1.3.1239 DSI[0..15]_DSIOUTT3

DSIOUTT3

Reset: N/A

Register : Address

DSI0_DSIOUTT3: 0x140DA

DSI1_DSIOUTT3: 0x141DA

DSI2_DSIOUTT3: 0x142DA

DSI3_DSIOUTT3: 0x143DA

DSI4_DSIOUTT3: 0x144DA

DSI5_DSIOUTT3: 0x145DA

DSI6_DSIOUTT3: 0x146DA

DSI7_DSIOUTT3: 0x147DA

DSI8_DSIOUTT3: 0x148DA

DSI9_DSIOUTT3: 0x149DA

DSI12_DSIOUTT3: 0x14CDA

DSI13_DSIOUTT3: 0x14DDA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	pi_bot				pi_top			

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks
3:0	pi_top[3:0]	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks

1.3.1240 DSI[0..15]_DSIOUTT4

DSIOUTT4

Reset: N/A

Register : Address

DSI0_DSIOUTT4: 0x140DC

DSI1_DSIOUTT4: 0x141DC

DSI2_DSIOUTT4: 0x142DC

DSI3_DSIOUTT4: 0x143DC

DSI4_DSIOUTT4: 0x144DC

DSI5_DSIOUTT4: 0x145DC

DSI6_DSIOUTT4: 0x146DC

DSI7_DSIOUTT4: 0x147DC

DSI8_DSIOUTT4: 0x148DC

DSI9_DSIOUTT4: 0x149DC

DSI12_DSIOUTT4: 0x14CDC

DSI13_DSIOUTT4: 0x14DDC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	pi_bot				pi_top			

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks
3:0	pi_top[3:0]	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks

1.3.1241 DSI[0..15]_DSIOUTT5

DSIOUTT5

Reset: N/A

Register : Address

DSI0_DSIOUTT5: 0x140DE

DSI1_DSIOUTT5: 0x141DE

DSI2_DSIOUTT5: 0x142DE

DSI3_DSIOUTT5: 0x143DE

DSI4_DSIOUTT5: 0x144DE

DSI5_DSIOUTT5: 0x145DE

DSI6_DSIOUTT5: 0x146DE

DSI7_DSIOUTT5: 0x147DE

DSI8_DSIOUTT5: 0x148DE

DSI9_DSIOUTT5: 0x149DE

DSI12_DSIOUTT5: 0x14CDE

DSI13_DSIOUTT5: 0x14DDE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	pi_bot				pi_top			

DSI PI Tile Configuration for DSI I/O. Top DSI block only contains the least significant nibble (pi_top[3:0]) and bottom DSI blocks only contains the most significant nibble (pi_bot[7:4]).

Bits	Name	Description
7:4	pi_bot[3:0]	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks
3:0	pi_top[3:0]	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks

1.3.1242 DSI[0..15]_VS0

VS0

Reset: N/A

Register : Address

DSI0_VS0: 0x140E0 DSI1_VS0: 0x141E0 DSI2_VS0: 0x142E0

DSI3_VS0: 0x143E0 DSI4_VS0: 0x144E0 DSI5_VS0: 0x145E0

DSI6_VS0: 0x146E0 DSI7_VS0: 0x147E0 DSI8_VS0: 0x148E0

DSI9_VS0: 0x149E0 DSI12_VS0: 0x14CE0 DSI13_VS0: 0x14DE0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	vs_bot				vs_top			

DSI VS Tile Configuration. Top DSI block only contains the least significant nibble (vs_top[3:0]) and bottom DSI blocks only contains the most significant nibble (vs_bot[7:4]).

Bits	Name	Description
7:4	vs_bot[3:0]	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks
3:0	vs_top[3:0]	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks

1.3.1243 DSI[0..15]_VS1

VS1

Reset: N/A

Register : Address

DSI0_VS1: 0x140E2 DSI1_VS1: 0x141E2 DSI2_VS1: 0x142E2

DSI3_VS1: 0x143E2 DSI4_VS1: 0x144E2 DSI5_VS1: 0x145E2

DSI6_VS1: 0x146E2 DSI7_VS1: 0x147E2 DSI8_VS1: 0x148E2

DSI9_VS1: 0x149E2 DSI12_VS1: 0x14CE2 DSI13_VS1: 0x14DE2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	vs_bot				vs_top			

DSI VS Tile Configuration. Top DSI block only contains the least significant nibble (vs_top[3:0]) and bottom DSI blocks only contains the most significant nibble (vs_bot[7:4]).

Bits	Name	Description
7:4	vs_bot[3:0]	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks
3:0	vs_top[3:0]	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks

1.3.1244 DSI[0..15]_VS2

VS2

Reset: N/A

Register : Address

DSI0_VS2: 0x140E4 DSI1_VS2: 0x141E4 DSI2_VS2: 0x142E4

DSI3_VS2: 0x143E4 DSI4_VS2: 0x144E4 DSI5_VS2: 0x145E4

DSI6_VS2: 0x146E4 DSI7_VS2: 0x147E4 DSI8_VS2: 0x148E4

DSI9_VS2: 0x149E4 DSI12_VS2: 0x14CE4 DSI13_VS2: 0x14DE4

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	vs_bot				vs_top			

DSI VS Tile Configuration. Top DSI block only contains the least significant nibble (vs_top[3:0]) and bottom DSI blocks only contains the most significant nibble (vs_bot[7:4]).

Bits	Name	Description
7:4	vs_bot[3:0]	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks
3:0	vs_top[3:0]	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks

1.3.1245 DSI[0..15]_VS3

VS3

Reset: N/A

Register : Address

DSI0_VS3: 0x140E6 DSI1_VS3: 0x141E6 DSI2_VS3: 0x142E6

DSI3_VS3: 0x143E6 DSI4_VS3: 0x144E6 DSI5_VS3: 0x145E6

DSI6_VS3: 0x146E6 DSI7_VS3: 0x147E6 DSI8_VS3: 0x148E6

DSI9_VS3: 0x149E6 DSI12_VS3: 0x14CE6 DSI13_VS3: 0x14DE6

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	vs_bot				vs_top			

DSI VS Tile Configuration. Top DSI block only contains the least significant nibble (vs_top[3:0]) and bottom DSI blocks only contains the most significant nibble (vs_bot[7:4]).

Bits	Name	Description
7:4	vs_bot[3:0]	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks
3:0	vs_top[3:0]	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks

1.3.1246 DSI[0..15]_VS4

VS4

Reset: N/A

Register : Address

DSI0_VS4: 0x140E8 DSI1_VS4: 0x141E8 DSI2_VS4: 0x142E8

DSI3_VS4: 0x143E8 DSI4_VS4: 0x144E8 DSI5_VS4: 0x145E8

DSI6_VS4: 0x146E8 DSI7_VS4: 0x147E8 DSI8_VS4: 0x148E8

DSI9_VS4: 0x149E8 DSI12_VS4: 0x14CE8 DSI13_VS4: 0x14DE8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	vs_bot				vs_top			

DSI VS Tile Configuration. Top DSI block only contains the least significant nibble (vs_top[3:0]) and bottom DSI blocks only contains the most significant nibble (vs_bot[7:4]).

Bits	Name	Description
7:4	vs_bot[3:0]	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks
3:0	vs_top[3:0]	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks

1.3.1247 DSI[0..15]_VS5

VS5

Reset: N/A

Register : Address

DSI0_VS5: 0x140EA | DSI1_VS5: 0x141EA | DSI2_VS5: 0x142EA

DSI3_VS5: 0x143EA | DSI4_VS5: 0x144EA | DSI5_VS5: 0x145EA

DSI6_VS5: 0x146EA | DSI7_VS5: 0x147EA | DSI8_VS5: 0x148EA

DSI9_VS5: 0x149EA | DSI12_VS5: 0x14CEA | DSI13_VS5: 0x14DEA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	vs_bot				vs_top			

DSI VS Tile Configuration. Top DSI block only contains the least significant nibble (vs_top[3:0]) and bottom DSI blocks only contains the most significant nibble (vs_bot[7:4]).

Bits	Name	Description
7:4	vs_bot[3:0]	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks
3:0	vs_top[3:0]	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks

1.3.1248 DSI[0..15]_VS6

VS6

Reset: N/A

Register : Address

DSI0_VS6: 0x140EC | DSI1_VS6: 0x141EC | DSI2_VS6: 0x142EC

DSI3_VS6: 0x143EC | DSI4_VS6: 0x144EC | DSI5_VS6: 0x145EC

DSI6_VS6: 0x146EC | DSI7_VS6: 0x147EC | DSI8_VS6: 0x148EC

DSI9_VS6: 0x149EC | DSI12_VS6: 0x14CEC | DSI13_VS6: 0x14DEC

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	vs_bot				vs_top			

DSI VS Tile Configuration. Top DSI block only contains the least significant nibble (vs_top[3:0]) and bottom DSI blocks only contains the most significant nibble (vs_bot[7:4]).

Bits	Name	Description
7:4	vs_bot[3:0]	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks
3:0	vs_top[3:0]	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks

1.3.1249 DSI[0..15]_VS7

VS7

Reset: N/A

Register : Address

DSI0_VS7: 0x140EE | DSI1_VS7: 0x141EE | DSI2_VS7: 0x142EE

DSI3_VS7: 0x143EE | DSI4_VS7: 0x144EE | DSI5_VS7: 0x145EE

DSI6_VS7: 0x146EE | DSI7_VS7: 0x147EE | DSI8_VS7: 0x148EE

DSI9_VS7: 0x149EE | DSI12_VS7: 0x14CEE | DSI13_VS7: 0x14DEE

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUU				R/W:UUUU			
HW Access	R				R			
Retention	RET				RET			
Name	vs_bot				vs_top			

DSI VS Tile Configuration. Top DSI block only contains the least significant nibble (vs_top[3:0]) and bottom DSI blocks only contains the most significant nibble (vs_bot[7:4]).

Bits	Name	Description
7:4	vs_bot[3:0]	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks
3:0	vs_top[3:0]	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks

1.3.1250 BCTL[0..3]_MDCLK_EN

MDCLK_EN

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BCTL0_MDCLK_EN: 0x15000 BCTL1_MDCLK_EN: 0x15010

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	DCEN7	DCEN6	DCEN5	DCEN4	DCEN3	DCEN2	DCEN1	DCEN0

Master Digital Global Clock Enable Register

Bits	Name	Description
7	DCEN7	Bank Clock Enable Control See Table 1-812.
6	DCEN6	Bank Clock Enable Control See Table 1-812.
5	DCEN5	Bank Clock Enable Control See Table 1-812.
4	DCEN4	Bank Clock Enable Control See Table 1-812.
3	DCEN3	Bank Clock Enable Control See Table 1-812.
2	DCEN2	Bank Clock Enable Control See Table 1-812.
1	DCEN1	Bank Clock Enable Control See Table 1-812.
0	DCEN0	Bank Clock Enable Control See Table 1-812.

Table 1-812. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	DISABLE	Digital Global clock is disabled.
1'b1	ENABLE	Digital Global clock is enabled.

1.3.1251 BCTL[0..3]_MBCLK_EN

MBCLK_EN

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BCTL0_MBCLK_EN: 0x15001 BCTL1_MBCLK_EN: 0x15011

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	NA:0	NA:0	NA:0	NA:0	NA:0	NA:0	R/W:0
HW Access	NA	NA	NA	NA	NA	NA	NA	R
Retention	NA	NA	NA	NA	NA	NA	NA	RET
Name	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	BCEN

Master Digital Global Clock Enable Register

Bits	Name	Description
0	BCEN	Bank Clock Enable Control See Table 1-814.

Table 1-813. Bit field encoding: CHAN_DRV_DIS_ENUM

Value	Name	Description
1'b0	ENABLE	Normal Operation, UDB drivers are enabled.
1'b1	DISABLE	UDB output drivers to routing are disabled.

Table 1-814. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	DISABLE	Digital Global clock is disabled.
1'b1	ENABLE	Digital Global clock is enabled.

Table 1-815. Bit field encoding: RDWR_RAM_OPT_ENUM

Value	Name	Description
1'b0	NEG_EDGE_GEN	RAM read/write signal is generated from the negative edge of bus clock. When this bit is zero single cycle configuration reads/writes are not available
1'b1	POS_EDGE_GEN	RAM read/write signal is generated from the positive edge of bus clock

Table 1-816. Bit field encoding: SA1_DSI_PD_EN_ENUM

Value	Name	Description
1'b0	DISABLE	Normal Operation, weak pulldown disabled.
1'b1	ENABLE	Weak pulldown enabled.

Table 1-817. Bit field encoding: SA1_PD_EN_ENUM

Value	Name	Description
1'b0	DISABLE	Normal Operation, weak pulldown disabled.
1'b1	ENABLE	Weak pulldown enabled.

Table 1-818. Bit field encoding: SA1_PU_EN_ENUM

Value	Name	Description
1'b0	DISABLE	Normal Operation, strong pullup disabled.
1'b1	ENABLE	Strong pullup enabled.

Table 1-819. Bit field encoding: SCAN_DRV_EN_ENUM

Value	Name	Description

(continued)

Table 1-819. Bit field encoding: SCAN_DRV_EN_ENUM

1'b0	DISABLE	Normal Operation, DSI input scan drivers are disabled. Bypass scan chain holds current data.
1'b1	ENABLE	DSI input scan drivers are enabled. Bypass scan chain will shift depending upon state of USCAN_SE.

Table 1-820. Bit field encoding: SCAN_MODE_ENUM

Value	Name	Description
1'b0	DISABLE	UDB DSI scan is used by full chip scan controller.
1'b1	ENABLE	UDB DSI scan is controlled by UDBIF interface.

1.3.1252 BCTL[0..3]_WAIT_CFG

WAIT_CFG

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BCTL0_WAIT_CFG: 0x15002 BCTL1_WAIT_CFG: 0x15012

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00		R/W:00		R/W:00		R/W:00	
HW Access	R		R		R		R	
Retention	RET		RET		RET		RET	
Name	WR_WRK_WAIT		RD_WRK_WAIT		WR_CFG_WAIT		RD_CFG_WAIT	

Wait State Configuration Register

Bits	Name	Description
7:6	WR_WRK_WAIT[1:0]	Wait States for Writing UDB Working Registers See Table 1-824.
5:4	RD_WRK_WAIT[1:0]	Wait States for Reading UDB Working Registers See Table 1-822.
3:2	WR_CFG_WAIT[1:0]	Wait States for Writing UDB Configuration See Table 1-823.
1:0	RD_CFG_WAIT[1:0]	Wait States for Reading UDB Configuration See Table 1-821.

Table 1-821. Bit field encoding: RD_CFG_WAIT_ENUM

Value	Name	Description
2'b00	FIVE_WAITS	5 wait states
2'b01	FOUR_WAITS	4 wait state
2'b10	THREE_WAITS	3 wait states
2'b11	ONE_WAITS	1 wait states

Table 1-822. Bit field encoding: RD_WRK_WAIT_ENUM

Value	Name	Description
2'b00	ONE_WAITS	1 wait states
2'b01	TWO_WAITS	2 wait state
2'b10	THREE_WAITS	3 wait states
2'b11	ZERO_WAITS	0 wait states

Table 1-823. Bit field encoding: WR_CFG_WAIT_ENUM

Value	Name	Description
2'b00	ONE_WAITS	1 wait state
2'b01	TWO_WAITS	2 wait states
2'b10	THREE_WAITS	3 wait states
2'b11	ILLEGAL	Unsupported configuration value. Use of this value will cause device to fail.

Table 1-824. Bit field encoding: WR_WRK_WAIT_ENUM

Value	Name	Description

(continued)

Table 1-824. Bit field encoding: WR_WRK_WAIT_ENUM

2'b00	ONE_WAITS	1 wait states
2'b01	TWO_WAITS	2 wait state
2'b10	THREE_WAITS	3 wait states
2'b11	ZERO_WAITS	0 wait states

1.3.1253 BCTL[0..3]_BANK_CTL

BANK_CTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BCTL0_BANK_CTL: 0x15003 BCTL1_BANK_CTL: 0x15013

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	NA:0	NA:0	NA:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA	NA	NA	NA	R	R	R	R
Retention	NA	NA	NA	NA	RET	RET	RET	RET
Name	RSVD	RSVD	RSVD	RSVD	GLBL_WR	DPARAM_TM	ROUTE_ENABLE	DIS_COR

Bank Control Register

Bits	Name	Description
3	GLBL_WR	Global Write Test Mode: The purpose of this bit is to accelerate configuration and working register writing for test purposes. When this bit is set, the bank is in global write mode. In this mode a set of UDBs or UDB channels are selected for writing in parallel based on the setting of the GUDB WR bits and GCH WR bits in the individual UDB. See Table 1-827.
2	DPARAM_TM	DPARAM Test Mode: The DP RAM (s8dparam_ram16x8) has two read ports, one connectred to the system bus (for configuration of the RAM), and one port that drives the DP control bits. When this bit is set, the DP RAM control port is connected to the system bus for reading (the system bus read port is tri-stated) See Table 1-826.
1	ROUTE_ENABLE	Route Enable: When this bit is a 0, all routing drivers are gated off to drive '0'. This results in nets either at 'Z' or '0' state and prevents driver conflicts with random configuration RAM on POR. This bit also controls gating of buffer inputs to prevent high current states in the case of 'Z' nets. After configuration, this bit may be enabled. See Table 1-828.
0	DIS_COR	Disable Clear On Read: The status registers have an automatic clear on read function to maintain firmware synchronization with UDB processing. When the system is stopped in debug mode, this bit can be used to prevent the statu from clearing on a debug read. It also prevents a read pop from the FIFO blocks. Only the top of FIFO can be read when this bit is set. See Table 1-825.

Table 1-825. Bit field encoding: COR_ENUM

Value	Name	Description
1'b0	ENABLE	Status register clear on read enabled. (default)
1'b1	DISABLE	Status register clear on read disabled.

Table 1-826. Bit field encoding: DPARAM_TM_ENUM

Value	Name	Description
1'b0	DISABLE	DPARAM test mode is disabled. (default)
1'b1	ENABLE	DPARAM test mode is enabled.

(continued)

Table 1-827. Bit field encoding: GLBL_WR_ENUM

Value	Name	Description
1'b0	DISABLE	Global Write Test Mode is disabled. (default)
1'b1	ENABLE	Global Write Test Mode enabled.

Table 1-828. Bit field encoding: ROUTE_ENABLE

Value	Name	Description
1'b0	DISABLE	Routing input drivers are gated off to '0' (default)
1'b1	ENABLE	Routing input drivers are enabled.

Table 1-829. Bit field encoding: USCAN_CLK_ENUM

Value	Name	Description
1'b0	DISABLE	UDB DSI scan clk is idle
1'b1	ENABLE	UDB DSI scan clk asserted for 1 clock pulse if USCAN_SE = 0 (capture mode) or for 32 clock pulses if USCAN_SE = 1 (shift mode). Register bit auto-clears after one clock.

Table 1-830. Bit field encoding: USCAN_RES_ENUM

Value	Name	Description
1'b0	DISABLE	RESET is not asserted to the UDB DSI scan registers.
1'b1	ENABLE	RESET is asserted to the UDB DSI scan registers.

Table 1-831. Bit field encoding: USCAN_SET_ENUM

Value	Name	Description
1'b0	DISABLE	SET is not asserted to the UDB DSI scan registers.
1'b1	ENABLE	SET is asserted to the UDB DSI scan registers.

Table 1-832. Bit field encoding: USCAN_SE_ENUM

Value	Name	Description
1'b0	DISABLE	UDB DSI scan chain is in capture mode.
1'b1	ENABLE	UDB DSI scan chain is in shift mode.

1.3.1254 BCTL[0..3]_DCLK_EN0

DCLK_EN

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BCTL0_DCLK_EN0: 0x15008 BCTL1_DCLK_EN0: 0x15018

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	DCEN7	DCEN6	DCEN5	DCEN4	DCEN3	DCEN2	DCEN1	DCEN0

Digital Global Clock Enable Register

Bits	Name	Description
7	DCEN7	Bank Clock Enable Control See Table 1-833.
6	DCEN6	Bank Clock Enable Control See Table 1-833.
5	DCEN5	Bank Clock Enable Control See Table 1-833.
4	DCEN4	Bank Clock Enable Control See Table 1-833.
3	DCEN3	Bank Clock Enable Control See Table 1-833.
2	DCEN2	Bank Clock Enable Control See Table 1-833.
1	DCEN1	Bank Clock Enable Control See Table 1-833.
0	DCEN0	Bank Clock Enable Control See Table 1-833.

Table 1-833. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	DISABLE	Digital Global clock is disabled.
1'b1	ENABLE	Digital Global clock is enabled.

1.3.1255 BCTL[0..3]_BCLK_EN0

BCLK_EN

Reset: Reset Signals Listed Below

Register : Address

BCTL0_BCLK_EN0: 0x15009 BCTL1_BCLK_EN0: 0x15019

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA	R	R	R	R	R	R	R
Retention	NA	RET	RET	RET	RET	RET	RET	RET
Name	RSVD	NC0	WR_CFG_OPT	GLB_DSI_WR	DISABLE_ROUTE	GCH_WR_HI	GCH_WR_LO	BCEN

Bus Clock Enable Register

Bits	Name	Description
6	NC0	Spare register bit
5	WR_CFG_OPT	Select 1/2 clock cycle or full clock cycle generation for bus_last_strobe used in generating write strobes for latches within the UDB. Only one BCLK_ENx register per bank has an active bit. BCTL0_BCLK_EN0 controls this bit for Bank 0. BCTL1_BCLK_EN1 controls this bit for Bank 1. The WR_CFG_OPT bits in the other BCTLx_BCLK_ENy registers are not used. See Table 1-840.
4	GLB_DSI_WR	Enable global write operation for the DSI routing channels. When this bit is set, the DSI ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Control is split top and bottom. BCTL0_BCLK_EN0 controls DSI blocks 0-3. BCTL0_BCLK_EN3 controls DSI blocks 4-7. BCTL1_BCLK_EN1 controls DSI blocks 8-9. BCTL1_BCLK_EN2 controls DSI blocks 12-13. The GLB_DSI_WR bits in the other BCTLx_BCLK_ENy registers are not used. See Table 1-838.
3	DISABLE_ROUTE	By default, when this bit is set to '0', the quadrant routing (for 2 channels in the quadrant) are enabled when the global route enable for the bank is set. However, when this bit is set to '1', the routing in the associated quadrant is disabled and is not enabled by the global route enable bit. The routing will remain in a benign state until it is subsequently configured and then enabled by clearing this bit. See Table 1-835.
2	GCH_WR_HI	Enable global write operation for the routing channel with the higher address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. See Table 1-836.
1	GCH_WR_LO	Enable global write operation for the routing channel with the lower address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. See Table 1-837.
0	BCEN	Bank Clock Enable Control See Table 1-834.

(continued)

Reset Table

Reset Signal	Applicable Register Bit(s)
System reset for retention flops [reset_all_retention]	BCEN, GCH_WR_LO, GCH_WR_HI, DISABLE_ROUTE, GLB_DSI_WR, WR_CFG_OPT, NC0
Domain reset for non-retention flops [reset_all_nonretention]	SLEEP_TEST

Table 1-834. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	DISABLE	Digital Global clock is disabled.
1'b1	ENABLE	Digital Global clock is enabled.

Table 1-835. Bit field encoding: DIS_ROUTE

Value	Name	Description
1'b0	ENABLE	The routing in this quadrant can be enabled with the bank route enable bit. (default)
1'b1	DISABLE	The routing in this quadrant is disabled and held in a benign state.

Table 1-836. Bit field encoding: GCH_WR_HI

Value	Name	Description
1'b0	DISABLE	Global UDB channel configuration write for higher order address is disabled.
1'b1	ENABLE	Global UDB channel configuration write for higher order address is enabled.

Table 1-837. Bit field encoding: GCH_WR_LO

Value	Name	Description
1'b0	DISABLE	Global UDB channel configuration write for lower order address is disabled.
1'b1	ENABLE	Global UDB channel configuration write for lower order address is enabled.

Table 1-838. Bit field encoding: GLB_DSI_WR

Value	Name	Description
1'b0	DISABLE	Global DSI channel configuration write is disabled.
1'b1	ENABLE	Global DSI channel configuration write is enabled.

Table 1-839. Bit field encoding: SLEEP_TEST_ENUM

Value	Name	Description
1'b0	DISABLE	sleep_test is not asserted.
1'b1	ENABLE	sleep_test is asserted.

Table 1-840. Bit field encoding: WR_CFG_OPT_ENUM

Value	Name	Description
1'b0	FULL_CYCLE_STB	bus_last_strobe is generated for the full final bus_clk cycle of a bus transaction.
1'b1	HALF_CYCLE_STB	bus_last_strobe is generated during the last 1/2 clock cycle of a bus transaction on the negative edge of bus_clk.

1.3.1256 BCTL[0..3]_DCLK_EN1

DCLK_EN

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BCTL0_DCLK_EN1: 0x1500A BCTL1_DCLK_EN1: 0x1501A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	DCEN7	DCEN6	DCEN5	DCEN4	DCEN3	DCEN2	DCEN1	DCEN0

Digital Global Clock Enable Register

Bits	Name	Description
7	DCEN7	Bank Clock Enable Control See Table 1-841.
6	DCEN6	Bank Clock Enable Control See Table 1-841.
5	DCEN5	Bank Clock Enable Control See Table 1-841.
4	DCEN4	Bank Clock Enable Control See Table 1-841.
3	DCEN3	Bank Clock Enable Control See Table 1-841.
2	DCEN2	Bank Clock Enable Control See Table 1-841.
1	DCEN1	Bank Clock Enable Control See Table 1-841.
0	DCEN0	Bank Clock Enable Control See Table 1-841.

Table 1-841. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	DISABLE	Digital Global clock is disabled.
1'b1	ENABLE	Digital Global clock is enabled.

1.3.1257 BCTL[0..3]_BCLK_EN1

BCLK_EN

Reset: Reset Signals Listed Below

Register : Address

BCTL0_BCLK_EN1: 0x1500B BCTL1_BCLK_EN1: 0x1501B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA	R	R	R	R	R	R	R
Retention	NA	RET	RET	RET	RET	RET	RET	RET
Name	RSVD	NC0	WR_CFG_OPT	GLB_DSI_WR	DISABLE_ROUTE	GCH_WR_HI	GCH_WR_LO	BCEN

Bus Clock Enable Register

Bits	Name	Description
6	NC0	Spare register bit
5	WR_CFG_OPT	Select 1/2 clock cycle or full clock cycle generation for bus_last_strobe used in generating write strobes for latches within the UDB. Only one BCLK_ENx register per bank has an active bit. BCTL0_BCLK_EN0 controls this bit for Bank 0. BCTL1_BCLK_EN1 controls this bit for Bank 1. The WR_CFG_OPT bits in the other BCTLx_BCLK_ENy registers are not used. See Table 1-848.
4	GLB_DSI_WR	Enable global write operation for the DSI routing channels. When this bit is set, the DSI ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Control is split top and bottom. BCTL0_BCLK_EN0 controls DSI blocks 0-3. BCTL0_BCLK_EN3 controls DSI blocks 4-7. BCTL1_BCLK_EN1 controls DSI blocks 8-9. BCTL1_BCLK_EN2 controls DSI blocks 12-13. The GLB_DSI_WR bits in the other BCTLx_BCLK_ENy registers are not used. See Table 1-846.
3	DISABLE_ROUTE	By default, when this bit is set to '0', the quadrant routing (for 2 channels in the quadrant) are enabled when the global route enable for the bank is set. However, when this bit is set to '1', the routing in the associated quadrant is disabled and is not enabled by the global route enable bit. The routing will remain in a benign state until it is subsequently configured and then enabled by clearing this bit. See Table 1-843.
2	GCH_WR_HI	Enable global write operation for the routing channel with the higher address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. See Table 1-844.
1	GCH_WR_LO	Enable global write operation for the routing channel with the lower address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. See Table 1-845.

(continued)

0	BCEN	Bank Clock Enable Control See Table 1-842.

Reset Table

Reset Signal	Applicable Register Bit(s)
System reset for retention flops [reset_all_retention]	BCEN, GCH_WR_LO, GCH_WR_HI, DISABLE_ROUTE, GLB_DSI_WR, WR_CFG_OPT, NC0
Domain reset for non-retention flops [reset_all_nonretention]	SLEEP_TEST

Table 1-842. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	DISABLE	Digital Global clock is disabled.
1'b1	ENABLE	Digital Global clock is enabled.

Table 1-843. Bit field encoding: DIS_ROUTE

Value	Name	Description
1'b0	ENABLE	The routing in this quadrant can be enabled with the bank route enable bit. (default)
1'b1	DISABLE	The routing in this quadrant is disabled and held in a benign state.

Table 1-844. Bit field encoding: GCH_WR_HI

Value	Name	Description
1'b0	DISABLE	Global UDB channel configuration write for higher order address is disabled.
1'b1	ENABLE	Global UDB channel configuration write for higher order address is enabled.

Table 1-845. Bit field encoding: GCH_WR_LO

Value	Name	Description
1'b0	DISABLE	Global UDB channel configuration write for lower order address is disabled.
1'b1	ENABLE	Global UDB channel configuration write for lower order address is enabled.

Table 1-846. Bit field encoding: GLB_DSI_WR

Value	Name	Description
1'b0	DISABLE	Global DSI channel configuration write is disabled.
1'b1	ENABLE	Global DSI channel configuration write is enabled.

Table 1-847. Bit field encoding: SLEEP_TEST_ENUM

Value	Name	Description
1'b0	DISABLE	sleep_test is not asserted.
1'b1	ENABLE	sleep_test is asserted.

Table 1-848. Bit field encoding: WR_CFG_OPT_ENUM

Value	Name	Description
1'b0	FULL_CYCLE_STB	bus_last_strobe is generated for the full final bus_clk cycle of a bus transaction.
1'b1	HALF_CYCLE_STB	bus_last_strobe is generated during the last 1/2 clock cycle of a bus transaction on the negative edge of bus_clk.

1.3.1258 BCTL[0..3]_DCLK_EN2

DCLK_EN

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BCTL0_DCLK_EN2: 0x1500C BCTL1_DCLK_EN2: 0x1501C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	DCEN7	DCEN6	DCEN5	DCEN4	DCEN3	DCEN2	DCEN1	DCEN0

Digital Global Clock Enable Register

Bits	Name	Description
7	DCEN7	Bank Clock Enable Control See Table 1-849.
6	DCEN6	Bank Clock Enable Control See Table 1-849.
5	DCEN5	Bank Clock Enable Control See Table 1-849.
4	DCEN4	Bank Clock Enable Control See Table 1-849.
3	DCEN3	Bank Clock Enable Control See Table 1-849.
2	DCEN2	Bank Clock Enable Control See Table 1-849.
1	DCEN1	Bank Clock Enable Control See Table 1-849.
0	DCEN0	Bank Clock Enable Control See Table 1-849.

Table 1-849. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	DISABLE	Digital Global clock is disabled.
1'b1	ENABLE	Digital Global clock is enabled.

1.3.1259 BCTL[0..3]_BCLK_EN2

BCLK_EN

Reset: Reset Signals Listed Below

Register : Address

BCTL0_BCLK_EN2: 0x1500D BCTL1_BCLK_EN2: 0x1501D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA	R	R	R	R	R	R	R
Retention	NA	RET	RET	RET	RET	RET	RET	RET
Name	RSVD	NC0	WR_CFG_OPT	GLB_DSI_WR	DISABLE_ROUTE	GCH_WR_HI	GCH_WR_LO	BCEN

Bus Clock Enable Register

Bits	Name	Description
6	NC0	Spare register bit
5	WR_CFG_OPT	Select 1/2 clock cycle or full clock cycle generation for bus_last_strobe used in generating write strobes for latches within the UDB. Only one BCLK_ENx register per bank has an active bit. BCTL0_BCLK_EN0 controls this bit for Bank 0. BCTL1_BCLK_EN1 controls this bit for Bank 1. The WR_CFG_OPT bits in the other BCTLx_BCLK_ENy registers are not used. See Table 1-856.
4	GLB_DSI_WR	Enable global write operation for the DSI routing channels. When this bit is set, the DSI ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Control is split top and bottom. BCTL0_BCLK_EN0 controls DSI blocks 0-3. BCTL0_BCLK_EN3 controls DSI blocks 4-7. BCTL1_BCLK_EN1 controls DSI blocks 8-9. BCTL1_BCLK_EN2 controls DSI blocks 12-13. The GLB_DSI_WR bits in the other BCTLx_BCLK_ENy registers are not used. See Table 1-854.
3	DISABLE_ROUTE	By default, when this bit is set to '0', the quadrant routing (for 2 channels in the quadrant) are enabled when the global route enable for the bank is set. However, when this bit is set to '1', the routing in the associated quadrant is disabled and is not enabled by the global route enable bit. The routing will remain in a benign state until it is subsequently configured and then enabled by clearing this bit. See Table 1-851.
2	GCH_WR_HI	Enable global write operation for the routing channel with the higher address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. See Table 1-852.
1	GCH_WR_LO	Enable global write operation for the routing channel with the lower address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. See Table 1-853.
0	BCEN	Bank Clock Enable Control See Table 1-850.

(continued)

Reset Table

Reset Signal	Applicable Register Bit(s)
System reset for retention flops [reset_all_retention]	BCEN, GCH_WR_LO, GCH_WR_HI, DISABLE_ROUTE, GLB_DSI_WR, WR_CFG_OPT, NC0
Domain reset for non-retention flops [reset_all_nonretention]	SLEEP_TEST

Table 1-850. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	DISABLE	Digital Global clock is disabled.
1'b1	ENABLE	Digital Global clock is enabled.

Table 1-851. Bit field encoding: DIS_ROUTE

Value	Name	Description
1'b0	ENABLE	The routing in this quadrant can be enabled with the bank route enable bit. (default)
1'b1	DISABLE	The routing in this quadrant is disabled and held in a benign state.

Table 1-852. Bit field encoding: GCH_WR_HI

Value	Name	Description
1'b0	DISABLE	Global UDB channel configuration write for higher order address is disabled.
1'b1	ENABLE	Global UDB channel configuration write for higher order address is enabled.

Table 1-853. Bit field encoding: GCH_WR_LO

Value	Name	Description
1'b0	DISABLE	Global UDB channel configuration write for lower order address is disabled.
1'b1	ENABLE	Global UDB channel configuration write for lower order address is enabled.

Table 1-854. Bit field encoding: GLB_DSI_WR

Value	Name	Description
1'b0	DISABLE	Global DSI channel configuration write is disabled.
1'b1	ENABLE	Global DSI channel configuration write is enabled.

Table 1-855. Bit field encoding: SLEEP_TEST_ENUM

Value	Name	Description
1'b0	DISABLE	sleep_test is not asserted.
1'b1	ENABLE	sleep_test is asserted.

Table 1-856. Bit field encoding: WR_CFG_OPT_ENUM

Value	Name	Description
1'b0	FULL_CYCLE_STB	bus_last_strobe is generated for the full final bus_clk cycle of a bus transaction.
1'b1	HALF_CYCLE_STB	bus_last_strobe is generated during the last 1/2 clock cycle of a bus transaction on the negative edge of bus_clk.

1.3.1260 BCTL[0..3]_DCLK_EN3

DCLK_EN

Reset: System reset for retention flops [reset_all_retention]

Register : Address

BCTL0_DCLK_EN3: 0x1500E BCTL1_DCLK_EN3: 0x1501E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R	R	R	R	R	R	R	R
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	DCEN7	DCEN6	DCEN5	DCEN4	DCEN3	DCEN2	DCEN1	DCEN0

Digital Global Clock Enable Register

Bits	Name	Description
7	DCEN7	Bank Clock Enable Control See Table 1-857.
6	DCEN6	Bank Clock Enable Control See Table 1-857.
5	DCEN5	Bank Clock Enable Control See Table 1-857.
4	DCEN4	Bank Clock Enable Control See Table 1-857.
3	DCEN3	Bank Clock Enable Control See Table 1-857.
2	DCEN2	Bank Clock Enable Control See Table 1-857.
1	DCEN1	Bank Clock Enable Control See Table 1-857.
0	DCEN0	Bank Clock Enable Control See Table 1-857.

Table 1-857. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	DISABLE	Digital Global clock is disabled.
1'b1	ENABLE	Digital Global clock is enabled.

1.3.1261 BCTL[0..3]_BCLK_EN3

BCLK_EN

Reset: Reset Signals Listed Below

Register : Address

BCTL0_BCLK_EN3: 0x1500F BCTL1_BCLK_EN3: 0x1501F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	NA	R	R	R	R	R	R	R
Retention	NA	RET	RET	RET	RET	RET	RET	RET
Name	RSVD	NC0	WR_CFG_OPT	GLB_DSI_WR	DISABLE_ROUTE	GCH_WR_HI	GCH_WR_LO	BCEN

Bus Clock Enable Register

Bits	Name	Description
6	NC0	Spare register bit
5	WR_CFG_OPT	Select 1/2 clock cycle or full clock cycle generation for bus_last_strobe used in generating write strobes for latches within the UDB. Only one BCLK_ENx register per bank has an active bit. BCTL0_BCLK_EN0 controls this bit for Bank 0. BCTL1_BCLK_EN1 controls this bit for Bank 1. The WR_CFG_OPT bits in the other BCTLx_BCLK_ENy registers are not used. See Table 1-864.
4	GLB_DSI_WR	Enable global write operation for the DSI routing channels. When this bit is set, the DSI ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Control is split top and bottom. BCTL0_BCLK_EN0 controls DSI blocks 0-3. BCTL0_BCLK_EN3 controls DSI blocks 4-7. BCTL1_BCLK_EN1 controls DSI blocks 8-9. BCTL1_BCLK_EN2 controls DSI blocks 12-13. The GLB_DSI_WR bits in the other BCTLx_BCLK_ENy registers are not used. See Table 1-862.
3	DISABLE_ROUTE	By default, when this bit is set to '0', the quadrant routing (for 2 channels in the quadrant) are enabled when the global route enable for the bank is set. However, when this bit is set to '1', the routing in the associated quadrant is disabled and is not enabled by the global route enable bit. The routing will remain in a benign state until it is subsequently configured and then enabled by clearing this bit. See Table 1-859.
2	GCH_WR_HI	Enable global write operation for the routing channel with the higher address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. See Table 1-860.
1	GCH_WR_LO	Enable global write operation for the routing channel with the lower address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. See Table 1-861.

(continued)

0	BCEN	Bank Clock Enable Control See Table 1-858.

Reset Table

Reset Signal	Applicable Register Bit(s)
System reset for retention flops [reset_all_retention]	BCEN, GCH_WR_LO, GCH_WR_HI, DISABLE_ROUTE, GLB_DSI_WR, WR_CFG_OPT, NC0
Domain reset for non-retention flops [reset_all_nonretention]	SLEEP_TEST

Table 1-858. Bit field encoding: CLK_EN_ENUM

Value	Name	Description
1'b0	DISABLE	Digital Global clock is disabled.
1'b1	ENABLE	Digital Global clock is enabled.

Table 1-859. Bit field encoding: DIS_ROUTE

Value	Name	Description
1'b0	ENABLE	The routing in this quadrant can be enabled with the bank route enable bit. (default)
1'b1	DISABLE	The routing in this quadrant is disabled and held in a benign state.

Table 1-860. Bit field encoding: GCH_WR_HI

Value	Name	Description
1'b0	DISABLE	Global UDB channel configuration write for higher order address is disabled.
1'b1	ENABLE	Global UDB channel configuration write for higher order address is enabled.

Table 1-861. Bit field encoding: GCH_WR_LO

Value	Name	Description
1'b0	DISABLE	Global UDB channel configuration write for lower order address is disabled.
1'b1	ENABLE	Global UDB channel configuration write for lower order address is enabled.

Table 1-862. Bit field encoding: GLB_DSI_WR

Value	Name	Description
1'b0	DISABLE	Global DSI channel configuration write is disabled.
1'b1	ENABLE	Global DSI channel configuration write is enabled.

Table 1-863. Bit field encoding: SLEEP_TEST_ENUM

Value	Name	Description
1'b0	DISABLE	sleep_test is not asserted.
1'b1	ENABLE	sleep_test is asserted.

Table 1-864. Bit field encoding: WR_CFG_OPT_ENUM

Value	Name	Description
1'b0	FULL_CYCLE_STB	bus_last_strobe is generated for the full final bus_clk cycle of a bus transaction.
1'b1	HALF_CYCLE_STB	bus_last_strobe is generated during the last 1/2 clock cycle of a bus transaction on the negative edge of bus_clk.

1.3.1262 IDMUX_IRQ_CTL[0..7]

Control Register IRQ_CTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

IDMUX_IRQ_CTL0: 0x15100
IDMUX_IRQ_CTL1: 0x15101
IDMUX_IRQ_CTL2: 0x15102
IDMUX_IRQ_CTL3: 0x15103
IDMUX_IRQ_CTL4: 0x15104
IDMUX_IRQ_CTL5: 0x15105
IDMUX_IRQ_CTL6: 0x15106
IDMUX_IRQ_CTL7: 0x15107

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00		R/W:00		R/W:00		R/W:00	
HW Access	R		R		R		R	
Retention	RET		RET		RET		RET	
Name	ICTRL3		ICTRL2		ICTRL1		ICTRL0	

This register is used to configure the routing and processing of interrupts.

Bits	Name	Description
7:6	ICTRL3[1:0]	IRQ Control See Table 1-865.
5:4	ICTRL2[1:0]	IRQ Control See Table 1-865.
3:2	ICTRL1[1:0]	IRQ Control See Table 1-865.
1:0	ICTRL0[1:0]	IRQ Control See Table 1-865.

Table 1-865. Bit field encoding: irq_enum

Value	Name	Description
2'b00	Fixed Function	Fixed Function Interrupt.
2'b01	DMA	DMA Interrupt
2'b10	UDB	UDB Level Interrupt
2'b11	UDB EDGE	UDB Edge Detect Interrupt

1.3.1263 IDMUX_DRQ_CTL[0..5]

Configuration Register DRQ_CTL

Reset: System reset for retention flops [reset_all_retention]

Register : Address

IDMUX_DRQ_CTL0: 0x15110

IDMUX_DRQ_CTL1: 0x15111

IDMUX_DRQ_CTL2: 0x15112

IDMUX_DRQ_CTL3: 0x15113

IDMUX_DRQ_CTL4: 0x15114

IDMUX_DRQ_CTL5: 0x15115

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00		R/W:00		R/W:00		R/W:00	
HW Access	R		R		R		R	
Retention	RET		RET		RET		RET	
Name	DCTRL3		DCTRL2		DCTRL1		DCTRL0	

This register is used to select between DMA requests (fixed function or udb).

Bits	Name	Description
7:6	DCTRL3[1:0]	DMA input type. See Table 1-866.
5:4	DCTRL2[1:0]	DMA input type. See Table 1-866.
3:2	DCTRL1[1:0]	DMA input type. See Table 1-866.
1:0	DCTRL0[1:0]	DMA input type. See Table 1-866.

Table 1-866. Bit field encoding: drq_enum

Value	Name	Description
2'b00	Fixed Function	Fixed Function DMA request.
2'b01	UDB	UDB Level DMA request
2'b10	UDB EDGE	UDB Edge Detect DMA request
2'b11	RESERVED	RESERVED

1.3.1264 IRAM_IRAM_L_DATA_RAM_L[0..127]

Internal Data RAM

Reset: N/A

Register : Address

IRAM_IRAM_L_DATA_RAM_L: 0x50000-0x5007F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	INT_RAM_REG							

This is internal data RAM space for DP8051.

Bits	Name	Description
7:0	INT_RAM_REG[7:0]	Internal data ram space

1.3.1265 IRAM_IRAM_H_DATA_RAM_H[0..127]

Internal Data RAM

Reset: N/A

Register : Address

IRAM_IRAM_H_DATA_RAM_H: 0x50080-0x500FF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	INT_RAM_REG							

This is internal data RAM space for DP8051.

Bits	Name	Description
7:0	INT_RAM_REG[7:0]	Internal data ram space

1.3.1266 SFR_REGS_SP

Stack Pointer

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_REGS_SP: 0x50181

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000111							
HW Access	R/W							
Retention	RET							
Name	sp							

Stack Pointer Register of DP8051. It is incremented before data is stored during PUSH and CALL execution and decremented after data is popped during POP, RET and RETI execution.

Bits	Name	Description
7:0	sp[7:0]	Stack Pointer: It always points to last valid stack byte

1.3.1267 SFR_REGS_DPL

Data Pointer 0 Low

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_REGS_DPL: 0x50182

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	dpl							

Lower Byte of Data Pointer Register DPTR0. Data pointers are used to speed up data block copying.

Bits	Name	Description
7:0	dpl[7:0]	Lower Byte of DPTR0 register

1.3.1268 SFR_REGS_DPH

Data Pointer 0 High

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_REGS_DPH: 0x50183

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	dph							

Upper Byte of Data Pointer Register DPTR0. Data pointers are used to speed up data block copying.

Bits	Name	Description
7:0	dph[7:0]	Upper Byte of DPTR0 register

1.3.1269 SFR_REGS_DPL1

Data Pointer 1 Low

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_REGS_DPL1: 0x50184

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	dpl1							

Lower Byte of Data Pointer Register DPTR1. Data pointers are used to speed up data block copying.

Bits	Name	Description
7:0	dpl1[7:0]	Lower Byte of DPTR1 register

1.3.1270 SFR_REGS_DPH1

Data Pointer 1 High

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_REGS_DPH1: 0x50185

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	dph1							

Upper Byte of Data Pointer Register DPTR1. Data pointers are used to speed up data block copying.

Bits	Name	Description
7:0	dph1[7:0]	Upper Byte of DPTR1 register

1.3.1271 SFR_REGS_DPS

Data pointer select register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_REGS_DPS: 0x50186

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R
Retention	NA							RET
Name	RSVD							SEL

The SEL bit of DPS register is used to select one of data pointer DPTR0 or DPTR1

Bits	Name	Description
0	SEL	1'b0: Select DPTR0. 1'b1: Select DPTR1

1.3.1272 SFR_REGS_DPX

Data Pointer Extended 0 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_REGS_DPX: 0x50193

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	dpx							

Data pointer extended registers hold the most significant part of program memory during access to data located above 64KB

Bits	Name	Description
7:0	dpx[7:0]	During MOVX instruction using DPTR0 register, the most significant part of address XRAMADDR[23:16] is always equal to DPX0(0x93) contents.

1.3.1273 SFR_REGS_DPX1

Data Pointer Extended 1 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_REGS_DPX1: 0x50195

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	dpx1							

Data pointer extended registers hold the most significant part of program memory during access to data located above 64KB.

Bits	Name	Description
7:0	dpx1[7:0]	During MOVX instruction using DPTR1 register, the most significant part of address XRAMADDR[23:16] is always equal to DPX1(0x95) contents.

1.3.1274 SFR_REGS_P2

P2 read-write Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_REGS_P2: 0x501A0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	P2							

This register holds XRAMADDR[15:8] bits during MOVX using R0 or R1

Bits	Name	Description
7:0	P2[7:0]	During MOVX using R0 or R1 register, XRAMADDR[15:8] is always equal to P2(0xA0) contents.

1.3.1275 SFR_REGS_IE

Interrupt Enable Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_REGS_IE: 0x501A8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	NA:0000000						
HW Access	R	NA						
Retention	RET	NA						
Name	EA	RSVD						

The Interrupt system can be enabled/disabled using EA bit IE register

Bits	Name	Description
7	EA	Enable Interrupt Controller at logic high

1.3.1276 SFR_REGS_PSW

Program Status Word Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_REGS_PSW: 0x501D0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:00		R/W:0	R/W:0	R:0
HW Access	R/W	R/W	R	R		R/W	R	R/W
Retention	RET	RET	RET	RET		RET	RET	RET
Name	CY	AC	F0	RS		OV	F1	P

The PSW contains several bits that reflect the current state of the CPU.

Bits	Name	Description
7	CY	Carry Flag
6	AC	Auxilar Carry Flag
5	F0	General Purpose Flag 0
4:3	RS[1:0]	Register Bank Select. 2'b00: Bank 0 - data address 0x00-0x07. 2'b01: Bank 1 - data address 0x08-0x0F. 2'b10: Bank 2 - data address 0x10-0x17. 2'b11: Bank 3 - data address 0x18-0x1F
2	OV	Over Flow Flag
1	F1	General Purpose Flag 1
0	P	Parity Flag

1.3.1277 SFR_REGS_ACC

Accumulator register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_REGS_ACC: 0x501E0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	ACC							

Accumulator Register of DP8051

Bits	Name	Description
7:0	ACC[7:0]	Accumulator

1.3.1278 SFR_REGS_MXAX

MOVX @Ri extended Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_REGS_MXAX: 0x501EA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R							
Retention	RET							
Name	MXAX							

This register holds the most significant part of address XRAMADDR[23:16] during MOVX using R0 or R1.

Bits	Name	Description
7:0	MXAX[7:0]	During MOVX using R0 or R1 register, XRAMADDR[23:16] is always equal to MAXA(0xEA) contents.

1.3.1279 SFR_REGS_B

B Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_REGS_B: 0x501F0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	B							

The B register is used during multiply and divide operations. In other cases may be used as normal SFR.

Bits	Name	Description
7:0	B[7:0]	B Register

1.3.1280 SFR_USER_GPIO0

GPIO0 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_USER_GPIO0: 0x50180

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	GPIO0							

This register is used to set the output data state for Port0

Bits	Name	Description
7:0	GPIO0[7:0]	The data written to this register specifies the high or low state for GPIO pin if the corresponding bit of GPIO0_SEL register is set to high

1.3.1281 SFR_USER_GPIRD0

GPIRD0 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_USER_GPIRD0: 0x50189

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	RET							
Name	GPIRD0							

This read only register contains pin state value of Port0

Bits	Name	Description
7:0	GPIRD0[7:0]	This register contains the pin state values of Port0 pins

1.3.1282 SFR_USER_GPIO0_SEL

GPIO0_SEL Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_USER_GPIO0_SEL: 0x5018A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	GPIO0_SEL							

This register is used to select the GPIO0 register to set the output data state for Port0

Bits	Name	Description
7:0	GPIO0_SEL[7:0]	This register is used to select each bit of the GPIO0 register to set the output data state for the corresponding pin of Port0.

1.3.1283 SFR_USER_GPIO1

GPIO1 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_USER_GPIO1: 0x50190

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	GPIO1							

This register is used to set the output data state for Port1

Bits	Name	Description
7:0	GPIO1[7:0]	The data written to this register specifies the high or low state for GPIO pin if the corresponding bit of GPIO1_SEL register is set to high

1.3.1284 SFR_USER_GPIRD1

GPIRD1 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_USER_GPIRD1: 0x50191

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	RET							
Name	GPIRD1							

This read only register contains pin state value of Port1

Bits	Name	Description
7:0	GPIRD1[7:0]	This register contains the pin state values of Port1 pins

1.3.1285 SFR_USER_GPIO2

GPIO2 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_USER_GPIO2: 0x50198

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	GPIO2							

This register is used to set the output data state for Port2

Bits	Name	Description
7:0	GPIO2[7:0]	The data written to this register specifies the high or low state for GPIO pin if the corresponding bit of GPIO2_SEL register is set to high

1.3.1286 SFR_USER_GPIRD2

GPIRD2 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_USER_GPIRD2: 0x50199

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	RET							
Name	GPIRD2							

This read only register contains pin state values of Port2

Bits	Name	Description
7:0	GPIRD2[7:0]	This register contains the pin state values of Port2 pins

1.3.1287 SFR_USER_GPIO2_SEL

GPIO2_SEL Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_USER_GPIO2_SEL: 0x5019A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	GPIO2_SEL							

This register is used to select the GPIO2 register to set the output data state for Port2

Bits	Name	Description
7:0	GPIO2_SEL[7:0]	This register is used to select each bit of the GPIO2 register to set the output data state for the corresponding pin of Port2.

1.3.1288 SFR_USER_GPIO1_SEL

GPIO1_SEL Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_USER_GPIO1_SEL: 0x501A2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	GPIO1_SEL							

This register is used to select the GPIO1 register to set the output data state for Port1

Bits	Name	Description
7:0	GPIO1_SEL[7:0]	This register is used to select each bit of the GPIO1 register to set the output data state for the corresponding pin of Port1.

1.3.1289 SFR_USER_GPIO3

GPIO3 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_USER_GPIO3: 0x501B0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	GPIO3							

This register is used to set the output data state for Port3

Bits	Name	Description
7:0	GPIO3[7:0]	The data written to this register specifies the high or low state for GPIO pin if the corresponding bit of GPIO3_SEL register is set to high

1.3.1290 SFR_USER_GPIRD3

GPIRD3 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_USER_GPIRD3: 0x501B1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	RET							
Name	GPIRD3							

This read only register contains pin state values of Port3

Bits	Name	Description
7:0	GPIRD3[7:0]	This register contains the pin state values of Port3 pins

1.3.1291 SFR_USER_GPIO3_SEL

GPIO3_SEL Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_USER_GPIO3_SEL: 0x501B2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	GPIO3_SEL							

This register is used to select the GPIO3 register to set the output data state for Port3

Bits	Name	Description
7:0	GPIO3_SEL[7:0]	This register is used to select each bit of the GPIO3 register to set the output data state for the corresponding pin of Port3.

1.3.1292 SFR_USER_GPIO4

GPIO4 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_USER_GPIO4: 0x501C0

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	GPIO4							

This register is used to set the output data state for Port4

Bits	Name	Description
7:0	GPIO4[7:0]	The data written to this register specifies the high or low state for GPIO pin if the corresponding bit of GPIO4_SEL register is set to high

1.3.1293 SFR_USER_GPIRD4

GPIRD4 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_USER_GPIRD4: 0x501C1

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	RET							
Name	GPIRD4							

This read only register contains pin state values of Port4

Bits	Name	Description
7:0	GPIRD4[7:0]	This register contains the pin state values of Port4 pins

1.3.1294 SFR_USER_GPIO4_SEL

GPIO4_SEL Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_USER_GPIO4_SEL: 0x501C2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	GPIO4_SEL							

This register is used to select the GPIO4 register to set the output data state for Port4

Bits	Name	Description
7:0	GPIO4_SEL[7:0]	This register is used to select each bit of the GPIO4 register to set the output data state for the corresponding pin of Port4.

1.3.1295 SFR_USER_GPIO5

GPIO5 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_USER_GPIO5: 0x501C8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	GPIO5							

This register is used to set the output data state for Port5

Bits	Name	Description
7:0	GPIO5[7:0]	The data written to this register specifies the high or low state for GPIO pin if the corresponding bit of GPIO5_SEL register is set to high

1.3.1296 SFR_USER_GPIRD5

GPIRD5 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_USER_GPIRD5: 0x501C9

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	RET							
Name	GPIRD5							

This read only register contains pin state values of Port5

Bits	Name	Description
7:0	GPIRD5[7:0]	This register contains the pin state values of Port5 pins

1.3.1297 SFR_USER_GPIO5_SEL

GPIO5_SEL Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_USER_GPIO5_SEL: 0x501CA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	GPIO5_SEL							

This register is used to select the GPIO5 register to set the output data state for Port5

Bits	Name	Description
7:0	GPIO5_SEL[7:0]	This register is used to select each bit of the GPIO5 register to set the output data state for the corresponding pin of Port5.

1.3.1298 SFR_USER_GPIO6

GPIO6 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_USER_GPIO6: 0x501D8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	GPIO6							

This register is used to set the output data state for Port6

Bits	Name	Description
7:0	GPIO6[7:0]	The data written to this register specifies the high or low state for GPIO pin if the corresponding bit of GPIO6_SEL register is set to high

1.3.1299 SFR_USER_GPIRD6

GPIRD6 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_USER_GPIRD6: 0x501D9

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	RET							
Name	GPIRD6							

This read only register contains pin state values of Port6

Bits	Name	Description
7:0	GPIRD6[7:0]	This register contains the pin state values of Port6 pins

1.3.1300 SFR_USER_GPIO6_SEL

GPIO6_SEL Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_USER_GPIO6_SEL: 0x501DA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	GPIO6_SEL							

This register is used to select the GPIO6 register to set the output data state for Port6

Bits	Name	Description
7:0	GPIO6_SEL[7:0]	This register is used to select each bit of the GPIO6 register to set the output data state for the corresponding pin of Port6.

1.3.1301 SFR_USER_GPIO12

GPIO12 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_USER_GPIO12: 0x501E8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	GPIO12							

This register is used to set the output data state for Port12

Bits	Name	Description
7:0	GPIO12[7:0]	The data written to this register specifies the high or low state for GPIO pin if the corresponding bit of GPIO12_SEL register is set to high

1.3.1302 SFR_USER_GPIRD12

GPIRD12 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_USER_GPIRD12: 0x501E9

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	RET							
Name	GPIRD12							

This read only register contains pin state values of Port12

Bits	Name	Description
7:0	GPIRD12[7:0]	This register contains the pin state values of Port12 pins

1.3.1303 SFR_USER_GPIO12_SEL

GPIO12_SEL Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_USER_GPIO12_SEL: 0x501F2

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	GPIO12_SEL							

This register is used to select the GPIO12 register to set the output data state for Port12

Bits	Name	Description
7:0	GPIO12_SEL[7:0]	This register is used to select each bit of the GPIO12 register to set the output data state for the corresponding pin of Port12.

1.3.1304 SFR_USER_GPIO15

GPIO15 Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_USER_GPIO15: 0x501F8

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	GPIO15							

This register is used to set the output data state for Port15

Bits	Name	Description
7:0	GPIO15[7:0]	The data written to this register specifies the high or low state for GPIO pin if the corresponding bit of GPIO15_SEL register is set to high

1.3.1305 SFR_USER_GPIRD15

GPIRD15 Register

Reset: Reset Signals Listed Below

Register : Address

SFR_USER_GPIRD15: 0x501F9

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UU		R:000000					
HW Access	R/W		R/W					
Retention	NONRET		RET					
Name	GPIRD15_7_6		GPIRD15_5_0					

This read only register contains pin state values of Port15

Bits	Name	Description
7:6	GPIRD15_7_6[1:0]	Contains the pin state values of Port15 pins 7 to 6
5:0	GPIRD15_5_0[5:0]	Contains the pin state values of Port15 pins 5 to 0

Reset Table

Reset Signal	Applicable Register Bit(s)
N/A	GPIRD15_7_6[1:0]
System reset for retention flops [reset_all_retention]	GPIRD15_5_0[5:0]

1.3.1306 SFR_USER_GPIO15_SEL

GPIO15_SEL Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_USER_GPIO15_SEL: 0x501FA

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	GPIO15_SEL							

This register is used to select the GPIO15 register to set the output data state for Port15

Bits	Name	Description
7:0	GPIO15_SEL[7:0]	This register is used to select each bit of the GPIO15 register to set the output data state for the corresponding pin of Port15.

1.3.1307 SFR_SPACE_RSVD[0..255]

Placeholder Memory Space

Reset: System reset for retention flops [reset_all_retention]

Register : Address

SFR_SPACE_RSVD: 0x50100-0x501FF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R							
Retention	NA							
Name	RSVD							

Bits	Name	Description
7:0	RSVD[7:0]	(no description)

1.3.1308 DOC_DBG_CTRL

Debug Control Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DOC_DBG_CTRL: 0x50220

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	W:0000				R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R/W				R/W	R/W	R/W	R/W
Retention	RET				RET	RET	RET	RET
Name	DBG_KEY				A_TMRS	STEP	HALT	DBG_ACT

The DBG_CTRL Register (DGB_CTRL) is used to enable debug, halt and single step the 8051 CPU.

Bits	Name	Description
7:4	DBG_KEY[3:0]	Every write to this register must contain the debug key value of 0b1011. Writes to this register are ignored if the correct key is not written.
3	A_TMRS	Allow Timers, is used to enable timers such as the WDT and CTW that are normally paused when the CPU is halted in debug mode. Setting A_TMRS to '1' allows the WDT and CTW to operate as if the part was not in debug mode.
2	STEP	The STEP bit steps one instruction on the 8051 CPU. The HALT bit must be set to 1 to write this bit. This bit is reset to 0 after the step operation is complete. Writing 0 to this bit has no effect.
1	HALT	Halts the 8051 CPU if written to 1, if the CPU is halted writing 0 to the HALT bits un-halts the CPU. A read of the HALT bit returns the current state of CPU: 1 - halted, 0 - running.
0	DBG_ACT	This bit activates debug. This bit must be set to 1 to halt, single step, break, trace or read and write memory address with the DoC

1.3.1309 DOC_PA_BKPT0

Program Address Breakpoint Register 0

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DOC_PA_BKPT0: 0x50224

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	COMP							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	COMP							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Retention	NA							RET
Name	RSVD							ENA

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

The Program Address Breakpoint Regsiter (PA_BKPT) is used to set a Program address breapoint

Bits	Name	Description
16	ENA	Enables breakpoint when set to 1, disables breakpoint when set to 0
15:0	COMP[15:0]	Halts the CPU if stored value matches the program counter when the breakpoint is enabled.

1.3.1310 DOC_PA_BKPT1

Program Address Breakpoint Register 1

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DOC_PA_BKPT1: 0x50228

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	COMP							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	COMP							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Retention	NA							RET
Name	RSVD							ENA

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

The Program Address Breakpoint Regsiter (PA_BKPT) is used to set a Program address breapoint

Bits	Name	Description
16	ENA	Enables breakpoint when set to 1, disables breakpoint when set to 0
15:0	COMP[15:0]	Halts the CPU if stored value matches the program counter when the breakpoint is enabled.

1.3.1311 DOC_PA_BKPT2

Program Address Breakpoint Register 2

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DOC_PA_BKPT2: 0x5022C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	COMP							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	COMP							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Retention	NA							RET
Name	RSVD							ENA

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

The Program Address Breakpoint Regsiter (PA_BKPT) is used to set a Program address breapoint

Bits	Name	Description
16	ENA	Enables breakpoint when set to 1, disables breakpoint when set to 0
15:0	COMP[15:0]	Halts the CPU if stored value matches the program counter when the breakpoint is enabled.

1.3.1312 DOC_PA_BKPT3

Program Address Breakpoint Register 3

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DOC_PA_BKPT3: 0x50230

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	COMP							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	COMP							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Retention	NA							RET
Name	RSVD							ENA

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

The Program Address Breakpoint Regsiter (PA_BKPT) is used to set a Program address breapoint

Bits	Name	Description
16	ENA	Enables breakpoint when set to 1, disables breakpoint when set to 0
15:0	COMP[15:0]	Halts the CPU if stored value matches the program counter when the breakpoint is enabled.

1.3.1313 DOC_PA_BKPT4

Program Address Breakpoint Register 4

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DOC_PA_BKPT4: 0x50234

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	COMP							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	COMP							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Retention	NA							RET
Name	RSVD							ENA

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

The Program Address Breakpoint Regsiter (PA_BKPT) is used to set a Program address breapoint

Bits	Name	Description
16	ENA	Enables breakpoint when set to 1, disables breakpoint when set to 0
15:0	COMP[15:0]	Halts the CPU if stored value matches the program counter when the breakpoint is enabled.

1.3.1314 DOC_PA_BKPT5

Program Address Breakpoint Register 5

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DOC_PA_BKPT5: 0x50238

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	COMP							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	COMP							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Retention	NA							RET
Name	RSVD							ENA

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

The Program Address Breakpoint Regsiter (PA_BKPT) is used to set a Program address breapoint

Bits	Name	Description
16	ENA	Enables breakpoint when set to 1, disables breakpoint when set to 0
15:0	COMP[15:0]	Halts the CPU if stored value matches the program counter when the breakpoint is enabled.

1.3.1315 DOC_PA_BKPT6

Program Address Breakpoint Register 6

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DOC_PA_BKPT6: 0x5023C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	COMP							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	COMP							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Retention	NA							RET
Name	RSVD							ENA

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

The Program Address Breakpoint Regsiter (PA_BKPT) is used to set a Program address breapoint

Bits	Name	Description
16	ENA	Enables breakpoint when set to 1, disables breakpoint when set to 0
15:0	COMP[15:0]	Halts the CPU if stored value matches the program counter when the breakpoint is enabled.

1.3.1316 DOC_PA_BKPT7

Program Address Breakpoint Register 7

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DOC_PA_BKPT7: 0x50240

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	COMP							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	COMP							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Retention	NA							RET
Name	RSVD							ENA

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:00000000							
HW Access	NA							
Retention	NA							
Name	RSVD							

The Program Address Breakpoint Regsiter (PA_BKPT) is used to set a Program address breapoint

Bits	Name	Description
16	ENA	Enables breakpoint when set to 1, disables breakpoint when set to 0
15:0	COMP[15:0]	Halts the CPU if stored value matches the program counter when the breakpoint is enabled.

1.3.1317 DOC_MEM_BKPT

Memory Breakpoint Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DOC_MEM_BKPT: 0x50244

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	COMP							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	COMP							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	COMP							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	NA:0	R/W:00000					R/W:00	
HW Access	NA	R/W					R/W	
Retention	NA	RET					RET	
Name	RSVD	MASK					MB_CFG	

The Memory Breakpoint register is used (MEM_BKPT) is used to set a memory breakpoint, this breakpoint is enabled in the BKPT_CFG register. This register can be used to halt the CPU on any CPU accessible register with the exection of the 8051's internal memory.

Bits	Name	Description
30:26	MASK[4:0]	Mask, the MASK bits are used to allow the memory breakpoint to break on a range of values. The value entered as the MASK ingores that bit of the COMP value and every bit to its right. Example: If MASK = 4, COMP will ignore the least significant 4 bits when comparing the memory address. If the compare address was 0xDEAF only 0xDEA* would be compared.
25:24	MB_CFG[1:0]	Memory Breakpoint Configuration. See Table 1-867.
23:0	COMP[23:0]	Halts the CPU if stored value matches address of current next address access.

(continued)

Table 1-867. Bit field encoding: MB_CFG_ENUM

Value	Name	Description
2'b00	MB_CFG_DIS	Memory Breakpoint disabled
2'b01	MB_CFG_R	Break on read only
2'b10	MB_CFG_W	Break on write only
2'b11	MB_CFG_RW	Break on read or write

1.3.1318 DOC_BKPT_CFG

Breakpoint Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DOC_BKPT_CFG: 0x50248

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0	R/W:0
HW Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Retention	RET	RET	RET	RET	RET	RET	RET	RET
Name	CBKPT_6	CBKPT_5	CBKPT_4	CBKPT_3	CBKPT_2	CBKPT_1	CBKPT_0	BC_ENA

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0000				R:0	R/W:0	R/W:0	R/W:0
HW Access	NA				R/W	R/W	R/W	R/W
Retention	NA				RET	RET	RET	RET
Name	RSVD				WDR_TRG	WDRBKPT	CBKPT_8	CBKPT_7

The breakpoint chaining register is used to enable the memory breakpoint, and to configure breakpoint chaining

Bits	Name	Description
11	WDR_TRG	Watch Dog Reset Triggered, this is a read-only bit that can be used to determine if the CPU was halted because a WDR occurred. This bit will be set to 1 if the CPU was halted due to WDR, otherwise it will be read as a 0.
10	WDRBKPT	Watch Dog Reset Breakpoint Disable, controls the halting of the CPU when a WDR is triggered when debugging. The WDR breakpoint is enabled by default, (WDRBKPT = 0) but can be disabled by writing this bit to 1.
9	CBKPT_8	Set to 1 to add the memory breakpoint to the breakpoint chain.
8	CBKPT_7	Set to 1 to add breakpoint 7 to the breakpoint chain.
7	CBKPT_6	Set to 1 to add breakpoint 6 to the breakpoint chain.
6	CBKPT_5	Set to 1 to add breakpoint 5 to the breakpoint chain.
5	CBKPT_4	Set to 1 to add breakpoint 4 to the breakpoint chain.
4	CBKPT_3	Set to 1 to add breakpoint 3 to the breakpoint chain.
3	CBKPT_2	Set to 1 to add breakpoint 2 to the breakpoint chain.
2	CBKPT_1	set to 1, to add breakpoint 1 to the breakpoint chain.
1	CBKPT_0	set to 1, to add breakpoint 0 to the breakpoint chain.
0	BC_ENA	Enables breakpoint chaining, writing to bits[9:1] of this register has no effect on breakpoint chaining unless this bit set to 1, but the bits [9:1] can always be set regardless of the state of this bit.

1.3.1319 DOC_BKPTCS

Breakpoint Chain Status

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DOC_BKPTCS: 0x5024A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	RET							
Name	RBIC							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	NA:0000000							R:0
HW Access	NA							R/W
Retention	NA							RET
Name	RSVD							RBIC

The Breakpoint chain status register contains the current status of the breakpoint chain, which breakpoints have been triggered and which breakpoints remain in the chain

Bits	Name	Description
8:0	RBIC[8:0]	Remaining Breakpoints In Chain, the read value of 1 indicates that the corresponding breakpoint has not been triggered yet. Example: if bit[0] of BKPTCS reads as 1, this means that breakpoint chaining of breakpoint 0 is enabled and that the PC has not matched the value contained in register PA_BKPT0[15:0]

1.3.1320 DOC_TRC_CFG

Trace Configuration Register

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DOC_TRC_CFG: 0x5024C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000				R/W:0	R/W:0	R/W:00	
HW Access	NA				R/W	R/W	R/W	
Retention	NA				RET	RET	RET	
Name	RSVD				TRC_FULL	TRC_FLTR	TRC_CNTRL	

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	TRC_PMEM							

The Trace Configuration register configures instruction trace

Bits	Name	Description
15:8	TRC_PMEM[7:0]	Trace Private Memory, this register is used to trace a register in private memory. TRC_PMEM contains the address of private memory data value that will be stored in the trace buffer when the TRC_FLTR is set to 0. The default of this register is 0, which corresponds to trace register 0 (R0)
3	TRC_FULL	Trace Full, when set to 1 the CPU is halted when the trace buffer is full, otherwise the trace buffer data continuously overlaps.
2	TRC_FLTR	Trace Filter, Sets filterable data for trace buffer, when set to .0. the trace buffer records the PC, the accumulator and a specified SFR or Internal memory location. The location depends on the value stored in the TRC_PMEM register. When set to .1. the trace buffer only records the PC value.
1:0	TRC_CNTRL[1:0]	Trace Control, enables trace, and configures trace buffer mode See Table 1-868.

Table 1-868. Bit field encoding: TRC_CNTRL_ENUM

Value	Name	Description
2'b00	trace_disabled	Trace Disabled
2'b01	run_cont	Run Continuously
2'b10	trig_point	Trigger point mode, when set 7th breakpoint comparator register is used a the trigger point
2'b11	win_mode	Window mode, when set the 7th and 8th breakpoint comparator register are used for window points

1.3.1321 DOC_PC

Program Counter

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DOC_PC: 0x5024E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	PC							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R/W:00000000							
HW Access	R/W							
Retention	RET							
Name	PC							

This program counter register acts as a place holder for the program coutner so that reads and writes to the PC can be accessed through the DoC using this addres

Bits	Name	Description
15:0	PC[15:0]	Current PC value on reads, new PC value for writes. The CPU must be halted to read or write the PC otherwise reads will return 0, and writes will have no effect

1.3.1322 DOC_CPU_RST

CPU reset

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DOC_CPU_RST: 0x50250

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	NA:0000000							R/W:0
HW Access	NA							R/W
Retention	NA							RET
Name	RSVD							RST

Virtural register for CPU reset

Bits	Name	Description
0	RST	Reset, when set to 1 the DoC holds the CPU in the reset state, when set to 0 the DoC releases the CPU from the reset state (does not override other reset signals).

1.3.1323 DOC_ENTR_TS

Entry Timestamp

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DOC_ENTR_TS: 0x50254

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	RET							
Name	TSTMP							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	RET							
Name	TSTMP							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	RET							
Name	TSTMP							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	RET							
Name	TSTMP							

Holds the number of clock cycles from the point trace is enabled and the cpu is running to the entry of the trace window when window mode is enabled

Bits	Name	Description
31:0	TSTMP[31:0]	Holds the number of clock cycles from the point trace is enabled and the cpu is running to the entry point of the trace window when window mode is enabled

1.3.1324 DOC_EXIT_TS

Exit Timestamp

Reset: System reset for retention flops [reset_all_retention]

Register : Address

DOC_EXIT_TS: 0x50258

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	RET							
Name	TSTMP							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	RET							
Name	TSTMP							

Bits	23	22	21	20	19	18	17	16
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	RET							
Name	TSTMP							

Bits	31	30	29	28	27	26	25	24
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	RET							
Name	TSTMP							

Holds the number of clock cycles from the time trace is enabled and the cpu is running to the exit of the window when window mode is enabled

Bits	Name	Description
31:0	TSTMP[31:0]	Holds the number of clock cycles from the time trace is enabled and the cpu is running to the exit of the window when window mode is enabled

1.3.1325 FLSHID_RSVD[0..127]

RSVD

Reset: N/A

Register : Address

FLSHID_RSVD: 0xC0000-0xC007F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	RSVD							

Bits	Name	Description
7:0	RSVD[7:0]	(no description)

1.3.1326 FLSHID_CUST_MDATA[0..127]

Customer Meta Data

Reset: N/A

Register : Address

FLSHID_CUST_MDATA: 0xC0080-0xC00FF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	cust_mdata							

Contains customer meta data such as information on the programmer used and the build number of the Cypress tool used. See Flash chapter for more information on the use of this field and a breakdown of the individual bytes

Bits	Name	Description
7:0	cust_mdata[7:0]	Customer Meta Data

1.3.1327 FLSHID_CUST_TABLES_Y_LOC

Y location

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_Y_LOC: 0xC0100

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	y_loc							

Y location of die on the wafer

Bits	Name	Description
7:0	y_loc[7:0]	Y location of die on the wafer (row number)

1.3.1328 FLSHID_CUST_TABLES_X_LOC

X location

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_X_LOC: 0xC0101

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	x_loc							

X location of die on the wafer

Bits	Name	Description
7:0	x_loc[7:0]	X location of die on the wafer (column number)

1.3.1329 FLSHID_CUST_TABLES_WAFER_NUM

Wafer Number

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_WAFER_NUM: 0xC0102

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	wafer_num							

Wafer Number

Bits	Name	Description
7:0	wafer_num[7:0]	Wafer Number: 1 to 24

1.3.1330 FLSHID_CUST_TABLES_LOT_LSB

Lot Number LSB

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_LOT_LSB: 0xC0103

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	lot_lsb							

Lot Number LSB

Bits	Name	Description
7:0	lot_lsb[7:0]	LSB of lot number/wafer start

1.3.1331 FLSHID_CUST_TABLES_LOT_MSB

Lot Number MSB

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_LOT_MSB: 0xC0104

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	lot_msb							

Lot Number MSB

Bits	Name	Description
7:0	lot_msb[7:0]	MSB of lot number/wafer start

1.3.1332 FLSHID_CUST_TABLES_WRK_WK

Work Week

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_WRK_WK: 0xC0105

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	work_week							

Work week

Bits	Name	Description
7:0	work_week[7:0]	Work week: 1 to 53

1.3.1333 FLSHID_CUST_TABLES_FAB_YR

Fab/Yr

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_CUST_TABLES_FAB_YR: 0xC0106

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:0000				R:0000			
HW Access	R/W				R/W			
Retention	RET				RET			
Name	year				fab			

Fab ID and Year Produced

Bits	Name	Description
7:4	year[3:0]	Year: 0 to 9
3:0	fab[3:0]	Fab Number: 4 or 5

1.3.1334 FLSHID_CUST_TABLES_MINOR

Minor Part Number

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_MINOR: 0xC0107

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	minor							

Marketing part number - minor

Bits	Name	Description
7:0	minor[7:0]	Marketing part number - minor: 000 to 999

1.3.1335 FLSHID_CUST_TABLES_IMO_3MHZ

IMO Trim - 3 MHz

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_IMO_3MHZ: 0xC0108

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	imo_3mhz							

IMO Frequency Trim - 3 MHz

Bits	Name	Description
7:0	imo_3mhz[7:0]	IMO Frequency Trim - 3 MHz: trim value to write to register IMO.TR1 to trim for 3 MHz setting

1.3.1336 FLSHID_CUST_TABLES_IMO_6MHZ

IMO Trim - 6 MHz

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_IMO_6MHZ: 0xC0109

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	imo_6mhz							

IMO Frequency Trim - 6 MHz

Bits	Name	Description
7:0	imo_6mhz[7:0]	IMO Frequency Trim - 6 MHz: trim value to write to register IMO.TR1 to trim for 6 MHz setting

1.3.1337 FLSHID_CUST_TABLES_IMO_12MHZ

IMO Trim - 12 MHz

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_IMO_12MHZ: 0xC010A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	imo_12mhz							

IMO Frequency Trim - 12 MHz

Bits	Name	Description
7:0	imo_12mhz[7:0]	IMO Frequency Trim - 12 MHz: trim value to write to register IMO.TR1 to trim for 12 MHz setting

1.3.1338 FLSHID_CUST_TABLES_IMO_24MHZ

IMO Trim - 24 MHz

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_IMO_24MHZ: 0xC010B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	imo_24mhz							

IMO Frequency Trim - 24 MHz

Bits	Name	Description
7:0	imo_24mhz[7:0]	IMO Frequency Trim - 24 MHz: trim value to write to register IMO.TR1 to trim for 24 MHz setting

1.3.1339 FLSHID_CUST_TABLES_IMO_67MHZ

IMO Trim - 67 MHz

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_IMO_67MHZ: 0xC010C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	imo_67mhz							

IMO Frequency Trim - 67 MHz

Bits	Name	Description
7:0	imo_67mhz[7:0]	IMO Frequency Trim - 67 MHz: trim value to write to register IMO.TR1 to trim for 67 MHz setting

1.3.1340 FLSHID_CUST_TABLES_IMO_80MHZ

IMO Trim - 80 MHz

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_IMO_80MHZ: 0xC010D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	imo_80mhz							

IMO Frequency Trim - 80 MHz

Bits	Name	Description
7:0	imo_80mhz[7:0]	IMO Frequency Trim - 80 MHz: trim value to write to register IMO.TR1 to trim for 80 MHz setting

1.3.1341 FLSHID_CUST_TABLES_IMO_92MHZ

IMO Trim - 92 MHz

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_IMO_92MHZ: 0xC010E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	imo_92mhz							

IMO Frequency Trim - 92 MHz

Bits	Name	Description
7:0	imo_92mhz[7:0]	IMO Frequency Trim - 92 MHz: trim value to write to register IMO.TR1 to trim for 92 MHz setting

1.3.1342 FLSHID_CUST_TABLES_IMO_USB

IMO Trim - USB Mode

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_IMO_USB: 0xC010F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	imo_usb							

IMO Frequency Trim - USB Mode

Bits	Name	Description
7:0	imo_usb[7:0]	IMO Frequency Trim - USB Mode: trim value to write to register IMO.TR1 to trim for USB mode setting

1.3.1343 FLSHID_CUST_TABLES_CMP0_TR0_HS

CMP0_TR0 High Speed

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_CMP0_TR0_HS: 0xC0110

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	cmp0_tr0_hs							

Trim for CMP0_TR0 for offset high speed mode (mode 1)

Bits	Name	Description
7:0	cmp0_tr0_hs[7:0]	Trim for CMP0_TR0 for offset high speed mode (mode 1)

1.3.1344 FLSHID_CUST_TABLES_CMP1_TR0_HS

CMP1_TR0 High Speed

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_CMP1_TR0_HS: 0xC0111

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	cmp1_tr0_hs							

Trim for CMP1_TR0 for offset high speed mode (mode 1)

Bits	Name	Description
7:0	cmp1_tr0_hs[7:0]	Trim for CMP1_TR0 for offset high speed mode (mode 1)

1.3.1345 FLSHID_CUST_TABLES_CMP2_TR0_HS

CMP2_TR0 High Speed

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_CMP2_TR0_HS: 0xC0112

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	cmp2_tr0_hs							

Trim for CMP2_TR0 for offset high speed mode (mode 1)

Bits	Name	Description
7:0	cmp2_tr0_hs[7:0]	Trim for CMP2_TR0 for offset high speed mode (mode 1)

1.3.1346 FLSHID_CUST_TABLES_CMP3_TR0_HS

CMP3_TR0 High Speed

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_CMP3_TR0_HS: 0xC0113

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	cmp3_tr0_hs							

Trim for CMP3_TR0 for offset high speed mode (mode 1)

Bits	Name	Description
7:0	cmp3_tr0_hs[7:0]	Trim for CMP3_TR0 for offset high speed mode (mode 1)

1.3.1347 FLSHID_CUST_TABLES_CMP0_TR1_HS

CMP0_TR1 High Speed

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_CMP0_TR1_HS: 0xC0114

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	cmp0_tr1_hs							

Trim for CMP0_TR1 for offset high speed mode (mode 1)

Bits	Name	Description
7:0	cmp0_tr1_hs[7:0]	Trim for CMP0_TR1 for offset high speed mode (mode 1)

1.3.1348 FLSHID_CUST_TABLES_CMP1_TR1_HS

CMP1_TR1 High Speed

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_CMP1_TR1_HS: 0xC0115

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	cmp1_tr1_hs							

Trim for CMP1_TR1 for offset high speed mode (mode 1)

Bits	Name	Description
7:0	cmp1_tr1_hs[7:0]	Trim for CMP1_TR1 for offset high speed mode (mode 1)

1.3.1349 FLSHID_CUST_TABLES_CMP2_TR1_HS

CMP2_TR1 High Speed

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_CMP2_TR1_HS: 0xC0116

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	cmp2_tr1_hs							

Trim for CMP2_TR1 for offset high speed mode (mode 1)

Bits	Name	Description
7:0	cmp2_tr1_hs[7:0]	Trim for CMP2_TR1 for offset high speed mode (mode 1)

1.3.1350 FLSHID_CUST_TABLES_CMP3_TR1_HS

CMP3_TR1 High Speed

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_CMP3_TR1_HS: 0xC0117

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	cmp3_tr1_hs							

Trim for CMP3_TR1 for offset high speed mode (mode 1)

Bits	Name	Description
7:0	cmp3_tr1_hs[7:0]	Trim for CMP3_TR1 for offset high speed mode (mode 1)

1.3.1351 FLSHID_CUST_TABLES_DEC_M1

Decimator Trim - Mode 1

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DEC_M1: 0xC0118

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dec_tr_m1							

Decimator Trim - Mode 1

Bits	Name	Description
7:0	dec_tr_m1[7:0]	Decimator Trim - Mode 1: Offset value to add to base decimator gain correction coefficient (GCOR). Value is 8-bit signed.

1.3.1352 FLSHID_CUST_TABLES_DEC_M2

Decimator Trim - mode 2

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DEC_M2: 0xC0119

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dec_tr_m2							

Decimator Trim - mode 2

Bits	Name	Description
7:0	dec_tr_m2[7:0]	Decimator Trim - mode 2: Offset value to add to base decimator gain correction coefficient (GCOR). Value is 8-bit signed.

1.3.1353 FLSHID_CUST_TABLES_DEC_M3

Decimator Trim - mode 3

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DEC_M3: 0xC011A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dec_tr_m3							

Decimator Trim - mode 3

Bits	Name	Description
7:0	dec_tr_m3[7:0]	Decimator Trim - mode 3: Offset value to add to base decimator gain correction coefficient (GCOR). Value is 8-bit signed.

1.3.1354 FLSHID_CUST_TABLES_DEC_M4

Decimator Trim - mode 4

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DEC_M4: 0xC011B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dec_tr_m4							

Decimator Trim - mode 4

Bits	Name	Description
7:0	dec_tr_m4[7:0]	Decimator Trim - mode 4: Offset value to add to base decimator gain correction coefficient (GCOR). Value is 8-bit signed.

1.3.1355 FLSHID_CUST_TABLES_DEC_M5

Decimator Trim - mode 5

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DEC_M5: 0xC011C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dec_tr_m5							

Decimator Trim - mode 5

Bits	Name	Description
7:0	dec_tr_m5[7:0]	Decimator Trim - mode 5: Offset value to add to base decimator gain correction coefficient (GCOR). Value is 8-bit signed.

1.3.1356 FLSHID_CUST_TABLES_DEC_M6

Decimator Trim - mode 6

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DEC_M6: 0xC011D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dec_tr_m6							

Decimator Trim - mode 6

Bits	Name	Description
7:0	dec_tr_m6[7:0]	Decimator Trim - mode 6: Offset value to add to base decimator gain correction coefficient (GCOR). Value is 8-bit signed.

1.3.1357 FLSHID_CUST_TABLES_DEC_M7

Decimator Trim - Mode 7

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DEC_M7: 0xC011E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dec_tr_m7							

Decimator Trim - Mode 7

Bits	Name	Description
7:0	dec_tr_m7[7:0]	Decimator Trim - Mode 7: Offset value to add to base decimator gain correction coefficient (GCOR). Value is 8-bit signed.

1.3.1358 FLSHID_CUST_TABLES_DEC_M8

Decimator Trim - Mode 8

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DEC_M8: 0xC011F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dec_tr_m8							

Decimator Trim - Mode 8

Bits	Name	Description
7:0	dec_tr_m8[7:0]	Decimator Trim - Mode 8: Offset value to add to base decimator gain correction coefficient (GCOR). Value is 8-bit signed.

1.3.1359 FLSHID_CUST_TABLES_DAC0_M1

DAC0_TR Trim - Mode 1

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DAC0_M1: 0xC0120

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dac0_m1							

DAC0_TR Trim - Mode 1

Bits	Name	Description
7:0	dac0_m1[7:0]	DAC0_TR Trim - Mode 1

1.3.1360 FLSHID_CUST_TABLES_DAC0_M2

DAC0_TR Trim - mode 2

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DAC0_M2: 0xC0121

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dac0_m2							

DAC0_TR Trim - mode 2

Bits	Name	Description
7:0	dac0_m2[7:0]	DAC0_TR Trim - mode 2

1.3.1361 FLSHID_CUST_TABLES_DAC0_M3

DAC0_TR Trim - mode 3

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DAC0_M3: 0xC0122

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dac0_m3							

DAC0_TR Trim - mode 3

Bits	Name	Description
7:0	dac0_m3[7:0]	DAC0_TR Trim - mode 3

1.3.1362 FLSHID_CUST_TABLES_DAC0_M4

DAC0_TR Trim - mode 4

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DAC0_M4: 0xC0123

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dac0_m4							

DAC0_TR Trim - mode 4

Bits	Name	Description
7:0	dac0_m4[7:0]	DAC0_TR Trim - mode 4

1.3.1363 FLSHID_CUST_TABLES_DAC0_M5

DAC0_TR Trim - mode 5

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DAC0_M5: 0xC0124

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dac0_m5							

DAC0_TR Trim - mode 5

Bits	Name	Description
7:0	dac0_m5[7:0]	DAC0_TR Trim - mode 5

1.3.1364 FLSHID_CUST_TABLES_DAC0_M6

DAC0_TR Trim - mode 6

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DAC0_M6: 0xC0125

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dac0_m6							

DAC0_TR Trim - mode 6

Bits	Name	Description
7:0	dac0_m6[7:0]	DAC0_TR Trim - mode 6

1.3.1365 FLSHID_CUST_TABLES_DAC0_M7

DAC0_TR Trim - mode 7

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DAC0_M7: 0xC0126

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dac0_m7							

DAC0_TR Trim - mode 7

Bits	Name	Description
7:0	dac0_m7[7:0]	DAC0_TR Trim - mode 7

1.3.1366 FLSHID_CUST_TABLES_DAC0_M8

DAC0_TR Trim - mode 8

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DAC0_M8: 0xC0127

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dac0_m8							

DAC0_TR Trim - mode 8

Bits	Name	Description
7:0	dac0_m8[7:0]	DAC0_TR Trim - mode 8

1.3.1367 FLSHID_CUST_TABLES_DAC2_M1

DAC2_TR Trim - Mode 1

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DAC2_M1: 0xC0128

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dac2_m1							

DAC2_TR Trim - Mode 1

Bits	Name	Description
7:0	dac2_m1[7:0]	DAC2_TR Trim - Mode 1

1.3.1368 FLSHID_CUST_TABLES_DAC2_M2

DAC2_TR Trim - mode 2

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DAC2_M2: 0xC0129

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dac2_m2							

DAC2_TR Trim - mode 2

Bits	Name	Description
7:0	dac2_m2[7:0]	DAC2_TR Trim - mode 2

1.3.1369 FLSHID_CUST_TABLES_DAC2_M3

DAC2_TR Trim - mode 3

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DAC2_M3: 0xC012A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dac2_m3							

DAC2_TR Trim - mode 3

Bits	Name	Description
7:0	dac2_m3[7:0]	DAC2_TR Trim - mode 3

1.3.1370 FLSHID_CUST_TABLES_DAC2_M4

DAC2_TR Trim - mode 4

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DAC2_M4: 0xC012B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dac2_m4							

DAC2_TR Trim - mode 4

Bits	Name	Description
7:0	dac2_m4[7:0]	DAC2_TR Trim - mode 4

1.3.1371 FLSHID_CUST_TABLES_DAC2_M5

DAC2_TR Trim - mode 5

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DAC2_M5: 0xC012C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dac2_m5							

DAC2_TR Trim - mode 5

Bits	Name	Description
7:0	dac2_m5[7:0]	DAC2_TR Trim - mode 5

1.3.1372 FLSHID_CUST_TABLES_DAC2_M6

DAC2_TR Trim - mode 6

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DAC2_M6: 0xC012D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dac2_m6							

DAC2_TR Trim - mode 6

Bits	Name	Description
7:0	dac2_m6[7:0]	DAC2_TR Trim - mode 6

1.3.1373 FLSHID_CUST_TABLES_DAC2_M7

DAC2_TR Trim - mode 7

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DAC2_M7: 0xC012E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dac2_m7							

DAC2_TR Trim - mode 7

Bits	Name	Description
7:0	dac2_m7[7:0]	DAC2_TR Trim - mode 7

1.3.1374 FLSHID_CUST_TABLES_DAC2_M8

DAC2_TR Trim - mode 8

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DAC2_M8: 0xC012F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dac2_m8							

DAC2_TR Trim - mode 8

Bits	Name	Description
7:0	dac2_m8[7:0]	DAC2_TR Trim - mode 8

1.3.1375 FLSHID_CUST_TABLES_DAC1_M1

DAC1_TR Trim - Mode 1

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DAC1_M1: 0xC0130

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dac1_m1							

DAC1_TR Trim - Mode 1

Bits	Name	Description
7:0	dac1_m1[7:0]	DAC1_TR Trim - Mode 1

1.3.1376 FLSHID_CUST_TABLES_DAC1_M2

DAC1_TR Trim - mode 2

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DAC1_M2: 0xC0131

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dac1_m2							

DAC1_TR Trim - mode 2

Bits	Name	Description
7:0	dac1_m2[7:0]	DAC1_TR Trim - mode 2

1.3.1377 FLSHID_CUST_TABLES_DAC1_M3

DAC1_TR Trim - mode 3

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DAC1_M3: 0xC0132

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dac1_m3							

DAC1_TR Trim - mode 3

Bits	Name	Description
7:0	dac1_m3[7:0]	DAC1_TR Trim - mode 3

1.3.1378 FLSHID_CUST_TABLES_DAC1_M4

DAC1_TR Trim - mode 4

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DAC1_M4: 0xC0133

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dac1_m4							

DAC1_TR Trim - mode 4

Bits	Name	Description
7:0	dac1_m4[7:0]	DAC1_TR Trim - mode 4

1.3.1379 FLSHID_CUST_TABLES_DAC1_M5

DAC1_TR Trim - mode 5

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DAC1_M5: 0xC0134

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dac1_m5							

DAC1_TR Trim - mode 5

Bits	Name	Description
7:0	dac1_m5[7:0]	DAC1_TR Trim - mode 5

1.3.1380 FLSHID_CUST_TABLES_DAC1_M6

DAC1_TR Trim - mode 6

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DAC1_M6: 0xC0135

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dac1_m6							

DAC1_TR Trim - mode 6

Bits	Name	Description
7:0	dac1_m6[7:0]	DAC1_TR Trim - mode 6

1.3.1381 FLSHID_CUST_TABLES_DAC1_M7

DAC1_TR Trim - mode 7

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DAC1_M7: 0xC0136

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dac1_m7							

DAC1_TR Trim - mode 7

Bits	Name	Description
7:0	dac1_m7[7:0]	DAC1_TR Trim - mode 7

1.3.1382 FLSHID_CUST_TABLES_DAC1_M8

DAC1_TR Trim - mode 8

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DAC1_M8: 0xC0137

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dac1_m8							

DAC1_TR Trim - mode 8

Bits	Name	Description
7:0	dac1_m8[7:0]	DAC1_TR Trim - mode 8

1.3.1383 FLSHID_CUST_TABLES_DAC3_M1

DAC3_TR Trim - Mode 1

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DAC3_M1: 0xC0138

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dac3_m1							

DAC3_TR Trim - Mode 1

Bits	Name	Description
7:0	dac3_m1[7:0]	DAC3_TR Trim - Mode 1

1.3.1384 FLSHID_CUST_TABLES_DAC3_M2

DAC3_TR Trim - mode 2

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DAC3_M2: 0xC0139

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dac3_m2							

DAC3_TR Trim - mode 2

Bits	Name	Description
7:0	dac3_m2[7:0]	DAC3_TR Trim - mode 2

1.3.1385 FLSHID_CUST_TABLES_DAC3_M3

DAC3_TR Trim - mode 3

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DAC3_M3: 0xC013A

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dac3_m3							

DAC3_TR Trim - mode 3

Bits	Name	Description
7:0	dac3_m3[7:0]	DAC3_TR Trim - mode 3

1.3.1386 FLSHID_CUST_TABLES_DAC3_M4

DAC3_TR Trim - mode 4

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DAC3_M4: 0xC013B

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dac3_m4							

DAC3_TR Trim - mode 4

Bits	Name	Description
7:0	dac3_m4[7:0]	DAC3_TR Trim - mode 4

1.3.1387 FLSHID_CUST_TABLES_DAC3_M5

DAC3_TR Trim - mode 5

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DAC3_M5: 0xC013C

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dac3_m5							

DAC3_TR Trim - mode 5

Bits	Name	Description
7:0	dac3_m5[7:0]	DAC3_TR Trim - mode 5

1.3.1388 FLSHID_CUST_TABLES_DAC3_M6

DAC3_TR Trim - mode 6

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DAC3_M6: 0xC013D

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dac3_m6							

DAC3_TR Trim - mode 6

Bits	Name	Description
7:0	dac3_m6[7:0]	DAC3_TR Trim - mode 6

1.3.1389 FLSHID_CUST_TABLES_DAC3_M7

DAC3_TR Trim - mode 7

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DAC3_M7: 0xC013E

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dac3_m7							

DAC3_TR Trim - mode 7

Bits	Name	Description
7:0	dac3_m7[7:0]	DAC3_TR Trim - mode 7

1.3.1390 FLSHID_CUST_TABLES_DAC3_M8

DAC3_TR Trim - mode 8

Reset: N/A

Register : Address

FLSHID_CUST_TABLES_DAC3_M8: 0xC013F

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	dac3_m8							

DAC3_TR Trim - mode 8

Bits	Name	Description
7:0	dac3_m8[7:0]	DAC3_TR Trim - mode 8

1.3.1391 FLSHID_MFG_CFG_IMO_TR1

IMO_TR1 Trim

Reset: System reset for retention flops [reset_all_retention]

Register : Address

FLSHID_MFG_CFG_IMO_TR1: 0xC0188

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:10100001							
HW Access	R/W							
Retention	RET							
Name	addr							

Bits	15	14	13	12	11	10	9	8
SW Access:Reset	R:00000000							
HW Access	R/W							
Retention	RET							
Name	data							

IMO Trim for 48 MHz frequency setting

Bits	Name	Description
15:8	data[7:0]	Data byte to write to address
7:0	addr[7:0]	Address offset to add to 0x4600

1.3.1392 FLS_DATA[0..65535]

FLASH Data

Reset: N/A

Register : Address

FLS_DATA: 0x100000-0x10FFFF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R:UUUUUUUU							
HW Access	R/W							
Retention	RET							
Name	data							

FLASH data. 8051 may access only through extended data space.

Bits	Name	Description
7:0	data[7:0]	FLASH data

1.3.1393 EXTMEM_DATA[0..8388607]

DATA

Reset: N/A

Register : Address

EXTMEM_DATA: 0x800000-0xFFFFFF

Bits	7	6	5	4	3	2	1	0
SW Access:Reset	R/W:UUUUUUUU							
HW Access	R/W							
Retention	NONRET							
Name	data							

Bits	Name	Description
7:0	data[7:0]	(no description)

Revision History

Revision History

Document Title: PSoC® 3 REGISTERS TRM (TECHNICAL REFERENCE MANUAL) Document Number: 001-50581			
Revision	**ECN#**	**Issue Date**	**Description of Change**
**	2658937	01/05/2009	Initial internal publication.
*A	2622249	02/17/2009	ES10 update.
*B	2738258	07/14/2009	Initial external publication, non NDA.
*C	2762360	09/10/2009	Incorporated updates through 09/09/2009.
*D	3117373	12/23/2010	Incremental Edit
*E	3634126	06/01/2012	Incorporated updates through 05/31/2012.
*F	4136831	09/26/2013	Incorporated updates through 09/25/2013
*G	4247592	01/15/2014	Incorporated updates through 01/15/2014
*H	4446627	07/17/2014	Incorporated updates through 07/16/2014
*I	4813026	06/30/2015	Updated avail_main in PM_AVAIL_CR4 Register Updated vsel_enum (vsel[4:0]) in BOOST_CR0 Register Updated nobat in BOOST_SR Register Updated CMP[0..3]_TR0 and CMP[0..3]_TR1 Registers Updated wait[1:0], delay[1:0], lockdet ilock changed to high_phase_error for FASTCLK_PLL_CFG0 and FASTCLK_PLL_SR Registers Updated extmode, clk_ilo, and clk_eco for BOOST_CR1 and BOOST_CR4 Registers Updated bitfield description in CAN_TX_CMD and CAN_RX_CMD registers.
*J	5758771	01/06/2017	Updated logo and copyright information
*K	6836882	03/25/2020	Updated 1.3.344 SC[0..3]_CR0 register. Completing the Sunset review.