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FM3 Family, MB9AF0A1M Peripheral Manual Sensor Microcontroller Part

Doc. No. 002-07831 Rev. *A

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Preface

Thank you for your continued use of Cypress semiconductor products. Read "Peripheral manual" and "Data Sheet" thoroughly before using products in this product.

This manual has indicated the difference function to a related manual (four volumes).

- **Purpose of this manual and intended readers**

This manual explains the functions and operations of this product and describes how it is used. The manual is intended for engineers engaged in the actual development of products using this product.

* This manual explains the configuration and operation of the peripheral functions, but does not cover the specifics of each device in the series.
Users should refer to the respective data sheets of devices for device-specific details.

- **Overall Organization of This Manual**

Peripheral Manual Sensor Microcontroller Part has 8 chapters and APPENDIX as shown below.

CHAPTER 1: System Overview

CHAPTER 2 : Low Power Consumption Mode

CHAPTER 3 : I/O Port

CHAPTER 4 : Base Timer I/O Select Function

CHAPTER 5 : PGA

CHAPTER 6 : CSIO (Clock Synchronous Serial Interface)

CHAPTER 7 : IrDA

CHAPTER 8 : Feedthrough

APPENDIX

Please read the following chapters from "Peripheral manual".

Chapter System Overview
Chapter Low Power Consumption Mode
Chapter I/O Port

Please read the following chapters form "Timer Part".

Chapter Base Timer I/O Select Function

Please read the following chapters form "Communication Macro Part".

Chapter CSIO (Clock Synchronous Serial Interface)

* : However, this product is classification of TYPE6 product, it has not built-in the USB function.

Related Manuals

The manuals related to this product are listed below. See the manual appropriate to the applicable conditions.

The contents of these manuals are subject to change without notice. Contact us to check the latest versions available.

- **Peripheral Manual**
  - ☐ FM3 Family PERIPHERAL MANUAL

    (Called "PERIPHERAL MANUAL" hereafter)
  - ☐ FM3 Family PERIPHERAL MANUAL Timer Part

    (Called "Timer Part" hereafter)
  - ☐ FM3 Family PERIPHERAL MANUAL Analog Macro Part

    (Called "Analog Macro Part" hereafter)
  - ☐ FM3 Family PERIPHERAL MANUAL Communication Macro Part

    (Called "PERIPHERAL MANUAL" hereafter)
  - ☐ FM3 Family MB9AF0A1M PERIPHERAL MANUAL Sensor Microcontroller Part (this manual)
- **Data sheet**

For details about device-specific, electrical characteristics, package dimensions, ordering information etc., see the following document.

- ☐ 32-bit Microcontroller FM3 Family MB9AF0A1M DATA SHEET

- **CPU Programming manual**

For details about ARM Cortex-M3 core, see the following documents that can be obtained from http://www.arm.com

- ☐ Cortex-M3 Technical Reference Manual
- ☐ ARMv7-M Architecture Application Level Reference Manual

- **Flash Programming manual**

For details about the functions and operations of the built-in flash memory, see the following document.

- ☐ FM3 Family MB9AF0A1M PROGRAMMING MANUAL

How to Use This Manual

- **Finding a function**

The following methods can be used to search for the explanation of a desired function in this manual:

Search from the table of the contents

The table of the contents lists the manual contents in the order of description.

Search from the register

The address where each register is located is not described in the text. To verify the address of a register, see "1. Register Map" in "APPENDIX".

- **About the chapters**

Basically, this manual explains 1 peripheral function per chapter.

■ Terminology

This manual uses the following terminology.

Term	Explanation
Word	Indicates access in units of 32 bits.
Half word	Indicates access in units of 16 bits.
Byte	Indicates access in units of 8 bits.

■ Notations

☐ The notations in bit configuration of the register explanation of this manual are written as follows.

- bit : bit number
- Field : bit field name
- Attribute : Attributes for read and write of each bit

R : Read only

W : Write only

R/W : Readable/Writable

\- : Undefined

- Initial value : Initial value of the register after reset

0 : Initial value is "0"

1 : Initial value is "1"

X : Initial value is undefined

☐ The multiple bits are written as follows in this manual.
Example : bit7:0 indicates the bits from bit7 to bit0

☐ The values such as for addresses are written as follows in this manual.

Hexadecimal number (example : 0xFFFF) :"0x" is attached in the beginning of a value as a prefix

Binary number (example: 0b1111) : "0b" is attached in the beginning of a value as a prefix

Decimal number : Written using numbers only (example : 1000)

This product is classification of TYPE6 product
* : However, This product has not built-in the USB function.

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1. System Overview

This chapter explains the system overview.

1.1 Bus Architecture

1.2 Cortex-M4F Architecture

1.3 Memory Map

1.1 Bus Architecture

This section explains the bus architecture.

For this product bus, AHB Bus Matrix circuit actualizes a multi-layer bus. Master and slave architectures are shown below:

Master

- ☐ Cortex-M3 CPU(I-code Bus, D-code Bus, System Bus)
- ☐ DMAC

Slave

- ☐ On-chip Flash Memory (MainFlash, WorkFlash)
- ☐ On-chip SRAM (SRAM0, SRAM1)
- ☐ RAC
- ☐ AHB-AHB Bus Bridge
- ☐ AHB-APB Bus Bridge (APB0 to APB2)

See Bus Block Diagram for the bus block diagram.

- Features

  ☐ RAM Architecture

  This product divides the on-chip SRAM area into two separate SRAM (SRAM0 and SRAM1). SRAM0 is connected to the I-Code bus and D-Code bus of the Cortex-M3 core. SRAM1 is connected to the System bus of the Cortex-M3 core. Also, SRAM0 and SRAM1 are connected to DMAC and other bus masters. This allows for preventing conflicts to RAM by multiple bus masters such as CPU and DMAC and allows for improving the performance.
  Also, because the divided RAM address areas are serial, RAM area can be utilized to the maximum extent.

  ☐ APB Extension Bus

  APB1 and APB2 Peripheral Buses are APB extension bus that the following functions are originally added based on AMBA3.0. (APB0 is not included.)

  - Supporting Halfword (16 bits) and Byte (8 bits) Accesses

  For supported registers, halfword access and byte access are enabled.
  See "1. Register Map" in "APPENDIX" for the supported registers.

  - Adding Read-Modify-Write (RMW) Signal

  HMASTLOCK signal in bit-band operations is used to generate.

  RMW signal is a signal added to prevent that an unrelated flag is cleared mistakenly in read-modify-write process of bit-band operations.
  The corresponding flag reads "1" in read during the read-modify-write process and is designed to ignore "1" write. This prevents any unrelated flag from being mistakenly cleared in the next write when the flag is set immediately after the read in the sequence from read to modify to write.

  For the corresponding flags and registers, it is described that "regardless of bit values, "1" can be read in "Read-Modify-Write".

Notes:

- Bit-band operation must not be performed to a register which RMW is prohibited.
- When Read-Modify-Write process is performed over the software without bit-band operation, RMW signal is not output.

  Therefore, in this case, the flag value can be read in read operation although a register supports RMW process, and it is necessary not to be cleared an unrelated flag mistakenly in write operation.
- For the details of bit-band operations, see the Cortex-M4 Technical Reference Manual.

☐ Power on

With the WLCSP package of this product, core voltage is supplied from the exterior by no regulator.

When power on / power off of power supply, perform power on / power off in simultaneous or the following order.

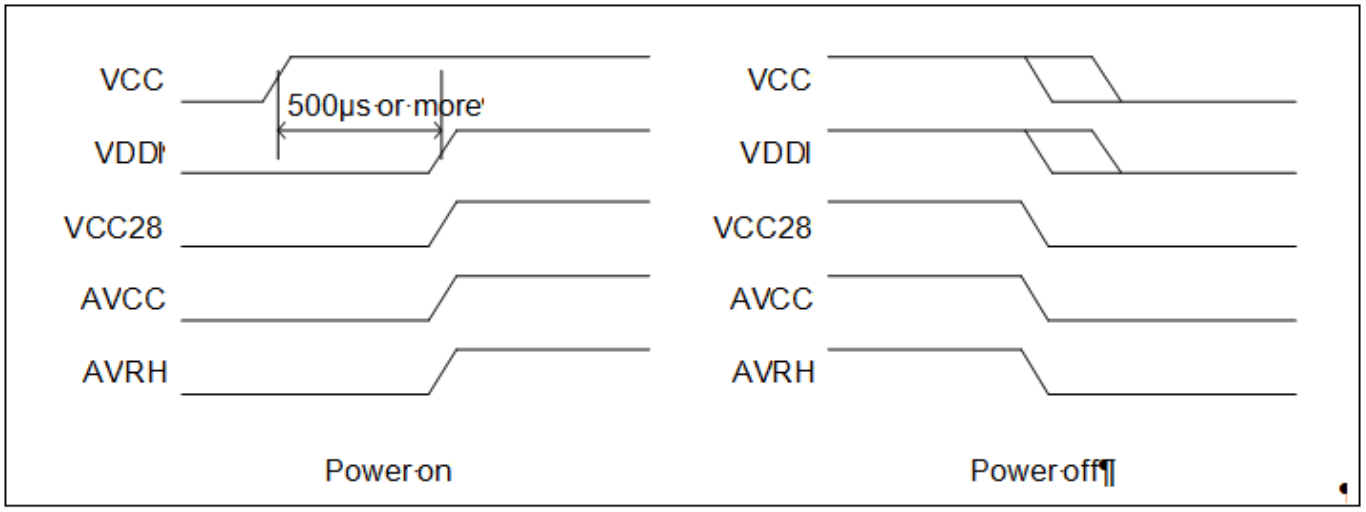
In addition, when not use A/D converter, please connect with an AVCC=VCC28 level and an AVSS=VSS level.

The time of 500 µs or more is required for VCC->VDDI at power on.

Power on : VCC -> (500 µs) -> VDDI -> VCC28 -> AVCC -> AVRH

Power off : AVRH -> AVCC -> VCC28 -> VDDI, VCC (there is no specification order of power off.)

Figure 1- 1. Power On Power off



☐ Priority Level

According to DMAC access settings such as a case where DMAC is always accessed by a burst transfer, access to CPU may be controlled. Please pay extra attention to DMAC transfer settings.

A priority of the bus right is determined in round-robin fashion.

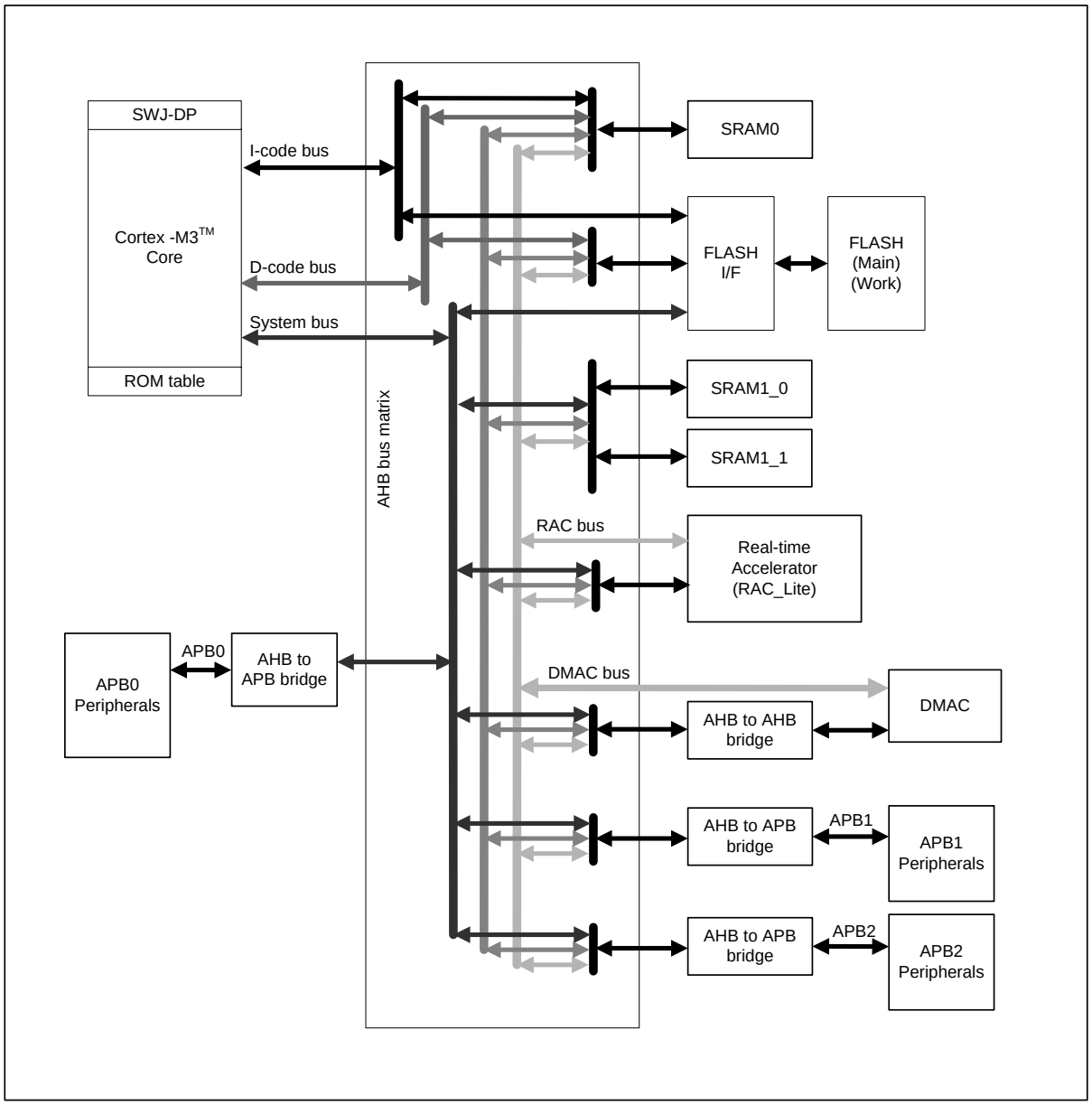
☐ Endian

This product uses Little endian byte order.

1.1.1 Bus Block Diagram

Figure 1- 2 illustrates the bus block diagram.

Figure 1- 2. Bus Block Diagram



Note:

There are some areas to which no DMAC transfer can be performed. For details, see the DMAC Transfer column in Table-1-1

1.1.2 Memory Architecture

This section shows the memory architecture.

For this family, 4G-byte address space is available.

256 Kbyte Main FLASH memory, 32 Kbyte WorkFlash memory, 16 Kbyte SRAM0 area, and 32 Kbyte SRAM1 area (each 16Kbyte control power supply) are defined.

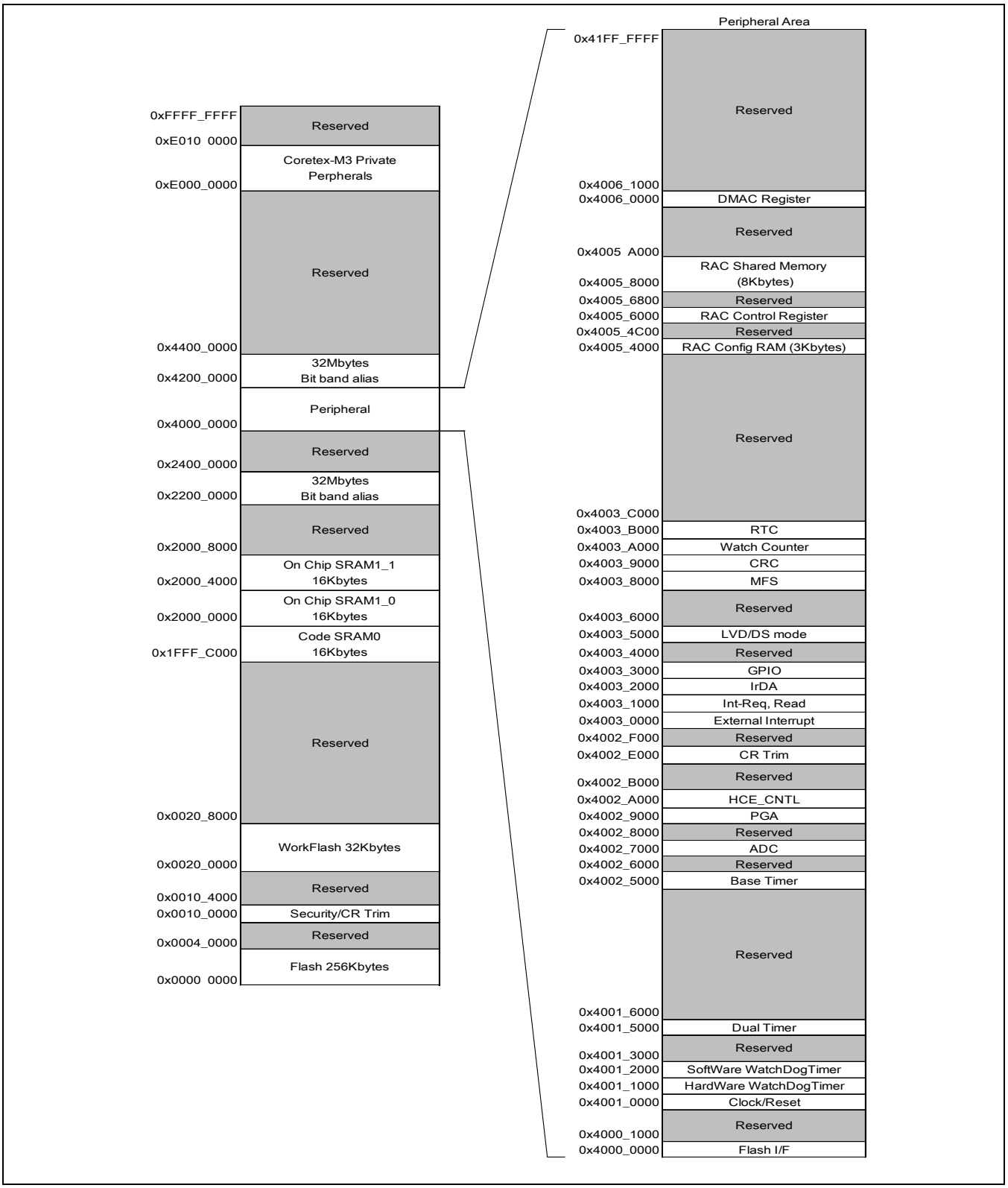
Section "1.1.3 Memory Map" illustrates the memory map, and Section "1.1.4 Peripheral Address Map " illustrates the peripheral address map.

For the details of Cortex-M3 private peripheral area and bit-band area shown in, 1.2 Cortex-M4F Architecture see "Cortex-M3 Technical Reference Manual".

1.1.3 Memory Map

Figure 1- 3 illustrates the memory map.

Figure 1- 3. Memory Map



Note:

- Do not access to reserved area.
- For the details of flash memory, see "MB9AF0A1M FLASH PROGRAMMING MANUAL" of the product used.

1.1.4 Peripheral Address Maps

Table 1 1 shows the peripheral address map.

Table 1-1. Peripheral Address Map

Start Address	End Address	Bus	DMACTransfer	Peripheral	Register Map	CHAPTER
0x4000_0000	0x4000_0FFF	AHB	Disabled	FLASH IF Register (Main)	FLASH_IF	*1
0x4000_1000	0x4000_FFFF			Reserved	-	-
0x4001_0000	0x4001_0FFF	APB0	Disabled	Clock and Reset Control	Clock / Reset	*2
0x4001_1000	0x4001_1FFF			Hardware Watchdog Timer	HWWDT	*3
0x4001_2000	0x4001_2FFF			Software Watchdog Timer	SWWDT	*3
0x4001_3000	0x4001_4FFF			Reserved	-	-
0x4001_5000	0x4001_5FFF			Dual Timer	Dual_ Timer	*3
0x4001_6000	0x4001_FFFF			Reserved	-	-
0x4002_0000	0x4002_4FFF	APB1	Enabled	Reserved	-	-
0x4002_5000	0x4002_5FFF			Base Timer	Base Timer/ Base Timer Selector	*3 Chapter 3
0x4002_6000	0x4002_6FFF			Reserved	-	-
0x4002_7000	0x4002_7FFF			A/D Converter	A/DC	*4
0x4002_8000	0x4002_8FFF			Reserved	-	-
0x4002_9000	0x4002_9FFF			PGA	PGA	Chapter 4
0x4002_A000	0x4002_AFFF			Feedthrough	FTH	Chapter 7
0x4002_B000	0x4002_DFFF			Reserved	-	-

Start Address	End Address	Bus	DMACTransfer	Peripheral	Register Map	CHAPTER
0x4002_E000	0x4002_EFFF			High Speed CR trmming	CR trim	*2
0x4002_F000	0x4002_FFFF			Reserved	-	-
0x4003_0000	0x4003_0FFF	APB2	Enabled	External Interrupt	EXTI	*2
0x4003_1000	0x4003_1FFF			Interrupt Factor Check Register	INT-Req READ	*2
0x4003_2000	0x4003_2FFF			IrDA	IrDA	Chapter 6
0x4003_3000	0x4003_3FFF			GPIO	GPIO	*2
0x4003_4000	0x4003_4FFF			Reserved	-	-
0x4003_5000	0x4003_50FF			Low Voltage Detection	LVD	*2
0x4003_5100	0x4003_5FFF			Deep standby control block	DS_Mode	Chapter 2
0x4003_6000	0x4003_7FFF			Reserved	-	-
0x4003_8000	0x4003_8FFF	APB2	Enabled	Multi-function serial	MFS	*2 Chapter 4
0x4003_9000	0x4003_9FFF			CRC	CRC	*2
0x4003_A000	0x4003_AFFF			Watch counter	Watch Counter	*3
0x4003_B000	0x4003_EFFF			Real time clock	RTC	*3
0x4003_F000	0x4003_FFFF			Reserved	-	-
0x4004_0000	0x4005_3FFF	AHB	Enabled	Reserved	-	-
0x4005_4000	0x4005_9FFF			RAC	RAC	-
0x4005_A000	0x4005_FFFF			Reserved	-	-
0x4006_0000	0x4006_0FFF			DMAC Register	DMAC	*2
0x4006_1000	0x41FF_FFFF			Reserved	-	-

*1 For the details of "FLASH IF Register", see "MB9AF0A1M FLASH PROGRAMMING MANUAL".

*2 For the details of "PERIPHERAL MANUAL".

*3 For the details of "Timer Part".

*4 For the details of "Analog Macro Part".

*5 For the details of "Communication Macro Part".

Start Address	End Address	Bus	DMAC Transfer	Peripheral	Register Map	Details
0x200E_0000	0x200E_1000	AHB	Enabled	Flash IF register (Work)	"FLASH IF"	*6

*6 For the details of "FLASH IF register (Work)", see " MB9AF0A1M FLASH PROGRAMMING MANUAL".

1.2 Cortex-M4F Architecture

This section explains the core architecture used in S6E2F34G0A.

Cortex-M3 core block architecture* used in this product is as follows:

Cortex-M3 Core

NVIC

MPU

DWT

ITM

FPB

ETM

SWJ-DP

ROM Table

- **Cortex-M3 Core**

  High-performance 32-bit processor core (ARM Cortex-M3 core) is equipped with this product.
  This manual does not describe the details of Cortex-M3 core.
  For the details, see "Cortex-M3 Technical Reference Manual".

  ☐ Cortex-M3 Core Version

  For the version of Cortex-M3 core, See "Data sheet" of the product used.

- **NVIC (Nested Vectored Interrupt Controller)**

  For this product, one NMI (non-maskable interrupt) and maximum 48 peripheral interrupts (IRQ0 to IRQ47)*[1] can be used.
  Also, interrupt priority register (from 0xE000E400) is comprised of 4 bits, and 16 interrupt priority levels can be configured.

  For the details of peripheral interrupts, see another chapter "Interrupts" in "PERIPHERAL MANUAL",
  and for NMI operations, see also another chapter "External Interrupt and NMI Control Block" in "PERIPHERAL MANUAL".

  NMI pin is assigned for a combined use with a general-purpose port. Its initial value after a reset release is set to the general-purpose port, and NMI input is masked.
  When NMI is used, enable NMI in the port setting.
  For the details, see another chapter "I/O Port" in "PERIPHERAL MANUAL".

  *1: "Cortex-M3 Technical Reference Manual" defines an exception type: IRQ as an external interrupt.
  In this peripheral manual, to distinguish from an interrupt by an external pin "External Interrupt and NMI Control Block," the exception type: IRQ is indicated as a peripheral interrupt.

  ☐ **SysTick Timer**

  SysTick Timer is a system timer for OS task management integrated into NVIC.

  This product generates STCLK through dividing HCLK by eight and sets the values of SysTick Calibration Value Register (Address: 0xE000E01C) as shown below:

  bit31 : NOREF = 0

  bit30 : SKEW = 1

  bit23:0 : TENMS = 0x0186A0 (100000)*[1]

  *[1] : TENMS value is set to a value which becomes 10 ms when 1/8 clock of HCLK is input to STCLK and that HCLK is in 80 MHz (10 MHz in 1/8 case).
  The value of TENMS is not always 10ms because HCLK can be changed to another frequency in the clock control block. Therefore, it is required to calculate an appropriate interrupt timing according to HCLK frequency.

- **DWT (Data Watch point & Trace Unit)**

  This family is equipped with DWT to use as the debug function.
  DWT contains four comparators, and each comparator can be set as a hardware watch point.

- **ITM (Instrumentation Trace Macro cell)**

  This product is equipped with ITM as a debug function.
  ITM is an optional application driven trace source that supports printf style debugging. The operation system (OS) and application event are traced, and the system diagnostic information is sent.

- **FPB (Flash Patch & Breakpoint)**

  FPB has the following functions:

  - ☐ Hardware Breakpoint function
  - ☐ The function of remapping from Code memory space (FLASH) to SRAM space.

  FPB is equipped with six instruction comparators and two literal comparators.

- **MPU (Memory Protection Unit)**

  This product is equipped with a Cortex-M3 optional component MPU, and maximum eight areas can be defined.

- **ETM (Embedded Trace Macro cell)**

  This product is equipped with a Cortex-M3 optional component ETM to support instruction trace.

- **SWJ-DP**

  This product is equipped with SWJ-DP to support both serial wire protocol and JTAG protocol.

- **ROM Table**

  ROM table provides the address information of a debug component to an external debug tool.

1.3 Mode

This section explains the function of operating modes.

In this product, the following operating modes can be used:

- User Mode

  Internal ROM (Flash) Startup : CPU obtains a reset vector from Flash memory and starts operations.

- Serial Writer Mode

  Flash serial write is enabled.
  * : For the details of this mode, see "MA9AF0A1M PROGRAMMING MANUAL" of the product used.

Operating modes are determined after a release of respective power-on reset, low voltage detection reset, and INITX pin input reset.

* : For the details of power consumption control and clock selection modes, see other chapters "Low Power Consumption Mode" and "Clock" in "PERIPHERAL MANUAL".

How to Set Operating Mode

Operating modes are configured by MD pins' (MD1 and MD0) inputs.

MD Pins		Operating Mode
MD1	MD0	
-	0	User Mode Internal ROM(Flash) Startup
0	1	Serial Writer Mode
1	1	Setting is prohibited.

Startup Sequence

Processes to determine operating modes in the startup sequence are shown below:

1. MD Pin Sampling
2. Determining Operating Mode and Retaining Mode Data

The descriptions of these processes are as follows:

- MD Pin Sampling

  Operating mode is configured by MD pin inputs (MD1, MD0). These inputs are sampled by power-on reset, low-voltage detection reset, and INITX pin input reset.
  Until each reset, which is the sampling factor, is released, MD1 and MD0 pin inputs need to be determined.

- Determining Operating Mode and Retaining Mode Data

  MD1 and MD0 which are sampled by respective resets are retained until respective resets are input again.
  Operating modes are determined by the retained MD1 and MD0. Therefore, even MD1 and MD0 are changed after a reset is released, it does not affect an operating mode.

MD1 pin

MD1 pin is used also as GPIO. This pin can be continually used as GPIO after setting a mode.

2. Low Power Consumption Mode

This chapter explains the system overview.

2.1 Overview of Low Power Consumption Mode
2.2 Configuration of CPU Operation Modes
2.3 Operations of Standby Modes
2.4 Standby Mode Setting Procedure Examples
2.5 Description of Deep Standby Mode Operation
2.6 Deep Standby Mode Setting Procedure Examples
2.7 Deep Standby Return Factor Determination Procedure
2.8 Power Supply OFF/SLEEP for Every Power Supply Domain by Register Control
2.9 List of Low Power Consumption Mode Registers
2.10 Usage Precautions

2.1 Overview of Low Power Consumption Mode

To reduce the power consumption, the system provides low power consumption mode, which enables the use of the standby mode of SLEEP, TIMER, RTC and STOP modes and the deep standby mode of deep standby RTC and deep standby STOP modes.
FLASH, RAM0, RAM1_0, RAM1_1, RAC of Power supply OFF, or SLEEP by register setting.

Overview of CPU operation modes

CPU operation modes are classified into the following types.

- **Run modes**
  - High speed CR run mode
  - Main run mode
  - PLL run mode
  - Low speed CR run mode
  - Sub run mode
- **Standby modes**
  - Sleep modes
    - High speed CR sleep mode
    - Main sleep mode
    - PLL sleep mode
    - Low speed CR sleep mode
    - Sub sleep mode
  - Timer modes
    - High speed CR timer mode
    - Main timer mode
    - PLL timer mode
    - Low speed CR timer mode
    - Sub timer mode
  - RTC mode
  - STOP mode
- **Deep Standby modes**
  - Deep Standby RTC mode
  - Deep Standby STOP mode

Low Power Consumption Modes

Low Power Consumption has operation modes are classified into the following types

- **Standby Modes**
  - Sleep Mode
  - Timer Mode
  - RTC Mode
  - STOP Mode
- **Deep Standby Modes**
  - Deep Standby RTC Mode

- ☐ Deep Standby RTC Mode (On-chip SRAM retention)
- ☐ Deep Standby STOP Mode
- ☐ Deep Standby STOP Mode (On-chip SRAM retention)

Overview of RUN mode

RUN mode is defined with a clock selected as a master clock. The base clocks, which are obtained by dividing the master clock frequency, are supplied to CPU clock, AHB bus clock, and APB bus clock to run the CPU, buses, and most peripherals.

The source clock frequency can be changed dynamically. When not using the main or sub oscillator, the source clock oscillator can be stopped.

RUN mode is divided into the following modes depending on the clock selected as a master clock.

- **High speed CR run mode**

  In this mode, the high speed CR oscillator clock is used as a master clock. When not using the main or sub oscillator, the respective oscillators can be stopped. The status of PLL Multiplier Circuit varies depending on the setting of the PLLE bit. The low speed CR oscillator is always set to the active state. It changes to this mode after a reset has been released.

- **Main run mode**

  In this mode, the main oscillator clock is used as a master clock. The status of the PLL Multiplier Circuit or sub oscillator varies depending on the setting of the PLLE or SOSCE bit. The high and low speed CR oscillators are always set to the active state.

- **PLL run mode**

  In this mode, the PLL clock obtained by multiplying the main oscillator clock or high speed CR oscillator clock is used as a master clock. The main, high speed CR, and low speed CR oscillators are always set to the active state. The status of the main or sub oscillator varies depending on the setting of the MOSCE or SOSCE bit.

- **Low speed CR run mode**

  In this mode, the low speed CR oscillator clock is used as a master clock. The status of the sub oscillator varies depending on the setting of the SOSCE bit. The main oscillator, high speed CR oscillator, and PLL Multiplier Circuit are not available in this mode.

- **Sub run mode**

  In this mode, the sub oscillator clock is used as a master clock. The low speed CR oscillator is always set to the active state. The main oscillator, high speed CR oscillator, and PLL Multiplier Circuit are not available in this mode.

Overview of SLEEP mode

SLEEP mode is classified as one of standby modes. SLEEP mode is used to stop CPU clocks. This causes the CPU to be stopped, reducing the power consumption. The resources connected to the AHB and APB bus clocks continue operations.

SLEEP mode is divided into the following modes depending on a master clock at the transition to SLEEP mode.

- **High speed CR sleep mode**

  When the high speed CR oscillator clock is selected as a master clock, the system changes to high speed CR sleep mode if the transition to SLEEP mode is requested. In this mode, the status of the PLL Multiplier Circuit, main or sub oscillator varies depending on the setting of the PLLE, MOSCE or SOSCE bit. The low speed CR oscillator is always set to the active state.

- **Main sleep mode**

  When the main clock is selected as a master clock, the system changes to main sleep mode if the transition to SLEEP mode is requested. In this mode, the status of the PLL Multiplier Circuit or sub oscillator varies depending on the setting of the PLLE or SOSCE bit. The high and low speed CR oscillators are always set to the active state.

- **PLL sleep mode**

  When the main PLL clock is selected as a master clock, the system changes to PLL sleep mode if the transition to SLEEP mode is requested. In this mode, the main, high speed CR, and low speed CR oscillators are always set to the active state. The status of the main or sub oscillator varies depending on the setting of the MOSCE or SOSCE bit.

- **Low speed CR sleep mode**

When the low speed CR clock is selected as a master clock, the system changes to low speed CR sleep mode if the transition to SLEEP mode is requested. In this mode, the status of the sub oscillator varies depending on the setting of the SOSCE bit. The main oscillator, high speed CR oscillator, and PLL Multiplier Circuit are not available in this mode.

- **Sub sleep mode**

  When the sub clock is selected as a master clock, the system changes to sub sleep mode if the transition to SLEEP mode is requested. In this mode, the low speed CR oscillator is always set to the active state. The main oscillator, high speed CR oscillator, and PLL Multiplier Circuit are not available in this mode.

Overview of TIMER mode

TIMER mode is classified as one of standby modes. TIMER mode is used to stop supplying a base clock. This causes the CPU clock, AHB bus clock, and all APB bus clocks to be stopped, reducing the power consumption. In this case, all functions are stopped, excluding the oscillators, PLL, hardware watchdog timer, watch counter, RTC, clock failure detector, and Low Voltage Detection Circuit.

TIMER mode is divided into the following modes depending on a master clock at the transition to TIMER mode.

- **High speed CR timer mode**

  When the high speed CR oscillator clock is selected as a master clock, the system changes to high speed CR timer mode if the transition to TIMER mode is requested. In this mode, the status of the PLL Multiplier Circuit, main or sub oscillator varies depending on the setting of the PLLE, MOSCE or SOSCE bit. The low speed CR oscillator is always set to the active state.

- **Main timer mode**

  When the main clock is selected as a master clock, the system changes to main timer mode if the transition to TIMER mode is requested. In this mode, the status of the PLL Multiplier Circuit or sub oscillator varies depending on the setting of the PLLE or SOSCE bit. The high and low speed CR oscillators are always set to the active state.

- **PLL timer mode**

  When the main PLL clock is selected as a master clock, the system changes to PLL timer mode if the transition to TIMER mode is requested. In this mode, the high speed CR and low speed CR oscillators are always set to the active state. The status of the main or sub oscillator varies depending on the setting of the MOSCE or SOSCE bit.

- **Low speed CR timer mode**

  When the low speed CR clock is selected as a master clock, the system changes to low speed CR timer mode if the transition to TIMER mode is requested. In this mode, the status of the sub oscillator varies depending on the setting of the SOSCE bit. The main oscillator, high speed CR oscillator, and PLL Multiplier Circuit are not available in this mode.

- **Sub timer mode**

  When the sub clock is selected as a master clock, the system changes to sub timer mode if the transition to TIMER mode is requested. In this mode, the sub oscillator and low speed CR oscillator are always set to the active state. The main oscillator, high speed CR oscillator, and PLL Multiplier Circuit are not available in this mode.

Overview of RTC mode

RTC mode is classified as one of the standby modes. RTC mode stops oscillation other than that of the sub oscillator. All the functions except for watch counter, RTC, and low voltage detection circuit will be stopped.

Overview of STOP mode

STOP mode is classified as one of standby modes. STOP mode is used to stop all oscillating operations. Enabling this mode stops all functions, excluding the Low Voltage Detection Circuit.

Overview of deep standby RTC mode

Deep standby RTC mode is classified as one of the deep standby modes. Deep standby RTC mode stops oscillation other than that of the sub oscillator. All the functions except for the RTC and low voltage detection circuit will be stopped. It turns off RTC, low voltage detection circuit, CPUs other than GPIO, on-chip Flash, on-chip SRAM*, and peripheral functions inside the chip.

Overview of deep standby stop mode

Deep standby stop mode is classified as one of the deep standby modes. Deep standby stop mode stops all oscillations. All the functions except for the low voltage detection circuit will be stopped. It turns off RTC, low voltage detection circuit, CPUs other than GPIO, on-chip Flash, on-chip SRAM*, and peripheral functions inside the chip.

*: MB9AF0A1M can retain the data in on-chip SRAM.

In the setting to retain on-chip SRAM data, the power of on-chip SRAM is ON.

The overview of power supply OFF / SLEEP for each power supply domain by register control

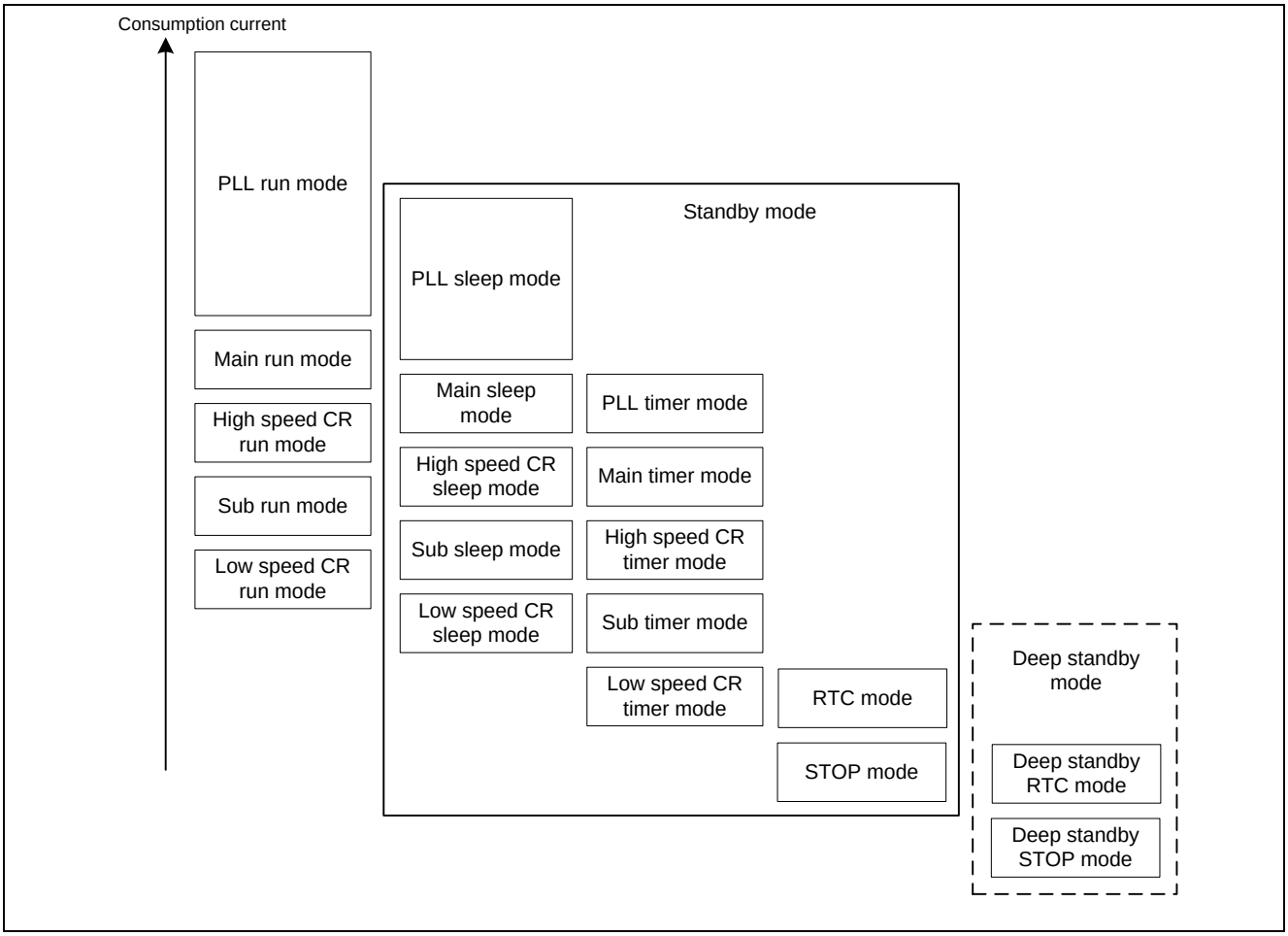
The power supply control function by register control

The target domains of power supply control are FLASH, RAM0, RAM1_0, RAM1_1, and RAC, are OFF/SLEEP and using an unnecessary power supply domain according to a use, and enable power-saving control.

Relationships between CPU operation modes and consumption current values

Figure 2.1-1 shows the relationships between CPU operation modes and consumption current values.

Figure 2.1-1 Relationships between CPU operation modes and consumption current values



Note:

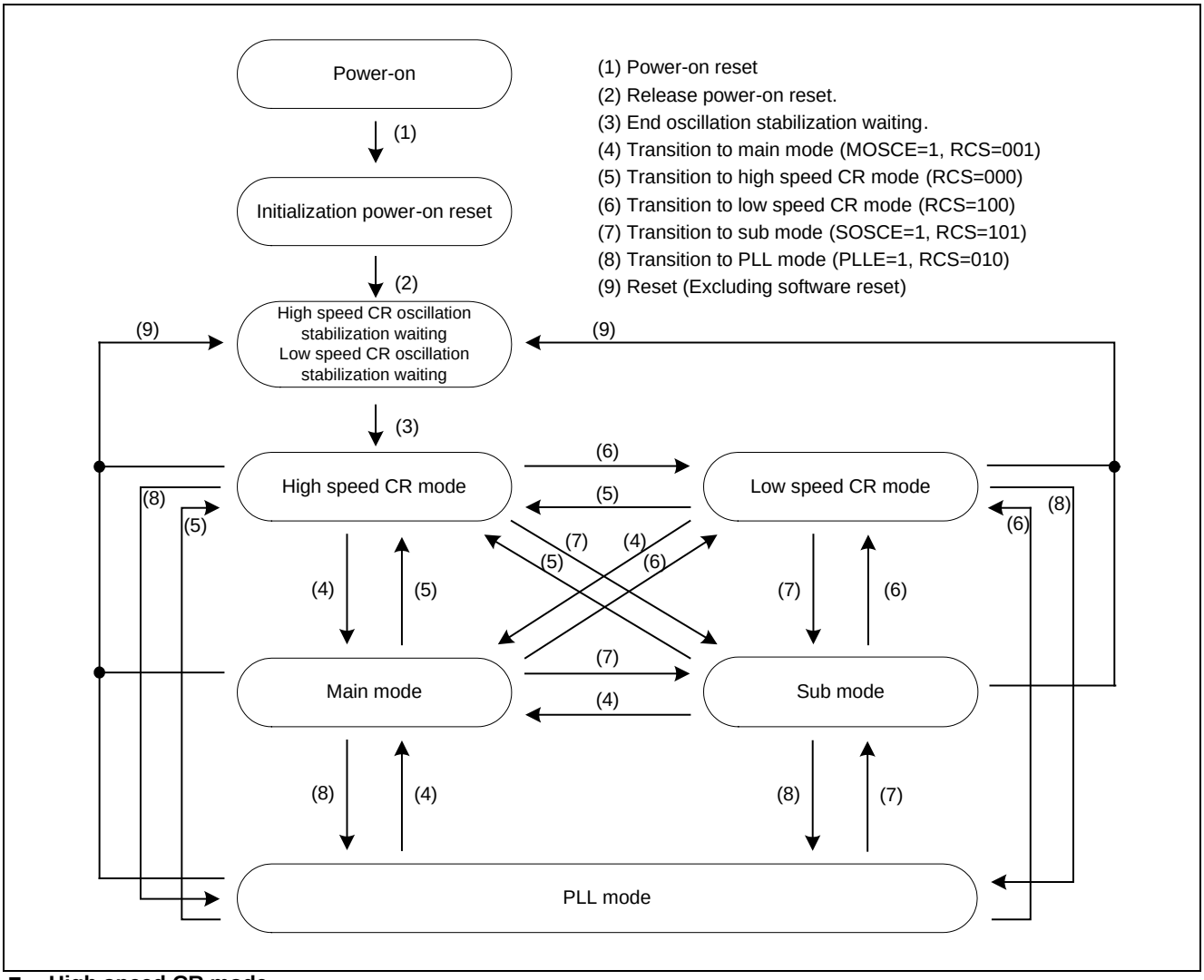
Figure 2.1-1 shows only an overview of the magnitude relationship among consumption currents of each mode. The actual consumption current values vary depending on the oscillator and PLL starting conditions in each mode or the clock configuration of the selected frequency and other elements.

2.2 Configuration of CPU Operation Modes

CPU operation mode transition diagram

Figure 2.2-1 shows the CPU operation mode transition diagram.

Figure 2.2-1 CPU operation mode transition diagram



- **High speed CR mode**

In this mode, the high speed CR oscillator clock is used as a master clock.

- **Main mode**

In this mode, the main oscillator clock is used as a master clock.

- **Low speed CR mode**

In this mode, the low speed CR oscillator clock is used as a master clock.

- **Sub mode**

In this mode, the sub oscillator clock is used as a master clock.

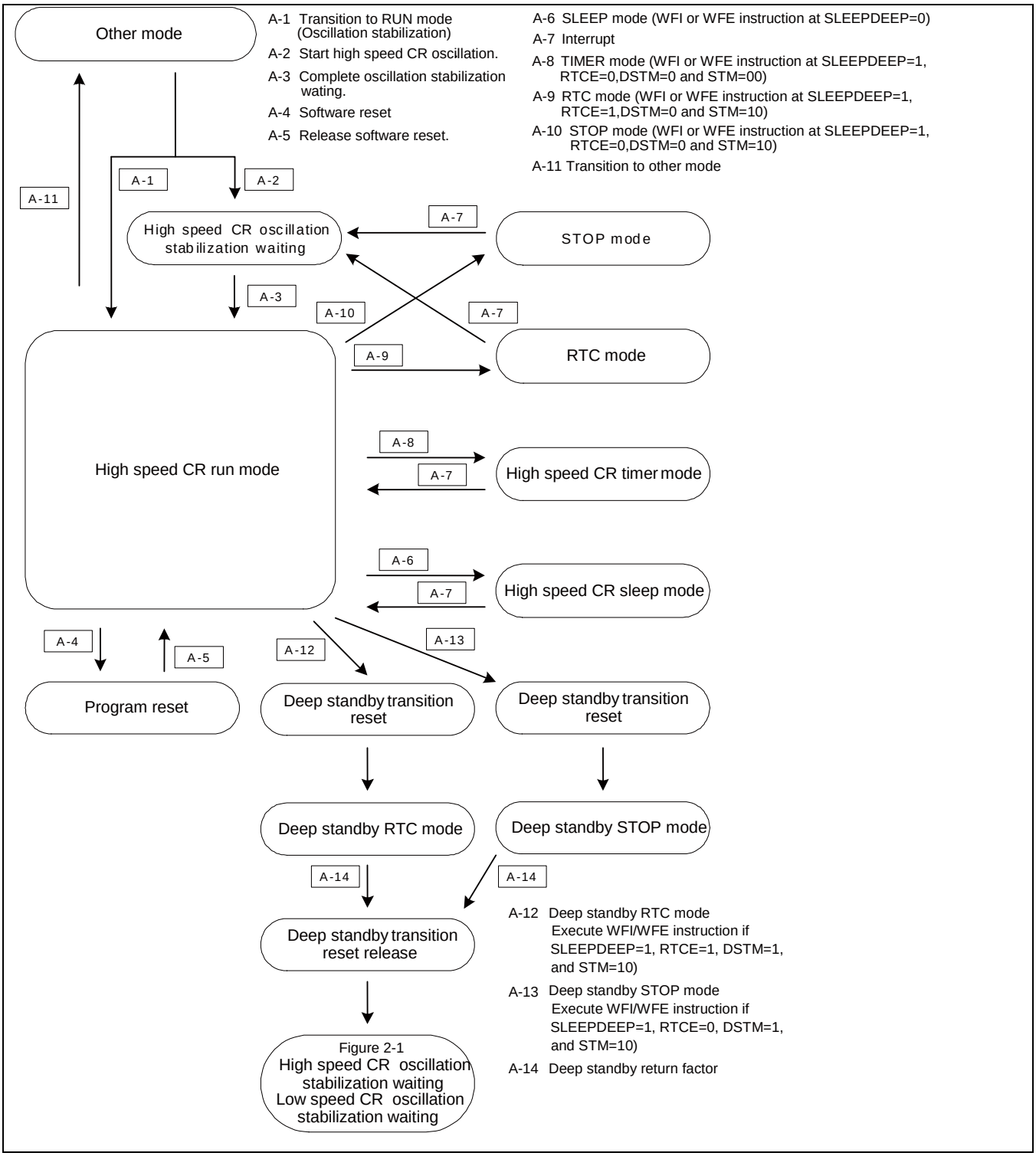
- **PLL mode**

In this mode, the PLL oscillator clock is used as a master clock.

High speed CR mode transition diagram

In high speed CR mode, the high speed CR oscillator clock is used as a master clock.

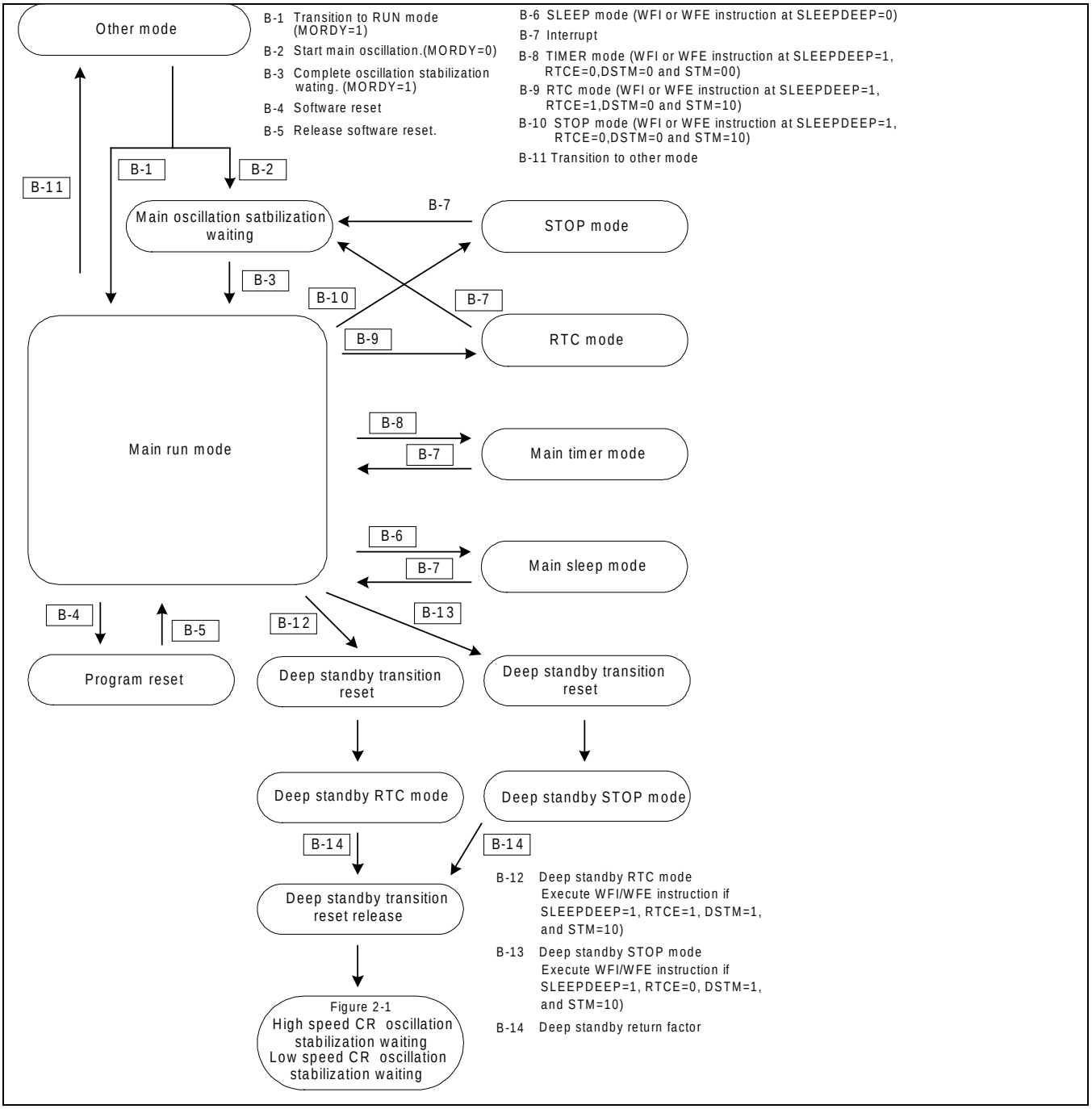
Figure 2.2-2 High speed CR mode transition diagram



Main mode transition diagram

In main mode, the main oscillator clock is used as a master clock.

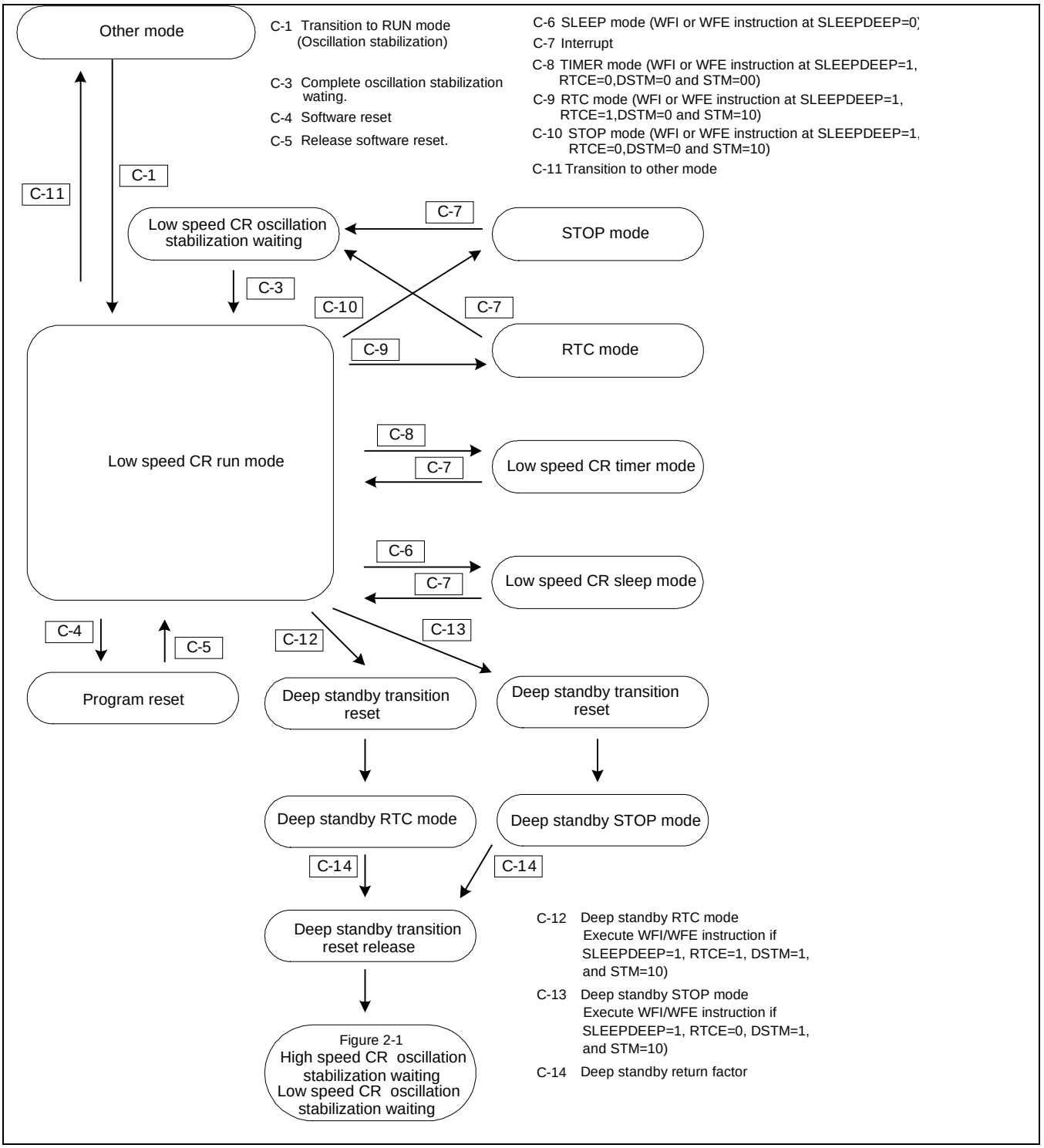
Figure 2.2-3 Main mode transition diagram



Low speed CR mode transition diagram

In low speed CR mode, the low speed CR oscillator clock is used as a master clock.

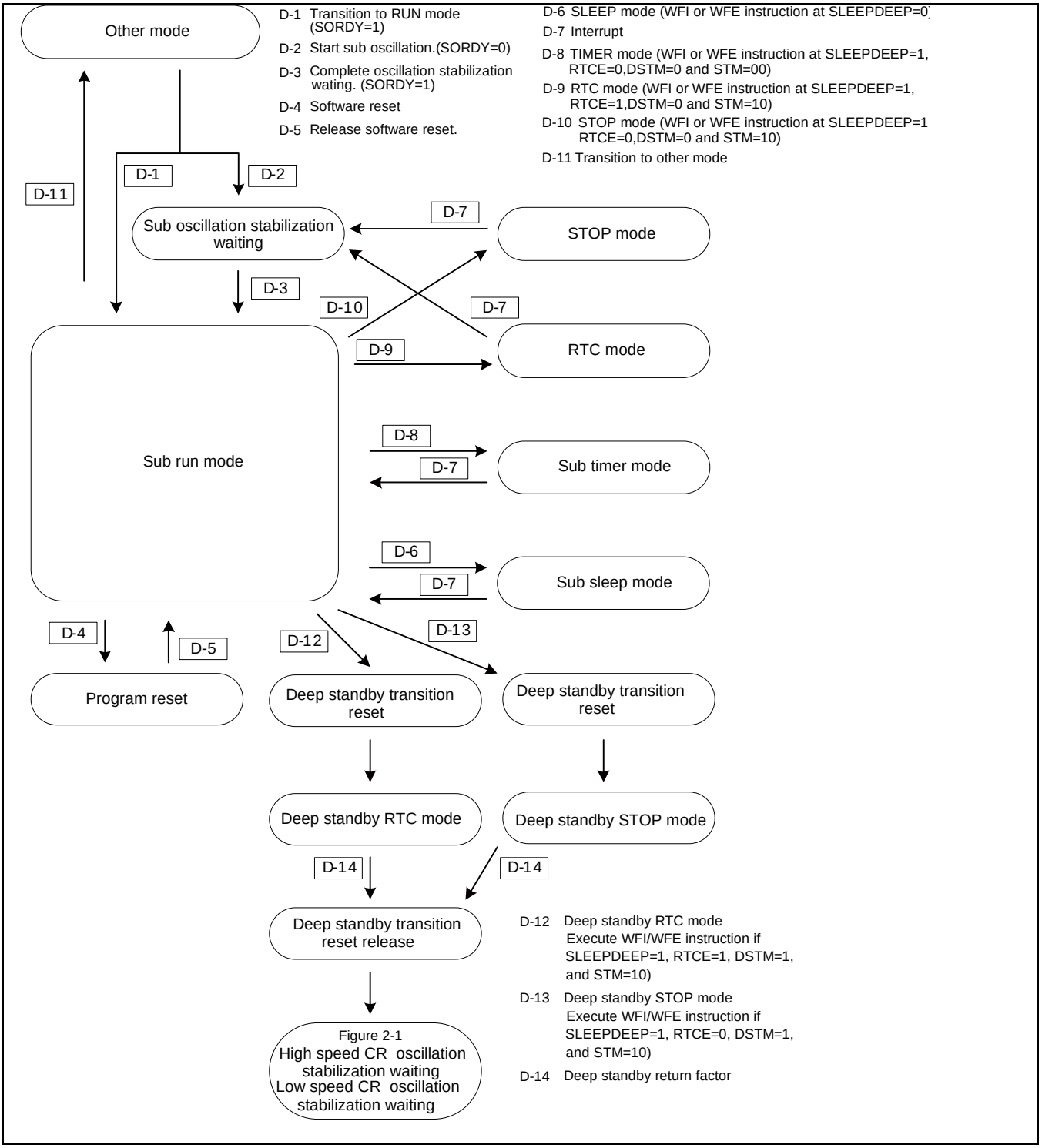
Figure 2.2-4 Low speed CR mode transition diagram



Sub mode transition diagram

In sub mode, the sub oscillator clock is used as a master clock.

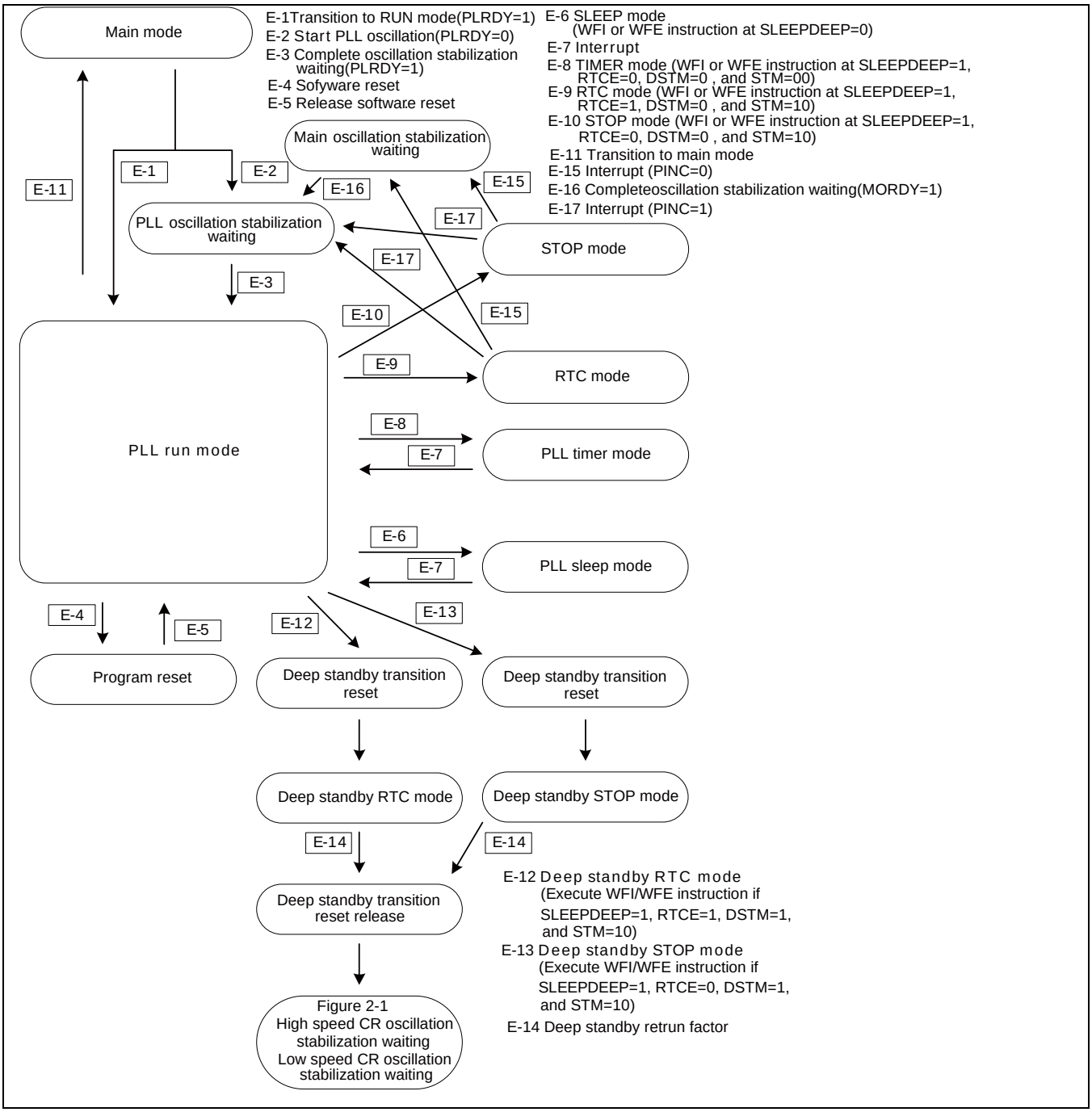
Figure 2.2-5 Sub mode transition diagram



PLL mode transition diagram

In PLL mode, the main PLL clock is used as a master clock.

Figure 2.2-6 PLL mode transition diagram



MOSCE : MOSCE bit of System Clock Mode Control Register (SCM_CTL)
SOSCE : SOSCE bit of System Clock Mode Control Register (SCM_CTL)
PLLE : PLLE bit of System Clock Mode Control Register (SCM_CTL)
RCS : RCS bit of System Clock Mode Control Register (SCM_CTL)
MORDY : MORDY bit of System Clock Mode Status Register (SCM_STR)
SORDY : SORDY bit of System Clock Mode Status Register (SCM_STR)
PLRDY : PLRDY bit of System Clock Mode Status Register (SCM_STR)
PINC : PINC bit of PLL Clock Stabilization Wait Time Setup Register (PSW_TMR)

* For the SCM_CTL, SCM_STR and PSW_TMR Registers, refer to Chapter "Clock" in "Peripheral Manual".

Note:

To return from low speed CR timer mode, sub timer mode, RTC mode, STOP mode, Deep standby RTC mode, Deep standby STOP mode, the voltage stabilization wait time (a few hundred µs) of the built-in regulator is ensured. After the wait time has lapsed, the system performs operations to return to each RUN mode.

2.3 Operations of Standby Modes

This section explains operations of standby modes.
Standby modes are classified into four types: SLEEP modes (high speed CR sleep, main sleep, PLL sleep, low speed CR sleep, and sub sleep), TIMER modes (high speed CR timer, main timer, PLL timer, low speed CR timer, and sub timer), RTC mode and STOP mode.

- **Clock operation states in standby modes**

  The table below shows the states of the oscillator clock, CPU clock, AHB bus clock, and APB bus clock in SLEEP, TIMER, RTC and STOP modes.

Table 2.3-1 Clock operation states in SLEEP modes

	SLEEP modes				
	High speed CR sleep mode	**Main sleep mode**	**PLL sleep mode**	**Low speed CR sleep mode**	**Sub sleep mode**
High speed CR clock	Operating	Operating	Operating	Stopped	Stopped
Main clock	Varies depending on the setting of the MOSCE bit.	Operating	Varies depending on the setting of the MOSCE bit.	Stopped	Stopped
Main PLL clock	Varies depending on the setting of the PLLE bit.	Varies depending on the setting of the PLLE bit.	Operating	Stopped	Stopped
Low speed CR clock	Operating	Operating	Operating	Operating	Operating
Sub clock	Varies depending on the setting of the SOSCE bit.	Varies depending on the setting of the SOSCE bit.	Varies depending on the setting of the SOSCE bit.	Varies depending on the setting of the SOSCE bit.	Operating
CPU clock	Stopped				
AHB bus clock	High speed CR clock	Main clock	PLL clock	Low speed CR clock	Sub clock
APB0 bus clock	High speed CR clock	Main clock	PLL clock	Low speed CR clock	Sub clock
APB1 bus clock	High speed CR clock	Main clock	PLL clock	Low speed CR clock	Sub clock
	* Whether or not operation is enabled is determined depending on the setting of the APBC1EN bit.				
APB2 bus clock	High speed CR clock	Main clock	PLL clock	Low speed CR clock	Sub clock
	* Whether or not operation is enabled is determined depending on the setting of the APBC2EN bit.				

Table 2.3-2 Clock operation states in TIMER modes

	TIMER modes				
	High speed CR timer mode	**Main timer mode**	**PLL timer mode**	**Low speed CR timer mode**	**Sub timer mode**
High speed CR clock	Operating	Operating	Operating	Stopped	Stopped
Main clock	Varies depending on the setting of the MOSCE bit.	Operating	Varies depending on the setting of the MOSCE bit.	Stopped	Stopped
Main PLL clock	Varies depending on the setting of the PLLE bit.	Varies depending on the setting of the PLLE bit.	Operating	Stopped	Stopped
Low speed CR clock	Operating	Operating	Operating	Operating	Operating
Sub clock	Varies depending on the setting of the SOSCE bit.	Varies depending on the setting of the SOSCE bit.	Varies depending on the setting of the SOSCE bit.	Varies depending on the setting of the SOSCE bit.	Operating
CPU clock	Stopped				
AHB bus clock	Stopped				
APB0 bus clock	Stopped				
APB1 bus clock	Stopped				
APB2 bus clock	Stopped				

Table 2.3-3 Clock operation state in RTC mode and STOP mode

	RTC mode	**STOP mode**
High speed CR clock	Stopped	Stopped
Main clock		
Main PLL clock		
Low speed CR clock		
Sub clock	Operating	
CPU clock	Stopped	
AHB bus clock		
APB0 bus clock		
APB1 bus clock		
APB2 bus clock		

MOSCE : MOSCE bit of System Clock Mode Control Register (SCM_CTL)
SOSCE : MOSCE bit of System Clock Mode Control Register (SCM_CTL)
PLLE : PLLE bit of System Clock Mode Control Register (SCM_CTL)
APBC1EN : APBC1EN bit of Peripheral Bus Clock Frequency Division Register (APBC1_PSR)
APBC2EN : APBC2EN bit of Peripheral Bus Clock Frequency Division Register (APBC2_PSR)

* : For the SCM_CTL, APBC1_PSR, and APBC2_PSR Registers, see Chapter "Clock" in "Peripheral Manual".

- **Return factors from standby modes**

Table 2.3-4 below shows the factors by which the system returns from the SLEEP, TIMER, RTC and STOP modes.

Table 2.3-4 Return factors from standby modes

	SLEEP mode	TIMER mode	RTC mode	STOP mode
Return factors by reset	INITX pin input reset Low-voltage detection reset Software watchdog reset Hardware watchdog reset Clock failure detection reset Anomalous frequency detection reset	INITX pin input reset Low-voltage detection reset Hardware watchdog reset Clock failure detection reset Anomalous frequency detection reset (Main Timer Mode, PLL Timer Mode)	INITX pin input reset Low-voltage detection reset	INITX pin input reset Low-voltage detection reset
Return factors by interrupt	Effective interrupt from each peripheral	NMI interrupt External interrupt Hardware watchdog timer interrupt Watch counter interrupt RTC interrupt Low voltage detection interrupt	NMI interrupt External interrupt Watch counter interrupt RTC interrupt Low voltage detection interrupt	NMI interrupt External interrupt Low voltage detection interrupt

2.3.1 Operations of SLEEP modes (high speed CR sleep, main sleep, PLL sleep, low speed CR sleep, and sub sleep modes)

SLEEP mode is classified as one of standby modes. Enabling SLEEP mode stops CPU clocks, reducing the power consumption.

- **Functions of SLEEP mode**
  - ☐ CPU and on-chip memory

    In SLEEP mode, the clock supplied to the CPU is stopped. AHB bus clock continues to operate. On-chip memory keeps operating and retains the data.
  - ☐ Peripherals

    The APB0 bus clock is still active in SLEEP mode. The states of the APB1 and APB2 bus clocks vary depending on the APBC1EN and APBC2EN bits settings. Peripherals are operated in the state that is set at transition.
  - ☐ Watch counter and RTC

    Watch counter and RTC remain unaffected by SLEEP mode. They continue to operate according to the setting before transiting to SLEEP mode.
  - ☐ Oscillator clocks

    Table 2.3-1 shows the status of each oscillator clock.
  - ☐ Reset and interrupt

    Reset and interrupt are available to return from SLEEP mode.
  - ☐ External bus

    The external bus is still active in SLEEP mode.
  - ☐ Status of pin

    All pin settings are held in SLEEP mode.
- **SLEEP mode setting procedure**

Execute the following steps to transit to SLEEP mode.

1. Set "0" to the SLEEPDEEP bit of the Cortex-M3 System Control Register.
2. Execute the WFI or WFE instruction.
   The system transits to the appropriate SLEEP mode according to the current clock mode indicated in the RCM bit of the System Clock Mode Control Register (SCM).

For the System Clock Mode Control Register (SCM_CTL), see Chapter "Clock" in "Peripheral Manual".

- **Return from SLEEP mode**

  The CPU returns from SLEEP mode in one of the following cases.
  - ☐ Return by reset

    If a reset (INITX pin input reset, low-voltage detection reset, software watchdog reset, hardware watchdog reset, clock supervisor reset, or anomalous frequency detection reset) occurs, the CPU changes to high speed CR run mode regardless of clock mode.
  - ☐ Return by interrupt

    If an effective interrupt is received from a peripheral in SLEEP mode, the CPU returns from SLEEP mode and changes to RUN mode to fit clock mode indicated in the RCM[2:0] bits of System Clock Mode Status Register (SCM_STR).

Table 2.3-5 Operation modes after the CPU returned from SLEEP mode by interrupt

	Status of master clock before transition to SLEEP mode				
	RCM=000 (High speed CR oscillator)	**RCM=001 (Main oscillator)**	**RCM=010 (PLL oscillator)**	**RCM=100 (Low speed CR oscillator)**	**RCM=101 (Sub oscillator)**
Operation modes after return by interrupt	High speed CR run mode	Main run mode	PLL run mode	Low speed CR run mode	Sub run mode

RCM: RCM[2:0] bits of System Clock Mode Status Register (SCM_STR)

* : For the SCM_CTL and SCM_STR Registers, refer to Chapter "Clock" in "Peripheral Manual".

☐ Waiting for oscillation stabilization at return

When the CPU returns by reset, it waits for the stabilization of high and low speed CR clock oscillations. If the CPU returns by interrupt, it does not need to wait for oscillation to stabilize.

2.3.2 Operations of TIMER modes (high speed CR timer, main timer, PLL timer, low speed CR timer, and sub timer modes)

TIMER mode is used to stop supplying a base clock. This causes the CPU clock, AHB bus clock, and all APB bus clocks to be stopped, leading to the further reduction of power consumption. In this case, all functions are stopped, excluding the oscillators, PLL, hardware watchdog timer, watch counter, RTC clock failure detector, and Low Voltage Detection Circuit.

■ **Functions of TIMER mode**

☐ CPU and on-chip memory

In TIMER mode, the CPU clock supplied to the CPU and AHB bus clock supplied to the on-chip memory and DMA controller are stopped. However, the contents of on-chip memory are retained. Also, the debug function is stopped.

☐ Peripherals

In TIMER mode, all APB clocks are stopped, and all resources, excluding the hardware watchdog timer, watch counter, RTC, clock supervisor, and Low Voltage Detection Circuit, are stopped in the last state.

☐ Watch counter and RTC

Watch counter and RTC remain unaffected by TIMER mode. They continue to operate according to the setting before transiting to TIMER mode.

☐ Oscillator clocks

Table 2.3-2 shows the status of each oscillator clock.

☐ Reset and interrupt

Reset and interrupt are available to return from TIMER mode.

☐ External bus

The external bus is stopped in TIMER mode.

☐ Status of pin

The system can control whether to retain the state just before the external pin changes to TIMER mode or change to high impedance status depending on the setting of the SPL bit in the Standby Mode Control Register (STB_CTL).

■ **TIMER mode setting procedure**

Execute the following steps to transit to TIMER mode.

1. Set "0" in RTCE bit of RTC Mode Control Register (PMD_CTL).

2. Write "0x1ACC" to the KEY bit and "0" to DSTM bit and "0b00" to the STM bit of the Standby Mode Control Register (STB_CTL). Use the SPL bit to set the status of each pin in TIMER mode.
3. Set "1" to the SLEEPDEEP bit of the Cortex-M3 System Control Register.
4. Execute the WFI or WFE instruction.
   The system transits to the appropriate TIMER mode according to the current clock mode indicated in the RCM[2:0] bits of the System Clock Mode Status Register (SCM_STR).

- **Return from TIMER mode**

The CPU returns from TIMER mode in one of the following cases.

☐ Return by reset

If a reset (INITX pin input reset, low-voltage detection reset, hardware watchdog reset, or clock supervisor reset) occurs, the CPU changes to high speed CR run mode regardless of clock mode.

Software watchdog reset not available in this mode; therefore, the CPU cannot return by those resets.

☐ Return by interrupt

If an effective NMI interrupt, external interrupt, hardware watchdog timer interrupt, USB wake up interrupt, watch counter interrupt, RTC interrupt or low voltage detection interrupt request is received in TIMER mode, the CPU returns from TIMER mode and changes to RUN mode to fit clock mode indicated in the RCM[2:0] bits of System Clock Mode Status Register (SCM_STR).

Table 2.3-6. Operation modes after the CPU returned from TIMER mode by interrupt

	Status of master clock before transition to TIMER mode				
	RCM=000 (High speed CR oscillator)	**RCM=001 (Main oscillator)**	**RCM=010 (PLL oscillator)**	**RCM=100 (Low speed CR oscillator)**	**RCM=101 (Sub oscillator)**
Operation modes after return by interrupt	High speed CR run mode	Main run mode	PLL run mode	Low speed CR run mode	Sub run mode

☐ Waiting for oscillation stabilization at return

When the CPU returns by reset, it waits for the stabilization of high and low speed CR clock oscillations. If the CPU returns by interrupt, it does not need to wait for oscillation to stabilize.

☐ Waiting for the stabilization of the built-in regulator voltage at return

To return from low speed CR timer mode or sub timer mode by reset or interrupt, the voltage stabilization wait time (a few hundred μs) of the built-in regulator is ensured automatically. After the wait time has lapsed, return operations are performed.

Notes:

- When an interrupt priority used for return is not set at a level to return the CPU, clock will be returned with the interrupt but the CPU remains stop state without returning. In order to do this, be sure to set the interrupt priority at a level which CPU is able to return.
- Before transiting to the timer mode, ensure that the causes of return from timer mode in **Table 2.3-4** are not set. If these return factors are set, clear them.
- If the transition to TIMER mode is made during debugging, as the clock to the CPU stops, a return to RUN mode cannot be performed by the ICE. Use a return by reset or interrupt.
- In case of transiting to the Low speed CR timer mode or Sub timer mode, ensure that the flash memory automatic algorithm is terminated before executing transition.

2.3.3 Operation of RTC Mode

RTC mode stops oscillation other than that of the sub oscillator. All the functions except for the watch counter, RTC, and low voltage detection circuit will be stopped.

- **Functions of RTC mode**

  ☐ CPU and on-chip memory

  In RTC mode, the CPU clock supplied to the CPU and AHB bus clock supplied to the on-chip memory and DMA controller are stopped. However, the contents of on-chip memory are retained. Also, the debug function is stopped.

  ☐ Peripheral functions

  In RTC mode, all APB clocks are stopped, and all resources, excluding the watch counter, RTC, and Low-voltage Detection Circuit, are stopped keeping the last state.

  ☐ Watch counter and RTC

  Watch counter and RTC remain unaffected by RTC mode. They continue to operate according to the setting before transiting to RTC mode.

  ☐ Oscillation clocks

  Table 3-3 (Clock operation states in RTC and STOP modes) shows the status of each oscillation clock.

  ☐ Reset and interrupt

  Reset and interrupt can be used to return from RTC mode.

  ☐ External bus

  The external bus is stopped in RTC mode.

  ☐ Status of pin

  The system can control whether to retain the status just before the external pin changes to RTC mode or changes to the high impedance status depending on the setting of the SPL bit in the Standby Mode Control Register (STB_CTL).

- **RTC mode setting procedure**

  Execute the following steps to transit to RTC mode.

  1. Set "1" in RTCE bit of RTC mode control register (PMD_CTL) while SORDY bit of System Clock Mode Status Register (SCM_STR) is "1".
  2. Write "0x1ACC" to the KEY bit, "0" to the DSTM bit, and "0b10" to the STM bit of the Standby Mode Control Register (STB_CTL). Use the SPL bit to set the status of each pin in RTC mode.
  3. Set "1" to the SLEEPDEEP bit of the Cortex-M3 System Control Register.
  4. Execute the WFI or WFE instruction.

- **Return from RTC mode**

  The CPU returns from RTC mode in any one of the following cases.

  ☐ Return by reset

  If a reset (INITX pin input reset, low-voltage detection reset) occurs, the CPU changes to high-speed CR run mode regardless of clock mode.
  Software watchdog reset, hardware watchdog reset, clock supervisor reset, and anomalous frequency detection reset do not operate; therefore, the CPU cannot return by those resets.

  ☐ Return by interrupt

  If an effective NMI interrupt, external interrupt, USB wake up interrupt, watch counter interrupt, RTC interrupt, or low voltage detection interrupt request is received in RTC mode, the CPU returns from RTC mode and transits to RUN mode to fit clock mode indicated in the RCM[2:0] bits of System Clock Mode Status Register (SCM_STR).

Table 2.3-7 Operation modes after the CPU has returned from RTC mode by interrupt.

	Status of master clock before transition to RTC mode				
	RCM = 000 (High speed CR oscillator)	**RCM = 001 (Main oscillator)**	**RCM = 010 (PLL oscillator)**	**RCM = 100 (Low speed CR oscillator)**	**RCM = 101 (Sub oscillator)**
Operation modes after return by interrupt	High speed CR run mode	Main run mode	PLL run mode	Low speed CR run mode	Sub run mode

☐ Waiting for oscillation stabilization at return

When the CPU returns by reset, it waits for the stabilization of high and low speed CR clock oscillations. If the CPU returns by interrupt, the oscillation stabilization wait changes by the master clock before transition to the RTC mode as shown in Table 2.3-8.

Table 2.3-8 Oscillation stabilization wait when returning by interrupt from RTC mode

		Status of master clock before transition to RTC mode				
		RCM = 000 (High speed CR oscillator)	**RCM = 001 (Main oscillator)**	**RCM = 010 (PLL oscillator)**	**RCM = 100 (Low speed CR oscillator)**	**RCM = 101 (Sub oscillator)**
Oscillation stabilization wait after returning by interrupt	High speed CR clock	ON	ON	ON	OFF	OFF
	Main clock	MOSCE="0": OFF MOSCE="1": ON	ON	PINC="0": ON PINC="1": OFF	OFF	OFF
	Main PLL clock	OFF	PLLE="0": OFF PLLE="1": ON	ON	OFF	OFF
	Low speed CR clock	ON	ON	ON	ON	ON
	Sub clock	OFF	OFF	OFF	OFF	OFF

☐ Waiting for the stabilization of the built-in regulator voltage at return

To return from RTC mode, the voltage stabilization wait time (a few hundred μs) of the built-in regulator is ensured automatically. After the wait time has lapsed, return operations are performed.

Notes:

- When an interrupt priority used for return is not set at a level to return the CPU, the clock will be returned by the interrupt but the CPU remains in stop state without returning. In order to do this, be sure to set the interrupt priority at a level which the CPU is able to return.
- Before transiting to the RTC mode, ensure that the causes of return from timer mode in Table 2.3-4 are not set. If these return factors are set, clear them.
- If the transition to RTC mode is made during debugging, as the clock to the CPU stops, a return to RUN mode cannot be performed by the ICE. Use a return by reset or interrupt.
- In case of transiting to the RTC mode, ensure that the flash memory automatic algorithm is terminated before executing the transition.

2.3.4 Operations of STOP mode

STOP mode is used to stop all oscillating operations. Enabling this mode stops all functions, excluding the Low Voltage Detection Circuit.

- **Functions of STOP mode**

  ☐ CPU and on-chip memory

  In STOP mode, the CPU clock supplied to the CPU and AHB bus clock supplied to the on-chip memory and DMA controller are stopped. However, the contents of on-chip memory are retained. The debug function is stopped.

  ☐ Peripheral functions

  All APB bus clocks are stopped, and all resources, excluding the Low Voltage Detection Circuit, are stopped in the last state.

  ☐ Oscillator clocks

  All oscillator clocks are stopped.

  ☐ Reset and interrupt

  Reset and interrupt are available to return from STOP mode.

  ☐ External bus

  The external bus is stopped in STOP mode.

  ☐ Status of pin

  The system can control whether to retain the state just before the external pin changes to STOP mode or change to high impedance status depending on the setting of the SPL bit in the Standby Mode Control Register (STB_CTL).

- **STOP mode setting procedure**

  Execute the following steps to transit to STOP mode.

  1. Set "0" in RTCE bit of RTC Mode Control Register (PMD_CTL).
  2. Write "0x1ACC" to the KEY bit and "0" to DSTM bit and "0b00" to the STM bit of the Standby Mode Control Register (STB_CTL). Use the SPL bit to set the status of each pin in STOP mode.
  3. Set "1" to the SLEEPDEEP bit of the Cortex-M3 System Control Register.
  4. Execute the WFI or WFE instruction.

- **Return from STOP mode**

  The CPU returns from STOP mode in one of the following cases.

  ☐ Return by reset

  If a reset (INITX pin input reset or low-voltage detection reset) occurs, the CPU changes to the high speed CR run mode regardless of clock mode.

  Software watchdog reset, hardware watch dog reset, clock supervisor reset, and anomalous frequency detection reset are not available in this mode; therefore, the CPU cannot return by those resets.

  ☐ Return by interrupt

  If an effective NMI interrupt, external interrupt, USB wake up interrupt, or low voltage detection interrupt request is received in STOP mode, the CPU returns from STOP mode and changes to RUN mode to fit clock mode indicated in the RCM[2:0] bits of System Clock Mode Status Register (SCM_CTL).

Table 2.3-9 Operation modes after the CPU returned from the STOP mode by interrupt

	Status of master clock before changing to STOP mode				
	RCM=000 (High speed CR oscillator)	**RCM=001 (Main oscillator)**	**RCM=010 (PLL oscillator)**	**RCM=100 (Low speed CR oscillator)**	**RCM=101 (Sub oscillator)**
Operation modes after return by interrupt	High speed CR run mode	Main run mode	PLL run mode	Low speed CR run mode	Sub run mode

☐ Waiting for oscillation stabilization at return

When the CPU returns by reset, it waits for the stabilization of high and low speed CR clock oscillations. If the CPU returns by interrupt, the oscillation stabilization wait state varies depending on the master clock that is output before the CPU changes to STOP mode as shown in Table 2.3-10.

Table 2.3-10 Waiting for oscillation to stabilize at return from STOP mode by interrupt

		Status of master clock before changing to STOP mode				
		RCM=000 (High speed CR oscillator)	**RCM=001 (Main oscillator)**	**RCM=010 (PLL oscillator)**	**RCM=100 (Low speed CR oscillator)**	**RCM=101 (Sub oscillator)**
Oscillation stabilization waiting after return by interrupt	High speed CR clock	ON	ON	ON	OFF	OFF
	Main clock	MOSCE="0": OFF MOSCE="1": ON	ON	PINC="0": ON PINC="1": OFF	OFF	OFF
	Main PLL clock	OFF	PLLE="0": OFF PLLE="1": ON	ON	OFF	OFF
	Low speed CR clock	ON	ON	ON	ON	ON
	Sub clock	SOSCE="0": OFF SOSCE="1": ON	SOSCE="0": OFF SOSCE="1": ON	SOSCE="0": OFF SOSCE="1": ON	SOSCE="0": OFF SOSCE="1": ON	ON

☐ Waiting for the stabilization of the built-in regulator voltage at return

When the CPU returns from STOP mode, the voltage stabilization wait time (a few hundred μs) of the built-in regulator is ensured automatically. After the wait time has lapsed, return operations are performed.

Notes:

- When an interrupt priority used for return is not set at a level to return the CPU, clock will be returned with the interrupt but the CPU remains stop state without returning. In order to do this, be sure to set the interrupt priority at a level which CPU is able to return.
- Before transiting to the STOP mode, ensure that the causes of return from timer mode in Table 2.3-4 are not set. If these return factors are set, clear them.
- If the transition to STOP mode is made during debugging, as the clock to the CPU stops, a return to RUN mode cannot be performed by the ICE. Use a return by reset or interrupt.
- In case of transiting to the STOP mode, ensure that the flash memory automatic algorithm is terminated before executing transition.

2.4 Standby Mode Setting Procedure Examples

This section provides standby mode setting procedure examples.
Figure 2.4-1 Main timer mode setting procedure example

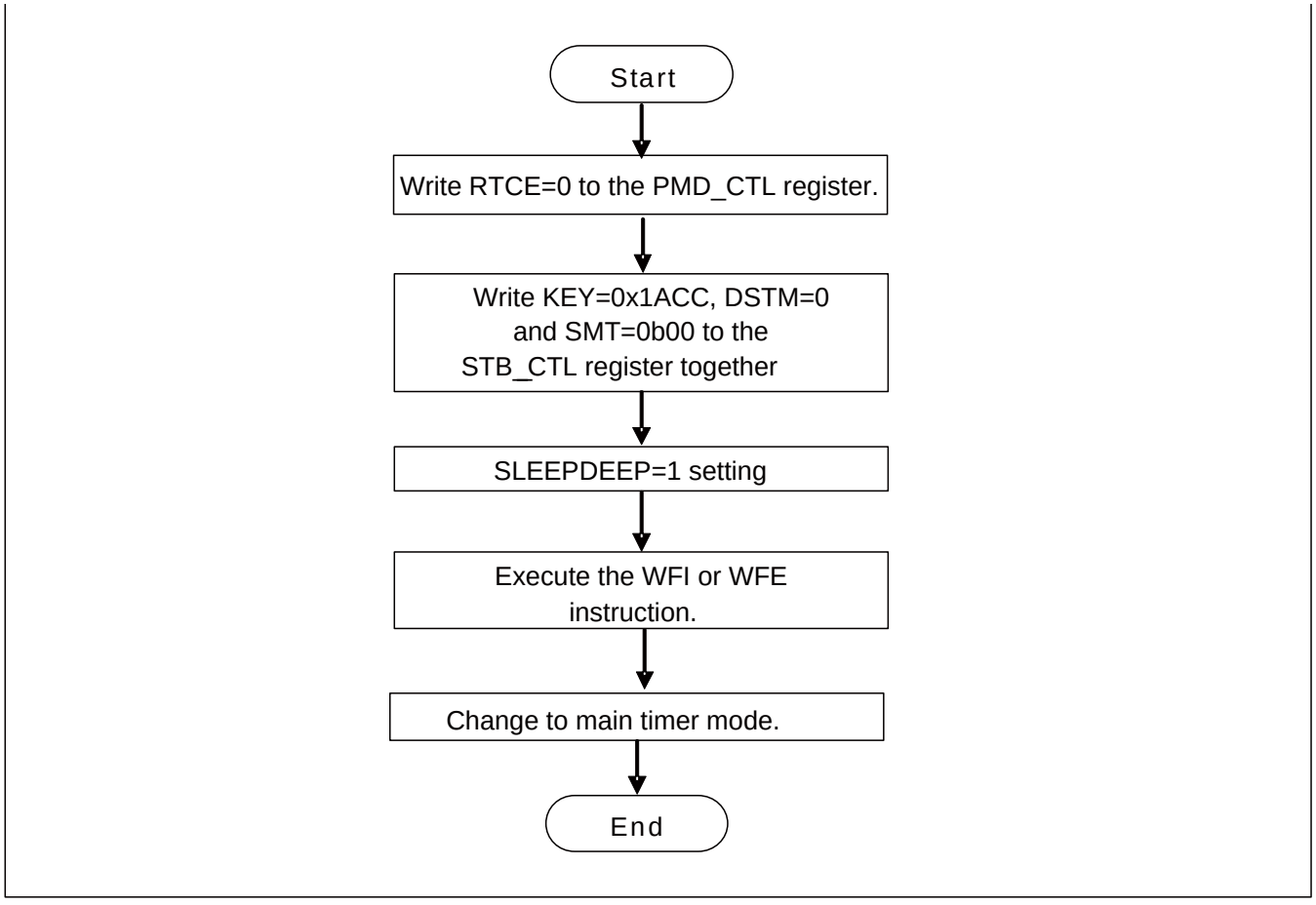
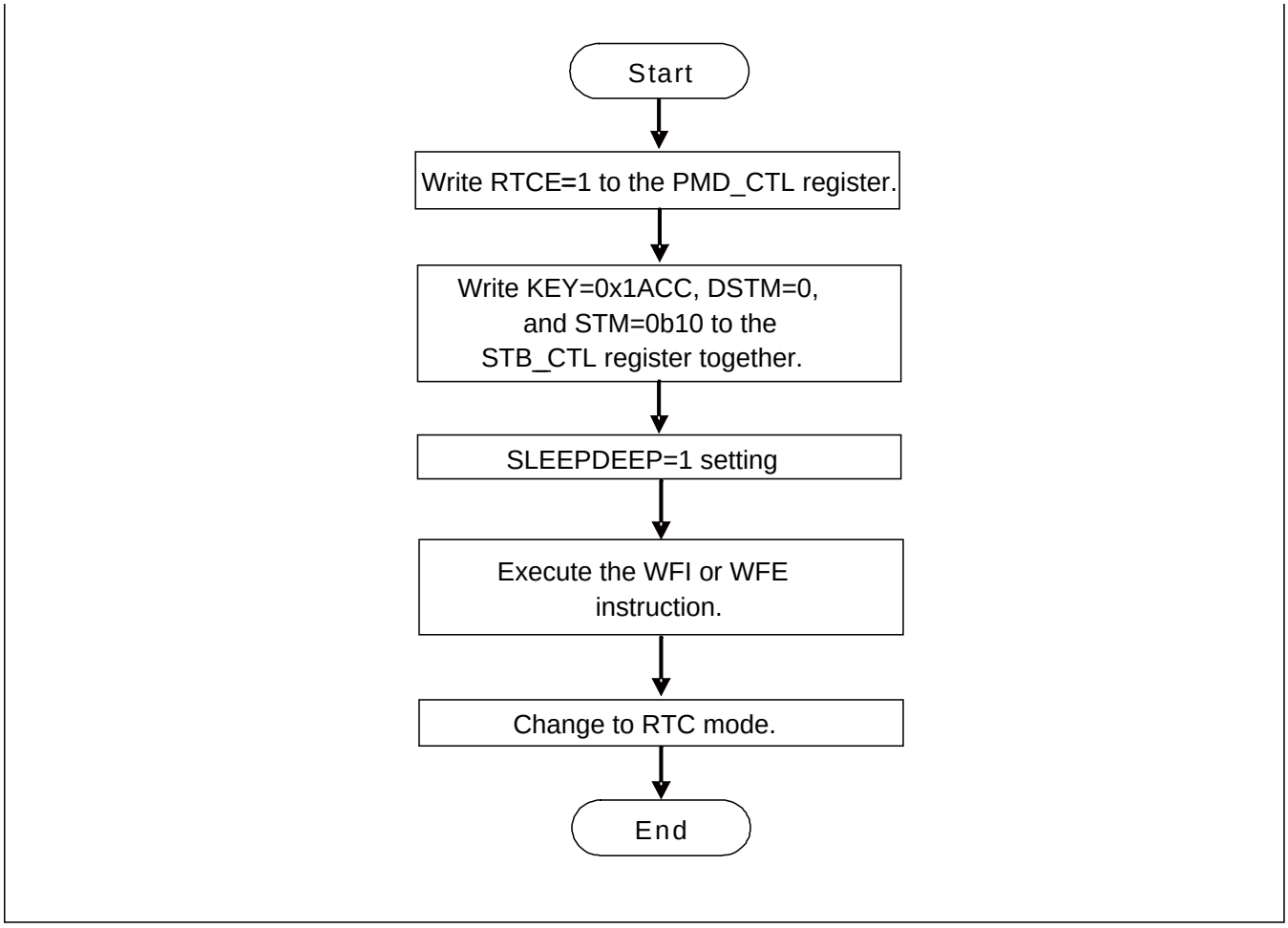


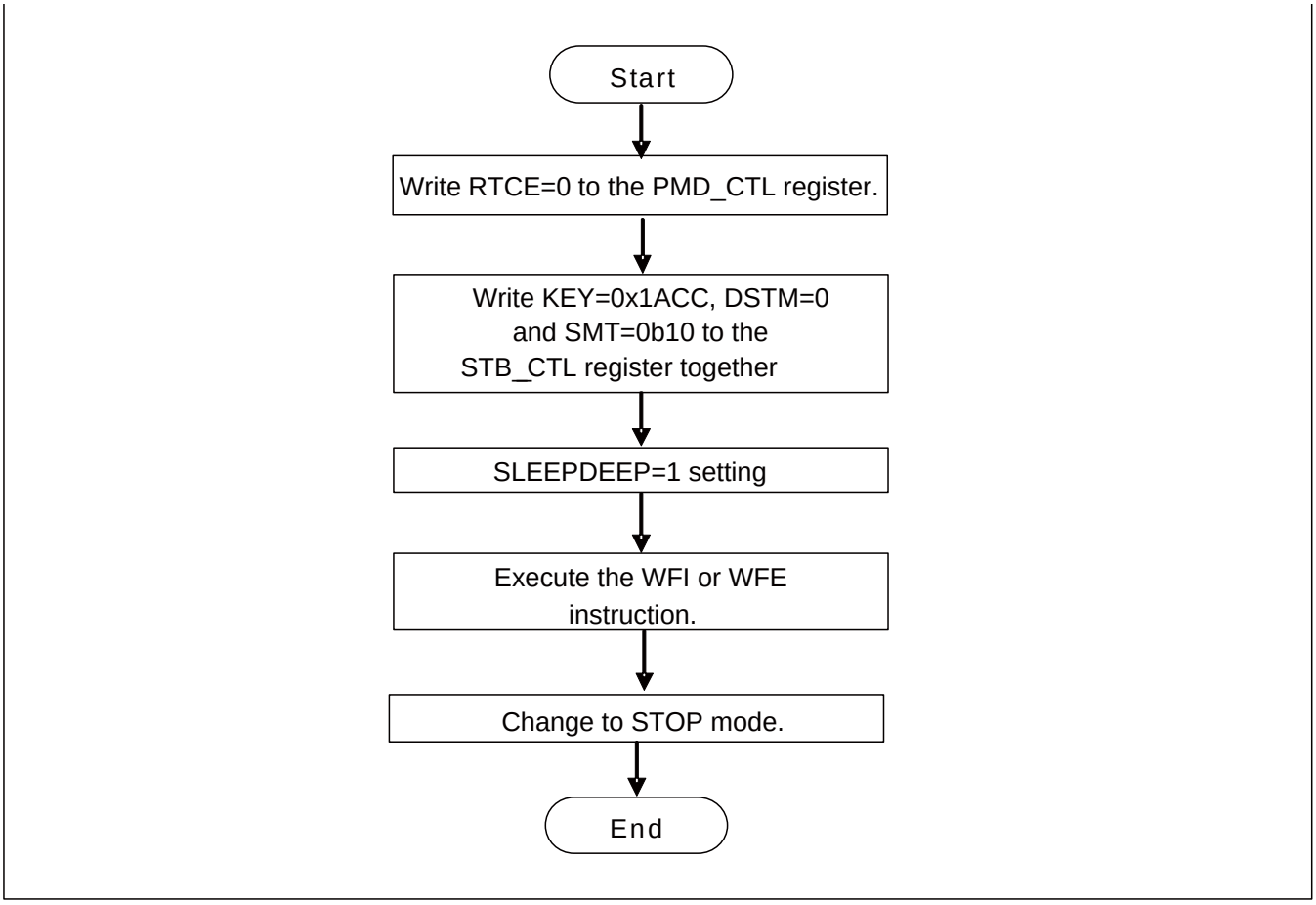
Figure 2.4-2 RTC mode setting procedure example (Main clock is selected as a master clock)



Notes

- In case of transiting to the RTC mode, ensure that the flash memory automatic algorithm is terminated before executing the transition.
- Writing "1" to RTCE bit of the RTC Mode Control Register (PMD_CTL) is valid only when the SORDY bit of the System Clock Mode Status Register (SCM_STR) is "1".

Figure 2.4-3 STOP mode setting procedure example (Main clock is selected as a master clock)



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Note

- In case of transiting to the STOP mode, ensure that the flash memory automatic algorithm is terminated before executing the transition.

2.5 Description of Deep Standby Mode Operation

This section describes the operation of deep standby mode.
Deep standby mode includes deep standby RTC mode and deep standby STOP mode.

- **Clock operation status in deep standby mode**

  The following shows the status of the oscillation clock, CPU clock, AHB bus clock, and APB bus clock while in deep standby RTC mode and deep standby STOP mode.

Table 2.5-1 Clock operation state in deep standby mode

	Deep standby RTC mode	Deep standby STOP mode
High speed CR clock	Stopped	Stopped
Main clock		
Main PLL clock		
Low speed CR clock		
Sub clock	Operating	

	Deep standby RTC mode	Deep standby STOP mode
CPU clock	Stopped	
AHB bus clock		
APB0 bus clock		
APB1 bus clock		
APB2 bus clock		

- **Return factors from deep standby mode**

  The following shows the return factors from deep standby RTC mode and deep standby STOP mode.

Table 2.5-2 Return factors from deep standby mode

	Deep standby RTC mode	Deep standby STOP mode
Deep standby return factor	INITX pin input reset Low-voltage detection reset	INITX pin input reset Low-voltage detection reset
	Low-voltage detection interrupt RTC interrupt	Low-voltage detection interrupt
	WKUP pin input	WKUP pin input

Note:

Although each interrupt cause is retained after returning from deep standby mode, interrupt processing will not be executed since NVIC is initialized by deep standby transition reset.

- **Internal power supply status and reset status in deep standby mode**

  The following shows the power supply status of each function in deep standby mode and initialization status in deep standby transition reset.

Table 2.5-3 Internal power supply status and initialization status in deep standby mode

	Power supply status	Reset status
CPU	Off	Initialize
On-chip Flash	Off	*1
On-chip SRAM	Off	*2
RTC	On	Do not initialize
Low-voltage detection circuit	On	Do not initialize
GPIO	On	Partly initialize *3
Deep standby control block	On	Do not initialize
Peripheral functions other than the above	Off	Initialize

*1: The contents of on-chip Flash are retained.

*2: The contents of on-chip SRAM are not retained.

*3: PFRx registers excluding bit4:0 of PFR0 are initialized and others are not initialized.

2.5.1 Operation of Deep Standby RTC Mode

Deep standby RTC mode stops oscillation other than that of the sub oscillator. All the functions except for RTC, and low voltage detection circuit will be stopped. It turns off RTC, low voltage detection circuit, CPUs other than GPIO, on-chip Flash, on-chip SRAM*, and peripheral functions inside the chip.

- **Functions of deep standby RTC mode**

  ☐ CPU and on-chip memory

  In deep standby RTC mode, the CPU clock supplied to CPU and AHB bus clock supplied to on-chip memory and DMA controller are stopped. It turns off the CPU, on-chip Flash, and on-chip SRAM*. The contents of the CPU register and on-chip SRAM are not retained*. The contents of on-chip flash memory are retained. Also, the debug function is stopped and turned off.

  *: In the setting to retain on-chip SRAM data, the power of on-chip SRAM is ON.

  ☐ Peripheral functions

  All APB bus clocks are stopped, and all resources, excluding RTC, Low-voltage Detection Circuit, and GPIO are turned off.

  ☐ RTC

  RTC remains unaffected by deep standby RTC mode. It continues to operate according to the setting before transiting to deep standby RTC mode.

  ☐ Oscillation clock

  The status of each oscillation clock is shown in Table 5-1.

  ☐ Reset, interrupt, and WKUP pin input

  Reset, interrupt, and WKUP pin input can be used for returning from deep standby RTC mode.

  ☐ Status of pin

  The system can control whether the external pin switches to GPIO in deep standby RTC mode or to high impedance status by the SPL bit in the Standby Mode Control Register (STB_CTL).

- **Setting procedure of deep standby RTC mode**

  Execute the following steps to transit to deep standby RTC mode.

  1. Set "1" in RTCE bit of the RTC Mode Control Register (PMD_CTL) while the SORDY bit of the System Clock Mode Status Register (SCM_STR) is "1".
  2. Write "0x1ACC" to the KEY bit, "1" to the DSTM bit, and "0b10" to the STM bit of the Standby Mode Control Register (STB_CTL). Use the SPL bit to set the status of each pin in deep standby RTC mode.
  3. Set "1" to the SLEEPDEEP bit of the Cortex-M3 System Control Register.
  4. Execute the WFI or WFE instruction.

- **Return from deep standby RTC mode**

  CPU returns from deep standby RTC mode in any one of the following cases.

  ☐ Return by reset, interrupt, and WKUP pin input

  If a reset (INITX pin input reset and low-voltage detection reset) occurs or if effective RTC interrupt, low-voltage detection interrupt, and WKUP pin input request are received while in deep standby RTC mode, the CPU returns from deep standby RTC mode and changes to high speed CR run mode regardless of clock mode.

  Software watchdog reset, hardware watchdog reset, clock supervisor reset, and anomalous frequency detection reset do not operate; therefore, the CPU cannot return by those resets.

  ☐ Waiting for oscillation stabilization at return

  The oscillation stabilization wait for the high speed CR clock and low speed CR clock is executed regardless of return factor.

  ☐ Waiting for the stabilization of the built-in regulator voltage at return

To return from deep standby RTC mode, the voltage stabilization wait time (a few hundred ☐ Waiting for the stabilization of the built-in regulator voltage at return ensured automatically. After the wait time has lapsed, return operations are performed.

Notes:

- Before transiting to the deep standby RTC mode, ensure that RTC interrupt, the low-voltage detection interrupt cause, and the WKUP pin input return factor are not set. If these interrupt causes are set, clear them.
- If the transition to deep standby RTC mode is made during debugging, a return to RUN mode cannot be performed by the ICE as the debug function is turned off. Use a return by reset, interrupt, or WKUP pin input.
- In the case of transiting to the deep standby RTC mode, ensure that the flash memory automatic algorithm is terminated before executing the transition.

2.5.2 Operation of Deep Standby Stop Mode

Deep standby stop mode stops all oscillations. All the functions except for the low voltage detection circuit will be stopped. It turns off RTC, the low-voltage detection circuit, CPUs other than GPIO, on-chip Flash, on-chip SRAM*, and peripheral functions inside the chip.

- **Functions of deep standby STOP mode**

  ☐ CPU and on-chip memory

  In deep standby RTC mode, the CPU clock supplied to CPU and AHB bus clock supplied to on-chip memory and DMA controller are stopped. It turns off the CPU and on-chip Flash, on-chip SRAM*. The contents of the CPU register and on-chip SRAM are not retained*. The contents of on-chip flash memory are retained. Also, the debug function is stopped and turned off.

  *: In the setting to retain on-chip SRAM data, the power of on-chip SRAM is ON.

  ☐ Peripherals

  All APB bus clocks are stopped, and all resources, excluding RTC, Low-voltage Detection Circuit, and GPIO are turned off.

  ☐ Oscillation clock

All oscillations are stopped.

☐ Reset and WKUP pin input

Reset and WKUP pin input can be used for returning from deep standby STOP mode.

☐ Status of pin

The system can control whether the external pin switches to GPIO in deep standby STOP mode or to high impedance status by the SPL bit in the Standby Mode Control Register (STB_CTL).

- **Setting procedure of deep standby STOP mode**

Execute the following steps to transit to deep standby STOP mode.

1. Set "0" in RTCE bit of the RTC Mode Control Register (PMD_CTL).
2. Write "0x1ACC" to the KEY bit, "1" to the DSTM bit, and "0b10" to the STM bit of the Standby Mode Control Register (STB_CTL). Use the SPL bit to set the status of each pin in deep standby STOP mode.
3. Set "1" to the SLEEPDEEP bit of the Cortex-M3 System Control Register.
4. Execute the WFI or WFE instruction.

- **Return from deep standby STOP mode**

CPU returns from deep standby STOP mode in any one of the following cases.

☐ Return by reset, interrupt, and WKUP pin input

If a reset (INITX pin input reset and low-voltage detection reset) occurs, or if effective low-voltage detection interrupt, or WKUP pin input request is received while in deep standby STOP mode, the CPU returns from deep standby STOP mode and changes to high speed CR run mode regardless of clock mode.

Software watchdog reset, hardware watchdog reset, clock supervisor reset, and anomalous frequency detection reset do not operate; therefore, the CPU cannot return by those resets.

☐ Waiting for oscillation stabilization at return

The oscillation stabilization wait for the high speed CR clock and low speed CR clock is executed regardless of return factor.

☐ Waiting for the stabilization of the built-in regulator voltage at return

To return from deep standby STOP mode, the voltage stabilization wait time (a few hundred μs) of the built-in regulator is ensured automatically. After the wait time has lapsed, return operations are performed.

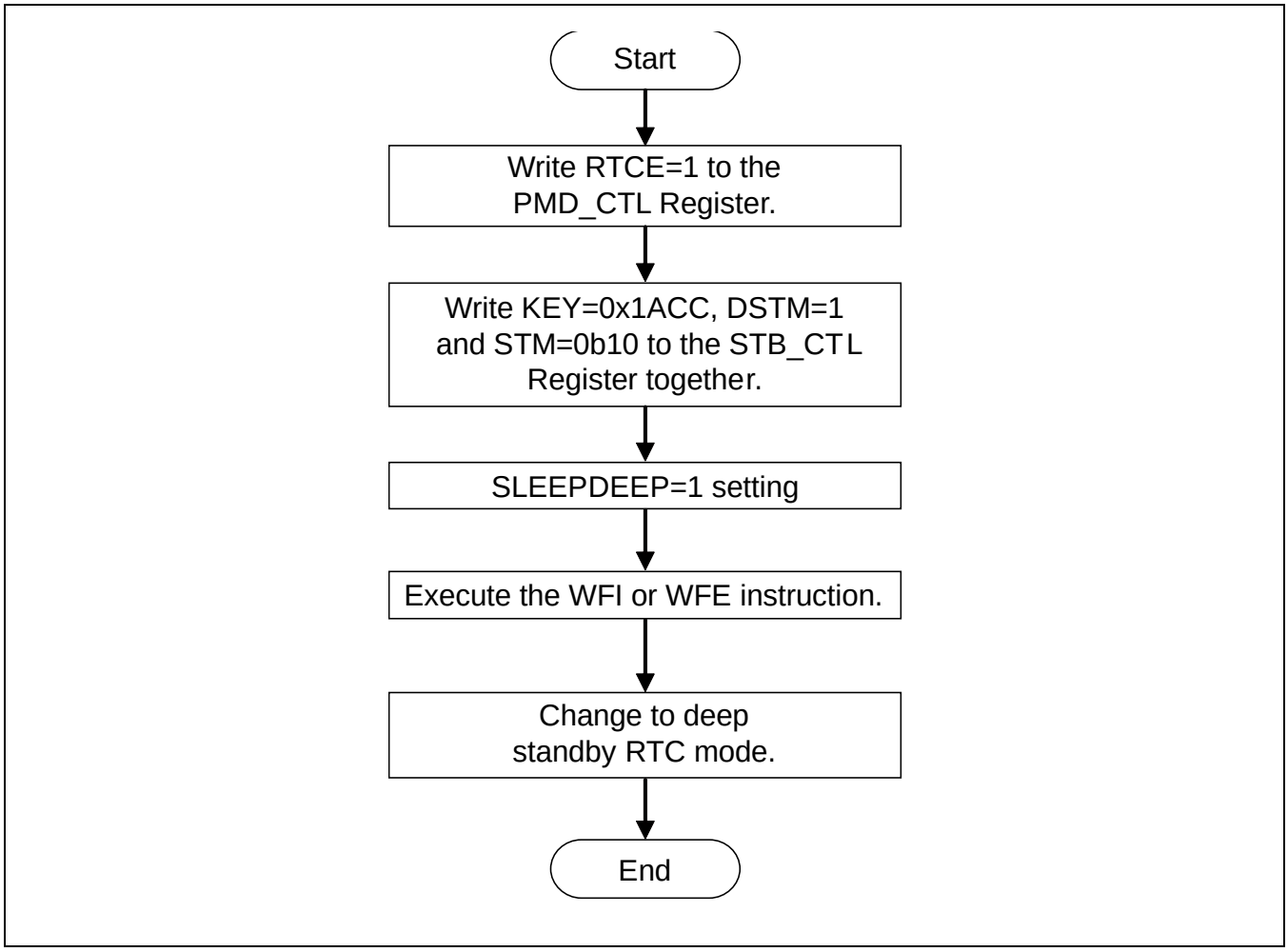
Notes:

- Before transiting to the deep standby STOP mode, ensure that the low-voltage detection interrupt cause, and the WKUP pin input return factor are not set. If these interrupt causes are set, clear them.
- If the transition to deep standby stop mode is made during debugging, a return to RUN mode cannot be performed by the ICE as the debug function turns off. Use a return by reset, interrupt, or WKUP pin input.
- In the case of transiting to the deep standby STOP mode, ensure that the flash memory automatic algorithm is terminated before executing the transition.

2.6 Deep Standby Mode Setting Procedure Examples

This section explains the deep standby mode setting procedure examples.

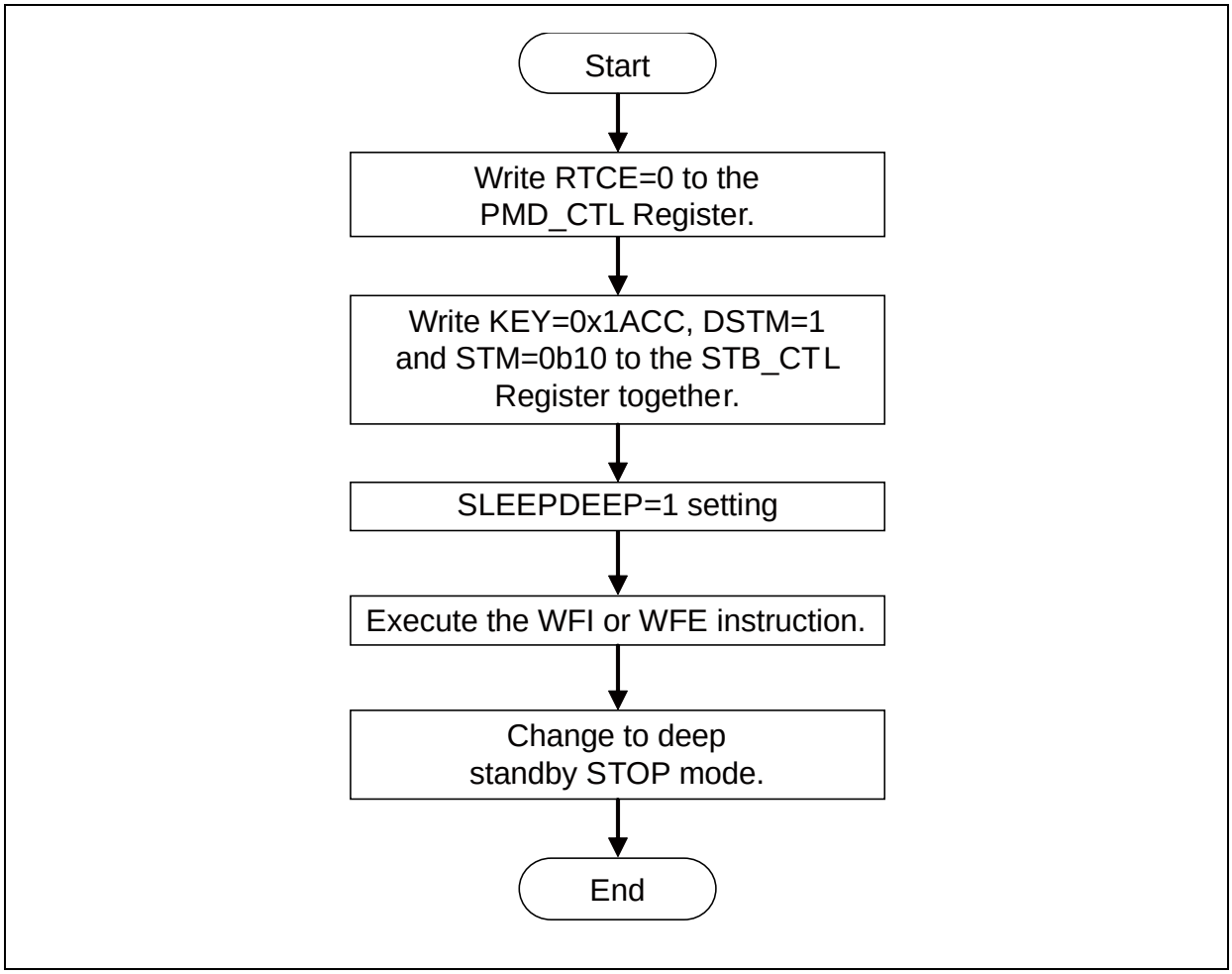
Figure 2.6-1 Setting procedure example for deep standby RTC mode



Notes:

- In case of transiting to the deep standby RTC mode, ensure that the flash memory automatic algorithm is terminated before executing the transition.
- Writing "1" to RTCE bit of the RTC Mode Control Register (PMD_CTL) is valid only when the SORDY bit of the System Clock Mode Status Register (SCM_STR) is "1".

Figure 2.6-2 Setting procedure example for deep standby STOP mode



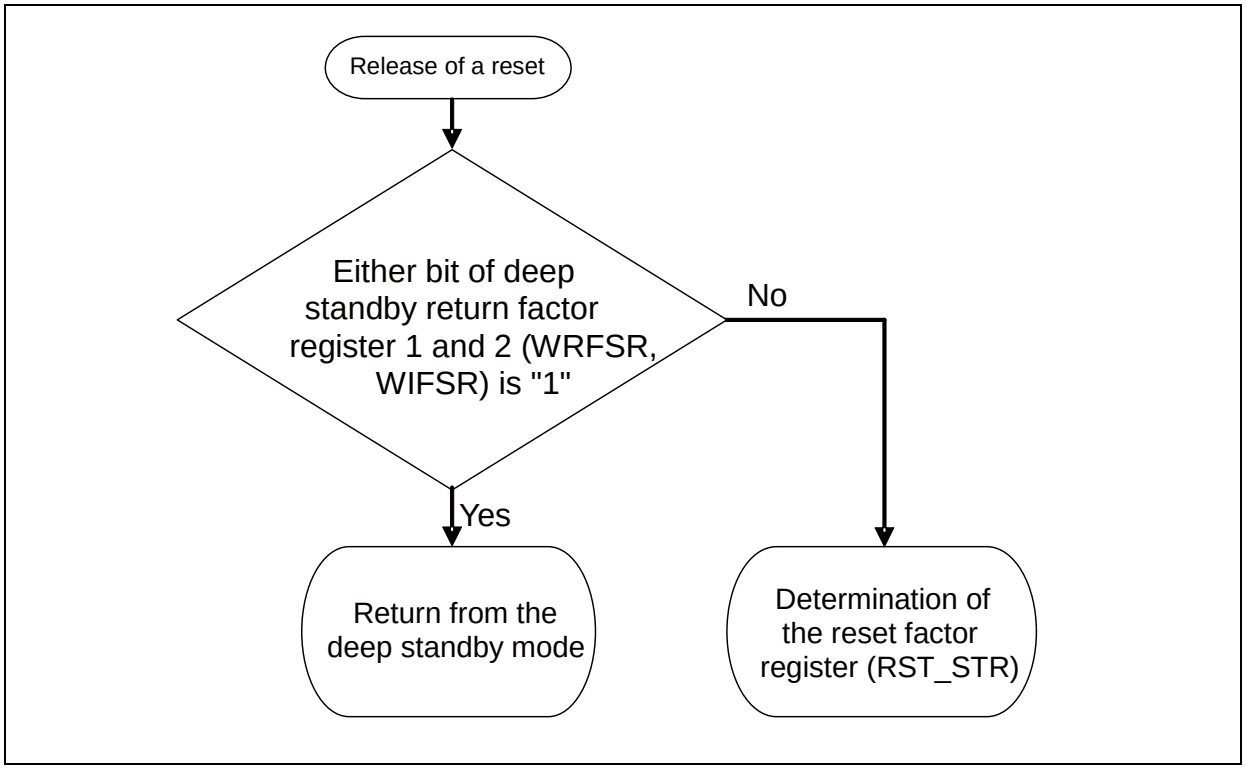
Note:

In case of transiting to the deep standby STOP mode, ensure that the flash memory automatic algorithm is terminated before executing the transition.

2.7 Deep Standby Return Factor Determination Procedure

This section shows a procedure example to determine a return from deep standby mode.

Figure 2.7-1 Procedure example for deep standby return factor determination



Note:

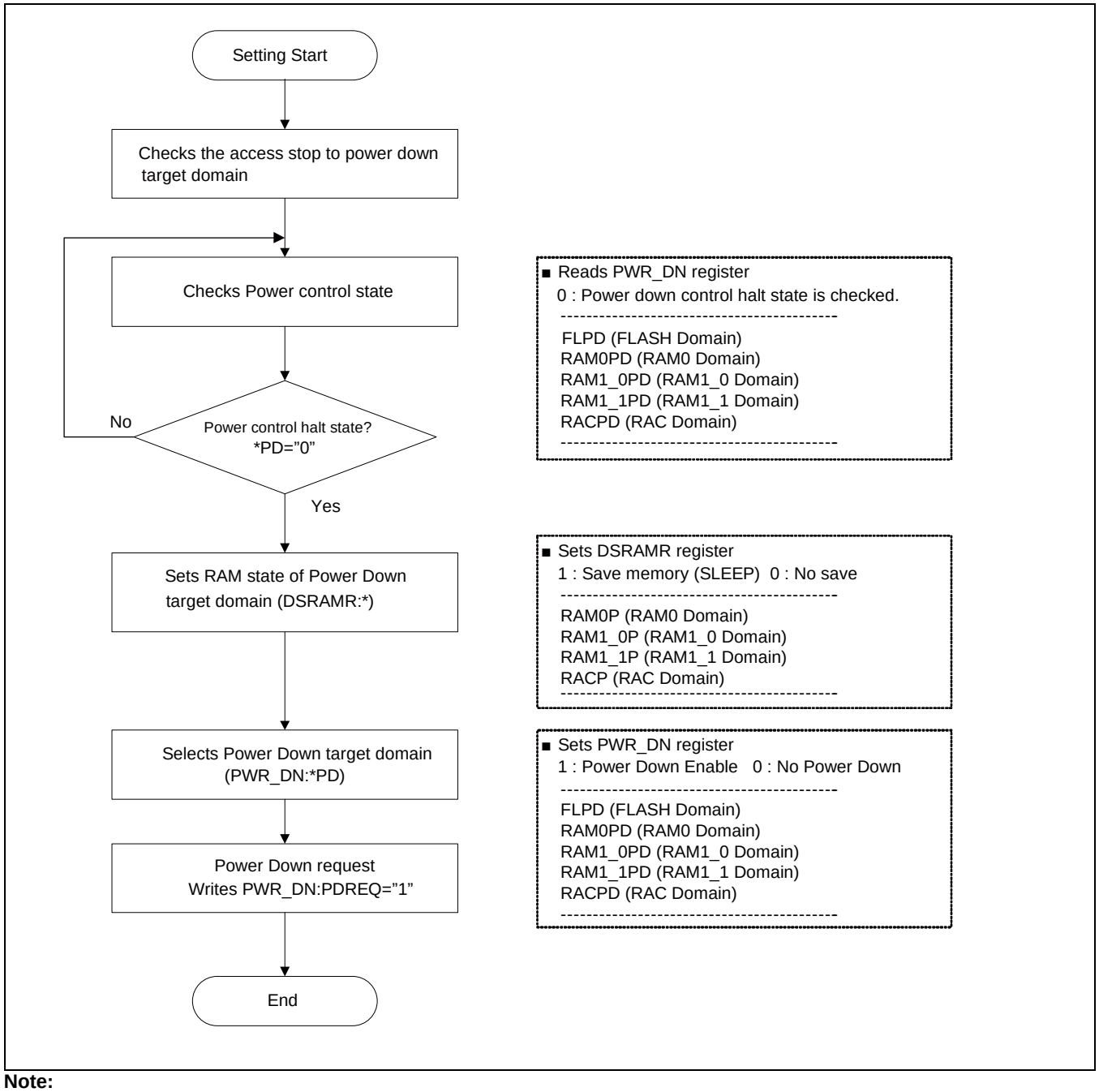
At the transition to deep standby mode, the power supply of the CPU is turned off after deep standby transition reset. Therefore, the value of the reset factor register (RST_STR) is invalid when returning from deep standby mode.

2.8 Power Supply OFF/SLEEP for Every Power Supply Domain by Register Control

This section explains the power supply / SLEEP setup steps of each power supply domain.

- **Power Down Control**

Figure 2.8-1 Example of Power Supply OFF setup steps by register control



Note:

When you repeat and carry out operation, set up, after more than 10µs wait.

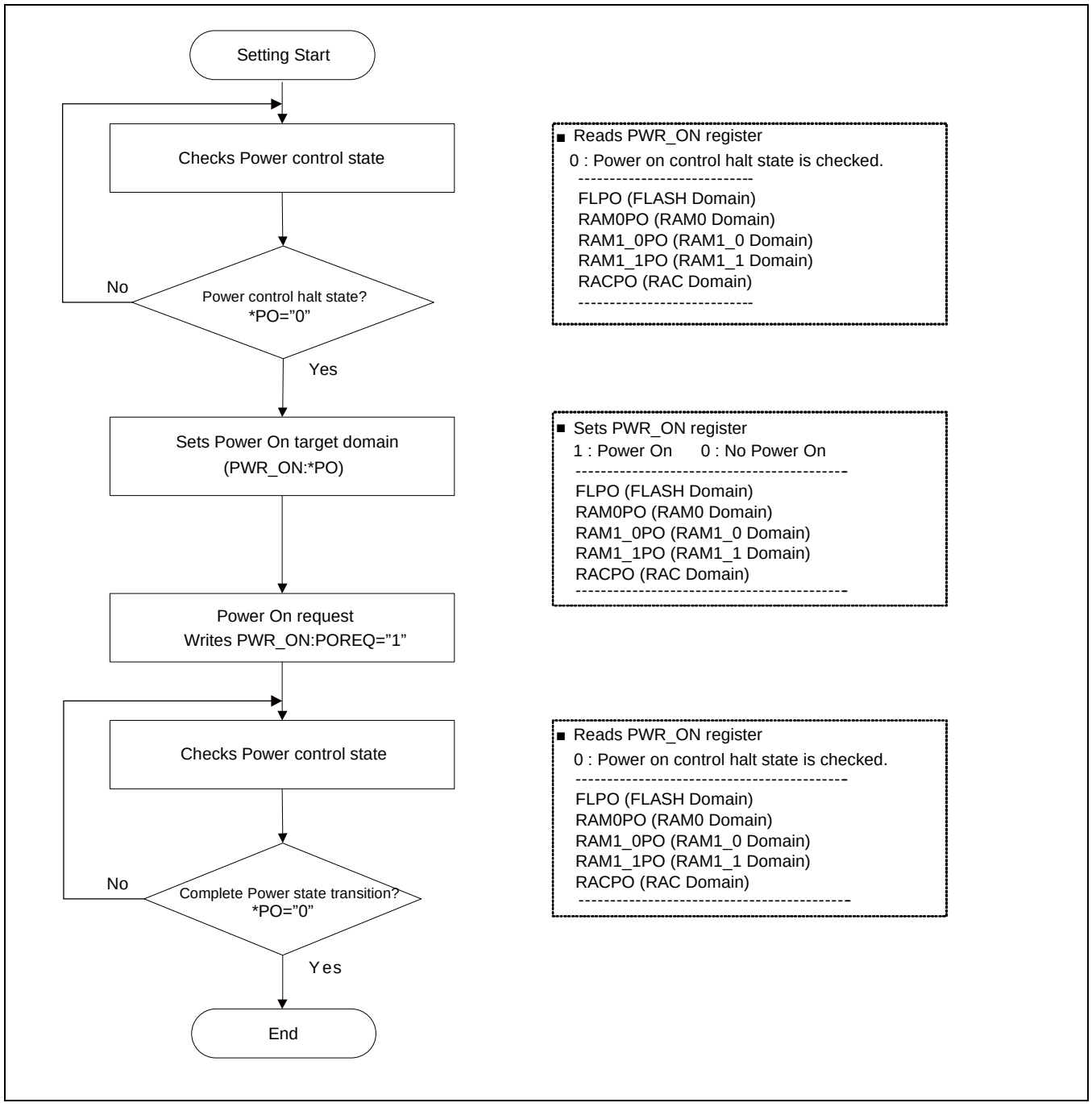
Table 2.8-1 shows power down setting (PWR_DN register) and Power supply domain status.

Table 2.8-1 Power down setting and Power supply domain status

Power down control(PWR_DN)					RAM retention control (DSRAMR)				Each power supply domain status				
FLPD	RAM0PD	RAM1_0PD	RAM1_1PD	RACPD	RAM0P	RAM1_0P	RAM1_1P	RACP	Flash	RAM0	RAM1_0	RAM1_1	RAC
0	0	0	0	0	-	-	-	-	hold	hold	hold	hold	hold
1	0	0	0	0	0	0	0	0	OFF	hold	hold	hold	hold
0	1	0	0	0	0	0	0	0	hold	OFF	hold	hold	hold
0	0	1	0	0	0	0	0	0	hold	hold	OFF	hold	hold
0	0	0	1	0	0	0	0	0	hold	hold	hold	OFF	hold
0	0	0	0	1	0	0	0	0	hold	hold	hold	hold	OFF
1	1	1	1	1	1	0	0	0	OFF	SLEEP	OFF	OFF	OFF
1	1	1	1	1	0	1	0	0	OFF	OFF	SLEEP	OFF	OFF
1	1	1	1	1	0	0	1	0	OFF	OFF	OFF	SLEEP	OFF
1	1	1	1	1	0	0	0	1	OFF	OFF	OFF	OFF	SLEEP

■ **Power on Control**

Figure 2.8-2 Example of Power Supply ON setup steps by register control



Note:

When you repeat and carry out operation, set up, after more than 10µs wait.

Table 2.8-2 shows power on setting(PWR_ON register) and power supply domain status.

Table 2.8-2 Power on setting and Power supply domain status

Power On control (PWR_ON)					RAM retention control (DSRAMR)				Each power supply domain status				
FLPO	RAM0PO	RAM1_0PO	RAM1_1PO	RACPO	RAM0P	RAM1_0P	RAM1_1P	RACP	Flash	RAM0	RAM1_0	RAM1_1	RAC
0	0	0	0	0	-	-	-	-	hold	Hold	hold	hold	Hold
1	0	0	0	0	-	-	-	-	ON	Hold	hold	hold	Hold
0	1	0	0	0	-	-	-	-	hold	ON SLEEP Release	hold	hold	Hold
0	0	1	0	0	-	-	-	-	hold	Hold	ON SLEEP Release	hold	Hold
0	0	0	1	0	-	-	-	-	hold	Hold	hold	ON SLEEP Release	Hold
0	0	0	0	1	-	-	-	-	hold	Hold	hold	hold	ON SLEEP Release

It is not based on the RAM retention control register, but is turned on power by setting "1" to the power on control register at power down, and SLEEP is canceled at SLEEP.

2.9 List of Low Power Consumption Mode Registers

This section explains the configuration and functions of the registers used in low power consumption mode.

- **List of Low Power Consumption Mode Registers**

Abbreviation	Register name	Reference
STB_CTL	Standby Mode Control Register	2.9.1

☐ Registers of Deep Standby Control Block

Abbreviation	Register name	Reference
RCK_CTL	Sub clock control register	2.9.2
PMD_CTL	RTC mode control register	2.9.3
WRFSR	Deep standby return factor register 1	2.9.4
WIFSR	Deep standby return factor register 2	2.9.5
WIER	Deep standby return enable register	2.9.6
WILVR	WKUP pin input level register	2.9.7

Abbreviation	Register name	Reference
RCK_CTL	Sub clock control register	2.9.2
DSRAMR	Deep standby RAM retention register	2.9.8
PWR_DN	Power down control register	2.9.9
PWR_ON	Power on control register	2.9.10
PWR_ST	Power supply status register	2.9.11
BUR01 to 12	Backup registers from 01 to 12	2.9.12

☐ Registers of PGA Power Supply Control Block

Abbreviation	Register name	Reference
PGA_PWR	PGA power supply setting register	2.9.13
PGA_XSTB	PGA standby register	2.9.14

Note:

- For the System Clock Mode Selection Register, refer to Chapter "Clock" in "Peripheral manual".
- Registers of the deep standby control block are not turned off in deep standby mode.

2.9.1 Standby Mode Control Register (STB_CTL)

Standby mode control register controls standby mode and deep standby mode. The value written to the SPL, DSTM or STM bit is effective only when 0x1ACC is simultaneously written to the KEY bit.

.

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8
Field	KEY																Reserved							
Attribute	R/W																-							
Initial value	0x0000																0x00							

bit	7	6	5	4	3	2	1	0
Field	Reserved			SPL	Reserved	DSTM	STM	
Attribute	-			R/W	-	R/W	R/W	
Initial value	000			0	0	0	00	

[bit31:16] KEY: Standby mode control write control bits

These bits release the SPL bit, DSTM bit or STM bit writing control.

The value written to the SPL bit, DSTM bit or STM bit is effective only when 0x1ACC is written to the KEY bit.

If a value other than 0x1ACC is written to the KEY bit, the value written to the SPL bit, DSTM bit or STM bit is not effective.

0x0000 is always read in read mode.

[bit15:5] Reserved: Reserved bits

The read value is always "0".
Writing has no effect on operation.

[bit4] SPL: Standby pin level setting bit

This bit sets the status of pin in TIMER mode, RTC mode, STOP mode, Deep standby RTC mode, or Deep standby STOP mode.

Bit	Description
0	Retains status of each pin in TIMER mode, RTC mode, and STOP mode and switches to GPIO in deep standby RTC mode and deep standby stop mode. [Initial value]
1	Sets the status of each pin to high impedance in TIMER mode, RTC mode, STOP mode, Deep standby RTC mode, or Deep standby STOP mode.

[bit3] Reserved: Reserved bit

The read value is always "0".
Writing has no effect on operation.

[bit2] DSTM: Deep standby mode select bit

This bit selects transiting to either standby mode or deep standby mode.

[bit1:0] STM: Standby mode select bit

This bit is a combination of DSTM bit and RTCE bit of the RTC Mode Control Register (PMD_CTL) and selects transiting to any one of the following: TIMER mode, RTC mode, STOP mode, deep standby RTC mode, and deep standby STOP mode.

bit2	STM		RTCE bit	Description
	bit1	bit0		
0	0	0	0	TIMER mode [initial value]
0	0	0	1	Setting is prohibited.
0	0	1	0	Setting is prohibited.
0	0	1	1	Setting is prohibited.
0	1	0	0	STOP mode
0	1	0	1	RTC mode
0	1	1	0	Setting is prohibited.
0	1	1	1	Setting is prohibited.
1	0	0	0	Setting is prohibited.
1	0	0	1	Setting is prohibited.
1	0	1	0	Setting is prohibited.

bit2	STM		RTCE bit	Description
	bit1	bit0		
1	0	1	1	Setting is prohibited.
1	1	0	0	Deep standby STOP mode
1	1	0	1	Deep standby RTC mode
1	1	1	0	Setting is prohibited.
1	1	1	1	Setting is prohibited.

Note:

The written value to SPL bit, DSTM bit, STM bit of Standby Mode Control Register (STB_CTL) is valid only when "0x1ACC" is written to KEY bit at the same time. If a value other than "0x1ACC" is written to KEY bit, writing to SPL bit, DSTM bit, and STM bit becomes invalid.

2.9.2 Sub Clock Control Register (RCK_CTL)

Sub clock control register controls the clock to RTC, HDMI-CEC/remote control reception. Current consumption can be reduced by stopping the clock supply to unused resource.

Bit	7	6	5	4	3	2	1	0
Field	Reserved							RTCCKE
Attribute	-							R/W
Initial value	0000000							1

[bit7:1] Reserved: Reserved bits

The read value is always "0".
These bits have no effect on the operation in write mode.

[bit0] RTCCKE : RTC clock control bit

This bit controls sub clock for RTC macro.

bit	Description
0	Sub clock is not supplied to RTC macro.
1	Sub clock is supplied to RTC macro. [Initial value]

2.9.3 RTC Mode Control Register (PMD_CTL)

RTC mode control register controls either RTC mode or STOP mode and either deep standby RTC mode or deep standby STOP mode.

Bit	7	6	5	4	3	2	1	0
Field	Reserved							RTCE
Attribute	-							R/W
Initial value	0000000							0

[bit7:1] Reserved: Reserved bits

The read value is always "0".

Writing has no effect on the operation.

[bit0] RTCE: RTC mode control bit

This bit selects transiting to either RTC mode or STOP mode and either deep standby RTC mode or deep standby stop mode.

Bit	Description
0	STOP mode and deep standby stop mode [initial value]
1	RTC mode and deep standby RTC mode

Standby mode is selected when DSTM is "0" and deep standby mode is selected when DSTM is "1".

Notes:

- This register is not initialized by software reset and deep standby transition reset.
- Writing "1" to RTCE bit is valid only when the SORDY bit of the System Clock Mode Status Register (SCM_STR) is "1".
- Sub oscillation is enabled when RTCE is "1" regardless of the SOSCE bit value of System Clock Mode Control Register (SCM_CTL) and the SORDY bit value of the System Clock Mode Status Register (SCM_STR).

2.9.4 Deep Standby Return Factor Register 1 (WRFSR)

Deep standby return factor register 1 indicates return factors by low-voltage detection reset and the INITX pin input reset that occur in deep standby mode.

Bit	7	6	5	4	3	2	1	0
Field	Reserved						WLVDH	WINITX
Attribute	-						R/W	R/W
Initial value	000000						0	0

[bit7:2] Reserved: Reserved bits

The read value is always "0".

Writing has no effect on the operation.

[bit1] WLVHD: Low-voltage detection reset return bit

This bit indicates returning from deep standby mode by low-voltage detection reset.

bit	Description
0	Not returned by low-voltage detection reset [initial value]
1	Returned by low-voltage detection reset

[bit0] WINITX: INITX pin input reset return bit

This bit indicates returning from deep standby mode by INITX pin input reset.

Bit	Description
0	Not returned by INITX pin input reset [initial value]
1	Returned by INITX pin input reset

Notes:

- This register is initialized by power-on reset and low-voltage detection reset. It is not initialized by other reset factors. Also, all bits are cleared by reading.
- This register can be set only in the deep standby mode.

2.9.5 Deep Standby Return Factor Register 2 (WIFSR)

Deep standby return factor register 2 indicates return factors by WKUPx pin input, low-voltage detection interrupt, and RTC interrupt that occur in deep standby mode.

Bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	-							
Initial value	0x00							

Bit	7	6	5	4	3	2	1	0
Field	Reserved		WUI3	WUI2	WUI1	WUI0	WLVDI	WRTCI
Attribute	-		R	R	R	R	R	R
Initial value	00		0	0	0	0	0	0

[bit15:6] Reserved: Reserved bits

The read value is always "0".
Writing has no effect on the operation.

[bit5:2] WUI3 to WUI0: WKUP pin input return bits

These bits indicate returning from deep standby mode by WKUPx pin input.

Bit	Description
0	Not returned by WKUPx pin input [initial value]
1	Returned by WKUPx pin input

[bit1] WLVDI: LVD interrupt return bit

This bit indicates returning from deep standby mode by LVD interrupt.

bit	Description
0	Not returned by LVD interrupt [initial value]
1	Returned by LVD interrupt

[bit0] WRTCI: RTC interrupt return bit

This bit indicates returning from deep standby mode by RTC interrupt.

bit	Description
0	Not returned by RTC interrupt [initial value]
1	Returned by RTC interrupt

Notes:

- This register is initialized by power-on reset and low-voltage detection reset. It is not initialized by other reset causes. Also, all bits are cleared by reading.
- This register can be set only in the deep standby mode.

2.9.6 Deep Standby Return Enable Register (WIER)

Deep standby return enable register enables a return by WKUPx pin input, low-voltage detection interrupt, RTC interrupt that occur in deep standby mode.

Bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	-							
Initial value	0x00							

Bit	7	6	5	4	3	2	1	0
Field	Reserved		WUI3E	WUI2E	WUI1E	Reserved	WLVDE	WRTCE
Attribute	-		R	R	R	R	R	R
Initial value	00		0	0	0	0	0	0

[bit15:6] Reserved: Reserved bits

The read value is always "0".
Writing has no effect on the operation.

[bit5:3] WUI3E to WUI1E: WKUPx pin input return enable bits

A return from deep standby mode by WKUPx pin input is disabled or enabled.

Bit	Description
0	Disable a return by WKUPx pin input [initial value]
1	Enable a return by WKUPx pin input

[bit2] Reserved: Reserved bit

The read value is always "0".

Writing has no effect on the operation.

[bit1] WLVDE: LVD interrupt return enable bit

A return from deep standby mode by LVD interrupt is disabled or enabled.

Bit	Description
0	Disable a return by LVD interrupt [initial value]
1	Enable a return by LVD interrupt

[bit0] WRTCE: RTC interrupt return enable bit

A return from deep standby mode by RTC interrupt is disabled or enabled.

Bit	Description
0	Disable a return by RTC interrupt [initial value]
1	Enable a return by RTC interrupt

Notes:

- A return from deep standby mode by WKUP0 pin input is always enabled.
- This register is not initialized by deep standby transition reset.

2.9.7 WKUP Pin Input Level Register (WILVR)

WKUP pin input level register selects a valid level of WKUP1 to WKUP3 pin inputs that occur in deep standby mode.

Bit	7	6	5	4	3	2	1	0
Field	Reserved					WUI3LV	WUI2LV	WUI1LV
Attribute	-					R/W	R/W	R/W
Initial value	00000					0	0	0

[bit7:3] Reserved: Reserved bits

The read value is always "0".

Writing has no effect on the operation.

[bit2:0] WUI3LV to WUI1LV: WKUP pin input level select bits

A valid level of WKUP pin input is selected.

Bit	Description
0	Request a return when WKUPx pin input is Low level [initial value]
1	Request a return when WKUPx pin input is High level

Notes:

- WKUP0 pin input always requests a return in Low level

  For example, it returns as soon as it transits to deep standby mode when WKUP1 inputs in Low level (WUI1LV = 0).

- This register is not initialized by deep standby transition reset.

2.9.8 Deep Standby RAM Retention Register (DSRAMR)

Deep standby RAM retention register controls the retention of the on-chip SRAM contents in deep standby modes.

Bit	7	6	5	4	3	2	1	0
Field	Reserved				RACR	RAM1_1R	RAM1_0R	RAM0R
Attribute	-				R/W	R/W	R/W	R/W
Initial value	0000				0	0	0	0

[bit7:4] Reserved: Reserved bits

The read value is always "0".

Writing has no effect on the operation.

[bit3] RACR : RAC domain on chip SRAM retention control bit

This bit performs retention control of the contents of RAC domain SRAM at deep standby mode.

bit	Description
0	The contents of RAC domain SRAM are not held at deep standby mode. [Initial value]
1	The contents of RAC domain SRAM are held at deep standby mode.

[bit2] RAM1_1R : RAM1_1 domain on chip SRAM retention control bit

This bit performs retention control of the contents of RAM1_1 domain SRAM at deep standby mode.

bit	Description
0	The contents of RAM1_1 domain SRAM are not held at deep standby mode. [Initial value]
1	The contents of RAM1_1 domain SRAM are held at deep standby mode.

[bit1] RAM1_0R : RAM1_0 domain on chip SRAM retention control bit

This bit performs retention control of the contents of RAM1_0 domain SRAM at deep standby mode.

bit	Description
0	The contents of RAM1_0 domain SRAM are not held at deep standby mode. [Initial value]
1	The contents of RAM1_0 domain SRAM are held at deep standby mode.

[bit0] RAM0R : RAM0 domain on chip SRAM retention control bit

This bit performs retention control of the contents of RAM0 domain SRAM at deep standby mode.

Bit	Description
0	The contents of RAM0 domain SRAM are not held at deep standby mode. [Initial value]
1	The contents of RAM0 domain SRAM are held at deep standby mode.

Note:

This register is initialized by power-on reset and low-voltage detection reset. It is not initialized by other reset causes.

2.9.9 Power Down Control Register (PWR_DN)

This register is register which controls the power down of each power supply domain. A power down request can be validated by setting up PDREQ=1 after a power down request setup of each power supply domain. When memory maintenance is set up by the DSRAMR register, RAM domain serves as SLEEP mode instead of power supply intercept.

Bit	31	30	29	28	27	26	25	24
Field	PDREQ	Reserved						
Attribute	W	R						
Initial value	X	0000000						

Bit	23	22	21	20	19	18	17	16
Field	Reserved							
Attribute	R							
Initial value	0x00							

Bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	R							
Initial value	0x00							

Bit	7	6	5	4	3	2	1	0
Field	Reserved			FLPD	RACPD	RAM1_1PD	RAM1_0PD	RAM0PD
Attribute	R			R/W	R/W	R/W	R/W	R/W
Initial value	000			0	0	0	0	0

[bit31] PDREQ : Power Down request Control bit

This bit controls power down of request start.

bit	Description
0	Disable
1	Power down request

[bit30:5] Reserved: Reserved bits

The read value is always "0".
Writing has no effect on operation.

[bit4] FLPD : FLASH Power Down Control bit

This bit cleared to "0" by hardware after power down control completed.

bit	Description
0	Write : Not power down [Initial value] Read : Power down control halt condition
1	Write : Power down Read : Power down change

[bit3] RACPD : RAC Power Down Control bit

This bit cleared to "0" by hardware after power down control completed.

Bit	Description
0	Write : Not power down [Initial value] Read : Power down control halt condition
1	Write : Power down Read : Power down change

[bit2] RAM1_1PD : RAM1_1 Power Down Control bit

This bit cleared to "0" by hardware after power down control completed.

Bit	Description
0	Write : Not power down [Initial value] Read : Power down control halt condition
1	Write : Power down Read : Power down change

[bit1] RAM1_0PD : RAM1_0 Power Down Control bit

This bit cleared to "0" by hardware after power down control completed.

bit	Description
0	Write : Not power down [Initial value] Read : Power down control halt condition
1	Write : Power down Read : Power down change

[bit0] RAM0PD : RAM0 Power Down Control bit

This bit cleared to "0" by hardware after power down control completed.

Bit	Description
0	Write : Not power down [Initial value] Read : Power down control halt condition
1	Write : Power down Read : Power down change

2.9.10 Power On Control Register (PWR_ON)

This register is registered which controls power-on of each power supply domain. A power on demand can be validated by setting up POREQ=1 after a power on demand setup of each power supply domain. SLEEP release of RAM is also canceled by this register setup.

Bit	31	30	29	28	27	26	25	24
Field	POREQ	Reserved						
Attribute	W	R						
Initial value	X	0000000						

Bit	23	22	21	20	19	18	17	16
Field	Reserved							
Attribute	R							
Initial value	0x00							

Bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	R							
Initial value	0x00							

Bit	7	6	5	4	3	2	1	0
Field	Reserved			FLPO	RACPO	RAM1_1PO	RAM1_0PO	RAM0PO
Attribute	R			R/W	R/W	R/W	R/W	R/W
Initial value	000			0	0	0	0	0

[bit31] POREQ : Power on Request Control bit

This bit controls request start of power on.

This bit is Write-only. The read value is undefined.

Bit	Description
0	Disable
1	Power on request

[bit30:5] Reserved: Reserved bits

The read value is always "0".
Writing has no effect on operation.

[bit4] FLPO : FLASH Power on Control bit

This bit cleared to "0" by hardware after power on control completed.

bit	Description
0	Write : Not power on [Initial value] Read : Power on control halt condition
1	Write : Power on Read : Power on change

[bit3] RACPO: RAC Power on Control bit

This bit cleared to "0" by hardware after power on control completed.

bit	Description
0	Write : Not power on [Initial value] Read : Power on control halt condition
1	Write : Power on Read : Power on change

[bit2] RAM1_1PO: RAM1_1 Power on Control bit

This bit cleared to "0" by hardware after power on control completed.

bit	Description
0	Write : Not power on [Initial value] Read : Power on control halt condition
1	Write : Power on Read : Power on change

[bit1] RAM1_0PO : RAM1_0 Power on Control bit

This bit cleared to "0" by hardware after power on control completed.

bit	Description
0	Write : Not power on [Initial value] Read : Power on control halt condition
1	Write : Power on Read : Power on change

[bit0] RAM0PO : RAM0 Power on Control bit

This bit cleared to "0" by hardware after power on control completed.

Bit	Description
0	Write : Not power on [Initial value] Read : Power on control halt condition
1	Write : Power on Read : Power on change

2.9.11 Power Supply Status Register (PWR_ST)

This register is power supply status register of each power supply domain. This register is read-only and a user cannot write.

Bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	R							
Initial value	0x00							

Bit	23	22	21	20	19	18	17	16
Field	Reserved				RACSLP	RAM1_1SLP	RAM1_0SLP	RAM0SLP
Attribute	R				R	R	R	R
Initial value	0000				0	0	0	0

Bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	R							
Initial value	0x00							

Bit	7	6	5	4	3	2	1	0
Field	Reserved			FLST	RACST	RAM1_1ST	RAM1_0ST	RAM0ST
Attribute	R			R	R	R	R	R
Initial value	000			1	1	1	1	1

[bit31:20] Reserved : Reserved bits

The read value is always "0".
Writing has no effect on operation.

[bit19] RACSLP : RAC RAM SLEEP Status Register

Bit	Description
0	SLEEP release [Initial value]
1	SLEEP status

[bit18] RAM1_1SLP : RAM1_1 SLEEP Status Register

Bit	Description
0	SLEEP release [Initial value]
1	SLEEP status

[bit17] RAM1_0SLP : RAM1_0 SLEEP Status Register

Bit	Description
0	SLEEP release [Initial value]
1	SLEEP status

[bit16] RAM0SLP : RAM0 SLEEP Status Register

Bit	Description
0	SLEEP release [Initial value]
1	SLEEP status

[bit15:5] Reserved : Reserved bits

The read value is always "0".
Writing has no effect on operation.

[bit4] FLST : FLASH Power Status Register

Bit	Description
0	OFF
1	ON [Initial value]

[bit3] RACST : RAC Power Status Register

bit	Description
0	OFF
1	ON [Initial value]

[bit2] RAM1_1ST : RAM1_1 Power Status Register

bit	Description
0	OFF
1	ON [Initial value]

[bit1] RAM1_0ST : RAM1_0 Power Status Register

bit	Description
0	OFF
1	ON [Initial value]

[bit0] RAM0ST : RAM0 Power Status Register

bit	Description
0	OFF
1	ON [Initial value]

2.9.12 Backup Registers from 01 to 12 (BUR01 to 12)

Backup registers (BUR) are general registers that retain values in deep standby mode.

Bit	31 24	23 16	15 8	7 0
Field	BUR04	BUR03	BUR02	BUR01
Attribute	R/W	R/W	R/W	R/W
Initial value	0x00	0x00	0x00	0x00

bit	31 24	23 16	15 8	7 0
Field	BUR08	BUR07	BUR06	BUR05
Attribute	R/W	R/W	R/W	R/W
Initial value	0x00	0x00	0x00	0x00

bit	31 24	23 16	15 8	7 0
Field	BUR12	BUR11	BUR10	BUR09
Attribute	R/W	R/W	R/W	R/W
Initial value	0x00	0x00	0x00	0x00

Note:

This register is initialized by power-on reset and low-voltage detection reset. It is not initialized by other reset factors.

2.9.13 PGA Power Supply Setting Register (PGA_PWR)

PGA Power Supply Setting Register (PGA_PWR) controls PGA of power supply.

bit	7	6	5	4	3	2	1	0
Field	Reserved							PGA_PWR
Attribute	-							R/W
Initial value	-							0

[bit7:1] Reserved : Reserved bits

The read value is undefined.
Writing has no effect on operation.

[bit0] PGA_PWR : PGA Power Supply Control bit

This bit selects power supply of PGA.

Bit	Operation
0	Stops power supply [Initial value]
1	Perform power supply.
When reading	The register value is read.

2.9.14 PGA Standby Control Register (PGA_XSTB)

PGA Standby Control Register (PGA_XSTB) controls standby /Ready mode of PGA.

Bit	7	6	5	4	3	2	1	0
Field	Reserved							PGA_XSTB
Attribute	-							R/W
Initial value	-							0

[bit7:1] Reserved : Reserved bits

The read value is undefined.
Writing has no effect on operation.

[bit0] PGA_XSTB : PGA Standby Control bit

This bit selects standby/ready mode.

Bit	Operation
0	Standby [Initial value]
1	Ready mode
When reading	The register value is read.

2.10 Usage Precautions

Note on the following points when using low power consumption mode.

For the pin shared for analog input and WKUP, WKUPx pin input is blocked when ADE is set to 1 even if the recovery by WKUPx pin input is allowed. To use the recovery by WKUPx pin input, set ADE to 0 before shifting to deep standby mode.

3. I/O Port

This chapter explains the I/O Port

3.1 Overview

3.2 Configuration, Block Diagram, and Operation

3.3 Setup Procedure Example

3.4 Registers

3.5 Usage Precautions

3.1 Overview

The I/O port of this series provides the following features.

The I/O port of this series shares the following functions.

- GPIO

  General-purpose I/O ports, which can read an input level and set an output level from the CPU.

- Peripheral input/output
- Digital input/output signal ports of peripheral functions.
- Special I/O ports
  - ☐ Analog input port

  An analog input port of an A/D converter and PGA.

  - ☐ Oscillation port

The followings settings can be made for each pin.

- You can set whether the I/O port will be used as a GPIO, a digital pin of peripheral functions, or a special pin.
- You can set whether the I/O port will be used as an input port or an output port.
- You can enable or disable pull-up.
- Peripheral functions are assigned to two or more I/O ports with input/output of the same function. You can set to which I/O port the function can be allocated (relocation function).
- By setting registers, you can set the I/O port to Hi-Z status while the CPU is in standby mode.

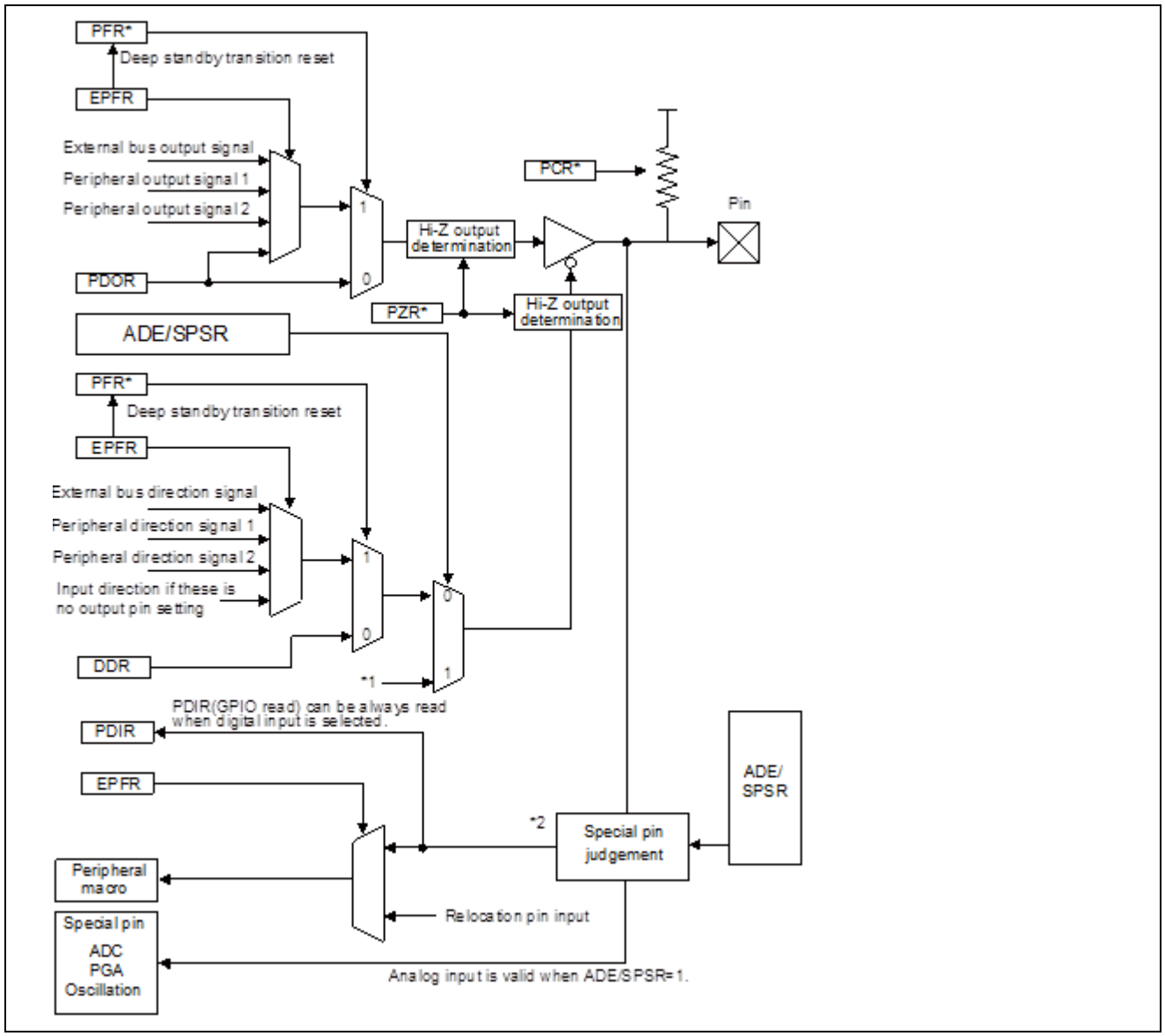
3.2 Configuration, Block Diagram, and Operation

This section explains the configuration, block diagram, and operation of the I/O port.

- Configuration of the I/O Port

By setting registers of the I/O port, select Input/Output direction and select GPIO/peripheral. Figure 3.2-1 shows the details of the I/O port.

Figure 3.2-1 Block Diagram of the I/O Port



*1: When one of the followings is set, I/O port is set to input direction.

ADE/SPSR=1

*2: When one of the followings is set, the input value is fixed to "0".

Otherwise, the pin is set as the digital input pin.

ADE/SPSR=1

Notes:

- PZR register function is implemented only in some specific pins.
- Only pins described as "PZR register control is enabled" in the remarks column of "□□/O CIRCUIT TYPE" of the Data Sheet can control this feature.
- PFR0 register is not initialized by deep standby transition reset.

Table 3.2-1 describes register function.

- The PFR, DDR, PDIR, PDOR, and PCR register have 1-bit control register for each I/O port and select a function for the I/O port.
- The ADE register has 1-bit control register for each I/O port which doubles as an analog input pin and selects a function for the I/O port.
- The SPSR register selects a function for the I/O port which doubles as an oscillation pin.
- The EPFR register has control register for each I/O pin of peripheral functions and selects to which I/O port an I/O pin of peripheral functions will be relocated.
- PZR register sets open drain control in pseudo mode by the Hi-Zing I/O port when outputting the High level of a particular pin.

Table 3.2-1 Register Function Descriptions

Register name	Function description
ADE	A register to set whether the I/O port will be used as a special pin (analog input pins) or a digital input/output pin.
SPSR	A register to set whether the I/O port will be used as a special pin (oscillation) or a digital input/output pin.
PFR	A register to set whether the I/O port will be used as an input/output pin of GPIO function or an input/output pin of peripheral functions.
PCR	A register to set whether a pull-up resistor of the I/O port will be connected or disconnected if the I/O port is used as a digital input pin or a digital bidirectional pin.
DDR	A register to set whether the I/O port will be used as an input pin or an output pin if the I/O port is used as a GPIO function pin. Note: If a pin is selected as an I/O pin of peripheral functions, a setting value is invalid.
PDIR	A register to read the level status of the I/O port. If the I/O port is used as a digital input pin, it reads input level. If the I/O port is used as a digital output pin, it reads output level. If the I/O port is used as an analog input pin, it always reads "0".

Register name	Function description
PDOR	A register to set output level if the I/O port is used as an output pin of GPIO function. When "0" is set, it outputs Low level. When "1" is set, it outputs High level. Note: If a pin is selected as GPIO input or input/output of peripheral functions, a setting value is invalid.
EPFR	A register to select a function for an input/output of peripheral functions and set relocation function. Setting a peripheral output pin It sets whether to produce output for the I/O port or not. In addition, it can also set to which I/O port a pin of peripheral functions will be relocated for each pin. Setting a peripheral input pin It can set to which I/O port a pin of peripheral functions will be relocated for each pin. Setting a peripheral bidirectional pin It can set to which I/O port a pin of peripheral functions will be relocated for each pin
PZR	This register sets open the drain control of the I/O port. Set the I/O port to Low output when the I/O port is outputting Low level (pull-up disconnection regardless of PCR setting value) Set open drain control in pseudo mode by setting the I/O port on Hi-Z status when the I/O port outputs High level (pull-up disconnection regardless of PCR setting value) Set the I/O port on Hi-Z status when the I/O port is used for input (pull-up disconnection regardless of PCR setting value) Note: This function is implemented only in some specific pins. Only pins described as "PZR register control is enabled" in the remarks column of "□□/O CIRCUIT TYPE" of the Data Sheet can control the open drain.

Table 3.2-2 lists pin functions which availability depends on selected I/O port functions and register setting values.

Table 3.2-2 I/O Port Functions and Register Setting Values

I/O Port Function		ADE/ SPSR	PFR	DDR	PZR	PCR	EPFR
Available main function	Available sub function						
Special pin (Analog input, Oscillation)	N/A	1	-	-	-	Disconnect	*0
GPIO function input pin	Peripheral function input pin	0	0	0	0	Valid	*1
				0	1	Disconnect	
GPIO function output pin	GPIO function input pin (FB) Peripheral function input pin (FB)			1	0	Disconnect	
				1	1	Disconnect	
Peripheral function output pin	GPIO function input pin (FB)		1	-	0	Disconnect	*2

I/O Port Function		ADE/ SPSR	PFR	DDR	PZR	PCR	EPFR
Available main function	**Available sub function**						
	Peripheral function input pin (FB)				1	Disconnect	
Peripheral function bidirectional pin	GPIO function input pin (FB)				0	Valid	*3
	Peripheral function input pin (FB)				1	Disconnect	
Peripheral function input pin	GPIO function input pin				0	Valid	*4
					1	Disconnect	

Legends

- : Indicates that a register setting value does not affect pin functions.

Valid:Indicates that a pull-up resistor is disconnected if PCR register value is 0.
Indicates that a pull-up resistor is connected if PCR register value is 1.

Disconnect: Indicates that a pull-up resistor is disconnected regardless of PCR register value.

(FB) :Indicates that an output signal of the I/O port provides feedback and the level of the I/O port can be read from PDIR. The signal can be also used as input for peripheral functions.

*0:If the input pin of peripheral functions is selected for the I/O port, the setting is invalid.
If the output pin of peripheral functions is selected for the I/O port, the setting is invalid.
If the bidirectional pin of peripheral functions is selected for the I/O port, the setting is invalid.

*1: If the input pin of peripheral functions is selected for the I/O port, the setting is valid.
If the output pin of peripheral functions is selected for the I/O port, the setting is invalid.
If the bidirectional pin of peripheral functions is selected for the I/O port, the setting is invalid.

*2: Indicates that the output pin of peripheral functions is selected for the I/O port.

*3: Indicates that the bidirectional pin of peripheral functions is selected for the I/O port.

*4: Indicates that neither the output pin nor the bidirectional pin of peripheral functions is selected for the I/O port.

- **Initially Selected Functions for the I/O Port**

Table 3.2-3 describes initially selected functions for each I/O port after reset is released.

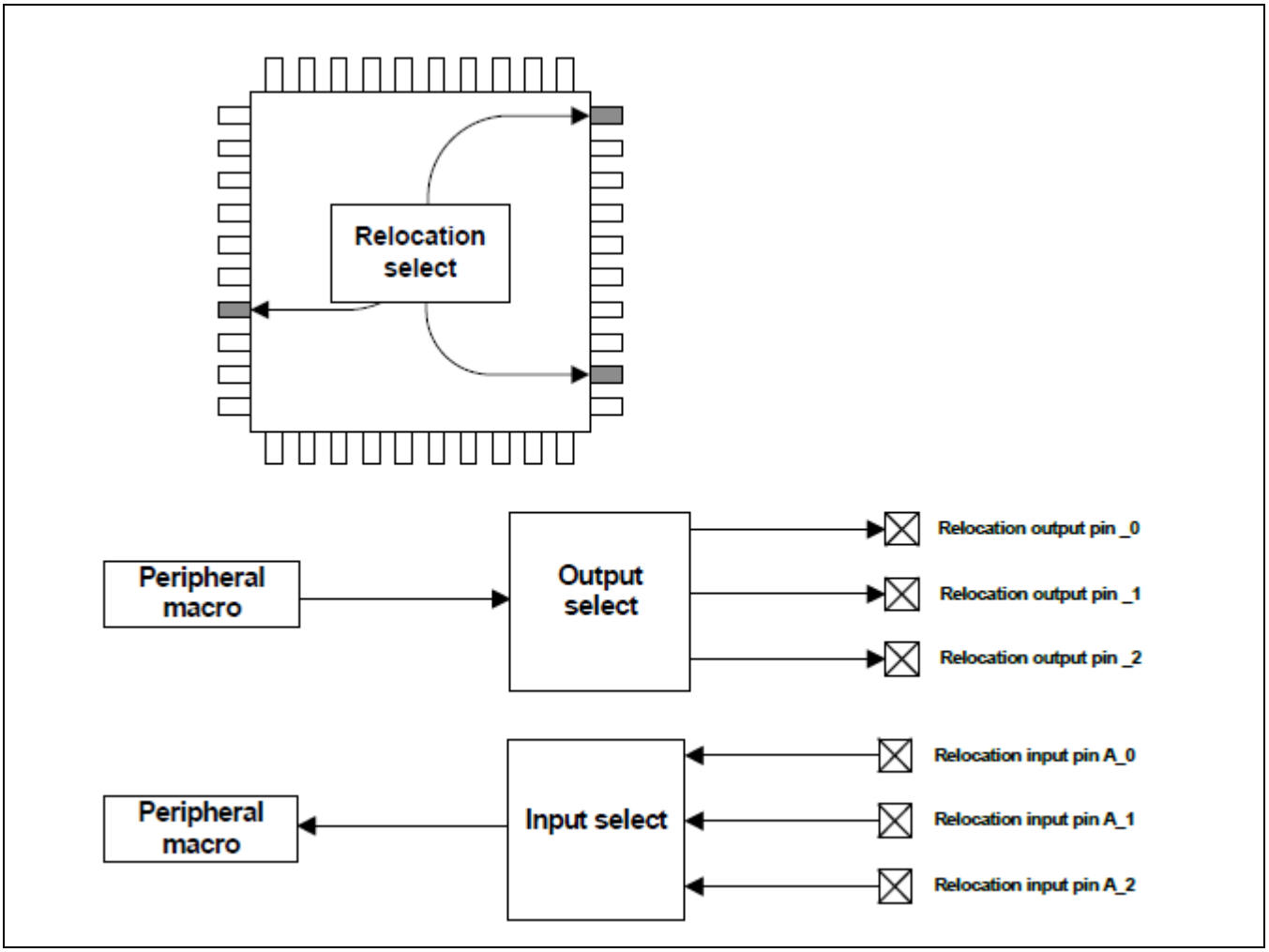
Table 3.2-3 Initially Selected Functions for Each I/O Port after Reset Is Released

No	Pin	Initially selected function
1	TRSTX, TCK, TDI, TMS, TDO	JTAG pin is selected. Pull-up is enabled.
2	AN07 to AN00	Can be used as an analog input pin. Digital input is cut off and "0" is input.
3	X0,X1,X0A, X1A	Can be used as an oscillation pin. Digital input is cut off and "0" is input.
4	All GPIO pins other than the above pins	Digital input. Output is Hi-Z.

Note:
For the status of pins other than GPIO (MD pins, a reset pin), see "Data Sheet" of this product.
All the output selection values of EPFR during reset are "no output".

- **Relocation Function**
  - Some input/output of peripheral functions have more than one pin (relocation pin).
    One of the pins can be selected by setting EPFR. Figure 3.2-2 show the schematic view of relocation function.

Figure 3.2-2 Schematic View of Relocation Function

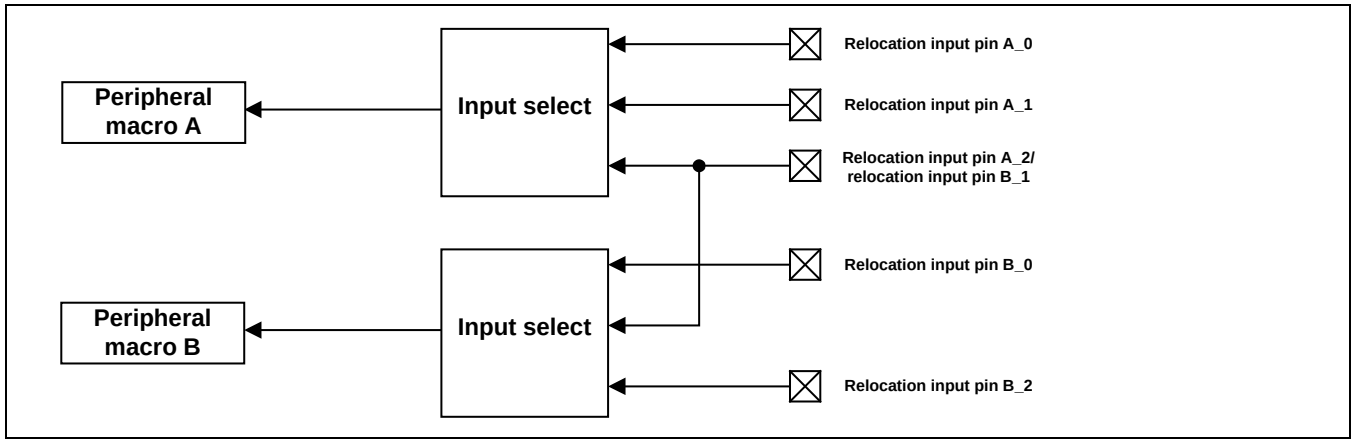


Note:

Which peripheral function is allocated to which pin depends see the pin function list of "Data Sheet" of this product.

- Even if the input of one I/O port is connected to two or more peripheral functions, all peripheral inputs can be used by setting EPFR. For example, in Figure 3.2-3, by selecting input for both "Relocation input pin A_2" and "Relocation input pin B_1", simultaneous usage is possible. In this way, it is possible to use external interrupt and a multi-function serial input pin shared by one I/O port simultaneously.

Figure 3.2-3 Multiple Peripheral Inputs



- Even if an I/O pin is set as output, it can work as an input pin because input is not masked. For example, timer output can be used as external interrupt input which shared.

■ **Fixed Priority of EPFR Outputs**

Only one output pin function among two or more outputs is allocated to one I/O port.
By setting the EPFR register, if more than one output is set, fixed priority is applied and output pins are selected. Figure 3.2-4 shows output pins and fixed priority.

Figure 3.2-4 Output Pins and Fixed Priority

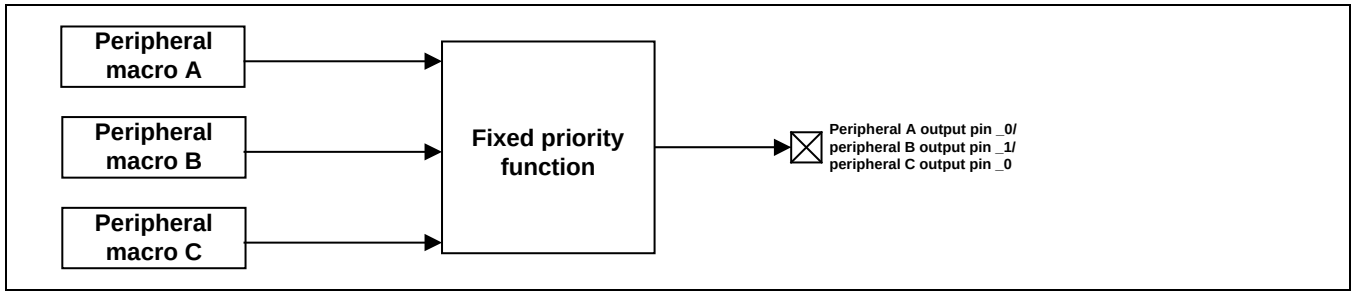


Table 3.2-4 describes the fixed priority of EPFR.

Table 3.2-4 Fixed Priority of EPFR

Priority Higher	Peripheral function	Applied pin
↓	Special input	JTAG input, NMI input
↓	JTAG	Output pin, I/O pin
↓	Multi-function serial	Output pin, I/O pin
↓	Base timer output	I/O pin
↓	Internal CR waveform output	Output pin
↓	RTC Output	Output pin
↓	SUBCLK Output	Output pin

Priority Higher	Peripheral function	Applied pin
Priority Lower		

Note:

The fixed priority is only applicable when "output" is set for more than one function. In case of "input", there is no fixed priority.
However, "Special input" has a higher priority than any other "output" setting. When "Special input" is set, the "output" setting allocated to the same port is invalid.

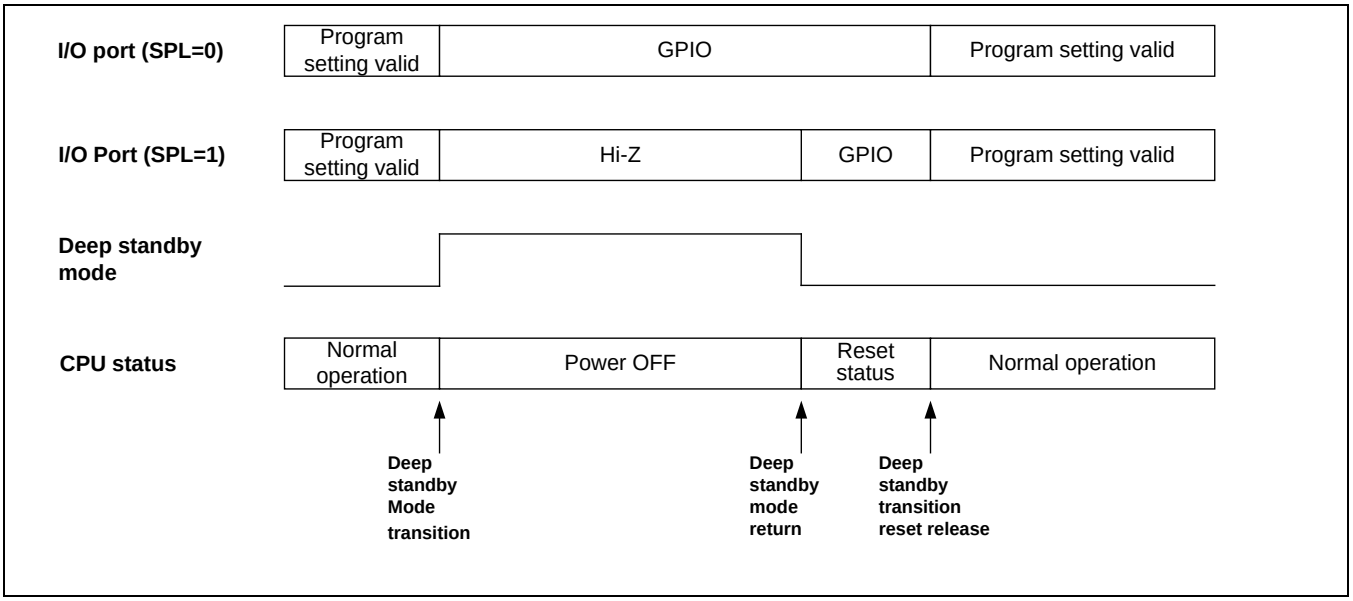
Because following are not lower contents of below Note.

- ☐ Due to output setting on the lower part of the priority, the EPFR register always includes "no output" setting.
- ☐ If you are going to use a pin as an external input pin of peripheral functions, disable all shared output settings. If every output of a pin is not selected by the EPFR register, the pin works as an external input pin.

■ Operation in deep standby mode

GPIO function is selected in deep standby mode. Figure 3.2-5 shows I/O port operation in deep standby mode.

Figure 3.2-5 I/O port operation in deep standby mode



Note

For the state of each pin in deep standby mode, refer to the pin state table in the "Data Sheet".

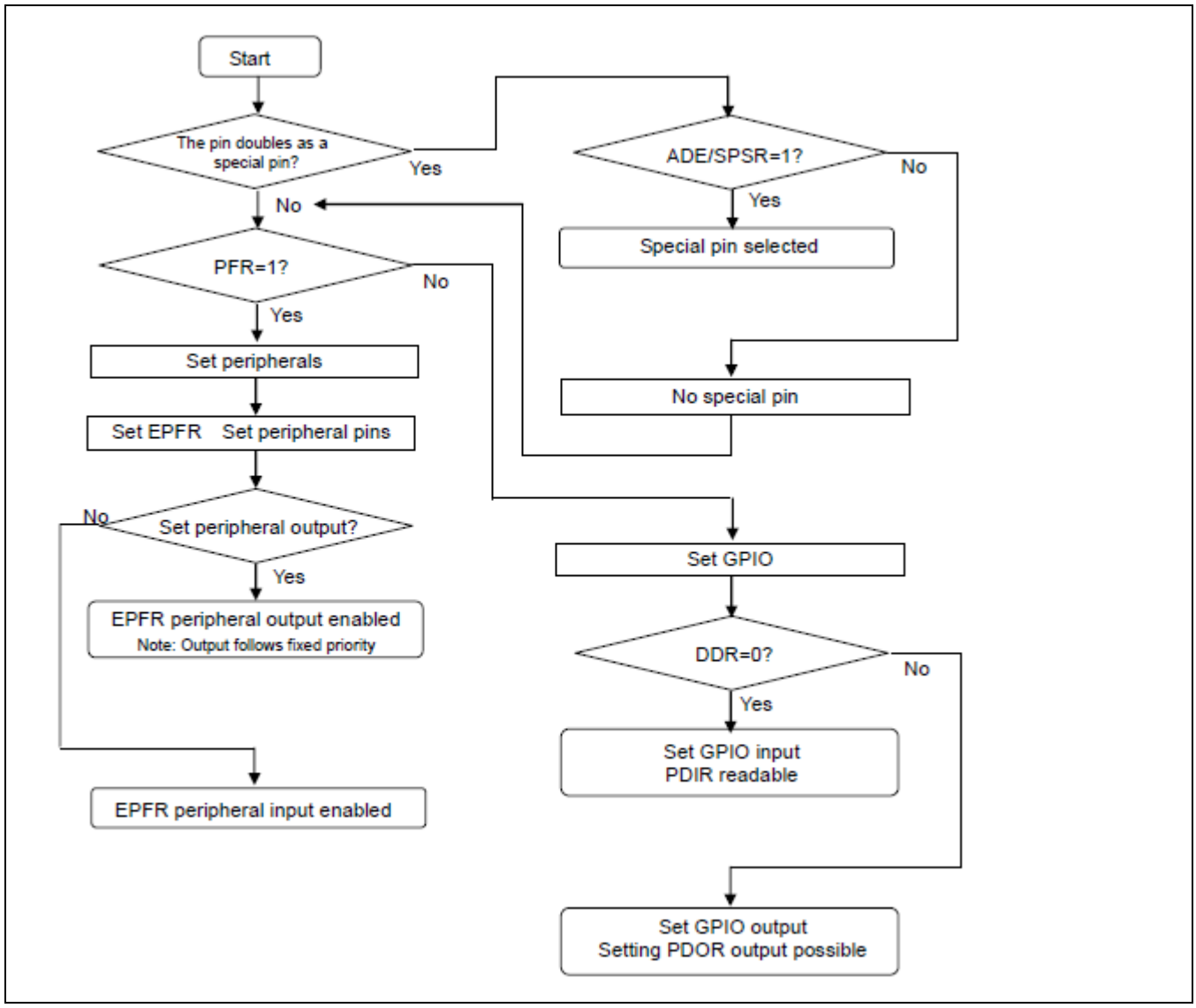
3.3 Setup Procedure Example

This section explains a procedure example of setting up the I/O port.

- Setup of the I/O Port

By setting registers of the I/O port, select I/O direction and select GPIO/peripheral.
Figure 3.3-1 shows a setup procedure example.

Figure 3.3-1 Setup Procedure Example of the I/O Port



3.4 Registers

This section provides the register list of the I/O port.

Table 3.4-1 provides the register list.

Table 3.4-1 Register List of the I/O Port

Abbreviation	Register name	Reference
PFR0	Port function setting register 0	3.4.1
PFR1	Port function setting register 1	
PFR2	Port function setting register 2	
PFR3	Port function setting register 3	
PFR4	Port function setting register 4	
PFR5	Port function setting register 5	
PFR6	Port function setting register 6	
PFRE	Port function setting register E	
PCR0	Pull-up setting register 0	3.4.2
PCR1	Pull-up setting register 1	
PCR2	Pull-up setting register 2	
PCR3	Pull-up setting register 3	
PCR4	Pull-up setting register 4	
PCR5	Pull-up setting register 5	
PCR6	Pull-up setting register 6	
PCRE	Pull-up setting register E	
DDR0	Port input/output direction setting register 0	3.4.3
DDR1	Port input/output direction setting register 1	
DDR2	Port input/output direction setting register 2	
DDR3	Port input/output direction setting register 3	
DDR4	Port input/output direction setting register 4	
DDR5	Port input/output direction setting register 5	
DDR6	Port input/output direction setting register 6	
DDRE	Port input/output direction setting register E	

Abbreviation	Register name	Reference
PDIR0	Port input data register 0	3.4.4
PDIR1	Port input data register 1	
PDIR2	Port input data register 2	
PDIR3	Port input data register 3	
PDIR4	Port input data register 4	
PDIR5	Port input data register 5	3.4.4
PDIR6	Port input data register 6	
PDIRE	Port input data register E	
PDOR0	Port output data register 0	3.4.5
PDOR1	Port output data register 1	
PDOR2	Port output data register 2	
PDOR3	Port output data register 3	
PDOR4	Port output data register 4	
PDOR5	Port output data register 5	
PDOR6	Port output data register 6	
PDORE	Port output data register E	
ADE	Analog input setting register	3.4.6
SPSR	Special Port Setting Register	3.4.15
EPFR00	Extended pin function setting register 00	3.4.8
EPFR04	Extended pin function setting register 04	3.4.9
EPFR05	Extended pin function setting register 05	3.4.10
EPFR06	Extended pin function setting register 06	3.4.11
EPFR07	Extended pin function setting register 07	3.4.12
EPFR08	Extended pin function setting register 08	3.4.13
EPFR09	Extended pin function setting register 09	3.4.14

Abbreviation	Register name	Reference
PZR0	Port pseudo open drain setting register 0	3.4.16
PZR1	Port pseudo open drain setting register 1	
PZR2	Port pseudo open drain setting register 2	
PZR3	Port pseudo open drain setting register 3	
PZR4	Port pseudo open drain setting register 4	
PZR5	Port pseudo open drain setting register 5	
PZR6	Port pseudo open drain setting register 6	
PZRE	Port pseudo open drain setting register E	

3.4.1 Port Function Setting Register (PFRx)

The PFRx register selects usage of a pin.

- **List of PFR Register Configuration**

Bit 31 to 16	Bit 15 to 0	Initial value	Attribute	Corresponding port
Reserved	PFR0	0x001F	R/W	P0F to P00
Reserved	PFR1	0x0000	R/W	P1F to P10
Reserved	PFR2	0x0000	R/W	P2F to P20
Reserved	PFR3	0x0000	R/W	P3F to P30
Reserved	PFR4	0x0000	R/W	P4F to P40
Reserved	PFR5	0x0000	R/W	P5F to P50
Reserved	PFR6	0x0000	R/W	P6F to P60
Reserved	-	-	-	-
Reserved	-	-	-	-
Reserved	-	-	-	-
Reserved	-	-	-	-
Reserved	-	-	-	-
Reserved	-	-	-	-
Reserved	-	-	-	-
Reserved	PFRE	0x0000	R/W	PEF to PE0
Reserved	-	-	-	-

- **Detailed Register Configuration**

Bit	31	16	15	0
Field	Reserved		PFRx	

- **Register Function**

[bit31:16] Reserved: Reserved bits

"0x0000" is read out from these bits.
When writing these bits, set them to "0x0000".

[bit15:0] PFRx: Port Function Setting Register x

Selects usage of a pin.

bit15:0		Description
Reading		Can read out the setting value of the register.
Writing	0	Uses a pin as a GPIO pin.
	1	Uses a pin as an input/output pin of peripheral functions.

Notes:

- The "x" of PFRx is a wildcard. PFRx indicates PFR0, PFR1, PFR2, etc.
- The "x" of Px0 and PxF is a wildcard. Px0 indicates P00, P10, P20, etc. PxF indicates P0F, P1F, P2F, etc.
- Functions can be set for 16 ports from PxF to Px0.
- Each bit in the register sets each pin individually. There is a one-to-one correspondence between bit assignment and the order of pins. For example, the 15th bit of PFR0 sets P0F, the 14th bit of PFR0 sets P0E, and the 0th bit of PFR0 sets P00.
- As a JTAG pin is selected for P04 to P00, the initial value is "1".
- PFR7 to PFRD and PFRF are not available.
- For a pin which is not available in this product, writing a value to the bit is invalid, and the read value is undefined.
- PFR0 register is not initialized by deep standby transition reset.

3.4.2 Pull-up Setting Register (PCRx)

The PCRx register sets pull-up of a pin.

- **List of PCR Register Configuration**

Bit	31 to 16	15 to 0	Initial value	Attribute	Corresponding port
Reserved	PCR0		0xFFFF	R/W	P0F to P00
Reserved	PCR1		0xFFFF	R/W	P1F to P10
Reserved	PCR2		0xFFFF	R/W	P2F to P20
Reserved	PCR3		0xFFFF	R/W	P3F to P30
Reserved	PCR4		0xFFFF	R/W	P4F to P40
Reserved	PCR5		0xFFFF	R/W	P5F to P50
Reserved	PCR6		0xFFFF	R/W	P6F to P60
Reserved	-		-	-	-
Reserved	-		-	-	-
Reserved	-		-	-	-
Reserved	-		-	-	-
Reserved	-		-	-	-
Reserved	-		-	-	-
Reserved	-		-	-	-
Reserved	PCRE		0xFFFF	R/W	PEF to PE0
Reserved	-		-	-	-

- **Detailed Register Configuration**

bit	31 to 16	15 to 0
Field	Reserved	PCRx

- **Register Function**

[bit31:16] Reserved: Register bits

"0x0000" is read out from these bits.
When writing these bits, set them to "0x0000".

[bit15:0] PCRx: Pull-up Setting Register x

Sets pull-up of a pin

bit15:0		Description
Reading		Can read out the setting value of the register.
Writing	0	Disconnects the pull-up resistor of a pin.
	1	When a pin is in input status (for both GPIO and peripheral functions), the pull-up resistor is connected. When a pin is in output status, the pull-up resistor is disconnected.

Notes:

- The "x" of PCRx is a wildcard. PCRx indicates PCR0, PCR1, PCR2, etc.
- The "x" of Px0 and PxF is a wildcard. Px0 indicates P00, P10, P20, etc. PxF indicates P0F, P1F, P2F, etc.
- One register allows setting 16 pull-ups from PxF to Px0.
- Each bit in the register sets each pin individually. There is a one-to-one correspondence between bit assignment and the order of pins. For example, the 15th bit of PCR0 sets P0F, the 14th bit of PCR0 sets P0E, and the 0th bit of PCR0 sets P00.
- As a JTAG pin is selected for P00 to P04, the initial value is "1".
- The initial value of PCR0 to PCR6 and PCRE register are set to "1".
- When using I^2C function, use external pull-up by setting PCRx=0.
- PCR7 to PCRD and PCRF are not available.
- For a pin which is not available in this product, writing a value to the bit is invalid, and the read value is undefined.
- PE0, PE1 ports do not have a pull-up resistor. Because of this, writing a value to PE register is invalid. An initial value or a write value is read in this register.
- PCRx register is not initialized by deep standby transition reset.

3.4.3 Port input/output Direction Setting Register (DDRx)

The DDRx register sets input/output direction of a pin.

- **List of DDR Register Configuration**

bit 31 to 16	bit 15 to 0	Initial value	Attribute	Corresponding port
Reserved	DDR0	0x0000	R/W	P0F to P00
Reserved	DDR1	0x0000	R/W	P1F to P10
Reserved	DDR2	0x0000	R/W	P2F to P20
Reserved	DDR3	0x0000	R/W	P3F to P30
Reserved	DDR4	0x0000	R/W	P4F to P40
Reserved	DDR5	0x0000	R/W	P5F to P50
Reserved	DDR6	0x0000	R/W	P6F to P60
Reserved	-	-	-	-
Reserved	-	-	-	-
Reserved	-	-	-	-
Reserved	-	-	-	-
Reserved	-	-	-	-
Reserved	-	-	-	-
Reserved	-	-	-	-
Reserved	DDRE	0x0000	R/W	PEF to PE0
Reserved	-	-	-	-

- **Detailed Register Configuration**

Bit	31 to 16	15 to 0
Field	Reserved	DDRx

- **Register Function**

[bit31:16] Reserved: Reserved bits

"0x0000" is read out from these bits.
When writing these bits, set them to "0x0000".

[bit15:0] DDRx: Port input/output Direction Setting Register x

Sets input/output direction of a pin.

bit15:0		Description
Reading		Can read out the setting value of the register.
Writing	0	Uses GPIO in input direction. If a pin is selected as an input/output pin of peripheral functions, this setting value is invalid.
	1	Uses GPIO in output direction. If a pin is selected as an input/output pin of peripheral functions, this setting value is invalid.

Notes:

- The "x" of DDRx is a wildcard. DDRx indicates DDR0, DDR1, DDR2, etc.
- The "x" of Px0 and PxF is a wildcard. Px0 indicates P00, P10, P20, etc. PxF indicates P0F, P1F, P2F, etc.
- One register allows setting the input/output direction of 16 ports from PxF to Px0.
- Each bit in the register sets each pin individually. There is a one-to-one correspondence between bit assignment and the order of pins. For example, the 15th bit of DDR0 sets P0F, the 14th bit of DDR0 sets P0E, and the 0th bit of DDR0 sets P00.
- DDR7 to DDRD and DDRF are not available.
- For a pin which is not available in this product, writing a value to the bit is invalid, and the read value is undefined.
- DDRx register is not initialized by deep standby transition reset.

3.4.4 Port Input Data Register (PDIRx)

The PDIRx register indicates input data of a pin.

- **List of PDIR Register Configuration**

Bit 31 to 16	Bit 15 to 0	Initial value	Attribute	Corresponding port
Reserved	PDIR0	0x0000	R	P0F to P00
Reserved	PDIR1	0x0000	R	P1F to P10
Reserved	PDIR2	0x0000	R	P2F to P20
Reserved	PDIR3	0x0000	R	P3F to P30
Reserved	PDIR4	0x0000	R	P4F to P40
Reserved	PDIR5	0x0000	R	P5F to P50
Reserved	PDIR6	0x0000	R	P6F to P60
Reserved	-	-	-	-
Reserved	-	-	-	-
Reserved	-	-	-	-
Reserved	-	-	-	-
Reserved	-	-	-	-
Reserved	-	-	-	-
Reserved	-	-	-	-
Reserved	PDIRE	0x0000	R	PEF to PE0
Reserved	-	-	-	-

- **Detailed Register Configuration**

Bit	31 to 16	15 to 0
Field	Reserved	PDIRx

- **Register Function**

[bit31:16] Reserved: Reserved bits

"0x0000" is read out from these bits.
When writing these bits, set them to "0x0000".

[bit15:0] PDIRx: Port Input Data Register x

Reads out input data of a pin.

bit15:0		Description
Reading	0	Regardless of pin function settings (PFR/EPFR/DDR/PDOR), it indicates that a pin is in the status of "L" level input or "L" level output. When a special pin is selected by ADE/SPSR, as input is cut off, 0 is always read out.
	1	Regardless of pin function settings (PFR/EPFR/DDR/PDOR), it indicates that a pin is in the status of "H" level input or "H" level output.
Writing		Writing does not affect anything.

Notes:

- The "x" of PDIRx is a wildcard. PDIRx indicates PDIR0, PDIR1, PDIR2, etc.
- The "x" of Px0 and PxF is a wildcard. Px0 indicates P00, P10, P20, etc. PxF indicates P0F, P1F, P2F, etc.
- One register allows reading input data of 16 ports from PxF to Px0.
- Each bit in the register indicates the status of each pin individually. There is a one-to-one correspondence between bit assignment and the order of pins. For example, the 15th bit of PDIR0 indicates P0F, the 14th bit of PDIR0 indicates P0E, and the 0th bit of PDIR0 indicates P00.
- PDIR7 to PDIRD and PDIRF are not available.
- "0" is always read for a bit value of the pin which is not available in this product.
- PDIRx register is not initialized by deep standby transition reset.

3.4.5 Port Output Data Register x (PDORx)

The PDORx register sets output data to a pin.

- **List of PDOR Register Configuration**

bit 31	16	bit 15	0	Initial value	Attribute	Corresponding port
Reserved		PDOR0		0x0000	R/W	P0F to P00
Reserved		PDOR1		0x0000	R/W	P1F to P10
Reserved		PDOR2		0x0000	R/W	P2F to P20
Reserved		PDOR3		0x0000	R/W	P3F to P30
Reserved		PDOR4		0x0000	R/W	P4F to P40
Reserved		PDOR5		0x0000	R/W	P5F to P50
Reserved		PDOR6		0x0000	R/W	P6F to P60
Reserved		-		-	-	-
Reserved		-		-	-	-
Reserved		-		-	-	-
Reserved		-		-	-	-
Reserved		-		-	-	-
Reserved		-		-	-	-
Reserved		-		-	-	-
Reserved		PDORE		0x0000	R/W	PEF to PE0
Reserved		-		-	-	-

- **Detailed Register Configuration**

Bit	31	16	15	0
Field	Reserved		PDORx	

- **Register Function**

[bit31:16] Reserved: Reserved bits

"0x0000" is read out from these bits.
When writing these bits, set them to "0x0000".

[bit15:0] PDORx: Port Output Data Register x

Sets output data of a pin.

bit15:0		Description
Reading		Reads out the register value.
Writing	0	Outputs "L" level to GPIO. If a pin is selected as I/O input or peripheral functions input/output, a setting value is invalid.
	1	Outputs "H" level to GPIO. If a pin is selected as I/O input or peripheral functions input/output, a setting value is invalid.

Notes:

- The "x" of PDORx is a wildcard. PDORx indicates PDOR0, PDOR1, PDOR2, etc.
- The "x" of Px0 and PxF is a wildcard. Px0 indicates P00, P10, P20, etc. PxF indicates P0F, P1F, P2F, etc.
- One register allows setting output data of 16 ports from PxF to Px0.
- Each bit in the register sets each pin individually. There is a one-to-one correspondence between bit assignment and the order of pins. For example, the 15th bit of PDOR0 sets P0F, the 14th bit of PDOR0 sets P0E, and the 0th bit of PDOR0 sets P00.
- PDOR7 to PDORD and PDORF are not available.
- For a pin which is not available in this product, writing a value to the bit is invalid, and the read value is undefined.
- PDORx register is not initialized by deep standby transition reset.

3.4.6 Analog Input Setting Register (ADE)

The ADE register sets an external pin as an analog signal input pin of ADC and PGA.

- **Register Configuration**

Bit	31	0
Field	ADE	
Attribute	R/W	
Initial value	0xXXXXXXFF	

- **Register Function**

[bit31:0] ADE: Analog Input Setting Register

Sets as an analog signal input pin.

bit31:0		Description
Reading		Reads out the register value.
Writing	0	Uses an external pin not as analog input but digital input/output.
	1	Uses an external pin as analog input. (An I/O cell will be in a state of input direction, input cut-off, and pull-up disconnection.)

Notes:

- This register sets analog input pins from AN07 to AN00.
- Each bit in the register sets each pin individually. There is a one-to-one correspondence between bit assignment and the order of pins. For example, the 7th bit of ADE sets AN07, the 6th bit of ADE sets AN06, and the 0th bit of ADE sets AN00. With this product, setup of the analog input pin of AN07 to AN00 can be performed. For detail, refer to the "Data Sheet" of the this products.
- AN06 and AN07 are connected to the input of PGA.
- For a pin which is not available in this product, writing a value to the bit is invalid, and the read value is undefined.
- This register is not initialized by deep standby transition reset.

3.4.7 Extended Pin Function Setting Register x (EPFRx)

The EPFRx register assigns functions to a pin if there is more than one function.. EPFR01 to EPFR03 and EPFR10 to EPFR15 do not exist in products.

- **List of EPFRx Register Configuration**

bit 31 to 0	Initial value	Attribute	Corresponding function
EPFR00	0x00030000	R/W	System function
EPFR01	0x00000000	R/W	-
EPFR02	0x00000000	R/W	
EPFR03	0x00000000	R/W	
EPFR04	0x00000000	R/W	Base timer
EPFR05	0x00000000	R/W	
EPFR06	0x00000000	R/W	External interrupt
EPFR07	0x00000000	R/W	Multi-function serial
EPFR08	0x00000000	R/W	
EPFR09	0x00000000	R/W	ADC trigger
EPFR10	0x00000000	R/W	-
EPFR11	0x00000000	R/W	
EPFR12	0x00000000	R/W	
EPFR13	0x00000000	R/W	
EPFR14	0x00000000	R/W	
EPFR15	0x00000000	R/W	

Notes:

- For product, the registers of EPFR01 to EPFR03 and EPFR10 to EPFR15 do not exist.
- EPFRx register is not initialized by deep standby transition reset.

3.4.8 Extended Pin Function Setting Register 00 (EPFR00)

The EPFR00 register assigns functions to a pin if there is more than one function.

■ **Register Configuration**

Bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	-							
Initial value	-							

Bit	23	22	21	20	19	18	17	16
Field	Reserved						JTAGEN1S	JTAGEN0B
Attribute	-						R/W	R/W
Initial value							1	1

Bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	-							
Initial value	-							

Bit	7	6	5	4	3	2	1	0
Field	SUBOUTE		RTCCOE		Reserved	CROUTE		NMIS
Attribute	R/W		R/W		-	R/W		R/W
Initial value	00		00			00		0

■ **Register Function**

[bit31:18] Reserved: Reserved bits

"0b00000000000000" is read out from these bits.
When writing these bits, set them to "0b00000000000000".

[bit17] JTAGEN1S: JTAG Function Select bit 1

Selects a function for TRSTX and TDI pins.

Bit		Description
Reading		Reads out the register value.
Writing	0	Does not use two pins of TRSTX and TDI. (A shared pin is available.)
	1	Uses two pins of TRSTX and TDI. [Initial value]

[bit16] JTAGEN0B: JTAG Function Select bit 0

Selects a function for TCK, TMS, and TDO pins.

Bit		Description
Reading		Reads out the register value.
Writing	0	Does not use three pins of TCK, TMS, and TDO. (A shared pin is available.)
	1	Uses three pins of TCK, TMS, and TDO. [Initial value]

[bit15:8] Reserved: Reserved bits

"0b00000000" is read out from these bits.
When writing these bits, set them to "0b00000000".

[bit7:6] SUBOUTE: Sub clock divide output function select bit

Selects sub clock divide output.

bit7:6		Description
Reading		Reads out the register value.
Writing	0 0	Sub clock divide output is not executed. [initial value]
	0 1	SUBOUT_0 is used as the sub clock divide output pin.
	1 0	SUBOUT_1 is used as the sub clock divide output pin.
	1 1	SUBOUT_2 is used as the sub clock divide output pin.

[bit5:4] RTCCOE: RTC clock output select bit

Selects a RTC clock output.

bit5:4		Description
Reading		Reads out the register value.
Writing	0 0	RTC clock output is not executed. [initial value]
	0 1	RTCCO_0 is used as the RTC clock output pin.
	1 0	RTCCO_1 is used as the RTC clock output pin.
	1 1	RTCCO_2 is used as the RTC clock output pin.

[bit3] Reserved: Reserved bit

"0" is read out from this bit.
When writing this bit, set it to "0".

[bit2:1] CROUTE: Internal high-speed CR Oscillation Output Function Select bit

Selects internal high-speed CR oscillation output.

bit2:1		Description
Reading		Reads out the register value.
Writing	00	Does not produce internal high-speed CR oscillation output. [Initial value]
	01	Uses CROUT_0 at the internal high-speed CR oscillation output pin.
	10	Uses CROUT_1 at the internal high-speed CR oscillation output pin.
	11	Setting is prohibited.

[bit0] NMIS: NMIX Function Select bit

Selects a function for the NMIX pin.

Bit		Description
Reading		Reads out the register value.
Writing	0	Does not use the NMIX pin. [Initial value]
	1	Uses the NMIX pin.

Note

This register is not initialized by deep standby transition reset.

3.4.9 Extended Pin Function Setting Register 04 (EPFR04)

The EPFR04 register assigns functions to pins of ch.0, ch.1, ch.2, and ch.3 of the base timer.

■ **Register Configuration**

Bit	31	30	29	28	27	26	25	24
Field	Reserved		TIOB3S		TIOA3E		TIOA3S	
Attribute	-		R/W		R/W		R/W	
Initial value	-		00		00		00	

Bit	23	22	21	20	19	18	17	16
Field	Reserved		TIOB2S		TIOA2E		Reserved	
Attribute	-		R/W		R/W		-	
Initial value	-		00		00		-	

Bit	15	14	13	12	11	10	9	8
Field	Reserved		TIOB1S		TIOA1E		TIOA1S	
Attribute	-		R/W		R/W		R/W	
Initial value	-		00		00		00	

Bit	7	6	5	4	3	2	1	0
Field	Reserved	TIOB0S			TIOA0E		Reserved	
Attribute	-	R/W			R/W		-	
Initial value	-	000			00		-	

■ **Register Function**

[bit31:30] Reserved: Reserved bits

"0b00" is read out from these bits.
When writing these bits, set them to "0b00".

[bit29:28] TIOB3S: TIOB3 Input Select bits

Selects input for TIOB3.

bit29:28		Description
Reading		Reads out the register value.
Writing	00	Does not produce input for BT ch.3 TIOB. [Initial value]
	01	Setting is prohibited.
	10	Uses TIOB3_1 at the input pin of BT ch.3 TIOB.
	11	Uses TIOB3_2 at the input pin of BT ch.3 TIOB.

[bit27:26] TIOA3E: TIOA3 Output Select bits

Selects output for TIOA3.

bit27:26		Description
Reading		Reads out the register value.
Writing	0 0	Does not produce output for BT ch.3 TIOA. [Initial value]
	0 1	Setting is prohibited.
	1 0	Uses TIOA3_1 at the output pin of BT ch.3 TIOA.
	1 1	Uses TIOA3_2 at the output pin of BT ch.3 TIOA.

[bit25:24] TIOA3S: TIOA3 Input Select bits

Selects input for TIOA3.

bit25:24		Description
Reading		Reads out the register value.
Writing	0 0	Does not produce input for BT ch.3 TIOA. [Initial value]
	0 1	Setting is prohibited.
	1 0	Uses TIOA3_1 at the input pin of BT ch.3 TIOA.
	1 1	Uses TIOA3_2 at the input pin of BT ch.3 TIOA.

[bit23:22] Reserved: Reserved bits

"0b00" is read out from these bits.
When writing these bits, set them to "0b00".

[bit21:20] TIOB2S: TIOB2 Input Select bits

Selects input for TIOB2.

bit21:20		Description
Reading		Reads out the register value.
Writing	0 0	Uses TIOB2_0 at the input pin of BT ch.2 TIOB. [Initial value]
	0 1	Same as Writing 00.
	1 0	Uses TIOB2_1 at the input pin of BT ch.2 TIOB.
	1 1	Uses TIOB2_2 at the input pin of BT ch.2 TIOB.

[bit19:18] TIOA2E: TIOA2 Output Select bits

Selects output for TIOA2.

bit19:18		Description
Reading		Reads out the register value.
Writing	0 0	Does not produce output for BT ch.2 TIOA. [Initial value]
	0 1	Setting is prohibited.
	1 0	Uses TIOA2_1 at the output pin of BT ch.2 TIOA.
	1 1	Uses TIOA2_2 at the output pin of BT ch.2 TIOA.

[bit17:14] Reserved: Reserved bits

"0b0000" is read out from these bits.
When writing these bits, set them to "0b0000".

[bit13:12] TIOB1S: TIOB1 Input Select bits

Selects input for TIOB1.

bit13:12		Description
Reading		Reads out the register value.
Writing	0 0	Does not produce input for BT ch.1 TIOB. [Initial value]
	0 1	Setting is prohibited.
	1 0	Uses TIOB1_1 at the input pin of BT ch.1 TIOB.
	1 1	Setting is prohibited.

[bit11:10] TIOA1E: TIOA1 Output Select bits

Selects output for TIOA1.

bit11:10		Description
Reading		Reads out the register value.
Writing	00	Does not produce output for BT ch.1 TIOA. [Initial value]
	01	Setting is prohibited.
	10	Uses TIOA1_1 at the output pin of BT ch.1 TIOA.
	11	Setting is prohibited.

[bit9:8] TIOA1S: TIOA1 Input Select bits

Selects input for TIOA1.

bit9:8		Description
Reading		Reads out the register value.
Writing	0 0	Does not produce input for BT ch.1 TIOA. [Initial value]
	0 1	Setting is prohibited.
	1 0	Uses TIOA1_1 at the input pin of BT ch.1 TIOA.
	1 1	Setting is prohibited.

[bit7] Reserved: Reserved bit

"0" is read out from this bit.
When writing this bit, set it to "0".

[bit6:4] TIOB0S: TIOB0 Input Select bits

Selects input for TIOB0.

bit6:4		Description
Reading		Reads out the register value.
Writing	000	Uses TIOB0_0 at the input pin of BT ch.0 TIOB. [Initial value]
	001	Same as Writing 000.
	010	Uses TIOB0_1 at the input pin of BT ch.0 TIOB.
	011	Uses TIOB0_2 at the input pin of BT ch.0 TIOB.
	100	Setting is prohibited.
	101	Setting is prohibited.
	110	Setting is prohibited.
	111	Uses at the pin for measuring trimming of the high-speed CR frequency division clock.

[bit3:2] TIOA0E: TIOA0 Output Select bits

Selects output for TIOA0.

bit3:2		Description
Reading		Reads out the register value.
Writing	0 0	Produces output for BT ch.0 TIOA. [Initial value]
	0 1	Setting is prohibited.
	1 0	Uses TIOA0_1 at the output pin of BT ch.0 TIOA.
	1 1	Uses TIOA0_2 at the output pin of BT ch.0 TIOA.

[bit1:0] Reserved: Reserved bits

"0b00" is read out from these bits.
When writing these bits, set them to "0b00".

Notes:

- TIOA
  Even channels are for output only.
  Odd channels are for both input and output.
- TIOB
  Input only.
- TIOA1, TIOA3 (odd number of "A") are not bidirectional pins so that choose either input pin or output pin for them.
  When output is chosen for odd TIOA channel, input setting will be ignored.

Example1 : Use TIOA1 as an output pin:
When TIOA1 is output to TIOA1_0, select EPFR04:TIOA1E = 00 or 01.(With this product, setting is prohibited.)
When TIOA1 is output to TIOA1_1, select EPFR04:TIOA1E = 10.
When TIOA1 is output to TIOA1_2, select EPFR04:TIOA1E = 11. (With this product, setting is prohibited.)
Settings for EPFR04:TIOA1S will be ignored.
Select ADE=0, PFR=1 for selected pins (DDR will be ignored).
All the output of other peripheral function pins which are also used by selected pins must be OFF.

Example2 : When TIOA1 is used as an input pin:
Select EPFR04:TIOA1E = 00.
When TIOA1 is input from TIOA1_0, select EPFR04:TIOA1S = 00 or 01.(With this product, setting is prohibited.)
When TIOA1 is input from TIOA1_1, select EPFR04:TIOA1S = 10.
When TIOA1 is input from TIOA1_2, select EPFR04:TIOA1S = 11. (With this product, setting is prohibited.)
Select ADE=0, PFR=1 for selected pins (DDR will be ignored).
All the output of other peripheral function pins which are also used by selected pins must be OFF.

* When a pin is set to input, the output of the pin which is also used by selected pins (GPIO, other peripheral function pins) can be input to the base timer as Feedback with a setting not described above.

This register is not initialized by deep standby transition reset.

3.4.10 Extended Pin Function Setting Register 05 (EPFR05)

The EPFR05 register assigns functions to pins of ch.4, ch.5, ch.6, and ch.7 of the base timer.

■ **Register Configuration**

bit	31	30	29	28	27	26	25	24
Field	Reserved		TIOB7S		TIOA7E		TIOA7S	
Attribute	-		R/W		R/W		R/W	
Initial value	-		00		00		00	

bit	23	22	21	20	19	18	17	16
Field	Reserved		TIOB6S		TIOA6E		Reserved	
Attribute	-		R/W		R/W		-	
Initial value	-		00		00		-	

bit	15	14	13	12	11	10	9	8
Field	Reserved		TIOB5S		TIOA5E		TIOA5S	
Attribute	-		R/W		R/W		R/W	
Initial value	-		00		00		00	

bit	7	6	5	4	3	2	1	0
Field	Reserved		TIOB4S		TIOA4E		Reserved	
Attribute	-		R/W		R/W		-	
Initial value	-		00		00		-	

■ **Register Function**

[bit31:30] Reserved: Reserved bits

"0b00" is read out from these bits.
When writing these bits, set them to "0b00".

[bit29:28] TIOB7S: TIOB7 Input Select bits

Selects input for TIOB7.

bit29:28		Description
Reading		Reads out the register value.
Writing	0 0	Does not produce the input of BT ch.7 TIOB. [Initial value]
	0 1	Setting is prohibited.
	1 0	Uses TIOB7_1 at the input pin of BT ch.7 TIOB.
	1 1	Setting is prohibited.

[bit27:26] TIOA7E: TIOA7 Output Select bits

Selects output for TIOA7.

bit27:26		Description
Reading		Reads out the register value.
Writing	0 0	Does not produce the output of BT ch.7 TIOA. [Initial value]
	0 1	Setting is prohibited.
	1 0	Uses TIOA7_1 at the output pin of BT ch.7 TIOA.
	1 1	Setting is prohibited.

[bit25:24] TIOA7S: TIOA7 Input Select bits

Selects input for TIOA7.

bit25:24		Description
Reading		Reads out the register value.
Writing	00	Does not produce the input of BT ch.7 TIOA. [Initial value]
	01	Setting is prohibited.
	10	Uses TIOA7_1 at the input pin of BT ch.7 TIOA.
	11	Setting is prohibited.

[bit23:22] Reserved: Reserved bits

"0b00" is read out from these bits.
When writing these bits, set them to "0b00".

[bit21:20] TIOB6S: TIOB6 Input Select bits

Selects input for TIOB6.

bit21:20		Description
Reading		Reads out the register value.
Writing	00	Does not produce the input of BT ch.6 TIOB. [Initial value]
	01	Setting is prohibited.
	10	Uses TIOB6_1 at the input pin of BT ch.6 TIOB.
	11	Setting is prohibited.

[bit19:18] TIOA6E: TIOA6 Output Select bits

Selects output for TIOA6.

bit19:18		Description
Reading		Reads out the register value.
Writing	00	Does not produce the output of BT ch.6 TIOA. [Initial value]
	01	Setting is prohibited.
	10	Uses TIOA6_1 at the output pin of BT ch.6 TIOA.
	11	Setting is prohibited.

[bit17:14] Reserved: Reserved bits

"0b0000" is read out from these bits.
When writing these bits, set them to "0b0000".

[bit13:12] TIOB5S: TIOB5 Input Select bits

Selects input for TIOB5.

bit13:12		Description
Reading		Reads out the register value.
Writing	0 0	Does not produce the input of BT ch.5 TIOB. [Initial value]
	0 1	Uses TIOB5_0 at the input pin of BT ch.5 TIOB.
	1 0	Setting is prohibited.
	1 1	Uses TIOB5_2 at the input pin of BT ch.5 TIOB.

[bit11:10] TIOA5E: TIOA5 Output Select bits

Selects output for TIOA5.

bit11:10		Description
Reading		Reads out the register value.
Writing	0 0	Does not produce the output of BT ch.5 TIOA. [Initial value]
	0 1	Setting is prohibited.
	1 0	Uses TIOA5_1 at the output pin of BT ch.5 TIOA.
	1 1	Uses TIOA5_2 at the output pin of BT ch.5 TIOA.

[bit9:8] TIOA5S: TIOA5 Input Select bits

Selects input for TIOA5.

bit9:8		Description
Reading		Reads out the register value.
Writing	00	Does not produce the input of BT ch.5 TIOA. [Initial value]
	01	Setting is prohibited.
	10	Uses TIOA5_1 at the input pin of BT ch.5 TIOA.
	11	Uses TIOA5_2 at the input pin of BT ch.5 TIOA.

[bit7:6] Reserved: Reserved bits

"0b00" is read out from these bits.
When writing these bits, set them to "0b00".

[bit5:4] TIOB4S: TIOB4 Input Select bits

Selects input for TIOB4.

bit5:4		Description
Reading		Reads out the register value.
Writing	0 0	Does not produce the input of BT ch.4 TIOB. [Initial value]
	0 1	Uses TIOB4_0 at the input pin of BT ch.4 TIOB.
	1 0	Uses TIOB4_1 at the input pin of BT ch.4 TIOB.
	1 1	Setting is prohibited.

[bit3:2] TIOA4E: TIOA4 Output Select bits

Selects output for TIOA4.

bit3:2		Description
Reading		Reads out the register value.
Writing	0 0	Does not produce the output of BT ch.4 TIOA. [Initial value]
	0 1	Setting is prohibited.
	1 0	Uses TIOA4_1 at the output pin of BT ch.4 TIOA.
	1 1	Setting is prohibited.

[bit1:0] Reserved: Reserved bits

"0b00" is read out from these bits.
When writing these bits, set them to "0b00".

Notes:

- TIOA
  Even channels are for output only.
  Odd channels are for both input and output.
- TIOB
  Input only.
- TIOA5, TIOA7 (odd number of "A") are not bidirectional pins so that choose either input pin or output pin for them.
  When output is chosen for odd TIOA channel, input setting will be ignored.

  Example1 : Use TIOA5 as an output pin:
  When TIOA5 is output to TIOA5_0, select EPFR05:TIOA5E = 01. (With this product, setting is prohibited.)
  When TIOA5 is output to TIOA5_1, select EPFR05:TIOA5E = 10.
  When TIOA5 is output to TIOA5_2, select EPFR05:TIOA5E = 11.
  Settings for EPFR05:TIOA5S will be ignored.
  Select ADE=0, PFR=1 for selected pins (DDR will be ignored).
  All the output of other peripheral function pins which are also used by selected pins must be OFF.

  Example2 : When TIOA5 is used as an input pin:
  Select EPFR05:TIOA5E = 00.
  When TIOA5 is input from TIOA5_0, select EPFR05:TIOA5S = 00 or 01. (With this product, setting is prohibited.)
  When TIOA5 is input from TIOA5_1, select EPFR05:TIOA5S = 10.
  When TIOA5 is input from TIOA5_2, select EPFR05:TIOA5S = 11.
  Select ADE=0, PFR=1 for selected pins (DDR will be ignored).
  All the output of other peripheral function pins which are also used by selected pins must be OFF.

  * When a pin is set to input, the output of the pin which is also used by selected pins (GPIO, other peripheral function pins) can be input to the base timer as Feedback with a setting not described above.

  This register is not initialized by deep standby transition reset.

3.4.11 Extended Pin Function Setting Register 06 (EPFR06)

The EPFR06 register assigns functions to external interrupt pins.

■ **Register Configuration**

Bit	31	30	29	28	27	26	25	24
Field	EINT15S		Reserved		Reserved		Reserved	
Attribute	R/W		-		-		-	
Initial value	00		-		-		-	

Bit	23	22	21	20	19	18	17	16
Field	Reserved		Reserved		Reserved		EINT08S	
Attribute	-		-		-		R/W	
Initial value	-		-		-		00	

bit	15	14	13	12	11	10	9	8
Field	Reserved		EINT06S		EINT05S		EINT04S	
Attribute	-		R/W		R/W		R/W	
Initial value	-		00		00		00	

Bit	7	6	5	4	3	2	1	0
Field	EINT03S		EINT02S		EINT01S		EINT00S	
Attribute	R/W		R/W		R/W		R/W	
Initial value	00		00		00		00	

Register Function

[bit31:30] EINT15S: External Interrupt Input Select bits

Selects input for EINT15.

bit31:30		Description
Reading		Reads out the register value.
Writing	00	Does not produce the input of EINT ch.15. [Initial value]
	01	Setting is prohibited.
	10	Uses INT15_1 at the input pin of EINT ch.15.
	11	Setting is prohibited.

[bit29:18] Reserved : Reserved bits

"0x000" is read out from these bits.
When writing these bits, set them to "0x000".

[bit17:16] EINT08S: External Interrupt Input Select bits

Selects input for EINT08.

bit17:16		Description
Reading		Reads out the register value.
Writing	00	Does not produce the input of EINT ch.8. [Initial value]
	01	Setting is prohibited.
	10	Setting is prohibited.
	11	Uses INT08_2 at the input pin of EINT ch.8.

[bit15:14] Reserved : Reserved bits

"0b00" is read out from these bits.
When writing these bits, set them to "0b00".

[bit13:12] EINT06S: External Interrupt Input Select bits

Selects input for EINT06.

bit13:12		Description
Reading		Reads out the register value.
Writing	0 0	Does not produce the input of EINT ch.6. [Initial value]
	0 1	Setting is prohibited.
	1 0	Uses INT06_1 at the input pin of EINT ch.6.
	1 1	Setting is prohibited.

[bit11:10] EINT05S: External Interrupt Input Select bits

Selects input for EINT05.

bit11:10		Description
Reading		Reads out the register value.
Writing	00	Uses INT05_0 at the input pin of EINT ch.5. [Initial value]
	01	Same as Writing 00.
	10	Uses INT05_1 at the input pin of EINT ch.5.
	11	Uses INT05_2 at the input pin of EINT ch.5.

[bit9:8] EINT04S: External Interrupt Input Select bits

Selects input for EINT04.

bit9:8		Description
Reading		Reads out the register value.
Writing	0 0	Uses INT04_0 at the input pin of EINT ch.4. [Initial value]
	0 1	Same as Writing 00.
	1 0	Uses INT04_1 at the input pin of EINT ch.4.
	1 1	Uses INT04_2 at the input pin of EINT ch.4.

[bit7:6] EINT03S: External Interrupt Input Select bits

Selects input for EINT03.

bit7:6		Description
Reading		Reads out the register value.
Writing	0 0	Uses INT03_0 at the input pin of EINT ch.3. [Initial value]
	0 1	Same as Writing 00.
	1 0	Uses INT03_1 at the input pin of EINT ch.3.
	1 1	Uses INT03_2 at the input pin of EINT ch.3.

[bit5:4] EINT02S: External Interrupt Input Select bits

Selects input for EINT02.

bit5:4		Description
Reading		Reads out the register value.
Writing	0 0	Uses INT02_0 at the input pin of EINT ch.2. [Initial value]
	0 1	Same as Writing 00.
	1 0	Uses INT02_1 at the input pin of EINT ch.2.
	1 1	Setting is prohibited.

[bit3:2] EINT01S: External Interrupt Input Select bits

Selects input for EINT01.

bit3:2		Description
Reading		Reads out the register value.
Writing	00	Uses INT01_0 at the input pin of EINT ch.1. [Initial value]
	01	Same as Writing 00.
	10	Uses INT01_1 at the input pin of EINT ch.1.
	11	Setting is prohibited.

[bit1:0] EINT00S: External Interrupt Input Select bits

Selects input for EINT00.

bit1:0		Description
Reading		Reads out the register value.
Writing	0 0	Uses INT00_0 at the input pin of EINT ch.0. [Initial value]
	0 1	Same as Writing 00.
	1 0	Uses INT00_1 at the input pin of EINT ch.0.
	1 1	Uses INT00_2 at the input pin of EINT ch.0.

Note

- This register is not initialized by deep standby transition reset.

3.4.12 Extended Pin Function Setting Register 07 (EPFR07)

The EPFR07 register assigns functions of multi-function serial ch.0 to ch.5.

■ **Register Configuration**

bit	31	30	29	28	27	26	25	24
Field	Reserved	SCSI5	SCSI4	SCSI0	SCK3B		SOT3B	
Attribute	-	R/W	R/W	R/W	R/W		R/W	
Initial value	-	0	0	0	00		00	

bit	23	22	21	20	19	18	17	16
Field	SIN3S		SCK2B		SOT2B		SIN2S	
Attribute	R/W		R/W		R/W		R/W	
Initial value	00		00		00		00	

bit	15	14	13	12	11	10	9	8
Field	SCK1B		SOT1B		SIN1S		SCK0B	
Attribute	R/W		R/W		R/W		R/W	
Initial value	00		00		00		00	

bit	7	6	5	4	3	2	1	0
Field	SOT0B		SIN0S		Reserved			
Attribute	R/W		R/W		-			
Initial value	00		00		-			

■ **Register Function**

[bit31] Reserved: Reserved bits

"0b0" is read from these bits.
When writing these bits, set them to "0b0".

[bit30] SCSI5 :SCSI5 Function Select bit

Selects a function for the MFS ch.5.

bit		Description
Reading		Reads out the register value.
Writing	0	The input pin of MFS ch.5 SCSI is made "0" fixation. [Initial value]
	1	SCSI5_0 is used for the input pin of MFS ch.5 SCSI.

[bit29] SCSI4 :SCSI4 Function Select bit

Selects a function for the MFS ch.4.

bit		Description
Reading		Reads out the register value.
Writing	0	The input pin of MFS ch.4 SCSI is made "0" fixation. [Initial value]
	1	SCSI4_2 is used for the input pin of MFS ch.4 SCSI.

[bit28] SCSI0 :SCSI0 Function Select bit

Selects a function for the MFS ch.0.

bit		Description
Reading		Reads out the register value.
Writing	0	The input pin of MFS ch.0 SCSI is made "0" fixation. [Initial value]
	1	SCSI0_0 is used for the input pin of MFS ch.0 SCSI.

[bit27:26] SCK3B: SCK3 Input/Output Select bits

Selects input/output for SCK3.

bit27:26		Description
Reading		Reads out the register value.
Writing	0 0	Uses SCK3_0 at the input pin of MFS ch.3 SCK. Does not produce output. [Initial value]
	0 1	Uses SCK3_0 at the input pin of MFS ch.3 SCK. Uses SCK3_0 at the output pin.
	1 0	Uses SCK3_1 at the input pin of MFS ch.3 SCK. Uses SCK3_1 at the output pin.
	1 1	Setting is prohibited.

[bit25:24] SOT3B: SOT3 Input/Output Select bits

Selects input/output for SOT3.

bit25:24		Description
Reading		Reads out the register value.
Writing	00	Uses SOT3_0 at the input pin of MFS ch.3 SOT. Does not produce output. [Initial value]
	01	Uses SOT3_0 at the input pin of MFS ch.3 SOT. Uses SOT3_0 at the output pin.
	10	Uses SOT3_1 at the input pin of MFS ch.3 SOT. Uses SOT3_1 at the output pin.
	11	Setting is prohibited.

[bit23:22] SIN3S: SIN3 Input Select bits

Selects input for SIN3.

bit23:22		Description
Reading		Reads out the register value.
Writing	00	Uses SIN3_0 at the input pin of MFS ch.3 SIN. [Initial value]
	01	Same as Writing 00.
	10	Uses SIN3_1 at the input pin of MFS ch.3 SIN.
	11	Setting is prohibited.

[bit21:20] SCK2B: SCK2 Input/Output Select bits

Selects input/output for SCK2.

bit21:20		Description
Reading		Reads out the register value.
Writing	00	Does not produce the pin of MFS ch.2 SCK. [Initial value]
	01	Setting is prohibited.
	10	Setting is prohibited.
	11	Uses SCK2_2 at the input pin of MFS ch.2 SCK. Uses SCK2_2 at the output pin.

[bit19:18] SOT2B: SOT2 Input/Output Select bits

Selects input/output for SOT2.

bit19:18		Description
Reading		Reads out the register value.
Writing	00	Does not produce the pin of MFS ch.2 SOT. [Initial value]
	01	Setting is prohibited.
	10	Setting is prohibited.
	11	Uses SOT2_2 at the input pin of MFS ch.2 SOT. Uses SOT2_2 at the output pin.

[bit17:16] SIN2S: SIN2 Input Select bits

Selects input for SIN2.

bit17:16		Description
Reading		Reads out the register value.
Writing	00	Does not produce the input pin of MFS ch.2 SIN. [Initial value]
	01	Setting is prohibited.
	10	Setting is prohibited.
	11	Uses SIN2_2 at the input pin of MFS ch.2 SIN.

[bit15:14] SCK1B: SCK1 Input/Output Select bits

Selects input/output for SCK1.

bit15:14		Description
Reading		Reads out the register value.
Writing	00	Does not produce the pin of MFS ch.1 SCK. [Initial value]
	01	Setting is prohibited.
	10	Uses SCK1_1 at the input pin of MFS ch.1 SCK. Uses SCK1_1 at the output pin.
	11	Setting is prohibited.

[bit13:12] SOT1B: SOT1 Input/Output Select bits

Selects input/output for SOT1.

bit13:12		Description
Reading		Reads out the register value.
Writing	00	Does not produce the pin of MFS ch.1 SOT. [Initial value]
	01	Setting is prohibited.
	10	Uses SOT1_1 at the input pin of MFS ch.1 SOT. Uses SOT1_1 at the output pin.
	11	Setting is prohibited.

[bit11:10] SIN1S: SIN1 Input Select bits

Selects input for SIN1.

bit11:10		Description
Reading		Reads out the register value.
Writing	00	Does not produce the input pin of MFS ch.1 SIN. [Initial value]
	01	Setting is prohibited.
	10	Uses SIN1_1 at the input pin of MFS ch.1 SIN.
	11	Setting is prohibited.

[bit9:8] SCK0B: SCK0 Input/Output Select bits

Selects input/output for SCK0.

bit9:8		Description
Reading		Reads out the register value.
Writing	00	Uses SCK0_0 at the input pin of MFS ch.0 SCK. Does not produce output. [Initial value]
	01	Uses SCK0_0 at the input pin of MFS ch.0 SCK. Uses SCK0_0 at the output pin.
	10	Uses SCK0_1 at the input pin of MFS ch.0 SCK. Uses SCK0_1 at the output pin.
	11	Setting is prohibited.

[bit7:6] SOT0B: SOT0 Input/Output Select bits

Selects input/output for SOT0.

bit7:6		Description
Reading		Reads out the register value.
Writing	00	Uses SOT0_0 at the input pin of MFS ch.0 SOT. Does not produce output. [Initial value]
	01	Uses SOT0_0 at the input pin of MFS ch.0 SOT. Uses SOT0_0 at the output pin.
	10	Uses SOT0_1 at the input pin of MFS ch.0 SOT. Uses SOT0_1 at the output pin.
	11	Setting is prohibited.

[bit5:4] SIN0S: SIN0 Input Select bits

Selects input for SIN0.

bit5:4		Description
Reading		Reads out the register value.
Writing	00	Uses SIN0_0 at the input pin of MFS ch.0 SIN. [Initial value]
	01	Same as Writing 00.
	10	Uses SIN0_1 at the input pin of MFS ch.0 SIN.
	11	Setting is prohibited.

[bit3:0] Reserved: Reserved bits

"0b0000" is read from these bits.
When writing these bits, set them to "0b0000".

Note

- This register is not initialized by deep standby transition reset.

3.4.13 Extended Pin Function Setting Register 08 (EPFR08)

The EPFR08 register assigns functions of multi-function serial ch.0 and ch.4 to ch.6.

■ **Register Configuration**

bit	31	30	29	28	27	26	25	24
Field	Reserved	SCSO5	SCSO4	SCSO0	Reserved		Reserved	
Attribute	-	R/W	R/W	R/W	-		-	
Initial value	-	0	0	0	-		-	

bit	23	22	21	20	19	18	17	16
Field	Reserved		SCK6B		SOT6B		SIN6S	
Attribute	-		R/W		R/W		R/W	
Initial value	-		00		00		00	

bit	15	14	13	12	11	10	9	8
Field	SCK5B		SOT5B		SIN5S		SCK4B	
Attribute	R/W		R/W		R/W		R/W	
Initial value	00		00		00		00	

bit	7	6	5	4	3	2	1	0
Field	SOT4B		SIN4S		CTS4S		RTS4E	
Attribute	R/W		R/W		R/W		R/W	
Initial value	00		00		00		00	

■ **Register Function**

[bit31] Reserved: Reserved bits

"0b0" is read from these bits.
When writing these bits, set them to "0b0".

[bit30] SCSO5 :SCSO5 Function Select bit

Selects a function for the MFS ch.5.

bit		Description
Reading		Reads out the register value.
Writing	0	The input pin of MFS ch.5 SCSO is made "0" fixation. [Initial value]
	1	SCSO5_0 is used for the input pin of MFS ch.5 SCSO.

[bit29] SCSO4 :SCSO4 Function Select bit

Selects a function for the MFS ch.4.

bit		Description
Reading		Reads out the register value.
Writing	0	The input pin of MFS ch.4 SCSO is made "0" fixation. [Initial value]
	1	SCSO4_2 is used for the input pin of MFS ch.4 SCSO.

[bit28] SCSO0 :SCSO0 Function Select bit

Selects a function for the MFS ch.0.

bit		Description
Reading		Reads out the register value.
Writing	0	The input pin of MFS ch.0 SCSO is made "0" fixation. [Initial value]
	1	SCSIO0_0 is used for the input pin of MFS ch.0 SCSO.

[bit27:22] Reserved: Reserved bits

"0b000000" is read out from these bits.
When writing these bits, set them to "0b000000".

[bit21:20] SCK6B: SCK6 Input/Output Select bits

Selects input/output for SCK6.

bit21:20		Description
Reading		Reads out the register value.
Writing	0 0	Does not produce the pin of MFS ch.6 SCK. [Initial value]
	0 1	Setting is prohibited.
	1 0	Uses SCK6_1 at the input pin of MFS ch.6 SCK. Uses SCK6_1 at the output pin.
	1 1	Setting is prohibited.

[bit19:18] SOT6B: SOT6 Input/Output Select bits

Selects input/output for SOT6.

bit19:18		Description
Reading		Reads out the register value.
Writing	00	Does not produce the pin of MFS ch.6 SOT. [Initial value]
	01	Setting is prohibited.
	10	Uses SOT6_1 at the input pin of MFS ch.6 SOT. Uses SOT6_1 at the output pin.
	11	Setting is prohibited.

[bit17:16] SIN6S: SIN6 Input Select bits

Selects input for SIN6.

bit17:16		Description
Reading		Reads out the register value.
Writing	0 0	Does not produce the input pin of MFS ch.6 SIN. [Initial value]
	0 1	Setting is prohibited.
	1 0	Uses SIN6_1 at the input pin of MFS ch.6 SIN.
	1 1	Setting is prohibited.

[bit15:14] SCK5B: SCK5 Input/Output Select bits

Selects input/output for SCK5.

bit15:14		Description
Reading		Reads out the register value.
Writing	0 0	Uses SCK5_0 at the input pin of MFS ch.5 SCK. Does not produce output. [Initial value]
	0 1	Uses SCK5_0 at the input pin of MFS ch.5 SCK. Uses SCK5_0 at the output pin.
	1 0	Setting is prohibited.
	1 1	Setting is prohibited.

[bit13:12] SOT5B: SOT5 Input/Output Select bits

Selects input/output for SOT5.

bit13:12		Description
Reading		Reads out the register value.
Writing	00	Uses SOT5_0 at the input pin of MFS ch.5 SOT. Does not produce output. [Initial value]
	01	Uses SOT5_0 at the input pin of MFS ch.5 SOT. Uses SOT5_0 at the output pin.
	10	Setting is prohibited.
	11	Setting is prohibited.

[bit11:10] SIN5S: SIN5 Input Select bits

Selects input for SIN5.

bit11:10		Description
Reading		Reads out the register value.
Writing	0 0	Uses SIN5_0 at the input pin of MFS ch.5 SIN. [Initial value]
	0 1	Same as Writing 00.
	1 0	Setting is prohibited.
	1 1	Setting is prohibited.

[bit9:8] SCK4B: SCK4 Input/Output Select bits

Selects input/output for SCK4.

bit9:8		Description
Reading		Reads out the register value.
Writing	00	Uses SCK4_0 at the input pin of MFS ch.4 SCK. Does not produce output. [Initial value]
	01	Uses SCK4_0 at the input pin of MFS ch.4 SCK. Uses SCK4_0 at the output pin.
	10	Setting is prohibited.
	11	Uses SCK4_2 at the input pin of MFS ch.4 SCK. Uses SCK4_2 at the output pin.

[bit7:6] SOT4B: SOT4 Input/Output Select bits

Selects input/output for SOT4.

bit7:6		Description
Reading		Reads out the register value.
Writing	0 0	Uses SOT4_0 at the input pin of MFS ch.4 SOT. Does not produce output. [Initial value]
	0 1	Uses SOT4_0 at the input pin of MFS ch.4 SOT. Uses SOT4_0 at the output pin.
	1 0	Setting is prohibited.
	1 1	Uses SOT4_2 at the input pin of MFS ch.4 SOT. Uses SOT4_2 at the output pin.

[bit5:4] SIN4S: SIN4 Input Select bits

Selects input for SIN4.

bit5:4		Description
Reading		Reads out the register value.
Writing	00	Uses SIN4_0 at the input pin of MFS ch.4 SIN. [Initial value]
	01	Same as Writing 00.
	10	Setting is prohibited.
	11	Uses SIN4_2 at the input pin of MFS ch.4 SIN.

[bit3:2] CTS4S: CTS4 Input Select bits

Selects input for CTS4.

bit3:2		Description
Reading		Reads out the register value.
Writing	0 0	Uses CTS4_0 at the input pin of MFS ch.4 CTS. [Initial value]
	0 1	Same as Writing 00.
	1 0	Setting is prohibited.
	1 1	Uses CTS4_2 at the input pin of MFS ch.4 CTS.

[bit1:0] RTS4E: RTS4 Output Select bits

Selects output for RTS4.

bit1:0		Description
Reading		Reads out the register value.
Writing	00	Does not produce output for MFS ch.4 RTS. [Initial value]
	01	Uses RTS4_0 at the output pin of MFS ch.4 RTS.
	10	Setting is prohibited.
	11	Uses RTS4_2 at the output pin of MFS ch.4 RTS.

Note

This register is not initialized by deep standby transition reset.

3.4.14 Extended Pin Function Setting Register 09 (EPFR09)

The EPFR09 register assigns functions to ADC trigger peripheral pins.

■ **Register Configuration**

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	-							
Initial value	-							

Bit	23	22	21	20	19	18	17	16
Field	Reserved				ADTRG1S			
Attribute	-				R/W			
Initial value	-				0000			

Bit	15	14	13	12	11	10	9	8
Field	ADTRG0S				Reserved			
Attribute	R/W				-			
Initial value	0000				-			

Bit	7	6	5	4	3	2	1	0
Field	Reserved							
Attribute	-							
Initial value	-							

■ **Register Function**

[bit31:20] Reserved: Reserved bits

"0x000" is read from these bits.
When writing these bits, set them to "0x000".

[bit19:16] ADTRG1S: ADTRG1 Input Select bits

Selects input for ADTRG1.

bit19:16		Description
Reading		Reads out the register value.
Writing	0000	Uses ADTG_0 at the input pin of ADC unit 1's startup trigger. [Initial value]
	0001	Same as Writing 0000.
	0010	Setting is prohibited.
	0011	Uses ADTG_2 at the input pin of ADC unit 1's startup trigger.
	0100	Uses ADTG_3 at the input pin of ADC unit 1's startup trigger.
	0101	Setting is prohibited.
	0110	Setting is prohibited.
	0111	Uses ADTG_6 at the input pin of ADC unit 1's startup trigger.
Writing other data		Setting is prohibited.

[bit15:12] ADTRG0S: ADTRG0 Input Select bits

Selects input for ADTRG0.

bit15:12		Description
Reading		Reads out the register value.
Writing	0000	Uses ADTG_0 at the input pin of ADC unit 0's startup trigger. [Initial value]
	0001	Same as Writing 0000.
	0010	Setting is prohibited.
	0011	Uses ADTG_2 at the input pin of ADC unit 0's startup trigger.
	0100	Uses ADTG_3 at the input pin of ADC unit 0's startup trigger.
	0101	Setting is prohibited.
	0110	Setting is prohibited.
	0111	Uses ADTG_6 at the input pin of ADC unit 0's startup trigger.
Writing other data		Setting is prohibited.

[bit11:0] Reserved: Reserved bits

"0x000" is read from these bits.
When writing these bits, set them to "0x000".

Note

- This register is not initialized by deep standby transition reset.

3.4.15 Special Port Setting Register (SPSR)

The SPSR register sets a pin as a signal pin of special functions.

■ **Register Configuration**

Bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	-							
Initial value	-							

Bit	23	22	21	20	19	18	17	16
Field	Reserved							
Attribute	-							
Initial value	-							

Bit	15	14	13	12	11	10	9	8
Field	Reserved							
Attribute	-							
Initial value	-							

Bit	7	6	5	4	3	2	1	0
Field	Reserved				MAINXC		SUBXC	
Attribute	-				R/W		R/W	
Initial value	-				01		01	

■ **Register Function**

[bit31:4] Reserved: Reserved bits

"0x0000000" is read from these bits.
When writing these bits, set them to "0x0000000".

[bit3:2] MAINXC : Main Clock (Oscillation) Pin Setting Register

This bit sets a pin as a main clock (oscillation) pin.

bit		Description
Reading		Reads out the register value.
Writing	0 0	Does not use two pins of X0 and X1 as main clock (oscillation) pins but as digital input/output pins.
	0 1	Uses two pins of X0 and X1 as main clock (oscillation) pins. [Initial value] (An I/O cell will be in a state of input direction, input cut-off, and pull-up disconnection.)
	1 0	Setting is prohibited.
	1 1	Uses X0A pin as an external clock input pin. Uses X1A pin as a digital input/output.

[bit1:0] SUBXC : Sub Clock (Oscillation) Pin Setting Register

This bit sets a pin as a sub clock (oscillation) pin.

bit1:0		Description
Reading		Reads out the register value.
Writing	0 0	Does not use two pins of X0A and X1A as sub clock (oscillation) pins but as digital input/output pins.
	0 1	Uses two pins of X0A and X1A as sub clock (oscillation) pins. [Initial value] (An I/O cell will be in a state of input direction, input cut-off, and pull-up disconnection.)
	1 0	Setting is prohibited.
	1 1	Uses X0A pin as an external clock input pin. Uses X1A pin as a digital input/output.

Notes:

- Only writing "01" to the MAINXC bit does not make a main clock start oscillation.
  To start oscillation, enable oscillation by the MOSCE bit of the System Clock Mode Control Register (SCM_CTL), which is described in "FM3 Family Peripheral Manual" of the chapter "Clock", after writing "01" to the MAINXC bit.
- Only writing "01" to the SUBXC bit does not make a sub clock start oscillation.
  To start oscillation, enable oscillation by the SOSCE bit of the System Clock Mode Control Register (SCM_CTL), which is described in "FM3 Family Peripheral Manual" of the chapter "Clock", after writing "01" to the SUBXC bit.
- This register is not initialized by deep standby transition reset.

3.4.16 Port Pseudo Open Drain Setting Register (PZRx)

PZRx register makes I/O port Hi-Z when output is High level and sets pseudo open drain control.

- **List of PZR register configuration**

bit	31 16	15 0	Initial value	Attribute
	Reserved	PZR0	0x0000	R/W
	Reserved	PZR1	0x0000	R/W
	Reserved	PZR2	0x0000	R/W
	Reserved	PZR3	0x0000	R/W
	Reserved	PZR4	0x0000	R/W
	Reserved	PZR5	0x0000	R/W
	Reserved	PZR6	0x0000	R/W
	Reserved	-	-	-
	Reserved	-	-	-
	Reserved	-	-	-
	Reserved	-	-	-
	Reserved	-	-	-
	Reserved	-	-	-
	Reserved	-		-
	Reserved	PZRE	0x0000	R/W
	Reserved	-	-	-

- **Details of Register Configuration**

Bit	31 16	15 0
Field	Reserved	PZRx

- **Register Function**

[bit31:16] Reserved: Reserved bits

"0x0000" is read from these bits.
When writing these bits, set them to "0x0000".

[bit15:0] PZRx: Port Pseudo Open Drain Setting Register x

Sets the pseudo open drain of the pin.

bit15:0		Description
Reading		Reads out the register value.
Writing	0	Set the pin to High level when outputting digital High level by GPIO or peripheral macro.
	1	Set the pin to Hi-Z when outputting digital High level by GPIO or peripheral macro. Disconnect the pull-up resistor regardless of the PCR setting.

Notes:

- The "x" description of PZRx is wildcard. It shows PZR0, PZR1, PZR2, and so on.
- The function of the PZR register is implemented only in some specific pins.
  Only pins described as "PZR register control is enabled" in remarks column of "I/O circuit type" of "Data Sheet" can control open drain.
- PZR register does not exist in all pins. However, even the pins that do not have PZR registers can control pseudo open drain by the setting of DDR register if they are used as GPIO.
  In such a case, after setting PFR = 0 (GPIO setting) and PDOR = 0,
  When setting L output: used as DDR = 1 (output direction).
  When setting Hi-Z output: used as DDR = 0 (input direction).

However, in open drain by the GPIO setting, you cannot apply voltage that exceeds VCC at Hi-Z.

This register is not initialized by deep standby transition reset.

3.5 Usage Precautions

This section describes precautions for using the I/O port.

- **ON/OFF of the Pull-up Resistance When SPL=1**

SPL is a signal for turning a pin into Hi-Z state during standby mode.

When SPL=0	Normal operations
When SPL=1	Pin Hi-Z, input cut-off, pull-up disconnection

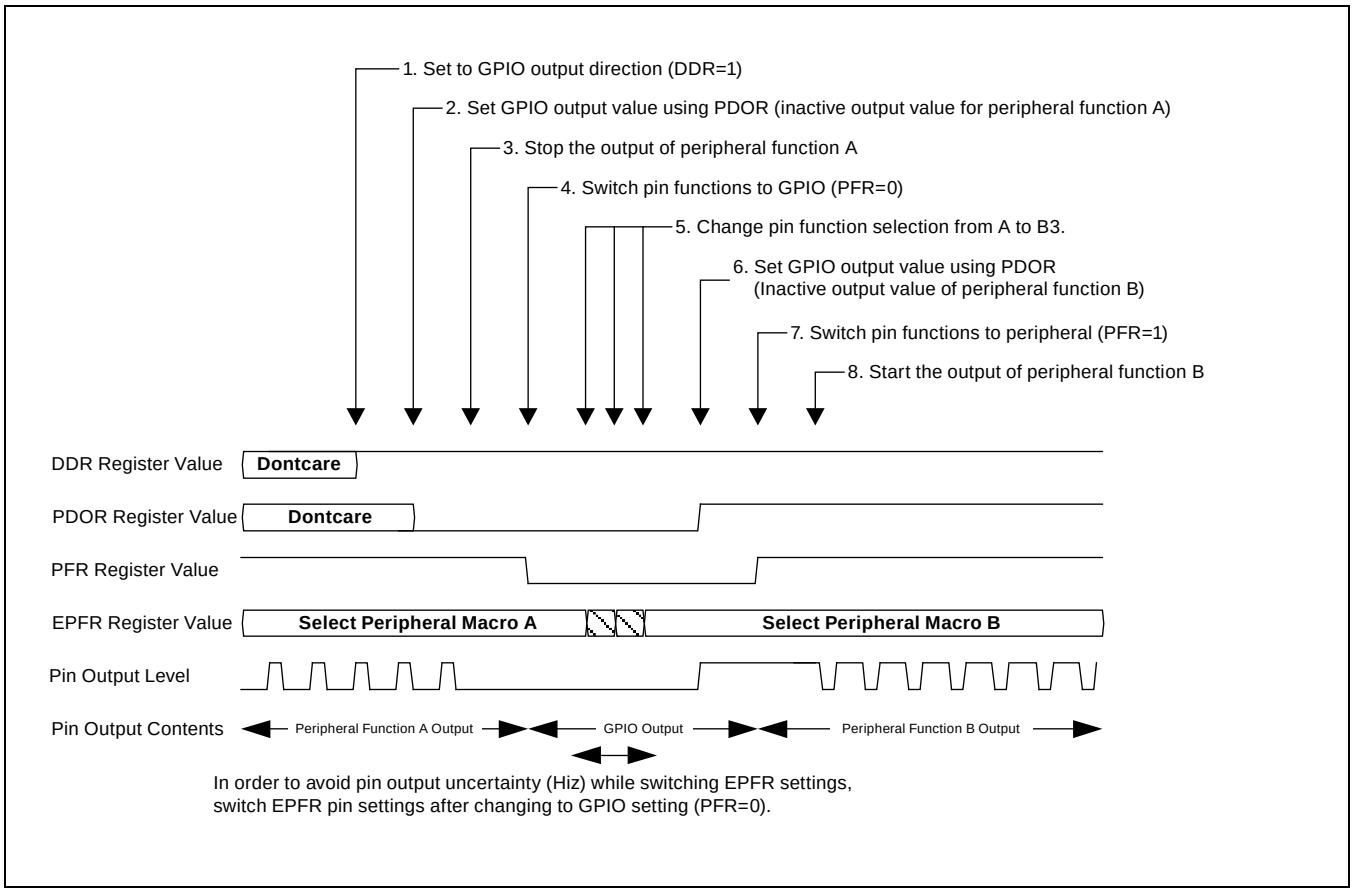
However, the SPL bit cannot be used for setting external interrupts, NMIX, or JTAG pins.

For details of the SPL bit, see Chapter "Low Power Consumption Mode".

- **Procedures for Switching Pin Functions**

When switching the outputs for peripheral functions using the EPFR register, to prevent pin uncertain output (Hi-Z), switch settings according to the procedures similar to the switching example shown in the following Figure 3.5-1.

Figure 3.5-1 Procedures for Switching Pin Functions



- **Reserved bit**

This bit is read out as "0" except for that of ADE register. When writing, always write "0". The ADE reserved bit is read out as "1". When writing, always write "1".

- **Connecting External Bus Pin and SRAM**

When accessing SRAM via external bus, either perform pull-up setting for the pin or connect it to external pull-up pin.

- **Multi-function Serial Pin Group**

When there are some multi-function serial inputs/outputs, set each input/output to the port of the same group. "The port of the same group" means that relocate function numbers attached to the pin name are the same, just like "xxx_0" or "yyy_1".
Table 3.5-1 shows an example setting.

Table 3.5-1 Multi-function Serial Interface example setting

Serial Data Output	Serial Clock Input/Output	Serial Data Input	Effective Port
Pin SOT0_0 (Port 0)	Pin SCK0_0 (Port 0)	Pin SIN0_0 (Port 0)	Port 0
		Pin SIN0_1 (Port 1)	Setting is prohibited.
	Pin SCK0_1 (Port 1)	Pin SIN0_0 (Port 0)	
		Pin SIN0_1 (Port 1)	
Pin SOT0_1 (Port 1)	Pin SCK0_0 (Port 0)	Pin SIN0_0 (Port 0)	
		Pin SIN0_1 (Port 1)	
	Pin SCK0_1 (Port 1)	Pin SIN0 (Port 0)	
		Pin SIN0_1 (Port 1)	Port 1

- **Peripheral Function Output**

As output pins for peripheral functions are uniquely determined by EPFR settings, Output for peripheral functions cannot be assigned to separate pins.
(Disabled example) Assign multifunction serial output SOT0_0 and SOT0_1 to the same output.

- **Pin Settings and Operation Mode**

For JTAG settings, see Chapter "Debug Interface" in "FM3 Family Peripheral Manual".
For state of each pin during standby mode or reset, see "Data Sheet" of the this product.

- **Product Specifications and Peripheral Function Pin Assignment**

Functions which are assigned to pins (GPO, peripheral I/O and special I/O) vary in different products. Please see the pin function table of "Data Sheet" to confirm the pin function of this product. Do not select a function for a pin which is not available in this product by using the EPFR register setting.

- **When MDI pin is used as GPIO**

To use MD1 pin, the following settings are required.

Input: By reading PDIR, the value is read.
Output: Only L output
is available because I/O of MD1 pin is N-ch open drain pin.
PFR=0 (Used as GPIO.)
DDR=1(Used as output)
PDOR=0 (Output data is "0".)
SPL=0 (GPIO status is retained in STOP mode.)

- **External Interrupt Pin Settings in Standby Mode**

When the mode is transferred to the Standby mode under the setting of SPL=1, set PFR=1 and select peripheral functions to enable the external interrupt assignment pin for returning.
If the setting of a pin used for external interrupt is remained PFR=0, unintended operation occurs.

4. Base Timer I/O Select Function



4.1 Overview
4.2 Configuration
4.3 I/O Mode
4.4 External Input Clock Selection
4.5 Registers

4.1 Overview

The base timer I/O select function sets the I/O mode, and thereby determines the method to input and output signals (external clock, external start trigger, and waveform) to/from the base timer.

By switching timer function, each channel of the base timer can be also used as one of the following timers:

- 16-bit PWM timer
- 16-bit PPG timer
- 16/32-bit reload timer
- 16/32-bit PWC timer

- Overview

  One of the following 9 types of I/O modes can be selected for each 2 channels.

  Software-based simultaneous startup function is provided for multiple channels, enabling up to 16 channels to be started up via software.

  - ☐ I/O mode 0: Standard 16-bit timer mode

    This mode operates each channel of the base timer individually.

  - ☐ I/O mode 1: Timer full mode

    This mode assigns each even channel signal of the base timer with an external pin individually to operate the channel.

  - ☐ I/O mode 2: Shared external trigger mode

    This mode can input an external startup trigger to two channels of the base timer simultaneously. Using this mode, the base timer of two channels can be started up simultaneously.

  - ☐ I/O mode 3: Shared channel signal trigger mode

    This mode uses an external signal from another channel as an external startup trigger. This mode cannot be selected for channel 0 or 1.

  - ☐ I/O mode 4: Timer start/stop mode

    This mode controls the start/stop of the odd channel using the even channel. The odd channel starts on the rising edge of output signal from the even channel, and stops on the falling edge.

  - ☐ I/O mode 5: Software-based simultaneous startup mode

    This mode starts up multiple channels simultaneously via software.

  - ☐ I/O mode 6: Software-based startup and timer start/stop mode

    This mode controls the start/stop of the odd channel using the even channel. An even channel is started up via software. The odd channel starts on the rising edge of output signal from the even channel, and stops on the falling edge.

  - ☐ I/O mode 7: Timer start mode

    This mode controls the start of the odd channel using the even channel. The odd channel starts on the rising edge of output signal from the even channel.

  - ☐ I/O mode 8: Shared channel signal trigger and timer start/stop mode

    This mode uses an external signal from another channel as an external startup trigger. This mode cannot be selected for channel 0 or 1.

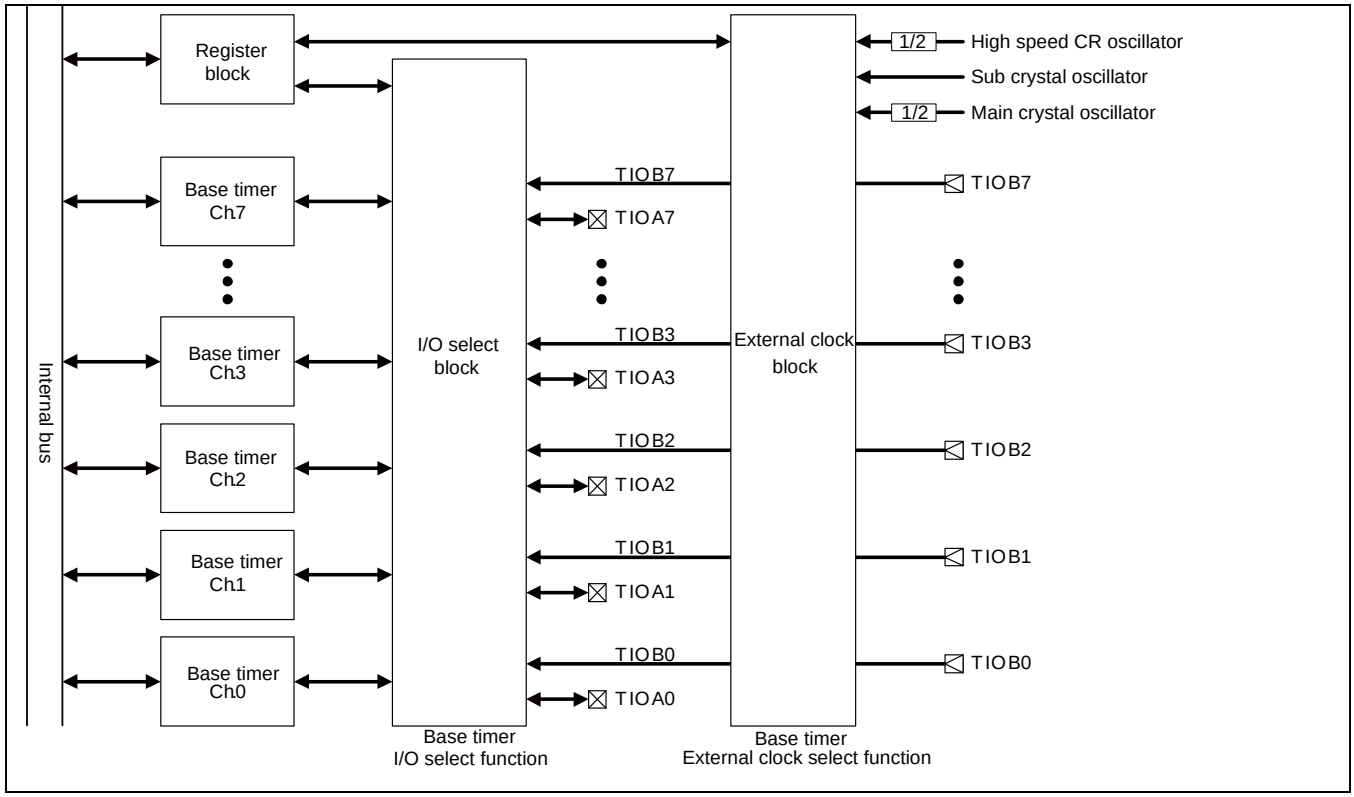
4.2 Configuration

The base timer I/O select function consists of the following blocks.

Block Diagram

Figure 4.2-1. shows the block diagram of the base timer I/O select function.

Figure 4.2-1. Block diagram of base timer I/O select function



- I/O select block
  A circuit that selects the I/O mode of the base timer for each channel.
- External clock select block
  A circuit that selects the external input clock of the base timer for each channel.
- Base timer (Channels 0 to 7)
  Base timer channels 0 to 7 (8 channels).
- Register block
  Registers of base timer I/O select function and external input clock select function.

4.3 I/O Mode

This section explains pins used by the base timer I/O select function to set the I/O mode, and also explains each I/O mode.

4.3.1 Pins

4.3.2 I/O Mode

4.3.1 Pins

This section explains pins used by the base timer I/O select function to set the I/O mode.

Each channel of the base timer has 2 types of external pins and 5 types of internal signals. Also the base timer I/O select function has 2 types of internal signals. By connecting an internal signal with an external pin, the signal corresponding to the connected (external clock (ECK signal)/external startup trigger (TGIN signal)/waveform (TIN signal)) is input or output to/from the base timer. The external pin and internal signal can be connected by setting the I/O mode of the base timer. The pin used and the signal input or output differ depending on the I/O mode.

- External pins
  - ☐ TIOA pin

    This pin is used to output the base timer waveform (TOUT signal), or input an external startup trigger (TGIN signal).
  - ☐ TIOB pin

    This pin is used to input external startup trigger (TGIN signal)/external clock (ECK signal)/another channel waveform (TIN signal).
- Internal signals

A signal is input or output to/from the base timer by being connected with an above external pin, or by inputting an output signal from another channel.

- ☐ TOUT signal

  This signal is the output waveform of the base timer. (Not used by the 16/32-bit PWC timer.)
- ☐ ECK signal

  This signal is an external clock of the base timer. (Not used by the 16/32-bit PWC timer.)
  It is input when the external clock is selected as a counting clock.
- ☐ TGIN signal

  This signal is the external startup trigger of the base timer. (Not used by the 16/32-bit PWC timer.)
  When the valid edge of external startup trigger is selected, the base timer detects the edge of this signal to start up.
- ☐ TIN signal

  This signal is the input waveform of the base timer. This signal is the waveform to be measured. (Used only by the 16/32-bit PWC timer.)
- ☐ DTRG signal

  This signal is the trigger input to the base timer. The base timer stops operating on the falling edge of this signal.
- ☐ COUT signal

  This signal is the trigger output of the base timer I/O select function. This signal is output signal to another channel of the base timer.
- ☐ CIN signal

  This signal is the trigger input to the base timer I/O select function. This signal is input signal from another channel of the base timer.

- Connecting the external pin to the internal signal

The external pin and internal signal can be connected by setting the I/O mode of the base timer

Table 4.3 1. Correspondence between I/O modes and pin connections

I/O mode	TIOAn (Even channel)		TIOBn (Even channel)		TIOAn+1 (Odd channel)		TIOBn+1 (Odd channel)	
	Connected to	I/O	Connected to	I/O	Connected to	I/O	Connected to	I/O
0	Ch.n TOUT	Output	Ch.n ECK/TGIN/ TIN	Input	Ch.n+1 TOUT	Output	Ch.n+1 ECK/TGIN/ TIN	Input
1			Ch.n ECK	Input	Ch.n TGIN	Input	Ch.n TIN	Input
2			Ch.n/Ch.n+1 ECK/TGIN/ TIN *1	Input	Ch.n+1 TOUT	Output	Not used	
3			Not used					
4			Ch.n ECK/TGIN/ TIN	Input				
5			Not used					
6								
7			Ch.n ECK/TGIN/ TIN	Input				
8			Not used					

n : Even (n=0, 2, 4, 6)

Ch.n : Even channel

Ch.n+1 : Odd channel

*1 : Synchronized by the peripheral clock (PCLK)

4.3.2 I/O Mode

I/O mode selected by the I/O Select Register (BTSEL) determines the functions of external pins and the start/stop timing of the base timer.

- **I/O mode 0 (Standard 16-bit timer mode)**

This mode uses each channel of the base timer individually

Table 4.3-2 shows the external pins used when this mode is selected.

Table 4.3-2 External pins used when I/O mode 0 is selected.

	Even channel	Odd channel
Number of input pins	1	1
Number of output pins	1	1

Table 4.3-3 shows the internal signals to which the external pins connect, and signals input or output.

Table 4.3-3 External pin connections and input/output signals when I/O mode 0 is selected.

External pin	I/O	Connected to (internal signal)	Signal input/output
TIOA	Output	TOUT	Outputs the base timer waveform
TIOB	Input	ECK/TGIN/TIN*	Uses the input signal as one of the following signals: External clock (ECK signal) External startup trigger (TGIN signal) Waveform to be measured (TIN signal)

* :The usage of input signals (ECK/TGIN/TIN) differs depending on the Timer Control Register (TMCR) setting of the base timer.

Figure 4.3-3 provides the block diagram of I/O mode 0 (Standard 16-bit timer mode).

Figure 4.3-2. 1 I/O mode 0 (Standard 16-bit timer mode) block diagram

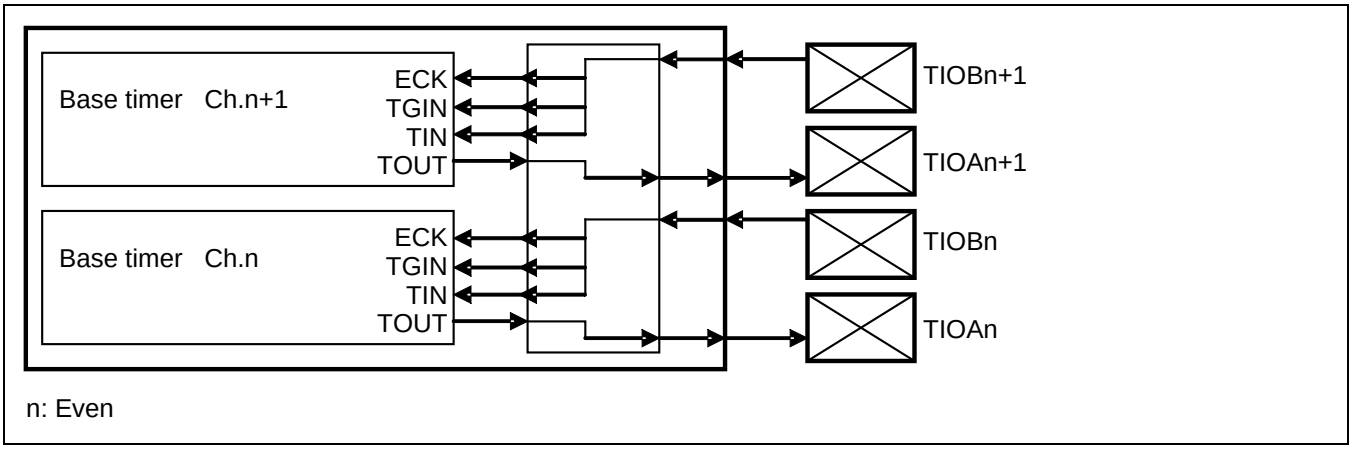


Table 4.3-1 shows signal connections in I/O mode 0.

Table 4.3-1 I/O mode 0 signal connections

Connected from (Signal)	Connected to
Ch.n TOUT signal	Output from the TIOAn pin
Input signal from the TIOBn pin	Input to Ch.n as ECK/TGIN/TIN signals
Ch.n+1 TOUT signal	Output from the TIOAn+1 pin
Input signal from the TIOBn+1 pin	Input to Ch.n+1 as ECK/TGIN/TIN signals

n : Even

- I/O mode 1 (timer full mode)

This mode assigns every even channel signal with an external pin individually.

Table 4.3-2 shows the external pins used when this mode is selected.

Table 4.3-2 External pins used when I/O mode 1 is selected.

	Even channel
Number of input pins	3
Number of output pins	1

Table 4.3-3 shows the internal signals to which the external pins connect, and signals input or output.

Table 4.3-3 External pin connections and input/output signals when I/O mode 1 is selected.

External pin	I/O	Connected to (internal signal)	Signal input/output
TIOAn	Output	Even channel TOUT	Outputs the even channel waveform
TIOBn	Input	Even channel ECK	Inputs an external clock (ECK signal) to the even channel.
TIOAn+1	Input	Even channel TGIN	Inputs an external startup trigger (TGIN signal) to the even channel.
TIOBn+1	Input	Even channel TIN	Inputs the waveform to be measured (TIN signal) to the even channel.

n : Even

Figure 4.3-1 shows the block diagram of I/O mode 1 (timer full mode).

Figure 4.3-1 I/O mode 1 (timer full mode) block diagram

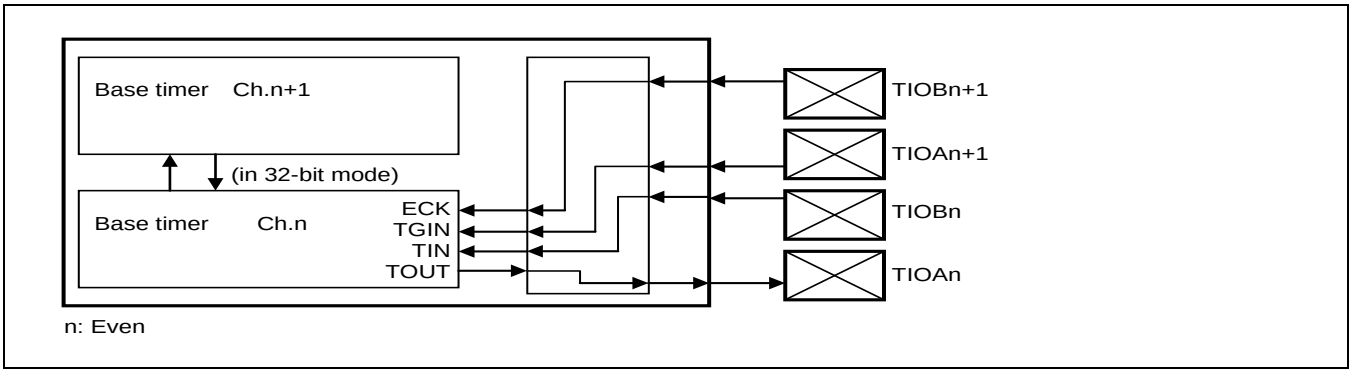


Table 4.3-4 shows signal connections in I/O mode 1.

Table 4.3-4 I/O mode 1 signal connections

Connected from (Signal)	Connected to
Ch.n TOUT signal	Output from the TIOAn pin
Input signal from the TIOBn pin	Input to Ch.n as a TIN signal
TIOAn+1 pin	Input to Ch.n as a TGIN signal
TIOBn+1 pin	Input to Ch.n as an ECK signal

n : Even

<Note>

When this mode is selected, the TIOA pins (TIOA1, TIOA3, etc.) corresponding to the odd channel must be set to port input mode with the Port Function Register (PFR) of GPIO.

- I/O mode 2 (Shared external trigger mode)

This mode shares the input signals (ECK/TGIN/TIN) of the base timer between two channels.

Table 4.3-5 shows the external pins used when this mode is selected.

Table 4.3-5 External pins used when I/O mode 2 is selected.

	Even channel	Odd channel
Number of input pins	1 (shared by two channels)	
Number of output pins	1	1

Table 4.3-6 shows the internal signals to which the external pins connect, and signals input or output.

Table 4.3-6 External pin connections and input/output signals when I/O mode 2 is selected.

External pin	I/O	Connected to (internal signal)	Signal input/output
TIOAn	Output	Even channel TOUT	Outputs the even channel waveform
TIOAn+1	Output	Odd channel TOUT	Outputs the odd channel waveform
TIOBn	Input	ECK/TGIN/TIN of even and odd channels *	Input to both the even and odd channels (synchronized by the peripheral clock (PCLK)) and used as one of the following signals: External clock (ECK signal) External startup trigger (TGIN signal) Waveform to be measured (TIN signal)
TIOBn+1	-	-	Not used

n :Even

* :The usage of input signals (ECK/TGIN/TIN) differs depending on the Timer Control Register (TMCR) setting of the base timer.

Figure 4.3-2 shows the block diagram of I/O mode 2 (Shared external trigger mode).

Figure 4.3-2 I/O mode 2 (Shared external trigger mode) block diagram

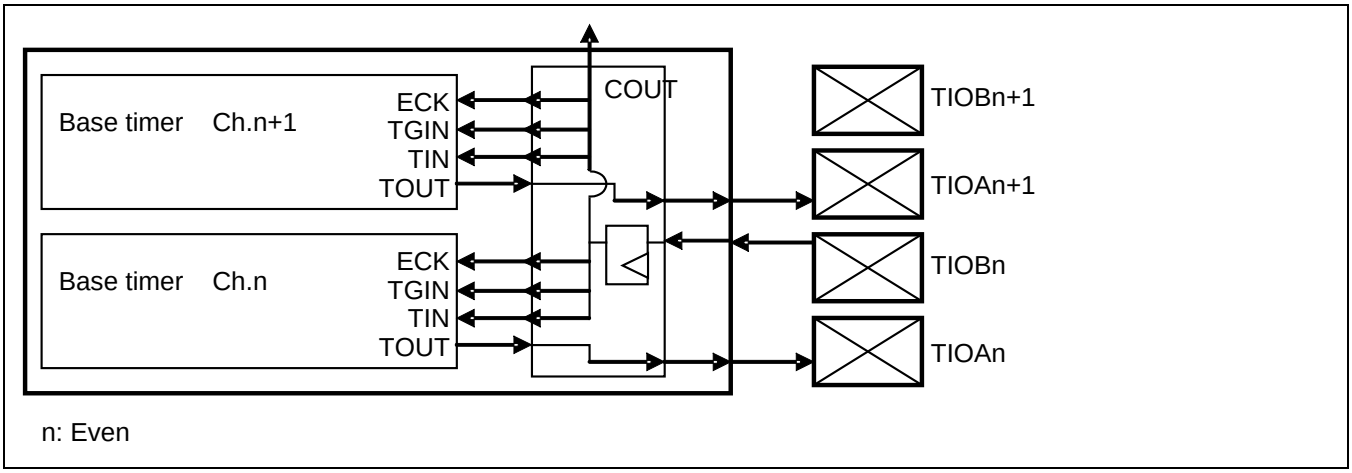


Table 4.3-7 shows signal connections in I/O mode 2.

Table 4.3-7 I/O mode 2 signal connections

Connected from (Signal)	Connected to	Remarks
Ch.n TOUT signal	Output from the TIOAn pin	
Input signal from the TIOBn pin	Input to Ch.n and Ch.n+1 as ECK/TGIN/TIN signals Output to another channel as a COUT signal	Synchronized by the peripheral clock (PCLK)
Ch.n+1 TOUT signal	Output from the TIOAn+1 pin	

n : Even

Note:

If the upper two channels of the channels set to this mode (n+2, n+3) are set to I/O mode 3 (Shared channel signal trigger mode), the input signals (ECK/TGIN/TIN) can be input to the 4 channels simultaneously.

(Example: If channels 0 and 1 are set to this mode, and channels 2 and 3 are set to I/O mode 3, input signals (ECK/TGIN/TIN) can be input to four channels of 0 to 3 simultaneously.)

- I/O mode 3 (Shared channel signal trigger mode)

This mode inputs the COUT signal from channels of the lower two channels as a CIN signal, and uses it as ECK/TGIN/TIN signals.

Table 4.3-8 shows the external pins used when this mode is selected.

Table 4.3-8 External pins used when I/O mode 3 is selected.

	Even channel	Odd channel
Number of input pins	Not used	
Number of output pins	1	1

Table 4.3-9 shows the internal signals to which the external pins connect, and signals input or output.

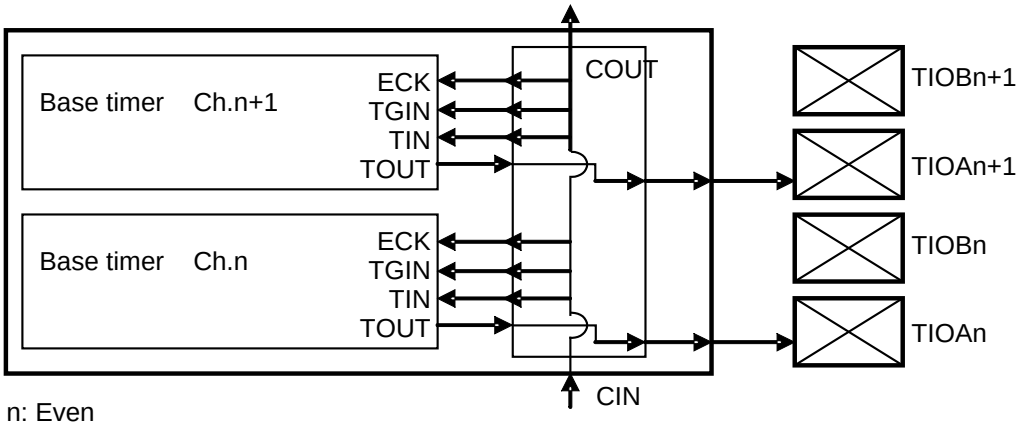
Table 4.3-9 External pin connections and input/output signals when I/O mode 3 is selected.

External pin	I/O	Connected to (internal signal)	Signal input/output
TIOAn	Output	Even channel TOUT	Outputs the even channel waveform
TIOAn+1	Output	Odd channel TOUT	Outputs the odd channel waveform
TIOBn TIOBn+1	-	-	Not used

n : Even

Figure 4.3-3 shows the block diagram of I/O mode 3 (Shared channel signal trigger mode).

Figure 4.3-3 I/O mode 3 (Shared channel signal trigger mode) block diagram



n: Even

Table 4.3-10 shows signal connections in I/O mode 3.

Table 4.3-10 I/O mode 3 signal connections

Connected from (Signal)	Connected to
Ch.n TOUT signal	Output from the TIOAn pin
CIN signal *	Input to Ch.n and Ch.n+1 as ECK/TGIN/TIN signals Output to another channel as a COUT signal
Ch.n+1 TOUT signal	Output from the TIOAn+1 pin

n : Even

* : The COUT signal from another channel is input as a CIN signal.

The following shows Ch.n-2/n-1 signals that can be input to ECK/TGIN/TIN of Ch.n/n+1.

- ☐ Signal that the peripheral clock generates by synchronizing TIOBn-2 input in I/O mode 2.
- ☐ Trigger signal input from Ch.n-4/n-3 in I/O mode 3.
- ☐ TIOAn-2 output in I/O mode 4.
- ☐ TIOAn-2 output in I/O mode 6.
- ☐ TIOAn-2 output in I/O mode 7.
- ☐ Trigger signal input from Ch.n-4/n-3 in I/O mode 8.

Notes

- Select the rising edge as a trigger input edge using the EGS1 and EGS0 bits in the Timer Control Register (TMCR) of the base timer. (Set EGS1 and EGS0 to 0b01.)
- The channels set to this mode use the COUT signal from lower two channels (n-2 and n-1) as a CIN signal. (Example: If channels 2 and 3 are set to this mode, they use the COUT signal from channels 0 and 1.) Therefore, channels 0 and 1 cannot be set to this mode.

- I/O mode 4 (Timer start/stop mode)

This mode can control the start/stop of the odd channel using the even channel.

The odd channel starts on the rising edge of output waveform (TOUT signal) of the even channel, and stops on the falling edge.

Table 4.3-11 shows the external pins used when this mode is selected.

Table 4.3-11 External pins used when I/O mode 4 is selected.

	Even channel	Odd channel
Number of input pins	1	Not used
Number of output pins	1	1

Table 4.3-12 shows the internal signals to which the external pins connect, and signals input or output.

Table 4.3-12 External pin connections and input/output signals when I/O mode 4 is selected.

External pin	I/O	Connected to (internal signal)	Signal input/output
TIOAn	Output	Even channel TOUT	Outputs the even channel waveform
TIOAn+1	Output	Odd channel TOUT	Outputs the odd channel waveform
TIOBn	Input	ECK/TGIN/TIN of even channel *	Input to the even channel and used as one of the following signals: External clock (ECK signal) External startup trigger (TGIN signal) Waveform to be measured (TIN signal)
TIOBn+1	-	-	Not used

n :Even

* :The usage of input signals (ECK/TGIN/TIN) differs depending on the Timer Control Register (TMCR) setting of the base timer.

Figure 4.3-4 shows the block diagram of I/O mode 4 (Timer start/stop mode).

Figure 4.3-4 I/O mode 4 (Timer start/stop mode) block diagram

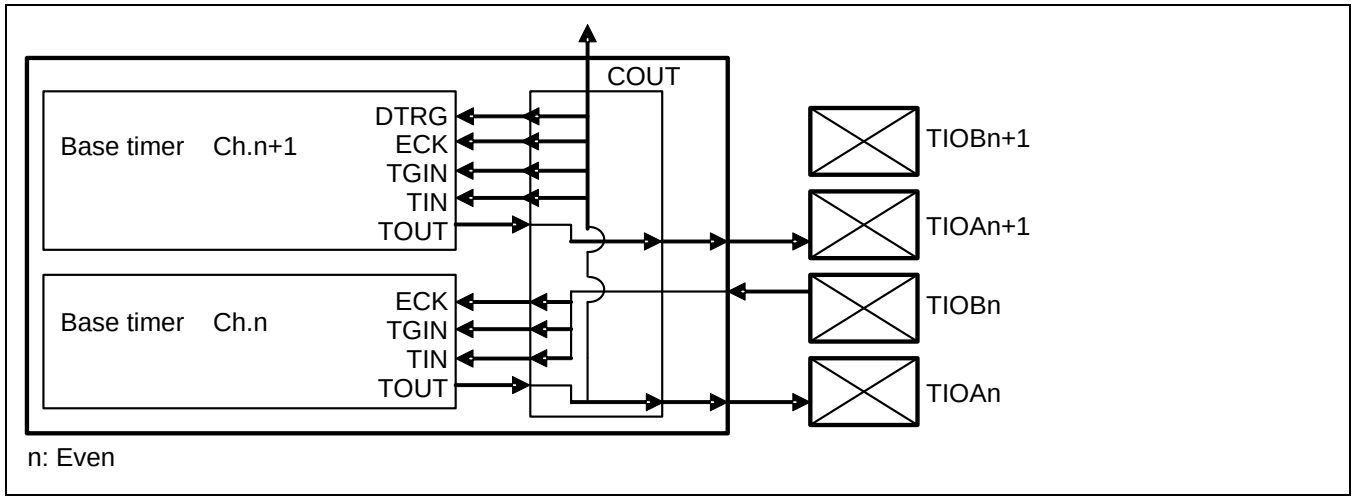


Table 4.3-13 shows signal connections in I/O mode 4.

Table 4.3-13 I/O mode 4 signal connections

Connected from (Signal)	Connected to
Ch.n TOUT signal	Output from the TIOAn pin Input to Ch.n+1 as ECK/TGIN/TIN and DTRG signals Output to another channel as a COUT signal
Input signal from the TIOBn pin	Input to Ch.n as ECK/TGIN/TIN signals
Ch.n+1 TOUT signal	Output from the TIOAn+1 pin

n : Even

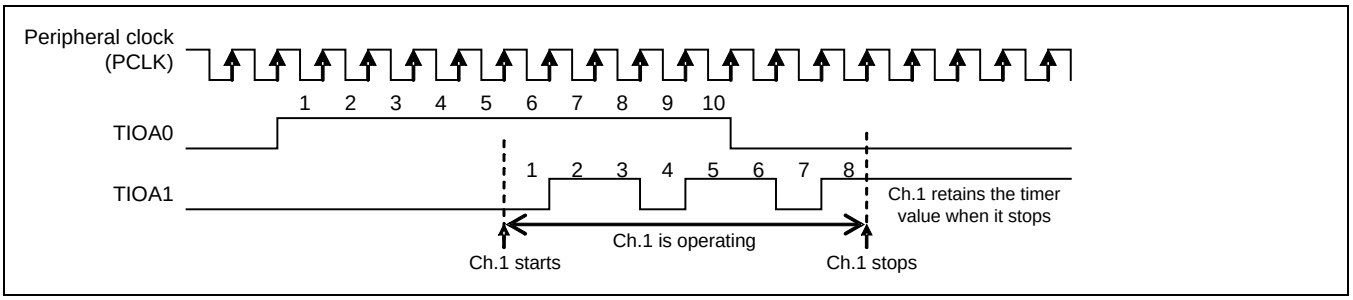
<Notes>

- Select the rising edge as a trigger input edge of the odd channel using the EGS1 and EGS0 bits in the Timer Control Register (TMCR) of the base timer. (Set EGS1 and EGS0 to 0b01.)
- The odd channel stops operating when a falling edge is detected in the DTRG signal.

Figure 4.3-5 shows example operation when I/O mode 4 (Timer start/stop mode) is selected, and when channels 0 and 1 are used as PWM timer.

Base timer Ch.0	Set value	Base timer Ch.1	Set value
Cycle Setup Register (PCSR)	0x0010	Cycle Setup Register (PCSR)	0x0002
Duty Setup Register (PDUT)	0x0009	Duty Setup Register (PDUT)	0x0001
Timer Control Register (TMCR)	0x0013	Timer Control Register (TMCR)	0x0112

Figure 4.3-5 I/O mode 4 (Timer start/stop mode) operation example



- I/O mode 5 (Software-based simultaneous startup mode)

This mode starts up multiple channels simultaneously using the Software-based Simultaneous Startup Register (BTSSSR).

All the channels corresponding to the Software-based Simultaneous Startup Register (BTSSSR) bits that have been set to "1" start up simultaneously.

Table 4.3-14 shows the external pins used when this mode is selected.

Table 4.3-14 External pins used when I/O mode 5 is selected.

	Even channel	Odd channel
Number of input pins	Not used	
Number of output pins	1	1

Table 4.3-15 shows the internal signals to which the external pins connect, and signals input or output.

Table 4.3-15 External pin connections and input/output signals when I/O mode 5 is selected.

External pin	I/O	Connected to (internal signal)	Signal input/output
TIOAn	Output	Even channel TOUT	Outputs the even channel waveform
TIOAn+1	Output	Odd channel TOUT	Outputs the odd channel waveform
TIOBn TIOBn+1	-	-	Not used

n : Even

Figure 4.3-6 shows the block diagram of I/O mode 5 (Software-based simultaneous startup mode).

Figure 4.3-6 I/O mode 5 (Software-based simultaneous startup mode) block diagram

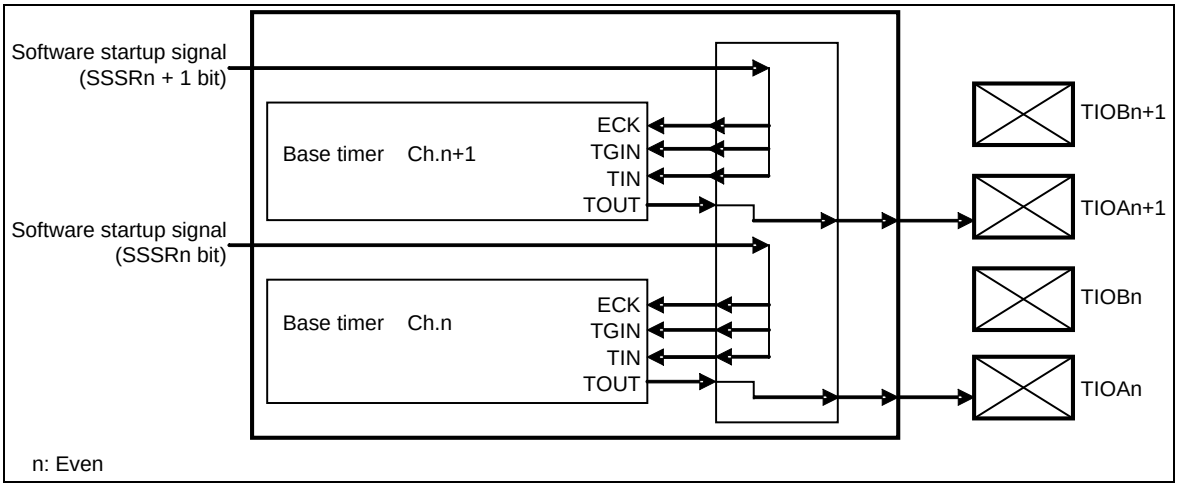


Table 4.3-16 shows signal connections in I/O mode 5.

Table 4.3-16 I/O mode 5 signal connections

Connected from (Signal)	Connected to
Ch.n TOUT signal	Output from the TIOAn pin
Software startup signal (Write "1" to the SSSRn bit in the BTSSSR)	Input to Ch.n as ECK/TGIN/TIN signals
Ch.n+1 TOUT signal	Output from the TIOAn+1 pin
Software startup signal (Write "1" to the SSSRn+1 bit in the BTSSSR)	Input to Ch.n+1 as ECK/TGIN/TIN signals

n : Even

BTSSSR : Software-based Simultaneous Startup Register

When "1" is written to a Software-based Simultaneous Startup Register (BTSSSR), a rising edge is input (ECK/TGIN/TIN signals) to the channel corresponding to the bit.

Note:

Select the rising edge as a trigger input edge using the EGS1 and EGS0 bits in the Timer Control Register (TMCR) of the base timer. (Set EGS1 and EGS0 to 0b01.)

- I/O mode 6 (Software-based startup and timer start/stop mode)

This mode can control the start/stop of the odd channel using the even channel.

The even channel can be started by writing "1" to the Software-based Simultaneous Startup Register (BTSSSR).

The odd channel starts when the rising edge is detected in output waveform (TOUT signal) of the even channel, and stops when the falling edge is detected.

Table 4.3-17 shows the external pins used when this mode is selected.

Table 4.3-17 External pins used when I/O mode 6 is selected.

	Even channel	Odd channel
Number of input pins	Not used	
Number of output pins	1	1

Table 4.3-18 shows the internal signals to which the external pins connect, and signals input or output.

Table 4.3-18 External pin connections and input/output signals when I/O mode 6 is selected.

External pin	**I/O**	**Connected to (internal signal)**	**Signal input/output**
TIOAn	Output	Even channel TOUT	Outputs the even channel waveform
TIOAn+1	Output	Odd channel TOUT	Outputs the odd channel waveform
TIOBn TIOBn+1	-	-	Not used

n : Even

Figure 4.3-7 shows the block diagram of I/O mode 6 (Software-based startup and timer start/stop mode).

Figure 4.3-7 I/O mode 6 (Software-based startup and timer start/stop mode) block diagram

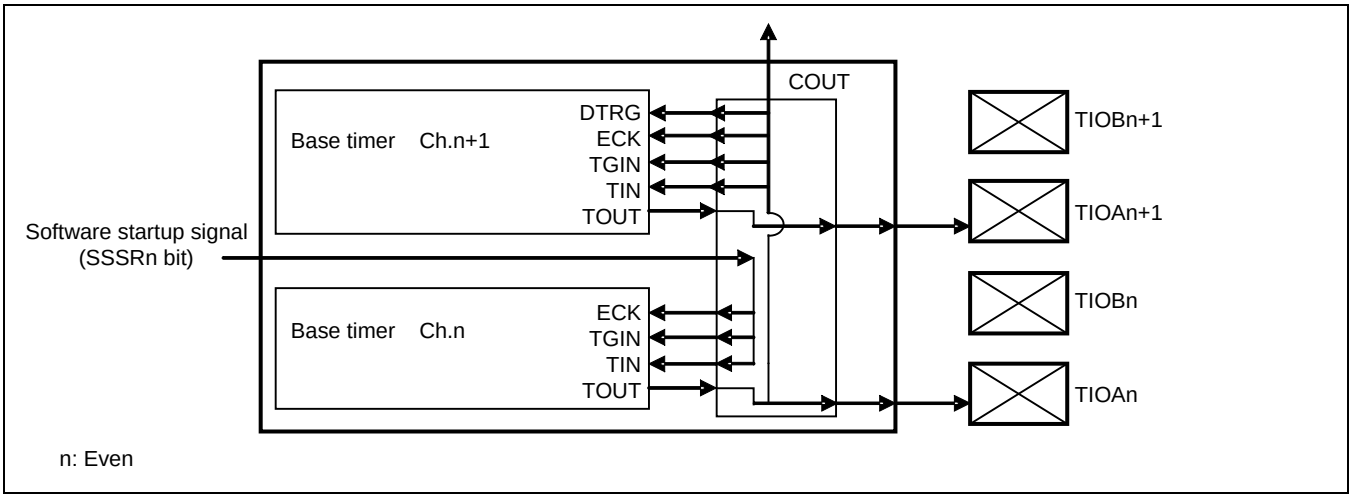


Table 4.3-19 shows signal connections in I/O mode 6.

Table 4.3-19 I/O mode 6 signal connections

Connected from (Signal)	Connected to
Ch.n TOUT signal	Output from the TIOAn pin Input to Ch.n+1 as ECK/TGIN/TIN/DTRG signals Output to another channel as a COUT signal
Software startup signal (Write "1" to the SSSRn bit in the BTSSSR)	Input to Ch.n as ECK/TGIN/TIN signals
Ch.n+1 TOUT signal	Output from the TIOAn+1 pin

n : Even

BTSSSR : Software-based Simultaneous Startup Register

When "1" is written to the Software-based Simultaneous Startup Register (BTSSSR) bit corresponding to the even channel you want to start up, a rising edge is input (ECK/TGIN/TIN signals) to the channel.

The start/stop timing of Ch.n is the same as that for I/O mode 4.

<Notes>

- Select the rising edge as a trigger input edge using the EGS1 and EGS0 bits in the Timer Control Register (TMCR) of the base timer. (Set EGS1 and EGS0 to 0b01.)
- The odd channel stops operating when a falling edge is detected in the DTRG signal.

- I/O mode 7 (Timer start mode)

This mode uses the output waveform (TOUT signal) from the even channel as input signals (ECK/TGIN/TIN signals) of the odd channel.

Table 4.3-20 shows the external pins used when this mode is selected.

Table 4.3-20 External pins used when I/O mode 7 is selected.

	Even channel	Odd channel
Number of input pins	1	Not used
Number of output pins	1	1

Table 4.3-21 shows the internal signals to which the external pins connect, and signals input or output.

Table 4.3-21 External pin connections and input/output signals when I/O mode 7 is selected.

External pin	I/O	Connected to (internal signal)	Signal input/output
TIOAn	Output	Even channel TOUT	Outputs the even channel waveform
TIOAn+1	Output	Odd channel TOUT	Outputs the odd channel waveform
TIOBn	Input	Even channel ECK/ TGIN/TIN *	Input to the even channel and used as one of the following signals: External clock (ECK signal) External startup trigger (TGIN signal) Waveform to be measured (TIN signal)
TIOBn+1	-	-	Not used

n :Even

* :The usage of input waveforms (ECK/TGIN/TIN signals) differs depending on the Timer Control Register (TMCR) setting.

Figure 4.3-8 shows the block diagram of I/O mode 7 (Timer start mode).

Figure 4.3-8 I/O mode 7 (Timer start mode) block diagram

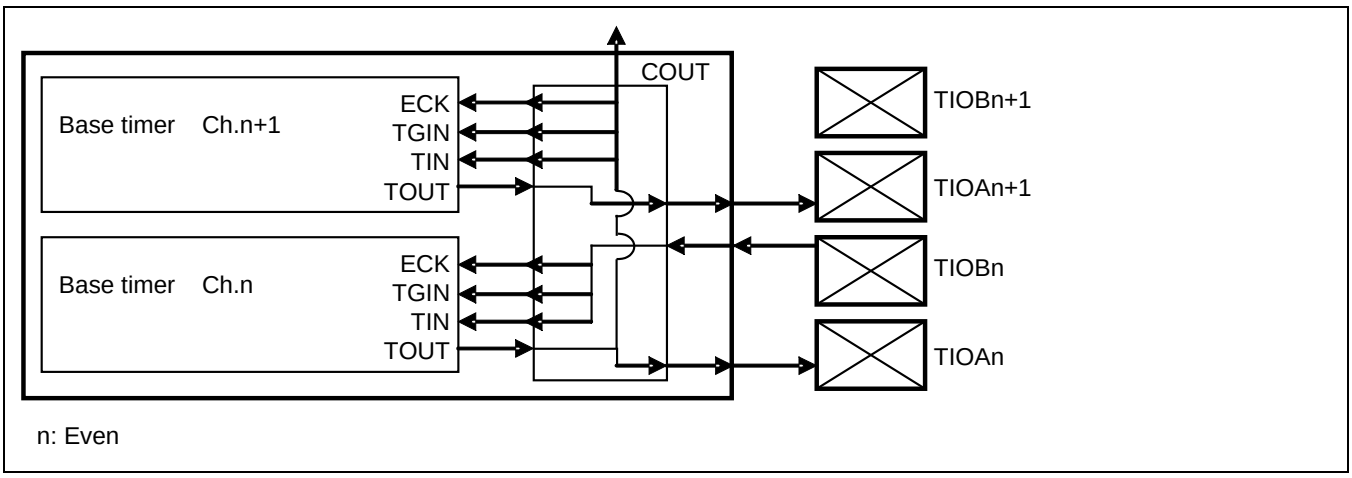


Table 4.3-22 shows signal connections in I/O mode 7.

Table 4.3-22 I/O mode 7 signal connections

Connected from (Signal)	Connected to
Ch.n TOUT signal	Output from the TIOAn pin Input to Ch.n+1 as ECK/TGIN/TIN signals Output to another channel as a COUT signal
Input signal from the TIOBn pin	Input to Ch.n as ECK/TGIN/TIN signals
Ch.n+1 TOUT signal	Output from the TIOAn+1 pin

n : Even

The start timing of Ch.n is the same as that for I/O mode 4.

■ I/O mode 8 (Shared channel signal trigger and timer start/stop mode)

This mode inputs the COUT signal from channels of the lower two channels as a CIN signal, and uses it as an external startup trigger (TGIN signal).

Table 4.3-23 shows the external pins used when this mode is selected.

Table 4.3-23 External pins used when I/O mode 8 is selected.

	Even channel	Odd channel
Number of input pins	Not used	
Number of output pins	1	1

Table 4.3-24 shows the internal signals to which the external pins connect, and signals input or output.

Table 4.3-24 External pin connections and input/output signals when I/O mode 8 is selected.

External pin	I/O	Connected to (internal signal)	Signal input/output
TIOAn	Output	Even channel TOUT	Outputs the even channel waveform
TIOAn+1	Output	Odd channel TOUT	Outputs the odd channel waveform
TIOBn TIOBn+1	-	-	Not used

n : Even

Figure 4.3-9 shows the block diagram of I/O mode 8 (Shared channel signal trigger and timer start/stop mode).

Figure 4.3-9 I/O mode 8 (Shared channel signal trigger and timer start/stop mode) block diagram

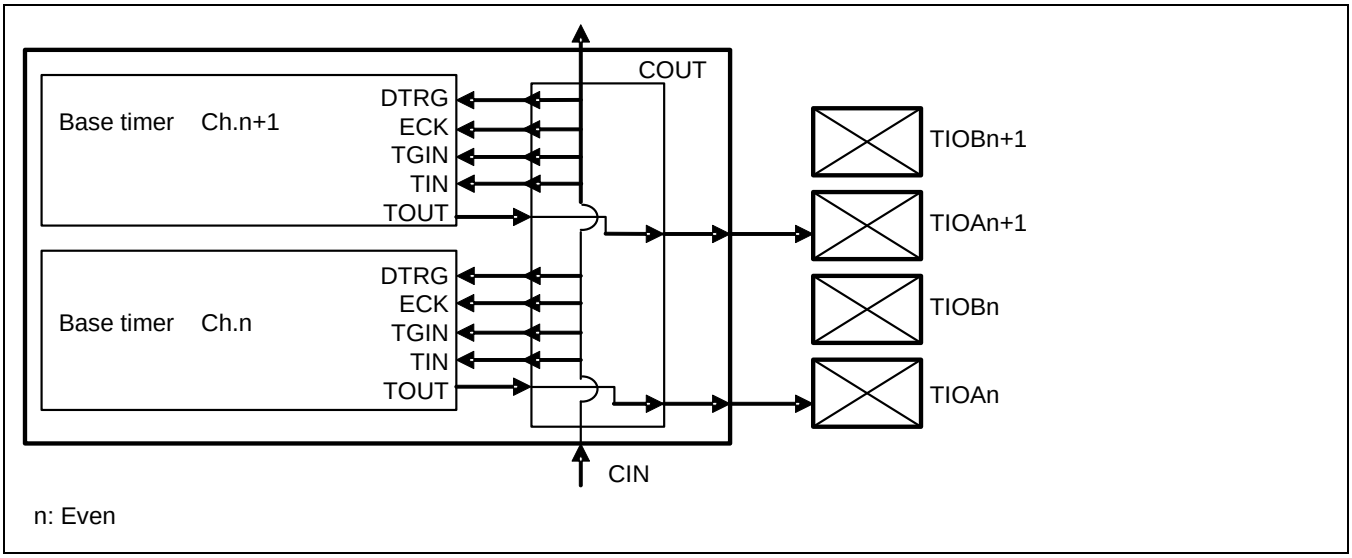


Table 4.3-25 shows signal connections in I/O mode 8.

Table 4.3-25 I/O mode 8 signal connections

Connected from (Signal)	Connected to
Ch.n TOUT signal	Output from the TIOAn pin
Ch.n+1 TOUT signal	Output from the TIOAn+1 pin
CIN signal *	Input to Ch.n and Ch.n+1 as ECK/TGIN/TIN and DTRG signals Output to another channel as a COUT signal

n : Even

* : The COUT signal from another channel is input as a CIN signal. The following shows Ch.n-2/n-1 signals that can be input to ECK/TGIN/TIN of Ch.n/n+1.

- ☐ Signal that the peripheral clock generates by synchronizing TIOBn-2 input in I/O mode 2.
- ☐ Trigger signal input from Ch.n-4/n-3 in I/O mode 3.
- ☐ TIOAn-2 output in I/O mode 4.
- ☐ TIOAn-2 output in I/O mode 6.
- ☐ TIOAn-2 output in I/O mode 7.
- ☐ Trigger signal input from Ch.n-4/n-3 in I/O mode 8.

Notes:

- The channels set to this mode use the COUT signal from lower 2 channels (n-2 and n-1) as a CIN signal. (Example: If channels 2 and 3 are set to this mode, they use the COUT signal from channels 0 and 1.) Therefore, channels 0 and 1 cannot be set to this mode.
- Select the rising edge as a trigger input edge, for the channel set in this mode, using the EGS1 and EGS0 bits in the Timer Control Register (TMCR) of the base timer. (Set EGS1 and EGS0 to 0b01.)
  However, do not enable this setting if the timer function is set to the 16/32-bit PWC timer using FMD[2:0] bits in the Timer Control Register (TMCR) of the base timer (FMD[2:0] bits are set to 0b100).
- Base timer stops operating when a falling edge is detected in the DTRG signal.

4.4 External Input Clock Selection

When an external input is chosen by a base timer input-and-output function preselection capability, the function which chooses the clock to input is explained.

- High speed CR Oscillator

  It is an output clock of a high-speed CR oscillator.

- Sub Crystal Oscillator

  It is a clock which connects crystal oscillator to a sub oscillation pins (X0A, X1A), and it makes it generate.

- Main Oscillator

  It is a clock which connects crystal oscillator to a main oscillation pins (X0, X1), and it makes it generate.

- External Input

  It is a clock inputted from an external input external terminal (TIOB).

4.5 Registers

This section provides the register list of the base timer I/O select function.

- **Base Timer I/O Select Function Registers**

Table 4.5-1 Register list of Base timer I/O select function

Abbreviation	Register name	Reference
BTSEL0123	I/O Select Register	4.5.1
BTSEL4567	I/O Select Register	4.5.2
BTSSSR	Software-based Simultaneous Startup Register	4.5.3

Table 4.5-2 Register list of Base timer External Input Clock select function

Abbreviation	Register name	Reference
BTCLKSEL	External Input Clock Select Register	4.5.4

4.5.1 I/O Select Register (BTSEL0123)

This register selects the I/O mode for channels 0 to 3 of the base timer.

- **Register configuration**

bit	15	14	13	12	11	10	9	8
Field	SEL23_3	SEL23_2	SEL23_1	SEL23_0	SEL01_3	SEL01_2	SEL01_1	SEL01_0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

- **Register functions**

[bit15:12] SEL23_3 to SEL23_0: I/O select bits for Ch.2/Ch.3

bit15	bit14	bit13	bit12	I/O select bits
0	0	0	0	I/O mode 0 (Standard 16-bit timer mode)
0	0	0	1	I/O mode 1 (Timer full mode)
0	0	1	0	I/O mode 2 (Shared external trigger mode)
0	0	1	1	I/O mode 3 (Shared channel signal trigger mode)
0	1	0	0	I/O mode 4 (Timer start/stop mode)
0	1	0	1	I/O mode 5 (Software-based simultaneous startup mode)
0	1	1	0	I/O mode 6 (Software-based startup and timer start/stop mode)
0	1	1	1	I/O mode 7 (Timer start mode)
1	0	0	0	I/O mode 8 (Shared channel signal trigger and timer start/stop mode)
Others				Setting is prohibited.

[bit11:8] SEL01_3 to SEL01_0: I/O select bits for Ch.0/Ch.1

bit11	bit10	bit9	bit8	I/O select bits
0	0	0	0	I/O mode 0 (Standard 16-bit timer mode)
0	0	0	1	I/O mode 1 (Timer full mode)
0	0	1	0	I/O mode 2 (Shared external trigger mode)
0	0	1	1	I/O mode 3 (Shared channel signal trigger mode)
0	1	0	0	I/O mode 4 (Timer start/stop mode)
0	1	0	1	I/O mode 5 (Software-based simultaneous startup mode)
0	1	1	0	I/O mode 6 (Software-based startup and timer start/stop mode)
0	1	1	1	I/O mode 7 (Timer start mode)
1	0	0	0	I/O mode 8 (Shared channel signal trigger and timer start/stop mode)
Others				Setting is prohibited.

<Notes>

- Channels 0 and 1 are the lowest channels of the base timer, and cannot use the modes that use signal from lower channels. Therefore, the following modes cannot be selected for the channels:
  - ☐ I/O mode 3 (Shared channel signal trigger mode)
  - ☐ I/O mode 8 (Shared channel signal trigger and timer start/stop mode)
- Before rewriting this register, set the base timer to reset mode using the FMD[2:0] bits in the Timer Control Register (TMCR) of the base timer. (Set FMD[2:0] bits to 0b000.)

4.5.2 I/O Select Register (BTSEL4567)

This register selects the I/O mode for channels 4 to 7 of the base timer.

- **Register configuration**

bit	15	14	13	12	11	10	9	8
Field	SEL67_3	SEL67_2	SEL67_1	SEL67_0	SEL45_3	SEL45_2	SEL45_1	SEL45_0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

- **Register functions**

[bit15:12] SEL67_3 to SEL67_0: I/O select bits for Ch.6/Ch.7

bit15	bit14	bit13	bit12	I/O select bits
0	0	0	0	I/O mode 0 (Standard 16-bit timer mode)
0	0	0	1	I/O mode 1 (Timer full mode)
0	0	1	0	I/O mode 2 (Shared external trigger mode)
0	0	1	1	I/O mode 3 (Shared channel signal trigger mode)
0	1	0	0	I/O mode 4 (Timer start/stop mode)
0	1	0	1	I/O mode 5 (Software-based simultaneous startup mode)
0	1	1	0	I/O mode 6 (Software-based startup and timer start/stop mode)
0	1	1	1	I/O mode 7 (Timer start mode)
1	0	0	0	I/O mode 8 (Shared channel signal trigger and timer start/stop mode)
Others				Setting is prohibited.

[bit11:8] SEL45_3 to SEL45_0: I/O select bits for Ch.4/Ch.5

bit11	bit10	bit9	bit8	I/O select bits
0	0	0	0	I/O mode 0 (Standard 16-bit timer mode)
0	0	0	1	I/O mode 1 (Timer full mode)
0	0	1	0	I/O mode 2 (Shared external trigger mode)
0	0	1	1	I/O mode 3 (Shared channel signal trigger mode)
0	1	0	0	I/O mode 4 (Timer start/stop mode)
0	1	0	1	I/O mode 5 (Software-based simultaneous startup mode)
0	1	1	0	I/O mode 6 (Software-based startup and timer start/stop mode)
0	1	1	1	I/O mode 7 (Timer start mode)
1	0	0	0	I/O mode 8 (Shared channel signal trigger and timer start/stop mode)
Others				Setting is prohibited.

<Note>

Before rewriting this register, set the base timer to reset mode using the FMD[2:0] bits in the Timer Control Register (TMCR) of the base timer. (Set FMD[2:0] bits to 0b000.)

4.5.3 Software-based Simultaneous Startup Register (BTSSSR)

This register starts up the base timer using software simultaneously.

Up to 16 channels can be started simultaneously if the bits corresponding to the channel are set to "1".

- **Register configuration**

bit	15							8
Field	Reserved							
Attribute	-							
Initial value	-							

bit	7							0
Field	SSSR7 to SSSR0							
Attribute	W							
Initial value	0xXX							

- **Register functions**

[bit15:8] Reserved : Reserved bits

Set these bits to "0" when writing.

[bit7:0] SSSR7 to SSSR0: Software-based simultaneous startup bits

bit	Software-based simultaneous startup bits
0	Writing "0" to these bits is invalid
1	Starts Ch.x of the base timer

<Notes>

- Do not write to this register unless set to either of the following modes:
  - ☐ I/O mode 5 (Software-based simultaneous startup mode)
  - ☐ I/O mode 6 (Software-based startup and timer start/stop mode)(Even channels only)
- For the channel started up by using this register, select the rising edge as a trigger input edge using the EGS1 and EGS0 bits in the Timer Control Register (TMCR) of the base timer. (Set EGS1 and EGS0 to 0b01.)

4.5.4 External Input Clock Select Register (BTCLKSEL)

This register which chooses the input clock to the external clock (TIOB) of a base timer.

■ **Register configuration**

bit	31	30	29	28	27	26	25	24
Field	Reserved							
Attribute	-							
Initial value	-							

bit	23	22	21	20	19	18	17	16
Field	Reserved							
Attribute	-							
Initial value	-							

bit	15	14	13	12	11	10	9	8
Field	BTCLKSEL[15:8]							
Attribute	R/W							
Initial value	0x00							

bit	7	6	5	4	3	2	1	0
Field	BTCLKSEL[7:0]							
Attribute	R/W							
Initial value	0x00							

■ **Register functions**

[bit31:16] Reserved : reserved bits

The read value is undefined. Writing has no effect on operation.

[bit15:0] BTCLKSEL15 to BTCLKSEL0 : External Input Clock Select bits

- ☐ This bit is the clock inputted from the external input TIOB of a base timer.
- ☐ This register becomes effective only when an external clock is chosen in the count clock selection bits (CSK3 to CSK0) of the timer control register (TMCR and TMCR2) of base timer.

bit[n+1:n]	Function
00	Selects external input pins (TIOB[x]) [Initial value]
01	Selects high-speed CR oscillation 2 dividing.
10	Selects sub oscillation 32 kHz
11	Selects main oscillation 2 dividing

* : As for n, the even number to 0 to 14 and x indicate even the channel 0 to 7 of a base timer (x=n/2).

bit	Relation of External Input Pin (TIOB)
BCLKSEL[15:14]	Selects the input clock of TIOB[7].
BCLKSEL[13:12]	Selects the input clock of TIOB[6].
BCLKSEL[11:10]	Selects the input clock of TIOB[5].
BCLKSEL[9:8]	Selects the input clock of TIOB[4].
BCLKSEL[7:6]	Selects the input clock of TIOB[3].
BCLKSEL[5:4]	Selects the input clock of TIOB[2].
BCLKSEL[3:2]	Selects the input clock of TIOB[1].
BCLKSEL[1:0]	Selects the input clock of TIOB[0].

<Note>

This register should be a CTEN bit of the timer control register (TMCR) of base timer, and rewrite it after suspending a base timer (CTEN = 0).

5. PGA (Programmable Gain AMP)

This chapter explains PGA.

5.1 Overview

5.2 I/O Signal of PGA

5.3 Method for PGA

5.4 Setting Procedure of PGA

5.5 Initial Setting

5.6 PGA Registers

5.7 PGA Characteristic

5.1 Overview

This section explains the overview of PGA.

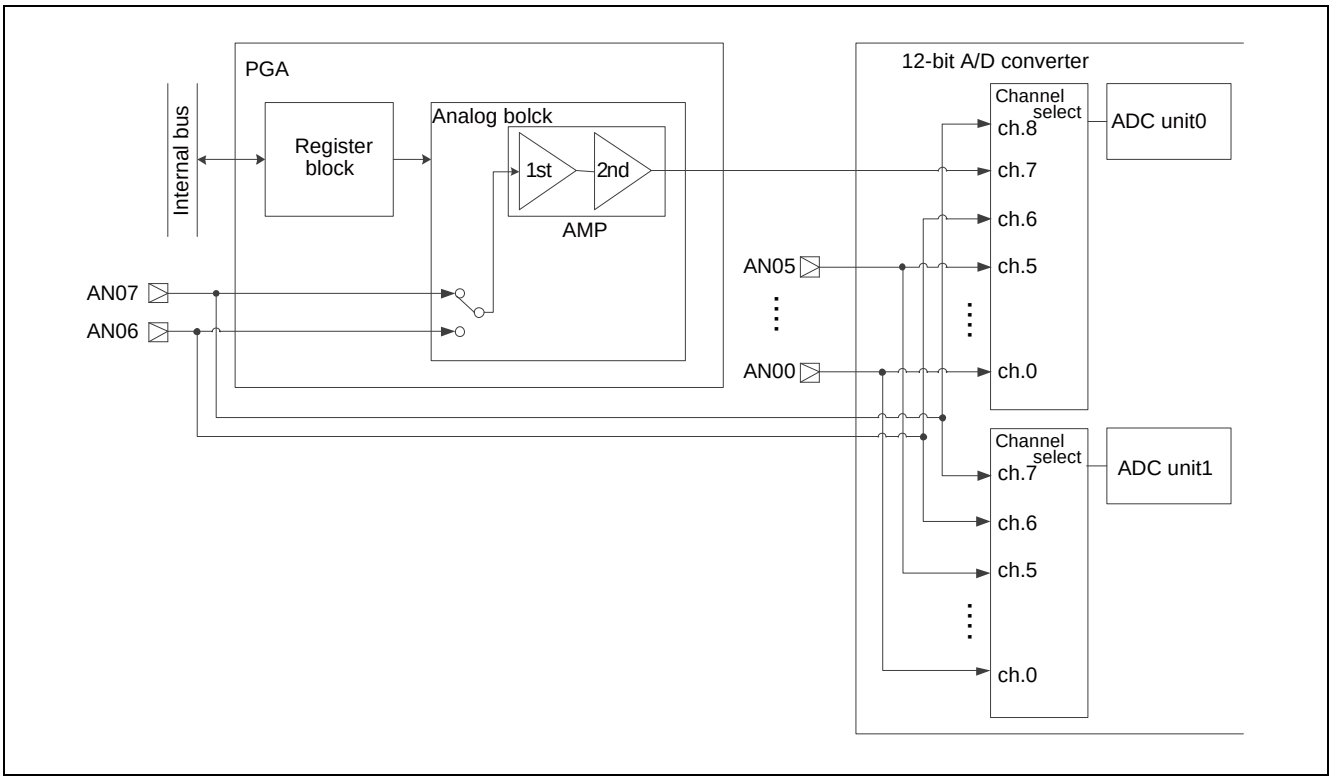
- **Overview**

PGA (Programmable Gain AMP) is the amplifier which amplifies the analog input voltage from external pins, and it outputs to an A/D converter.

- ☐ PGA can amplify programmable from 0 dB to 48 dB.
- ☐ An anti-aliasing filter is carried and cut-off frequency can be chosen from 4 KHz or 8 KHz.
- ☐ One unit of amplifier of 2 channels input selection is carried.

■ Block Diagram

Figure 5.1-1. Block Diagram of PGA



* : For the setup of 12-bit A/D converter, see Chapter "12-bit A/D converter (B)" in "Analog Macro Part".

■ Explanation of each block

☐ Register Block

Register block controls AMP of analog block.
Operation is controlled by the directions to each register from CPU.

☐ Analog Block

An analog block amplifies analog input voltage according to the control set up by the register block. The inside has two-step composition and can amplify the carried amplifier programmable from 0 dB to 48 db.

5.2 I/O Signal of PGA

This section explains connection of the input-and-output signal relevant to PGA.

- **Microcontroller External Pin**
  - ☐ **Analog Input Signal**

    The external input pins of analog signal have connected AN06 and AN07.
- **Internal Connection Pin**
  - ☐ System Clock Signal and Internal Bus Interface

    The internal bus interface of PGA is connected to CPU and memory.
  - ☐ Amplifier Output Signal

    This signal has connected with ch.7 of A/D converter unit0.

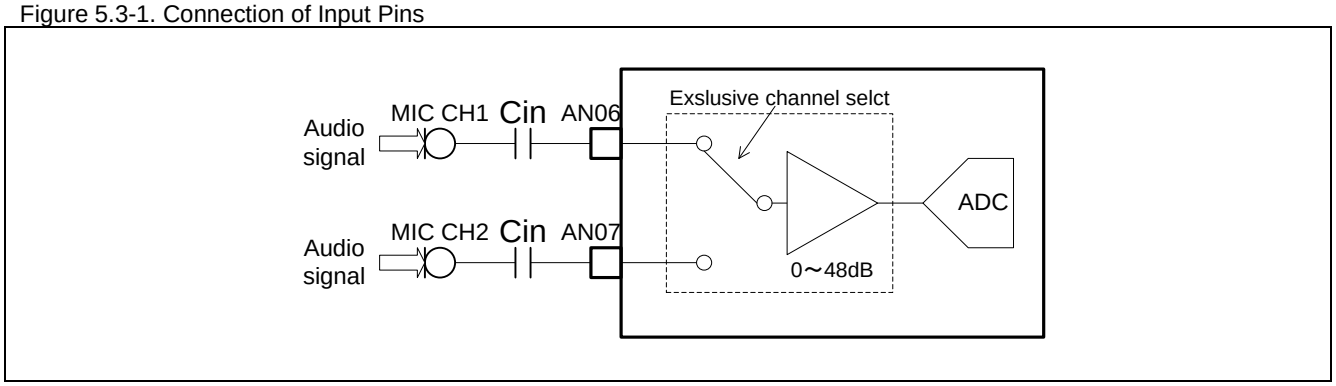
5.3 Method for PGA

This section explains the method for PGA.

- **The Connection Method of Input Pins**

The analog signal from the outside is inputted and carried out through external capacity to be shown in Figure 5.3-1. As for devices, such as external sensor and input pins (AN07, AN06) not connect directly.

Figure 5.3-1. Connection of Input Pins



- **Start-up Procedure**

By power on etc., when reset occurs in an internal bus, carry out the following start-up control.
Before performing an analog input, the following procedures perform start-up of PGA.

1. "1" is written in the PGA_EN bit of an operational mode control register (PGA_EN), and it sets to normal operation mode.
2. Initial setting of PGA (filter selection, channel selection, GAIN setup) is performed, and operation is started.

- **Start-up**

Figure 5.3-2. Circuit operation at the waiting for voltage stability

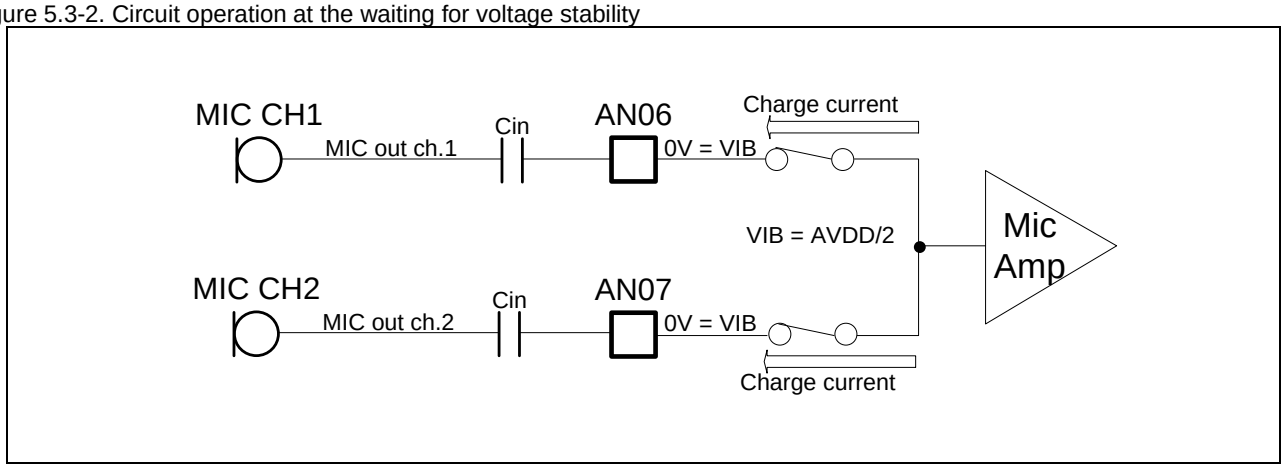
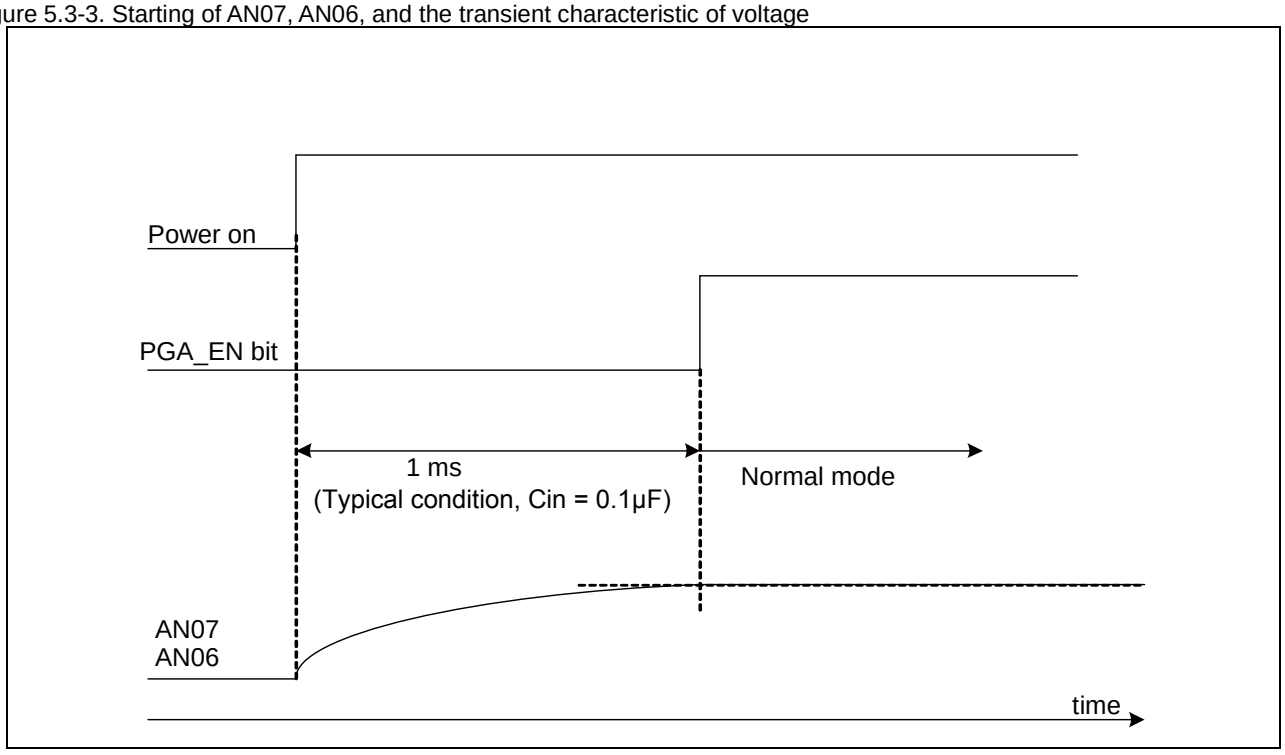


Figure 5.3-3. Starting of AN07, AN06, and the transient characteristic of voltage



The voltage (AN07, AN06) of the node in which capacitive coupling was carried out by Cin is not input bias voltage VIB=AVDD / 2 at normal operation immediately after starting. Therefore, stabilize the voltage of this node before beginning normal operation.

It is Figure 5.3-2 in order to stabilize the voltage of this node in PGA. It charges to an external capacitor (Cin) so that it may be shown.

At a PGA start-up, as shown in Figure 5.3-3, power supply is started, and please stabilizes the voltage of AN07 and AN06 by changing pin state in order of PGA_EN after that.

External capacity (Cin) is set to 1 ms at 0.1 µF time required to stabilize the voltage of AN07 and AN06 at conditions of Typical.

In addition, it is time of the signal to this point being a non-signal that the voltage of AN07 and AN06 is stabilized and it is completed as the voltage of VIB=AVDD/2 in 1.0 ms. The voltage of AN07 and AN06 is subject to the influence of the signal of MIC CH1 and MIC CH2 through Cin like the time of normal operation.

Please make the input to AN07 and AN06 into a non-signal state to be stabilized and start the voltage of AN07 and AN06 within 1 ms.

Moreover, when TOTAL GAIN is as large as 48 dB, few errors of the charged voltage are amplified and it is outputted as big output voltage. It takes about tens ms stably.

- **When only 1 channel is used**

Figure 5.3-4. Voltage stability wait in only 1 channel

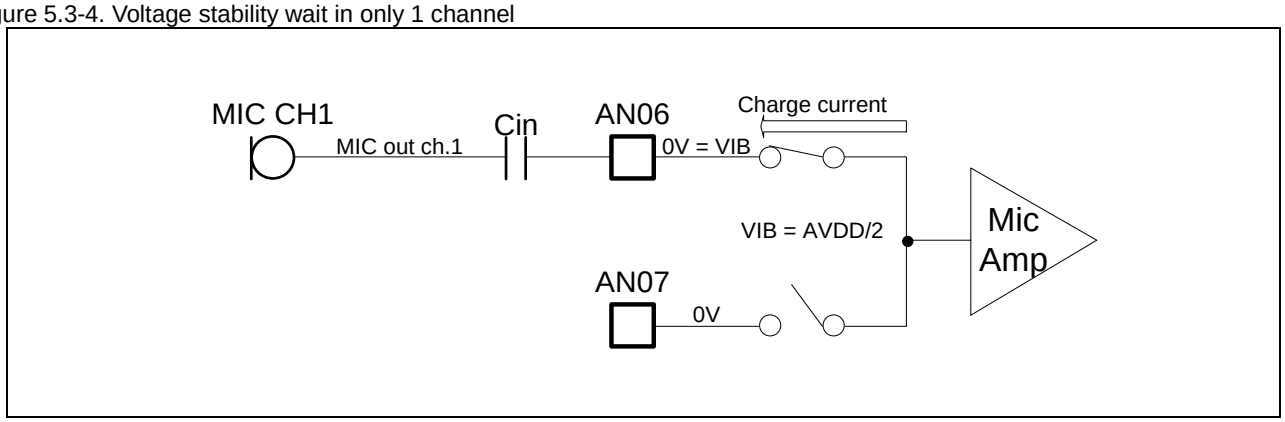


Table 5.3-1. Operation mode in only 1 channel

PGA_EN bit	CHSW bit	AN06 operation mode
1	0	AN06 enable normal operation mode
0	0	Only AN06 voltage stable wait

- ☐ When use only 1 channel of PGA input, input signal into AN06 side.
- ☐ The function to stabilize only the voltage by the side of AN06 for those who use only 1 channel of PGA is carried.
- ☐ When starting PGA according to a start-up procedure, it is Table 5.3-1 in the case of one-channel use. Sets setup of a CHSW bit to "0" to be shown.
- ☐ Input to AN07 pin as an analog signal. When digital signal is inputted, the characteristic of the output signal of microphone amplifier is degraded as noise.

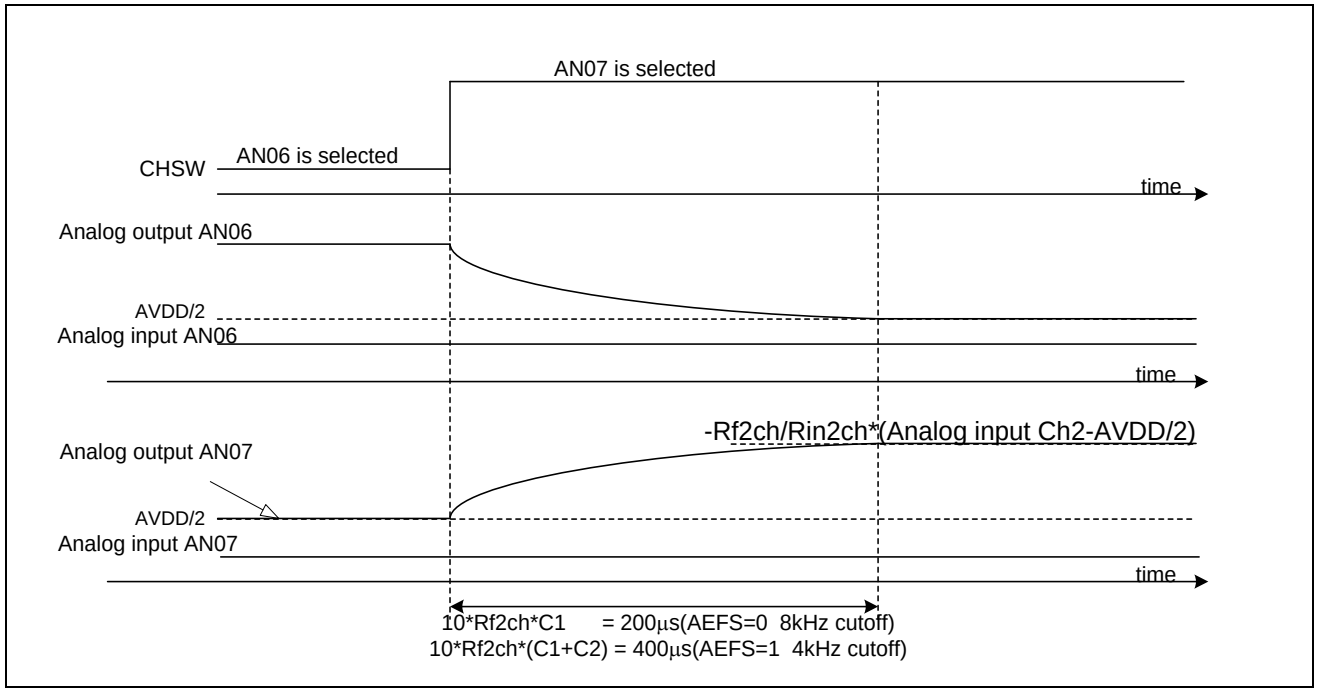
- **Transits to normal operation mode from power-on**

When transits from power-on to normal operation mode, and the signal from microphone is equal to bias voltage, the voltage of input pin is stabilized in the range for few hundreds of µs.

On the other hand, when the signal from a microphone is separated from the bias point, before the voltage of input pin is stabilized, it will take time. Time until it is stabilized takes about few tens ms, when TOTAL GAIN is 48 dB.

- **Notes on Gain and Channel Change Time**

Figure 5.3-5. Channel Change Time



Output voltage when switching channel to AN07 from AN06 is shown in Figure 5.3-5. By the damping time constant of an anti-aliasing filter, constant time is needed for a channel change.

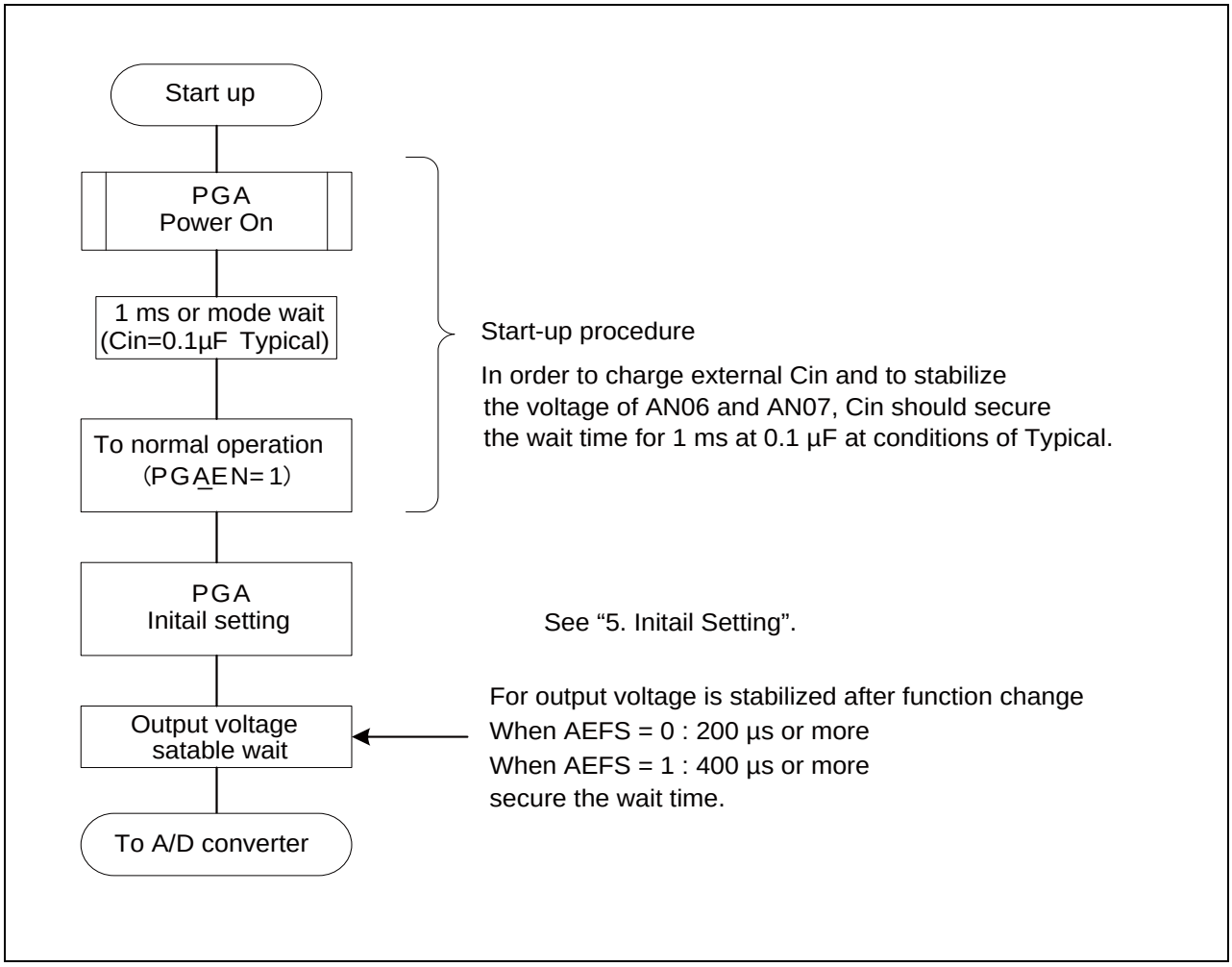
When it is AEFS=0 (the cut-off frequency of a filter is 8 kHz), it has been about 200 μs.

Moreover, after changing function pin also about gain change and power down release, the time same with output voltage being stabilized is needed.

5.4 Setting Procedure of PGA

This section explains the example of procedure until it outputs to an A/D converter from starting of PGA.

Figure 5.4-1. Example Setting Procedure of PGA



5.5 Initial Setting

This section explains Initial setting of PGA.

- **Operation Mode and Channel Change Function**

Table 5.5-1. Operation Mode and Channel Change Function

PGA_EN bit	CHSW bit	Function
1	1	AN07 normal operation mode
1	0	AN06 normal operation mode
0	1	AN06 & AN07 voltage stable wait
0	0	Only AN06 voltage stable wait

- **Gain Setting**

Table 5.5-2. 1st AMP Gain Setting

AMP 1st Stage Gain Setting	1st stage AMP GAIN
GAIN1ST	
0	0dB
1	24dB

Table 5.5-3. 2nd Stage AMP Gain Setting

AMP 2nd Stage Gain Setting			2nd stage AMP GAIN
GAIN2ND[2]	GAIN2ND[1]	GAIN2ND[0]	
0	0	0	0dB
0	0	1	6dB
0	1	0	12dB
0	1	1	18dB
1	X	X	24dB

* : When the 1st stage and the 2nd stage of total gain are used at 24 dB, Use it by setup of GAIN1ST=1 (24 dB) and GAIN2ND="000" (0 dB). When it is used by setup of GAIN1ST=0 (0 dB) and GAIN2ND="1xx" (24 dB), that the gain characteristic deteriorates.

5.6 PGA Registers

This section explains register of PGA.

Table 5.6-1 shows list of PGA register.

Table 5.6-1. List of PGA Register

Abbreviation	Register name	Reference
PGA_EN	Operation Mode Control Register	
AEFS	Anti-Aliasing Filter Select Register	5.6.2
CHSW	AMP Channel Select Register	5.6.3
GAIN	Gain Adjustment Setting Register	5.6.4

5.6.1 Operation Mode Control Register (PGA_EN)

Operation Mode Control Register (PGA_EN) controls voltage stable wait/normal operation mode of PGA.

bit	7	6	5	4	3	2	1	0
Field	Reserved							PGA_EN
Attribute	R							R/W
Initial value	0000000							0

[bit7:1] Reserved : Reserved bits

Read out "0". Writing has no effect on operation.

[bit0] PGA_EN : PGA operation mode control bit

This bit selects voltage stable wait/normal operation mode.

bit	Operation
0	Voltage stable wait [Initial value]
1	Normal operation mode
When writing	Read the register-setting value.

5.6.2 Anti-Aliasing Filter Select Register (AEFS)

Anti-Aliasing Filter Select Register (AEFS) selects ant aliasing filter.

bit	7	6	5	4	3	2	1	0
Field	Reserved							AEFS
Attribute	R							R/W
Initial value	0000000							0

[bit7:1] Reserved : Reserved bits

Read out "0". Writing has no effect on operation.

[bit0] AEFS : Anti-Aliasing filter select bit

This bit selects anti-aliasing filter.

bit	Operation
0	Maximum of 8 kHz input filter is used. [Initial value]
1	Maximum of 4 kHz input filter is used.
When writing	Read the register-setting value.

5.6.3 AMP Channel Select Register (CHSW)

AMP Channel Select Register (CHSW) selects AMP channel of PGA.

bit	7	6	5	4	3	2	1	0
Field	Reserved							CHSW
Attribute				R				R/W
Initial value				0000000				0

[bit7:1] Reserved : Reserved bits

Read out "0". Writing has no effect on operation.

[bit0] CHSW : AMP selection bit

This bit selects AMP channel.

bit	Operation
0	Use AN06 channel [Initial value]
1	Use AN07 channel
When writing	Read the register-setting value.

5.6.4 Gain Adjustment Setting Register (GAIN)

Gain Adjustment Setting Register (GAIN) sets gain adjustment of PGA.

bit	15	14	13	12	11	10	9	8
Field	Reserved					GAIN2ND[2:0]		
Attribute			R			R/W		
Initial value			00000			000		

bit	7	6	5	4	3	2	1	0
Field	Reserved							GAIN1ST
Attribute				R				R/W
Initial value				0000000				0

[bit15:11] Reserved : Reserved bits

Read out "0". Writing has no effect on operation.

[bit10:8] GAIN2ND[2:0]

This bit sets 2nd AMP Gain.

bit10	bit9	bit8	Operation
0	0	0	0dB [Initial value]
0	0	1	6dB
0	1	0	12dB
0	1	1	18dB
1	X	X	24dB
When writing: Read the register-setting value.			

[bit7:1] Reserved : Reserved bits

Read out "0". Writing has no effect on operation.

[bit0] GAIN1ST

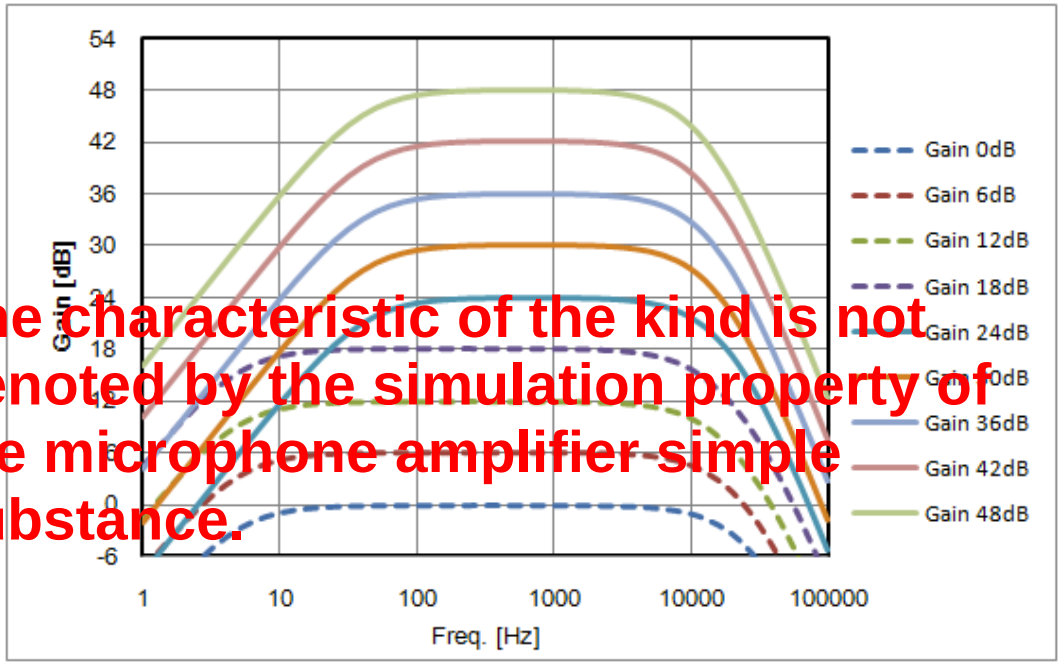
This bit sets 1st AMP Gain.

bit	Operation
0	0dB [Initial value]
1	24dB
When writing	Read the register-setting value.

5.7 PGA Characteristic

This section explains characteristic of PGA.

Figure 5.7-1. Example of e frequency characteristic (AEFS=0, Cin=0.1µF)



The characteristic of the kind is not denoted by the simulation property of the microphone amplifier simple substance.

Figure 5.7-1 shows the gain of PGA and the relation of frequency. PGA can set up a gain at intervals of 6 dB from 0 dB to 48 dB. The frequency band which realizes the set-up gain is 100 Hz to 8 kHz (When AEFS=0).

PGA is designing the filter by composition of simple RC, and a frequency band determines it by the time constant of the RC. therefore, Figure 5.7-1 shown the gain by which the signal near the lowest frequency (100 Hz) of a pass band and the highest frequency (8 kHz) is realized rather than the gain to which RC filter is set inevitably becomes small.

The position of the zero point of the high pass filter characteristic by the side of low frequency wave is influenced by the value of the external capacity Cin used. The time constant of RC the reason has decided the zero point to be is the input impedance of the external capacity Cin and microphone amplifier. Therefore, the zone by the side of low frequency wave can be further made low by enlarging capacity value of Cin. However, enlarging capacity value of Cin makes voltage stable waiting time increase.

Figure 5.7-2. Example of frequency characteristic when AEFS is switched. (Cin=0.1µF)

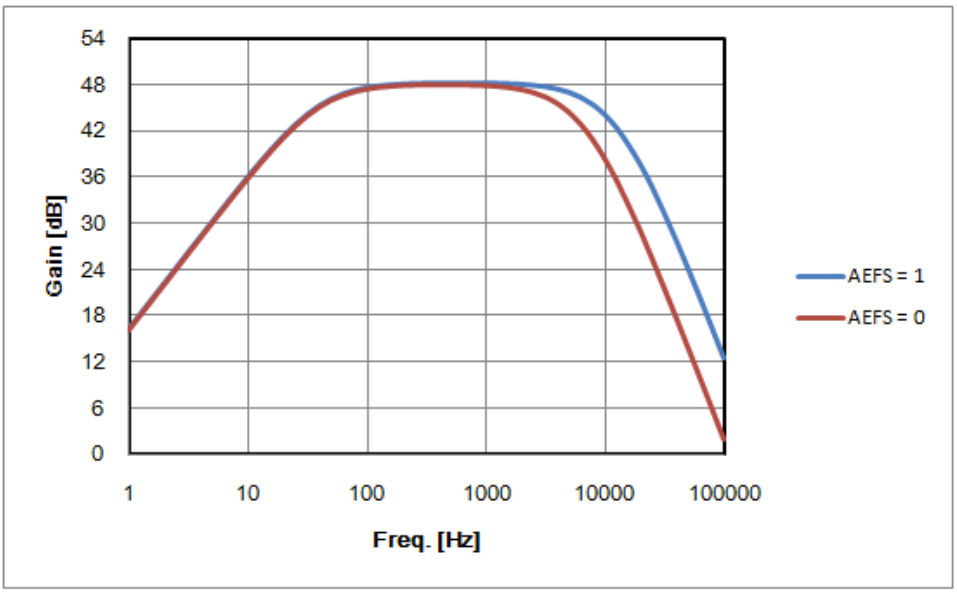


Figure 5.7-2 shows the frequency characteristic of a gain when AEFS is switched. PGA can change the damping time constant of the cut-off frequency of the maximum frequency of a gain by AEFS setup.

Although the cut-off frequency of the maximum frequency is near 8 kHz at AEFS=0, at AEFS=1, cut-off frequency serves as near 4 kHz, and reduces the gain of a high-frequency signal more.

6. Overview of CSIO (Clock Synchronous Serial Interface)

This chapter explains the Clock Synchronous Serial Interface (CSIO) function that is supported in Operation mode 2. This CSIO is a part of the multifunction serial interface functions.

6.1 Overview of CSIO (Clock Synchronous Serial Interface)

6.2 CSIO (Clock Synchronous Serial Interface) interrupts

6.3 CSIO (Clock Synchronous Serial Interface) operations

6.4 Operation of Serial Chip Select

6.5 Dedicated baud rate generator

6.6 CSIO (Clock Synchronous Serial Interface) registers

6.1 Overview of CSIO (Clock Synchronous Serial Interface)

The CSIO is a general-purpose serial data communication interface (supporting the SPI) to allow synchronous communication with an external device.

- **CSIO (Clock Synchronous Serial Interface) functions**

		Function
1	Data buffer	Full duplex double buffer
2	Transfer system	Clock synchronization (without start/stop bit) Master/slave function SPI supported (for both master and slave modes)
3	Baud rate	Dedicate baud rate generator provided (configured with a 15-bit reload counter; in master mode operation) An external clock can be entered (in the slave mode operation).
4	Data length	Variable from 5 bits to 9 bits
5	Received error detection	Overrun error
6	Interrupt request	Received interrupt (a received completion, an overrun error) Transmit interrupt (a transmit data empty, a transmit bus idle) DMA(Transmit/Received) transferring support function are available.
7	Serial chip select	4 ch control (Single control and round control) Setup to variable is possible in setup / hold / de-select time. Active level selection by each channel is possible
8	Synchronous mode	Master or slave function
9	Pin access	The serial data output pin can be set to "1".

6.2 CSIO (Clock Synchronous Serial Interface) interrupts

The CSIO interrupts contain the received interrupt and the transmit interrupt. These interrupt requests can be generated if:

- A received data is set in the Received Data Register (RDR) or a data received error occurs.
- A transmit data is transferred from the Transmit Data Register (TDR) to the transmit shift register and the data transmission is started
- The transmit bus is idle (No data transmission occurs).
- Chip select error occurs

- **CSIO interrupts**

Table 6.2-1 shows the CSIO interrupt control bits and the interrupt factors.

Table 6.2-1. CSIO interrupt control bits and interrupt factors

Interrupt type	Interrupt request flag bit	Flag register	Interrupt factor	Interrupt factor enable bit	Operation to clear interrupt request flag
Reception	RDRF	SSR	A single-byte reception	SCR:RIE	Reading from the received data register (RDR)
	ORE	SSR	Overrun error		Setting the Received Error Flag Clear bit (SSR:REC) to "1"
Transmission	TDRE	SSR	The Transmit Data Register is empty.	SCR:TIE	Writing to the Transmit Data Register (TDR) *
	TBI	SSR	No data transmission	SCR:TBIE	Writing to the Transmit Data Register (TDR) *
	CSE	SACSR	When slave mode(SCR:MS=1), the following transmission data is not written the serial chip select pin in for the number of transmission below with the preset value of TBYTE during transmitting operation at TDR at inactive master mode (SCR:MS=0). (SSR:TDRE=1)	SACSR:CSEIE	Setting the Serial Chip Select Flag bit (SACSR:CSE) to "1"

*1 : Set the TIE bit to "1" only after the TDRE bit has been set to "0".

6.2.1 Received interrupt and flag set timing

Data reception can be interrupted by a Received Completion (SSR:RDRF=1) or a Received Error Occurrence (SSR:ORE=1).

- **Received interrupt and flag set timing**

When the last data bit is detected, the received data is stored in the Received Data Register (RDR). When the data reception is completed (SSR:RDRF=1) or when a data received error occurs (SSR:ORE=1), each flag is set. If a received interrupt is enabled (SCR:RIE=1) during this time, a received interrupt occurs.

Note

If a received error occurs, data in the Received Data Register (RDR) is invalidated.

Figure 6.2-1. Data receiving and flag set timing

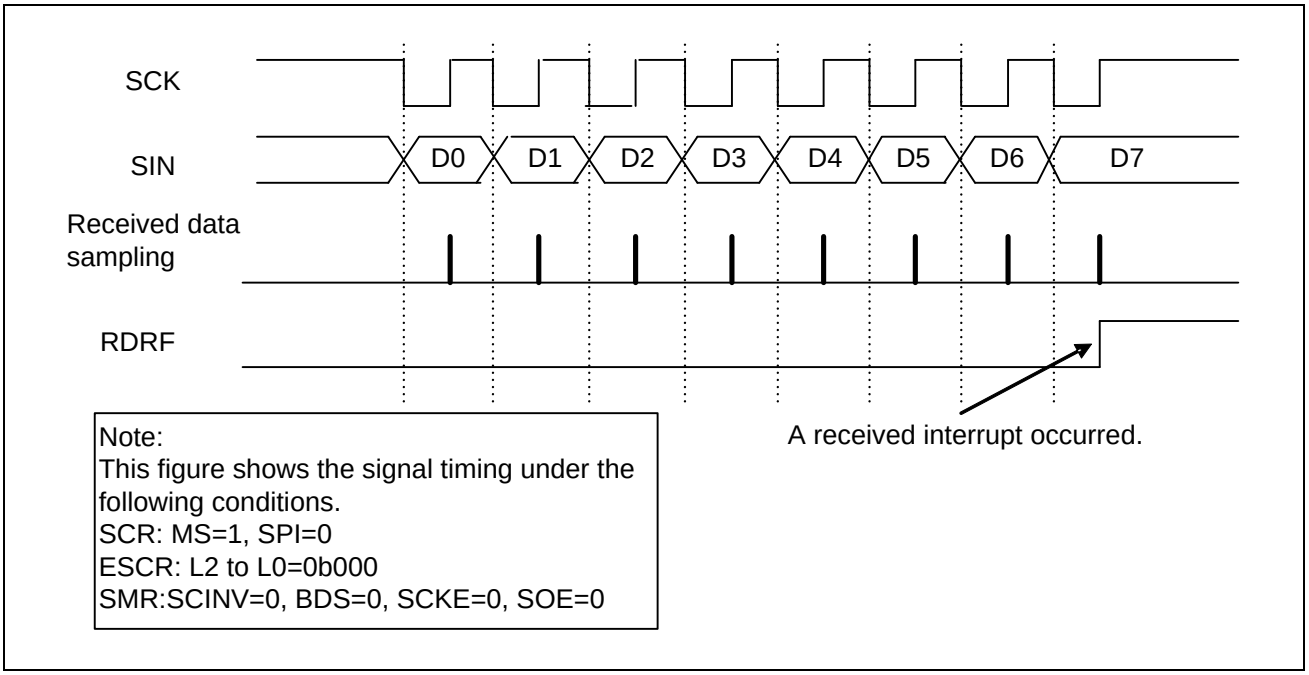
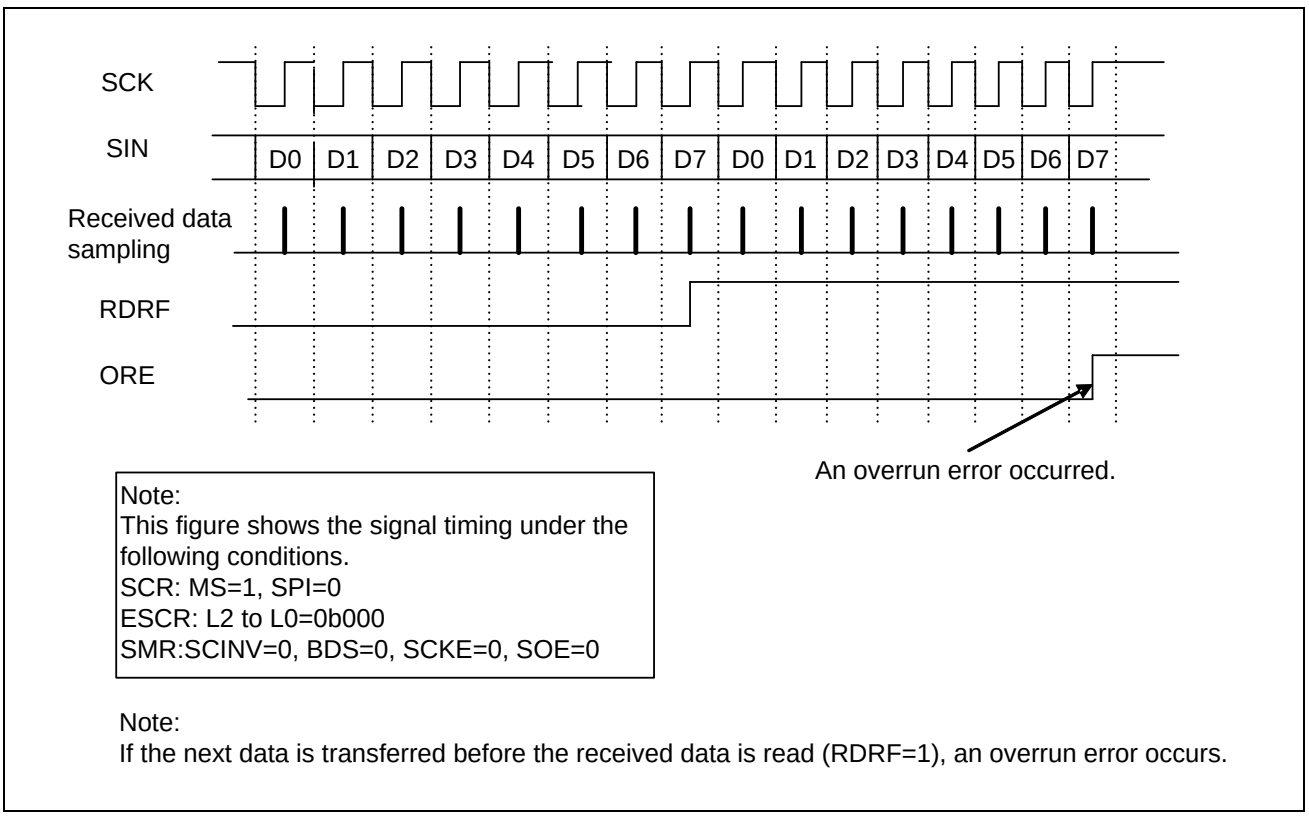


Figure 6.2-2. ORE (Overrun Error) flag set timing



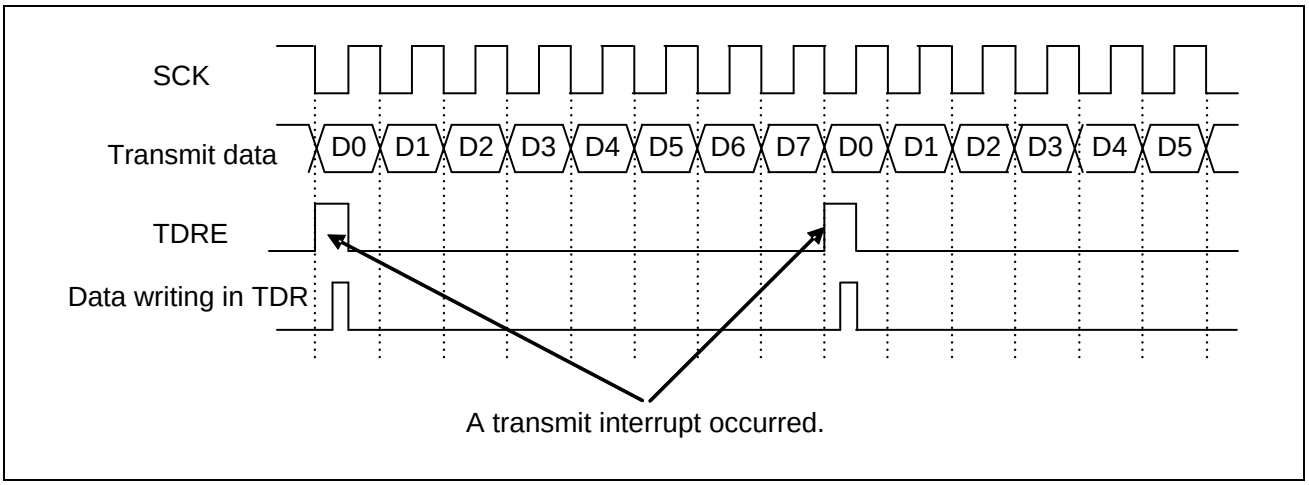
6.2.2 Transmit interrupt and flag set timing

A transmit interrupt occurs if transmit data is transferred from the Transmit Data Register (TDR) to the transmit shift register (SSR:TDRE=1) and the data transmission is started, or if no data is transmitted (SSR:TBI=1).

- **Transmit interrupt and flag set timing**
  - **Transmit data empty flag (SSR:TDRE) set timing**

After data has been transferred from the Transmit Data Register (TDR) to the transmit shift register, the next data can be written in the TDR (SSR:TDRE=1). If a transmit interrupt is enabled (SCR:TIE=1) during this time, a transmit interrupt occurs. As the SSR:TDRE bit is read only, the SSR:TDRE bit is cleared to "0" when data is written to the Transmit Data Register (TDR).

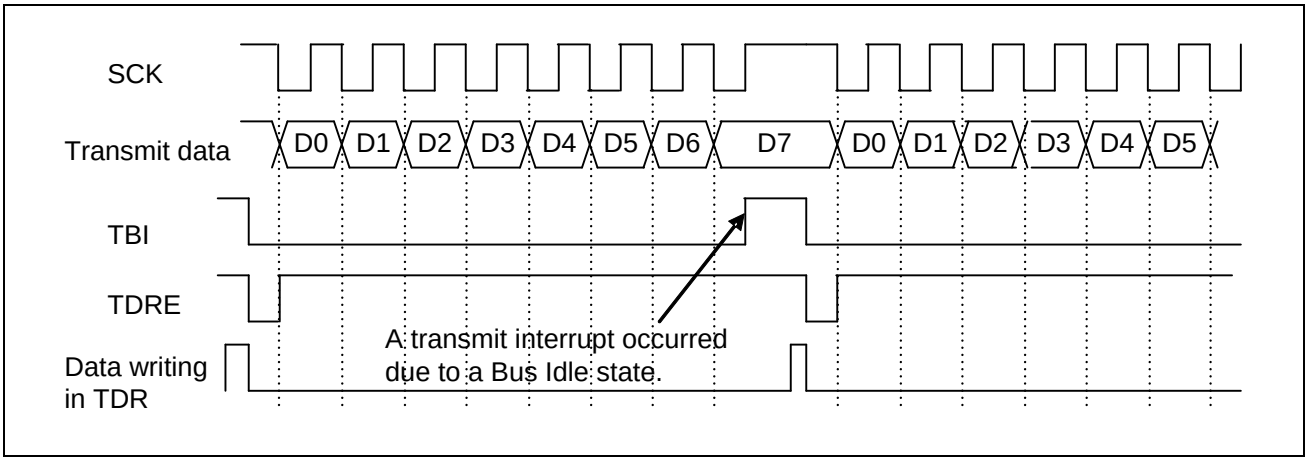
Figure 6.2-3. Transmit data empty flag (SSR:TDRE) set timing



  - **Transmit bus idle flag (SSR:TBI) set timing**

If the Transmit Data Register is empty (SSR:TDRE=1) and no data is transmitted, the SSR:TBI bit is set to "1". If a transmit bus idle interrupt is enabled (SCR:TBIE=1) during this time, a transmit interrupt occurs. When transmit data is written to the Transmit Data Register (TDR), both the SSR:TBI bit and the transmit interrupt request are cleared.

Figure 6.2-4. Transmit bus idle flag (TBI) set timing



6.2.3 Chip Select Error occurs and Timing of Flag set

The chip select error occurs, when only the number of frames smaller than the setting value of TBYTE has transmitted at master mode (SCR:MS=0), and there is no data effective in transmit data register (TDR) after one-frame transmission (SSR:TDRE=1). Moreover, if serial chip select pin becomes inactive during transmitting operation of slave mode (SCR:MS=1), chip select error will occur.

- **Chip Select Error occurs and Timing of Flag set**

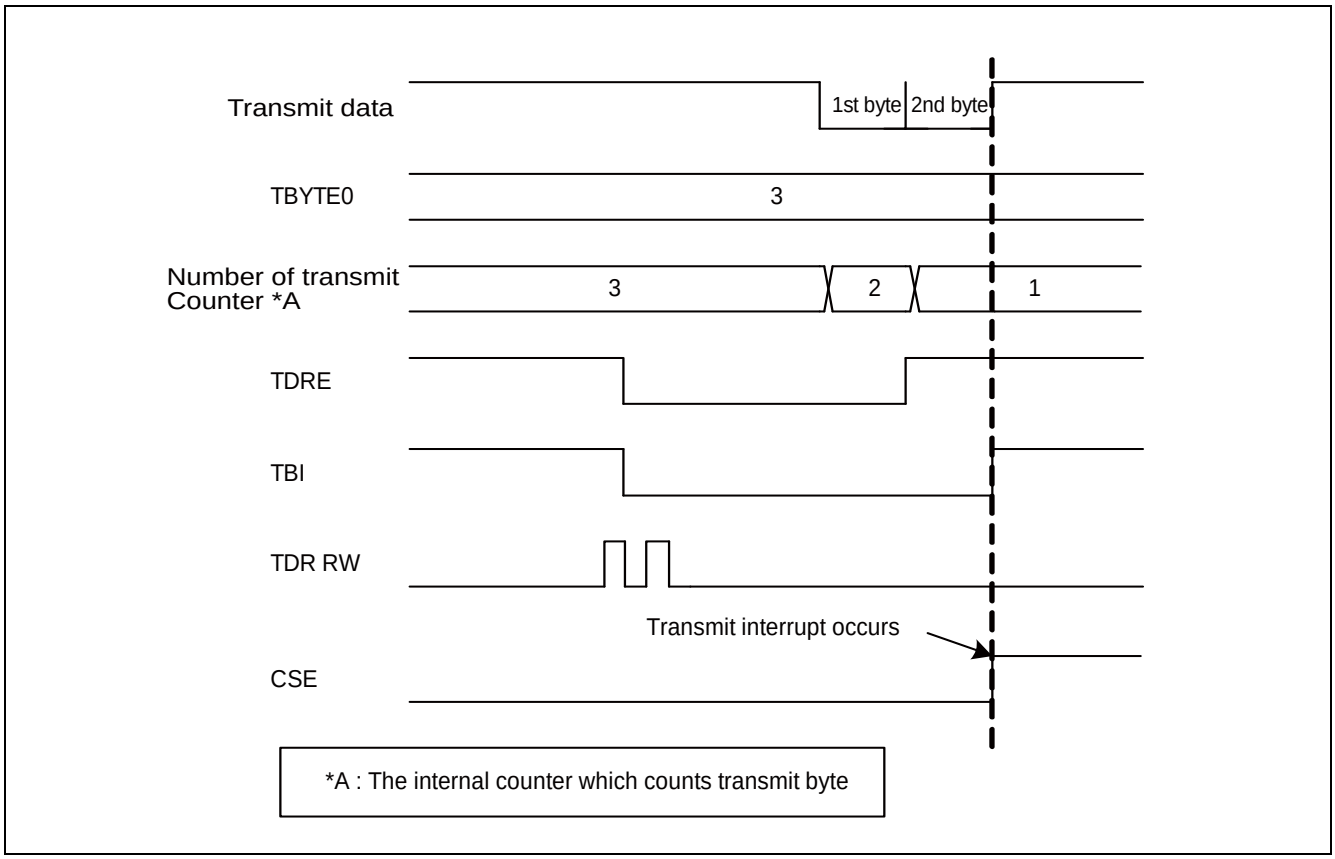
  ☐ Master mode (SCR:MS=0)

  The chip select error occurs, when there is no transmit data effective (SSR:TDRE=1) in Transmit Data Register (TDR) before transmitting the data frame of the setting value of TBYTE by transmission byte error enable (TBEEN=1) at following either.

  - When chip select is used
  - When transmitting starting by an external trigger is used

In this case, if chip select error interrupt enable (SACSR:CSEIE=1) is set, a transmit interrupt will occur.

Figure 6.2-5. Timing of Chip Select Error Occur



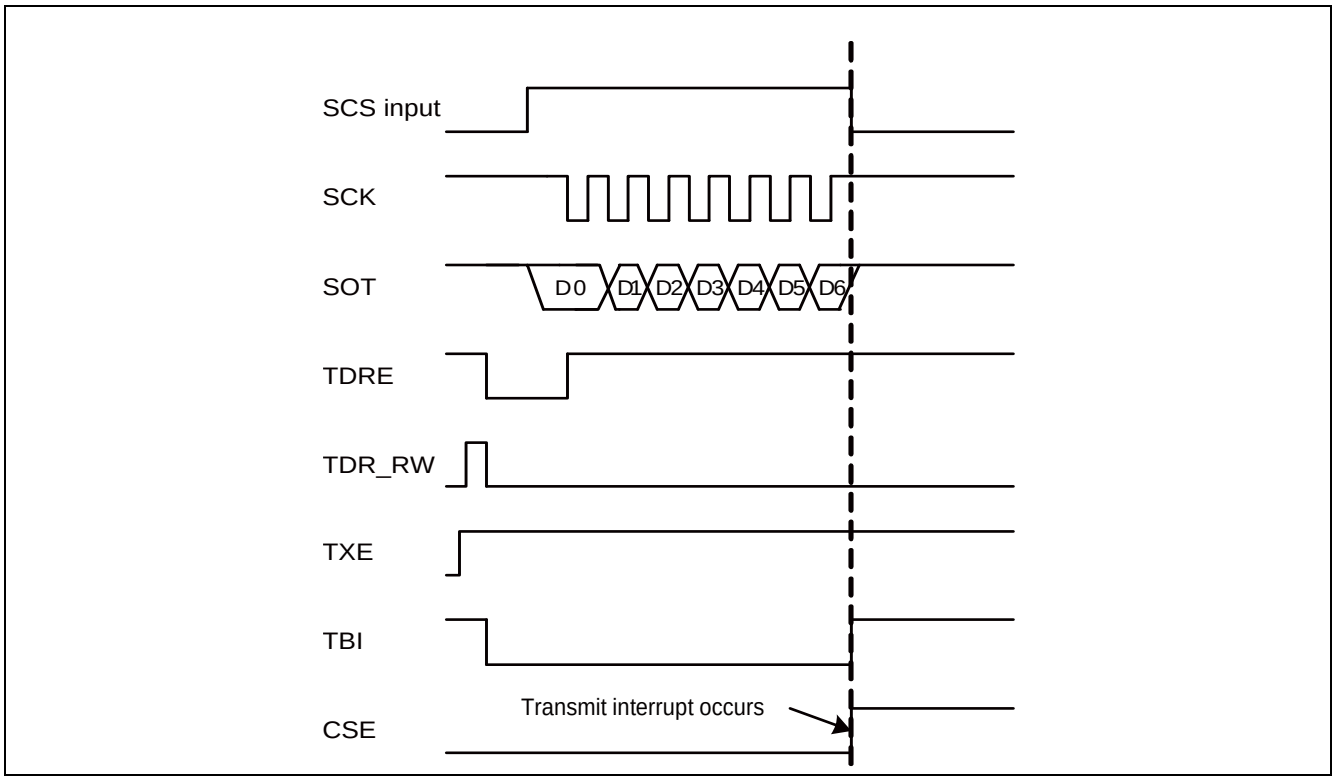
Notes

- The chip select error flag (SACSR:CSE) is set as "1" after deselect time progress after chip select error generating at serial chip select use. Moreover, although a transmitting data register (TDR) writes in transmit data during hold delay time, transmit operation is not started, but chip select error flag (SACSR:CSE) is set as "1" after deselect time progress.
- When "1" is set to the chip select error flag (SACSR:CSE), transmit operation is not started although transmit data is written in a Transmit Data Register (TDR).

☐ **Slave mode (SCR:MS=1)**

The chip select error will occur, if serial chip select pin becomes inactive during transmit operation (SSR:TBI=0). In this case, if the chip select error interrupt enable (SACSR:CSEIE=1) is set, transmit interrupt will occur.

Figure 6.2-6. Timing of Chip Select Error Occur



6.3 CSIO (Clock Synchronous Serial Interface) operations

The clock synchronous data transfer is used.

6.3.1 Normal transfer (I)

■ **Features**

	Item	Description
1	Serial clock (SCK) signal mark level	"HIGH"
2	Transmit data output timing	SCK signal falling edge
3	Received data sampling	SCK signal rising edge
4	Data length	5 to 9 bits

■ **Register settings**

The register values required for normal transfer (I) is shown below.

SCR:SPI(*1)=0, SMR:MD2= 0, MD1=1, MD0=0, and SCINV(*1)=0
When master operation : SCR:MS=0 and SMR:SCKE=1
When slave operation : SCR:MS=1 and SMR:SCKE=0

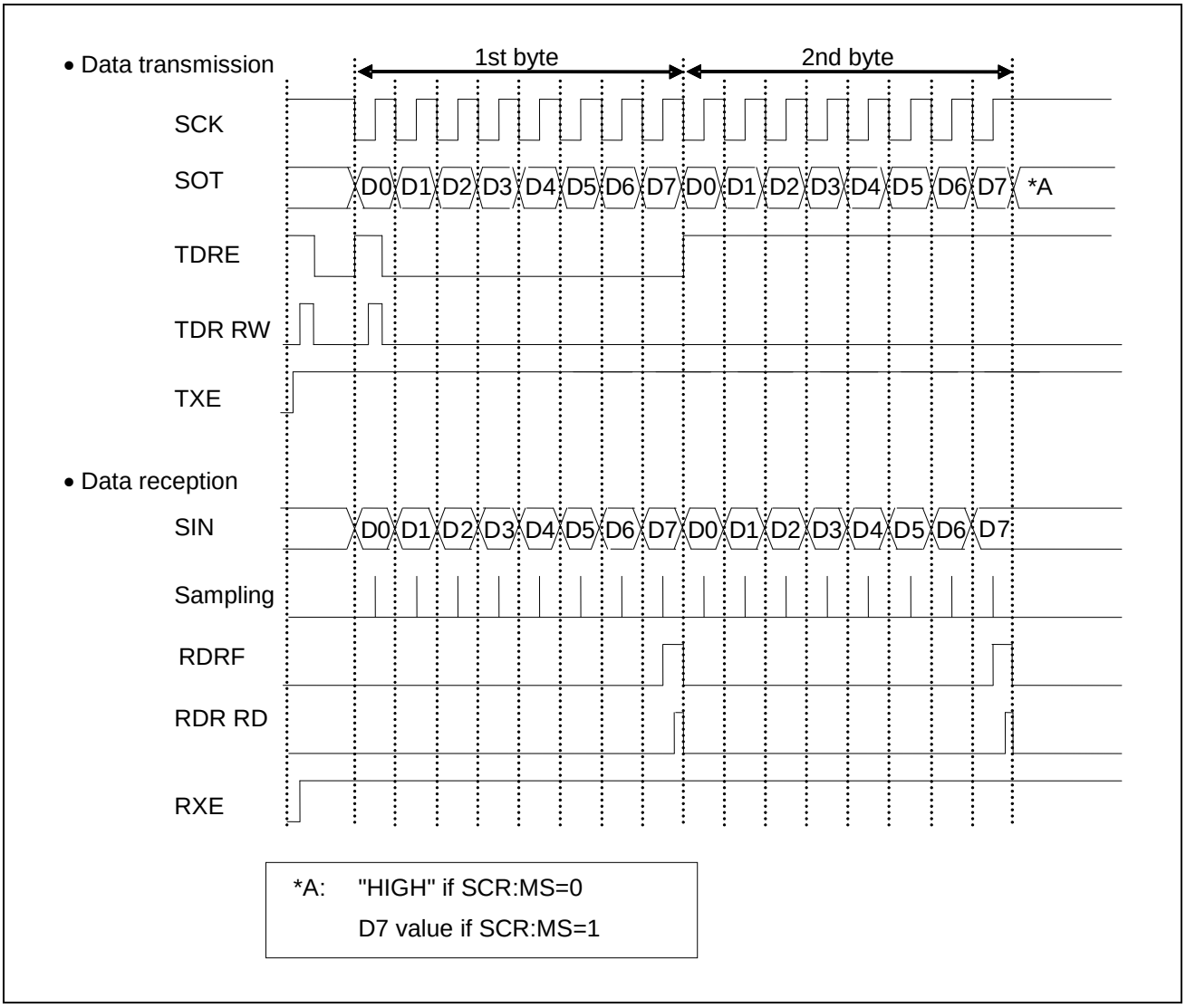
(*1) The bits set up according to conditions differ. See Table 6.4-2.

Note

Set up registers other than the above-mentioned bit according to directions for use.

■ **Normal transfer (I) timing chart (When Serial Chip Select Pin is unused.)**

Figure 6.3-1. Timing chart of normal transfer



- **Master mode operation (SCR:MS=0, SMR:SCKE=1, SCSCR:CSEN[3:0]=”0b0000”)**

  - **Data transmission**

  1. If serial data output is enabled (SMR:SOE=1), data transmission is enabled (SCR:TXE=1) and data reception is disabled (SCR:RXE=0), and when the transmit data is written in the TDR, the SSR:TDRE bit is set to "0". This causes the transmit data to be output in synchronization with a falling edge of the serial clock (SCK) output.
  2. When the transmit data of the first bit is output, the SSR:TDRE bit is set to "1". Therefore, if the transmit interrupt is enabled (SCR:TIE=1), a transmit interrupt request is output. During this time, the transmit data of the 2nd byte can be written in the register.

  - **Data reception**

  1. If the serial data output is disabled (SMR:SOE=0), data transmission is enabled (SCR:TXE=1) and data reception is enabled (SCR:RXE=1), and when a dummy data is written in the TDR, the received data is sampled at a rising edge of serial clock (SCK) output.
  2. When the last bit is received, the SSR:RDRF bit is set to "1". If a received interrupt is enabled (SCR:RIE=1) during this time, a received interrupt request is output. The received data (RDR) can be read during this time.
  3. When the received data (RDR) is read, the SSR:RDRF bit is cleared to "0".

Note

To perform data reception only, write a dummy data in the TDR so that the serial clock (SCK) is output.

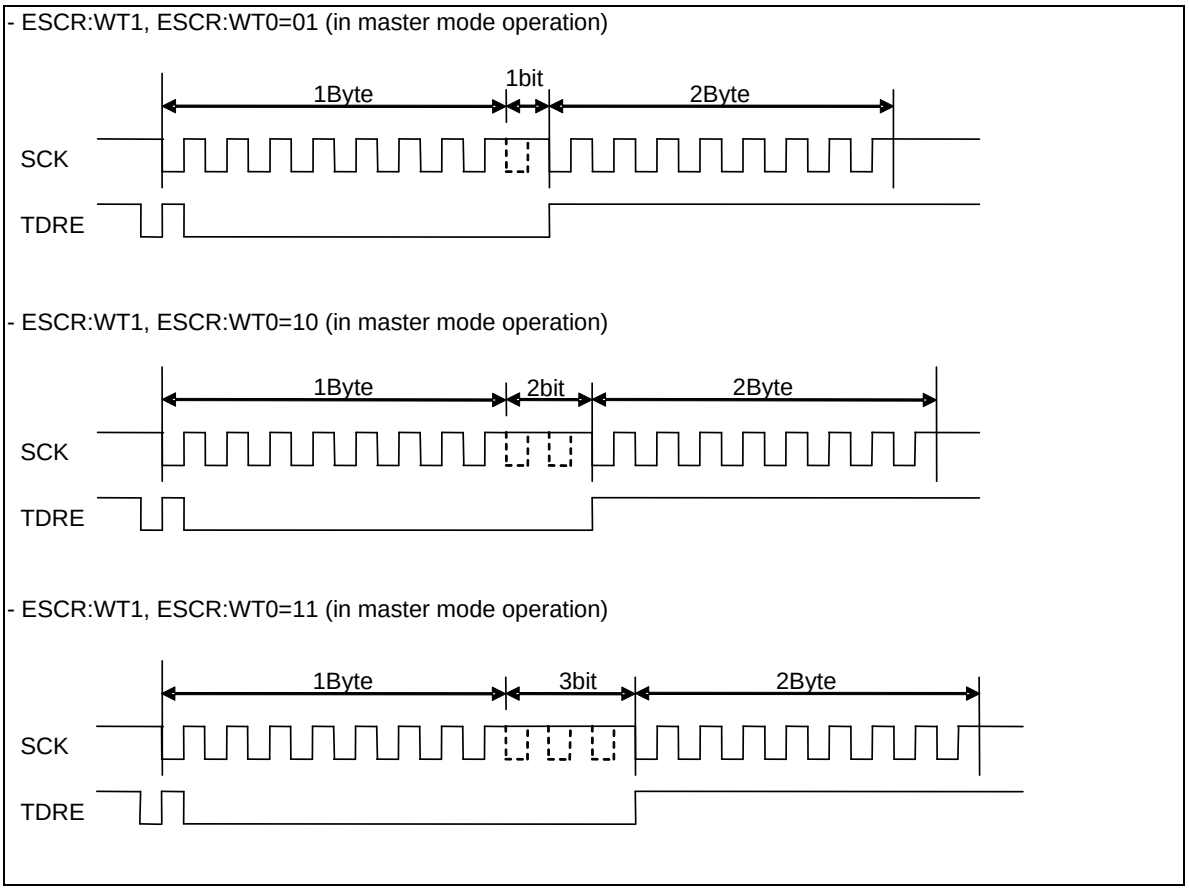
  - **Data transmission and reception**

  1. To perform data transmission and reception simultaneously, enable the serial data output (SMR:SOE=1) and enable the data transmission and reception (SCR:TXE, RXE=1).
  2. When the transmit data is written in the TDR, the SSR:TDRE bit is set to "0" and the transmit data is output in synchronization with a falling edge of the serial clock (SCK) output. When the transmit data of the first bit is output, the SSR:TDRE bit is set to "1". If a transmit interrupt is enabled (SCR:TIE=1), a transmit interrupt request is output. During this time, the transmit data of the 2nd byte can be written in the register.
  3. The received data is sampled at a rising edge of the serial clock (SCK) output. When the last bit of received data is received, the SSR:RDRF bit is set to "1". If a received interrupt is enabled (SCR:RIE=1), a received interrupt request is output. The received data (RDR) can be read during this time. When the received data is read, the SSR:RDRF bit is cleared to "0".

☐ **Continuous data transmit or reception waiting**

If anything other than ESCR:WT1, ESCR:WT0=00 is set for the continuous data transmission or reception, a wait is inserted between frames.

Figure 6.3-2. Continuous data transmit or reception waiting



■ **Slave mode operation (SCR:MS=1, SMR:SCKE=0, SCSCR:CSEN0=0)**

☐ **Data transmission**

1. If serial data output is enabled (SMR:SOE=1) and data transmission is enabled (SCR:TXE=1) and when the transmit data is written in the TDR, the SSR:TDRE bit is set to "0". This causes the transmit data to be output in synchronization with a falling edge of the serial clock (SCK) input.
2. When the transmit data of the first bit is output, the SSR:TDRE bit is set to "1". If a transmit interrupt is enabled (SCR:TIE=1), a transmit interrupt request is output. During this time, the transmit data of the 2nd byte can be written in the register.

☐ **Data reception**

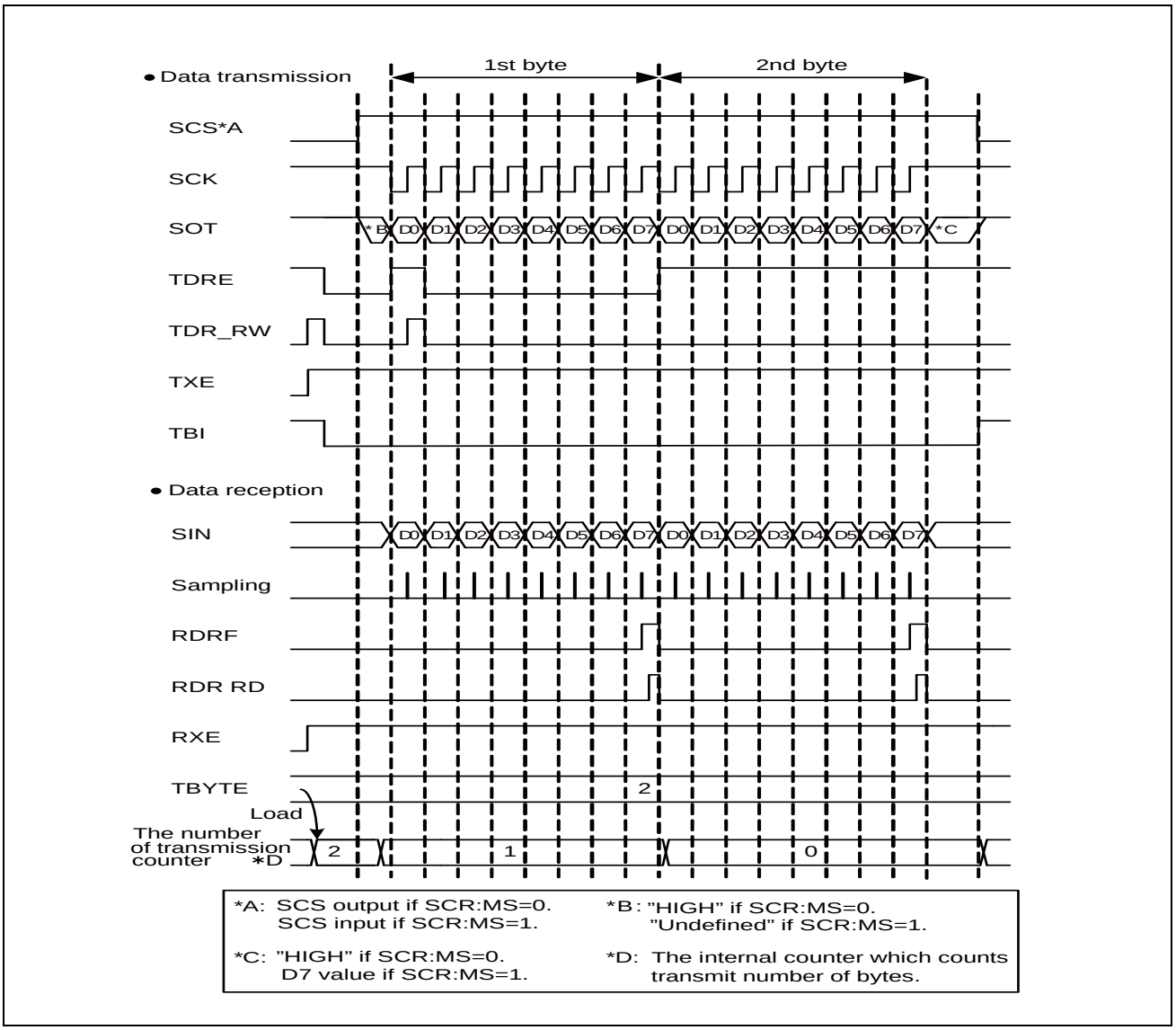
1. If the serial data output is disabled (SMR:SOE=0) and data reception is enabled (SCR:RXE=1), the received data is sampled at a rising edge of serial clock (SCK) input.
2. When the last bit is received, the SSR:RDRF bit is set to "1". If a received interrupt is enabled (SCR:RIE=1), a received interrupt request is output.
   The received data (RDR) can be read during this time.
3. When the received data (RDR) is read, the SSR:RDRF bit is cleared to "0".

☐ **Data transmission and reception**

1. To perform data transmission and reception simultaneously, enable the serial data output (SMR:SOE=1) and enable the data transmission and reception (SCR:TXE, RXE=1).
2. When the transmit data is written in the TDR, the SSR:TDRE bit is set to "0" and the transmit data is output in synchronization with a falling edge of the serial clock (SCK) input. When the transmit data of the first bit is output, the SSR:TDRE bit is set to "1". If a transmit interrupt is enabled (SCR:TIE=1), a transmit interrupt request is output. During this time, the transmit data of the 2nd byte can be written in the register.
3. The received data is sampled at a rising edge of the serial clock (SCK) input. When the last bit of received data is received, the SSR:RDRF bit is set to "1". If the received interrupt is enabled (SCR:RIE=1), a received interrupt request is output. The received data (RDR) can be read during this time. When the received data is read, the SSR:RDRF bit is cleared to "0".

■ **Normal transfer (I) timing chart (When Serial Chip Select Pin is used.)**

Figure 6.3-3. Timing chart of normal transfer



■ **Master mode operation (SCR:MS=0, SMR:SCKE=1, SCSCR:CSOE=1, SCSCR:CSENn*=1)**

* : The serial chip select pin number to be used into n.

☐ **Data transmission**

1. If serial data output is enabled (SMR:SOE=1), data transmission is enabled (SCR:TXE=1) and data reception is disabled (SCR:RXE=0), and when the transmit data is written in the TDR, the SSR:TDRE bit is set to "0". This causes the transmit data to be output in synchronization with a falling edge of the serial clock (SCK) output.
2. When the transmit data of the first bit is output, the SSR:TDRE bit is set to "1". Therefore, if the transmit interrupt is enabled (SCR:TIE=1), a transmit interrupt request is output. During this time, the transmit data of the 2nd byte can be written in the register.
3. Transmission operation is completed after the end of data transmitting of the setting number by TBYTE.
4. After ending transmit operation, a serial chip select pin (SCS) becomes inactive after hold time progress of serial chip select pin. However, when the serial chip select active level (SCSCR:SCAM=1) is kept at this time, serial chip select pin (SCS) holds an active state.

☐ **Data reception**

1. If the serial data output is disabled (SMR:SOE=0), data transmission is enabled (SCR:TXE=1) and data reception is enabled (SCR:RXE=1), and when a dummy data is written in the TDR, the received data is sampled at a rising edge of serial clock (SCK) output.
2. When the last bit is received, the SSR:RDRF bit is set to "1". If a received interrupt is enabled (SCR:RIE=1) during this time, a received interrupt request is output.
   The received data (RDR) can be read during this time.
3. When the received data (RDR) is read, the SSR:RDRF bit is cleared to "0".
4. Reception operation is completed after the end of data receiving of the setting number by TBYTE.
5. After ending reception operation, a serial chip select pin (SCS) becomes inactive after hold time progress of serial chip select pin. However, when the serial chip select active level (SCSCR:SCAM=1) is kept at this time, serial chip select pin (SCS) holds an active state.

Note

To perform data reception only, write a dummy data in the TDR so that the serial clock (SCK) is output.

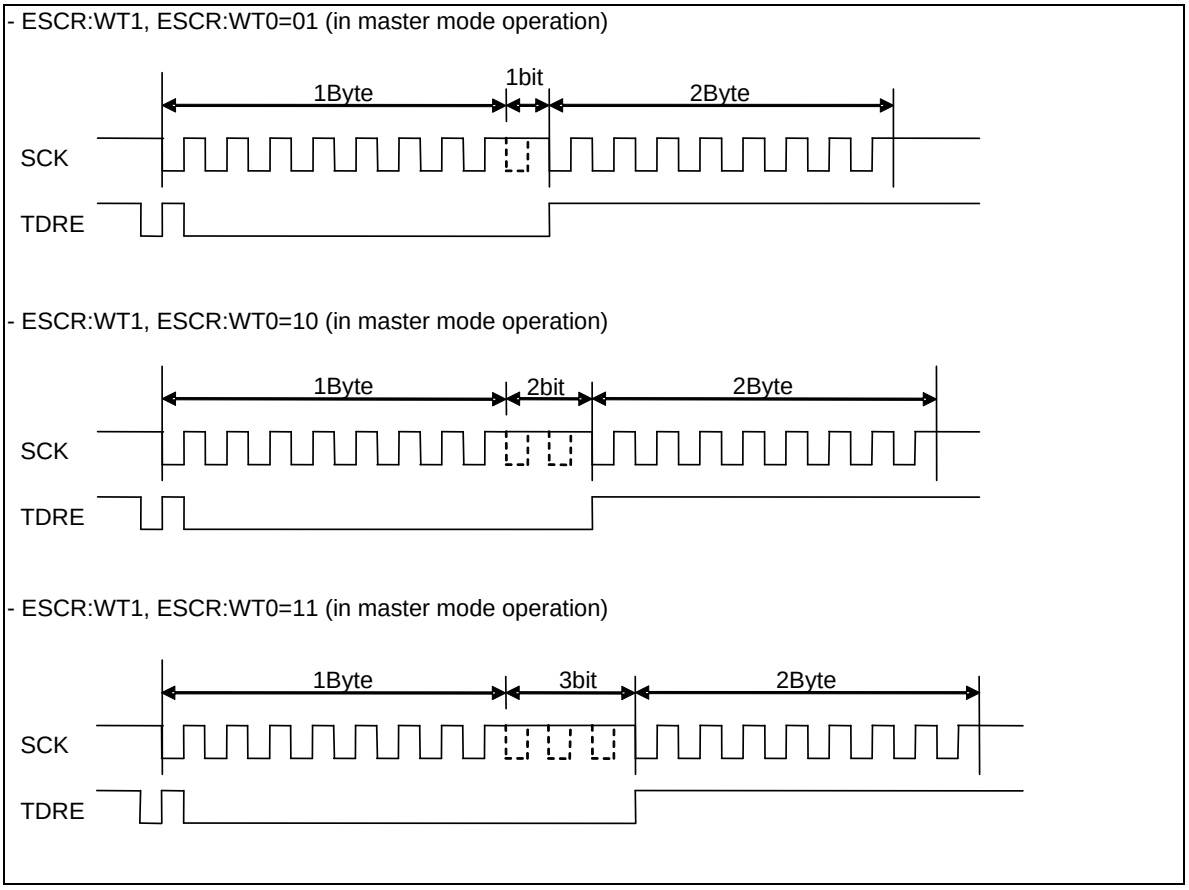
☐ **Data transmission and reception**

1. To perform data transmission and reception simultaneously, enable the serial data output (SMR:SOE=1) and enable the data transmission and reception (SCR:TXE, RXE=1).
2. When the transmit data is written in the TDR, the SSR:TDRE bit is set to "0" and the transmit data is output in synchronization with a falling edge of the serial clock (SCK) output. When the transmit data of the first bit is output, the SSR:TDRE bit is set to "1". If a transmit interrupt is enabled (SCR:TIE=1), a transmit interrupt request is output. During this time, the transmit data of the 2nd byte can be written in the register.
3. The received data is sampled at a rising edge of the serial clock (SCK) output. When the last bit of received data is received, the SSR:RDRF bit is set to "1". If a received interrupt is enabled (SCR:RIE=1), a received interrupt request is output. The received data (RDR) can be read during this time. When the received data is read, the SSR:RDRF bit is cleared to "0".
4. T Transmission/reception operation is completed after the end of data transmitting/receiving of the setting number by TBYTE.
5. After ending transmit/reception operation, a serial chip select pin (SCS) becomes inactive after hold time progress of serial chip select pin. However, when the serial chip select active level (SCSCR:SCAM=1) is kept at this time, serial chip select pin (SCS) holds an active state.

☐ Continuous data transmit or reception waiting

If anything other than ESCR:WT1, ESCR:WT0=00 is set for the continuous data transmission or reception, a wait is inserted between frames.

Figure 6.3-4. Continuous data transmit or reception waiting



- **Slave mode operation (SCR:MS=1, SMR:SCKE=0, SCSCR:CSEN0=1, SCSCR:CSOE=0, SCSCR:SCAM=0)**

  - **Data transmission**

1. If serial data output is enabled (SMR:SOE=1) and data transmission is enabled (SCR:TXE=1) and when the transmit data is written in the TDR, the SSR:TDRE bit is set to "0". This causes the transmit data to be output in synchronization with a falling edge of the serial clock (SCK) input.
2. When the transmit data of the first bit is output, the SSR:TDRE bit is set to "1". If a transmit interrupt is enabled (SCR:TIE=1), a transmit interrupt request is output. During this time, the transmit data of the 2nd byte can be written in the register.
3. If the 1st bit of transmit data is outputted, it is set to SSR:TDRE=1, and if transmitting interrupt enable (SCR:TIE=1) is carried out, a transmitting interrupt request will be outputted. The 2nd byte of transmit data can be written in at this time.
4. If serial chip select pin (SCS) becomes inactive, transmission / reception operation will be completed and serial output pin (SOT) will become "H".

  - **Data reception**

1. If the serial data output is disabled (SMR:SOE=0) and data reception is enabled (SCR:RXE=1), the received data is sampled at a rising edge of serial clock (SCK) input.
2. When the last bit is received, the SSR:RDRF bit is set to "1". If a received interrupt is enabled (SCR:RIE=1), a received interrupt request is output.
   The received data (RDR) can be read during this time.
3. When the received data (RDR) is read, the SSR:RDRF bit is cleared to "0".

☐ **Data transmission and reception**

1. To perform data transmission and reception simultaneously, enable the serial data output (SMR:SOE=1) and enable the data transmission and reception (SCR:TXE, RXE=1).
2. When the transmit data is written in the TDR, the SSR:TDRE bit is set to "0" and the transmit data is output in synchronization with a falling edge of the serial clock (SCK) input. When the transmit data of the first bit is output, the SSR:TDRE bit is set to "1". If a transmit interrupt is enabled (SCR:TIE=1), a transmit interrupt request is output. During this time, the transmit data of the 2nd byte can be written in the register.
3. The received data is sampled at a rising edge of the serial clock (SCK) input. When the last bit of received data is received, the SSR:RDRF bit is set to "1". If the received interrupt is enabled (SCR:RIE=1), a received interrupt request is output. The received data (RDR) can be read during this time. When the received data is read, the SSR:RDRF bit is cleared to "0".
4. If serial chip select pin (SCS) becomes inactive, transmission / reception operation will be completed and serial output pin (SOT) will become "H".

6.3.2 Normal transfer (II)

■ **Features**

	Item	Description
1	Serial clock (SCK) signal mark level	"LOW"
2	Transmit data output timing	SCK signal rising edge
3	Received data sampling	SCK signal falling edge
4	Data length	5 to 9 bits

■ **Register settings**

The register values required for normal transfer (II) is shown below.

SCR:SPI(*1)=0, SMR:MD2=0, MD1=1, MD0=0, and SCINV(*1)=1
When master operation : SCR:MS=0 and SMR:SCKE=1
When slave operation : SCR:MS=1 and SMR:SCKE=0

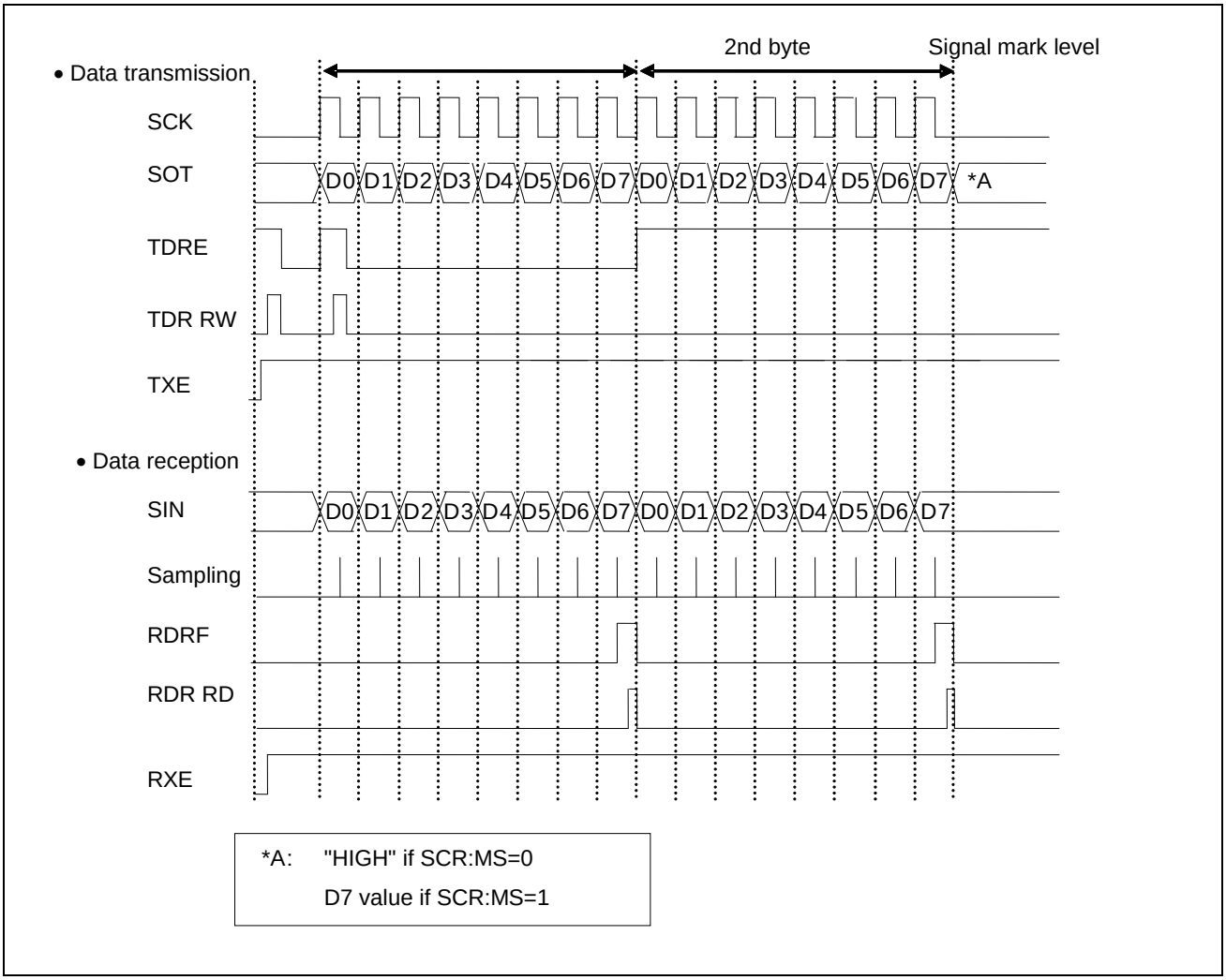
(*1) The bits set up according to conditions differ. See Table 6.4-2.

Note

Set up registers other than the above-mentioned bit according to directions for use.

■ **Normal transfer (II) timing chart (When Serial Chip Select Pin is unused.)**

Figure 6.3-5. Timing chart of normal transfer



- **Master mode operation (SCR:MS=0, SMR:SCKE=1, SCSCR:CSEN[3:0]=”0b0000”)**

  ☐ Data transmission

  1. If serial data output is enabled (SMR:SOE=1), data transmission is enabled (SCR:TXE=1) and data reception is disabled (SCR:RXE=0), and when the transmit data is written in the TDR, the SSR:TDRE bit is set to "0". This causes the transmit data to be output in synchronization with a rising edge of the serial clock (SCK) output.
  2. When the transmit data of the first bit is output, the SSR:TDRE bit is set to "1". Therefore, if the transmit interrupt is enabled (SCR:TIE=1), a transmit interrupt request is output. During this time, the transmit data of the 2nd byte can be written in the register.

- **Data reception**

  1. If the serial data output is disabled (SMR:SOE=0), data transmission is enabled (SCR:TXE=1) and data reception is enabled (SCR:RXE=1), and when a dummy data is written in the TDR, the received data is sampled at a falling edge of serial clock (SCK) output.
  2. When the last bit is received, the SSR:RDRF bit is set to "1". If a received interrupt is enabled (SCR:RIE=1) during this time, a received interrupt request is output.
     The received data (RDR) can be read during this time.
  3. When the received data (RDR) is read, the SSR:RDRF bit is cleared to "0".

Note

To perform data reception only, write a dummy data in the TDR so that the serial clock (SCK) is output.

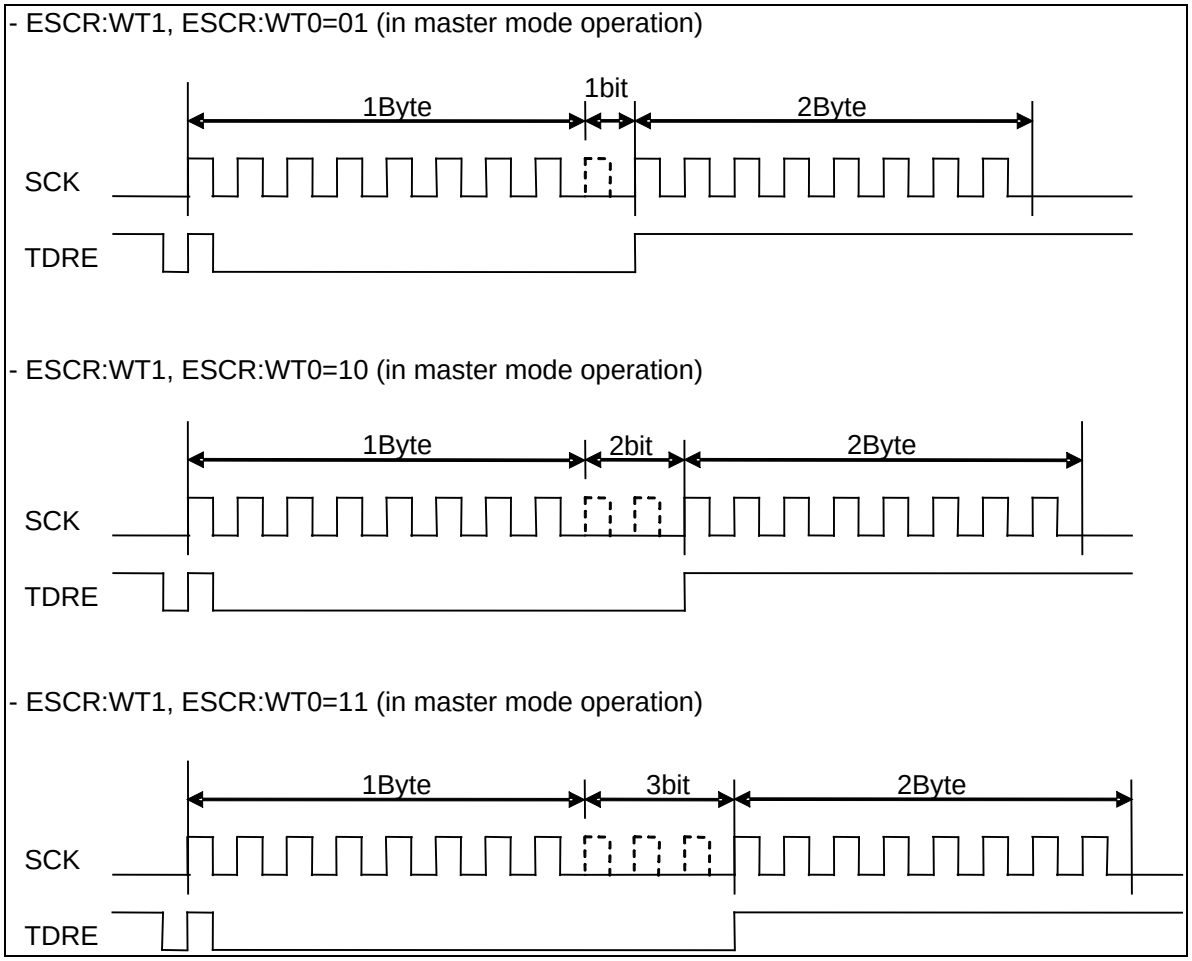
☐ **Data transmission and reception**

1. To perform data transmission and reception simultaneously, enable the serial data output (SMR:SOE=1) and enable the data transmission and reception (SCR:TXE, RXE=1).
2. When the transmit data is written in the TDR, the SSR:TDRE bit is set to "0" and the transmit data is output in synchronization with a rising edge of the serial clock (SCK) output. When the transmit data of the first bit is output, the SSR:TDRE bit is set to "1". If a transmit interrupt is enabled (SCR:TIE=1), a transmit interrupt request is output. During this time, the transmit data of the 2nd byte can be written in the register.
3. The received data is sampled at a falling edge of the serial clock (SCK) output. When the last bit of received data is received, the SSR:RDRF bit is set to "1". If a received interrupt is enabled (SCR:RIE=1), a received interrupt request is output. The received data (RDR) can be read during this time. When the received data is read, the SSR:RDRF bit is cleared to "0".

☐ **Continuous data transmit or reception waiting**

If anything other than ESCR:WT1, ESCR:WT0=00 is set for the continuous data transmission or reception, a wait is inserted between frames.

Figure 6.3-6. Continuous data transmit or reception waiting



- **Slave mode operation (SCR:MS=1, SMR:SCKE=0, SCSCR:CSEN0=0)**

  ☐ Data transmission

  1. If serial data output is enabled (SMR:SOE=1) and data transmission is enabled (SCR:TXE=1) and when the transmit data is written in the TDR, the SSR:TDRE bit is set to "0". This causes the transmit data to be output in synchronization with a rising edge of the serial clock (SCK) input.
  2. When the transmit data of the first bit is output, the SSR:TDRE bit is set to "1". If a transmit interrupt is enabled (SCR:TIE=1), a transmit interrupt request is output. During this time, the transmit data of the 2nd byte can be written in the register.

  ☐ Data reception

  1. If the serial data output is disabled (SMR:SOE=0) and data reception is enabled (SCR:RXE=1), the received data is sampled at a falling edge of serial clock (SCK) input.
  2. When the last bit is received, the SSR:RDRF bit is set to "1". If a received interrupt is enabled (SCR:RIE=1), a received interrupt request is output. The received data (RDR) can be read during this time.
  3. When the received data (RDR) is read, the SSR:RDRF bit is cleared to "0".

  ☐ Data transmission and reception

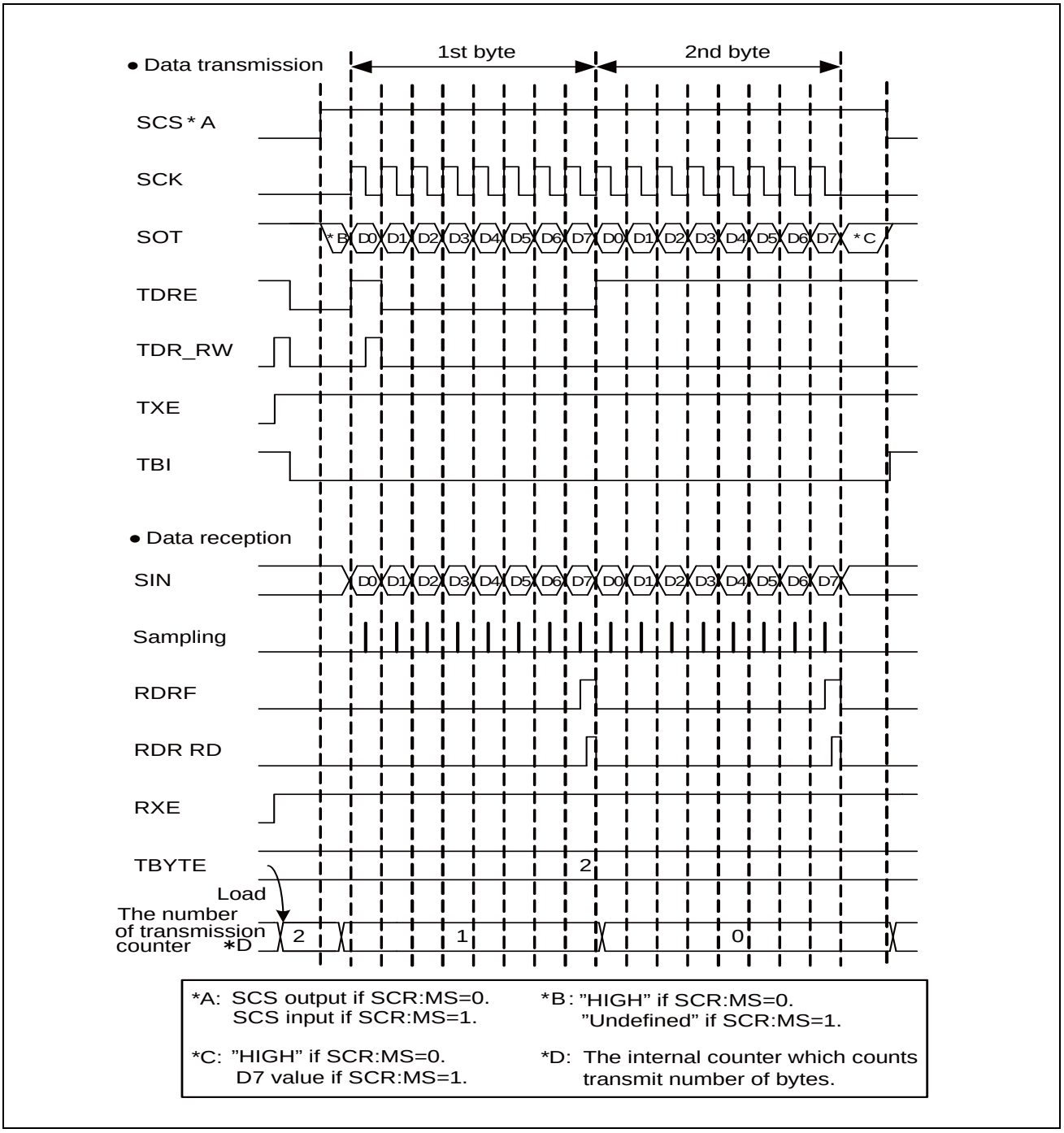
  1. To perform data transmission and reception simultaneously, enable the serial data output (SMR:SOE=1) and enable the data transmission and reception (SCR:TXE, RXE=1).
  2. When the transmit data is written in the TDR, the SSR:TDRE bit is set to "0" and the transmit data is output in synchronization with a rising edge of the serial clock (SCK) input. When the transmit data of the first bit is output,

the SSR:TDRE bit is set to "1". If a transmit interrupt is enabled (SCR:TIE=1), a transmit interrupt request is output. During this time, the transmit data of the 2nd byte can be written in the register.

3. The received data is sampled at a falling edge of the serial clock (SCK) input. When the last bit of received data is received, the SSR:RDRF bit is set to "1". If the received interrupt is enabled (SCR:RIE=1), a received interrupt request is output. The received data (RDR) can be read during this time. When the received data is read, the SSR:RDRF bit is cleared to "0".

- **Normal transfer (II) timing chart (When Serial Chip Select Pin is used.)**

Figure 6.3-7. Timing chart of normal transfer



- **Master mode operation (SCR:MS=0, SMR:SCKE=1, SCSCR:CSOE=1, SCSCR:CSENn*=1)**

* : The serial chip select pin number to be used into n.

- **Data transmission**

1. If serial data output is enabled (SMR:SOE=1), data transmission is enabled (SCR:TXE=1) and data reception is disabled (SCR:RXE=0), and when the transmit data is written in the TDR, the SSR:TDRE bit is set to "0". This causes the transmit data to be output in synchronization with a rising edge of the serial clock (SCK) output.
2. When the transmit data of the first bit is output, the SSR:TDRE bit is set to "1". Therefore, if the transmit interrupt is enabled (SCR:TIE=1), a transmit interrupt request is output. During this time, the transmit data of the 2nd byte can be written in the register.
3. T Transmission operation is completed after the end of data transmitting of the setting number by TBYTE.
4. After ending transmit operation, a serial chip select pin (SCS) becomes inactive after hold time progress of serial chip select pin. However, when the serial chip select active level (SCSCR:SCAM=1) is kept at this time, serial chip select pin (SCS) holds an active state.

- **Data reception**

1. If the serial data output is disabled (SMR:SOE=0), data transmission is enabled (SCR:TXE=1) and data reception is enabled (SCR:RXE=1), and when a dummy data is written in the TDR, the received data is sampled at a falling edge of serial clock (SCK) output.
2. When the last bit is received, the SSR:RDRF bit is set to "1". If a received interrupt is enabled (SCR:RIE=1) during this time, a received interrupt request is output.
   The received data (RDR) can be read during this time.
3. When the received data (RDR) is read, the SSR:RDRF bit is cleared to "0".
4. Reception operation is completed after the end of data receiving of the setting number by TBYTE.
5. After ending reception operation, a serial chip select pin (SCS) becomes inactive after hold time progress of serial chip select pin. However, when the serial chip select active level (SCSCR:SCAM=1) is kept at this time, serial chip select pin (SCS) holds an active state.

Note

To perform data reception only, write a dummy data in the TDR so that the serial clock (SCK) is output.

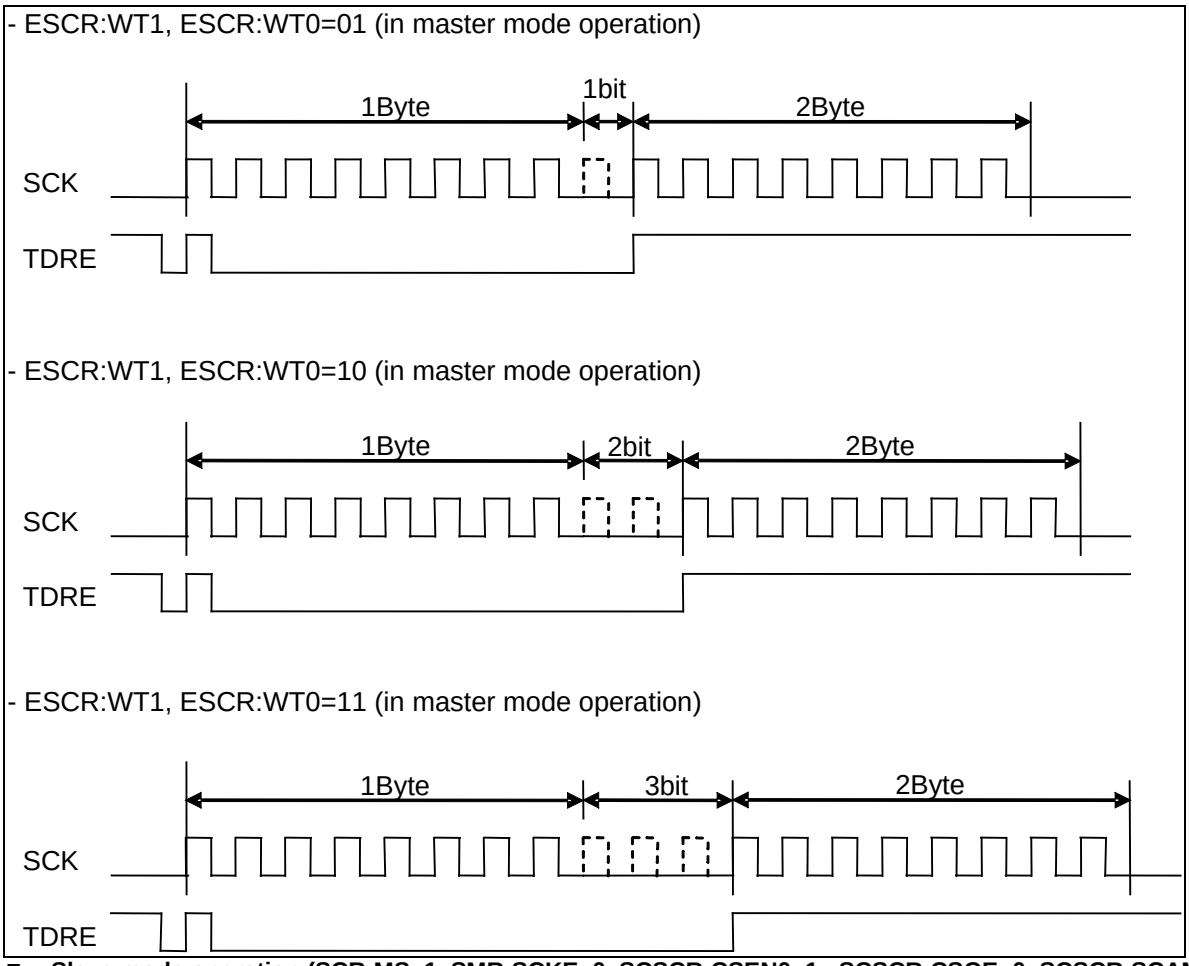
- **Data transmission and reception**

1. To perform data transmission and reception simultaneously, enable the serial data output (SMR:SOE=1) and enable the data transmission and reception (SCR:TXE, RXE=1).
2. When the transmit data is written in the TDR, the SSR:TDRE bit is set to "0" and the transmit data is output in synchronization with a rising edge of the serial clock (SCK) output. When the transmit data of the first bit is output, the SSR:TDRE bit is set to "1". If a transmit interrupt is enabled (SCR:TIE=1), a transmit interrupt request is output. During this time, the transmit data of the 2nd byte can be written in the register.
3. The received data is sampled at a falling edge of the serial clock (SCK) output. When the last bit of received data is received, the SSR:RDRF bit is set to "1". If a received interrupt is enabled (SCR:RIE=1), a received interrupt request is output. The received data (RDR) can be read during this time. When the received data is read, the SSR:RDRF bit is cleared to "0".
4. Transmission/reception operation is completed after the end of data transmitting/receiving of the setting number by TBYTE.
5. After ending transmit/reception operation, a serial chip select pin (SCS) becomes inactive after hold time progress of serial chip select pin. However, when the serial chip select active level (SCSCR:SCAM=1) is kept at this time, serial chip select pin (SCS) holds an active state.

☐ Continuous data transmit or reception waiting

If anything other than ESCR:WT1, ESCR:WT0=00 is set for the continuous data transmission or reception, a wait is inserted between frames.

Figure 6.3-8. Continuous data transmit or reception waiting



■ **Slave mode operation (SCR:MS=1, SMR:SCKE=0, SCSCR:CSEN0=1, SCSCR:CSOE=0, SCSCR:SCAM=0)**

☐ **Data transmission**

1. If serial data output is enabled (SMR:SOE=1) and data transmission is enabled (SCR:TXE=1) and when the transmit data is written in the TDR, the SSR:TDRE bit is set to "0". This causes the transmit data to be output in synchronization with a rising edge of the serial clock (SCK) input.
2. When the transmit data of the first bit is output, the SSR:TDRE bit is set to "1". If a transmit interrupt is enabled (SCR:TIE=1), a transmit interrupt request is output. During this time, the transmit data of the 2nd byte can be written in the register.
3. If the 1st bit of transmit data is outputted, it is set to SSR:TDRE=1, and if transmitting interrupt enable (SCR:TIE=1) is carried out, a transmitting interrupt request will be outputted. The 2nd byte of transmit data can be written in at this time.
4. If serial chip select pin (SCS) becomes inactive, transmission / reception operation will be completed and serial output pin (SOT) will become "H".

☐ Data reception

1. If the serial data output is disabled (SMR:SOE=0) and data reception is enabled (SCR:RXE=1), the received data is sampled at a falling edge of serial clock (SCK) input.

2. When the last bit is received, the SSR:RDRF bit is set to "1". If a received interrupt is enabled (SCR:RIE=1), a received interrupt request is output.
   The received data (RDR) can be read during this time.
3. When the received data (RDR) is read, the SSR:RDRF bit is cleared to "0".
4. SSR:RDRF will be cleared by "0" if received data register (RDR) are read.
5. Reception operation will be completed if a serial chip select pin (SCS) becomes inactive.

☐ **Data transmission and reception**

1. To perform data transmission and reception simultaneously, enable the serial data output (SMR:SOE=1) and enable the data transmission and reception (SCR:TXE, RXE=1).
2. When the transmit data is written in the TDR, the SSR:TDRE bit is set to "0" and the transmit data is output in synchronization with a rising edge of the serial clock (SCK) input. When the transmit data of the first bit is output, the SSR:TDRE bit is set to "1". If a transmit interrupt is enabled (SCR:TIE=1), a transmit interrupt request is output. During this time, the transmit data of the 2nd byte can be written in the register.
3. The received data is sampled at a falling edge of the serial clock (SCK) input. When the last bit of received data is received, the SSR:RDRF bit is set to "1". If the received interrupt is enabled (SCR:RIE=1), a received interrupt request is output. The received data (RDR) can be read during this time. When the received data is read, the SSR:RDRF bit is cleared to "0".
4. If serial chip select pin (SCS) becomes inactive, transmission / reception operation will be completed and serial output pin (SOT) will become "H".

6.3.3 SPI transfer (I)

■ **Features**

	Item	Description
1	Serial clock (SCK) signal mark level	"HIGH"
2	Transmit data output timing	SCK signal rising edge
3	Received data sampling	SCK signal falling edge
4	Data length	5 to 9 bits

■ **Register settings**

The register values required for SPI transfer (I) is shown below.

SCR:SPI(*1)=0, SMR:MD2=0, MD1=1, MD0=0, and SCINV(*1)=0
When master operation : SCR:MS=0 and SMR:SCKE=1
When slave operation : SCR:MS=1 and SMR:SCKE=0

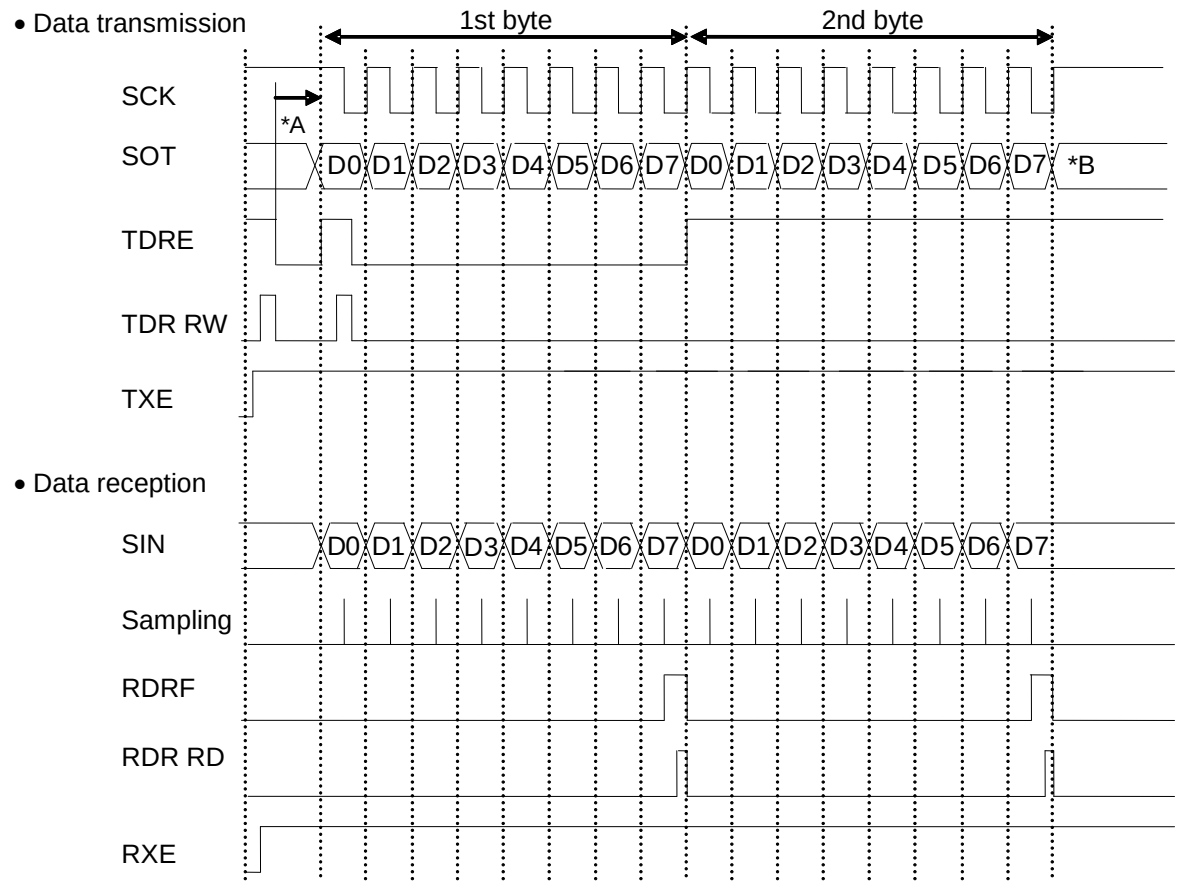
(*1) The bits set up according to conditions differ. See Table 6.4-2.

Note

Set up registers other than the above-mentioned bit according to directions for use.

■ **SPI transfer (I) timing chart (When Serial Chip Select Pin is unused.)**

Figure 6.3-9. Timing chart of normal transfer



*A: During slave mode transmission (MS=1, SCKE=0, SOE=1), 4 machine cycles or more time is required after writing data in the TDR
*B: "HIGH" if SCR:MS=0
"D0" of the 3rd byte if SCR:MS=1 and TDRE is "LOW"
"HIGH" if SCR:MS=1 and TDRE is "HIGH"

■ **Master mode operation (SCR:MS=0, SMR:SCKE=1, SCSCR:CSEN[3:0]=”0b0000”)**

☐ **Data transmission**

1. If serial data output is enabled (SMR:SOE=1), data transmission is enabled (SCR:TXE=1) and data reception is disabled (SCR:RXE=0), and when the transmit data is written in the TDR, the SSR:TDRE bit is set to "0". This causes the first bit to output. Then, the transmit data is output in synchronization with a rising edge of the serial clock (SCK) output.
2. The SSR:TDRE bit is set to "1" before a half cycle of a falling edge of serial clock (SCK) output. Therefore, if the transmit interrupt is enabled (SCR:TIE=1), a transmit interrupt request is output. During this time, the transmit data of the 2nd byte can be written in the register.

☐ **Data reception**

1. If the serial data output is disabled (SMR:SOE=0), data transmission is enabled (SCR:TXE=1) and data reception is enabled (SCR:RXE=1), and when a dummy data is written in the TDR, the received data is sampled at a falling edge of serial clock (SCK) output.
2. When the last bit is received, the SSR:RDRF bit is set to "1". If a received interrupt is enabled (SCR:RIE=1) during this time, a received interrupt request is output. The received data (RDR) can be read during this time.
3. When the received data (RDR) is read, the SSR:RDRF bit is cleared to "0".

Note

To perform data reception only, write a dummy data in the TDR so that the serial clock (SCK) is output.

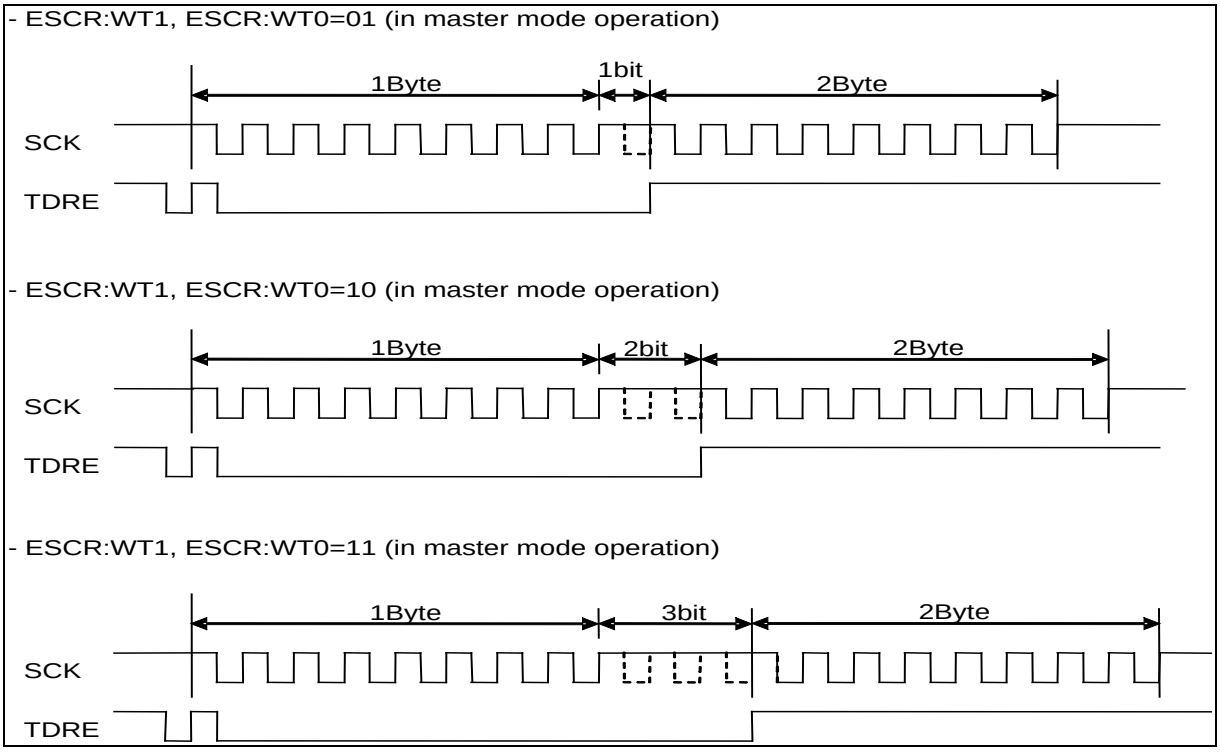
☐ Data transmission and reception

1. To perform data transmission and reception simultaneously, enable the serial data output (SMR:SOE=1) and enable the data transmission and reception (SCR:TXE, RXE=1).
2. When the transmit data is written in the TDR, the SSR:TDRE is set to "0" and the first bit is output. Then, the transmit data is output in synchronization with a rising edge of the serial clock (SCK) output. The SSR:TDRE bit is set to "1" before a half cycle of a falling edge of the first serial clock. If a transmit interrupt is enabled (SCR:TIE=1), a transmit interrupt request is output. During this time, the transmit data of the 2nd byte can be written in the register.
3. The received data is sampled at a falling edge of the serial clock (SCK) output. When the last bit of received data is received, the SSR:RDRF bit is set to "1". If a received interrupt is enabled (SCR:RIE=1), a received interrupt request is output. The received data (RDR) can be read during this time. When the received data is read, the SSR:RDRF bit is cleared to "0".

☐ **Continuous data transmit or reception waiting**

If anything other than ESCR:WT1, ESCR:WT0=00 is set for the continuous data transmission or reception, a wait is inserted between frames.

Figure 6.3-10. Continuous data transmit or reception waiting



- **Slave mode operation (SCR:MS=1, SMR:SCKE=0, SCSCR:CSEN0=0)**

  ☐ **Data transmission**

1. If serial data output is enabled (SMR:SOE=1) and data transmission is enabled (SCR:TXE=1) and when the transmit data is written in the TDR, the SSR:TDRE bit is set to "0". This causes the first bit to output. Then, the transmit data is output in synchronization with a rising edge of the serial clock (SCK) output.
2. When the first bit of transmit data is output, the SSR:TDRE bit is set to "1". If a transmit interrupt is enabled (SCR:TIE=1), a transmit interrupt request is output. During this time, the transmit data of the 2nd byte can be written in the register.

Note

If data transmission is enabled (SCR:TXE=1) and if the first transmit data is written in the TDR at a time other than the serial clock (SCK) signal mark level, the first data bit is not output and the data transmission may fail. After the data transmission is enabled (SCR:TXE=1), the first transmit data must be written in the TDR at a signal mark level of the serial clock (SCK).

☐ **Data reception**

1. If the serial data output is disabled (SMR:SOE=0) and data reception is enabled (SCR:RXE=1), the received data is sampled at a falling edge of serial clock (SCK) input.
2. When the last bit is received, the SSR:RDRF bit is set to "1". If a received interrupt is enabled (SCR:RIE=1), a received interrupt request is output.
   The received data (RDR) can be read during this time.
3. When the received data (RDR) is read, the SSR:RDRF bit is cleared to "0".

☐ **Data transmission and reception**

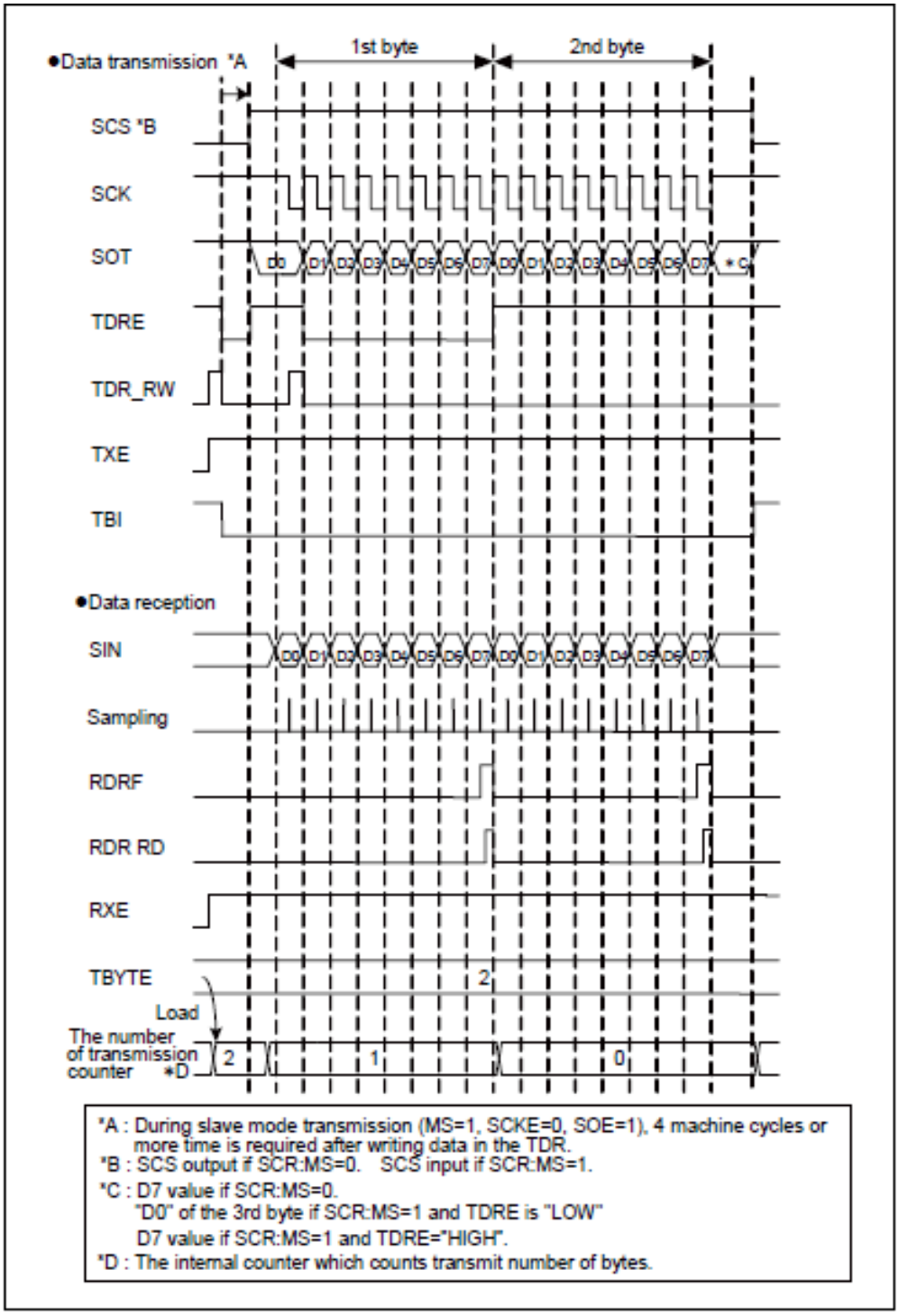
1. To perform data transmission and reception simultaneously, enable the serial data output (SMR:SOE=1) and enable the data transmission and reception (SCR:TXE, RXE=1).
2. When the transmit data is written in the TDR, the SSR:TDRE is set to "0" and the first bit is output. Then, the transmit data is output in synchronization with a rising edge of the serial clock (SCK) input. When the first bit of transmit data is output, the SSR:TDRE bit is set to "1". If a transmit interrupt is enabled (SCR:TIE=1), a transmit interrupt request is output. During this time, the transmit data of the 2nd byte can be written in the register.
3. The received data is sampled at a falling edge of the serial clock (SCK) input. When the last bit of received data is received, the SSR:RDRF bit is set to "1". If the received interrupt is enabled (SCR:RIE=1), a received interrupt request is output. The received data (RDR) can be read during this time. When the received data is read, the SSR:RDRF bit is cleared to "0".

☐ **Continuous switching from data reception to transmission**

1. Disable the serial data output (SMR:SOE=0), enable a received interrupt (SCR:RIE=1), enable data reception (SCR:RXE=1), and enable data transmission (SCR:TXE=1). If dummy data is written in the TDR at a signal mark level of serial clock (SCK), the received data is sampled at a falling edge of serial clock (SCK) input.
2. To continue data reception, write a dummy data in the TDR between the time when a received interrupt is requested and when the next serial clock (SCK) rises.
3. To switch the data reception to the data transmission, enable the serial data output (SMR:SOE=1), disable a received interrupt (SCR:RIE=0), and disable data reception (SCR:RXE=0) between the time when a received interrupt is requested and when the next serial clock (SCK) rises. Also, output the transmit data in synchronization with a rising edge of serial clock after the transmit data has been written in the TDR and the data reception has completed.

- **SPI transfer (I) timing chart (When Serial Chip Select Pin is used.)**

Figure 6.3-11. Timing chart of normal transfer



- **Master mode operation (SCR:MS=0, SMR:SCKE=1, SCSCR:CSOE=1, SCSCR:CSENn*=1))**

*: The serial chip select pin number to be used into n.

☐ **Data transmission**

1. If serial data output is enabled (SMR:SOE=1), data transmission is enabled (SCR:TXE=1) and data reception is disabled (SCR:RXE=0), and when the transmit data is written in the TDR, the SSR:TDRE bit is set to "0". This causes the first bit to output. Then, the transmit data is output in synchronization with a rising edge of the serial clock (SCK) output.
2. The SSR:TDRE bit is set to "1" before a half cycle of a falling edge of serial clock (SCK) output. Therefore, if the transmit interrupt is enabled (SCR:TIE=1), a transmit interrupt request is output. During this time, the transmit data of the 2nd byte can be written in the register.
3. Transmission operation is completed after the end of data transmitting of the setting number by TBYTE.
4. After ending transmit operation, a serial chip select pin (SCS) becomes inactive after hold time progress of serial chip select pin. However, when the serial chip select active level (SCSCR:SCAM=1) is kept at this time, serial chip select pin (SCS) holds an active state.

☐ **Data reception**

1. If the serial data output is disabled (SMR:SOE=0), data transmission is enabled (SCR:TXE=1) and data reception is enabled (SCR:RXE=1), and when a dummy data is written in the TDR, the received data is sampled at a falling edge of serial clock (SCK) output.
2. When the last bit is received, the SSR:RDRF bit is set to "1". If a received interrupt is enabled (SCR:RIE=1) during this time, a received interrupt request is output.
   The received data (RDR) can be read during this time.
3. When the received data (RDR) is read, the SSR:RDRF bit is cleared to "0".
4. Reception operation is completed after the end of data receiving of the setting number by TBYTE.
5. After ending reception operation, a serial chip select pin (SCS) becomes inactive after hold time progress of serial chip select pin. However, when the serial chip select active level (SCSCR:SCAM=1) is kept at this time, serial chip select pin (SCS) holds an active state.

Note

To perform data reception only, write a dummy data in the TDR so that the serial clock (SCK) is output.

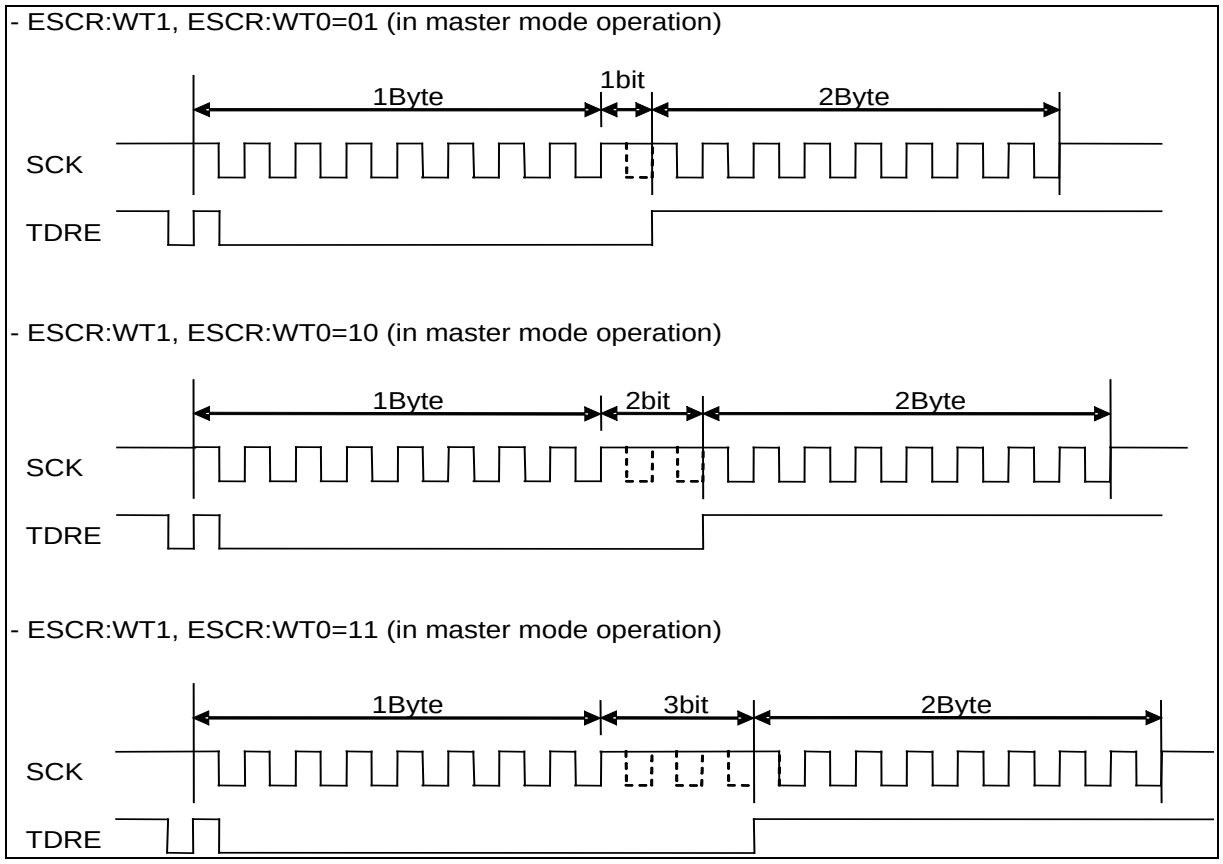
☐ **Data transmission and reception**

1. To perform data transmission and reception simultaneously, enable the serial data output (SMR:SOE=1) and enable the data transmission and reception (SCR:TXE, RXE=1).
2. When the transmit data is written in the TDR, the SSR:TDRE is set to "0" and the first bit is output. Then, the transmit data is output in synchronization with a rising edge of the serial clock (SCK) output. The SSR:TDRE bit is set to "1" before a half cycle of a falling edge of the first serial clock. If a transmit interrupt is enabled (SCR:TIE=1), a transmit interrupt request is output. During this time, the transmit data of the 2nd byte can be written in the register.
3. The received data is sampled at a falling edge of the serial clock (SCK) output. When the last bit of received data is received, the SSR:RDRF bit is set to "1". If a received interrupt is enabled (SCR:RIE=1), a received interrupt request is output. The received data (RDR) can be read during this time. When the received data is read, the SSR:RDRF bit is cleared to "0".
4. Transmission/reception operation is completed after the end of data transmitting/receiving of the setting number by TBYTE.
5. After ending transmit/reception operation, a serial chip select pin (SCS) becomes inactive after hold time progress of serial chip select pin. However, when the serial chip select active level (SCSCR:SCAM=1) is kept at this time, serial chip select pin (SCS) holds an active state.

☐ **Continuous data transmit or reception waiting**

If anything other than ESCR:WT1, ESCR:WT0=00 is set for the continuous data transmission or reception, a wait is inserted between frames.

Figure 6.3-12. Continuous Data Transmit or Reception Waiting



■ **Slave mode operation (SCR:MS=1, SMR:SCKE=0, SCSCR:CSEN=1, SCSCR:SCAM=0)**

☐ **Data transmission**

1. If serial data output is enabled (SMR:SOE=1) and data transmission is enabled (SCR:TXE=1) and when the transmit data is written in the TDR, the SSR:TDRE bit is set to "0". This causes the first bit to output. Then, the transmit data is output in synchronization with a rising edge of the serial clock (SCK) output.
2. When the first bit of transmit data is output, the SSR:TDRE bit is set to "1". If a transmit interrupt is enabled (SCR:TIE=1), a transmit interrupt request is output. During this time, the transmit data of the 2nd byte can be written in the register.
3. If the 1st bit of transmit data is outputted, it is set to SSR:TDRE=1, and if transmitting interrupt enable (SCR:TIE=1) is carried out, a transmitting interrupt request will be outputted. The 2nd byte of transmit data can be written in at this time.
4. If serial chip select pin (SCS) becomes inactive, transmission / reception operation will be completed and serial output pin (SOT) will become "H".

Note

If data transmission is enabled (SCR:TXE=1) and if the first transmit data is written in the TDR at a time other than the serial clock (SCK) signal mark level, the first data bit is not output and the data transmission may fail. After the data transmission is enabled (SCR:TXE=1), the first transmit data must be written in the TDR at a signal mark level of the serial clock (SCK).

☐ **Data reception**

1. If the serial data output is disabled (SMR:SOE=0) and data reception is enabled (SCR:RXE=1), the received data is sampled at a falling edge of serial clock (SCK) input.
2. When the last bit is received, the SSR:RDRF bit is set to "1". If a received interrupt is enabled (SCR:RIE=1), a received interrupt request is output. The received data (RDR) can be read during this time.
3. When the received data (RDR) is read, the SSR:RDRF bit is cleared to "0".
4. SSR:RDRF will be cleared by "0" if received data register (RDR) are read.
5. Reception operation will be completed if a serial chip select pin (SCS) becomes inactive.

☐ **Data transmission and reception**

1. To perform data transmission and reception simultaneously, enable the serial data output (SMR:SOE=1) and enable the data transmission and reception (SCR:TXE, RXE=1).
2. When the transmit data is written in the TDR, the SSR:TDRE is set to "0" and the first bit is output. Then, the transmit data is output in synchronization with a rising edge of the serial clock (SCK) input. When the first bit of transmit data is output, the SSR:TDRE bit is set to "1". If a transmit interrupt is enabled (SCR:TIE=1), a transmit interrupt request is output. During this time, the transmit data of the 2nd byte can be written in the register.
3. The received data is sampled at a falling edge of the serial clock (SCK) input. When the last bit of received data is received, the SSR:RDRF bit is set to "1". If the received interrupt is enabled (SCR:RIE=1), a received interrupt request is output. The received data (RDR) can be read during this time. When the received data is read, the SSR:RDRF bit is cleared to "0".
4. If serial chip select pin (SCS) becomes inactive, transmission / reception operation will be completed and serial output pin (SOT) will become "H".

6.3.4 SPI transfer (II)

■ **Features**

	Item	Description
1	Serial clock (SCK) signal mark level	"LOW"
2	Transmit data output timing	SCK signal falling edge
3	Received data sampling	SCK signal rising edge
4	Data length	5 to 9 bits

■ **Register settings**

The register values required for SPI transfer (II) are listed on the table below.

The register values required for SPI transfer (I) is shown below.

SCR:SPI(*1)=0, SMR:MD2=0, MD1=1, MD0=0, and SCINV(*1)=1
When master operation : SCR:MS=0 and SMR:SCKE=1
When slave operation : SCR:MS=1 and SMR:SCKE=0

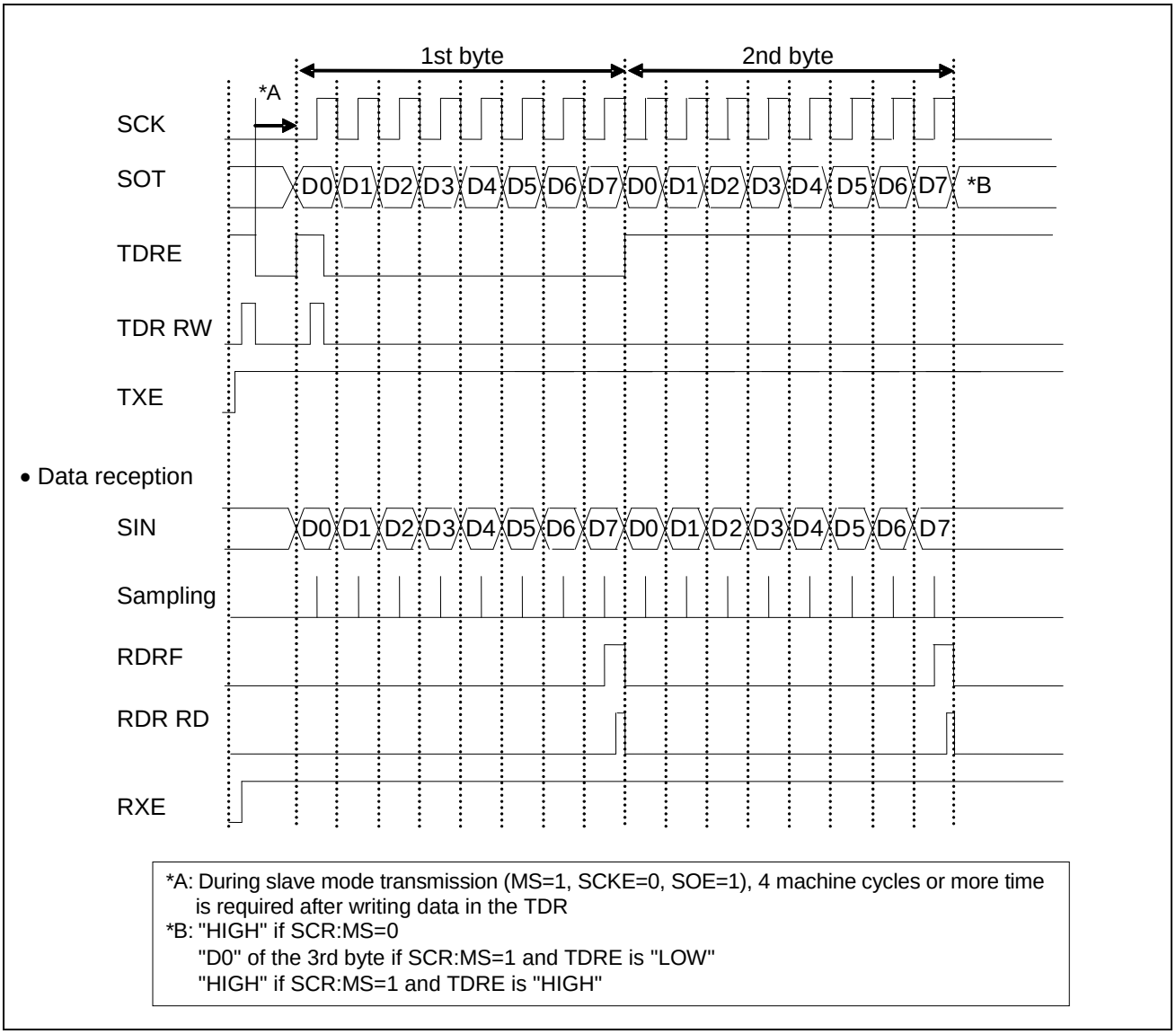
(*1) The bits set up according to conditions differ. See Table 6.4-2.

Note

Set up registers other than the above-mentioned bit according to directions for use.

■ **SPI transfer (II) timing chart (When Serial Chip Select Pin is unused.)**

Figure 6.3-13. Timing Chart of Normal Transfer



■ **Master mode operation (SCR:MS=0, SMR:SCKE=1)**

☐ **Data transmission**

1. If serial data output is enabled (SMR:SOE=1), data transmission is enabled (SCR:TXE=1) and data reception is disabled (SCR:RXE=0), and when the transmit data is written in the TDR, the SSR:TDRE bit is set to "0". This causes the transmit data to be output in synchronization with a falling edge of the serial clock (SCK) output.
2. The SSR:TDRE bit is set to "1" before a half cycle of a rising edge of the first serial clock (SCK) output. Therefore, if the transmit interrupt is enabled (SCR:TIE=1), a transmit interrupt request is output. During this time, the transmit data of the 2nd byte can be written in the register.

☐ **Data reception**

1. If the serial data output is disabled (SMR:SOE=0), data transmission is enabled (SCR:TXE=1) and data reception is enabled (SCR:RXE=1), and when a dummy data is written in the TDR, the received data is sampled at a rising edge of serial clock (SCK) output.
2. When the last bit is received, the SSR:RDRF bit is set to "1". If a received interrupt is enabled (SCR:RIE=1) during this time, a received interrupt request is output.
   The received data (RDR) can be read during this time.
3. When the received data (RDR) is read, the SSR:RDRF bit is cleared to "0".

Note

To perform data reception only, write a dummy data in the TDR so that the serial clock (SCK) is output.

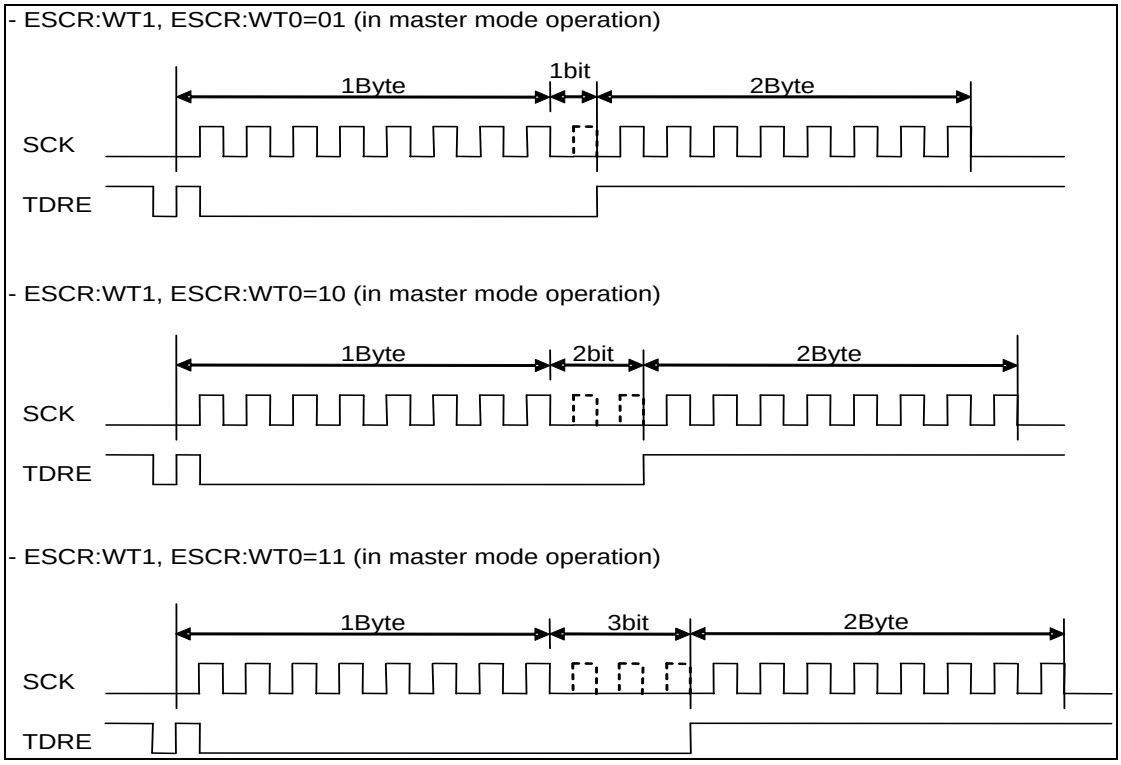
☐ **Data transmission and reception**

1. To perform data transmission and reception simultaneously, enable the serial data output (SMR:SOE=1) and enable the data transmission and reception (SCR:TXE, RXE=1).
2. When the transmit data is written in the TDR, the SSR:TDRE is set to "0" and the first bit is output. Then, the transmit data is output in synchronization with a falling edge of the serial clock (SCK) output. The SSR:TDRE bit is set to "1" before a half cycle of a rising edge of the first serial clock. If a transmit interrupt is enabled (SCR:TIE=1), a transmit interrupt request is output. During this time, the transmit data of the 2nd byte can be written in the register.
3. The received data is sampled at a rising edge of the serial clock (SCK) output. When the last bit of received data is received, the SSR:RDRF bit is set to "1". If a received interrupt is enabled (SCR:RIE=1), a received interrupt request is output. The received data (RDR) can be read during this time. When the received data is read, the SSR:RDRF bit is cleared to "0".

☐ **Continuous data transmit or reception waiting**

If anything other than ESCR:WT1, ESCR:WT0=00 is set for the continuous data transmission or reception, a wait is inserted between frames.

Figure 6.3-14. Continuous data transmit or reception waiting



- **Slave mode operation (SCR:MS=1, SMR:SCKE=0)**

  ☐ Data transmission

  1. If serial data output is enabled (SMR:SOE=1) and data transmission is enabled (SCR:TXE=1) and when the transmit data is written in the TDR, the SSR:TDRE bit is set to "0". This causes the first bit to output. Then, the transmit data is output in synchronization with a falling edge of the serial clock (SCK) input.
  2. When the first bit of transmit data is output, the SSR:TDRE bit is set to "1". If a transmit interrupt is enabled (SCR:TIE=1), a transmit interrupt request is output. During this time, the transmit data of the 2nd byte can be written in the register.

Note

If data transmission is enabled (SCR:TXE=1) and if the first transmit data is written in the TDR at a time other than the serial clock (SCK) signal mark level, the first data bit is not output and the data transmission may fail. After the data transmission is enabled (SCR:TXE=1), the first transmit data must be written in the TDR at a signal mark level of the serial clock (SCK).

☐ **Data reception**

1. If the serial data output is disabled (SMR:SOE=0) and data reception is enabled (SCR:RXE=1), the received data is sampled at a rising edge of serial clock (SCK) input.
2. When the last bit is received, the SSR:RDRF bit is set to "1". If a received interrupt is enabled (SCR:RIE=1), a received interrupt request is output. The received data (RDR) can be read during this time.
3. When the received data (RDR) is read, the SSR:RDRF bit is cleared to "0".

☐ **Data transmission and reception**

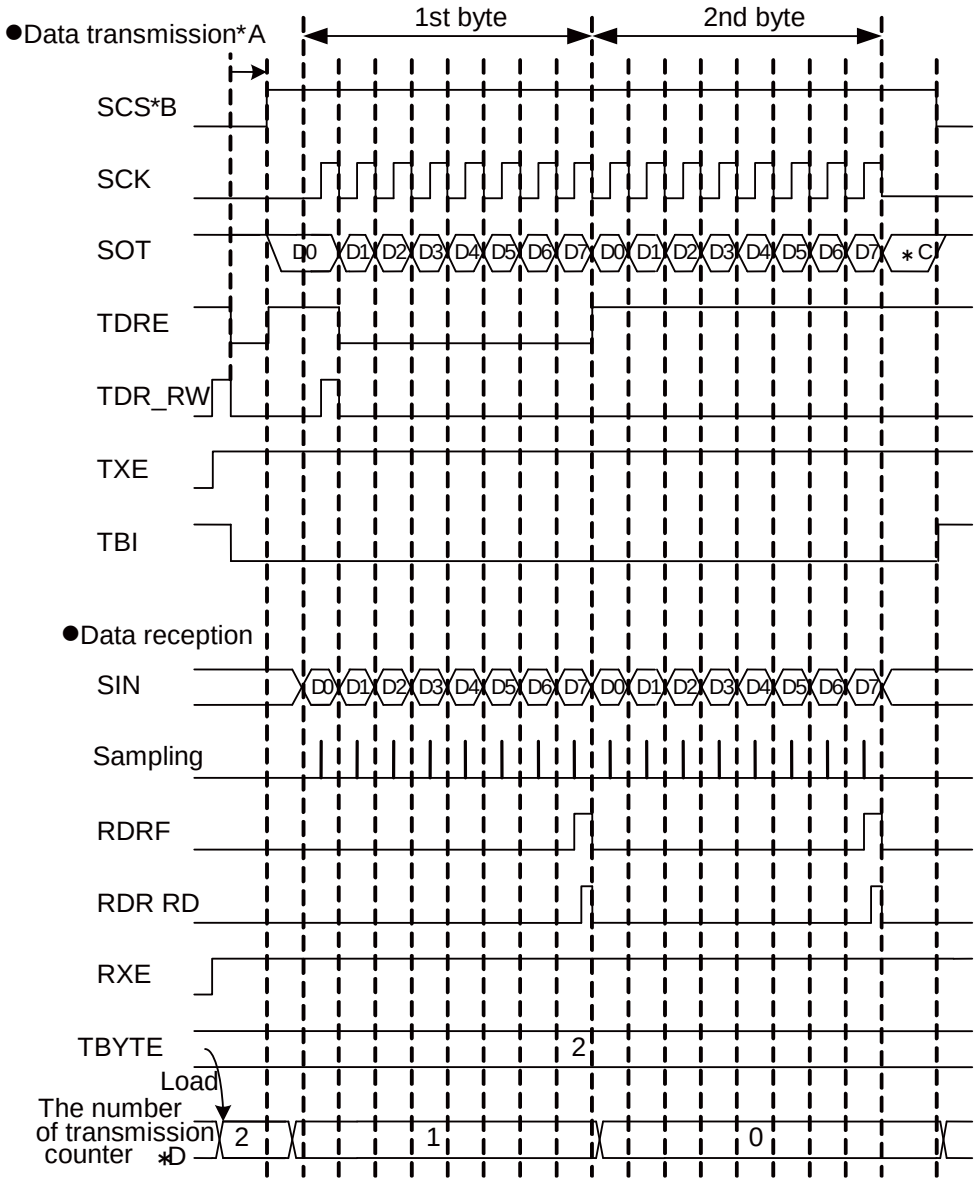
1. To perform data transmission and reception simultaneously, enable the serial data output (SMR:SOE=1) and enable the data transmission and reception (SCR:TXE, RXE=1).
2. When the transmit data is written in the TDR, the SSR:TDRE is set to "0" and the first bit is output. Then, the transmit data is output in synchronization with a falling edge of the serial clock (SCK) input. When the first bit of transmit data is output, the SSR:TDRE bit is set to "1". If a transmit interrupt is enabled (SCR:TIE=1), a transmit interrupt request is output. During this time, the transmit data of the 2nd byte can be written in the register.
3. The received data is sampled at a rising edge of the serial clock (SCK) input. When the last bit of received data is received, the SSR:RDRF bit is set to "1". If the received interrupt is enabled (SCR:RIE=1), a received interrupt request is output. The received data (RDR) can be read during this time. When the received data is read, the SSR:RDRF bit is cleared to "0".

☐ **Continuous switching from data reception to transmission**

1. Disable the serial data output (SMR:SOE=0), enable a received interrupt (SCR:RIE=1), enable data reception (SCR:RXE=1), and enable data transmission (SCR:TXE=1). If dummy data is written in the TDR at a signal mark level of serial clock (SCK), the received data is sampled at a falling edge of serial clock (SCK) input.
2. To continue data reception, write a dummy data in the TDR between the time when a received interrupt is requested and when the next serial clock (SCK) rises.
3. To switch the data reception to the data transmission, enable the serial data output (SMR:SOE=1), disable a received interrupt (SCR:RIE=0), and disable data reception (SCR:RXE=0) between the time when a received interrupt is requested and when the next serial clock (SCK) rises. Also, output the transmit data in synchronization with a rising edge of serial clock after the transmit data has been written in the TDR and the data reception has completed.

■ **SPI transfer (II) timing chart (When Serial Chip Select Pin is used.)**

Figure 6.3-15. Timing chart of normal transfer



*A : During slave mode transmission (MS=1, SCKE=0, SOE=1), 4 machine cycles or more time is required after writing data in the TDR.

*B : SCS output if SCR:MS=0. SCS input if SCR:MS=1.

*C : D7 value if SCR:MS=0.
"D0" of the 3rd byte if SCR:MS=1 and TDRE is "LOW"
D7 value if SCR:MS=1 and TDRE="HIGH".

*D : The internal counter which counts transmit number of bytes.

- **Master mode operation (SCR:MS=0, SMR:SCKE=1, SCSCR:CSOE=1, SCSCR:CSENn*=1)**

*: The serial chip select pin number to be used into n.

☐ **Data transmission**

1. If serial data output is enabled (SMR:SOE=1), data transmission is enabled (SCR:TXE=1) and data reception is disabled (SCR:RXE=0), and when the transmit data is written in the TDR, the SSR:TDRE bit is set to "0". This causes the transmit data to be output in synchronization with a falling edge of the serial clock (SCK) output.
2. The SSR:TDRE bit is set to "1" before a half cycle of a rising edge of the first serial clock (SCK) output. Therefore, if the transmit interrupt is enabled (SCR:TIE=1), a transmit interrupt request is output. During this time, the transmit data of the 2nd byte can be written in the register.
3. Transmission operation is completed after the end of data transmitting of the setting number by TBYTE.
4. After ending transmit operation, a serial chip select pin (SCS) becomes inactive after hold time progress of serial chip select pin. However, when the serial chip select active level (SCSCR:SCAM=1) is kept at this time, serial chip select pin (SCS) holds an active state.

☐ **Data reception**

1. If the serial data output is disabled (SMR:SOE=0), data transmission is enabled (SCR:TXE=1) and data reception is enabled (SCR:RXE=1), and when a dummy data is written in the TDR, the received data is sampled at a rising edge of serial clock (SCK) output.
2. When the last bit is received, the SSR:RDRF bit is set to "1". If a received interrupt is enabled (SCR:RIE=1) during this time, a received interrupt request is output. The received data (RDR) can be read during this time.
3. When the received data (RDR) is read, the SSR:RDRF bit is cleared to "0".
4. Reception operation is completed after the end of data receiving of the setting number by TBYTE.
5. After ending reception operation, a serial chip select pin (SCS) becomes inactive after hold time progress of serial chip select pin. However, when the serial chip select active level (SCSCR:SCAM=1) is kept at this time, serial chip select pin (SCS) holds an active state.

Note

To perform data reception only, write a dummy data in the TDR so that the serial clock (SCK) is output.

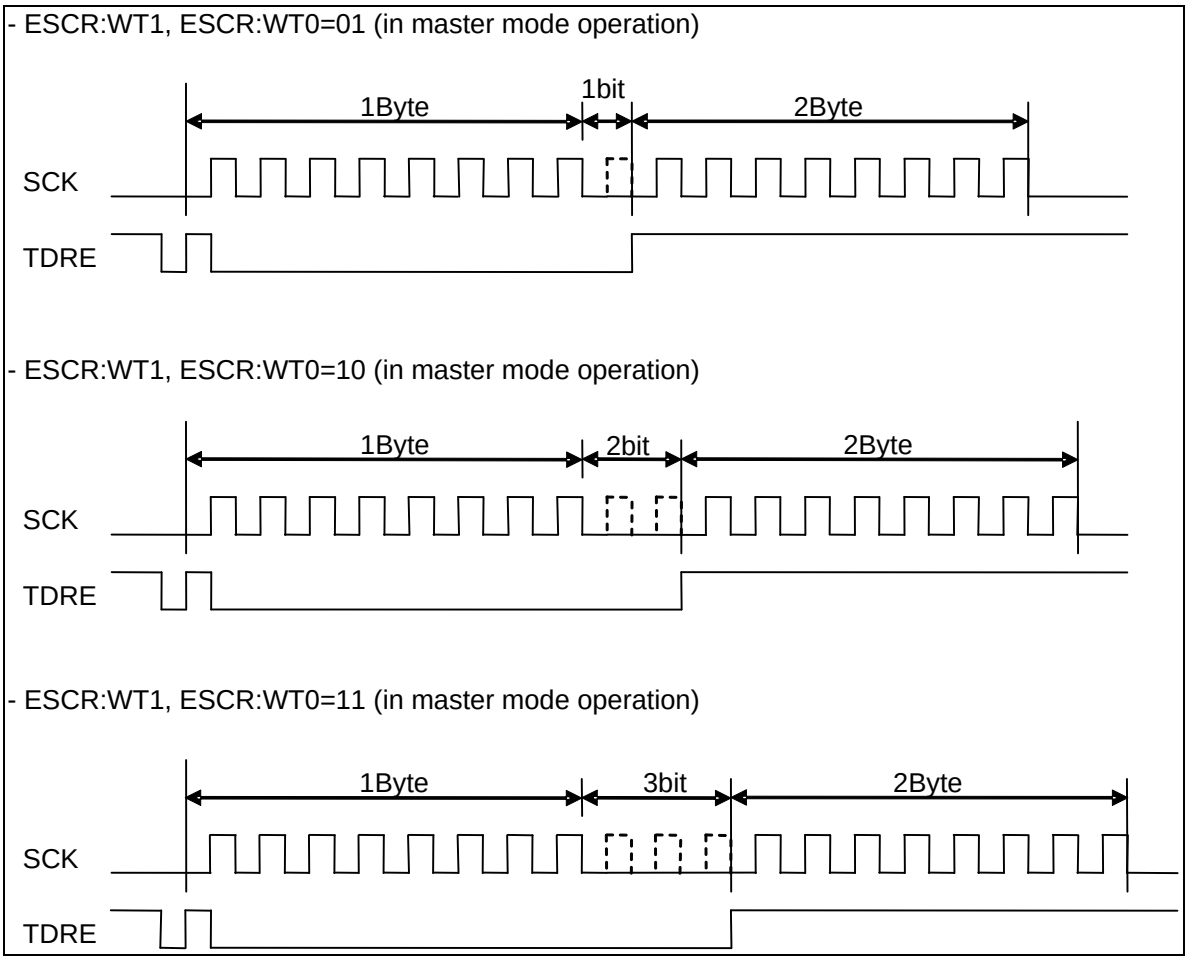
☐ Data transmission and reception

1. To perform data transmission and reception simultaneously, enable the serial data output (SMR:SOE=1) and enable the data transmission and reception (SCR:TXE, RXE=1).
2. When the transmit data is written in the TDR, the SSR:TDRE is set to "0" and the first bit is output. Then, the transmit data is output in synchronization with a falling edge of the serial clock (SCK) output. The SSR:TDRE bit is set to "1" before a half cycle of a rising edge of the first serial clock. If a transmit interrupt is enabled (SCR:TIE=1), a transmit interrupt request is output. During this time, the transmit data of the 2nd byte can be written in the register.
3. The received data is sampled at a rising edge of the serial clock (SCK) output. When the last bit of received data is received, the SSR:RDRF bit is set to "1". If a received interrupt is enabled (SCR:RIE=1), a received interrupt request is output. The received data (RDR) can be read during this time. When the received data is read, the SSR:RDRF bit is cleared to "0".
4. Transmission/reception operation is completed after the end of data transmitting/receiving of the setting number by TBYTE.
5. After ending transmit/reception operation, a serial chip select pin (SCS) becomes inactive after hold time progress of serial chip select pin. However, when the serial chip select active level (SCSCR:SCAM=1) is kept at this time, serial chip select pin (SCS) holds an active state.

- **Continuous data transmit or reception waiting**

If anything other than ESCR:WT1, ESCR:WT0=00 is set for the continuous data transmission or reception, a wait is inserted between frames.

Figure 6.3-16. Continuous Data Transmit or Reception Waiting



- **Slave mode operation (SCR:MS=1, SMR:SCKE=0, SCSCR:CSEN=1, SCSCR:SCAM=0)**

  ☐ Data transmission

  1. If serial data output is enabled (SMR:SOE=1) and data transmission is enabled (SCR:TXE=1) and when the transmit data is written in the TDR, the SSR:TDRE bit is set to "0". This causes the first bit to output. Then, the transmit data is output in synchronization with a falling edge of the serial clock (SCK) input.
  2. When the first bit of transmit data is output, the SSR:TDRE bit is set to "1". If a transmit interrupt is enabled (SCR:TIE=1), a transmit interrupt request is output. During this time, the transmit data of the 2nd byte can be written in the register.
  3. If the 1st bit of transmit data is outputted, it is set to SSR:TDRE=1, and if transmitting interrupt enable (SCR:TIE=1) is carried out, a transmitting interrupt request will be outputted. The 2nd byte of transmit data can be written in at this time.
  4. If serial chip select pin (SCS) becomes inactive, transmission / reception operation will be completed and serial output pin (SOT) will become "H".

Note

If data transmission is enabled (SCR:TXE=1) and if the first transmit data is written in the TDR at a time other than the serial clock (SCK) signal mark level, the first data bit is not output and the data transmission may fail. After the data transmission is enabled (SCR:TXE=1), the first transmit data must be written in the TDR at a signal mark level of the serial clock (SCK).

☐ Data reception

1. If the serial data output is disabled (SMR:SOE=0) and data reception is enabled (SCR:RXE=1), the received data is sampled at a rising edge of serial clock (SCK) input.
2. When the last bit is received, the SSR:RDRF bit is set to "1". If a received interrupt is enabled (SCR:RIE=1), a received interrupt request is output. The received data (RDR) can be read during this time.
3. When the received data (RDR) is read, the SSR:RDRF bit is cleared to "0".
4. Reception operation will be completed if a serial chip select pin (SCS) becomes inactive.

☐ Data transmission and reception

1. To perform data transmission and reception simultaneously, enable the serial data output (SMR:SOE=1) and enable the data transmission and reception (SCR:TXE, RXE=1).
2. When the transmit data is written in the TDR, the SSR:TDRE is set to "0" and the first bit is output. Then, the transmit data is output in synchronization with a falling edge of the serial clock (SCK) input. When the first bit of transmit data is output, the SSR:TDRE bit is set to "1". If a transmit interrupt is enabled (SCR:TIE=1), a transmit interrupt request is output. During this time, the transmit data of the 2nd byte can be written in the register.
3. The received data is sampled at a rising edge of the serial clock (SCK) input. When the last bit of received data is received, the SSR:RDRF bit is set to "1". If the received interrupt is enabled (SCR:RIE=1), a received interrupt request is output. The received data (RDR) can be read during this time. When the received data is read, the SSR:RDRF bit is cleared to "0".
4. If serial chip select pin (SCS) becomes inactive, transmission / reception operation will be completed and serial output pin (SOT) will become "H".

6.4 Operation of Serial Chip Select

This section explains operation of the serial chip select.

- **Operation of master mode (SCR:MS=0)**

  The serial chip select pin operates as follows at master mode (SCR:MS=0).

1. If transmit data is written in during transmit enable (SCR:TXE=1) by serial chip select operation enable (SCSCR:CSENn=1), serial chip select pin will become active.
2. Transmit/reception operation is started after setup-time progress of serial chip select pin.
3. Transmit/reception operation is ended after data transmit/reception operation of the number of setting up by TBYTE.
4. After ending transmit/reception operation, serial chip select pin becomes inactive after hold time progress of serial chip select pin.

Figure 6.4-1. Operation of Serial Chip Select (Master transmit (MS=0), Normal transfer SPI=0), SCINV=0)

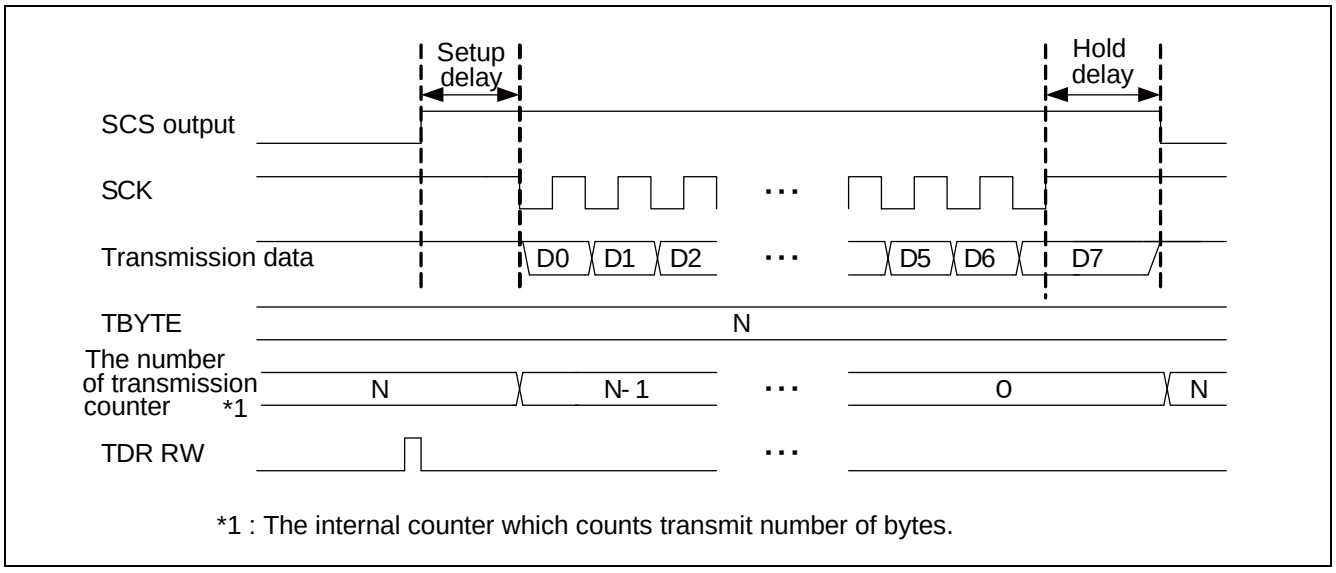
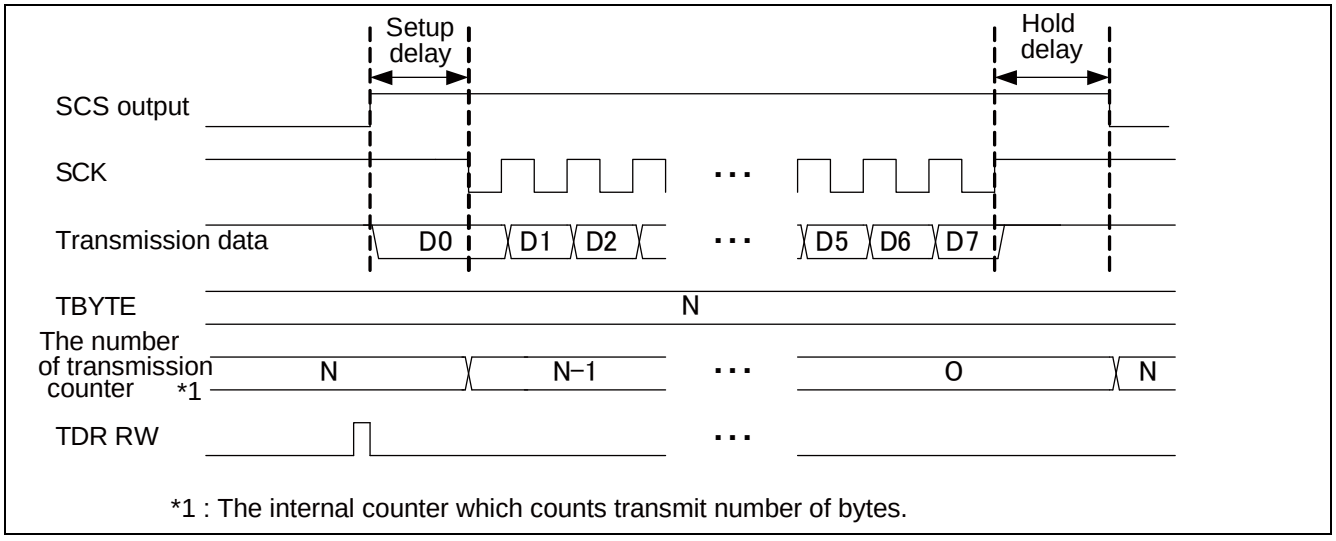


Figure 6.4-2. Operation of Serial Chip Select (Master transmit (MS=0), SPI transfer SPI=1), SCINV=0)



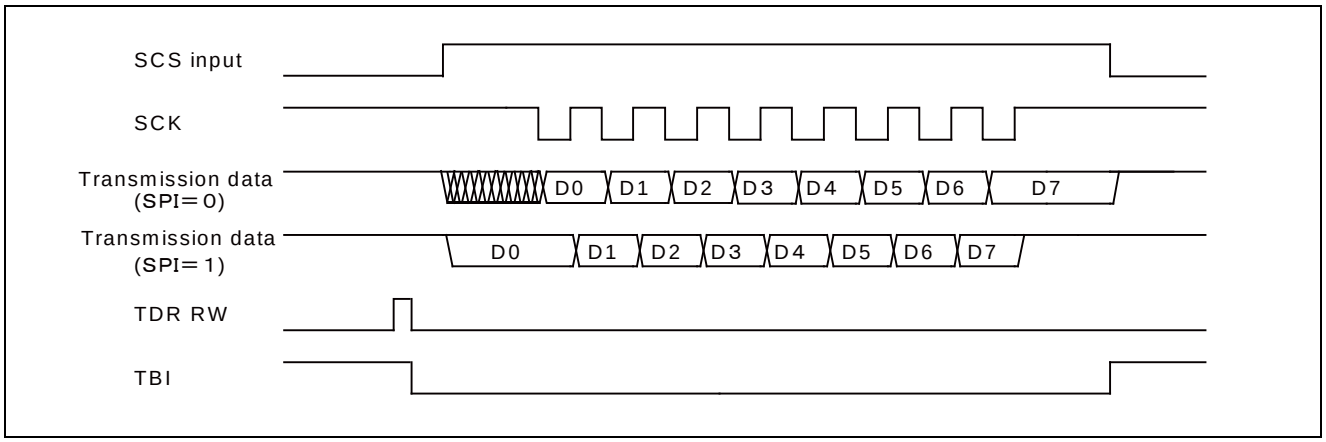
Notes

- When serial chip select pin uses on transmission disable (SCR:TXE=0), and software reset (SCR:UPCL=1) at active, serial chip select pin becomes inactive.
- When transmit data is written in the hold delay time of serial chip select pin, serial chip select pin does not become inactive, but transmits the next transmit data.
- When the active state of serial chip select pin is not held (SCSCR:SCAM=0), serial chip select pin becomes inactive and becomes transmit bus idle (SSR:TBI=1) after deselect time progress.
- When SCSCR:CSEN [3:0] is set as "0b0000" at master mode (SCR:MS=0), transmit/reception operation is performed without being dependent on serial chip select pin.
- The following operations are performed, when only the number of frames smaller than the preset value of TBYTE has transmitted, one-frame transmission is completed and there is no transmit data effective (SSR:TDRE=1) in a Transmit Data Register (TDR).
  - ☐ In transfer byte error enable (TBEEN=1), chip select error (SACSR:CSE=1) occurs. After chip select error (SACSR:CSE=1) occurs, serial chip select pin becomes inactive after hold delay time progress. When "1" is set to the chip select error flag (SACSR:CSE), transmit operation is not started even if transmit data is written in Transmit Data Register (TDR).
  - ☐ In the transfer byte error disable (TBEEN=0), transmit operation is stopped until transmit data is written in Transmit Data Register (TDR). In this case, serial chip select pin is active. Transmit operation will be resumed if transmit data is written in a Transmit Data Register (TDR).

☐ Operation of slave mode (SCR:MS=1)

The serial chip select pin 0 (SCS0) will perform transmit operation or reception operation synchronizing with serial clock (SCK), if serial chip select pin input becomes active by permission (SCSCR:CSEN0="1"). Then, if serial chip select pin input becomes inactive, transmit operation or reception operation will be ended.

Figure 6.4-3. Serial chip select operation at slave mode (Slave transmit, SCINV=0)



Notes

- The serial chip select pin input does not operate, even if serial clock is inputted at inactive.
- If serial chip select input becomes inactive before sampling bit finally during reception operation, the data under reception will be erased.
- If serial chip select input becomes inactive during transmit operation, the data under transmission will be erased and chip select error will occur it (SACSR:CSE).
- TDR will become transmitting bus idle (SSR:TBI=1), if serial chip select pin input becomes inactive in the empty (SSR:TDRE=1)
- When SCSCR:CSEN0 is set as "0" at slave mode (SCR:MS=1), transmit / reception operation is performed without being dependent on serial chip select pin.

☐ Timing adjustment of serial chip select

By master mode (SCR:MS=0), in the case of serial chip select operation enable (SCSCR:CSENn=1) Setup delay, hold delay, and deselect time can be adjusted by adjusting Serial Chip Select Timing Register (SCSTR[3:0]).

- Setup delay time
  Setup delay time is time after serial chip select pin becomes active until serial clock is outputted. See Figure 6.4-4 and Figure 6.4-5 for regulation of setup delay time.

  Setup delay time can adjust in chip select setup delay bits (SCSTR0:CSSU[7:0]).

- Hold delay time
  Hold delay time is time after ending the output of serial clock until serial chip select pin becomes inactive. See Figure 6.4-4 and Figure 6.4-5 for regulation of hold delay time.

  Hold delay time can adjust in chip select hold delay bits (SCSTR1:CSHD[7:0]).

- Deselect time
  Deselect time is minimum time after serial chip select pin becomes inactive until serial chip select pin next becomes active. Although transmit data is written in transmit data register (TDR) during deselect time, serial chip select pin does not become active till the end of deselect time. See Figure 6.4-4 and Figure 6.4-5 for regulation of deselect time.

  Deselect time can adjust in a chip select deselect bit (SCSTR3-2:CSDS[15:0]).

Figure 6.4-4. Timing adjustment (Normal transfer (SPI=0), SCINV=0)

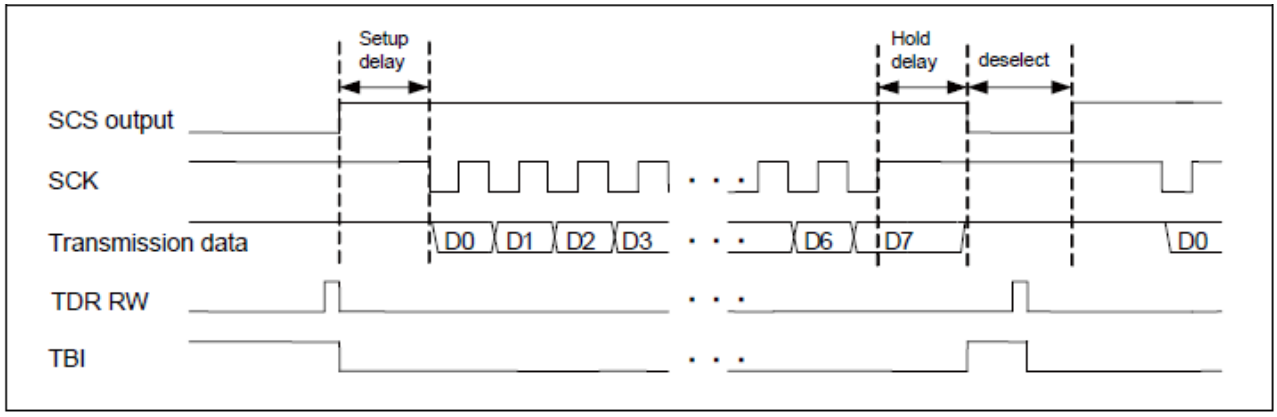
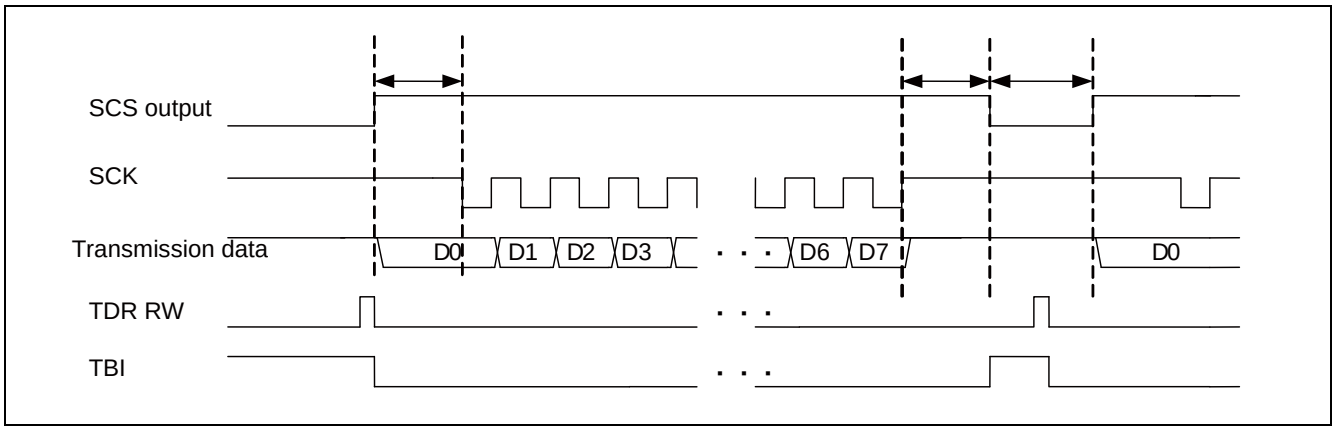


Figure 6.4-5. Timing adjustment (Normal transfer (SPI=1), SCINV=0)



Note

The normal transfer (SPI=0), when you have no hold delay time (SCSTR1:CSHD[7:0] = (0x00)), chip select pin may become inactive before the sampling of the last bit. In that case, increase and adjust the value of SCSTR1:CSHD[7:0].

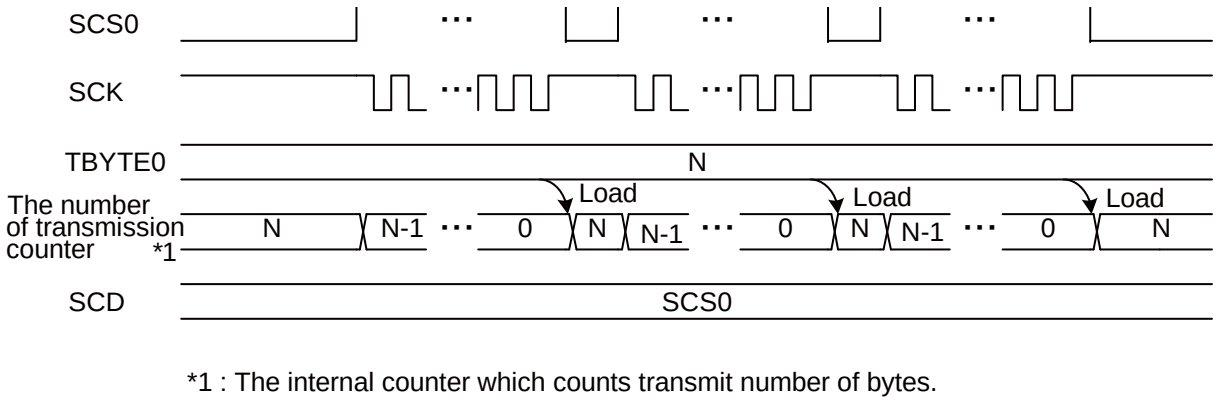
- ☐ Single operation of chip select pin (When only master mode (SCR:MS=0) is valid)

When serial chip select start bits (SCSCR:SST[1:0]) and serial chip select stop bits (SCSCR:SED [1:0]) are equal, it operates only with the set-up serial chip select pin.

The serial chip select pin becomes inactive for every data transmission and reception of the number of having set up by TBYTE, at serial chip select active no hold (SCSCR:SCAM=0).

As for serial chip select pin, see "**Serial Chip Select Active Hold Operation (SCSCR:SCAM=1) (When only master mode (SCR:MS=0) is valid)**" for the operation in serial chip select active hold (SCSCR:SCAM=1).

Figure 6.4-6. Single operation of chip select (SST[1:0]=0, SED1-0=0, CSEN0=1, SCAM=0)



Note

Timing adjustment (the setup time, hold time, deselect time) of serial chip select pin is effective at single operation.

☐ **Round operation of chip select pin (Only Master mode(SCR:MS=0) is valid)**

When serial chip select start bits (SCSCR:SST[1:0]) differs from serial chip select stop bits (SCSCR:SED[1:0]), two or more serial chip select pins become active in order.

1. It becomes active from the serial chip select pin which the serial chip select pin specified that it writes in transmit data Serial chip select output enable (SCSCR:CSOE=1) and during transmit enable (SCR:TXE=1) by the serial chip select start bits (SCSCR:SST[1:0]).
2. The serial chip select pin becomes inactive after the end of data transmit/reception of number setting to TBYTE, at serial chip select active no hold (SCSCR:SCAM=0). Then, the serial chip select pin made into the serial chip select pin number which became active in front +1 becomes active. *1
3. However, when the serial chip select pin which becomes active next is diable (SCSCR:CSENn=0), the serial chip select pin does not become active, but is skipped.
4. When the serial chip select pin specified by the serial chip select pin number which is active, and the serial chip select stop bit (SCSCR:SED [1:0]) is in agreement, the serial chip select pin which becomes next active turns into serial chip select pin specified by the serial chip select start bits (SCSCR:SST [1:0]).

   *1 : As for the case of the pin 3 and the pin 3, in the case of the pin 1 and the pin 1, in the case of the pin 2 and the pin 2, the pin 0 becomes active when the serial chip select which became active in front is the pin 0.

As for serial chip select pin, See "**Serial Chip Select Active Hold Operation (SCSCR:SCAM=1) (When only master mode (SCR:MS=0) is valid)**" for the operation in serial chip select active hold (SCSCR:SCAM=1).

Figure 6.4-7 is timing chart in case the start, pin of serial chip select pin is SCS0 (SST[1:0]=0) and end pin is SCS3 (SED[1:0]=3).

Figure 6.4-7. Round operation of chip select (SST[1:0]=0, SED[1:0]=3, CSEN3=1, CSEN2=1, CSEN1=1, CSEN0=1, SCAM=0)

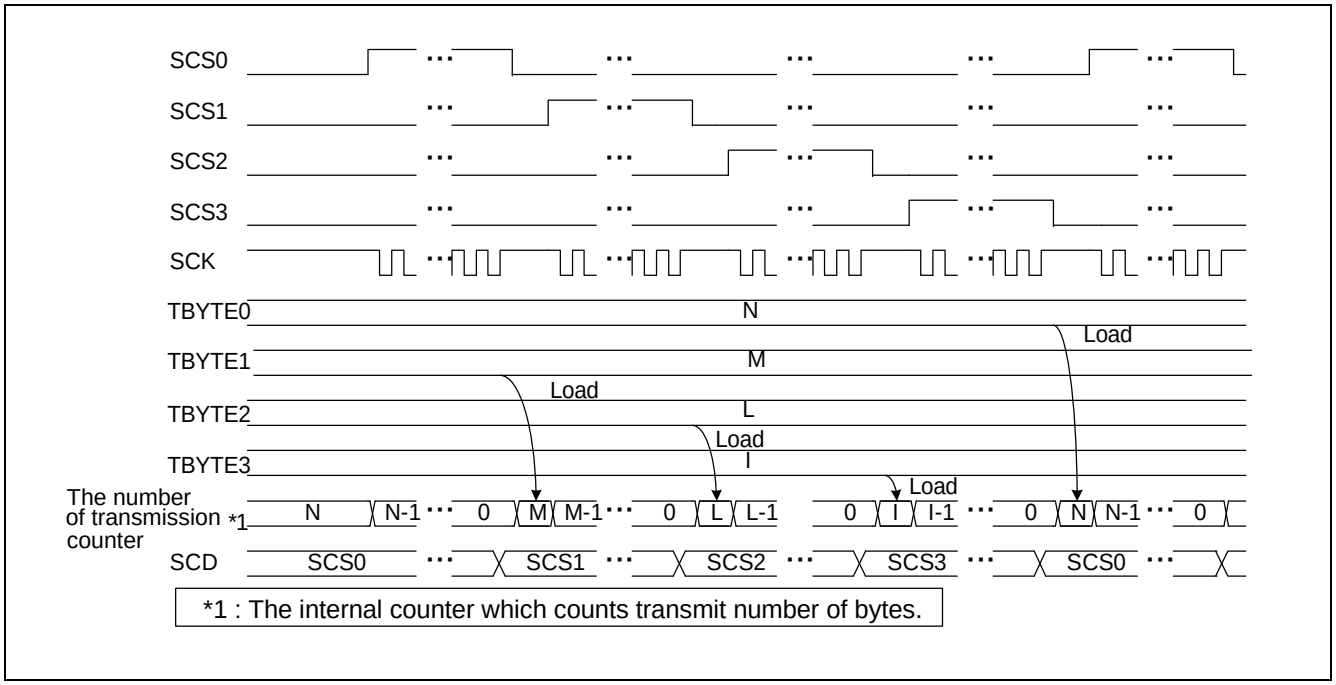
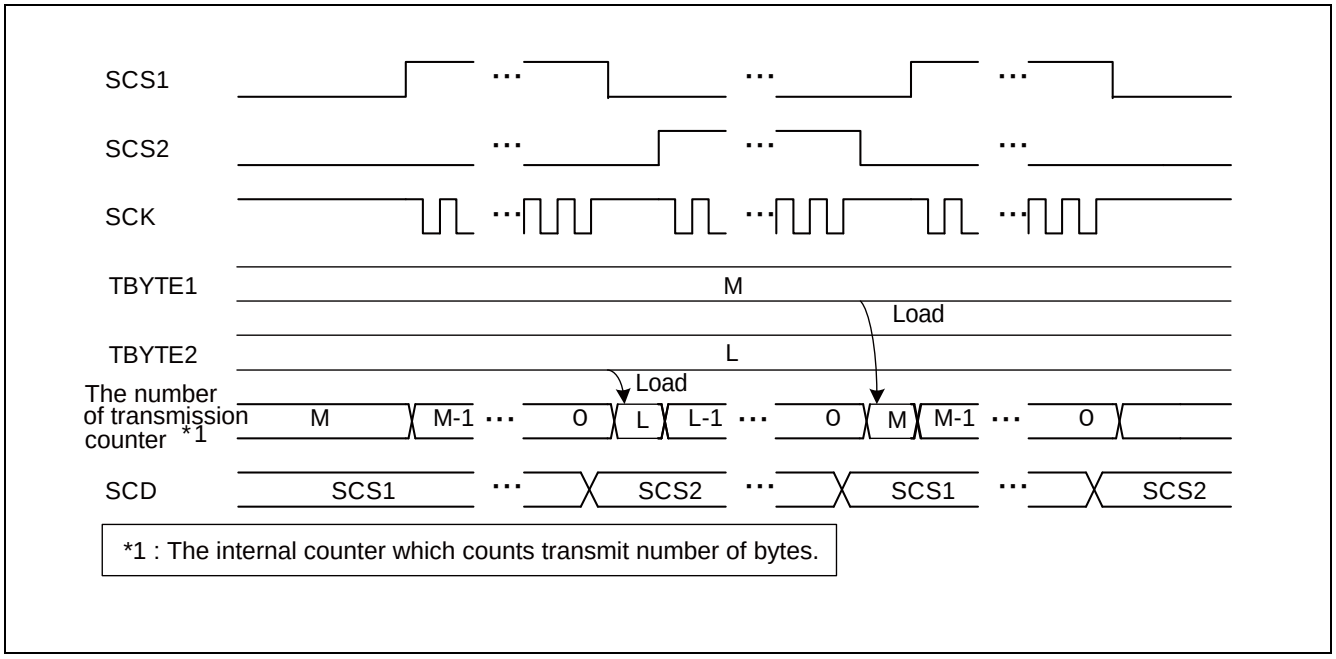


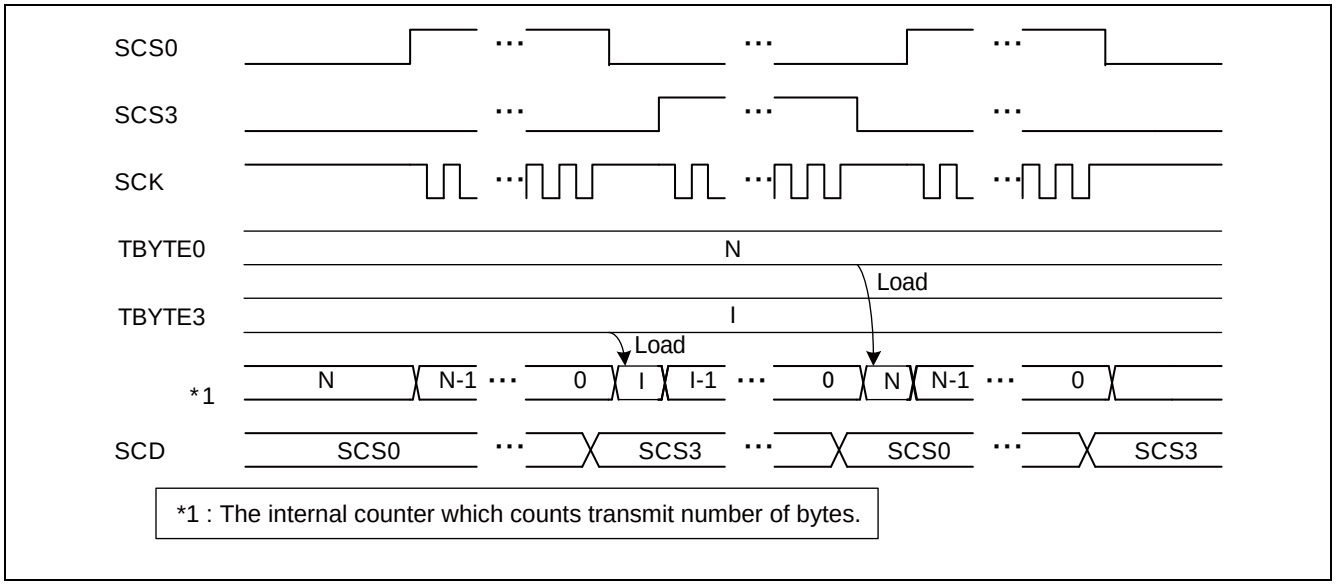
Figure 6.4-8 is timing chart in case, the start pin of serial chip select pin is SCS1 (SST[1:0]=1) and end pin is SCS2 (SED[1:0]=2).

Figure 6.4-8. Round operation of chip select (SST[1:0]=1, SED[1:0]=2, CSEN3=1, CSEN2=1, CSEN1=1, CSEN0=1, SCAM=0)



In case Figure 6.4-9 is a timing chart, the start pin of serial chip select pin is SCS0 (SST[1:0]=0) , end pin is SCS3 (SED[1:0]=3), and the chip select pins 1 and 2 are prohibition (CSEN [1:2] =0b00). As for serial chip select pin, the pin 0 becomes active, not the pins 1 and 2 but the pin 3 becomes active.

Figure 6.4-9. Round operation of chip select (SST[1:0]=0, SED[1:0]=3, CSEN3=1, CSEN2=0, CSEN1=0, CSEN0=1, SCAM=0)



Notes

- When it changes into transmit operation enable (SCR:TXE=1) from the transmit operation disable (SCR:TXE=0), it becomes active from the serial chip select pin specified by the serial chip select start bits (SCSCR:SST [1:0]).
- Timing adjustment (the setup time, hold time, and deselect time) of serial chip select pin is effective at round operation.
- The serial chip select pin becomes active from the serial chip select pin specified by the serial chip select start bits (SCSCR:SST [1:0]) after software reset (SCR:UPCL=1).

- **Serial Chip Select Active Hold Operation (SCSCR:SCAM=1) (When only master mode (SCR:MS=0) is valid)**

  When serial chip select active hold bit (SCSCR:SCAM) is set as "1" and transmit operation is started, serial chip select pin is held at active state.

Table 6.4-1. Serial chip select active hlod bit (SCSCR:SCAM)

Current state	Current SCSCR: SCAM bit	Current SSR: TDRE bit	Next state
Transmit (Number of transmit< TBYTE)	0	-	The serial chip select pin is active hold until it transmits the frame of the setup number of TBYTE
	1		
The end of transmit about the frame of the number setup of TBYTE	0		The serial chip select pin is inactive after hold delay time
	1	1	Active state hold of serial chip select
		0	At the active state of serial chip select, it is continuation of transmit operation Again, serial chip select pin is active hold until it transmits the frame of the setup number of TBYTE
Hold delay	0	-	The serial chip select pin is inactive after hold delay time
	0->1	1	Hold delay operation is interrupted and it is active state hold of serial chip select
		0	Hold delay operation is interrupted and it is restart transmit/reception operation at the active state of serial chip select Again, serial chip select pin is active hold until it transmits the frame of the number setup of TBYTE
Active state hold of serial chip select	1->0	-	The serial chip select pin is inactive after hold delay time
	1	1	Continuation of active state hold of serial chip select
		0	At the active state of serial chip select, it is restart of transmit operation Again, serial chip select pin is active hold until it transmits the frame of the number setup of TBYTE
Chip select error (SACSR:CSE=1) is occurs	-	-	Serial chip select pin is inactive, regardless of setup of SCAM after hold delay time
Software reset execute (SCR:UPCL=1)			Serial chip select pin immediately inactive, regardless of setup of SCAM
Transmit disable (SCR:TXE=0)			

Note

When data transmit/reception of the number of setting to TBYTE are not ended at transmit byte error enable (SACSR:TBEEN=1) and Transmit Data Register (TDR) is empty (SSR:TDRE=1), serial chip select pin is not held, but serial chip select pin becomes inactive after hold delay time progress, and it occurs chip select error (SACSR:CSE=1).

☐ **Format setting of serial chip select pins**

The active level of the chip select, the mark level of serial clock, enable/disable of SPI mode, the direction data of serial data output, and data length of each serial chip select pin can be set up in the bit shown in Table 6.4-2.

Table 6.4-2. Format setting of serial chip select pins

Condition		Active level of chip select	Invert of serial clock	SPI setting	Direction of data	Data length
Chip select format enable (SCR:CSFE=1) and Master mode (SCR:MS=0)	Serial chip select pin 0 output	SCSCR:SCLVL	SMR:SCINV	SCR:SPI	SMR:BDS	ESCR:L[3:0]
	Serial chip select pin 1 output	SCSFR0: CS0SCLVL	SCSFR0: CS0SCINV	SCSFR0: CS0SPI	SCSFR0: CS0BDS	SCSFR0: CS0L[3:0]
	Serial chip select pin 2 output	SCSFR1: CS1SCLVL	SCSFR1: CS1SCINV	SCSFR1: CS1SPI	SCSFR1: CS1BDS	SCSFR1: CS1L[3:0]
	Serial chip select pin 3 output	SCSFR2: CS2SCLVL	SCSFR2: CS2SCINV	SCSFR2: CS2SPI	SCSFR2: CS2BDS	SCSFR2: CS2L[3:0]
Chip select format disable (SCR:CSFE=0)		SCSCR:SCLVL	SMR:SCINV	SCR:SPI	SMR:BDS	ESCR:L[3:0]
Slave mode (SCR:MS=1)						
When Chip select is unused. (CSEN[3:0]=”0b0000”)						

6.5 Dedicated baud rate generator

The dedicated baud rate generator functions in the master mode operation only.

■ **CSIO (Clock Synchronous Serial Interface) baud rate selection**

The dedicated baud rate generator settings vary depending on the master or slave mode operation.

☐ **During master mode operation**

Divide the internal clock frequency using the dedicated baud rate generator, and select a baud rate.

- This generator provides two internal reload counters, which support transmitting and receiving serial clocks respectively. To select the baud rate, specify the 15-bit reload value using Baud Rate Generator Registers 1 and 0 (BGR1 and BGR0).
- The internal clock frequency is divided by the reload counter set value.

☐ **During slave mode operation**

The dedicated baud rate generator does not function in the slave mode operation (SCR:MS=1). (An external clock, entered from the SCK clock input pin, is used directly.)

6.5.1 Baud rate settings

This section explains how to set the baud rate. Also, the calculation result of serial clock frequency is shown.

- **Calculating the baud rate**

Two 15-bit reload counters are set using the Baud Rate Generator Registers 1 and 0 (BGR1 and BGR0). The baud rate is obtained in the following formulas.

(1) Reload value

$V = \phi / b - 1$

V : Reload value; b : Baud rate; ϕ: Bus clock frequency

(2) Calculation example

To set the 16 MHz bus clock, use the internal clock, and set the 19200 bps baud rate, set the reload value as follows:

Reload value:

$V = (16 \times 1000000) / 19200 - 1 = 832$

Therefore, the baud rate is:

$b = (16 \times 1000000) / (832 + 1) = 19208$ bps

(3) Baud rate error

The baud rate error can be calculated by the following equation.

Error (%) = (Calculated value – Target value) / Target value 100

Example: To set the 20 MHz bus clock and 153600 bps target baud rate:

Reload value = $(20 \times 1000000) / 153600 - 1 = 129$

Buad rate (Calculated value) = $(20 \times 1000000) / (129 + 1) = 153846$ (bps)

Notes

- If the reload value is set to "0", the reload counter is stopped.
- If the reload value is even, the "HIGH" and "LOW" width of serial clock changes as follows, depending on SMR:SCINV bit settings. If the value is odd, the serial clock has the same "HIGH" and "LOW" signal width.
  - ☐ SMR:SCINV="0" : The "HIGH" width of serial clock is longer for 1 cycle of bus clock.
  - ☐ SMR:SCINV="1" : The "LOW" width of serial clock is longer for 1 cycle of bus clock.
- Set the reload value to 3 or more.

- **Reload values and baud rates for each bus clock frequency**

Table 6.5-1. Reload Values and Baud Rates

Baud rate (bps)	8 MHz		10 MHz		16 MHz		20 MHz		24 MHz		32 MHz	
	Value	ERR	Value	ERR	Value	ERR	Value	ERR	Value	ERR	Value	ERR
8 M	-	-	-	-	-	-	-	-	-	-	3	0
6 M	-	-	-	-	-	-	-	-	3	0	-	-
5 M	-	-	-	-	-	-	3	0	-	-	-	-
4 M	-	-	-	-	3	0	4	0	5	0	7	0
2.5 M	-	-	3	0	-	-	-	-	-	-	-	-
2 M	3	0	4	0	7	0	9	0	11	0	15	0
1 M	7	0	9	0	15	0	19	0	23	0	31	0
500000	15	0	19	0	31	0	39	0	47	0	63	0
460800	-	-	-	-	-	-	-	-	51	-0.16	-	-
250000	31	0	39	0	63	0	79	0	95	0	127	0
230400	-	-	-	-	-	-	-	-	103	-0.16	-	-
153600	51	-0.16	64	-0.16	103	-0.16	129	-0.16	155	-0.16	207	-0.16
125000	63	0	79	0	127	0	159	0	191	0	255	0
115200	68	-0.64	86	0.22	138	0.08	173	0.22	207	-0.16	277	0.08
76800	103	-0.16	129	-0.16	207	-0.16	259	-0.16	311	-0.16	416	0.08
57600	138	0.08	173	0.22	277	0.08	346	-0.16	416	0.08	555	0.08
38400	207	-0.16	259	-0.16	416	0.08	520	0.03	624	0	832	-0.04
28800	277	0.08	346	<0.01	554	-0.01	693	-0.06	832	-0.03	1110	-0.01
19200	416	0.08	520	0.03	832	-0.03	1041	0.03	1249	0	1666	0.02
10417	767	<0.01	959	<0.01	1535	<0.01	1919	<0.01	2303	<0.01	3071	<0.01
9600	832	0.04	1041	0.03	1666	0.02	2083	0.03	2499	0	3332	-0.01
7200	1110	<0.01	1388	<0.01	2221	<0.01	2777	<0.01	3332	<0.01	4443	-0.01
4800	1666	0.02	2082	-0.02	3332	<0.01	4166	<0.01	4999	0	6666	<0.01
2400	3332	<0.01	4166	<0.01	6666	<0.01	8332	<0.01	9999	0	13332	<-0.01
1200	6666	<0.01	8334	0.02	13332	<0.01	16666	<0.01	19999	0	26666	<0.01
600	13332	<0.01	16666	<0.01	26666	<0.01	-	-	-	-	-	-
300	26666	26666	<0.01	-	-	-	-	-	-	-	-	-

- Value: BGR1/0 register set value
- ERR: Baud rate error (%)

- **Functions of reload counter**

There are two types of reload counter: the transmit reload counter and the received reload counter. They function as the dedicated baud rate generators. Each reload counter consists of a 15-bit register for the reload value, and generates transmitting and receiving clocks from internal clocks.

- **Starting counting**

When the reload value is written to the Baud Rate Generator Register (BGR1 or BGR0), the reload counter starts counting.

- **Restarting**

The reload counter restarts counting in the following conditions.

- ☐ **Common to transmit and received reload counters**

  A programmable reset (SCR:UPCL bit)

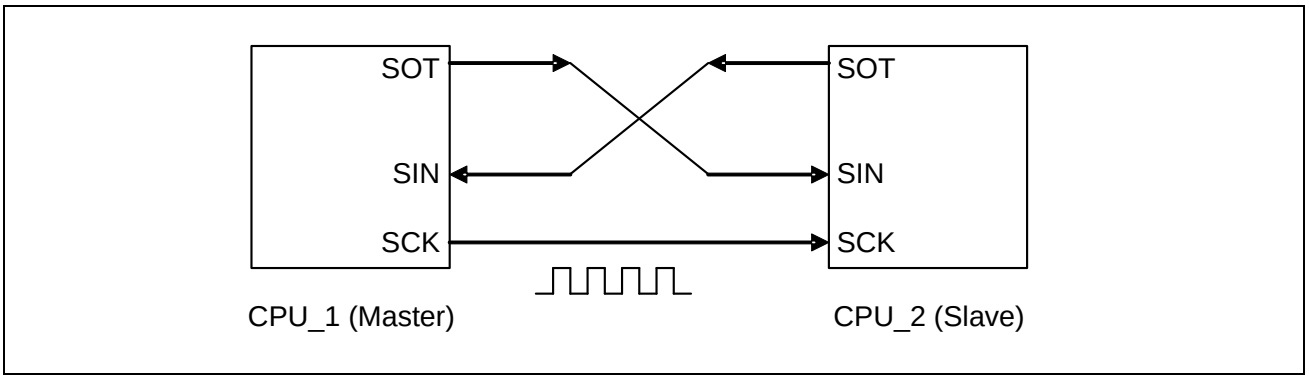
6.5.2 CSIO (Clock Synchronous Serial Interface) setup procedure and program flow

The CSIO (Clock Synchronous Serial Interface) allows bidirectional and synchronous serial data transmission.

- ☐ **CPU-to-CPU connection**

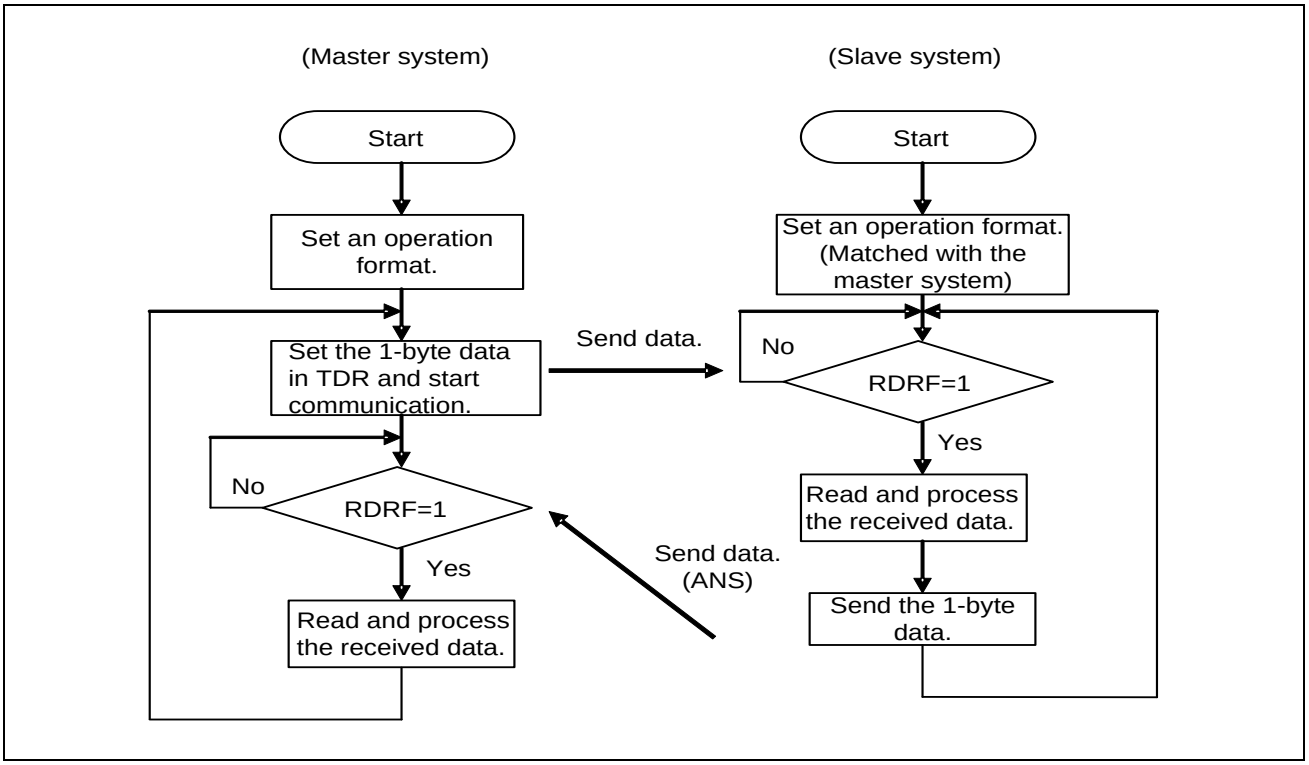
  Select the bidirectional communication for the CSIO (Clock Synchronous Serial Interface). Connect two CPUs to each other as shown in Figure 6.5-1.

Figure 6.5-1. Connection Example for CSIO (Clock Synchronous Serial Interface) Bidirectional Communication



- **Flowcharts**

Figure 6.5-2. Example of Bidirectional Communication Flowchart



6.6 CSIO (Clock Synchronous Serial Interface) registers

This section provides a list of CSIO (Clock Synchronous Serial Interface) registers.

- **CSIO (Clock Synchronous Serial Interface) register list**

Table 6.6-1. CSIO (Clock Synchronous Serial Interface) Register List

	bit15 bit8	bit7 bit0
CSIO	SCR (Serial Control Register)	SMR (Serial Mode Register)
	SSR (Serial Status Register)	ESCR (Extended Communication Control Register)
	RDR/TDR (Transmit/Received Data register)	
	SACSR (Serial Aid Control Status Register)	
	SCSCR (Serial Chip Select Control Status Register)	
	SCSTR1 (Serial Chip Select Timing Register 1)	SCSTR0 (Serial Chip Select Timing Register 0)
	SCSTR3 (Serial Chip Select Timing Register 3)	SCSTR2 (Serial Chip Select Timing Register 2)
	SCSFR1 (Serial Chip Select Format Register 1)	SCSFR0 (Serial Chip Select Format Register 0)
	-	SCSFR2 (Serial Chip Select Format Register 2)
	TBYTE1 (Transfer Byte Register 1)	TBYTE0 (Transfer Byte Register 0)
	TBYTE3 (Transfer Byte Register 3)	TBYTE2 (Transfer Byte Register 2)
	BGR1 (Baud Rate Generator Register 1)	BGR0 (Baud Rate Generator Register 0)
	-	-

Table 6.6-2. CSIO (Clock Synchronous Serial Interface) Bit Assignment

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SCR/ SMR	UPCL	MS	SPI	RIE	TIE	TBIE	RXE	TXE	MD2	MD1	MD0	WUCR	SCINV	BDS	SCKE	SOE
SSR/ ESCR	REC	Reserved			ORE	RDRF	TDRE	TBI	SOP	-	CSFE	WT1	WT0	L2	L1	L0
TDR/ RDR	-							D8	D7	D6	D5	D4	D3	D2	D1	D0
SACSR	Reserved		TBEEN	B12	CSE	-	-	-	-	-	-	-	-	-	-	-
SCSCR	SST1	SST0	SED1	SED0	SCD1	SCD0	SCAM	CDIV2	CDIV1	CDIV0	CSLVL	Reserved			CSEN0	CSOE
SCSTR0/1	CSSU7	CSSU6	CSSU5	CSSU4	CSSU3	CSSU2	CSSU1	CSSU0	CSHD7	CSHD6	CSHD5	CSHD4	CSHD3	CSHD2	CSHD1	CSHD0
SCSTR3/2	CSDS15	CSDS14	CSDS13	CSDS12	CSDS11	CSDS10	CSDS9	CSDS8	CSDS7	CSDS6	CSDS5	CSDS4	CSDS3	CSDS2	CSDS1	CSDS0
SCSFR1/0	CS2CSLVL	CS2SCINV	CS2SPI	CS2BDS	-	CS2L2	CS2L1	CS2L0	CS1CSLVL	CS1SCINV	CS1SPI	CS1BDS	-	CS1L2	CS1L1	CS1L0
SCSFR2									CS3CSLVL	CS3SCINV	CS3SPI	CS3BDS	-	CS3L2	CS3L1	CS3L0
TBYTE1/0	CS1TD7	CS1TD6	CS1TD5	CS1TD4	CS1TD3	CS1TD2	CS1TD1	CS1TD0	CS0TD7	CS0TD6	CS0TD5	CS0TD4	CS0TD3	CS0TD2	CS0TD1	CS0TD0
TBYTE3/2	CS3TD7	CS3TD6	CS3TD5	CS3TD4	CS3TD3	CS3TD2	CS3TD1	CS3TD0	CS2TD7	CS2TD6	CS2TD5	CS2TD4	CS2TD3	CS2TD2	CS2TD1	CS2TD0
BGR1/ BGR0	-	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
-	-								-							

6.6.1 Serial Control Register (SCR)

The Serial Control Register (SCR) is used to enable/disable a transmit/received interrupt, enable/disable transmit idle interrupt, and enable/disable data transmission and reception. Also, the register can set the SPI connection and reset the CSIO settings.

bit	15	14	13	12	11	10	9	8	7 ... 0
Field	UPCL	MS	SPI	RIE	TIE	TBIE	RXE	TXE	(SMR)
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

[bit15] UPCL: Programmable clear bit

Initializes the CSIO internal state.

If set to "1":

- The CSIO is reset directly (software reset). However, the current register settings are kept. The transmit or received state is disconnected immediately.
- The baud rate generator reloads the BGR1/0 register value and restarts operation.
- All of transmit/received interrupt factors (SSR:TDRE, TBI, RDRF, ORE and SACSR:CSE) are initialized.
- All serial chip select pin becomes inactive.

If set to "0":

No effect on the operation.

"0" is always read from this bit.

bit	Description	
	Writing	Reading
0	No effect on the operation.	"0" is always read.
1	Programmable clear	

Note

Disable an interrupt first, and then execute the programmable clear instruction.

[bit14] MS: Master/Slave function select bit

Selects the master or slave mode.

bit	Description
0	Master mode
1	Slave mode

Notes

- If the slave mode is selected and if SMR:SCKE=0, the external clock is entered directly.
- This bit sets, when transmission / reception are prohibition (TXE=RXE=0).
- After you have set the MS bit, enable data reception (RXE=1).

[bit13] SPI: SPI corresponding bit

This bit allows the SPI communication.

bit	Description
0	Normal synchronous transfer
1	SPI correspond

Notes

- This bit sets, when transmission / reception are prohibition (TXE=RXE=0).
- This bit is used by following either.
  - ☐ When chip select pin prohibition (SCSCR:CSEN [3:0] ="0b0000")
  - ☐ When slave mode (SCR:MS=1)
  - ☐ When data format prohibition (ESCR:CSFE=0) of chip select
  - ☐ When the serial chip select pin 0 is active at data format permission (ESCR:CSFE=1) of chip select

[bit12] RIE: Received interrupt enable bit

- This bit enables or disables an output of received interrupt request to the CPU.
- If the RIE bit and the received data flag bit (SSR:RDRF) are "1", or if any of error flag bits (ORE) is "1", a received interrupt request is output.

bit	Description
0	Disables the received interrupt.
1	Enables the received interrupt.

[bit11] TIE: Transmit interrupt enable bit

- This bit enables or disables an output of transmit interrupt request to the CPU.
- If the TIE and SSR:TDRE bits are "1", a transmit interrupt request is output.

bit	Description
0	Disables a transmit interrupt.
1	Enables a transmit interrupt.

[bit10] TBIE: Transmit bus idle interrupt enable bit

- This bit enables or disables an output of transmit bus idle interrupt request to the CPU.
- If the TBIE bit and SSR:TBI bit are "1", a transmit bus idle interrupt request is output.

bit	Description
0	Disables the transmit bus idle interrupt.
1	Enables the transmit bus idle interrupt.

[bit9] RXE: Data received enable bit

Enables or disables a CSIO data reception.

bit	Description
0	Disables data reception.
1	Enables data reception.

Notes

- If data reception is disabled (RXE=0), the current data reception is stopped immediately.
- After you have set the MS bit and SMR:SCINV bit, enable the data reception (RXE=1).

[bit8] TXE: Data transmission enable bit

Enables or disables a CSIO data transmission.

bit	Description
0	Disables the transmission.
1	Enables the transmission.

Note

If data transmission is disabled (TXE=0), the current data transmission is stopped immediately.

6.6.2 Serial Mode Register (SMR)

The Serial Mode Register (SMR) is used to select an operation mode, to set a transmission direction, data length and serial clock inversion, and to enable or disable an output of serial data and clock to their pins.

bit	15 ... 8	7	6	5	4	3	2	1	0
Field	(SCR)	MD2	MD1	MD0	WUCR	SCINV	BDS	SCKE	SOE
Attribute		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value		0	0	0	0	0	0	0	0

[bit7:5] MD2, MD1, MD0: Operation mode set bits

These bits set an operation mode.

"0b000": Sets operation mode 0 (asynchronous normal mode).
"0b001": Sets operation mode 1 (asynchronous multiprocessor mode).
"0b010": Sets operation mode 2 (clock synchronous mode).
"0b011": Sets operation mode 3 (LIN communication mode).
"0b100": Sets operation mode 4 (I^2C mode).

*This chapter explains the registers and their operation in operation mode 2 (clock synchronous mode).

bit7	bit6	bit5	Description
0	0	0	Operation mode 0 (asynchronous normal mode)
0	0	1	Operation mode 1 (asynchronous multiprocessor mode)
0	1	0	Operation mode 2 (clock synchronous mode)
0	1	1	Operation mode 3 (LIN communication mode)
1	0	0	Operation mode 4 (I^2C mode)
Values other than the above			Setting is prohibited.

Notes

- Any bit setting other than above is inhibited.
- To switch the current operation mode, issue a programmable clear instruction (SCR:UPCL=1) and switch the operation mode continuously.
- After the operation mode has been set, set each register correctly.

[bit4] WUCR: Wake-up control bit

This bit selects a pin to be used for an external interrupt.

If set to "0": The INT pin is set as an external interrupt pin.
If set to "1": The SCK pin is set as an external interrupt pin.

bit	Description
0	Disables the Wake-up function.
1	Enables the Wake-up function.

[bit3] SCINV: Serial clock invert bit

This bit inverts the serial clock format. When master mode (SCR:MS=0) and chip select is used, this bit used communication of serial chip select pin 0.

If set to "0":

- The signal mark level of serial clock output is set to "HIGH".
- The transmit data is output at a falling edge of serial clock during normal transfer, but it is output in synchronization with a rising edge of serial clock during SPI transfer.
- The received data is sampled at a rising edge of serial clock during normal transfer, but it is sampled at a falling edge of serial clock during SPI transfer.

If set to "1":

- The signal mark level of serial clock output is set to "LOW".
- The transmit data is output at a rising edge of serial clock during normal transfer, but it is output in synchronization with a falling edge of serial clock during SPI transfer.
- The received data is sampled at a falling edge of serial clock during normal transfer, but it is sampled at a rising edge of serial clock during SPI transfer.

bit	Description
0	Signal mark level "HIGH" format
1	Signal mark level "LOW" format

Notes

- This bit sets, when serial clock output is prohibition (SCKE=0)
- After you have set the SCINV bit, enable data reception (SCR:RXE=1).
- This bit is used by following either.
  - ☐ When chip select pin prohibition (SCSCR:CSEN [3:0] ="0b0000")
  - ☐ When slave mode (SCR:MS=1)
  - ☐ When data format prohibition (ESCR:CSFE=0) of chip select
  - ☐ When the serial chip select pin 0 is active at data format permission (ESCR:CSFE=1) of chip select

[bit2] BDS: Transfer direction select bit

Specifies to transfer the least significant bit of the transfer serial data first (LSB first; BDS=0) or the most significant bit first (MSB first; BDS=1). When master mode (SCR:MS=0) and chip select is used, this bit used communication of serial chip select pin 0.

bit	Description
0	LSB first (The least significant bit is first transferred.)
1	MSB first (The most significant bit is first transferred.)

Notes

- This bit sets, when transmission / reception are prohibition (TXE=RXE=0).
- This bit is used by following either.
  - ☐ When chip select pin prohibition (SCSCR:CSEN [3:0] ="0b0000")
  - ☐ When slave mode (SCR:MS=1)
  - ☐ When data format prohibition (ESCR:CSFE=0) of chip select
  - ☐ When the serial chip select pin 0 is active at data format permission (ESCR:CSFE=1) of chip select.

[bit1] SCKE: Master mode serial clock output enable bit

This bit controls the serial clock I/O port.

If set to "0" : SCK pin is GPIO port or serial clock input pin.

If set to "1" : It becomes a serial clock output pin and outputs clock during transmitting operation.

bit	Description
0	Selects GPIO port or serial clock input.
1	Selects serial clock output.

Notes

- When you use a SCK pin as serial clock input (SCKE=0), sets GPIO port as input port.
- Set to serial clock output permission (SCKE=1) after SCINV bit setup.

[Reference]
When the SCK pin is set as the serial clock output (SCKE=1), it functions as serial clock output pin irrespective of a setup of GPIO port (DDR).

[bit0] SOE: Serial data output enable bit

This bit enables or disables a serial data output.

If set to "0" : SOT pin is GPIO port.

If set to "1" : SOT pin is serial data output pin (SOT).

bit	Description
0	Enables GPIO port.
1	Enables serial data output.

[Reference]
In the case of serial data output (SOE=1), SOT pin functions as SOT pin irrespective of setup of GPIO port (DDR).

6.6.3 Serial Status Register (SSR)

The Serial Status Register (SSR) is used to check the current transmission/reception state, check the Received Error flag, and clear the Received Error flag.

bit	15	14	13	12	11	10	9	8	7 ... 0
Field	REC	Reserved			ORE	RDRF	TDRE	TBI	(ESCR)
Attribute	R/W	-			R	R	R	R	
Initial value	0	000			0	0	1	1	

[bit15] REC: Received error flag clear bit

This bit clears the ORE flag of the Serial Status Register (SSR).

- If this bit is set to "1", the error flag is cleared.
- This bit has no effect on the operation if set to "0".

"0" is always read.

bit	Description	
	At writing	At reading
0	No effect on the operation.	"0" is always read.
1	Clears the Received Error flag (FRE, ORE).	

[bit14:12] Reserved : Reserved bits

When read : The read value is undefined.
When write : This bit has no effect on the operation.

[bit11] ORE: Overrun error flag bit

- If an overrun occurs during data reception, this bit is set to "1". This is cleared if the REC bit of Serial Status Register (SSR) is set to "1".
- If the ORE and SCR:RIE bits are "1", a received interrupt request is output.
- If this flag is set, data of the Received Data Register (RDR) is invalid.

bit	Description
0	No overrun error occurred.
1	An overrun error occurred.

[bit10] RDRF: Received data full flag bit

- This flag shows the state of Received Data Register (RDR).
- When the received data is loaded in the RDR, this bit is set to "1". When data is read from the Received Data Register (RDR), this bit is cleared to "0".
- If the RDRF bit and SCR:RIE bit are "1", a received interrupt request is output.

bit	Description
0	The Received Data Register (RDR) is empty.
1	The Received Data Register (RDR) contains data.

[bit9] TDRE: Transmit data empty flag bit

- This flag shows the state of Transmit Data Register (TDR).
- If transmit data is written in the TDR, this bit is set to "0" to indicate that the TDR contains valid data. When data is loaded to the transmit shift register and when the transmission is started, this bit is set to "1" to indicate that the TDR does not have the valid data. If the TDRE bit and SCR:TIE bit are "1", a transmit interrupt request is output.

bit	Description
0	The Transmit Data Register (TDR) contains data.
1	The Transmit Data Register (TDR) is empty.

[bit8] TBI: Transmit bus idle flag bit

- This bit indicates that the CSIO is not transmitting data.
- When data is written in the Transmit Data Register (TDR), this bit is set to "0".
- If the Transmit Data Register (TDR) is empty (TDRE=1) and if no transmission is started, this bit is set to "1".
- When the UPCL bit of the Serial Control Register (SCR) is set to "1", the TDRE bit is set to "1".
- If this bit is "1" and if a transmit bus Idle interrupt is enabled (SCR:TBIE=1), a transmit interrupt request is output.

bit	Description
0	During data transmission
1	No data transmission

Note

This bit is set to "1" when transmit data register (TDR) is empty (TDRE=1), and serial chip select error (CSE=1) occurs.

6.6.4 Extended Communication Control Register (ESCR)

The Extended Communication Control Register (ESCR) is used to set a transmit/received data length and to fix the serial data output to the "HIGH" state.

bit	15 ... 8	7	6	5	4	3	2	1	0
Field	-	SOP	-	CSFE	WT1	WT0	L2	L1	L0
Attribute		R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Initial value		0	-	0	0	0	0	0	0

[bit7] SOP: Serial output pin set bit

- This bit sets the serial data output pin to the "HIGH" state. When this bit is set to "1", the SOT pin is set to "HIGH". After that, this bit needs not be set to "0".
- When it is read, "0" is always read.

bit	Description	
	At writing	At reading
0	No effect on the operation.	"0" is always read.
1	Sets the SOT pin to "HIGH" state.	

Note

Do not set this bit during serial data transmission.

[bit6] - : Unused bit

When read : The read value is undefined.
When write : This bit has no effect on the operation.

[bit5] CSFE : Data transmit/received wait select bits

This bit carries out permission or prohibition for a format setup for every serial chip select pin. When this bit is set as "1", the following setup is performed for every serial chip select pin.

- The inactive level of serial chip select
- The mark level of serial clock
- Selection of SPI transmission / normal transmission
- The transmission direction of serial data
- Data length of serial data

bit	Description
0	The same data format and clock format are set up with all the serial chip select pins.
1	A data format and clock format are set up for every serial chip select pin..

Note

In one of the following cases, a setup of this bit is invalid.

- When chip select pin prohibition (SCSCR:CSEN [3:0] ="0b0000")
- When slave mode (SCR:MS=1)

[bit4:3] WT1, WT0: Data transmit/received wait select bits

In master operation mode, these bits set a wait count for continuous data transmission or reception. In slave operation mode, these bits are set to "00".

- When these bits set as "00" : SCK is outputted continuously.
- When these bits set as "01" : SCK is outputted after 1-bit time wait.
- When these bits set as "10" : SCK is outputted after 2-bit time wait.
- When these bits set as "11" : SCK is outputted after 3-bit time wait.

bit4	bit3	Description
0	0	0 bit
0	1	1 bit
1	0	2 bits
1	1	3 bits

[bit2:0] L2, L1, L0: Data length select bits

These bits set a length of transmit/received data. This bit used for communication of the serial chip select pin 0 by master mode (SCR:MS=0) at chip select use.

bit2	bit1	bit0	Description
0	0	0	8-bit length
0	0	1	5-bit length
0	1	0	6-bit length
0	1	1	7-bit length
1	0	0	9-bit length
Values other than the above			Setting is prohibited.

Notes:

- Any bit setting other than above is inhibited.
- This bit is used by following either.
  - ☐ When chip select pin prohibition (SCSCR:CSEN [3:0] ="0b0000")
  - ☐ When slave mode (SCR:MS=1)
  - ☐ When data format prohibition (ESCR:CSFE=0) of chip select
  - ☐ When the serial chip select pin 0 is active at data format permission (ESCR:CSFE=1) of chip select

6.6.5 Received Data Register/Transmit Data Register (RDR/TDR)

The Received and Transmit Data Registers are allocated at the same address. This register functions as the Received Data Register when data is read from it. This register functions as the Transmit Data Register when data is written in it.

- **Received Data Register (RDR)**

bit	15 ... 9	8	7	6	5	4	3	2	1	0
Field		D8	D7	D6	D5	D4	D3	D2	D1	D0
Attribute		R	R	R	R	R	R	R	R	R
Initial value		0	0	0	0	0	0	0	0	0

The Received Data Register (RDR) is a 9-bit data buffer register for serial data reception.

- ☐ When serial data signals are sent to the Serial input pin (SIN), they are converted by a shift register and stored in the Received Data Register (RDR).
- ☐ The high-order bits are sequentially set to "0" according to the data length as follows.

Data length	D8	D7	D6	D5	D4	D3	D2	D1	D0
9 bits	X	X	X	X	X	X	X	X	X
8 bits	0	X	X	X	X	X	X	X	X
7 bits	0	0	X	X	X	X	X	X	X
6 bits	0	0	0	X	X	X	X	X	X
5 bits	0	0	0	0	X	X	X	X	X

- ☐ When the received data is stored in the Received Data Register (RDR), the received data full flag bit (SSR:RDRF) is set to "1". If a received interrupt is enabled (SCR:RIE=1), a received interrupt request is generated.
- ☐ The Received Data Register (RDR) must be read only when the received data full flag bit (SSR:RDRF) is "1". When data is read from the Serial Received Data Register (RDR), the received data full flag bit (SSR:RDRF) is cleared to "0" automatically.
- ☐ If a received error occurs (SSR:ORE), data in the Received Data Register (RDR) is invalid.
- ☐ When the 9-bit length data is transferred, the RDR must be read in the 16-bit access mode.

■ Transmit Data Register (TDR)

bit	15 ... 9	8	7	6	5	4	3	2	1	0
Field		D8	D7	D6	D5	D4	D3	D2	D1	D0
Attribute		W	W	W	W	W	W	W	W	W
Initial value		1	1	1	1	1	1	1	1	1

The Transmit Data Register (TDR) is a 9-bit data buffer register for serial data transmission.

- ☐ If data transmission is enabled (SCR:TXE=1) and if the transmit data is written in the Transmit Data Register (TDR), the transmit data is transferred to the transmit shift register. Then, the data is converted into serial data, and output at the serial data output pin (SOT).
- ☐ The high-order bits are sequentially set to invalid data according to the data length as follows.

Data length	D8	D7	D6	D5	D4	D3	D2	D1	D0
9 bits	X	X	X	X	X	X	X	X	X
8 bits	Invalid	X	X	X	X	X	X	X	X
7 bits	Invalid	Invalid	X	X	X	X	X	X	X
6 bits	Invalid	Invalid	Invalid	X	X	X	X	X	X
5 bits	Invalid	Invalid	Invalid	Invalid	X	X	X	X	X

- ☐ When the transmit data is written in the Transmit Data Register (TDR), the transmit data empty flag (SSR:TDRE) is cleared to "0".
- ☐ A transmit data empty flag (SSR:TDRE) will be set as "1", if transmi data is transmitted to the shift register for transmission and transmission is started.
- ☐ If the transmit data empty flag (SSR:TDRE) is "1", the next transmit data can be written in the buffer. If a transmit interrupt is enabled, a transmit interrupt occurs. The next transmit data must be written only after the transmit interrupt has occurred or when the transmit data empty flag (SSR:TDRE) is "1".
- ☐ When transmit data empty flag (SSR:TDRE) is "0", transmit data cannot be written in a transmit data register (TDR).
- ☐ When the 9-bit length data is transferred, data must be written in the TDR in the 16-bit access mode.

Note

The Transmit Data Register is a write-only register. While the Received Data Register is a read-only register. As these two registers are allocated at the same address, the write and read values differ from each other. Therefore, the INC/DEC instruction and other read-modify-write (RMW) operation cannot be used.

- **Relation between transmit data register (TDR) and transmit data empty flag**

In 16-bit access, TDR register becomes 16 bit boundaries and 16 bits of transmit data are stored at time in one writing. Moreover, when TDR register has 32-bit transmit data, transmit data empty flag (SSR:TDRE) is set to "0".

In 32-bit access, TDR register becomes 32 bit boundaries and 32 bits of transmit data are stored at time in one writing.

Table 6.6-3. Relation Between Transmit Data Register (TDR) and Transmit Data Empty Flag

Data access width	Data length	The number of TDR register stored data	TBI flag	TDRE flag	Transmission
16-bit access	5 bits to 16 bits	0 bit	1	1	NoTransmission
		16 bit	0		Enables Transmission
		32 bit		0	
	20 bits, 24 bits, 32 bits	0 bit	1	1	NoTransmission
		32 bit	0		Enables Transmission
				0	
32-bit access	All bit	0 bit	1	1	NoTransmission
		32 bit	0	0	Enables Transmission

6.6.6 Serial Aid Control Status Register (SACSR)

The serial aid control status register (SACSR) can perform a setup of enable/disable of each error.

bit	15	14	13	12	11	10	9	8
Field	Reserved		TBEEN	CSEIE	CSE	-	-	-
Attribute	-		R/W	R/W	R/W	-	-	-
Initial value	00		0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Field	-	-	-	-	-	-	-	-
Attribute	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

[bit15:14] Reserved : Reserved bits

When read : The read value is "0".
When write: Be sure to write "0".

[bit13] TBEEN: Transfer Byte Error Enable bit

When there is no transmit data effective in transmit data register (TDR) when only the number of frames smaller than the preset value of TBYTE has transmitted at master mode (SCR:MS=0) in one of the following cases and one-frame transmission is completed (SSR:TDRE), The existence of generating of serial chip select error is chosen.

- When chip select use
- When the transmit starting use by an external trigger

bit	Description
0	Disables chip select error generating at master mode (SCR:MS=0)
1	Enables chip select error generating at master mode (SCR:MS=0)

Note

This bit can change only when transmission / reception are prohibition (SCR:TXE=RXE=0).

[bit12] CSEIE: Chip Select Error Interrupt Enable bit

- This bit enables / disables chip select error interrupt request output.
- When the CSEIE bit and chip select error flag bit (CSE) are "1", transmit interrupt request is outputted.

bit	Description
0	Disables chip select error interrupt
1	Enables chip select error interrupt

[bit11] CSE: Chip Select Error Flag bit

In one of the following cases, by transmission byte error permission (TBEEN=1) at the time of master mode (SCR:MS=0), When only the number of frames smaller than the preset value of TBYTE has transmitted, one-frame transmission is completed and there is no send data effective in a transmitting data register (TDR) (SSR:TDRE=1), this bit is set as "1".

- When chip select use
- When the transmit starting use by an external trigger

When serial chip select pin becomes inactive during transmit operation (SSR:TBI=0) at slave mode (SCR:MS=1), this bit is set as "1" .
This bit outputs transmit interrupt request, when this bit is "1" and chip select error interrupt enable bit (CSEIE) are "1".

It will be reset by "0" if "0" is written in this bit.
"1" writing to this bit does no effect on operation.

bit	Description
0	No ocurr of chip select error
1	Ocurr of chip select error

[bit10:0] Reserved : Reserved bits

When read : The read value is "0".
When write: Be sure to write "0".

Notes

- This bit will be reset by "0" if software reset (SCR:UPCL=1) is performed.
- As for read of read-modified-write instruction, "1" is read.
- This bit is not set to "1" by slave mode (SCR:MS=1) at serial chip select unused (SCSCR:CSEN0= 0).
- Write "0" in this bit after setting transmission as prohibition (SCR:TXE=0) at chip select error generating (CSE=1). When you make transmission resume, write "0" in this bit and the back writes in transmit data to transmit enable (SCR:TXE=1) and a transmit data buffer (TDR).
- It is 1 to serial chip select input at slave transmission. When the noise more than a bus clock occurs, this bit may be set as "1". Resume transmission after the end of transmission of a master then.

6.6.7 Serial Chip Select Control Status Register (SCSCR)

Serial chip select control status register (SCSCR), Selection of the start pin of serial chip select and an end pin, the display of the output pin of serial chip select, maintenance of the active level of serial chip select, reversal of serial chip select, and output enable / disable of serial chip select pin are set up.

bit	15	14	13	12	11	10	9	8
Field	SST1	SST0	SED1	SED0	SCD1	SCD0	SCAM	CDIV2
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	00		0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Field	CDIV1	CDIV0	CSLVL	Reserved			CSEN0	CSOE
Attribute	R/W	R/W	R/W	-			R/W	R/W
Initial value	0	0	1	-			0	0

[bit15:14] SST[1:0] : Serial chip Select Start bits

These bits choose the pin which serial chip select starts.

When transmit enable (SCR:TXE=1) is used from the transmit disable (SCR:TXE=0), it becomes active from the serial chip select pin set up in this bit.

bit15	bit14	Start pin
0	0	SCS0 (Connects with SCSO)
0	1	Setting is prohibited.
1	0	Setting is prohibited.
1	1	Setting is prohibited.

Notes

- This bit can change only when transmission / reception are prohibition (SCR:TXE=RXE=0).
- When the same value as serial chip select start bits (SST1, SST0) and serial chip select stop bits (SED1, SED0) is set up, only the set-up serial chip select pin becomes active.
- A setup of these bits are invalid at slave mode (SCR:MS=1).
- Only the serial chip select pin by which serial chip select enable (CSEN=1) is carried out becomes active.

[bit13:12] SED[1:0] :Serial chip select End bits

These bits choose the pin which serial chip select end.

If even the serial chip select pin set up in this bit becomes active, the serial chip select pin which becomes active next will turn into a terminal specified by the serial chip select start bits (SST1, SST0).

bit13	bit12	End pin
0	0	SCS0 (Connects with SCSO)
0	1	Setting is prohibited.
1	0	Setting is prohibited.
1	1	Setting is prohibited.

Notes

- This bit can change only when transmission / reception are prohibition (SCR:TXE=RXE=0).
- When the same value as serial chip select start bits (SST1, SST0) and serial chip select stop bits (SED1, SED0) is set up, only the set-up serial chip select pin becomes active.
- A setup of these bits are invalid at slave mode (SCR:MS=1).
- Only the serial chip select pin by which serial chip select enable (CSEN=1) is carried out becomes active.

[bit11:10] SCD[1:0] : Serial Chip select Display bits

These bits display the pin in which the serial chip select pin is active.

bit11	bit10	Display pin
0	0	SCS0 (Connects with SCSO)
0	1	Setting is prohibited.
1	0	Setting is prohibited.
1	1	Setting is prohibited.

Notes

- When serial chip select pin is inactive, the serial chip select pin which becomes active next is displayed.
- These bits are set to "0b00" at transmission disable (SCR:TXE="0") on slave mode (SCR:MS=1), software reset (SCR:UPCL=1).

[bit9] SCAM: Serial Chip Select Active Maintenance bit

This bit chooses maintenance of the active state of a serial chip select pin, or un-holding.

When this bit is set to "1", even if it ends transmitting operation after serial chip select pin becomes active (SSR:TBI=1), serial chip select pin does not become inactive.

A serial chip select pin is active, and when this bit is "1" and it sets to this bit "0", a serial chip select pin becomes inactive after the end of transmitting.

bit	Description
0	The active state of serial chip select pin is not held.
1	The active state of serial chip select pin is held.

Notes

- In the transmission disable (SCR:TXE="0"), and software reset (SCR:UPCL="1"), regardless of the value of this bit, serial chip select pin becomes inactive.
- Regardless of the value of this bit, serial chip select pin becomes inactive at serial chip error generating (SACSR:CSE=1).

[bit8:6] CDIV [2:0] : serial chip select timing operation Clock Dividing bits

These bits set up the dividing ratio of a serial chip select timing operation clock.

bit8	bit7	bit6	Serial chip select timing operation clock						
			Divide ratio	ϕ= 8 MHz	ϕ= 10 MHz	ϕ= 16 MHz	ϕ= 20 MHz	ϕ= 24 MHz	ϕ= 32 MHz
0	0	0	ϕ	125 ns	100 ns	62.5 ns	50 ns	41.67 ns	31.25 ns
0	0	1	ϕ/2	250 ns	200 ns	125 ns	100 ns	83.33 ns	62.5 ns
0	1	0	ϕ/4	500 ns	400 ns	250 ns	200 ns	166.67 ns	125 ns
0	1	1	ϕ/8	1 µs	800 ns	500 ns	400 ns	333.33 ns	250 ns
1	0	0	ϕ/16	2 µs	1.6 µs	1 µs	800 ns	666.67 ns	500 ns
1	0	1	ϕ/32	4 µs	3.2 µs	2 µs	1.6 µs	1.33 µs	1 µs
1	1	0	ϕ/64	8 µs	6.4 µs	4 µs	3.2 µs	2.67 µs	2 µs

ϕ : Bus clcock

Notes

- These bits can change only when transmission / reception are prohibition (SCR:TXE=RXE=0).
- A setup of these bits are invalid at slave mode (SCR:MS=1).
- These bits are prohibition except setup of the above-mentioned table.

[bit5] CSLVL : serial Chip Select Level Setting bit

This bit chooses the level at inactive of serial chip select pin as "H" or "L."

This bit is used by communication of the chip select pin 0.

bit	Description
0	Selects inactive level "L"
1	Selects inactive level "H"

Notes

- This bit can change only when transmission / reception are prohibition (SCR:TXE=RXE=0).
- This bit is used by following either.
  - ☐ When slave mode (SCR:MS=1)
  - ☐ When data format prohibition (ESCR:CSFE=0) of chip select
  - ☐ When the serial chip select pin 0 is active at data format permission (ESCR:CSFE=1) of chip select

[bit4:2] Reserved : Reserved bits

When read : The read value is undefined.
When write : This bit has no effect on the operation.

[bit1] CSEN0 : serial Chip Select Enable bit

These bits choose enable or disable of each serial chip select pin.

In the case of slave mode (SCR:MS=1), enable or disable of serial chip pin is set up by the CSEN0 bit.

bit	Description
0	Disables operation of serial chip select pin
1	Enables operation of serial chip select pin

Notes

- This bit can change only when transmission / reception are prohibition (SCR:TXE=RXE=0).
- When the CSEN0 bit is set as "0" at master mode (SCR:MS=0), itransmit /reception operation is performed without being dependent on serial chip select pin.
- When the CSEN0 bit is set as "0" at slave mode (SCR:MS=1), transmit /reception operation is performed without being dependent on serial chip select pin.

[bit0] CSOE : serial Chip Select Output Enable bit

This bit chooses enable or disable of each serial chip select pin.

bit	Description
0	Disables output of serial chip select pin
1	Enables output of serial chip select pin

Notes

- This bit can change only when transmission / reception are prohibition (SCR:TXE=RXE=0).
- This bit set as "0" at slave mode (SCR:MS=1).

6.6.8 Serial Chip Select Timing Register (SCSTR3 to SCSTR0)

Serial chip select timing register (SCSTR3 to SCSTR0) sets up the setup delay time of serial chip select, the hold delay time of serial chip select, and the deselect time of serial chip select.

- **Bit configuration of serial chip select timing register (SCSTR3 to SCSTR0)**
  - ☐ **Bit configuration of serial chip select timing register (SCSTR1, SCSTR0)**

bit	15	14	13	12	11	10	9	8
Field	CSSU7	CSSU6	CSSU5	CSSU4	CSSU3	CSSU2	CSSU1	CSSU0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Field	CSHD7	CSHD6	CSHD5	CSHD4	CSHD3	CSHD2	CSHD1	CSHD0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit15:8] CSSU[7:0] : serial Chip Select Set-Up delay bits

These bits set up time after serial chip select pin becomes active until a serial clock is outputted. When "0x00" are set to these bits, the timing to which a serial clock is outputted, and the timing to which serial chip select pin becomes active become simultaneous.

bit15:8	Set-up delay time
00000000	Setting is prohibited.
00000001	1× serial chip select timing operation clock
00000010	2× serial chip select timing operation clock
. .	. .
11111110	254× serial chip select timing operation clock
11111111	255× serial chip select timing operation clock

Notes

- These bits can change only when transmission / reception are prohibition (SCR:TXE=RXE=0).
- A setup of these bits are invalid at slave mode (SCR:MS=1).
- These bits are disable "0x00".

[bit7:0] CSHD[7:0] : serial Chip Select Hold delay bits

These bit set up time after the output of serial clock is completed until serial chip select pin becomes inactive.

bit7:0	Hold delay time
00000000	Setting is prohibited.
00000001	1× serial chip select timing operation clock
00000010	2× serial chip select timing operation clock
. .	. .
11111110	254× serial chip select timing operation clock
11111111	255× serial chip select timing operation clock

Notes

- These bits can change only when transmission / reception are prohibition (SCR:TXE=RXE=0).
- A setup of these bits are invalid at slave mode (SCR:MS=1).
- These bits are disable "0x00".

☐ **Bit configuration of serial chip select timing register (SCSTR3, SCSTR2)**

bit	15	14	13	12	11	10	9	8
Field	CSDS15	CSDS14	CSDS13	CSDS12	CSDS11	CSDS10	CSDS9	CSDS8
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	00		0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Field	CSDS7	CSDS6	CSDS5	CSDS4	CSDS3	CSDS2	CSDS1	CSDS0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

[bit15:0] CSDS[15:0] : serial Chip Deselect bits

These bits set up minimum time after a serial chip select pin becomes inactive until serial chip select pin next becomes active.

bit15:0	Deselect minimum time
0x0000	No deselect minimum time (five bus clock time)
0x0001	1 × serial chip select timing operation clock
0x0002	2 × serial chip select timing operation clock
. .	. .
0xFFFE	65534 × serial chip select timing operation clock
0xFFFF	65535 × serial chip select timing operation clock

Notes

- These bits can change only when transmission / reception are prohibition (SCR:TXE=RXE=0).
- A setup of these bits are invalid at slave mode (SCR:MS=1).
- It starts more than minimum of 5 bus clock time after serial chip select pin becomes inactive irrespective of setup of deselect time until it next becomes active.

6.6.9 Serial Chip Select Format Register (SCSFR2 to SCSFR0)

The serial chip select format register (SCSFR2 to SCSFR0) performs the direction of data of a setup for connecting with selection of the active level of the chip select of each serial chip select, reversal of serial clock, SPI, and serial-data output, and setup of data length.

- **Bit configuration of serial chip select format register (SCSFR2 to SCSFR0)**
  - ☐ **Bit configuration of serial chip select format register (SCSFR1, SCSFR0)**

bit	15	14	13	12	11	10	9	8
Field	CS2 CSLCV	CS2 SCINV	CS2SPI	CS2 BDS	-	CS2L2	CS2L1	CS2L0
Attribute	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W
Initial value	1	0	0	0	0	0	0	0

bit	7	6	5	4	3	2	1	0
Field	CS1 CSLCV	CS1 SCINV	CS1SPI	CS1 BDS	-	CS1L2	CS1L1	CS1L0
Attribute	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W
Initial value	1	0	0	0	0	0	0	0

[bit15] CS2CSLVL : Serial Chip Select Level Setting bit of chip select 2

In data format enable (ESCR:CSFE=1) of chip select, this bit chooses the level at inactive of the serial chip select pin 2.

bit	Description
0	Selects inactive level "L"
1	Selects inactive level "H"

Notes

- This bit can change only when transmission / reception are prohibition (SCR:TXE=RXE=0).
- A setup of this bit is invalid at slave mode (SCR:MS=1).
- When the data format of chip select is disable (ESCR:CSFE=0), setup of this bit is invalid.

[bit14] CS2SCINV : Serial Clock Invert bit of chip select 2

The serial chip select pin 2 is bit which sets up the serial clock format at active, when data format enable (ESCR:CSFE=1) of chip select.

When this bit set to "0":

The mark level of a serial clock output is made into "H".
Transmit data is outputted by the falling edge of serial clock, and SPI transmission by normal transmission synchronizing with the falling edge of serial clock.
Received data are sampled with the falling edge of serial clock by normal transmission at the rising edge of serial clock, and SPI transmission.

When this bit set to "1":

The mark level of a serial clock output is set to "L".
Transmit data is outputted by the rising edge of a serial clock, and SPI transmission by normal transmission synchronizing with the falling edge of serial clock.
Received data are sampled with the rising edge of serial clock by normal transmission at the falling edge of serial clock, and SPI transmission.

bit	Description
0	Sets mark level "H" format
1	Sets mark level "L" format

Notes

- This bit can change only when transmission / reception are prohibition (SCR:TXE=RXE=0).
- A setup of this bit is invalid at slave mode (SCR:MS=1).
- When the data format of chip select is disable (ESCR:CSFE=0), setup of this bit is invalid.

[bit13] CS2SPI : The bit corresponding to SPI of the serial chip select pin 2

It is a bit for the serial chip select terminal 2 to carry out communication corresponding to SPI at active ,when data format permission (ESCR:CSFE=1) of chip select.

- When this bit set to "0" : Normal synchronous communications are performed.
- When this bit set to "1" : It corresponds to SPI.

bit	Description
0	Normal synchronous transfer
1	Corresponds to SPI

Notes

- This bit can change only when transmission / reception are prohibition (SCR:TXE=RXE=0).
- A setup of this bit is invalid at slave mode (SCR:MS=1).
- When the data format of chip select is disable (ESCR:CSFE=0), setup of this bit is invalid.

[bit12] CS2BDS : The transmission direction selection bit of the serial chip select pin 2

The serial chip select pin 2 is a bit which chooses whether transfer serial data are previously transmitted from the least significant bit side (LSB first, BDS=0), or it transmits previously from the most significant bit side (MSB first, BDS=1) at active, when data format enable (ESCR:CSFE=1) of chip select.

bit	Description
0	LSB first (From least significant bit to transfer)
1	MSB first (From most significant bit to tranfer)

Notes

- This bit can change only when transmission / reception are prohibition (SCR:TXE=RXE=0).
- A setup of this bit is invalid at slave mode (SCR:MS=1).
- When the data format of chip select is disable (ESCR:CSFE=0), setup of this bit is invalid.

[bit10:8] CS2L[2:0] : Data length select bits of of the serial chip select pin 2

The serial chip select pin 2 specifies the data length of transmitted and received data at active, when data format enable (ESCR:CSFE=1) of chip select.

bit10	bit9	bit8	Description
0	0	0	8-bit length
0	0	1	5-bit length
0	1	0	6-bit length
0	1	1	7-bit length
1	0	0	9-bit length

Notes

- Any bit setting other than above is inhibited.
- This bit can change only when transmission / reception are prohibition (SCR:TXE=RXE=0).
- A setup of this bit is invalid at slave mode (SCR:MS=1).
- When the data format of chip select is disable (ESCR:CSFE=0), setup of this bit is invalid.

[bit7] CS1CSLVL : Serial Chip Select Level Setting bit of chip select 1

In data format enable (ESCR:CSFE=1) of chip select, this bit chooses the level at inactive of the serial chip select pin 1.

bit	Description
0	Selects inactive level "L"
1	Selects inactive level "H"

Notes

- This bit can change only when transmission / reception are prohibition (SCR:TXE=RXE=0).
- A setup of this bit is invalid at slave mode (SCR:MS=1).
- When the data format of chip select is disable (ESCR:CSFE=0), setup of this bit is invalid.

[bit6] CS1SCINV : Serial Clock Invert bit of chip select 1

The serial chip select pin 1 is bit which sets up the serial clock format at active, when data format enable (ESCR:CSFE=1) of chip select.

When this bit set to "0":

The mark level of a serial clock output is made into "H".
Transmit data is outputted by the falling edge of serial clock, and SPI transmission by normal transmission synchronizing with the rising edge of serial clock.
Received data are sampled with the falling edge of serial clock by normal transmission at the rising edge of serial clock, and SPI transmission.

When this bit set to "1":

The mark level of a serial clock output is set to "L".
Transmit data is outputted by the rising edge of serial clock, and SPI transmission by normal transmission synchronizing with the falling edge of serial clock.

Received data are sampled with the rising edge of serial clock by normal transmission at the falling edge of serial clock, and SPI transmission.

bit	Description
0	Sets mark level "H" format
1	Sets mark level "L" format

Notes

- This bit can change only when transmission / reception are prohibition (SCR:TXE=RXE=0).
- A setup of this bit is invalid at slave mode (SCR:MS=1).
- When the data format of chip select is disable (ESCR:CSFE=0), setup of this bit is invalid.

[bit5] CS1SPI : The bit corresponding to SPI of the serial chip select pin 1

It is a bit for the serial chip select pin 1 to carry out communication corresponding to SPI at active, when data format permission (ESCR:CSFE=1) of chip select.

- When this bit set to "0" : Normal synchronous communications are performed.
- When this bit set to "1" : It corresponds to SPI.

bit	Description
0	Normal synchronous transfer
1	Corresponds to SPI

Notes

- This bit can change only when transmission / reception are prohibition (SCR:TXE=RXE=0).
- A setup of this bit is invalid at slave mode (SCR:MS=1).
- When the data format of chip select is disable (ESCR:CSFE=0), setup of this bit is invalid.

[bit4] CS1BDS : The transmission direction selection bit of the serial chip select pin 1

The serial chip select pin 1 is a bit which chooses whether transfer serial data are previously transmitted from the least significant bit side (LSB first, BDS=0), or it transmits previously from the most significant bit side (MSB first, BDS=1) at active, when data format enable (ESCR:CSFE=1) of chip select.

bit	Description
0	LSB first (From least significant bit to transfer)
1	MSB first (From most significant bit to tranfer)

Notes

- This bit can change only when transmission / reception are prohibition (SCR:TXE=RXE=0).
- A setup of this bit is invalid at slave mode (SCR:MS=1).
- When the data format of chip select is disable (ESCR:CSFE=0), setup of this bit is invalid.

[bit2:0] CS1L[2:0] : Data length select bits of of the serial chip select pin 1

The serial chip select pin 1 specifies the data length of transmitted and received data at active, when data format enable (ESCR:CSFE=1) of chip select.

bit2	bit1	bit0	Description
0	0	0	8-bit length
0	0	1	5-bit length
0	1	0	6-bit length
0	1	1	7-bit length
1	0	0	9-bit length

Notes

- Any bit setting other than above is inhibited.
- This bit can change only when transmission / reception are prohibition (SCR:TXE=RXE=0).
- A setup of this bit is invalid at slave mode (SCR:MS=1).
- When the data format of chip select is disable (ESCR:CSFE=0), setup of this bit is invalid.

☐ **Bit configuration of serial chip select format register (SCSFR2)**

bit	7	6	5	4	3	2	1	0
Field	CS3 CSLCV	CS3 SCINV	CS3SPI	CS32 BDS	-	CS3L2	CS3L1	CS3L0
Attribute	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W
Initial value	1	0	0	0	0	0	0	0

[bit7] CS3CSLVL : Serial Chip Select Level Setting bit of chip select 3

In data format enable (ESCR:CSFE=1) of chip select, this bit chooses the level at inactive of the serial chip select pin 3.

bit	Description
0	Selects inactive level "L"
1	Selects inactive level "H"

Notes

- This bit can change only when transmission / reception are prohibition (SCR:TXE=RXE=0).
- A setup of this bit is invalid at slave mode (SCR:MS=1).
- When the data format of chip select is disable (ESCR:CSFE=0), setup of this bit is invalid.

[bit6] CS3SCINV : Serial Clock Invert bit of chip select 3

The serial chip select pin 3 is bit which sets up the serial clock format at active, when data format enable (ESCR:CSFE=1) of chip select.

When this bit set to "0":

The mark level of a serial clock output is made into "H".
Transmit data is outputted by the falling edge of serial clock, and SPI transmission by normal transmission synchronizing with the falling edge of serial clock.
Received data are sampled with the falling edge of serial clock by normal transmission at the rising edge of serial clock, and SPI transmission.

When this bit set to "1":

The mark level of a serial clock output is set to "L".
Transmit data is outputted by the rising edge of a serial clock, and SPI transmission by normal transmission synchronizing with the falling edge of serial clock.
Received data are sampled with the rising edge of serial clock by normal transmission at the falling edge of serial clock, and SPI transmission.

bit	Description
0	Sets mark level "H" format
1	Sets mark level "L" format

Notes

- This bit can change only when transmission / reception are prohibition (SCR:TXE=RXE=0).
- A setup of this bit is invalid at slave mode (SCR:MS=1).
- When the data format of chip select is disable (ESCR:CSFE=0), setup of this bit is invalid.

[bit5] CS3SPI : The bit corresponding to SPI of the serial chip select pin 3

It is a bit for the serial chip select pin 3 to carry out communication corresponding to SPI at active ,when data format enable (ESCR:CSFE=1) of chip select.

- When this bit set to "0" : Normal synchronous communications are performed.
- When this bit set to "1" : It corresponds to SPI.

bit	Description
0	Normal synchronous transfer
1	Corresponds to SPI

Notes

- This bit can change only when transmission / reception are prohibition (SCR:TXE=RXE=0).
- A setup of this bit is invalid at slave mode (SCR:MS=1).
- When the data format of chip select is disable (ESCR:CSFE=0), setup of this bit is invalid.

[bit4] CS3BDS : The transmission direction selection bit of the serial chip select pin 3

The serial chip select pin 3 is a bit which chooses whether transfer serial data are previously transmitted from the least significant bit side (LSB first, BDS=0), or it transmits previously from the most significant bit side (MSB first, BDS=1) at active, when data format enable (ESCR:CSFE=1) of chip select.

bit	Description
0	LSB first (From least significant bit to transfer)
1	MSB first (From most significant bit to tranfer)

Notes

- This bit can change only when transmission / reception are prohibition (SCR:TXE=RXE=0).
- A setup of this bit is invalid at slave mode (SCR:MS=1).
- When the data format of chip select is disable (ESCR:CSFE=0), setup of this bit is invalid.

[bit2:0] CS3L[2:0] : Data length select bits of of the serial chip select pin 3

The serial chip select pin 3 specifies the data length of transmitted and received data at active, when data format enable (ESCR:CSFE=1) of chip select.

bit10	bit9	bit8	Description
0	0	0	8-bit length
0	0	1	5-bit length
0	1	0	6-bit length
0	1	1	7-bit length
1	0	0	9-bit length

Notes

- Any bit setting other than above is inhibited.
- This bit can change only when transmission / reception are prohibition (SCR:TXE=RXE=0).
- A setup of this bit is invalid at slave mode (SCR:MS=1).
- When the data format of chip select is disable (ESCR:CSFE=0), setup of this bit is invalid.

6.6.10 Transfer Byte Register (TBYTE3 TBYTE0)

Transfer byte register (TBYTE3 to TBYTE0) sets up the number of transmission data at active of each serial chip select pin.

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	(TBYTE1)								(TBYTE0)							
Attribute	R/W								R/W							
Initial value	00000000								00000000							

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	(TBYTE3)								(TBYTE2)							
Attribute	R/W								R/W							
Initial value	00000000								00000000							

The transfer byte register can set up the number of transfer data at active of each serial chip select pin. When serial chip select pin completes transfer of the data number value set, serial chip select pin becomes inactive.

The serial chip select pin 0 (SCS0) correspond to TBYTE0, the serial chip select pin 1 (SCS1) correspond to TBYTE1, the serial chip select pin 2 (SCS2) correspond to TBYTE2, and the serial chip select pin 3 (SCS3) corresponds to TBYTE3.

When filling following either, the transfer byte register 0 (TBYTE0) is used for synchronous transmission or external trigger transmission. After transmitting operation begins by synchronous transmission or external trigger transmission, the number of data of the value set as TBYTE0 is transmitted.

At the time of serial chip select enable (SCSCR:CSEN [3:0] ="0b0000")

When the value of these bits are changed during transmit operation (SSR:TBI=0), setup of the number of transmission data after changing, after ending transmit operation of the number of transmit data set up before change becomes effective.

bit	Description
Write	Writing to TBYTE
Read	The setting value of TBYTE

Notes

- When these bits set to (0x00), the number of transfer is 8 times.
- When performing synchronous transmission or external trigger transmission in master operation (SCR:MS=0) at chip select use, the number of transfer is as follows.
  - ☐ When the chip select pin 0 is active, it is the setting value of TBYTE0.
  - ☐ When the chip select pin 1 is active, it is the setting value of TBYTE1.
  - ☐ When the chip select pin 2 is active, it is the setting value of TBYTE2.
  - ☐ When the chip select pin 3 is active, it is the setting value of TBYTE3.

6.6.11 Baud Rate Generator Registers 1 and 0 (BGR1 and BGR0)

Baud Rate Generator Registers 1 and 0 (BGR1 and BGR0) are used to set a frequency division ratio of serial clocks.

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	-	(BGR1)							(BGR0)							
Attribute	-	R/W							R/W							
Initial value	-	0000000							00000000							

- Set a clock frequency division to the Baud Rate Generator Registers 1 and 0 (BGR1 and BGR0).
- The BGR1 register corresponds to the high-order bits, and the BGR0 register corresponds to the low-order bits. The reload value to be counted can be written, and the BGR1/BGR0 set value can be read.
- When the reload value is written in Baud Rate Generator Registers 1 and 0 (BGR1 and BGR0), the reload counter starts its counting.

[bit15] - : Unused bit

This bit value is undefined when read.
This bit has no effect on the operation when written.

[bit14:8] BGR1: Baud Rate Generator Register 1

bit14:8	Description
Write	Writes data in bit8 to 14 of reload counter.
Read	Reads the BGR1 set value.

[bit7:0] BGR0: Baud Rate Generator Register 0

bit7:0	Description
Write	Write data in bit0 to 7 of reload counter.
Read	Reads the BGR0 set value.

Notes

- Data must be written in the Baud Rate Generator Register1, 0(BGR1 and BGR0) by 16-bit data accessing.
- If the reload value is even, the "HIGH" and "LOW" width of serial clock are as follows. If the value is odd, the serial clock has the same "HIGH" and "LOW" signal width.
  If SMR:SCINV="0", the "HIGH" width of serial clock is longer for 1 cycle of bus clock.
  If SMR:SCINV="1", the "LOW" width of serial clock is longer for 1 cycle of bus clock.
- Set the reload value to 3 or more.
- If the current values of Baud Rate Generator Register1, 0(BGR1, BGR0) are changed, the new values are reloaded only after the counter value has reached "15h00". In order to validate the new set values immediately, change the BGR1/BGR0 set values and execute the CSIO reset instruction (SCR:UPCL).

7. IrDA

This chapter explains IrDA function.

7.1 Overview
7.2 Block Configuration
7.3 Architecture
7.4 IrDA Setup Control Procedure
7.5 IrDA Registers
7.6 Transmit cycle accuracy, Jitter, and initial pulse width
7.6.1 Transmit cycle accuracy and Jitter
7.7 Example of Register Setting Procedure

7.1 Overview

IrDA consists of the following four blocks. This section explains the main functions of each block.

- ☐ Serial communication Interface block
- ☐ CPU bus I/F conversion block
- ☐ System control register block
- ☐ Clock divider block

- **Serial communication Interface block**

This block is the block which performs infrared serial communication based on IrDA Ver1.0.

The main functions are as follows.

- ☐ IrDA 1.0 SIR (2.4 kbps to 115.2 kbps Half Duplex)
- ☐ Support interrupt control
- ☐ 32 stage 2 transmission/reception data FIFO
- ☐ 8 stage status FIFO
- ☐ Transmission FIFO under run function
- ☐ Auto/manual IR-UNIT configuration function
- ☐ 48 MHz single clock input operation (Internal generated clock by baud rate generation block) timer
- ☐ Clock stop function
  1. Start the clock supply which receives to IrDA.
  2. Change a serial communication selection register to a setup which uses IrDA.
  3. Cancel IrDA hardware reset and start IrDA macro.

See "7.4 . IrDA Setup Control Procedure" for the above. IrDA performs initial setting after IrDA macroscopic reset release of the above-mentioned setup, and directs a start of operation.

- **CPU Bus IF Conversion Block**

This block has the function to convert APB I/F into host I/F.

- **System Control Register Block**

This block has the APB register function.

- **Clock Divider Block**

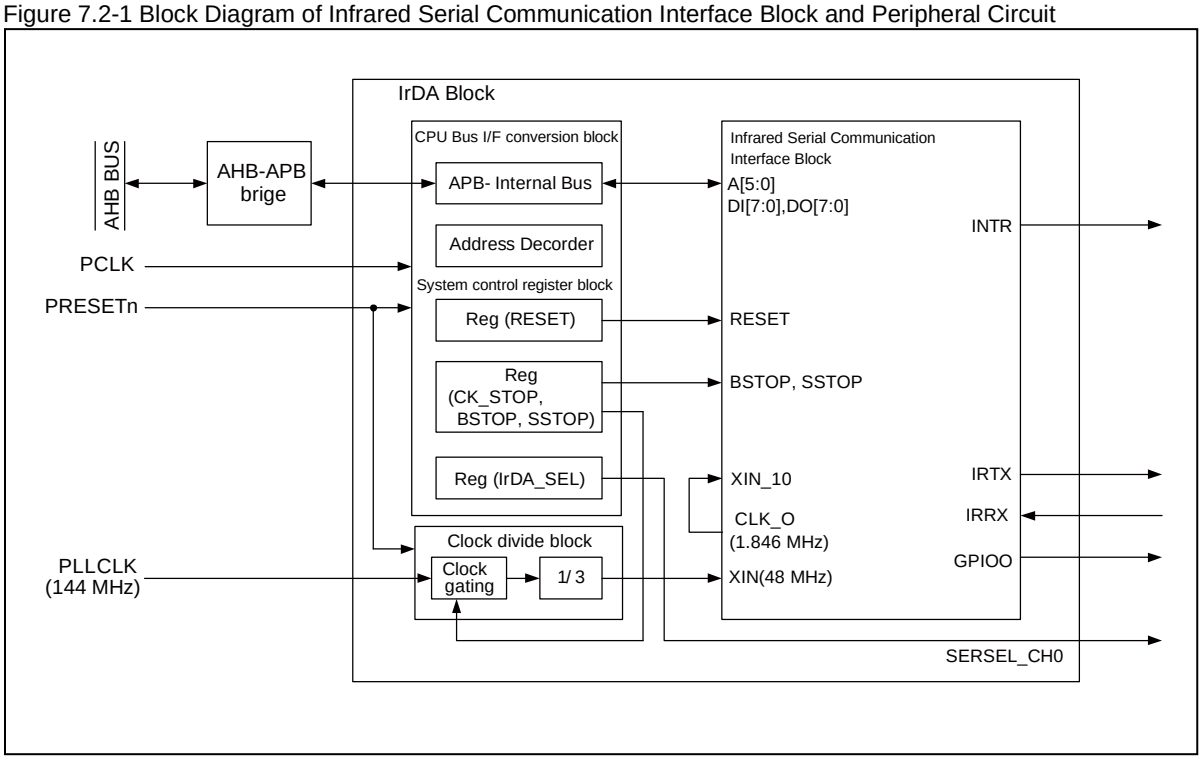
This block has the function which carries out 3 dividing of the input clock.

7.2 Block Configuration

This section explains block configuration of IrDA.

The block diagram of an infrared serial communication interface block and peripheral circuit is shown in Figure 7.2-1.

Figure 7.2-1 Block Diagram of Infrared Serial Communication Interface Block and Peripheral Circuit



7.3 Architecture

This section explains architecture of IrDA.

7.3.1 Configuration
7.3.2 IrDA 1.0 SIR Mode
7.3.3 Interrupt Control
7.3.4 Reception FIFO Timeout
7.3.5 IR-UINIT Control I/F
7.3.6 General-purpose Timer
7.3.7 Clock STOP Function

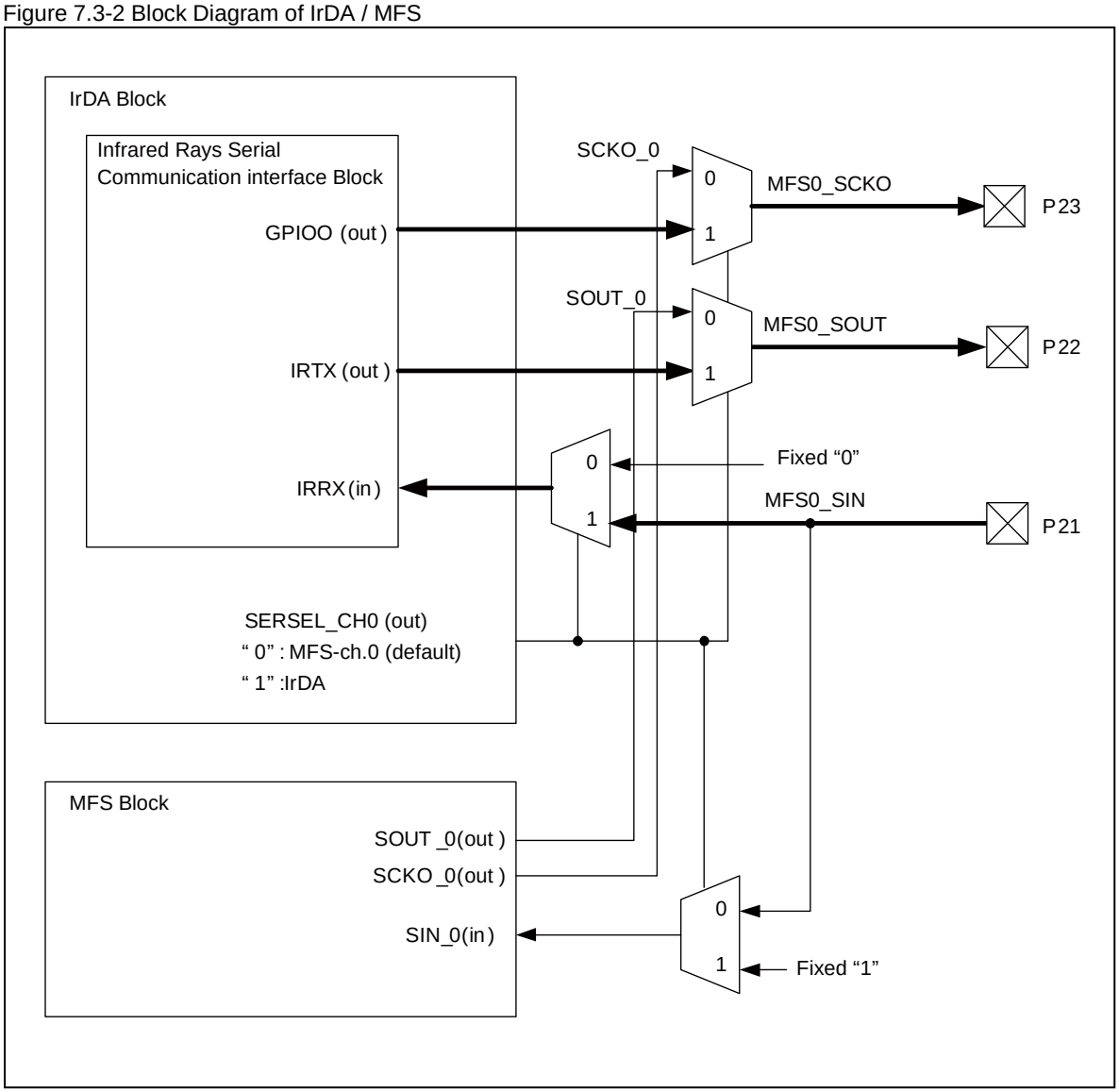
7.3.1 Configuration

The function of IrDA consists of the following blocks.

- **Block Diagram**

Figure 7.3-2 shows the block diagram of IrDA.

Figure 7.3-2 Block Diagram of IrDA / MFS



- **Internal Connection Signal**
  - **System Clock Signal and APB Bus Interface**

    IrDA connects with CPU and a memory via APB bus.
  - IrDA Clock Signal

    This signal is a clock signal used with an IrDA serial communication interface. 144 MHz of PLL outputs are inputted, 3 dividing is carried out inside, and a 48 MHz clock is used.
  - Interrupt Signal Interface

    The interrupt signal outputted from the IrDA section is shown in Table 7.3 1 These interrupt are connected to vector No.53 of NVIC, and IRQ No.37 (bit7).

Table 7.3-1 Interrupt Signal from IrDA

Signal name	I/O	Function
IRDA_INT	OUT	Interrupt Request(Active High) : Interrupt request signal This interrupt signal is shown that the interruption factor has occurred. This interrupt signal is a level output.

7.3.2 IrDA 1.0 SIR Mode

This section explains SIR mode of IrDA.

After converting asynchronous parallel data into asynchronous serial data, the data is modulated at the time of transmission, and it outputs it from IRTX. It restores to the input pulse from IRRX, and it converted from an asynchronous serial asynchronously parallel, and outputs it.
A transmission rate is 115.2 kbps or less, and is a half-duplex (Half Duplex).
Moreover, the pulse width at the time of modulation/demodulation is 3/16 of a bit time, or 1.625 µs (fixed).

7.3.3 Interrupt Control

This section explains interrupt control of IrDA.

By asserting Output (INTR), it is notified to CPU that the interrupt occurred. Control of this interruption is performed by the register IER (Interrupt Enable Register). Moreover, it can check by reading LSR (Link Status Register) of the sauce IIR (Interrupt Identification Register) of interrupt, and MSR (Modem Status Register). The source type of interrupt and the format to read are described below.

7.3.3.1 SIR Mode

There is a priority in the interrupt factor in this mode. The list and contents are shown below.

IIR[3:0]	Priority	Interrupt type
0001	-	
0110	1	Receiver Line Status
0100	2	Receiver Data Available
1100	2	Character Timeout Indication
0010	3	Transmitter Data Register Empty

- **IIR[3:0] = 0110 : Receiver Line Status interrupt**

This interrupt is operating by IER[2] =1.

The interrupt factor can be checked by reading LSR register.

LSR:OVE=1 : Overrun error
When it is overwritten before received data read from CPU

LSR:PTE=1 : Priority error
When parity error is detected by received data

LSR:FME=1 : Frame error
When the stop bit of received data is not detected

LSR:BRI=1 : Break interrupt
When all received data are "0"

LSR register is negated in read operation.

- **IIR[3:0] = 0100 : Receiver Data Available interrupt**

This interrupt becomes effective by IER[0] =1.

The interrupt factor is time of the data more than a trigger level being written in RX_FIFO. RDR register is read and INTR is negated by lowering trigger level.

- **IIR[3:0] = 1100 : Timeout interrupt**

This interrupt becomes effective by IER[0] =1.

The interrupt occurs, when there is no access to RX_FIFO in more than 4 character time. It is negated by reading RDR register.

- **IIR[3:0] = 0010 : Transmitter Data Register Empty interrupt**

This interrupt becomes effective by IER[1] =1.

The interrupt factor is time of TX_FIFO becomes empty.

When negate of INTR has not validated interrupt of priorities the writing to TDR register, or other than this, read of IIR is also performed (See the following <notes>).

Note

When IIR[3:0] =0010 has not validated interrupt of priorities the writing to TDR, or other than this, read of IIR is also performed. When it completely becomes TX_FIFO simultaneously during read of IIR, since priority is given to read / clear function, IIR is not set to "IIR[1:0] =10" and an interrupt does not occurred it. For this reason, this interrupt may be undetectable if polling operation which repeats and detects IIR register read is performed without checking asserting of an INTR pin for Transmitter Data Register Empty interrupt. In performing the read/polling operation of Transmitter Data Register Empty interrupt of IIR as a measure, perform operation which resets TDIE of IER [1] before read of IIR. (Read operation of IIR is performed by making "IER[1] =0 -> IER[1] =1 -> Read IIR" into combination.) Also when interruption is not set more clear simultaneous the above, by resetting IER, Transmitter Data Register Empty interrupt is asserted and Transmitter Data Register Empty interrupt can be detected normally.

7.3.3.2 Timer Interrupt

See "7.3.6 General-purpose Timer" for the details of a general-purpose timer.

When IER[7]:TMIE=1, this interrupt is enabled.
An interrupt occurs in the following sequences.

- Set IRCR1[0]:TMREN=1.
- Set the initial value of a timer counter in TMRL and TMRU register.
- Set IRCR1[2]:TMST=1.
- A timer counter starts a decrement.
- Counted value is set to 0 and an interrupt occurs.
  At this time, interrupt status by IRCR1[3]:TMREV2=1, and check.
- Set IRCR1[7]:CTE2 to "1", and negate INTR.

<Notes on use of general-purpose timer>

- The counted value under execution can be read by the initial value and IRCR1[1]:CTST=0 which were set up by, and IRCR1[1]:CTST=1, respectively.
- As long as a timer is enabling (IRCR1 [0]:TMREN=1), whenever it writes "1" in IRCR1[2]:TMST, count restart starts from the initial value set to the counter.
- Set of IRCR1 [0]:TMREN = 0, it will suspend a timer counter compulsorily.
  Counted value is re-set to the initial value set up first in that case.

7.3.4 Reception FIFO Timeout

This section explains the reception FIFO timeout.

It is timing out when data remains in FIFO at the time of reception, and there is no over a period of time access. Timeout conditions difference with modes.

- **SIR Mode Timeout**

When the following three conditions are satisfied:

1. FIFO has data of one or more characters.
2. A modem does not receive the data more than 4 character time.
3. CPU does not read the data more than 4 character time.

< Operation after timeout occurring >

- ☐ When IER[0]:RDIE=1, Interrupt occurs
- ☐ The state of timeout can be read by IIR register.

RX_FIFO

When the following three conditions are satisfied:

1. RX FIFO has 1 byte or more of data.
2. The writing to RX FIFO does not have 64 µs or more.
3. Read from CPU does not have 64µs or more.

< Operation after timeout occurring >

- ☐ When IER[0]:RDIE =1, Interrupt occurs

ST_FIFO

When the following three conditions are satisfied:

1. ST FIFO has 1 byte or more of data.
2. The writing to ST FIFO does not have 1 ms or more.
3. Read from CPU does not have 1 ms or more.

7.3.5 IR-UINIT Control I/F

This section explains the IR_UNIT control I/F of IrDA.

In order to perform an interface with IR-UNIT, there is the following setup.

- **Input Pins**

ID[3:0] pins : This pins are ID read for IR_UNIT.

- **Output Pins**

IRSL[2:0] pins : This pins are mode select for IR_UNIT.

7.3.6 General-purpose Timer

This section explains the general-purpose timer of IrDA.

IER[7]:	TMRIE	Timer Intr Enable Enables timer interrupt
TMRL:		0000_0000
TMRU:		RRRR_0000
		Perform read order in order of TMRL and TMRU registers. With this bit and the combination of IRCR1[1]:CTST, present counted value and counter initial value are acquirable. Maximum of 4s count is possible for a counter (12 bits), and resolution is 1 ms.
IRCR1[0]:	TMREN	Timer Enable bit This bit enables general-purpose time.
IRCR1[1]:	CTST	0 : Value of current count
		1 : Counter initial value
IRCR1[3]:	TMREV2	Timer Event 2
		When Timer Enable bit is "1" and Timer Count="0", Timer Event Interrupt occurs.
IRCR1[7]:	CTE2	
		When "1" is written in this bit, Timer Event Interrupt will be canceled.

7.3.7 Clock STOP Function

This section explains clock stop function of IrDA.

The BSTOP pin and the SSTOP pin stop the clock supply to internal block, respectively. Use pins, when you save consumption current.

- **BSTOP Pin**

The clock supply to a transmit/receive-related block is stopped. Although read and the writing through CPU of a register are effective, neither the data left behind to TX_FIFO and RX_FIFO before asserting nor transmit/receive operation while asserting this pin is guaranteed. The reset by the hardware and software after dissert is unnecessary.

- **SSTOP Pin**

The clock supply to HOST_REG and HOST_IF blocks are stopped. By this register, while stopping a clock, writing/read to register cannot be performed (however, RST_CTL, CLK_CTL, and the SER_SEL register can perform writing/read).

7.4 IrDA Setup Control Procedure

This section explains the IrDA Setup Control Procedure.

- **Setup**

By power on etc., when reset occurs on APB bus, carry out the following setup control.

A following procedure is carried out and IrDA is setup, after selecting an I/O Port part. The clock supply to IrDA, select serial communication to IrDA use, and hardware reset release to IrDA. Initial setting of IRDA is performed after the completion of a setup, and starts operation.

To IrDA Selection and hardware reset release to IrDA are carried out for clock supply and serial communication to IrDA use.

- **Procedure of Setup**

1. Write "0" in the MSTOP bit, the BSTOP bit, and the SSTOP bit of CLK_CTL register. Clock supply is started to IrDA.
2. "1" is written in the SER_SEL:SERSEL bit and it sets up to output IrDA from MFS (CH0).
3. "0" is written in the RST_CTL:RST bit and reset of IrDA is canceled.

7.5 IrDA Registers

This section explains IrDA registers.

Table 7.5-2 shows list of IrDA registers.

Table 7.5-3 List of IrDA Registers

Abbreviation	Register name	Reference
RST_CTL	Reset Control Register	7.5.1
CLK_CTL	Clock Control Register	7.5.2
SER_SEL	Serial Communication Select Register	7.5.3
RDR/TDR	Transmit/Reception Data Register	7.5.4
IER	Interrupt Control Register	7.5.5
IIR/FCR	Interrupt Identification Register / FIFO Control Register	7.5.6 , 7.5.7
LCR	Link Control Register	7.5.8
LSR	Line Status Register	7.5.9
MSR	Mode Status Register	7.5.10
SCR	Scratch Pad Register	7.5.11
FCR	FIFO Control Register (Read)	7.5.12
BGDL	Baud Rate Generator Divisor Lower 8bit Store Register	7.5.13
BGDU	Baud Rate Generator Divisor Upper 8bit Store Register	7.5.14
EXCR2	Extended Register	7.5.15
TFLV	TX FIFO Data Number Store Register	7.5.16
RFLV	RX FIFO Data Number Store Register	7.5.17
TMRL	General-purpose Timer Initial Value(8LSB) Store Register	7.5.18
TMRU	General-purpose Timer Initial Value(4MSB) Store Register	7.5.19
IRCR1	General-purpose Timer Counter Control Register	7.5.20
TFLL	Transfer Frame Length (8LSB) Store Register	7.5.21
TFLU	Transfer Frame Length (5MSB) Store Register	7.5.22
RFLL	Maximum Reception Frame Length (8LSB) Store Register	7.5.23
RFLU	Maximum Reception Frame Length (5MSB) Store Register	7.5.24
IRCR2	Infrared Rays Control Register	7.5.25
IRCR3	Infrared Rays Control Register	7.5.26
SIRPW	SIR Pulse Width Register	7.5.27
GPDATA	General-purpose Output Register	7.5.28
IRCFG1	Infrared Rays I/F Setting Register	7.5.29
IRCFG4	Infrared Rays I/F Setting Register	7.5.30

7.5.1 Reset Control Register (RST_CTL)

RST_CTL Register controls macro reset of IrDA.

- **Register configuration**

bit	7	6	5	4	3	2	1	0
Field	Reserved							RST
Attribute	-							R/W
Initial Value	0000000							1

- **Register functions**

[bit7:1] Reserved：Reserved bits

The read value is "0". Writing has no effect on operation.

[bit0] RST

This bit controls reset of IrDA macro. The setting value of register is read at reading.

bit	Description
0	IrDA macro reset is released.
1	IrDA macro reset is performed. [Initial Value]

7.5.2 Clock Control Register (CLK_CTL)

CLK_CTL Register controls clock supply to IrDA

- **Register configuration**

bit	7	6	5	4	3	2	1	0
Field	Reserved					SSTOP	BSTOP	MSTOP
Attribute	-					R/W	R/W	R/W
Initial Value	00000					1	1	1

- **Register functions**

[bit7:3] Reserved：Reserved bits

The read value is "0". Writing has no effect on operation.

[bit2] SSTOP

This bit controls operation of IrDA internal clock. The setting value of register is read at reading.

bit	Description
0	Clock supply
1	Clock stop [Initial Value]

[bit1] BSTOP

This bit controls operation of IrDA internal clock. The setting value of register is read at reading.

bit	Description
0	Clock supply
1	Clock stop [Initial Value]

[bit0] MSTOP

This bit controls clock supply to IrDA. The setting value of register is read at reading.

bit	Description
0	Clock supply
1	Clock stop [Initial Value]

7.5.3 Serial Communication Select Register (SER_SEL)

SER_SEL Register selects serial function of MFS(CH0).

- **Register configuration**

bit	7	6	5	4	3	2	1	0
Field	Reserved							SERSEL
Attribute	-							R/W
Initial Value	0000000							0

- **Register functions**

[bit7:1] Reserved：Reserved bits

The read value is "0". Writing has no effect on operation.

[bit0] SERSEL

This bit selects serial function of MFS (CH0). The setting value of register is read at reading.

bit	Description
0	MFS (CH0) selects [Initial Value]
1	IrDA selects

7.5.4 Transmit/Reception Data Register (RDR/TDR)

RDR register stores IrDA received data and TDR register stores IrDA transmit data.

- **Register configuration (RDR)**

bit	7	6	5	4	3	2	1	0
Field	RDR							
Attribute	R							
Initial Value	0x00							

- **Register configuration (TDR)**

bit	7	6	5	4	3	2	1	0
Field	TDR							
Attribute	W							
Initial Value	0x00							

■ **Register functions**

[bit7:0] TDR/RDR

The TDR/RDR register is sharing the same address. RDR is accessed by the read cycle by CPU. If data is read from RDR, data will be read from Receiver FIFO. "0" will be read, if data is read from this register when there are no received data. In this case, the read pointer of FIFO does not move. If reset with a RESET pin, Receiver FIFO will serve as empty and this register will also become empty.

TDR is accessed in the write cycle by CPU. If data is written in TDR, data will be written in Transmitter FIFO. When Transmitter FIFO is full, data is not rewritten although data is written in this register. Moreover, FIFO write pointer does not move, either.

If reset with a RESET pin, Transmitter FIFO will serve as empty and this register will also become empty.

7.5.5 Interrupt Control Register (IER)

IER Register controls interrupt.

■ **Register configuration (SIR 1.0Mode)**

bit	7	6	5	4	3	2	1	0
Field	TMIE	Reserved				RLS	TDIE	RDIE
Attribute	R/W	R				R/W	R/W	R/W
Initial Value	0	0000				0	0	0

■ **Register functions**

[bit7] TMIE (GP Timer Interrupt Enable)

This bit controls general-purpose timer interrupt. The setting value of register is read at reading.

bit	Description
0	Disable [Initial Value]
1	Enable

[bit6:3] Reserved：Reserved bits

Accesses to these bits are prohibition.

[bit2] RLS (Receiver Line Status Interrupt Enable)

This bit controls Receiver Line Status Interrupt. The setting value of register is read at reading.

bit	Description
0	Disable [Initial Value]
1	Enable

[bit1] TDIE (Transmitter Low Data Level Interrupt Enable)

This bit controls Transmitter Low Data Level Interrupt. The setting value of register is read at reading.

bit	Description
0	Disable [Initial Value]
1	Enable

[bit0] RDIE (Receiver High Data Level Interrupt Enable)

This bit controls Receiver High Data Level Interrupt. The setting value of register is read at reading.

bit	Description
0	Disable [Initial Value]
1	Enable

7.5.6 Interrupt Identification Register (IIR)

IIR Register is register which identifies interrupt.

- **Register configuration (SIR 1.0Mode Read)**

bit	7	6	5	4	3	2	1	0
Field	FIE1	FIE0	Reserved		TMI	ILV1	ILV0	IPD
Attribute	R	R	R		R	R	R	R
Initial Value	1	1	00		0	0	0	1

In order to reduce the overhead of the software at the time of data transfer, interrupt is divided into three priority level, and it records on IIR. Below, it is shown at order with a high priority of interrupt.

1. Receiver Line Status Interrupt
2. Received Data Available Interrupt and Timeout Error Interrupt
3. Transmitter Data Register Empty Interrupt

Interrupt which has the highest priority in read of IIR is shown.

If new interrupt factor occurs during this read, the stack of it will be carried out, but the value of IIR is not changed until this read period expires.

- **Register functions**

[bit7:6] FIE1, FIE0 (FIFO Enable Status)

These bits indicate status of FIFO mode. Writing has no effect on operation.

bit7	bit6	Description
0	0	Non FIFO Mode
1	1	FIFO Mode [Initial Value]

[bit5:4] Reserved : Reserved bit

The read value is "0". Writing has no effect on operation.

[bit3] TMI (RX FIFO Timeout Interrupt)

This indicates the status of Timeout Interrupt Pending. Writing has no effect on operation.

bit	Description
0	Timeout Interrupt not Pending(Initial Value)
1	Timeout interrupt Pending

[bit2:1] ILV1, ILV0 (Interrupt Level)

These bits indicate the interrupt level.

[bit0] IPD (Interrupt Pending)

This bit indicates status of Interrupt Pending. Writing has no effect on operation.

bit	Description
0	Interrupt Pending
1	Interrupt not Pending [Initial Value]

7.5.7 FIFO Control Register (FCR)

FCR register controls FIFO.

- **Register configuration (SIR 1.0 Mode Write)**

bit	7	6	5	4	3	2	1	0
Field	RTL1	RTL0	Reserved	Reserved	Reserved	TFR	RFR	FEN
Attribute	W	W	-			W	W	W
Initial Value	0	0	000			0	0	1

The writing to this register value can be performed by IIR/FCR register, and read can be performed by FCR register. This register is used for setup in the setting mode enabling of FIFO, clear, and the interrupt occurring Threshold Level.

- **Register functions**

[bit7:6] RTL1, RTL0 (RX_FIFO Interrupt Trigger Level)

The trigger level of interrupt asserting by RX_FIFO is setup. The setting value of register is read at reading.

bit7	bit6	Description(Trigger Level(FIFO Level 32))
0	0	Trigger Level=1 [Initial Value]
0	1	Trigger Level=8
1	0	Trigger Level=16
1	1	Trigger Level=30

[bit5:3] Reserved: Reserved bits

This bit is always "0" read.
Write to this bit is prohibition.

[bit2] TFR (Transmitter Soft Reset)

This bit issue Transmitter Soft Reset. The setting value of register is read at reading.

bit	Description
0	No issue Reset [Initial Value]
1	The following operations will be performed if this bit is set to "1". The data of TX_FIFO is cleared. The pointer of TX_FIFO is cleared.

[bit1] RFR (Receiver Soft Reset)

This bit issue Receiver Soft Reset. The setting value of register is read at reading.

bit	Description
0	Reset issue is not performed. [Initial Value]
1	This bit set to “1” and execute following operation. ■ Cleared data of RX_FIFO ■ Cleared pointer of RX_FIFO

[bit0] FEN (Enable FIFOs)

This bit sets FIFO mode. The setting value of register is read at reading.
Always write in "1".

7.5.8 Link Control Register (LCR)

LCR Register controls the Link.

■ **Register configuration**

bit	7	6	5	4	3	2	1	0
Field	Reserved	BRC	STP	EPS	PE	STL	CHL1	CHL0
Attribute	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

■ **Register functions**

[bit7] Reserved : Reserved bit

Access to this bit is prohibition.

[bit6] BRC (Break Control)

This bit is used for control of the space state of a SOT pin.

[bit5] STP (Stick Parity)

This bit is used for setup of the parity of a fixed value. The setting value of register is read at reading.

[bit4] EPS (Even Parity Select)

This bit set up parity.

[bit3] PE (Parity Enable)

This bit setup enable/disable of parity.

bit5	bit4	bit3	Setting of Parity
0	0	0	Parity Disable [Initial Value]
	0	1	Odd Parity
	1	0	Parity Disable
	1	1	Even Parity
1	0	0	Parity Disable
	0	1	Fix 1
	1	0	Parity Disable
	1	1	Fix 0

[bit2] STL (Stop bit Length)

This bit set up stop bit length. The setting value of register is read at reading.

bit2	bit1	bit0	Stop bit length
0	0	0	1 [Initial Value]
	0	1	1
	1	0	1
	1	1	1
1	0	0	1.5
	0	1	2
	1	0	2
	1	1	2

[bit1:0] CHL1, CHL0 (Character Length)

These bits set up character bit length.

bit1	bit0	Character bit length
0	0	5 [Initial Value]
0	1	6
1	0	7
1	1	8

7.5.9 Line Status Register (LSR)

LSR Register reads the status of line.

- **Register configuration (SIR 1.0Mode)**

bit	7	6	5	4	3	2	1	0
Field	FE	TE	TDRE	BRI	FME	PTE	OVE	RDA
Attribute	R	R	R	R	R	R	R	R
Initial Value	0	1	1	0	0	0	0	0

- **Register functions**

[bit7] FE (FIFO Error)

This bit indicates status of FIFO error.

bit	Description
0	With no FIFO error occurs [Initial Value]
1	This bit will be set to "1" if parity error, framing error, and one error of the break interrupt are detected in RX_FIFO. When an error is not except the lowest of FIFO, it will be set to "0" if LSR is read. This bit is set to "0" by reset.

[bit6] TE (Transmitter Empty)

This bit indicates empty status of Transmitter.

bit	Description
0	Data is not empty in the block of FIFO, register, and parallel-serial conversion at transmission.
1	This bit will be set to "1" if data becomes empty by all the blocks of FIFO, register, and parallel-serial conversion at transmission. This bit becomes "1" by reset, and becomes "0" in TDR register writing. [Initial Value]

[bit5] TDRE (Transmitter Data Register Empty)

This bit indicates empty status of Transmitter Data Register.

bit	Description
0	FIFO or Register value is not empty.
1	This bit is set to "1" when FIFO or the register of the transmitting side becomes empty. This bit becomes "1" by reset, and becomes "0" in TDR register writing. [Initial Value]

[bit4] BRI (Break Event Detected)

This bit indicates status of interrupt. If error occurs, this bit set to "1".

bit	Description
0	No interrupt occur [Initial Value]
1	The Break interrupt bit is set to "1" when the data in which this bit is "1" reaches the lowest of RX_FIFO. This bit is set to "0" by reset or read of LSR register.

[bit3] FME (Framing Error)

This bit indicates status of framing. If error occurs, this bit set to "1".

bit	Description
0	No framing error occur [Initial Value]
1	The Framing error bit is set to "1" when the data in which this bit is "1" reaches the lowest of RX_FIFO. This bit is set to "0" by reset or read of LSR register.

[bit2] PTE (Parity Error)

This bit indicates status of parity. If error occurs, this bit set to "1".

bit	Description
0	No parity error occur [Initial Value]
1	This bit is set to "1" when the data in which this bit is "1" reaches the lowest of RX_FIFO. This bit is set to "0" by reset or read of LSR register.

[bit1] OVE (Overrun Error)

This bit indicates status of overrun error. If overrun error occurs, this bit set to "1".

bit	Description
0	No overrun error occur [Initial Value]
1	This bit is set to "1" when the data in which this bit is "1" reaches the lowest of RX_FIFO. This bit is set to "0" by reset or read of LSR register.

[bit0] RDA (Receiver Data Available)

Received data show from CPU that read is possible.

bit	Description
0	Reception data not Ready [Initial Value]
1	Reception data Ready

7.5.10 Mode Status Register (MSR)

MSR register can read the state in the mode.

- **Register configuration**

bit	7	6	5	4	3	2	1	0
Field	Reserved				DDCD	TERI	DDSR	DCTS
Attribute	R				R	R	R	R
Initial Value	0000				0	0	0	0

- **Register functions**

[bit7:4] Reserved：Reserved bit

The read value is "0". Writing has no effect on operation.

[bit3] DDCD (Delta Data Carrier Detect)

This bit indicates status of "Delta Data Carrier Detect".

bit	Description
0	It is not changing from the last read. [Initial Value]
1	It changed from the last read.

[bit2] TERI (Ring Indicator Trailing Edge)

This bit indicates status of "Ring Indicator Trailing Edge".

bit	Description
0	It is not changing from the last read to Low->High. [Initial Value]
1	It changed from the last read to Low->High.

[bit1] DDSR (Delta Data Set Ready)

This bit indicates status of "Delta Data Set Read".

bit	Description
0	It is not changing from the last read. [Initial Value]
1	It changed from the last read.

[bit0] DCTS (Delta Clear to Send)

This bit indicates status of "Delta Clear to Send".

bit	Description
0	It is not changing from the last read. [Initial Value]
1	It changed from the last read.

7.5.11 Scratch Pad Register (SCR)

SCR register holds data temporarily as a scratch pad register.

- **Register configuration (SIR 1.0 Mode)**

bit	7	6	5	4	3	2	1	0
Field	SPR7	SPR6	SPR5	SPR4	SPR3	SPR2	SPR1	SPR0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	1	1	1	1	1	1	1	1

- **Register functions**

[bit7:0] SPR7 to SPR0 (Scratch pad Register)

This register holds data temporarily as a scratch pad register.

7.5.12 FIFO Control Register(Read) (FCR)

FCR register reads the register value of FIFO.

- **Register configuration**

bit	7	6	5	4	3	2	1	0
Field	Reserved					TFR	RFR	FEN
Attribute	R					R	R	R
Initial Value	00000					0	0	1

Read-out of FCR register is performed by this register.

- **Register functions**

[bit7:3] Reserved: Reserved bit

This bit is always "0" read.
Writing has no effect on operation.

[bit2] TFR (Transmitter Soft Reset)

The value of Transmitter Soft Reset can be read.

bit	Description
0	Not issue reset [Initial Value]
1	Issue reset

[bit1] RFR (Receiver Soft Reset)

The value of Receiver Soft Reset can be read.

bit	Description
0	Not issue reset [Initial Value]
1	Issue reset

[bit0] FEN (Enable FIFOs)

This bit is always being fixed to FIFO mode.
This bit is always "1" read.

7.5.13 Baud Rate Generator Divisor Lower 8bit Hold Register (BGDL)

BGDL register holds 8 bits of divisor lower byte of a baud rate generator.

- **Register configuration**

bit	7	6	5	4	3	2	1	0
Field	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	1	1	1	1	1	1	1	1

- **Register functions**

[bit7:0] Data7 to Data0

This register holds 8 bits of divisor lower byte of a baud rate generator.

7.5.14 Baud Rate Generator Divisor Upper 8bit Hold Register (BGDU)

BGDU register holds 8 bits of divisor upper byte of a baud rate generator.

■ **Register configuration**

bit	7	6	5	4	3	2	1	0
Field	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

■ **Register functions**

[bit7:0] Data7 to Data0

This register holds 8 bits of divisor upper byte of a baud rate generator.

Dividing setup of a baud rate generator

Baud Rate (bps)	1.846 MHz	
	Divisor Latch Value	Error (%)
2400	48	0
4800	24	0
9600	12	0
19200	6	0
38400	3	0
57600	2	0
115200	1	0

With the value set as BGDU register and BGDL register, dividing of XIN_10 is carried out and a 16 times as many clock as a required baud rate is generated.
The relation of a baud rate, BGDU register, and BGDL register are calculable by following formula.

Baud rate $\times$ 16 = CLK_O/{(15bit) $\times 2^{15}$ + (14bit) $\times 2^{14}$ + … + (1bit) $\times 2^{1}$ + (0bit) $\times 2^{0}$}

In order to set up 115.2k bps, these registers set up 1. (BGDL = 0x01, BGDU = 0x00)

When initial setting, sure to set up BGDU register and BGDL register.

See "7.6.1 Transmit cycle accuracy and Jitter" for an error rate.

7.5.15 Extended Register (EXCR2)

EXCR2 register is a register for extension.

■ **Register configuration**

bit	7	6	5	4	3	2	1	0
Field	Reserved				Ext3	Ext2	Ext1	Ext0
Attribute	R				R/W	R/W	R/W	R/W
Initial value	0000				0	0	0	0

■ **Register functions**

[bit7:4] Reserved : Reserved bits

The read value is "0". Writing has no effect on operation.

[bit3:0] Ext3 to Ext0

These bits are a register for extension. Accesses to these bits are prohibition.

7.5.16 TX FIFO Data Number Store Register (TFLV)

TFLV register stores the number of data for transmit FIFO.

■ **Register configuration**

bit	7	6	5	4	3	2	1	0
Field	Reserved		TFL5	TFL4	TFL3	TFL2	TFL1	TFL0
Attribute	R		R	R	R	R	R	R
Initial value	00		0	0	0	0	0	0

■ **Register functions**

[bit7:6] Reserved : Reserved bits

The read value is "0". Writing has no effect on operation.

[bit5:0] TFL5 to TFL0 (TX FIFO Level)

The number of data of transmit FIFO is stored.

7.5.17 RX FIFO Data Number Store Register (RFLV)

RFLV register stores the number of data for receive FIFO.

■ **Register configuration**

bit	7	6	5	4	3	2	1	0
Field	Reserved		RFL5	RFL4	RFL3	RFL2	RFL1	RFL0
Attribute	R		R	R	R	R	R	R
Initial Value	00		0	0	0	0	0	0

■ **Register functions**

[bit7:6] Reserved : Reserved bits

The read value is "0". Writing has no effect on operation.

[bit5:0] RFL5 to RFL0 (RX FIFO Level)

The number of data of receive FIFO is stored.

7.5.18 General-purpose Timer Initial Value (8LSB) Store Register (TMRL)

TMRL register stores the general-purpose timer Initial Value (8LSB).

- **Register configuration**

bit	7	6	5	4	3	2	1	0
Field	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	1

- **Register functions**

[bit7:0] Data7 to Data0

These bits set initial value of general-purpose timer (8LSB).

In order to read the data set as this register, the IRCR1:CTS bit set to "1".

The minimum unit is 1 ms and can count a maximum of 4 s.

A read-out order becomes the order of TMRL register and TMRU register.

7.5.19 General-purpose Timer Initial Value (4MSB) Store Register (TMRU)

TMRU register stores the general-purpose timer Initial Value (4MSB).

- **Register configuration**

bit	7	6	5	4	3	2	1	0
Field	Reserved				Data3	Data2	Data1	Data0
Attribute	R				R/W	R/W	R/W	R/W
Initial Value	0000				0	0	0	0

- **Register functions**

[bit7:4] Reserved : Reserved bits

The read value is "0". Writing has no effect on operation.

[bit3:0] Data3 to Data0

Initial value of general-purpose timer : 4 MSB

In order to read the data set as this register, the IRCR1:CTS bit set to "1".

The minimum unit is 1 ms and can count a maximum of 4 s.

A read-out order becomes the order of TMRL register and TMRU register.

7.5.20 General-purpose Timer Counter Control Register (IRCR1)

IRCR1 register controls the infrared ray.

- **Register configuration**

bit	7	6	5	4	3	2	1	0
Field	CTE2	Reserved			TMREV2	TMST	CTST	TMREN
Attribute	R/W	R			R	R/W	R/W	R/W
Initial Value	0	000			0	0	0	0

- **Register functions**

[bit7] CTE2 (Clear Timer Event)

If "1" is written in this bit, timer event interrupt will be canceled.

[bit6:4] Reserved : Reserved bits

The read value is "0". Writing has no effect on operation.

[bit3] TMREV2 (Timer Event)

The TMREN bit is "1", and when timer counter is 0, time event interrupt occurs.

[bit2] TMST (Timer Start)

A count start set point of a general-purpose timer is performed. The setting value of register is read at reading.

bit	Description
0	A counter stops. However, when "1" is set next, a count begins from Initial Value. [Initial Value]
1	A counter starts by writing in "1". Initial Value will be loaded automatically and a general-purpose timer will carry out a count start, if this bit is set to "1".

[bit1] CTST (Counter Test)

A read-out setup of count value is performed. The setting value of register is read at reading.

bit	Description
0	The count value under execution can be read by TMRL and TMRU. [Initial Value]
1	Initial Value set up by read-out of TMRL and TMRU can be read.

[bit0] TMREN (Timer Enable)

This bit sets general-purpose timer. The setting value of register is read at reading.

bit	Description
0	Disables general-purpose timer counter [Initial Value]
1	Enables general-purpose timer counter When you use general-purpose timer, this bit set to "1".

7.5.21 Transfer Frame Length (8LSB) Store Register (TFLL)

TFLL register is accessed as the number of data bytes under frame transmission (8LSB) in writing by the set of the transmission frame length at transmission (8LSB), and read.

- **Register configuration**

bit	7	6	5	4	3	2	1	0
Field	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

- **Register functions**

[bit7:0] Data7 to Data0

This register is accessed as the number of data bytes under frame transmission in writing by the set of the transmission frame length at transmission, and read.

7.5.22 Transfer Frame Length (5MSB) Store Register (TFLU)

TFLU register is accessed as upper byte 5 bits from MSB of the number of data bytes under frame transmission by upper byte 5-bit set and read from transmission frame length MSB at transmission in writing.

- **Register configuration**

bit	7	6	5	4	3	2	1	0
Field	Reserved			Data4	Data3	Data2	Data1	Data0
Attribute	R			R/W	R/W	R/W	R/W	R/W
Initial Value	000			0	1	0	0	0

- **Register functions**

[bit7:5] Reserved : Reserved bits

The read value is “0”. Writing has no effect on operation.

[bit4:0] Data4 to Data0

Data4 to Data0 are accessed as upper byte 5 bits from MSB of the number of data bytes under frame transmission by upper byte 5-bit set and read from transmission frame length MSB at transmission in writing.

7.5.23 Maximum Reception Frame Length (8LSB) Store Register (RFLL)

RFLL register is accessed in writing as 8 bits of LSB lower byte of the number of data bytes under frame reception by 8 bits of LSB lower byte of the maximum frame length at reception, and read.

- **Register configuration**

bit	7	6	5	4	3	2	1	0
Field	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

- **Register functions**

[bit7:0] Data7 to Data0

This register is accessed in writing as 8 bits of LSB lower byte of the number of data bytes under frame reception by 8 bits of LSB lower byte of the maximum frame length at reception, and read.

Initial Value of the maximum frame length at reception is RFLU=0x08 and RFLL=0x00.

7.5.24 Maximum Reception Frame Length (5MSB) Store Register (RFLU)

RFLU register is accessed in writing as 5 bits of MSB upper byte of the number of data bytes under frame reception by 5 bits of MSB upper byte of the maximum frame length at the time of reception, and read.

- **Register configuration**

bit	7	6	5	4	3	2	1	0
Field	Reserved			Data4	Data3	Data2	Data1	Data0
Attribute	R			R/W	R/W	R/W	R/W	R/W
Initial Value	000			0	0	0	0	0

- **Register functions**

[bit7:5] Reserved：Reserved bits

The read value is "0". Writing has no effect on operation.

[bit4:0] Data4 to Data0

This register is accessed in writing as 5 bits of MSB upper byte of the number of data bytes under frame reception by 5 bits of MSB upper byte of the maximum frame length at the time of reception, and read.

Initial Value of the maximum frame length at reception is RFLU=0x08 and RFLL=0x00.

7.5.25 Infrared Rays Control Register (IRCR2)

IRCR2 register controls the infrared ray.

- **Register configuration**

bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved			TXMD	Reserved		
Attribute	R	-			R/W	R		
Initial Value	0	-			0	000		

- **Register functions**

[bit7] Reserved：Reserved bit

The read value is "0". Writing has no effect on operation.

[bit6:4] Reserved: Reserved bits

Accesses to these bits are prohibition.

[bit3] TXMD (Transmitter Mode Select)

This bit sets Transmitter Mode. The setting value of register is read at reading.

bit	Description
0	Normal mode [Initial Value]
1	Transmit end stop mode TFL counter is set to 0. It stops, after End of Frame conditions occur after that, and a transmitting part completes transmission of a frame.

[bit2] Reserved : Reserved bit

Access to this bit is prohibition.

[bit1] Reserved : Reserved bit

The read value is "0". Writing has no effect on operation.

[bit0] Reserved : Reserved bit

Access to this bit is prohibition.

7.5.26 Infrared Rays Control Register (IRCR3)

IRCR3 register can read the state in the mode.

- **Register configuration**

bit	7	6	5	4	3	2	1	0
Field	Reserved					ICRC	DCRC	Reserved
Attribute	R					R/W	R/W	R
Initial Value	00000					0	0	0

- **Register functions**

[bit7:3] Reserved : Reserved bits

The read value is "0". Writing has no effect on operation.

[bit2] ICRC (Invert Transmitter CRC)

CRC transmission is set up. The setting value of register is read at reading.

bit	Description
0	CRC is transmitted by positive logic.[Initial Value]
1	CRC is reversed and transmitted.

[bit1] DCRC (Disable Transmitter CRC)

CRC transmission is set up. The setting value of register is read at reading.

bit	Description
0	Transmit CRC [Initial Value]
1	No transmit CRC

[bit0] Reserved : Reserved bit

The read value is "0". Writing has no effect on operation.

7.5.27 SIR Pulse Width Register (SIRPW)

SIRPW register sets up the pulse width of SIR signal.

- **Register configuration**

bit	7	6	5	4	3	2	1	0
Field	Reserved				SPW3	SPW2	SPW1	SPW0
Attribute	R				R/W	R/W	R/W	R/W
Initial Value	0000				0	0	0	0

- **Register functions**

[bit7:4] Reserved：Reserved bits

The read value is "0". Writing has no effect on operation.

[bit3:0] SPW3 to SPW0 (SIR Signal Pulse Width)

bit3	bit2	bit1	bit0	Pulse Width
0	0	0	0	3/16 of Bit time(Initial Value)
1	1	0	1	Fixed 1.625μs
Setting values other than the above				Fixed 3/16

7.5.28 General-purpose Output Register (GPDATA)

GPDATA register drives the value of a general-purpose output.

- **Register configuration**

bit	7	4	3	1	0
Field	Reserved		Reserved		GPDATA0
Attribute	R		R		W
Initial Value	0000		000		0

- **Register functions**

[bit7:4] Reserved：Reserved bits

The read value is "0". Writing has no effect on operation.

[bit3:1] Reserved：Reserved bit

The read value is undefined. Writing has no effect on operation.

[bit0]GPDATA0 (GPO DATA)

bit	Description
0	GPDATA0 drives GPIOO.[Initial Value]
1	The value of the input pin (GPIOI) is read.

7.5.29 Infrared Rays I/F Setting Register (IRCFG1)

IRCFG1 register sets up infrared rays I/F.

- **Register configuration**

bit	7	6	5	4	3	2	1	0
Field	DS20	SIRC2	SIRC1	SIRC0	IRIC3	IRIC2	IRIC1	IRIC0
Attribute	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

- **Register functions**

[bit7] DS20 (Direction of IRCFG1[2:0])

IRIC [2:0] shares read of ID and an IRSL drive. The setting value of register is read at reading.

bit	Description
0	Read ID [Initial Value]
1	CPU reads the data written in IRIC[2:0].

[bit6:4] SIRC2 to SIRC0 (SIR Mode Transceiver Configuration)

In case IRCFG4:AMCF=1 and selects SIR mode, the SIRC[2:0] drive IRSL.

[bit3] IRIC3 (Transceiver Identification)

This bit kept the value of input ID[3]. Writing has no effect on operation.

[bit2:0] IRIC2 to IRIC0 (Transceiver Identification/Control)

When reading:

When DS20=0: These bits return value of input ID[2:0].

When DS20=1: CPU reads the data written in IRIC[2:0].

When writing:

In case IRCFG4:AMCF=0, drive IRSL[2:0].

7.5.30 Infrared Rays I/F Setting Register (IRCFG4)

IRCFG4 register sets up infrared rays I/F.

- **Register configuration**

bit	7	6	5	4	3	2	1	0
Field	AMCF	Reserved		RXINV	Reserved			
Attribute	R/W	R		R/W	R			
Initial Value	0	00		0	0000			

■ **Register functions**

[bit7] AMCF

The setting value of register is read at reading.

bit	Description
0	Automatic infrared Transceiver Configuration Disable (Initial Value)
1	Automatic infrared Transceiver Configuration Enable

[bit6:5] Reserved：Reserved bits

The read value is "0". Writing has no effect on operation.

[bit4] RXINV

The setting value of register is read at reading.

bit	Description
0	Light reception module positive logic (active low) [Initial Value]
1	It can respond now to IRRX of light reception module reverse logic (active high).

[bit3:0] Reserved：Reserved bits

The read value is "0". Writing has no effect on operation.

7.6 Transmit cycle accuracy, Jitter, and initial pulse width

This section explains the transmit cycle accuracy, Jitter, and initial pulse width.

7.6.1 Transmit cycle accuracy and Jitter

7.6.2 Initial pulse width

7.6.1 Transmit cycle accuracy and Jitter

Since dividing of 144 MHz of the PLL outputs is carried out and they are generated as a SIR Mode processing clock, it is set to 1.846 MHz.

The error rate whose baud rate is 115.2k bps is called for by the following ceremony.

{(1.846×16 - 1.8432×16) / (1.8432×16)}×100=0.15%

Tolerance level of a standard specification (+/- 0.87%)

7.6.2 Initial pulse width

When baud rate setup is performed by SIR, two kinds of following pulse width can be chosen.

Baud Rate (kbps)	Case1 (s)	Case2 (s)
9.6	19.50	1.625
115.2	1.625	1.625

Case1 : When baud rate setup is performed at 1.846 MHz which carried out dividing from PLL 144MHz
Case2 : When it depended and fixes to baud rate by setup of a SIR pulse width register (SIRPW)

7.7 Example of Register Setting Procedure

This section explains example of register setting procedure for SIR mode.

The example of the setup steps of the register for operating IrDA in SIR mode is shown in "7.7.1 Example of Procedure" See "7.5 . IrDA Registers" for detail of each register.

7.7.1 Example of Procedure

The Setting of baud rate (See "7.5.13 Baud Rate Generator Divisor Lower 8bit Hold Register (BGDL)" and "7.5.14 Baud Rate Generator Divisor Upper 8bit Hold Register (BGDU)".)

In order to use 1.846 MHz which carried out dividing from PLL 144 MHz as a SIR Mode processing clock, error rate in case transmit speed is 115.2 kbps is called for by the following formula.

{(1.846×16 - 1.8432×16) / (1.8432×16)}×100=0.15 %

The tolerance level in a standard is (+/-0.87%).

When the baud rate is set as 115.2 kbps :

IO_WRITE BGDL 0x00000001

IO_WRITE BGDU 0x00000000

When the baud rate is set as 9600 bps :

IO_WRITE BGDL 0x0000000B

IO_WRITE BGDU 0x00000000

Setting of character (See "7.5.8 Link Control Register (LCR)".)

Selects the number of character bits, stop bit length, and parity.

When setting to character 8bit, the stop bit 0x1, those with parity, and Parity EVEN :

IO_WRITE LCR 0x0000001B

Setting of interrupt (See "7.5.5 Interrupt Control Register (IER)".)

Enables interrupt.

Receiver Data Available, Timeout, Transmitter Data Register Empty, and Receiver Line Status interrupt are enabled :

IO_WRITE LCR 0x00000007

Setting of SIR pulse width (See "7.5.27 SIR Pulse Width Register (SIRPW)".)

The pulse width of SIR has two kinds, 1.625 μs fixed, and 3 / 16 × bit time. For 1.625 μs is equivalent to 3 / 16 × bit time at the time of 115.2 kbps, when transmission speed is slower than 115.2 kbps, such as 9600 bps, the power consumption by luminescence can be stopped by fixed to 1.625 μs.

When pulse width is 1.625 μs fixed :

IO_WRITE SIRPW 0x0000000D

Setting of FIFO mode (See "7.5.7 FIFO Control Register (FCR)".)

The trigger level of interrupt generating of receiving FIFO is set up. On this macro, it is not concerned with setup but FIFO is always effective.

When FIFO Enable and trigger level 1:

IO_WRITE FCR 0x00000001(This setup is omissible for default.)

Transmitting of data (See "7.5.4 Transmit/Reception Data Register (RDR/TDR)".)

When send data (1, 2, 3) is transmitted in order :

IO_WRITE TDR 0x00000001

IO_WRITE TDR 0x00000002

IO_WRITE TDR 0x00000003

Reception of data (See "7.5.4 Transmit/Reception Data Register (RDR/TDR)".)

When data is received, whenever it carries out 1 character reception, and interrupt INTR occurs.

It is IO_READ RDR whenever INTR is asserted.

8. Feedthrough



This chapter explains the feedthrough.

8.1 Overview

8.2 I/O Signal of Feedthrough

8.3 Feedthrough Control

8.4 Feedthrough Register

8.1 Overview

This section explains overview of feedthrough.

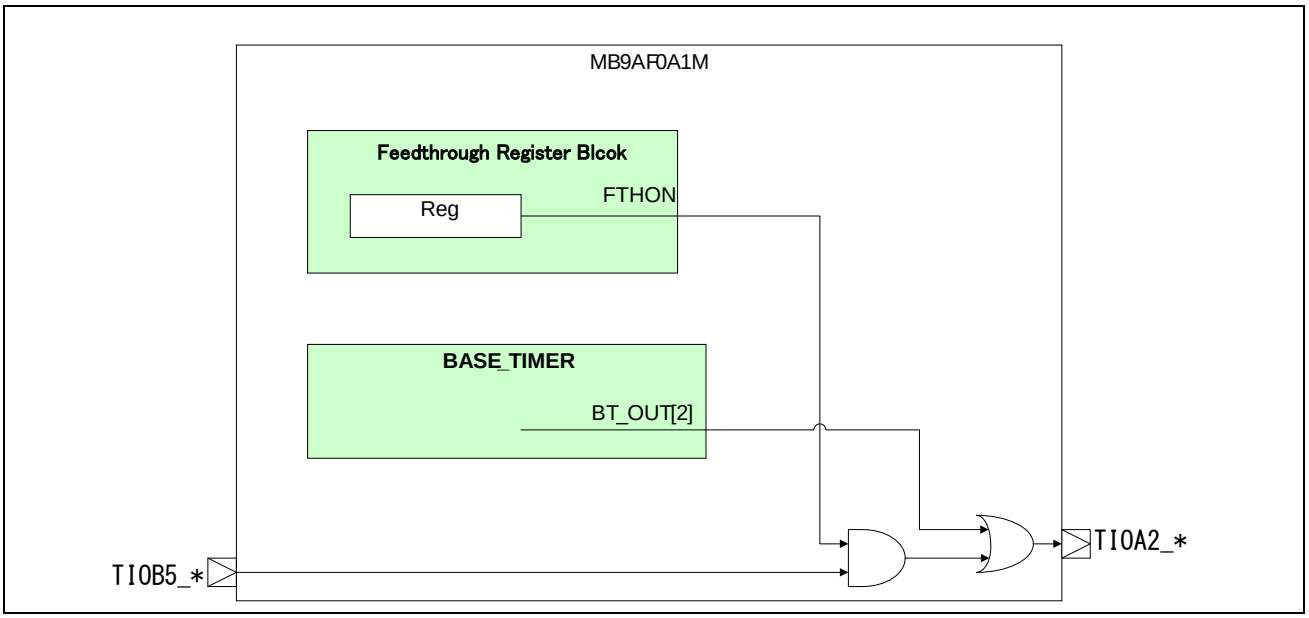
■ **Overview**

Feedthrough is the function to pass the input signal from the outside as it is.

- ☐ ON/OFF control is possible.
- ☐ The circuit of a base timer and the logic OR is constituted.
- ☐ An input pin is as common as TIOB5 of the timer channel 5 of a base timer.
- ☐ An output pin is as common as TIOA2 of the timer channel 2 of a base timer.

■ **Block Diagram**

Figure 8.1-1 Block Diagram of Feedthrough



■ **Explanation of Block**

☐ **Feedthrough Register Block**

This block is control of feedthrough.
This block controls operation by the directions to a register from CPU.

8.2 I/O Signal of Feedthrough

This section explains connection of the I/O signal relevant to feedthrough.

■ **Microcontroller External Pins**

☐ **I/O Signal**

The external pin has connected TIOA pin (TIOA2) of the timer channel 2 of an input and a base timer to an output for TIOB pin (TIOB5) of the timer channel 5 of a base timer.

TIOB5 performs input selection by TIOB5S of the Extended Pin Function Setting Register 05 (EPFR05). TIOA2 performs output selection by TIOA2E of the Extended Pin Function Setting Register 04 (EPFR04).

■ **Internal Connection Pins**

☐ **System Clock Signal and AHB Bus Interface**

The APB bus of feedthrough is connected to CPU and a memory via an AHB bus.

8.3 Feedthrough Control

This section explains the feedthrough control.

The power supply is always on. The feedthrough becomes usable only by setting up a register.

8.4 Feedthrough Register

This section explains register of the feedthrough.

Table 8.4-1 shows register of feedthrough.

Table 8.4-1 Register

Abbreviation	Register name	Reference
FTHON	Feedthrough Setting Register	**Error! Reference source not found.**

8.4.1 Feedthrough Setting Register (FTHON)

The FTHON Register controls feedthrough.

- **Register configuration**

bit	7	6	5	4	3	2	1	0
Field	Reserved							FTHON
Aributte	R							R/W
Initail value	0000000							0

- **Register functions**

[bit7:1] Reserved : Reserved bits

"0b0000000" is always read.
Writing has no effect on operation.

[bit0] FTHON

This bit selects enable/disable of feedthrough.

bit	Description
0	An external signal is not passed. (Initial value)
1	An external signal is passed.

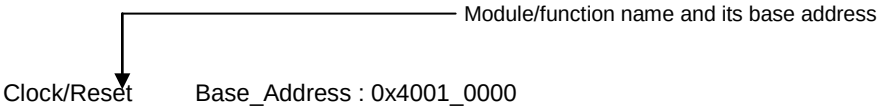
A. Appendix

This appendix explains the register map.

A.1 Register Map

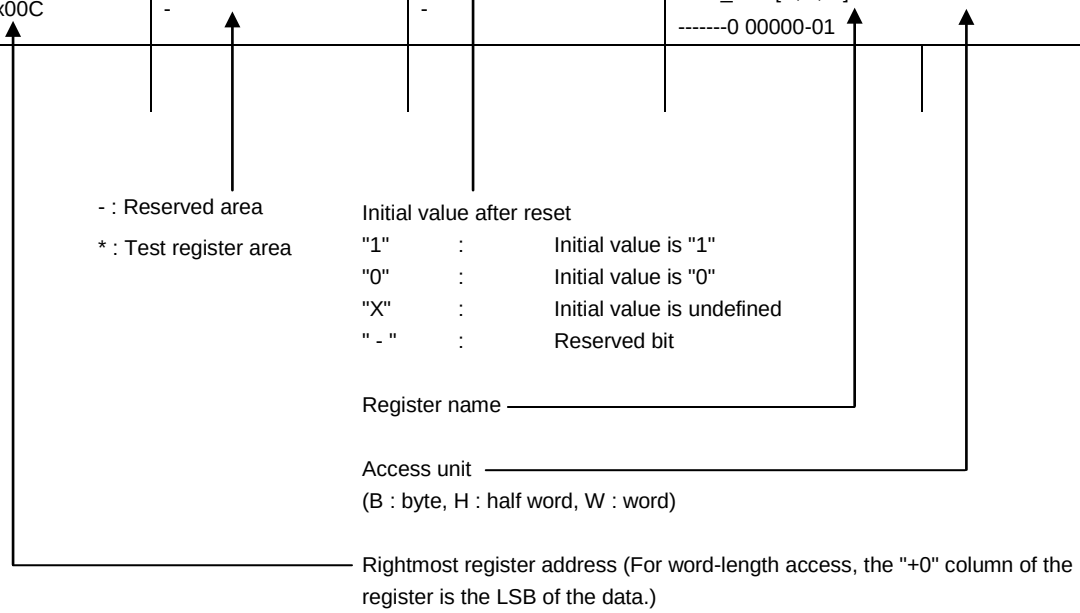
Register map is shown on the table every module/function.

[How to read the each table]



Clock/Reset Base_Address : 0x4001_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	SCM_CTL[B,H,W] 00000-0-
0x004	-	-	-	SCM_STR[B,H,W] 00000-0-
0x008	STB_CTL[B,H,W] 00000000 00000000 -------- ---0--00			
0x00C	-	-	RST_STR[B,H,W] -------0 00000-01	



Notes

- The register table is represented in the little-endian.
- When performing a data access, the addresses should be as below according to the access size.
  - ☐ Word access : Address should be multiples of 4 (least significant 2 bits should be "0x00")
  - ☐ Half word access : Address should be multiples of 2 (least significant bit should be "0x0")
  - ☐ Byte access : -
- Do not access the test register area.
- Do not access the area that is not written in the register table.

Flash I/F Base_Address : 0x4000_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	-
0x004	FRWTR[B,H,W]			
0x008	FSTR[B,H,W]			
0x00C - 0x01C	-	-	-	-
0x020	FICR[B,H,W]			
0x024	FISR[B,H,W]			
0x028	FICLR[B,H,W]			
0x02C - 0x0FC	-	-	-	-
0x100	CRTRMM[B,H,W]			
0x104 - 0xFFC	-	-	-	-

Note

For details of Flash I/F registers, see "MB9AF0A1M FLASH PROGRAMMING MANUAL" of the product used.

Clock/Reset Base_Address : 0x4001_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	SCM_CTL[W] 00000-0-
0x004	-	-	-	SCM_STR[W] 00000-0-
0x008	STB_CTL[W] 00000000 00000000 -------- ---0-000			
0x00C	-	-	RST_STR[W] -------0 00000-01	
0x010	-	-	-	BSC_PSR[W] -----000
0x014	-	-	-	APBC0_PSR[W] ------00
0x018	-	-	-	APBC1_PSR[W] 1--0--00
0x01C	-	-	-	APBC2_PSR[W] 1--0--00
0x020	-	-	-	SWC_PSR[W] X-----00
0x024 - 0x027	-	-	-	-
0x028	-	-	-	TTC_PSR[W] ------00
0x02C - 0x02F	-	-	-	-
0x030	-	-	-	CSW_TMR[W] -0000000
0x034	-	-	-	PSW_TMR[W] ---0-000
0x038	-	-	-	PLL_CTL1[W] 00000000
0x03C	-	-	-	PLL_CTL2[W] ---00000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x040	-	-	CSV_CTL[W] -111--00 ------11	
0x044	-	-	-	CSV_STR[W] ------00
0x048	-	-	FCSWH_CTL[W] 11111111 11111111	
0x04C	-	-	FCSWL_CTL[W] 00000000 00000000	
0x050	-	-	FCSWD_CTL[W] 00000000 00000000	
0x054	-	-	-	DBWDT_CTL[W] 0-0-----
0x058	-	-	-	*
0x05C - 0x05F	-	-	-	-
0x060	-	-	-	INT_ENR[W] --0--000
0x064	-	-	-	INT_STR[W] --0--000
0x068	-	-	-	INT_CLR[W] --0--000
0x06C - 0xFFC	-	-	-	-

HW WDT Base_Address : 0x4001_1000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	WDG_LDR[W] 00000000 00000000 11111111 11111111			
0x004	WDG_VLR[W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x008	WDG_CTL[W]			
	-------- -------- -------- ------11			
0x00C	WDG_ICL[W]			
	-------- -------- -------- XXXXXXXX			
0x010	WDG_RIS[W]			
	-------- -------- -------- -------0			
0x014 - 0xBFC	-	-	-	-
0xC00	WDG_LCK[W] 00000000 00000000 00000000 00000001			
0xC04 - 0xFFC	-	-	-	-

SW WDT Base_Address : 0x4001_2000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	WdogLoad[W] 11111111 11111111 11111111 11111111			
0x004	WdogValue[W] 11111111 11111111 11111111 11111111			
0x008	WdogControl[W]			
	-------- -------- -------- ------00			
0x00C	WdogIntClr[W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x010	WdogRIS[W]			
	-------- -------- -------- -------0			
0x014 - 0xBFC	-	-	-	-
0xC00	WdogLock[W] 00000000 00000000 00000000 00000000			
0xC04 - 0xFFC	-	-	-	-

Dual_Timer Base_Address : 0x4001_5000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	Timer1Load[W] 00000000 00000000 00000000 00000000			
0x004	Timer1Value[W] 11111111 11111111 11111111 11111111			
0x008	Timer1Control[W] -------- -------- -------- 00100000			
0x00C	Timer1IntClr[W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x010	Timer1RIS[W] -------- -------- -------- -------0			
0x014	Timer1MIS[W] -------- -------- -------- -------0			
0x018	Timer1BGLoad[W] 00000000 00000000 00000000 00000000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x020	Timer2Load[W] 00000000 00000000 00000000 00000000			
0x024	Timer2Value[W] 11111111 11111111 11111111 11111111			
0x028	Timer2Control[W] -------- -------- -------- 00100000			
0x02C	Timer2IntClr[W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x030	Timer2RIS[W] -------- -------- -------- -------0			
0x034	Timer2MIS[W] -------- -------- -------- -------0			
0x038	Timer2BGLoad[W] 00000000 00000000 00000000 00000000			
0x040 - 0xFFC	-	-	-	-

Base Timer ch.0 Base Address : 0x4002_5000

Base Timer ch.1 Base Address : 0x4002_5040

Base Timer ch.2 Base Address : 0x4002_5080

Base Timer ch.3 Base Address : 0x4002_50C0

Base Timer ch.4 Base Address : 0x4002_5200

Base Timer ch.5 Base Address : 0x4002_5240

Base Timer ch.6 Base Address : 0x4002_5280

Base Timer ch.7 Base Address : 0x4002_52C0

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	PCSR/PRLL [H,W] XXXXXXXX XXXXXXXX	
0x004	-	-	PDUT/PRLH/DTBF [H,W] XXXXXXXX XXXXXXXX	
0x008	-	-	TMR [H,W] 00000000 00000000	
0x00C	-	-	TMCR [B,H,W] -0000000 00000000	
0x010	-	-	TMCR2 [B,H,W] -------0	STC [B,H,W] 0000-000
0x014 - 0x03C	-	-	-	-

IO Selector for ch.0-ch.3 (Base Timer) Base Address : 0x4002_5100

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	BTSEL0123 [B,H,W] 00000000	-
0x004 - 0x0FC	-	-	-	-

IO Selector for ch.4-ch.7(Base Timer) Base Address : 0x4002_5300

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	BTSEL4567 [B,H,W] 00000000	-
0x004 - 0x0FC	-	-	-	-

Software-based Simulation Startup (Base Timer) Base Address : 0x4002_5F00

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000 - 0x0FB	-	-	-	-
0x0FC	-	-	BTSSSR [B,H,W] XXXXXXXX XXXXXXXX	

12-bit A/DC unit0 **Base_Address : 0x4002_7000**

12-bit A/DC unit1 **Base_Address : 0x4002_7100**

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	ADCR[B,H,W] 000-0000	ADSR[B,H,W] 00---000
0x004	-	-	-	*
0x008	-	-	SCCR[B,H,W] 1000-000	SFNS[B,H,W] ----0000
0x00C	SCFD[B,H,W] XXXXXXXX XXXX---- 0001—XX ---XXXXX			
0x010	-	-	SCIS3[B,H,W] 00000000	SCIS2[B,H,W] 00000000
0x014	-	-	SCIS1[B,H,W] 00000000	SCIS0[B,H,W] 00000000
0x018	-	-	PCCR[B,H,W] 1000-000	PFNS[B,H,W] --XX--00
0x01C	PCFD[B,H,W] XXXXXXXX XXXX---- ---1-XXX ---XXXXX			
0x020	-	-	-	PCIS[B,H,W] 00000000
0x024	CMPD[B,H,W] 00000000 00------		-	CMPCR[B,H,W] 00000000
0x028	-	-	ADSS3[B,H,W] 00000000	ADSS2[B,H,W] 00000000
0x02C	-	-	ADSS1[B,H,W] 00000000	ADSS0[B,H,W] 00000000
0x030	-	-	ADST0[B,H,W] 00010000	ADST1[B,H,W] 00010000
0x034	-	-	-	ADCT[B,H,W] 00000111
0x038	-	-	SCTSL[B,H,W] ----0000	PRTSL[B,H,W] ----0000
0x03C	-	-	-	ADCEN[B,H,W] --00--00
0x040 - 0x0FC	-	-	-	-

PGA Base_Address : 0x4002_9000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	PGA_PWR[B,H,W] -------- -------- -------- -------0			
0x004	PGA_XSTB[B,H,W] -------- -------- -------- -------0			
0x008	PGA_EN[B,H,W] -------- -------- -------- -------0			
0x00C	AEFS[B,H,W] -------- -------- -------- -------0			
0x010	CHSW[B,H,W] -------- -------- -------- -------0			
0x014	GAIN[H,W] -------- -------- -----000 -------0			

FTH Base_Address : 0x4002_A000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	FTHON[B,H,W] -------- -------- -------- -------0			
0x004-0x0FC	-	-	-	-
0x100	BTCLKSEL[H,W] -------- -------- 00000000 00000000			

CR Trim Base_Address : 0x4002_E000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	MCR_PSR [B,H,W] ------01
0x004	-	-	MCR_FTRM[B,H,W] ------10 00000000	
0x008	-	-	-	*
0x00C	MCR_RLR[W] 00000000 00000000 00000000 00000001			
0x010 - 0x0FC	-	-	-	-

EXTI Base_Address : 0x4003_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	ENIR[B,H,W] 00000000 00000000 00000000 00000000			
0x004	EIRR[B,H,W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX			
0x008	EICL[B,H,W] 11111111 11111111 11111111 11111111			
0x00C	ELVR[R/W] 00000000 00000000 00000000 00000000			
0x010	ELVR1[R/W] 00000000 00000000 00000000 00000000			
0x014	-	-	NMIRR[B,H,W] -------- -------0	
0x018	-	-	NMICL[B,H,W] -------- -------1	
0x01C	-	-	-	-
0x020 - 0x0FC	-	-	-	-

INT-Req. READ Base_Address : 0x4003_1000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	DRQSEL[B,H,W] 00000000 00000000 00000000 00000000			
0x004	*			
0x008	-	-	-	*
0x00C	-	-	-	IRQCMODE[B,H,W] -------0
0x010	EXC02MON[B,H,W] -------- -------- -------- ------00			
0x014	IRQ00MON[B,H,W] -------- -------- -------- -------0			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x018	IRQ01MON[B,H,W] -------- -------- -------- -------0			
0x01C	IRQ02MON[B,H,W] -------- -------- -------- -------0			
0x020	IRQ03MON[B,H,W] -------- -------- -------- 00000000			
0x024	IRQ04MON[B,H,W] -------- -------- -------- 00000000			
0x028	IRQ05MON[B,H,W] -------- 00000000 00000000 00000000			
0x02C	IRQ06MON[B,H,W] -------- ----0000 00000000 00000000			
0x030	IRQ07MON[B,H,W] -------- -------- -------- -------0			
0x034	IRQ08MON[B,H,W] -------- -------- -------- ------00			
0x038	IRQ09MON[B,H,W] -------- -------- -------- -------0			
0x03C	IRQ10MON[B,H,W] -------- -------- -------- ------00			
0x040	IRQ11MON[B,H,W] -------- -------- -------- -------0			
0x044	IRQ12MON[B,H,W] -------- -------- -------- ------00			
0x048	IRQ13MON[B,H,W] -------- -------- -------- -------0			
0x04C	IRQ14MON[B,H,W] -------- -------- -------- ------00			
0x050	IRQ15MON[B,H,W] -------- -------- -------- -------0			
0x054	IRQ16MON[B,H,W] -------- -------- -------- ------00			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x058	IRQ17MON[B,H,W] -------- -------- -------- -------0			
0x05C	IRQ18MON[B,H,W] -------- -------- -------- ------00			
0x060	IRQ19MON[B,H,W] -------- -------- -------- -------0			
0x064	IRQ20MON[B,H,W] -------- -------- -------- ------00			
0x068	IRQ21MON[B,H,W] -------- -------- -------- -------0			
0x06C	IRQ22MON[B,H,W] -------- -------- -------- ------00			
0x070	IRQ23MON[B,H,W] -------- -------- -------0 00000000			
0x074	IRQ24MON[B,H,W] -------- -------- -------- 00000000			
0x078	IRQ25MON[B,H,W] -------- -------- -------- ----0000			
0x07C	IRQ26MON[B,H,W] -------- -------- -------- ----0000			
0x080	IRQ27MON[B,H,W] -------- -------- -------- ---00000			
0x084	IRQ28MON[B,H,W] -------- ------00 00000000 00000000			
0x088	IRQ29MON[B,H,W] -------- -------- ----0000 00000000			
0x08C	IRQ30MON[B,H,W] -------- ------00 00000000 00000000			
0x090	IRQ31MON[B,H,W] -------- -------- 00000000 00000000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x094	IRQ32MON[B,H,W] -------- -------- -------- 00000000			
0x098	IRQ33MON[B,H,W] -------- -------- -------- -----000			
0x09C	IRQ34MON[B,H,W] -------- -------- -------- ---00000			
0x0A0	IRQ35MON[B,H,W] -------- -------- -------- --000000			
0x0A4	IRQ36MON[B,H,W] -------- -------- -------- --000000			
0x0A8	IRQ37MON[B,H,W] -------- -------- -------- -0000000			
0x0AC	IRQ38MON[B,H,W] -------- -------- -------- -------0			
0x0B0	IRQ39MON[B,H,W] -------- -------- -------- -------0			
0x0B4	IRQ40MON[B,H,W] -------- -------- -------- -------0			
0x0B8	IRQ41MON[B,H,W] -------- -------- -------- -------0			
0x0BC	IRQ42MON[B,H,W] -------- -------- -------- -------0			
0x0C0	IRQ43MON[B,H,W] -------- -------- -------- -------0			
0x0C4	IRQ44MON[B,H,W] -------- -------- -------- -------0			
0x0C8	IRQ45MON[B,H,W] -------- -------- -------- -------0			
0x0CC	IRQ46MON[B,H,W] -------- -------- 00000000 00000000			
0x0D0	IRQ47MON[B,H,W] -------- -------- 00000000 00000000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0D4 - 0x1FC	-	-	-	-
0x200	DRQSEL1[B,H,W] 00000000 00000000 00000000 00000000			
0x204	DQESEL[B,H,W] 00000000 00000000 00000000 00000000			
0x208	*			
0x20C	-	-	-	*
0x210	RCINTSEL0[B,H,W] ---00000 ---00000 ---00000 ---00000			
0x214	RCINTSEL1[B,H,W] ---00000 ---00000 ---00000 ---00000			
0x218 - 0xFFC	-	-	-	-

IrDA Base_Address : 0x4003_2000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	RST_CTL[B,H,W] -------1
0x004	-	-	-	CLK_CTL[B,H,W] -----111
0x008	-	-	-	SER_SEL[B,H,W] -------0
0x00C-0x0FC	-	-	-	-
0x100	-	-	-	RDR/TDR[B,H,W] 00000000
0x104	-	-	-	IER[B,H,W] 0---0000(SIR1.0)
0x108	-	-	-	IIR[B,H,W] 11—0001(SIR1.0)
				FCR[B,H,W] 00000001(SIR1.0)
0x10C	-	-	-	LCR[B,H,W] -0000000
0x110	-	-	-	MCR[B,H,W] --000000
0x114	-	-	-	LSR[B,H,W] 01100000(SIR1.0)
0x118	-	-	-	MSR[B,H,W] ----0000
0x11C	-	-	-	SCR[B,H,W] 11111111(SIR1.0)
0x120-0x124	-	-	-	-
0x128	-	-	-	FCR[B,H,W] 00000001
0x12C-0x13C	-	-	-	-
0x140	-	-	-	BGDL[B,H,W] 11111111
0x144	-	-	-	BGDU[B,H,W] 11111111
0x148	-	-	-	EXCR2[B,H,W] ----0000
0x14C-0x150	-	-	-	-
0x154	-	-	-	-
0x158	-	-	-	TFLV[B,H,W] --000000
0x15C				RFLV[B,H,W] --000000
0x160-0x17C	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x180	-	-	-	TMRL[B,H,W] 00000001
0x184	-	-	-	TMRU[B,H,W] ----0000
0x188	-	-	-	IRCR1[B,H,W] 0---0000
0x18C	-	-	-	-
0x190	-	-	-	TFLL[B,H,W] 00000000
0x194	-	-	-	TFLU[B,H,W] ---00000
0x198	-	-	-	RFLL[B,H,W] 00000000
0x19C	-	-	-	RFLU[B,H,W] ---00000
0x1A0-0x1AC	-	-	-	-
0x1B0	-	-	-	IRCR2[B,H,W] -00000--
0x1B4	-	-	-	-
0x1B8	-	-	-	-
0x1BC	-	-	-	-
0x1C0	-	-	-	IRCR3[B,H,W] -----00-
0x1C4	-	-	-	-
0x1C8	-	-	-	SIRPW[B,H,W] ----0000
0x1CC-0x1E0	-	-	-	-
0x1E4	-	-	-	GPDATA[B,H,W] -------0
0x1E8-0x1EC	-	-	-	-
0x1F0	-	-	-	IRCFG1[B,H,W] 00000000
0x1F4-0x1F8	-	-	-	-
0x1FC	-	-	-	IRCFG4[B,H,W] 00-0----
0x200-0xFFC	-	-	-	-

GPIO Base_Address : 0x4003_3000

Base_Address + Address	Register +3	+2	+1	+0
0x000	PFR0[B,H,W] ---- ---- ---- ---- 0000 0000 0001 1111			
0x004	PFR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x008	PFR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x00C	PFR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x010	PFR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x014	PFR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x018	PFR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x01C – 0x34	-	-	-	-
0x038	PFRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x03C - 0x0FC	-	-	-	-
0x100	PCR0[B,H,W] ---- ---- ---- ---- 1111 1111 1111 1111			
0x104	PCR1[B,H,W] ---- ---- ---- ---- 1111 1111 1111 1111			
0x108	PCR2[B,H,W] ---- ---- ---- ---- 1111 1111 1111 1111			
0x10C	PCR3[B,H,W] ---- ---- ---- ---- 1111 1111 1111 1111			
0x110	PCR4[B,H,W] ---- ---- ---- ---- 1111 1111 1111 1111			
0x114	PCR5[B,H,W] ---- ---- ---- ---- 1111 1111 1111 1111			

Base_Address + Address	Register +3	+2	+1	+0
0x118	PCR6[B,H,W] ---- ---- ---- ---- 1111 1111 1111 1111			
0x11C - 0x134	-	-	-	-
0x138	PCRE[B,H,W] ---- ---- ---- ---- 1111 1111 1111 1111			
0x13C - 0x1FC	-	-	-	-
0x200	DDR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x204	DDR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x208	DDR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x20C	DDR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x210	DDR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x214	DDR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x218	DDR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x21C-0x234	-	-	-	-
0x238	DDRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x23C - 0x2FC	-	-	-	-
0x300	PDIR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x304	PDIR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			

Base_Address + Address	Register +3	+2	+1	+0
0x308	PDIR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x30C	PDIR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x310	PDIR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x314	PDIR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x318	PDIR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x31C – 0x334	-	-	-	-
0x338	PDIRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x33C - 0x3FC	-	-	-	-
0x400	PDOR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x404	PDOR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x408	PDOR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x40C	PDOR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x410	PDOR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x414	PDOR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x418	PDOR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x41C -0x434	-	-	-	-

Base_Address + Address	Register			
	+3	+2	+1	+0
0x438	PDORE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x43C - 0x4FC	-	-	-	-
0x500	ADE[B,H,W] ---- ---- ---- ---- ---- ---- 1111 1111			
0x504 - 0x57C	-	-	-	-
0x580	SPSR[B,H,W] ---- ---- ---- ---- ---- ---- --00 0101			
0x584 - 0x5FC	-	-	-	-
0x600	EPFR00[B,H,W] ---- --00 ---- --11 -000 -000 0000 -000			
0x604	-			
0x608	-			
0x60C	-			
0x610	EPFR04[B,H,W] --00 0000 --00 00-- --00 0000 -000 00--			
0x614	EPFR05[B,H,W] --00 0000 --00 00-- --00 0000 --00 00--			
0x618	EPFR06[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x61C	EPFR07[B,H,W] -000 0000 0000 0000 0000 0000 0000 ----			
0x620	EPFR08[B,H,W] -000 0000 0000 0000 0000 0000 0000 0000			
0x624	EPFR09[B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x628	-			
0x62C	-			
0x630	-			

Base_Address + Address	Register +3	+2	+1	+0
0x634	-			
0x638	-			
0x63C	-			
0x640	-			
0x644	-			
0x648	-			
0x64C - 0x6FC	-	-	-	-
0x700	PZR0[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x704	PZR1[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x708	PZR2[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x70C	PZR3[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x710	PZR4[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x714	PZR5[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x718	PZR6[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x71C	-	-	-	-
0x738	PZRE[B,H,W] ---- ---- ---- ---- 0000 0000 0000 0000			
0x73C - 0x7FC	-	-	-	-
0x800	*			
0x804	*			
0x808 - 0xFFC	-	-	-	-

LVD Base_Address : 0x4003_5000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	LVD_CTL [B,H,W] 010000--
0x004	-	-	-	LVD_STR [B,H,W] 0-------
0x008	-	-	-	LVD_CLR [B,H,W] 1-------
0x00C	STB_CTL[W] 00000000 00000000 -------- ---0-000			
0x010	-	-	-	LVD_STR2 0-------
0x014 - 0xFFC	-	-	-	-

DS_Mode Base_Address : 0x4003_5100

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	REG_CTL[B,H,W] -------0
0x004	-	-	-	RCK_CTL[B,H,W] ------01
0x008 - 0x6FC	-	-	-	-
0x700	-	-	-	PMD_CTL[B,H,W] -------0
0x704	-	-	-	WRFSR[B,H,W] ------00
0x708	-	-	WIFSR[B,H,W] ------00 00000000	
0x70C	-	-	WIER[B,H,W] ------00 00000000	
0x710	-	-	-	WILVR[B,H,W] ---00000
0x714	-	-	-	DSRAMR[B,H,W] ----0000
0x718	PWR_DN [B, H, W] x------- -------- -------- ---00000			
0x71C	PWR_ON [B, H, W] x------- -------- -------- ---00000			
0x720	PWR_ST [B, H, W] -------- ----0000 -------- ---11111			
0x800	BUR04[B,H,W] 00000000	BUR03[B,H,W] 00000000	BUR02[B,H,W] 00000000	BUR01[B,H,W] 00000000
0x804	BUR08[B,H,W] 00000000	BUR07[B,H,W] 00000000	BUR06[B,H,W] 00000000	BUR05[B,H,W] 00000000
0x808	BUR012[B,H,W] 00000000	BUR11[B,H,W] 00000000	BUR10[B,H,W] 00000000	BUR09[B,H,W] 00000000
0x80C	BUR16[B,H,W] 00000000	BUR15[B,H,W] 00000000	BUR14[B,H,W] 00000000	BUR13[B,H,W] 00000000
0x810 - 0xEFC	-	-	-	-

MFS ch.0 Base_Address : 0x4003_8000

MFS ch.1 Base_Address : 0x4003_8100

MFS ch.2 Base_Address : 0x4003_8200

MFS ch.3 Base_Address : 0x4003_8300

MFS ch.4 Base_Address : 0x4003_8400

MFS ch.5 Base_Address : 0x4003_8500

MFS ch.6 Base_Address : 0x4003_8600

MFS ch.0, ch.4, ch.5

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	SCR/ IBCR[B,H,W] 0--00000	SMR[B,H,W] 000000-0
0x004	-	-	SSR[B,H,W] 0-000011	ESCR/ IBSR[B,H,W] 00000000
0x008	-	-	RDR/TDR[H,W] -------0 00000000	
0x00C	-	-	BGR1[B,H,W] 00000000	BGR0[B,H,W] 00000000
0x010	-	-	ISMK[B,H,W] --------	ISBA[B,H,W] --------
0x014 - 0x01C	-	-	-	-
0x020	-	-	SACSR [B,H,W] --000--- --------	
0x024	-	-	SCSCR [B,H,W] 00000000 001---00	
0x028	-	-	SCSTR1/EIBCR [B, H, W] 00000000/--001100	SCSTR0[B, H, W] 00000000
0x2C	-	-	SCSTR3[B, H, W] 00000000	SCSTR2[B, H, W] 00000000
0x030	-	-	SCSFR1[B, H, W] 10000000	SCSFR0[B, H, W] 10000000
0x034	-	-	-	SCSFR2[B, H, W] 10000000
0x038	-	-	TBYTE1[B, H, W] 00000000	TBYTE0[B, H, W] 00000000
0x03C	-	-	TBYTE3[B, H, W] 00000000	TBYTE2[B, H, W] 00000000
0x040 - 0x0FF	-	-	-	-

MFS ch.1, ch.2, ch.3, ch.6

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	SCR/ IBCR[B,H,W] 0--00000	SMR[B,H,W] 000000-0
0x004	-	-	SSR[B,H,W] 0-000011	ESCR/ IBSR[B,H,W] 00000000
0x008	-	-	RDR/TDR[H,W] -------0 00000000	
0x00C	-	-	BGR1[B,H,W] 00000000	BGR0[B,H,W] 00000000
0x010	-	-	ISMK[B,H,W] --------	ISBA[B,H,W] --------
0x014 - 0x024	-	-	-	-
0x028	-	-	SCSTR1/EIBCR [B, H, W] 00000000/--001100	-
0x02C - 0x0FF	-	-	-	-

CRC Base_Address : 0x4003_9000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	-	-	CRCCR[B,H,W] -0000000
0x004	CRCINIT[B,H,W] 11111111 11111111 11111111 11111111			
0x008	CRCIN[B,H,W] 00000000 00000000 00000000 00000000			
0x00C	CRCR[B,H,W] 11111111 11111111 11111111 11111111			

Watch Counter Base_Address : 0x4003_A000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	-	WCCR[B,H,W] 00--0000	WCRL[B,H,W] --000000	WCRD[B,H,W] --000000
0x004 - 0x00C	-	-	-	-
0x010	-	-	CLK_SEL[B,H,W] -----000 -------0	
0x014	-	-	-	CLK_EN[B,H,W] ------00
0x018 - 0xFFC	-	-	-	-

RTC Base_Address : 0x4003_B000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x000	WTCR1[B,H,W] 00000000 00000000 ---00000 -00000-0			
0x004	WTCR2[B,H,W] -------- -------- -----000 -------0			
0x008	WTBR[B,H,W] -------- 00000000 00000000 00000000			
0x00C	WTDR[B,H,W] --000000	WTHR[B,H,W] --000000	WTMIR[B,H,W] -0000000	WTSR[B,H,W] -0000000
0x010	-	WTYR[B,H,W] 00000000	WTMOR[B,H,W] ---00000	WTDW[B,H,W] -----000
0x014	ALDR[B,H,W] --000000	ALHR[B,H,W] --000000	ALMIR[B,H,W] -0000000	-
0x018	-	ALYR[B,H,W] 00000000	ALMOR[B,H,W] ---00000	-
0x01C	WTTR[B,H,W] -------- ------00 00000000 00000000			
0x020	-	-	WTCLKM[B,H,W] ------00	WTCLKS [B,H,W] -------0
0x024	-	WTCALEN[B,H,W] -------0	WTCAL [B,H,W] ------00 00000000	
0x028	-	-	WTDIVEN[B,H,W] ------00	WTDIV [B,H,W] ----0000
0x02C	-	-	-	WTCALPRD [B,H,W] --010011
0x030	-	-	-	WTCOSEL [B,H,W] -------0
0x034 - 0xFFC	-	-	-	-

RAC Base_Address : 0x4005_6000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0000	CITR [B,H,W] ---- ---- 0000 0000 ---- ---- ---0 ----			
0x0004	- -	- -	- -	- -
0x0008	AITR [B,H,W] ---0 0000 –00 0000 ---- 0000 ---- 0000			
0x000C	CIMR [B,H,W] ---- ---- ---- -000 ---- ---- ---0 ----			
0x0010	AIMR [B,H,W] ---- ---- ---- ---- ---- ---- ---- 1111			
0x0014	CFSMR [B,H,W] ---- ---- ---- -11- ---- ---- ---- ----			
0x0018	AFSMR [B,H,W] ---- ---- ---- ---- ---- ---- ---- 1111			
0x001C	CITR_CLR [B,H,W] ---- ---- ---- 1111 ---- ---- ---1 ----			
0x0020 - 0x0034	- -	- -	- -	- -
0x0038	MEMCNTL [B,H,W] ---- ---- ---- ---- ---- ---0 ---- ----			
0x003C - 0x0040	- -	- -	- -	- -
0x0044	RCSM [B,H,W] ---0 0000 ---0 0000 ---0 0000 ---0 0000			
0x0048 - 0x005C	- -	- -	- -	- -
0x0060	SRCR [B,H,W] ---- ---- ---- ---- ---- ---- ---- --00			
0x0064 - 0x0068	- -	- -	- -	- -
0x006C	RMCR [B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x0070	FST [B,H,W] ---- ---- ---- ---- ---- ---- ---- ---0			
0x0074 - 0x00FC	- -	- -	- -	- -
0x0100	RLAR [B,H,W] 0-00 0000 0-00 0000 ---- -000 ---0 0000			
0x0104	RSTS [B,H,W] 0000 0000 0000 0000 0000 0000 ---- 00-0			
0x0108	RCLR [B,H,W] ---1 ---1 ---- ---1 ---- ---1 ---- 11-1			
0x010C	RMSK [B,H,W] ---1 ---1 ---- ---0 ---- ---0 ---- 00-0			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0110	RTMR [B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x0114 - 0x013C	- -	- -	- -	- -
0x0140	RSMB0 [B,H,W] ---- -000 0000 00-- ---- -000 0000 00--			
0x0144	RSMB1 [B,H,W] ---- -000 0000 00-- ---- -000 0000 00--			
0x0148	RSMB2 [B,H,W] ---- -000 0000 00-- ---- -000 0000 00--			
0x014C	RSMB3 [B,H,W] ---- -000 0000 00-- ---- -000 0000 00--			
0x0150	RLPC0 [B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x0154	RLPC1 [B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x0158 – 0x015C	- -	- -	- -	- -
0x0160	ACC0VAL0 [B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x0164	ACC0VAL1 [B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x0168	ACC0VAL2 [B,H,W] ---- ---- ---- ---- ---- ---- 0000 0000			
0x016C	- -	- -	- -	- -
0x0170	ACC1VAL0 [B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x0174	ACC1VAL1 [B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x0178	ACC1VAL2 [B,H,W] ---- ---- ---- ---- ---- ---- 0000 0000			
0x017C	- -	- -	- -	- -
0x0180	RSREG0 [B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x0184	RSREG1 [B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x0188	RSREG2 [B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x018C	RSREG3 [B,H,W] 0000 0000 0000 0000 0000 0000 0000 0000			
0x0190 - 0x03FC	- -	- -	- -	- -

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0400 + 0x8 * n [n]: 0 to 63	RDDC [B,H,W] 0XXX -XXX XXXX XXXX XXXX XXXX XXXX XXXX			
0x0404 + 0x8 * n [n]: 0 to 63	RDDA [B,H,W] XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX			
0x0600	- -	- -	- -	- -
0x0604	RDSTS [B,H,W] ---- ---- ---- ---- ---- --00 ---- -000			
0x0608	RDCLR [B,H,W] ---- ---- ---- ---- ---- ---1 ---- --11			
0x060C	RDMSK [B,H,W] ---- ---- ---- ---- ---- ---0 ---- --00			
0x0610 - 0x07FC	- -	- -	- -	- -

DMAC Base_Address : 0x4006_0000

Base_Address + Address	Register			
	+3	+2	+1	+0
0x0000	DMACR[B,H,W] 00-00000 -------- -------- --------			
0x0010	DMACA0[B,H,W] 00000000 0---0000 00000000 00000000			
0x0014	DMACB0[B,H,W] --000000 00000000 00000000 -------0			
0x0018	DMACSA0[B,H,W] 00000000 00000000 00000000 00000000			
0x001C	DMACDA0[B,H,W] 00000000 00000000 00000000 00000000			
0x0020	DMACA1[B,H,W] 00000000 0---0000 00000000 00000000			
0x0024	DMACB1[B,H,W] --000000 00000000 00000000 -------0			
0x0028	DMACSA1[B,H,W] 00000000 00000000 00000000 00000000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x002C	DMACDA1[B,H,W] 00000000 00000000 00000000 00000000			
0x0030	DMACA2[B,H,W] 00000000 0---0000 00000000 00000000			
0x0034	DMACB2[B,H,W] --000000 00000000 00000000 -------0			
0x0038	DMACSA2[B,H,W] 00000000 00000000 00000000 00000000			
0x003C	DMACDA2[B,H,W] 00000000 00000000 00000000 00000000			
0x0040	DMACA3[B,H,W] 00000000 0---0000 00000000 00000000			
0x0044	DMACB3[B,H,W] --000000 00000000 00000000 -------0			
0x0048	DMACSA3[B,H,W] 00000000 00000000 00000000 00000000			
0x004C	DMACDA3[B,H,W] 00000000 00000000 00000000 00000000			
0x0050	DMACA4[B,H,W] 00000000 0---0000 00000000 00000000			
0x0054	DMACB4[B,H,W] --000000 00000000 00000000 -------0			
0x0058	DMACSA4[B,H,W] 00000000 00000000 00000000 00000000			
0x005C	DMACDA4[B,H,W] 00000000 00000000 00000000 00000000			
0x0060	DMACA5[B,H,W] 00000000 0---0000 00000000 00000000			
0x0064	DMACB5[B,H,W] --000000 00000000 00000000 -------0			
0x0068	DMACSA5[B,H,W] 00000000 00000000 00000000 00000000			

Base_Address + Address	Register			
	+3	+2	+1	+0
0x006C	DMACDA5[B,H,W] 00000000 00000000 00000000 00000000			
0x0070	DMACA6[B,H,W] 00000000 0---0000 00000000 00000000			
0x0074	DMACB6[B,H,W] --000000 00000000 00000000 -------0			
0x0078	DMACSA6[B,H,W] 00000000 00000000 00000000 00000000			
0x007C	DMACDA6[B,H,W] 00000000 00000000 00000000 00000000			
0x0080	DMACA7[B,H,W] 00000000 0---0000 00000000 00000000			
0x0084	DMACB7[B,H,W] --000000 00000000 00000000 -------0			
0x0088	DMACSA7[B,H,W] 00000000 00000000 00000000 00000000			
0x008C	DMACDA7[B,H,W] 00000000 00000000 00000000 00000000			
0x0090 - 0x00FC	-	-	-	-

Revision History

Document Revision History

Document Title: FM3 Family, MB9AF0A1M Peripheral Manual Sensor Microcontroller Part Document Number: 002-07831				
Revision	**ECN No.**	**Date**	**Origin of Change**	**Description of Change**
**	—	12/26/2012	AKIH	Initial release
*A	5338093	07/05/2016	AKIH	Migrated to Cypress format