EZ-PD™ PMG1-S0 MCU architecture

Reference manual

About this document

Scope and purpose

EZ-PD™ PMG1-Sx (Power Delivery MCU Gen1) is a family of high-voltage USB-C Power Delivery (PD) microcontrollers (MCU). These chips include an Arm® Cortex®-M0/M0+ CPU and USB-C PD controller along with analog and digital peripherals. EZ-PD™ PMG1-S0 MCU is targeted for any embedded system that provides/consumes power to/from a high-voltage USB-C PD port and leverages the microcontroller to provide additional control capability.

Intended audience

The document is intended for users of EZ-PD™ PMG1-S0 MCU.

Table of contents

Scope and purpose 1

Intended audience 1

Table of contents 2

Section A: Overview 9

1 Introduction 10
1.1 Top-level architecture 13
1.2 Features 14

1 Getting started 15
1.1 EZ-PD™ PMG1 MCU resources 15

1 Document construction 16
1.1 Major sections 16
1.2 Documentation conventions 16
1.2.1 Register conventions 16
1.2.2 Numeric naming 16
1.2.3 Units of measure 17
1.2.4 Acronyms 18

Section B: CPU system 22

1 Arm® Cortex®-M0 CPU 23
1.1 Features 23
1.2 Block diagram 23
1.3 How it works 24
1.3.1 Registers 24
1.3.2 Operating modes 25
1.3.3 Instruction set 26
1.3.3.1 Address alignment 27
1.3.3.2 Memory endianness 27
1.3.4 Systick timer 27
1.3.5 Debug 28

1 Interrupts 29
1.1 Features 29
1.2 How it works 29
1.3 Interrupts and exceptions - operation 30
1.3.1 Interrupt/Exception handling in EZ-PD™ PMG1-S0 MCU 30
1.3.2 Level and pulse interrupts 31
1.3.3 Exception vector table 32
1.4 Exception sources 33
1.4.1 Reset exception 33
1.4.2 Non-Maskable Interrupt (NMI) exception 33
1.4.3 HardFault exception 33
1.4.4 Supervisor Call (SVCall) exception 33
1.4.5 PendSV exception 34
1.4.6 SysTick exception 34
1.5 Interrupt sources 34
1.6 Exception priority 35

Table of contents

1.7 Enabling/disabling interrupts . . . 36
1.8 Exception states . . . 37
1.8.1 Pending exceptions . . . 37
1.9 Stack usage for exceptions . . . 38
1.10 Interrupts and low-power modes . . . 38
1.11 Exception - initialization and configuration . . . 39
1.12 Registers . . . 39
1.13 Associated documents . . . 39

Section C: Memory system 40

1 Memory map . . . 41
1.1 Features . . . 41
1.2 How it works . . . 41

Section D: System-wide resources 43

1 I/O system . . . 44
1.1 Features . . . 44
1.2 Block diagram . . . 45
1.3 GPIO drive modes . . . 46
1.3.1 High-impedance (high-Z) analog . . . 47
1.3.2 High-impedance (high-Z) digital . . . 47
1.3.3 Resistive pull-up or resistive pull-down . . . 47
1.3.4 Open drain drives HIGH and open drain drives LOW . . . 48
1.3.5 Strong drive . . . 48
1.3.6 Resistive pull-up and resistive pull-down . . . 48
1.4 Slew rate control . . . 48
1.5 CMOS LVTTL level control . . . 48
1.6 Fail-Safe GPIOs . . . 49
1.7 High-Speed I/O Matrix . . . 49
1.8 Firmware controlled GPIO . . . 50
1.9 I/O port reconfiguration . . . 50
1.10 I/O state on power up . . . 50
1.11 Behavior in low-power modes . . . 50
1.12 GPIO Interrupt . . . 51
1.12.1 Features . . . 51
1.12.2 Interrupt controller block diagram . . . 51
1.12.3 Function and configuration . . . 52
1.13 Registers . . . 52

1 Clocking system . . . 53
1.1 Block diagram . . . 53
1.2 Clock sources . . . 54
1.2.1 Internal main oscillator (IMO) . . . 54
1.2.1.1 Startup behavior . . . 54
1.2.2 Internal low-speed oscillator (ILO) . . . 54
1.2.3 External clock . . . 54
1.3 Clock distribution . . . 54
1.3.1 HFCLK input selection . . . 55
1.3.2 HFCLK predivider configuration . . . 55
1.3.3 SYSCLK prescaler configuration . . . 55
1.3.4 Peripheral clock divider configuration . . . 56

Table of contents

1.4 Low-power mode operation . . . 57
1.5 Register list . . . 57

1 Power supply and modes . . . 58
1.1 Block diagram . . . 58
1.2 Power system requirement overview . . . 58
1.3 Power modes . . . 59
1.4 Mode transitions . . . 59

1 Chip operational modes . . . 60
1.1 Boot . . . 60
1.2 User . . . 60
1.3 Privileged . . . 60
1.4 Debug . . . 60

1 Watchdog timer (WDT) . . . 61
1.1 Features . . . 61
1.2 Block diagram . . . 61
1.3 How it works . . . 61
1.3.1 Enabling and disabling WDT . . . 62
1.3.2 WDT interrupts and Low-power modes . . . 62
1.3.3 WDT reset mode . . . 62
1.4 Register list . . . 63

1 Reset system . . . 64
1.1 Reset sources . . . 64
1.1.1 Power-on reset (POR) . . . 64
1.1.2 Brownout reset (BOD) . . . 64
1.1.3 Watchdog reset (WRES) . . . 64
1.1.4 Software initiated reset (SRES) . . . 64
1.1.5 Protection fault reset (PROT_FAULT) . . . 65
1.2 Identifying reset sources . . . 65
1.3 Register list . . . 65

1 Device security . . . 66
1.1 Features . . . 66
1.2 How it works . . . 66

Section E: Digital system 67

1 Serial communications block (SCB) . . . 68
1.1 Features . . . 68
1.2 Serial peripheral interface (SPI) . . . 68
1.2.1 Features . . . 68
1.2.2 General description . . . 69
1.2.3 SPI modes of operation . . . 70
1.2.3.1 Motorola SPI . . . 70
1.2.3.2 Texas Instruments SPI . . . 73
1.2.3.3 National Semiconductors SPI . . . 75
1.2.4 Easy SPI (EZSPI) protocol . . . 76
1.2.4.1 EZ Address Write . . . 76
1.2.4.2 Memory Array Write . . . 76
1.2.4.3 Memory Array Read . . . 76
1.2.4.4 Configuring SCB for EZSPI mode . . . 78

Table of contents

1.2.5 SPI registers . . . 78
1.2.6 SPI interrupts . . . 79
1.2.7 Enabling and initializing SPI . . . 79
1.2.8 Internally and externally clocked SPI operations . . . 81
1.2.8.1 Non-EZ mode of operation . . . 82
1.2.8.2 EZ mode of operation . . . 83
1.3 Universal asynchronous receiver/transmitter (UART) . . . 84
1.3.1 Features . . . 84
1.3.2 General description . . . 85
1.3.3 UART modes of operation . . . 85
1.3.3.1 Standard protocol . . . 85
1.3.3.2 SmartCard (ISO7816) . . . 89
1.3.3.3 IrDA . . . 90
1.3.4 UART registers . . . 91
1.3.5 UART interrupts . . . 91
1.3.6 Enabling and initializing UART . . . 92
1.4 Inter integrated cCircuit (I2C) . . . 93
1.4.1 Features . . . 93
1.4.2 General description . . . 94
1.4.3 Terms and definitions . . . 94
1.4.4 I2C modes of operation . . . 95
1.4.4.1 Write transfer . . . 96
1.4.4.2 Read transfer . . . 97
1.4.5 Easy I2C (EZI2C) protocol . . . 97
1.4.6 Memory array write . . . 98
1.4.7 Memory array read . . . 98
1.4.8 I2C registers . . . 99
1.4.9 I2C interrupts . . . 100
1.4.10 Enabling and initializing the I2C . . . 100
1.4.11 Internal and external clock operation in I2C . . . 102
1.4.11.1 I2C Non-EZ operation mode . . . 102
1.4.11.2 EZ operation mode . . . 103
1.4.12 Wake up from sleep . . . 103
1.4.13 Master mode transfer examples . . . 104
1.4.13.1 Master transmit . . . 104
1.4.13.2 Master receive . . . 105
1.4.14 Slave mode transfer examples . . . 106
1.4.14.1 Slave transmit . . . 106
1.4.14.2 Slave receive . . . 107
1.4.15 EZ slave mode transfer example . . . 108
1.4.15.1 EZ slave transmit . . . 108
1.4.15.2 EZ slave receive . . . 109
1.4.16 Multi-master mode transfer example . . . 110
1.4.16.1 Multi-master - slave not enabled . . . 110
1.4.16.2 Multi-master - slave enabled . . . 111

1 Timer, Counter, and PWM . . . 112

1.1 Features . . . 112
1.2 Block diagram . . . 112
1.2.1 Enabling and disabling counter in TCPWM block . . . 113

Table of contents

1.2.2 Clocking . . . 113
1.2.3 Events-based on trigger inputs . . . 114
1.2.4 Output signals . . . 115
1.2.4.1 Signals upon trigger conditions . . . 115
1.2.4.2 Interrupts . . . 116
1.2.4.3 Outputs . . . 116
1.2.5 Power modes . . . 117
1.3 Modes of operation . . . 117
1.3.1 Timer mode . . . 118
1.3.1.1 Block diagram . . . 118
1.3.1.2 How it works . . . 118
1.3.1.3 Configuring counter for timer mode . . . 120
1.3.2 Capture mode . . . 120
1.3.2.1 Block diagram . . . 120
1.3.2.2 How it works . . . 121
1.3.2.3 Configuring counter for capture mode . . . 122
1.3.3 Quadrature decoder mode . . . 122
1.3.3.1 Block diagram . . . 122
1.3.3.2 How it works . . . 123
1.3.3.3 Configuring counter for quadrature mode . . . 125
1.3.4 Pulse width modulation (PWM) mode . . . 125
1.3.4.1 Block diagram . . . 125
1.3.4.2 How it works . . . 126
1.3.4.3 Other configurations . . . 127
1.3.4.4 Kill feature . . . 128
1.3.4.5 Configuring counter for PWM mode . . . 128
1.3.5 Pulse width modulation pseudo-random mode . . . 129
1.3.5.1 Block diagram . . . 129
1.3.5.2 How it works . . . 129
1.3.5.3 Configuring counter for pseudo-random PWM mode . . . 130
1.4 TCPWM registers . . . 131

Section F: Universal serial bus (USB) Power Delivery (PD) 132

1 Universal serial bus (USB) Power Delivery (PD) . . . 133
1.1 Block applications . . . 134
1.2 ADC block . . . 134
1.2.1 ADC block architecture and functional overview . . . 134
1.2.2 CC Block . . . 135
1.2.2.1 CC block architecture and functional overview . . . 135
1.2.3 CHGDET block . . . 137
1.2.3.1 CHGDET block architecture and functional overview . . . 137
1.2.4 Low-side CSA block . . . 138
1.2.4.1 Low-side CSA block architecture and functional overview . . . 138
1.2.5 PGDO block . . . 140
1.2.5.1 PGDO block architecture and functional overview . . . 140
1.2.6 REFGEN block . . . 141
1.2.6.1 REFGEN functional description . . . 141
1.2.7 SHV_REG block . . . 142
1.2.7.1 SHV_REG block architecture and functional overview . . . 142
1.2.8 UVOV block . . . 143

Table of contents

1.2.8.1 UVOV block architecture and functional description ... 143
1.2.9 VBUS_DISCHG_PROG block ... 144
1.2.9.1 VBUS_DISCHG_PROG block architecture and functional overview ... 144
1.2.10 VBUS_DISCHG block ... 145
1.2.10.1 VBUS_DISCHG block architecture and functional overview ... 145

Section G: Program and debug 146

1 Program and debug interface ... 147
1.1 Features ... 147
1.2 Functional description ... 147
1.3 Serial wire debug (SWD) interface ... 148
1.3.1 SWD timing details ... 149
1.3.2 Acknowledge (ACK) details ... 150
1.3.3 Turnaround (Trn) period details ... 150
1.4 Arm® Cortex®-M0 debug and access port (DAP) ... 150
1.4.1 Debug port (DP) registers ... 151
1.4.2 Access port (AP) registers ... 151
1.5 Programming the EZ-PD™ PMG1-S0 MCU device ... 152
1.5.1 SWD port acquisition ... 152
1.5.1.1 Primary and secondary SWD pin pairs ... 152
1.5.1.2 SWD port acquire sequence ... 152
1.5.2 SWD programming mode entry ... 152
1.5.3 SWD programming routines executions ... 153
1.6 EZ-PD™ PMG1-S0 MCU SWD debug interface ... 153
1.6.1 Debug control and configuration registers ... 153
1.6.2 Breakpoint unit (BPU) ... 153
1.6.3 Data watchpoint (DWT) ... 154
1.6.4 Debugging the EZ-PD™ PMG1-S0 MCU device ... 154
1.7 Registers ... 155

1 Nonvolatile memory programming ... 156
1.1 Features ... 156
1.2 Functional description ... 156
1.3 System call implementation ... 157
1.4 Blocking and non-blocking system calls ... 157
1.4.1 Performing a system call ... 158
1.5 System calls ... 159
1.5.1 Silicon ID ... 160
1.5.2 Configure clock ... 161
1.5.3 Load flash bytes ... 162
1.5.4 Write row ... 163
1.5.5 Program row ... 164
1.5.6 Erase all ... 165
1.5.7 Checksum ... 166
1.5.8 Write protection ... 166
1.5.9 Non-Blocking write row ... 167
1.5.10 Non-blocking program row ... 168
1.5.11 Resume non-blocking ... 169
1.6 System call status ... 170
1.7 Non-blocking system call pseudo code ... 171

Table of contents

References 175
Glossary 176
Revision history 192
Disclaimer 193

Section A: Overview

This section encompasses the following chapters:

- **"Introduction"** on page 10
- **"Getting started"** on page 15
- **"Document construction"** on page 16

1 Introduction

EZ-PD™ PMG1 (Power Delivery microcontroller Gen1) is a family of high-voltage USB-C Power Delivery (PD) microcontrollers (MCU). These chips include an Arm® Cortex®-M0/M0+ CPU and USB-C PD controller along with analog and digital peripherals. EZ-PD™ PMG1 is targeted for any embedded system that provides/consumes powers to/from a high-voltage USB-C PD port and leverages the microcontroller to provide additional control capability. **Figure 1-1** shows the EZ-PD™ PMG1 family segmentation.

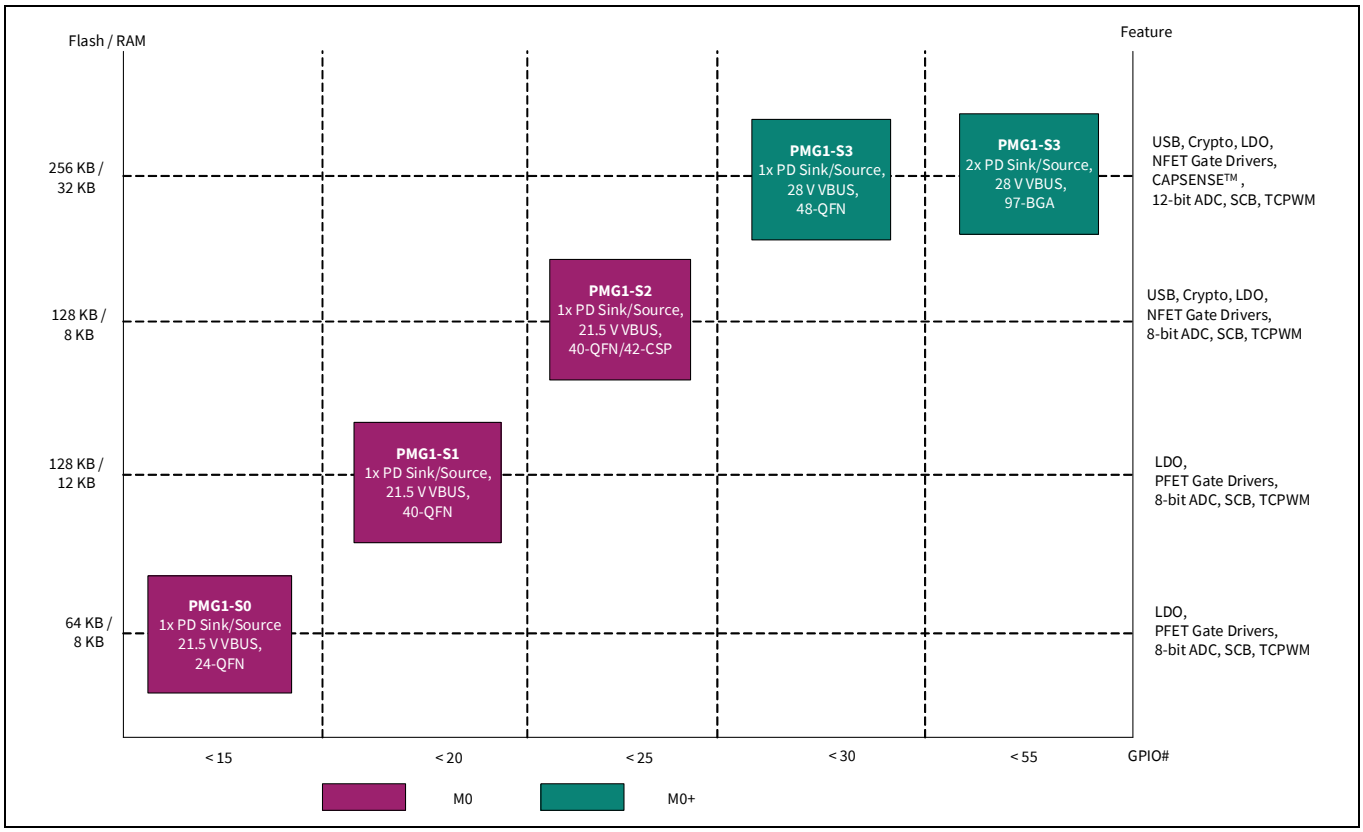


Figure 1-1. EZ-PD™ PMG1-Sx family segmentation

Table shows the comparison of features of different MCUs of the EZ-PD™ PMG1 family.

Table 1-1. Comparison of features of different MCUs of the EZ-PD™ PMG1 family

Subsystem or range	Item	EZ-PD™ PMG1-S0	EZ-PD™ PMG1-S1	EZ-PD™ PMG1-S2	EZ-PD™ PMG1-S3
CPU and Memory subsystem	Core	Arm® Cortex®-M0	Arm® Cortex®-M0	Arm® Cortex®-M0	Arm® Cortex®-M0+
	Max. freq (MHz)	48	48	48	48
	Flash (KB)	64	128	128	256
	SRAM (KB)	8	12	8	32

Table 1-1. Comparison of features of different MCUs of the EZ-PD™ PMG1 family (continued)

Subsystem or range	Item	EZ-PD™ PMG1-S0	EZ-PD™ PMG1-S1	EZ-PD™ PMG1-S2	EZ-PD™ PMG1-S3
Power delivery	Power delivery Ports	1	1	1	1 port for 48-QFN 2 ports for 97-BGA
	Role	DRP	DRP	DRP	DRP
	MOSFET gate drivers	2x PFET	2x PFET	2x NFET	Flexible 2x NFET
	Fault protections	VBUS OVP, UVP, and OCP. SCP (for source configuration only)	VBUS OVP, UVP, and OCP. SCP and RCP (for Source Configuration only)	VBUS, OVP, UVP, and OCP	VBUS OVP, UVP, and OCP. SCP and RCP (for Source Configuration only).
USB	Integrated full speed USB 2.0 Device with Billboard class support	No	No	Yes	Yes
Voltage Range	Supply (V)	VDDD (2.7–5.5) VBUS (4–21.5)	VSYS (2.75–5.5) VBUS (4– 21.5)	VSYS (2.7–5.5) VBUS (4–21.5)	VSYS (2.8–5.5) VBUS (4–28)
	IO (V)	1.71 - 5.5	1.71 - 5.5	1.71 - 5.5	1.71 - 5.5
Digital	SCB (configurable as I^2C/UART/SPI)	2	4	4	7 for 48-QFN (out of which only 5 can be configured as SPI and UART) 8 for 97-BGA
	TCPWM Block (configurable as timer, counter or pulse-width modulator)	4	2	4	8
	Hardware authentication block (Crypto)	No	No	Yes (AES-128/192/256, SHA1, SHA2-224, SHA2-256, PRNG, CRC)	Yes (AES-128, SHA2-256, TRNG, vector unit)
Analog	ADC	2x 8-bit SAR	1x 8-bit SAR	2x 8-bit SAR	2x 8-bit SAR 1x 12-bit SAR
	On-chip Temperature Sensor	Yes	Yes	Yes	Yes
Direct memory access (DMA)	DMA	No	No	No	Yes

Table 1-1. Comparison of features of different MCUs of the EZ-PD™ PMG1 family (continued)

Subsystem or range	Item	EZ-PD™ PMG1-S0	EZ-PD™ PMG1-S1	EZ-PD™ PMG1-S2	EZ-PD™ PMG1-S3
GPIO	Max # of I/Os	12 (10 + 2 Fail-Safe)	17 (15 + 2 Fail-Safe)	20 (18 + 2 Fail-Safe)	26 (24 + 2 Fail-Safe) for 48-QFN 50 (48 + 2 Fail-Safe) for 97-BGA
Charging Standards	Charging source	BC 1.2, AC, AFC and QC 3.0	BC 1.2, AC	BC 1.2, AC	BC 1.2, AC, AFC, and QC 3.0
	Charging sink	BC 1.2, AC and QC 2.0	BC 1.2, AC	BC 1.2, AC	BC 1.2, AC and QC 2.0
ESD protection	ESD protection	Yes (Human body model and charged device model)	Yes (Human body model and charged device model)	Yes (Human body model and charged device model)	Yes (Human body model and charged device model)
Packages	Package options	24-QFN (4 × 4 mm, 0.5 mm pitch)	40-QFN (6 × 6 mm, 0.5 mm pitch)	40-QFN (6 × 6 mm, 0.5 mm pitch) 42-CSP (2.63 × 3.18 mm, 0.4 mm pitch)	48-QFN (6 × 6 mm, 0.5 mm pitch) 97-BGA (6 × 6 mm, 0.5 mm and 0.65 mm pitch)

The rest of the document discusses the EZ-PD™ PMG1-S0 device in detail.

EZ-PD™ PMG1-S0 MCU is the first member of the EZ-PD™ PMG1 MCU Family. It has a 32-bit Arm® Cortex®-M0 processor, 64-KB flash, a complete Type-C USB PD transceiver with all termination resistors R_p, R_d, $R_{d\text{-}db}$ and can be used in dual-role power (D) applications. It is available in 24-pin QFN package.

This document describes each function block of the EZ-PD™ PMG1-S0 MCU device in detail. This information will help designers to create system-level designs.

1.1 Top-level architecture

Figure 1-2 shows the major components of the EZ-PD™ PMG1-S0 MCU architecture.

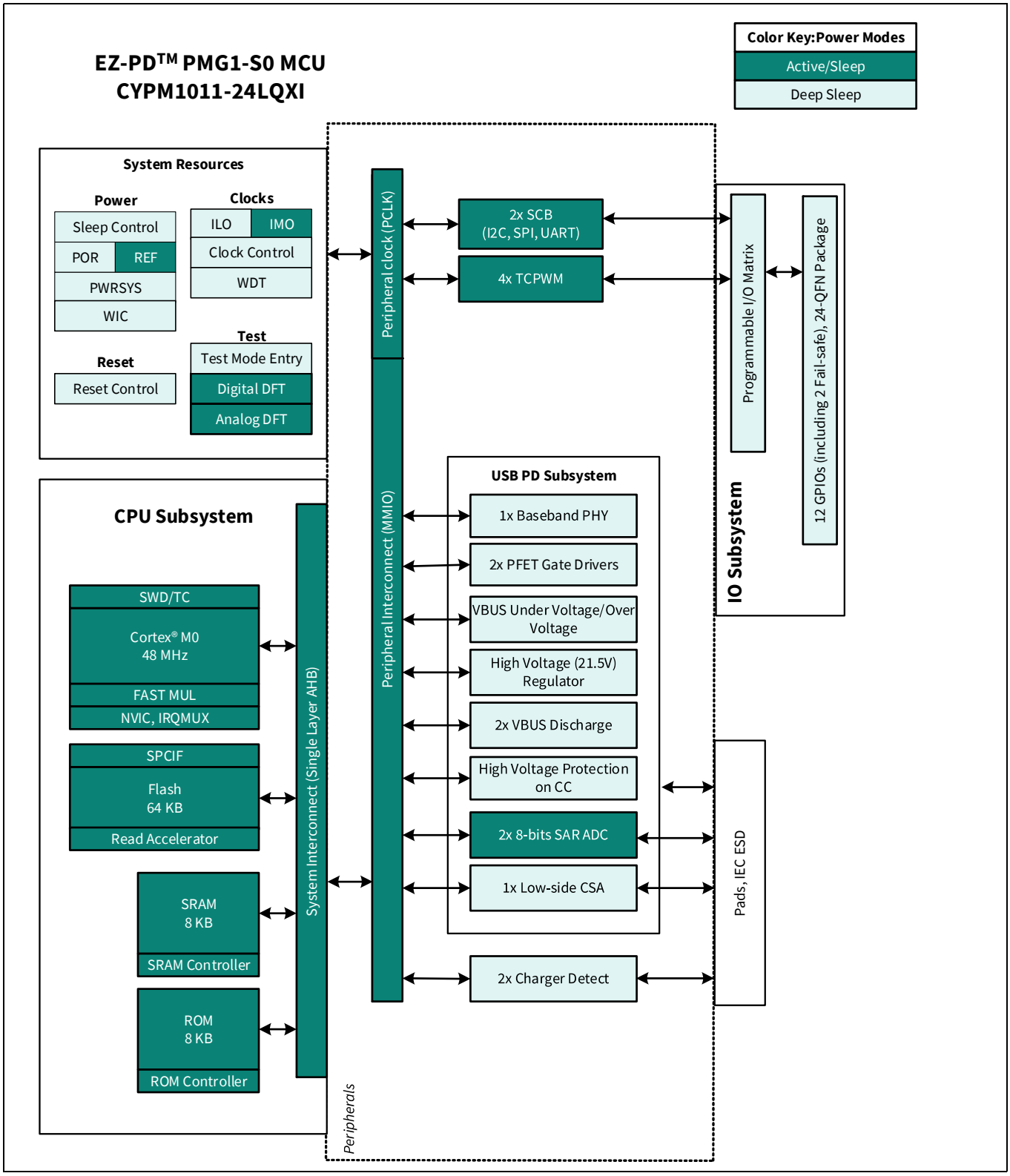


Figure 1-2. EZ-PD™ PMG1-S0 MCU functional block diagram

Applications

- Smart speakers, portable electronics, power banks
- Battery powered applications
- Cordless power tools
- Home appliances such as vacuum cleaners
- Electric bikes, robots, and drones

1.2 Features

- **32-bit MCU subsystem**
- **48-MHz Arm® Cortex®-M0 CPU**
- **Memory**
  - 64-KB flash
  - 8-KB SRAM
  - 8-KB SROM
- **Type-C/PD blocks**
  - USB-IF certified (TID: 7915)
  - Integrated USB power-delivery (USB PD) 3.2 support
  - Termination resistors R_p, R_d and $R_{d\text{-}db}$
  - Supports one USB-C port and one USB-A port
- **Legacy charging (source and sink)**
- **System-level fault protection**
  - VBUS to CC short protection
  - Low-side current sense amplifier (CSA) for overcurrent protection (OCP) and short-circuit protection (SCP)
- **Liquid detection and corrosion mitigation**
  - Supports moisture/liquid detection on Type-C connector
  - Integrated liquid detection blocks
  - Implements Corrosion Mitigation mode
- **Clocks and oscillators**
  - Integrated oscillator eliminating the need for external clock
- **Power**
  - VDDD (2.7 V–5.5 V)
  - VBUS (4.0 V–21.5 V)
- **System-Level ESD protection**
  - On CC, VBUS_MON, USBDP, USBDM, P2.2, and P2.3 pins
  - ± 8-kV contact discharge and ±15-kV air gap discharge based on IEC61000-4-2 level 4C
- **Packages**
  - 24-pin QFN
  - Supports extended industrial temperature range (–40°C to +105°C)
- **Software tool**
  - ModusToolbox™

2 Getting started

2.1 EZ-PD™ PMG1 MCU resources

This chapter provides the complete list of EZ-PD™ PMG1 MCU resources that will help you get started with the device and design your applications with them. If you are new to EZ-PD™ PMG1 MCU, there is a wealth of data at **USB-C High Voltage Microcontrollers** to help you to select the right EZ-PD™ PMG1 MCU device quickly and effectively integrate it into your design.

The following is an abbreviated list of EZ-PD™ PMG1 MCU resources:

- **Overview**: **USB-C High Voltage Microcontrollers**
- **Datasheets** describe and provide electrical specifications for each device family
- **Application notes and Code examples** cover a broad range of topics, from basic to advanced level. Many of the application notes include code examples, which can be opened from ModusToolbox™
- **Reference manuals** provide detailed descriptions of the architecture and registers in each device family
- **Development Tools**
  - **ModusToolbox™ software** is a free integrated design environment (IDE). It enables you to design hardware and firmware systems concurrently with EZ-PD™ PMG1 MCU devices. In addition, ModusToolbox™ includes a device selection/configuration tool to select devices and configure them for ModusToolbox™ projects.
  - ModusToolbox™ is an Eclipse-based development environment on Windows, MacOS, and Linux platforms that includes the ModusToolbox™ IDE and the EZ-PD™ PMG1 SDK. The ModusToolbox™ IDE brings together several device resources, middleware, and firmware to build an application. Using ModusToolbox™, you can enable and configure device resources and middleware libraries, write C/C++/assembly source code, and program and debug the device.
  - EZ-PD™ PMG1 MCU prototyping kits offer an easy-to-use, inexpensive platform to build EZ-PD™ PMG1 MCU-based systems.
  - The EZ-PD™ PMG1 SDK is the software development kit for the **EZ-PD™ PMG1 MCU**. The SDK makes it easier to develop firmware for supported devices without the need to understand the intricacies of the device resources.
- **Additional resources**
  - Go to **EZ-PD™ PMG1 MCU** webpage for additional resources such as IBIS, BSDL models, CAD library files, programming specifications and application notes
- **Technical**
  - **Forum**: See if your question is already answered by fellow developers **EZ-PD™ PMG1 forums.**
  - For any technical support, see the **support** page or contact the local sales representatives

3 Document construction

The following sections in this document include these topics:

- **"CPU system"** on page 22
- **"Memory system"** on page 40
- **"System-wide resources"** on page 43
- **"Digital system"** on page 67
- **"Universal serial bus (USB) Power Delivery (PD)"** on page 132
- **"Program and debug"** on page 146

3.1 Major sections

For ease of use, information is organized into sections and chapters that are divided according to device functionality.

- Section – Presents the top-level architecture, how to get started, and conventions and overview information about any particular area that inform the reader about the construction and organization of the product.
- Chapter – Presents the chapters specific to an individual aspect of the section topic. These are the detailed implementation and use information for some aspect of the integrated circuit.
- Glossary – Defines the specialized terminology used in this reference manual. Glossary terms are presented in bold, italic font throughout.
- Registers reference manual – Supplies all device register details summarized in the reference manual. These are additional documents.

3.2 Documentation conventions

3.2.1 Register conventions

The register conventions are detailed in **[2]**.

3.2.2 Numeric naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah') and *hexadecimal* numbers may also be represented by a '0x' prefix, the *C* coding convention. Binary numbers have an appended lowercase 'b' (for example, 01010100b' or '01000011b'). Numbers not indicated by an 'h' or 'b' are *decimal*.

3.2.3 Units of measure

This table lists the units of measure used in this document.

Table 3-1. Units of measure

Acronyms	Description
A	amperes
°C	degree celsius
dB	decibels
fF	femtofarads
Hz	hertz
k	kilo, 1000
K	kilo, 2^{10}
KB	1024 bytes, or approximately one thousand bytes
Kbit	1024 bits
kHz	kilohertz
kΩ	kilohms
MHz	megahertz
MΩ	megaohms
µA	microamperes
µF	microfarads
µs	microseconds
µV	microvolts
µVrms	microvolts root-mean-square
mA	milliamperes
ms	milliseconds
mV	millivolts
nA	nanoamperes
ns	nanoseconds
nV	nanovolts
Ω	ohms
pF	picofarads
pp	peak-to-peak
ppm	parts per million
s	seconds
sps	samples per second
V	volts
W	watts

3.2.4 Acronyms

This table lists the acronyms used in this document

Table 3-2. Acronyms

Acronyms	Description
ABUS	analog output bus
AC	alternating current
ADC	analog-to-digital converter
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm® data transfer bus
AMUXBUS	analog multiplexer bus
API	application programming interface
BMC	Bi-Phase Mark Coding
BOD	brownout detection
BR	bit rate
BRA	bus request acknowledge
BRQ	bus request
CAN	controller area network
CC	Configuration Channel
CI	carry in
CMP	compare
CO	carry out
CPU	central processing unit
CRC	cyclic redundancy check
CT	continuous time
DAC	digital-to-analog converter
DC	direct current
DFP	Downstream Facing Port
DI	digital or data input
DMA	direct memory access
DMIPS	dhrystone million instructions per second
DNL	differential nonlinearity
DO	digital or data output
DRP	Dual Role Power
DSI	digital signal interface
DSM	Deep Sleep mode
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read only memory
EMCA	Electronically Marked Cable Assembly
EMIF	external memory interface
EOC	end of conversion

Table 3-2. Acronyms (continued)

Acronyms	Description
FB	feedback
FIFO	first in first out
FSR	full scale range
GPIO	general purpose I/O
HCI	host-controller interface
HFCLK	high-frequency clock
I^2C	inter-integrated circuit
IDE	integrated development environment
ILO	internal low-speed oscillator
IMO	internal main oscillator
INL	integral nonlinearity
I/O	input/output
IOR	I/O read
IOW	I/O write
IRES	initial power on reset
IRA	interrupt request acknowledge
IRQ	interrupt request
ISR	interrupt service routine
IVR	interrupt vector read
LRb	last received bit
LRB	last received byte
LSb	least significant bit
LSB	least significant byte
LUT	lookup table
MISO	master-in-slave-out
MMIO	memory mapped input/output
MOSI	master-out-slave-in
MSb	most significant bit
MSB	most significant byte
MSP	main stack pointer
OVP	overvoltage protection
PC	program counter
PCH	program counter high
PCL	program counter low
PD	power delivery
PFC	power factor correction
PGA	programmable gain amplifier
PM	power management

Document construction

Table 3-2. Acronyms (continued)

Acronyms	Description
PMA	EZ-PD™ PMG1-S0 MCU memory arbiter
POR	power-on reset
PPOR	precision power-on reset
PRS	pseudo random sequence
PSP	process stack pointer
PSRR	power supply rejection ratio
PSSDC	power system sleep duty cycle
PWM	pulse width modulator
RAM	random-access memory
RETI	return from interrupt
RF	radio frequency
ROM	read only memory
RW	read/write
SAR	successive approximation register
SC	switched capacitor
SCB	serial communication block
SIE	serial interface engine
SIO	special I/O
SE0	single-ended zero
SNR	signal-to-noise ratio
SOF	start of frame
SOI	start of instruction
SOP	Start of Packet
SP	stack pointer
SPD	sequential phase detector
SPI	serial peripheral interconnect
SPIM	serial peripheral interconnect master
SPIS	serial peripheral interconnect slave
SRAM	static random-access memory
SROM	supervisory read only memory
SSADC	single slope ADC
SSC	supervisory system call
SYSCLK	system clock
SWD	single wire debug
TC	terminal count
TD	transaction descriptors
UART	universal asynchronous receiver/transmitter
UFP	Upstream Facing Port

Table 3-2. Acronyms (continued)

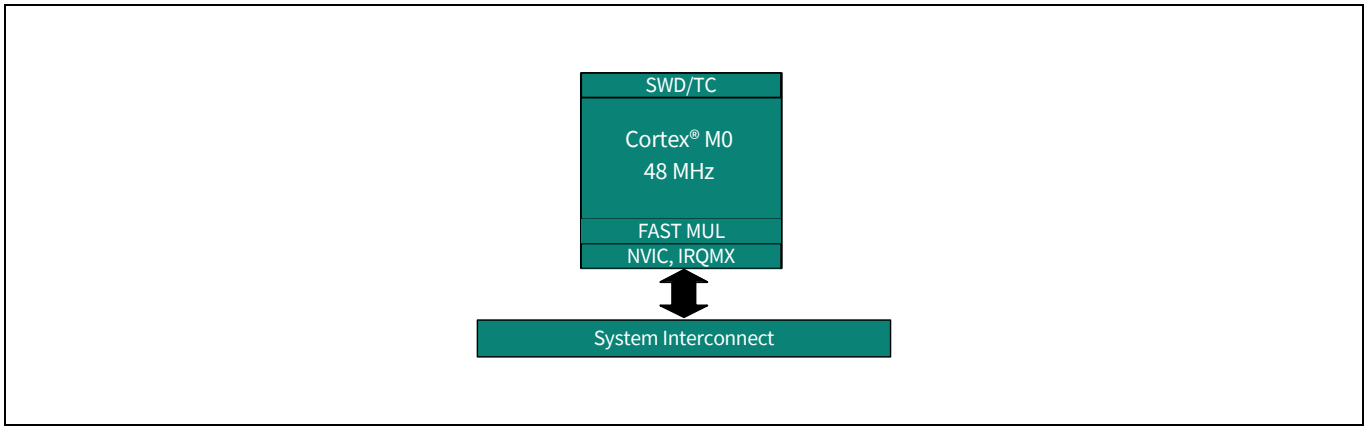
Acronyms	Description
USB	universal serial bus
USBIO	USB I/O
USB PD	USB Power Delivery
UVP	undervoltage protection
VU	vector unit
WCO	watch crystal oscillator
WDT	watchdog timer
WDR	watchdog reset
XRES	external reset

Section B: CPU system

This section encompasses the following chapters:

- **“Arm® Cortex®-M0 CPU”** on page 23
- **“Interrupts”** on page 29

Top-level architecture



5 Arm® Cortex®-M0 CPU

EZ-PD™ PMG1-S0 MCU Arm® Cortex®-M0 core is a 32-bit CPU optimized for low-power operation. It has an efficient three-stage pipeline, a fixed 4-GB memory map, and supports the Armv6-M Thumb instruction set. The Arm® Cortex®-M0 also features a low-latency interrupt service routine (ISR) entry and exit.

The Arm® Cortex®-M0 processor includes a number of other components that are tightly linked to the CPU core. These include a nested vectored interrupt controller (NVIC), a SYSTICK timer, and a debug.

This section gives an overview of the Arm® Cortex®-M0 processor. For more details, see the Arm® Cortex®-M0 user guide or reference manual, both available at **w ww.arm.com**.

5.1 Features

EZ-PD™ PMG1-S0 MCU Arm® Cortex®-M0 has the following features:

- Easy-to-use, program and debug, ensuring easier migration from 8-bit and 16-bit processors
- Operates at up to 0.9 DMIPS/MHz; this helps to increase execution speed or reduce power
- Supports Thumb instruction set for improved code density, ensuring efficient use of memory
- NVIC unit to support interrupts and exceptions for rapid and deterministic interrupt response
- Extensive debug support including:
  - Serial wire debug (SWD) port
  - Breakpoints
  - Watchpoints

5.2 Block diagram

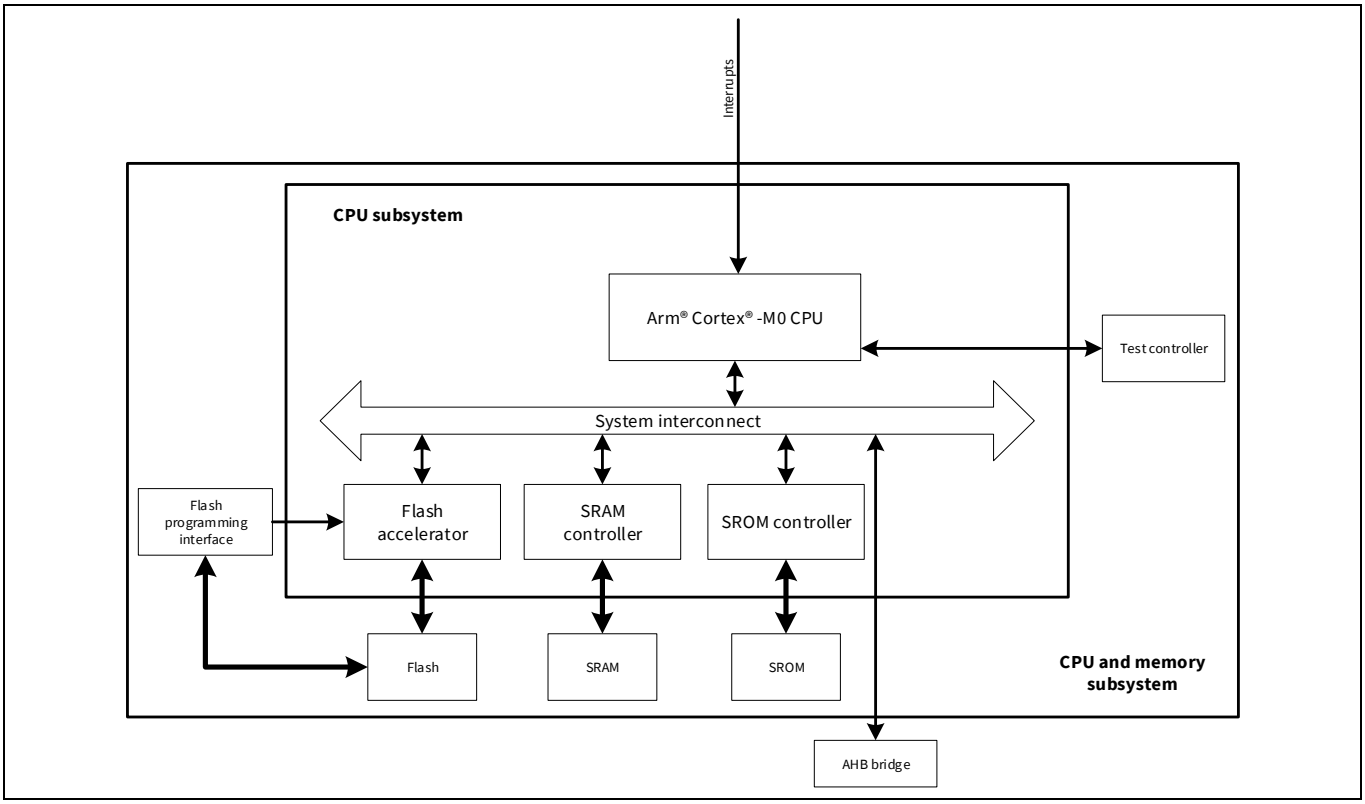


Figure 5-1. EZ-PD™ PMG1-S0 MCU CPU subsystem block diagram

5.3 How it works

The Arm® Cortex®-M0 is a 32-bit processor with a 32-bit data path, 32-bit registers, and a 32-bit memory interface. It supports most 16-bit instructions in the Thumb instruction set and some 32-bit instructions in the Thumb-2 instruction set.

5.3.1 Registers

The Arm® Cortex®-M0 has sixteen 32-bit registers, as **Table 5-1** shows:

- **R0 to R12 – General-purpose registers**: R0 to R7 can be accessed by all instructions; the other registers can be accessed by a subset of the instructions.
- **R13 – Stack pointer (SP)**: There are two stack pointers, with only one available at a time. In thread mode, the CONTROL register indicates the stack pointer to use, Main Stack Pointer (MSP) or Process Stack Pointer (PSP).
- **R14 – Link register**: Stores the return program counter during function calls.
- **R15 – Program counter**: This register can be written to control program flow.

Table 5-1. Arm® Cortex®-M0 registers

Name	Type[a)]	Reset value	Description
R0-R12	RW	Unknown	R0-R12 are 32-bit general-purpose registers for data operations.
MSP	RW	[0x00000000]	The stack pointer (SP) is register R13. In thread mode, bit[1] of the CONTROL register indicates the stack pointer to use: • 0 = Main stack pointer (MSP). This is the reset value • 1 = Process stack pointer (PSP) On reset, the processor loads the MSP with the value from address 0x00000000.
PSP			
LR	RW	Unknown	The link register (LR) is register R14. It stores the return information for subroutines, function calls, and exceptions.
PC	RW	[0x00000004]	The program counter (PC) is register R15. It contains the current program address. On reset, the processor loads the PC with the value from address 0x00000004. Bit[0] of the value is loaded into the EPSR T-bit at reset and must be '1'.
PSR	RW	Unknown[b)]	The program status register (PSR) combines: • Application Program Status Register (APSR) • Execution Program Status Register (EPSR) • Interrupt Program Status Register (IPSR)
APSR	RW	Unknown	The APSR contains the current state of the condition flags from previous instruction executions.
EPSR	RO	Unknown[b]	The EPSR contains the Thumb state bit.
IPSR	RO	0	The IPSR contains the exception number of the current ISR.
PRIMASK	RW	0	The PRIMASK register prevents activation of all exceptions with configurable priority.
CONTROL	RW	0	The CONTROL register controls the stack used when the processor is in Thread mode.

a) Describes access type during program execution in thread mode and handler mode. Debug access can differ.
b) Bit[24] is the T-bit and is loaded from bit[0] of the reset vector.

Table 5-2 shows how the PSR bits are assigned.

Table 5-2. Arm® Cortex®-M0 PSR bit assignments

Bit	PSR register	Name	Usage
31	APSR	N	Negative flag
30	APSR	Z	Zero flag
29	APSR	C	Carry or borrow flag
28	APSE	V	Overflow flag
27–25	–	–	Reserved
24	EPSR	T	Thumb state bit. Must always be '1'. Attempting to execute instructions when the T bit is 0 results in a HardFault exception.
23–6	–	–	Reserved
5–0	IPSR	N/A	Exception number of current ISR: 0 = thread mode 1 = reserved 2 = Non maskable interrupt (NMI) 3 = HardFault 4 – 10 = reserved 11 = SVCall 12, 13 = reserved 14 = PendSV 15 = SysTick 16 = IRQ0 … 47 = IRQ31

Use the MSR or CPS instruction to set or clear bit 0 of the PRIMASK register. If the bit is 0, exceptions are enabled. If the bit is 1, all exceptions with configurable priority, that is, all exceptions except HardFault, NMI, and Reset are disabled. See **"Interrupts"** on page 29 for a list of exceptions.

5.3.2 Operating modes

The Arm® Cortex®-M0 processor supports two operating modes:

- Thread Mode – used by all normal applications. In the thread mode, the MSP or PSP can be used. The CONTROL register bit 1 determines which stack pointer is used:
  - 0 = MSP is the current stack pointer
  - 1 = PSP is the current stack pointer
- Handler Mode – used to execute exception handlers. The MSP is always used.

In thread mode, use the MSR instruction to set the stack pointer bit in the CONTROL register. When changing the stack pointer, use an ISB instruction immediately after the MSR instruction. This ensures that instructions after the ISB execute using the new stack pointer.

In handler mode, explicit writes to the CONTROL register are ignored, because the MSP is always used. The exception entry and return mechanisms automatically update the CONTROL register.

5.3.3 Instruction set

The Arm® Cortex®-M0 implements a version of the Thumb instruction set. For details, see the Arm® Cortex®-M0 Generic User Guide.

An instruction operand can be an Arm® register, a constant, or another instruction-specific parameter. Instructions act on the operands and often store the result in a destination register. Many instructions are unable to use, or have restrictions on using, the PC or SP for the operands or destination register.

Table 5-3. Thumb instruction set

Mnemonic	Brief description
ADCS	Add with Carry
ADD{S}	Add
ADR	PC-relative Address to Register
ANDS	bitwise AND
ASRS	arithmetic shift right
B{cc}	Branch {conditionally}
BICS	bit Clear
BKPT	breakpoint
BL	branch with link
BLX	branch indirect with link
BX	branch indirect
CMN	compare negative
CMP	compare
CPSID	change processor state, disable interrupts
CPSIE	change processor state, enable interrupts
DMB	data memory barrier
DSB	data synchronization barrier
EORS	exclusive OR
ISB	instruction synchronization barrier
LDM	Load Multiple Registers, increment after
LDR	Load Register from PC-relative address
LDRB	Load Register with word
LDRH	Load Register with half-word
LDRSB	Load Register with signed byte
LDRSH	Load Register with signed half-word
LSLS	logical shift left
LSRS	logical shift right
MOV{S}	move
MRS	move to general register from special register
MSR	move to special register from general register
MULS	multiply, 32-bit result
MVNS	bitwise NOT
NOP	no operation
ORRS	logical OR

Table 5-3. Thumb instruction set (continued)

Mnemonic	Brief description
POP	Pop registers from stack
PUSH	Push registers onto stack
REV	byte-reverse word
REV16	byte-reverse packed half-words
REVSH	byte-reverse signed half-word
RORS	rotate right
RSBS	reverse subtract
SBCS	subtract with carry
SEV	send event
STM	Store Multiple registers, increment after
STR	Store Register as word
STRB	Store Register as byte
STRH	Store Register as half-word
SUB{S}	subtract
SVC	Supervisor Call
SXTB	sign extend byte
SXTH	sign extend half-word
TST	logical AND based test
UXTB	zero extend a byte
UXTH	zero extend a half-word
WFE	wait for event
WFI	wait for interrupt

5.3.3.1 Address alignment

An aligned access is an operation where a word-aligned address is used for a word or multiple word access, or where a half word-aligned address is used for a half word access. Byte accesses are always aligned.

No support is provided for unaligned accesses on the Arm® Cortex®-M0 processor. Any attempt to perform an unaligned memory access operation results in a HardFault exception.

5.3.3.2 Memory endianness

The EZ-PD™ PMG1-S0 MCU, Arm® Cortex®-M0 uses little-endian format, where the least-significant byte of a word is stored at the lowest address and the most significant byte is stored at the highest address.

5.3.4 Systick timer

The Systick timer is integrated with the NVIC and generates the SYSTICK interrupt. This interrupt can be used for task management in a real-time system. The timer has a reload register with 24 bits available to use as a countdown value. The Systick timer uses the Arm® Cortex®-M0 internal clock as a source and can work in Sleep mode.

5.3.5 Debug

EZ-PD™ PMG1-S0 MCU Arm® Cortex®-M0 contains a debug interface based on SWD; it features four breakpoint (address) comparators and two watchpoint (data) comparators.

6 Interrupts

The Arm® Cortex®-M0 (CM0) CPU in EZ-PD™ PMG1-S0 MCU supports interrupts and exceptions. Interrupts refer to those events generated by peripherals external to the CPU such as timers, serial communication block, and port pin signals. Exceptions refer to those events that are generated by the CPU such as memory access faults and internal system timer events. Both interrupts and exceptions result in the current program flow being stopped and the exception handler or interrupt service routine (ISR) being executed by the CPU. The EZ-PD™ PMG1-S0 MCU provides a unified exception vector table for both interrupt handlers/ISR and exception handlers.

6.1 Features

EZ-PD™ PMG1-S0 MCU supports the following interrupt features:

- Supports 32 interrupts
- Nested vectored interrupt controller (NVIC) integrated with CPU core, yielding low interrupt latency
- Vector table may be placed in either flash or SRAM
- Configurable priority levels from 0 to 3 for each interrupt
- Level-triggered and pulse-triggered interrupt signals

6.2 How it works

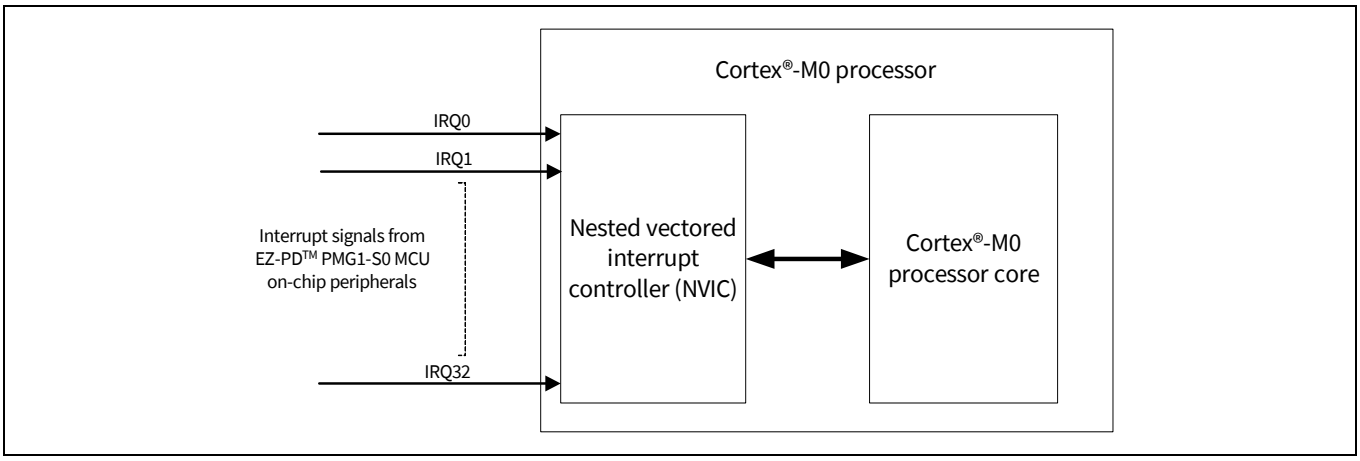


Figure 6-1. Interrupts block diagram

Figure 6-1 shows the interaction between interrupt signals and the Arm® Cortex®-M0 CPU. The EZ-PD™ PMG1-S0 MCU has 32 interrupts; these interrupt signals are processed by the NVIC. The NVIC takes care of enabling/disabling individual interrupts, priority resolution, and communication with the CPU core. The exceptions are not shown in **Figure 6-1** because they are part of CM0 core generated events, unlike interrupts, which are generated by peripherals external to the CPU.

6.3 Interrupts and exceptions - operation

6.3.1 Interrupt/Exception handling in EZ-PD™ PMG1-S0 MCU

The sequence of events that occur when an interrupt or exception event is triggered is:

1. Assuming that all the interrupt signals are initially low (idle or inactive state) and the processor is executing the main code, a rising edge on any one of the interrupt lines is registered by the NVIC. The interrupt line is now in a pending state waiting to be serviced by the CPU
2. On detecting the interrupt request signal from the NVIC, the CPU stores its current context by pushing the contents of the CPU registers onto the stack
3. The CPU also receives the unique number of the triggered interrupt from the NVIC. All interrupts and exceptions in EZ-PD™ PMG1-S0 MCU have a unique number (to index into a vector table). By using this unique number, the CPU fetches the address of the specific (exception or interrupt handler) from the vector table
4. The CPU then branches to this address and executes the specific handler
5. Upon completion of the specific handler, the CPU registers are restored to their original state using stack pop operations; the CPU resumes the main code execution

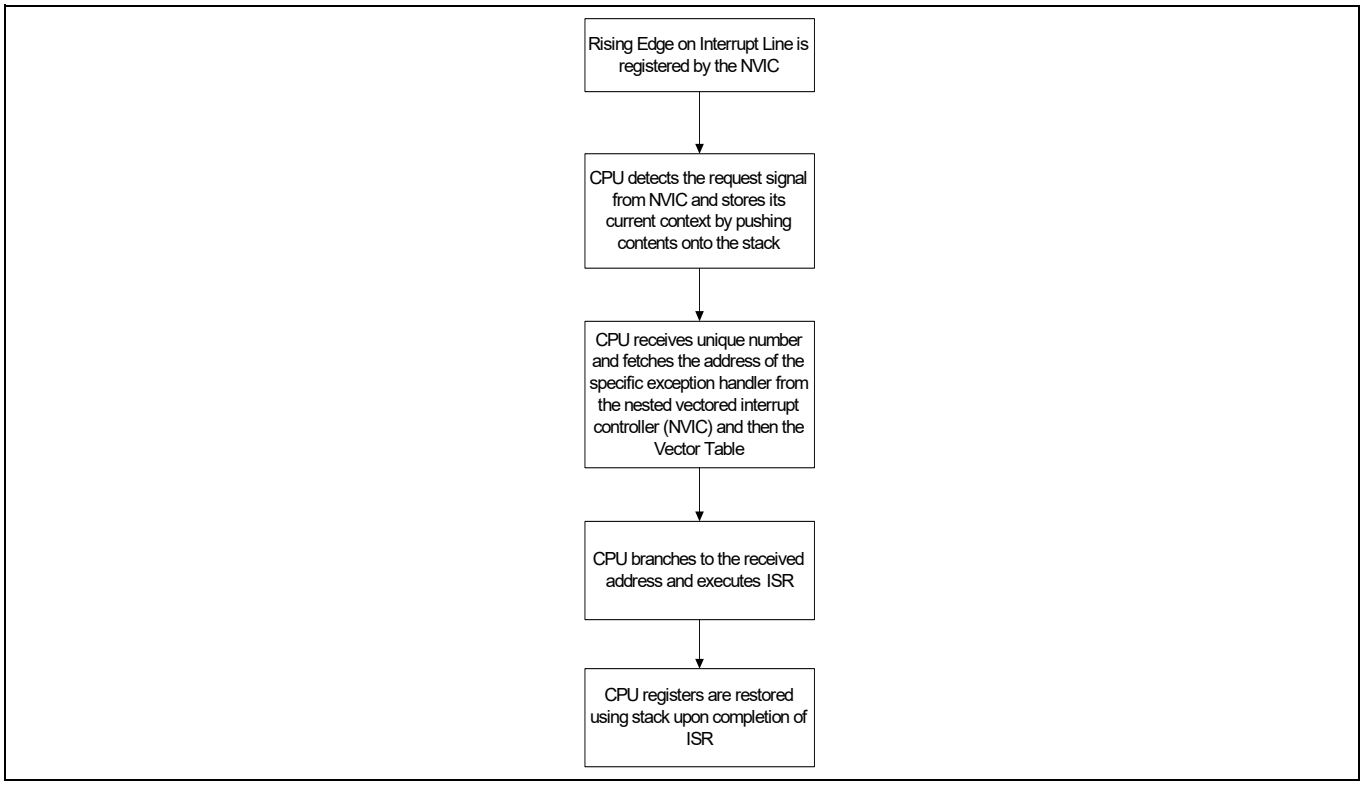


Figure 6-2. Interrupt handling when triggered

When the NVIC receives an interrupt request while another interrupt is being serviced or receives multiple interrupt requests at the same time, it evaluates the priority of all these interrupts, sending the exception number of the highest priority interrupt to the CPU. Thus, a higher priority interrupt can block the execution of a lower priority ISR at any time.

Exceptions are handled in the same way that interrupts are handled. Each exception event has a unique number, which is used by the CPU to execute the appropriate exception handler.

6.3.2 Level and pulse interrupts

The EZ-PD™ PMG1-S0 MCU NVIC supports both level and pulse signals on the interrupt lines (IRQ0 to IRQ31). The classification of an interrupt as level or pulse is based on the interrupt source.

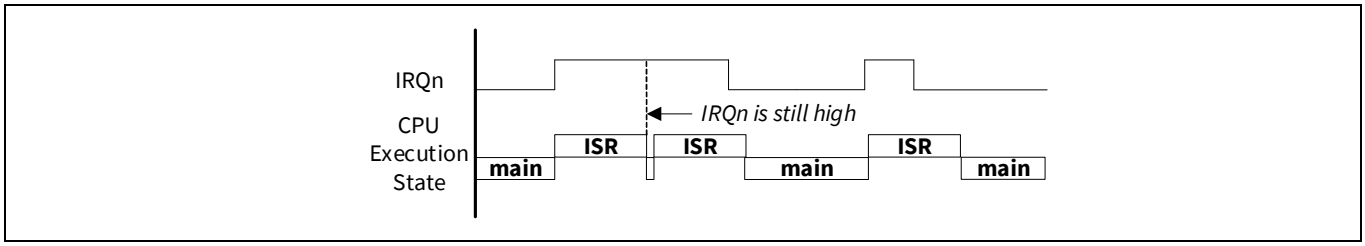


Figure 6-3. Level interrupts

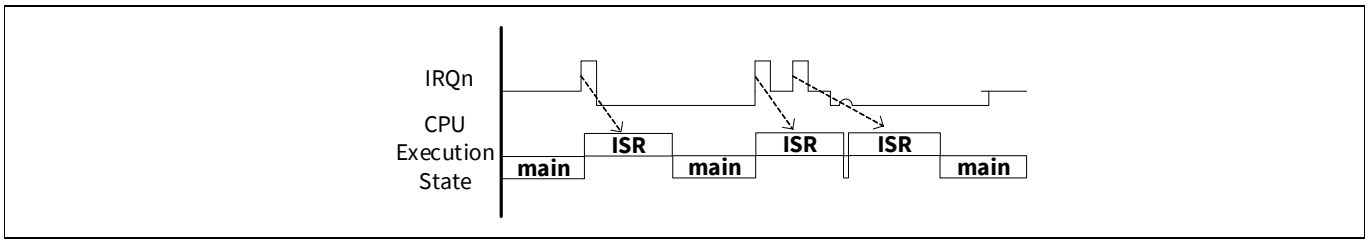


Figure 6-4. Pulse interrupts

Figure 6-3 and **Figure 6-4** show the working of level and pulse interrupts, respectively. Assuming the interrupt signal is initially inactive (logic LOW), the following sequence of events explains the handling of level and pulse interrupts:

1. On a rising edge event of the interrupt signal, the NVIC registers the interrupt request. The interrupt is now in the pending state, which means the interrupt requests have not yet been serviced by the CPU
2. The NVIC then sends the unique number along with the interrupt request signal to the CPU. When the CPU starts executing the ISR, the pending state of the interrupt is cleared
3. When the ISR is being executed by the CPU, one or more rising edges of the interrupt signal are logged as a single pending request. The pending interrupt is serviced again after the current ISR execution is complete (see **Figure 6-4** for pulse interrupts)
4. If the interrupt signal is still high after completing the ISR, it will be pending and the ISR is executed again. **Figure 6-3** illustrates this for level triggered interrupts, where the ISR is executed as long as the interrupt signal is HIGH

6.3.3 Exception vector table

The exception vector table (**Table 6-1**), stores the entry point addresses for all exception handlers in the EZ-PD™ PMG1-S0 MCU. The CPU fetches the appropriate address based on the exception number.

Table 6-1. EZ-PD™ PMG1-S0 MCU exception vector table

Exception number	Exception	Exception priority	Vector address
–	Initial Stack Pointer Value	Not applicable (NA)	Base_Address - Can be 0x00000000 (start of flash memory) or 0x20000000 (start of SRAM)[a]
1	Reset	–3, the highest priority	Base_Address + 0x04
2	Non Maskable Interrupt (NMI)	–2	Base_Address + 0x08
3	HardFault	–1	Base_Address + 0x0C
4–10	Reserved	NA	Base_Address + 0x10 to Base_Address + 0x28
11	Supervisory Call (SVCall)	Configurable (0–3)	Base_Address + 0x2C
12–13	Reserved	NA	Base_Address + 0x30 to Base_Address + 0x34
14	PendSupervisory (PendSV)	Configurable (0–3)	Base_Address + 0x38
15	System Timer (SysTick)	Configurable (0–3)	Base_Address + 0x3C
16	External Interrupt (IRQ0)	Configurable (0–3)	Base_Address + 0x40
…	…	Configurable (0–3)	…
47	External Interrupt (IRQ31)	Configurable (0–3)	Base_Address + 0xBC

a) Note that the reset exception address in SRAM vector table will never be used because the device comes out of reset with the flash vector table selected.

In **Table 6-1**, the first word (4 bytes) is not marked as exception number zero. This is because the first word in the exception table is used to initialize the main stack pointer (MSP) value on device reset; it is not considered as an exception. In EZ-PD™ PMG1-S0 MCU, the vector table can be configured to be located either in flash memory (base address of 0x00000000) or SRAM (base address of 0x20000000). This configuration is done by writing to the VECT_IN_RAM bit field (bit 0) in the CPUSS_CONFIG register. When the VECT_IN_RAM bit field is '1', CPU fetches exception handler addresses from the SRAM vector table location. When this bit field is '0' (reset state), the vector table in flash memory is used for exception address fetches. You must set the VECT_IN_RAM bit field as part of the device boot code to configure the vector table to be in SRAM. The advantage of moving the vector table to SRAM is that the exception handler addresses can be dynamically changed by modifying the SRAM vector table contents. However, the nonvolatile flash memory vector table must be modified by a flash memory write.

The exception sources (exception numbers 1 to 15) are explained in **"Exception sources"** on page 33. The exceptions marked as Reserved in **Table 6-1** are not used in EZ-PD™ PMG1-S0 MCU, though they have addresses reserved for them in the vector table. The interrupt sources (exception numbers 16 to 47) are explained in **"Interrupt sources"** on page 34.

6.4 Exception sources

This section explains the different exception sources listed in **Table 6-1** (exception numbers 1 to 15).

6.4.1 Reset exception

The device reset is treated as an exception in EZ-PD™ PMG1-S0 MCU. It is always enabled with a fixed priority of –3, the highest priority exception. A device reset can occur due to multiple reasons, such as power-on-reset (POR) or watchdog reset. When the device is reset, the initial boot code for configuring the device is executed out of supervisory read-only memory (SROM). The boot code and other data in SROM memory are programmed by Cypress, and are not read/write accessible to external users. After completing the SROM boot sequence, the CPU code execution jumps to flash memory. Flash memory address 0x00000004 (Exception#1 in **Table 6-1**) stores the location of the startup code in flash memory. The CPU starts executing code out of this address. Note that the reset exception address in SRAM vector table will never be used because the device comes out of reset with the flash vector table selected. The register configuration to select the SRAM vector table can be done only as part of the startup code in flash after the reset is de-asserted.

6.4.2 Non-Maskable Interrupt (NMI) exception

The Non-maskable interrupt (NMI) is the highest priority exception other than reset. It is always enabled with a fixed priority of –2. There are two ways to trigger an NMI exception in EZ-PD™ PMG1-S0 MCU:

- **NMI exception by setting NMIPENDSET bit (user NMI exception):** NMI exception can be triggered in software by setting the NMIPENDSET bit in the interrupt control state register (CM0_ICSR register). Setting this bit will execute the NMI handler pointed to by the active vector table (flash or SRAM vector table).
- **System Call NMI exception:** This exception is used for nonvolatile programming operations in EZ-PD™ PMG1-S0 MCU such as flash write operation and flash checksum operation. It is triggered by setting the SYSCALL_REQ bit in the CPUSS_SYSREQ register. An NMI exception triggered by SYSCALL_REQ bit always executes the NMI exception handler code that resides in SROM. Flash or SRAM exception vector table is not used for system call NMI exception. The NMI handler code in SROM is not read/write accessible because it contains nonvolatile programming routines that should not be modified by the user.

6.4.3 HardFault exception

The HardFault is an always-enabled exception that occurs because of an error during normal or exception processing. HardFault has a fixed priority of –1, meaning it has higher priority than any exception with configurable priority. HardFault exception is a catch-all exception for different types of fault conditions, which include executing an undefined instruction and accessing an invalid memory addresses. The Cortex®-M0 CPU does not provide fault status information to the HardFault exception handler, but it does permit the handler to perform an exception return and continue execution in cases where software has the ability to recover from the fault situation.

6.4.4 Supervisor Call (SVCall) exception

The Supervisor Call (SVCall) is an always-enabled exception caused when the CPU executes the SVC instruction as part of the application code. Application software uses the SVC instruction to make a call to an underlying operating system and provide a service. This is known as a supervisor call. The SVC instruction enables the application to issue a supervisor call that requires privileged access to the system. Note that the CM0 in EZ-PD™ PMG1-S0 MCU uses a privileged mode for the system call NMI exception, which is not related to the SVCall exception. (See the **“Chip operational modes”** on page 60 for details on privileged mode.) There is no other privileged mode support for SVCall at the architecture level in the EZ-PD™ PMG1-S0 MCU. The application developer must define the SVCall exception handler according to the end application requirements.

The priority of a SVCall exception can be configured to a value between 0 and 3 by writing to the two bit fields PRI_11[31:30] of the System Handler Priority Register 2 (SHPR2). When the SVC instruction is executed, the SVCall exception enters the pending state and waits to be serviced by the CPU. The SVCALLPENDED bit in the System Handler Control and State Register (SHCSR) can be used to check or modify the pending status of the SVCall exception.

6.4.5 PendSV exception

The PendSV is another supervisor call related exception similar to SVCall, normally being software-generated. PendSV is always enabled and its priority is configurable. The PendSV exception is triggered by setting the PENDSVSET bit in the Interrupt Control State Register, CM0_ICSR. On setting this bit, the PendSV exception enters the pending state, and waits to be serviced by the CPU. The pending state of a PendSV exception can be cleared by setting the PENDSVCLR bit in the Interrupt Control State Register, CM0_ICSR. The priority of a PendSV exception can be configured to a value between 0 and 3 by writing to the two bit fields PRI_14[23:22] of the System Handler Priority Register 3 (CM0_SHPR3). See the **Armv6-M architecture Reference Manual** for more details.

6.4.6 SysTick exception

The Cortex®-M0 CPU in EZ-PD™ PMG1-S0 MCU supports a system timer, referred to as SysTick, as part of its internal architecture. SysTick provides a simple, 24-bit decrementing counter for various time keeping puoses such as an RTOS tick timer, high-speed alarm timer, or simple counter. The SysTick timer can be configured to generate an interrupt when its count value reaches zero, which is referred to as SysTick Exception. The exception is enabled by setting the TICKINT bit in the SysTick Control and Status Register (CM0_SYST_CSR). The priority of a SysTick exception can be configured to a value between 0 and 3 by writing to the two bit fields PRI_15[31:30] of the System Handler Priority Register 3 (SHPR3). The SysTick exception can always be generated in software at any instant by writing a one to the PENDSTSETb bit in the Interrupt Control State Register, CM0_ICSR. Similarly, the pending state of the SysTick exception can be cleared by writing a one to the PENDSTCLR bit in the Interrupt Control State Register, CM0_ICSR.

6.5 Interrupt sources

The EZ-PD™ PMG1-S0 MCU supports fifteen interrupts from peripherals. The source of each interrupt is listed in **Table 6-2**. The EZ-PD™ PMG1-S0 MCU provides flexible sourcing options for each of the 22 interrupt lines. The interrupts include standard interrupts from on-chip peripherals such as TCPWM, serial communication block, and interrupts from ports. The interrupt generated is usually the logical OR of the different peripheral states. The peripheral status register should be read in the ISR to detect which condition generated the interrupt. These interrupts are usually level interrupts, which require the peripheral status register to be read in the ISR to clear the interrupt. If the status register is not read in the ISR, the interrupt will remain asserted and the ISR will be executed continuously.

Table 6-2. List of EZ-PD™ PMG1-S0 MCU interrupt sources

Interrupt no.	Interrupt source
NMI	
0	GPIO Interrupt - Port0
1	GPIO Interrupt - Port1
2	GPIO Interrupt - Port2
3	GPIO Interrupt - Port3
4	GPIO All ports
5	Ganged USBPD Interrupt

Table 6-2. List of EZ-PD™ PMG1-S0 MCU interrupt sources (continued)

Interrupt no.	Interrupt source
6	WDT or Temp (WDT only in Deep Sleep)
7	SCB[0]
8	SCB[1]
9	SPC
10	Synchronous USBPD Interrupts
11	TCPWM counter #0
12	TCPWM counter #1
13	TCPWM counter #2
14	TCPWM counter #3

See the **"I/O system"** on page 44 for more details on GPIO interrupts.

6.6 Exception priority

The Exception priority is useful for exception arbitration when there are multiple exceptions that need to be serviced by the CPU. EZ-PD™ PMG1-S0 MCU provides flexibility in choosing priority values for different exceptions. All exceptions except Reset, NMI, and HardFault can be assigned a configurable priority level. The Reset, NMI, and HardFault exceptions have a fixed priority of –3, –2, and –1 respectively. In EZ-PD™ PMG1-S0 MCU, lower priority numbers represent higher priorities. This means that the Reset, NMI, and HardFault exceptions have the highest priorities. The other exceptions can be assigned a configurable priority level between 0 and 3.

EZ-PD™ PMG1-S0 MCU supports nested exceptions in which a higher priority exception can obstruct (interrupt) the currently active exception handler. This pre-emption does not happen if the incoming exception priority is the same as active exception. The CPU resumes execution of the lower priority exception handler after servicing the higher priority exception. The Cortex®-M0 CPU in EZ-PD™ PMG1-S0 MCU allows nesting of up to four exceptions. When the CPU receives two or more exceptions requests of the same priority, the lowest exception number is serviced first.

The registers to configure the priority of exception numbers 1 to 15 are explained in **"Exception sources"** on page 33.

The priority of the 32 interrupts (IRQ0–IRQ31) can be configured by writing to the Interrupt Priority registers (CM0_IPR). This is a group of four 32-bit registers with each register storing the priority values of four interrupts, as given in **Table 6-3**. The other bit fields in the register are not used.

Table 6-3. Interrupt priority register bit definitions

Bits	Name	Description
7:6	PRI_N0	Priority of interrupt number N
15:14	PRI_N1	Priority of interrupt number N+1
23:22	PRI_N2	Priority of interrupt number N+2
31:30	PRI_N3	Priority of interrupt number N+3

6.7 Enabling/disabling interrupts

The NVIC provides registers to individually enable and disable the 32 interrupts in software. If an interrupt is not enabled, the NVIC will not process the interrupt requests on that interrupt line. The Interrupt Set-Enable Register (CM0_ISER) and the Interrupt Clear-Enable Register (CM0_ICER) are used to enable and disable the interrupts respectively. These registers are 32-bit wide and each bit corresponds to the same numbered interrupt. These registers can also be read in software to get the enable status of the interrupts. **Table 6-4** shows the register access properties for these two registers. Note that writing zero to these registers has no effect.

Table 6-4. Interrupt enable/disable registers

Register	Operation	Bit value	Comment
Interrupt Set Enable Register (CM0_ISER)	Write	1	To enable the interrupt
		0	No effect
	Read	1	Interrupt is enabled
		0	Interrupt is disabled
Interrupt Clear Enable Register (CM0_ICER)	Write	1	To disable the interrupt
		0	No effect
	Read	1	Interrupt is enabled
		0	Interrupt is disabled

The CM0_ISER and CM0_ICER registers are applicable only for the interrupts (IRQ0–IRQ31). These registers cannot be used to enable or disable the exception numbers 1 to 15. The 15 exceptions have their own support for enabling and disabling, as explained in **"Exception sources"** on page 33.

The PRIMASK register in Arm® Cortex®-M0 (CM0) CPU can be used as a global exception enable register to mask all the configurable priority exceptions irrespective of whether they are enabled. Configurable priority exceptions include all the exceptions except Reset, NMI, and HardFault listed in **Table 6-1**. They can be configured to a priority level between 0 and 3, 0 being the highest priority and 3 being the lowest priority. When the PM bit (bit 0) in PRIMASK register is set, none of the configurable priority exceptions can be serviced by the CPU, though they can be in the pending state waiting to be serviced by the CPU after the PM bit is cleared.

6.8 Exception states

Each exception can be in one of the following states.

Table 6-5. Exception states

Exception state	Meaning
Inactive	The exception is not active and not pending. Either the exception is disabled or the enabled exception has not been triggered.
Pending	The exception request was received by the CPU/NVIC and the exception is waiting to be serviced by the CPU.
Active	An exception that is being serviced by the CPU but whose exception handler execution is not yet complete. A high-priority exception can interrupt the execution of lower priority exception. In this case, both the exceptions are in the Active state.
Active and pending	The exception is being serviced by the processor and there is a pending request from the same source during its exception handler execution.

The Interrupt Control State Register (CM0_ICSR) contains status bits describing the various exceptions states.

- The VECTACTIVE bits ([8:0]) in the CM0_ICSR store the exception number for the current executing exception. This value is zero if the CPU is not executing any exception handler (CPU is in thread mode). Note that the value in VECTACTIVE bit fields is the same as the value in bits [8:0] of the Interrupt Control State Register (ICSR), which is also used to store the active exception number
- The VECTPENDING bits ([20:12]) in the CM0_ICSR store the exception number of the highest priority pending exception. This value is zero if there are no pending exceptions
- The ISENDING bit (bit 22) in the CM0_ICSR indicates if a NVIC generated interrupt (IRQ0 to IRQ31) is in a pending state

6.8.1 Pending exceptions

When a peripheral generates an interrupt request signal to the NVIC or an exception event occurs, the corresponding exception enters the pending state. When the CPU starts executing the corresponding exception handler routine, the exception is changed from the pending state to the active state.

The NVIC allows software pending of the 32 interrupt lines by providing separate register bits for setting and clearing the pending states of the interrupts. The Interrupt Set-Pending Register (CM0_ISPR) and the Interrupt Clear-Pending Register (CM0_ICPR) are used to set and clear the pending status of the interrupt lines. These registers are 32 bits wide, and each bit corresponds to the same numbered interrupt. **Table 6-6** shows the register access properties for these two registers. Note that writing zero to these registers has no effect.

Table 6-6. Interrupt set pending/clear pending registers

Register	Operation	Bit value	Comment
Interrupt Set-Pending Register (CM0_ISPR)	Write	1	To put an interrupt to pending state
		0	No effect
	Read	1	Interrupt is pending
		0	Interrupt is not pending
Interrupt Clear-Pending Register (CM0_ICPR)	Write	1	To clear a pending interrupt
		0	No effect
	Read	1	Interrupt is pending
		0	Interrupt is not pending

Setting the pending bit when the same bit is already set results in only one execution of the ISR. The pending bit can be updated regardless of whether the corresponding interrupt is enabled. If the interrupt is not enabled, the interrupt line will not move to the pending state until it is enabled by writing to the CM0_ISER register.

Note that the CM0_ISPR and CM0_ICPR registers are used only for the 32 peripheral interrupts (exception numbers 16-47). These registers cannot be used for pending the exception numbers 1 to 15. These 15 exceptions have their own support for pending, as explained in **"Exception sources"** on page 33.

6.9 Stack usage for exceptions

When the CPU executes the main code (in thread mode) and an exception request occurs, the CPU stores the state of its general-puose registers in the stack. It then starts executing the corresponding exception handler (in handler mode). The CPU pushes the contents of the eight 32-bit internal registers into the stack. These registers are the Program and Status Register (PSR), ReturnAddress, Link Register (LR or R14), R12, R3, R2, R1, and R0. Arm® Cortex®-M0 has two stack pointers - MSP and PSP. Only one of the stack pointers can be active at a time. When in thread mode, the Active Stack Pointer bit in the Control register is used to define the current active stack pointer. When in handler mode, the MSP is always used as the stack pointer. The stack pointer in Arm® Cortex®-M0 always grows downwards and points to the address that has the last pushed data.

When the CPU is in thread mode and an exception request comes, the CPU uses the stack pointer defined in the control register to store the general-purpose register contents. After the stack push operations, the CPU enters handler mode to execute the exception handler. When another higher priority exception occurs while executing the current exception, the MSP is used for stack push/pop operations, because the CPU is already in handler mode. See the **"Arm® Cortex®-M0 CPU"** on page 23 for more details.

The Arm® Cortex®-M0 uses two techniques, tail chaining and late arrival, to reduce latency in servicing exceptions. These techniques are not visible to the external user and are done as part of the internal processor architecture, see **Arm developer**.

6.10 Interrupts and low-power modes

EZ-PD™ PMG1-S0 MCU allows device wakeup from low-power modes when certain peripheral interrupt requests are generated. The wakeup interrupt controller (WIC) block generates a wakeup signal that causes the device to enter Active mode when one or more wakeup sources generate an interrupt signal. After entering Active mode, the ISR of the peripheral interrupt is executed.

The Wait For Interrupt (WFI) instruction, executed by the Cortex®-M0 CPU, triggers the transition into Sleep and Deep Sleep modes. The sequence of entering the different low-power modes is detailed in the **"Power supply and modes"** on page 58. The chip low-power modes have two categories of fixed-function interrupt sources:

- Fixed-function interrupt sources that are available only in the Active and Deep Sleep modes (watchdog timer interrupt, I^2C interrupts, USBPD and GPIO interrupts)
- Fixed-function interrupt sources that are available only in the Active mode (all other fixed-function interrupts)

6.11 Exception - initialization and configuration

This section covers the different steps involved in initializing and configuring exceptions in EZ-PD™ PMG1-S0 MCU:

1. **Configuring the Exception Vector Table Location:** The first step in using exceptions is to configure the vector table location as required - either in flash memory or SRAM. This configuration is done by writing either a '1' (SRAM vector table) or '0' (flash vector table) to the VECT_IN_RAM bit field (bit 0) in the CPUSS_CONFIG register. This register write is done as part of device initialization code. It is recommended that the vector table be available in SRAM if the application will need to change the vector addresses dynamically. If the table is located in flash, then a flash write operation is required to modify the vector table contents.
2. **Configuring Individual Exceptions:** The next step is to configure individual exceptions required in an application.
   a. Configure the exception or interrupt source; this includes setting up the interrupt generation conditions. The register configuration depends on the specific exception required.
   b. Define the exception handler function and write the address of the function to the exception vector table. **Table 6-1** gives the exception vector table format; the exception handler address should be written to the appropriate exception number entry in the table.
   c. Set up the exception priority, as explained in **"Exception priority"** on page 35.
   d. Enable the exception, as explained in **"Enabling/disabling interrupts"** on page 36.

6.12 Registers

Table 6-7. List of registers

Register name	Description
CM0_ISER	Interrupt Set-Enable Register
CM0_ICER	Interrupt Clear Enable Register
CM0_ISPR	Interrupt Set-Pending Register
CM0_ICPR	Interrupt Clear-Pending Register
CM0_IPR	Interrupt Priority Registers
CM0_ICSR	Interrupt Control State Register
CM0_AIRCR	Application Interrupt and Reset Control Register
CM0_SCR	System Control Register
CM0_CCR	Configuration and Control Register
CM0_SHPR2	System Handler Priority Register 2
CM0_SHPR3	System Handler Priority Register 3
CM0_SHCSR	System Handler Control and State Register
CM0_SYST_CSR	Systick Control and Status
CPUSS_CONFIG	CPU Subsystem Configuration
CPUSS_SYSREQ	System Request Register

6.13 Associated documents

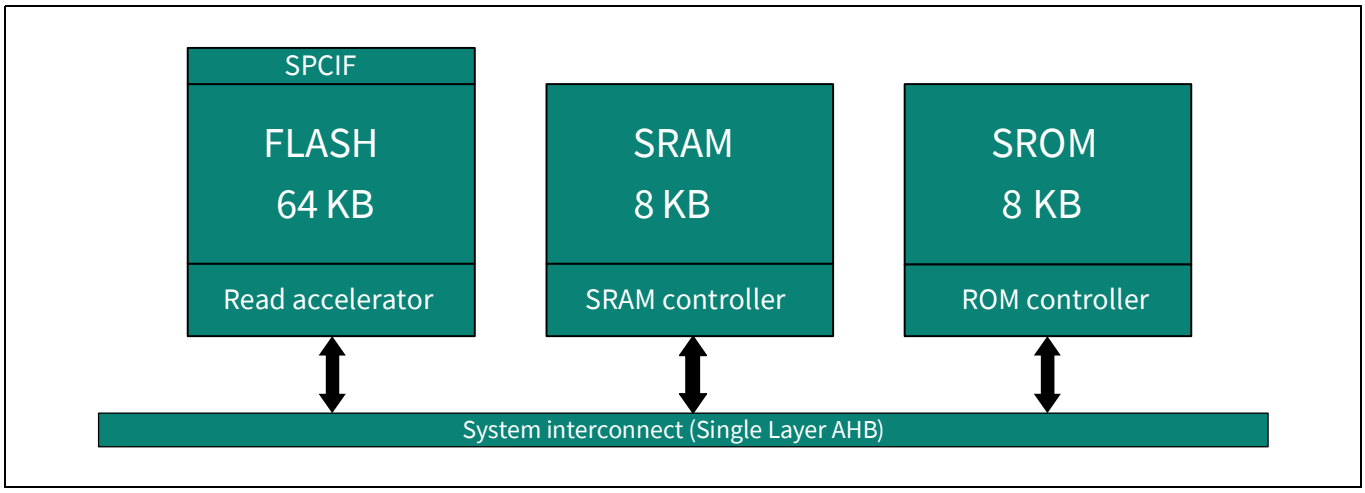
Armv6-M architecture Reference Manual - This document explains the Arm® Cortex®-M0 architecture, including the instruction set, NVIC architecture, and CPU register descriptions.

Section C: Memory system

This section presents the following chapter:

- **"Memory map"** on page 41

Top-level architecture



8 Memory map

All the EZ-PD™ PMG1-S0 MCU memory (flash, SRAM, and SROM) and all registers are accessible by the CPU and in most cases by the debug system. This chapter contains an overall map of the addresses of the memories and registers.

8.1 Features

The EZ-PD™ PMG1-S0 MCU memory system has the following features:

- 64K bytes flash, 8K bytes SRAM
- 8K byte SROM contains boot and configuration routines
- Arm® Cortex®-M0 32-bit linear address space, with regions for code, SRAM, peripherals, and CPU internal registers
- Flash is mapped to the Arm® Cortex®-M0 code region
- SRAM is mapped to the Arm® Cortex®-M0 SRAM region
- Peripheral registers are mapped to the Arm® Cortex®-M0 peripheral region
- The Arm® Cortex®-M0 private peripheral bus (PPB) region includes registers implemented in the CPU core. These include registers for NVIC, SysTick timer, and serial communication block (SCB). For more information, see the **"Arm® Cortex®-M0 CPU"** on page 23.

8.2 How it works

The EZ-PD™ PMG1-S0 MCU memory map is detailed in the following tables. For additional information, see **[2]**.

The Arm® Cortex®-M0 has a fixed address map allowing access to memory and peripherals using simple memory access instructions. The 32-bit (4 GB) address space is divided into the regions shown in **Table 8-1**. Note that code can be executed from the code and SRAM regions.

Table 8-1. Arm® Cortex®-M0 address map

Address range	Name	Use
0x00000000–0x1FFFFFFF	Code	Executable region for program code. You can also put data here. Includes the exception vector table, which starts at address 0.
0x20000000–0x3FFFFFFF	SRAM	Executable region for data. You can also put code her
0x40000000–0x5FFFFFFF	Peripheral	All peripheral registers. Code cannot be executed out of this region
0x60000000–0xDFFFFFFF	–	Not used
0xE0000000–0xE00FFFFF	PPB	Peripheral registers within the CPU core

Memory map

Table 8-2 shows the EZ-PD™ PMG1-S0 MCU address map.

Table 8-2. EZ-PD™ PMG1-S0 MCU address map

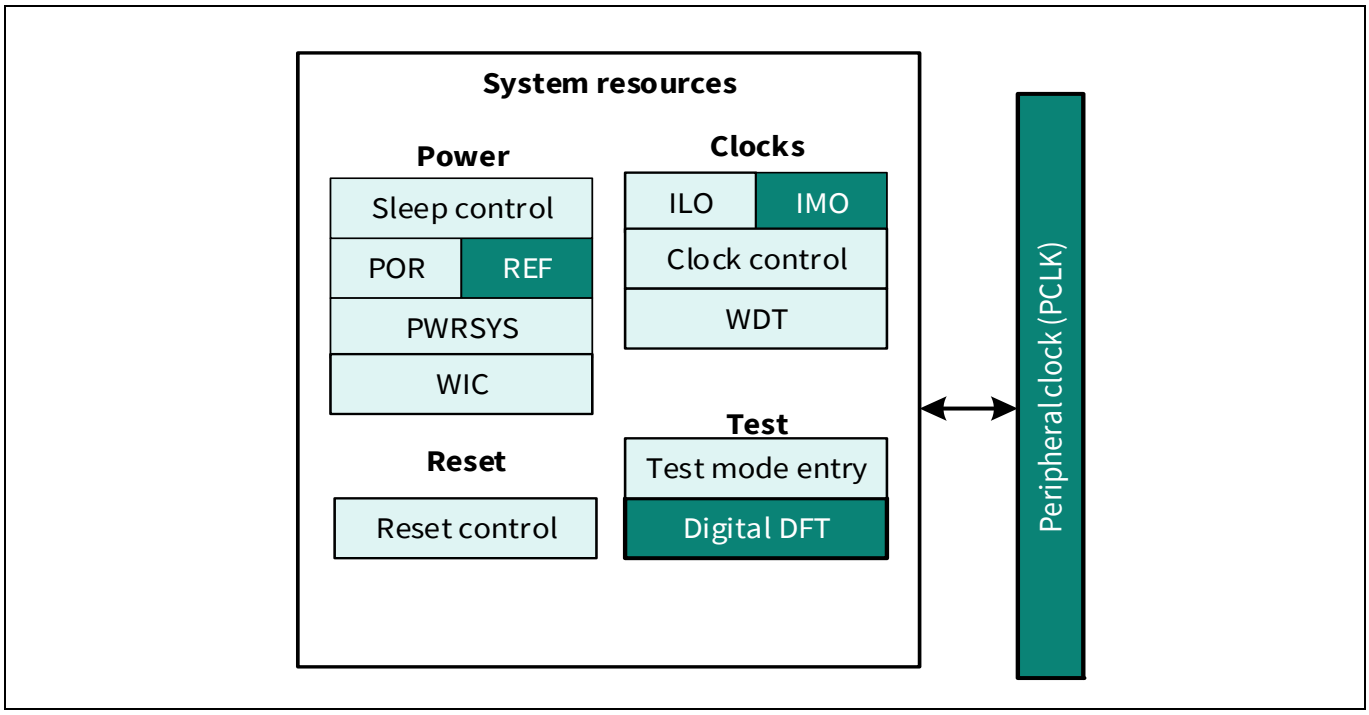
Address Range	Use
0x00000000–0x0000FFFF	64 KB flash
0x0FFFF000–0x0FFFF3FF	1 KB supervisory flash
0x20000000–0x20001FFF	8 KB SRAM
0x40020000–0x40023FFF	I/O port control (high-speed I/O matrix) Registers
0x40030000–0x4003FFFF	Power, clock, reset control Registers
0x40040000–0x40043FFF	I/O port Registers
0x40050000–0x4005FFFF	SCB 0 Registers
0x40060000-0x4006FFFF	SCB 1 Registers
0x40090000 - 0x4009FFFF	TCPWM Registers
0x400A0000 - 0x400AFFFF	USB Power Delivery Controller Registers
0x40100000–0x4011FFFF	CPU subsystem Registers
0xE0000000–0xE00FFFFF	Arm® Cortex®-M0 PPB Registers
0xF0000000–0xF0000FFF	CoreSight ROM

Section D: System-wide resources

This section encompasses the following chapters:

- **"I/O system"** on page 44
- **"Clocking system"** on page 53
- **"Power supply and modes"** on page 58
- **"Chip operational modes"** on page 60
- **"Watchdog timer (WDT)"** on page 61
- **"Reset system"** on page 64
- **"Device security"** on page 66

Top-level architecture



10 I/O system

This chapter explains the EZ-PD™ PMG1-S0 MCU I/O system, its features, architecture, operating modes, and interrupts. The general-purpose I/O (GPIOs) pins in EZ-PD™ PMG1-S0 MCU are grouped into ports; a port can have a maximum of eight GPIOs. The EZ-PD™ PMG1-S0 MCU die has a maximum of twelve GPIOs arranged in four ports.

10.1 Features

The EZ-PD™ PMG1-S0 MCU GPIOs have the following features:

- Analog and digital input and output capabilities
- 10 mA sink and 4 mA source current in digital mode
- Separate port read (PS) and write (DR) data registers to avoid read-modify-write errors
- Edge-triggered interrupts on rising edge, falling edge, or on both the edges, on pin basis
- Slew rate control
- Selectable CMOS and low-voltage LVTTL input buffer mode
- Two Fail-Safe GPIOs (I^2C pins from SCB0)

10.2 Block diagram

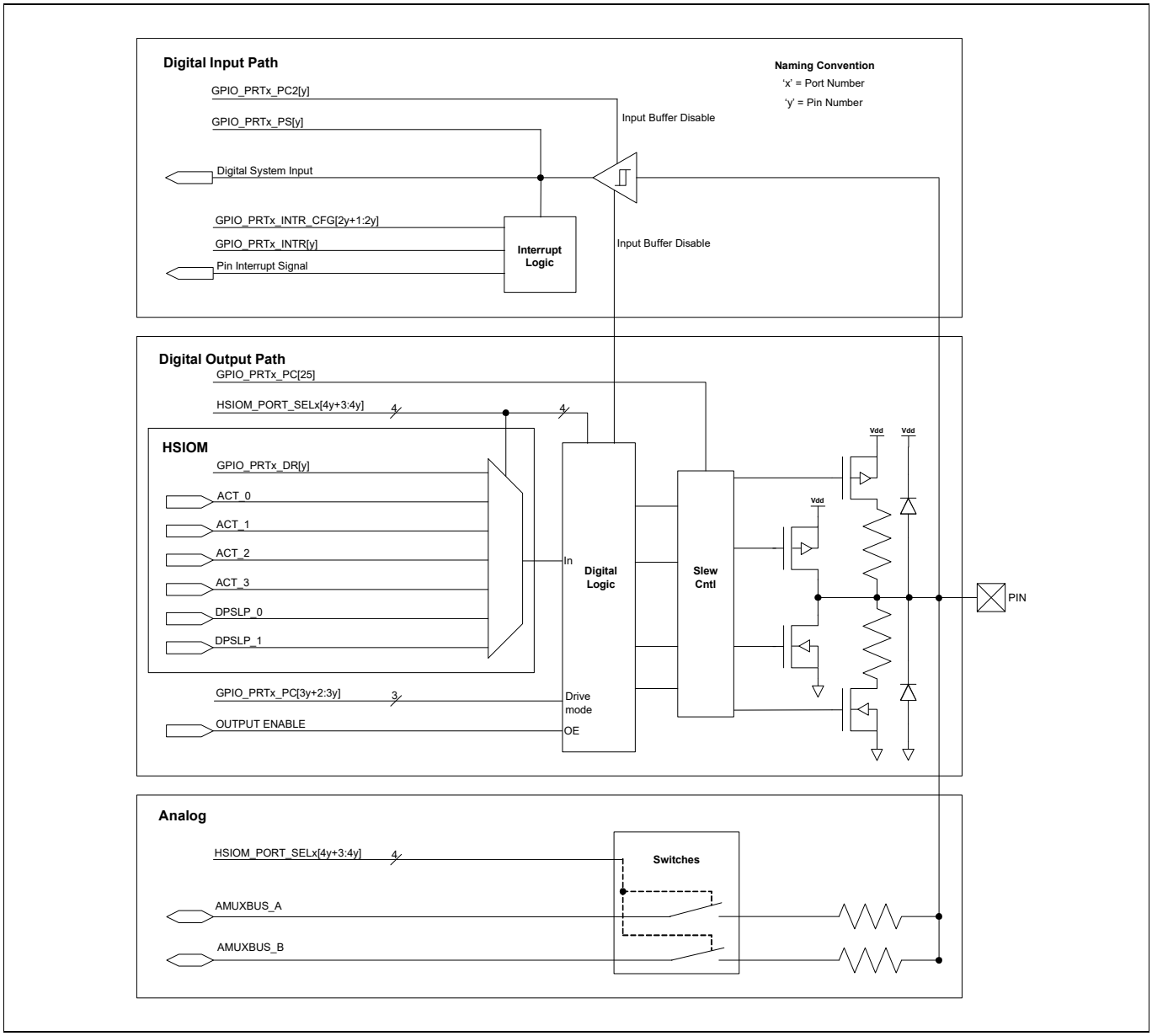


Figure 10-1. GPIO block diagram

Note: The GPIO features shown in this image may not be available on all the pins.

10.3 GPIO drive modes

Each I/O is individually configurable into one of the eight drive modes listed in **Table 10-1**.
Table 10-2 is a simplified pin diagram that shows the pin view based on each of the eight drive modes.

Two port configuration registers are used to configure GPIOs in EZ-PD™ PMG1-S0 MCU: Port Configuration Register (GPIO_PRTx_PC) and Port Secondary Configuration Register (GPIO_PRTx_PC2). All the EZ-PD™ PMG1-S0 MCU devices have ports with dedicated GPIO_PRTx_PC and GPIO_PRTx_PC2 registers.

GPIO_PRTx_PC is used to configure the following properties of a port:

- Output drive mode of each pin (three bits select a particular drive mode for a pin)
- Slew rate of the whole port (see **"Slew rate control"** on page 48)
- Input threshold selection of the whole port (see **"CMOS LVTTL level control"** on page 48)

GPIO_PRTx_PC2 is used to enable/disable the input buffer of each pin on the port, irrespective of the drive mode configured in GPIO_PRTx_PC. When analog signals are present on the pin, input buffer should be disabled by setting the bit to '1'.

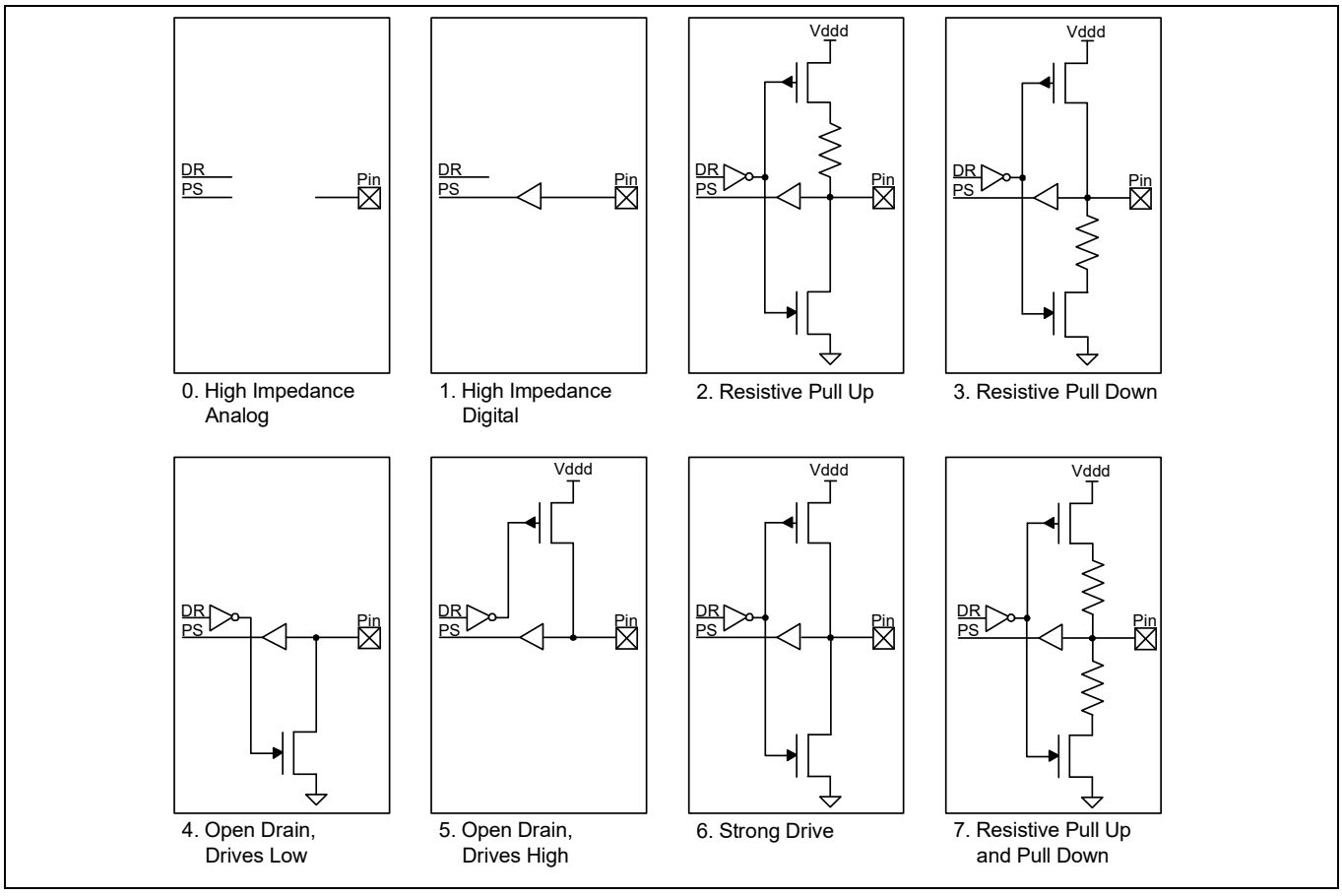


Figure 10-2. I/O drive mode block diagram

Table 10-1. Drive mode settings

GPIO_PRTx_PC ('x' denotes port number and 'y' denotes pin number)				
Bits	**Drive mode**	**Value**	**Data = 1**	**Data = 0**
3y+2: 3y	SEL'y'	Selects Drive Mode for Pin 'y' ($0 \le y \le 7$)		
	High-Z analog	0	High-Z	High-Z
	High-Z digital	1	High-Z	High-Z
	Resistive pull up	2	Weak 1	Strong 0
	Resistive pull down	3	Strong 1	Weak 0
	Open drain, drives LOW	4	High-Z	Strong 0
	Open drain, drives HIGH	5	Strong 1	High-Z
	Strong drive	6	Strong 1	Strong 0
	Resistive pull up and down	7	Weak 1	Weak 0

Table 10-2. Input buffer disable (port configuration 2)

GPIO_PRTx_PC2 ('x' denotes port number and 'y' denotes pin number)		
Bits	**Name**	**Description**
7:0	INP_DIS	Disables the input buffer independent of the port control drive mode. This bit should be set when analog signals are present on the pin.

10.3.1 High-impedance (high-Z) analog

The High-Z analog mode is the default reset state; both output driver and digital input buffer are turned off. This state prevents an external voltage from causing a current to flow into the digital input buffer. This drive mode is recommended for pins that are floating or that support an analog voltage. The High-impedance analog pins cannot be used for digital inputs. Reading the pin state register returns a 0x00 regardless of the data register value.

To achieve the lowest device current in low-power modes, unused GPIOs must be configured to the high-impedance analog mode.

10.3.2 High-impedance (high-Z) digital

The High-impedance digital mode is the standard high-impedance (High-Z) state recommended for digital inputs. In this state, the input buffer is enabled for digital input signals.

10.3.3 Resistive pull-up or resistive pull-down

The Resistive modes provide a series resistance in one of the data states and strong drive in the other. Pins can be used for either digital input or digital output in these modes. If resistive pull-up is required, a ‘1’ must be written to that pin’s Data Register bit. If resistive pull-down is required, a ‘0’ must be written to that pin’s Data Register. Interfacing mechanical switches is a common application of these drive modes. The resistive modes are also used to interface the EZ-PD™ PMG1-S0 MCU with open drain drive lines. Resistive pull-up is used when input is open drain low and resistive pull-down is used when input is open drain HIGH.

10.3.4 Open drain drives HIGH and open drain drives LOW

The Open drain modes provide high-Z in one of the data states and strong drive in the other. The pins can be used as digital input or output in these modes. Therefore, these modes are widely used in bi-directional digital communication. Open drain drive high mode is used when signal is externally pulled down and open drain drive low is used when signal is externally pulled high. A common application for open drain drives low mode is driving I^2C bus signal lines.

10.3.5 Strong drive

The strong drive mode is the standard digital output mode for pins; it provides a strong CMOS output drive in both high and low states. Strong drive mode pins must not be used as inputs under normal circumstances. This mode is often used for digital output signals or to drive external transistors.

10.3.6 Resistive pull-up and resistive pull-down

This mode is similar to the drive modes explained in **“Resistive pull-up and resistive pull-down”** on page 48. In the resistive pull-up and resistive pull-down mode, the GPIO will have a series resistance in both logic 1 and logic 0 output states. The high data state is pulled up while the low data state is pulled down. This mode is used when the bus is driven by other signals that may cause shorts.

10.4 Slew rate control

The GPIO pins have fast and slow output slew rate options in strong drive mode; this can be configured using the GPIO_PRTx_PC[25] bit. The slew rate is individually configurable for each port. This bit is cleared by default and the port works in fast slew mode. This bit can be set if a slow slew rate is required. The fast slew rate is recommended for signals higher than 1 MHz. Slower slew rate results in reduced EMI and crosstalk; hence, the slow option is recommended for signals that are not speed critical – generally less than 1 MHz.

10.5 CMOS LVTTL level control

The I/O pins can work at two voltage levels. These levels can be selected by writing to the GPIO_PRTx_PC[24] bit.

Input level is individually configurable for each port. This bit is cleared by default and the port works in CMOS mode. This bit can be set to reconfigure the port to LVTTL mode.

The CMOS mode can be used in most cases, whereas LVTTL can be used for custom interface requirements, which works at lower voltage levels. See the datasheet **[1]** for the input voltage thresholds (VIH and VIL) for the modes.

To change the input GPIO to work in LVTTL logic level, modify the “Threshold” parameter in the device configurator from “CMOS” to “TTL”. EZ-PD™ PMG1 devices cannot drive 1.8 V output through any GPIOs. The output GPIO should be configured with GPIO

Drive mode set to “Open Drain, Drives Low” in the device configurator. The pin should be pulled up to 1.8 V externally. To configure PMG1 GPIOs to the LVTTL threshold to connect to the I^2C bus, use EZ-PD™ PMG1-S0 SCB0 with P0.0 (I2C_0_SDA) and P0.1 (I2C_0_SCL). The pins for these SCBs form a separate GPIO port. Therefore, the change will not affect the logic levels of other GPIOs.

10.6 Fail-Safe GPIOs

The EZ-PD™ PMG1-S0 MCU device has two Fail-Safe GPIOs. These are P0.0 and P0.1 - I^2C pins from SCB0. It is similar to regular GPIOs with the following additional features:

- The Fail-Safe feature ensures that, in the absence of V_{BUS}/V_{SYS} power to the MCU, a logic high level on these pins due to I^2C line activity will not back-power the MCU.
- Provides better pull-down drive strength
- Serial Communication Block (SCB) when configured as I^2C and its lines routed to Fail-Safe GPIOs. It meets the following I^2C specifications:
  - Fast Mode hot-swap
  - Fast Mode Plus IOL Specification
  - Fast Mode and Fast Mode Plus Hysteresis and minimum fall time specifications

See the datasheet **[1]** for specifications.

10.7 High-Speed I/O Matrix

The high-speed I/O matrix (HSIOM) is a group of high-speed switches that routes GPIOs to the resources inside EZ-PD™ PMG1-S0 MCU. These resources include TCPWMs, SCB, and the USB PD. The HSIOM selects Active and Deep Sleep power domain sources for a pin. HSIOM_PORT_SELx are 32-bit wide registers that control the routing of GPIOs. Each register controls one port; four dedicated bits are assigned to each GPIO in the port. This provides up to 16 different options for GPIO routing. This selection provides different pin functions, as listed in **Table 10-3**.

Table 10-3. HSIOM port settings

HSIOM_PORT_SELx ('x' denotes port number and 'y' denotes pin number)			
Bits	**Name (SEL 'y')**	**Value**	**Description (Selects pin 'y' source (0 ≤ y ≤ 7)**
4y+3 : 4y	DR	0	Pin is regular firmware-controlled GPIO.
	AMUXA	6	Pin is connected to AMUXBUS-A.
	AMUXB	7	Pin is connected to AMUXBUS-B. This mode is also used for GPIO pre-charging of tank capacitors.
	ACT_0	8	Pin-specific Active source # 0 (TCPWM, EXT CLOCK)
	ACT_1	9	Pin-specific Active source #1.
	ACT_2	10	Pin-specific Active source #2.
	ACT_3	11	Pin-specific Active source #3.
	DPSLP_0	14	Pin-specific Deep Sleep source #0 (SCB - I^2C)
	DPSLP_1	15	Pin-specific Deep Sleep source #1 (SWD)

*Note: The active and deep sleep sources are pin dependent. See the "Pinouts" section of the **[1]** for more details on the features supported by each pin.*

10.8 Firmware controlled GPIO

See **Table 10-3** to know the HSIOM settings for a firmware controlled GPIO. GPIO_PRTx_DR is the data register used to read and write the output data for the GPIOs. A write operation to this register changes the GPIO output to the written value. Note that a read operation reflects the output data written to this register and not the current state of the GPIOs. Using this register, read-modify-write sequences can be safely performed on a port that has both input and output GPIOs.

In addition to the data register, two other registers - GPIO_PRTx_DR_SET and GPIO_PRTx_DR_CLR - are provided to set or clear the output data of specific GPIOs in port. Additionally, the GPIO_PRTx_DR_INV register can be used to invert the output data of a specific GPIO.

GPIO_PRTx_PS is the port I/O pad register that provides the state of the GPIOs when read. Writes to this register have no effect. See **[2]** for the details of these registers.

10.9 I/O port reconfiguration

Drive mode and GPIO can be reconfigured in runtime by changing the value of the GPIO_PRTx_PC and HSIOM_PORT_SELx registers. Take care to retain the pin state during reconfiguration of pins when they are connected directly to a digital peripheral. If the ports are driven by the data registers, state maintenance is automatic. During port configuration, the current configuration should be saved as follows:

1. Read the GPIO pin state - GPIO_PRTx_PS in software.
2. Write the GPIO_PRTx_PS value into the data registers - GPIO_PRTx_DR.
3. Change the corresponding field in HSIOM_PORT_SELx to drive the pin by the data register - GPIO_PRTx_DR.

10.10 I/O state on power up

By default, during power up all GPIOs are in high-impedance analog state and input buffers are disabled. When the chip is powered, its GPIOs can be configured according to the required application, by writing to the associated registers.

10.11 Behavior in low-power modes

The GPIOs maintain the current pin state during Sleep mode. In Sleep mode, all the GPIOs are active and can be driven by active peripherals, such as USB PD, TCPWM, and SCB.

In Deep Sleep mode, all the pin states are latched and the pin signals are retained, except the SCB pins, which remain functional and can wake up the processor on I^2C address matching event. The GPIO interrupts are also available in Deep Sleep mode with wake up ability.

For more details, see the **"Power supply and modes"** on page 58, **"Interrupts"** on page 29, and **"Serial communications block (SCB)"** on page 68.

To achieve the lowest device current in low-power modes, unused I/Os must be configured in the high-impedance analog mode.

10.12 GPIO Interrupt

This section describes the interrupt functionality of the EZ-PD™ PMG1-S0 MCU GPIOs.

10.12.1 Features

The features of the GPIO interrupt are:

- All eight pins in each port interface have an interrupt and an associated interrupt vector
- Pin status bits provide easy determination of interrupt source down to the pin level
- Rising, falling, or both edge-triggered interrupts are handled
- Pin interrupts can be individually enabled or disabled
- AHB interfaces for read and write into its registers
- Sends out a single port interrupt request (PIRQ) signal, derived from all GPIOs in a port, to the interrupt controller

10.12.2 Interrupt controller block diagram

Each port has its own individual interrupt request and associated interrupt request (IRQ) vector and interrupt service routine (ISR). Additionally, one pin can be selected on each port that is routed through a 50-ns glitch filter to form a glitch-tolerant interrupt for the port. The details are shown in **Figure 10-3**.

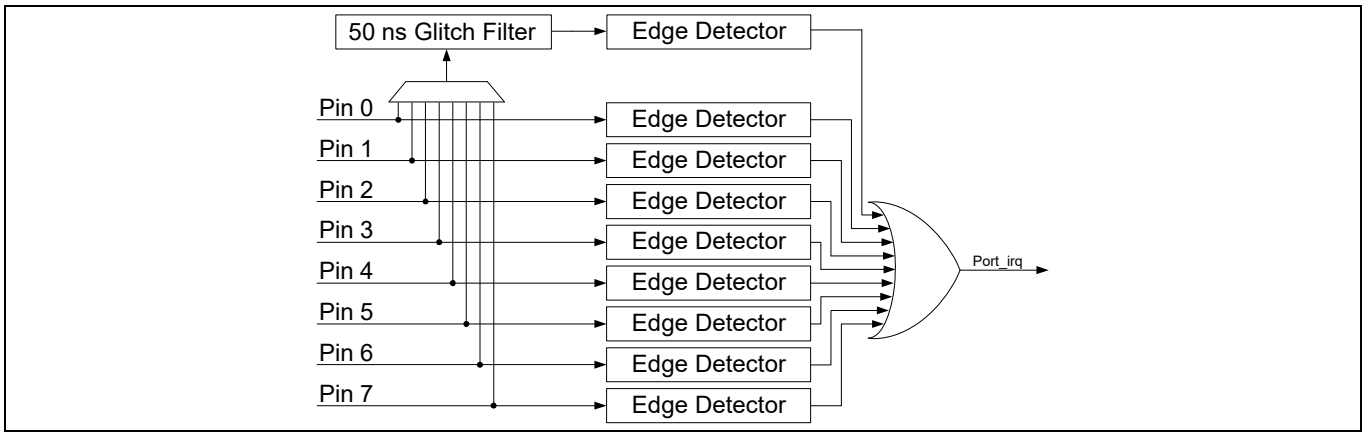


Figure 10-3. Interrupt generator

10.12.3 Function and configuration

Each pin of the port can be configured independently to generate an interrupt on the rising edge, falling edge, or on both edges by writing to the GPIO_PRTx_INTR_CFG register. Level-sensitive interrupts are not supported. GPIO_PRTx_INTR_CFG is also used to route a specific channel to the glitch filter and generate a ninth glitch-tolerant interrupt.

When a GPIO interrupt is triggered by a signal on an interrupt-enabled port pin, the GPIO_PRTx_INTR register (Port Interrupt Status Register) is updated. The firmware can read this register to determine which GPIO triggered the interrupt. Firmware can then clear the IRQ bit by writing a '1' to its corresponding bit.

Additionally, when the Port Interrupt Control Status Register is read at the same time an interrupt is occurring on the corresponding port, it can result in the interrupt not being properly detected. Therefore, when using GPIO interrupts, it is recommended to read the status register only inside the corresponding interrupt service routine and not in any other part of the code.

See GPIO_PRTx_INTR_CFG and GPIO_PRTx_INTR in **[2]** for more details.

10.13 Registers

Table 10-4. I/O registers

Name	Description
GPIO_PRTx_DR	Port Output Data Register
GPIO_PRTx_DR_SET	Port Output Data Set Register
GPIO_PRTx_DR_CLR	Port Output Data Clear Register
GPIO_PRTx_DR_INV	Port Output Data Inverting Register
GPIO_PRTx_PS	Port Pin State Register - Used to read logical pin state of I/O
GPIO_PRTx_PC	Port Configuration Register - Configures the output drive mode, input threshold, and slew rate
GPIO_PRTx_PC2	Port Secondary Configuration Register - Configures the input buffer of I/O pin
GPIO_PRTx_INTR_CFG	Port Interrupt Configuration Register
GPIO_PRTx_INTR	Port Interrupt Status Register
HSIOM_PORT_SELx	HSIOM Port Selection Register

Note: The 'x' in the register name denotes the port number. For example, GPIO_PTR1_DR is the port 1 output data register.

11 Clocking system

The EZ-PD™ PMG1-S0 MCU clock system includes these clock resources:

- Two internal clock sources:
  - 24–48 MHz internal main oscillator (IMO)
  - Internal low speed oscillator (ILO)- 40 kHz
- External clock (EXTCLK) generated using a signal from an I/O pin
- High-frequency clock (HFCLK) of up to 48 MHz selected from IMO or external clock
  - Dedicated prescaler for HFCLK
- Low-frequency clock (LFCLK) sourced by ILO
- Dedicated prescaler for system clock (SYSCLK) of up to 48 MHz sourced by HFCLK
- Ten peripheral clocks, four clocks with an 8-bit divider, four clocks are with 16-bit dividers and two with 16.5-bit divider

11.1 Block diagram

Figure 11-1 gives a generic view of the clocking system in EZ-PD™ PMG1-S0 MCU devices.

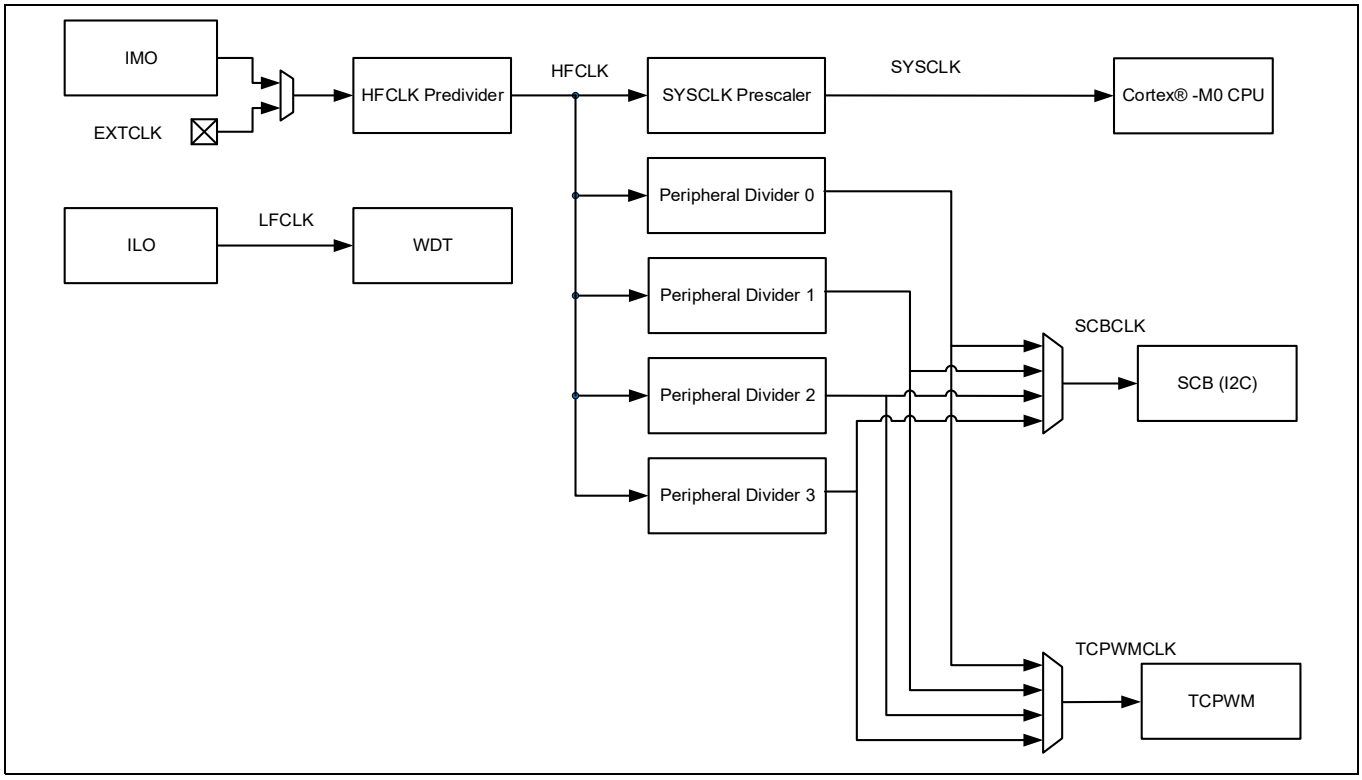


Figure 11-1. Clocking system block diagram

The three clock sources in the device are shown in **Figure 11-1**, on the left. The HFCLK mux selects the HFCLK source from an external clock source or the IMO. The HFCLK prescaler divides the HFCLK input. The SYSCLK prescaler generates the SYSCLK and the peripheral dividers generate the individual peripheral clocks. The ILO sources the LFCLK.

11.2 Clock sources

11.2.1 Internal main oscillator (IMO)

The IMO operates with no external components and outputs a stable clock at 24 MHz and 48 MHz frequencies. The frequencies are selected by setting the frequency range in the CLK_IMO_TRIM2 register and setting the IMO trim in the CLK_IMO_TRIM1 register. Each device has IMO trim measured during manufacturing to meet datasheet specifications; the trim is stored in manufacturing configuration data in SFLASH. These values may be loaded at startup to achieve the desired configuration. Firmware can retrieve these trim values and reconfigure the device to change the frequency at run-time.

11.2.1.1 Startup behavior

After reset, the IMO is configured for 24-MHz operation. During the “boot” portion of startup, trim values are read from flash and the IMO is configured to achieve datasheet specified accuracy. The HFCLK predivider is initially set to a divide value of 4 to reduce current consumption at startup.

11.2.2 Internal low-speed oscillator (ILO)

The ILO operates with no external components and outputs a stable clock at 40 kHz nominal. The ILO is relatively low power and low accuracy. It is available in all power modes. The ILO is always used as the system low-frequency clock LFCLK in EZ-PD™ PMG1-S0 MCU. The ILO is recommended to be always on, because it is the source of the WDT, which is required for reliable system operation. The ILO can be disabled by clearing the ENABLE bit in the CLK_ILO_CONFIG register. The WDT reset must be disabled before disabling the ILO. Otherwise, any register write to disable the ILO will be ignored. Enabling the WDT reset will automatically enable the ILO.

Notes: *Disabling the ILO reset is not recommended if:*

- *WDT protection is required against firmware crashes*
- *WDT protection is required against the power supply events that produce sudden brownout events that may in turn compromise the CPU functionality*

See the **“Clocking system”** on page 53 for details.

11.2.3 External clock

The external clock is a MHz range clock that can be generated from a signal on a designated EZ-PD™ PMG1-S0 MCU pin. This clock may be used in place of the IMO as the source of the system high-frequency clock HFCLK. The allowable external clock frequencies are 24 MHz and 48 MHz. EZ-PD™ PMG1-S0 MCU always starts up using the IMO, and the external clock must be enabled in user mode, so the device cannot be started from a reset clocked by the external clock.

11.3 Clock distribution

The EZ-PD™ PMG1-S0 MCU clocks are developed and distributed throughout the device, as shown in **Figure 11-1**. The distribution configuration options are as follows:

- HFCLK input selection
- HFCLK predivider configuration
- SYSCLK prescaler configuration
- Peripheral divider configuration

11.3.1 HFCLK input selection

HFCLK in EZ-PD™ PMG1-S0 MCU has input options: IMO and EXTCLK. The HFCLK input is selected using the CLK_SELECT register's DIRECT_SEL bits, as described in **Table 11-1**.

Table 11-1. HFCLK Input Selection Bits HFCLK_SEL

Name	Description
HFCLK_SEL[1:0]	HFCLK input clock selection 0: IMO. Uses the IMO as the source of the HFCLK 1: EXTCLK. Uses the EXTCLK as the source of the HFCLK 2–7: Reserved. Do not use

When manually configuring a pin as the input to the EXTCLK, the drive mode of the pin must be set to high-Z digital to enable the digital input buffer. See **"I/O system"** on page 44 for more details.

11.3.2 HFCLK predivider configuration

The HFCLK predivider allows the device to divide the HFCLK selection mux input before use as HFCLK. The predivider is capable of dividing the HFCLK by powers of 2 between 1 and 8. The predivider value is set using register CLK_SELECT bits HFCLK_DIV, as described in **Table 11-2**. The HFCLK predivider is set to a divide value of 4 during boot to reduce current consumption.

Note: HFCLK's frequency cannot exceed 16 MHz.

Table 11-2. HFCLK predivider value bits HFCLK_DIV

Name	Description
HFCLK_DIV[3:2]	HFCLK predivider value 0: 1. no divider on HFCLK 1: 2. divides HFCLK by 2 2: 4. divides HFCLK by 4 3: 8. divides HFCLK by 8

11.3.3 SYSCLK prescaler configuration

The SYSCLK Prescaler allows the device to divide the predivided HFCLK before use as SYSCLK, which allows for non-integer relationships between peripheral clocks and the system clock. SYSCLK must be equal to or faster than all other clocks in the device that are derived from HFCLK. The SYSCLK prescaler is capable of dividing the HFCLK by powers of 2 between 1 and 8. The prescaler divide value is set using register CLK_SELECT bits SYSCLK_DIV, as described in **Table 11-3**. The prescaler is initially configured to divide by 1.

Table 11-3. SYSCLK prescaler divide value bits SYSCLK_DIV

Name	Description
SYSCLK_DIV[7:6]	SYSCLK prescaler divide value 0: 1. SYSCLK = HFCLK 1: 2. SYSCLK = HFCLK/2 2: 4. SYSCLK = HFCLK/4 3: 8. SYSCLK = HFCLK/8

11.3.4 Peripheral clock divider configuration

The ten peripheral clocks are derived from the HFCLK using the 8-bit or 16-bit or 16.5 bit peripheral clock dividers. Each of the ten dividers is controlled by a PERI_DIV_8_CTL or PERI_DIV_16_CTL or PERI_DIV_16_5_CTL register, whose mapping is explained in **Table 11-4** and **Table 11-6**.

Table 11-4. Peripheral Cclock Divider Control Register PERI_DIV_8_CTLx

Bits	Name	Description
0	EN	Enables or disables the divider 0: Divider disabled 1: Divider enabled
15:8	INT8_DIV	Divide value of the divider. Output = Input/(INT8_DIV + 1)

Table 11-5. Peripheral Clock Divider Control Register PERI_DIV_16_5_CTLx

Bits	Name	Description
0	EN	Enables or disables the divider 0: Divider disabled 1: Divider enabled
23:8	INT16_DIV	Divide value for the divider. Output = Input/(INT16_DIV + 1) Acceptable divide values range from 1 to 65,536.

Table 11-6. Peripheral Clock Divider Control Register PERI_DIV_16_CTLx

Bits	Name	Description
0	EN	Enables or disables the divider 0: Divider disabled 1: Divider enabled
23:8	INT16_DIV	Divide value for the divider. Output = Input/(INT16_DIV + 1) Acceptable divide values range from 1 to 65,536.

The PERI_DIV_CMD register can be used to enable, disable, and select the type of clock dividers for all peripheral clock dividers. See the PERI_DIV_CMD in the EZ-PD™ PMG1-S0 MCU Registers TRM for more details.

The input clocks to the peripherals are selected by PERI_PCLK_CTLx registers. **Table 11-7** shows the peripheral clocks and their respective registers. See **[2]** for more details.

Table 11-7. Selecting Peripheral Clocks

Clock	Register
SCB0	PERI_PCLK_CTL0
SCB1	PERI_PCLK_CTL1
TCPWM	PERI_PCLK_CTLx (x = 2–7)
USBPD (RX)	PERI_PCLK_CTL8
USBPD (TX)	PERI_PCLK_CTL9
USBPD (8-bit SAR ADC)	PERI_PCLK_CTL10

11.4 Low-power mode operation

EZ-PD™ PMG1-S0 MCU clock behavior is different in different power modes. The MHz frequency clocks including the IMO, EXTCLK, HFCLK, SYSCLK, and peripheral clocks operate only in Active and Sleep modes. The ILO and LFCLK operate in all power modes.

11.5 Register list

Table 11-8. Clocking system register list

Register Name	Description
CLK_IMO_TRIM1	IMO Trim Register - This register contains IMO trim, allowing fine manipulation of its frequency.
CLK_IMO_TRIM2	IMO Frequency Selection Register - This register controls the frequency range of the IMO, allowing gross manipulation of its frequency.
CLK_ILO_CONFIG	ILO Configuration Register - This register controls the ILO configuration.
CLK_SELECT	Clock Select - This register controls clock tree configuration, selecting different sources for the system clocks.
PERI_DIV_8_CTLx/ PERI_DIV_16_CTLx/ PERI_DIV_16_5_CTLx	Peripheral Clock Divider Control Registers - These registers configure each of the peripheral clock dividers, enabling or disabling the divider and setting the integer divide value.
PERI_PCLK_CTLx	Programmable clock control registers - These registers are used to select the input clocks to peripherals.
PERI_DIV_CMD	Peripheral Divider command - This register enables the PCLK divider.

12 Power supply and modes

12.1 Block diagram

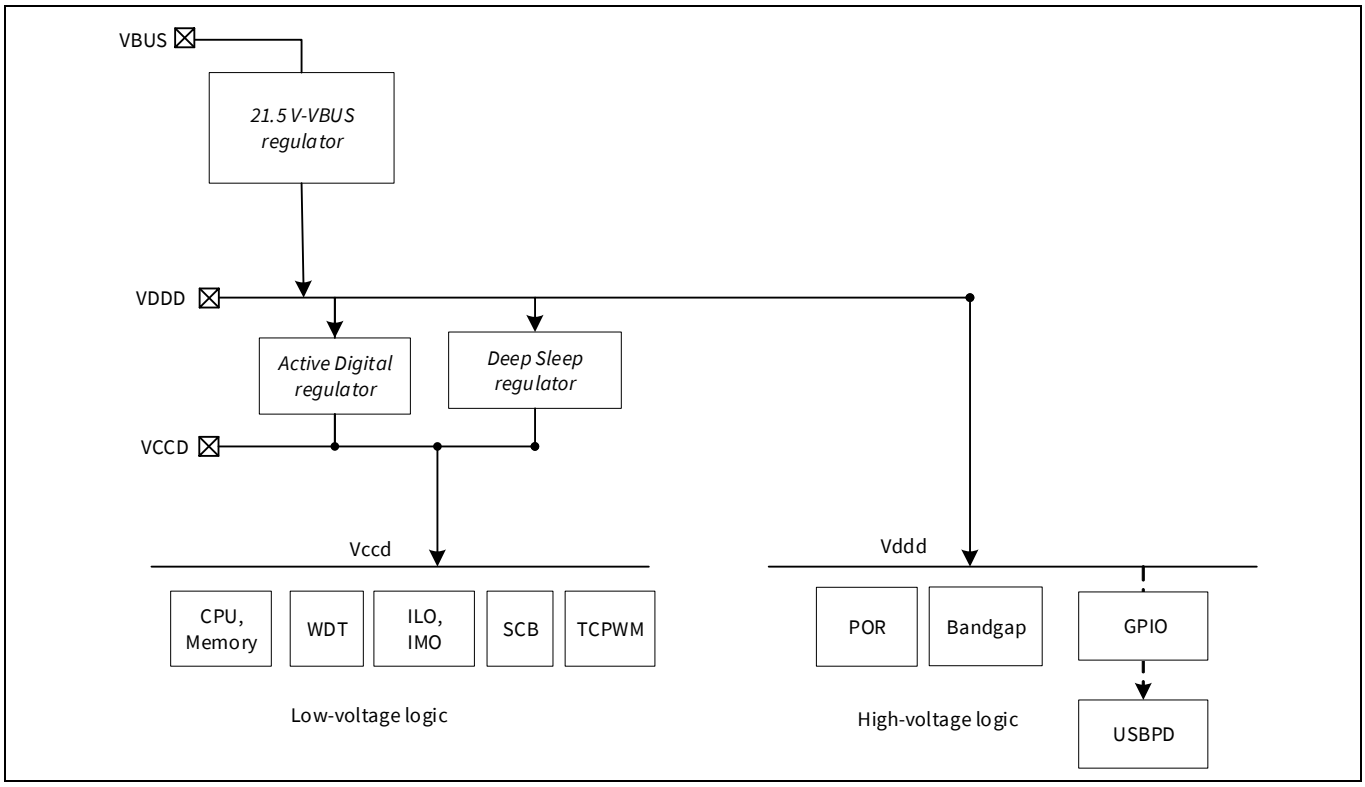


Figure 12-1. Power system requirement block diagram

12.2 Power system requirement overview

EZ-PD™ PMG1-S0 MCU can operate from two possible external supply sources: VBUS (4.0 V–21.5 V) or VDDD (2.7 V–5.5 V). The VBUS supply is regulated inside the device with an LDO. The switched supply, VDDD, is either used directly inside some analog blocks or further regulated down to VCCD, which powers most of the core using the regulators. EZ-PD™ PMG1-S0 MCU has three different power modes: Active, Sleep, and Deep Sleep. Transitions between these power modes are managed by the power system. A separate power domain, VDDD, is provided for the GPIOs. The VDDD and VCCD pins, both outputs of regulators, are brought out for connecting a 1-µF capacitor for the regulator stability only. These pins are not supported as power supplies.

12.3 Power modes

The power modes of the device accessible and observable by the user are listed in the **Table 12-1**.

Table 12-1. EZ-PD™ PMG1-S0 MCU power modes

Mode	Description
RESET	Power is valid and an internal reset source is asserted or SleepController is sequencing the system out of reset
ACTIVE	Power is valid and CPU is executing instructions
SLEEP	Power is valid and CPU is not executing instructions. All logic that is not operating is clock gated to save power.
DEEP SLEEP	Main regulator and most blocks are shut off. The Deep Sleep regulator powers logic, but only the low-frequency clock is available.

12.4 Mode transitions

The primary mode transition diagram is shown in **Figure 12-2**.

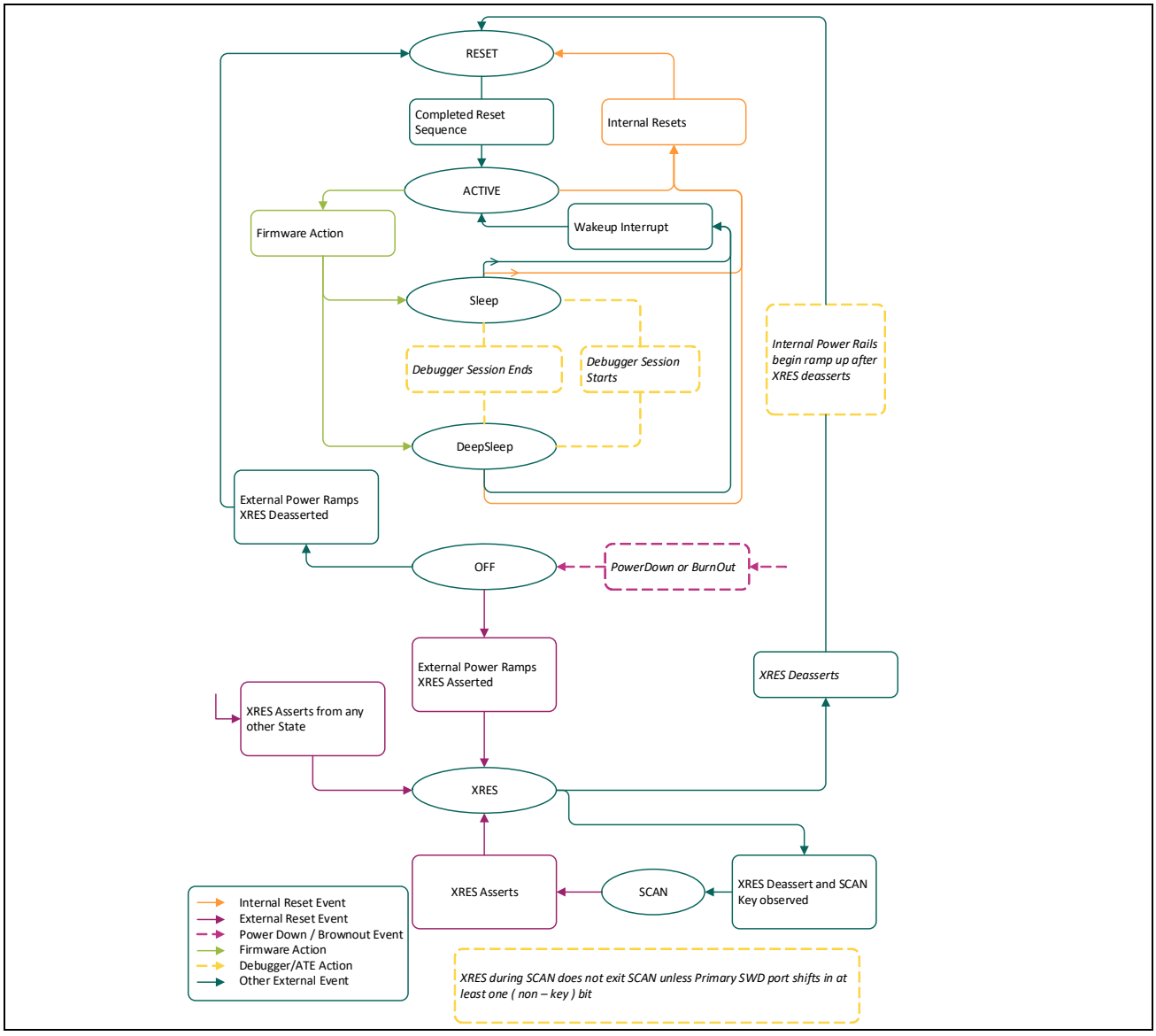


Figure 12-2. EZ-PD™ PMG1-S0 MCU power mode transition diagram

13 Chip operational modes

EZ-PD™ PMG1-S0 MCU is capable of executing firmware in four different modes. These modes dictate execution from different locations in Flash and ROM, with different levels of hardware privileges. Only three of these modes are used in end-applications; debug mode is used exclusively to debug designs during firmware development.

EZ-PD™ PMG1-S0 MCU's operational modes are:

- Boot
- User
- Privileged
- Debug

13.1 Boot

The boot mode is an operational mode where the device is configured by instructions hard-coded in the device SROM. This mode is entered after the end of a reset, provided no debug-acquire sequence is received by the device. The boot mode is a privileged mode; interrupts are disabled in this mode so that the boot firmware can set up the device for operation without being interrupted. During the power-up phase, hardware trim settings are loaded from nonvolatile (NV) latches to guarantee proper operation during power-up. When boot concludes, the device enters user mode and code execution from flash begins.

13.2 User

The user mode is an operational mode where normal user firmware from flash is executed. User mode cannot execute code from SROM. Firmware execution in this mode includes the automatically generated firmware by the IDE and the firmware written by the user. The automatically generated firmware can govern both the firmware startup and portions of normal operation. The boot process transfers control to this mode after it has completed its tasks.

13.3 Privileged

The privileged mode is an operational mode, which allows execution of special subroutines that are stored in the device ROM. These subroutines cannot be modified by the user and are used to execute proprietary code that is not meant to be interrupted or observed. Debugging is not allowed in privileged mode.

The CPU can transition to privileged mode through the execution of a system call. For more information on how to perform a system call, see **"Performing a system call"** on page 158. Exit from this mode returns the device to user mode.

13.4 Debug

the debug mode is an operational mode that allows observation of the EZ-PD™ PMG1-S0 MCU operational parameters. This mode is used to debug the firmware during development. The debug mode is entered when an SWD debugger connects to the device during the acquire time window, which occurs during the device reset. Debug mode allows IDEs such as Eclipse and Arm MDK to debug the firmware. Debug mode is only available on devices in open mode (one of the four protection modes). For more details on the debug interface, see the **"Program and debug interface"** on page 147.

For more details on protection modes, see the **"Device security"** on page 66.

14 Watchdog timer (WDT)

The WDT is used to automatically reset the device in the event of an unexpected firmware execution path or a brownout that compromises the CPU functionality. The WDT runs from the LFCLK (40 kHz clock), generated by the ILO. The timer must be serviced periodically in firmware to avoid a reset. Otherwise, the timer will elapse and generate a device reset. The WDT can be used as an interrupt source or a wakeup source in low-power modes.

14.1 Features

The WDT has these features:

- Configurable timer period
- Generates an interrupt in Sleep and Deep Sleep power modes to wake up the device
- Generate interrupts in Active mode at specified interval

14.2 Block diagram

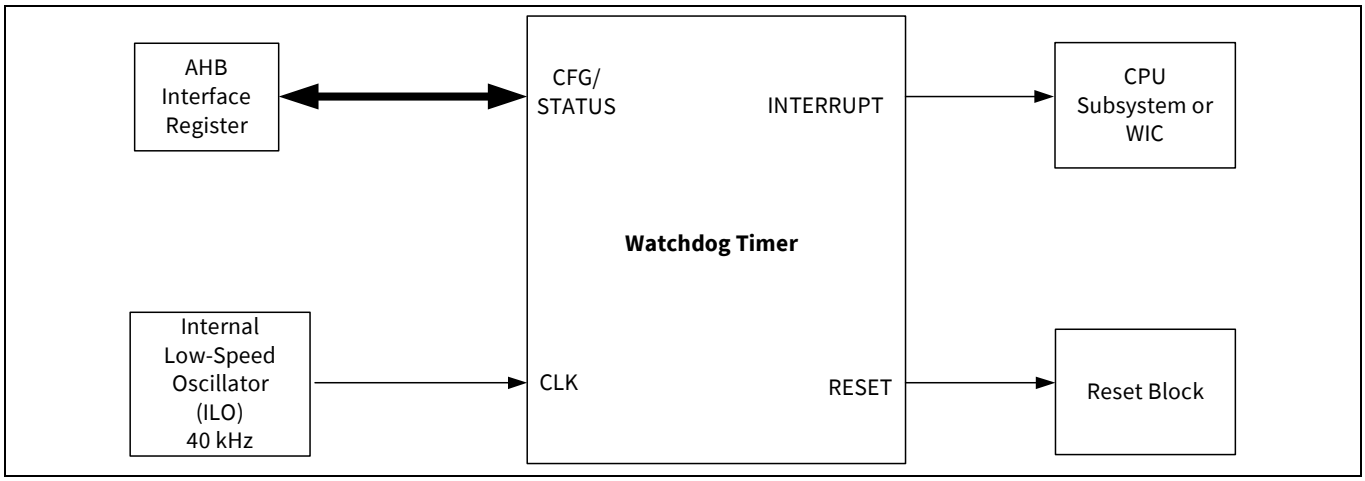


Figure 14-1. Watchdog timer block diagram

14.3 How it works

The WDT asserts a hardware reset to the device after three WDT interrupts each of programmable interval of up to 1638.4 ms (assuming 40 kHz clock frequency), unless it is periodically serviced in firmware. The WDT is a 16-bit free-running wraparound up-counter.

The WDT_COUNTER register provides the count value of the WDT. The WDT generates an interrupt when the count value in WDT_COUNTER equals the match value stored in the WDT_MATCH register, but it does not reset the count to '0'. Instead, the WDT keeps counting until it overflows and rolls back to ‘0’. When the count value again reaches the match value, another interrupt is generated.

A bit named WDT_MATCH in the SRSS_INTR register is set whenever the WDT interrupt occurs. This interrupt must be cleared by writing a '1' to the WDT_MATCH bit in SRSS_INTR to feed the watchdog timer. If the firmware does not feed the WDT for two consecutive interrupts, the third match event will generate a hardware reset.

For details, see the WDT_COUNTER, WDT_MATCH, and SRSS_INTR registers in the section [2].

When the WDT is used to protect against system crashes, clearing the WDT interrupt bit to feed the watchdog must be done from a portion of the code that is not directly associated with the WDT interrupt. Otherwise, even if the main function of the firmware crashes or is in an endless loop, the WDT interrupt vector can still be intact and feed the WDT periodically.

The safest way to use the WDT against system crashes is:

- Feed the watchdog by clearing the interrupt bit regularly in the main body of the firmware code.
- Guarantee that the interrupt is cleared at least once every WDT period.
- Use the WDT interrupt service routine (ISR) only as a timer to trigger certain actions and to change the next WDT_MATCH value. Do not feed WDT in this ISR.

Follow these steps to use WDT as a periodic interrupt generator:

1. Write the desired match value to the WDT_MATCH register.
2. Clear the WDT_MATCH bit in SRSS_INTR to clear any pending WDT interrupt.
3. Unmask the WDT interrupt by setting the WDT_MATCH bit in SRSS_INTR_MASK.
4. In the ISR, clear the WDT interrupt and update the match value. By doing so, another periodic interrupt will be generated when the counter reaches the new match value.
5. The IGNORE_BITS in the WDT_MATCH register can be used to reduce the entire WDT counter period. The ignore bits can specify the number of MSBs that needs to be discarded. For example, if the IGNORE_BITS value is 3, then WDT counter becomes a 13-bit counter.

14.3.1 Enabling and disabling WDT

The WDT is a free-running counter that cannot be disabled. However, it is possible to disable the WDT reset by writing a key '0xACED8865' to the WDT_DISABLE_KEY Register. Writing any other value to this register will enable the WDT reset. If WDT reset is disabled, the firmware does not need to periodically feed the WDT to avoid a reset. The WDT can still be used as an interrupt source or wakeup source. The only way to stop WDT from generating interrupts and wakeup events is to disable the ILO by clearing the ENABLE bit in the CLK_ILO_CONFIG Register. The WDT reset must be disabled before disabling the ILO. Otherwise, any register write to disable the ILO will be ignored. Enabling the WDT reset will automatically enable the ILO.

Notes: *Disabling the WDT reset is not recommended if:*

- *Protection is required against firmware crashes*
- *The power supply can produce sudden brownout events that may compromise the CPU functionality*

14.3.2 WDT interrupts and Low-power modes

The WDT counter sends the interrupt requests to the CPU in Active power mode and to the wakeup interrupt controller (WIC) in Sleep and Deep Sleep power modes. It works as follows:

- **Active mode:** In Active power mode, the WDT sends the interrupt to the CPU. The CPU acknowledges the interrupt request and executes the ISR. The interrupt must be cleared after entering the ISR in firmware.
- **Sleep or Deep Sleep mode:** In this mode, the CPU subsystem is powered down. Therefore, the interrupt request from the WDT is directly sent to the WIC, which will then wake up the CPU. The CPU acknowledges the interrupt request and executes the ISR. The interrupt must be cleared after entering the ISR in firmware.

For more details, see **“Power supply and modes”** on page 58.

14.3.3 WDT reset mode

The RESET_WDT bit in the RES_CAUSE register indicates the reset generated by the WDT. This bit remains set until cleared or until a power-on reset (POR) or brownout reset (BOD) occurs. All other resets leave this bit untouched.

For more details, see **“Reset system”** on page 64.

14.4 Register list

Table 14-1. WDT registers

Register name	Description
WDT_DISABLE_KEY	Disables the WDT reset when 0XACED8865 is written, for any other value WDT works normally
WDT_COUNTER	Provides the count value of the WDT
WDT_MATCH	Stores the match value and ignores bits of the WDT
SRSS_INTR	Feeds the WDT to avoid reset
SRSS_INTR_SET	sets the overtemperature interrupt
SRSS_INTR_MASK	Masks/unmasks the WDT interrupt to the CPU

15 Reset system

EZ-PD™ PMG1-S0 MCU supports several types of resets that guarantee error-free operation during power up and allow the device to reset based on user-supplied external hardware or internal software reset signals. EZ-PD™ PMG1-S0 MCU also contains hardware to enable the detection of certain resets.

The reset system has these sources:

- Power-on reset (POR) to hold the device in reset while the power supply ramps up
- Brownout reset (BOD) to reset the device if the power supply falls below specifications during operation
- Watchdog reset (WRES) to reset the device if firmware execution fails to service the watchdog timer
- Software initiated reset (SRES) to reset the device on demand using firmware
- Protection fault reset (PROT_FAULT) to reset the device if unauthorized operating conditions occur

15.1 Reset sources

The following sections provide a description of the reset sources available in EZ-PD™ PMG1-S0 MCU.

15.1.1 Power-on reset (POR)

The POR is provided for system reset at power-up. POR holds the device in reset until the supply voltage, V_{DDD} reaches a threshold as per **[1]**. The POR activates automatically at power-up.

POR events do not set a reset cause status bit, but can be partially inferred by the absence of any other reset source. If no other reset event is detected, then the reset is caused by POR or BOD.

15.1.2 Brownout reset (BOD)

The BOD monitors the digital voltage supply V_{CCD} and generates a reset if V_{CCD} is below the minimum logic operating voltage specified in the section **[1]**. BOD is available in all power modes.

The BOD events do not set a reset cause status bit, but in some cases they can be detected. In some BOD events, V_{CCD} will fall below the minimum logic operating voltage, but remain above the minimum logic retention voltage. Thus, some BOD events may be distinguished from POR events by checking for logic retention.

15.1.3 Watchdog reset (WRES)

The WRES detects errant code by causing a reset if the watchdog timer is not cleared within the user-specified time limit. This feature is enabled by setting the WDT_ENABLEx bit in the WDT_CONTROL register.

The RESET_WDT status bit of the RES_CAUSE register is set when a watchdog reset occurs. This bit remains set until cleared or until a POR or BOD reset; for example, in the case of a device power cycle. All other resets leave this bit untouched.

For more details, see **Watchdog timer (WDT)**.

15.1.4 Software initiated reset (SRES)

The SRES is a mechanism that allows a software-driven reset. The Arm® Cortex®-M0 application interrupt and reset control register (CM0_AIRCR) forces a device reset when a ‘1’ is written into the SYSRESETREQ bit. CM0_AIRCR requires a value of A05F written to the top two bytes for writes. Therefore, write A05F0004 for the reset.

The RESET_SOFT status bit of the RES_CAUSE register is set when a software reset occurs. This bit remains set until cleared or until a POR or BOD reset; for example, in the case of a device power cycle. All other resets leave this bit untouched.

15.1.5 Protection fault reset (PROT_FAULT)

The PROT_FAULT detects unauthorized protection violations and causes a device reset if they occur. One example of a protection fault is if a debug breakpoint is reached while executing privileged code. For details about privilege code, see **"Privileged"** on page 60.

The RESET_PROT_FAULT bit of the RES_CAUSE register is set when a protection fault occurs. This bit remains set until cleared or until a POR or BOD reset; for example, in the case of a device power cycle. All other resets leave this bit untouched.

15.2 Identifying reset sources

When the device comes out of reset, it is often useful to know the cause of the most recent or even older resets. This is achieved in the device primarily through the RES_CAUSE register. This register has specific status bits allocated for some of the reset sources. The RES_CAUSE register supports detection of watchdog reset, software reset, and protection fault reset. It does not record the occurrences of either POR or BOD. The bits are set on the occurrence of the corresponding reset and remain set after the reset, until cleared or a loss of retention, such as a POR reset or brownout below the logic retention voltage.

If the RES_CAUSE register cannot detect the cause of the reset, then it can be one of the non-recorded and non-retention resets: BOD or POR. These resets cannot be distinguished using on-chip resources.

15.3 Register list

Table 15-1. Reset system register list

Register name	Description
WDT_CONTROL	Watchdog Timer Control register - This register allows configuration of the device watchdog timer.
CM0_AIRCR	Arm® Cortex®-M0 Application Interrupt and Reset Control register - This register allows initiation of software resets, among other Arm® Cortex®-M0 functions.
RES_CAUSE	Reset Cause register - This register captures the cause of recent resets.

16 Device security

EZ-PD™ PMG1-S0 MCU offers a number of options for protecting user designs from unauthorized access or copying. Disabling debug features and robust flash protection provide a high level of security.

The debug circuits are enabled by default and can only be disabled in firmware. If disabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging. Additionally, all device interfaces can be permanently disabled for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. Permanently disabling interfaces is not recommended for most applications because the designer cannot access the device. For more information, as well as a discussion of flash row and chip protection, see **[3]**.

Note: Because all programming, debug, and test interfaces are disabled when maximum device security is enabled, EZ-PD™ PMG1-S0 MCU devices with full device security enabled may not be returned for failure analysis.

16.1 Features

The EZ-PD™ PMG1-S0 MCU device security system has the following features:

- User-selectable levels of protection
- In the most secure case provided, the chip can be “locked” such that it cannot be acquired for test/debug and it cannot enter erase cycles. Interrupting erase cycles is a known way for hackers to leave chips in an undefined state and open to observation
- CPU execution in a privileged mode by use of the non-maskable interrupt (NMI). When in privileged mode, NMI remains asserted to prevent any inadvertent return from interrupt instructions causing a security leak

16.2 How it works

The CPU operates in normal user mode or in privileged mode, and the device operates in one of four protection modes: BOOT, OPEN, PROTECTED, and KILL. Each mode provides specific capabilities for the CPU software and debug. You can change the mode by writing to the CPUSS_PROTECTION register.

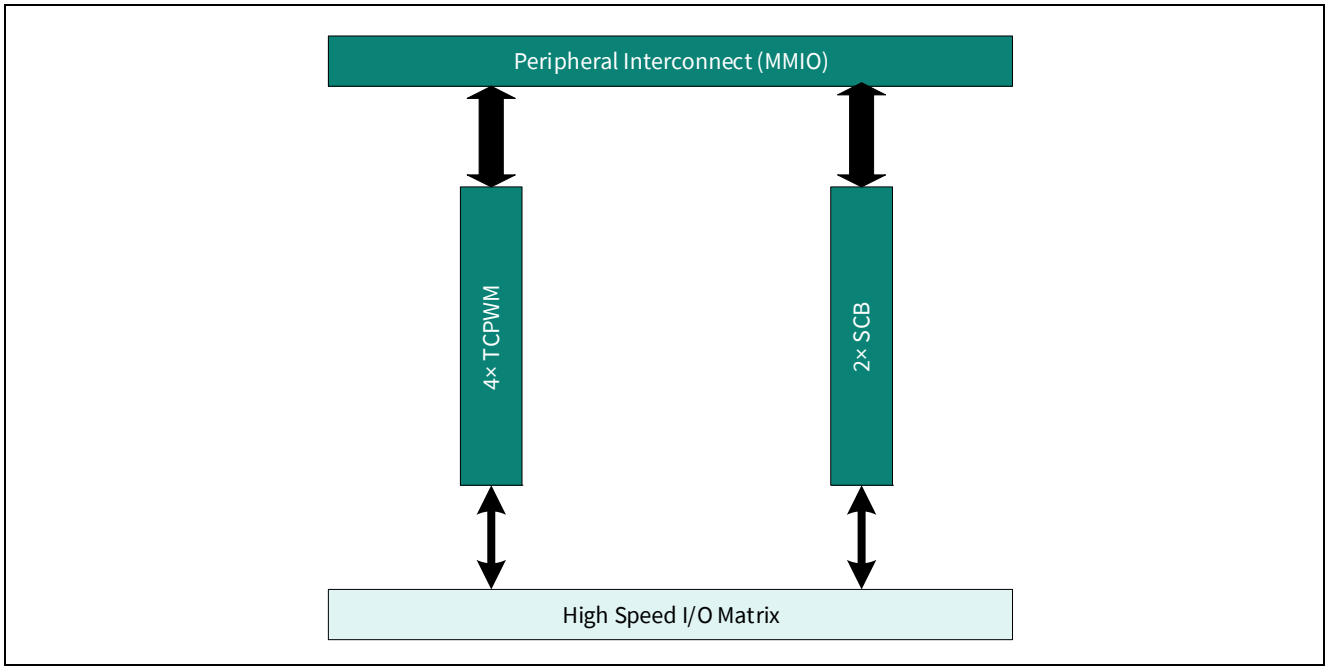
- **BOOT mode**: The device comes out of reset in BOOT mode. It stays there until its protection state is copied from supervisor flash to the protection control register (CPUSS_PROTECTION). The debug-access port is stalled until this has happened. BOOT is a transitory mode required to set the part to its configured protection state. During BOOT mode, the CPU always operates in privileged mode.
- **OPEN mode**: This is the factory default. The CPU can operate in user mode or privileged mode. In user mode, flash can be programmed and debugger features are supported. In privileged mode, access restrictions are enforced.
- **PROTECTED mode**: The user may change the mode from OPEN to PROTECTED. This disables all debug access to user code or memory. Access to most registers is still available; debug access to registers to reprogram flash is not available. The mode can be set back to OPEN but only after completely erasing the flash.
- **KILL mode**: The user may change the mode from OPEN to KILL. This removes all debug access to user code or memory, and the flash cannot be erased. Access to most registers is still available; debug access to registers to reprogram flash is not available. The part cannot be taken out of KILL mode; devices in KILL mode may not be returned for failure analysis.

Section E: Digital system

This section encompasses the following chapters:

- **"Serial communications block (SCB)"** on page 68
- **"Timer, Counter, and PWM"** on page 112

Top-level architecture



18 Serial communications block (SCB)

The SCB of EZ-PD™ PMG1-S0 MCU supports three serial interface protocols: SPI, UART, and I^2C. Only one of the protocols is supported by an SCB at any given time. EZ-PD™ PMG1-S0 MCU devices have four SCBs.

18.1 Features

This block supports the following features:

- Standard SPI master and slave functionality with Motorola, Texas Instruments, and National Semiconductor protocols
- Standard UART functionality with SmartCard reader, Local Interconnect Network, and IrDA protocols
- Standard I^2C master and slave functionality
- SPI and I^2C EZ mode, which allows for operation without CPU intervention
- Low-power (Deep Sleep) mode of operation for SPI and I^2C protocols (using external clocking)

Each of the three protocols is explained in the following sections.

18.2 Serial peripheral interface (SPI)

The SPI protocol is a synchronous serial interface protocol. Devices operate in either master or slave mode. The master initiates the data transfer. The SCB supports single master-multiple slaves topology for SPI. Multiple slaves are supported with individual slave select lines.

You can use the SPI master mode when the EZ-PD™ PMG1-S0 MCU has to communicate with one or more SPI slave devices. The SPI slave mode can be used when the EZ-PD™ PMG1-S0 MCU has to communicate with an SPI master device.

18.2.1 Features

- Supports master and slave functionality
- Supports 3 types of SPI protocols:
  - Motorola SPI – modes 0, 1, 2, and 3
  - TI SPI, with coinciding and preceding data frame indicator for mode 1
  - National (MicroWire) SPI for mode 0
- Data frame size programmable from 4 bits to 16 bits
- Interrupts or polling CPU interface
- Programmable oversampling
- Supports EZ mode of operation (**Easy SPI (EZSPI) protocol** (applicable only for SPI slave functionality))
- Supports externally clocked slave operation:
  - In this mode, the slave operates in Active, Sleep, and Deep Sleep system power modes
  - EZSPI mode allows for operation without CPU intervention

18.2.2 General description

Figure 18-1 illustrates an example of SPI master with four slaves.

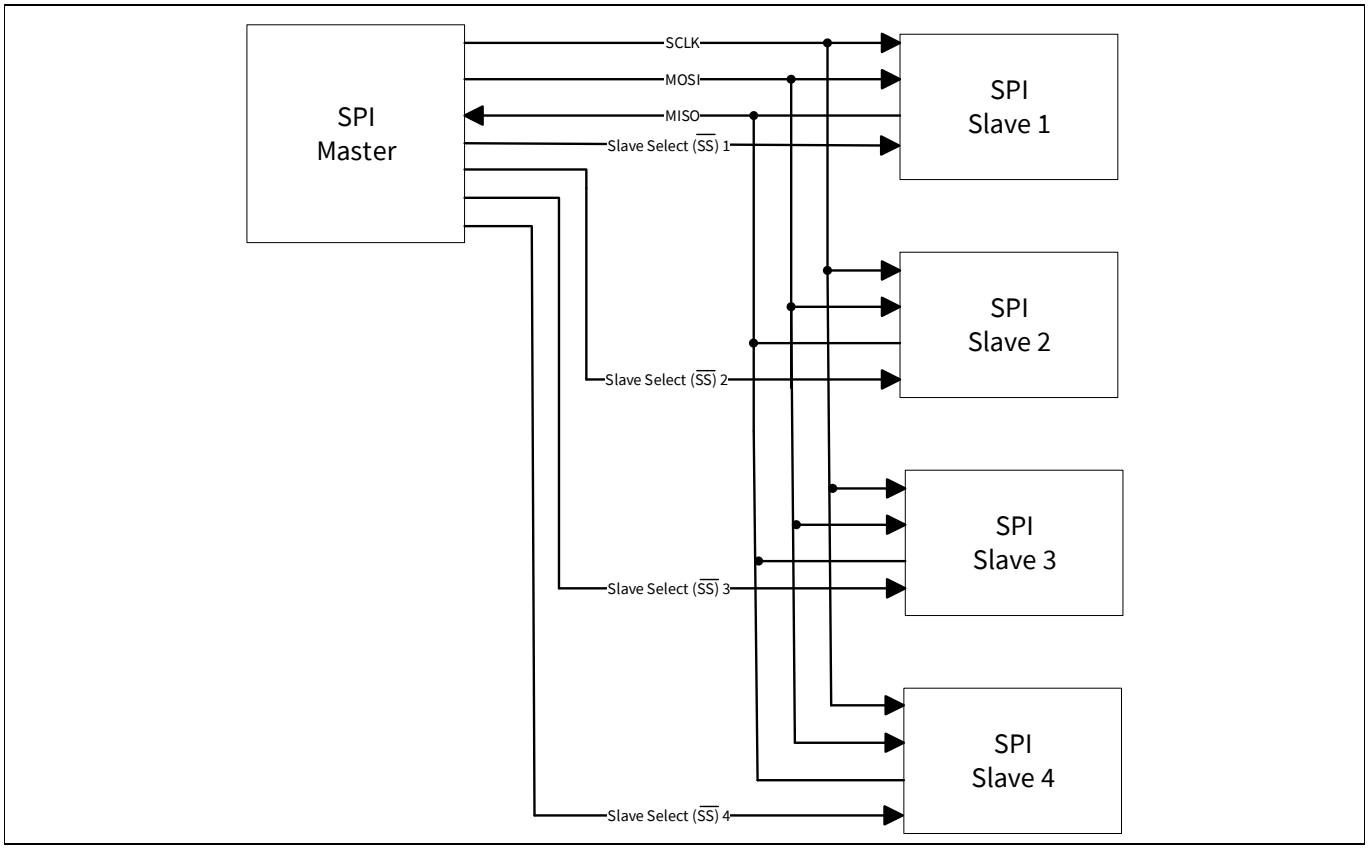


Figure 18-1. SPI example

A standard SPI interface consists of four signals as follows.

- **SCLK**: Serial clock (clock output from the master, input to the slave)
- **MOSI**: Master-out-slave-in (data output from the master, input to the slave)
- **MISO**: Master-in-slave-out (data input to the master, output from the slave)
- **Slave Select ($\overline{SS}$)**: Typically an active low signal (output from the master, input to the slave)

A simple SPI data transfer involves the following: the master selects a slave by driving its SS line, then it drives data on the MOSI line and a clock on the SCLK line, The slave uses the edges of SCLK to capture the data on the MOSI line; it also drives data on the MISO line, which is captured by the master.

By default, the SPI interface supports a data frame size of eight bits (1 byte). The data frame size can be configured to any value in the range 4 to 16 bits. The serial data can be transmitted either most significant bit (MSB) first or least significant bit (LSB) first.

Three different variants of the SPI protocol are supported by the SCB:

- **Motorola SPI**: This is the original SPI protocol
- **Texas Instruments SPI**: A variation of the original SPI protocol, in which data frames are identified by a pulse on the $\overline{SS}$ line
- **National Semiconductors SPI**: A half duplex variation of the original SPI protocol

18.2.3 SPI modes of operation

18.2.3.1 Motorola SPI

The original SPI protocol was defined by Motorola. It is a full duplex protocol. Multiple data transfers may happen with the SS line held at '0'. As a result, slave devices must keep track of the progress of data transfers to separate individual data frames. When not transmitting data, the SS line is held at '1' and SCLK is typically OFF.

- **Motorola SPI modes**

The Motorola SPI protocol has four different modes based on how data is driven and captured on the MOSI and MISO lines. These modes are determined by clock polarity (CPOL) and clock phase (CPHA).

Clock polarity determines the value of the SCLK line when not transmitting data. CPOL = '0' indicates that SCLK is '0' when not transmitting data. CPOL = '1' indicates that SCLK is '1' when not transmitting data.

Clock phase determines when data is driven and captured. CPHA=0 means sample (capture data) on the leading (first) clock edge, while CPHA=1 means sample on the trailing (second) clock edge, regardless of whether that clock edge is rising or falling. With CPHA=0, the data must be stable for setup time before the first clock cycle.

- **Mode 0: CPOL is '0', CPHA is '0'** - Data is driven on a falling edge of SCLK. Data is captured on a rising edge of SCLK
- **Mode 1: CPOL is '0', CPHA is '1'** - Data is driven on a rising edge of SCLK. Data is captured on a falling edge of SCLK
- **Mode 2: CPOL is '1', CPHA is '0'** - Data is driven on a rising edge of SCLK. Data is captured on a falling edge of SCLK
- **Mode 3: CPOL is '1', CPHA is '1'** - Data is driven on a falling edge of SCLK. Data is captured on a rising edge of SCLK

Figure 18-2 illustrates driving and capturing of MOSI/MISO data as a function of CPOL and CPHA.

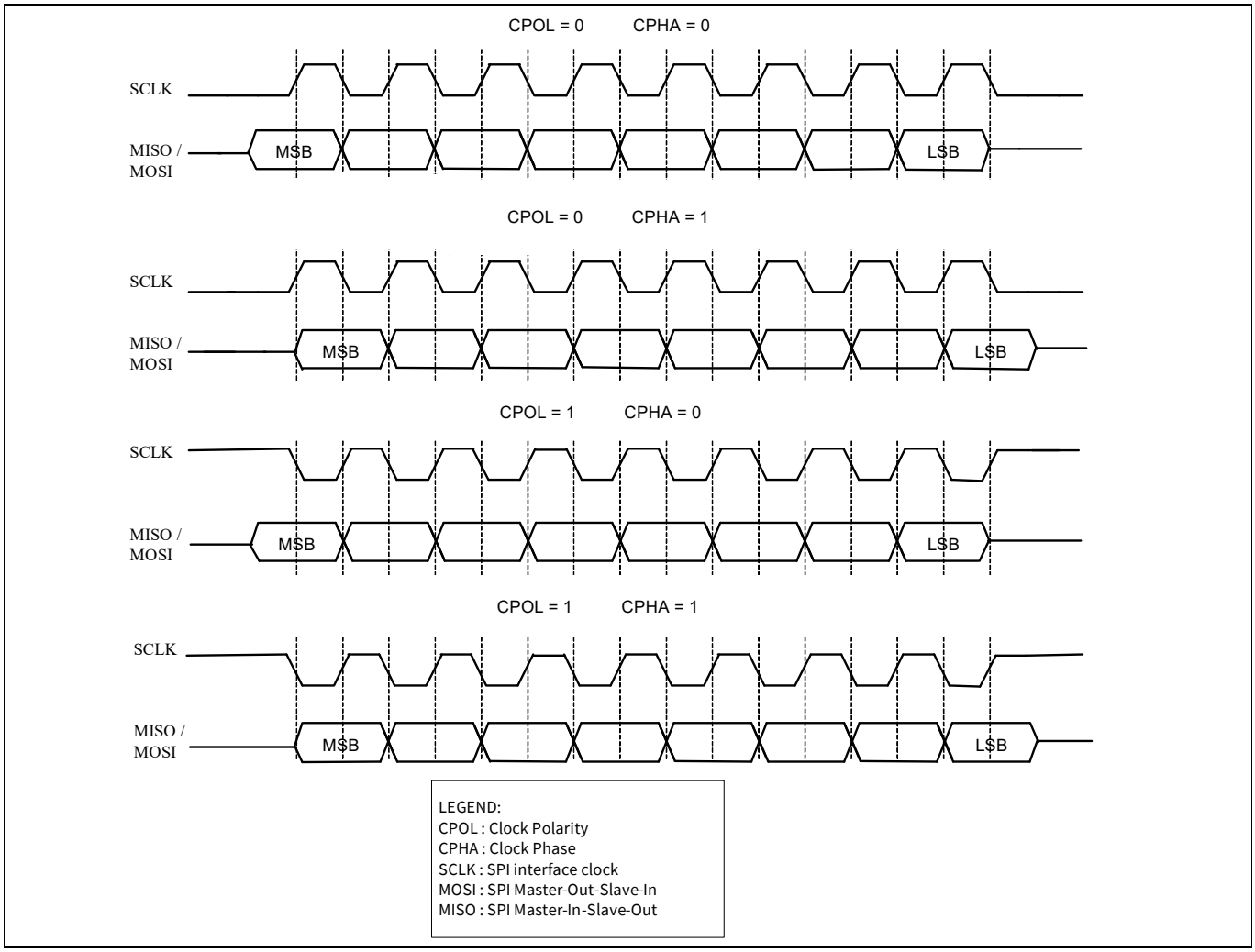


Figure 18-2. SPI Motorola, 4 modes

Figure 18-3 illustrates a single 8-bit data transfer and two successive 8-bit data transfers in mode 0 (CPOL is '0', CPHA is '0').

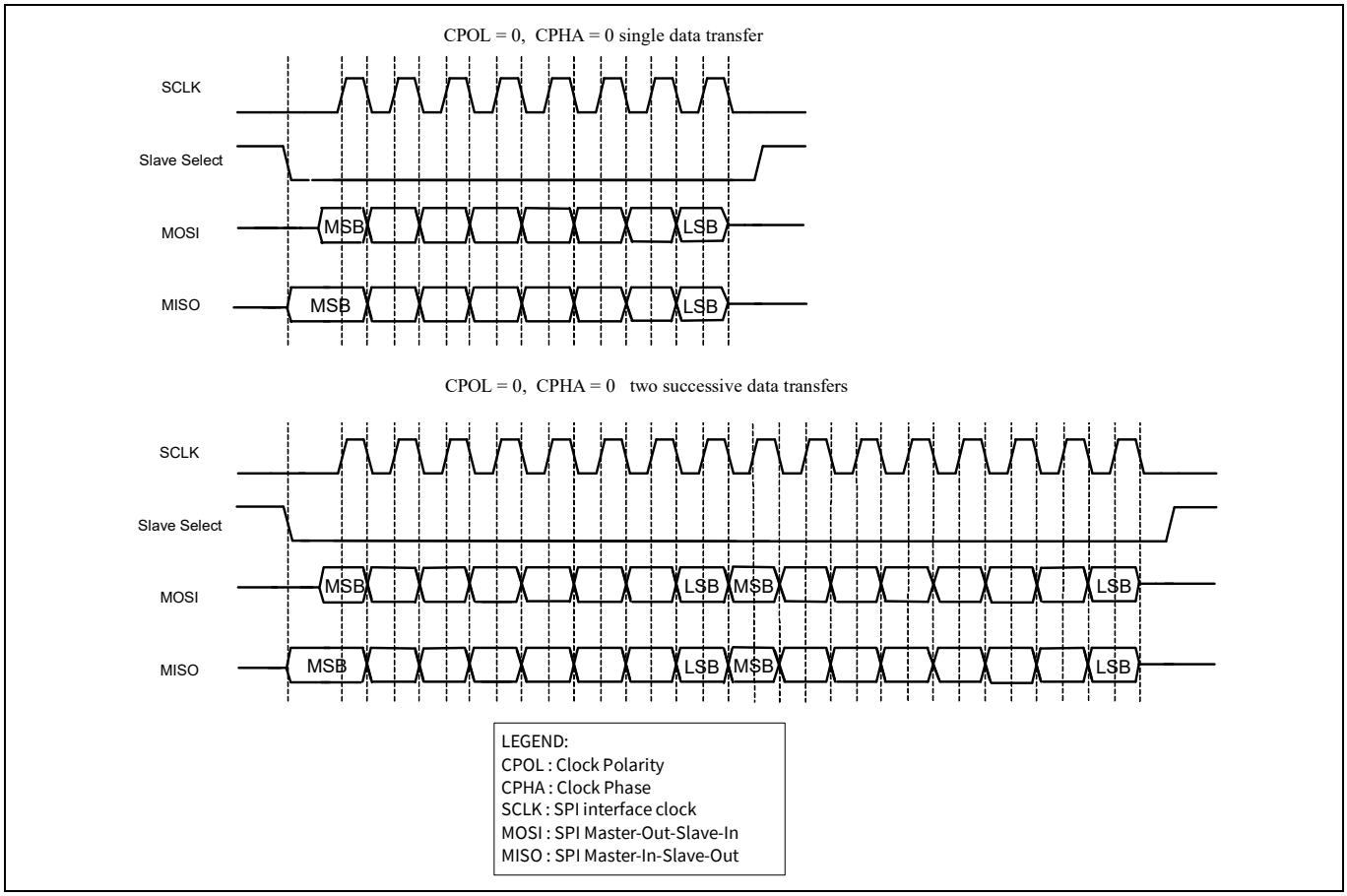


Figure 18-3. SPI Motorola data transfer example

- **Configuring SCB for SPI Motorola mode**

To configure the SCB for SPI Motorola mode, set various register bits in the following order:

1. Select SPI by writing '01' to the MODE (bits [25:24]) of the SCBx_CTRL register
2. Select SPI Motorola mode by writing '00' to the MODE (bits [25:24]) of the SCBx_SPI_CTRL register
3. Select the mode of operation in Motorola by writing to the CPHA and CPHA fields (bits 2 and 3 respectively) of the SCBx_SPI_CTRL register
4. Follow steps 2 to 4 mentioned in **“Enabling and initializing SPI”** on page 79

For more information on these registers, see **[2]**.

18.2.3.2 Texas Instruments SPI

The Texas Instruments' SPI protocol redefines the use of the $\overline{SS}$ signal. It uses the signal to indicate the start of a data transfer, rather than a low active slave select signal, as in the case of Motorola SPI. As a result, slave devices need not keep track of the progress of data transfers to separate individual data frames. The start of a transfer is indicated by a high active pulse on slave select signal for a single bit transfer period. This pulse can be configured to occur one cycle before the transmission of the first data bit, or coincide with the transmission of the first data bit. The TI SPI protocol supports only mode 1 (CPOL is '0' and CPHA is '1'): data is driven on a rising edge of SCLK and data is captured on a falling edge of SCLK.

Figure 14-4 illustrates a single 8-bit data transfer and two successive 8-bit data transfers. The SELECT pulse precedes the first data bit. Note how the SELECT pulse of the second data transfer coincides with the last data bit of the first data transfer.

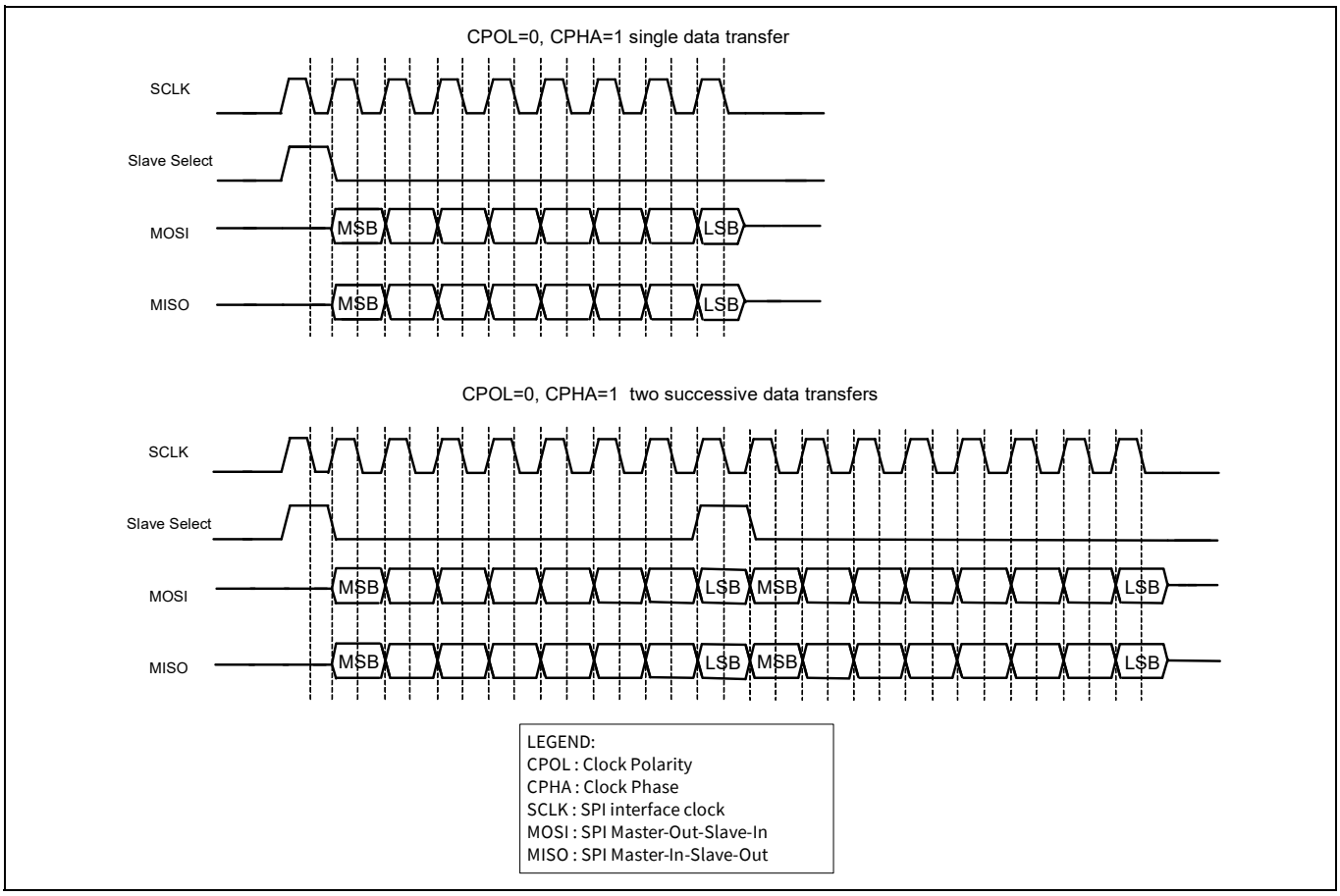


Figure 18-4. SPI TI data transfer example

Figure 18-5 illustrates a single 8-bit data transfer and two successive 8-bit data transfers. The SELECT pulse coincides with the first data bit of a frame.

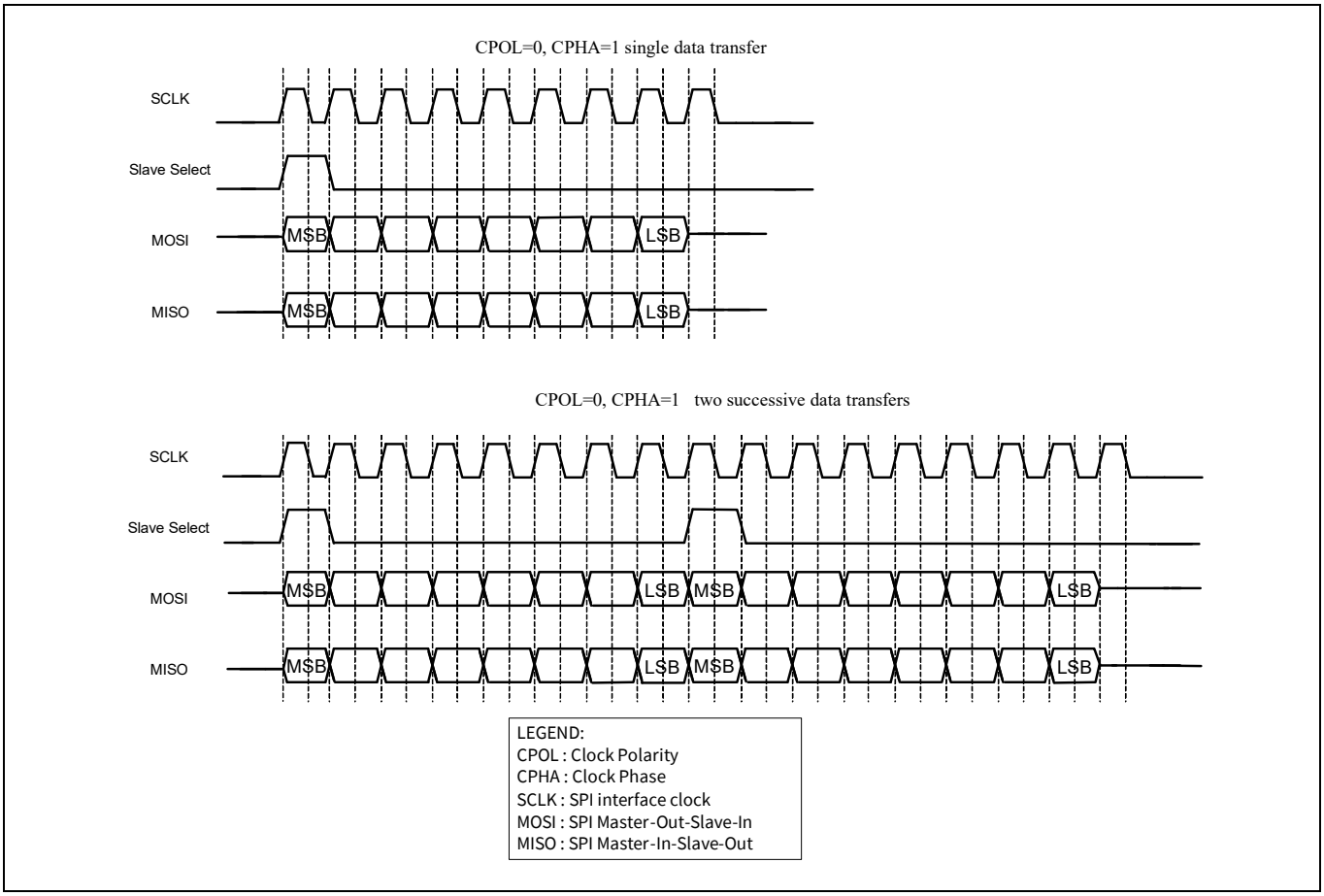


Figure 18-5. SPI TI data transfer example

- **Configuring the SCB for SPI TI mode**

To configure the SCB for SPI TI mode, set various register bits in the following order:

1. Select SPI by writing '01' to the MODE (bits [25:24]) of the SCBx_CTRL register
2. Select SPI TI mode by writing '01' to the MODE (bits [25:24]) of the SCBx_SPI_CTRL register
3. Select the mode of operation in TI by writing to the SELECT_PRECEDE field (bit 1) of the SCBx_SPI_CTRL register ('1' configures the SELECT pulse to precede the first bit of next frame and '0' otherwise)
4. Follow steps 2 to 4 mentioned in **"Enabling and initializing SPI"** on page 79

For more information on these registers, see **[2]**.

18.2.3.3 National Semiconductors SPI

The National Semiconductors' SPI protocol is a half duplex protocol. Rather than transmission and reception occurring at the same time, they take turns. The transmission and reception data sizes may differ. A single "idle" bit transfer period separates transmission from reception. However, the successive data transfers are NOT separated by an "idle" bit transfer period.

The National Semiconductors SPI protocol only supports mode 0 (CPOL is '0' and CPHA is '0'): data is driven on a falling edge of SCLK and data is captured on a rising edge of SCLK.

Figure 18-6 illustrates a single data transfer and two successive data transfers. In both cases the transmission data transfer size is eight bits and the reception data transfer size is four bits.

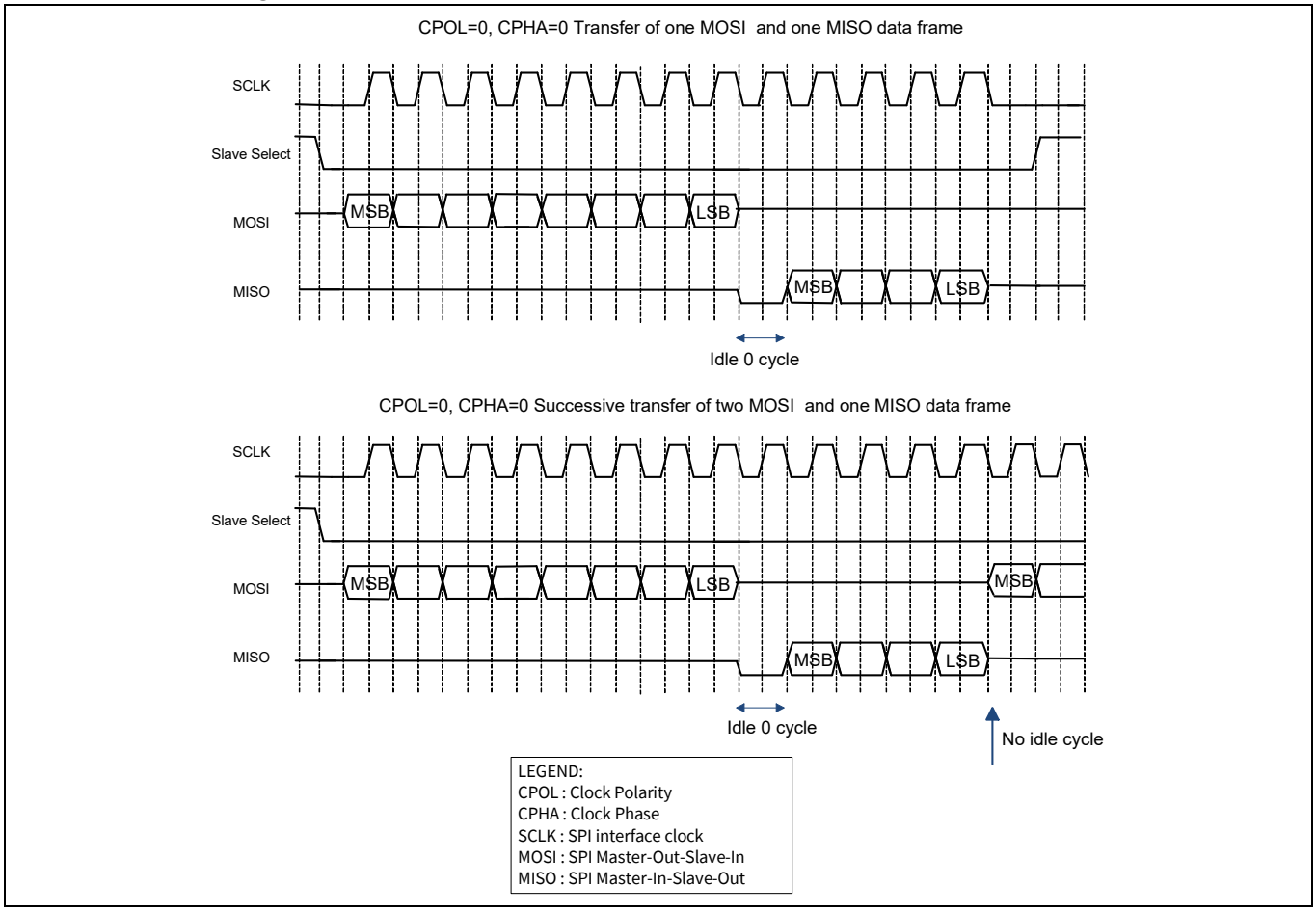


Figure 18-6. SPI NS data transfer example

- **Configuring the SCB for SPI NS mode**

To configure the SCB for SPI NS mode, set various register bits in the following order:

1. Select SPI by writing '01' to the MODE (bits [25:24]) of the SCBx_CTRL register
2. Select SPI NS mode by writing '10' to the MODE (bits [25:24]) of the SCBx_SPI_CTRL register
3. Follow steps 2 to 4 mentioned in **"Enabling and initializing SPI"** on page 79

For more information on these registers, see **[2]**.

18.2.4 Easy SPI (EZSPI) protocol

The easy SPI (EZSPI) protocol is based on the Motorola SPI operating in mode 0 (CPOL is '0' and CPHA is '0'). EZSPI mode is applicable only for slave functionality in a single slave topology. It allows communication between a master and a single slave without the need for CPU intervention at the level of individual frames.

The EZSPI protocol defines an 8-bit EZ address that indexes a memory array (32-entry array of eight bit per entry is supported) located on the slave device. To address these 32 locations, the lower five bits of the EZ address are used. All EZSPI data transfers have 8-bit data frames.

Note: The SCB has a FIFO memory, which is a 16 word by 16-bit SRAM, with byte write enable. The access methods for EZ and non-EZ functions are different. In non-EZ mode, the FIFO is split into TXFIFO and RXFIFO. Each has eight entries of 16 bits per entry. The 16-bit width per entry is used to accommodate configurable data width. In EZ mode, it is used as a single 32x8 bit EZFIFO because only a fixed 8-bit width data is used in EZ mode.

EZSPI has three types of transfers: a write of the EZ address from the master to the slave, a write of data from the master to an addressed slave memory location, and a read by the master from an addressed slave memory location.

18.2.4.1 EZ Address Write

A write of the EZ address starts with a command byte (0x00) on the MOSI line indicating the master's intent to write the EZ address. The slave then drives a reply byte on the MISO line to indicate that the command is observed (0xFE) or not (0xFF). The second byte on the MOSI line is the EZ address.

18.2.4.2 Memory Array Write

A write to a memory array index starts with a command byte (0x01) on the MOSI line indicating the master's intent to write to the memory array. The slave then drives a reply byte on the MISO line to indicate that the command was observed (0xFE) or not (0xFF). Any additional write data bytes on the MOSI line are written to the memory array at locations indicated by the communicated EZ address. The EZ address is automatically incremented by the slave as bytes are written into the memory array. When the EZ address exceeds the maximum number of memory entries (32), it wraps around to 0.

18.2.4.3 Memory Array Read

A read from a memory array index starts with a command byte (0x02) on the MOSI line indicating the master's intent to read from the memory array. The slave then drives a reply byte on the MISO line to indicate that the command was observed (0xFE) or not (0xFF). Any additional read data bytes on the MISO line are read from the memory array at locations indicated by the communicated EZ address. The EZ address is automatically incremented by the slave as bytes are read from the memory array. When the EZ address exceeds the maximum number of memory entries (32), it wraps around to 0.

Figure 18-7 illustrates the write of EZ address, write to a memory array and read from a memory array operations in the EZSPI protocol.

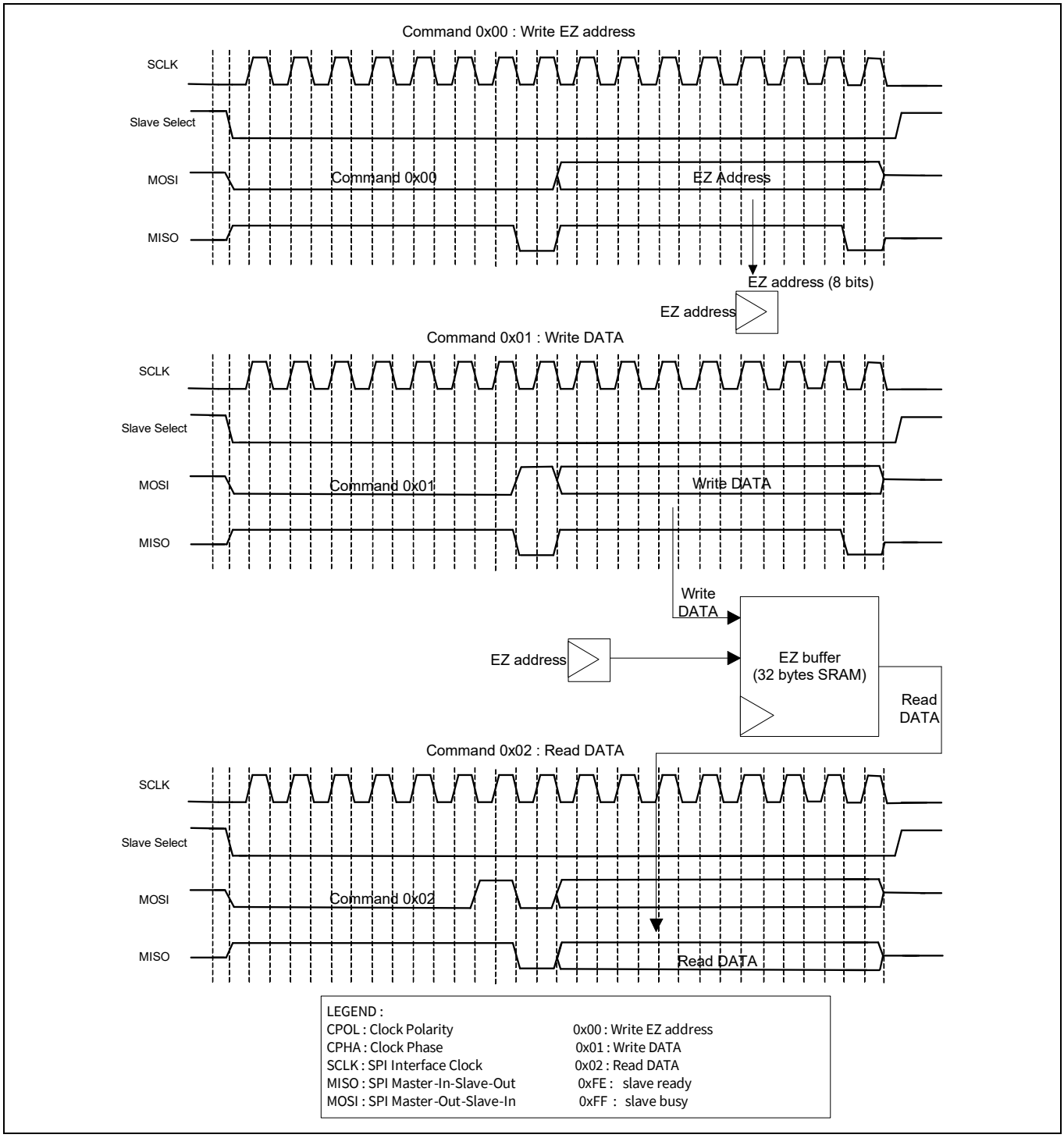


Figure 18-7. EZSPI example

18.2.4.4 Configuring SCB for EZSPI mode

By default, the SCB is configured for non-EZ mode of operation. To configure the SCB for EZSPI mode, set various register bits in the following order:

1. Select EZ mode by writing '1' to the EZ_MODE bit (bit 10) of the SCBx_CTRL register
2. Follow steps 2 to 4 mentioned in **"Enabling and initializing SPI"** on page 79
3. Use continuous transmission mode for transmitter by writing '1' to the CONTINUOUS bit of SCBx_SPI_CTRL register
4. EZSPI mode is applicable only for slave functionality (write '0' to the MASTER_MODE field, bit 31 of SCB_xSPI_CTRL register)
5. Set the data frame width eight bits long (write '0111' to the DATA_WIDTH field, bits [3:0] of SCBx_TX_CTRL and SCBx_RX_CTRL registers)
6. Set the shift direction as MSB first (write '1' to the MSB_FIRST field, bit 8 of SCBx_TX_CTRL and SCBx_RX_CTRL registers)

For more information on these registers, see **[2]**.

18.2.5 SPI registers

The SPI interface is controlled using a set of 32-bit control and status registers listed in **Table 18-1**. For more information on these registers, see **[2]**.

Table 18-1. SPI registers

Register name	Operation
SCBx_CTRL	Enables the SCB, selects the type of serial interface (SPI, UART, I^2C), and selects internally and externally clocked operation, EZ and non-EZ modes of operation.
SCBx_STATUS	In EZ mode, this register indicates whether the externally clocked logic is potentially using the EZ memory.
SCBx_SPI_CTRL	Configures the SPI as either a master or a slave, selects SPI protocols (Motorola, TI, National) and clock-based submodes in Motorola SPI (modes 0,1,2,3), selects the type of SELECT signal in TI SPI.
SCBx_SPI_STATUS	Indicates whether the SPI bus is busy and sets the SPI slave EZ address in the internally clocked mode.
SCBx_TX_CTRL	Enables the transmitter, specifies the data frame width, and specifies whether MSB or LSB is the first bit in transmission.
SCBx_RX_CTRL	Performs the same function as that of the SCBx_TX_CTRL register, but for the receiver.
SCBx_TX_FIFO_CTRL	Specifies the trigger level, clears the transmitter FIFO and shift registers, and performs the FREEZE operation of the transmitter FIFO.
SCBx_RX_FIFO_CTRL	Performs the same function as that of the SCBx_TX_FIFO_CTRL register, but for the receiver.
SCBx_TX_FIFO_WR	Holds the data frame written into the transmitter FIFO. Behavior is similar to that of a PUSH operation.
SCBx_RX_FIFO_RD	Holds the data read from the receiver FIFO. Reading a data frame removes the data frame from the FIFO - behavior is similar to that of a POP operation. This register has a side effect when read by software: a data frame is removed from the FIFO.
SCBx_RX_FIFO_RD_SILENT	Holds the data read from the receiver FIFO. Reading a data frame does not remove the data frame from the FIFO; behavior is similar to that of a PEEK operation.

Table 18-1. SPI registers (continued)

Register name	Operation
SCBx_TX_FIFO_STATUS	Indicates the number of bytes stored in the transmitter FIFO, the location from which a data frame is read by the hardware (read pointer), the location from which a new data frame is written (write pointer), and decides if the transmitter FIFO holds the valid data.
SCBx_RX_FIFO_STATUS	Performs the same function as that of the SCBx_TX_FIFO_STATUS register, but for the receiver.
SCBx_EZ_DATA	Holds the data in EZ memory location

18.2.6 SPI interrupts

The SPI supports both internal and external interrupt requests. The internal interrupt events are listed here.

The SPI predefined interrupts can be classified as TX interrupts and RX interrupts. The TX interrupt output is the logical OR of the group of all possible TX interrupt sources. This signal goes high when any of the enabled TX interrupt sources are true. The RX interrupt output is the logical OR of the group of all possible RX interrupt sources. This signal goes high when any of the enabled RX interrupt sources are true. Various interrupt registers are used to determine the actual source of the interrupt.

The SPI supports interrupts on the following events:

- SPI transfer done
- SPI is Idle
- TX FIFO is not full
- TX FIFO is empty
- SPI Byte/Word transfer complete
- RX FIFO is empty
- RX FIFO is not empty
- Attempt to write to a full RX FIFO.
- RX FIFO is Full

18.2.7 Enabling and initializing SPI

The SPI must be programmed in the following order:

1. Program protocol specific information using the SCBx_SPI_CTRL register, according to **Table 18-2**. This includes selecting the submodes of the protocol and selecting master-slave functionality
2. Program the generic transmitter and receiver information using the SCBx_TX_CTRL and SCBx_RX_CTRL registers, as shown in **Table 18-3**:
   - Specify the data frame width
   - Specify whether MSB or LSB is the first bit to be transmitted/received
   - Enable the transmitter and receiver
3. Program the transmitter and receiver FIFOs using the SCBx_TX_FIFO_CTRL and SCBx_RX_FIFO_CTRL registers respectively, as shown in **Table 18-4**:
   - Set the trigger level
   - Clear the transmitter and receiver FIFO and Shift registers
   - Freeze the TX and RX FIFO
4. Program SCBx_CTRL register to enable the SCB block. Also select the mode of operation. These register bits are shown in **Table 18-5**

Table 18-2. SCBx_SPI_CTRL register

Bits	Name	Value	Description
[25:24]	MODE	00	SPI Motorola submode
		01	SPI Texas Instruments submode
		10	SPI National Semiconductors submode
		11	Reserved
31	MASTER_MODE	0	Slave mode
		1	Master mode

Table 18-3. SCBx_TX_CTRL/SCB_RX_CTRL registers

Bits	Name	Description
[3:0]	DATA_ WIDTH	'DATA_WIDTH + 1' is the number of bits in the transmitted or received data frame. The valid range is [3, 15]. This does not include start, stop, and parity bits.
8	MSB_FIRST	1= MSB first 0= LSB first
31	ENABLED	Transmitter enable bit for SCBx_TX_CTRL and receiver enable bit for SCBx_RX_CTRL registers. They must be enabled for all the protocols. Otherwise, the block may not function or the data may get lost.

Table 18-4. SCBx_TX_FIFO_CTRL/SCB_RX_FIFO_CTRL registers

Bits	Name	Description
[2:0]	TRIGGER_LEVEL	Trigger level. When the transmitter FIFO has less entries or receiver FIFO has more entries than the value of this field, a transmitter or receiver trigger event is generated in the respective case.
16	CLEAR	When '1', the transmitter or receiver FIFO and the shift registers are cleared.
17	FREEZE	When '1', hardware reads/writes to the transmitter or receiver FIFO have no effect. Freeze does not advance the TX or RX FIFO read/write pointer.

Table 18-5. SCBx_CTRL register

Bits	Name	Value	Description
[25:24]	MODE	00	I^2C mode
		01	SPI mode
		10	UART mode
		11	Reserved
31	ENABLED	0	SCB block disabled
		1	SCB block enabled

After the block is enabled, control bits should not be changed. The changes should be made AFTER disabling the block; for example, to modify the operation mode (from Motorola mode to TI mode) or to go from externally to internally clocked operation. The change takes effect only after the block is re-enabled. Note that re-enabling the block causes re-initialization and the associated state is lost (for example, FIFO content).

The last step of initialization should always be to enable the block (write a '1' to the ENABLED bit of the SCBx_CTRL register).

18.2.8 Internally and externally clocked SPI operations

The SCB supports both internally and externally clocked operations for SPI and I^2C functions. An internally clocked operation uses a clock provided by the chip. An externally clocked operation uses a clock provided by the serial interface. Externally clocked operation enables operation in the Deep Sleep system power mode, in which a no-chip internal clock is provided to the block.

Internally clocked operation uses the high-frequency clock of the system. For more information on system clocking, see **"Clocking system"** on page 53. It also supports oversampling. Oversampling is implemented with respect to the high-frequency clock. The OVS (bits [3:0]) of the SCBx_CTRL register specify the oversampling.

In SPI master mode, the valid range for oversampling is 4 to 16. Hence, the maximum bit rate is 12 Mbps. However, if you consider the I/O cell and routing delays, the effective oversampling range becomes 6 to 16. So, the maximum bit rate is 8 Mbps.

Note: LATE_MISO_SAMPLE must be set to '1' in SPIM mode.

In SPI slave mode, the oversampling field (bits [3:0]) of SCBx_CTRL register is not used. However, there is a frequency requirement for the SCB clock with respect to the interface clock (SCLK). This requirement is expressed in terms of the ratio (SCB clock/SCLK). This ratio is dependent on two fields: MEDIAN of SCBx_RX_CTRL register and LATE_MISO_SAMPLE of SCBx_CTRL register. With the MEDIAN bit set to '0' and LATE_MISO_SAMPLE bit set to '1', the SCB can achieve a maximum bit rate of 16 Mbps. However, if you consider the I/O cell and routing delays, the maximum data rate that can be achieved becomes 8 Mbps. Based on these bits, the maximum bit rates are given in **Table 18-6**.

Table 18-6. SPI slave maximum data rates

Median of SCBx_RX_CTRL	LATE_MISO_SAMPLE of SCBx_CTRL	Ratio requirement	Maximum bit rate at peripheral clock of 48 MHz
0	0	≥12	4 Mbps
0	1	≥6	8 Mbps
1	0	≥16	3 Mbps
1	1	≥8	6 Mbps

Externally clocked operation is limited to:

- Slave functionality
- EZ functionality. EZ functionality uses the block's SRAM as a memory structure. Non-EZ functionality uses the block's SRAM as TX and RX FIFOs; FIFO support is not available in externally clocked operation.
- Motorola mode 0 (in the case of SPI slave functionality)

Externally clocked EZ mode of operation can support a data rate of 48 Mbps (at a peripheral clock of 48 MHz).

Internally and externally clocked operation is determined by two register fields of the SCBx_CTRL register:

- **EC_AM_MODE:** Indicates whether SPI slave selection is internally ('0') or externally ('1') clocked. SPI slave selection comprises the first part of the protocol
- **EC_OP_MODE:** Indicates whether the rest of the protocol operation (besides SPI slave selection) is internally ('0') or externally ('1') clocked. As mentioned earlier, externally clocked operation does NOT support non-EZ functionality

These two register fields determine the functional behavior of SPI. The register fields should be set based on the required behavior in Active, Sleep, and Deep Sleep system power mode. Improper setting may result in faulty

behavior in certain system power modes. Table 18-7 and Table 18-8 describe the settings for SPI (in EZ and non-EZ mode).

18.2.8.1 Non-EZ mode of operation

In non-EZ mode there are two possible settings. As externally clocked operation is not supported for non-EZ functionality (no FIFO support), EC_OP_MODE should always be set to '0'. However, EC_AM_MODE can be set to '0' or '1'.

Table 18-7 gives an overview of the possibilities. The combination EC_AM_MODE=0 and EC_OP_MODE=1 is invalid and the block will not respond.

Table 18-7. SPI Non-EZ mode

SPI, Standard (non-EZ) Mode				
	EC_OP_MODE = 0		EC_OP_MODE = 1	
System power mode	**EC_AM_MODE = 0**	**EC_AM_MODE = 1**	**EC_AM_MODE = 1**	**EC_AM_MODE=0**
Active and Sleep	Selection using internal clock. Operation using internal clock.	Selection using external clock: Wakeup interrupt cause is disabled in Active mode (MASK = 0) and in the Sleep mode, the MASK bit can be configured by the user. After that, selection using internal clock. Operation using internal clock.	Not supported	Invalid configuration
Deep Sleep	Not supported	Selection using external clock: Wakeup interrupt cause in enabled (MASK = 1).Generate 0xff bytes.	Not supported	

- **EC_OP_MODE is '0' and EC_AM_MODE is '0'**: This setting only works in Active and Sleep system power modes. The entire block's functionality is provided in the internally clocked domain.
- **EC_OP_MODE is '0' and EC_AM_MODE is '1'**: This setting works in Active and Sleep system power mode and provides limited (wake up) functionality in Deep Sleep system power mode. SPI slave selection is performed by both the internally and externally clocked logic: in Active system power mode both are active and in Deep Sleep system power mode only the externally clocked logic is active. When the externally clocked logic detects slave selection, it sets a wakeup interrupt cause bit, which can be used to generate an interrupt to wake up the CPU.
  - In Active system power mode, the CPU and the block's internally clocked slave selection logic are active and the wakeup interrupt cause is disabled (associated MASK bit is '0'). But in the Sleep mode, wakeup interrupt cause can be either enabled or disabled (MASK bit can be either '1' or '0') based on the application. The remaining operations in the Sleep mode are same as that of the Active mode. The internally clocked logic takes care of the ongoing SPI transfer
  - In Deep Sleep system power mode, the CPU needs to be woken up and the wakeup interrupt cause is enabled (MASK bit is '1'). Waking up takes time, so the ongoing SPI transfer is negatively acknowledged ('1' bits or 0xFF bytes are send out on the MISO line) and the internally clocked logic takes care of the next SPI transfer when it is woken up

18.2.8.2 EZ mode of operation

The EZ mode has three possible settings. EC_AM_MODE can be set to '0' or '1' when EC_OP_MODE is '0' and EC_AM_MODE must be set to '1' when EC_OP_MODE is '1'. **Table 18-8** gives an overview of the possibilities. The gray cells indicate a possible, yet not recommended, setting because it involves a switch from the externally clocked logic (slave selection) to the internally clocked logic (rest of the operation). The combination EC_AM_MODE=0 and EC_OP_MODE=1 is invalid and the block will not respond.

Table 18-8. SPI EZ mode

SPI, EZ mode				
	EC_OP_MODE = 0		**EC_OP_MODE = 1**	
System power mode	**EC_AM_MODE = 0**	**EC_AM_MODE = 1**	**EC_AM_MODE = 1**	**EC_AM_MODE=0**
Active and Sleep	Selection using internal clock. Operation using internal clock.	Selection using external clock: Wakeup interrupt cause is disabled in Active mode (MASK = 0) and in Sleep mode, the mask bit can be configured by the user. After that, selection using internal clock. Operation using internal clock.	Selection using external clock. Operation using external clock.	Invalid configuration
Deep Sleep	Not supported	Selection using external clock: Wakeup interrupt cause is enabled (MASK = 1). Generate 0xff bytes.	Selection using external clock. Operation using external clock.	

- **EC_OP_MODE is '0' and EC_AM_MODE is '0'**: This setting only works in Active system power mode. The entire block's functionality is provided in the internally clocked domain.
- **EC_OP_MODE is '0' and EC_AM_MODE is '1'**: This setting works in Active system power mode and provides limited (wake up) functionality in Deep Sleep system power mode. SPI slave selection is performed by both the internally and externally clocked logic: in Active system power mode both are active and in Deep Sleep system power mode only the externally clocked logic is active. When the externally clocked logic detects slave selection, it sets a wakeup interrupt cause bit, which can be used to generate an interrupt to wake up the CPU.
  - In Active system power mode, the CPU and the block's internally clocked slave selection logic are active and the wakeup interrupt cause is disabled (associated MASK bit is '0'). But in Sleep mode, wakeup interrupt cause can be either enabled or disabled (MASK bit can be either '1' or '0') based on the application. The remaining operations in the Sleep mode are same as that of the Active mode. The internally clocked logic takes care of the ongoing SPI transfer.
  - In Deep Sleep system power mode, the CPU needs to be woken up and the wakeup interrupt cause is enabled (MASK bit is '1'). Waking up takes time, so the ongoing SPI transfer is negatively acknowledged ('1' bits or 0xFF bytes are send out on the MISO line) and the internally clocked logic takes care of the next SPI transfer when it is woken up.
- **EC_OP_MODE is '1' and EC_AM_MODE is '1'**: This setting works in Active system power mode and Deep Sleep system power mode. The SCB functionality is provided in the externally clocked domain. Note that this setting results in externally clocked accesses to the block's SRAM. These accesses may conflict with internally clocked

accesses from the device. This may cause wait states or bus errors. The field FIFO_BLOCK of the SCBx_CTRL register determines whether wait states ('1') or bus errors ('0') are generated.

18.3 Universal asynchronous receiver/transmitter (UART)

The UART protocol is an asynchronous serial interface protocol. UART communication is typically point-to-point. The UART interface consists of two signals:

- TX: Transmitter output
- RX: Receiver input

18.3.1 Features

- Asynchronous transmitter and receiver functionality
- Supports a maximum data rate of 1 Mbps
- Supports UART protocol
  - Standard UART
  - SmartCard (ISO7816) reader
  - IrDA
- Supports Local Interconnect Network (LIN)
  - Break detection
  - Baud rate detection
  - Collision detection (ability to detect that a driven bit value is not reflected on the bus, indicating that another component is driving the same bus)
- Multi-processor mode
- Data frame size programmable from 4 bits to 16 bits.
- Programmable number of STOP bits, which can be set to 1, 1.5, or 2 data bits
- Parity support (odd and even parity)
- Interrupt or polling CPU interface
- Programmable oversampling

18.3.2 General description

Figure 18-8 illustrates a standard UART TX and RX.

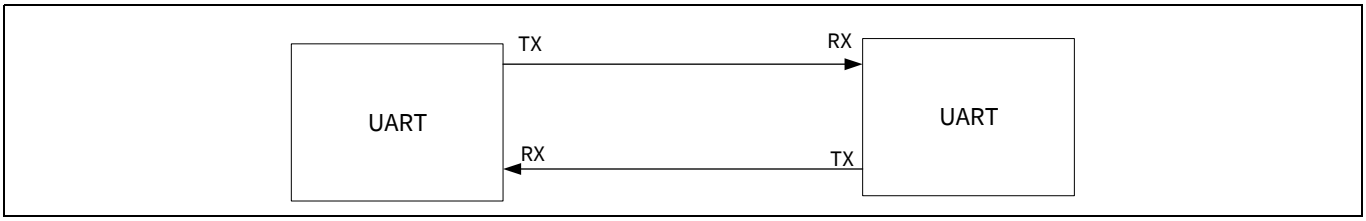


Figure 18-8. UART example

A typical UART transfer consists of a "Start Bit" followed by multiple "Data Bits", optionally followed by a "Parity Bit" and finally completed by one or more "Stop Bits". The Start and Stop bits indicate the start and end of data transmission. The Parity bit is sent by the transmitter and is used be the receiver to detect single bit errors. As the interface does not have a clock (asynchronous), the transmitter and receiver use their own clocks; also, they need to agree upon the period of a bit transfer.

Three different serial interface protocols are supported:

- Standard UART protocol
  - Multi-processor mode
  - Local interconnect network (LIN)
- SmartCard, similar to UART, but with a possibility to send a negative acknowledgment
- IrDA, modification to the UART with a modulation scheme

By default, UART supports a data frame width of eight bits. However, this can be configured to any value in the range of 4 to 9. This does not include start, stop, and parity bits. The number of stop bits can be in the range of 1 to 3. The parity bit can be either enabled or disabled. If enabled, the type of parity can be set to either even parity or odd parity. The option of using the parity bit is available only in the Standard UART and SmartCard UART modes. For IrDA UART mode, the parity bit is automatically disabled. **Figure 18-9** depicts the default configuration of the UART interface of the SCB.

Note: UART interface does not support external clocking operation. Hence, UART operates only in the Active and Sleep system power modes.

18.3.3 UART modes of operation

18.3.3.1 Standard protocol

A typical UART transfer consists of a start bit followed by multiple data bits, optionally followed by a parity bit and finally completed by one or more stop bits. The start bit value is always '0', the data bits values are dependent on the data transferred, the parity bit value is set to a value guaranteeing an even or odd parity over the data bits, and the stop bits value is '1'. The parity bit is generated by the transmitter and can be used by the receiver to detect single bit transmission errors. When not transmitting data, the TX line is '1' – the same value as the stop bits.

Because the interface does not have a clock, the transmitter and receiver need to agree upon the period of a bit transfer. The transmitter and receiver have their own internal clocks. The receiver clock runs at a higher frequency than the bit transfer frequency, such that the receiver may oversample the incoming signal.

The transition of a stop bit to a start bit is represented by a change from '1' to '0' on the TX line. This transition can be used by the receiver to synchronize with the transmitter clock. Synchronization at the start of each data transfer allows error-free transmission even in the presence of frequency drift between transmitter and receiver clocks. The required clock accuracy is dependent on the data transfer size.

The stop period or the amount of stop bits between successive data transfers is typically agreed upon between transmitter and receiver, and is typically in the range of 1 to 3-bit transfer periods.

Figure 18-9 illustrates the UART protocol.

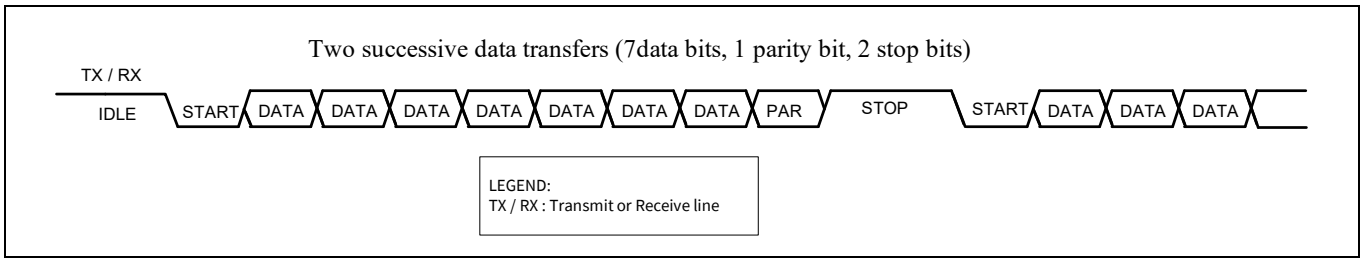


Figure 18-9. UART, standard protocol example

The receiver oversamples the incoming signal; the value of the sample point in the middle of the bit transfer period (on the receiver's clock) is used. **Figure 18-10** illustrates this.

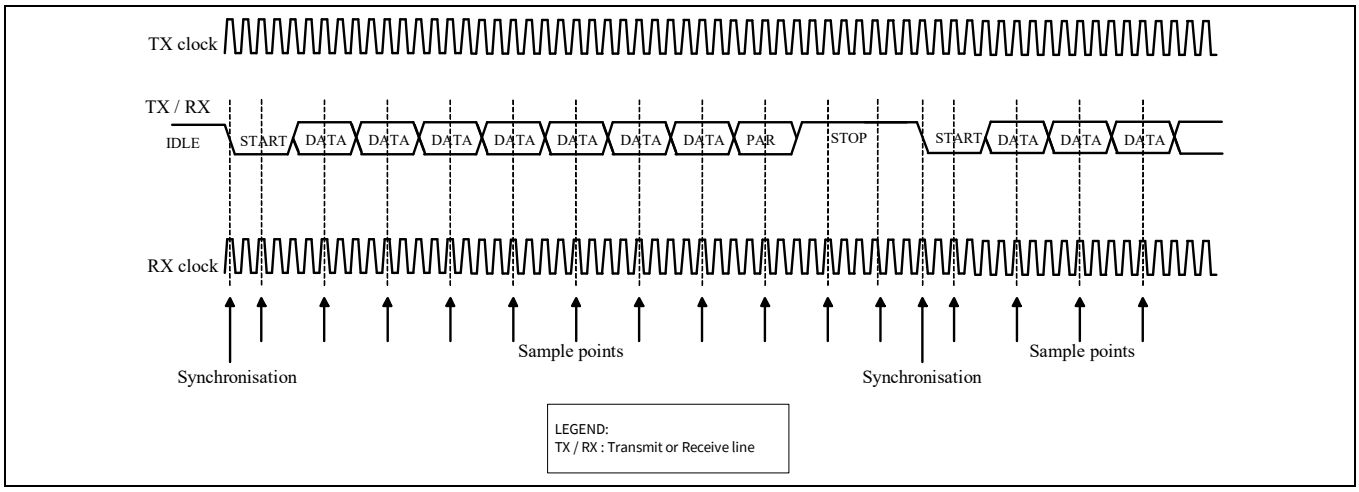


Figure 18-10. UART, standard protocol example (single sample)

Alternatively, three samples around the middle of the bit transfer period (on the receiver's clock) are used for a majority vote to increase accuracy. **Figure 18-11** illustrates this.

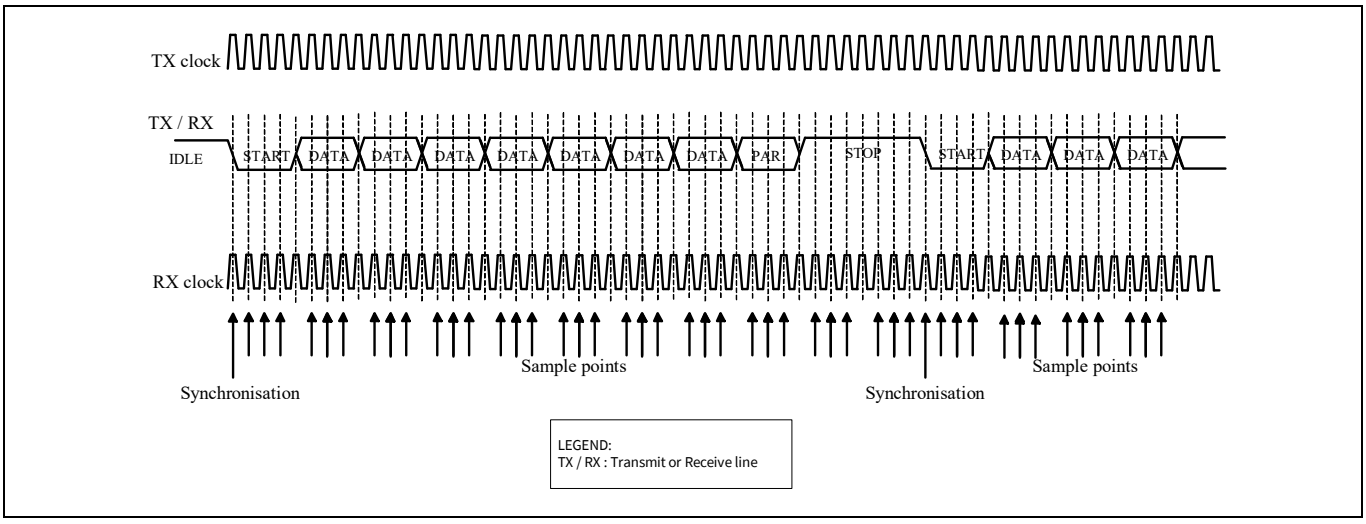


Figure 18-11. UART, standard protocol (multiple samples)

18.3.3.1.1 UART multi-processor mode

The UART_MP (multi-processor) mode is defined with "single-master-multi-slave" topology, as shown in **Figure 18-12**. This mode is also known as UART 9-bit protocol because the data field is nine bits wide. UART_MP is part of Standard UART mode.

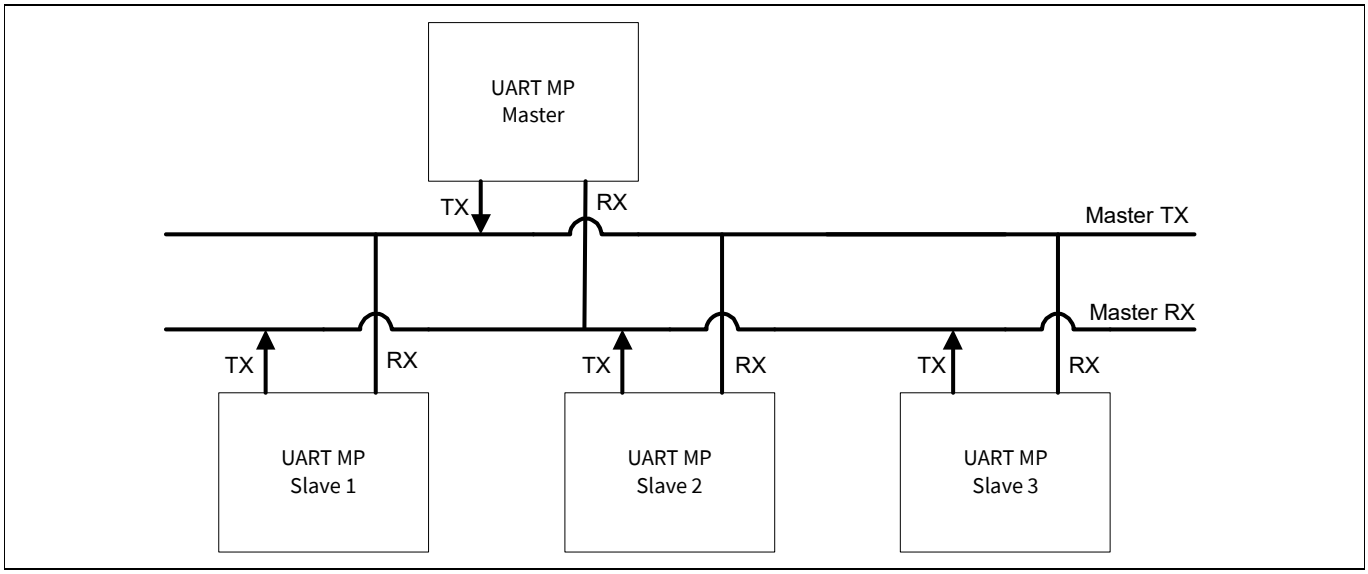


Figure 18-12. UART MP mode bus connections

The main properties of UART_MP mode are:

- Single master with multiple slave concept (multi-drop network)
- Each slave is identified by a unique address
- Using 9-bit data field, with the ninth bit as address/data flag (MP bit). When set high, it indicates an address byte; when set low it indicates a data byte. A data frame is illustrated in **Figure 18-13**
- Parity bit is disabled

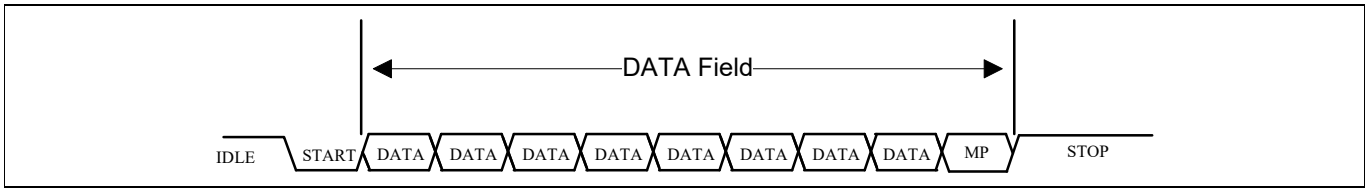


Figure 18-13. UART MP data frame

The SCB can be used as either master or slave device in UART_MP mode. Both SCBx_TX_CTRL and SCBx_RX_CTRL registers should be set to 9-bit data frame size. When the SCB works as UART_MP master device, the firmware changes the MP flag for every address or data frame. When it works as UART_MP slave device, the MP_MODE field of the SCBx_UART_RX_CTRL register should be set to '1'. The SCBx_RX_MATCH register should be set for the slave address and address mask. The matched address is written in the RX_FIFO when ADDR_ACCEPT field of the SCBx_CTRL register is set to '1'. If received address does not match its own address, then the interface ignores the following data, until next address is received for compare.

18.3.3.1.2 UART local interconnect network (LIN) mode

The LIN protocol is supported by the SCB as part of the standard UART. LIN is designed with single master-multi slave topology. There is one master node and multiple slave nodes on the LIN bus. The SCB UART supports both LIN master and slave functionality. **Figure 18-14** illustrates the UART_LIN and LIN Transceiver.

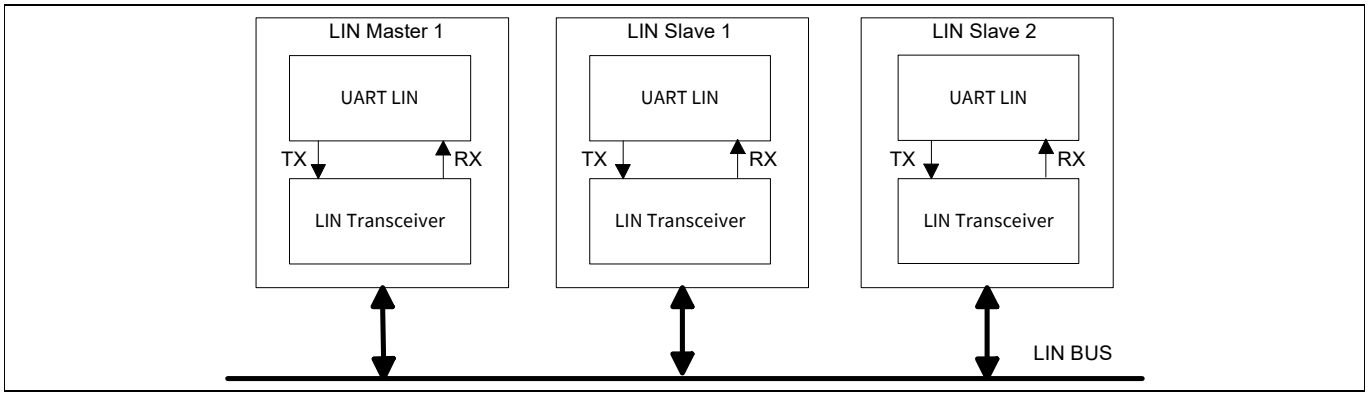


Figure 18-14. UART_LIN and LIN Transceiver

LIN protocol defines two tasks:

- **Master task**: This task involves sending a header packet to initiate a LIN transfer
- **Slave task**: This task involves transmitting or receiving a response

The master node supports master task and slave task; the slave node supports only slave task, as shown in **Figure 18-15**.

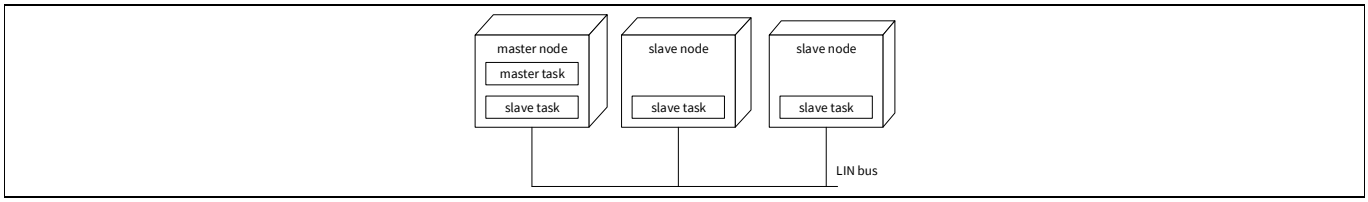


Figure 18-15. LIN bus nodes and tasks

The LIN is based on the transmission of frames at pre-determined moments of time. A frame is divided into header and response fields.

- The header field consists of:
  - Break field (at least 13 bit periods with the value '0')
  - Sync field (a 0x55 byte frame). A sync field can be used to synchronize the clock of the slave task with that of the master task
  - Identifier field (a frame specifying a specific slave)
- The response field consists of data and checksum

The UART LIN of SCB supports slave task, receiving the header and transmitting the response. It provides baud rate detection (using sync field - 0x55) operation. Apart from the break field, a frame transmission (both header and response) consist of one or multiple byte frame transmissions, with each byte transmission consisting of a start bit, 8 data bits and 1 or more stop bits (on both the UART TX and RX lines).

To support LIN, a dedicated (off-chip) line driver/receiver is required. Supply voltage range on the LIN bus is 7 V to 18 V. Typically, LIN line drivers will drive the LIN line with the value provided on the SCB TX line and present the value on the LIN line to the SCB RX line. By comparing TX and RX lines in the SCB, bus collisions can be detected (indicated by the UART_ARB_LOST field of the SCBx_INTR_TX register).

- **Configuring the SCB as Standard UART interface**

To configure the SCB as a standard UART interface, set various register bits in the following order:

1. Configure the SCB as UART interface by writing '10' to the MODE field (bits [25:24]) of the SCBx_CTRL register
2. Configure the UART interface to operate as a Standard protocol by writing '00' to the SCBx_MODE field (bits [25:24]) of the SCBx_UART_CTRL register
3. To enable the UART MP Mode or UART LIN Mode, write '1' to the MP_MODE (bit 11) or LIN_MODE (bit 12) respectively of the SCBx_UART_RX_CTRL register
4. Follow steps 2 to 4 described in **"Enabling and initializing UART"** on page 92

For more information on these registers, see **[2]**.

18.3.3.2 SmartCard (ISO7816)

ISO7816 is asynchronous serial interface, defined with single-master-single slave topology. ISO7816 defines both Reader (master) and Card (slave) functionality. For more information, refer to the **ISO7816 Specification**. Only master (reader) function is supported by the SCB. This block provides the basic physical layer support with asynchronous character transmission. UART_TX line is connected to SmartCard IO line, by internally multiplexing between UART_TX and UART_RX control modules.

The SmartCard transfer is similar to a UART transfer, with the addition of a negative acknowledgment (NACK) that may be sent from the receiver to the transmitter. A NACK is always '0'. Both master and slave may drive the same line, although never at the same time.

A SmartCard transfer has the transmitter drive the start bit and data bits (and optionally a parity bit). After these bits, it enters its stop period by releasing the bus. Releasing results in the line being '1' (the value of a stop bit). After one bit transfer period into the stop period, the receiver may drive a NACK on the line (a value of '0') for one bit transfer period. This NACK is observed by the transmitter, which reacts by extending its stop period by one bit transfer period. For this protocol to work, the stop period should be longer than one bit transfer period. Note that a data transfer with a NACK takes one bit transfer period longer, than a data transfer without a NACK. Typically, implementations use a tristate driver with a pull-up resistor, such that when the line is not transmitting data or transmitting the Stop bit, its value is '1'.

Figure 18-16 illustrates the SmartCard protocol.

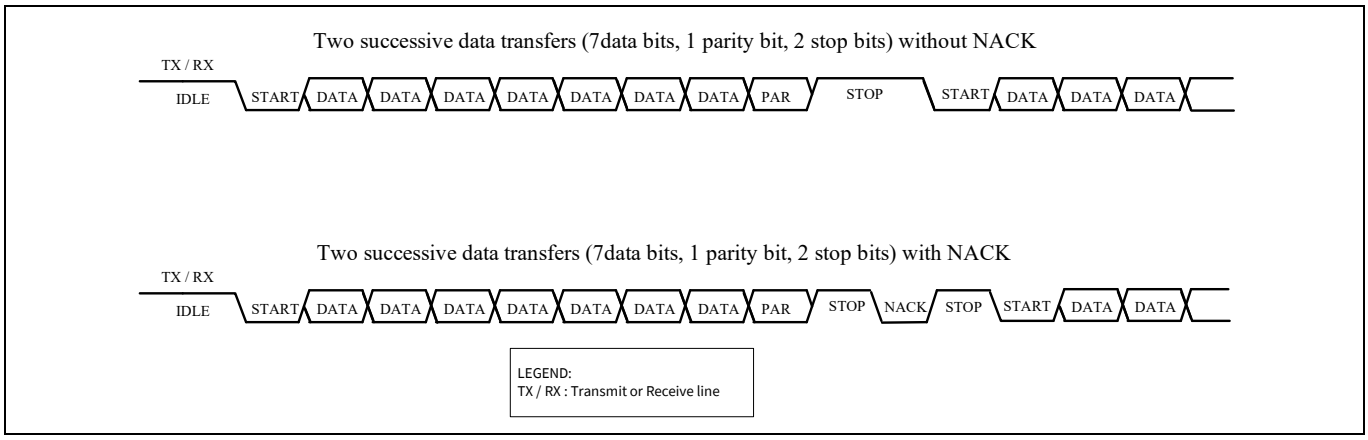


Figure 18-16. SmartCard example

The communication Baud rate for ISO7816 is given as:

Baud rate= f7816 × (D/F)

Where f7816 is the clock frequency, F is the clock rate conversion integer, and D is the baud rate adjustment integer.

By default, F = 372, D = f1, and the maximum clock frequency is 5 MHz. Thus, maximum baud rate is 13.4 Kbps. Typically, a 3.57-MHz clock is selected. The typical value of the baud rate is 9.6 Kbps.

- **Configuring SCB as UART SmartCard Interface**

To configure the SCB as a UART SmartCard interface, set various register bits in the following order. For more information on these registers, see **[2]**

1. Configure the SCB as UART interface by writing '10' to the MODE (bits [25:24]) of the SCBx_CTRL register.
2. Configure the UART interface to operate as a SmartCard protocol by writing '01' to the MODE (bits [25:24]) of the SCBx_UART_CTRL register
3. Follow steps 2 to 4 described in **"Enabling and initializing UART"** on page 92

18.3.3.3 IrDA

The SCB supports the Infrared Data Association (IrDA) protocol for data rates of up to 115.2 Kbps using the UART interface. It supports only the basic physical layer of IrDA protocol with rates less than 115.2 Kbps. Hence, the system instantiating this block must consider how to implement a complete IrDA communication system with other available system resources.

The IrDA protocol adds a modulation scheme to the UART signaling. At the transmitter, bits are modulated. At the receiver, bits are demodulated. The modulation scheme uses a Return-to-Zero-Inverted (RZI) format. A bit value of '0' is signaled by a short '1' pulse on the line and a bit value of '1' is signaled by holding the line to '0'. For these data rates (<=115.2 Kbps), the RZI modulation scheme is used and the pulse duration is 3/16 of the bit period. The sampling clock frequency should be set 16 times the selected baud rate, by configuring the OVS field of the SCBx_CTRL register.

Different communication speeds under 115.2 Kbps can be achieved by configuring corresponding block clock frequency. Additional allowable rates are 2.4 Kbps, 9.6 Kbps, 19.2 Kbps, 38.4 Kbps, and 57.6 Kbps. An IrDA serial infrared interface operates at 9.6 Kbps. **Figure 18-17** shows how a UART transfer is IrDA modulated.

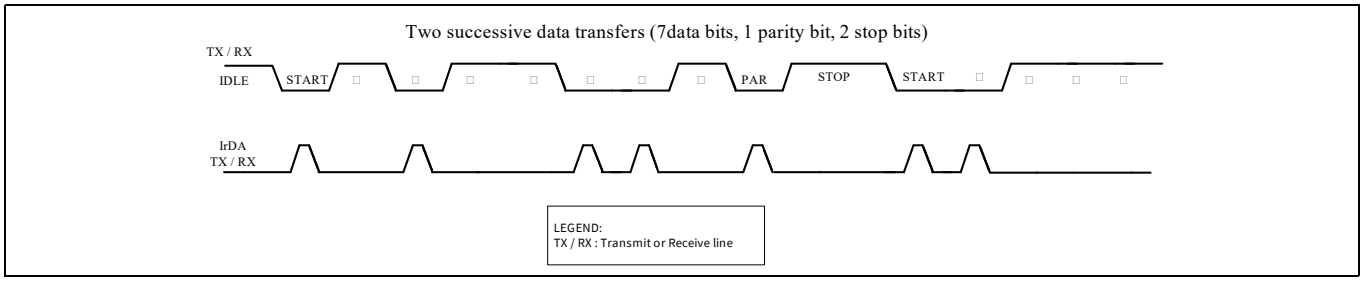


Figure 18-17. IrDA example

- **Configuring the SCB as UART IrDA interface**

To configure the SCB as a UART IrDA interface, set various register bits in the following order. For more information on these registers, see **[2]**.

1. Configure the SCB as UART interface by writing '10' to the MODE (bits [25:24]) of the SCBx_CTRL register
2. Configure the UART interface to operate as IrDA protocol by writing '10' to the MODE (bits [25:24]) of the SCBx_UART_CTRL register
3. Configure the SCB as described in **"Enabling and initializing UART"** on page 92

18.3.4 UART registers

The UART interface is controlled using a set of 32-bit registers listed in **Table 18-9**. For more information on these registers, see **[2]**.

Table 18-9. UART registers

Register name	Operation
SCBx_UART_CTRL	Used to select the sub-modes of UART (standard UART, SmartCard, IrDA), also used for local loop back control.
SCBx_UART_STATUS	Used to specify the BR_COUNTER value that determines the bit period.
SCBx_UART_TX_CTRL	Used to specify the number of stop bits, enable parity, select the type of parity, and enable retransmission on NACK.
SCBx_UART_RX_CTRL	Performs same function as SCBx_UART_TX_CTRL but is also used for enabling multi processor mode, LIN mode drop on parity error, and drop on frame error.
SCBx_TX_CTRL	Used to enable the transmitter, also to specify the data frame width and to specify whether MSB or LSB is the first bit in transmission.
SCBx_RX_CTRL	Performs the same function as that of the SCBx_TX_CTRL register, but for the receiver.

18.3.5 UART interrupts

The UART supports both internal and external interrupt requests. The internal interrupt events are listed in this section.

The UART predefined interrupts can be classified as TX interrupts and RX interrupts. The TX interrupt output is the logical OR of the group of all possible TX interrupt sources. This signal goes high when any of the enabled TX interrupt sources are true. The RX interrupt output is the logical OR of the group of all possible RX interrupt sources. This signal goes high when any of the enabled RX interrupt sources are true. The UART provides interrupts on the following events:

- UART transmission done.
- UART TX received a NACK in SmartCard mode
- UART arbitration lost (in LIN or SmartCard modes)
- Frame error in received data frame
- Parity error in received data frame
- LIN baud rate detection is completed
- LIN break detection is successful

18.3.6 Enabling and initializing UART

The UART must be programmed in the following order:

1. Program protocol specific information using the SCBx_UART_CTRL register, according to **Table 18-10**. This includes selecting the submodes of the protocol, transmitter-receiver functionality, and so o
2. Program the generic transmitter and receiver information using the SCBx_TX_CTRL and SCBx_RX_CTRL registers, as shown in **Table 18-11**
   a) Specify the data frame width
   b) Specify whether MSB or LSB is the first bit to be transmitted or received
   c) Enable the transmitter and receiver
3. Program the transmitter and receiver FIFOs using the SCBx_TX_FIFO_CTRL and SCBx_RX_FIFO_CTRL registers respectively, as shown in **Table 18-12**
   a) Set the trigger level
   b) Clear the transmitter and receiver FIFO and Shift registers
   c) Freeze the TX and RX FIFOs
4. Program the SCBx_CTRL register to enable the SCB block. Also select the mode of operation, as shown in **Table 18-13**

Table 18-10. SCBx_UART_CTRL register

Bits	Name	Value	Description
[25:24]	MODE	00	Standard UART
		01	SmartCard
		10	IrDA
		11	Reserved
16	LOOP_BACK	Loop back control. This allows a SCB UART transmitter to communicate with its receiver counteart.	

Table 18-11. SCBx_TX_CTRL/SCBx_RX_CTRL registers

Bits	Name	Description
[3:0]	DATA_ WIDTH	'DATA_WIDTH + 1' is the no. of bits in the transmitted or received data frame. The valid range is [3, 15]. This does not include start, stop, and parity bits.
8	MSB_FIRST	1= MSB first 0= LSB first
31	ENABLED	Transmitter enable bit for SCBx_TX_CTRL and receiver enable bit for SCBx_RX_CTRL registers. They must be enabled for all the protocols. Otherwise, the block may not function or the data may get lost.

Table 18-12. SCBx_TX_FIFO_CTRL/SCBx_RX_FIFO_CTRL registers

Bits	Name	Description
[2:0]	TRIGGER_LEVEL	Trigger level. When the transmitter FIFO has less entries or receiver FIFO has more entries than the value of this field, a transmitter or receiver trigger event is generated in the respective case.
16	CLEAR	When '1', the transmitter or receiver FIFO and the shift registers are cleared/invalidated.
17	FREEZE	When '1', hardware reads/writes to the transmitter or receiver FIFO have no effect. Freeze will not advance the TX or RX FIFO read/write pointer.

Table 18-13. SCBx_CTRL register

Bits	Name	Value	Description
[25:24]	MODE	00	I^2C mode
		01	SPI mode
		10	UART mode
		11	Reserved
31	ENABLED	0	SCB block enabled
		1	SCB block disabled

After the block is enabled, control bits should not be changed. Changes should be made AFTER disabling the block; for example, to modify the operation mode (from SmartCard to IrDA). The change takes effect only after the block is re-enabled. Note that re-enabling the block causes re-initialization and the associated state is lost (for example FIFO content).

The last step of initialization should always be to enable the block (write a '1' to the ENABLED bit of the SCBx_CTRL register).

18.4 Inter integrated cCircuit (I^2C)

EZ-PD™ PMG1-S0 MCU contains a Serial Communication Block (SCB) configured to operate only as a I^2C block. This section explains the I^2C implementation in EZ-PD™ PMG1-S0 MCU. For more information on the I^2C protocol specification, see the I^2C-bus specification available on the **NXP website**.

18.4.1 Features

EZ-PD™ PMG1-S0 MCU supports the following I^2C features:

- Master, slave, and master/slave mode
- Slow-mode (50 kbps), standard-mode (100 kbps), fast-mode (400 kbps), and fast-mode plus (1000 kbps) data-rates
- 7- or 10-bit slave addressing (10-bit addressing requires firmware support)
- Clock stretching and collision detection
- Programmable oversampling of I^2C clock signal (SCL)
- Error reduction using an digital median filter on the input path of the I^2C data signal (SDA)
- Glitch-free signal transmission with an analog glitch filter
- Interrupt or polling CPU interface
- Supports EZ mode of operation (Easy I^2C (EZI^2C) Protocol - applicable only for I^2C slave functionality)

18.4.2 General description

Figure 18-18 illustrates an example of an I²C communication network.

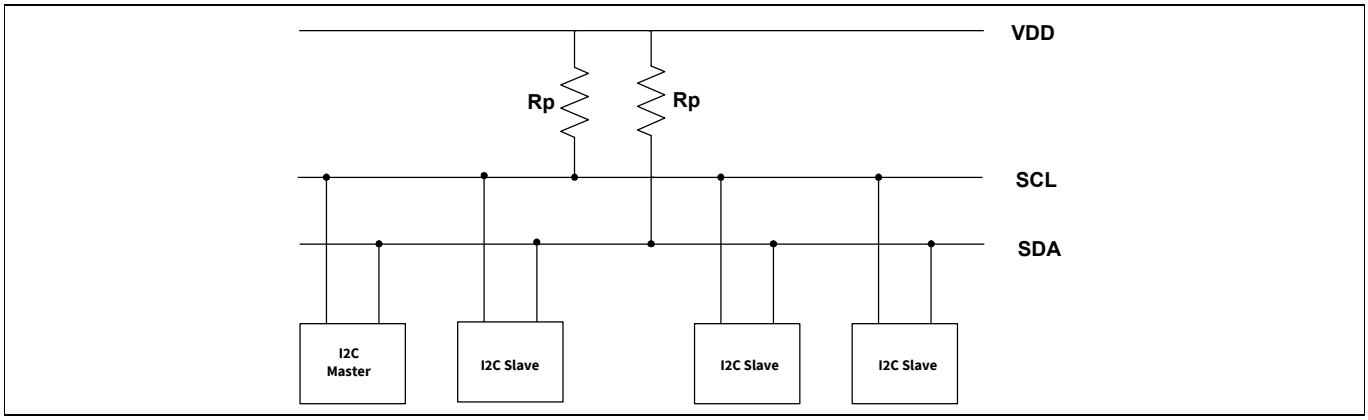


Figure 18-18. I²C interface block diagram

The standard I²C bus is a two wire interface with the following lines:

- Serial Data (SDA)
- Serial Clock (SCL)

I²C devices are connected to these lines using open collector or open-drain output stages, with pull-up resistors. A simple master/slave relationship exists between devices. Masters and slaves can operate as either transmitter or receiver. Each slave device connected to the bus is software addressable by a unique 7-bit address.

18.4.3 Terms and definitions

Table 18-14 explains the commonly used terms in an I²C communication network.

Table 18-14. Definition of I²C bus terminology

Term	Description
Transmitter	The device that sends data to the bus
Receiver	The device that receives data from the bus
Master	The device that initiates a transfer, generates clock signals, and terminates a transfer
Slave	The device addressed by a master
Multi-master	More than one master can attempt to control the bus at the same time without corrupting the message
Arbitration	Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the winning message is not corrupted
Synchronization	Procedure to synchronize the clock signals of two or more devices

- **Bus stalling (clock stretching)**

When a slave device is not yet ready to process data, it may drive a ‘0’ on the SCL line to hold it down. Due to the implementation of the I/O signal interface, the SCL line value will be '0', independent of the values that any other master or slave may be driving on the SCL line. This is known as clock stretching and is the only situation in which a slave drives the SCL line. The master device monitors the SCL line and detects it when it cannot generate a positive clock pulse ('1') on the SCL line. It then reacts by postponing the generation of a positive edge on the SCL line, effectively synchronizing with the slave device that is stretching the clock.

- **Bus arbitration**

The I²C protocol is a multi-master, multi-slave interface. Bus arbitration is implemented on master devices by monitoring the SDA line. Bus collisions are detected when the master observes an SDA line value that is not the same as the value it is driving on the SDA line. For example, when master 1 is driving the value '1' on the SDA line and master 2 is driving the value '0' on the SDA line, the actual line value will be '0' due to the implementation of the I/O signal interface. Master 1 detects the inconsistency and loses control of the bus. Master 2 does not detect any inconsistency and keeps control of the bus.

18.4.4 I²C modes of operation

I²C is a synchronous single master, multi-master, multi-slave serial interface. Devices operate in either master mode, slave mode, or master/slave mode. In master/slave mode, the device switches from master to slave mode when it is addressed. Only a single master may be active during a data transfer. The active master is responsible for driving the clock on the SCL line. **Table 18-15** illustrates the I²C modes of operation.

Table 18-15. I²C modes

Mode	Description
Slave	Slave only operation (default)
Master	Master only operation
Multi-master	Supports more than one master on the bus
Multi-master-slave	Simultaneous slave and multi-master operation

Data transfer through the I²C bus follows a specific format. **Table 18-16** lists some common bus events that are part of an I²C data transfer. The **"Write transfer"** on page 96 and **"Read transfer"** on page 97 sections explain the format of bits on an I²C bus during data transfer.

Table 18-16. I²C bus events terminology

Bus Event	Description
START	A HIGH to LOW transition on the SDA line while SCL is HIGH
STOP	A LOW to HIGH transition on the SDA line while SCL is HIGH
ACK	The receiver pulls the SDA line LOW and it remains LOW during the HIGH period of the clock pulse after the transmitter transmits each byte.
NACK	The receiver does not pull the SDA line LOW and it remains HIGH during the HIGH period of clock pulse after the transmitter transmits each byte.
Repeated START	START condition generated by master at the end of a transfer instead of a STOP condition

When operating in multi-master mode, the bus should always be checked to see if it is busy; another master may already be communicating with a slave. In this case, the master must wait until the current operation is complete before issuing a START signal (see **Table 18-16**, **Table 18-19** and **Table 18-20**). The master looks for a STOP signal as an indicator that it can start its data transmission.

When operating in multi-master-slave mode, if the master loses arbitration during data transmission, the hardware reverts to slave mode and the received byte generates a slave address interrupt.

With all of these modes, there are two types of transfer - read and write. In write transfer, the master sends data to slave; in read transfer, the master receives data from slave. Write and read transfer examples are available in **"Master mode transfer examples"** on page 104, **"Slave mode transfer examples"** on page 106, and **"Multi-master mode transfer example"** on page 110.

18.4.4.1 Write transfer

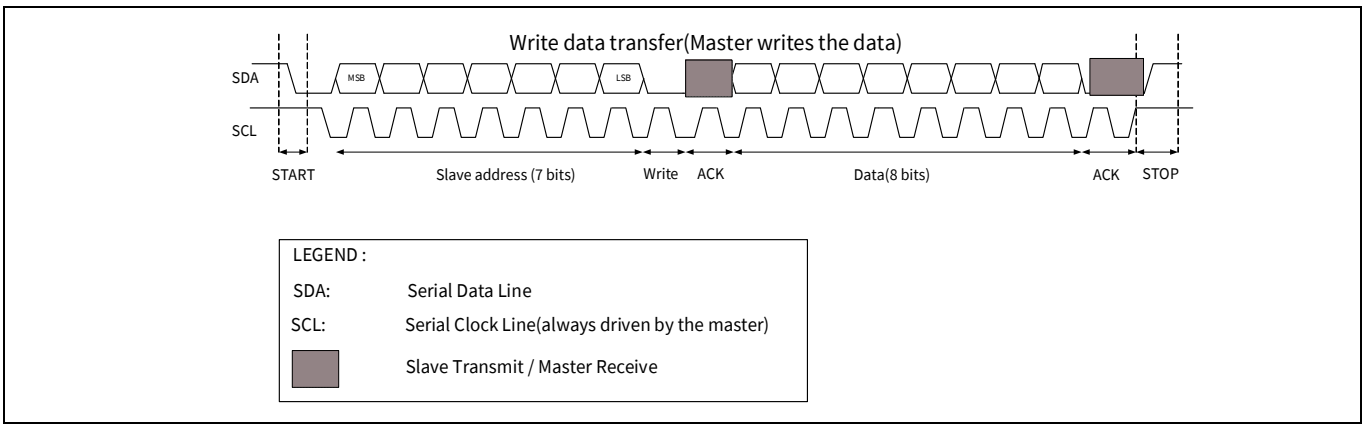


Figure 18-19. Master write data transfer

- A typical write transfer begins with the master generating a START condition on the I^2C bus. The master then writes a 7-bit I^2C slave address and a write indicator ('0') after the START condition. The addressed slave transmits an acknowledgment byte by pulling the data line low during the ninth bit time
- If the slave address does not match any of the slave devices or if the addressed device does not want to acknowledge the request, it transmits a no acknowledgment (NACK). The absence of an acknowledgment, results in an SDA line value of '1' due to the pull-up resistor implementation
- If no acknowledgment is transmitted by the slave, the master may end the write transfer with a STOP event. The master can also generate a repeated START condition for a retry attempt
- The master may transmit write data to the bus if it receives an acknowledgment. The addressed slave transmits an acknowledgment to confirm the receipt of the write data. Upon receipt of this acknowledgment, the master may transmit another data byte
- When the transfer is complete, the master generates a STOP condition

18.4.4.2 Read transfer

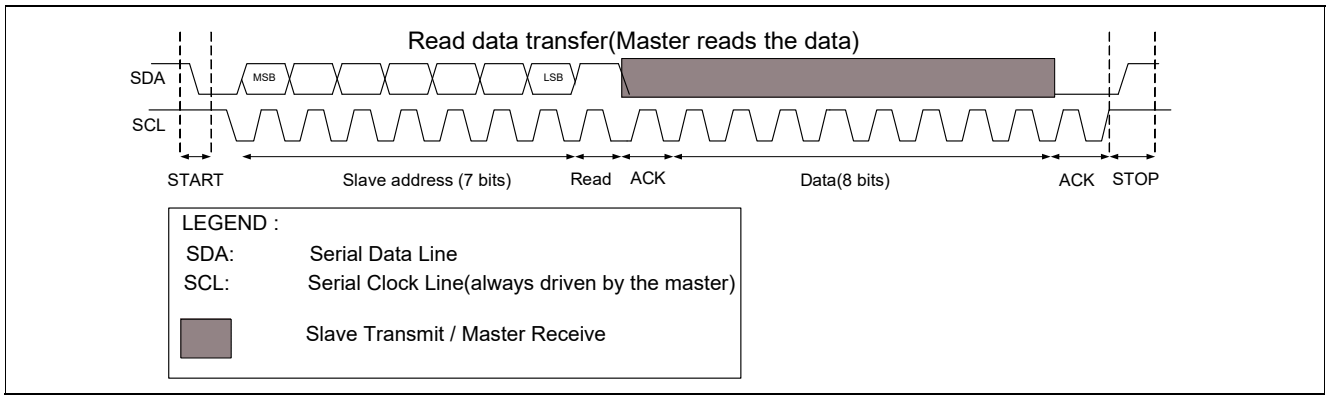


Figure 18-20. Master read data transfer

- A typical read transfer begins with the master generating a START condition on the I²C bus. The master then writes a 7-bit I²C slave address and a read indicator ('1') after the START condition. The addressed slave transmits an acknowledgment by pulling the data line low during the ninth bit time
- If the slave address does not match with that of the connected slave device or if the addressed device does not want to acknowledge the request, a no acknowledgment (NACK) is transmitted. The absence of an acknowledgment, results in an SDA line value of '1' due to the pull-up resistor implementation
- If no acknowledgment is transmitted by the slave, the master may end the read transfer with a STOP event. The master can also generate a repeated START condition for a retry attempt
- If the slave acknowledges the address, it starts transmitting data after the acknowledgment signal. The master transmits an acknowledgment to confirm the receipt of each data byte sent by the slave. Upon receipt of this acknowledgment, the addressed slave may transmit another data byte
- The master can send a NACK signal to the slave to stop the slave from sending data bytes. This completes the read transfer
- When the transfer is complete, the master generates a STOP condition

18.4.5 Easy I²C (EZI²C) protocol

The Easy I²C (EZI²C) protocol is a unique communication scheme built on top of the I²C protocol by Cypress. EZI²C mode is applicable only for slave functionality. It uses a software wrapper around the standard I²C protocol to communicate to an I²C slave using indexed memory transfers. This removes the need for CPU intervention at the level of individual frames.

The EZI²C protocol defines an 8-bit EZ address that indexes a memory array (8-bit wide 32 locations) located on the slave device. Five lower bits of the EZ address is used to address these 32 locations. The number of bytes transferred to or from the EZI²C memory array can be found by comparing the EZ address at the START event and the EZ address at the STOP event.

Note: The I²C block has a hardware FIFO memory, which is 16 bits wide and 16 locations deep with byte write enable. The access methods for EZ and non-EZ functions are different. In non-EZ mode, the FIFO is split into TXFIFO and RXFIFO. Each has 16-bit wide eight locations. In EZ mode, the FIFO is used as a single memory unit with 8-bit wide 32 locations.

EZI²C has two types of transfers: an EZ write of data from the master to an addressed slave memory location, and a read by the master from an addressed slave memory location.

18.4.6 Memory array write

An EZ write to a memory array index is by means of an I²C write transfer. The first transmitted write data is used to send an EZ address from the master to the slave. The five lowest significant bits of the write data are used as the "new" EZ address at the slave. Any additional write data elements in the write transfer are bytes that are written to the memory array. The EZ address is automatically incremented by the slave as bytes are written into the memory array. When the EZ address exceeds 32 memory entries, it wraps around to 0.

18.4.7 Memory array read

An EZ read from a memory array index is by means of an I²C read transfer. The EZ read relies on an earlier EZ write to have set the EZ address at the slave. The first received read data is the byte from the memory array at the EZ address memory location. The EZ address is automatically incremented as bytes are read from the memory array. When the EZ address exceeds the 32 memory entries, it wraps around to '0'.

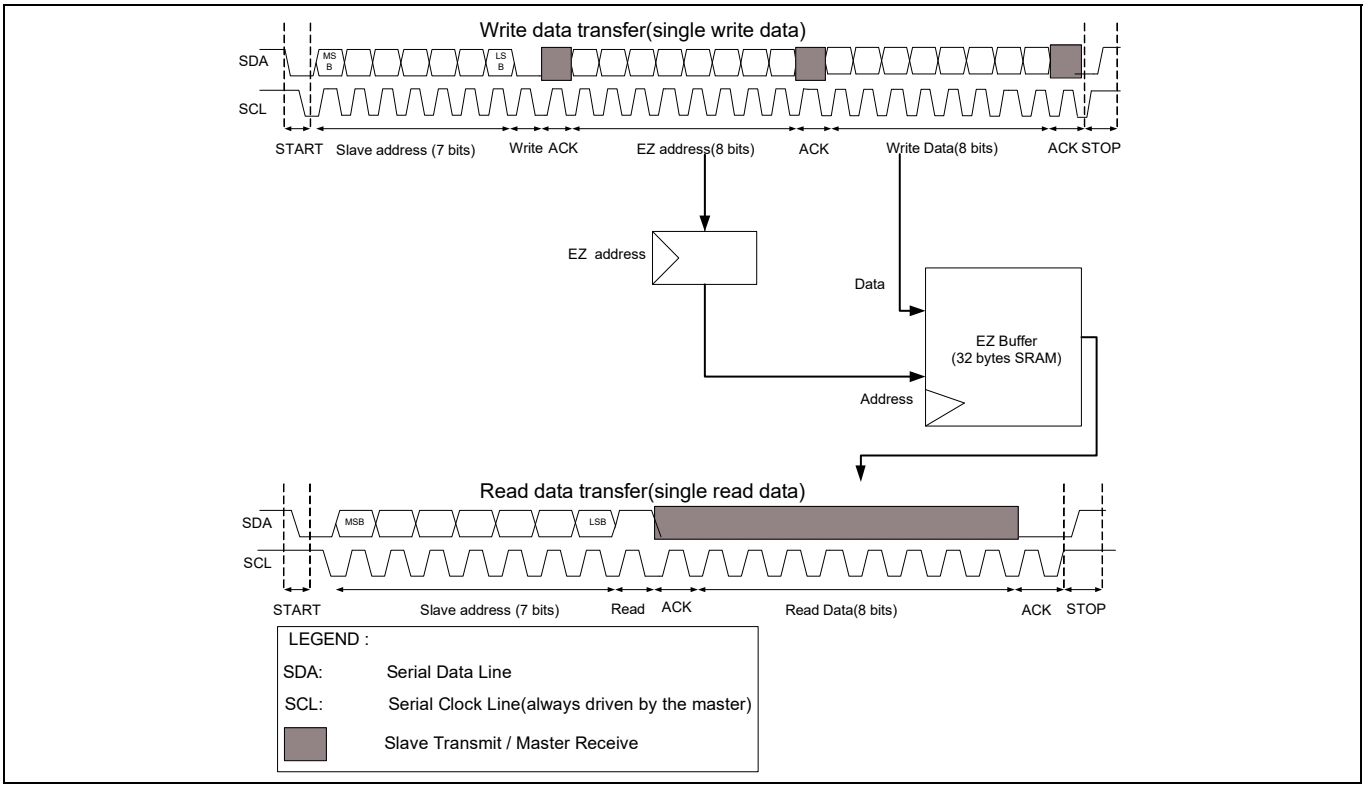


Figure 18-21. EZI²C write and read data transfer

See **"EZ slave mode transfer example"** on page 108 for examples.

18.4.8 I²C registers

The I²C interface is controlled by reading and writing a set of configuration, control, and status registers, as listed in **Table 18-22**.

Figure 18-22. I²C registers

Register name	Function
SCBx_CTRL	Enables the SCB block and selects the type of serial interface (SPI, UART, I²C). Also used to select internally and externally clocked operation and EZ and non-EZ modes of operation.
SCBx_I2C_CTRL	Selects the mode (master, slave) and sends an ACK or NACK signal based on receiver FIFO status.
SCBx_I2C_STATUS	Indicates bus busy status detection, read/write transfer status of the slave/master, and stores the EZ slave address.
SCBx_I2C_M_CMD	Enables the master to generate START, STOP, and ACK/NACK signals.
SCBx_I2C_S_CMD	Enables the slave to generate ACK/NACK signals.
SCBx_STATUS	Indicates whether the externally clocked logic is using the EZ memory. This bit can be used by software to determine whether it is safe to issue a software access to the EZ memory.
SCBx_TX_CTRL	Enables the transmitter and specifies the data frame width; also used to specify whether MSB or LSB is the first bit in transmission.
SCBx_TX_FIFO_CTRL	Specifies the trigger level, clearing of the transmitter FIFO and shift registers, and FREEZE operation of the transmitter FIFO.
SCBx_TX_FIFO_STATUS	Indicates the number of bytes stored in the transmitter FIFO, the location from which a data frame is read by the hardware (read pointer), the location from which a new data frame is written (write pointer), and decides if the transmitter FIFO holds the valid data.
SCBx_TX_FIFO_WR	Holds the data frame written into the transmitter FIFO. Behavior is similar to that of a PUSH operation.
SCBx_RX_CTRL	Performs the same function as that of the SCBx_TX_CTRL register, but for the receiver.
SCBx_RX_FIFO_CTRL	Performs the same function as that of the SCBx_TX_FIFO_CTRL register, but for the receiver.
SCBx_RX_FIFO_STATUS	Performs the same function as that of the SCBx_TX_FIFO_STATUS register, but for the receiver.
SCBx_RX_FIFO_RD	Holds the data read from the receiver FIFO. Reading a data frame removes the data frame from the FIFO; behavior is similar to that of a POP operation. This register has a side effect when read by software: a data frame is removed from the FIFO.
SCBx_RX_FIFO_RD_SILENT	Holds the data read from the receiver FIFO. Reading a data frame does not remove the data frame from the FIFO; behavior is similar to that of a PEEK operation.
SCBx_RX_MATCH	Stores slave device address and is also used as slave device address MASK.
SCBx_EZ_DATA	Holds the data in an EZ memory location.

*Note: For detailed descriptions of the I²C register bits, see **[2]**.*

18.4.9 I²C interrupts

The I²C block generates interrupts for the following conditions.

- Arbitration lost
- Slave address match
- I²C bus stop/start condition detected
- I²C bus error detected
- I²C byte/word transfer complete
- I²C TX FIFO not full
- I²C TX FIFO empty
- I²C RX FIFO empty
- I²C RX FIFO not empty
- I²C RX FIFO overrun
- I²C RX FIFO full

The I²C interrupt signal is hard-wired to the Arm® Cortex®-M0 NVIC and cannot be routed to external pins.

The interrupt output is the logical OR of the group of all possible interrupt sources. The interrupt is triggered when any of the enabled interrupt conditions are met. Interrupt status registers are used to determine the actual source of the interrupt. For more information on interrupt registers, see the EZ-PD™ PMG1-S0 MCU Registers TRM.

18.4.10 Enabling and initializing the I²C

The following section describes the method to configure the I²C block for standard (non-EZ) mode and EZI²C mode.

- **Configuring for I²C Standard (Non-EZ) mode**

The I²C interface must be programmed in the following order.

1. Program protocol specific information using the SCBx_I2C_CTRL register according to **Table 18-17**. This includes selecting master - slave functionality
2. Program the generic transmitter and receiver information using the SCBx_TX_CTRL and SCBx_RX_CTRL registers, as shown in **Table 18-18**
   - Specify the data frame width
   - Specify whether MSB or LSB is the first bit to be transmitted/received
   - Enable the transmitter and receiver
3. Program transmitter and receiver FIFO using the SCBx_TX_FIFO_CTRL and SCBx_RX_FIFO_CTRL registers, respectively, as shown in **Table 18-19**
   - Set the trigger level
   - Clear the transmitter and receiver FIFO and Shift registers
4. Program the SCBx_CTRL register to enable the SCB block and select the I²C mode. These register bits are shown in **Table 18-20**. For a complete description of the I²C registers, see **[2]**

Table 18-17. SCBx_I2C_CTRL register

Bits	Name	Value	Description
30	SLAVE_MODE	1	Slave mode
31	MASTER_MODE	1	Master mode

Table 18-18. SCBx_TX_CTRL/SCBx_RX_CTRL register

Bits	Name	Description
[3:0]	DATA_ WIDTH	'DATA_WIDTH + 1' is the number of bits in the transmitted or received data frame. The valid range is [3, 15].

Table 18-18. SCBx_TX_CTRL/SCBx_RX_CTRL register (continued)

8	MSB_FIRST	1= MSB first
		0= LSB first
31	ENABLED	Transmitter enable bit for SCBx_TX_CTRL and receiver enable bit for SCBx_RX_CTRL registers. They must be enabled for all the protocols. Otherwise, the block may not function or the data may get lost.

Table 18-19. SCBx_TX_FIFO_CTRL/ SCBx_RX_FIFO_CTRL registers

Bits	Name	Description
[2:0]	TRIGGER_LEVEL	Trigger level. When the transmitter FIFO has less entries or the receiver FIFO has more entries than the value of this field, a transmitter or receiver trigger event is generated in the respective case.
16	CLEAR	When '1', the transmitter or receiver FIFO and the shift registers are cleared.
17	FREEZE	When '1', hardware reads/writes to the transmitter or receiver FIFO have no effect. Freeze does not advance the TX or RX FIFO read/write pointer.

Table 18-20. SCBx_CTRL registers

Bits	Name	Value	Description
[25:24]	MODE	00	I^2C mode
		01	SPI mode
		10	UART mode
		11	Reserved
31	ENABLED	0	SCB block enabled
		1	SCB block disabled

- **Configuring for EZI^2C mode**

To configure the SCB block for EZI^2C mode, set the following I^2C register bits

1. Select the EZI^2C mode by writing '1' to the EZ_MODE bit (bit 10) of the SCBx_CTRL register
2. Follow steps 2 to 4 mentioned in **"Configuring for I2C Standard (Non-EZ) mode"** on page 100
3. Set the S_READY_ADDR_ACK (bit 12) and S_READY_DATA_ACK (bit 13) bits of the SCBx_I2C_CTRL register

18.4.11 Internal and external clock operation in I²C

The SCB supports both internally and externally clocked operation for data-rate generation. Internally clocked operations use a clock signal derived from the EZ-PD™ PMG1-S0 MCU system bus clock. Externally clocked operations use a clock provided by the user. Externally clocked operation allows limited functionality in the Deep Sleep power mode, in which on-chip clocks are not active. For more information on system clocking, see the **"Clocking system"** on page 53.

Externally clocked operation is limited to the following cases:

- Slave functionality
- EZ functionality. TX and RX FIFOs do not support externally clocked operation; therefore, it is not used for non-EZ functionality

Internally and externally clocked operations are determined by two register fields of the SCBx_CTRL register:

- **Externally clocked address matching mode (EC_AM_MODE)**: Indicates whether I²C address matching is internally ('0') or externally ('1') clocked.
- **Externally clocked operation mode (EC_OP_MODE)**: Indicates whether the rest of the protocol operation (besides I²C address match) is internally ('0') or externally ('1') clocked. As mentioned earlier, externally clocked operation does not support non-EZ functionality.

These two register fields determine the functional behavior of I²C. The register fields should be set based on the required behavior in Active, Sleep, and Deep Sleep system power modes. Improper setting may result in faulty behavior in certain power modes. **Table 18-21** describe the settings for I²C in EZ and non-EZ mode.

18.4.11.1 I²C Non-EZ operation mode

Externally clocked operation is not supported for non-EZ functionality because there is no FIFO support for this mode. So, the EC_OP_MODE should always be set to '0' for non-EZ mode. However, EC_AM_MODE can be set to '0' or '1'. **Table 18-9** gives an overview of the possibilities. The combination EC_AM_MODE = 0 and EC_OP_MODE = 1 is invalid and the block will not respond.

- **EC_AM_MODE is '0' and EC_OP_MODE is '0'**: This setting only works in Active and Sleep system power modes. All the I²C functionality is provided in the internally clocked domain.
- **EC_AM_MODE is '1' and EC_OP_MODE is '0'**:

This setting works in Active and Deep Sleep system power modes. I²C address matching is performed by the externally clocked logic in both these modes. When the externally clocked logic matches the address, it sets a wakeup interrupt cause bit, which can be used to generate an interrupt to wakeup the CPU.

- In Active system power mode, the CPU is active and the wakeup interrupt cause is disabled (associated MASK bit is '0'). The externally clocked logic takes care of the address matching and the internally locked logic takes care of the rest of the I²C transfer
- In the Sleep mode, wakeup interrupt cause can be either enabled or disabled based on the application. The remaining operations are similar to the Active mode
- In the Deep Sleep mode, the CPU is shut down and will wake up on I²C activity if the wakeup interrupt cause is enabled. CPU wakeup up takes time and the ongoing I²C transfer is either negatively acknowledged (NACK) or the clock is stretched. In the case of a NACK, the internally clocked logic takes care of the first I²C transfer after it wakes up. For clock stretching, the internally clocked logic takes care of the ongoing/stretched transfer when it wakes up. The register bit S_NOT_READY_ADDR_NACK (bit 14) of the SCBx_I2C_CTRL register determines whether the externally clocked logic performs a negative acknowledge ('1') or clock stretch ('0')

18.4.11.2 EZ operation mode

The EZ mode has three possible settings. EC_AM_MODE can be set to '0' or '1' when EC_OP_MODE is '0' and EC_AM_MODE must be set to '1' when EC_OP_MODE is '1'. **Table 18-21** gives an overview of the possibilities. The gray cells indicate a possible, yet not recommended setting because it involves a switch from the externally clocked logic (slave selection) to the internally clocked logic (rest of the operation). The combination EC_AM_MODE=0 and EC_OP_MODE=1 is invalid and the block will not respond.

Table 18-21. I²C EZ mode

I²C, EZ Mode				
System Power Mode	**EC_OP_MODE= 0**		**EC_OP_MODE = 1**	
	EC_AM_MODE = 0	**EC_AM_MODE = 1**	**EC_AM_MODE = 1**	**EC_AM_MODE=0**
Active and Sleep	Address match using internal clock Operation using internal clock	Address match using external clock Operation using internal clock	Address match using external clock Operation using external clock	Invalid configuration
Deep Sleep	Not supported	Address match using external clock Operation using internal clock	Address match using external clock Operation using external clock	

- **EC_AM_MODE is '0' and EC_OP_MODE is '0'**: This setting only works in Active/Sleep system power mode.
- **EC_AM_MODE is '1' and EC_OP_MODE is '0'**: This setting works same as I²C non-EZ mode.
- **EC_AM_MODE is '1' and EC_OP_MODE is '1'**: This setting works in Active system power mode and Deep Sleep system power mode.

The SCB functionality is provided in the externally clocked domain. Note that this setting results in externally clocked accesses to the block's SRAM. These accesses may conflict with internally clocked accesses from the device. This may cause wait states or bus errors. The field FIFO_BLOCK (bit 17) of the SCBx_CTRL register determines whether wait states ('1') or bus errors ('0') are generated.

18.4.12 Wake up from sleep

The system wakes up from Sleep or Deep Sleep system power modes when an I²C address match occurs. The I²C block performs either of two actions after address match: Address ACK or Address NACK.

- **Address ACK** - The I²C slave executes clock stretching and waits until the device wakes up and ACKs the address
- **Address NACK** - The I²C slave NACKs the address immediately. The master must poll the slave again after the device wakeup time is passed. This option is only valid in the slave or multi-master-slave modes

Note: The interrupt bit WAKEUP (bit 0) of the INTR_I2C_EC register must be enabled for the I²C to wake up the device on slave address match while switching to the Sleep mode.

18.4.13 Master mode transfer examples

Master mode transmits or receives data.

18.4.13.1 Master transmit

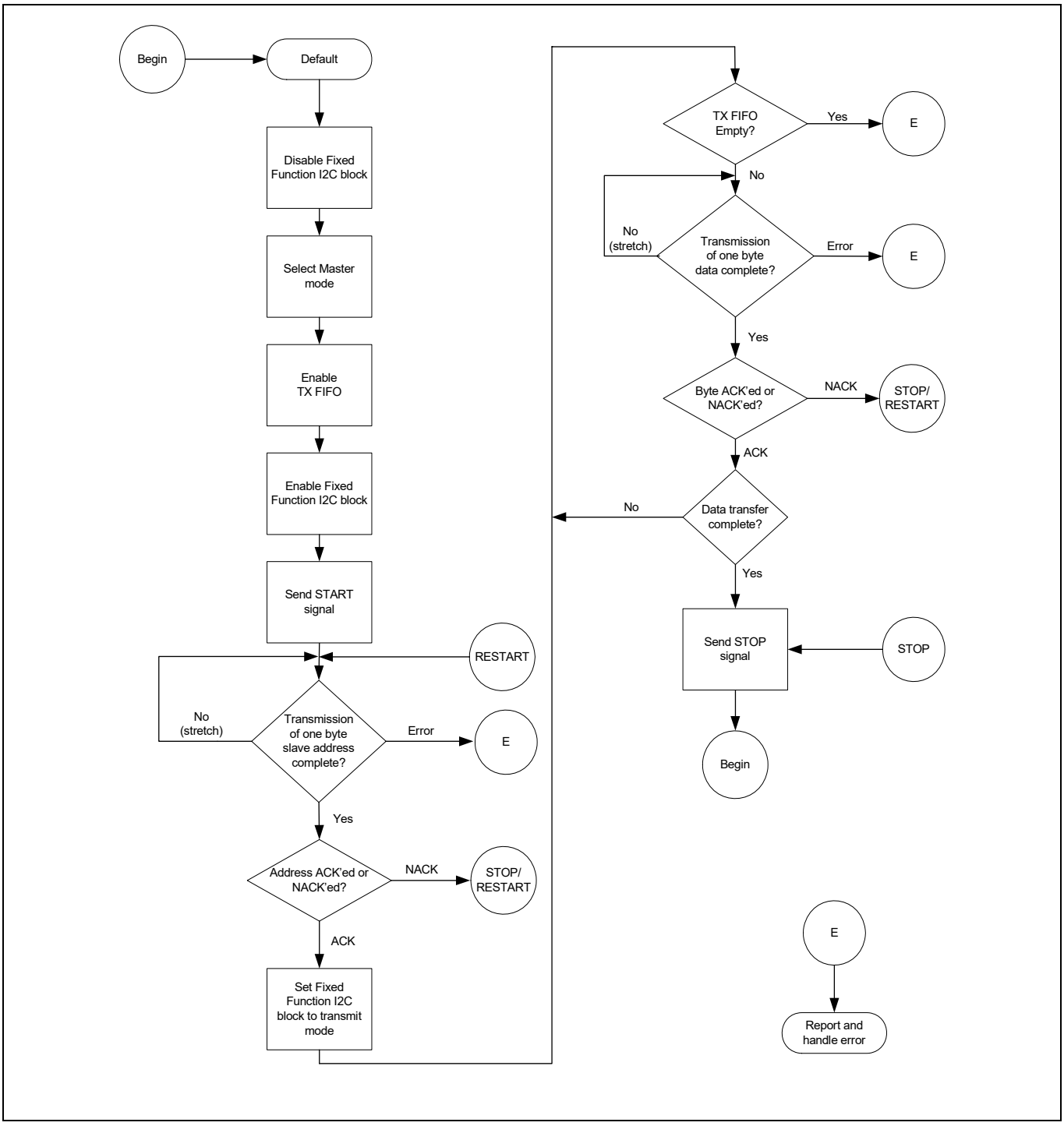


Figure 18-23. Single master mode Write operation flow chart

18.4.13.2 Master receive

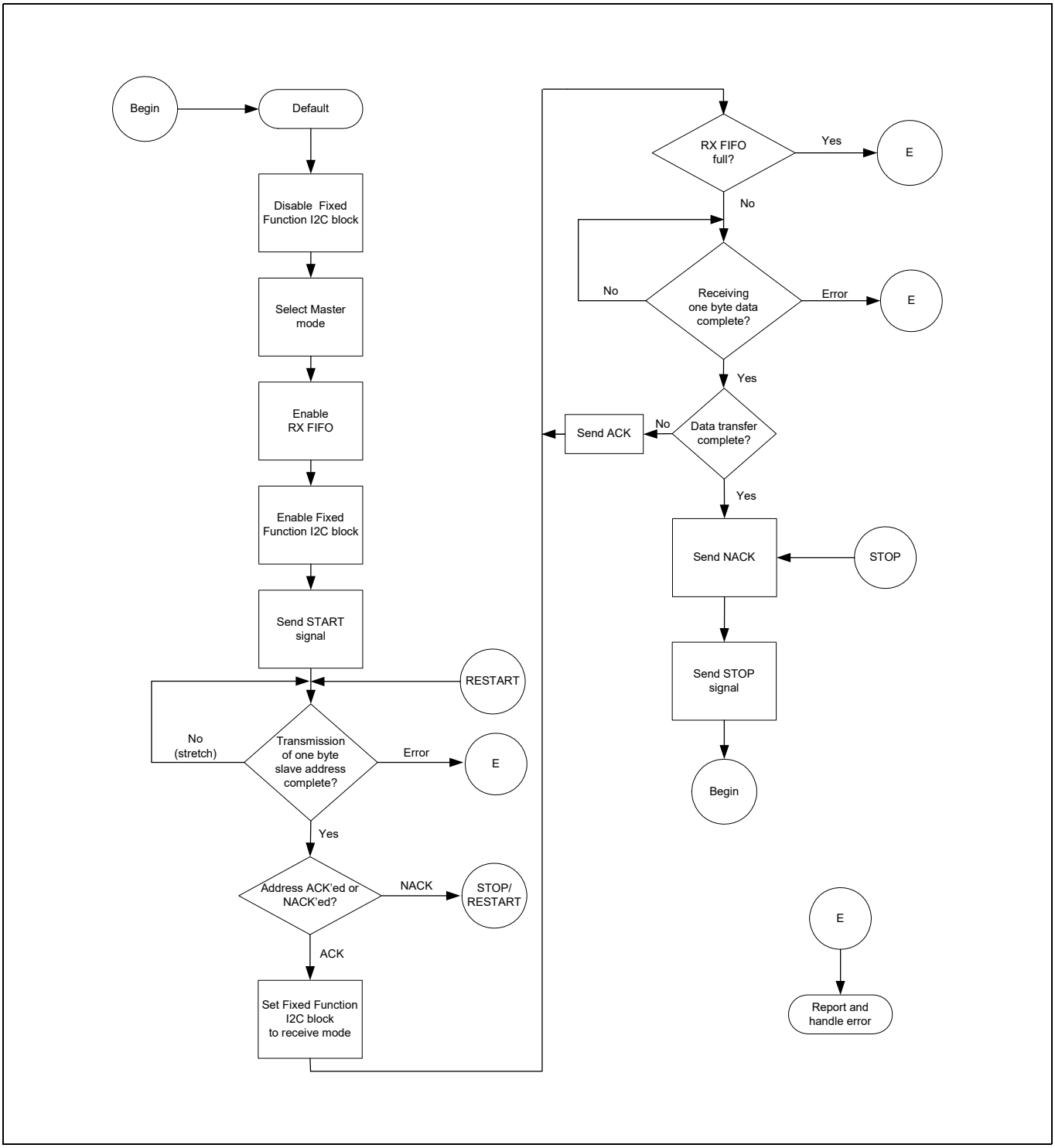


Figure 18-24. Single master mode read operation flow chart

18.4.14 Slave mode transfer examples

Slave mode transmits or receives data.

18.4.14.1 Slave transmit

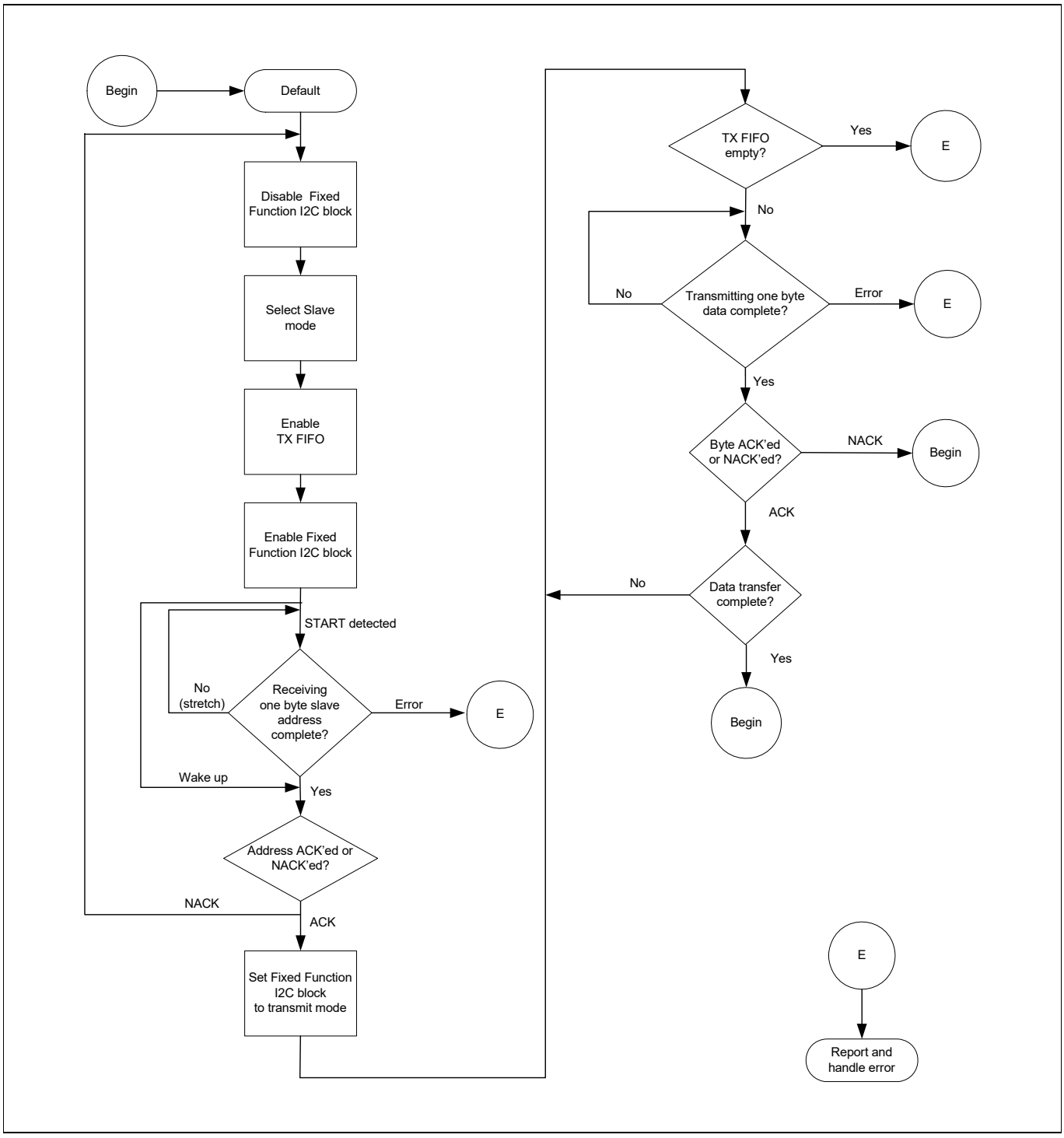


Figure 18-25. Slave mode write operation flow chart

18.4.14.2 Slave receive

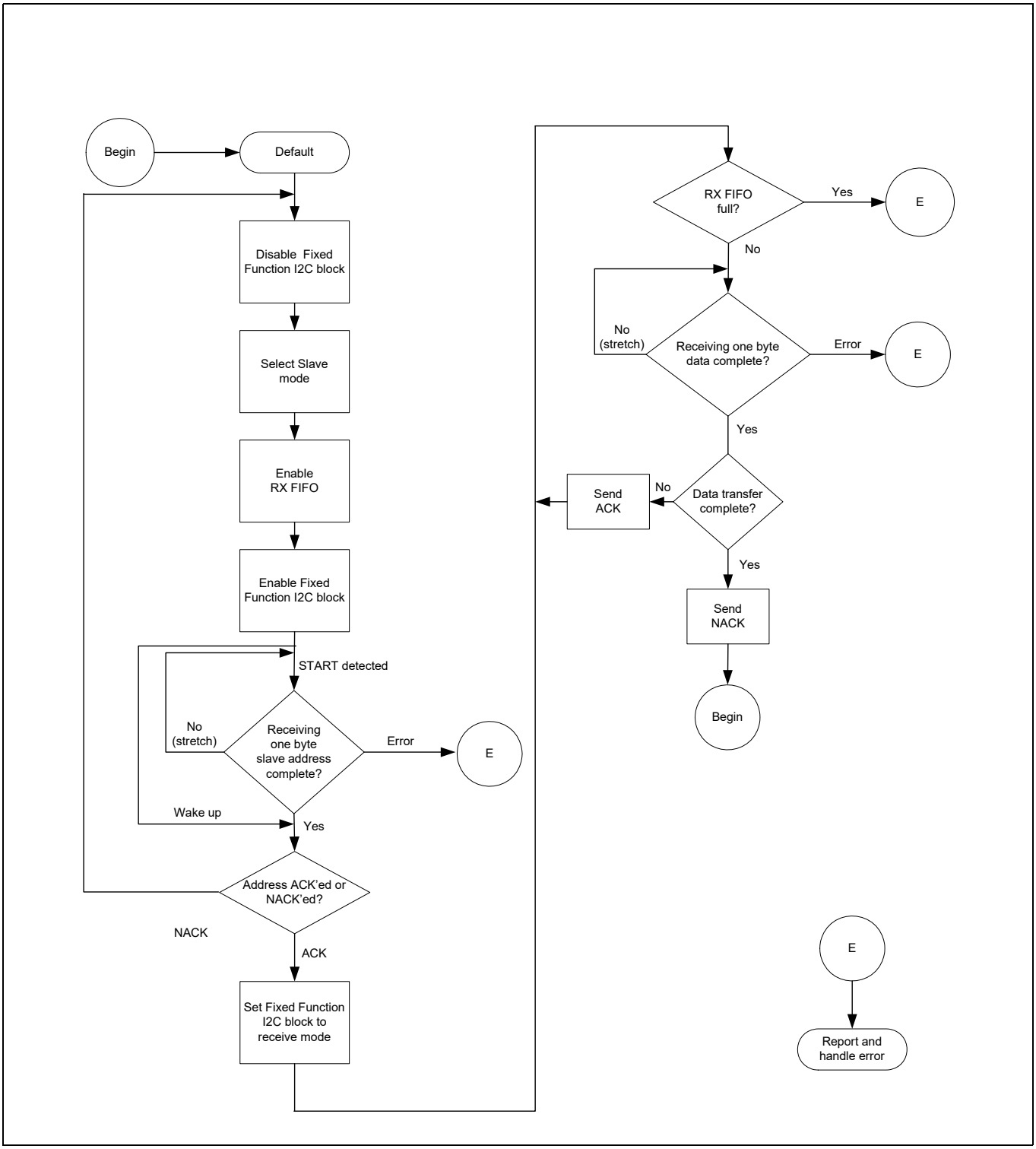


Figure 18-26. Slave mode read operation flow chart

18.4.15 EZ slave mode transfer example

The EZ Slave mode transmits or receives data.

18.4.15.1 EZ slave transmit

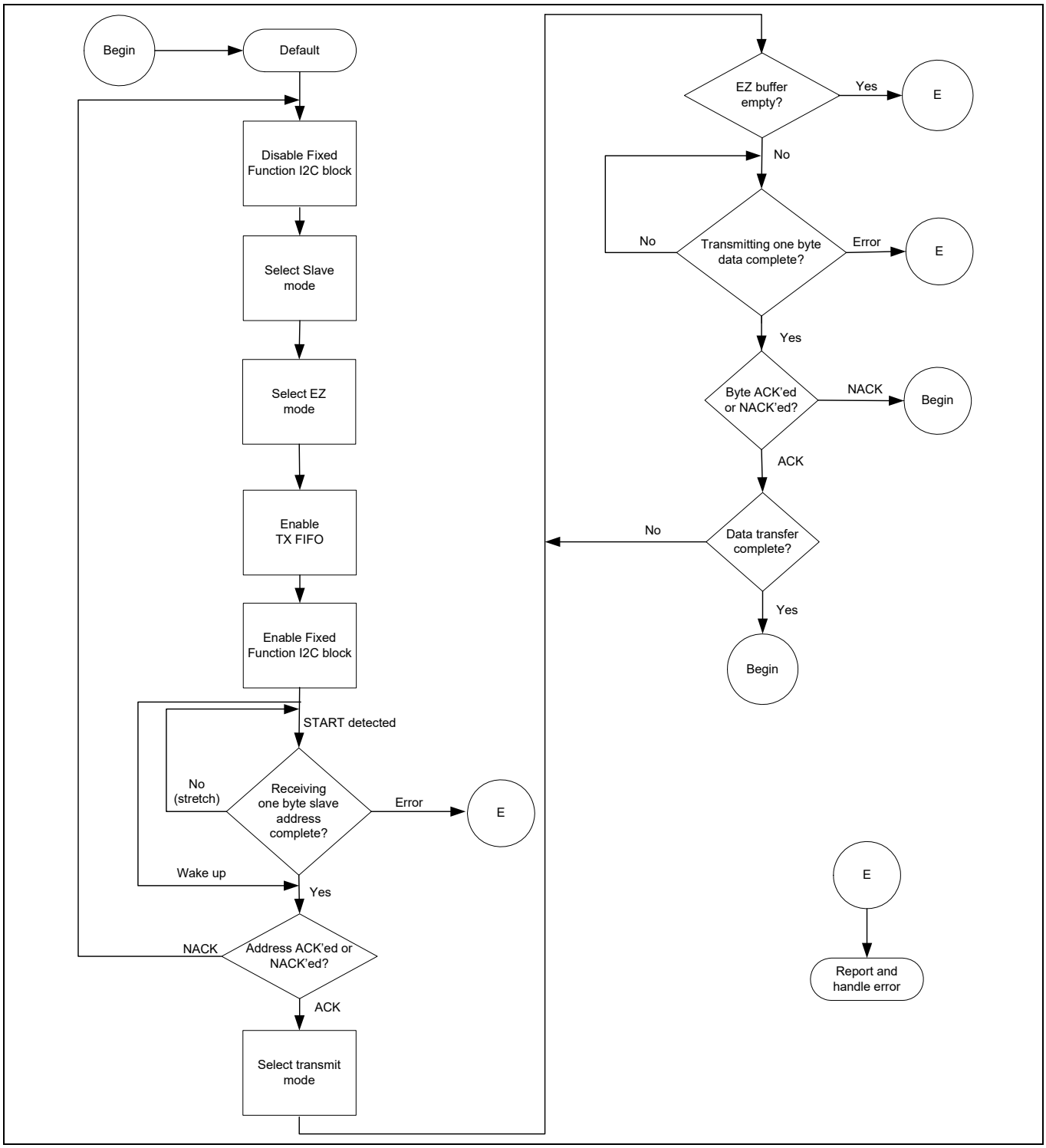


Figure 18-27. EZI²C slave mode write operation flow chart

18.4.15.2 EZ slave receive

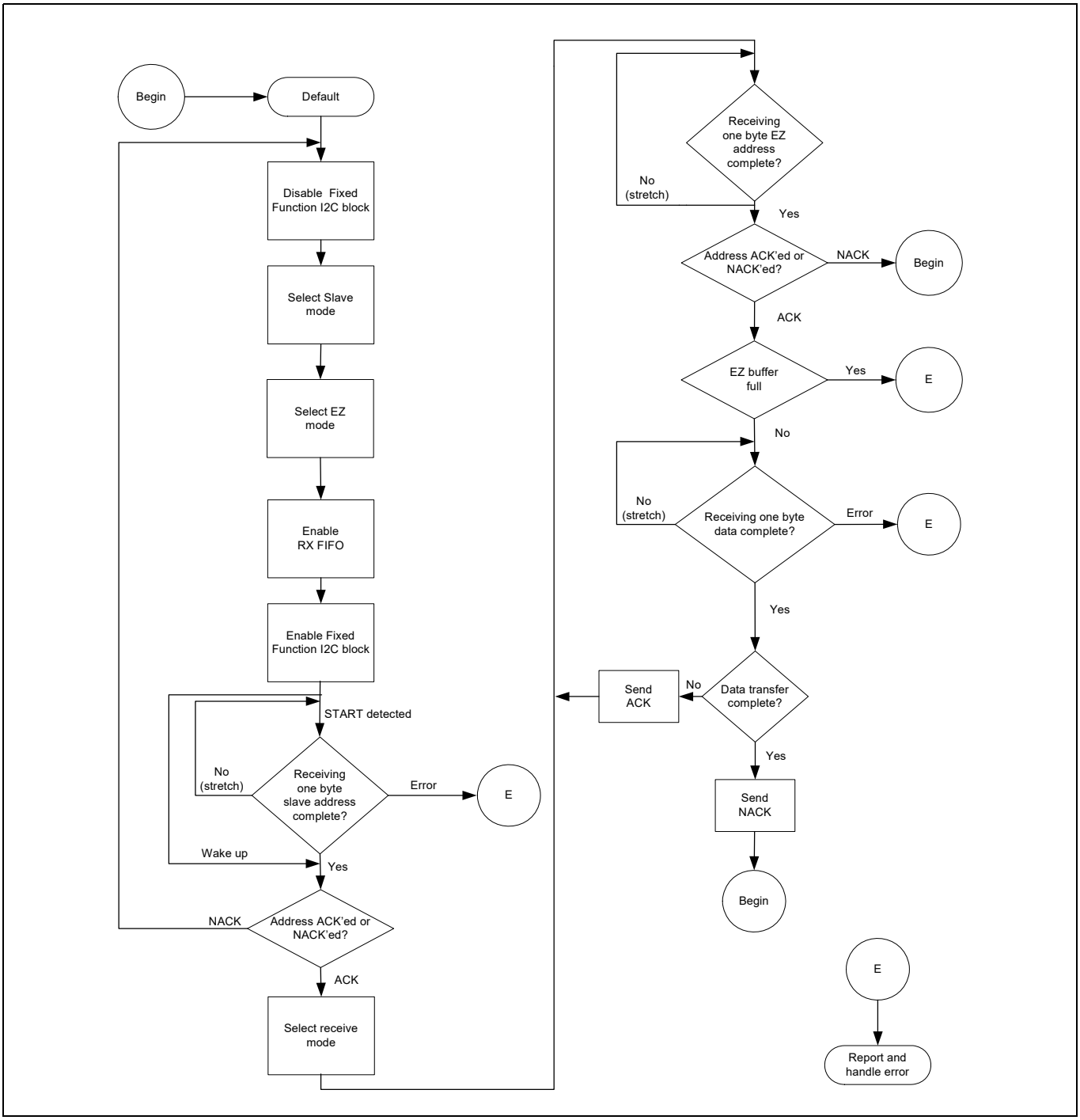


Figure 18-28. EZI²C slave mode read operation flow chart

18.4.16 Multi-master mode transfer example

In multi-master mode, data can be transferred with the slave mode enabled or not enabled.

18.4.16.1 Multi-master - slave not enabled

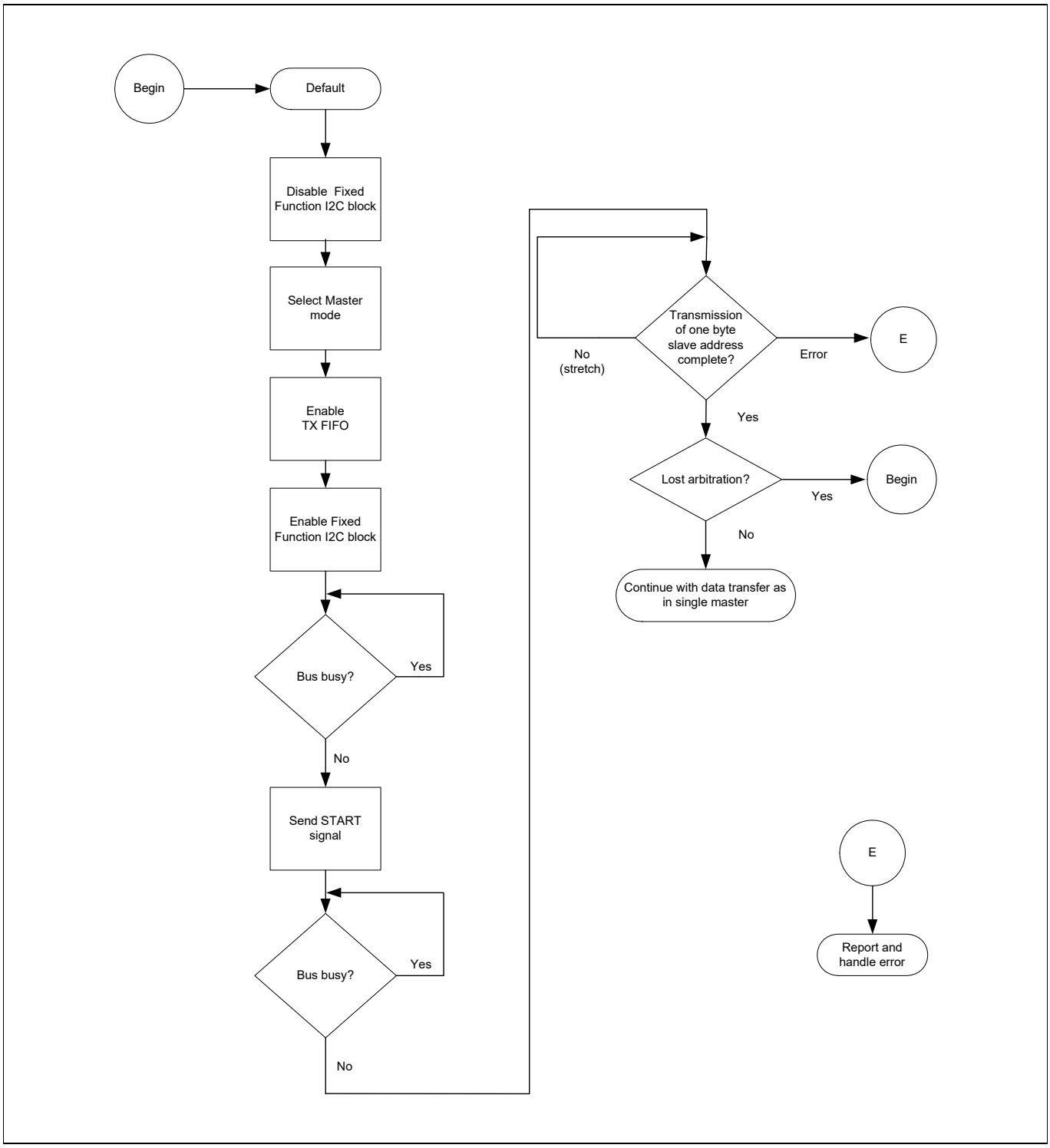


Figure 18-29. Multi-master, slave not enabled flow chart

18.4.16.2 Multi-master - slave enabled

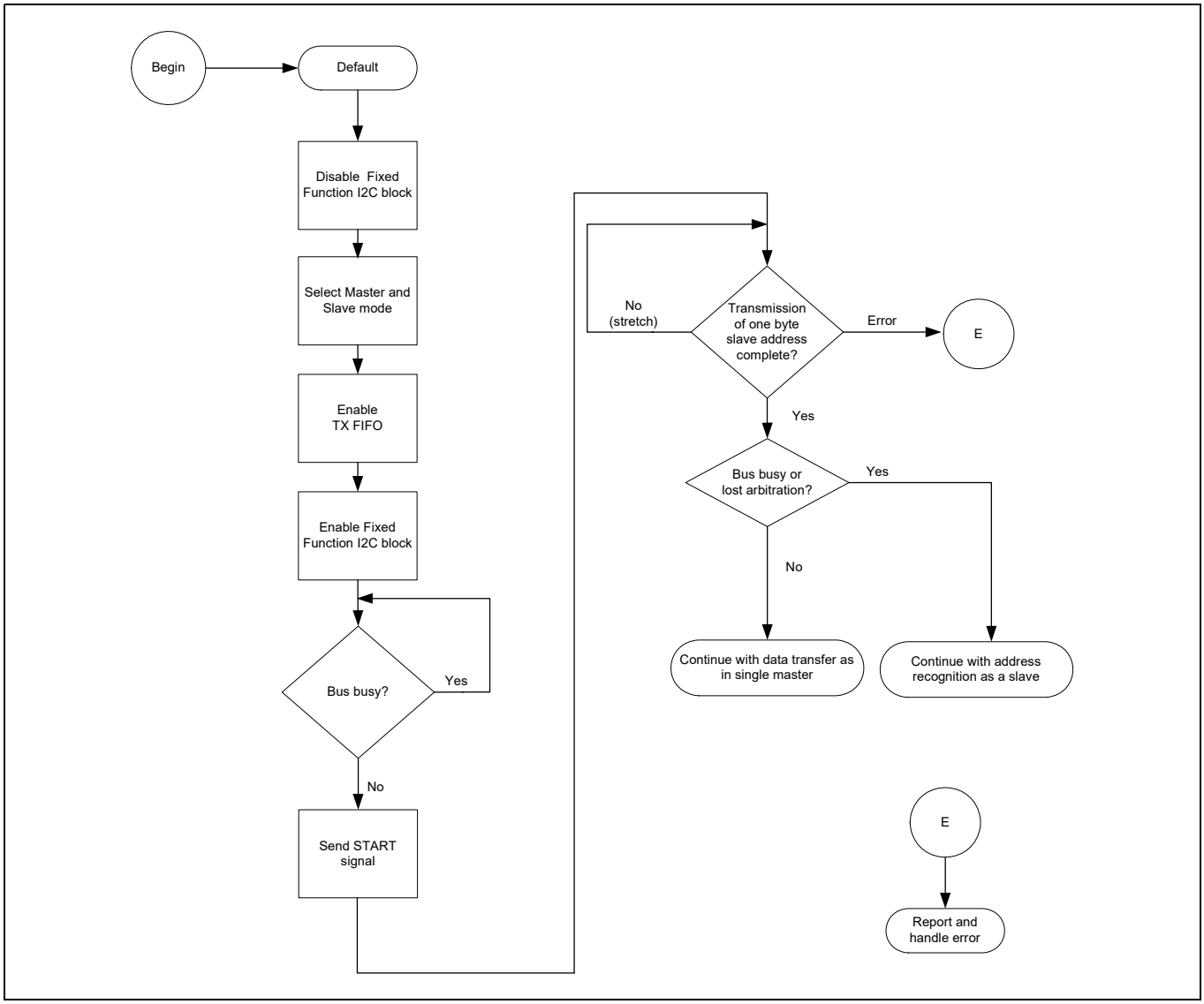


Figure 18-30. Multi-master, slave enabled flow chart

19 Timer, Counter, and PWM

EZ-PD™ PMG1-S0 MCU includes four blocks of the Timer, Counter, and Pulse Width Modulator (TCPWM) block. Each TCPWM in EZ-PD™ PMG1-S0 MCU implements the 16-bit timer, counter, pulse width modulator (PWM), and quadrature decoder functionality. The block can be used to measure the period and pulse width of an input signal (timer), find the number of times a particular event occurs (counter), generate PWM signals, or decode quadrature signals. This chapter explains the features, implementation, and operational modes of the TCPWM block.

19.1 Features

- Four 16-bit timers, counters, or pulse width modulators (PWM)
- The TCPWM block supports the following operational modes:
  - Timer/counter
  - Quadrature decoder
  - Pulse width modulation (PWM)
  - Pseudo-random PWM
- Multiple counting modes – up, down, and up/down
- Clock prescaling (division by 1, 2, 4, ... 64, 128)
- Double buffering of compare/capture and period values
- Supports interrupt on:
  - Terminal Count (TC) – The final value in the counter register is reached
  - Capture/Compare (CC) – The count is captured to the capture/compare register or the counter value equals the compare value
- Synchronized counters – The counters can reload, start, stop, and count at the same time

19.2 Block diagram

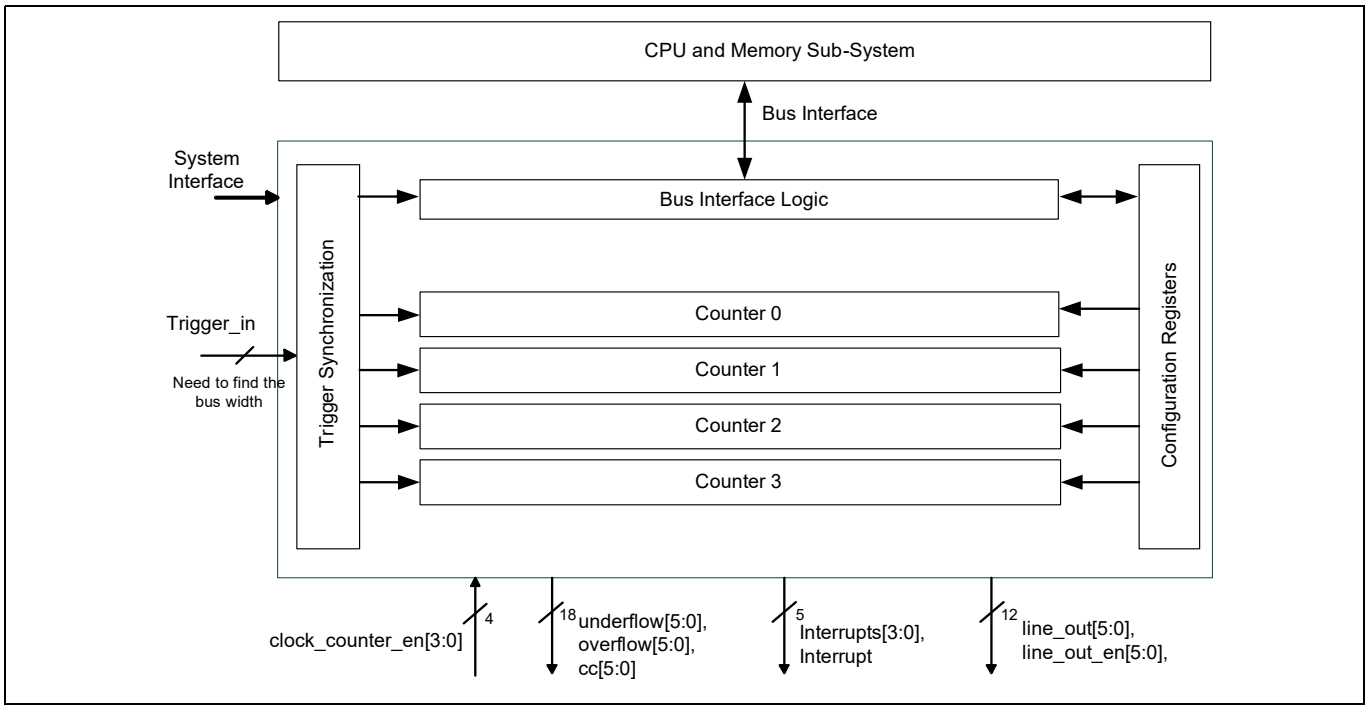


Figure 19-1. TCPWM block diagram

The block has these interfaces:

- **Bus interface**: Connects the block to the CPU subsystem.
- **Interrupts**: Provides interrupt request signals from each counter, based on terminal count (TC) or CC conditions, and a combined interrupt signal generated by the logical OR of all six interrupt request signals.
- **System interface**: Consists of control signals such as clock and reset from the system resources subsystem.

This TCPWM block can be configured by writing to the TCPWM registers. See **"TCPWM registers"** on page 131 for more information on all registers required for this block.

19.2.1 Enabling and disabling counter in TCPWM block

The counter can be enabled by setting the COUNTER_ENABLED field (bit 0) of the control register TCPWM_CTRL.

Note: The counter must be configured before enabling it. If the counter is enabled after being configured, registers are updated with the new configuration values. Disabling the counter retains the values in the registers until it is enabled again (or reconfigured).

19.2.2 Clocking

The TCPWM receives the HFCLK through the system interface to synchronize all events in the block. The counter enable signal (counter_en), which is generated when the counter is enabled, gates the HFCLK to provide a counter-specific clock (counter_clock). Output triggers (explained later in this chapter) are also synchronized with the HFCLK.

Clock pre-scaling: counter_clock can be prescaled, with divider values of 1, 2, 4… 64, 128. This is done by modifying the GENERIC field of the counter control (TCPWM_CNTx_CTRL) register, as shown in **Table 19-1**.

Table 19-1. Bit-field setting to prescale counter clock

GENERIC[10:8]	Description
0	Divide by 1
1	Divide by 2
2	Divide by 4
3	Divide by 8
4	Divide by 16
5	Divide by 32
6	Divide by 64
7	Divide by 128

Note: Clock prescaling cannot be done in quadrature mode and pulse width modulation mode with dead time (PWM-DT).

19.2.3 Events-based on trigger inputs

These are the events triggered by hardware or software.

- Reload
- Start
- Stop
- Count
- Capture/switch
- Hardware triggers can be level signal, rising edge, falling edge, or both edges.

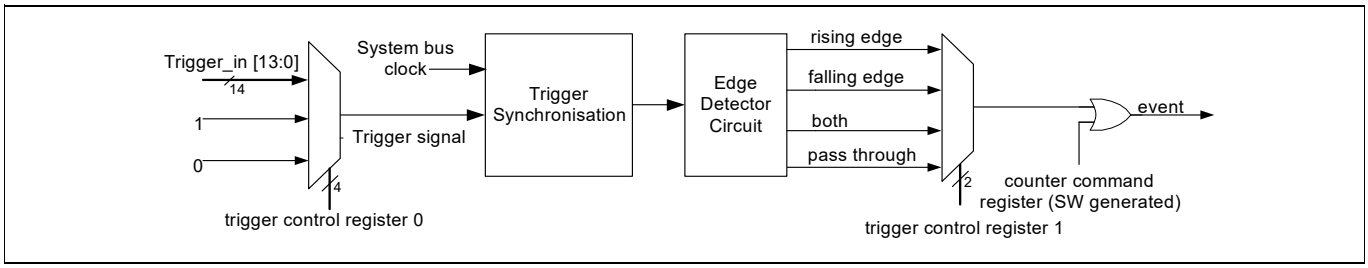


Figure 19-2. TCPWM trigger selection and event detection

Figure 19-2 shows the trigger selection and event detection in the TCPWM block. The trigger control register 0 (TCPWM_CNTx_TR_CTRL0) selects one of the 16 trigger inputs as the event signal. Additionally, a constant '0' and '1' signals are available to be used as the event signal.

As shown in the figure, the Trigger_in inputs on EZ-PD™ PMG1-S0 MCU have been connected internally to trigger outputs generated by the USBPD block. External (GPIO) trigger inputs are not supported.

Any edge (rising, falling, or both) or level (high or low) can be selected for the occurrence of an event by configuring the trigger control register 1 (TCPWM_CNTx_TR_CTRL1). This edge/level configuration can be selected for each trigger event separately. Alternatively, firmware can generate an event by writing to the counter command register (TCPWM_CMD), as shown in Figure 19-2.

The events derived from these triggers can have different definitions in different modes of the TCPWM block.

- **Reload:** A reload event initializes and starts the counter
  - In up counting mode, the count register (TCPWM_CNTx_COUNTER) is initialized with ‘0’
  - In down counting mode, the counter is initialized with the period value stored in the TCPWM_CNTx_PERIOD register
  - In up/down counting mode, the count register is initialized with ‘0’
  - In quadrature mode, the reload event acts as a quadrature index event. An index/reload event indicates a completed rotation and can be used to synchronize quadrature decoding
- **Start:** A start event is used to start counting; it can be used after a stop event or after re-initialization of the counter register to any value by software. Note that the count register is not initialized on this event
  - In quadrature mode, the start event acts as quadrature phase input phiB, which is explained in detail in **“Quadrature decoder mode”** on page 122
- **Count:** A count event causes the counter to increment or decrement, depending on its configuration
  - In quadrature mode, the count event acts as quadrature phase input phiA
- **Stop:** A stop event stops the counter from incrementing or decrementing. A start event will start the counting again.
  - In the PWM modes, the stop event acts as a kill event. A kill event disables all the PWM output lines
- **Capture:** A capture event copies the counter register value to the capture register and capture register value to the buffer capture register. In the PWM modes, the capture event acts as a switch event. It switches the values of the capture/compare and period registers with their buffer counterparts. This feature can be used to modulate the pulse width and frequency

Notes:

- *All trigger inputs are synchronized to the HFCLK.*
- *When more than one event occurs in the same counter clock period, one or more events may be missed. This can happen for high-frequency events (frequencies close to the counter frequency) and a timer configuration in which a prescaled (divided) counter clock is used.*

19.2.4 Output signals

The TCPWM block generates several output signals, as shown in **Figure 19-3**.

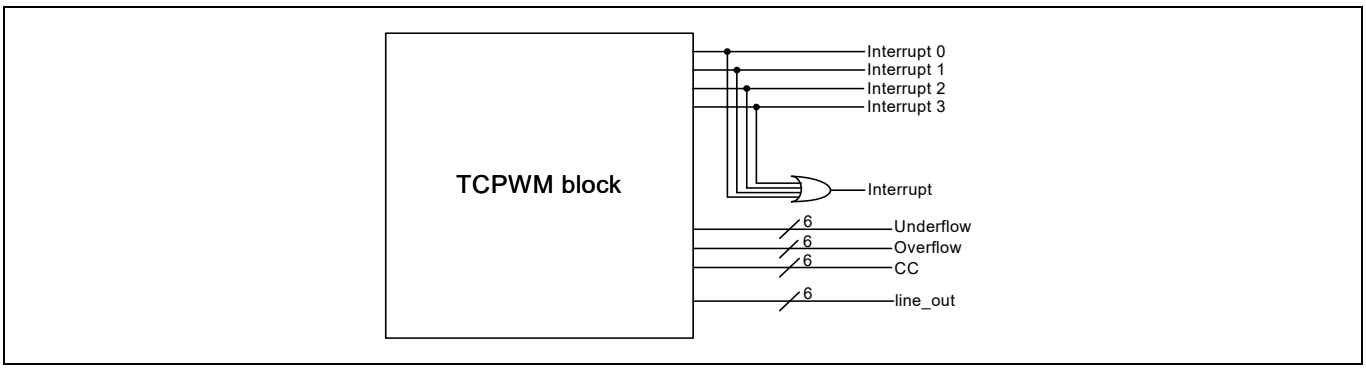


Figure 19-3. TCPWM output signals

19.2.4.1 Signals upon trigger conditions

- Counter generates an internal overflow (OV) condition when counting up and the count register reaches the period value
- Counter generates an internal underflow (UN) condition when counting down and the count register reaches zero
- The capture/compare (CC) condition is generated by the TCPWM when the counter is running and one of the following conditions occur:
  - The counter value equals the compare value
  - A capture event occurs - When a capture event occurs, the TCPWM_CNTx_COUNTER register value is copied to the capture register and the capture register value is copied to the buffer capture register

Note: *These signals, when they occur, remain at logic high for one cycle of the HFCLK. For reliable operation, the condition that causes this trigger should occur in a frequency less than a quarter of the HFCLK. For example, if the HFCLK is running at 24 MHz, the condition causing the trigger should occur at a frequency less than 6 MHz.*

19.2.4.2 Interrupts

The TCPWM block provides a dedicated interrupt output signal from the counter. An interrupt can be generated for a TC condition or a CC condition. The exact definition of these conditions is mode-specific. All six interrupt output signals from the four TCPWMs are also OR'ed together to produce a single interrupt output signal.

Four registers are used for interrupt handling in this block, as shown in **Table 19-2**.

Table 19-2. Interrupt register

Interrupt registers	Bits	Name	Description
TCPWM_CNTx_INTR (Interrupt request register)	0	TC	This bit is set to '1', when a terminal count is detected. Write '1' to clear this bit.
	1	CC_MATCH	This bit is set to '1' when the counter value matches capture/compare register value. Write with '1' to clear this bit.
TCPWM_CNTx_INTR_SET (Interrupt set request register)	0	TC	Write '1' to set the corresponding bit in the interrupt request register. When read, this register reflects the interrupt request register status.
	1	CC_MATCH	Write '1' to set the corresponding bit in the interrupt request register. When read, this register reflects the interrupt request register status.
TCPWM_CNTx_INTR_MASK (Interrupt mask register)	0	TC	Mask bit for the corresponding TC bit in the interrupt request register.
	1	CC_MATCH	Mask bit for the corresponding CC_MATCH bit in the interrupt request register.
TCPWM_CNTx_INTR_MASKED (Interrupt masked request register)	0	TC	Logical AND of the corresponding TC request and mask bits.
	1	CC_MATCH	Logical AND of the corresponding CC_MATCH request and mask bits.

19.2.4.3 Outputs

The TCPWM has one output line_out. Note that the OV, UN, and CC conditions can be used to drive line_out if needed, by configuring the TCPWM_CNTx_TR_CTRL2 register (see **Table 19-3**).

Table 19-3. Configuring output line for OV, UN, and CC conditions

Field	Bit	Value	Event	Description
CC_MATCH_MODE Default Value = 3	1:0	0	Set line_out to '1'	Configures output line on a compare match (CC) event
		1	Clear line_out to '0'	
		2	No change	
		3	No change	
OVERFLOW_MODE Default Value = 3	3:2	0	Set line_out to '1'	Configures output line on a overflow (OV) event
		1	Clear line_out to '0'	
		2	No change	
		3	No change	

Table 19-3. Configuring output line for OV, UN, and CC conditions (continued)

Field	Bit	Value	Event	Description
UNDERFLOW_MODE Default Value = 3	5:4	0	Set line_out to '1	Configures output line on a underflow (UN) event
		1	Clear line_out to '0	
		2	No change	
		3	No change	

19.2.5 Power modes

The TCPWM block works in Active and Sleep modes. The TCPWM block is powered from V_{CCD}. The configuration registers and other logic are powered in Deep Sleep mode to keep the states of configuration registers. See **Table 19-4**.

Table 19-4. Power modes in TCPWM block

Power mode	Block status
Active	This block is fully operational in this mode with clock running and power switched on.
Sleep	All counter clocks are on, but bus interface cannot be accessed.
Deep Sleep	In this mode, the power to this block is still on but no bus clock is provided; hence, the logic is not functional. All the configuration registers will keep their state.

19.3 Modes of operation

The counter block can function in six operational modes, as shown in **Table 19-5**. The MODE [26:24] field of the counter control register (TCPWM_CNTx_CTRL) configures the counter in the specific operational mode.

Table 19-5. Operational mode configuration

Mode	MODE field [26:24]	Description
Timer	000	Implements a timer or counter. The counter increments or decrements by '1' at every counter clock cycle in which a count event is detected.
Capture	010	Implements a timer or counter with capture input. The counter increments or decrements by '1' at every counter clock cycle in which a count event is detected. When a capture event occurs, the counter value copies into the capture register.
Quadrature Decoder	011	Implements a quadrature decoder, where the counter is decremented or incremented, based on two phase inputs according to the selected (X1, X2 or X4) encoding scheme.
PWM	100	Implements edge/center-aligned PWMs with an 8-bit clock prescaler and buffered compare/period registers.
PWM-DT	101	Implements edge/center-aligned PWMs with configurable 8-bit dead time (on both outputs) and buffered compare/period registers.
PWM-PR	110	Implements a pseudo-random PWM using a 16-bit linear feedback shift register (LFSR).

The counter can be configured to count up, down, and up/down by setting the UP_DOWN_MODE[17:16] field in the TCPWM_CNTx_CTRL register, as shown in **Table 19-6**.

Table 19-6. Counting mode configuration

Counting modes	UP_DOWN_MODE [17:16]	Description
UP Counting mode	00	Increments the counter until the period value is reached. A Terminal Count (TC) condition is generated when counter reaches the period value.
DOWN Counting mode	01	Decrements the counter from the period value until 0 is reached. A TC condition is generated when the counter reaches ‘0’.
UP/DOWN Counting Mode 0	10	Increments the counter until the period value is reached, and then decrements the counter until ‘0’ is reached. A TC condition is generated only when ‘0’ is reached.
UP/DOWN Counting mode 1	11	Similar to up/down counting mode 0 but a TC condition is generated when the counter reaches ‘0’ and when the counter value reaches the period value.

19.3.1 Timer mode

The timer mode is commonly used to measure time of occurrence of an event or to measure the time difference between two events.

19.3.1.1 Block diagram

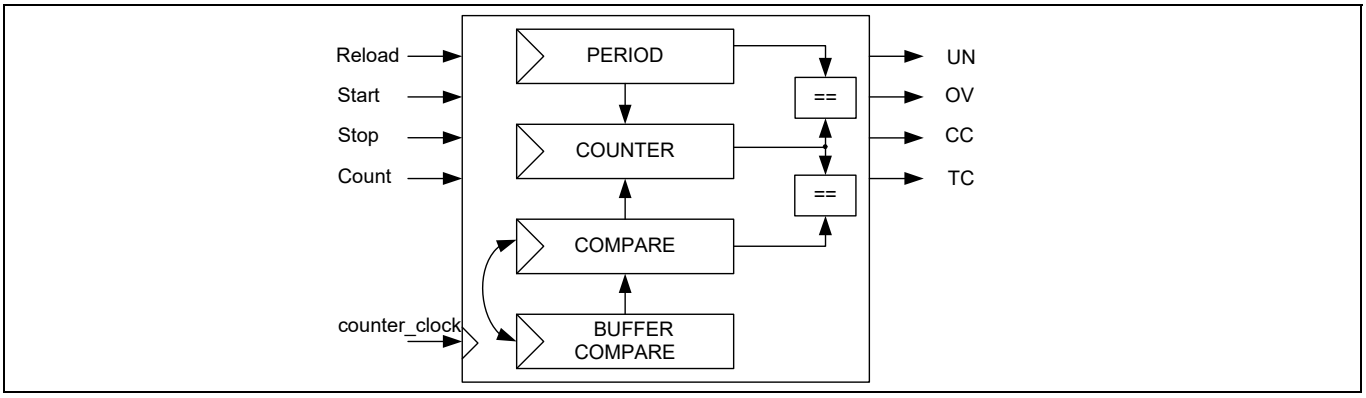


Figure 19-4. Timer mode block diagram

19.3.1.2 How it works

The timer can be configured to count in up, down, and up/down counting modes. It can also be configured to run in either continuous mode or one-shot mode.

The following explains the working of the timer:

- The timer is an up, down, and up/down counter
  - The current count value is stored in the count register (TCPWM_CNTx_COUNTER)

Note: It is not recommended to write values to this register while the counter is running

  - The period value for the timer is stored in the period register
- The counter is re-initialized in different counting modes as follows:
  - In the up counting mode, after the count reaches the period value, the count register is automatically reloaded with ‘0’

  - In the down counting mode, after the count register reaches zero, the count register is reloaded with the value in the period register
  - In the up/down counting modes, the count register value is not updated upon reaching the terminal values. Instead the direction of counting changes when the count value reaches 0 or the period value
- The CC condition is generated when the count register value equals the compare register value. Upon this condition, the compare register and buffer compare register switch their values if enabled by the AUTO_RELOAD_CC bit-field of the counter control (TCPWM_CNTx_CTRL) register. This condition can be used to generate an interrupt request

Figure 19-5 shows the timer operational mode of the counter in four different counting modes. The period register contains the maximum counter value.

- In the up counting mode, a period value of A results in A+1 counter cycles (0 to A)
- In the down counting mode, a period value of A results in A+1 counter cycles (A to 0)
- In the two up/down counting modes (both modes 0 and 1 both), a period value of A results in 2*A counter cycles (0 to A and back to 0)

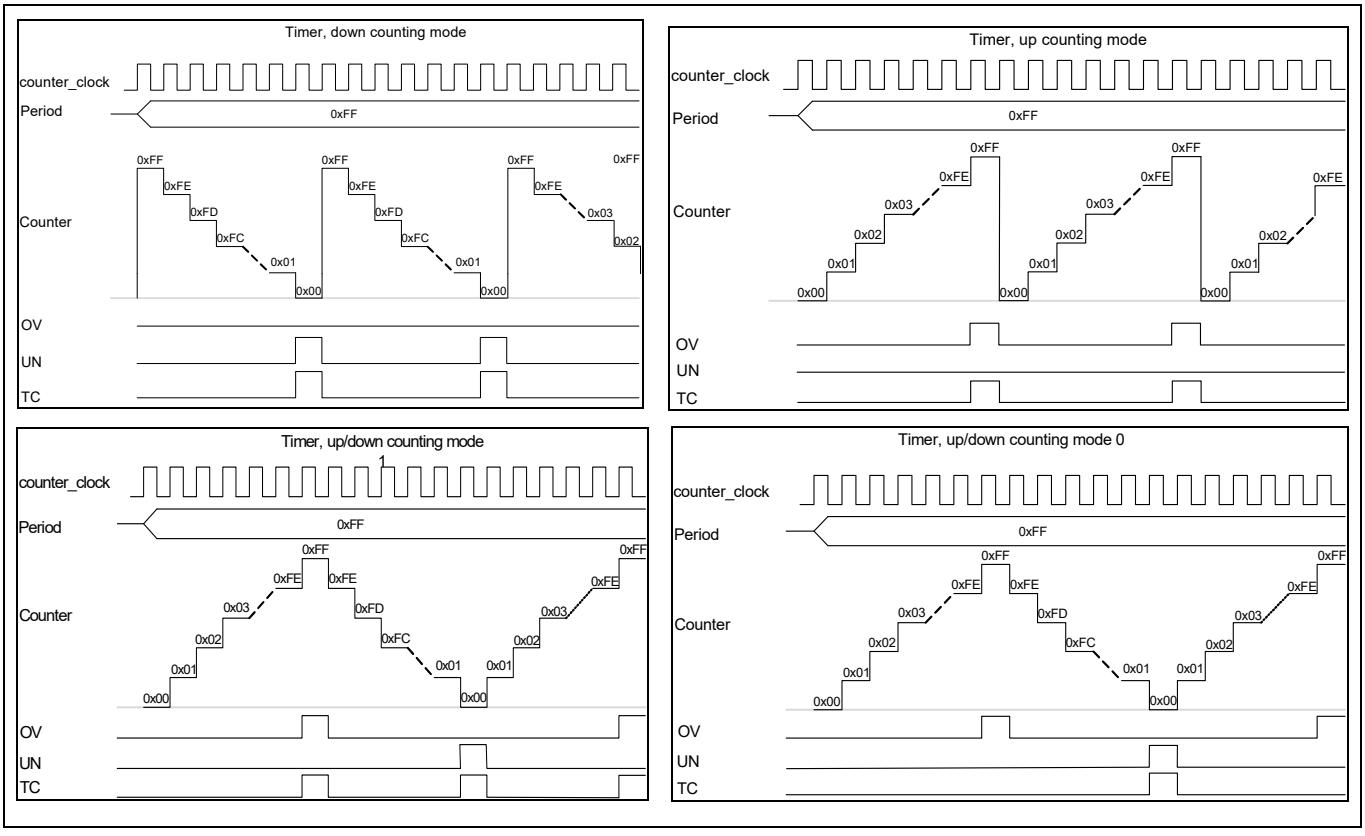


Figure 19-5. Timing diagram for timer in multiple counting modes

*Note: The OV and UN signals remain at logic high for one cycle of the HFCLCK, as explained in **"Signals upon trigger conditions"** on page 115. The figures in this chapter assume that HFCLK and counter clock are the same.*

19.3.1.3 Configuring counter for timer mode

The steps to configure the counter for Timer mode of operation and the affected register bits are as follows.

1. Disable the counter by writing '0' to the COUNTER_ENABLED field of the TCPWM_CTRL register
2. Select Timer mode by writing '000' to the MODE[26:24] field of the TCPWM_CNTx_CTRL register
3. Set the required 16-bit period in the TCPWM_CNTx_PERIOD register
4. Set the 16-bit compare value in the TCPWM_CNTx_CC register and the buffer compare value in the TCPWM_CNTx_CC_BUFF register. Set AUTO_RELOAD_CC field of counter control register, if required to switch values at every CC condition
5. Set clock prescaling by writing to the GENERIC[10:8] field of the counter control (TCPWM_CNTx_CTRL) register, as shown in **Table 19-1**
6. Set the direction of counting by writing to the UP_DOWN_MODE[17:16] field of the TCPWM_CNTx_CTRL register, as shown in **Table 19-6**
7. The timer can be configured to run either in continuous mode or one-shot mode by writing 0 or 1, respectively to the ONE_SHOT[18] field of TCPWM_CNTx_CTRL
8. Set the TCPWM_CNTx_TR_CTRL0 register to select the trigger that causes the event (Reload, Start, Stop, Capture, and Count)
9. Set the TCPWM_CNTx_TR_CTRL1 register to select the edge of the trigger that causes the event (Reload, Start, Stop, Capture, and Count)
10. If required, set the interrupt upon TC or CC condition, as shown in **"Interrupts"** on page 116
11. Enable the counter by writing '1' to the COUNTER_ENABLED field of the TCPWM_CTRL register. A start trigger must be provided through firmware (TCPWM_CMD register) to start the counter if the hardware start signal is not enabled

19.3.2 Capture mode

In the capture mode, the counter value can be captured at any time either through a firmware write to command register (TCPWM_CMD) or a capture trigger input. This mode is used for period and pulse width measurement.

19.3.2.1 Block diagram

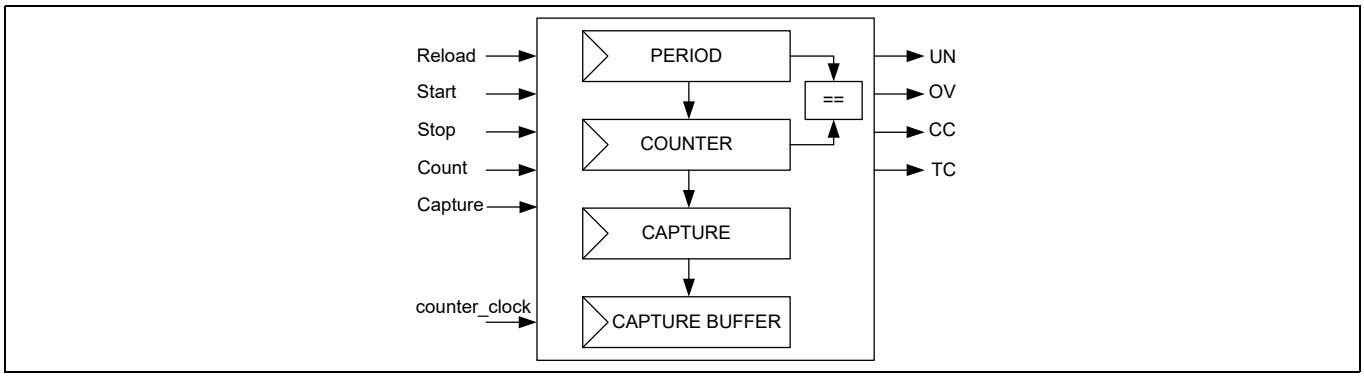


Figure 19-6. Capture mode block diagram

19.3.2.2 How it works

The counter can be set to count in up, down, and up/down counting modes by configuring the UP_DOWN_MODE[17:16] bit-field of the counter control register (TCPWM_CNTx_CTRL). Operation in capture mode occurs as follows:

- During a capture event, generated either by hardware or software, the existing capture register value is copied to the buffer capture register (TCPWM_CNTx_CC_BUFF) and the current count register value is copied to the capture register (TCPWM_CNTx_CC)
- A pulse on the CC output signal is generated when the counter value is copied to the capture register. This condition can also be used to generate an interrupt request

Figure 19-7 illustrates the capture behavior in the up counting mode.

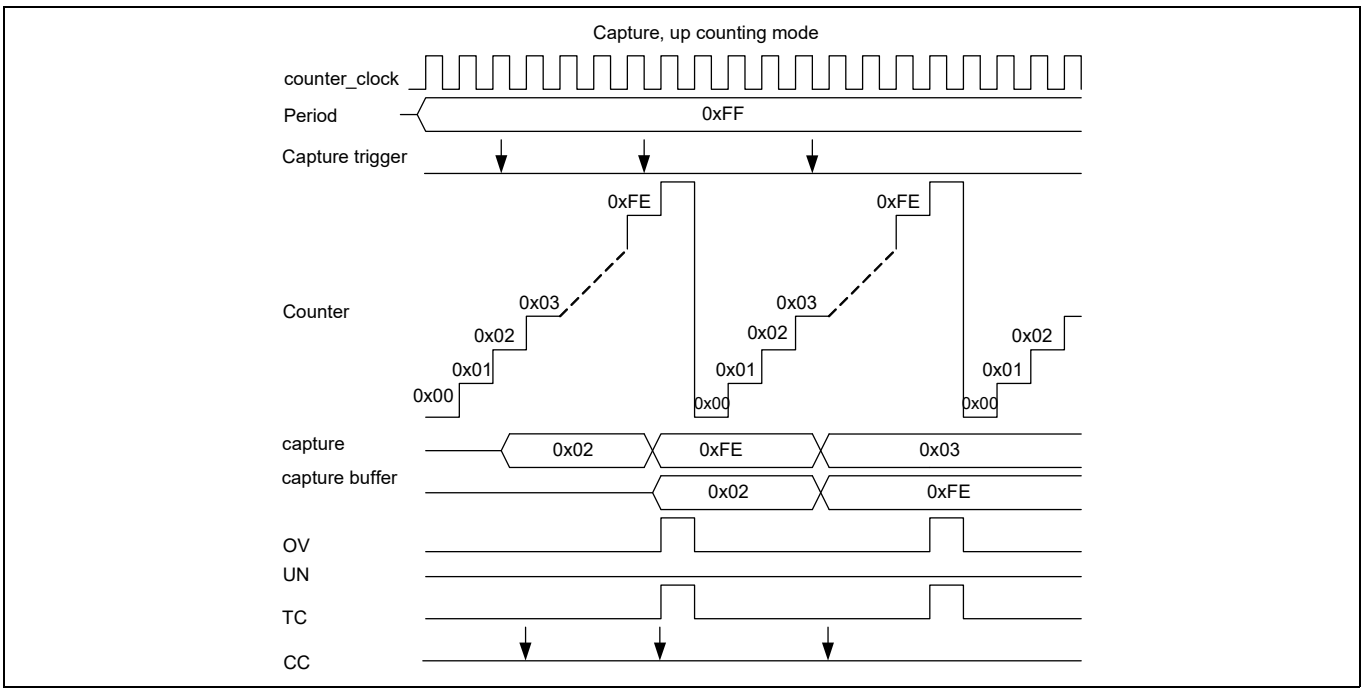


Figure 19-7. Timing diagram of counter in capture mode, up counting mode

In the figure, observe that:

- The period register contains the maximum count value
- Internal overflow (OV) and TC conditions are generated when the counter reaches the period value
- A capture event is only possible at the edges or through software. Use TCPWM_CNTx_TR_CTRL1 register to configure the edge detection
- Multiple capture events in a single clock cycle are handled as:
  - Even number of capture events - no event is observed
  - Odd number of capture events - single event is observed

This happens when the capture signal frequency is greater than the counter_clock frequency.

19.3.2.3 Configuring counter for capture mode

The steps to configure the counter for Capture mode operation and the affected register bits are as follows.

1. Disable the counter by writing '0' to the COUNTER_ENABLED field of the TCPWM_CTRL register
2. Select Capture mode by writing '010' to the MODE[26:24] field of the TCPWM_CNTx_CTRL register
3. Set the required 16-bit period in the TCPWM_CNTx_PERIOD register
4. Set clock prescaling by writing to the GENERIC[10:8] field of the TCPWM_CNTx_CTRL register, as shown in **Table 19-1**
5. Set the direction of counting by writing to the UP_DOWN_MODE[17:16] field of the TCPWM_CNTx_CTRL register, as shown in **Table 19-6**
6. Counter can be configured to run either in continuous mode or one-shot mode by writing 0 or 1, respectively to the ONE_SHOT[18] field of the TCPWM_CNTx_CTRL register
7. Set the TCPWM_CNTx_TR_CTRL0 register to select the trigger that causes the event (Reload, Start, Stop, Capture, and Count)
8. Set the TCPWM_CNTx_TR_CTRL1 register to select the edge that causes the event (Reload, Start, Stop, Capture, and Count)
9. If required, set the interrupt upon TC or CC condition, as shown in **"Interrupts"** on page 116
10. Enable the counter by writing '1' to the COUNTER_ENABLED field of the TCPWM_CTRL register. A start trigger must be provided through firmware (TCPWM_CMD register) to start the counter if the hardware start signal is not enabled

19.3.3 Quadrature decoder mode

Quadrature decoders are used to determine speed and position of a rotary device (such as servo motors, volume control wheels, and PC mice). The quadrature encoder signals are used as phiA and phiB inputs to the decoder.

19.3.3.1 Block diagram

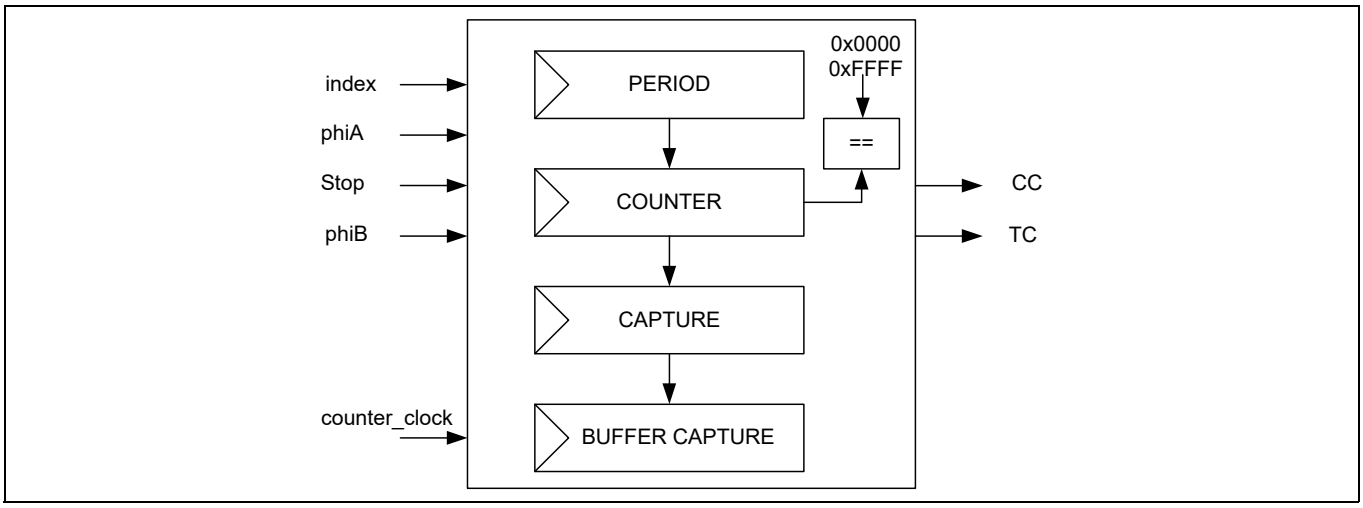


Figure 19-8. Quadrature mode block diagram

19.3.3.2 How it works

Quadrature decoding only runs on counter_clock. It can operate in three sub-modes: X1, X2, and X4. These encoding modes can be controlled by the QUADRATURE_MODE[21:20] field of the counter control register (TCPWM_CNTx_CTRL). This mode uses double buffered capture registers.

The Quadrature mode operation occurs as follows:

- Quadrature phases phiA and phiB: Counting direction is determined by the phase relationship between phiA and phiB. These phases are connected to the count and the start trigger inputs, respectively as hardware input to the decoder.
- Quadrature index signal: This is connected to the reload signal as a hardware input. This event generates a TC condition, as shown in **Figure 19-9**
- On TC, the counter is set to 0x0000 (in the up counting mode) or to the period value (in the down counting mode)

Note: The down counting mode is recommended to be used with a period value of 0x8000 (the mid-point value).

- A pulse on CC output signal is generated when the count register value reaches 0x0000 or 0xFFFF. On a CC condition, the count register is set to the period value (0x8000 in this case)
- On TC or CC condition:
  - Count register value is copied to the capture register
  - Capture register value is copied to the buffer capture register
  - This condition can be used to generate an interrupt request
- The value in the capture register can be used to determine which condition caused the event and whether:
  - A counter underflow occurred (value 0)
  - A counter overflow occurred (value 0xFFFF)
  - An index/TC event occurred (value is not equal to either ‘0’ or 0xFFFF)
- The DOWN bit field of counter status (TCPWM_CNTx_STATUS) register can be read to determine the current counting direction. Value '0' indicates a previous increment operation and value '1' indicates previous decrement operation. **Figure 19-9** illustrates quadrature behavior in the X1 encoding mode.
  - A positive edge on phiA increments the counter when phiB is '0' and decrements the counter when phiB is '1'
  - The count register is initialized with the period value on an index/reload event
  - Terminal count is generated when the counter is initialized by index event. This event can be used to generate an interrupt
  - When the count register reaches 0xFFFF (the maximum count register value), the count register value is copied to the capture register and the count register is initialized with period value (0x8000)

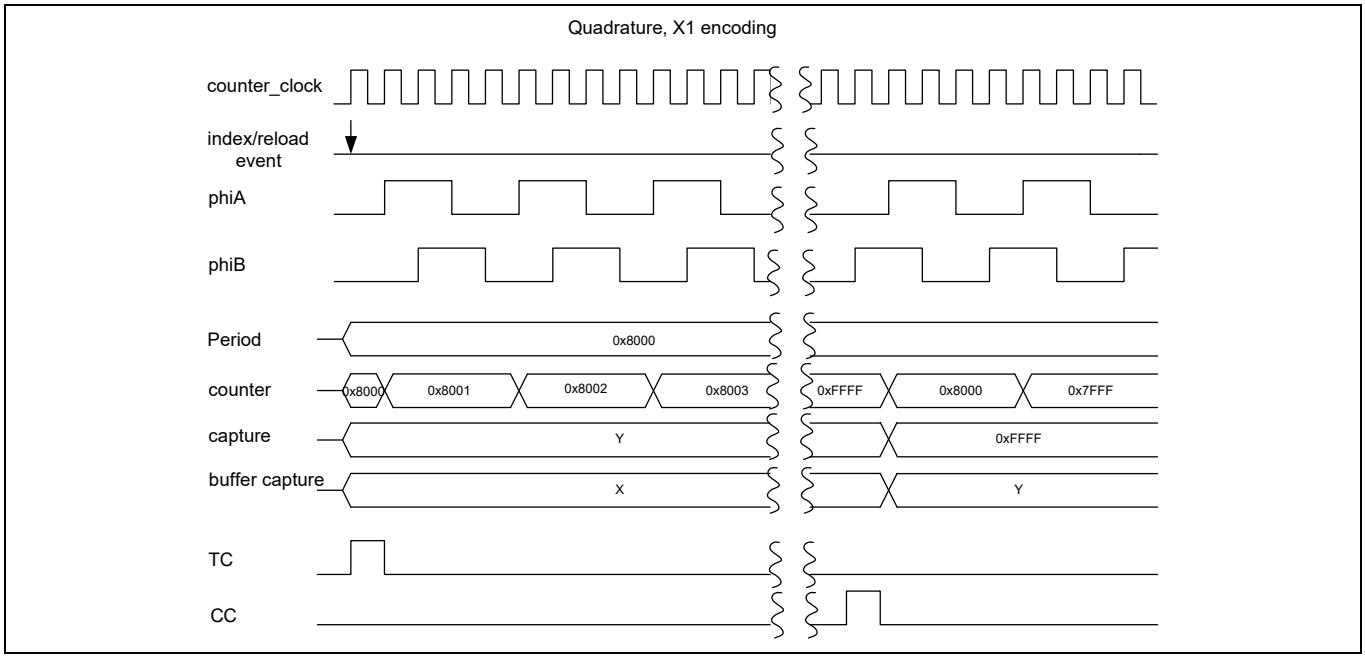


Figure 19-9. Timing diagram for quadrature mode, X1 e

The quadrature phases are detected on the counter_clock. Within a single counter period, the phases should not change value more than once.

The X2 and X4 quadrature encoding modes count twice and four times as fast as the X1 encoding mode.

Figure 19-10 illustrates the quadrature mode behavior in the X2 and X4 encoding modes.

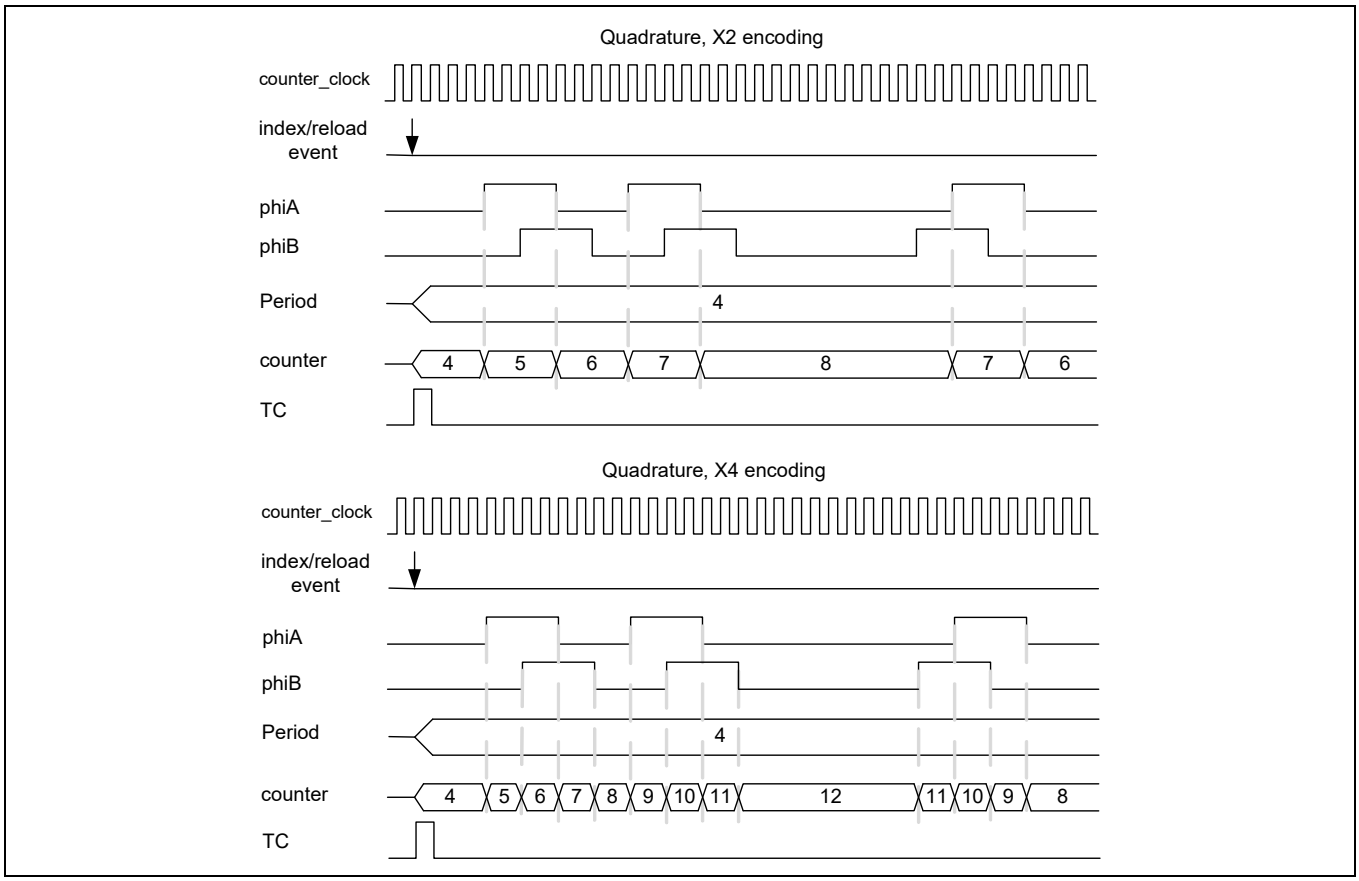


Figure 19-10. Timing diagram for quadrature mode, X2 and X4 encoding

19.3.3.3 Configuring counter for quadrature mode

The steps to configure the counter for quadrature mode of operation and the affected register bits are as follows.

1. Disable the counter by writing '0' to the COUNTER_ENABLED field of the TCPWM_CTRL register
2. Select Quadrature mode by writing '011' to the MODE[26:24] field of the TCPWM_CNTx_CTRL register
3. Set the required 16-bit period in the TCPWM_CNTx_PERIOD register
4. Set the required encoding mode by writing to the QUADRATURE_MODE[21:20] field of the TCPWM_CNTx_CTRL register
5. Set the TCPWM_CNTx_TR_CTRL0 register to select the trigger that causes the event (Index and Stop)
6. Set the TCPWM_CNTx_TR_CTRL1 register to select the edge that causes the event (Index and Stop)
7. If required, set the interrupt upon TC or CC condition, as shown in **"Interrupts"** on page 116
8. Enable the counter by writing '1' to the COUNTER_ENABLED field of the TCPWM_CTRL register

19.3.4 Pulse width modulation (PWM) mode

The PWM mode is also called the Digital Comparator mode. The comparison output is a PWM signal whose period depends on the period register value and duty cycle depends on the compare and period register values.

PWM period = (period value/counter clock frequency) in left- and right-aligned modes

PWM period = (2 × (period value/counter clock frequency)) in center-aligned mode

Duty cycle = (compare value/period value) in left- and right-aligned modes

Duty cycle = ((period value-compare value)/period value) in center-aligned mode

19.3.4.1 Block diagram

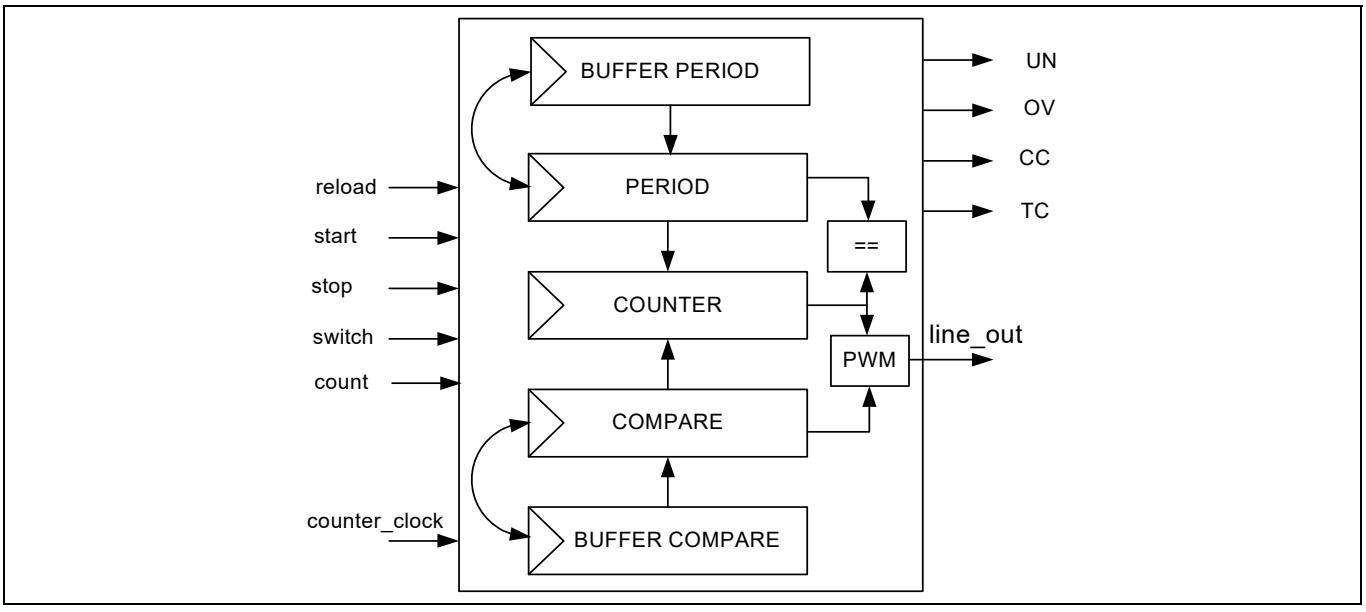


Figure 19-11. PWM mode block diagram

19.3.4.2 How it works

The PWM mode can output left, right, center, or asymmetrically aligned PWM signals. The desired output alignment is achieved by using the counter's up, down, and up/down counting modes selected using UP_DOWN_MODE [17:16] bits in the TCPWM_CNTx_CTRL register, as shown in **Table 19-6**.

This CC signal along with OV and UN signals control the PWM output line. The signals can toggle the output line or set it to a logic '0' or '1' by configuring the TCPWM_CNTx_TR_CTRL2 register. By configuring how the signals impact the output line, the desired PWM output alignment can be obtained.

The recommended way to modify the duty cycle is:

- The buffer period register and buffer compare register are updated with new values
- On TC, the period and compare registers are automatically updated with the buffer period and buffer compare registers when there is an active switch event. The AUTO_RELOAD_CC and AUTO_RELOAD_PERIOD fields of the counter control register are set to '1'. When a switch event is detected, it is remembered until the next TC event. Pass through signal (selected during event detection setting) cannot trigger a switch event
- Updates to the buffer period register and buffer compare register should be completed before the next TC with an active switch event; otherwise, switching does not reflect the register update, as shown in **Figure 19-13**

In the center-aligned mode, the output line is set to '0' at Terminal Count and toggled at the CC condition.

At the reload event, the count register is initialized and starts counting in the appropriate mode. At every count, the count register value is compared with compare register value to generate the CC signal on match.

Figure 19-12 illustrates center-aligned PWM with buffered period and compare registers (up/down counting mode 0).

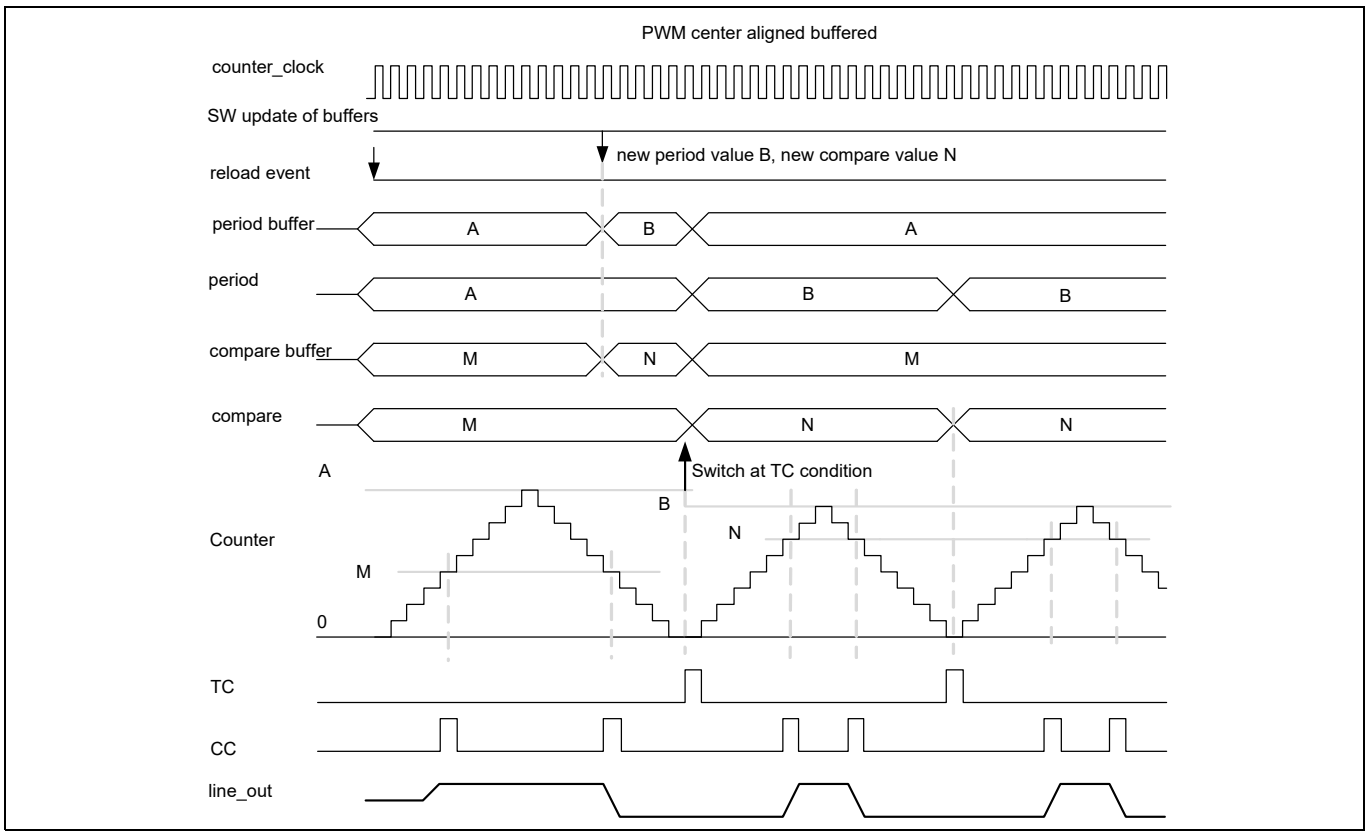


Figure 19-12. Timing diagram for center aligned PWM

Figure 19-13 illustrates center-aligned PWM with software generated switch events:

- Software generates a switch event only after both the period buffer and compare buffer registers are updated
- Because the updates of the second PWM pulse come late (after the terminal count), the first PWM pulse is repeated
- Note that the switch event is automatically cleared by hardware at TC after the event takes effect

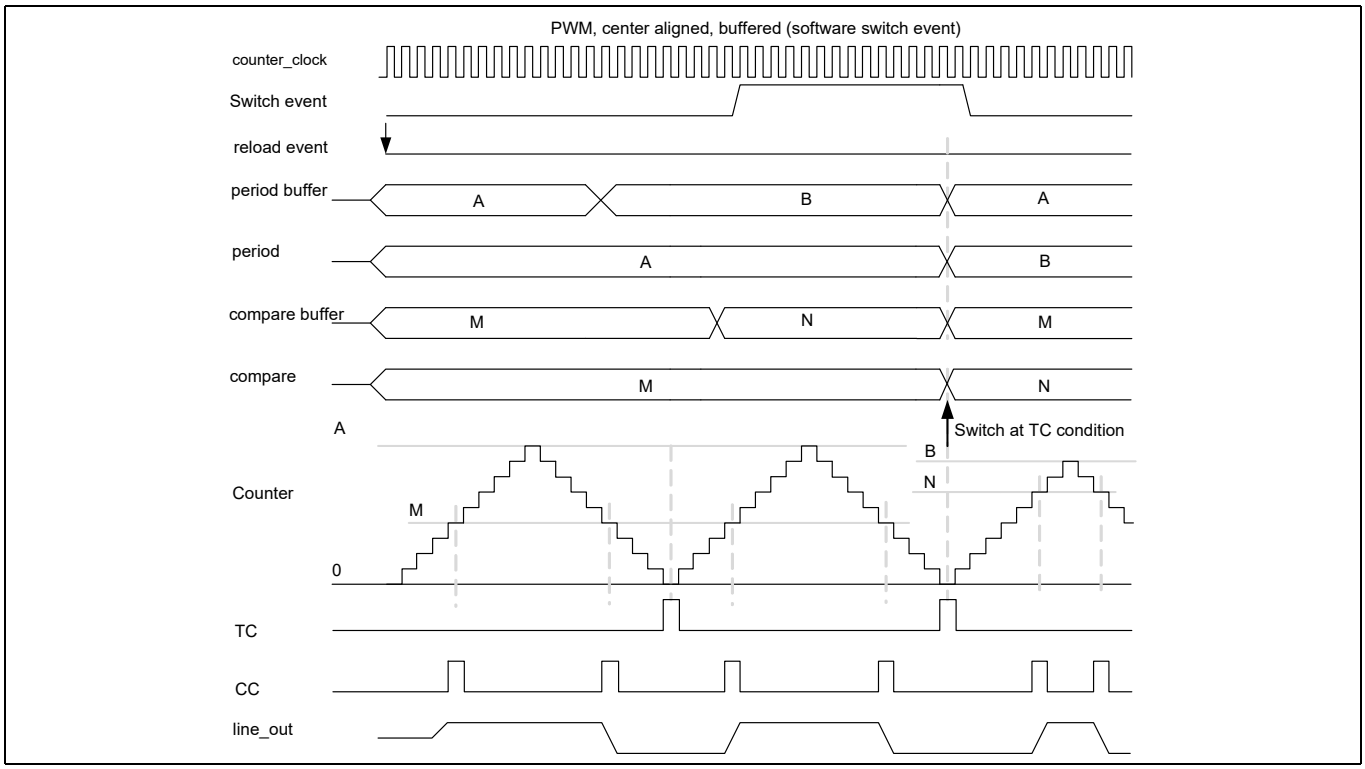


Figure 19-13. Timing diagram for center aligned PWM (software switch event)

19.3.4.3 Other configurations

- For asymmetric PWM, the up/down counting mode 1 should be used. This causes a TC when the counter reaches either ‘0’ or the period value. To create an asymmetric PWM, the compare register is changed at every TC (when the counter reaches either ‘0’ or the period value), whereas the period register is only changed at every other TC (only when the counter reaches ‘0’)
- For left-aligned PWM, use the up counting mode; configure the OV condition to set output line to '1' and CC condition to reset the output line to '0'. See **Table 19-3**
- For right-aligned PWM, use the down counting mode; configure UN condition to reset output line to '0' and CC condition to set the output line to '1'. See **Table 19-3**

19.3.4.4 Kill feature

A kill feature gives the ability to disable the output line immediately. This event can be programmed to stop the counter by modifying the PWM_STOP_ON_KILL and PWM_SYNC_KILL fields of the counter control register, as shown in **Table 19-7**.

Table 19-7. Field setting for stop on kill feature

PWM_STOP_ON_KILL field	Comments
0	The kill trigger temporarily blocks the PWM output line but the counter is still running.
1	The kill trigger temporarily blocks the PWM output line and the counter is also stopped.

The kill event can be programmed to be asynchronous or synchronous, as shown in **Table 19-8**.

Table 19-8. Field setting for synchronous/asynchronous kill

PWM_SYNC_KILL Field	Comments
0	An asynchronous kill event lasts as long as it is present. This event requires pass through mode.
1	A synchronous kill event disables the output lines until the next TC event. This event requires rising edge mode.

In the synchronous kill, PWM cannot be started before the next TC. To restart the PWM immediately after kill input is removed, kill event should be asynchronous (see **Table 19-8**). The generated stop event disables the output line. In this case, the reload event can use the same trigger input signal but should be used in falling edge detection mode.

19.3.4.5 Configuring counter for PWM mode

The steps to configure the counter for the PWM mode of operation and the affected register bits are as follows:

1. Disable the counter by writing '0' to the COUNTER_ENABLED field of the TCPWM_CTRL register.
2. Select PWM mode by writing '100' to the MODE[26:24] field of the TCPWM_CNTx_CTRL register.
3. Set clock prescaling by writing to the GENERIC[10:8] field of the TCPWM_CNTx_CTRL register, as shown in **Table 19-1**.
4. Set the required 16-bit period in the TCPWM_CNTx_PERIOD register and the buffer period value in the TCPWM_CNTx_PERIOD_BUFF register to switch values, if required
5. Set the 16-bit compare value in the TCPWM_CNTx_CC register and the buffer compare value in the TCPWM_CNTx_CC_BUFF register to switch values, if required
6. Set the direction of counting by writing to the UP_DOWN_MODE[17:16] field of the TCPWM_CNTx_CTRL register to configure left-aligned, right-aligned, or center-aligned PWM, as shown in **Table 19-6**.
7. Set the PWM_STOP_ON_KILL and PWM_SYNC_KILL fields of the TCPWM_CNTx_CTRL register as required.
8. Set the TCPWM_CNTx_TR_CTRL0 register to select the trigger that causes the event (Reload, Start, Kill, Switch, and Count)
9. Set the TCPWM_CNTx_TR_CTRL1 register to select the edge that causes the event (Reload, Start, Kill, Switch, and Count)
10. line_out can be controlled by the TCPWM_CNTx_TR_CTRL2 register to set, reset, or invert upon CC, OV, and UN conditions
11. If required, set the interrupt upon TC or CC condition, as shown in **"Interrupts"** on page 116.
12. Enable the counter by writing '1' to the COUNTER_ENABLED field of the TCPWM_CTRL register. A start trigger must be provided through firmware (TCPWM_CMD register) to start the counter if the hardware start signal is not enabled

19.3.5 Pulse width modulation pseudo-random mode

This mode uses the linear feedback shift register (LFSR). LFSR is a shift register whose input bit is a linear function of its previous state.

19.3.5.1 Block diagram

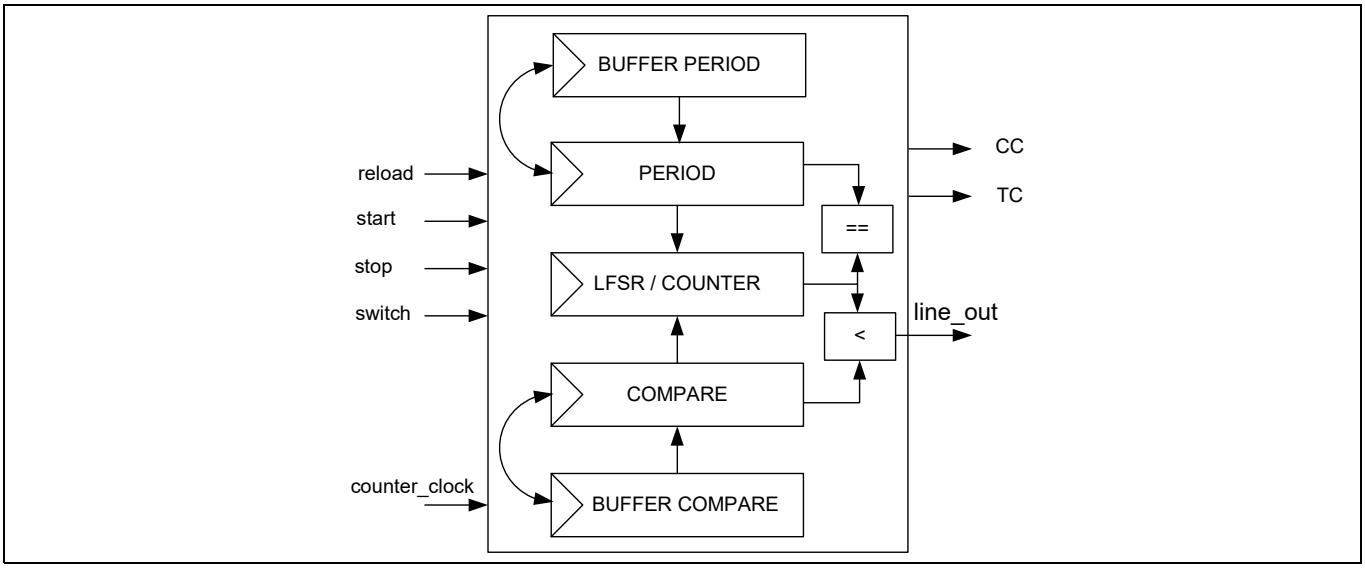


Figure 19-14. PWM-PR mode block diagram

19.3.5.2 How it works

The counter register is used to implement LFSR with the polynomial: $x^{16}+x^{14}+x^{13}+x^{11}+1$, as shown in **Figure 19-15**. It generates all the numbers in the range [1, 0xFFFF] in a pseudo-random sequence. Note that the counter register should be initialized with a non-zero value.

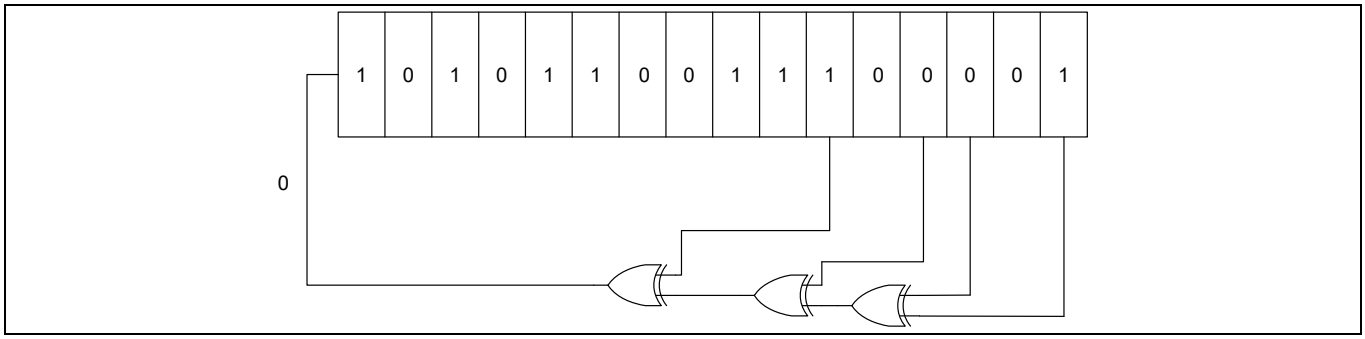


Figure 19-15. Pseudo-Random Sequence Generation using Counter Register

The following steps describe the process:

- The PWM output line ‘line_out’ is driven with '1' when the lower 15-bit value of the counter register is smaller than the value in the compare register (when counter[14:0] < compare[15:0]). A compare value of ‘0x8000’ or higher always results in a '1' on the PWM output line. A compare value of ‘0’ always results in a '0' on the PWM output line
- A reload event behaves similar to a start event; however, it does not initialize the counter
- Terminal count is generated when the counter value equals the period value. LFSR generates a predictable pattern of counter values for a certain initial value. This predictability can be used to calculate the counter

value after a certain amount of LFSR iterations ‘n’. This calculated counter value can be used as a period value and the TC is generated after ‘n’ iterations
- At TC, a switch/capture event conditionally switches the compare and period register pairs (based on the AUTO_RELOAD_CC and AUTO_RELOAD_PERIOD fields of the counter control register)
- A kill event can be programmed to stop the counter as described in previous sections
- One shot mode can be configured by setting the ONE_SHOT field of the counter control register. At terminal count, the counter is stopped by hardware
- In this mode, underflow, overflow, and trigger condition events do not occur
- CC condition occurs when the counter is running and its value equals compare value. **Figure 19-16** illustrates pseudo-random noise behavior
- A compare value of 0x4000 results in 50% duty cycle (only the lower 15 bits of the 16- bit counter are used to compare with the compare register value)

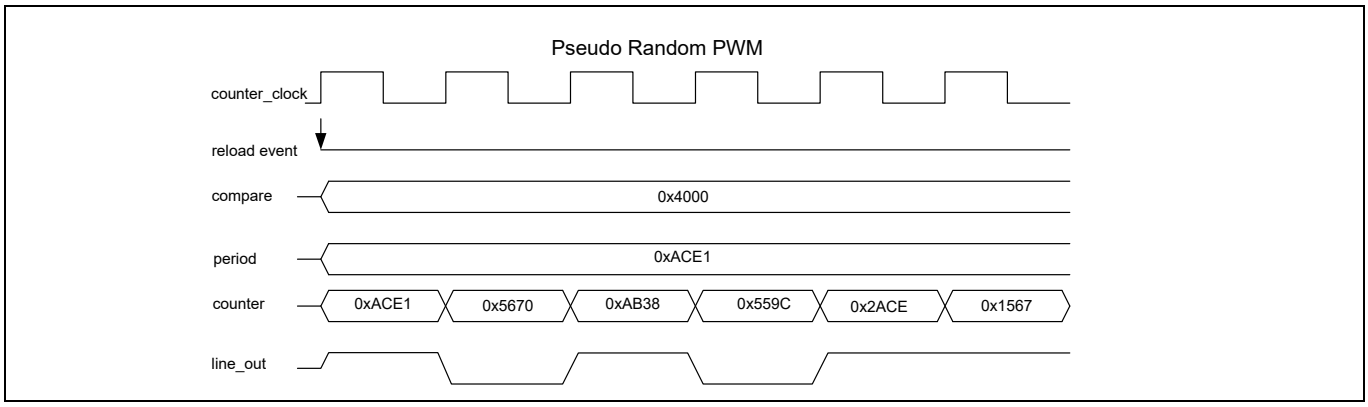


Figure 19-16. Timing diagram for pseudo-random PWM

A capture/switch input signal may switch the values between the compare and compare buffer registers and the period and period buffer registers. This functionality can be used to modulate between two different compare values using a trigger input signal to control the modulation.

Note: Capture/switch input signal can only be triggered by an edge (rising, falling, or both). This input signal is remembered until the next terminal count.

19.3.5.3 Configuring counter for pseudo-random PWM mode

The steps to configure the counter for pseudo-random PWM mode of operation and the affected register bits are as follows.

1. Disable the counter by writing '0' to the COUNTER_ENABLED field of the TCPWM_CTRL register
2. Select pseudo-random PWM mode by writing '110' to the MODE[26:24] field of the TCPWM_CNTx_CTRL register
3. Set the required period (16 bit) in the TCPWM_CNTx_PERIOD register and buffer period value in the TCPWM_CNTx_PERIOD_BUFF register to switch values, if required
4. Set the 16-bit compare value in the TCPWM_CNTx_CC register and the buffer compare value in the TCPWM_CNTx_CC_BUFF register to switch values
5. Set the PWM_STOP_ON_KILL and PWM_SYNC_KILL fields of the TCPWM_CNTx_CTRL register as required
6. Set the TCPWM_CNTx_TR_CTRL0 register to select the trigger that causes the event (Reload, Start, Kill, and Switch)
7. Set the TCPWM_CNTx_TR_CTRL1 register to select the edge that causes the event (Reload, Start, Kill, and Switch)

8. line_out can be controlled by the TCPWM_CNTx_TR_CTRL2 register to set, reset, or invert upon CC, OV, and UN conditions
9. If required, set the interrupt upon TC or CC condition, as shown in **"Interrupts"** on page 116
10. Enable the counter by writing '1' to the COUNTER_ENABLED field of the TCPWM_CTRL register

19.4 TCPWM registers

Table 19-9. List of TCPWM registers

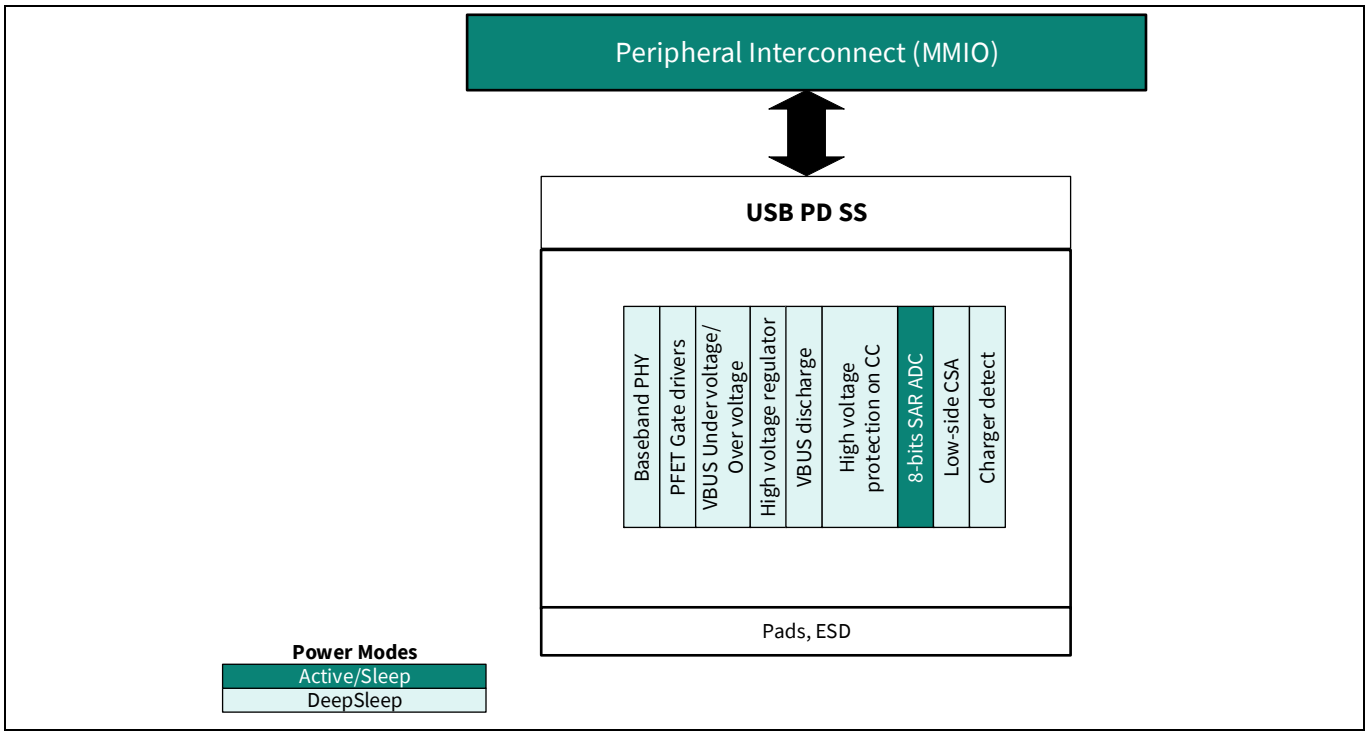
Register name	Comment	Features
TCPWM_CTRL	TCPWM control register	Enables the counter block
TCPWM_CMD	TCPWM command register	Generates software events
TCPWM_INTR_CAUSE	TCPWM counter interrupt cause register	Determines the source of the combined interrupt signal
TCPWM_CNTx_CTRL	Counter control register	Configures counter mode, encoding modes, one shot mode, switching, kill feature, dead time, clock prescaling, and counting direction
TCPWM_CNTx_STATUS	Counter status register	Reads the direction of counting, dead time duration, and clock prescaling; checks if counter is running
TCPWM_CNTx_COUNTER	Count register	Contains the 16-bit counter value
TCPWM_CNTx_CC	Counter compare/capture register	Captures the counter value or compares the value with the counter value
TCPWM_CNTx_CC_BUFF	Counter buffered compare/capture register	Buffer register for counter CC register; switches compare value
TCPWM_CNTx_PERIOD	Counter period register	Contains upper value of the counter
TCPWM_CNTx_PERIOD_BUFF	Counter buffered period register	Buffer register for counter period register; switches period value
TCPWM_CNTx_TR_CTRL0	Counter trigger control register 0	Selects trigger for specific counter events
TCPWM_CNTx_TR_CTRL1	Counter trigger control register 1	Determines edge detection for specific counter input signals
TCPWM_CNTx_TR_CTRL2	Counter trigger control register 2	Controls counter output lines upon CC, OV, and UN conditions
TCPWM_CNTx_INTR	Interrupt request register	Sets the register bit when TC or CC condition is detected
TCPWM_CNTx_INTR_SET	Interrupt set request register	Sets the corresponding bits in the interrupt request register
TCPWM_CNTx_INTR_MASK	Interrupt mask register	Mask for interrupt request register
TCPWM_CNTx_INTR_MASKED	Interrupt masked request register	Bitwise AND of interrupt request and mask registers

Section F: Universal serial bus (USB) Power Delivery (PD)

This section encompasses the following chapter:

- **"Universal serial bus (USB) Power Delivery (PD)"** on page 133

Top-level architecture



21 Universal serial bus (USB) Power Delivery (PD)

The EZ-PD™ PMG1-S0 MCU device uses a built-in USB Power Delivery (USB PD) block that supports all features as per USB Power Delivery specification 3.0 and USB Type-C cable and connector specification rev 1.0. This block supports Type-C cable and baseband USB-PD communication. It is configurable for upstream facing port (UFP), downstream facing port (DFP), dual role port (DRP), and powered cable accessory roles. It has a low-side current sense amplifier for use with an external resistor.

The USB PD block also has a gate driver circuit to drive an external PMOS-based power FET, which has current carrying capability up to 5 A and supports voltages up to 30 V. A 30-V to 3-V regulator is available with 20-V IEC ESD protection. It also consists of programmable under-voltage/over-voltage detectors from 3 V to 30 V. This block offers 8-kV IEC ESD protection for 30 VVBUS and 5 V on CC1 and CC2. It also consists of a shunt regulator for feedback to the primary side of the power plant loop for typical power adapter applications.

21.1 Features

- The USB-PD block of the EZ-PD™ PMG1-S0 devices provides power adapter functional blocks and adds 30 V tolerance for key functional blocks
- The ADC block is an 8-bit SAR ADC, which can measure the voltage on either of the AMUX buses, measure the supply voltage level, or measure the on-die temperature
- The charge pump block generates the gate voltage for NMOS back-power protection devices
- The super high voltage regulator (SHV_REG) block provides the original CC transceiver in a modified layout aspect ratio to provide more flexibility for top-level chip floor planning
- The CHGDET block implements battery charger emulation and detection for USB BC.1.2, Apple charge, and Qualcomm quick charge protocols
- The DPSLP_REF block implements voltage and current references, which are used by all other public cells of the IP
- The ERROR_AMP (error amplifier) block provides the means to function as a shunt regulator or as a feedback controller used in power adaptor applications
- A set of ESD-protection blocks are included as part of the USBPD block
- The Low-side current sense amplifier (CSA) block provides low-side current sense capability for general-purpose over-current protection (OCP) and analog current control for power adapter applications
- The SHV_REG block uses the USB Vbus input to generate a 3.3 V power supply output
- The UVOV block implements an undervoltage/overvoltage (UVOV) detection circuit for the VBUS supply. The thresholds for both OCP and UVOV are programmable
- The programmable VBUS discharge (VBUS_DISCHG_PROG) block pulls the connected USB VBUS supply to a programmable target voltage level when activated
- The VBUS discharge (VBUS_DISCHG) block pulls the connected USB VBUS supply to 0 V when activated
- The REFGEN block generates voltage references needed by the other sub-blocks within the USBPD block

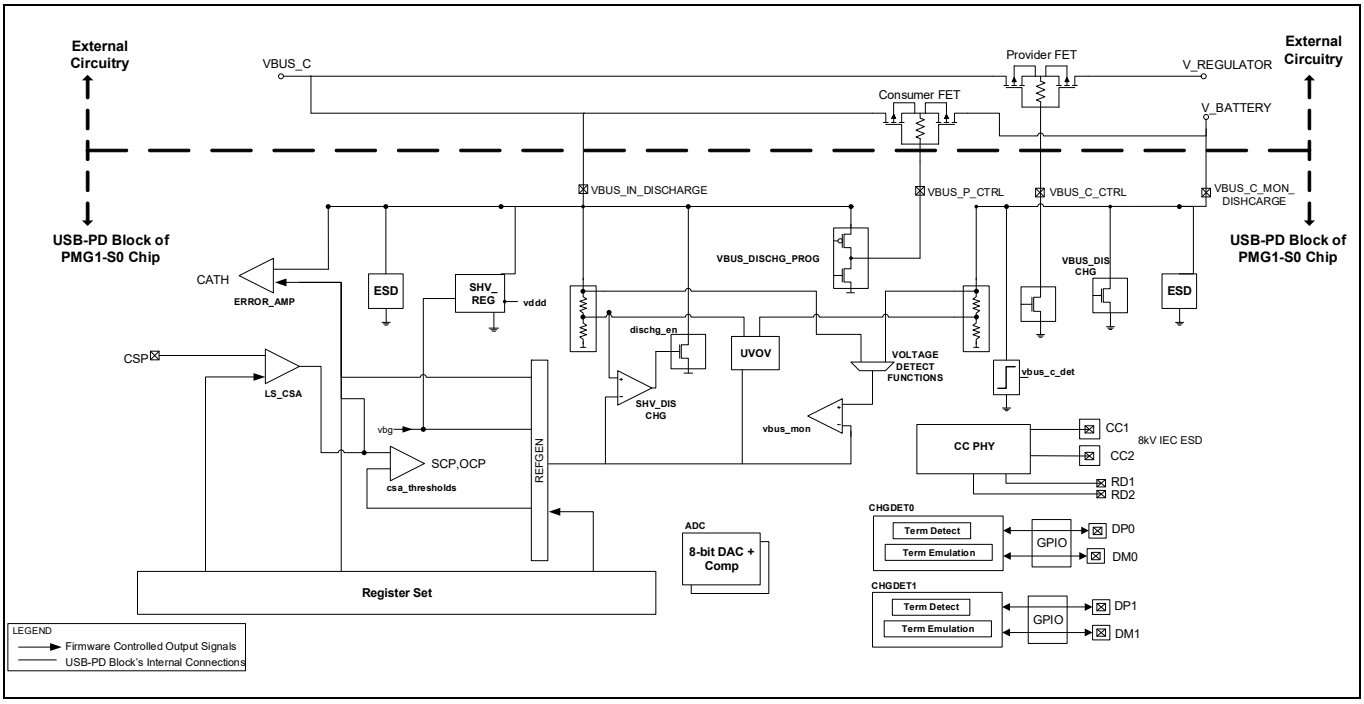


Figure 21-1. USB PD block diagram

21.1 Block applications

21.2 ADC block

21.2.1 ADC block architecture and functional overview

This block contains the analog circuitry necessary to implement an 8-bit Successive Approximation Register (SAR) ADC. The block contents are: control logic for level shifting and power down, 8-bit DAC, DFT switch, comparator (COMP), and a BJT NPN device, as shown in **Figure 16-2**.

The DAC takes an 8-bit control signal and outputs a voltage referenced to the supply voltage. The comparator compares the DAC voltage versus one of the following input voltages: either the amux_a or amux_b line, the bandgap voltage (vbg), or the voltage generated from sourcing current into a diode-connected BJT NPN device. If the DAC voltage potential is greater than the multiplexed voltage, then the comparator digital output is high. The BJT NPN device may be used as a temperature sensor as well.

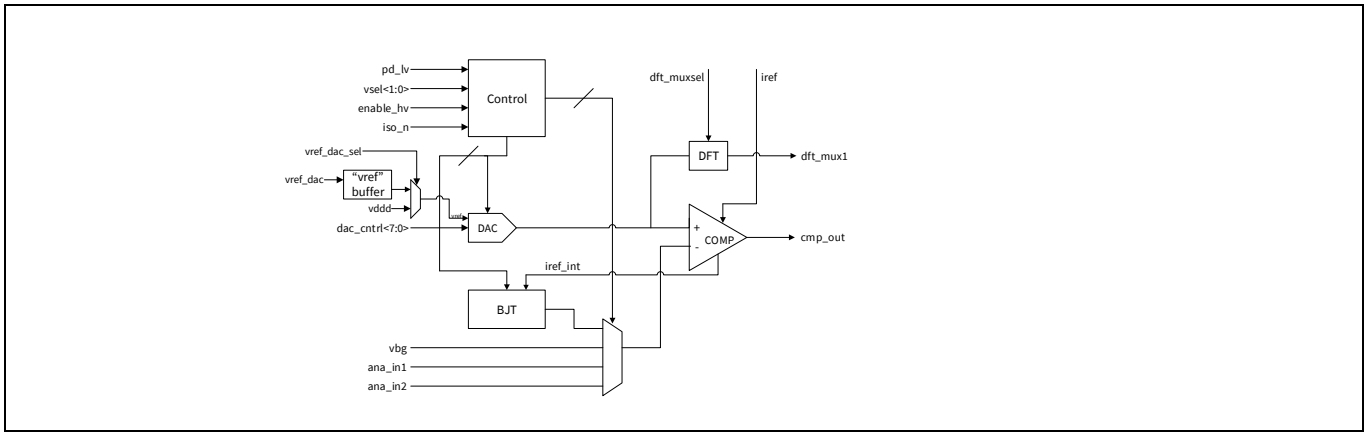


Figure 21-2. ADC block diagram

21.2.2 CC Block

21.2.2.1 CC block architecture and functional overview

The CC block, as shown in **Figure 21-3**, contains the USB PD transceiver for baseband signaling communication over the CC1 and CC2 lines. The transmitter (TX) drives 1.125 V slew-rate controlled data onto the chosen CC line. The receiver (RX) converts received data on the chosen CC line to a full-rail signal for decoding. The comparator (COMP) block contains two deep-sleep comparators to detect attach/detach and CC line activity events, and determine the voltage range on the chosen CC line. The idle voltage on the CC lines is generated by the voltage divider of the pull-up and pull-down termination, which indicates the advertised current capability of the DFP. The reference generator block generates the necessary voltages for the transmitter voltage, receiver threshold, and comparator thresholds.

The IPU blocks generate current sources for the pull up termination on the CC lines and they are configurable to indicate which current profile the DFP or DRP supports.

The Rd pull-down resistors are used for the UFP termination. When no power is present, the dead battery termination is presented by the Rd_db pull-down resistors. The dead battery termination is available only on certain part numbers. Refer to the CCG3PA device datasheet for more information.

Figure 21-3 shows the possible configuration options that support different Type-C applications. The DFP does not need any pull-down termination, so the chip level CC1 and CC2 pins are connected to the block's "cc1" and "cc2" ports. The UFP and DRP applications need to have Rd termination on the CC1 and CC2 pins, so they are additionally connected to the "rd1_term" and "rd2_term" ports.

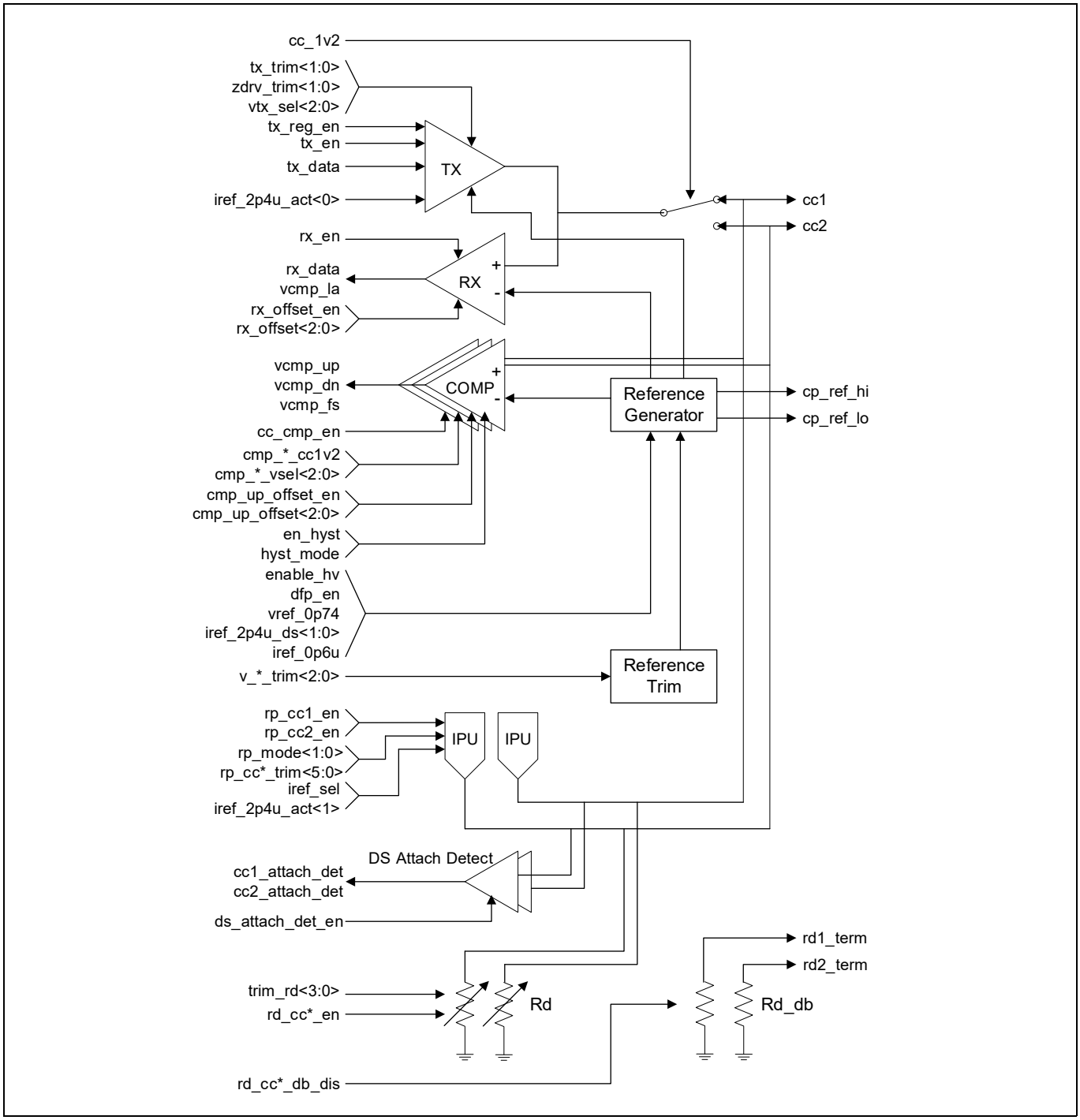


Figure 21-3. CC block diagram

21.2.3 CHGDET block

21.2.3.1 CHGDET block architecture and functional overview

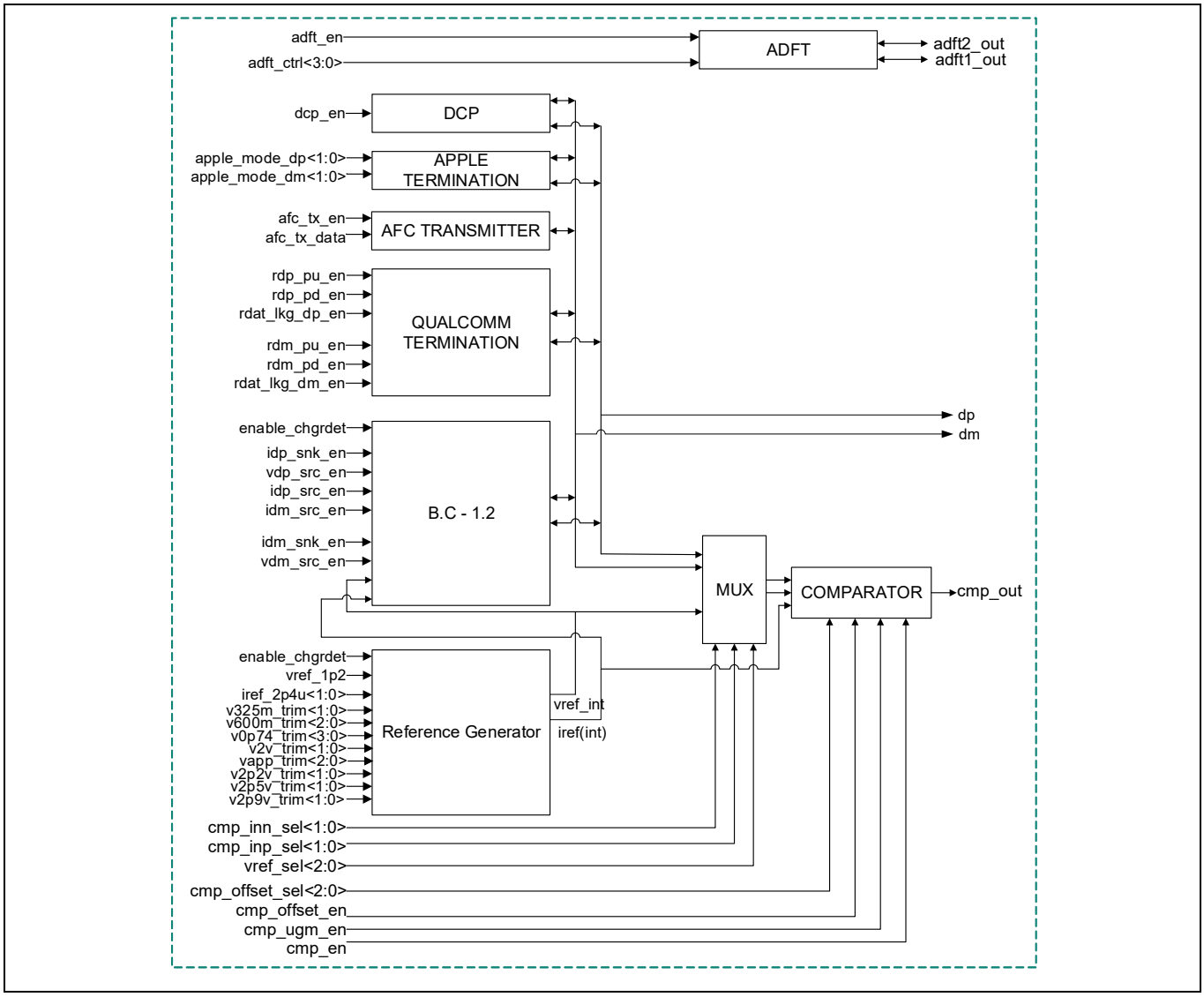


Figure 21-4. CHGDET block diagram

Figure 21-4 shows the charger detect (CHGDET) block top level architecture diagram. This block implements a charger detection circuit that is compliant with the BC 1.2 specification.

21.2.4 Low-side CSA block

21.2.4.1 Low-side CSA block architecture and functional overview

This block provides the following:

- The current sense amplifier translates a differential signal across signals "inp" and "vgnd" to a ground referenced signal, "out_analog". The CSA senses a voltage on the low side of the VBUS path, referenced to ground. This voltage will be used for the following primary functions in the USBPD system
- To provide analog feedback to the FB node for a direct charging application in constant current mode. In this application, the analog output, out1, is compared to a reference, Vref; the difference is amplified by an error amplifier. This output is translated to a current that manipulates the FB node to change the voltage on VBUS, thereby maintaining constant current on VBUS
- For over-current protection where the analog output, out1 is compared against a reference to generate a digital output, out_d

Four comparators are in place to provide simultaneous detection of different levels of current. They are used for the following purposes:

- **SCP**: Short-circuit protection for high levels of current
- **OCP**: Overcurrent protection to trigger current levels that are a certain percentage over the expected current
- **PFC**: Power factor correction will require two comparators to trigger at ON and OFF points. PFC disable and enable will have thresholds higher and lower than that for OCP
- **SR**: Synchronous rectifier enable and disable, used at very low current levels, potentially around 10 percent of the nominal current

Figure 21-5 shows the block diagram of Low-side CSA block.

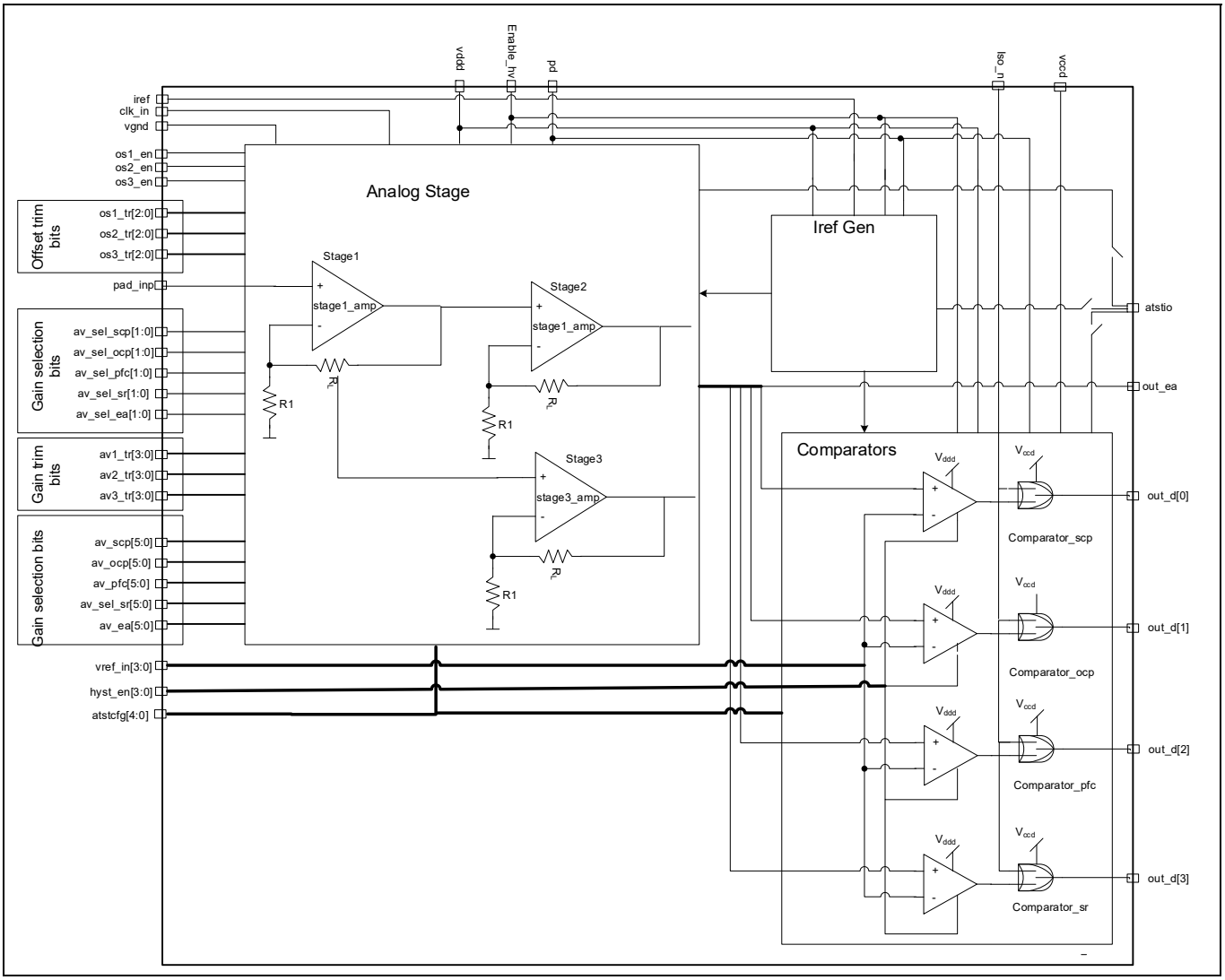


Figure 21-5. Low-side CSA block diagram

Since these comparators must be used simultaneously, the analog gain stage provides different gain options for each of the modes, along with a separate gain option and output to be used by the error amplifier in constant current mode.

The comparator block consists of five comparators that compare the respective analog outputs (out_ea, out_scp, out_ocp, out_sr, and out_pfc) to reference signals vref_in[3:0] to generate a digital output, comp_out[3:0].

21.2.5 PGDO block

21.2.5.1 PGDO block architecture and functional overview

The PGDO block is also referred to as the Gate Driver block. **Figure 21-6** shows the block diagram of the PMOS power-FET gate driver block. This is a simple programmable current sink.

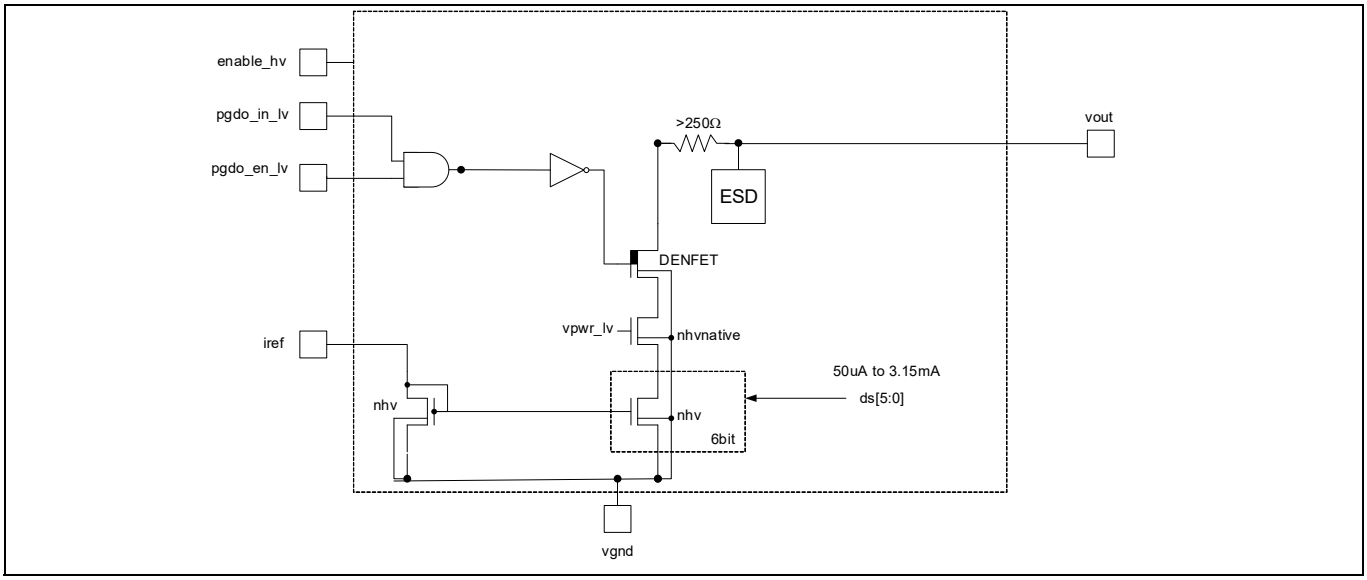


Figure 21-6. PGDO block diagram

In addition to the pull-up function, the PGDO pull-up block has a pull-down function, which ensures that the external PFET will turn OFF quickly.

21.2.6 REFGEN block

21.2.6.1 REFGEN functional description

The reference generator block provides an additional layer of reference signal derivation by providing the following:

- Common selection of the source Vref signal to be either the bandgap (1.2 V) or beta-multiplier (0.74 V) reference
- Voltage, current, and clock reference signals necessary to support the following blocks:
  - ERROR_AMP block
  - Low-side CSA block
  - ADC block
  - PROG_DISCHG block
  - UVOV block

Figure 21-7 shows how these blocks interface with each other.

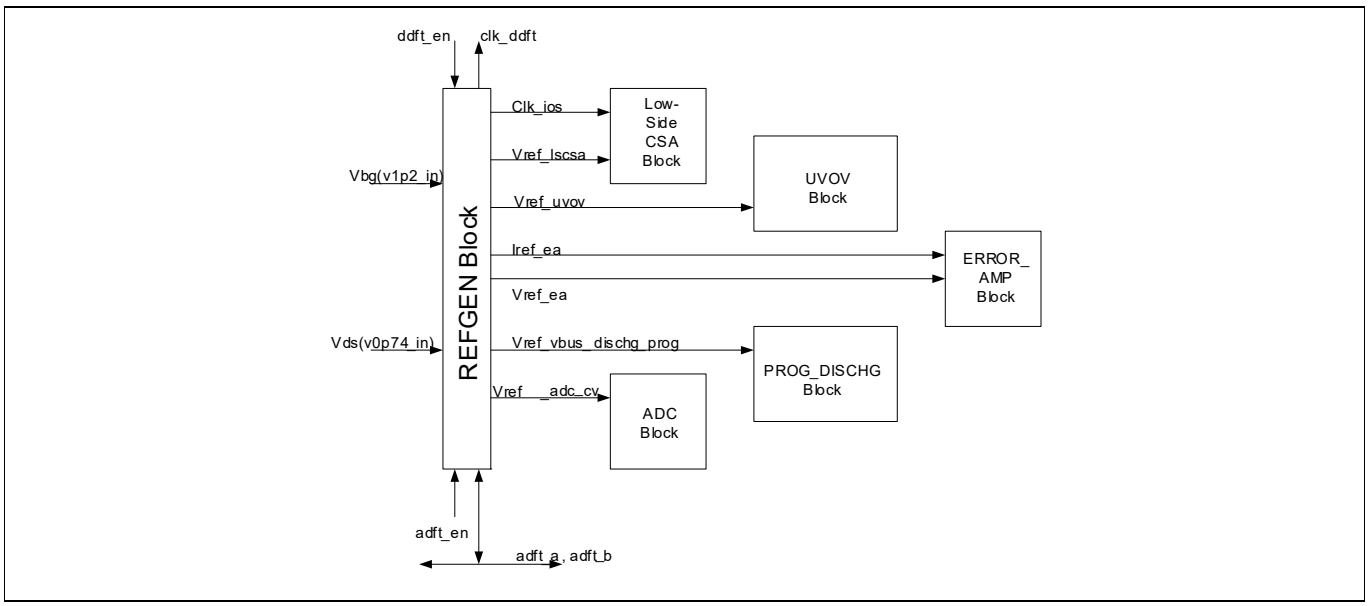


Figure 21-7. REFGEN block interface diagram

21.2.7 SHV_REG block

21.2.7.1 SHV_REG block architecture and functional overview

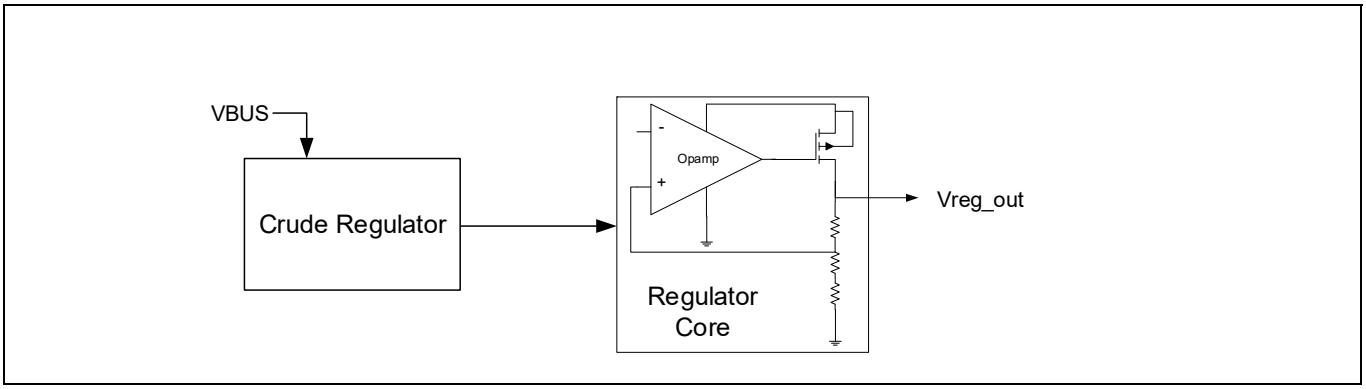


Figure 21-8. SHV_REG block diagram

Figure 21-8 shows the block diagram of the SHV_REG block. As per the USB PD specifications, VBUS can go from 3.75 V to 22 V. The regulator system has the following components:

- **Crude regulator** – This block gives a crude output voltage of minimum 2 V whenever VBUS is ON. This guarantees that the downstream blocks will receive power and there is no startup issue
- **Regulator core** – The regulator core is a low dropout-based architecture with the PMOS pass element. A typical regulator output is 3.3 V; it uses an internal reference voltage of 0.74 V. The load compensation scheme is used to attain stability with a 1.1 µF external capacitor. A source follower stage is added to improve the overall phase margin

21.2.8 UVOV block

21.2.8.1 UVOV block architecture and functional description

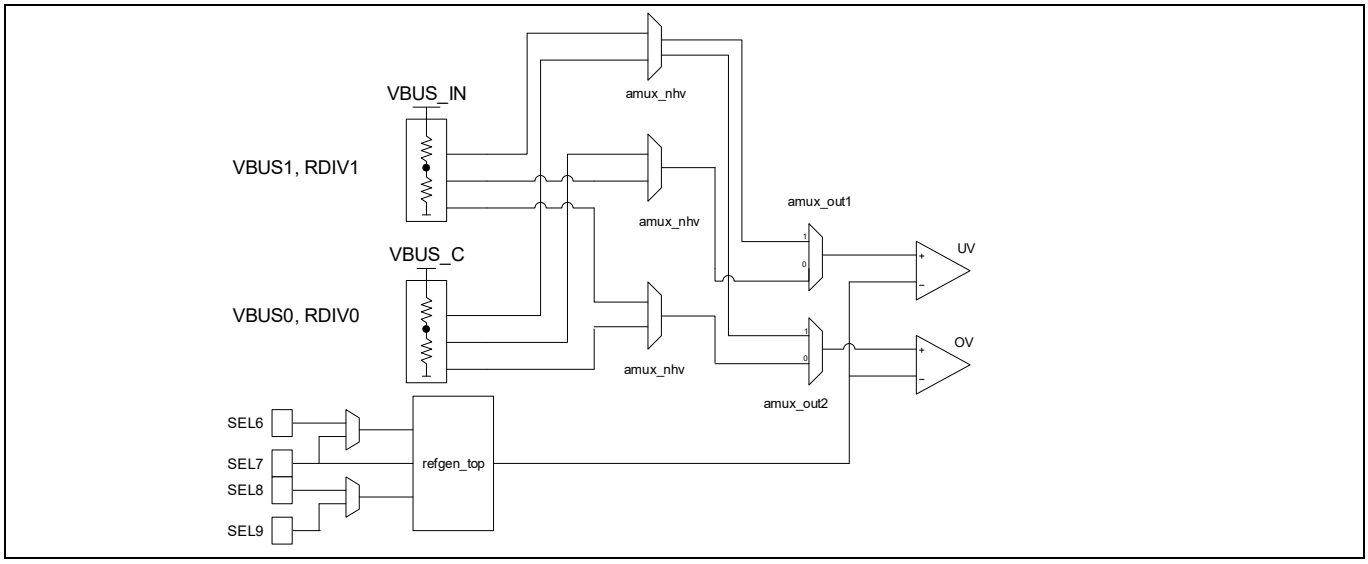


Figure 21-9. UVOV block diagram

Figure 21-9 shows how the UVOV block is used to detect the over-voltage and under-voltage conditions on the VBUS input line. The threshold levels for UV and OV detection can be set independent of each other. Both UV and OV detectors have programmable thresholds and can be programmed from 64 available values.

A single resistor string from VBUS is used to drop the voltage from VBUS down to '0'. The 6-bit input for both UV and OV is decoded in the LV domain and the outputs are level-shifted. The level-shifted output chooses one of the switches from the resistor string. The output from the switch is applied to the comparator. The comparator compares the switch output to a fixed voltage of 0.74 V.

21.2.9 VBUS_DISCHG_PROG block

21.2.9.1 VBUS_DISCHG_PROG block architecture and functional overview

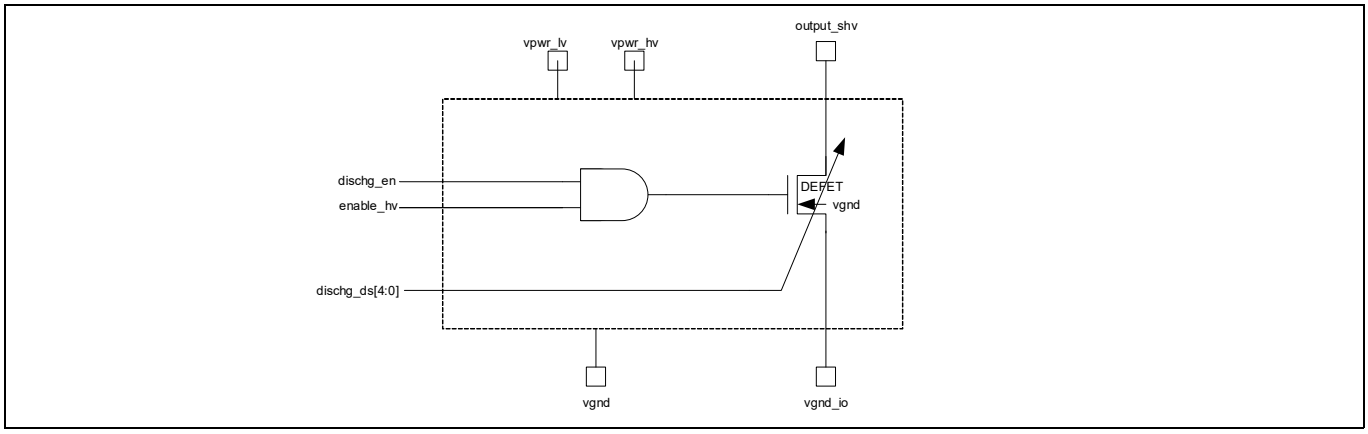


Figure 21-10. VBUS_DISCHG_PROG block diagram

Figure 21-10 shows the block diagram of the VBUS_DISCHG_PROG block, which has a 24.5-V drain extended NFET connected from VBUS supply to ground. There is an additional resistor ladder and a comparator that tracks the value of VBUS. VBUS can be discharged to the value set by dischg_ds[4:0].

21.2.10 VBUS_DISCHG block

21.2.10.1 VBUS_DISCHG block architecture and functional overview

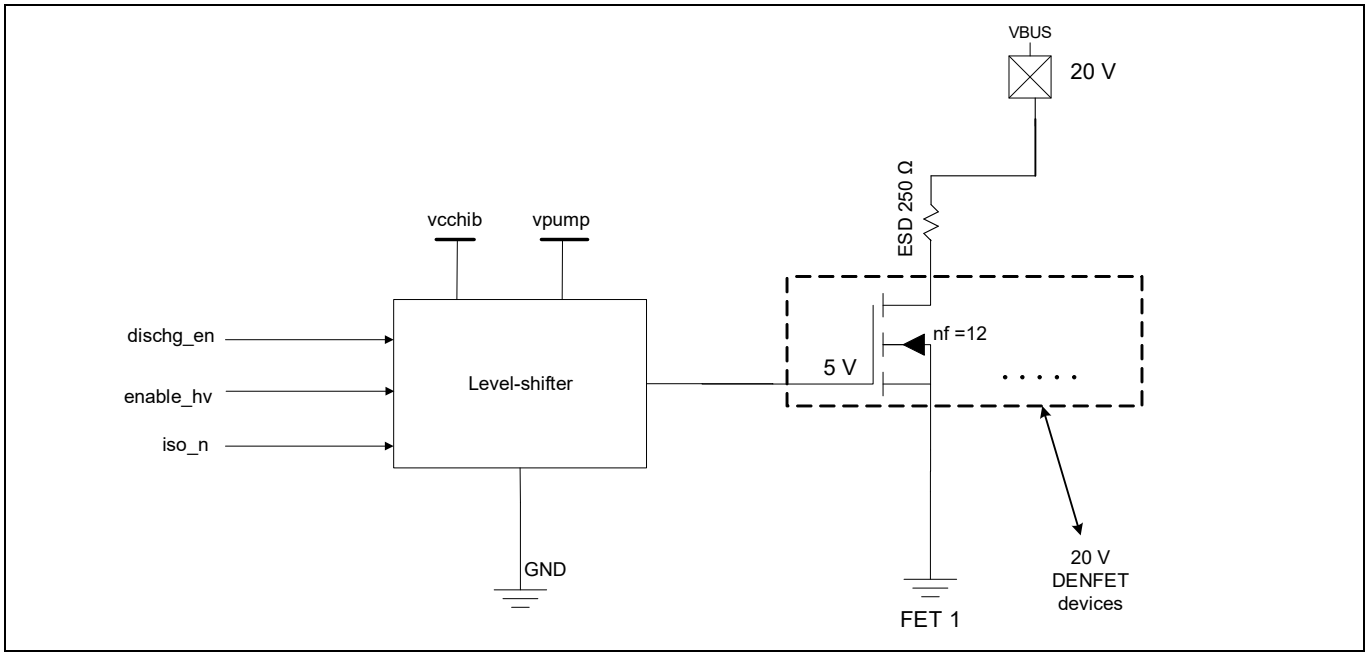


Figure 21-11. VBUS_DISCHG block diagram

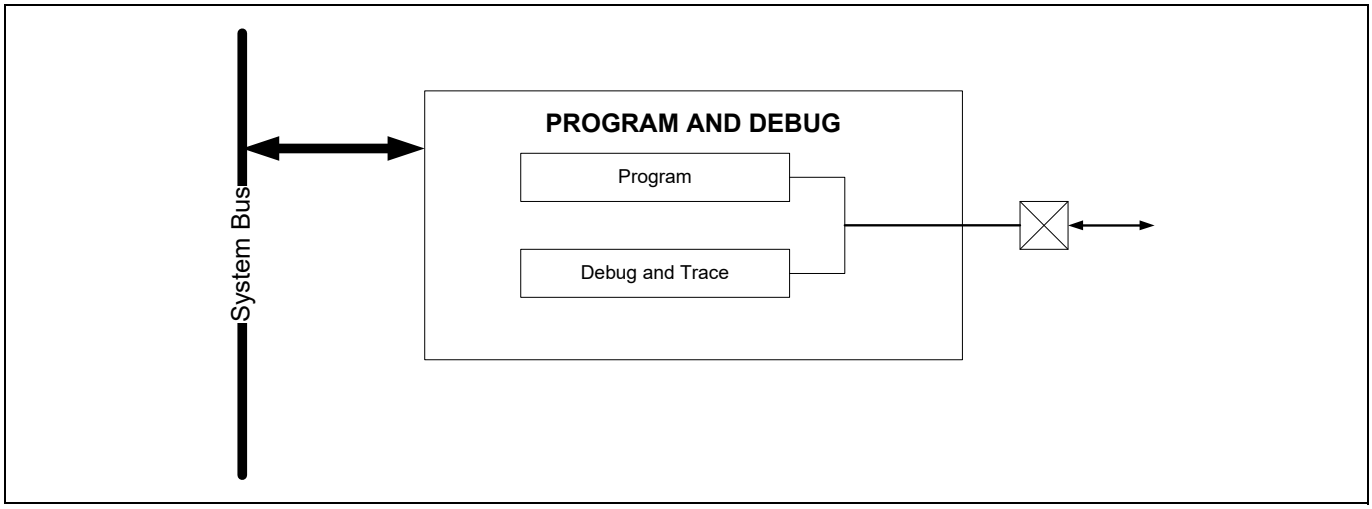
Figure 21-11 shows the block diagram of the VBUS_DISCHG block, which has a 20 V drain extended NFET connected from VBUS supply to ground. The level-shifted version of “dischg_en” controls the 20 V NFET gate after it level shifts. The behavior of this block is similar to that of the VBUS_DISCHG_PROG block without the comparator sub-block.

Section G: Program and debug

This section encompasses the following chapters:

- **“Program and debug interface”** on page 147
- **“Nonvolatile memory programming”** on page 156

Top-level architecture



23 Program and debug interface

The EZ-PD™ PMG1-S0 MCU Program and Debug interface provides a communication gateway for an external device to perform programming or debugging. The external device can be a Infineon-supplied programmer and debugger, or a third-party device that supports EZ-PD™ PMG1-S0 MCU programming and debugging. The serial wire debug (SWD) interface is used as the communication protocol between the external device and EZ-PD™ PMG1-S0 MCU.

23.1 Features

- Programming and debugging through the SWD interface
- Four hardware breakpoints and two hardware watchpoints while debugging
- Read and write access to all memory and registers in the system while debugging, including the Arm® Cortex®-M0 register bank when the core is running or halted

23.2 Functional description

Figure 23-1 shows the block diagram of the program and debug interface in EZ-PD™ PMG1-S0 MCU. The Arm® Cortex®-M0 debug and access port (DAP) acts as the program and debug interface. The external programmer or debugger, also known as the "host", communicates with the DAP of the EZ-PD™ PMG1-S0 MCU "target" using the two pins of the SWD interface - the bidirectional data pin (SWDIO) and the host-driven clock pin (SWDCK). The SWD physical port pins (SWDIO and SWDCK) communicate with the DAP through the high-speed I/O matrix (HSIOM). See the **"I/O system"** on page 44 for details on HSIOM.

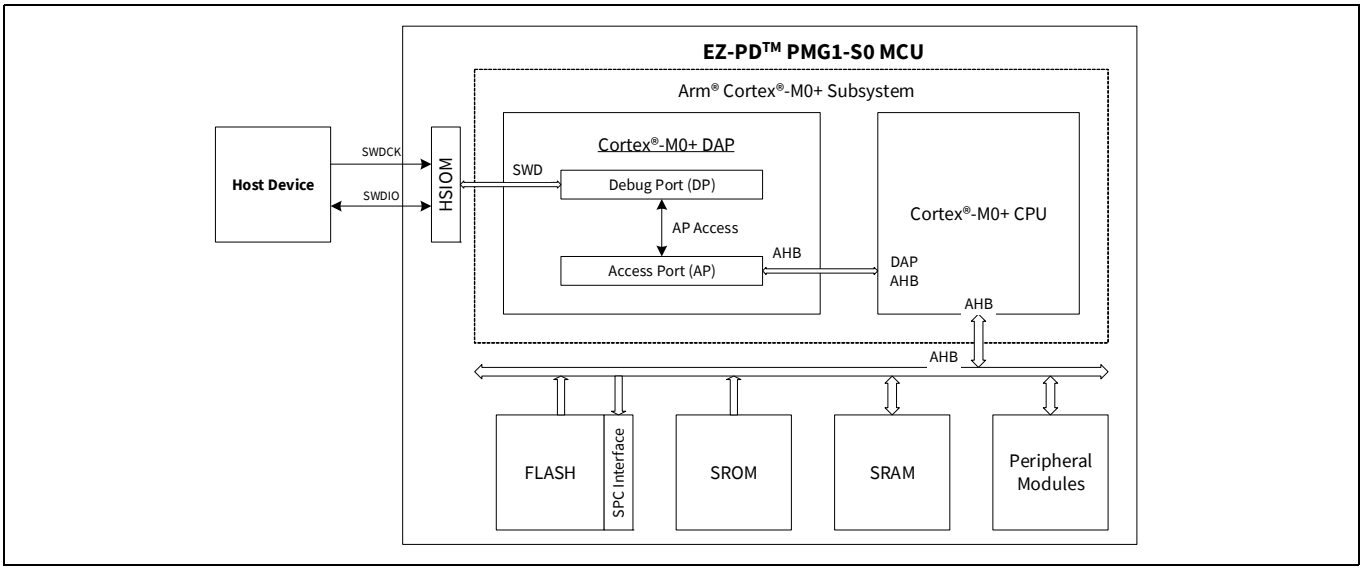


Figure 23-1. Program and debug interface

The DAP communicates with the Arm® Cortex®-M0 CPU using the Arm®-specified advanced high-performance bus (AHB) interface. AHB is the systems interconnect protocol used inside EZ-PD™ PMG1-S0 MCU, which facilitates memory and peripheral register access by the AHB master. EZ-PD™ PMG1-S0 MCU has two AHB masters –Arm® Cortex®-CM0 CPU core and DAP. The external device can effectively take control of the entire device through the DAP to perform programming and debugging operations.

23.3 Serial wire debug (SWD) interface

EZ-PD™ PMG1-S0 MCU's Arm® Cortex®-M0 supports programming and debugging through the SWD interface. The SWD protocol is a packet-based serial transaction protocol. At the pin level, it uses a single bidirectional data signal (SWDIO) and a unidirectional clock signal (SWDCK). The host programmer always drives the clock line, whereas either the host or the target drives the data line. A complete data transfer (one SWD packet) requires 46 clocks and consists of three phases:

- **Host Packet Request Phase** – The host issues a request to the EZ-PD™ PMG1-S0 MCU target.
- **Target Acknowledge Response Phase** – The EZ-PD™ PMG1-S0 MCU target sends an acknowledgment to the host.
- **Data Transfer Phase** – The host or target writes data to the bus, depending on the direction of the transfer.

When control of the SWDIO line passes from the host to the target, or vice versa, there is a turnaround period (Trn) where neither device drives the line and it floats in a high-impedance (Hi-Z) state. This period is either one-half or one and a half clock cycles, depending on the transition.

Figure 23-2 shows the timing diagrams of read and write SWD packets.

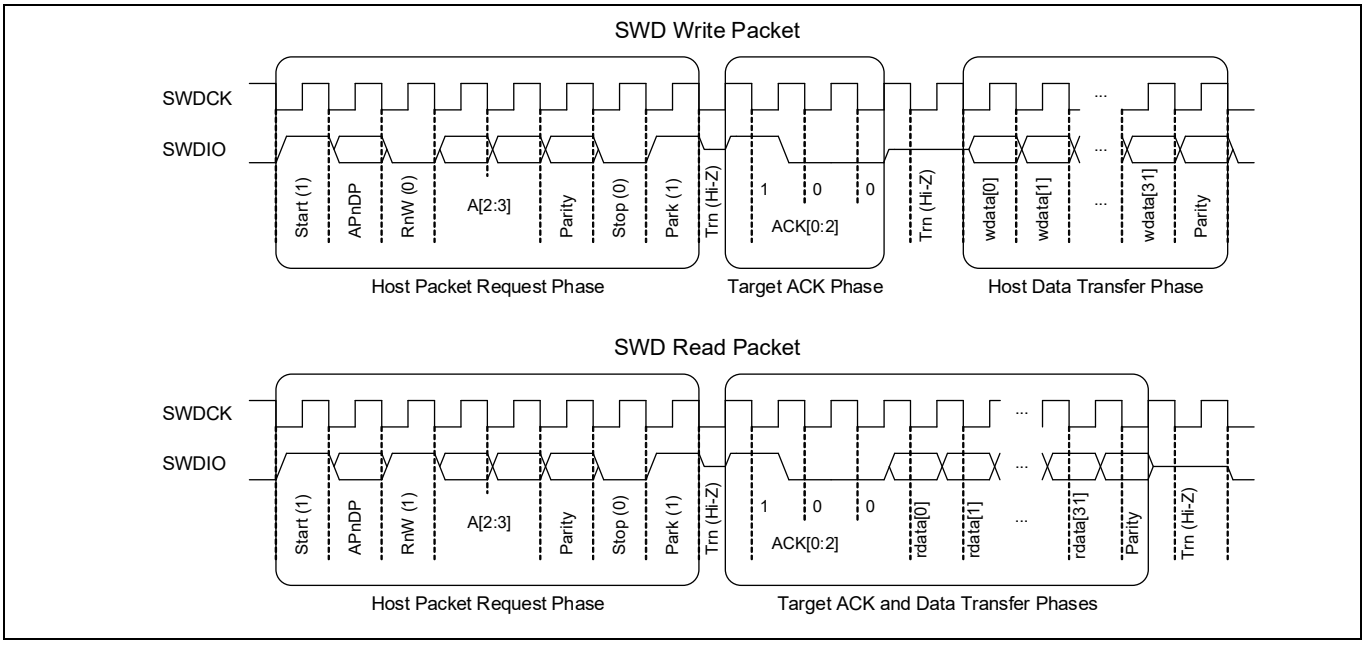


Figure 23-2. SWD write and read packet timing diagrams

The sequence to transmit SWD read and write packets are as follows:

1. Host Packet Request Phase: SWDIO driven by the host
   a. The start bit initiates a transfer; it is always logic 1
   b. The "AP not DP" (APnDP) bit determines whether the transfer is an AP access – 1b1 or a DP access – 1b0.
   c. The "Read not Write" bit (RnW) controls which direction the data transfer is in. 1b1 represents a 'read from' the target, or 1b0 for a 'write to' the target
   d. The Address bits (A[3:2]) are register select bits for AP or DP, depending on the APnDP bit value. See **Table 23-3** and **Table 23-4** for definitions

Note: Address bits are transmitted with the LSB first.

   e. The parity bit contains the parity of APnDP, RnW, and ADDR bits. It is an even parity bit; this means, when XORed with the other bits, the result will be '0'

If the parity bit is not correct, the header is ignored by EZ-PD™ PMG1-S0 MCU; there is no ACK response (ACK = 3b111). The programming operation should be aborted and retried again by following a device reset

f. The stop bit is always logic 0

g. The park bit is always logic 1

2. Target Acknowledge Response Phase: SWDIO driven by the target

a. The ACK[2:0] bits represent the target to host response, indicating failure or success, among other results. See **Table 23-2** for definitions

Note: ACK bits are transmitted with the LSB first.

3. Data Transfer Phase: SWDIO driven by either target or host depending on direction

a. The data for read or write is written to the bus, LSB first

b. The data parity bit indicates the parity of the data read or written. It is an even parity; this means when XORed with the data bits, the result will be '0'

If the parity bit indicates a data error, corrective action should be taken. For a read packet, if the host detects a parity error, it must abort the programming operation and restart. For a write packet, if the target detects a parity error, it generates a FAULT ACK response in the next packet

According to the SWD protocol, the host can generate any number of SWDCK clock cycles between two packets with SWDIO LOW. It is recommended to generate three or more dummy clock cycles between two SWD packets if the clock is not free-running or to make the clock free-running in IDLE mode.

The SWD interface can be reset by clocking the SWDCK line for 50 or more cycles with SWDIO HIGH. To return to the idle state, clock the SWDIO LOW once.

23.3.1 SWD timing details

The SWDIO line is written to and read at different times depending on the direction of communication. The host drives the SWDIO line during the Host Packet Request Phase and, if the host is writing data to the target, during the Data Transfer phase as well. When the host is driving the SWDIO line, each new bit is written by the host on falling SWDCK edges, and read by the target on rising SWDCK edges. The target drives the SWDIO line during the Target Acknowledge Response Phase and, if the target is reading out data, during the Data Transfer Phase as well. When the target is driving the SWDIO line, each new bit is written by the target on rising SWDCK edges, and read by the host on falling SWDCK edges.

Table 23-1 and **Figure 23-2** illustrate the timing of SWDIO bit writes and reads.

Table 23-1. SWDIO bit write and read timing

SWD packet phase	SWDIO edge	
	Falling	**Rising**
Host packet request	Host write	Target read
Host data transfer	–	–
Target ack response	Host read	Target write
Target data transfer	–	–

23.3.2 Acknowledge (ACK) details

The ACK bit-field is used to communicate the status of the previous transfer. OK ACK means that previous packet was successful. A WAIT response requires a data phase. For a FAULT status, the programming operation should be aborted immediately. **Table 23-2** shows the ACK bit-field decoding details.

Table 23-2. SWD transfer ACK response decoding

Response	ACK[2:0]
OK	3b001
WAIT	3b010
FAULT	3b100
NO ACK	3b111

Details on WAIT and FAULT response behaviors are as follows:

- For a WAIT response, if the transaction is a read, the host should ignore the data read in the data phase. The target does not drive the line and the host must not check the parity bit as well
- For a WAIT response, if the transaction is a write, the data phase is ignored by the EZ-PD™ PMG1-S0 MCU. But, the host must still send the data to be written to complete the packet. The parity bit corresponding to the data should also be sent by the host
- For a WAIT response, it means that the EZ-PD™ PMG1-S0 MCU is processing the previous transaction. The host can try for a maximum of four continuous WAIT responses to see if an OK response is received. If it fails, then the programming operation should be aborted and retried again
- For a FAULT response, the programming operation should be aborted and retried again by doing a device reset

23.3.3 Turnaround (Trn) period details

There is a turnaround period between the packet request and the ACK phases, as well as between the ACK and the data phases for host write transfers, as shown in **Figure 23-2**. According to the SWD protocol, the Trn period is used by both the host and target to change the drive modes on their respective SWDIO lines. During the first Trn period after the packet request, the target starts driving the ACK data on the SWDIO line on the rising edge of SWDCK. This ensures that the host can read the ACK data on the next falling edge. Thus, the first Trn period lasts only one-half cycle. The second Trn period of the SWD packet is one and a half cycles. Neither the host nor EZ-PD™ PMG1-S0 MCU should drive the SWDIO line during the Trn period.

23.4 Arm® Cortex®-M0 debug and access port (DAP)

The Arm® Cortex®-M0 program and debug interface includes a debug port (DP) and an access port (AP), which combine to form the DAP. The debug port implements the state machine for the SWD interface protocol that enables communication with the host device. It also includes registers for the configuration of access port, DAP identification code, and so on. The access port contains registers that enable the external device to access the Arm® Cortex®-M0 DAP-AHB interface. Typically, the DP registers are used for a one time configuration or for error detection puoses, and the AP registers are used to perform the programming and debugging operations. Complete architecture details of the DAP is available in the **Arm® Debug Interface v5 Architecture Specification**.

23.4.1 Debug port (DP) registers

Table 23-3 shows the Arm® Cortex®-M0 DP registers used for programming and debugging, along with the corresponding SWD address bit selections. The APnDP bit is always zero for DP register accesses. Two address bits (A[3:2]) are used for selecting among the different DP registers. Note that for the same address bits, different DP registers can be accessed depending on whether it is a read or a write operation. See the **Arm® Debug Interface v5 Architecture Specification** for details on all of the DP registers.

Table 23-3. Main debug port (DP) registers

Register	APnDP	Address A[3:2]	RnW	Full name	Register functionality
ABORT	0 (DP)	2b00	0 (W)	AP Abort Register	This register is used to force a DAP abort and to clear the error and sticky flag conditions.
IDCODE	0 (DP)	2b00	1 (R)	Identification Code Register	This register holds the SWD ID of the Arm® Cortex®-M0 CPU, which is 0x0BB11477.
CTRL/STAT	0 (DP)	2b01	X (R/W)	Control and Status Register	This register allows control of the DP and contains status information about the DP.
SELECT	0 (DP)	2b10	0 (W)	AP Select Register	This register is used to select the current AP. In EZ-PD™ PMG1-S0 MCU, there is only one AP, which interfaces with the DAP AHB.
RDBUFF	0 (DP)	2b11	1 (R)	Read Buffer Register	This register holds the result of the last AP read operation.

23.4.2 Access port (AP) registers

Table 23-4 lists the main Arm® Cortex®-M0 AP registers that are used for programming and debugging, along with the corresponding SWD address bit selections. The APnDP bit is always one for AP register accesses. Two address bits (A[3:2]) are used for selecting the different AP registers.

Table 23-4. Main access port (AP) registers

Register	APnDP	Address A[3:2]	RnW	Full name	Register functionality
CSW	1 (AP)	2b00	X (R/W)	Control and Status Word Register (CSW)	This register configures and controls accesses through the memory access port to a connected memory system (which is the EZ-PD™ PMG1-S0 MCU Memory map)
TAR	1 (AP)	2b01	X (R/W)	Transfer Address Register	This register is used to specify the 32-bit memory address to be read from or written to
DRW	1 (AP)	2b11	X (R/W)	Data Read and Write Register	This register holds the 32-bit data read from or to be written to the address specified in the TAR register

23.5 Programming the EZ-PD™ PMG1-S0 MCU device

EZ-PD™ PMG1-S0 MCU is programmed using the following sequence. See **[3]** for complete details on the programming algorithm, timing specifications, and hardware configuration required for programming.

1. Acquire the SWD port in EZ-PD™ PMG1-S0 MCU
2. Enter the programming mode
3. Execute the device programming routines such as Silicon ID Check, Flash Programming, Flash Verification, and Checksum Verification

23.5.1 SWD port acquisition

23.5.1.1 Primary and secondary SWD pin pairs

The first step in device programming is to acquire the SWD port in EZ-PD™ PMG1-S0 MCU. See **[1]** for information on SWD pins.

23.5.1.2 SWD port acquire sequence

To start programming, the host powers the target device and then sends SWD commands. The EZ-PD™ PMG1-S0 MCU device does not have the XRES pin; therefore, the XRES line from the programmer remains unconnected. Because of this, EZ-PD™ PMG1-S0 MCU device programming is supported only over the Power Cycle mode. Also, for EZ-PD™ PMG1-S0 MCU devices, the target board's power should be supplied by the host programmer.

```
PowerOn();
//Execute Arm's connection sequence to acquire SWD-port
do
{
        SWD_LineReset(); //perform a line reset (50+ SWDCK clocks with SWDIO high)
        ack = Read_DAP ( IDCODE, out ID); //Read the IDCODE DP register

}while ((ack != OK) && time_elapsed < 2 ms); //retry connection until OK ACK or timeout

if (time_elapsed >= 2 ms) return FAIL; //check for acquire time out

if (ID != CM0_ID) return FAIL; //confirm SWD ID of Cortex-M0 CPU. (0x0BB11477)
```

In this pseudo code, SWD_LineReset() is the standard Arm command to reset the debug access port. It consists of more than 49 SWDCK clock cycles with SWDIO HIGH. The transaction must be completed by sending at least one SWDCK clock cycle with SWDIO asserted LOW. This sequence synchronizes the programmer and the chip. Read_DAP() refers to the read of the IDCODE register in the debug port. The sequence of line reset and IDCODE read should be repeated until an OK ACK is received for the IDCODE read or a timeout (2 ms) occurs. The SWD port is said to be in the acquired state if an OK ACK is received within the time window and the IDCODE read matches with that of the Arm® Cortex®-M0 DAP.

23.5.2 SWD programming mode entry

After the SWD port is acquired, the host must enter the device programming mode within a specific time window. This is done by setting the TEST_MODE bit (bit 31) in the test mode control register (MODE register). The debug port should also be configured before entering the device programming mode. Timing specifications and pseudo code for entering the programming mode are detailed in **[3]** document.

23.5.3 SWD programming routines executions

When the device is in programming mode, the external programmer can start sending the SWD packet sequence for performing programming operations such as flash erase, flash program, checksum verification, and so on. The programming routines are explained in the **"Nonvolatile memory programming"** on page 156. The exact sequence of calling the programming routines is given in **[3]**.

23.6 EZ-PD™ PMG1-S0 MCU SWD debug interface

Arm® Cortex®-M0 DAP debugging features are classified into two types: invasive debugging and noninvasive debugging. Invasive debugging includes program halting and stepping, breakpoints, and data watchpoints. Noninvasive debugging includes instruction address profiling and device memory access, which includes the flash memory, SRAM, and other peripheral registers.

The DAP has three major debug subsystems:

- Debug Control and Configuration registers
- Breakpoint Unit (BPU) – provides breakpoint support
- Debug Watchpoint (DWT) – provides watchpoint support. Trace is not supported in Arm® Cortex®-M0 Debug

See the **Armv6-M architecture Reference Manual** for complete details on the debug architecture.

23.6.1 Debug control and configuration registers

The debug control and configuration registers are used to execute firmware debugging. The registers and their key functions are as follows. See the **Armv6-M architecture Reference Manual** for complete bit level definitions of these registers.

- **Debug Halting Control and Status Register (CM0_DHCSR)** – This register contains the control bits to enable debug, halt the CPU, and perform a single-step operation. It also includes status bits for the debug state of the processor
- **Debug Fault Status Register (CM0_DFSR)** – This register describes the reason a debug event has occurred. This includes debug events, which are caused by a CPU halt, breakpoint event, or watchpoint event
- **Debug Core Register Selector Register (CM0_DCRSR)** – This register is used to select the general-puose register in the Arm® Cortex®-M0 CPU to which a read or write operation must be performed by the external debugger
- **Debug Core Register Data Register (CM0_DCRDR)** – This register is used to store the data to write to or read from the register selected in the CM0_DCRSR register
- **Debug Exception and Monitor Control Register (CM0_DEMCR)** – This register contains the enable bits for global debug watchpoint (DWT) block enable, reset vector catch, and hard fault exception catch

23.6.2 Breakpoint unit (BPU)

The BPU provides breakpoint functionality on instruction fetches. The Arm® Cortex®-M0 DAP in EZ-PD™ PMG1-S0 MCU supports up to four hardware breakpoints. Along with the hardware breakpoints, any number of software breakpoints can be created by using the BKPT instruction in the Arm® Cortex®-M0. The BPU has two types of registers.

- The breakpoint control register (CM0_BP_CTRL) is used to enable the BPU and store the number of hardware breakpoints supported by the debug system (four for CM0 DAP in EZ-PD™ PMG1-S0 MCU).
- Each hardware breakpoint has a Breakpoint Compare Register (CM0_BP_COMPx). It contains the enable bit for the breakpoint, the compare address value, and the match condition that will trigger a breakpoint debug event. The typical use case is that when an instruction fetch address matches the compare address of a breakpoint, a breakpoint event is generated and the processor is halted.

23.6.3 Data watchpoint (DWT)

The DWT provides watchpoint support on a data address access or a program counter (PC) instruction address. Trace is not supported by the Arm® Cortex®-M0 in EZ-PD™ PMG1-S0 MCU. The DWT supports two watchpoints. It also provides external program counter sampling using a PC sample register, which can be used for noninvasive coarse profiling of the program counter. The most important registers in the DWT are as follows.

- The watchpoint compare (CM0_DWT_COMPx) registers store the compare values that are used by the watchpoint comparator for the generation of watchpoint events. Each watchpoint has an associated DWT_COMPx register
- The watchpoint mask (CM0_DWT_MASKx) registers store the ignore masks applied to the address range matching in the associated watchpoints
- The watchpoint function (CM0_DWT_FUNCTIONx) registers store the conditions that trigger the watchpoint events. They may be program counter watchpoint event or data address read/write access watchpoint events. A status bit is also set when the associated watchpoint event has occurred
- The watchpoint comparator PC sample register (CM0_DWT_PCSR) stores the current value of the program counter. This register is used for coarse, non-invasive profiling of the program counter register

23.6.4 Debugging the EZ-PD™ PMG1-S0 MCU device

The host debugs the target EZ-PD™ PMG1-S0 MCU device by accessing the debug control and configuration registers, registers in the BPU, and registers in the DWT. All registers are accessed through the SWD interface; the SWD debug port (SW-DP) in the Arm® Cortex®-M0 DAP converts the SWD packets to appropriate register access through the DAP-AHB interface.

The first step in debugging the target EZ-PD™ PMG1-S0 MCU device is to acquire the SWD port. The acquire sequence consists of an SWD line reset sequence and read of the DAP SWDID through the SWD interface. The SWD port is acquired when the correct CM0 DAP SWDID is read from the target device. For the debug transactions to occur on the SWD interface, the corresponding pins should not be used for any other puose. See **“I/O system”** on page 44 to understand how to configure the SWD port pins, allowing them to be used only for SWD interface or for other functions such as GPIO. If debugging is required, the SWD port pins should not be used for other purposes. If only programming support is needed, the SWD pins can be used for other puoses.

When the SWD port is acquired, the external debugger sets the C_DEBUGEN bit in the DHCSR register to enable debugging. Then, the different debugging operations such as stepping, halting, breakpoint configuration, and watchpoint configuration are carried out by writing to the appropriate registers in the debug system.

Debugging the target device is also affected by the overall device protection setting, which is explained in the **Device security**. Only the OPEN protected mode supports device debugging. The external debugger and the target device connection is not lost for a device transition from Active mode to either Sleep or Deep Sleep modes. When the device enters the Active mode from either Deep Sleep or Sleep modes, the debugger can resume its actions without initiating a connect sequence again.

23.7 Registers

Table 23-5. List of registers

Register name	Description
CM0_DHCSR	Debug Halting Control and Status Register
CM0_DFSR	Debug Fault Status Register
CM0_DCRSR	Debug Core Register Selector Register
CM0_DCRDR	Debug Core Register Data Register
CM0_DEMCR	Debug Exception and Monitor Control Register
CM0_BP_CTRL	Breakpoint control register
CM0_BP_COMPx	Breakpoint Compare Register
CM0_DWT_COMPx	Watchpoint Compare Register
CM0_DWT_MASKx	Watchpoint Mask Register
CM0_DWT_FUNCTIONx	Watchpoint Function Register
CM0_DWT_PCSR	Watchpoint Comparator PC Sample Register

24 Nonvolatile memory programming

Nonvolatile memory programming refers to the programming of flash memory in the EZ-PD™ PMG1-S0 MCU device. This chapter explains the different functions that are part of device programming, such as erase, write, program, and checksum calculation. Infineon-supplied programmers and other third-party programmers can use these functions to program the EZ-PD™ PMG1-S0 MCU device with the data in an application hex file. They can also be used to perform bootload operations where the CPU will update a portion of the flash memory.

24.1 Features

- Supports programming through the debug and access port (DAP) and Arm® Cortex®-M0 CPU
- Supports both blocking and non-blocking flash program and erase operations from the Arm® Cortex®-M0 CPU

24.2 Functional description

The flash programming operations are implemented as system calls. System calls are executed out of SROM in the privileged mode of operation. The user has no access to read or modify the SROM code. The DAP or the CM0 CPU requests the system call by writing the function opcode and parameters to the System Performance Controller Interface (SPCIF) input registers, and then requesting the SROM to execute the function. Based on the function opcode, the System Performance Controller (SPC) executes the corresponding system call from SROM and updates the SPCIF status register. The DAP or the CPU should read this status register for the pass/fail result of the function execution. As part of function execution, the code in SROM interacts with the SPCIF to do the actual flash programming operations.

EZ-PD™ PMG1-S0 MCU flash is programmed using a Program Erase Program (PEP) sequence. The flash cells are all programmed to a known state, erased, and then the selected bits are programmed. This increases the life of the flash by balancing the stored charge. When writing to flash the data is first copied to a page latch buffer. The flash write functions are then used to transfer this data to flash.

External programmers program the flash memory in EZ-PD™ PMG1-S0 MCU using the SWD protocol by sending the commands to the Debug and Access Port (DAP). The programming sequence for the EZ-PD™ PMG1-S0 MCU device with an external programmer is given in the EZ-PD™ PMG1-S0 MCU Device Programming Specifications. Flash memory can also be programmed by the CM0 CPU by accessing the relevant registers through the AHB interface. This type of programming is typically used to update a portion of the flash memory as part of a bootload operation, or other application requirements, such as updating a lookup table stored in the flash memory. All write operations to flash memory, whether from the DAP or from the CPU, are done through the SPCIF.

Note: *It can take as much as 20 ms to write to flash. During this time, the device should not be reset, or unexpected changes may be made to portions of the flash. Reset sources (see **"Reset system"** on page 64) include software reset and watchdog; make sure that these are not inadvertently activated. In addition, the low-voltage detect circuits should be configured to generate an interrupt instead of a reset.*

24.3 System call implementation

A system call consists of the following items:

- **Opcode**: A unique 8-bit opcode
- **Parameters**: Two 8-bit parameters are mandatory for all system calls. These parameters are referred to as key1 and key2, and are defined as follows:
  - key1 = 0xB6
  - key2 = 0xD3 + Opcode
    The two keys are passed to ensure that the user system call is not initiated by mistake. If the key1 and key2 parameters are not correct, the SROM does not execute the function, and returns an error code. Apart from these two parameters, additional parameters may be required depending on the specific function being called.
- **Return values**: Some system calls also return a value on completion of their execution, such as the silicon ID or a checksum
- **Completion status**: Each system call returns a 32-bit status that the CPU or DAP can read to verify success or determine the reason for failure

24.4 Blocking and non-blocking system calls

System call functions can be categorized as blocking or non-blocking based on the nature of their execution. Blocking system calls are those where the CPU cannot execute any other task in parallel other than the execution of the system call. When a blocking system call is called from a process, the CPU jumps to the code corresponding in SROM. When the execution is complete, the original thread execution resumes. Non-blocking system calls allow the CPU to execute some other code in parallel and communicate the completion of interim system call tasks to the CPU through an interrupt.

Non-blocking system calls are only used when the CPU initiates the system call. The DAP will only use system calls during the programming mode and the CPU is halted during this process.

The three non-blocking system calls are Non-Blocking Write Row, Non-Blocking Program Row, and Resume Non-Blocking, respectively. All other system calls are blocking.

Because the CPU cannot execute code from flash while doing an erase or program operation on the flash, the non-blocking system calls can only be called from a code executing out of SRAM. If the non-blocking functions are called from flash memory, the result is undefined and may return a bus error and trigger a hard fault when the flash fetch operation is being done.

The System Performance Controller (SPC) is the block that generates the properly sequenced high-voltage pulses required for erase and program operations of the flash memory. When a non-blocking function is called from SRAM, the SPC timer triggers its interrupt when each of the sub-operations in a write or program operation is complete. Call the Resume Non-Blocking function from the SPC interrupt service routine (ISR) to ensure that the subsequent steps in the system call are completed. Because the CPU can execute code only from the SRAM when a non-blocking write or program operation is being done, the SPC ISR should also be located in the SRAM. The SPC interrupt is triggered once in the case of a non-blocking program function or thrice in a non-blocking write operation. The Resume Non-Blocking function call done in the SPC ISR is called once in a non-blocking program operation and thrice in a non-blocking write operation.

The pseudo code for using a non-blocking write system call and executing user code out of SRAM is given later in this chapter.

24.4.1 Performing a system call

The steps to initiate a system call are as follows:

1. Set up the function parameters: The two possible methods for preparing the function parameters (key1, key2, additional parameters) are as follows:
   a. **Write the function parameters to the CPUSS_SYSARG register**: This method is used for functions that retrieve their parameters from the CPUSS_SYSARG register. The 32-bit CPUSS_SYSARG register must be written with the parameters in the sequence specified in the respective system call table
   b. **Write the function parameters to SRAM**: This method is used for functions that retrieve their parameters from SRAM. The parameters should first be written in the specified sequence to consecutive SRAM locations. Then, the starting address of the SRAM, which is the address of the first parameter, should be written to the CPUSS_SYSARG register. This starting address should always be a word-aligned (32-bit) address. The system call uses this address to fetch the parameters
2. **Specify the system call using its opcode and initiating the system call**: The 8-bit opcode should be written to the SYSCALL_COMMAND bits ([15:0]) in the CPUSS_SYSREQ register. The opcode is placed in the lower eight bits [7:0] and 0x00 be written to the upper eight bits [15:8]. To initiate the system call, set the SYSCALL_REQ bit (31) in the CPUSS_SYSREG register. Setting this bit triggers a non-maskable interrupt that jumps the CPU to the SROM code referenced by the opcode parameter
3. **Wait for the system call to finish executing**: When the system call begins execution, it sets the PRIVILEGED bit in the CPUSS_SYSREQ register. This bit can be set only by the system call, not by the CPU or DAP. The DAP should poll the PRIVILEGED and SYSCALL_REQ bits in the CPUSS_SYSREG register continuously to check whether the system call is completed. Both these bits are cleared on completion of the system call. The maximum execution time is one second. If these two bits are not cleared after one second, the operation should be considered a failure and aborted without executing the following steps. Note that unlike the DAP, the CPU application code cannot poll these bits during system call execution. This is because the CPU executes code out of the SROM during the system call. The application code can check only the final function pass/fail status after the execution returns from SROM
4. **Check the completion status**: After the PRIVILEGED and SYSCALL_REQ bits are cleared to indicate completion of the system call, the CPUSS_SYSARG register should be read to check for the status of the system call. If the 32-bit value read from the CPUSS_SYSARG register is 0xAXXXXXXX (where 'X' denotes don't care hex values), the system call was successfully executed. For a failed system call, the status code is 0xF00000YY where YY indicates the reason for failure. See **Table 24-1** for the complete list of status codes and their description
5. **Retrieve the return values**: For system calls that return values such as silicon ID and checksum, the CPU or DAP should read the CPUSS_SYSREG and CPUSS_SYSARG registers to fetch the values returned

24.5 System calls

Table 24-1 lists all the system calls supported in EZ-PD™ PMG1-S0 MCU along with the function description and availability in device protection modes. See the **Device security** for more information on the device protection settings. Note that some system calls cannot be called by the CPU as given in the table. Detailed information on each of the system calls follows the table.

Table 24-1. List of system calls

System call	Description	DAP access			CPU access
		Open	Protected	Kill	
Silicon ID	Returns the device Silicon ID, Family ID, and Revision ID	4	4	–	4
Load Flash Bytes	Loads data to the page latch buffer to be programmed later into the flash row, in 1 byte granularity, for a row size of 128 bytes	4	–	–	4
Write Row	Erases and then programs a row of flash with data in the page latch buffer	4	–	–	4
Program Row	Programs a row of flash with data in the page latch buffer	4	–	–	4
Erase All	Erases all user code in the flash array; the flash row-level protection data in the supervisory flash area	4	–	–	
Checksum	Calculates the checksum over the entire flash memory (user and supervisory area) or checksums a single row of flash	4	4	–	4
Write Protection	This programs both flash row-level protection settings and chip-level protection settings into the supervisory flash (row 0)	4	4	–	
Non-Blocking Write Row	Erases and then programs a row of flash with data in the page latch buffer. During program/erase pulses, the user may execute code from SRAM. This function is meant only for CPU access	–	–	–	4
Non-Blocking Program Row	Programs a row of flash with data in the page latch buffer. During program/erase pulses, the user may execute code from SRAM. This function is meant only for CPU access	–	–	–	4
Resume Non-Blocking	Resumes a non-blocking write row or non-blocking program row. This function is meant only for CPU access	–	–	–	4

24.5.1 Silicon ID

This function returns a 12-bit family ID, 16-bit silicon ID, and an 8-bit revision ID, and the current device protection mode. These values are returned to the CPUSS_SYSARG and CPUSS_SYSREQ registers. The parameters are passed through the CPUSS_SYSARG and CPUSS_SYSREQ registers.

Table 24-2. Parameters

Address	Value to be written	Description
CPUSS_SYSARG register		
Bits [7:0]	0xB6	Key1
Bits [15:8]	0xD3	Key2
Bits [31:16]	0x0000	Not used
CPUSS_SYSREQ register		
Bits [15:0]	0x0000	Silicon ID opcode
Bits [31:16]	0x8000	Set SYSCALL_REQ bit

Table 24-3. Return

Address	Return value	Description
CPUSS_SYSARG register		
Bits [7:0]	Silicon ID Lo	See the EZ-PD™ PMG1-S0 MCU device datasheet for Silicon ID values for different part numbers
Bits [15:8]	Silicon ID Hi	
Bits [19:16]	Minor Revision Id	See the EZ-PD™ PMG1 MCU Programming Specifications for these values
Bits [23:20]	Major Revision Id	
Bits [27:24]	0xXX	Not used (don’t care)
Bits [31:28]	0xA	Success status code
CPUSS_SYSREQ register		
Bits [11:0]	Family ID	Family ID is 0xB0 for EZ-PD™ PMG1-S0 MCU
Bits [15:12]	Chip Protection	See **“Device security”** on page 66 for more details
Bits [31:16]	0xXXXX	Not used

24.5.2 Configure clock

This function initializes the clock necessary for flash programming and erasing operations. This API is used to ensure that the charge pump clock (clk_pump) and the HF clock (clk_hf) are set to IMO at 48 MHz before calling the flash write and flash erase APIs. The flash write and erase APIs will exit without acting on the flash and return the "Invalid Pump Clock Frequency" status if the IMO is the source of the charge pump clock and is not 48 MHz.

Table 24-4. Parameters

Address	Value to be written	Description
SRAM Address: 32'hYY (32-bit wide, word-aligned SRAM address)		
Bits [7:0]	0xB6	Key1
Bits [15:8]	0xE8	Key2
Bits [31:16]	0xXXXX	Don't care
CPUSS_SYSARG register		
Bits [31:0]	32'hYY	32-bit word-aligned address of the SRAM that stores the first function parameter (key1)
CPUSS_SYSREQ register		
Bits [15:0]	0x0015	Configure clock opcode
Bits [31:16]	0x8000	Set SYSCALL_REQ bit

Table 24-5. Return

Address	Return value	Description
CPUSS_SYSARG register		
Bits [31:28]	0xA	Success status code
Bits [27:0]	0xXXXXXXX	Not used (don't care)

24.5.3 Load flash bytes

This function loads the page latch buffer with data to be programmed into a row of flash. The load size can range from 1-byte to the maximum number of bytes in a flash row, which is 64 bytes. Data is loaded into the page latch buffer starting at the location specified by the “Byte Addr” input parameter. Data loaded into the page latch buffer remains until a program operation is performed, which clears the page latch contents. The parameters for this function, including the data to be loaded into the page latch, are written to the SRAM; the starting address of the SRAM data is written to the CPUSS_SYSARG register. Note that the starting parameter address should be a word-aligned address.

Table 24-6. Parameters

Address	Value to be written	Description
SRAM Address - 32’hYY (32-bit wide, word-aligned SRAM address)		
Bits [7:0]	0xB6	Key1
Bits [15:8]	0xD7	Key2
Bits [23:16]	Byte Addr	Start address of page latch buffer to write data 0x00 – Byte 0 of latch buffer 0x80 - Byte 128 of latch buffer
Bits [31:24]	Flash Macro Select	0x00 – Flash Macro 0 0x01 – Flash Macro 1 (Refer to the **Arm® Cortex®-M0 CPU** for the number of flash macros in the device)
SRAM Address- 32’hYY + 0x04		
Bits [7:0]	Load Size	Number of bytes to be written to the page latch buffer. 0x00 – 1 byte 0x7F - 128 bytes
Bits [15:8]	0xXX	Don’t care parameter
Bits [23:16]	0xXX	Don’t care parameter
Bits [31:24]	0xXX	Don’t care parameter
SRAM address- From (32’hYY + 0x08) to (32’hYY + 0x08 + Load Size)		
Byte 0	Data Byte [0]	First data byte to be loaded
Byte (Load size –1)	Data Byte [Load size –1]	Last data byte to be loaded
CPUSS_SYSARG register		
Bits [31:0]	32’hYY	32-bit word-aligned address of the SRAM that stores the first function parameter (key1)
CPUSS_SYSREQ register		
Bits [15:0]	0x0004	Load Flash Bytes opcode
Bits [31:16]	0x8000	Set SYSCALL_REQ bit

Table 24-7. Return

Address	Return value	Description
CPUSS_SYSARG register		
Bits [31:28]	0xA	Success status code
Bits [27:0]	0xXXXXXXX	Not used (don’t care)

24.5.4 Write row

This function erases and then programs the addressed row of flash with the data in the page latch buffer. If all data in the page latch buffer is 0, then the program is skipped. The parameters for this function are stored in SRAM. The start address of the stored parameters is written to the CPUSS_SYSARG register. This function clears the page latch buffer contents after the row is programmed.

Usage Requirements: Call the Configure Clock API before calling this function. The Configure Clock API ensures that the charge pump clock (clk_pump) and the HF clock (clk_hf) are set to IMO at 48 MHz. Call the Load Flash Bytes function before calling this function. This function can do a write operation only if the corresponding flash row is not write protected.

Note that the SROM does not modify, enable, or disable any clock during any flash operation. See the CLK_IMO_CONFIG register in the section [2] for more information.

Table 24-8. Parameters

Address	Value to be written	Description
SRAM address: 32'hYY (32-bit wide, word-aligned SRAM address)		
Bits [7:0]	0xB6	Key1
Bits [15:8]	0xD8	Key2
Bits [31:16]	Row ID	Row number to write 0x0000 - Row 0 0x00FF - Row 255
CPUSS_SYSARG register		
Bits [31:0]	32'hYY	32-bit word-aligned address of the SRAM that stores the first function parameter (key1)
CPUSS_SYSREQ register		
Bits [15:0]	0x0005	Write Row opcode
Bits [31:16]	0x8000	Set SYSCALL_REQ bit

Table 24-9. Return

Address	Return value	Description
CPUSS_SYSARG register		
Bits [31:28]	0xA	Success status code
Bits [27:0]	0xXXXXXXX	Not used (don't care)

24.5.5 Program row

This function programs the addressed row of the flash, with data in the page latch buffer. If all data in the page latch buffer is 0, then the program is skipped. The row must be in an erased state before calling this function. This clears the page latch buffer contents after the row is programmed.

Usage requirements: Call the Configure Clock API before calling this function. The Configure Clock API ensures that the charge pump clock (clk_pump) and the HF clock (clk_hf) are set to IMO at 48 MHz. Call the Load Flash Bytes function before calling this function. The row must be in an erased state before calling this function. This function can do a program operation only if the corresponding flash row is not write-protected.

Table 24-10. Parameters

Address	Value to be written	Description
SRAM Address: 32'hYY (32-bit wide, word-aligned SRAM address)		
Bits [7:0]	0xB6	Key1
Bits [15:8]	0xD9	Key2
Bits [31:16]	Row ID	Row number to program 0x0000 - Row 0 0x00FF - Row 255
CPUSS_SYSARG register		
Bits [31:0]	32'hYY	32-bit word-aligned address of the SRAM that stores the first function parameter (key1)
CPUSS_SYSREQ register		
Bits [15:0]	0x0006	Program Row opcode
Bits [31:16]	0x8000	Set SYSCALL_REQ bit

Table 24-11. Return

Address	Return value	Description
CPUSS_SYSARG register		
Bits [31:28]	0xA	Success status code
Bits [27:0]	0xXXXXXXX	Not used (don't care)

24.5.6 Erase all

This function erases all the user code in the flash main arrays and the row-level protection data in supervisory flash row 0 of each flash macro.

Usage Requirements: Call the Configure Clock API before calling this function. The Configure Clock API ensures that the charge pump clock (clk_pump) and the HF clock (clk_hf) are set to IMO at 48 MHz. This API can be called only from the DAP in the programming mode and only if the chip protection mode is OPEN. If the chip protection mode is PROTECTED, then the Write Protection API must be used by the DAP to change the protection settings to OPEN. Changing the protection setting from PROTECTED to OPEN automatically does an erase all operation.

Table 24-12. Parameters

Address	Value to be written	Description
SRAM address: 32'hYY (32-bit wide, word-aligned SRAM address)		
Bits [7:0]	0xB6	Key1
Bits [15:8]	0xDD	Key2
Bits [31:16]	0xXXXX	Don't care
CPUSS_SYSARG register		
Bits [31:0]	32'hYY	32-bit word-aligned address of the SRAM that stores the first function parameter (key1)
CPUSS_SYSREQ register		
Bits [15:0]	0x000A	Erase All opcode
Bits [31:16]	0x8000	Set SYSCALL_REQ bit

Table 24-13. Return

Address	Return value	Description
CPUSS_SYSARG register		
Bits [31:28]	0xA	Success status code
Bits [27:0]	0xXXXXXXX	Not used (don't care)

24.5.7 Checksum

This function reads either the whole flash memory or a row of flash and returns the 24-bit sum of each byte read in that flash region. When performing a checksum on the whole flash, the user code and supervisory flash regions are included. When performing a checksum only on one row of flash, the flash row number is passed as a parameter. Bytes 2 and 3 of the parameters select whether the checksum is performed on the whole flash memory or a row of user code flash.

Table 24-14. Parameters

Address	Value to be written	Description
CPUSS_SYSARG register		
Bits [7:0]	0xB6	Key1
Bits [15:8]	0xDE	Key2
Bits [31:16]	Row ID	Selects the flash row number on which the checksum operation is done Row number – 16 bit flash row number or 0x8000 – Checksum is performed on entire flash memory
CPUSS_SYSREQ register		
Bits [15:0]	0x000B	Checksum opcode
Bits [31:16]	0x8000	Set SYSCALL_REQ bit

Table 24-15. Return

Address	Return Value	Description
CPUSS_SYSARG register		
Bits [31:28]	0xA	Success status code
Bits [27:24]	0xX	Not used (don't care)
Bits [23:0]	Checksum	24-bit checksum value of the selected flash region

24.5.8 Write protection

This function programs both the flash row-level protection settings and the device protection settings in the supervisory flash row. The flash row-level protection settings are programmed separately for each flash macro in the device. Each row has a single protection bit. The total number of protection bytes is the number of flash rows divided by eight. The chip-level protection settings (1-byte) are stored in flash macro zero in the last byte location in row zero of the supervisory flash. The size of the supervisory flash row is the same as the user code flash row size.

Usage requirements: Call the Configure Clock API before calling this function. The Configure Clock API ensures that the charge pump clock (clk_pump) and the HF clock (clk_hf) are set to IMO at 48 MHz. The Load Flash Bytes function is used to load the flash protection bytes of a flash macro into the page latch buffer corresponding to the macro. The starting address parameter for the load function should be zero. The flash macro number should be one that needs to be programmed; the number of bytes to load is the number of flash protection bytes in that macro.

Then, the Write Protection function is called, which programs the flash protection bytes from the page latch to be the corresponding flash macro's supervisory row. In flash macro zero, which also stores the device protection settings, the device level protection setting is passed as a parameter in the CPUSS_SYSARG register.

Table 24-16. Parameters

Address	Value to be written	Description
CPUSS_SYSARG register		
Bits [7:0]	0xB6	Key1
Bits [15:8]	0xE0	Key2
Bits [23:16]	Device Protection Byte	Parameter applicable only for Flash Macro 0 0x01 – OPEN mode 0x02 – PROTECTED mode 0x04 – KILL mode
Bits [31:24]	Flash Macro Select	0x00 – Flash Macro 0 0x01 – Flash Macro 1
CPUSS_SYSREQ register		
Bits [15:0]	0x000D	Write Protection opcode
Bits [31:16]	0x8000	Set SYSCALL_REQ bit

Table 24-17. Return

Address	Return value	Description
CPUSS_SYSARG register		
Bits [31:28]	0xA	Success status code
Bits [27:24]	0xX	Not used (don’t care)
Bits [23:0]	0x000000	

24.5.9 Non-Blocking write row

This function is used when a flash row needs to be written by the CM0 CPU in a non-blocking manner, so that the CPU can execute code from SRAM while the write operation is being done. The explanation of non-blocking system calls is explained in **“Blocking and non-blocking system calls”** on page 157.

The non-blocking write row system call has three phases: Preprogram, Erase, Program. Preprogram is the step in which all of the bits in the flash row are written a ‘1’ in preparation for an erase operation. The erase operation clears all of the bits in the row, and the program operation writes the new data to the row.

While each phase is being executed, the CPU can execute code from SRAM. When the non-blocking write row system call is initiated, the user cannot call any system call function other than the Resume Non-Blocking function, which is required for completion of the non-blocking write operation. After the completion of each phase, the SPC triggers its interrupt. In this interrupt, call the Resume Non-Blocking system call.

Usage Requirements: Call the Configure Clock API before calling this function. The Configure Clock API ensures that the charge pump clock (clk_pump) and the HF clock (clk_hf) are set to IMO at 48 MHz.

Note: *The device firmware must not attempt to put the device to sleep during a non-blocking write row. This will reset the page latch buffer and the flash will be written with all zeros.*

Call the Load Flash Bytes function before calling this function to load the data bytes that will be used for programming the row. In addition, the non-blocking write row function can be called only from the SRAM. This is because the CM0 CPU cannot execute code from flash while doing the flash erase program operations. If this function is called from the flash memory, the result is undefined, and may return a bus error and trigger a hard fault when the flash fetch operation is being done.

Table 24-18. Parameters

Address	Value to be written	Description
SRAM address 32'hYY (32-bit wide, word-aligned SRAM address)		
Bits [7:0]	0xB6	Key1
Bits [15:8]	0xDA	Key2
Bits [31:16]	Row ID	Row number to write 0x0000 - Row 0 0x00FF - Row 255
CPUSS_SYSARG register		
Bits [31:0]	32'hYY	32-bit word-aligned address of the SRAM that stores the first function parameter (key1)
CPUSS_SYSREQ register		
Bits [15:0]	0x0007	Non-Blocking Write Row opcode
Bits [31:16]	0x8000	Set SYSCALL_REQ bit

Table 24-19. Return

Address	Return value	Description
CPUSS_SYSARG register		
Bits [31:28]	0xA	Success status code
Bits [27:0]	0xXXXXXXX	Not used (don't care)

24.5.10 Non-blocking program row

This function is used when a flash row needs to be programmed by the CM0 CPU in a non-blocking manner, so that the CPU can execute code from the SRAM when the program operation is being done. The explanation of non-blocking system calls is explained in **"Blocking and non-blocking system calls"** on page 157. While the program operation is being done, the CPU can execute code from the SRAM. When the non-blocking program row system call is called, the user cannot call any other system call function other than the Resume Non-Blocking function, which is required for the completion of the non-blocking write operation.

Unlike the Non-Blocking Write Row system call, the Program system call only has a single phase. Therefore, the Resume Non-Blocking function only needs to be called once from the SPC interrupt when using the Non-Blocking Program Row system call.

Usage requirements: Call the Configure Clock API before calling this function. The Configure Clock API ensures that the charge pump clock (clk_pump) and the HF clock (clk_hf) are set to IMO at 48 MHz. Call the Load Flash Bytes function before calling this function to load the data bytes that will be used for programming the row. In addition, the non-blocking program row function can be called only from SRAM. This is because the CM0 CPU cannot execute code from flash while doing flash program operations. If this function is called from flash memory, the result is undefined, and may return a bus error and trigger a hard fault when the flash fetch operation is being done.

Table 24-20. Parameters

Address	Value to be written	Description
SRAM Address 32'hYY (32-bit wide, word-aligned SRAM address)		
Bits [7:0]	0xB6	Key1
Bits [15:8]	0xDB	Key2

Address	Value to be written	Description
Bits [31:16]	Row ID	Row number to write 0x0000 - Row 0 0x00FF - Row 255
CPUSS_SYSARG register		
Bits [31:0]	32'hYY	32-bit word-aligned address of the SRAM that stores the first function parameter (key1)
CPUSS_SYSREQ register		
Bits [15:0]	0x0008	Non-Blocking Program Row opcode
Bits [31:16]	0x8000	Set SYSCALL_REQ bit

Table 24-21. Return

Address	Return value	Description
CPUSS_SYSARG register		
Bits [31:28]	0xA	Success status code
Bits [27:0]	0xXXXXXXX	Not used (don't care)

24.5.11 Resume non-blocking

This function completes the additional phases of erase and program that were started using the non-blocking write row and non-blocking program row system calls. This function must be called thrice following a call to Non-Blocking Write Row or once following a call to Non-Blocking Program Row from the SPC ISR. No other system calls can execute until all phases of the program or erase operation are complete. More details on the procedure of using the non-blocking functions are explained in **"Blocking and non-blocking system calls"** on page 157.

Table 24-22. Parameters

Address	Value to be written	Description
SRAM address 32'hYY (32-bit wide, word-aligned SRAM address)		
Bits [7:0]	0xB6	Key1
Bits [15:8]	0xDC	Key2
Bits [31:16]	0xXXXX	Don't care. Not used by SROM
CPUSS_SYSARG register		
Bits [31:0]	32'hYY	32-bit word-aligned address of the SRAM that stores the first function parameter (key1)
CPUSS_SYSREQ register		
Bits [15:0]	0x0009	Resume Non-Blocking opcode
Bits [31:16]	0x8000	Set SYSCALL_REQ bit

Table 24-23. Return

Address	Return value	Description
CPUSS_SYSARG register		
Bits [31:28]	0xA	Success status code
Bits [27:0]	0xXXXXXXX	Not used (don't care)

24.6 System call status

At the end of every system call, a status code is written over the arguments in the CPUSS_SYSARG register. A success status is 0xAXXXXXXX, where X indicates don't care values or return data in the case of the system calls that return a value. A failure status is indicated by 0xF00000XX, where XX is the failure code.

Table 24-24. System call status codes

Status code (32-bit value in CPUSS_SYSARG register)	Description
AXXXXXXXh	Success – The "X" denotes a don't care value, which has a value of '0' returned by the SROM, unless the API returns parameters directly to the CPUSS_SYSARG register.
F0000001h	Invalid Chip Protection Mode – This API is not available during the current chip protection mode.
F0000003h	Invalid Page Latch Address – The address within the page latch buffer is either out of bounds or the size provided is too large for the page address.
F0000004h	Invalid Address – The row ID or byte address provided is outside of the available memory.
F0000005h	Row Protected – The row ID provided is a protected row.
F0000007h	Resume Completed – All non-blocking APIs have completed. The resume API cannot be called until the next non-blocking API.
F0000008h	Pending Resume – A non-blocking API was initiated and must be completed by calling the resume API, before any other API's may be called.
F0000009h	System Call Still In Progress – A resume or non-blocking is still in progress. The SPC ISR must fire before attempting the next resume.
F000000Ah	Checksum Zero Failed – The calculated checksum was not zero.
F000000Bh	Invalid Opcode – The opcode is not a valid API opcode.
F000000Ch	Key Opcode Mismatch – The opcode provided does not match key1 and key2.
F000000Eh	Invalid Start Address – The start address is greater than the end address provided.
F0000012h	Invalid Pump Clock Frequency - IMO must be set to 48 MHz and HF clock source to the IMO clock source before flash write/erase operations.

24.7 Non-blocking system call pseudo code

This section contains pseudo code to demonstrate how to set up a non-blocking system call and execute code out of SRAM during the flash programming operations.

```
#include "cy_device.h"
#include "cybsp.h"

// Flash row size
#define FLASH_ROW_SIZE (CY_FLASH_SIZEOF_ROW)

/* Keys used in SROM APIs. */
#define SROM_KEY_ONE (0xB6u)
#define SROM_KEY_TWO_OFFSET (8u)
#define SROM_PARAM_OFFSET (16u)

// Offset of Argument 1, 2 and data for SROM APIs in SRAM buffer.
#define SROM_API_ARG0_OFFSET (0x00u)
#define SROM_API_ARG1_OFFSET (0x01u)
#define SROM_API_DATA_OFFSET (0x02u)

// CPUSS SYSARG return value
#define CPUSS_SYSARG_RETURN_VALUE_MASK (0xF0000000u) // Mask
#define CPUSS_SYSARG_PASS_RETURN_VALUE (0xA0000000u) // Success
#define CPUSS_SYSARG_ERROR_RETURN_VALUE (0xF0000000u) // Error
#define ROW_NUMBER_TO_WRITE (255u)

// Buffer used for SROM APIs
uint32_t srom_arg_buf[(FLASH_ROW_SIZE / sizeof(uint32_t)) + 2];
// Data to write into flash
uint8_t data_to_write[FLASH_ROW_SIZE];
// Counter to keep track of the SPC interrupts during Non-Blocking Flash update.
static volatile uint8_t spc_intr_counter = 0;

// This example uses the simplest way to place a function in the RAM space; functions
// are mapped to .data section that is normally used for initialized variables.
// Code is tested with the GCC compiler.
void spc_interrupt_handler(void) __attribute__ ((section(".data")));
uint32_t non_blocking_flash_row_write(uint16_t row_num)
__attribute__((section(".data")));
bool load_flash_bytes(uint8_t *data);
bool configure_clock(void);

//SPC interrupt configuration
const cy_stc_sysint_t spc_int_config =
{
    .intrSrc = (IRQn_Type)cpuss_interrupt_spcif_IRQn,
    .intriority = 0U,
};

//--------------------------------------------------------
int main()
{
```

```
            bool ret;

                   // Create a dummy buffer with known data
            for(uint32_t i = 0u; i < FLASH_ROW_SIZE; i++)
                data_to_write[i] = i + 2;
                  }

           // Assign SPC interrupt handler
           Cy_SysInt_Init(&spc_int_config, &spc_interrupt_handler);

           // Enable interrupts
           __enable_irq();
           NVIC_EnableIRQ(spc_int_config.intrSrc);
       // Write to Flash; you should analyze each return value before proceeding to
next step
           ret = load_flash_bytes(data_to_write);
           ret = configure_clock();
           ret = non_blocking_flash_row_write(ROW_NUMBER_TO_WRITE);
           /* Loop forever */
           for(;;)
       {
           }
}
//-------------------------------------------------------------
// load_flash_bytes
//
// This function loads the page latch buffer with data to be programmed into a row of
// flash. Data loaded into the page latch buffer remains until a program operation
// is performed, which clears the page latch contents.
//-------------------------------------------------------------
#define SROM_LOAD_FLASH_API_OPCODE (0x04u)
#define SROM_LOAD_FLASH_KEY_TWO (0xD7u)
#define SROM_LATCH_BUFFER_ADDR (0x00u)
bool load_flash_bytes(uint8_t *data)
{
       uint32_t ret;
           // Fill in the arguments for API.
          srom_arg_buf[SROM_API_ARG0_OFFSET] = (uint32_t)((SROM_LATCH_BUFFER_ADDR <<
  SROM_PARAM_OFFSET)|(SROM_LOAD_FLASH_KEY_TWO << SROM_KEY_TWO_OFFSET)|SROM_KEY_ONE);
       // Number of bytes to flash - 1 (e.g., 0x00 - 1 byte, 0xFF - 256 bytes)
           srom_arg_buf[SROM_API_ARG1_OFFSET] = FLASH_ROW_SIZE-1;
           // Copy data to write in a temp buf which is eventually passed to SROM API.
          memcpy ((void *)&srom_arg_buf[SROM_API_DATA_OFFSET], data, FLASH_ROW_SIZE);
           //Set SYSARG, SYSREQ
           CPUSS_SYSARG = (uint32_t)&srom_arg_buf[SROM_API_ARG0_OFFSET];
          CPUSS_SYSREQ = (CPUSS_SYSREQ_SYSCALL_REQ_Msk | SROM_LOAD_FLASH_API_OPCODE);
           __asm("NOP\n");
           // Read the result and provide return.
           ret = CPUSS_SYSARG;
           return ((ret & CPUSS_SYSARG_RETURN_VALUE_MASK) ==
CPUSS_SYSARG_PASS_RETURN_VALUE);
}
```

```
//-------------------------------------------------------------
// configure_clock
//
// This function initializes the clock necessary for flash programming and erasing
// operations. This API is used to ensure that the charge pump clock and the HF clock
// are set to IMO at 48 MHz before calling the flash write and flash erase APIs.
//-------------------------------------------------------------
#define SROM_CONFIGURE_CLOCK_API_OPCODE (0x15u)
#define SROM_CONFIGURE_CLOCK_KEY_TWO (0xE8)
bool configure_clock(void)
{
          uint32_t ret;
          //Set SYSARG, SYSREQ
          CPUSS_SYSARG = (uint32_t)((SROM_CONFIGURE_CLOCK_KEY_TWO <<
SROM_KEY_TWO_OFFSET) |
   SROM_KEY_ONE);
       CPUSS_SYSREQ = (CPUSS_SYSREQ_SYSCALL_REQ_Msk |
SROM_CONFIGURE_CLOCK_API_OPCODE);
          __asm("NOP\n");
          ret = CPUSS_SYSARG;
          return ((ret & CPUSS_SYSARG_RETURN_VALUE_MASK) ==
CPUSS_SYSARG_PASS_RETURN_VALUE);
}

//-------------------------------------------------------------
// non_blocking_flash_row_write
//
// This function writes a flash row in a non-blocking manner, so that the CPU can
execute
// code from SRAM while the write operation is being done. Call the Load Flash Bytes
// function before calling this function, to load the data bytes that will be used for
// programming the row. Call the Configure Clock API before calling this function.
//-------------------------------------------------------------
#define SROM_NB_FLASH_ROW_API_OPCODE (0x07u)
#define SROM_NB_FLASH_ROW_NUM_KEY_TWO (0xDAu)
uint32_t non_blocking_flash_row_write(uint16_t row_num)
{
       uint32_t ret;
          /* This command results in three SPC interrupts. Reset the counter. */
          spc_intr_counter = 0;
          /* Arguments */
          srom_arg_buf[SROM_API_ARG0_OFFSET] = (uint32_t)((row_num <<
SROM_PARAM_OFFSET)|
   (SROM_NB_FLASH_ROW_NUM_KEY_TWO << SROM_KEY_TWO_OFFSET)|SROM_KEY_ONE);
          //Set SYSARG, SYSREQ
          CPUSS_SYSARG = (uint32_t)&srom_arg_buf[SROM_API_ARG0_OFFSET];
          CPUSS_SYSREQ = (CPUSS_SYSREQ_SYSCALL_REQ_Msk |
SROM_NB_FLASH_ROW_API_OPCODE);
          __asm("NOP\n");
```

```
// The non-blocking write row system call has three phases. Execute user code until
// three SPC interrupts have occurred.
          while (spc_intr_counter < 3)
       {
// PUT YOUR CODE THAT WILL BE EXECUTED DURING FLASH WRITE HERE
       }
          ret = CPUSS_SYSARG;
// PUT YOUR CODE THAT WILL BE EXECUTED DURING FLASH WRITE HERE
       }
          ret = CPUSS_SYSARG;
          return ((ret & CPUSS_SYSARG_RETURN_VALUE_MASK) ==
CPUSS_SYSARG_PASS_RETURN_VALUE);
}
// Interrupt handler that calls the Resume Non-Blocking function, which is required for
// completion of the non-blocking write operation.
// This function is executed from RAM as it is executed during a Non-Blocking System
Call.
#define SROM_RESUME_NB_API_OPCODE (0x09u)
#define SROM_RESUME_NB_KEY_TWO (0xDCu)
void spc_interrupt_handler(void)
{
// Execute Resume Non-Blocking API Syscall
// Arguments
         srom_arg_buf[SROM_API_ARG0_OFFSET] = (uint32_t)((SROM_RESUME_NB_KEY_TWO <<
   SROM_KEY_TWO_OFFSET)|SROM_KEY_ONE);
//Set SYSARG and SYSREQ
          CPUSS_SYSARG = (uint32_t)&srom_arg_buf[SROM_API_ARG0_OFFSET];
          CPUSS_SYSREQ = (CPUSS_SYSREQ_SYSCALL_REQ_Msk | SROM_RESUME_NB_API_OPCODE);
          spc_intr_counter++;
}
```

In the code, the CM0 exception table is configured to be in SRAM by writing 0x01 to the CPUSS_CONFIG register. The SRAM exception table should have the vector address of the SPC interrupt as the address of the *SpcIntHandler()* function, which is also defined to be in SRAM. See the **“Interrupts”** on page 29 for details on configuring the CM0 exception table to be in SRAM. The pseudo code for a non-blocking program system call is also similar, except that the function opcode and parameters will differ and the iStatusInt variable should be polled for 1 instead of 3. This is because the SPC ISR will be triggered only once for a non-blocking program system call.

References

[1] Infineon Technologies AG: *002-31596 – CYPM1011, EZ-PD™ PMG1-S0 Power Delivery MCU Gen 1;* **Available online**

[2] Infineon Technologies AG: *002-31842 – EZ-PD™ PMG1-S0 MCU registers reference manual* ; **Available online**

[3] Infineon Technologies AG: 002-33540 – *PMG1x (CYPMxxxx) Programming specification;* **Available online**

Glossary

The Glossary section explains the terminology used in this Reference Manual. Glossary terms are characterized in ***bold, italic font*** throughout the text of this manual.

A

accumulator — In a CPU, a register in which intermediate results are stored. Without an accumulator, it is necessary to write the result of each calculation (addition, subtraction, shift, and so on.) to main memory and read them back. Access to main memory is slower than access to the accumulator, which usually has direct paths to and from the arithmetic and logic unit (ALU).

active high — 1. A logic signal having its asserted state as the logic 1 state.
2. A logic signal having the logic 1 state as the higher voltage of the two states.

active low — 1. A logic signal having its asserted state as the logic 0 state.
2. A logic signal having its logic 1 state as the lower voltage of the two states: inverted logic.

address — The label or number identifying the memory location (RAM, ROM, or register) where a unit of information is stored.

algorithm — A procedure for solving a mathematical problem in a finite number of steps that frequently involve repetition of an operation.

ambient temperature — The temperature of the air in a designated area, particularly the area surrounding the device.

analog — See ***analog signals***.

analog blocks — The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.

analog output — An output that is capable of driving any voltage between the supply rails, instead of just a logic 1 or logic 0.

analog signals — A signal represented in a continuous form with respect to continuous times, as contrasted with a digital signal represented in a discrete (discontinuous) form in a sequence of time.

analog-to-digital (ADC) — A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The *digital-to-analog (DAC)* converter performs the reverse operation.

AND — See *Boolean Algebra*.

Glossary

API (Application Programming Interface)	A series of software routines that comprise an interface between a computer application and lower-level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
array	An array, also known as a vector or list, is one of the simplest data structures in computer programming. Arrays hold a fixed number of equally-sized data elements, generally of the same data type. Individual elements are accessed by index using a consecutive range of integers, as opposed to an associative array. Most high-level programming languages have arrays as a built-in data type. Some arrays are multi-dimensional, meaning they are indexed by a fixed number of integers; for example, by a group of two integers. One- and two-dimensional arrays are the most common. Also, an array can be a group of capacitors or resistors connected in some common form.
assembly	A symbolic representation of the machine language of a specific processor. Assembly language is converted to machine code by an assembler. Usually, each line of assembly code produces one machine instruction, though the use of macros is common. Assembly languages are considered low-level languages; where as C is considered a high-level language.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
attenuation	The decrease in intensity of a signal as a result of absotion of energy and of scattering out of the path to the detector, but not including the reduction due to geometric spreading. Attenuation is usually expressed in dB.

B

bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of V_T with the negative temperature coefficient of V_{BE}, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.
bias	1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.
bias current	The constant low-level DC current that is used to produce a stable operation in amplifiers. This current can sometimes be changed to alter the bandwidth of an amplifier.

Glossary

binary	The name for the base 2 numbering system. The most common numbering system is the base 10 numbering system. The base of a numbering system indicates the number of values that may exist for a particular positioning within a number for that system. For example, in base 2, binary, each position may have one of two values (0 or 1). In the base 10, decimal, numbering system, each position may have one of ten values (0, 1, 2, 3, 4, 5, 6, 7, 8, and 9).
bit	A single digit of a binary number. Therefore, a bit may only have a value of '0' or '1'. A group of 8 bits is called a byte. Because the EZ-PD™ PMG1-S0 MCU M8CP is an 8-bit microcontroller, the EZ-PD™ PMG1-S0 MCU device's native data chunk size is a byte.
bit rate (BR)	The number of bits occurring per unit of time in a bit stream, usually expressed in bits per second (bps).
block	1. A functional unit that performs a single function, such as an oscillator. 2. A functional unit that may be configured to perform one of several functions, such as a digital EZ-PD™ PMG1-S0 MCU block or an analog EZ-PD™ PMG1-S0 MCU block.
Boolean Algebra	In mathematics and computer science, Boolean algebras or Boolean lattices, are algebraic structures which "capture the essence" of the logical operations AND, OR and NOT as well as the set theoretic operations union, intersection, and complement. Boolean algebra also defines a set of theorems that describe how Boolean equations can be manipulated. For example, these theorems are used to simplify Boolean equations, which will reduce the number of logic elements needed to implement the equation. The operators of Boolean algebra may be represented in various ways. Often they are simply written as AND, OR, and NOT. In describing circuits, NAND (NOT AND), NOR (NOT OR), XNOR (exclusive NOT OR), and XOR (exclusive OR) may also be used. Mathematicians often use + (for example, A+B) for OR and • for AND (for example, A*B) (in some ways those operations are analogous to addition and multiplication in other algebraic structures) and represent NOT by a line drawn above the expression being negated (for example, ~A, A_, !A).
break-before-make	The elements involved go through a disconnected state entering ('break") before the new connected state ("make").
broadcast net	A signal that is routed throughout the microcontroller and is accessible by many blocks or systems.
buffer	1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for I/O operations, into which data is read, or from which data is written. 2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device. 3. An amplifier used to lower the output impedance of a system.

Glossary

bus	1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns. 2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0]. 3. One or more conductors that serve as a common connection for a group of related devices.
byte	A digital storage unit consisting of 8 bits.

C

C	A high-level programming language.
capacitance	A measure of the ability of two adjacent conductors, separated by an insulator, to hold a charge when a voltage differential is applied between them. Capacitance is measured in units of Farads.
capture	To extract information automatically through the use of software or hardware, as opposed to hand-entering of data into a computer file.
chaining	Connecting two or more 8-bit digital blocks to form 16-, 24-, and even 32-bit functions. Chaining allows certain signals such as Compare, Carry, Enable, Capture, and Gate to be produced from one block to another.
checksum	The checksum of a set of data is generated by adding the value of each data word to a sum. The actual checksum can simply be the result sum or a value that must be added to the sum to generate a pre-determined value.
clear	To force a bit/register to a value of logic ‘0’.
clock	The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.
clock generator	A circuit that is used to generate a clock signal.
CMOS	The logic gates constructed using *MOS* transistors connected in a complementary manner. CMOS is an acronym for complementary metal-oxide semiconductor.
comparator	An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.
compiler	A program that translates a high-level language, such as C, into machine language.
configuration	In a computer system, an arrangement of functional units according to their nature, number, and chief characteristics. Configuration pertains to hardware, software, firmware, and documentation. The configuration will affect system performance.
configuration space	In EZ-PD™ PMG1-S0 MCU devices, the register space accessed when the XIO bit, in the CPU_F register, is set to ‘1’.

Glossary

crowbar	A type of over-voltage protection that rapidly places a low-resistance shunt (typically an SCR) from the signal to one of the power supply rails, when the output voltage exceeds a predetermined value.
CPUSS	CPU subsystem
crystal oscillator	An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components.
cyclic redundancy check (CRC)	A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other puoses such as data compression.

D

data bus	A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions.
data stream	A sequence of digitally encoded signals used to represent information in transmission.
data transmission	Sending data from one place to another by means of signals over a channel.
debugger	A hardware and software system that allows the user to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory.
dead band	A period of time when neither of two or more signals are in their active state or in transition.
decimal	A base-10 numbering system, which uses the symbols 0, 1, 2, 3, 4, 5, 6, 7, 8 and 9 (called digits) together with the decimal point and the sign symbols + (plus) and - (minus) to represent numbers.
default value	Pertaining to the pre-defined initial, original, or specific setting, condition, value, or action a system will assume, use, or take in the absence of instructions from the user.
device	The device referred to in this manual is the EZ-PD™ PMG1-S0 MCU device, unless otherwise specified.
die	An non-packaged integrated circuit (IC), normally cut from a wafer.
digital	A signal or function, the amplitude of which is characterized by one of two discrete values: ‘0’ or ‘1’.
digital blocks	The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI.
digital logic	A methodology for dealing with expressions containing two-state variables that describe the behavior of a circuit or system.

Glossary

digital-to-analog (DAC)	A device that changes a digital signal to an analog signal of corresponding magnitude. The *analog-to-digital (ADC)* converter performs the reverse operation.
direct access	The capability to obtain data from a storage device, or to enter data into a storage device, in a sequence independent of their relative positions by means of addresses that indicate the physical location of the data.
duty cycle	The relationship of a clock period *high time* to its *low time*, expressed as a percent.

F

falling edge	A transition from a logic 1 to a logic 0. Also known as a negative edge.
feedback	The return of a portion of the output, or processed portion of the output, of a (usually active) device to the input.
filter	A device or process by which certain frequency components of a signal are attenuated.
firmware	The software that is embedded in a hardware device and executed by the CPU. The software may be executed by the end user, but it may not be modified.
flag	Any of various types of indicators used for identification of a condition or event (for example, a character that signals the termination of a transmission).
Flash	An electrically programmable and erasable, *volatile* technology that provides users with the programmability and data storage of EPROMs, plus in-system erasability. Nonvolatile means that the data is retained when power is off.
Flash bank	A group of flash ROM blocks where flash block numbers always begin with ‘0’ in an individual flash bank. A flash bank also has its own block level protection information.
Flash block	The smallest amount of flash ROM space that may be programmed at one time and the smallest amount of flash space that may be protected. A flash block holds 64 bytes.
flip-flop	A device having two stable states and two input terminals (or types of input signals) each of which corresponds with one of the two states. The circuit remains in either state until it is made to change to the other state by application of the corresponding signal.
frequency	The number of cycles or events per unit of time, for a periodic function.

G

gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
gate	1. A device having one output channel and one or more input channels, such that the output channel state is completely determined by the input channel states, except during switching transients. 2. One of many types of combinational logic elements having at least two inputs (for example, AND, OR, NAND, and NOR (also see *Boolean Algebra*)).

Glossary

ground

1. The electrical neutral line having the same potential as the surrounding earth.
2. The negative side of DC power supply.
3. The reference point for an electrical system.
4. The conducting paths between an electric circuit or equipment and the earth, or some conducting body serving in place of the earth.

H

hardware

A comprehensive term for all of the physical parts of a computer or embedded system, as distinguished from the data it contains or operates on, and the software that provides instructions for the hardware to accomplish tasks.

hardware reset

A reset that is caused by a circuit, such as a POR, watchdog reset, or external reset. A hardware reset restores the state of the device as it was when it was first powered up. Therefore, all registers are set to the POR value as indicated in register tables throughout this document.

hexadecimal

A base 16 numeral system (often abbreviated and called hex), usually written using the symbols 0-9 and A-F. It is a useful system in computers because there is an easy mapping from four bits to a single hex digit. Thus, one can represent every byte as two consecutive hexadecimal digits. Compare the binary, hex, and decimal representations:

bin = hex = dec
0000b = 0x0 = 0
0001b = 0x1 = 1
0010b = 0x2 = 2
...
1001b = 0x9 = 9
1010b = 0xA = 10
1011b = 0xB = 11
...
1111b = 0xF = 15

So the decimal numeral 79 whose binary representation is 0100 1111b can be written as 4Fh in hexadecimal (0x4F).

high time

The amount of time the signal has a value of '1' in one period, for a periodic digital signal.

I

I2C

A two-wire serial computer bus by Phillips Semiconductors (now NXP Semiconductors). I^2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I^2C uses only two bidirectional pins, clock and data, both running at +5 V and pulled high with resistors. The bus operates at 100 Kbps in standard mode and 400 Kbps in fast mode.

Glossary

idle state	A condition that exists whenever user messages are not being transmitted, but the service is immediately available for use.
impedance	1. The resistance to the flow of current caused by resistive, capacitive, or inductive devices in a circuit. 2. The total passive opposition offered to the flow of electric current. Note the impedance is determined by the particular combination of resistance, inductive reactance, and capacitive reactance in a given circuit.
input	A point that accepts data, in a device, process, or channel.
input/output (I/O)	A device that introduces data into or extracts data from a system.
instruction	An expression that specifies one operation and identifies its operands, if any, in a programming language such as C or assembly.
instruction mnemonics	A set of acronyms that represent the opcodes for each of the assembly-language instructions, for example, ADD, SUBB, MOV.
integrated circuit (IC)	A device in which components such as resistors, capacitors, diodes, and *transistors* are formed on the surface of a single piece of semiconductor.
interface	The means by which two systems or devices are connected and interact with each other.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8CP receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.

J

jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.

L

latency	The time or delay that it takes for a signal to pass through a given circuit or network.

Glossary

least significant bit (LSb)	The binary digit, or bit, in a binary number that represents the least significant value (typically the right-hand bit). The bit versus byte distinction is made by using a lower case “b” for bit in LSb.
least significant byte (LSB)	The byte in a multi-byte word that represents the least significant values (typically the right-hand byte). The byte versus bit distinction is made by using an upper case “B” for byte in LSB.
Linear Feedback Shift Register (LFSR)	A shift register whose data input is generated as an *XOR* of two or more elements in the register chain.
load	The electrical demand of a process expressed as power (watts), current (amps), or resistance (ohms).
logic function	A mathematical function that performs a digital operation on digital data and returns a digital value.
lookup table (LUT)	A logic block that implements several logic functions. The logic function is selected by means of select lines and is applied to the inputs of the block. For example: A 2 input LUT with 4 select lines can be used to perform any one of 16 logic functions on the two inputs resulting in a single logic output. The LUT is a combinational device; therefore, the input/output relationship is continuous, that is, not sampled.
low time	The amount of time the signal has a value of ‘0’ in one period, for a periodic digital signal.
low-voltage detect (LVD)	A circuit that senses V_{DDD} and provides an interrupt to the system when V_{DDD} falls below a selected threshold.

M

M8CP	An 8-bit Harvard Architecture microprocessor. The microprocessor coordinates all activity inside a EZ-PD™ PMG1-S0 MCU device by interfacing to the flash, SRAM, and register space.
macro	A programming language macro is an abstraction, whereby a certain textual pattern is replaced according to a defined set of rules. The intereter or compiler automatically replaces the macro instance with the macro contents when an instance of the macro is encountered. Therefore, if a macro is used five times and the macro definition required 10 bytes of code space, 50 bytes of code space will be needed in total.
mask	1. To obscure, hide, or otherwise prevent information from being derived from a signal. It is usually the result of interaction with another signal, such as noise, static, jamming, or other forms of interference. 2. A pattern of bits that can be used to retain or suppress segments of another pattern of bits, in computing and data processing systems.

Glossary

master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the *slave device*.
microcontroller	An integrated circuit device that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and I/O circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of devices, thus achieving maximal possible miniaturization. This in turn, will reduce the volume and the cost of the controller. The microcontroller is normally not used for general-puose computation as is a microprocessor.
mnemonic	A tool intended to assist the memory. Mnemonics rely on not only repetition to remember facts, but also on creating associations between easy-to-remember constructs and lists of data. A two to four character string representing a microprocessor instruction.
mode	A distinct method of operation for software or hardware. For example, the Digital EZ-PD™ PMG1-S0 MCU block may be in either counter mode or timer mode.
modulation	A range of techniques for encoding information on a carrier signal, typically a sine-wave signal. A device that performs modulation is known as a modulator.
Modulator	A device that imposes a signal on a carrier.
MOS	An acronym for metal-oxide semiconductor.
most significant bit (MSb)	The binary digit, or bit, in a binary number that represents the most significant value (typically the left-hand bit). The bit versus byte distinction is made by using a lower case “b” for bit in MSb.
most significant byte (MSB)	The byte in a multi-byte word that represents the most significant values (typically the left-hand byte). The byte versus bit distinction is made by using an upper case “B” for byte in MSB.
multiplexer (mux)	1. A logic function that uses a binary value, or address, to select between a number of inputs and conveys the data from the selected input to the output. 2. A technique which allows different input (or output) signals to use the same lines at different times, controlled by an external signal. Multiplexing is used to save on wiring and I/O ports.

N

NAND	See *Boolean Algebra*.
negative edge	A transition from a logic 1 to a logic 0. Also known as a falling edge.
net	The routing between devices.
nibble	A group of four bits, which is one-half of a byte.

Glossary

noise	1. A disturbance that affects a signal and that may distort the information carried by the signal. 2. The random variations of one or more characteristics of any entity such as voltage, current, or data.
NOR	See *Boolean Algebra*.
NOT	See *Boolean Algebra*.
O	
OR	See *Boolean Algebra*.
oscillator	A circuit that may be crystal controlled and is used to generate a clock frequency.
output	The electrical signal or signals which are produced by an analog or digital block.
P	
parallel	The means of communication in which digital data is sent multiple bits at a time, with each simultaneous bit being sent over a separate line.
parameter	Characteristics for a given block that have either been characterized or may be defined by the designer.
parameter block	A location in memory where parameters for the SSC instruction are placed before execution.
parity	A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).
path	1. The logical sequence of instructions executed by a computer. 2. The flow of an electrical signal through a circuit.
pending interrupts	An interrupt that is triggered but not serviced, either because the processor is busy servicing another interrupt or global interrupts are disabled.
phase	The relationship between two signals, usually the same frequency, that determines the delay between them. This delay between signals is either measured by time or angle (degrees).
pin	A terminal on a hardware component. Also called lead.
pinouts	The pin number assignment: the relation between the logical inputs and outputs of the EZ-PD™ PMG1-S0 MCU device and their physical countearts in the printed circuit board (PCB) package. Pinouts will involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.
port	A group of pins, usually eight.

Glossary

positive edge	A transition from a logic 0 to a logic 1. Also known as a rising edge.
posted interrupts	An interrupt that is detected by the hardware but may or may not be enabled by its mask bit. Posted interrupts that are not masked become pending interrupts.
Power On Reset (POR)	A circuit that forces the EZ-PD™ PMG1-S0 MCU device to reset when the voltage is below a pre-set level. This is one type of *hardware reset*.
program counter	The instruction pointer (also called the program counter) is a register in a computer processor that indicates where in memory the CPU is executing instructions. Depending on the details of the particular machine, it holds either the address of the instruction being executed, or the address of the next instruction to be executed.
protocol	A set of rules. Particularly the rules that govern networked communications.
pulse	A rapid change in some characteristic of a signal (for example, phase or frequency), from a baseline value to a higher or lower value, followed by a rapid return to the baseline value.
pulse width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied measure.

R

RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a know state. See *hardware reset* and *software reset*.
resistance	The resistance to the flow of electric current measured in ohms for a conductor.
revision ID	A unique identifier of the EZ-PD™ PMG1-S0 MCU device.
ripple divider	An asynchronous ripple counter constructed of flip-flops. The clock is fed to the first stage of the counter. An n-bit binary counter consisting of n flip-flops that can count in binary from 0 to 2^n - 1.
rising edge	*See positive edge*.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
routine	A block of code, called by another block of code, that may have some general or frequent use.
routing	Physically connecting objects in a design according to design rules set in the reference library.

Glossary

runt pulses	In digital circuits, narrow pulses that, due to non-zero rise and fall times of the signal, do not reach a valid high or low level. For example, a runt pulse may occur when switching between asynchronous clocks or as the result of a race condition in which a signal takes two separate paths through a circuit. These race conditions may have different delays and are then recombined to form a glitch or when the output of a flip-flop becomes metastable.

S

sampling	The process of converting an analog signal into a series of digital values or reversed.
schematic	A diagram, drawing, or sketch that details the elements of a system, such as the elements of an electrical circuit or the elements of a logic diagram for a computer.
seed value	An initial value loaded into a linear feedback shift register or random number generator.
serial	1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.
set	To force a bit/register to a value of logic 1.
settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.
shift	The movement of each bit in a word one position to either the left or right. For example, if the hex value 0x24 is shifted one place to the left, it becomes 0x48. If the hex value 0x24 is shifted one place to the right, it becomes 0x12.
shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
sign bit	The most significant binary digit, or bit, of a signed binary number. If set to a logic 1, this bit represents a negative quantity.
signal	A detectable transmitted energy that can be used to carry information. As applied to electronics, any transmitted electrical impulse.
silicon ID	A unique identifier of the EZ-PD™ PMG1-S0 MCU silicon.
skew	The difference in arrival time of bits transmitted at the same time, in parallel transmission.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.

Glossary

software	A set of computer programs, procedures, and associated documentation about the operation of a data processing system (for example, compilers, library routines, manuals, and circuit diagrams). Software is often written first as source code, and then converted to a binary format that is specific to the device on which the code will be executed.
software reset	A partial reset executed by software to bring part of the system back to a known state. A software reset will restore the M8CP to a know state but not EZ-PD™ PMG1-S0 MCU blocks, systems, peripherals, or registers. For a software reset, the CPU registers (CPU_A, CPU_F, CPU_PC, CPU_SP, and CPU_X) are set to 0x00. Therefore, code execution will begin at flash address 0x0000.
SRAM	An acronym for static random access memory. A memory device allowing users to store and retrieve data at a high rate of speed. The term static is used because, when a value is loaded into an SRAM cell, it will remain unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform flash operations. The functions of the SROM may be accessed in normal user code, operating from flash.
stack	A stack is a data structure that works on the principle of Last In First Out (LIFO). This means that the last item put on the stack is the first item that can be taken off.
stack pointer	A stack may be represented in a computer's inside blocks of memory cells, with the bottom at a fixed location and a variable stack pointer to the current top cell.
state machine	The actual implementation (in hardware or software) of a function that can be considered to consist of a set of states through which it sequences.
sticky	A bit in a register that maintains its value past the time of the event that caused its transition, has passed.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
switching	The controlling or routing of signals in circuits to execute logical or arithmetic operations, or to transmit data between specific points in a network.
switch phasing	The clock that controls a given switch, PHI1 or PHI2, in respect to the switch capacitor (SC) blocks. The EZ-PD™ PMG1-S0 MCU SC blocks have two groups of switches. One group of these switches is normally closed during PHI1 and open during PHI2. The other group is open during PHI1 and closed during PHI2. These switches can be controlled in the normal operation, or in reverse mode if the PHI1 and PHI2 clocks are reversed.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.

Glossary

T

tap	The connection between two blocks of a device created by connecting several blocks/components in a series, such as a shift register or resistive voltage divider.
terminal count	The state at which a counter is counted down to zero.
threshold	The minimum value of a signal that can be detected by the system or sensor under consideration.
Thumb-2	The Thumb-2 instruction set is a highly efficient and powerful instruction set that delivers significant benefits in terms of ease of use, code size, and performance. The Thumb-2 instruction set is a superset of the previous 16-bit Thumb instruction set, with additional 16-bit instructions alongside 32-bit instructions.
transistors	The transistor is a solid-state semiconductor device used for amplification and switching, and has three terminals: a small current or voltage applied to one terminal controls the current through the other two. It is the key component in all modern electronics. In digital circuits, transistors are used as very fast electrical switches, and arrangements of transistors can function as logic gates, RAM-type memory, and other devices. In analog circuits, transistors are essentially used as amplifiers.
tristate	A function whose output can adopt three states: 0, 1, and Z (high impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same *net*.

U

UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user	The person using the EZ-PD™ PMG1-S0 MCU device and reading this manual.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital EZ-PD™ PMG1-S0 MCU Blocks. User Modules also provide high level *API (Application Programming Interface)* for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.

V

VDDD	A name for a power net meaning "voltage drain." The most positive power supply signal. Usually 5 or 3.3 volts.
volatile	Not guaranteed to stay the same value or level when not in scope.

Glossary

VSS	A name for a power net meaning "voltage source." The most negative power supply signal.

W

watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU will reset after a specified period of time.
waveform	The representation of a signal as a plot of amplitude versus time.

X

XOR	See *Boolean Algebra*.

Revision history

Document revision	Date	Description of changes
*B	2026-09-23	Publish to web. Migrated to Infineon template. Updated the following sections: • **"Non-blocking system call pseudo code"** on page 171 • **"EZ-PD™ PMG1 MCU resources"** on page 15 • **"Units of measure"** on page 17 • **"Acronyms"** on page 18 • **"Watchdog timer (WDT)"** on page 61 • **"Fail-Safe GPIOs"** on page 49 • **"Reset sources"** on page 64 • **"Universal serial bus (USB) Power Delivery (PD)"** on page 133 Updated the following tables: **Table 11-1**, **Table 11-2**, **Table 11-3**, **Table 11-6**, **Table 8-1**, and **Table 8-2** Update the following figures: **Figure 1-1**, **Figure 12-2**, **Figure 21-1**, through **Figure 21-11**, and **Figure 23-2**.
*C	2026-10-12	Updated disclaimer. Corrected the revision version error related to *B.

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition: 2026-10-12

Published by
Infineon Technologies AG
Am Campeon 1-15
85579 Neubiberg, Germany

© 2026 Infineon Technologies AG.
All rights reserved

Do you have a question about this document?
Email: erratum@infineon.com

Document reference:
002-31770 Rev. *C

Important Notice

Products which may also include samples and may be comprised of hardware or software or both ("Product(s)") are sold or provided and delivered by Infineon Technologies AG and its affiliates ("Infineon") subject to the terms and conditions of the frame supply contract or other written agreement(s) executed by a customer and Infineon or, in the absence of the foregoing, the applicable Sales Conditions of Infineon. General terms and conditions of a customer or deviations from applicable Sales Conditions of Infineon shall only be binding for Infineon if and to the extent Infineon has given its express written consent.

For the avoidance of doubt, Infineon disclaims all warranties of non-infringement of third-party rights and implied warranties such as warranties of fitness for a specific use/purpose or merchantability.

Infineon shall not be responsible for any information with respect to samples, the application or customer's specific use of any Product or for any examples or typical values given in this document.

If this document is marked as 'Preliminary', 'Target', 'Draft' or 'Proposal', Infineon reserves the right to change all information given in this document at any time without notice. Subject to the development and release of a Product for series supply by Infineon, the technical specifications of the Product are set forth in the relevant datasheet provided by Infineon without such marking.

The data contained in this document is exclusively intended for technically qualified and skilled customer representatives. It is the responsibility of the customer to evaluate the suitability of the Product for the intended application and the customer's specific use and to verify all relevant technical data contained in this document in the intended application and the customer's specific use. The customer is responsible for properly designing, programming, and testing the functionality and safety of the intended application, as well as complying with any legal requirements related to its use.

Unless otherwise explicitly approved by Infineon, Products may not be used in any application where a failure of the Products or any consequences of the use thereof can reasonably be expected to result in personal injury. However, the foregoing shall not prevent the customer from using any Product in such fields of use that Infineon has explicitly designed and sold it for, provided that the overall responsibility for the application lies with the customer.

Infineon expressly reserves the right to use its content for commercial text and data mining (TDM) according to applicable laws, e.g. Section 44b of the German Copyright Act (UrhG).

If the Product includes security features:
Because no computing device can be absolutely secure, and despite security measures implemented in the Product, Infineon does not guarantee that the Product will be free from intrusion, data theft or loss, or other breaches ("Security Breaches"), and Infineon shall have no liability arising out of any Security Breaches.

If this document includes or references software:
The software is owned by Infineon under the intellectual property laws and treaties of the United States, Germany, and other countries worldwide. All rights reserved.

Therefore, you may use the software only as provided in the software license agreement accompanying the software.

If no software license agreement applies, Infineon hereby grants you a personal, non-exclusive, non-transferable license (without the right to sublicense) under its intellectual property rights in the software (a) for software provided in source code form, to modify and reproduce the software solely for use with Infineon hardware products, only internally within your organization, and (b) to distribute the software in binary code form externally to end users, solely for use on Infineon hardware products. Any other use, reproduction, modification, translation, or compilation of the software is prohibited.

For further information on the Product, technology, delivery terms and conditions, and prices, please contact your nearest Infineon office or visit https://www.infineon.com.