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CYBLE-413124-01

EZ-BLE™ Module with HomeKit

General Description

The CYBLE-413124-01 is a Bluetooth® Low Energy wireless module solution with integrated Apple HomeKit support, including the authentication co-processor. The CYBLE-413124-01 includes onboard crystal oscillators, passive components, and the Cypress CYW20719 silicon device.

The CYBLE-413124-01 supports a number of peripheral functions (ADC and PWM), as well as UART serial communication protocol. The CYBLE-413124-01 includes a royalty-free Bluetooth LE stack compatible with Bluetooth 4.2 in a 14.7 × 20.0 × 1.40 mm package.

The CYBLE-413124-01 is designed to be used with an external antenna, and provides solder pad connections for antenna and ground connections. The CYBLE-413124-01 is certified by Bluetooth SIG, but does not include regulatory certifications.

Module Description

- Module size: 14.70 mm × 20.00 mm × 1.40 mm
- Extended Range:
  - Up to 400 meters bi-directional communication[1, 2]
  - Up to 450 meters in beacon only mode[1]
- Bluetooth LE 4.2 single-mode module
  - QDID: 97525
  - Declaration ID: D035376
- Compliant to FCC, ISED, and CE standards
- Castelated solder pad connections for ease-of-use
- 1024-KB flash memory, 512-KB SRAM memory
- Extended Industrial temperature range: –30 °C to +105 °C
- Cortex-M4F 32-bit processor operating up to 96 MHz
- Watchdog timer with dedicated internal low-speed oscillator

Power Consumption

- Maximum TX output power: +8.0 dBm[3]
- RX Receive Sensitivity: –93 dBm
- Received signal strength indicator (RSSI) with 1-dB resolution
- TX current consumption
  - Bluetooth LE silicon: 5.7 mA (MCU + radio, 0 dBm)
  - RFX2401C: 27 mA (PA/LNA only, module +8 dBm)
- RX current consumption
  - Bluetooth LE silicon: 5.8 mA (MCU + radio only)
  - RFX2401C: 7.5 mA (PA/LNA only)
- Cypress CYW20719 silicon low power mode support
  - PDS: 70 µA with 512 KB SRAM retention
  - Deep Sleep: 1 µA with 16 KB SRAM retention
  - HIDOFF: 350 nA with XRES wake up

Functional Capabilities

- Apple HomeKit compliant with on-board authentication co-processor
- Switched-cap Sigma-Delta ADC with internal reference
- UART serial communication block (PUART)
- Up to five PWMs supported
- Bluetooth LE protocol stack supporting generic access profile (GAP) Central, Peripheral, Observer, or Broadcaster roles

Benefits

CYBLE-413124-01 is fully tested solution and provides all necessary components required to operate Bluetooth LE communication standards.

- Proven hardware design ready to use
- Large non-volatile memory for complex application development
- Over-the-air update capable for development or field updates
- Bluetooth SIG qualified with QDID and Declaration ID
- WICED™ Studio provides an easy-to-use integrated design environment (IDE) to configure, develop, program, and test a Bluetooth LE application

Notes
1. Connection range tested module-to-module in full line-of-sight environment, free of obstacles or interference sources with output power of +8.0 dBm.
2. Specified as module-to-module range. Mobile phone connection range will decrease based on the PA/LNA performance of the mobile phone used.
3. The CYBLE-413124-01 is capable of higher output power than specified, but is intentionally limited to +8.0dBm due to regulatory requirements for European Standards.

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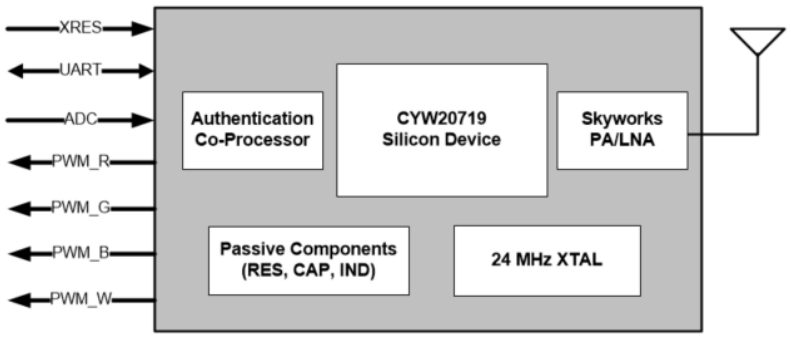
Overview

Functional Block Diagram

Figure 1 illustrates the CYBLE-413124-01 functional block diagram.

Figure 1. Functional Block Diagram



Module Description

The CYBLE-413124-01 module is a complete module designed to be soldered to the applications main board.

Module Dimensions and Drawing

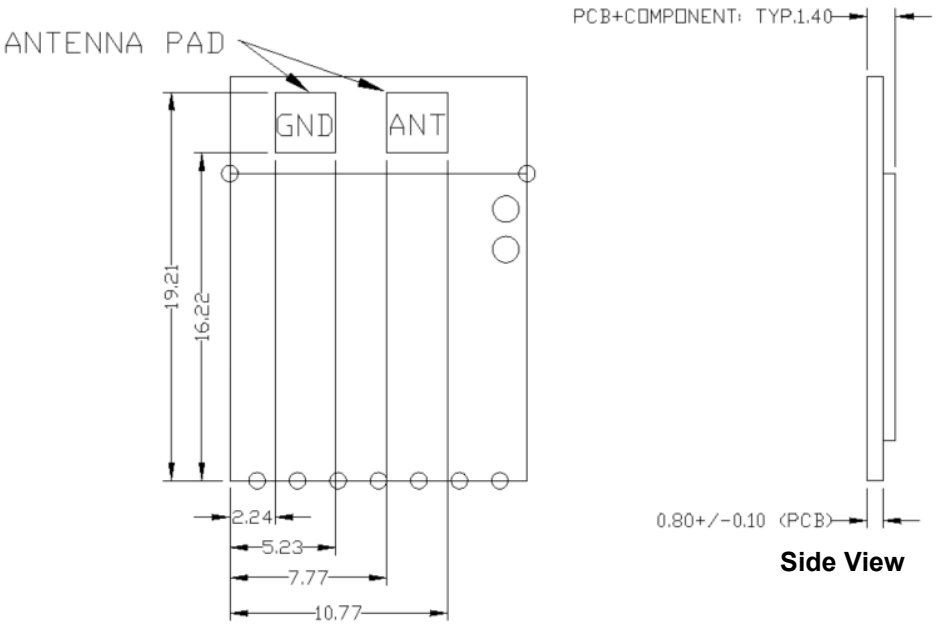
Cypress reserves the right to select components from various vendors to achieve the Bluetooth module functionality. Such selections will still guarantee that all mechanical specifications and module certifications are maintained. Any changes to the current BOM for the CYBLE-413124-01 will not be made until approval is provided by the end customer for this product. The CYBLE-413124-01 will be held within the physical dimensions shown in the mechanical drawings in Figure 2 on page 4. All dimensions are in millimeters (mm).

Table 1. Module Design Dimensions

Dimension Item		Specification
Module dimensions	Length (X)	14.70 ± 0.15 mm
	Width (Y)	20.00 ± 0.15 mm
Antenna connection location dimensions	Length (X)	14.70 mm
	Width (Y)	4.80 mm
PCB thickness	Height (H)	0.80 ± 0.10 mm
Shield height	Height (H)	N/A - No Shield
Maximum component height	Height (H)	0.60 mm typical
Total module thickness (bottom of module to highest component)	Height (H)	1.40 mm typical

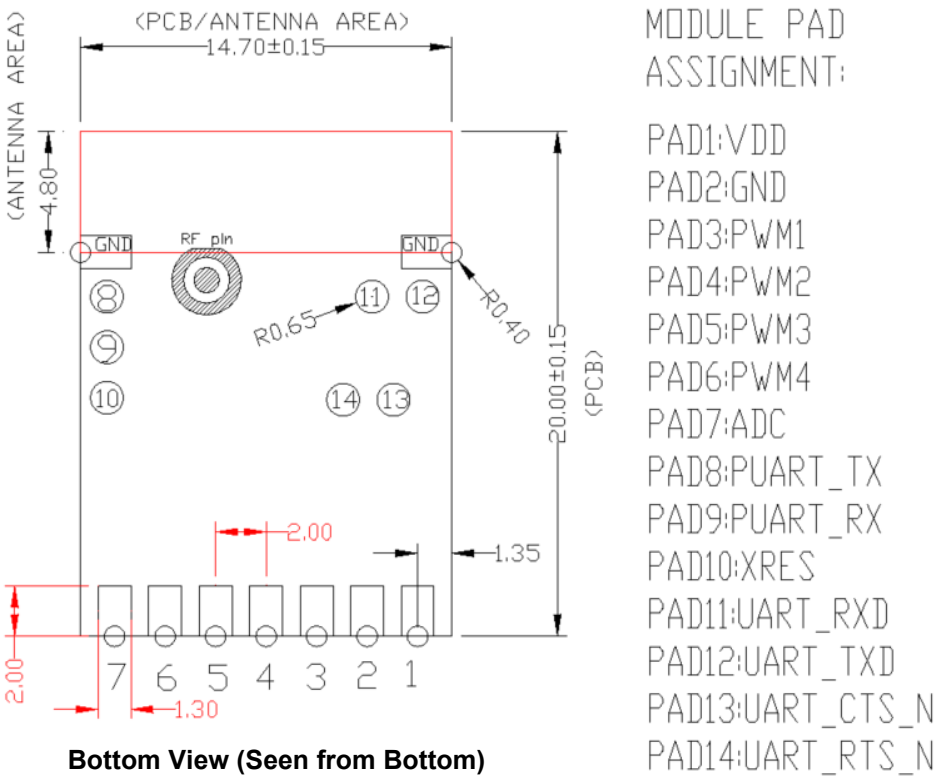
See Figure 2 on page 4 for the mechanical reference drawing for CYBLE-413124-01.

Figure 2. Module Mechanical Drawing[4, 5]



Top View (See from Top)

Side View



Bottom View (Seen from Bottom)

Notes

4. No metal should be located beneath or above the antenna area. Only bare PCB material should be located beneath the antenna area. For more information on recommended host PCB layout, see "Recommended Host PCB Layout" on page 6.
5. The CYBLE-413124-01 includes castellated pad connections, denoted as the circular openings at the pad location above.

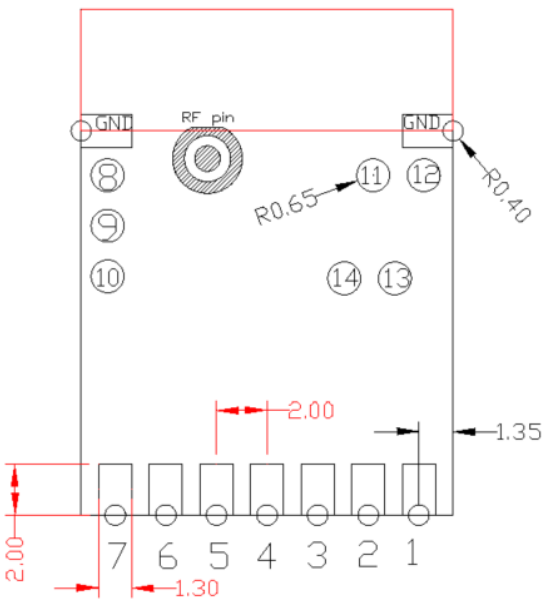
Pad Connection Interface

As shown in the bottom view of Figure 2 on page 4, the CYBLE-413124-01 has seven main connections that are connected to the host board via castellated solder pads (“CSP”). The CYBLE-413124-01 also includes additional solder pad connections (“SP”) used for debug or testing on the bottom side of the module. Table 2 and Figure 3 detail the solder pad length, width, and pitch dimensions of the CYBLE-413124-01 module.

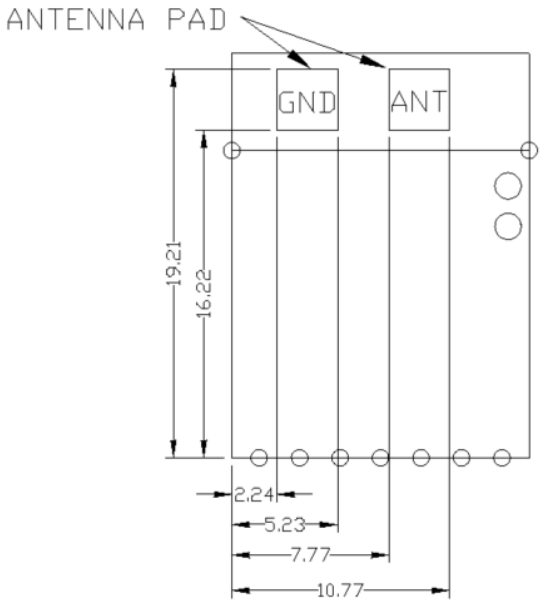
Table 2. Connection Description

Name	Connections	Connection Type	Pad Length Dimension	Pad Width Dimension	Pad Pitch
CSP	7	Castellated Solder Pads	2.00 mm	1.30 mm	2.00 mm
SP	7	Solder Pads	0.65 mm (Radius)	0.65 mm (Radius)	N/A
ANT	2	Solder Pads	3.00 mm	3.00 mm	5.54 mm

Figure 3. Solder Pad Dimensions (Seen from Bottom)



Signal Connection (Seen from Bottom)



Antenna Connection (Seen from Top)

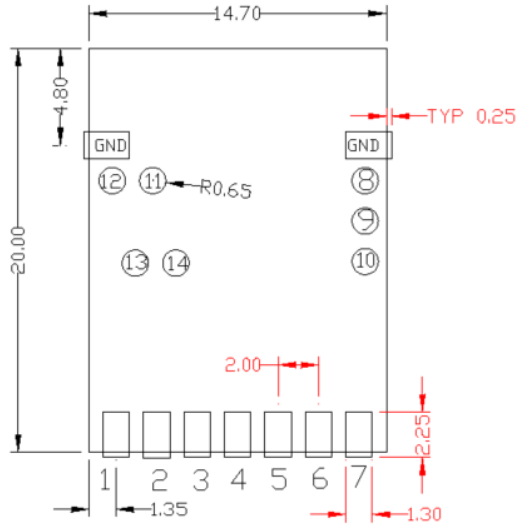
To maximize RF performance, the host layout should follow these recommendations:

1. Antenna Area Keepout: The host board directly below the antenna area of the Cypress module (see Figure 2 on page 4) must contain no ground or signal traces. This keep out area requirement applies to all layers of the host board.
2. Module Placement: The ideal placement of the Cypress Bluetooth module is in a corner of the host board with the PCB trace antenna located at the far corner. This placement minimizes the additional recommended keep out area stated in item 2. Please refer to AN96841 for module placement best practices.

Recommended Host PCB Layout

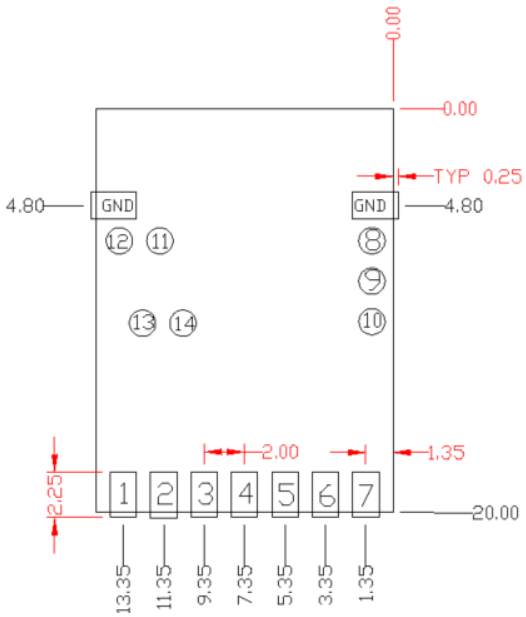
Figure 4 (Dimensioned) and Figure 5 (Relative to Origin) provide the recommended host PCB layout pattern for the CYBLE-413124-01. Pad length of 1.27 mm (0.655 mm from center of the pad on either side) shown in Figure 5 is the minimum recommended host pad length. All dimensions are in millimeters.

Figure 4. CYBLE-413124-01 Host Layout (Dimensioned)



Top View (Seen on Host PCB)

Figure 5. CYBLE-413124-01 Host Layout (Relative to Origin)



Top View (Seen on Host PCB)

Module Connections

Table 3 details the solder pad connection definitions and available functions for each connection pad. Table 3 lists the solder pads on the CYBLE-413124-01, the silicon device pin, and denotes what functions are available for each solder pad. Table 3 also lists the primary/intended function for each solder pad for the application this module was specifically designed for.

Table 3. Solder Pad Connection Definitions

Pad Number	Pad Name	UART	PWM	GPIO	Primary Function
1	VDD	Power Supply Input (3.30 V)			Power Supply Input
2	GND	Ground Connection			Ground Connection
3	PWM1		✓	✓	PWM R, G, B, or W Function
4	PWM2		✓	✓	PWM R, G, B, or W Function
5	PWM3		✓	✓	PWM R, G, B, or W Function
6	PWM4		✓	✓	PWM R, G, B, or W Function
7	ADC				ADC Input
8	PUART_TX	✓(PUART_TXD)			Peripheral UART TXD
9	PUART_RX	✓(PUART_RXD)	✓	✓	Peripheral UART RXD
10	XRES	External Reset Hardware Connection Input			External Reset (Active Low)
11	UART_RXD	✓(UART_RXD)			UART RXD
12	UART_TXD	✓(UART_TXD)			UART TXD
13	UART_CTS	✓(UART_CTS)			UART CTS
14	UART_RTS	✓(UART_RTS)			UART RTS
GND	GND	Ground Connection			Ground Connections Must be soldered to host board
GND	GND	Ground Connection			

Connections and Optional External Components

Power Connections (VDD)

The CYBLE-413124-01 contains one power supply connection, VDD.

VDD accepts a supply input of 3.30 V. Table 8 provides this specification. The maximum power supply ripple for this power connection is 300 mV, as shown in Table 8.

Considerations and Optional Components for Brown Out (BO) Conditions

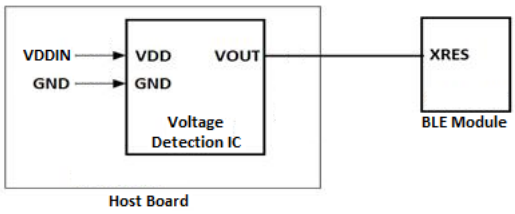
Power supply design must be completed to ensure that the CYBLE-413124-01 module does not encounter a Brown Out condition, which can lead to unexpected functionality, or module lock up. A Brown Out condition may be met if power supply provided to the module during power up or reset is in the range shown below:

$$V_{IL} \leq VDD \leq V_{IH}$$

Refer to Table 12 for the V_{IL} and V_{IH} specifications.

System design should ensure that the condition above is not encountered when power is removed from the system. In the event that this cannot be guaranteed (i.e. battery installation, high value power capacitors with slow discharge), it is recommended that an external voltage detection device be used to prevent the Brown Out voltage range from occurring during power removal. Please refer to Figure 6 for the recommended circuit design when using an external voltage detection IC.

Figure 6. Reference Circuit Block Diagram for External Voltage Detection IC



In the event that the module does encounter a Brown Out condition, and is operating erratically or not responsive, power cycling the module will correct this issue and once reset, the module should operate correctly. Brown Out conditions can potential cause issues that cannot be corrected, but in general, a power-on-reset operation will correct a Brown Out condition.

External Reset (XRES)

The CYBLE-413124-01 has an integrated power-on reset circuit which completely resets all circuits to a known power on state. This action can also be evoked by an external reset signal, forcing it into a power-on reset state. The XRES signal is an active-low signal, which is an input to the CYBLE-413124-01 module (solder pad 3). The CYBLE-413124-01 module does not require an external pull-up resistor on the XRES input

During power on operation, the XRES connection to the CYBLE-413124-01 is required to be held low 50 ms after the VDD power supply input to the module is stable. This can be accomplished in the following ways:

- The host device should connect a GPIO to the XRES of Cypress CYBLE-413124-01 module and pull XRES low until VDD is stable. XRES is recommended to be released 50 ms after VDD is stable.
- If the XRES connection of the CYBLE-413124-01 module is not used in the application, a 0.33 uF capacitor may be connected to the XRES solder pad of the CYBLE-413124-01 in order to delay the XRES release. The capacitor value for this recommended implementation is approximate, and the exact value may differ depending on the VDD power supply ramp time of the system. The capacitor value should result in an XRES release timing of 50 ms after VDD stability.
- The XRES release timing may be controlled by a external voltage detection IC. XRES should be released 50 ms after VDD is stable.

Refer to Figure 9 on page 12 for XRES operating and timing requirements during power on events.

UART Connections

For full UART functionality, all UART signals must be connected to the Host device. If full UART functionality is not being used, and only UART RXD and TXD are desired or capable, then the following connection considerations should be followed for UART RTS and CTS:

- UART RTS: Can be left floating, pulled low, or pulled high. RTS is not critical for initial firmware uploading at power on.
- UART CTS: Must by pulled low to bypass flow control and to ensure that continuous data transfers are made from the host to the module.

External Component Recommendation

Power Supply Circuitry

It is not required to place any power supply decoupling or noise reduction circuitry on the host PCB. If desired, an external ferrite bead between the supply and the module connection can be included, but is not necessary. If used, the ferrite bead should be positioned as close as possible to the module pin connection.

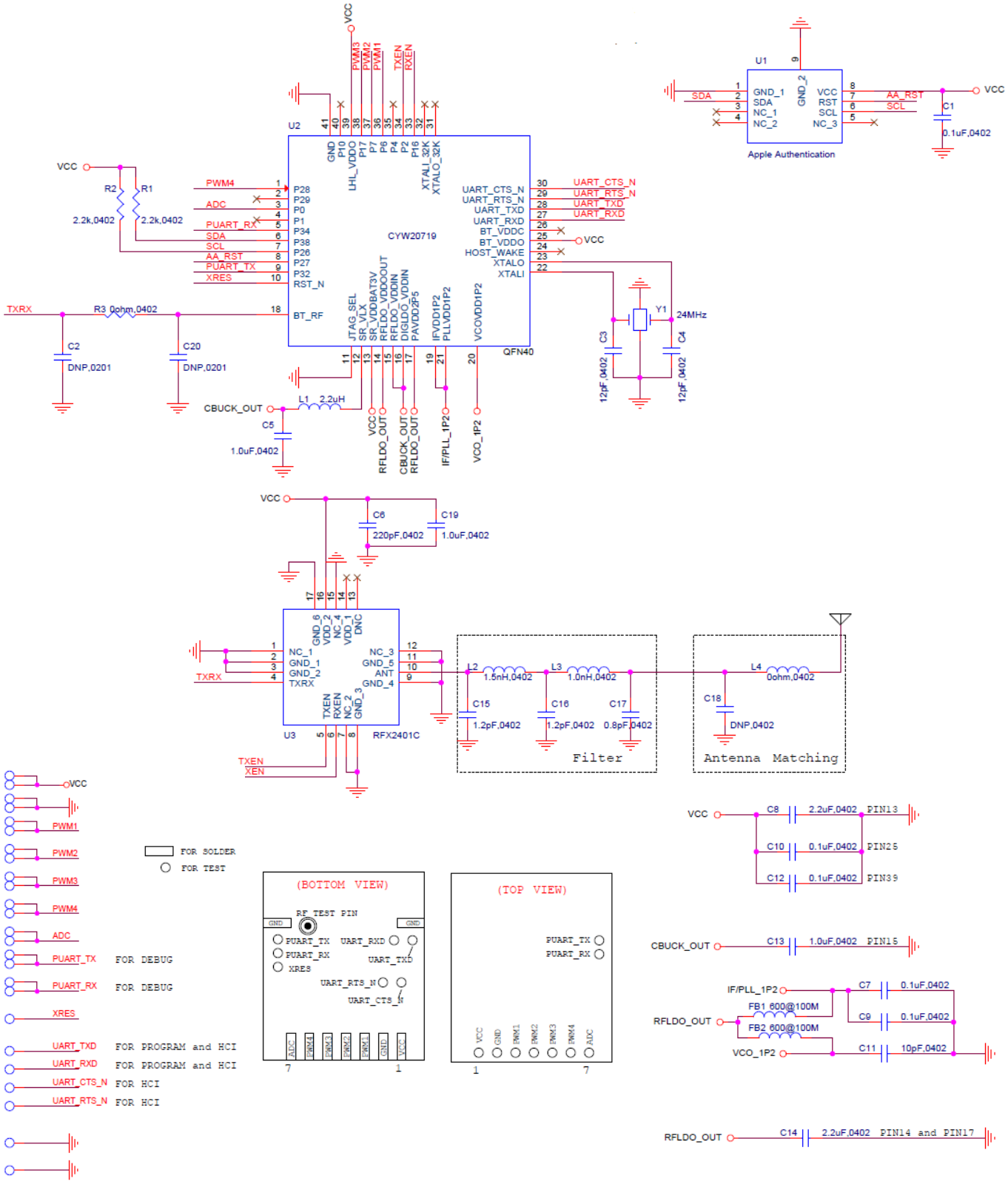
If used, the recommended ferrite bead value is 330 Ω, 100 MHz (Murata BLM21PG331SN1D).

Apple MFi Authentication Coprocessor Interface

The CYBLE-413124-01 comes with an integrated MFi authentication co-processor. No additional connections are required to be made to the module to enable Apple HomeKit functionality. All connections required are internally routed on the module PCB.

Figure 7 illustrates the CYBLE-413124-01 schematic.

Figure 7. CYBLE-413124-01 Schematic Diagram



Critical Components List

Table 4 details the critical components used in the CYBLE-413124-01 module.

Table 4. Critical Component List

Component	Reference Designator	Description
Authentication Co-Processor	U1	Apple Authentication Co-processor
Silicon	U2	40-pin QFN Bluetooth LE Silicon Device - CYW20719
PA/LNA	U3	17-pin QFN - Skyworks RFX2401C
Crystal	Y1	24.000 MHz, 12PF

Antenna Design

The CYBLE-413124-01 is designed to connect the Antenna path to the casing of the end product. There is no integrated antenna design on the CYBLE-413124-01 module.

Bluetooth Baseband Core

The Bluetooth Baseband Core (BBC) implements all of the time-critical functions required for high-performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles host controller interface (HCI) event types, and HCI command types.

The following transmit and receive functions are also implemented in the BBC hardware to increase reliability and security of the TX/RX data before sending over the air:

- Symbol timing recovery, data deframing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), data decryption, and data dewhitening in the receiver.
- Data framing, FEC generation, HEC generation, CRC generation, key generation, data encryption, and data whitening in the transmitter.

Bluetooth Low Energy

The CYBLE-413124-01 supports single-mode Bluetooth LE operation. The CYBLE-413124-01 supports all Bluetooth 4.2 and legacy LE features, with the following benefits:

- LE data packet length extension
- LE secure connections
- Link layer privacy
- Enables Bluetooth Smart sensors to access the Internet directly via IPv6/6LoWPAN

Link Control Layer

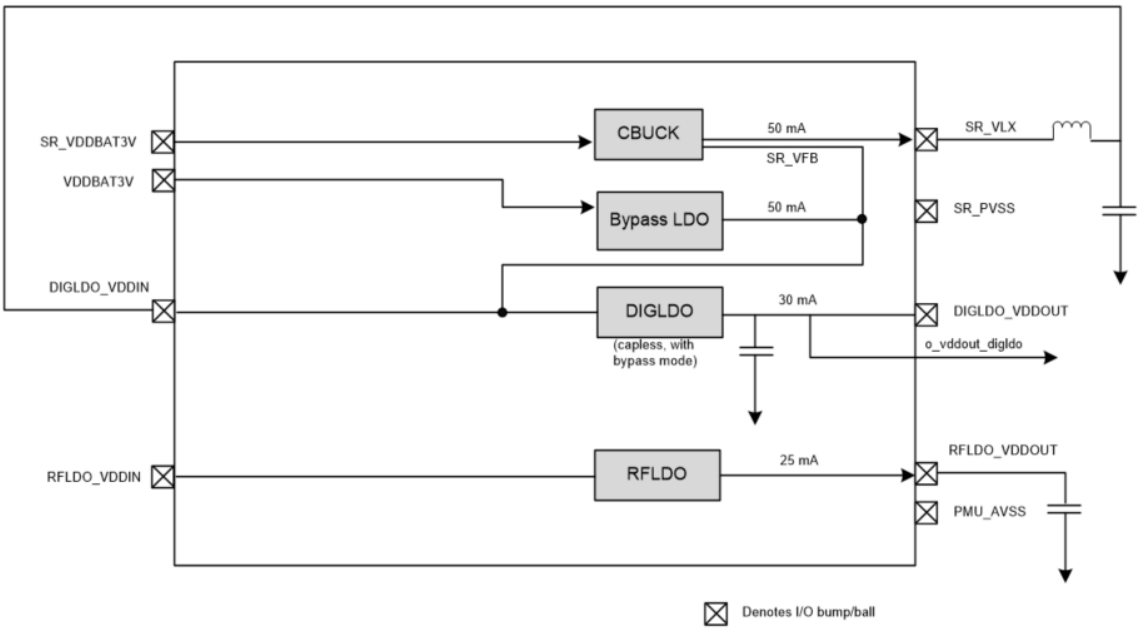
The link control layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the link control unit (LCU). This layer consists of the command controller that takes commands from the software, and other controllers that are activated or configured by the command controller, to perform the link control tasks. Each task performs a different state in the Bluetooth® Link Controller.

- Major states:
  - Standby
  - Connection

Power Management Unit

The Power Management Unit (PMU) provides power management features that can be invoked through power management registers or packet handling in the baseband core. This section contains descriptions of the PMU features.

Figure 8. Power Management Unit of CYW20719



RF Power Management

Figure 8 shows the CYBLE-413124-01 power management unit (PMU) block diagram that is contained in the CYW20719 silicon device. The CYW20719 includes an integrated buck regulator, a bypass LDO, a capless LDO, and an additional 1.2 V LDO for RF.

Host Controller Power Management

Power is automatically managed by the firmware based on input device activity. As a power-saving task, the firmware controls the disabling of the on-chip regulator when in HIDOFF (deep sleep) mode.

BBC Power Management

There are several low-power operations for the BBC:

- Physical layer packet handling turns RF on and off dynamically within packet TX and RX.
- Bluetooth-specified low-power connection mode. While in these low-power connection modes, the CYBLE-413124-01 runs on the Low Power Oscillator and wakes up after a predefined time period.

The CYBLE-413124-01 automatically adjusts its power dissipation based on user activity. It supports the following power modes:

- Active mode
- Idle mode
- Sleep mode (not enabled for the specific application the CYBLE-413124-01 is used in)
- HIDOFF (deep sleep) mode

The CYBLE-413124-01 transitions to the next lower state after a programmable period of user inactivity. When user activity resumes, the CYBLE-413124-01 immediately enters Active mode.

In HIDOFF mode, the CYBLE-413124-01 baseband and core are powered off by disabling power to VDDC_OUT and PAVDD. The VDDO domain remains powered up and will turn the remainder of the chip on when it detects user events. This mode minimizes chip power consumption and is used for extended periods of inactivity.

Microprocessor Unit

The CYBLE-413124-01 microprocessor unit runs software from the link control (LC) layer up to the host controller interface (HCI). The microprocessor is a Cortex®-M4 32-bit RISC processor with embedded ICE-RT debug and serial wire debug (SWD) interface units. The microprocessor also includes 2 MB of ROM memory for program storage and 512 KB of RAM for data scratch-pad.

The internal ROM provides flexibility during power-on reset to enable the same device to be used in various configurations. At power-up, the lower layer protocol stack is executed from the internal ROM.

External patches can be applied to the ROM-based firmware to provide flexibility for bug fixes and features additions. The device also supports the integration of user applications and profiles. Patches and applications can be stored in on-chip flash.

Floating Point Unit

The CYBLE-413124-01 includes the CM4 single precision IEEE-754 compliant floating point unit. For additional details, see the Cortex-M4 manual.

On-Chip Flash

The silicon device used in the CYBLE-413124-01 module includes 1 MB of on-chip flash. This flash can be used for direct program execution or for non-volatile data. Typical usage for the on-chip flash includes:

- Chip configuration
- Patches
- Peer addresses and link keys
- Application code
- Application non-volatile data
- Product information

OTP

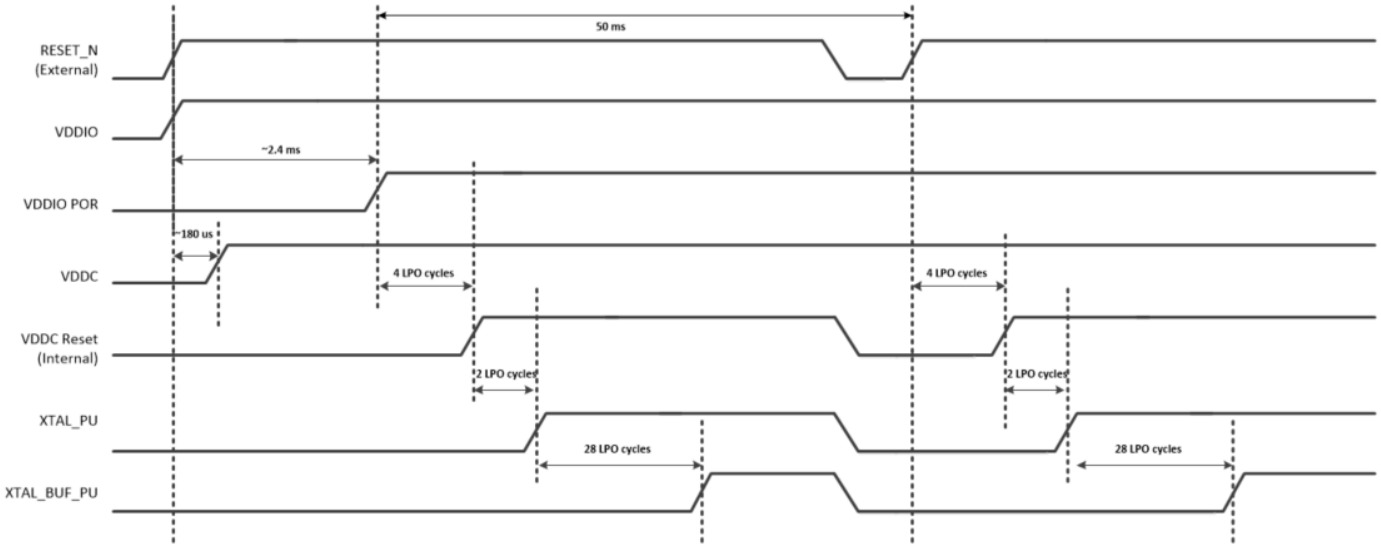
The CYBLE-413124-01 includes 2 KB of one-time programmable (OTP) memory. This memory can be used by the factory to store product specific information.

Note: Use of OTP requires a 3 V supply to be present at all times.

External Reset

An external active-low reset signal, XRES, can be used to put the CYBLE-413124-01 in the reset state. An external voltage detector reset IC with 50 ms delay is needed on the XRES. The XRES should be released only after the VDD supply voltage level has been stabilized for 50 ms.

Figure 9. Reset Timing



Integrated Radio Transceiver

The CYBLE-413124-01 has an integrated radio transceiver that is optimized for 2.4 GHz Bluetooth wireless systems. It has been designed to provide low power, low cost, and robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. It is fully compliant with Bluetooth Radio Specification 3.0 and meets or exceeds the requirements to provide the highest communication link quality of service.

Transmitter Path

The CYBLE-413124-01 features a fully integrated transmitter. The baseband transmit data is GFSK modulated in the 2.4 GHz ISM band.

Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal.

Power Amplifier

The CYBLE-413124-01 has an integrated power amplifier (PA) on the silicon device as well as a high power external power amplifier (PA) integrated on the module. The total output power that this module is designed to achieve is +8 dBm.

Receiver Path

The receiver path uses a low IF scheme to down convert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, and an extended dynamic range to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology, which has built-in out-of-band attenuation, enables the CYBLE-413124-01 to be used in most applications without off-chip filtering.

Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

Receiver Signal Strength Indicator

The radio portion of the CYBLE-413124-01 provides a receiver signal strength indicator (RSSI) to the baseband. This enables the controller to take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

Calibration

The CYBLE-413124-01 radio transceiver features a self-contained automated calibration scheme. No user interaction is required during normal operation or during manufacturing to provide optimal performance. Calibration compensates for filter, matching network, and amplifier gain and phase characteristics to yield radio performance within 2% of what is optimal. Calibration takes process and temperature variations into account, and it takes place transparently during normal operation and hop setting times.

Internal LDO Regulator

The CYBLE-413124-01 has an integrated 1.2 V LDO regulator that provides power to the digital and RF circuits. The 1.2 V LDO regulator operates from a 1.425 V to 3.63 V input supply with a 30 mA maximum load current.

Peripheral Transport Unit

UART Interface

The CYBLE-413124-01 includes a UART interface for factory programming as well as when operating as a BT HCI device in a system with an external host. The UART physical interface is a standard, 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 6 Mbps. During initial boot, UART speeds may be limited to 750 kbps. The baud rate may be selected via a vendor-specific UART HCI command. The CYBLE-413124-01 has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support enhanced data rates. The interface supports the Bluetooth UART HCI (H4) specification. The default baud rate for H4 is 115.2 kbaud.

The UART clock default setting is 24 MHz. The baud rate of the CYBLE-413124-01 UART is controlled by two values. The first is a UART clock divisor (set in the DLBR register) that divides the UART clock by an integer multiple of 16. The second is a baud rate adjustment (set in the DHBR register) that is used to specify a number of UART clock cycles to stuff in the first or second half of each bit time. Up to eight UART cycles can be inserted into the first half of each bit time, and up to eight UART clock cycles can be inserted into the end of each bit time. Table 5 contains example values to generate common baud rates with a 24 MHz UART clock.

Table 5. Common Baud Rate Examples, 24 MHz Clock

Baud Rate (bps)	DHBR	DLBR	Mode	Error (%)
3M	0xFF	0xF8	High rate	0.00
2M	0XFF	0XF4	High rate	0.00
1.5M	0X00	0XFF	Normal	0.00
1M	0x44	0xFF	Normal	0.00
921600	0x55	0xFF	Normal	0.16
460800	0x22	0xFD	Normal	0.16
230400	0x44	0xFA	Normal	0.16
115200	0x00	0xF3	Normal	0.16
38400	0x01	0xD9	Normal	0.00

Table 6 contains example values to generate common baud rates with a 48 MHz UART clock.

Table 6. Common Baud Rate Examples, 48 MHz Clock

Baud Rate (bps)	High Rate	Low Rate	Mode	Error (%)
6M	0xFF	0xF8	High rate	0.00
4M	0xFF	0xF4	High rate	0.00
3M	0x0	0xFF	Normal	0.00
2M	0x44	0xFF	Normal	0.00
1.5M	0x00	0xFE	Normal	0.00
1M	0x00	0xFD	Normal	0.00
921600	0x22	0xFD	Normal	0.16
460800	0x44	0xFA	Normal	0.16
230400	0x0	0xF3	Normal	0.16
115200	0x1	0xE6	Normal	–0.08
57600	0x1	0xCC	Normal	0.04
38400	0x11	0xB2	Normal	0.00
19200	0x22	0x64	Normal	0.00

Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers.

The CYBLE-413124-01 UART operates correctly with the host UART as long as the combined baud rate error of the two devices is within ±5%.

Peripheral UART Interface

The CYBLE-413124-01 has a second UART that may be used to interface to peripherals. This peripheral UART is accessed through the optional I/O ports, which can be configured individually and separately for each functional pin.

ADC Port

The ADC block is a single switched-cap Σ-Δ ADC core for audio and DC measurement. It operates at the 12 MHz clock rate. The internal bandgap reference has ±5% accuracy without calibration. Different calibration and digital correction schemes can be applied to reduce ADC absolute error and improve measurement accuracy in DC mode.

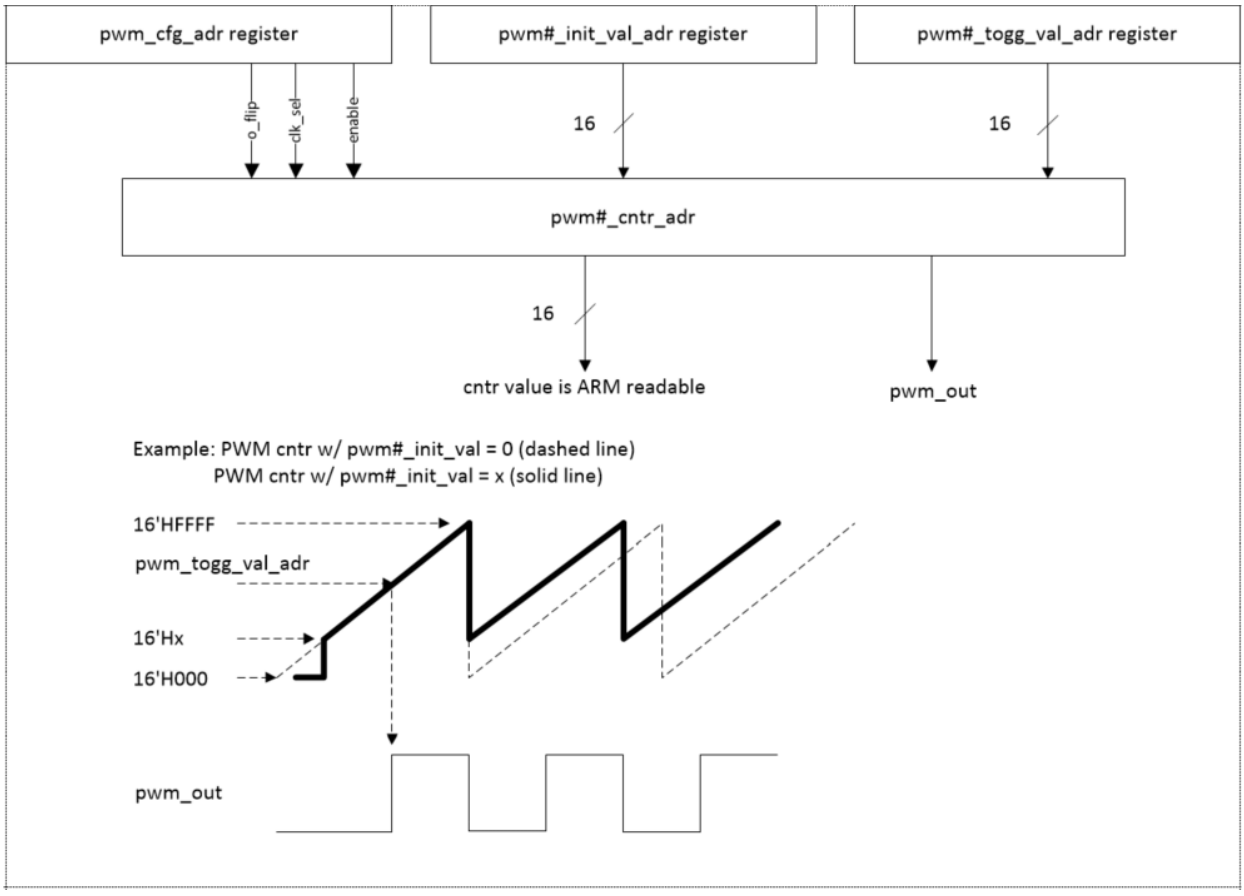
PWM

The CYBLE-413124-01 has five PWMs. The PWM module consists of the following:

- PWM1–5. Each of the five PWM channels contains the following registers:
  - 16-bit initial value register (read/write)
  - 16-bit toggle register (read/write)
  - 16-bit PWM counter value register (read)
- PWM configuration register shared among PWM1–5 (read/write). This 18-bit register is used:
  - To configure each PWM channel
  - To select the clock of each PWM channel
  - To change the phase of each PWM channel

Figure 10 shows the structure of one PWM.

Figure 10. PWM Block Diagram



Triac Control

The CYBLE-413124-01 includes hardware support for zero-crossing detection and trigger control for up to four triacs. The CYBLE-413124-01 detects zero-crossing on the AC zero detection line and uses that to provide a pulse that is offset from the zero crossing. This allows the CYBLE-413124-01 to be used in dimmer applications, as well as any other applications that require a control signal that is offset from an input event.

The zero-crossing hardware includes an option to suppress glitches.

Security Engine

The CYBLE-413124-01 includes a hardware security accelerator which greatly decreases the time required to perform typical security operations. Access to the hardware block is provided via a firmware interface (see firmware documentation for details).Thie security engine includes:

- Public key acceleration (PKA) cryptography
- AES-CTR/CBC-MAC/CCM acceleration
- SHA2 message hash and HMAC acceleration
- RSA encryption and decryption of modulus sizes up to 2048 bits
- Elliptic curve Diffie-Hellman in prime field GF(p)
- Generic modular math functions

Electrical Characteristics

Note: All voltages listed in Table 7 are referenced to VDD.

Table 7. Absolute Maximum Voltages

Requirement Parameter	Specification			Unit
	Minimum	Nominal	Maximum	
Ambient Temperature of Operation	–30	25	105	°C
Storage temperature	–30	–	110	°C
ESD Tolerance HBM (Silicon)	–2000	–	2000	V
ESD Tolerance MM (Silicon)	–100	–	100	V
ESD Tolerance CDM (Silicon)	–500	–	500	V
Latch-up (Silicon)	–	200	–	mA

Table 8 shows the power supply characteristics for the range T_J = 0 °C to 125 °C.

Table 8. Power Supply Specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
VDD Input	Module Input	3.0	3.3	3.6	V
VDD Ripple	Module Input	–	–	300	mV
VBAT Input	Internal to Module (not accessible)	1.62	3.3	3.6	V
PMU turn-on time	VBAT is ready	–	–	300	µs

Core Buck Regulator

Table 9. Core Buck Regulator (Internal to Module)

Parameter	Conditions	Min.	Typ.	Max.	Unit
Input supply voltage DC, VBAT	DC voltage range inclusive of disturbances	2.1	3.3	3.63	V
CBUCK output current	LPOM only	–	–	65	mA
Output over-current limit	Peak inductor current	–	–	–	mA
Output voltage range	Programmable, 30 mV/step default = 1.2 V (bits = 0000)	1.2	1.2	1.5	V
Output voltage DC accuracy	Includes load and line regulation: Before trimming After trimming	 –4 –2	 –	 +4 +2	 % %
LPOM ripple voltage, static	Measured with 20 MHz bandwidth limit, static load. Max ripple based on VBAT = 3 V, Vout = 1.2 V Inductor: 0806 inch-size, Tmax = 1 mm, 2.2 µH ±25%, DCR = 114 mW ±20%, ACR<1W (for frequency <1 MHz) Capacitor: 1 µF ±10%, 6.3 V, 0603 inch, X5R, MLCC capacitor + board total-ESR < 20 mW	–	–	30	mVpp
LPOM efficiency (high load)	10–50 mA load current, Vout = 1.2 V, Vbat = 3 V @ 25 °C Inductor: 0806 inch-size, Tmax = 1 mm, 2.2 µH ±25%, DCR = 114 mW ±20%, ACR < 1W (for frequency < 1 MHz) Capacitor: 1 µF ±10%, 6.3 V, 0603 inch, X5R, MLCC capacitor +board total-ESR < 20 mW	–	85	–	%
LPOM efficiency (low load)	1–5 mA load current, Vout = 1.2 V, Vbat = 3 V @ 25 °C Inductor: 0806 inch-size, Tmax = 1 mm, 2.2 µH ±25%, DCR = 114 mW ±20%, ACR<1W (for frequency<1 MHz) Capacitor: 1 µF ±10%, 6.3 V, 0603 inch, X5R, MLCC capacitor +board total-ESR < 20 mW	–	80	–	%
Startup time	See Table 10 on page 19.	–	–	–	–
External inductor L	2.2 µH ±25%, DCR=114 mW ±20%, ACR<1W (for frequency < 1 MHz)	–	2.2	–	µH
External output capacitor, Cout	1 µF ±10%, 6.3 V, 0603 inch, X5R, MLCC capacitor +board total-ESR < 20 mW	0.7	1	1.1	µF
External input capacitor, Cin	For SR_VDDBAT pin Ceramic, X5R, 0402, ESR < 30 mW at 4 MHz, +/-20%, 6.3V, 4.7 µF	0.7	4.7	5.64	µF
Input supply voltage ramp-up time	0 to 3.3 V	40	–	–	µs

- Minimum capacitor value refers to residual capacitor value after taking into account part-to-part tolerance, DC-bias, temperature, and aging.
- Maximum capacitor value refers to the total capacitance seen at a node where the capacitor is connected. This also includes any decoupling capacitors connected at the load side, if any.

Digital LDO

Table 10. Digital LDO (Internal to Module)

Parameter	Conditions	Min.	Typ.	Max.	Unit
Input supply voltage, Vin	Minimum Vin = Vo + 0.12 V requirement must be met under maximum load.	1.2	1.2	1.6	V
Nominal output voltage, Vo	Internal default bit setting	–	1.1	–	V
Output voltage programmability	Range Step size Accuracy at any step (including line/load regulation) before trimming Accuracy at any step (including line/load regulation) after trimming	0.9 – –4 –2	– 10 – –	1.25 – +4 +2	V mV % %
Dropout voltage	At maximum load	–	–	120	mV
Output current	DC load	0.2[6]	–	40	mA
Output loading capacitor	Internal, including the decoupling capacitor to be placed next to the load and the equivalent loading capacitor by the core.	4	–	10	nF
Quiescent current	At no load, excluding main bandgap Iq	–	90	120	µA
Line regulation	Vin from (Vo+0.12V) to 1.5V; 40 mA load	–	–	5	mV/V
Load regulation	Load from 1 mA to 25 mA; Vin (Vo + 0.12 V)	–	0.025	0.045	mV/mA
Leakage current	In full power-down mode or bypass mode: Junction temperature: 25 °C Junction temperature: 125 °C	 – –	 0.05 1.1	 0.2 5.0	 µA µA
PSRR	@1 kHz, Vin, Vo + 0.12 V Output cap of 4 nF~10 nF	40	–	–	dB
PMU startup time	VBAT is up and steady. Time from HID_OFF falling edge to DIGLDO reaching 99% of Vo.	–	100	–	µs
LDO turn-on time	LDO turn-on time when balance of chip is up	–	–	22	µs
External input capacitor	Only use an external input capacitor at VDD_DIGLDO pin if it is not supplied from CBUCK output.	–	1	2.2	µF

Note

6. By default, an internal loading of ~0.2 mA resides inside the LDO. This is to ensure the LDO is stable with zero loading from the core. After the core is up, digital logic can disable this internal loading by setting i_ldo_cntl<8:7> to 00.

RF LDO

Table 11. RF LDO (Internal to Module)

Parameter	Conditions	Min.	Typ.	Max.	Unit
Input supply voltage, Vin	Min Vin = Vo + 0.15 V = 1.35 V (for Vo = 1.2 V) Dropout voltage requirement must be met under maximum load.	1.2	1.35	1.5	V
Nominal output voltage, Vo	Internal default bit setting 000	–	1.2	–	V
Output voltage programmability	Range Step size Accuracy at any step (including line/load regulation) Accuracy at any step (including line/load regulation) after trimming	1.1 – –4 –2	– 25 – –	1.275 – +4 +2	V mV % %
Dropout voltage	At maximum load	–	–	150	mV
Output current	TBD	0.1	–	25	mA
Quiescent current	No load	–	44	–	µA
Line regulation	Vin from (Vo + 0.15 V) to 1.5 V; 25 mA load	–	–	5.5	mV/V
Load regulation	Load from 1 mA to 25 mA; Vin ≥ (Vo+0.15V)	–	0.025	0.045	mV/mA
Load step error	Load step from 1 mA–25 mA in 1 µs and 25 mA–1 mA in 1µs; Vin(Vo + 0.15 V); Co = 2.2 µF	–	–	35	mV
Leakage current	Power-down junction temperature: 85 °C	–	–	10	µA
Output noise	@30 kHz, 25 mA load, Co = 2.2 µF @100 kHz, 25 mA load, Co = 2.2 µF	–	–	60 35	nV/√Hz nV/√Hz
PSRR	@1kHz, Input > 1.35V, Co = 2.2 µF, Vo = 1.2V	20	–	–	dB
LDO turn-on time	LDO turn-on time when balance of chip is up	–	140	180	µs
In-rush current	Vin = Vo + 0.15 V to 1.5 V, Co = 2.2 µF, no load	–	–	100	mA
External output capacitor, Co	Total ESR (trace/cap): 5 m–240 mW	0.5	2.2	4.7	µF
External input capacitor	Only use an external input capacitor at VDD_DIGLDO pin if it is not supplied from CBUCK output.	–	1	2.2	µF
Minimum capacitor value refers to residual capacitor value after taking into account part-to-part tolerance, DC-bias, temperature, and aging.					

Digital I/O Characteristics

Table 12. Digital I/O Characteristics

Characteristics	Symbol	Minimum	Typical	Maximum	Unit
Input low voltage (VDD = 3.3V)	V_{IL}	–	–	0.8	V
Input high voltage (VDD = 3.3V)	V_{IH}	2.0	–	–	V
Output low voltage	V_{OL}	–	–	0.4	V
Output high voltage	V_{OH}	VDD – 0.4V	–	–	V
Input low current	I_{IL}	–	–	1.0	µA
Input high current	I_{IH}	–	–	1.0	µA
Output low current (VDD = 3.3 V, V_{OL} = 0.4 V)	I_{OL}	–	–	2.0	mA
Output high current (VDD = 3.3 V, V_{OH} = 2.9 V)	I_{OH}	–	–	4.0	mA
Input capacitance	C_{IN}	–	–	0.4	pF

Current Consumption

In Table 13, current consumption measurements are taken at VBAT with the assumption that VBAT is connected to VDDIO and LDOIN. Module current consumption measurements are taken at VDD.

Table 13. Bluetooth LE Current Consumption

Product	Operational Mode	Conditions	Typical	Unit
CYW20719 (Silicon)	Receiving	Receiver and baseband are both operating, 100% ON, silicon only.	5.8	mA
	Transmitting	Transmitter and baseband are both operating, 100% ON, silicon only.	5.7	mA
	PDS	512 KB SRAM memory retention, silicon only.	70	µA
	Deep Sleep	16 KB SRAM memory retention, silicon only.	1	µA
	HIDOFF	Wakeup only from XRES. No SRAM memory retention, silicon only.	350	nA
	Connection, 1-s Avg.	Average Power, 1-second connection interval, silicon only. Deep Sleep mode enabled during non-TX/RX	17	µA
	Connection, 4-s Avg.	Average Power, 4-second connection interval, silicon only. Deep Sleep mode enabled during non-TX/RX	5	µA
CYBLE-413124-01 (Module)	Receiving	Receiver and baseband are both operating, 100% ON, module.	13.3	mA
	Transmitting	Transmitter and baseband are both operating, 100% ON, module.	32.7	mA
	Connection	Average Power, using FW V0.3.6 of actual application	9.0	mA
	Advertising	Average Power, using FW V0.3.6 of actual application	11.0	mA

RF Specifications

Note: Table 14 and Table 15 apply to single-ended industrial temperatures. Unused inputs are left open.

Table 14. Receiver RF Specifications

Parameter	Mode and Conditions	Min	Typ	Max	Unit
Receiver Section					
Frequency range	–	2402	–	2480	MHz
RX sensitivity	GFSK, BDR GFSK 0.1% BER, 1 Mbps Module	–	–93.0	–	dBm
Maximum input	–	–20	–	–	dBm

Table 15. Transmitter RF Specifications

Parameter	Min	Typ	Max	Unit
Transmitter Section				
Frequency range	2402	–	2480	MHz
Class 2: GFSK Tx power (silicon)	–	4	–	dBm
Class 2: GFSK Tx power (module)	–	8	–	dBm
20 dB bandwidth	–	930	1000	kHz
Frequency Drift				
DH1 packet	–25	–	+25	kHz
DH3 packet	–40	–	+40	kHz
DH5 packet	–40	–	+40	kHz
Drift rate	–20	–	20	kHz/50 µs
Frequency Deviation				
Average deviation in payload (sequence used is 00001111)	140	–	175	kHz
Maximum deviation in payload (sequence used is 10101010)	115	–	–	kHz
Channel spacing	–	1	–	MHz

Table 16. Bluetooth LE RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Frequency range	N/A	2402	–	2480	MHz
Rx sensitivity[7]	GFSK, BDR GFSK 0.1% BER 0.1% BER, 1 Mbps	–	–93.0	–	dBm
Tx power	N/A	–	4	–	dBm
Mod Char: Delta F1 average	N/A	225	255	275	kHz
Mod Char: Delta F2 max[8]	N/A	99.9	–	–	%
Mod Char: Ratio	N/A	0.8	0.95	–	%

Notes
7. Dirty Tx is Off.
8. At least 99.9% of all delta F2 max frequency values recorded over 10 packets must be greater than 185 kHz.

Timing and AC Characteristics

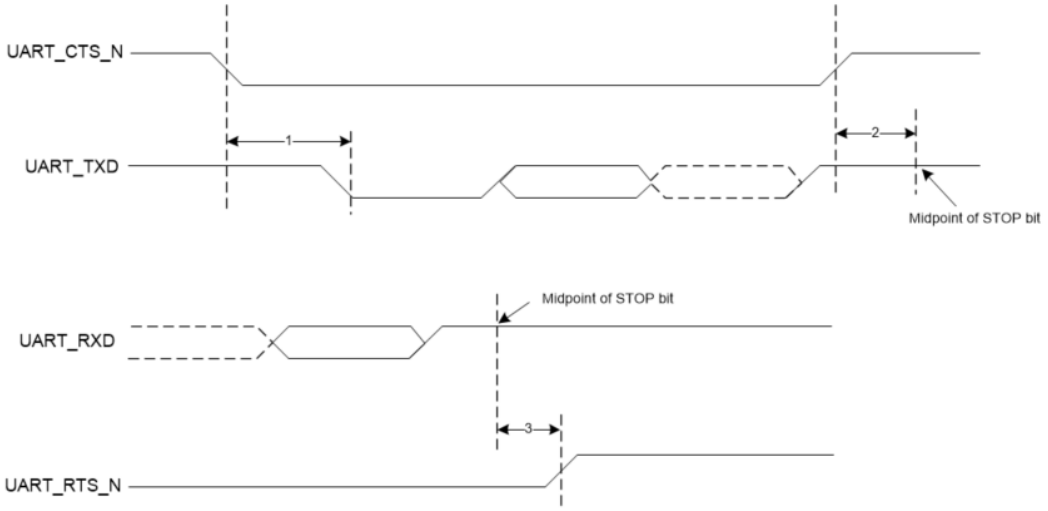
In this section, use the numbers listed in the **Reference** column of each table to interpret the following timing diagrams.

UART Timing

Table 17. UART Timing Specifications

Reference	Characteristics	Min.	Typ.	Max.	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid.	–	–	1.50	Bit periods
2	Setup time, UART_CTS_N high before midpoint of stop bit.	–	–	0.67	Bit periods
3	Delay time, midpoint of stop bit to UART_RTS_N high.	–	–	1.33	Bit periods

Figure 11. UART Timing



Environmental Specifications

Environmental Compliance

This Cypress Bluetooth LE module is produced in compliance with the Restriction of Hazardous Substances (RoHS), Halogen-Free (HF), and REACH directives. The Cypress module and components used to produce this module are RoHS, HF, and REACH compliant.

RF Certification

The CYBLE-413124-01 module does not contain any modular certifications for regulatory compliance. Testing on the end product must be performed to obtain regulatory approvals.

Safety Certification

The CYBLE-413124-01 module complies with the following safety regulations:

- Underwriters Laboratories, Inc. (UL): Filing E331901
- CSA
- TUV

Environmental Conditions

Table 18 describes the operating and storage conditions for the Cypress Bluetooth LE module.

Table 18. Environmental Conditions for CYBLE-413124-01

Description	Minimum Specification	Maximum Specification
Operating temperature	–30 °C	105 °C
Operating humidity (relative, non-condensation)	5%	85%
Thermal ramp rate	–	10 °C/minute
Storage temperature	–40 °C	110 °C
Storage temperature and humidity	–	110 °C at 85%
ESD: Module integrated into system Components[9]	–	15 kV Air 2.0 kV Contact

ESD and EMI Protection

Exposed components require special attention to ESD and electromagnetic interference (EMI).

A grounded conductive layer inside the device enclosure is suggested for EMI and ESD performance. Any openings in the enclosure near the module should be surrounded by a grounded conductive layer to provide ESD protection and a low-impedance path to ground.

Device Handling: Proper ESD protocol must be followed in manufacturing to ensure component reliability.

Note
9. This does not apply to the RF pins (ANT).

Packaging

Table 19. Solder Reflow Peak Temperature

Module Part Number	Package	Maximum Peak Temperature	Maximum Time at Peak Temperature	No. of Cycles
CYBLE-413124-01	14-pad SMT	260 °C	30 seconds	2

Table 20. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Module Part Number	Package	MSL
CYBLE-413124-01	14-pad SMT	MSL 3

The CYBLE-413124-01 is offered in tape and reel packaging. Figure 12 details the tape dimensions used for the CYBLE-413124-01.

Figure 12. CYBLE-413124-01 Tape Dimensions

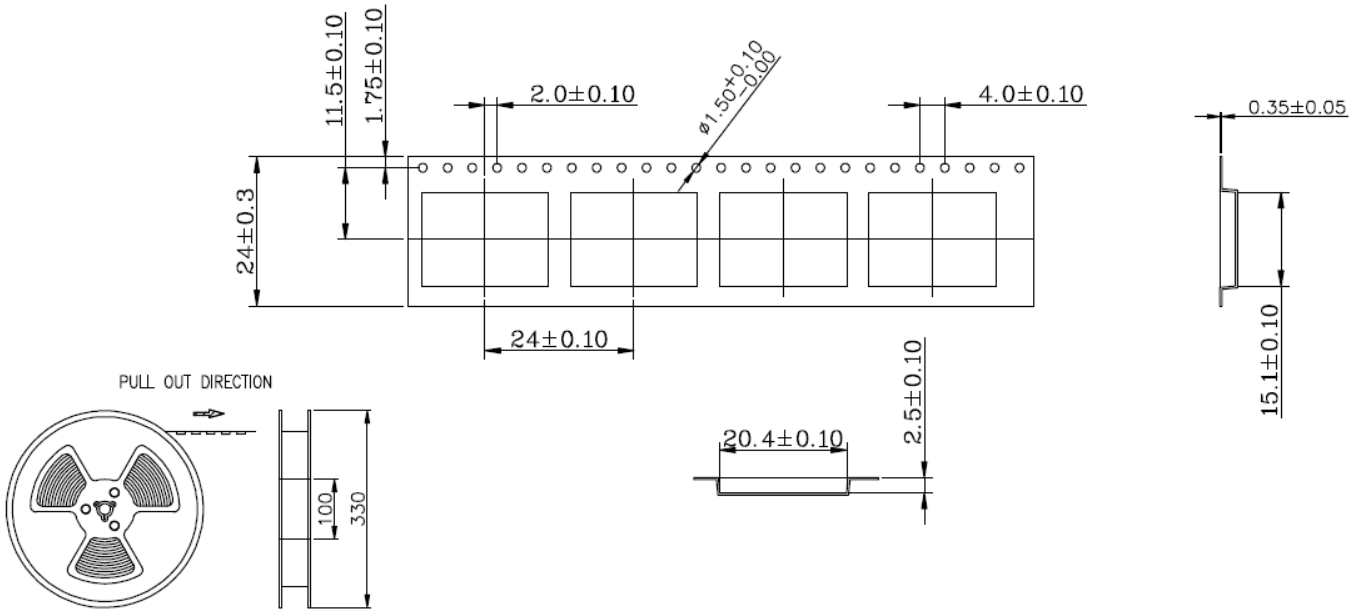


Figure 13 details the orientation of the CYBLE-413124-01 in the tape as well as the direction for unreeling.

Figure 13. Component Orientation in Tape and Unreeling Direction

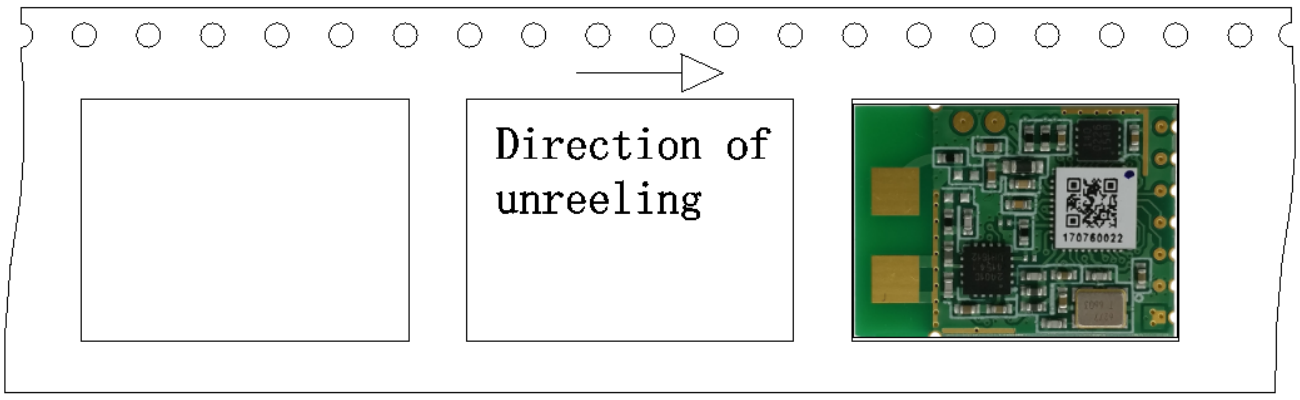
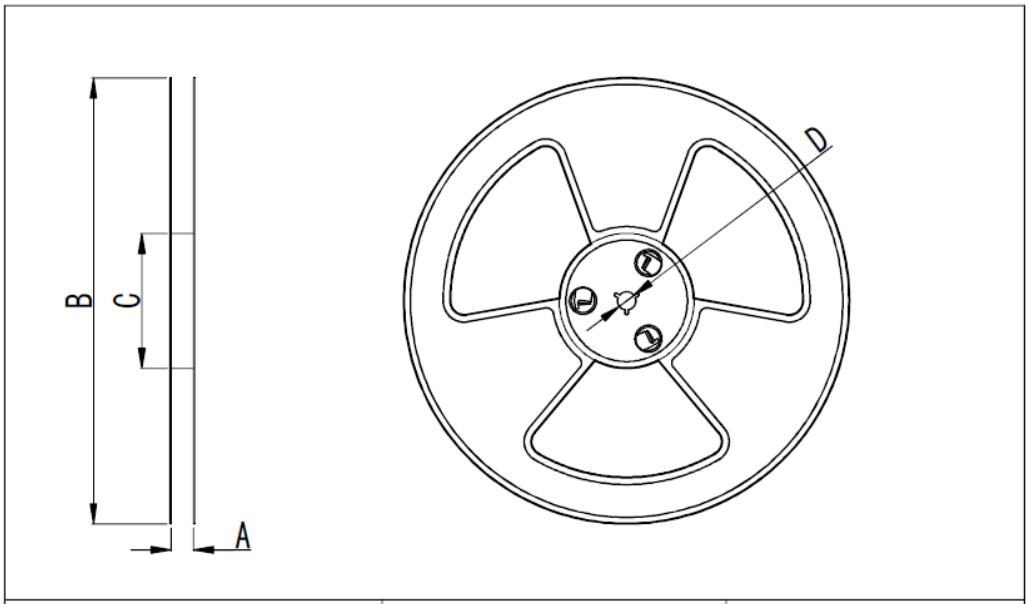


Figure 14 details reel dimensions used for the CYBLE-413124-01.

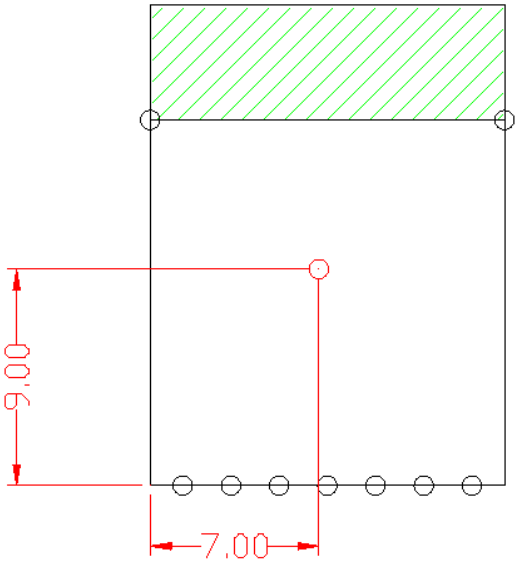
Figure 14. Reel Dimensions



Index	NOTE	Dimension	Tolerance	
A	Inside Width	24.5	+0.50mm	-0.50mm
B	Reel Diameter	330.00	+1.5mm	-1.5mm
C	Outer Axis Diameter	100.00	+1.5mm	-1.5mm
D	Inner Axis Diameter	13.00	+0.50mm	-0.50mm

The CYBLE-413124-01 is designed to be used with pick-and-place equipment in an SMT manufacturing environment. The center-of-mass for the CYBLE-413124-01 is detailed in Figure 15.

Figure 15. CYBLE-413124-01 Center of Mass



Ordering Information

Table 21 lists the CYBLE-413124-01 part number and features. Table 22 lists the reel shipment quantities for the CYBLE-413124-01.

Table 21. Ordering Information

Ordering Part Number	Base Part Number (Marking)	CPU Speed (MHz)	Flash Size (KB)	RAM Size (KB)	UART	PWM	Apple MFi Coprocessor	Package	Packaging	Program
CYBLE-413124-01	CYBLE-413124-01	24	1024	512	Yes	5	Yes	14-SMT	Tape and Reel	A19C
CP9093AT	CYBLE-413124-01	24	1024	512	Yes	5	Yes	14-SMT	Tape and Reel	A19C (Mesh)

Table 22. Tape and Reel Package Quantity and Minimum Order Amount

Description	Minimum Reel Quantity	Maximum Reel Quantity	Comments
Reel Quantity	800	800	Ships in 800 unit reel quantities.
Minimum Order Quantity (MOQ)	800	–	–
Order Increment (OI)	800	–	–

The CYBLE-413124-01 is offered in tape and reel packaging. The CYBLE-413124-01 ships in a reel size of 800.

For additional information and a complete list of Cypress Semiconductor Bluetooth LE products, contact your local Cypress sales representative. To locate the nearest Cypress office, visit our website.

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Acronyms

Table 23. Acronyms Used in this Document

Acronym	Description
BLE	Bluetooth Low Energy
Bluetooth SIG	Bluetooth Special Interest Group
CE	European Conformity
CSA	Canadian Standards Association
EMI	electromagnetic interference
ESD	electrostatic discharge
FCC	Federal Communications Commission
GPIO	general-purpose input/output
IC	Industry Canada
IDE	integrated design environment
KC	Korea Certification
MIC	Ministry of Internal Affairs and Communications (Japan)
PCB	printed circuit board
RX	receive
QDID	qualification design ID
SMT	surface-mount technology; a method for producing electronic circuitry in which the components are placed directly onto the surface of PCBs
TCPWM	timer, counter, pulse width modulator (PWM)
TUV	Germany: Technischer Überwachungs-Verein (Technical Inspection Association)
TX	transmit

Document Conventions

Units of Measure

Table 24. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
dB	decibel
dBm	decibel-milliwatts
kV	kilovolt
mA	milliamperes
mm	millimeters
mV	millivolt
µA	microamperes
µm	micrometers
MHz	megahertz
GHz	gigahertz
V	volt

Document History Page

Document Title: CYBLE-413124-01, EZ-BLE™ Module with HomeKit Document Number: 002-18777			
Revision	**ECN**	**Submission Date**	**Description of Change**
**	5796178	07/06/2017	Datasheet for CYBLE-413124-01 module.
*A	6613342	07/04/2019	Updated Ordering Information: Updated part numbers. Updated to new template. Completing Sunset Review.
*B	7045570	12/15/2020	Changed from Bluetooth Low Energy (BLE) to Bluetooth Low Energy and BLE to Bluetooth LE throughout the document.

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