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The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content
The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers
Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

CY96800 Series

ASSP DC/BLDC Motor controller for 12V-Battery Datasheet

CY96800 series is DC and BLDC* Motor controller corresponding to 12V-Battery. This series incorporates an built-in voltage regulator operable at 12Vcar battery voltages and including 12V and 5V power supplies, a three-phase motor pre-driver, a charge pump, and 16-bit CPU based on Cypress's advanced F2MC-16FX architecture (16-bit with instruction pipeline for RISC-like performance)

The CPU uses the same instruction set as the established F2MC-16LX family thus allowing for easy migration of F2MC-16LX software to the new F2MC-16FX products.

*:Brushless DC electric motor.

Features

Technology

- LDMOS + 0.18µm CMOS

CPU

- F²MC-16FX CPU
- Optimized instruction set for controller applications (bit, byte, word and long-word data types, 23 different addressing modes, barrel shift, a variety of pointers)
- 8-byte instruction queue
- Signed multiply (16-bit × 16-bit) and divide (32-bit/16-bit) instructions available

System Clock

- On-chip PLL clock multiplier (×1 to ×10, ×1 when PLL stop)
- 4MHz to 8MHz crystal oscillator (maximum frequency when using ceramic resonator depends on Q-factor)
- Up to 8MHz external clock for devices with fast clock input feature
- 100kHz/2MHz internal RC clock for quick and safe startup, clock stop detection function, watchdog
- Clock source selectable from main clock and internal RC clock, independently for CPU and 2 clock domains of peripherals
- 10 operating modes (different Run, Sleep, Timer, Stop modes)
- Internal CPU clock and internal peripheral clock operate up to 20MHz.

Built-in voltage regulator

Built-in voltage regulator supports inner circuits operating at low voltages, offering low power consumption

Output Voltage of Power Supply for External Parts

- Voltage regulator for the external can supply the output voltage of 5V (max 25mA) to external parts
- Power supply input voltage (BV_{CC}) can be supplied to external parts via built-in switch (max 30mA)

Low Voltage Detection Function

Reset is generated when supply voltage falls below programmable reference voltage

Code Security

Protects Flash Memory content from unintended read-out

DMA

Automatic transfer function independent of CPU, can be assigned freely to resources

Interrupts

- Fast Interrupt processing
- 8 programmable priority levels
- Non-Maskable Interrupt (NMI)

CAN

- Supports CAN protocol version 2.0 part A and B
- ISO16845 certified
- Bit rates up to 1Mbps
- 32 message objects
- Each message object has its own identifier mask
- Programmable FIFO mode (concatenation of message objects)
- Maskable interrupt
- Disabled Automatic Retransmission mode for Time Triggered CAN applications

- Programmable loop-back mode for self-test operation

USART

- Full duplex USARTs (SCI/LIN)
- Wide range of baud rate settings using a dedicated reload timer
- Special synchronous options for adapting to different synchronous serial protocols
- LIN functionality working either as master or slave LIN device
- Extended support for LIN-Protocol to reduce interrupt load

A/D Converter

- SAR-type
- 10-bit resolution
- Signals an interrupt on conversion end, single conversion mode, repeat conversion mode, activation by software, external trigger, reload timers, and multifunctional timers
- Range Comparator Function

Source Clock Timers

Two independent clock timers (23-bit RC clock timer, 23-bit Main clock timer)

Hardware Watchdog Timer

- Hardware watchdog timer is activated after reset
- Window function of Watchdog Timer is used to select the lower window limit of the watchdog interval

Reload Timers

- 16-bit wide
- Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency
- Event count function

Free-Running Timers

- 16-bit wide
- Signals an interrupt on overflow, supports timer clear upon match with Output Compare(0, 4)
- Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$, $1/2^8$ of peripheral clock frequency

Input Capture Units

- 16-bit wide
- Signals an interrupt on external event
- Rising edge, Falling edge or Both (rising & falling) edges sensitive

Output Compare Units

- 16-bit wide
- Signals an interrupt when a match with Free-Running Timer occurs
- A pair of compare registers can be used to generate an output signal

External Interrupts

- Edge or Level sensitive
- Interrupt mask bit per channel
- Each available CAN channel RX has an external interrupt for wake-up
- Selected USART channels SIN have an external interrupt for wake-up

Non-Maskable Interrupt

- Disable after resetting and enabled by Boot-ROM depending on ROM configuration block
- Once enabled, cannot be disabled other than by reset
- High or Low level sensitive
- Pin shared with external interrupt 0

I/O Ports

- All 5V I/O ports to enable push-pull outputs
- Bit-wise programmable as input/output or peripheral signal
- Bit-wise programmable input enable
- One input level per pin (either Automotive or CMOS hysteresis)
- Bit-wise programmable pull-up resistor (5V I/O port)
- Bit-wise programmable pull-down resistor (12V input port)

Built-in On-Chip Debugger (OCD)

- One-wire debug tool interface
- Break function:
  - Hardware break: 6 points (shared with code event)
  - Software break: 4096 points
- Event function
  - Code event: 6 points (shared with hardware break)
  - Data event: 6 points
  - Event sequencer: 2 levels + reset
- Execution time measurement function
- Trace function: 42 branches
- Security function

Flash Memory

- Dual operation Flash allowing reading of one Flash bank while programming or erasing the other bank
- Command sequencer for automatic execution of programming algorithm and for supporting DMA for programming of the Flash Memory
- Supports automatic programming, Embedded Algorithm
- Write/Erase/Erase-Suspend/Resume commands
- A flag indicating completion of the automatic algorithm
- Erase can be performed on each sector individually
- Sector protection
- Flash Security feature to protect the content of the Flash

Multifunctional Timer

- Supplies PWM driving signals to three-phase motor pre-driver
- Controls three-phase motor by the following configuration:
  - 5 channel 16-bit free-running timer
  - 6 channel 16-bit output compare
  - 4 channel 16-bit input capture
  - 3 channel 16-bit PPG
  - 6 channel waveform generator

Three-Phase Motor Pre-Driver

- Drives power NMOS-FETs to drive motors
- Supports H-Bridge

Charge Pump

- Built in charge pump driver for booster power supply
- Supplies high voltages to drive the High-side Power NMOS FET.

Motor Monitor

- Motor voltages detection function
- Can divide the voltage of the power step (High/Low side switch, bridge circuit) by 6, and put it into the A/D converter

Over-Temperature Detector

- Executes a reset when the junction temperature (Tj) of the device reaches a set temperature.

Temperature Sensor

- Can measure the junction temperature of the device (Tj).
- By using Range comparator function of A/D C, can generate an interrupt when the junction temperature (Tj) exceeds the set temperature for user to detect.

VB Monitor (VBMON)

- Battery voltage monitor functional
- Can be connected to the battery (voltage: VB) via an external series resistance.
- Can divide the input voltage by 6 with a built-in resistor, and put it into the A/D converter.

LIN Transceiver

- Built-in LIN Transceiver(only CY96F8E5K)
- Supports LIN physical layer2.1.

Contents

1. Product Lineup

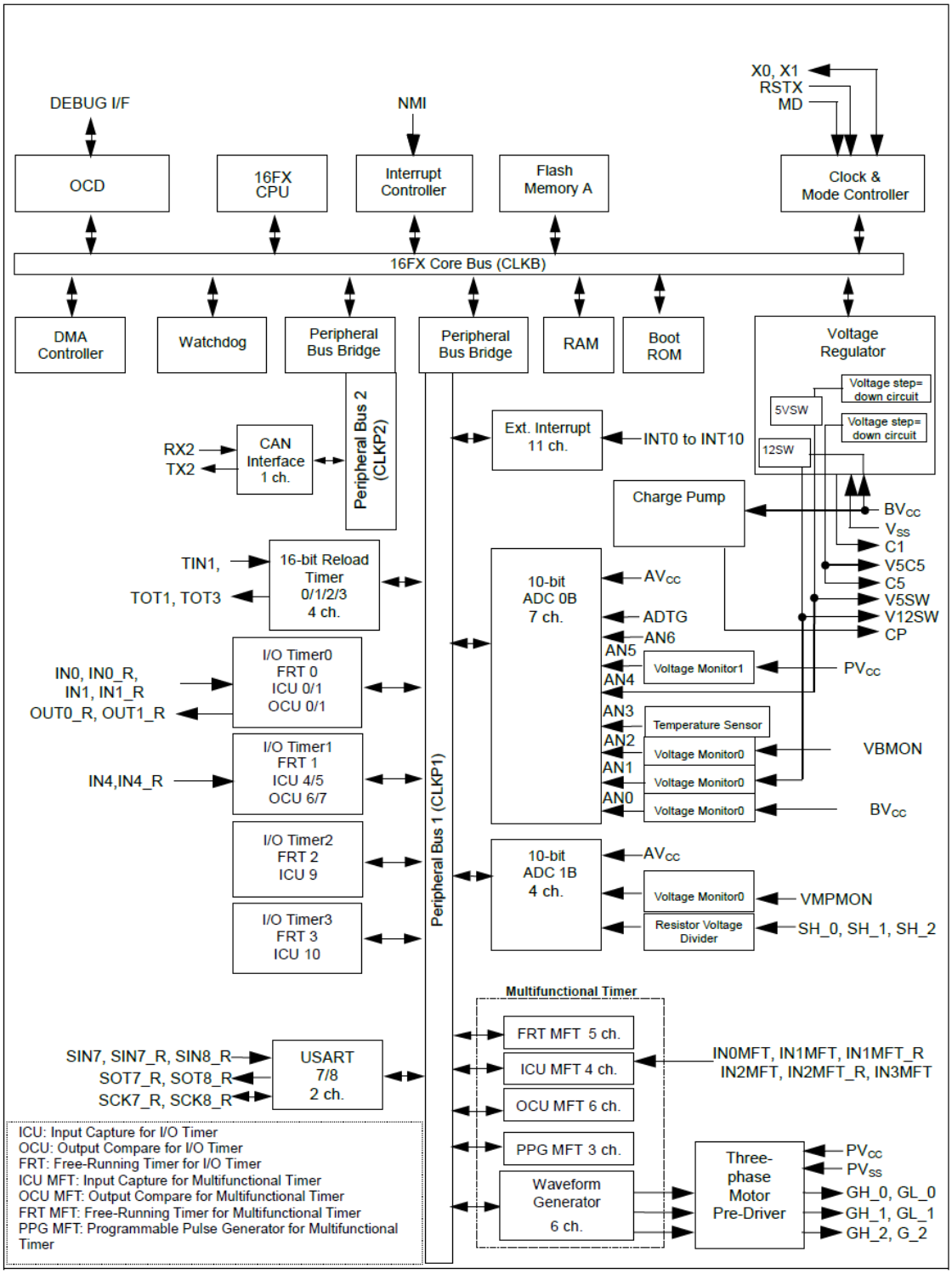
Features		CY96F8D0	CY96F8E0	Remarks
Product Type		Flash Memory Product	Flash Memory Product	-
Sub clock		No	No	-
Dual Operation Flash Memory	RAM	-	-	-
128.5KB + 8KB	8KB	CY96F8D5K3	CY96F8E5K3	-
128.5KB + 32KB	8KB	CY96F8D5KU	CY96F8E5KU	-
Package		TEQFP-48 LEC048	TEQFP-48 LEC048	-
DMA		2ch.	2ch.	-
USART		2ch.	3ch. (LIN-USART 2 only for LIN transceiver)	LIN-USART 2/7/8 LIN-USART 2 built in only CY96F8E0
with automatic LIN-Header transmission/reception		No	Yes(1ch.)	LIN-USART 2
with 16 byte RX- and TX-FIFO		No	No	-
LIN transceiver		No	Yes	-
10-bit A/D Converter 0B		7ch. (shared by internal 6ch.)	7ch. (shared by internal 6ch.)	AN 0 to 6
with Range Comparator		Yes	Yes	-
10-bit A/D Converter 1B		4ch. (dedicated for Multifunctional timer)	4ch. (dedicated for Multifunctional timer)	AN 8 to 11
with Range Comparator		Yes	Yes	--
16-bit Reload Timer (RLT)		4ch. (2 channels for Multifunctional timer)	4ch. (2 channels for Multifunctional timer)	RLT 0 to 3
16-bit Free-Running Timer (FRT)		4ch.	4ch.	FRT 0 to 3 FRT 0 to 3 does not have external clock input pin
16-bit Input Capture Unit (ICU)		6ch. (2 channels for LIN-USART)	7ch. (3 channels for LIN-USART)	ICU 0/1/4/5/6/9/10 ICU 6/9/10 for LIN-USART ICU6 built in only CY96F8E0
16-bit Output Compare Unit (OCU)		4ch.	5ch.	OCU 0/1/4/6/7 OUC4 built in only CY96F8E0

Features		CY96F8D0	CY96F8E0	Remarks
Multifunctional Timer				
	16-bit Free-Running Timer	5ch.	5ch.	FRT 0MFT-4MFT No external clock input pin
	16-bit Input Capture Unit	4ch.	4ch.	ICU 0MFT-3MFT
	16-bit Output Compare Unit	6ch.	6ch.	OCU 0MFT-5MFT
	16-bit Programmable Pulse Generator (PPG)	3ch.	3ch.	PPG 0MFT/2MFT/4MFT
	Waveform Generator (WFG)	6ch.	6ch.	-
Three-Phase Motor Pre-Driver				
	High Side FET Driver	3ch.	3ch.	-
	Low Side FET Driver	3ch.	3ch.	-
	Charge Pump	Yes	Yes	-
CAN Interface		1ch.	1ch.	CAN 2 32 Message Buffers
Motor Monitor		3ch.	3ch.	-
Over-Temperature Detector		Yes	Yes	-
Temperature Sensor		1ch.	1ch.	-
External Interrupts (INT)		11ch.	12ch. (INT 11 connects to LIN inside)	INT 0 to 11 INT 11 built in only CY96F8E0
Non-Maskable Interrupt (NMI)		1ch.	1ch.	-
Real Time Clock (RTC)		No	No	-
I/O Ports		16	16	-
	5/12V Inputs	7	7	-
	5V Input/Output	9	9	-
Clock Calibration Unit (CAL)		1ch.	1ch.	-
Low Voltage Detection Function		Yes	Yes	Low voltage detection function can be disabled by software
Hardware Watchdog Timer		Yes	Yes	-
Built-in RC-oscillator		Yes	Yes	-
On-chip Debugger		Yes	Yes	-
Parallel Flash programing mode		No	No	-

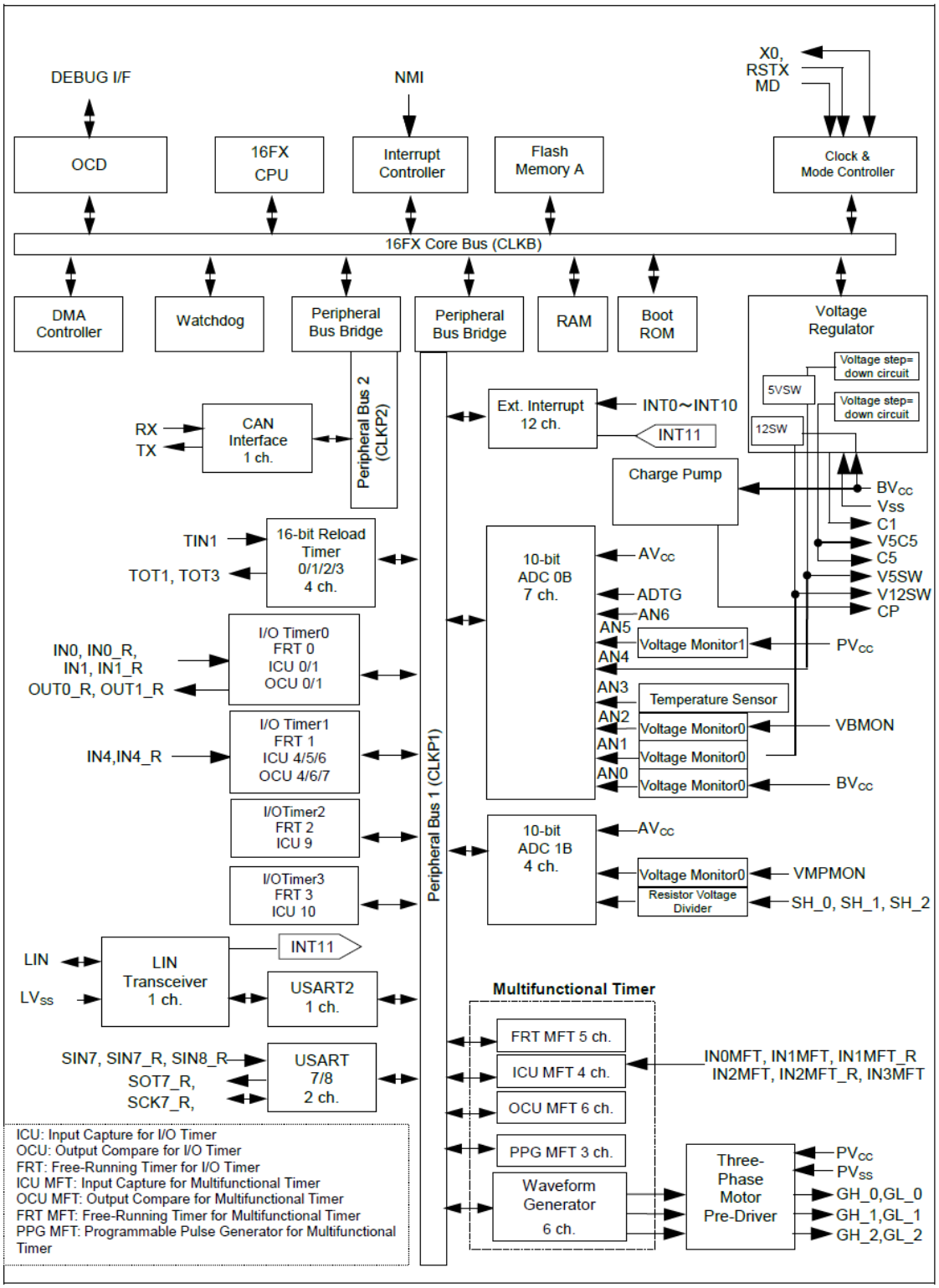
Note: All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the general I/O port according to your function use.

2. Block Diagram

CY96F8D0



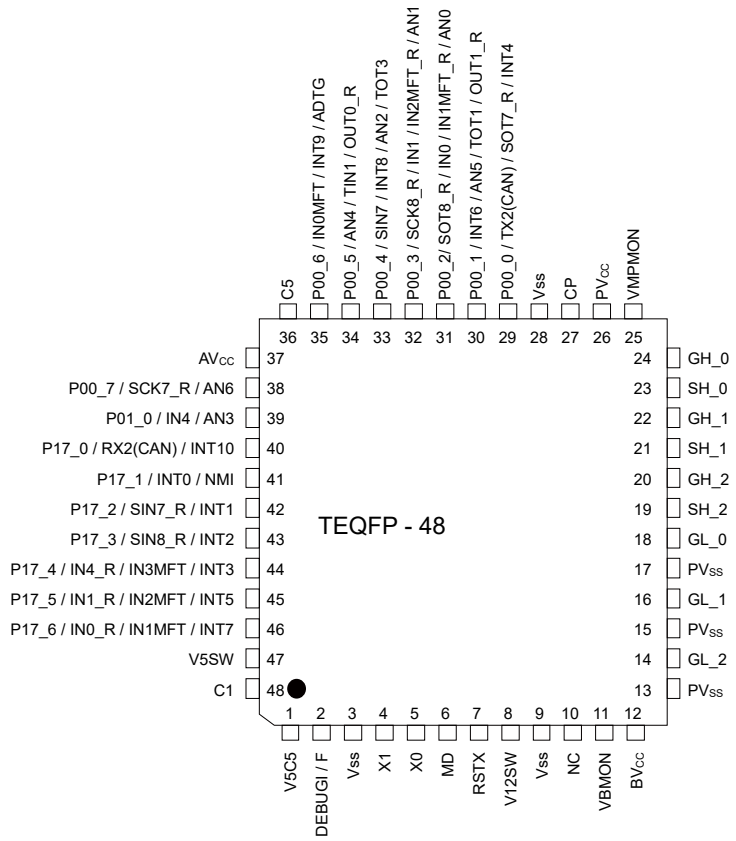
CY96F8E0


DEBUG I/F
NMI
X0, RSTX MD
OCD
16FX CPU
Interrupt Controller
Flash Memory A
Clock & Mode Controller
16FX Core Bus (CLKB)
DMA Controller
Watchdog
Peripheral Bus Bridge
Peripheral Bus Bridge
RAM
Boot ROM
Voltage Regulator
Voltage step= down circuit
5VSW
Voltage step= down circuit
12SW
Peripheral Bus 2 (CLKP2)
RX
TX
CAN Interface 1 ch.
Ext. Interrupt 12 ch.
INT0~INT10
INT11
Charge Pump
BVcc
Vss
C1
V5C5
C5
V5SW
V12SW
CP
TIN1
TOT1, TOT3
16-bit Reload Timer 0/1/2/3 4 ch.
10-bit ADC 0B 7 ch.
AVcc
ADTG
AN6
AN5
AN4
Voltage Monitor1
PVcc
IN0, IN0_R, IN1, IN1_R OUT0_R, OUT1_R
I/O Timer0 FRT 0 ICU 0/1 OCU 0/1
AN3
Temperature Sensor
AN2
Voltage Monitor0
VBMON
IN4,IN4_R
I/O Timer1 FRT 1 ICU 4/5/6 OCU 4/6/7
AN1
Voltage Monitor0
AN0
Voltage Monitor0
BVcc
I/OTimer2 FRT 2 ICU 9
10-bit ADC 1B 4 ch.
AVcc
Voltage Monitor0
VMPMON
I/OTimer3 FRT 3 ICU 10
Resistor Voltage Divider
SH_0, SH_1, SH_2
Peripheral Bus 1 (CLKP1)
LIN
LVss
LIN Transceiver 1 ch.
INT11
USART2 1 ch.
Multifunctional Timer
FRT MFT 5 ch.
ICU MFT 4 ch.
OCU MFT 6 ch.
PPG MFT 3 ch.
Waveform Generator 6 ch.
IN0MFT, IN1MFT, IN1MFT_R IN2MFT, IN2MFT_R, IN3MFT
Three-Phase Motor Pre-Driver
PVcc
PVss
GH_0,GL_0
GH_1,GL_1
GH_2,GL_2
SIN7, SIN7_R, SIN8_R
SOT7_R,
SCK7_R,
USART 7/8 2 ch.
ICU: Input Capture for I/O Timer
OCU: Output Compare for I/O Timer
FRT: Free-Running Timer for I/O Timer
ICU MFT: Input Capture for Multifunctional Timer
OCU MFT: Output Compare for Multifunctional Timer
FRT MFT: Free-Running Timer for Multifunctional Timer
PPG MFT: Programmable Pulse Generator for Multifunctional Timer

3. Pin Assignment

CY96F8D0

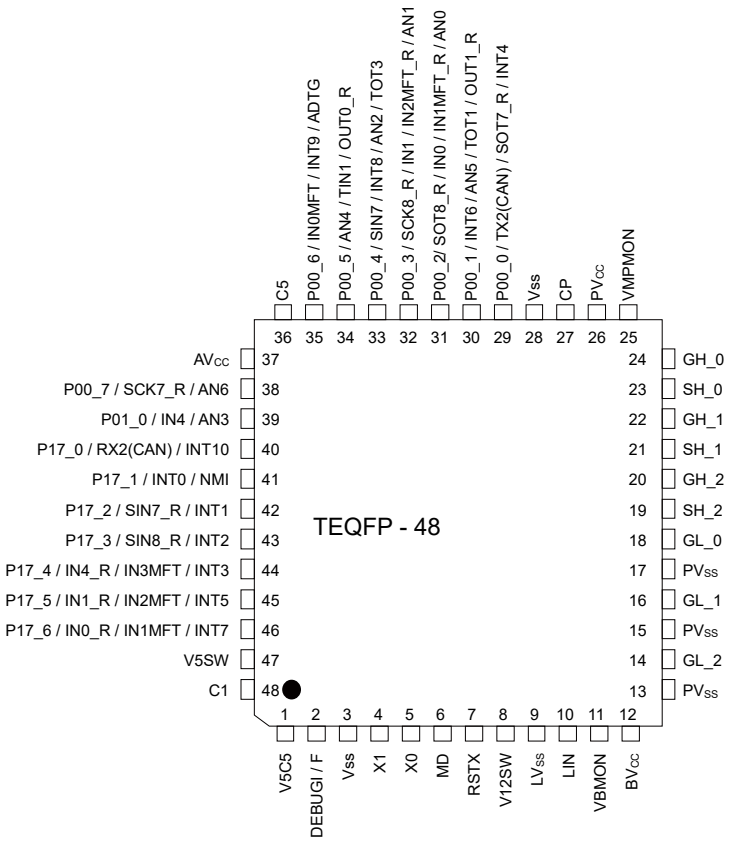
(TOP VIEW)



(LEC048)

CY96F8E0

(TOP VIEW)



(LEC048)

4. Pin Description

Pin Name	Feature	Description
ADTG	ADC	A/D converter trigger input pin
ANn	ADC	A/D converter channel n input pin
AV_{CC}	Supply	Analog circuits power supply pin
BV_{CC}	Supply	Power supply pin
C1	Voltage regulator	Core logic power supply stabilization capacitor pin
C5	Voltage regulator	Internal 5V regulated power supply stabilization capacitor pin
CP	Charge Pump for booster power supply	Output pin of Charge Pump for booster power supply
DEBUG I/F	OCD	On-Chip Debugger input/output pin
GH_n	Motor Pre-Driver	High side Nch driver n output pin
GL_n	Motor Pre-Driver	Low side Nch driver n output pin
INn	ICU	Input Capture Unit n input pin
INn_R	ICU	Relocated Input Capture Unit n input pin
INnMFT	ICU	Input pin for Input Capture Unit n for Multifunctional Timer
INnMFT_R	ICU	Relocated Input pin for Input Capture Unit n for Multifunctional Timer
INTn	External Interrupt	External Interrupt n input pin
LIN	LIN	LIN Transceiver input/output pin [*2]
LV_{SS}	Supply	Power supply pin for LIN Transceiver [*2]
MD	Core	Input pin for specifying the operating mode
NMI	External Interrupt	Non-Maskable Interrupt input pin
VMPMON	Voltage Monitor	Motor power supply monitor input pin
OUTn_R	OCU	Relocated Output Compare Unit n waveform output pin
Pnn_m	GPIO	General-purpose I/O pin
PV_{CC}	Supply	Power supply pin for three-phase motor pre-driver
PV_{SS}	Supply	Power supply pin for three-phase motor pre-driver
RSTX	Core	Reset input pin
RXn [*1]	CAN	CAN interface n RX input pin
SCKn	USART	USART n serial clock input/output pin
SCKn_R	USART	Relocated USART n serial clock input/output pin
SH_n	Resistor voltage divider	Motor Monitor n input pin
SINn	USART	USART n serial data input pin
SINn_R [*1]	USART	Relocated USART n serial data input pin
SOTn	USART	USART n serial data output pin
SOTn_R	USART	Relocated USART n serial data output pin
TINn	Reload Timer	Reload Timer n event input pin
TOTn	Reload Timer	Reload Timer n output pin
TXn	CAN	CAN interface n TX output pin
V5C5	Voltage regulator	Internal 5V regulated power supply stabilization capacitor pin. And output pin for supplying 5V to the external
V5SW	Voltage regulator	Output pin for supplying 5V to the external with ON/OFF control
V12SW	Voltage regulator	Output pin for supplying 12V to the external with ON/OFF control

Pin Name	Feature	Description
VBMON	VB Monitor	Battery voltage monitor input pin
V_{SS}	Supply	Power supply pin
X0	Clock	Oscillator input pin
X1	Clock	Oscillator output pin

*1: SINn_R pin functions only with CMOS hysteresis input (5V) in I/O circuit type: HB. Setting for normal input (12V) is prohibited.
*2: Only CY96F8E0

5. Pin Circuit Type

CY96F8D0

Pin No.	I/O Circuit Type*1	Pin Name
1	Z	V5C5
2	O	DEBUG I/F
3	Supply	VSS
4	A	X1
5	A	X0
6	C	MD
7	C	RSTX
8	HS	V12SW
9	Supply	VSS
10	—	NC
11	HM	VBMON
12	Supply	BVCC
13	Supply	PVSS
14	HG	GL_2
15	Supply	PVSS
16	HG	GL_1
17	Supply	PVSS
18	HG	GL_0
19	HF	SH_2
20	HH	GH_2
21	HF	SH_1
22	HH	GH_1
23	HF	SH_0
24	HH	GH_0
25	HM	VMPMON
26	Supply	PVCC
27	HP	CP

Pin No.	I/O Circuit Type*1	Pin Name
28	Supply	VSS
29	H	P00_0 / TX2(CAN) / SOT7_R*2 / INT4
30	K	P00_1 / INT6 / AN5 / TOT1 / OUT1_R*2
31	K	P00_2/ SOT8_R*2 / IN0 / IN1MFT_R / AN0
32	I	P00_3 / SCK8_R*2 / IN1 / IN2MFT_R / AN1
33	I	P00_4 / SIN7 / INT8/ AN2 / TOT3
34	K	P00_5 / AN4 / TIN1 / OUT0_R*2
35	H	P00_6 / IN0MFT / INT9 / ADTG
36	Z	C5
37	Supply	AV_{CC}
38	I	P00_7 / SCK7_R*2 / AN6
39	K	P01_0 / IN4 / AN3
40	HB	P17_0 / RX2(CAN) / INT10
41	HB	P17_1 / INT0 / NMI
42	HB	P17_2 / SIN7_R / INT1
43	HB	P17_3 / SIN8_R*2 / INT2
44	HB	P17_4 / IN4_R / IN3MFT / INT3
45	HB	P17_5 / IN1_R / IN2MFT / INT5
46	HB	P17_6 / IN0_R / IN1MFT / INT7
47	Z	V5SW
48	F	C1

*1: See "I/O Circuit Type" for details on the I/O circuit types.

*2: Only Relocation Pin. Original Peripheral Resource pin does not exist.

CY96F8E0

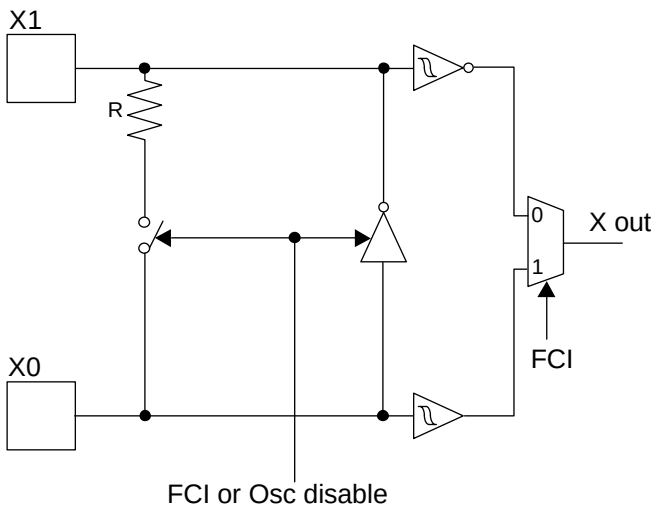
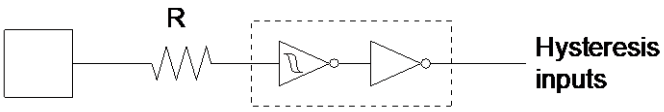
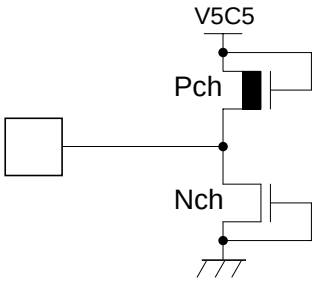
Pin No.	I/O Circuit Type*1	Pin Name
1	Z	V5C5
2	O	DEBUG I/F
3	Supply	V_{SS}
4	A	X1
5	A	X0
6	C	MD
7	C	RSTX
8	HS	V12SW
9	Supply	LV_{SS}
10	HL	LIN
11	HM	VBMON
12	Supply	BV_{CC}
13	Supply	PV_{SS}
14	HG	GL_2
15	Supply	PV_{SS}
16	HG	GL_1
17	Supply	PV_{SS}
18	HG	GL_0
19	HF	SH_2
20	HH	GH_2
21	HF	SH_1
22	HH	GH_1
23	HF	SH_0
24	HH	GH_0
25	HM	VMPMON
26	Supply	PV_{CC}
27	HP	CP
28	Supply	V_{SS}
29	H	P00_0 / TX2(CAN) / SOT7_R*2 / INT4
30	K	P00_1 / INT6 / AN5 / TOT1 / OUT1_R*2
31	K	P00_2/ SOT8_R*2 / IN0 / IN1MFT_R / AN0
32	I	P00_3 / SCK8_R*2 / IN1 / IN2MFT_R / AN1
33	I	P00_4 / SIN7 / INT8/ AN2 / TOT3
34	K	P00_5 / AN4 / TIN1 / OUT0_R*2
35	H	P00_6 / IN0MFT / INT9 / ADTG

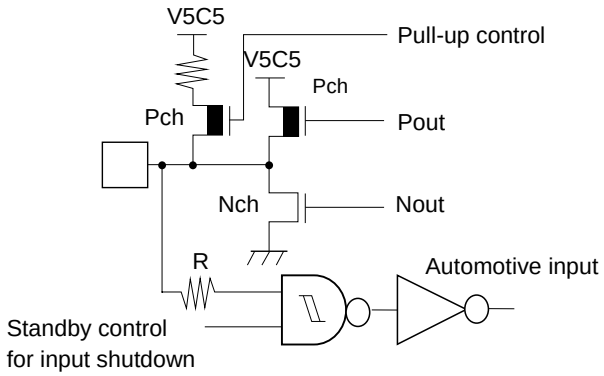
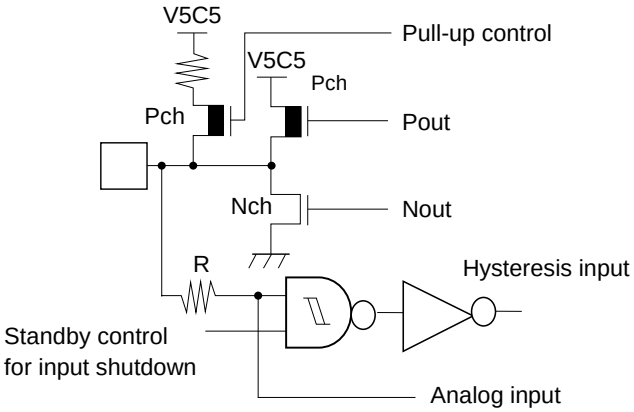
Pin No.	I/O Circuit Type*1	Pin Name
36	Z	C5
37	Supply	AV_{CC}
38	I	P00_7 / SCK7_R*2 / AN6
39	K	P01_0 / IN4 / AN3
40	HB	P17_0 / RX2(CAN) / INT10
41	HB	P17_1 / INT0 / NMI
42	HB	P17_2 / SIN7_R / INT1
43	HB	P17_3 / SIN8_R*2 / INT2
44	HB	P17_4 / IN4_R / IN3MFT / INT3
45	HB	P17_5 / IN1_R / IN2MFT / INT5
46	HB	P17_6 / IN0_R / IN1MFT / INT7
47	Z	V5SW
48	F	C1

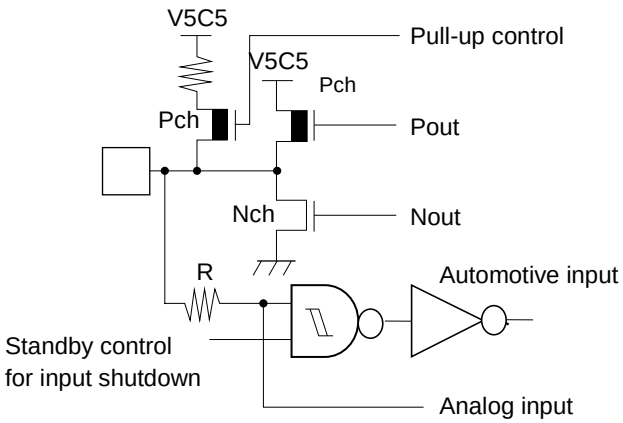
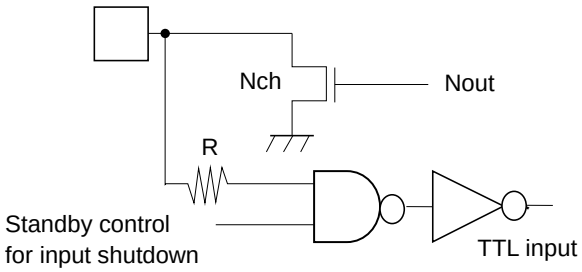
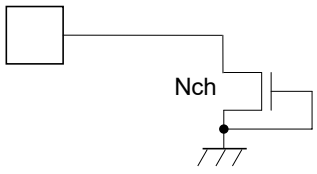
*1: See "I/O CIRCUIT TYPE" for details on the I/O circuit types.

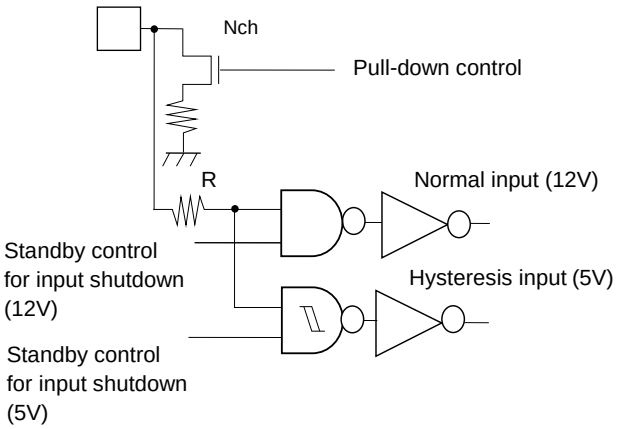
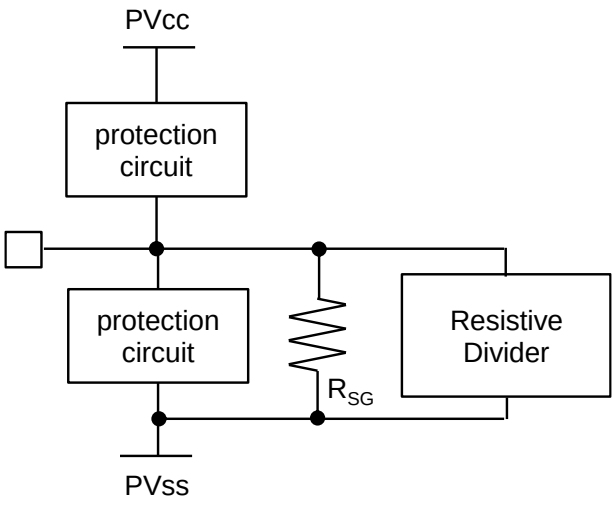
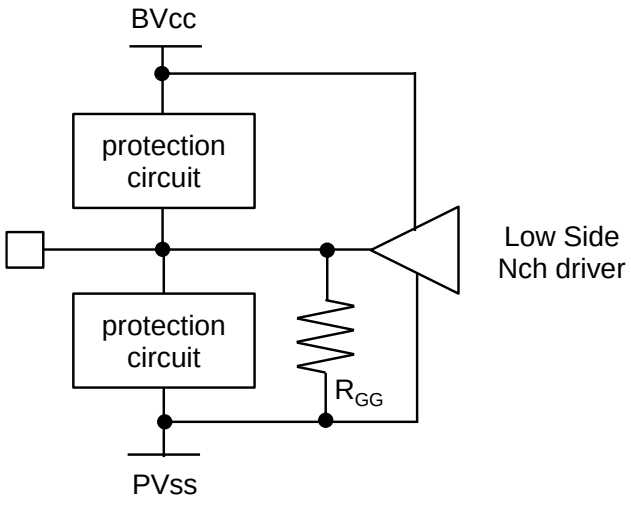
*2: Only Relocation Pin. Original Peripheral Resource pin does not exist.

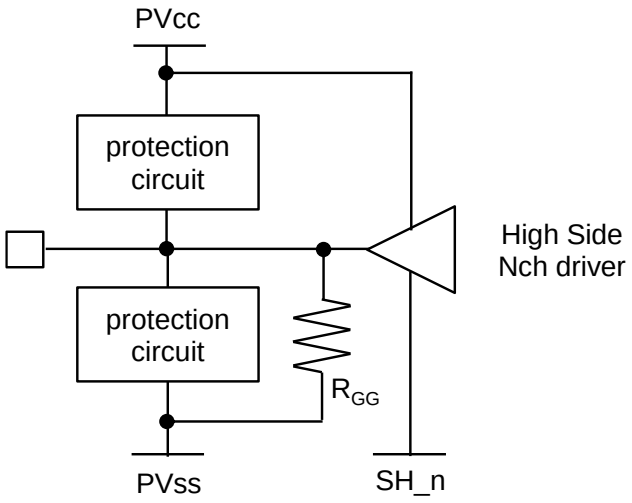
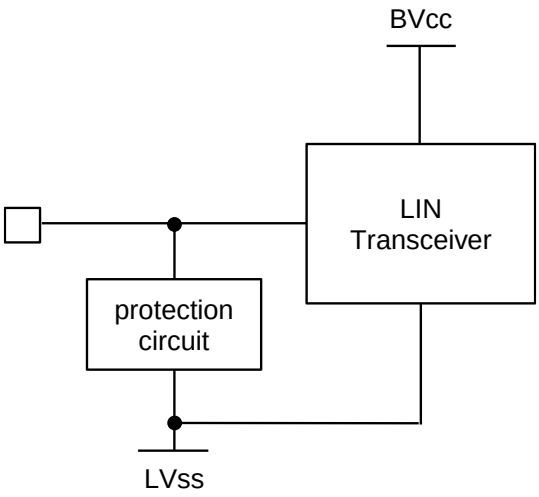
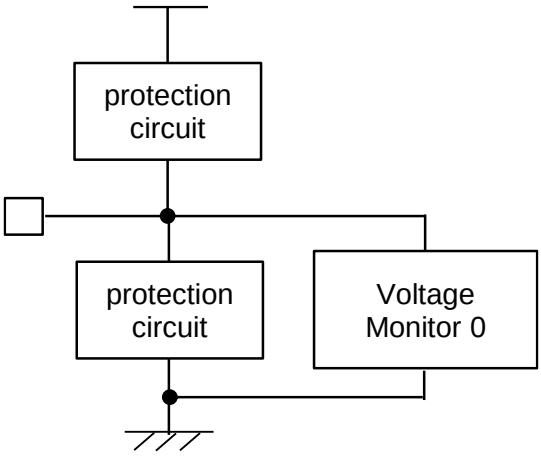
6. I/O Circuit Type

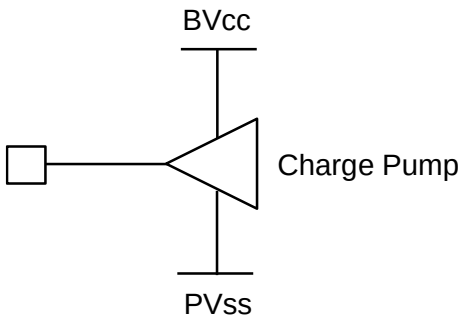
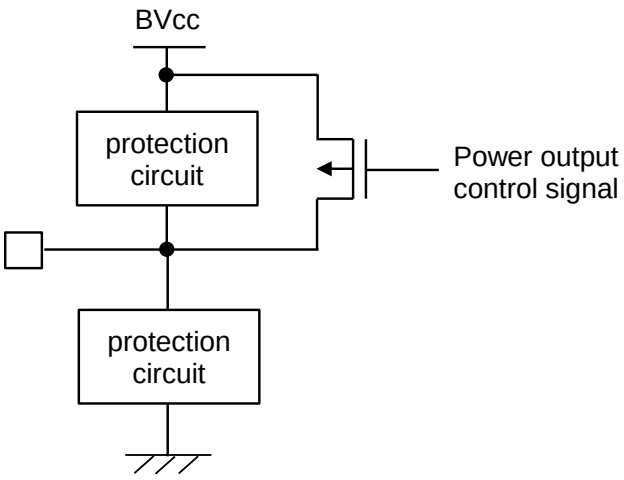
Type	Circuit	Remarks
A		High-speed oscillation circuit: ■ Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) ■ Feedback resistor = approx. 1.0MΩ ■ Feedback register is grounded in the center when the oscillator is disabled or in FCI mode ■ 5V signal
C		■ CMOS hysteresis input pin ■ 5V signal
F		■ Power supply input protection circuit ■ 1.8V signal

Type	Circuit	Remarks
H		■ CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) ■ Automotive input with input shutdown function ■ Programmable pull-up resistor ■ 5V signal
I		■ CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) ■ CMOS hysteresis input with input shutdown function ■ Programmable pull-up resistor ■ Analog input ■ 5V signal

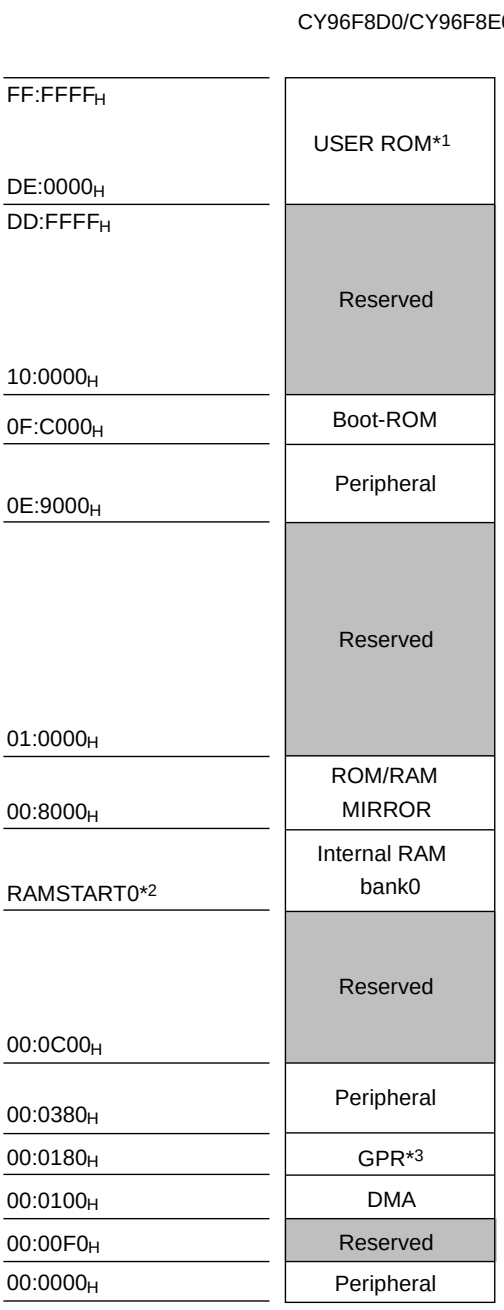
Type	Circuit	Remarks
K		■ CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) ■ Automotive input with input shutdown function ■ Programmable pull-up resistor ■ Analog input ■ 5V signal
O		■ Open-drain input/ output ■ Output 25mA, BV_{CC}=6V ■ TTL input ■ 5V signal
Z		■ Power supply input protection circuit ■ 5V signal

Type	Circuit	Remarks
HB		■ Programmable pull-down resistor ■ Normal input (12V) with input shutdown function ■ CMOS hysteresis input (5V) with input shutdown function ■ 5V/12V signal
HF		■ Motor Monitor input with Sink resistance ■ 12V signal
HG		■ Low Side Nch driver output with Gate discharge resistance for Three-Phase Motor Pre-Driver ■ 12V signal

Type	Circuit	Remarks
HH		■ High Side Nch driver output with Gate discharge resistance for Three-Phase Motor Pre-Driver ■ 12V signal
HL		■ LIN Transceiver input/ output ■ 12V signal
HM		■ Voltage monitor 0 input ■ 12V signal

Type	Circuit	Remarks
HP		■ Charge Pump output ■ 12V signal
HS		■ 12V Power Supply output ■ 12V signal

7. Memory Map



*1: For details about USER ROM area, see "User ROM Memory Map for Flash Devices" .

*2: For RAMSTART addresses, see "RAMSTART Addresses" .

*3: Unused GPR banks can be used as RAM area.

GPR: General-Purpose Register

The DMA area is only available if the device contains the corresponding resource.

The available RAM and ROM areas depend on the device.

8. RAMSTART Addresses

Device	Bank 0 RAM size	RAMSTART0
CY96F8D5K	8KB	$00:6200_H$
CY96F8E5K		

9. User ROM Memory Map for Flash Devices

CPU mode address	MB96F8D5K3 MB96F8E5K3 Flash size 128.5KB+8KB	MB96F8D5KU MB96F8E5KU Flash size 128.5KB+32KB	
$FF:FFFF_H$	SA39 - 64KB	SA39 - 64KB	Bank A of Flash A
$FF:0000_H$			
$FE:FFFF_H$	SA38 - 64KB	SA38 - 64KB	
$FE:0000_H$			
$FD:FFFF_H$	Reserved	Reserved	
$DF:A000_H$			
$DF:9FFF_H$	Reserved	SA4 - 8KB	Bank B of Flash A
$DF:8800_H$			
$DF:87FF_H$	SA4 - 2KB		
$DF:8000_H$			
$DF:7FFF_H$	Reserved	SA3 - 8KB	
$DF:6800_H$			
$DF:67FF_H$	SA3 - 2KB		
$DF:6000_H$			
$DF:5FFF_H$	Reserved	SA2 - 8KB	
$DF:4800_H$			
$DF:47FF_H$	SA2 - 2KB		
$DF:4000_H$			
$DF:3FFF_H$	Reserved	SA1 - 8KB	
$DF:2800_H$			
$DF:27FF_H$	SA1 - 2KB		
$DF:2000_H$			
$DF:1FFF_H$	SAS-512B *	SAS-512B *	Bank A of Flash A
$DF:0000_H$			
$DE:FFFF_H$	Reserved	Reserved	
$DE:0000_H$			

*: Physical address area of SAS-512B is from $DF:0000_H$ to $DF:01FF_H$.
Others (from $DF:0200_H$ to $DF:1FFF_H$) is mirror area of SAS-512B.
Sector SAS contains the ROM configuration block RCBA at CPU address $DF:0000_H$ -$DF:01FF_H$.
SAS can not be used for E^2PROM emulation.

10. Serial Programming Communication Interface

USART pins for Flash serial programming (MD = 0, DEBUG I/F = 0, Serial Communication mode)

CY96F8D5K/ CY96F8E5K		
Pin Number	**USART Number**	**Normal Function**
42	USART7	SIN7_R
29		SOT7_R
38		SCK7_R
43	USART8	SIN8_R
31		SOT8_R
32		SCK8_R

11. Interrupt Vector Table

Vector Number	Offset in Vector Table	Vector Name	Cleared by DMA	Index in ICR to Program	Description
0	$3FC_H$	CALLV0	No	-	CALLV instruction
1	$3F8_H$	CALLV1	No	-	CALLV instruction
2	$3F4_H$	CALLV2	No	-	CALLV instruction
3	$3F0_H$	CALLV3	No	-	CALLV instruction
4	$3EC_H$	CALLV4	No	-	CALLV instruction
5	$3E8_H$	CALLV5	No	-	CALLV instruction
6	$3E4_H$	CALLV6	No	-	CALLV instruction
7	$3E0_H$	CALLV7	No	-	CALLV instruction
8	$3DC_H$	RESET	No	-	Reset vector
9	$3D8_H$	INT9	No	-	INT9 instruction
10	$3D4_H$	EXCEPTION	No	-	Undefined instruction execution
11	$3D0_H$	NMI	No	-	Non-Maskable Interrupt
12	$3CC_H$	DLY	No	12	Delayed Interrupt
13	$3C8_H$	RC_TIMER	No	13	RC Clock Timer
14	$3C4_H$	MC_TIMER	No	14	Main Clock Timer
15	$3C0_H$	-	-	15	Reserved
16	$3BC_H$	LVDI	No	16	Low Voltage Detector
17	$3B8_H$	EXTINT0	Yes	17	External Interrupt 0
18	$3B4_H$	EXTINT1	Yes	18	External Interrupt 1
19	$3B0_H$	EXTINT2	Yes	19	External Interrupt 2
20	$3AC_H$	EXTINT3	Yes	20	External Interrupt 3
21	$3A8_H$	EXTINT4	Yes	21	External Interrupt 4
22	$3A4_H$	EXTINT5	Yes	22	External Interrupt 5
23	$3A0_H$	EXTINT6	Yes	23	External Interrupt 6
24	$39C_H$	EXTINT7	Yes	24	External Interrupt 7
25	398_H	EXTINT8	Yes	25	External Interrupt 8
26	394_H	EXTINT9	Yes	26	External Interrupt 9
27	390_H	EXTINT10	Yes	27	External Interrupt 10
28	$38C_H$	EXTINT11	Yes	28	External Interrupt 11 *
29	388_H	-	-	29	Reserved
30	384_H	-	-	30	Reserved
31	380_H	-	-	31	Reserved
32	$37C_H$	-	-	32	Reserved
33	378_H	-	-	33	Reserved
34	374_H	-	-	34	Reserved
35	370_H	CAN2	No	35	CAN Controller 2
36	$36C_H$	-	-	36	Reserved
37	368_H	-	-	37	Reserved
38	364_H	-	-	38	Reserved
39	360_H	-	-	39	Reserved
40	$35C_H$	-	-	40	Reserved
41	358_H	-	-	41	Reserved
42	354_H	-	-	42	Reserved
43	350_H	-	-	43	Reserved

Vector Number	Offset in Vector Table	Vector Name	Cleared by DMA	Index in ICR to Program	Description
44	$34C_H$	-	-	44	Reserved
45	348_H	-	-	45	Reserved
46	344_H	-	-	46	Reserved
47	340_H	-	-	47	Reserved
48	$33C_H$	-	-	48	Reserved
49	338_H	-	-	49	Reserved
50	334_H	-	-	50	Reserved
51	330_H	-	-	51	Reserved
52	$32C_H$	-	-	52	Reserved
53	328_H	-	-	53	Reserved
54	324_H	-	-	54	Reserved
55	320_H	-	-	55	Reserved
56	$31C_H$	-	-	56	Reserved
57	318_H	-	-	57	Reserved
58	314_H	RLT0	Yes	58	Reload Timer 0
59	310_H	RLT1	Yes	59	Reload Timer 1
60	$30C_H$	RLT2	Yes	60	Reload Timer 2
61	308_H	RLT3	Yes	61	Reload Timer 3
62	304_H	-	-	62	Reserved
63	300_H	-	-	63	Reserved
64	$2FC_H$	-	-	64	Reserved
65	$2F8_H$	ICU0	Yes	65	Input Capture Unit 0
66	$2F4_H$	ICU1	Yes	66	Input Capture Unit 1
67	$2F0_H$	-	-	67	Reserved
68	$2EC_H$	-	-	68	Reserved
69	$2E8_H$	ICU4	Yes	69	Input Capture Unit 4
70	$2E4_H$	ICU5	Yes	70	Input Capture Unit 5
71	$2E0_H$	ICU6	Yes	71	Input Capture Unit 6 *
72	$2DC_H$	-	-	72	Reserved
73	$2D8_H$	-	-	73	Reserved
74	$2D4_H$	ICU9	Yes	74	Input Capture Unit 9
75	$2D0_H$	ICU10	Yes	75	Input Capture Unit 10
76	$2CC_H$	-	-	76	Reserved
77	$2C8_H$	OCU0	Yes	77	Output Compare Unit 0
78	$2C4_H$	OCU1	Yes	78	Output Compare Unit 1
79	$2C0_H$	-	-	79	Reserved
80	$2BC_H$	-	-	80	Reserved
81	$2B8_H$	OCU4	Yes	81	Output Compare Unit 4 *
82	$2B4_H$	-	-	82	Reserved
83	$2B0_H$	OCU6	Yes	83	Output Compare Unit 6
84	$2AC_H$	OCU7	Yes	84	Output Compare Unit 7
85	$2A8_H$	-	-	85	Reserved
86	$2A4_H$	-	-	86	Reserved
87	$2A0_H$	-	-	87	Reserved
88	$29C_H$	-	-	88	Reserved

Vector Number	Offset in Vector Table	Vector Name	Cleared by DMA	Index in ICR to Program	Description
89	298_H	FRT0	Yes	89	Free-Running Timer 0
90	294_H	FRT1	Yes	90	Free-Running Timer 1
91	290_H	FRT2	Yes	91	Free-Running Timer 2
92	$28C_H$	FRT3	Yes	92	Free-Running Timer 3
93	288_H	-	-	93	Reserved
94	284_H	CAL0	No	94	Clock Calibration Unit
95	280_H	-	-	95	Reserved
96	$27C_H$	-	-	96	Reserved
97	278_H	-	-	97	Reserved
98	274_H	-	-	98	Reserved
99	270_H	-	-	99	Reserved
100	$26C_H$	-	-	100	Reserved
101	268_H	-	-	101	Reserved
102	264_H	-	-	102	Reserved
103	260_H	-	-	103	Reserved
104	$25C_H$	-	-	104	Reserved
105	258_H	LINR2	Yes	105	LIN USART 2 RX *
106	254_H	LINT2	Yes	106	LIN USART 2 TX *
107	250_H	-	-	107	Reserved
108	$24C_H$	-	-	108	Reserved
109	248_H	-	-	109	Reserved
110	244_H	-	-	110	Reserved
111	240_H	-	-	111	Reserved
112	$23C_H$	-	-	112	Reserved
113	238_H	-	-	113	Reserved
114	234_H	-	-	114	Reserved
115	230_H	LINR7	Yes	115	LIN USART 7 RX
116	$22C_H$	LINT7	Yes	116	LIN USART 7 TX
117	228_H	LINR8	Yes	117	LIN USART 8 RX
118	224_H	LINT8	Yes	118	LIN USART 8 TX
119	220_H	-	-	119	Reserved
120	$21C_H$	-	-	120	Reserved
121	218_H	-	-	121	Reserved
122	214_H	-	-	122	Reserved
123	210_H	-	-	123	Reserved
124	$20C_H$	-	-	124	Reserved
125	208_H	-	-	125	Reserved
126	204_H	-	-	126	Reserved
127	200_H	-	-	127	Reserved
128	$1FC_H$	-	-	128	Reserved
129	$1F8_H$	-	-	129	Reserved
130	$1F4_H$	-	-	130	Reserved
131	$1F0_H$	-	-	131	Reserved
132	$1EC_H$	-	-	132	Reserved
133	$1E8_H$	FLASHA	Yes	133	Flash memory A interrupt

Vector Number	Offset in Vector Table	Vector Name	Cleared by DMA	Index in ICR to Program	Description
134	$1E4_H$	-	-	134	Reserved
135	$1E0_H$	-	-	135	Reserved
136	$1DC_H$	-	-	136	Reserved
137	$1D8_H$	-	-	137	Reserved
138	$1D4_H$	-	-	138	Reserved
139	$1D0_H$	-	-	139	Reserved
140	$1CC_H$	-	-	140	Reserved
141	$1C8_H$	-	-	141	Reserved
142	$1C4_H$	-	-	142	Reserved
143	$1C0_H$	-	-	143	Reserved
144	$1BC_H$	-	-	144	Reserved
145	$1B8_H$	-	-	145	Reserved
146	$1B4_H$	-	-	146	Reserved
147	$1B0_H$	-	-	147	Reserved
148	$1AC_H$	PPG0MFT	Yes	148	Programmable Pulse Generator MFT0
149	$1A8_H$	-	-	149	Reserved
150	$1A4_H$	PPG2MFT	Yes	150	Programmable Pulse Generator MFT2
151	$1A0_H$	-	-	151	Reserved
152	$19C_H$	PPG4MFT	Yes	152	Programmable Pulse Generator MFT4
153	198_H	-	-	153	Reserved
154	194_H	ICU0MFT	Yes	154	Input Capture Unit MFT0
155	190_H	ICU1MFT	Yes	155	Input Capture Unit MFT1
156	$18C_H$	ICU2MFT	Yes	156	Input Capture Unit MFT2
157	188_H	ICU3MFT	Yes	157	Input Capture Unit MFT3
158	184_H	-	-	158	Reserved
159	180_H	-	-	159	Reserved
160	$17C_H$	-	-	160	Reserved
161	178_H	-	-	161	Reserved
162	174_H	OCU0MFT	Yes	162	Output Compare Unit MFT0
163	170_H	OCU1MFT	Yes	163	Output Compare Unit MFT1
164	$16C_H$	OCU2MFT	Yes	164	Output Compare Unit MFT2
165	168_H	OCU3MFT	Yes	165	Output Compare Unit MFT3
166	164_H	OCU4MFT	Yes	166	Output Compare Unit MFT4
167	160_H	OCU5MFT	Yes	167	Output Compare Unit MFT5
168	$15C_H$	-	-	168	Reserved
169	158_H	-	-	169	Reserved
170	154_H	FRTZD0MFT	Yes	170	Free-Running Timer MFT0-0 detection
171	150_H	FRTZD1MFT	Yes	171	Free-Running Timer MFT1-0 detection
172	$14C_H$	FRTZD2MFT	Yes	172	Free-Running Timer MFT2-0 detection
173	148_H	FRTZD3MFT	Yes	173	Free-Running Timer MFT3-0 detection
174	144_H	FRTZD4MFT	Yes	174	Free-Running Timer MFT4-

Vector Number	Offset in Vector Table	Vector Name	Cleared by DMA	Index in ICR to Program	Description
					0 detection
175	140_H	-	-	175	Reserved
176	$13C_H$	FRTCC0MFT	Yes	176	Free-Running Timer MFT0- compare clear
177	138_H	FRTCC1MFT	Yes	177	Free-Running Timer MFT1- compare clear
178	134_H	FRTCC2MFT	Yes	178	Free-Running Timer MFT2- compare clear
179	130_H	FRTCC3MFT	Yes	179	Free-Running Timer MFT3- compare clear
180	$12C_H$	FRTCC4MFT	Yes	180	Free-Running Timer MFT4- compare clear
181	128_H	-	-	181	Reserved
182	124_H	WGDTU0	Yes	182	Wave Generator Dead Timer Underflow 0
183	120_H	WGDTU1	Yes	183	Wave Generator Dead Timer Underflow 1
184	$11C_H$	WGDTU2	Yes	184	Wave Generator Dead Timer Underflow 2
185	118_H	-	-	185	Reserved
186	114_H	WGDTR0	Yes	186	Wave Generator Dead Timer Reload 0
187	110_H	WGDTR1	Yes	187	Wave Generator Dead Timer Reload 1
188	$10C_H$	WGDTR2	Yes	188	Wave Generator Dead Timer Reload 2
189	108_H	-	-	189	Reserved
190	104_H	DTTI	Yes	190	DTTI Interrupt
191	100_H	ADC0B_CH0	Yes	191	A/D Converter B0 ch.0 conversion end
192	FC_H	ADC0B_CH1	Yes	192	A/D Converter B0 ch.1 conversion end
193	$F8_H$	ADC0B_CH2	Yes	193	A/D Converter B0 ch.2 conversion end
194	$F4_H$	ADC0B_CH3	Yes	194	A/D Converter B0 ch.3 conversion end
195	$F0_H$	ADC0B_CH4	Yes	195	A/D Converter B0 ch.4 conversion end
196	EC_H	ADC0B_CH5	Yes	196	A/D Converter B0 ch.5 conversion end
197	$E8_H$	ADC0B_CH6	Yes	197	A/D Converter B0 ch.6 conversion end
198	$E4_H$	-	-	198	Reserved
199	$E0_H$	ADCRC0B_CH0	No	199	A/D Converter 0B Range Comparator 0 ch.0
200	DC_H	ADCRC0B_CH1	No	200	A/D Converter 0B Range Comparator 0 ch.1
201	$D8_H$	ADCRC0B_CH2	No	201	A/D Converter 0B Range Comparator 0 ch.2
202	$D4_H$	ADCRC0B_CH3	No	202	A/D Converter 0B Range Comparator 0 ch.3
203	$D0_H$	ADCRC0B_CH4	No	203	A/D Converter 0B Range Comparator 0 ch.4
204	CC_H	ADCRC0B_CH5	No	204	A/D Converter 0B Range Comparator 0 ch.5
205	$C8_H$	ADCRC0B_CH6	No	205	A/D Converter 0B Range Comparator 0 ch.6
206	$C4_H$	-	-	206	Reserved
207	$C0_H$	ADC1B_CH8	Yes	207	A/D Converter 1B ch.8 conversion end
208	BC_H	ADC1B_CH9	Yes	208	A/D Converter 1B ch.9 conversion end

Vector Number	Offset in Vector Table	Vector Name	Cleared by DMA	Index in ICR to Program	Description
209	$B8_H$	ADC1B_CH10	Yes	209	A/D Converter 1B ch.10 conversion end
210	$B4_H$	ADC1B_CH11	Yes	210	A/D Converter 1B ch.11 conversion end
211	$B0_H$	ADCRC1B_CH8	No	211	A/D Converter 1B Range Comparator 1 ch.8
212	AC_H	ADCRC1B_CH9	No	212	A/D Converter 1B Range Comparator 1 ch.9
213	$A8_H$	ADCRC1B_CH10	No	213	A/D Converter 1B Range Comparator 1 ch.10
214	$A4_H$	ADCRC1B_CH11	No	214	A/D Converter 1B Range Comparator 1 ch.11
215	$A0_H$	CPON	No	215	Charge Pump Stabilization Wait Timer
216	$9C_H$	PMD	No	216	Waveform Output Signal Pattern Detection

*: Only CY96F8E0

12. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

1. Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

■ Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

■ Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

■ Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

(2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
Therefore, avoid this type of connection.

(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

■ Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

(1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

(2) Be sure that abnormal current flows do not occur during the power-on sequence.

■ Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

■ Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

■ Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

2. Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

■ Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

■ Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

■ Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

■ Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

(1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.

(2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
When you open Dry Package that recommends humidity 40% to 70% relative humidity.

(3) When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

(4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

■ Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

■ Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

(1) Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.

(2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.

(3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.

(4) Ground all fixtures and instruments, or protect with anti-static measures.

(5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

3. Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

13. Handling Devices

Special care is required for the following when handling the device:

- Latch-up prevention
- Unused pins handling
- External clock usage
- Notes on PLL clock mode operation
- Power supply pins (BV_{CC}/V_{SS})
- Crystal oscillator and ceramic resonator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on Power-on
- Stabilization of power supply voltage
- Serial communication
- Mode Pin (MD)
- 5V power supply output (V5C5)
- Built-in 5V regulator stabilization capacitor pin (C5)

For Latch-up Prevention

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than BV_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between BV_{CC} pins and V_{SS} pins.
- The AV_{CC} power supply is applied before the BV_{CC} voltage.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

For the same reason, extra care is required not to let the analog power-supply voltage (AV_{CC}) exceed the digital power-supply voltage.

Unused Pins Handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register PIER = 0).

Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. To prevent latch-up, they must therefore be pulled up or pulled down through resistors which should be more than 2kΩ.

Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

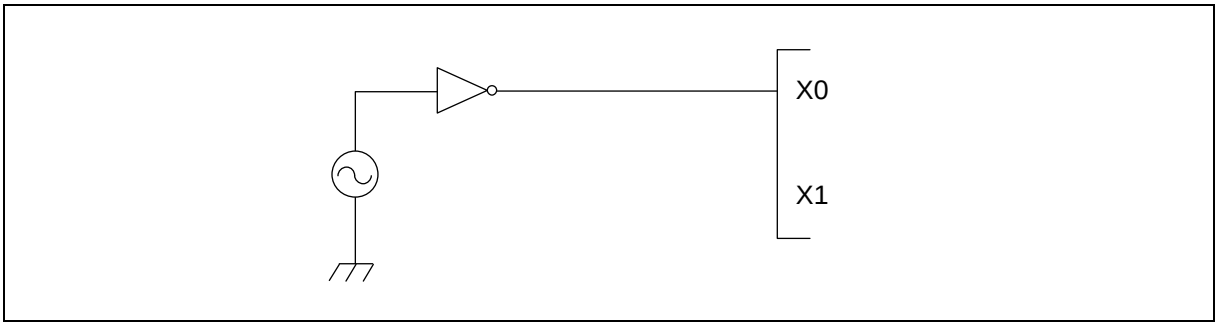
External Clock Usage

The permitted frequency range of an external clock depends on the oscillator type and configuration.

See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

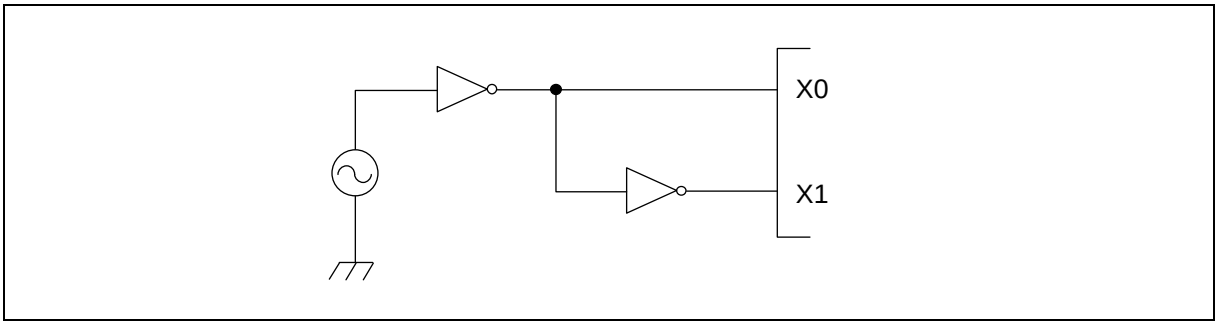
(1) Single phase external clock for Main oscillator

When using a single phase external clock for the Main oscillator, X0 pin must be driven and X1 pin left open.
And supply 5V power to the external clock.



(2) Opposite phase external clock

When using an opposite phase external clock, X1 pin must be supplied with a clock signal which has the opposite phase to the X0 pin.



Notes on PLL Clock Mode Operation

If the device is operated with PLL clock mode and no external oscillator is operating or no external clock is supplied, the device attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

Power Supply Pins (BV_{CC}/V_{SS})

It is required that all BV_{CC}-level as well as all V_{SS}-level power supply pins are at the same potential. If there is more than one BV_{CC} or V_{SS} level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

BV_{CC} and V_{SS} pins must be connected to the device from the power supply with lowest possible impedance.

The smoothing capacitor at BV_{CC} pin must use the one of a capacity value that is larger than C_{C1}.

Besides this, as a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1µF between BV_{CC} and V_{SS} pins as close as possible to BV_{CC} and V_{SS} pins.

Crystal Oscillator and Ceramic Resonator Circuit

Noise at X0, X1 pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

It must be highly provided a printed circuit board art work surrounding X0, X1 pins with a ground area for stabilizing the operation.

It must be highly evaluated the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

Turn on Sequence of Power Supply to A/D Converter and Analog Inputs

It is required to turn the A/D converter power supply (AV_{CC}) and analog inputs (ANn) on after turning power supply (BV_{CC}) on.

It is also required to turn power supply (BV_{CC}) off after turning the A/D converter supply and analog inputs off. Input voltage for ports shared with analog input ports also must not exceed AV_{CC} (turning the analog power (AV_{CC}) and power (BV_{CC}) supplies simultaneously on or off is acceptable).

Pin Handling When Not Using the A/D Converter

If the A/D converter is not used, the power supply pins for A/D converter should be connected such as AV_{CC} = V5C5.

Notes on Power-on

To prevent malfunction of the built-in voltage regulator, supply voltage profile while turning the power supply on should be slower than 20µs from 0.2V to 6.0V.

Stabilization of Power Supply Voltage

If the power supply voltage varies acutely even within the operation safety range of the BV_{CC} power supply voltage, a malfunction may occur. The BV_{CC} power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that BV_{CC} ripple fluctuations (peak to peak value) in the commercial frequencies (50Hz to 60Hz) fall within 10% of the standard BV_{CC} power supply voltage and the transient fluctuation rate becomes 0.1V/µs or less in instantaneous fluctuation for power supply switching.

Serial Communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication.

Therefore, design a printed circuit board so as to avoid noise.

Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

Mode Pin (MD)

Connect the mode pin directly to V5C5 or V_{SS} pin. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pin to V5C5 or V_{SS} pin and provide a low-impedance connection.

5V Power Supply Output (V5C5)

The V5C5 pin combines 5V power supply output and 5V internal power supply, hence the device will not operate due to voltage drops of the 5V internal power supply if the V5C5 pin outputs the currents exceeding the V5C5 output currents (I_{OV5C5}).

The 5V power supply output(V5C5) begins a normal operation immediately after the power supply (BV_{CC}) is turned on, hence be sure to adjust external circuits connected to the V5C5 pin so as not to exceed the V5C5 output currents (I_{OV5C5}), including that when BV_{CC} is turned on.

Built-in 5V Regulator Stabilization Capacitor pin (C5)

Internal 5V regulated power supply stabilization capacitor pin (C5) connects a smoothing capacitor.

Internal 5V regulated power supply stabilization capacitor pin (C5) cannot supply 5V voltages to external circuits.

14. Electrical Characteristics

14.1 Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit	Remarks
			Min	Max		
Power supply voltage *1	BV_{CC1}	-	V_{SS} - 0.3	V_{SS} + 40	V	-
12V analog power supply voltage *1	PV_{CC1}	-	V_{SS} - 0.3	V_{SS} + 40	V	-
5V analog power supply voltage*1	AV_{CC}	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V5C5 = AV_{CC}$*2
12V Input voltage *1	$V12_{I1}$	-	V_{SS} - 0.3	V_{SS} + 40	V	$V12_{I1} \leq BV_{CC} + 0.3V$
5V Input voltage*1	$V5_I$	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V5_I \leq V5C5 + 0.3V$*3
5V Output voltage*1	$V5_O$	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V5_O \leq V5C5 + 0.3V$*3
LIN Input voltage*1	LIN_I	-	-40	+40	V	Based on LV_{SS} and BV_{CC}
"L" level maximum output current for general-purpose I/O	I_{OL}	-	-	15	mA	-
"L" level average output current for general-purpose I/O	I_{OLAV}	-	-	4	mA	-
"L" level maximum overall output current for general-purpose I/O	ΣI_{OL}	-	-	16	mA	-
"L" level average overall output current for general-purpose I/O	ΣI_{OLAV}	-	-	12	mA	-
"H" level maximum output current for general-purpose I/O	I_{OH}	-	-	-15	mA	-
"H" level average output current for general-purpose I/O	I_{OHAV}	-	-	-4	mA	-
"H" level maximum overall output current for general-purpose I/O	ΣI_{OH}	-	-	-16	mA	-
"H" level average overall output current for general-purpose I/O	ΣI_{OHAV}	-	-	-12	mA	-
5Vsupply average overall output current	ΣI_{OV5}	+100°C < T_A ≤ +105°C	-	40	mA	$\Sigma I_{OV5} = I_{OV5SW} + I_{OV5C5}$
		-40°C ≤ T_A ≤ +100°C	-	50		
Permitted power dissipation *5 *8	P_D	T_A= +105°C	-	2050*4	mW	-
Junction Temperature	Tj *6	-	-	+150	°C	-
Operating ambient temperature *8	T_A	-	-40	+105*5 *7	°C	-
Storage temperature	T_{STG}	-	-55	+150	°C	-
Transient input voltage	V_{VBMON1}	-	-	V_{SS} + 40	V	VBMON pin

*1: This parameter is based on $V_{SS} = PV_{SS} = LV_{SS} = 0V$.

*2: AV_{CC} and V5C5 must be set to the same voltage. It is required that AV_{CC} does not exceed V5C5 and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

*3: $V5_I$ and $V5_O$ should not exceed V5C5 + 0.3V. $V5_I$ should also not exceed the specified ratings. Input/Output tages of general I/O ports depend on V5C5.

*4: The maximum permitted power dissipation depends on the ambient temperature, the airflow velocity and the thermal conductance of the package on the PCB.
The actual power dissipation depends on the customer application and can be calculated as follows:

$P_D = P_{IO} + P_{EXP} + P_{INT}$

$P_{IO} = \Sigma ((V_{OL} \times I_{OL}) + ((BV_{CC} - V_{OH}) \times I_{OH}) + (V_{SH} \times V_{SH} / R_{PDDIV} \times DUTY))$

(I/O load power dissipation)

$P_{EXP} = ((BV_{CC} – V_{O5VSW}) \times I_{OV5SW}) + ((BV_{CC} – V_{OV5C5}) \times (I_{OV5C5} + I_A + \Sigma I_{VM0} + I_{VM1})) + ((BV_{CC} – V_{O12VSW}) \times I_{O12})$

(Internal power dissipation in power supply output on the condition that AV_{CC} is supplied from V5C5)

$P_{INT} = (BV_{CC} \times (I_{CC} + I_{TMP} + I_{LINTR} + ICP + I_{HLGD})) + (PV_{CC} \times I_{HLGD}) + (AV_{CC} \times (I_A + \Sigma I_{VM0} + I_{VM1}))$

(Internal power dissipation)

I_{CC} is the total core current consumption into BV_{CC} as described in the "DC Characteristics" and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming.

V_{SH} is the High input voltage to the SH_n pin. DUTY is the High width ratio at the SH_n pin.

($I_A + \Sigma I_{VM0} + I_{VM1}$) is the analog current consumption into AV_{CC}. I_{HLGD} is the analog current consumption into PV_{CC}.

P_{IO} is the sum of the power dissipation for each pin and can be calculated as follows:

- I/O Ports (for each pin)
  Power dissipation = ($V_{OL4} \times I_{OL}$) or ((BV_{CC} -V_{OH4}) × I_{OH})
- Charge Pump (CP pin)
  Power dissipation = V_{OLCP} × ICPO + (BV_{CC} - V_{OHCP}) × ICPO
- Three-phase Motor Pre-Driver (for each phase)
  Power dissipation = $V_{SH} \times V_{SH} / R_{PDDIV} \times DUTY$

On the condition that AV_{CC} is supplied from another external power supply instead of V5C5, Internal power dissipation in power supply output can be calculated as follows:

$P_{EXP} = ((BV_{CC} – V_{O5VSW}) \times I_{OV5SW}) + ((BV_{CC} – V_{OV5C5}) \times I_{OV5C5}) + ((BV_{CC} – V_{O12VSW}) \times I_{O12})$

(Internal power dissipation in power supply output on the condition that AV_{CC} is supplied from another external power supply)

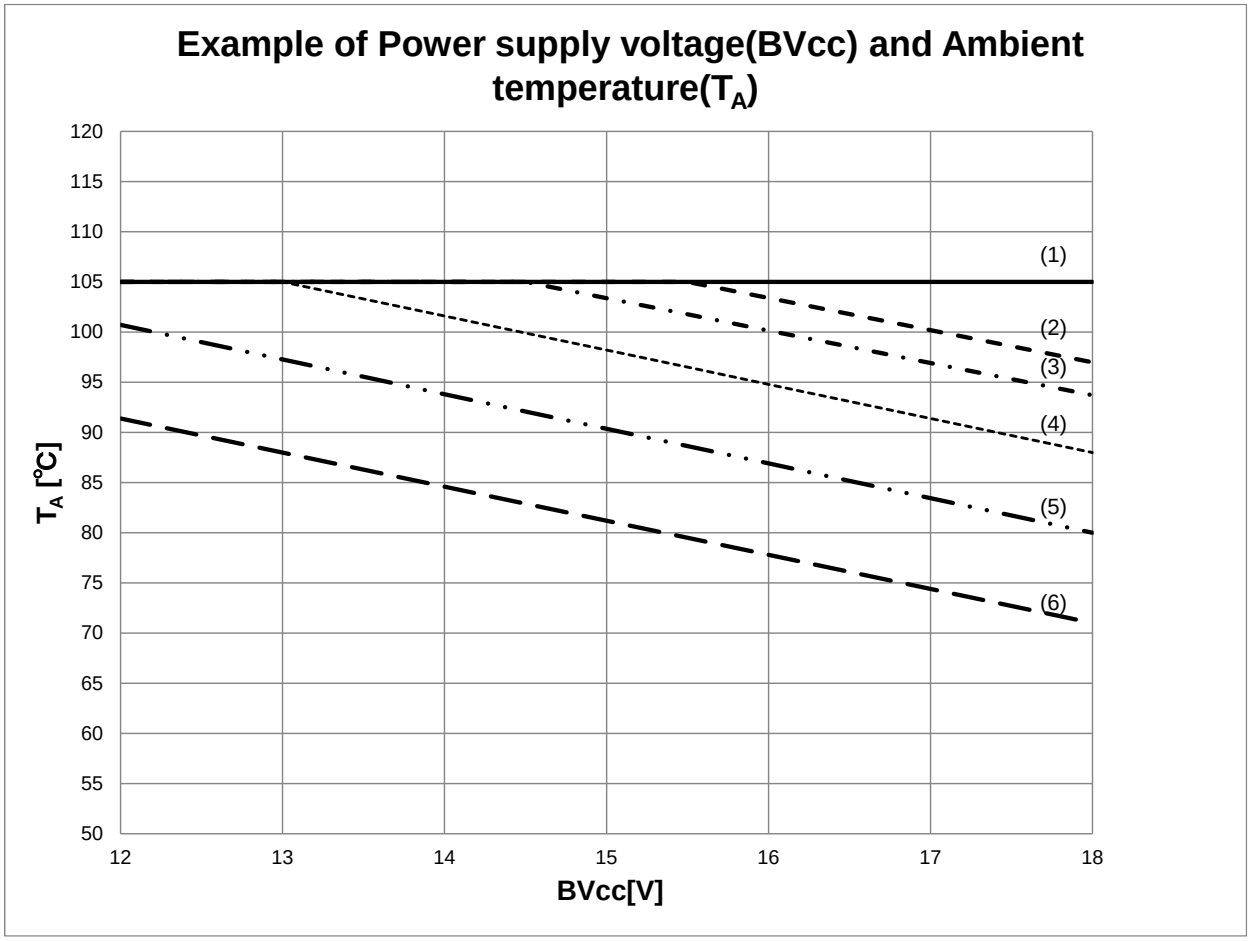
*5: Worst-case value for a package mounted on a 4-layer PCB at specified T_A without airflow.

*6: T_j=T_A (Operating ambient temperature) + (P_D(Power dissipation) × θ_{JA}(Package thermal resistance))

*7: Flash Write/Erase operation for large sector are warranted at $T_A \leq +80°C$.

*8: It is necessary to lower operating ambient temperature on the condition that the actual power dissipation is beyond permitted power dissipation.

An example of power supply voltage (BV_{CC}) and Ambient temperature(T_A) is shown below.



Number	5V Supply Average Overall Output Current	Three-phase Motor Pre-Driver	Flash Memory	
			Small Sector	Large Sector
(1)	40mA	Stop	Write/Read/Erase	Read
(2)	25mA	Enable	Read	Read
(3)	40mA	Enable	Read	Read
(4)	40mA	Enable	Write/Read/Erase	Read
(5)	40mA	Stop	Don't operate	Write/Read/Erase
(6)	40mA	Enable	Don't operate	Write/Read/Erase

WARNING

Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.
Do not exceed any of these ratings.

14.2 Recommended Operating Conditions

(V_{SS} = PV_{SS} = LV_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	BV_{CC}	6	-	18	V	Low-Voltage Detection Function works in 4.08V or more *
Smoothing capacitor at C1 pin	C_{C1}	-	4.7	-	µF	4.7µF (Allowance within ± 40%) Please use the ceramic capacitor or the capacitor of the frequency response of this level. The smoothing capacitor at BV_{CC} must use the one of a capacity value that is larger than C_{C1}.
Smoothing capacitor at V5C5 /C5 pin	C_{V5}	-	2.2	-	µF	2.2µF (Allowance within ± 40%) Please use the ceramic capacitor or the capacitor of the frequency response of this level. The smoothing capacitor at BV_{CC} must use the one of a capacity value that is larger than C_{V5}.
Smoothing capacitor at V5SW pin	C_{V5SW}	-	4.7	-	µF	4.7µF (Allowance within ± 40%) Please use the ceramic capacitor or the capacitor of the frequency response of this level. The smoothing capacitor at BV_{CC} must use the one of a capacity value that is larger than C_{V5SW}.
Smoothing capacitor at V12SW pin	C_{V12SW}	0.1	-	-	µF	0.1µF (Allowance within ± 40%) Please use the ceramic capacitor or the capacitor of the frequency response of this level. The smoothing capacitor at BV_{CC} must use the one of a capacity value that is larger than C_{V12SW}.

*: See ".Low Voltage Detection Function Characteristics" for Detected voltage of Low-Voltage Detection Function.

WARNING

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.
Any use of semiconductor devices will be under their recommended operating condition.
Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.
No warranty is made with respect to any use, operating conditions, or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

14.3 DC Characteristics

14.3.1 Current Ratings

■ CY96F8D5K

(BV_{CC} = 6V to 18V, V_{SS} = PV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Run modes*1*4*5*6	I_{CCPLL}	BV_{CC}	PLL Run mode with CLKS1/2 = CLKB = CLKP1/2 = 20MHz Flash 0 wait (CLKRC stopped)	-	22	-	mA	T_A = +25°C
				-	-	30.9	mA	T_A = +105°C
	I_{CCMAIN}		Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz Flash 0 wait (CLKPLL and CLKRC stopped)	-	3.8	-	mA	T_A = +25°C
				-	-	11	mA	T_A = +105°C
Power supply current in Sleep modes*1*4*6	I_{CCSPLL}		PLL Sleep mode with CLKS1/2 = CLKP1/2 = 20MHz (CLKRC stopped)	-	5.9	-	mA	T_A = +25°C
				-	-	13	mA	T_A = +105°C
	$I_{CCSMAIN}$		Main Sleep mode with CLKS1/2 = CLKP1/2 = 4MHz (CLKPLL and CLKRC stopped)	-	1.1	-	mA	T_A = +25°C
				-	-	6.4	mA	T_A = +105°C
Power supply current in Timer modes*2*4*6	$I_{CCTMAIN}$		Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0 (CLKPLL and CLKRC stopped)	-	430	-	µA	T_A = +25°C
				-	-	2800	µA	T_A =+105°C
	I_{CCTRCH}		RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKPLL and CLKMC stopped)	-	480	-	µA	T_A = +25°C
				-	-	3200	µA	T_A =+105°C
	I_{CCTRCL}		RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 0 (CLKPLL and CLKMC stopped)	-	63	-	µA	T_A = +25°C
				-	-	2000	µA	T_A =+105°C

(BV_{CC} = 6V to 18V, V_{SS} = PV_{SS} = LV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Stop mode*3*4*6	I_{CCH}	BV_{CC}	-	-	-	69	µA	T_A = +25°C BV_{CC}=13.5V
				-	-	1500	µA	T_A = +105°C
Increase current when Flash Memory is not in Power-down	$I_{CCFLASHPD}$		-	-	36	70	µA	-
Power supply current for active Low-Voltage detection function*4	I_{CCLVD}		Low-voltage detection function enabled	-	65	-	µA	T_A = +25°C
				-	-	130	µA	T_A = +105°C
Flash Write/ Erase current*5	$I_{CCFLASH}$		-	-	12.5	-	mA	T_A = +25°C
				-	-	20	mA	T_A = +105°C

*1: The power supply current is measured with a 4MHz external clock connected to the Main oscillator. The currents for the following parts are not included: "On-Chip Debugger" part and output currents of the general-purpose I/O. Power supply current in Run mode does not include Flash Write / Erase current.

*2: The power supply current in Timer mode is the value when Flash is in Power-down / reset mode.
When Flash is not in Power-down / reset mode, $I_{CCFLASHPD}$ must be added to the Power supply current.
The power supply current is measured with a 4MHz external clock connected to the Main oscillator. The currents for the following parts are not included: "On-Chip Debugger" part and output currents of the general-purpose I/O.

*3: The power supply current in Stop mode is the value when Flash is in Power-down / reset mode.
When Flash is not in Power-down / reset mode, $I_{CCFLASHPD}$ must be added to the Power supply current.
The currents for the following parts are not included: "On-Chip Debugger" part and output currents of the general-purpose I/O.

*4: When low-voltage detection function is enabled, I_{CCLVD} must be added to Power supply current.

*5: When Flash Write / Erase program is executed, $I_{CCFLASH}$ must be added to Power supply current.

*6: The power supply current under the following condition.

Function	Run Modes	Sleep Modes	Timer Modes	Stop Modes
Watchdog	Off	Off	Off	Off
10-bit A/D Converter B	Off	Off	Off	Off
5V Power Supply Output (V5SW)	Off	Off	Off	Off
12V Power Supply Output (V12SW)	Off	Off	Off	Off
Voltage Monitor 0	Off	Off	Off	Off
Voltage Monitor 1	Off	Off	Off	Off
Three-Phase Motor Pre-Driver	Off	Off	Off	Off
Charge Pump	Off	Off	Off	Off
Low-Voltage Detection Function	Off	Off	Off	Off
Temperature Sensor	Off	Off	Off	Off
Over-Temperature Detector	On	On	On	Off

Off: Disable or Power down mode

On : Enable mode

■ CY96F8E5K

(BV_{CC} = 6V to 18V, V_{SS} = PV_{SS} = LV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Run modes*1*4*5*6	I_{CCPLL}	BV_{CC}	PLL Run mode with CLKS1/2 = CLKB = CLKP1/2 = 20MHz Flash 0 wait (CLKRC stopped)	-	22	-	mA	T_A = +25°C
				-	-	30.9	mA	T_A = +105°C
	I_{CCMAIN}		Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz Flash 0 wait (CLKPLL and CLKRC stopped)	-	3.8	-	mA	T_A = +25°C
				-	-	11	mA	T_A = +105°C
Power supply current in Sleep modes*1*4*6	I_{CCSPLL}		PLL Sleep mode with CLKS1/2 = CLKP1/2 = 20MHz (CLKRC stopped)	-	5.9	-	mA	T_A = +25°C
				-	-	13	mA	T_A = +105°C
	$I_{CCSMAIN}$		Main Sleep mode with CLKS1/2 = CLKP1/2 = 4MHz (CLKPLL and CLKRC stopped)	-	1.1	-	mA	T_A = +25°C
				-	-	6.4	mA	T_A = +105°C
Power supply current in Timer modes*2*4*6	$I_{CCTMAIN}$		Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0 (CLKPLL and CLKRC stopped)	-	430	-	µA	T_A = +25°C
				-	-	2800	µA	T_A =+105°C
	I_{CCTRCH}		RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKPLL and CLKMC stopped)	-	480	-	µA	T_A = +25°C
				-	-	3200	µA	T_A =+105°C
	I_{CCTRCL}		RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 0 (CLKPLL and CLKMC stopped)	-	63	-	µA	T_A = +25°C
				-	-	2000	µA	T_A =+105°C
Power supply current in Stop mode*3*4*6	I_{CCH}		-	-	-	80	µA	T_A = +25°C BV_{CC}=13.5V
				-	-	1600	µA	T_A = +105°C

(BV_{CC} = 6V to 18V, V_{SS} = PV_{SS} = LV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Increase current when Flash Memory is not in Power-down	$I_{CCFLASHPD}$	BV_{CC}	-	-	36	70	µA	
Power supply current for active Low-Voltage detection function*4	I_{CCLVD}		Low-voltage detection function enabled	-	65	-	µA	T_A = +25°C
				-	-	130	µA	T_A = +105°C
Flash Write/ Erase current*5	$I_{CCFLASH}$		-	-	12.5	-	mA	T_A = +25°C
				-	-	20	mA	T_A = +105°C

*1: The power supply current is measured with a 4MHz external clock connected to the Main oscillator. Currents for the following parts are not included: "On-Chip Debugger" part and output currents of the general-purpose I/O and LIN transceiver. Power supply current in Run mode does not include Flash Write / Erase current.

*2: The power supply current in Timer mode is the value when Flash is in Power-down / reset mode.
When Flash is not in Power-down / reset mode, $I_{CCFLASHPD}$ must be added to the Power supply current.
The power supply current is measured with a 4MHz external clock connected to the Main oscillator. The currents for the following parts are not included: "On-Chip Debugger" part and output currents of the general-purpose I/O and LIN transceiver.

*3: The power supply current in Stop mode is the value when Flash is in Power-down / reset mode.
When Flash is not in Power-down / reset mode, $I_{CCFLASHPD}$ must be added to the Power supply current.
The currents for the following parts are not included: "On-Chip Debugger" part and output currents of the general-purpose I/O and LIN transceiver.

*4: When low-voltage detection function is enabled, I_{CCLVD} must be added to Power supply current.

*5: When Flash Write / Erase program is executed, $I_{CCFLASH}$ must be added to Power supply current.

*6: The power supply current under the following condition.

Function	Run Modes	Sleep Modes	Timer Modes	Stop Modes
Watchdog	Off	Off	Off	Off
10-bit A/D Converter B	Off	Off	Off	Off
5V Power Supply Output (V5SW)	Off	Off	Off	Off
12V Power Supply Output (V12SW)	Off	Off	Off	Off
Voltage Monitor 0	Off	Off	Off	Off
Voltage Monitor 1	Off	Off	Off	Off
Three-Phase Motor Pre-Driver	Off	Off	Off	Off
Charge Pump	Off	Off	Off	Off
Low-Voltage Detection Function	Off	Off	Off	Off
Temperature Sensor	Off	Off	Off	Off
LIN Transceiver (Driver)	Off	Off	Off	Off
LIN Transceiver (Receiver)	Off	Off	Off	On
Over-Temperature Detector	On	On	On	Off

Off: Disable or Power down mode

On : Enable mode

14.3.2 Pin Characteristics

(BV_{CC} = 6V to 18V, V_{SS} = PV_{SS} = LV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	$V5_{IH}$	5V port inputs Pnn_m	-	V5C5 × 0.7	-	V5C5 + 0.3	V	CMOS Hysteresis input
			-	V5C5 × 0.8	-	V5C5 + 0.3	V	AUTOMOTIVE Hysteresis input
	$V12_{IH}$	12V port inputs Pnn_m	5.5V<BV_{CC}	4.68	-	BV_{CC} + 0.3	V	-
			4.2V<BV_{CC}≤5.5V	BV_{CC} × 0.85	-	BV_{CC} + 0.3		
	V_{IHX0S}	X0	External clock in "Fast Clock Input mode"	V5C5 × 0.8	-	V5C5	V	-
	V_{IHR}	RSTX	-	V5C5 × 0.8	-	V5C5 + 0.3	V	CMOS Hysteresis input
	V_{IHM}	MD	-	V5C5 - 0.3	-	V5C5 + 0.3	V	CMOS Hysteresis input
	V_{IHD}	DEBUG I/F	-	2.0	-	V5C5 + 0.3	V	TTL Input
"L" level input voltage	$V5_{IL}$	5V port inputs Pnn_m	-	V_{SS} - 0.3	-	V5C5 × 0.3	V	CMOS Hysteresis input
			-	V_{SS} - 0.3	-	V5C5 × 0.5	V	AUTOMOTIVE Hysteresis input
	$V12_{IL}$	12V port inputs Pnn_m	5.5V<BV_{CC}	V_{SS} - 0.3	-	3.3	V	-
			4.2V<BV_{CC}≤5.5V	V_{SS} - 0.3	-	BV_{CC} × 0.60		
	V_{ILX0S}	X0	External clock in "Fast Clock Input mode"	V_{SS}	-	V5C5 × 0.2	V	-
	V_{ILR}	RSTX	-	V_{SS} - 0.3	-	V5C5 × 0.2	V	CMOS Hysteresis input
	V_{ILM}	MD	-	V_{SS} - 0.3	-	V_{SS} + 0.3	V	CMOS Hysteresis input
	V_{ILD}	DEBUG I/F	-	V_{SS} - 0.3	-	0.8	V	TTL Input
"H" level output voltage	V_{OH4}	4mA type	I_{OH} = -4mA	V5C5 - 0.5	-	V5C5	V	-
"L" level output voltage	V_{OL4}	4mA type	I_{OL} = +4mA	-	-	0.4	V	-
	V_{OL25}	DEBUG I/F	I_{OL} = +25mA	0	-	0.25	V	-
Input leakage current	$I12_{IL}$	12V port inputs Pnn_m	V_{SS} < $V12_I$ < BV_{CC}	- 1	-	+1	µA	-
	$I5_{IL}$	5V port inputs Pnn_m	V_{SS} < $V5_I$ < V5C5 V_{SS} < $V5_I$ < AV_{CC}	- 3	-	+3	µA	-
Pull-up resistance value (5V)	R_{PU}	5V port Pnn_m	V5C5 = 5.0V ±10%	25	50	100	kΩ	-

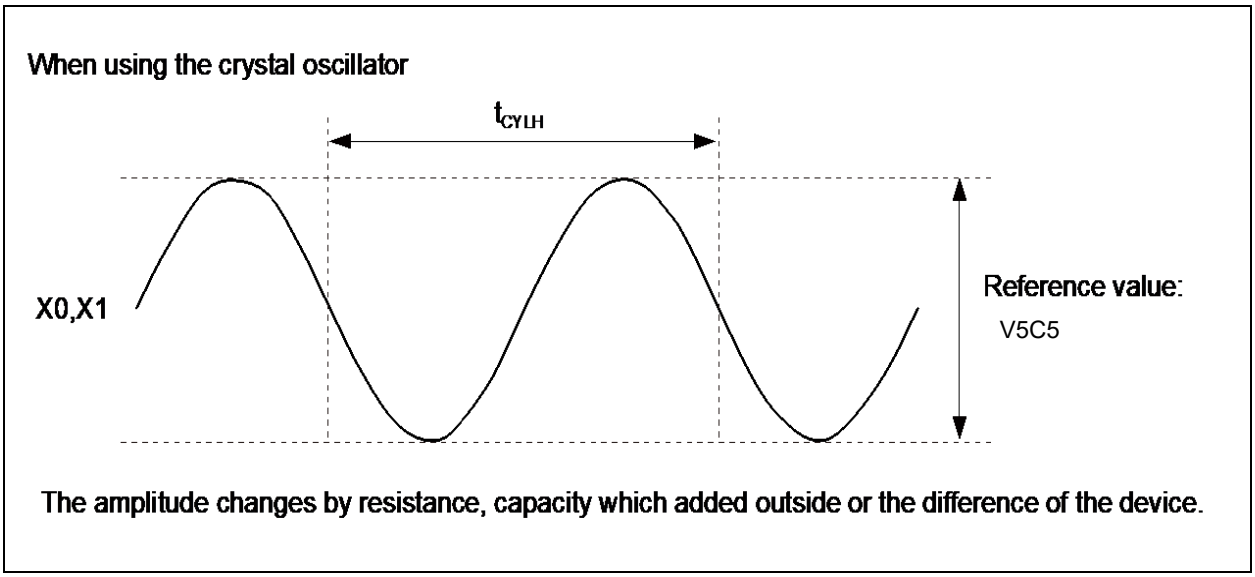
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Pull-down resistance value (12V)	R_{PD}	12V port inputs Pnn_m	V5C5 = 5.0V ±10%	100	135	170	kΩ	-
Input capacitance	$C5_{IN}$	5V port Pnn_m	-	-	15	30	pF	-
	$C12_{IN}$	12V port inputs Pnn_m	-	-	5	15	pF	-

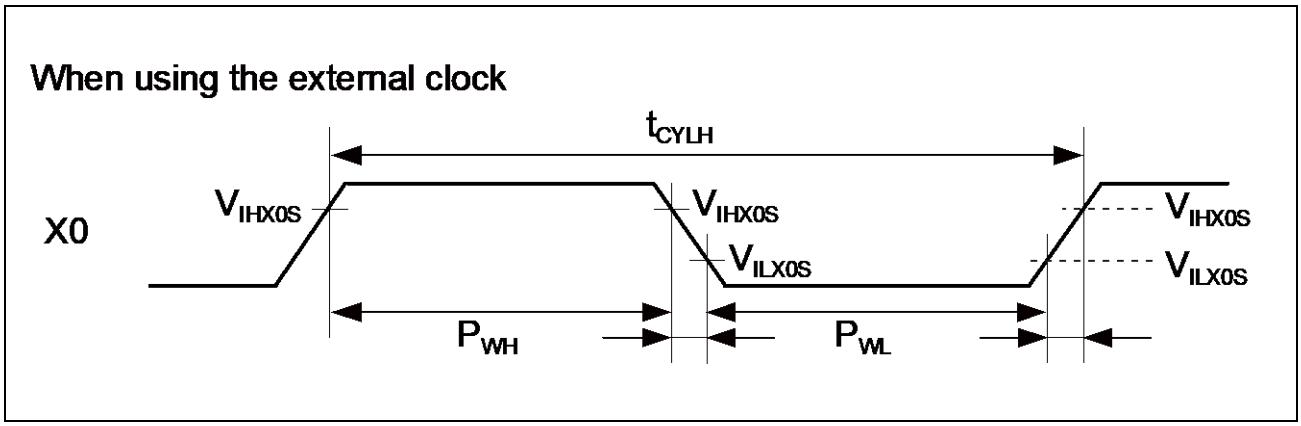
14.4 AC Characteristics

14.4.1 Main Clock Input Characteristics

(BV_{CC} = 6V to 18V, V_{SS} = PV_{SS} = LV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Input frequency	f_C	X0, X1	4	-	8	MHz	When using a crystal oscillator, PLL off
			-	-	8	MHz	When using an opposite phase external clock, PLL off
			4	-	8	MHz	When using a crystal oscillator or opposite phase external clock, PLL on
Input frequency	f_{FCI}	X0	-	-	8	MHz	When using a single phase external clock in "Fast Clock Input mode", PLL off
			4	-	8	MHz	When using a single phase external clock in "Fast Clock Input mode", PLL on
Input clock cycle	t_{CYLH}	-	125	-	-	ns	-
Input clock pulse width	P_{WH}, P_{WL}	-	55	-	-	ns	-





14.4.2 Built-in RC Oscillation Characteristics

(BV_{CC} = 6V to 18V, V_{SS} = PV_{SS} = LV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Clock frequency	f_{RC}	50	100	200	kHz	When using slow frequency of RC oscillator
		1	2	4	MHz	When using fast frequency of RC oscillator
RC clock stabilization time	t_{RCSTAB}	80	160	320	µs	When using slow frequency of RC oscillator (16 RC clock cycles)
		64	128	256	µs	When using fast frequency of RC oscillator (256 RC clock cycles)

14.4.3 Internal Clock Timing

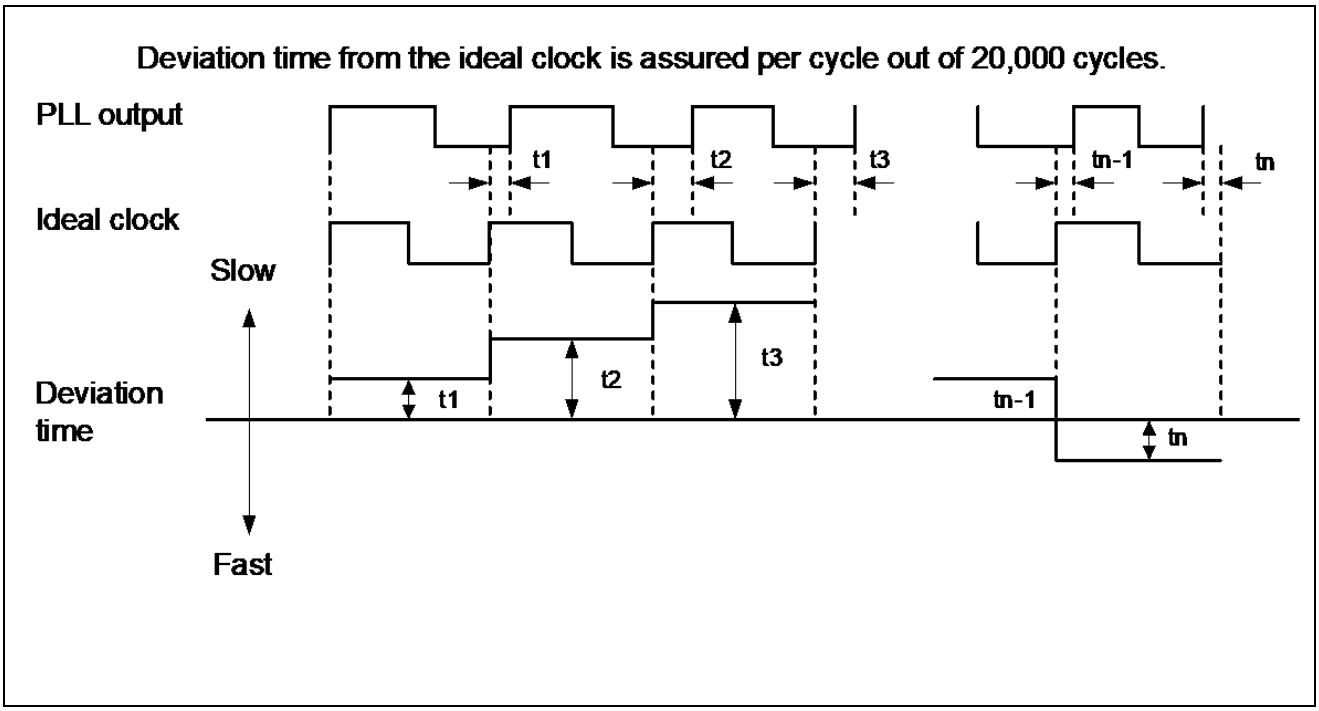
(BV_{CC} = 6V to 18V, V_{SS} = PV_{SS} = LV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Value		Unit
		Min	Max	
Internal System clock frequency (CLKS1 and CLKS2)	f_{CLKS1}, f_{CLKS2}	-	40	MHz
Internal CPU clock frequency (CLKB), Internal peripheral clock frequency (CLKP1)	f_{CLKB}, f_{CLKP1}	-	20	MHz
Internal peripheral clock frequency (CLKP2)	f_{CLKP2}	-	20	MHz

14.4.4 Operating Conditions of PLL

(BV_{CC} = 6V to 18V, V_{SS} = PV_{SS} = LV_{SS} = 0V, T_A = - 40°C to + 105°C)

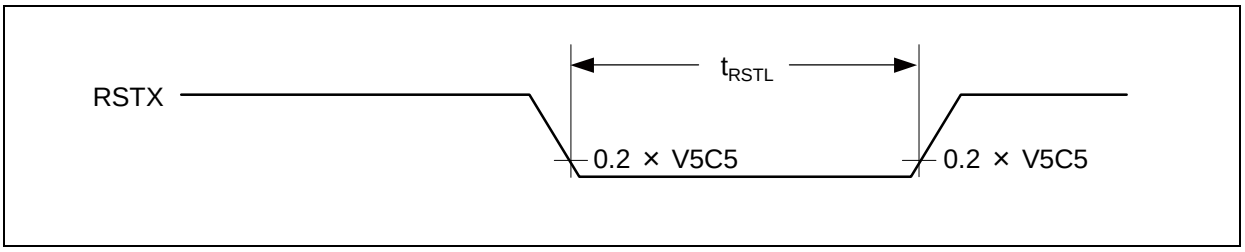
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time	t_{LOCK}	1	-	4	ms	For CLKMC = 4MHz
PLL input clock frequency	f_{PLLI}	4	-	8	MHz	-
PLL oscillation clock frequency	f_{CLKVCO}	56	-	108	MHz	Permitted VCO output frequency of PLL (CLKVCO)
PLL phase jitter	t_{PSKEW}	-5	-	+5	ns	For CLKMC (PLL input clock) ≥ 4MHz



14.4.5 Reset Input

(BV_{CC} = 6V to 18V, V_{SS} = PV_{SS} = LV_{SS} = 0V, T_A = - 40°C to + 105°C)

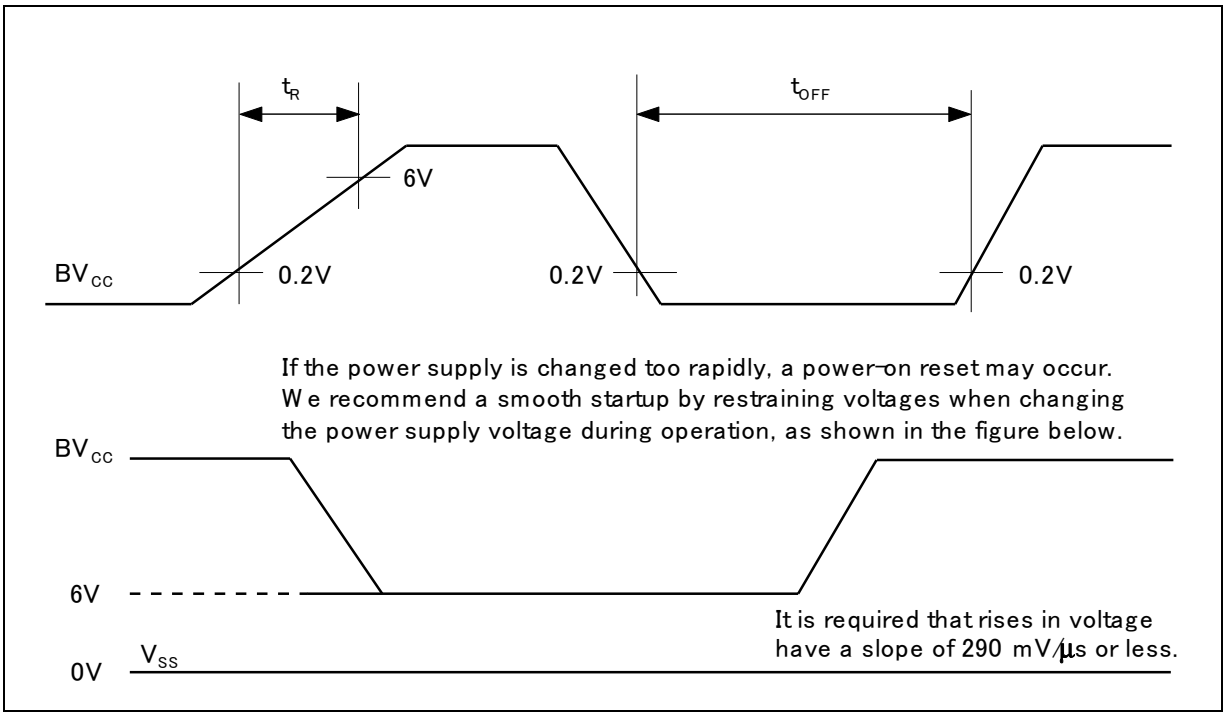
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Reset input time	t_{RSTL}	RSTX	10	-	µs
Rejection of reset input time			1	-	µs



14.4.6 Power-on Reset Timing

(BV_{CC} = 6V to 18V, V_{SS} = PV_{SS} = LV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power-on rise time	t_R	0.02	-	5800	ms
Power-off time	t_{OFF}	10	-	-	ms



14.4.7 USART Timing

(BV_{CC} = 6V to 18V, V_{SS} = PV_{SS} = LV_{SS} = 0V, T_A = - 40°C to + 105°C, C_L=50pF)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKn	Internal shift clock mode	$4t_{CLKP1}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKn, SOTn		- 20	+ 20	ns
SOT → SCK↑ delay time	t_{OVSHI}	SCKn, SOTn		$N \times t_{CLKP1}$ – 20*2	-	ns
SIN → SCK↑ setup time	t_{IVSHI}	SCKn, SINn		t_{CLKP1} +45*1	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKn, SINn		0*1	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKn	External shift clock mode	t_{CLKP1} + 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKn		t_{CLKP1} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKn, SOTn		-	$2t_{CLKP1}$ + 45	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKn, SINn		$t_{CLKP1}/2$ + 10*1	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKn, SINn		t_{CLKP1} + 10*1	-	ns
SCK fall time	t_F	SCKn		-	20	ns
SCK rise time	t_R	SCKn		-	20	ns

Notes:

- AC characteristic in CLK synchronized mode.
- C_L is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in "CY96800 series HARDWARE MANUAL".
- t_{CLKP1} indicates the peripheral clock 1 (CLKP1), Unit: ns.

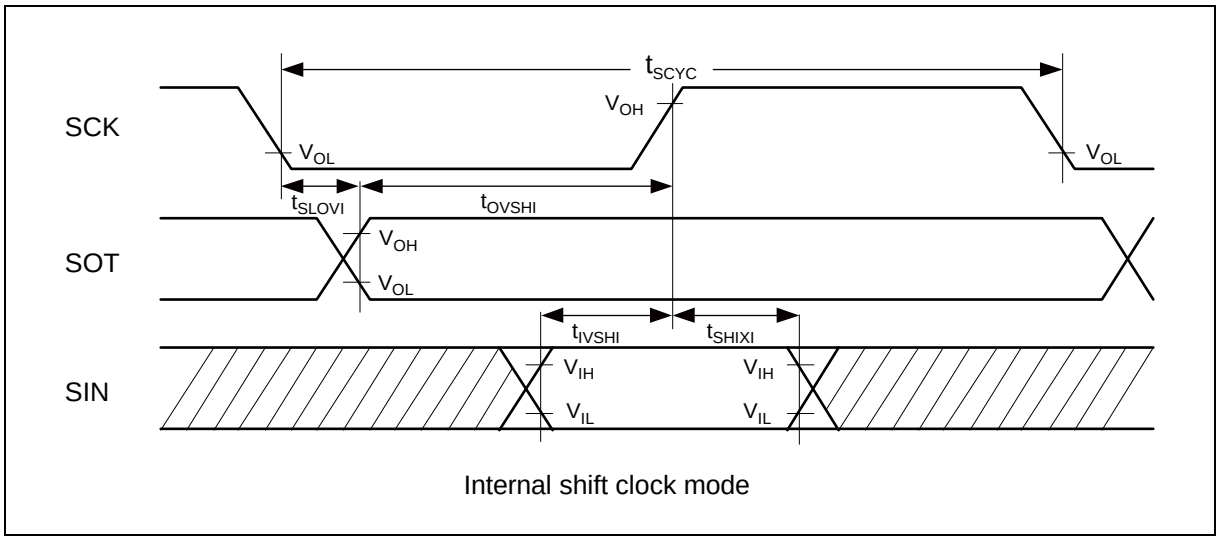
*1: Values for the I/O circuit type, HB, at CMOS hysteresis input voltage (5V). These values are not guaranteed for the normal input (12V).

*2: Parameter N depends on t_{SCYC} and can be calculated as follows:

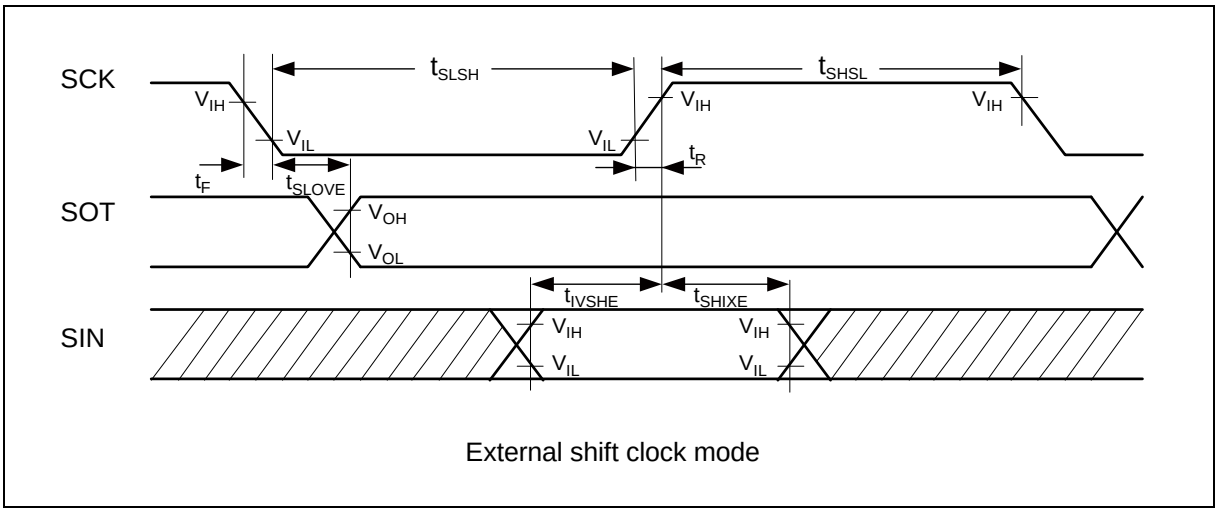
- If $t_{SCYC} = 2 \times k \times t_{CLKP1}$, then N = k, where k is an integer > 2
- If $t_{SCYC} = (2 \times k + 1) \times t_{CLKP1}$, then N = k + 1, where k is an integer > 1

Examples:

t_{SCYC}	N
$4 \times t_{CLKP1}$	2
$5 \times t_{CLKP1}$, $6 \times t_{CLKP1}$	3
$7 \times t_{CLKP1}$, $8 \times t_{CLKP1}$	4
...	...



Internal shift clock mode



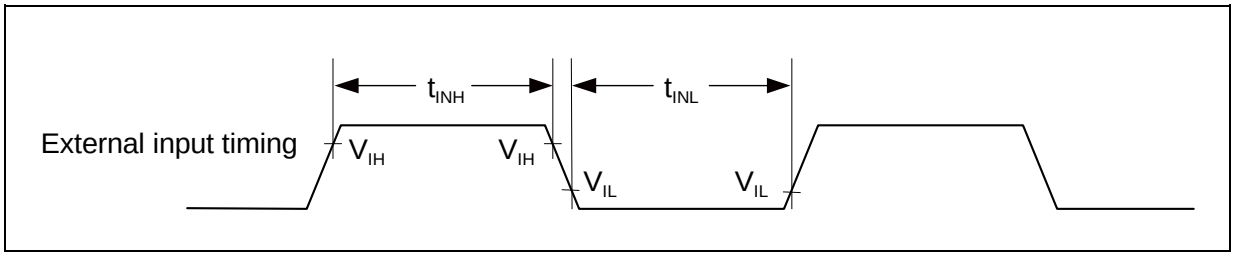
External shift clock mode

14.4.8 External Input Timing

(BV_{CC} = 6V to 18V, V_{SS} = PV_{SS} = LV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Input pulse width	t_{INH}, t_{INL}	Pnn_m	$2t_{CLKP1}$ +200 (t_{CLKP1}= $1/f_{CLKP1}$)*	-	ns	General-Purpose I/O (except I/O circuit type: HB)
		ADTG				A/D Converter trigger input
		TINn				Reload Timer
		INn				Input Capture (except I/O circuit type: HB)
		Pnn_m	$2t_{CLKP1}$ +400 (t_{CLKP1}= $1/f_{CLKP1}$)*	-	ns	General-Purpose I/O (I/O circuit type: HB)
		INn				Input Capture (I/O circuit type: HB)
		INTn	200	-	ns	External Interrupt (except I/O circuit type: HB)
			400	-	ns	External Interrupt (I/O circuit type: HB)
		NMI	400	-	ns	Non-Maskable Interrupt

*: t_{CLKP1} indicates the peripheral clock1 (CLKP1) cycle time except stop when in stop mode.



14.5 10-bit A/D Converter

14.5.1 Electrical Characteristics of the A/D Converter

(BV_{CC} = 6V to 18V, V_{SS} = PV_{SS} = LV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	-
Total error	-	-	- 3.0	-	+ 3.0	LSB	Except for SH_n pin*2
			- 12.0	-	+ 12.0	LSB	SH_n *3
Nonlinearity error	-	-	- 2.5	-	+ 2.5	LSB	-
Differential Nonlinearity error	-	-	- 1.9	-	+ 1.9	LSB	-
Zero transition voltage	V_{OT}	ANn	Typ - 20	V_{SS} + 0.5LSB	Typ + 20	mV	-
Full-scale transition voltage	V_{FST}	ANn	Typ - 20	AV_{CC} - 1.5LSB	Typ + 20	mV	-
Compare time *1	-	-	0.6	-	5.0	µs	4.5V ≤ AV_{CC} ≤ 5.5V
Sampling time *1	-	-	0.5 *2	-	-	µs	4.5V ≤ AV_{CC} ≤ 5.5V
Power supply current	I_A	AV_{CC}	-	2.5	3.5	mA	A/D Converter in operation (per unit)
	I_{AH}		-	-	4.3	µA	A/D Converter not in operation
Analog input capacity	C_{VIN}	ANn	-	-	20	pF	-
Analog impedance	R_{VIN}	ANn	-	-	1550	Ω	4.5V ≤ AV_{CC} ≤ 5.5V
Analog port input current (during conversion)	I_{AIN}	ANn	- 0.3	-	+ 0.3	µA	V_{SS} < V_{AIN} < AV_{CC}
Analog input voltage	V_{AIN}	ANn	V_{SS}	-	AV_{CC}	V	-
Variation between channels	-	ANn	-	-	4	LSB	-

*1: Time for each channel.

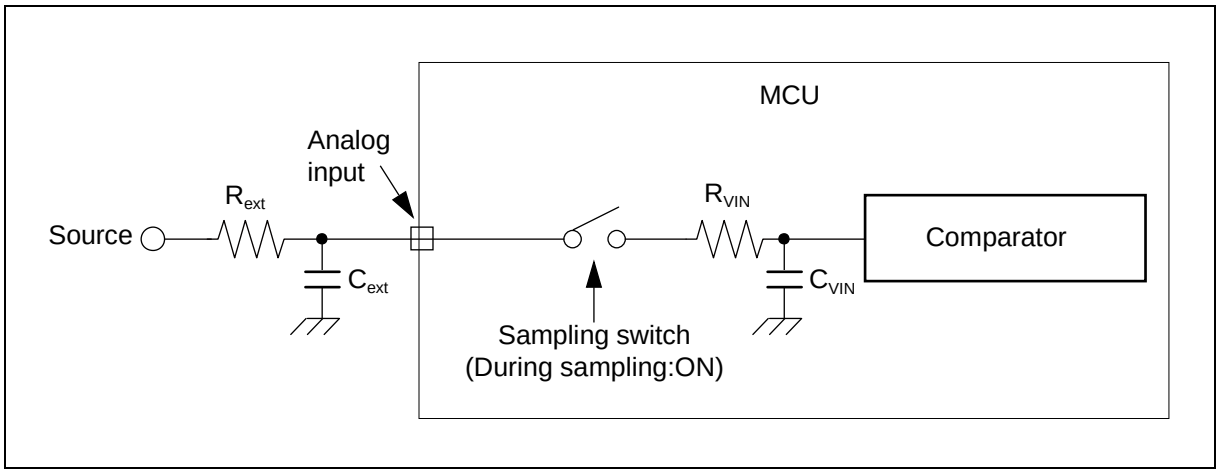
*2: The value is not the one at the minimum sampling time because a Resistor voltage divider more than 10kΩ is connected to the motor-monitor input terminal (SH_n).

*3:The value of Motor Monitor input terminal (SH_n) at the minimum sampling time

14.5.2 Accuracy and Setting of the A/D Converter Sampling Time

If the external impedance is too high or the sampling time too short, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting the A/D conversion precision.

To satisfy the A/D conversion precision, a sufficient sampling time must be selected. The required sampling time (Tsamp) depends on the external driving impedance Rext, the board capacitance of the A/D converter input pin Cext and the AV_{CC} voltage level. The following replacement model can be used for the calculation:



R_{ext}: External driving impedance

C_{ext}: Capacitance of PCB at A/D converter input

C_{VIN}: Analog input capacity (I/O, analog switch and A/D converter are contained)

R_{VIN}: Analog input impedance (I/O, analog switch and A/D converter are contained)

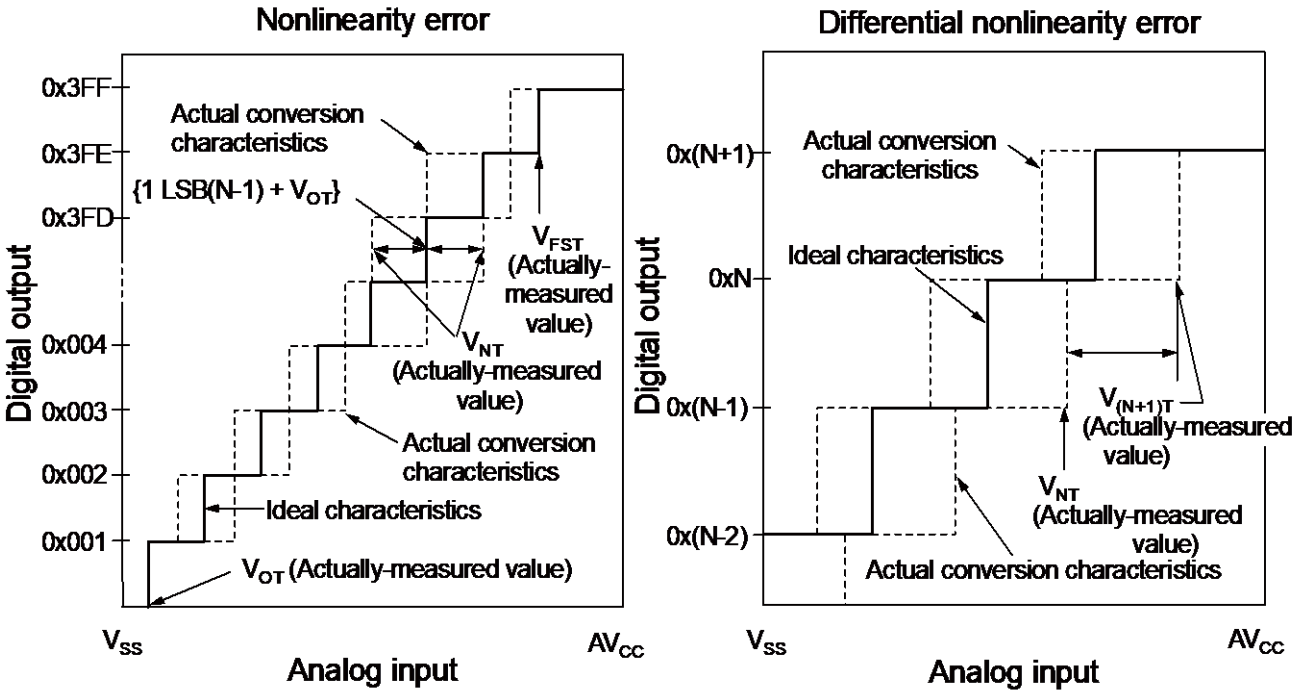
The following approximation formula for the replacement model above can be used:

Tsamp = 7.62 × (Rext × Cext + (Rext + RVIN) × CVIN)

- Do not select a sampling time below the absolute minimum permitted value. (0.5µs for 4.5V ≤ AV_{CC} ≤ 5.5V)
- If the sampling time cannot be sufficient, connect a capacitor of about 0.1µF to the analog input pin.
- A big external driving impedance also adversely affects the A/D conversion precision due to the pin input leakage current I_{IL} (static current before the sampling switch) or the analog input leakage current I_{AIN} (total leakage current of pin input and comparator during sampling). The effect of the pin input leakage current I_{IL} cannot be compensated by an external capacitor.
- The accuracy gets worse as |AV_{CC} - V_{SS}| becomes smaller.

14.5.3 Definition of A/D Converter Terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Nonlinearity error : Deviation of the actual conversion characteristics from a straight line that connects the zero transition point (0b0000000000 ⟷ 0b0000000001) to the full-scale transition point (0b1111111110 ⟷ 0b1111111111).
- Differential nonlinearity error : Deviation from the ideal value of the input voltage that is required to change the output code by 1LSB.
- Total error : Difference between the actual value and the theoretical value. The total error
- includes zero transition error, full-scale transition error and nonlinearity error.
- Zero transition voltage: Input voltage which results in the minimum conversion value.
- Full-scale transition voltage: Input voltage which results in the maximum conversion value.



$$\text{Nonlinearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{OT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential nonlinearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

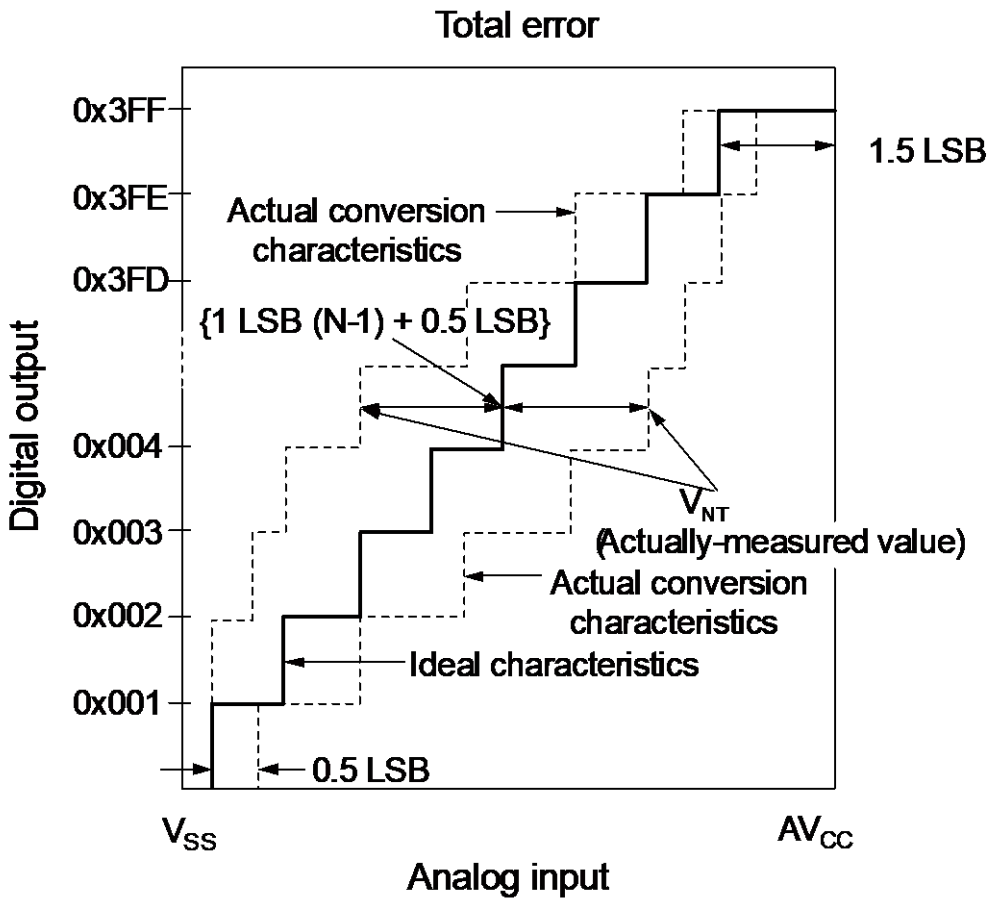
$$1LSB = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

N : A/D converter digital output value.

V_{OT}: Voltage at which the digital output changes from 0x000 to 0x001.

V_{FST}: Voltage at which the digital output changes from 0x3FE to 0x3FF.

V_{NT}: Voltage at which the digital output changes from 0x(N − 1) to 0xN.



$$1LSB\ (Ideal\ value) = \frac{AV_{CC} - V_{SS}}{1024}\ [V]$$

$$Total\ error\ of\ digital\ output\ N = \frac{V_{NT} - \{1LSB \times (N - 1) + 0.5LSB\}}{1LSB}\ [LSB]$$

N : A/D converter digital output value.

V_{NT}: Voltage at which the digital output changes from 0x(N + 1) to 0xN.

V_{OT} (Ideal value) = V_{SS} + 0.5LSB[V]

V_{FST} (Ideal value) = AV_{CC} - 1.5LSB[V]

14.6 Voltage monitor 0

Electrical Characteristics of Voltage Monitor 0

(BV_{CC} = 6V to 18V, V_{SS} = PV_{SS} = LV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input voltage *2	V_{IN0}	VBMON, VMPMON V12SW BV_{CC}	-	3.0	-	BV_{CC} +0.3	V	-
Input resistance *3	R_{PD0}	VBMON, VMPMON V12SW BV_{CC}	-	100	240	530	kΩ	R_{PD0}=R01+R02
	R03		-	180	400	880	kΩ	-
	R04		-	900	2000	4400	kΩ	-
Zener voltage	V_{Z01}	-	-	5.2	5.8	6.4	V	Zener diode voltage of D_{Z01}
Offset error *1*2	V_{OFF0}	VBMON, VMPMON V12SW BV_{CC}	-	-90	-	+90	mV	-
Resistor voltage division ratio *2	R_{DIV0}	-	-	-	1/6	-	-	R_{DIV0} =R02/(R01+R02) Error = ±1.4%
Power supply current	I_{VM0}	AV_{CC}	-	-	1	2.0	mA	Voltage monitor 0 in operation

*1: The offset error occurs with an built-in amplifier. The value is voltage on pins. The input voltage into A/D C is divided by resistance.

*2: When the input voltage is monitored, the measurement error including the error for A/D C can be calculated by the following approximate expression.

Measurement error =

± (V_{IN0} × (Resistor voltage division ratio error + Voltage error of AV_{CC}) + V_{OFF0} + ((total error of A/D C)/ R_{DIV0}))

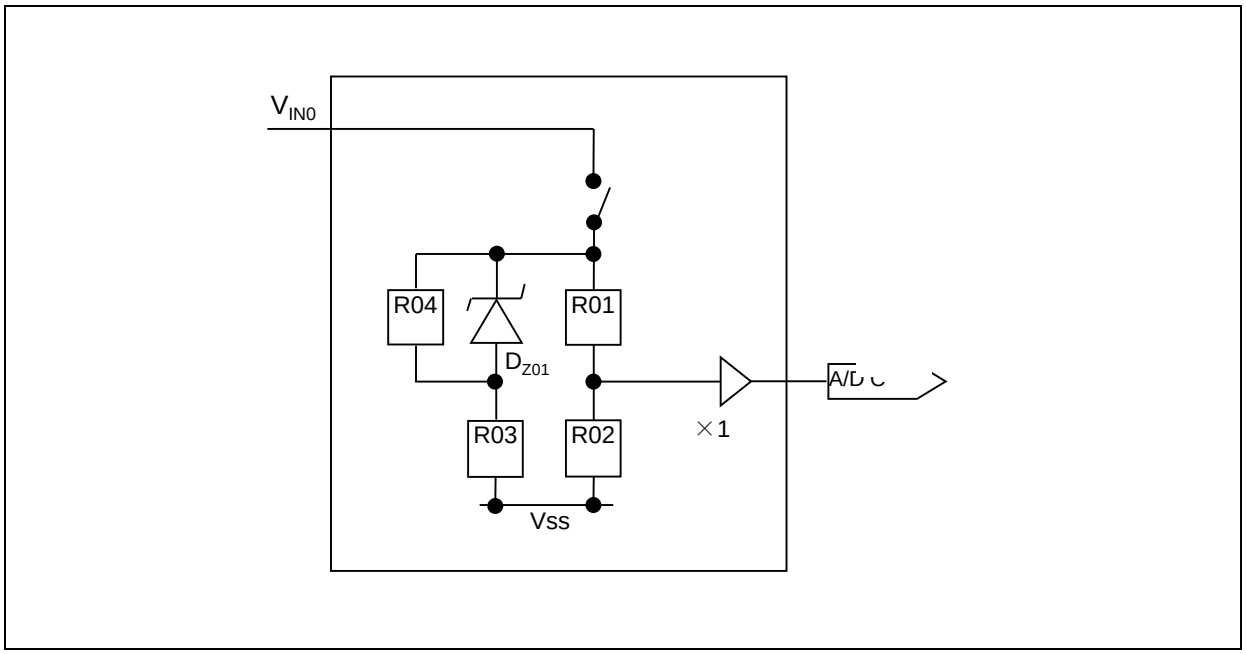
For example: the measurement error of input voltage at AV_{CC} = V5C5

Measurement error = ± (V_{IN0} × (0.014 +0.03) + 0.09 + (5/1024) × 3 × 6)

*3: When the input voltage is high, the voltage of R04 is fixed to Zener voltage and combined resistance changes as follows

- V_{IN0} > V_{Z01}×(R03+R04) /R04:
  combined resistance = 1 / ((R01+R02+R03)/((R01+R02)×R03) -V_{Z01}/(V_{IN0}×R03))
- V_{IN0} ≤ V_{Z01}×(R03+R04) /R04:
  combined resistance = ((R01+R02)×(R03+R04)) / (R01+R02+R03+R04)
  For example: In the case that the value of Input resistance is Typical.
- combined resistance = 179 kΩ (V_{IN0} = 13.5V)
- combined resistance = 218 kΩ (V_{IN0} ≤ 6.96V)

Block Diagram of Voltage Monitor 0



14.7 Voltage Monitor 1

Electrical Characteristics of the Voltage Monitor 1

(BV_{CC} = 6V to 18V, V_{SS} = PV_{SS} = LV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input voltage *2	V_{IN1}	PV_{CC}	-	-	PV_{CC}	-	V	-
Input resistance *3	R_{PD1}	PV_{CC}	-	180	400	880	kΩ	R_{PD1}=R11+R12
	R13		-	180	400	880	kΩ	-
	R14		-	900	2000	4400	kΩ	-
Zener voltage	V_{Z11}	-	-	5.2	5.8	6.4	V	Zener diode voltage of D_{Z11}
Offset error *1*2	V_{OFF1}	PV_{CC}	-	-150	-	+150	mV	-
Resistor voltage division ratio *2	R_{DIV1}	-	-	-	1/10	-	-	R_{DIV0} =R12/(R11+R12) Error = ±1.3%
Power supply current	I_{VM1}	AV_{CC}	-	-	1	2.1	mA	Voltage monitor 1 in operation

*1: The offset error occurs with an built-in amplifier. The value is voltage on pins. The input voltage into A/D C is divided by resistance.

*2: When the input voltage is monitored, the measurement error including the error for A/D C can be calculated by the following approximate expression.

Measurement error =

± (V_{IN1} × (Resistor voltage division ratio error + Voltage error of AV_{CC}) + V_{OFF1} + ((total error of A/D C)/ R_{DIV1}))

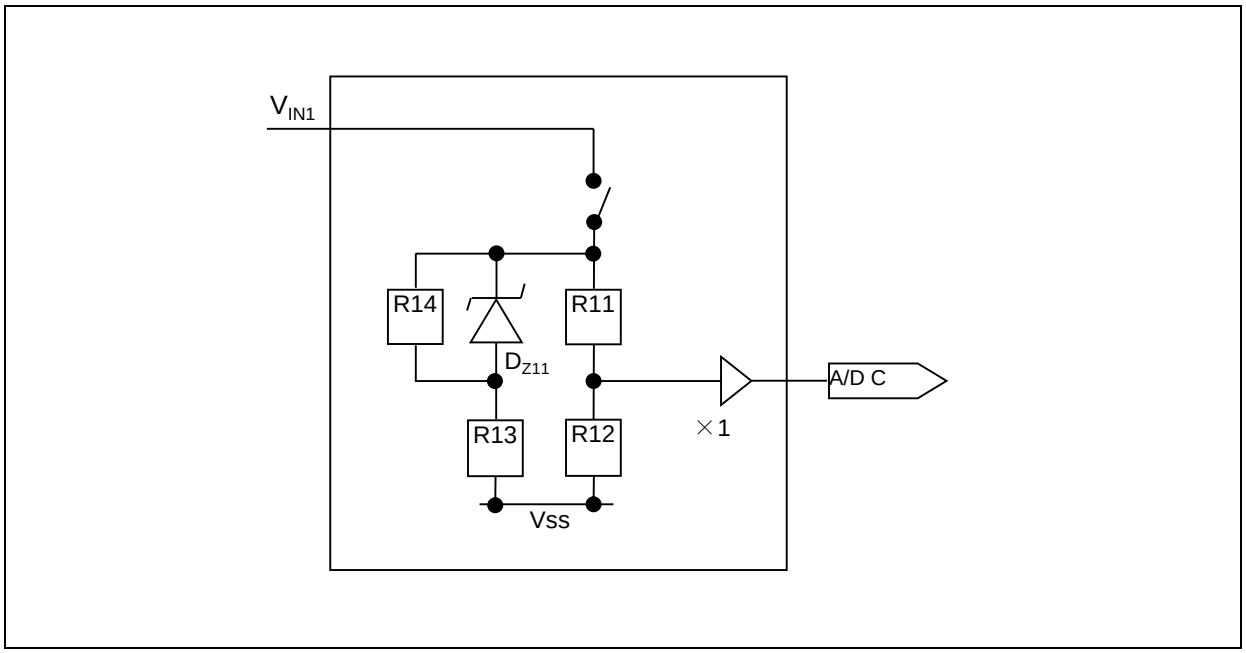
For example: the measurement error of input voltage at AV_{CC} = V5C5

Measurement error = ± (V_{IN1} × (0.013 +0.03) + 0.15 + (5/1024) × 3 × 10)

*3: When the input voltage is high, the voltage of R14 is fixed to Zener voltage and combined resistance changes as follows

- V_{IN1} > V_{Z11}×(R13+R14) /R14:
  combined resistance = 1 / ((R11+R12+R13)/((R11+R12)×R13) -V_{Z11}/(V_{IN1}×R13))
- V_{IN1} ≤ V_{Z11}×(R13+R14) /R14:
  combined resistance = ((R11+R12)×(R13+R14)) / (R11+R12+R13+R14)
  For example: In the case that the value of Input resistance is Typical.
- combined resistance = 255 kΩ (V_{IN1} = 13.5V)
- combined resistance = 343 kΩ (V_{IN1} ≤ 6.96V)

Block Diagram of the Voltage Monitor 1



14.8 Resistor Voltage Divider

Electrical Characteristics of Resistor Voltage Divider

(BV_{CC} = 6V to 18V, V_{SS} = PV_{SS} = LV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input voltage *1	V_{INDIV}	SH_0, SH_1, SH_2	-	V_{SS}	-	BV_{CC} +0.3	V	-
Input resistance *2	R_{PDDIV}		-	7.9	13	18	kΩ	R_{PDDIV}=Rd1+Rd2
Resistor voltage division ratio *1	R_{DIVD}	-	-	-	1/6	-	-	R_{DIVD} =Rd2/(Rd1+Rd2) Error = ±0.9%

*1: When the input voltage is monitored, the measurement error including the error for A/D C can be calculated by the following approximate expression.

Measurement error =

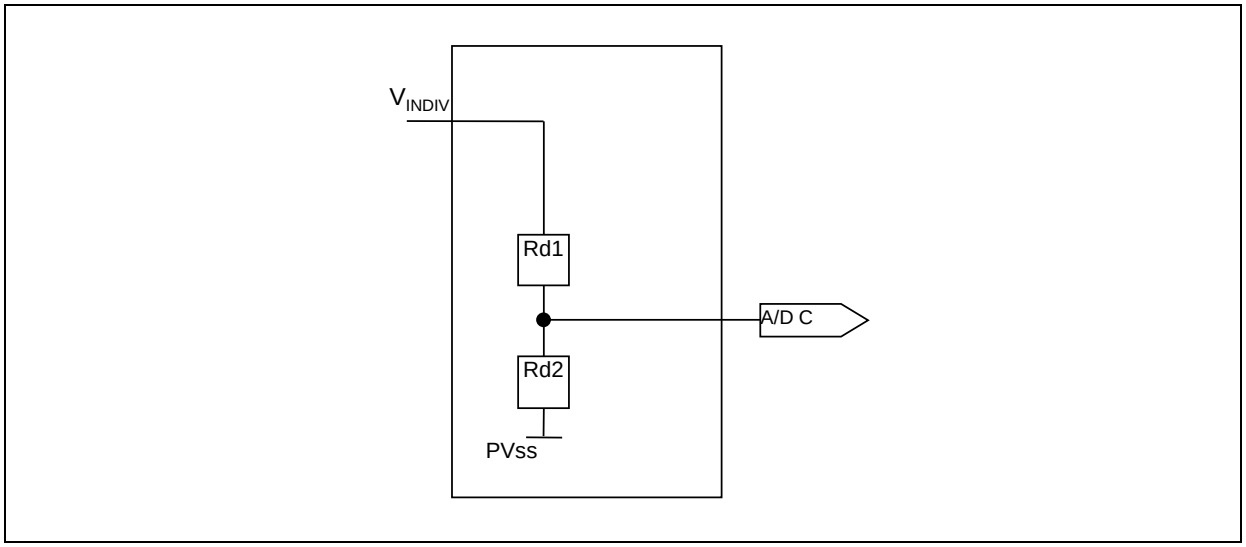
± (V_{INDIV} × (Resistor voltage division ratio error + Voltage error of AV_{CC}) + ((total error of A/D C)/ R_{DIVD}))

For example: the measurement error of input voltage at AV_{CC} = V5C5

Measurement error = ± (V_{INDIV} × (0.009 +0.03) + (5/1024) × 12 × 6)

*2: The SH_n pin is pulled down by combined resistance that composed Sink resistance: RSG of Three-Phase Motor Pre-Driver and Input resistance: R_{PDDIV}.

Block Diagram of Resistor Voltage Divider



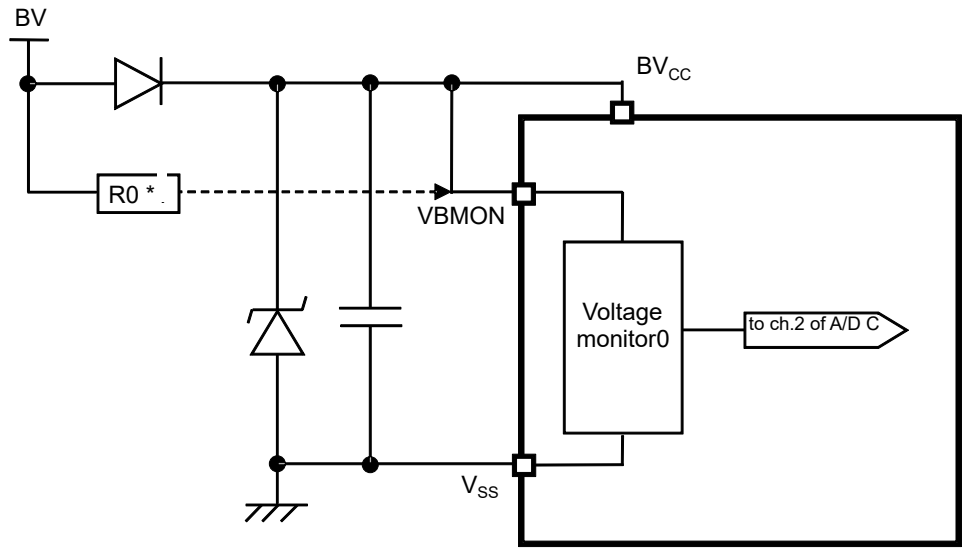
14.9 VB Monitor (VBMON)

Pin Characteristics

(BV_{CC} = 6V to 18V, V_{SS} = PV_{SS} = LV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input voltage	V_{IN}	VBMON	-	3.0	-	BV_{CC}+0.3	V	-
External resistor	R0	VBMON	-14V < BV	1	-	-	kΩ	Needed when connecting BV 1 kΩ (Allowance within ±10%)

Explanatory Diagram



*: Need a series resistor when connecting to BV

14.10 Charge Pump

Pin Characteristics

(BV_{CC} = 6V to 18V, V_{SS} = PV_{SS} = LV_{SS} = 0V, T_A = - 40°C to + 105°C)

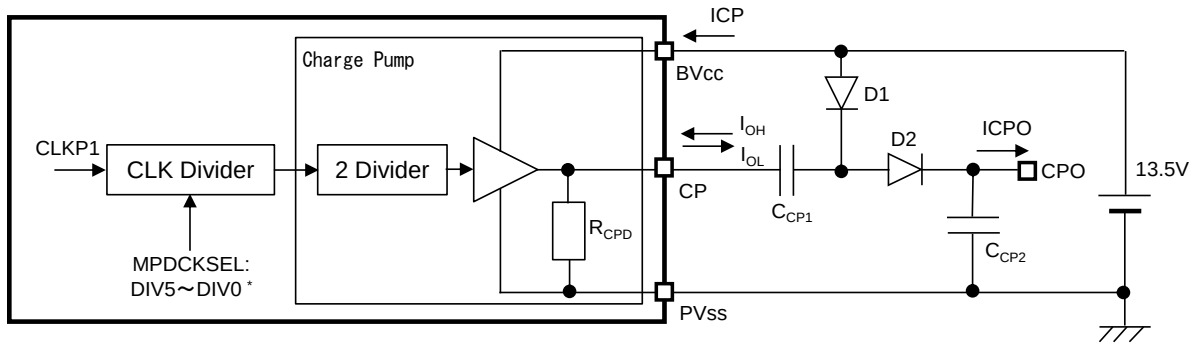
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OHCP}	CP	BV_{CC} =13.5V I_{OH}= -50mA	11	BV_{CC} -0.5	-	V	Schematic Diagram
"L" level output voltage	V_{OLCP}	CP	BV_{CC} =13.5V I_{OL}= +50mA	-	0.7	1.1	V	Schematic Diagram
External capacitance	C_{CP1}	-	-	-	0.022	-	µF	-
	C_{CP2}	-	-	-	0.47	-	µF	
Pull-down resistance value	R_{CPD}	CP	-	45	100	220	kΩ	-
Charge pump voltage*1*2	V_{CPO}	-	ICPO=20mA fCP=500kHz C_{CP1}, C_{CP2}=values shown in this table	9.3	-	-	V	BV_{CC}=6V
				-	24.5	-	V	BV_{CC}= 13.5V
				-	-	33.8	V	BV_{CC}=18V
Output frequency	fCP	CP	BV_{CC} =13.5V	250	500	750	kHz	-
Charge pump output current	ICPO	-	BV_{CC} =13.5V PV_{CC} = BV_{CC} +8V	22	-	-	mA	*1
Charging time	tCP	-	BV_{CC} =13.5V fCP=500kHz C_{CP1}, C_{CP2}=values shown in this table ICPO=0mA	-	0.11	-	ms	Charge time of the external capacitance: C_{CP2} *1
Power supply current	ICP	BV_{CC}	BV_{CC} =13.5V fCP=500kHz C_{CP1}, C_{CP2}=values shown in this table ICPO=0mA	-	4.6	9.3	mA	-

*1: Reference values obtained with simulations in the explanatory diagram for measuring booster characteristics. Because the value varies depending on the external elements, the characteristics are not guaranteed.

*2: The forward voltage of the diode D1 and D2 is the following conditions

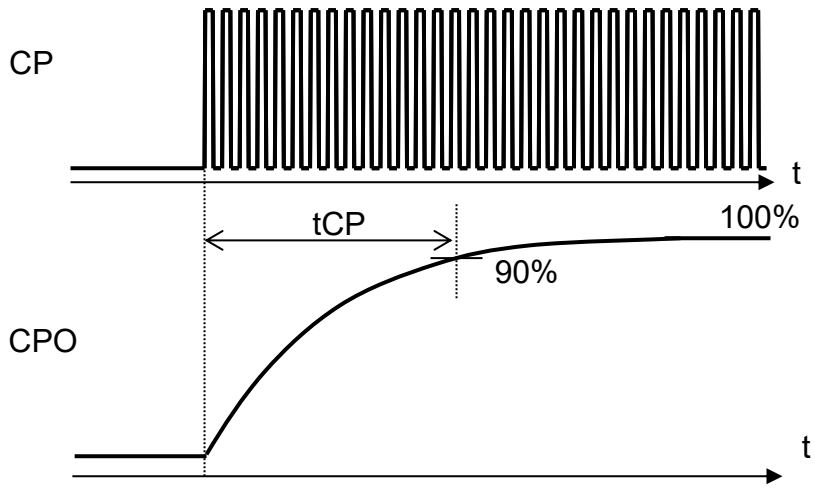
Forward voltage of D1/D2:0.28[V] (Forward current=0.1[A] , T_A = +25°C)

Explanatory Diagram for Measuring booster characteristics



*: MPDCKSEL:DIV5 to DIV0:Charge pump clock divider selection bits

Timing Chart for Charge Pump Operation



14.11 Three-phase Motor Pre-Driver

Pin characteristics

(BV_{CC} = 6V to 18V, V_{SS} = PV_{SS} = LV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OHPD}	GH_0, GH_1, GH_2	PV_{CC} =25V VSH=0V *1 I_{OHGH} = -10mA MPDC2.HSR=111_B/ SSWSDC.HBST=1111_B	8.6	12	15	V	-
		GL_0, GL_1, GL_2	BV_{CC} =13.5V I_{OHGL} = -10mA MPDC2.LSR=111_B/ SSWSDC.LBST=1111_B	8.4	12	14	V	-
"L" level output voltage	V_{OLPD}	GH_0, GH_1, GH_2	PV_{CC} =25V VSH=0V *1 I_{OLGH} = +10mA MPDC2.HSR=111_B/ SSWSDC.HBST=1111_B	-	0.46	1.1	V	-
		GL_0, GL_1, GL_2	BV_{CC} =13.5V I_{OLGL} = +10mA MPDC2.LSR=111_B/ SSWSDC.LBST=1111_B	-	0.53	1.3	V	-
Load capacitance	C_{LPD}	GH_0, GH_1, GH_2	PV_{CC} =25V VSH=0V *1	-	-	12	nF	-
		GL_0, GL_1, GL_2	BV_{CC} =13.5V	-	-	12	nF	-
Gate discharge resistance	R_{GG}	GH_0, GH_1, GH_2, GL_0, GL_1, GL_2	Output disabled	40	100	250	kΩ	-
Sink resistance*3	R_{SG}	SH_0, SH_1, SH_2	-	40	100	250	kΩ	-
Protection resistance	R_S	SH_0, SH_1, SH_2	-	150	-	-	Ω	-
	R_{vmp}	VMPMON	-14V < BV	1	-	-	kΩ	1 kΩ (Allowance within ±10%)

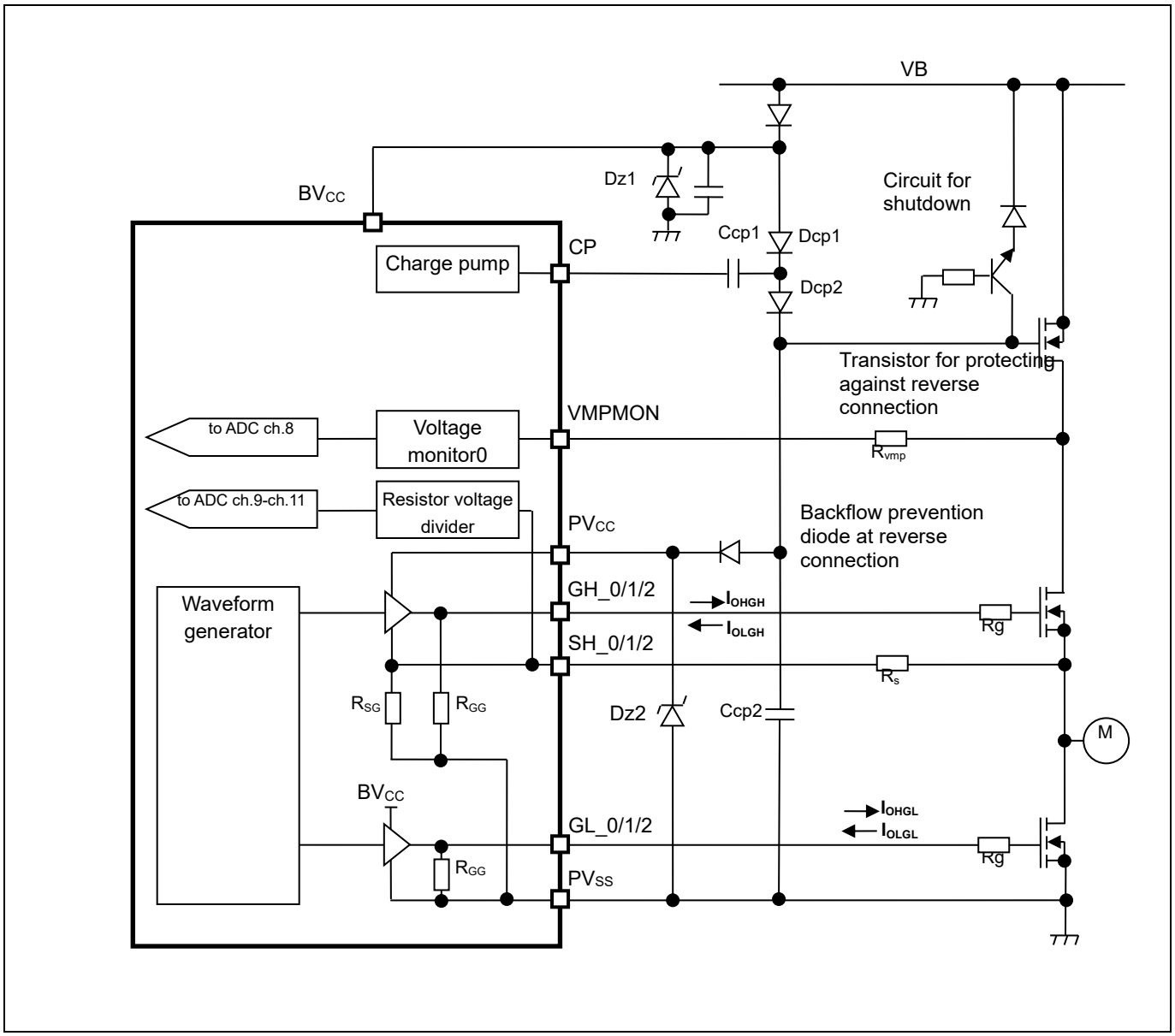
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{HLGD}	PV_{CC}	PV_{CC} =25V VSH=0V *1 C_{LPD}=12nF F_{SW} =20kHz	-	6.3	9.9	mA	*2
			VSH=0V *1 F_{SW} =0kHz I_{OHGH}=0mA I_{OLGH}=0mA	-	3.6	6.3	mA	*2 Fixed output
		BV_{CC}	BV_{CC} =13.5V VSH=0V *1 C_{LPD}=12nF F_{SW} =20kHz	-	6.1	9.8	mA	*2
			VSH=0V *1 F_{SW} =0kHz I_{OHGH}=0mA I_{OLGH}=0mA	-	3.6	6.1	mA	*2 Fixed output

*1: VSH:SH_0, SH_1, SH_2

*2: Current dissipation per driver

*3: The SH_n pin is pulled down by combined resistance that composed Input resistance: R_{PDDIV} of Resistor Voltage Divider and Sink resistance: R_{SG}.

Explanatory Diagram



Output Characteristics

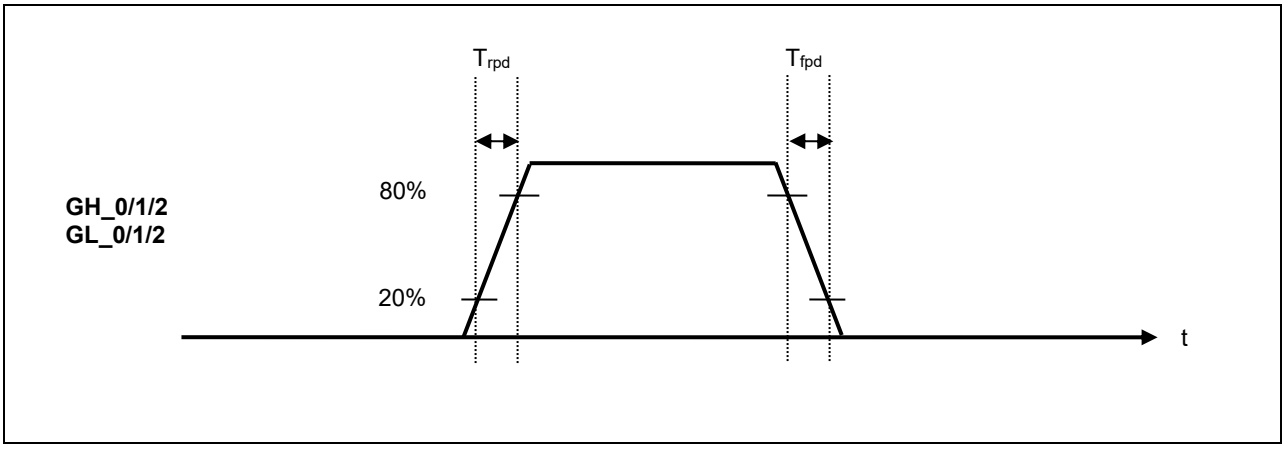
(BV_{CC} = 6V to 18V, V_{SS} = PV_{SS} = LV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Switching frequency	F_{SW}	GH_0, GH_1, GH_2	PV_{CC}=25V C_{CP2}=0.47µF C_{LPD}=12000pF *1	-	-	30	kHz	-
		GL_0, GL_1, GL_2	BV_{CC} =13.5V C_{CP2}=0.47µF C_{LPD} =12000pF *1	-	-	30	kHz	-
Rise time	T_{rpd}	GH_0, GH_1, GH_2	PV_{CC}=25V C_{CP2}=0.47µF C_{LPD} =12000pF *1 MPDC2.HSR=111_B/ SSWSDC.HBST=1111_B	-	1	-	µs	*2
		GL_0, GL_1, GL_2	BV_{CC} =13.5V C_{CP2}=0.47µF C_{LPD} =12000pF *1 MPDC2.LSR=111_B/ SSWSDC.LBST=1111_B	-	1	-	µs	*2
Fall time	T_{fpd}	GH_0, GH_1, GH_2	PV_{CC} =25V C_{CP2}=0.47µF C_{LPD} =12000pF *1 MPDC2.HSR=111_B/ SSWSDC.HBST=1111_B	-	1	-	µs	*2
		GL_0, GL_1, GL_2	BV_{CC} =13.5V C_{CP2}=0.47µF C_{LPD} =12000pF *1 MPDC2.LSR=111_B/ SSWSDC.HBST=1111_B	-	1	-	µs	*2

*1: C_{LPD}: Load capacitance of each pin: GH_0, GH_1, GH_2, GL_0, GL_1, GL_2

*2: Reference value obtained with simulations. Because the value depends on external environments, the output characteristics are not guaranteed.

Timing Chart



14.12 12V Power Supply Output

(BV_{CC} = 6V to 18V, V_{SS} = PV_{SS} = LV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
12V power supply output voltage	V_{O12VSW}	V12SW	I_{O12}=30mA	BV_{CC}-0.5	-	BV_{CC}	V	-
12V power supply output current	I_{O12}	V12SW	-	-	-	30	mA	-

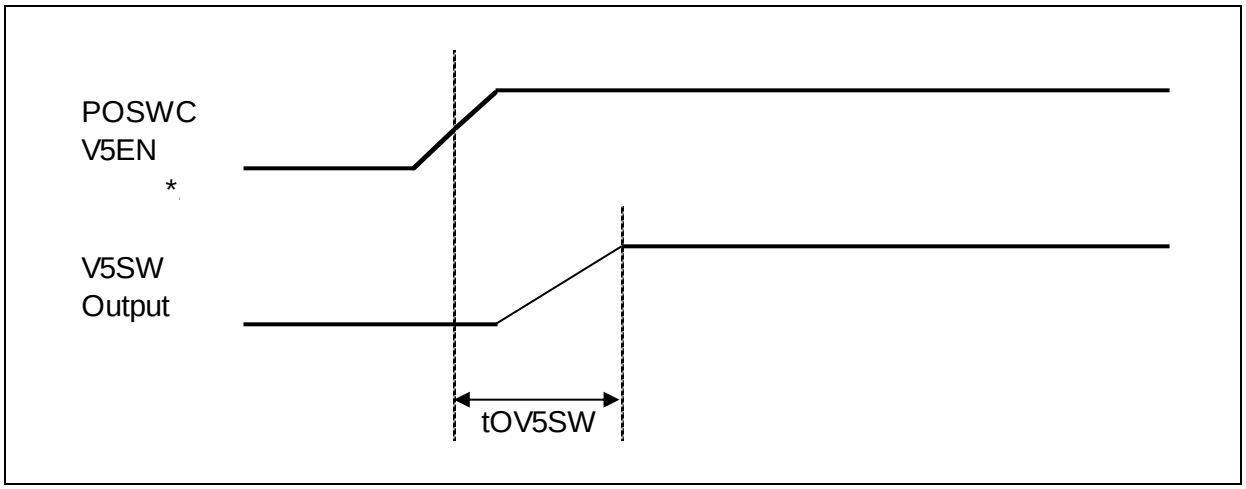
14.13 5V Power Supply Output

(BV_{CC} = 6V to 18V, V_{SS} = PV_{SS} = LV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
V5SW power supply output voltage	V_{O5VSW}	V5SW	I_{OV5SW}=25mA	4.85	5	5.15	V	-
V5SW power supply output current *	I_{OV5SW}	V5SW	-	-	-	25	mA	-
V5SW power supply output stabilization time	t_{OV5SW}	V5SW	I_{OV5SW}=0mA	-	760	1800	µs	
V5C5 output voltage	V_{OV5C5}	V5C5	I_{OV5C5}=25mA	4.85	5	5.15	V	-
V5C5 output current *	I_{OV5C5}	V5C5	-	-	-	25	mA	Except internal consumption current and current into AV_{CC}

*: See "Absolute Maximum Ratings for 5Vsupply average overall output current (ΣI_{OV5}=I_{OV5SW}+I_{OV5C5})

Timing Chart of V5SW Power Supply Output



*: POSWC-V5EN: V5SW output control bit

14.14 Connection Pins for Smoothing Capacitor

(BV_{CC} = 6V to 18V, V_{SS} = PV_{SS} = LV_{SS} = 0V, T_A = - 40°C to + 105°C)

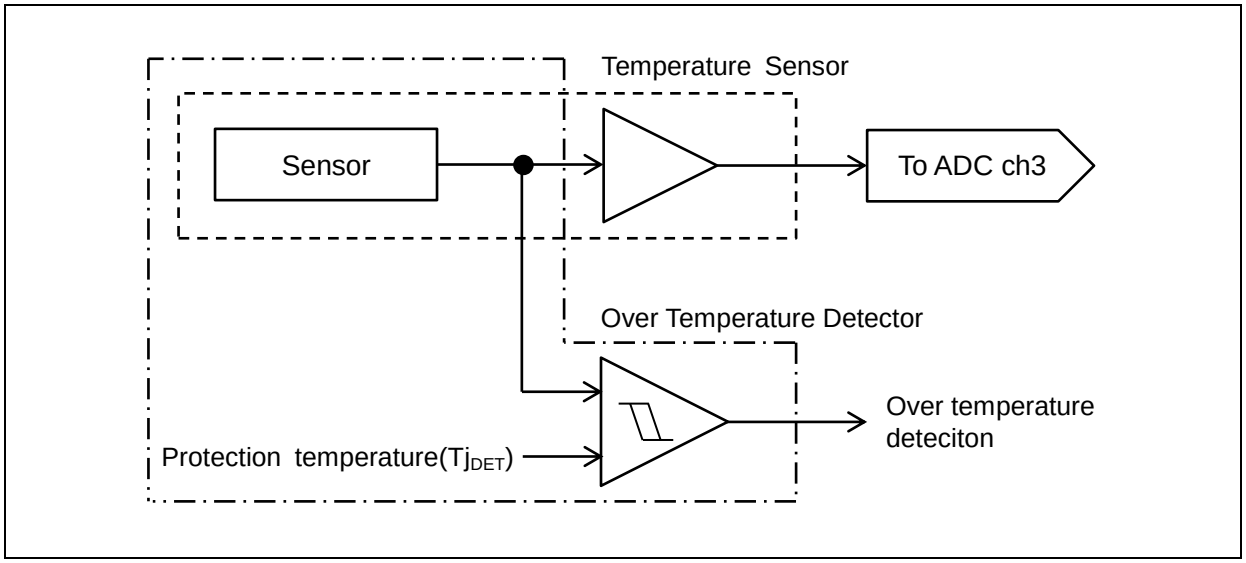
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
5Vpower supply stabilized output pin voltage	V_{C5}	V5C5, C5	I_O=0mA	4.85	5	5.15	V	-
1.8Vpower supply stabilized output pin voltage	V_{C1}	C1	RSTX="L" I_O=0mA	1.65	1.8	1.95	V	-

14.15 Over-Temperature Detector

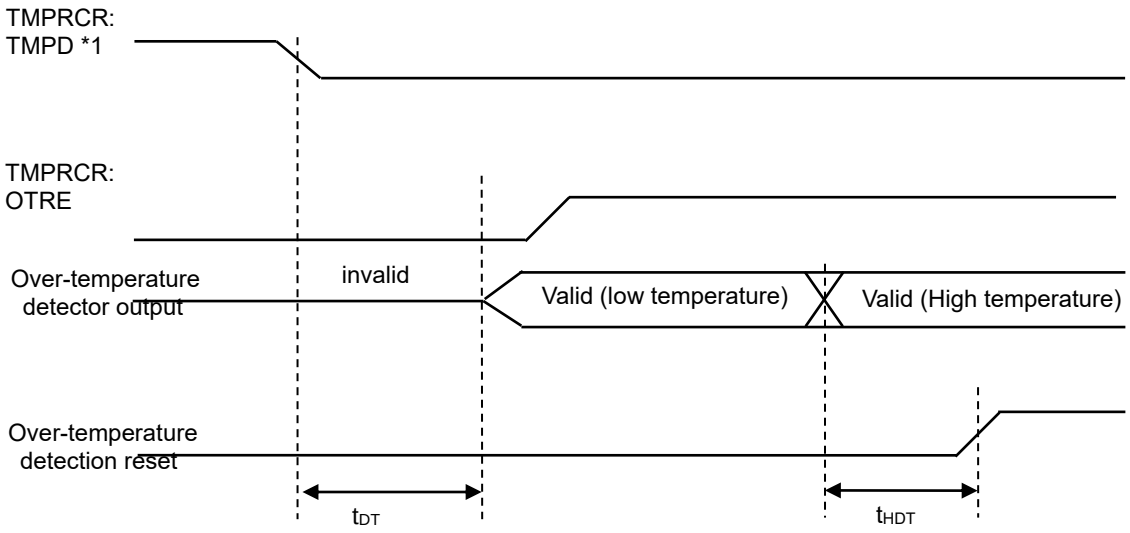
(BV_{CC} = 6V to 18V, V_{SS} = PV_{SS} = LV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Protection temperature	Tj_{DET}	-	142	146	150	°C	-
Recovery temperature	Tj_{CNL}	-	135	140	145	°C	-
Temperature hysteresis	Tj_{HYS}	-	5	6	7	°C	-
Stabilization time	t_{DT}	-	-	-	200	µs	-
Over-temperature detection filtering time	t_{HDT2}	TMPRCR:TMFT=10_B	-	1	-	µs	-
	t_{HDT1}	TMPRCR:TMFT=01_B	-	5	-	µs	-
	t_{HDT0}	TMPRCR:TMFT=00_B	-	15	-	µs	Initial value
	t_{HDT3}	TMPRCR:TMFT=11_B	-	30	-	µs	-
Power supply current	I_{OTD}	TMPRCR:TMPD=0	-	0.25	7.1	µA	-

Block Diagram of Temperature Sensor and Over-Temperature Detector

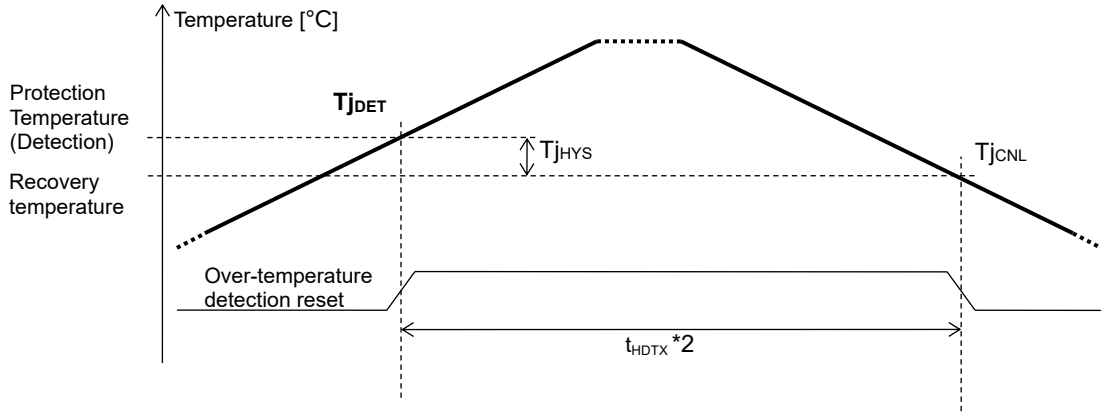


Timing Chart of Over-Temperature Detector



*1: TMPRCR:TMPD: Over-temperature Detector Disable

If Junction temperature ≥ Protection temperature then Over-temperature detection reset = H-level
If Junction temperature < Protection temperature then Over-temperature detection reset = L-level



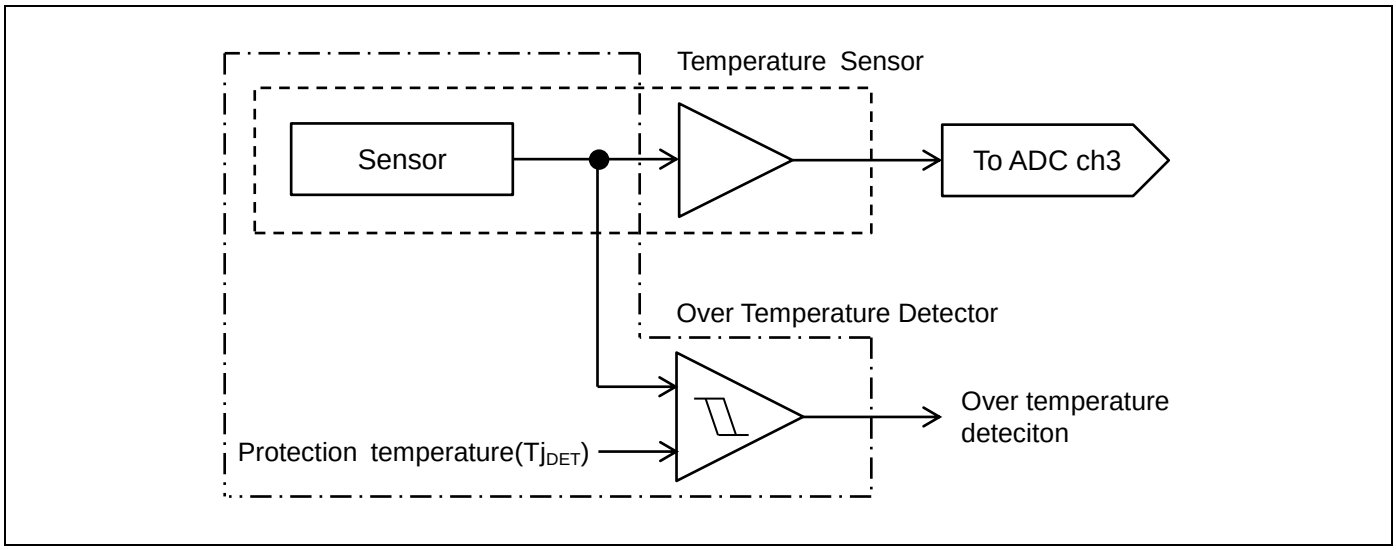
*2: t_{HDTX} : Temperature rise (momentary temperature rise) cannot be detected if they occur during the time interval shorter than this filtering time.

14.16 Temperature Sensor

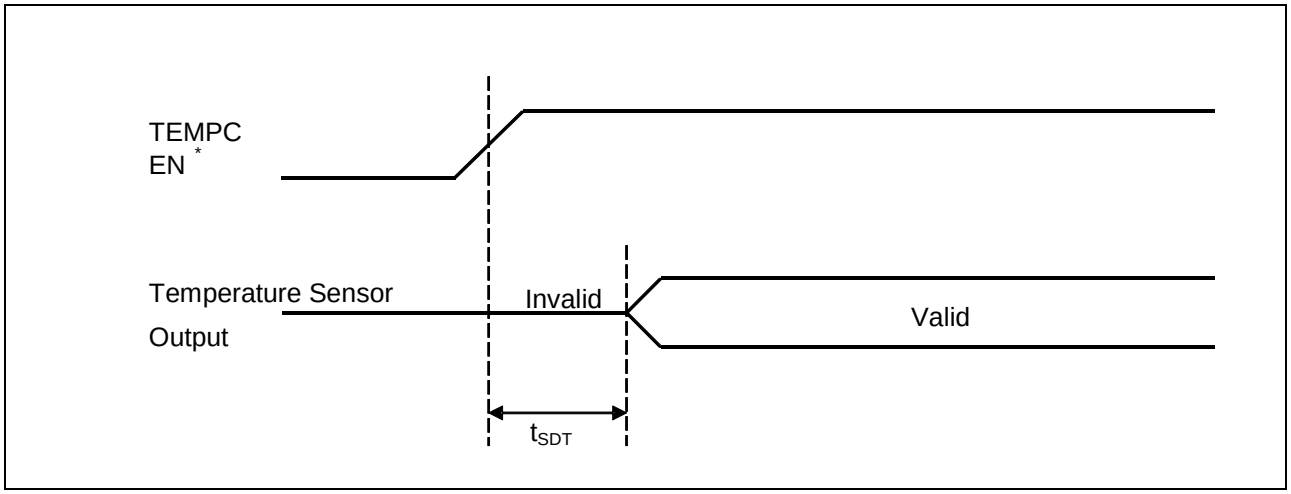
(BV_{CC} = 6V to 18V, V_{SS} = PV_{SS} = LV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Temperature detection range	Tj_{RNG}	-	-	-40	-	+150	°C	-
Temperature detection Error	Tj_{EMA}	-	Tj = +25°C	-14	-	+14	°C	-
Temperature sensor stabilization time	t_{SDT}	-	-	-	-	50	µs	-
Power supply current	I_{TMP}	BV_{CC}	-	-	1	2.4	mA	Temperature sensor in operation

Block Diagram of Temperature Sensor and Over-Temperature Detector



Timing Chart of Temperature Sensor



*: TEMPC:EN: Temperature sensor control bit

14.17 Low Voltage Detection Function Characteristics

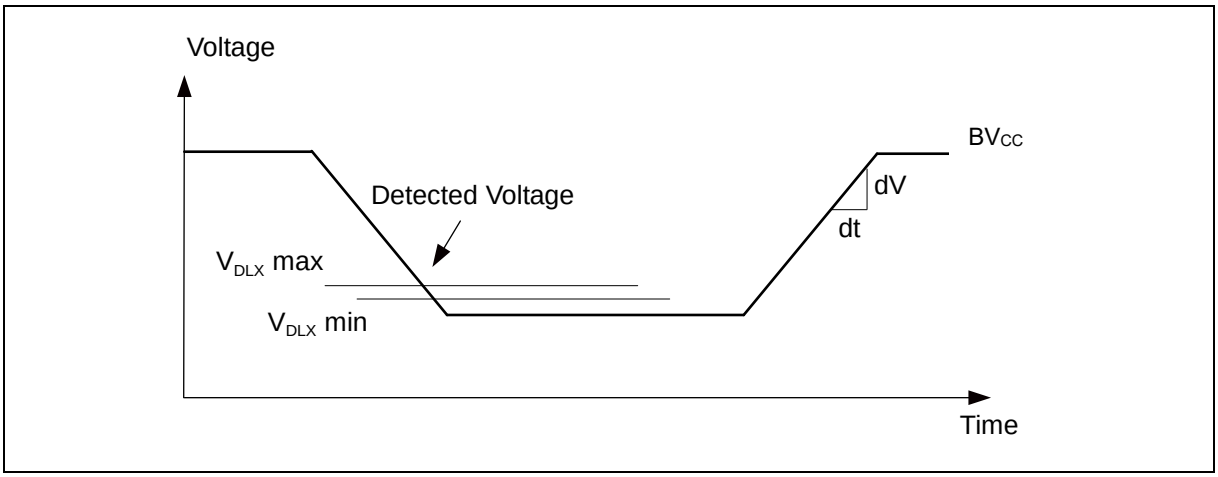
(BV_{CC} = 4.08V to 18V, V_{SS} = PV_{SS} = LV_{SS} = 0V, T_A = - 40°C to + 105°C)

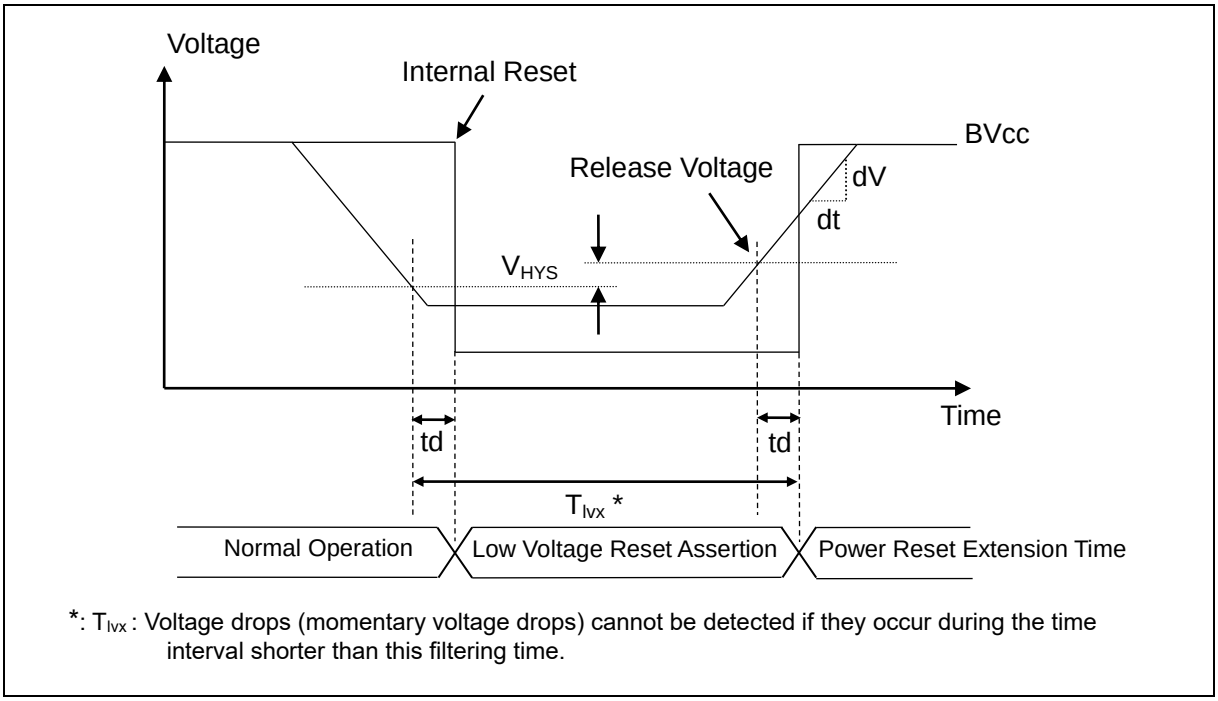
Parameter	Symbol	Conditions	Value(BV_{CC})			Unit	Remarks
			Min	Typ	Max		
Detected voltage (BV_{CC})*1, *3	V_{DL3}	CILCR:LVL = 11_B	4.08	4.20	4.32	V	-
	V_{DL0}	CILCR:LVL = 00_B	4.38	4.50	4.62	V	Initial value
	V_{DL1}	CILCR:LVL = 01_B	4.58	4.70	4.82	V	-
Power supply voltage change rate*2	dV/dt	-	- 0.004	-	+ 0.004	V/µs	-
Hysteresis width	V_{HYS}	-	0.29	0.30	0.31	V	-
Stabilization time	$T_{LVDSTAB}$	-	-	-	140	µs	-
Detection delay time	t_d	dV/dt= -4mV/µs -	-	-	5	µs	Except for filtering time
Low-voltage detection filtering time	T_{lv2}	CILCR:LVFT=10_B	-	1	-	µs	-
	T_{lv1}	CILCR:LVFT=01_B	-	5	-	µs	-
	T_{lv0}	CILCR:LVFT=00_B	-	15	-	µs	Initial value
	T_{lv3}	CILCR:LVFT=11_B	-	30	-	µs	-

*1: If the power supply voltage fluctuates within the time less than the detection delay time (td), there is a possibility that the low-voltage detection will occur or stop after the power supply voltage passes the detection range.

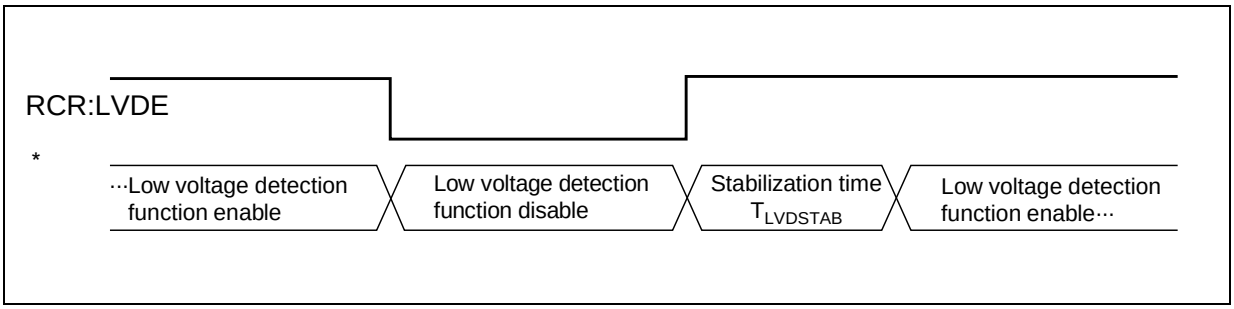
*2: In order to perform the low-voltage detection at the detection voltage (V_{DLX}), be sure to suppress fluctuation of the power supply voltage within the limits of the change ration of power supply voltage.

*3: Setting the condition, CILCR:LVL=10_B, is prohibited.





*: T_{Ivx} : Voltage drops (momentary voltage drops) cannot be detected if they occur during the time interval shorter than this filtering time.



*: RCR:LVDE: Low Voltage Detector Enable Bit

14.18 LIN Transceiver

(BV_{CC} = 7V to 18V, V_{SS} = PV_{SS} = LV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin Name	Conditions	Value(BV_{CC})			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{LINTR}	BV_{CC}	LINTRC.XLDPD=1 LINTRC.XLRPD=1 SOT2=0	-	2.5	5.4	mA	BV_{CC}=13.5V Drive dominant state
	I_{LINSLP}		LIN=OPEN LINTRC.XLDPD=0 LINTRC.XLRPD=1 LINTRC.PURSEL=1	-	-	11	µA	T_A=+25°C BV_{CC}=13.5V
				-	-	100	µA	T_A=+105°C
Pull-up resistance value	R_{LINPU}	LIN	LINTRC.PURSEL=1	20	30	60	kΩ	-
			LINTRC.PURSEL=0	180	300	520	kΩ	-
"L" level output current	I_{OLLIN}	LIN	LIN=BV_{CC}=18V	40	-	200	mA	-
Input leakage current receiver recessive state	I_{LINIL_REC}	LIN	7V≤LIN≤18V BV_{CC}≤ LIN SOT2=1	-	-	20	µA	-
Input leakage current receiver dominant state	I_{LINIL_DOM}	LIN	LIN=0V BV_{CC}=13.5V SOT2=1	-1	-	-	mA	-
Input leakage current disconnected from ground	I_{LINIL_GND}	LIN	BV_{CC}=V_{SS}=18V LIN=0V	-1	-	+1	mA	-
Input leakage current BV_{CC} disconnected	I_{LINIL_BV}	LIN	BV_{CC}=V_{SS}=0V LIN=18V	-	-	100	µA	-
recessive output voltage	V_{OLINR}	LIN	SOT2=1 BV_{CC}=7.0V	BV_{CC} × 0.78	-	BV_{CC}	V	-
dominant output voltage	V_{OLIND}	LIN	SOT2=0 BV_{CC}=7.0V	V_{SS}	-	1.6	V	-
recessive input voltage	V_{IREC}	LIN	-	BV_{CC} × 0.6	-	-	V	-
dominant input voltage	V_{IDOM}	LIN	-	-	-	BV_{CC} × 0.4	V	-
central voltage of receiver threshold	V_{CNTRX}	LIN	-	BV_{CC} × 0.475	BV_{CC} × 0.500	BV_{CC} × 0.525	V	*1
Hysteresis voltage of receiver threshold	V_{HYSRX}	LIN	-	-	-	BV_{CC} × 0.175	V	*2
stabilization time	t_{LDT}	-	-	-	-	70	µs	-
Pull-up resistance value for master node	$R_{LINMSTR}$	LIN	-	900	1000	1100	Ω	-

Parameter	Symbol	Pin Name	Conditions	Value(BV_{CC})			Unit	Remarks
				Min	Typ	Max		
Duty cycle 1 *4	$D1_{LINTX}$	LIN	tbit=50µs	0.396	-	-	-	= tbus_rec_min /(2×tbit) VTHRX1_REC =0.744×BV_{CC} VTHRX1_DOM =0.581× BV_{CC}
Duty cycle 2 *4	$D2_{LINTX}$	LIN	tbit=50µs BV_{CC}=7.6V to 18V	-	-	0.581	-	= tbus_rec_max /(2×tbit) VTHRX2_REC =0.422×BV_{CC} VTHRX2_DOM =0.284×BV_{CC}
Duty cycle 3 *4 *5	$D3_{LINTX}$	LIN	tbit=96µs	0.417	-	-	-	= tbus_rec_min /(2×tbit) VTHRX1_REC =0.778×BV_{CC} VTHRX1_DOM =0.616×BV_{CC}
Duty cycle 4 *4 *5	$D4_{LINTX}$	LIN	tbit=96µs BV_{CC}=7.6V to 18V	-	-	0.590	-	= tbus_rec_max /(2×tbit) VTHRX2_REC =0.389×BV_{CC} VTHRX2_DOM =0.251×BV_{CC}
Propagation delay of receiver	t_{rx_pd}	- (SIN2)	-	-	-	6	µs	-
Symmetry of receiver propagation delay	t_{rx_sym}	- (SIN2)	-	-2	-	2	µs	= $t_{rx\_pd(raising)}$ - $t_{rx\_pd(falling)}$
Input capacitance	C_{LININ}	LIN	-	-	-	100	pF	-

*1:V_{CNTRX} = (Vth_dom + Vth_rec)/2 *3

*2:V_{HYSRX} = Vth_rec – Vth_dom *3

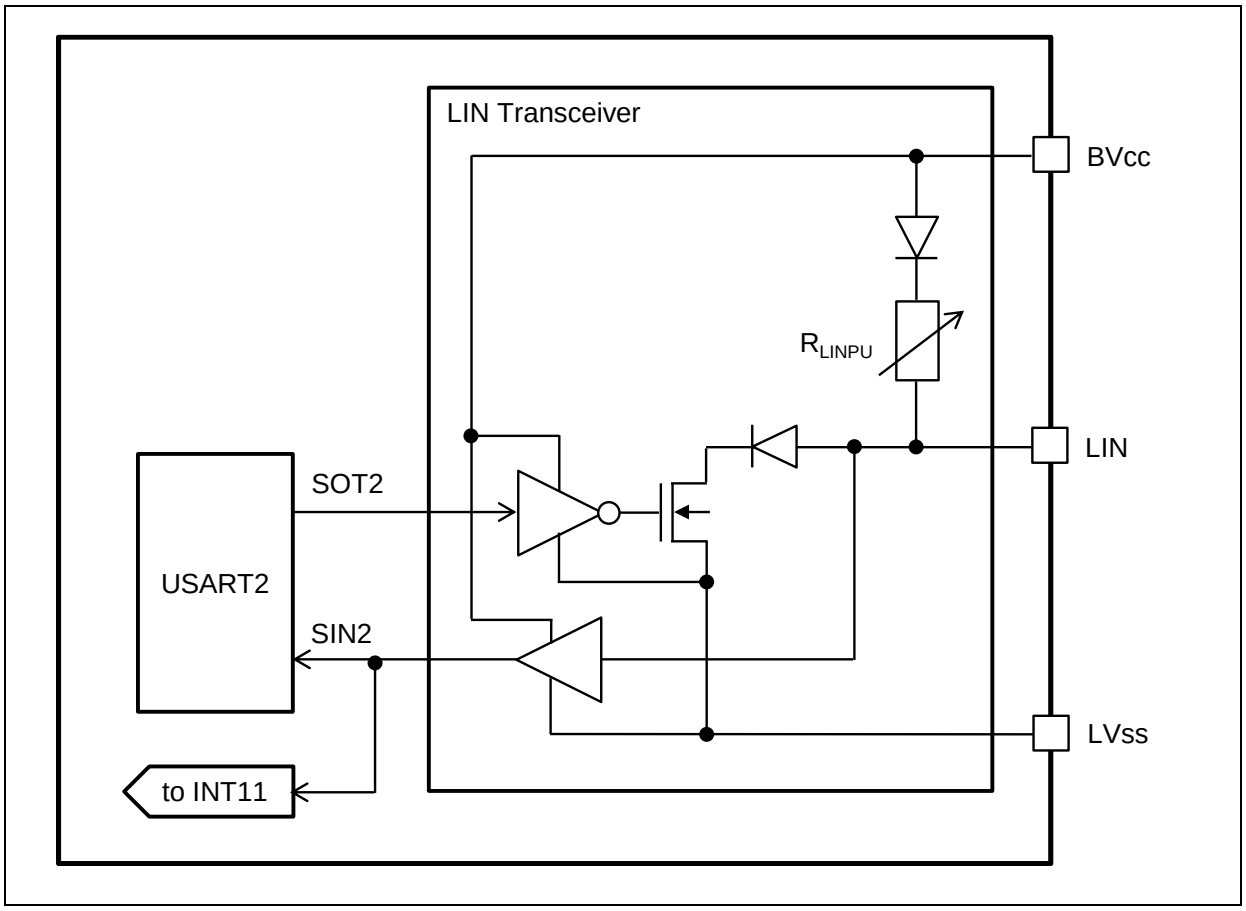
*3:Vth_dom: receiver threshold of the recessive to dominant LIN bus edge.

Vth_rec: receiver threshold of the dominant to recessive LIN bus edge.

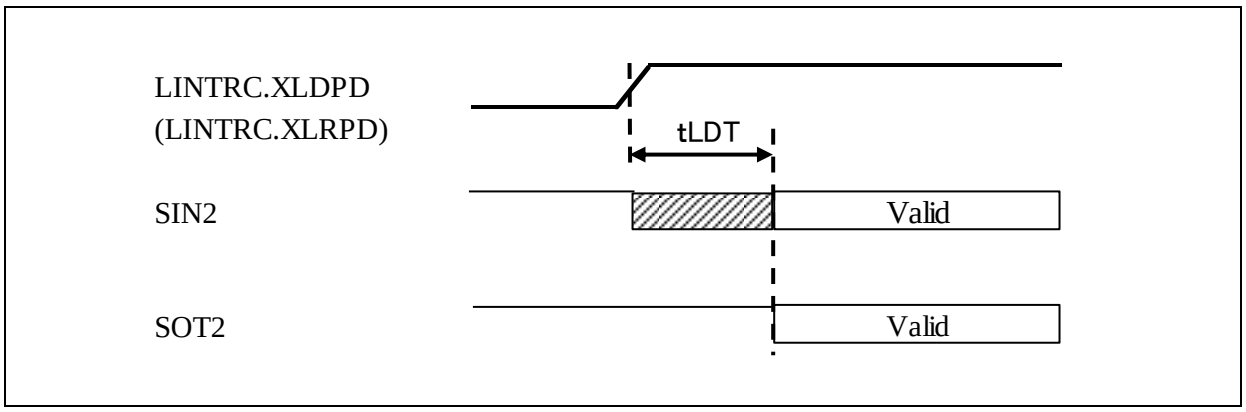
*4: Bus load conditions (CBUS / RBUS): 1nF/1kΩ, 6.8nF/660Ω, 10nF/500Ω.

*5: For reference purpose only

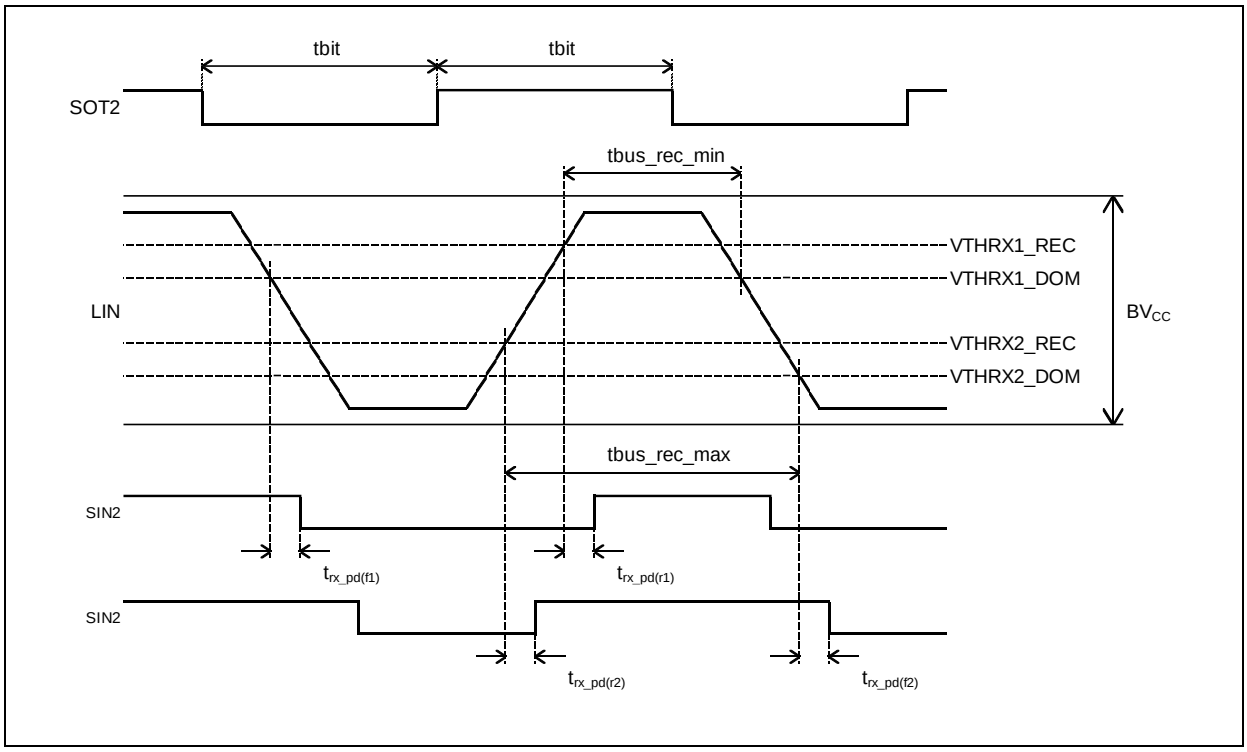
Block Diagram of LIN Transceiver



Timing Chart of Stabilization time



Timing Chart of LIN Transceiver



14.19 Flash Memory Write/Erase Characteristics

(BV_{CC} = 6V to 18V, V_{SS} = PV_{SS} = LV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter		Value			Unit	Conditions	Remarks
		Min	Typ	Max			
Sector erase time	Large Sector	-	1.6	7.5	s	$T_A \leq$ + 80°C	Includes write time prior to internal erase.
	Small Sector	-	0.4	2.1	s	-	
	Security Sector	-	0.31	1.65	s	-	
Word (16-bit) write time	Large Sector	-	25	400	µs	$T_A \leq$ + 80°C	Not including system-level overhead time.
	Small Sector	-	25	400	µs	-	
Chip erase time		-	5.1	25.05	s	$T_A \leq$ + 80°C	Includes write time prior to internal erase.

Note: While the Flash memory is written or erased, shutdown of the external power (BV_{CC}) is prohibited. In the application system where the external power might be shut down while writing or erasing, be sure to turn the power off by using a low voltage detection function.

To put it concrete, change the external power in the range of change ration of power supply voltage (-0.004V/µs to +0.004V/µs) after the external power falls below the detection voltage (VDLX)*1

Write/Erase cycles and data hold time

Write/Erase Cycles (cycle)	Data Hold Time (year)
1,000	20 *2
10,000	10 *2
100,000	5 *2

*1: See " Low Voltage Detection Function Characteristics".

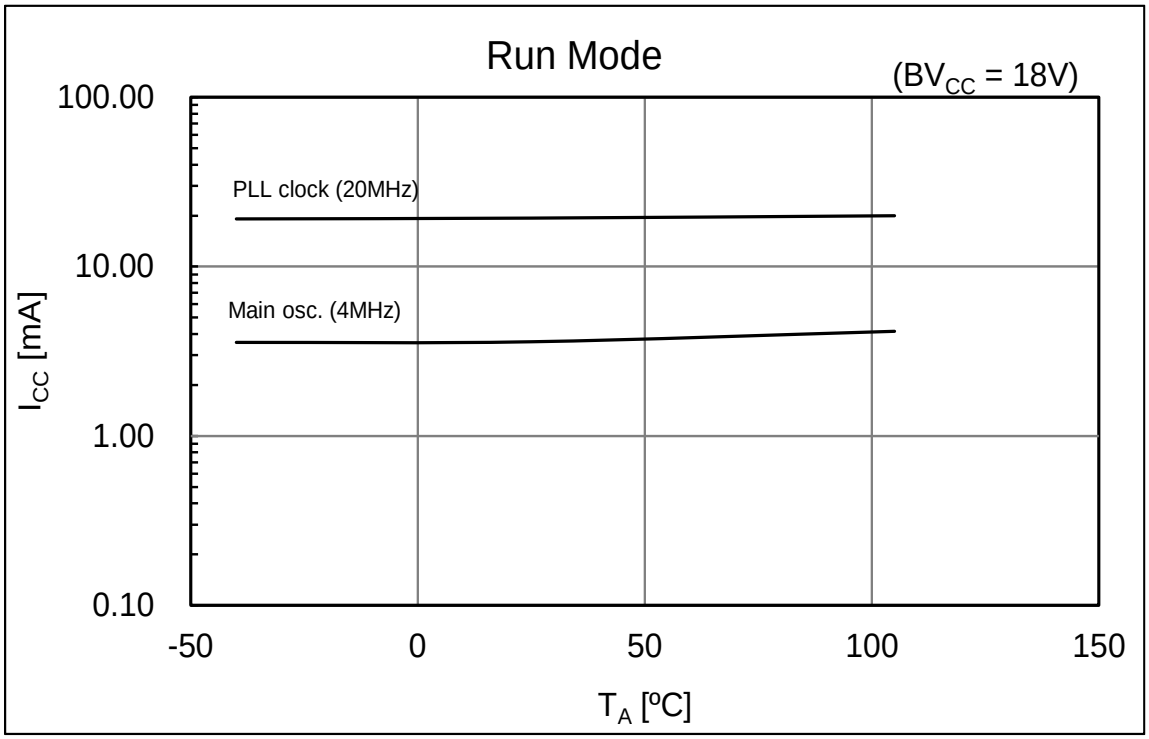
*2: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

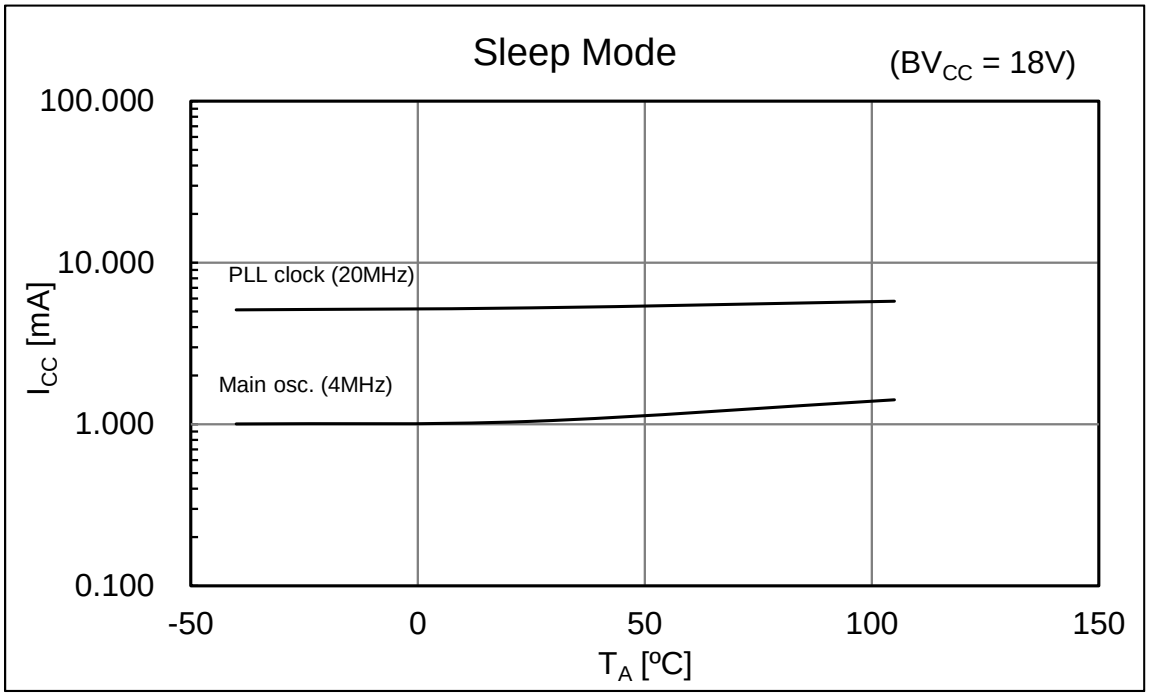
15. Example Characteristics

■ Power supply current

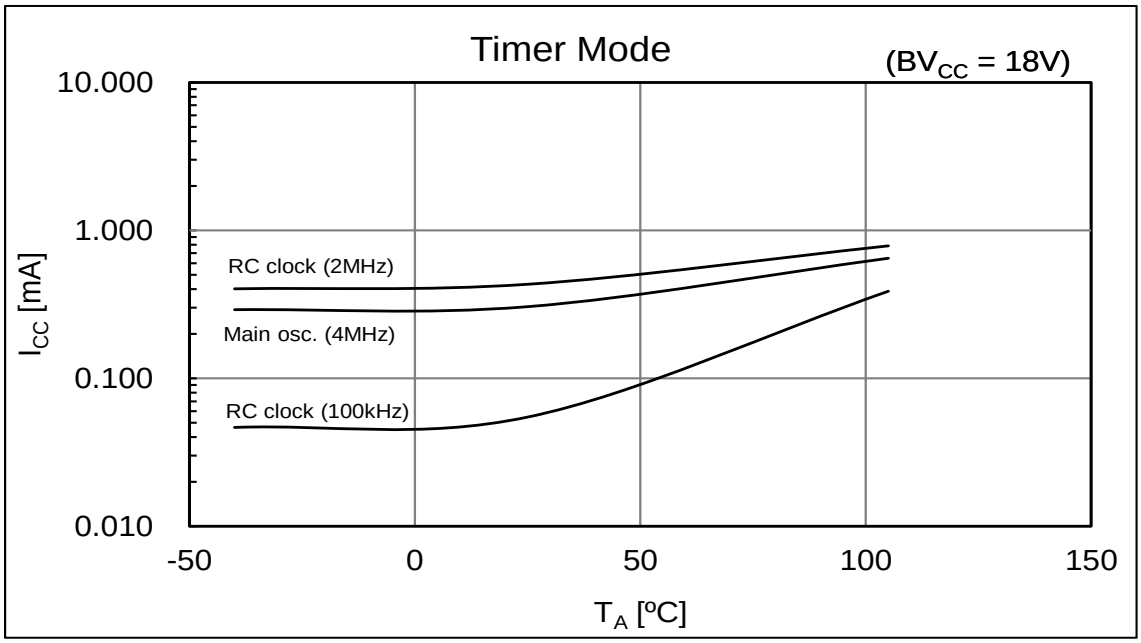
This characteristic is an actual value of the arbitrary sample. It is not the guaranteed value.

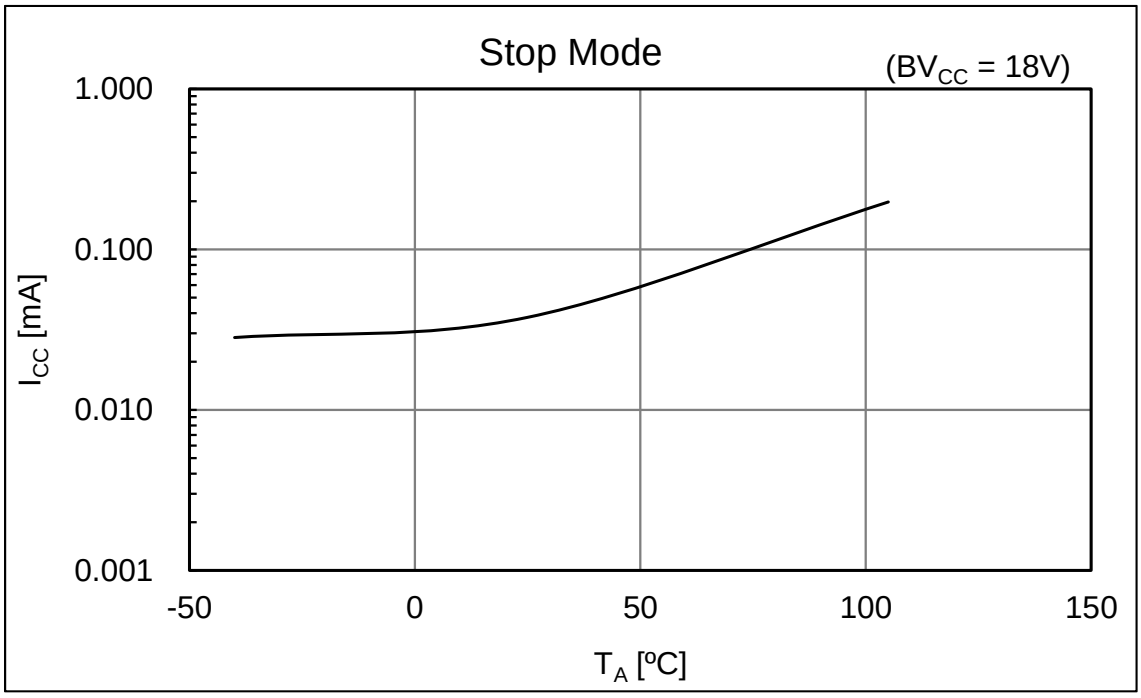
CY96F8D5K



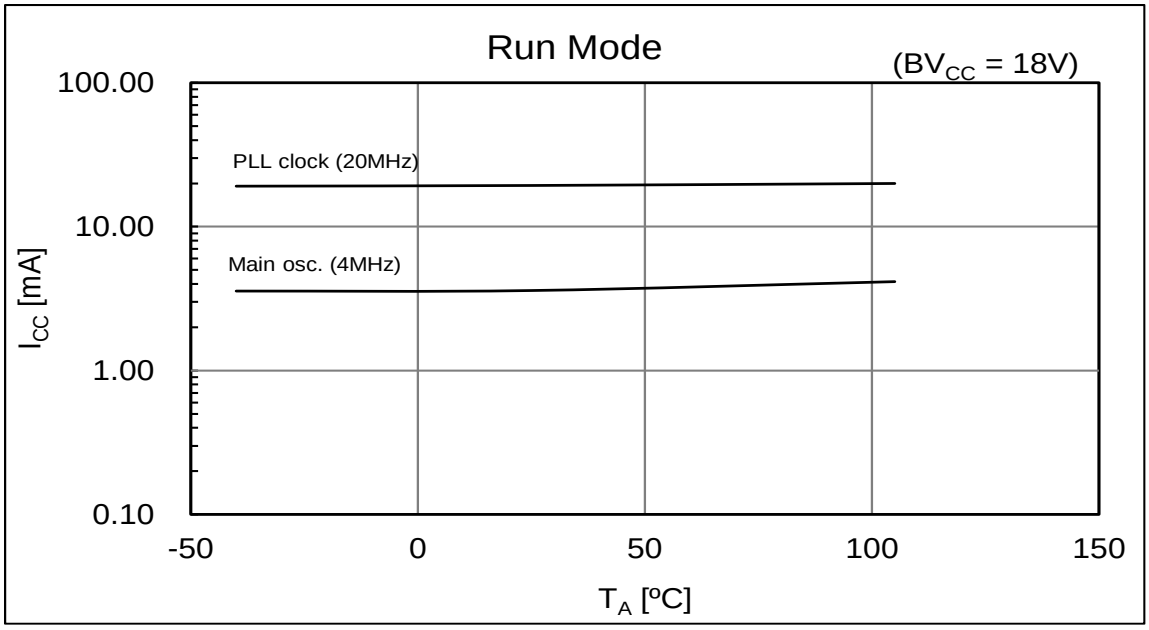


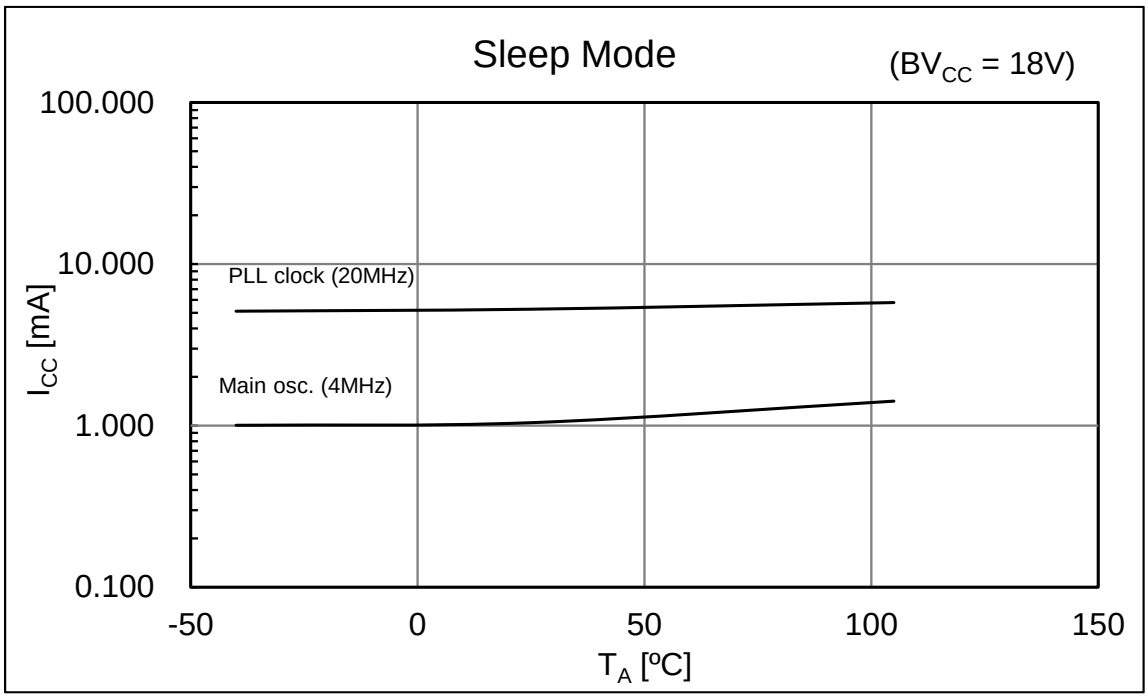
CY96F8D5K


Timer Mode
(BVCC = 18V)
10.000
1.000
0.100
0.010
ICC [mA]
RC clock (2MHz)
Main osc. (4MHz)
RC clock (100kHz)
-50
0
50
100
150
TA [ºC]

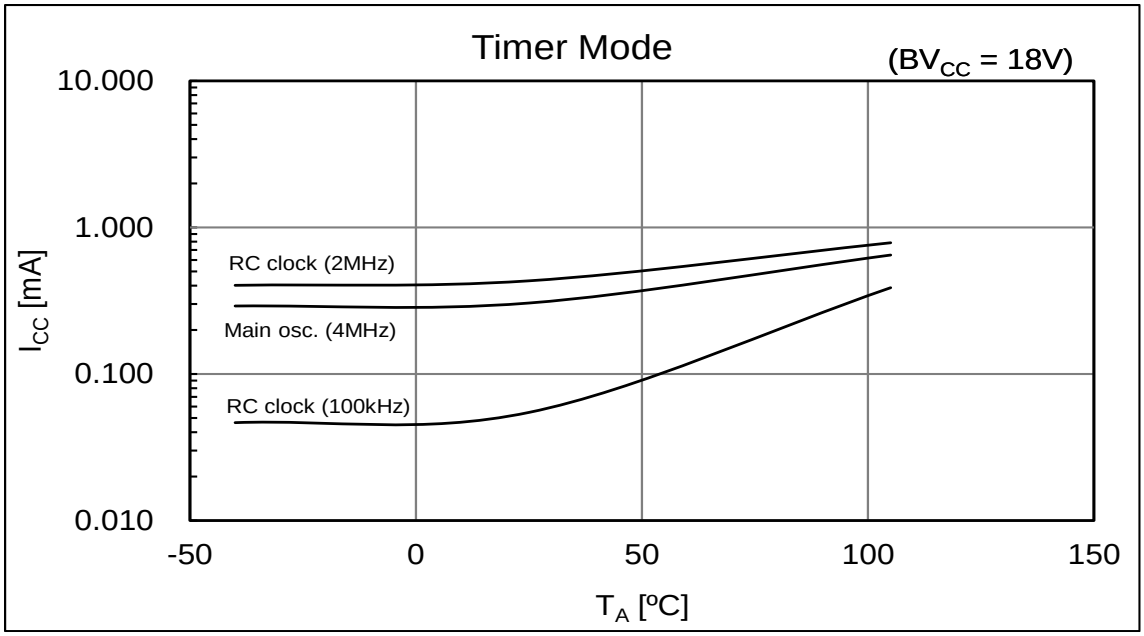

Stop Mode
(BVCC = 18V)
1.000
0.100
0.010
0.001
ICC [mA]
-50
0
50
100
150
TA [ºC]

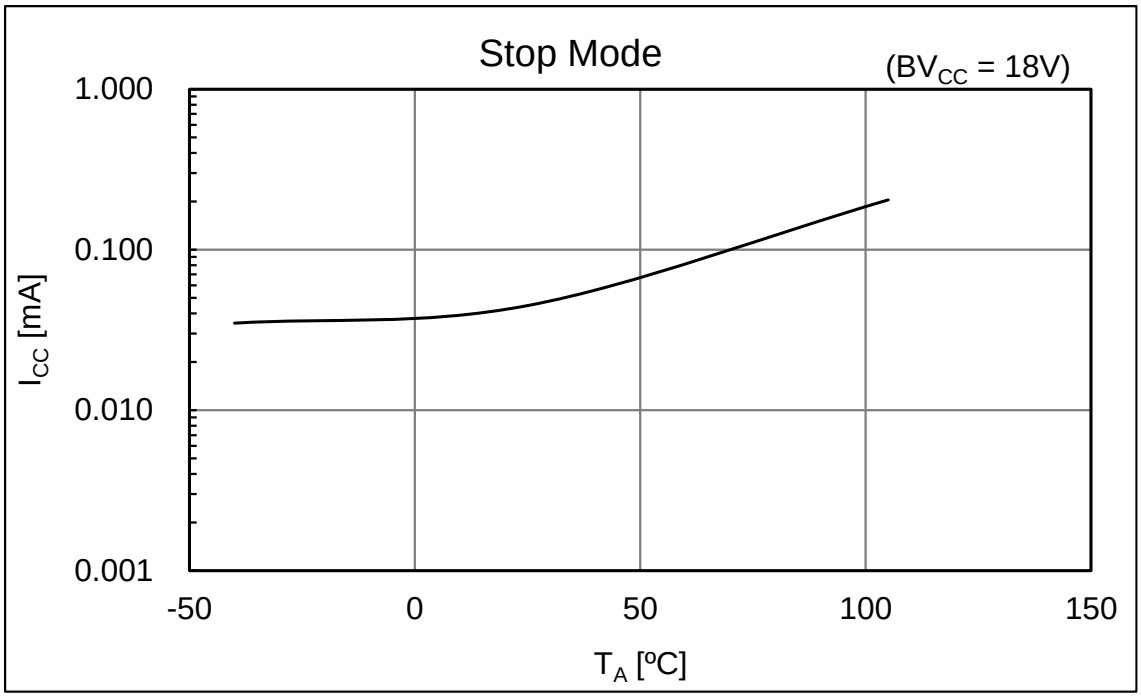
CY96F8E5K


Run Mode
(BVCC = 18V)
100.00
10.00
1.00
0.10
PLL clock (20MHz)
Main osc. (4MHz)
ICC [mA]
-50
0
50
100
150
TA [ºC]


Sleep Mode
(BVCC = 18V)
100.000
10.000
1.000
0.100
PLL clock (20MHz)
Main osc. (4MHz)
ICC [mA]
-50
0
50
100
150
TA [ºC]

CY96F8E5K


Timer Mode
(BVCC = 18V)
10.000
1.000
0.100
0.010
ICC [mA]
RC clock (2MHz)
Main osc. (4MHz)
RC clock (100kHz)
-50
0
50
100
150
TA [ºC]


Stop Mode
(BVCC = 18V)
1.000
0.100
0.010
0.001
ICC [mA]
-50
0
50
100
150
TA [ºC]

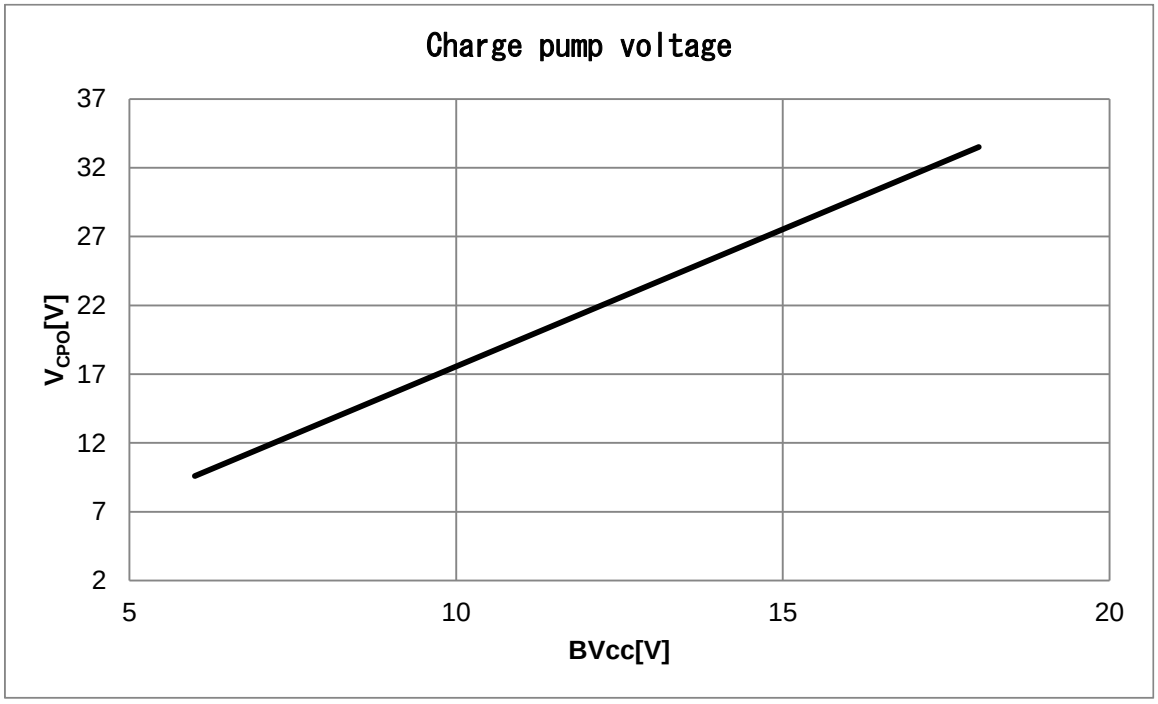
■ Used setting

Mode	Selected Source Clock	Clock/Regulator and FLASH Settings
Run mode	PLL	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 20MHz
	Main osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 4MHz
Sleep mode	PLL	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 20MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	Main osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 4MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
Timer mode	Main osc.	CLKMC = 4MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	RC clock fast	CLKRC = 2MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	RC clock slow	CLKRC = 100kHz (System clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode
Stop mode	stopped	(All clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode

■ Charge pump voltage

Reference values obtained with simulations. It is not the guaranteed value.

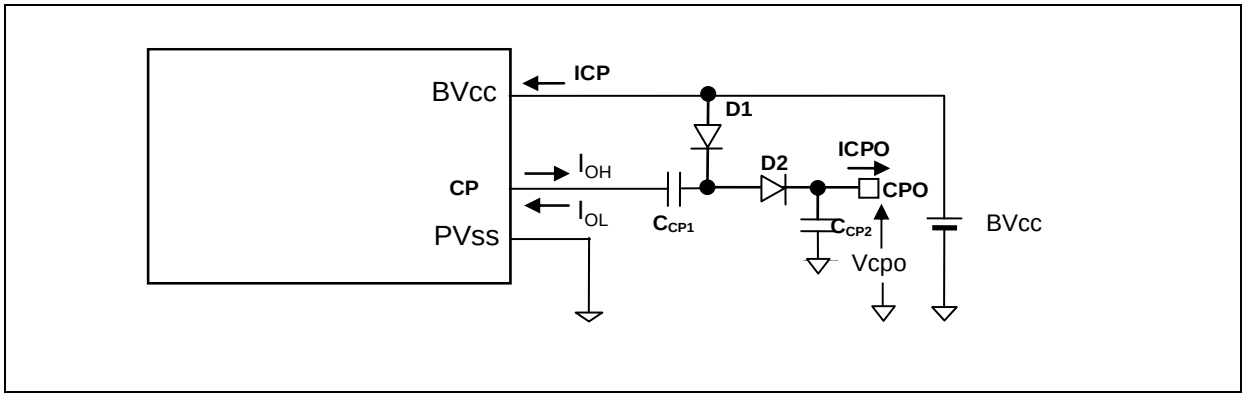
(V_{SS} = PV_{SS} = LV_{SS} = 0V, T_A = - 40°C to + 105°C)



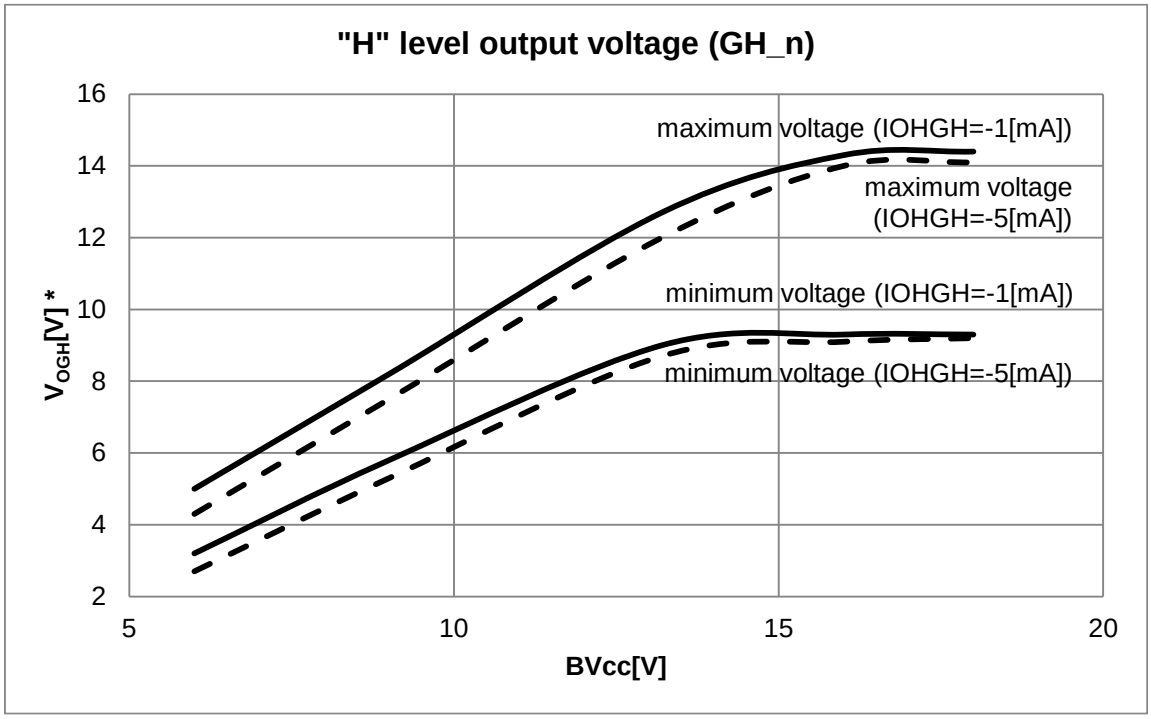
■ Condition of a simulation

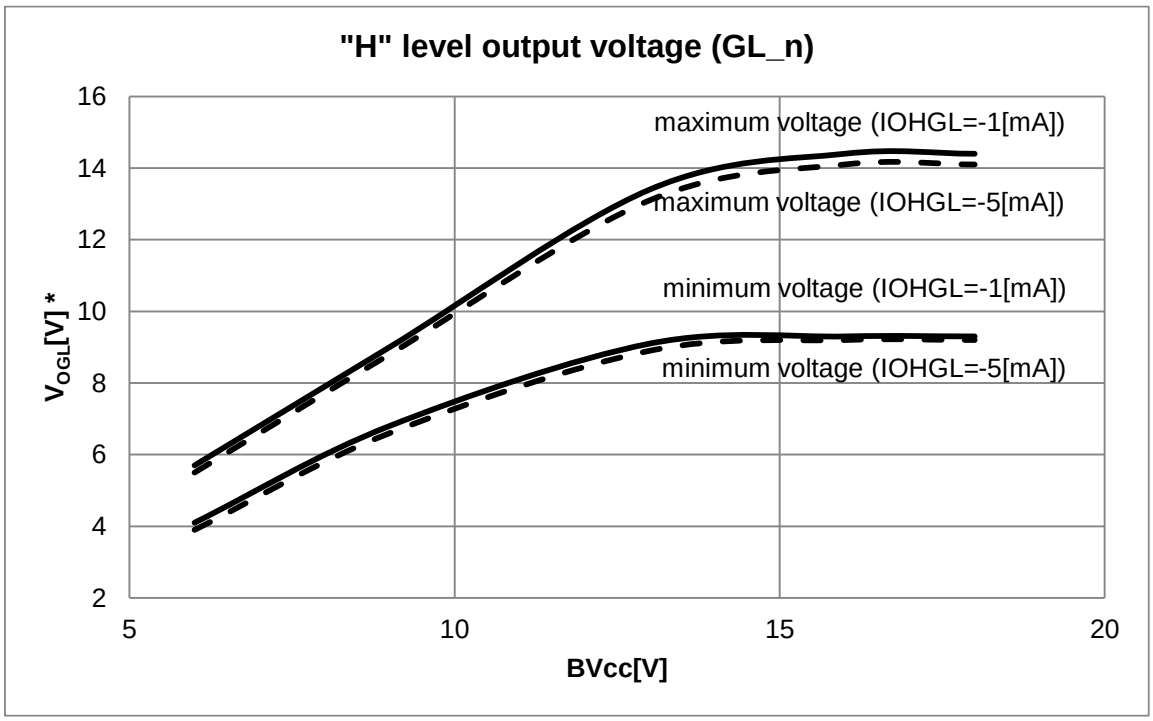
Title	Condition of a Simulation
Charge pump voltage	Charge pump output current(ICPO):20[mA] Output frequency(fCP):500[kHz] C_{CP1}=0.022[µF]/ C_{CP2}=0.47[µF] Forward voltage of D1/D2:0.28[V] (Forward current=0.1[A] , T_A = +25°C)

Simulation circuit



■ "H" level output voltage of Three-phase Motor Pre-Driver
Reference values obtained with simulations. It is not the guaranteed value.
(V_{SS} = PV_{SS} = LV_{SS} = 0V, T_A = - 40°C to + 105°C)



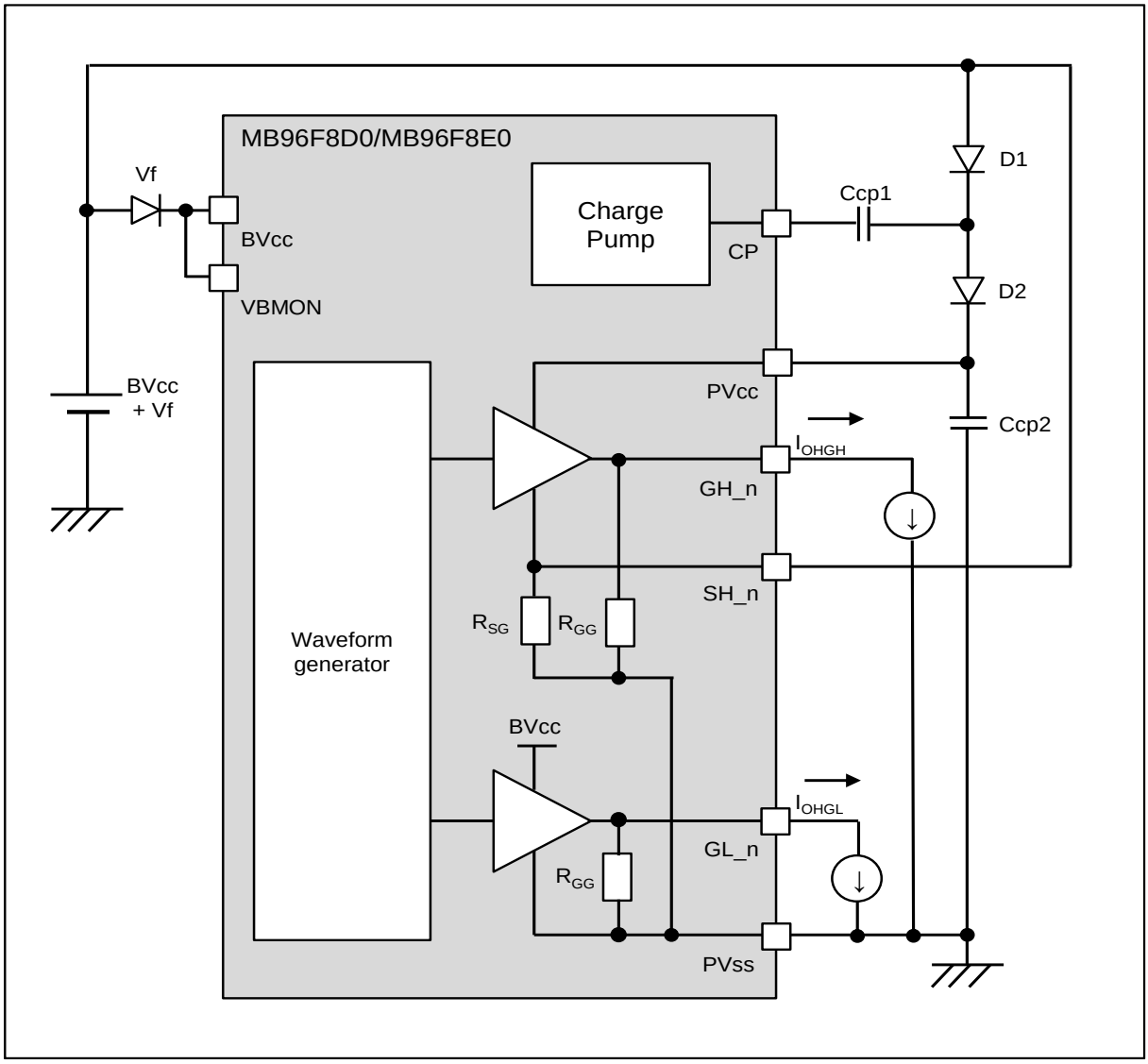


*: VOGH = GH_n – SH_n, VOGL = GL_n

■ Condition of a simulation

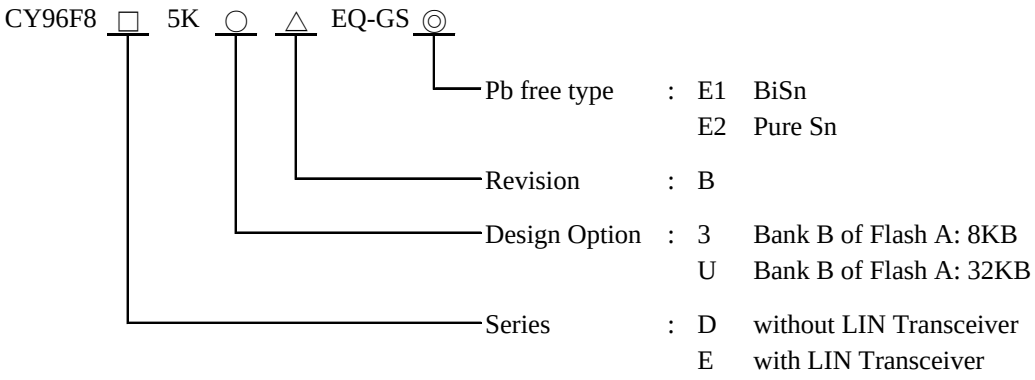
Title	Condition of a Simulation
"H" level output voltage (GH_n) "H" level output voltage (GL_n)	Charge pump output frequency:500[kHz] C_{CP1}=0.022[µF]/ C_{CP2}=0.47[µF] Forward voltage of D1/D2:0.28[V] (Forward current=0.1[A] , T_A = +25°C) SSWSDC.LBST3 to LBST0=1111_B SSWSDC.HBST3 to HBST0=1111_B MPDC2.LSR2 to LSR0=111_B MPDC2.HSR2 to HSR0=111_B Vf (forward voltage of reverse connection protection diode): Minimum condition:0.9[V]/ maximum condition:0.7[V]

■ Simulation circuit



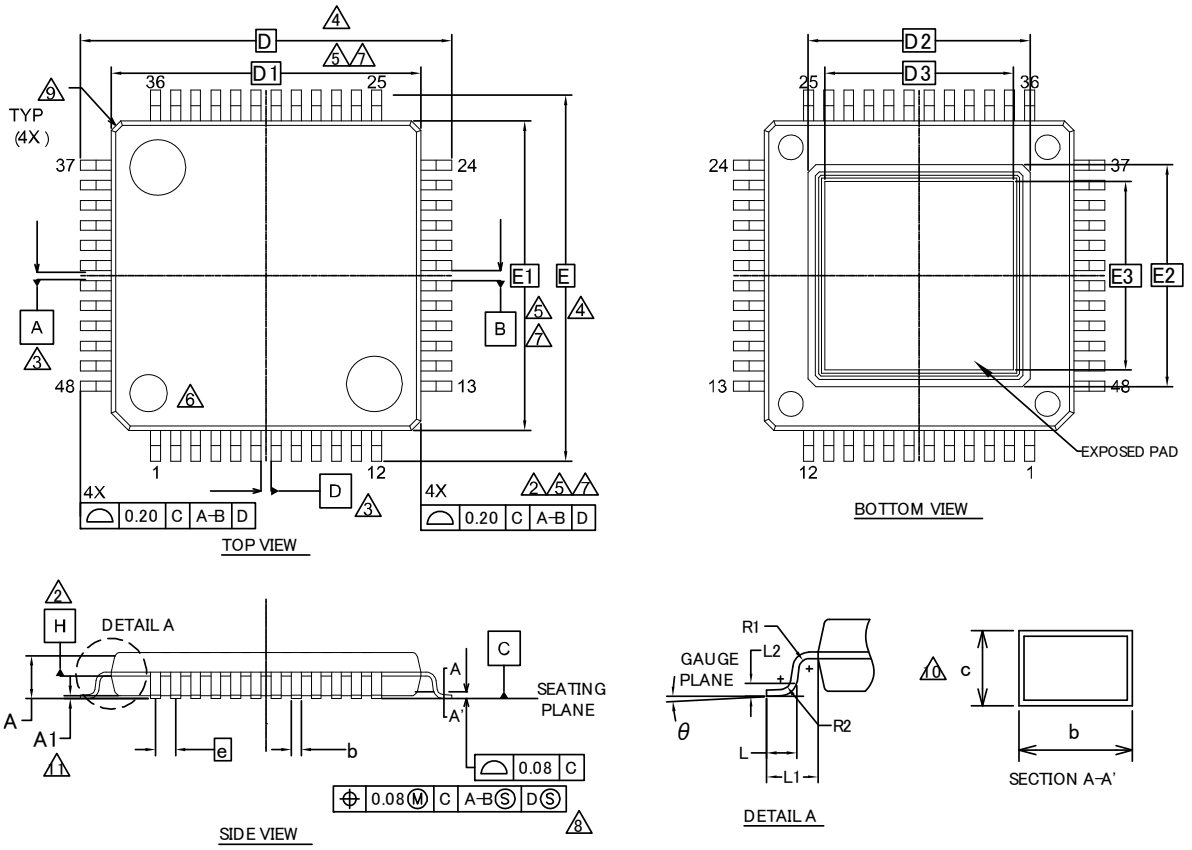
16. Ordering Information

Part Number	Flash Memory	Package*
CY96F8D5K3BEQ-GSE1	Flash A (136.5KB)	48-pin plastic TEQFP (LEC048)
CY96F8D5K3BEQ-GSE2		
CY96F8E5K3BEQ-GSE1		
CY96F8E5K3BEQ-GSE2		
CY96F8D5KUBEQ-GSE1	Flash A (160.5KB)	
CY96F8D5KUBEQ-GSE2		
CY96F8E5KUBEQ-GSE1		
CY96F8E5KUBEQ-GSE2		



*: For details about package, see "Package Dimension".

17. Package Dimension



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
D		12.00 BSC	
D1		10.00 BSC	
D2		7.17 REF	
D3		6.10 REF	
E		12.00 BSC	
E1		10.00 BSC	
E2		7.17 REF	
E3		6.10 REF	
R1	0.08	—	—
R2	0.08	—	0.20
θ	0°	4°	8°
c	0.09	—	0.20
b	0.27	0.32	0.37
L	0.45	0.60	0.75
L1		1.00 REF	
L2		0.25	
e		0.65 BSC	

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
11. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
12. JEDEC SPECIFICATION NO. REF : N/A

002-15529 **

PACKAGE OUTLINE, 48 LEAD TEQFP
10.0X10.0X1.7 MM LEC048 6.1X6.1 MM EPAD (SAWN) REV*

18. Package Thermal Resistance

This characteristic is the reference values measured under the following conditions. It is not the guaranteed value.
PCB(FR4) : JEDEC STANDARD
PCB SIZE : 114.3mm × 76.2mm × 1.6mm (4 layer)
L2/ L3 Residual copper rate : 90%
OTHER : It connects between PCB PAD with the Exposure PAD with the solder paste.
Place the thermal via hole to the PCB PAD.

Package	Symbol	Measurement Value			Unit	Remarks
		Min	Typ	Max		
LEC048	θ_{JA} *1	-	18	-	°C /W	-
	Ψ_{JT} *2	-	9	-	°C /W	-

*1: θ_{JA}= (T_j(Junction Temperature) - T_A(Ambient Temperature)) / P_D(Power Dissipation)
*2: Ψ_{JT}= (T_j(Junction Temperature) – Package Surface Temperature) / P_D(Power Dissipation)

19. Major Changes

Spansion Publication Number: M96800_DS704-00016

Page	Section	Change Results
Revision 2.0		
-	-	Initial release
Revision 3.0		
41, 42	ELECTRICAL CHARACTERISTICS 1. Absolute Maximum Ratings	Remove "1" from name of the following parameters - Power supply voltage : BV_{CC1} - 12V analog power supply voltage : PV_{CC1} - 12V Input voltage : $V12_{I1}$ - Transient input voltage : V_{VBMON1}
		Change the condition of the following parameters - Power supply voltage : BV_{CC1} - 12V analog power supply voltage : PV_{CC1} - 12V Input voltage : $V12_{I1}$ - LIN Input voltage : LIN_I - Transient input voltage : V_{VBMON1}
		Remove the following parameters - Power supply voltage 2 : BV_{CC2} - 12V Input voltage 2 : $V12_{I2}$ - Transient input voltage 2 : V_{VBMON2}
82	18. LIN Transceiver	Change the condition of Input leakage current receiver recessive state : I_{LINIL_REC} LIN=18V, SOT2=1 → 7V≤LIN≤18V, BVCC≤ LIN, SOT2=1
		Correct the unit of Input leakage current receiver recessive state : I_{LINIL_REC}
83		Add the following parameters - Duty cycle 1 : $D1_{LINTX}$ - Duty cycle 2 : $D2_{LINTX}$ - Duty cycle 3 : $D3_{LINTX}$ - Duty cycle 4 : $D4_{LINTX}$ - Propagation delay of receiver : t_{rx_pd} - Symmetry of receiver propagation delay : t_{rx_sym} - Input capacitance : C_{LININ}
85		Add the Timing Chart of LIN Transceiver

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: CY96800 Series ASSP DC/BLDC Motor controller for 12V-Battery Datasheet
Document Number: 002-07479

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	–	HIHA	04/28/2015	Migrated to Cypress and assigned document number 002-07479. No change to document contents or format.
*A	5132858	HIHA	03/14/2016	Updated to Cypress template
*B	6495611	TORS	02/27/2018	Update Cypress Logo. Change parts number from MB to CY. Change package dimension.

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