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How to Check the Ordering Part Number

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MB95F352E/F352L/F353E/F353L/F354E/F354L

CMOS F^{2}MC-8FX MB95350L Series 8-bit Microcontrollers

MB95350L is a series of general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers of this series contain a variety of peripheral resources.

Features

F^{2}MC-8FX CPU core

Instruction set optimized for controllers

- Multiplication and division instructions
- 16-bit arithmetic operations
- Bit test branch instructions
- Bit manipulation instructions, etc.

Clock

- Selectable main clock source
  - Main OSC clock (up to 16.25 MHz, maximum machine clock frequency: 8.125 MHz)
  - External clock (up to 32.5 MHz, maximum machine clock frequency: 16.25 MHz)
  - Main CR clock (1/8/10/12.5 MHz ±2%, maximum machine clock frequency: 12.5 MHz)
- Selectable subclock source
  - Sub-OSC clock (32.768 kHz)
  - External clock (32.768 kHz)
  - Sub-CR clock (Typ: 100 kHz, Min: 50 kHz, Max: 200 kHz)

Timer

- 8/16-bit composite timer × 2 channels
- Time-base timer × 1 channel
- Watch prescaler × 1 channel

UART/SIO × 1 channel (The channel can be used either as a UART/SIO channel or as an I^{2}C channel.)

- Alternative selection of UART/SIO
- Full duplex double buffer
- Capable of clock-asynchronous (UART) serial data transfer and clock-synchronous (SIO) serial data transfer

I^{2}C × 2 channels (One of the two channels can be used either as an I^{2}C channel or as a UART/SIO channel.)

- Supports Standard-mode and Fast-mode (400 kHz)
- Built-in wake-up function

LIN-UART

- Full duplex double buffer
- Capable of clock-synchronous serial data transfer and clock-asynchronous serial data transfer

External interrupt × 6 channels

- Interrupt by edge detection (rising edge, falling edge, and both edges can be selected)
- Can be used to wake up the device from different low power consumption (standby) modes

8/10-bit A/D converter × 6 channels

- 8-bit and 10-bit resolution can be chosen.

Low power consumption (standby) modes

- Stop mode
- Sleep mode
- Watch mode
- Time-base timer mode

I/O port

- MB95F352L/F353L/F354L (maximum no. of I/O ports: 21)
  - General-purpose I/O ports (N-ch open drain) ..... : 3
  - General-purpose I/O ports (CMOS I/O) ..... : 18
- MB95F352E/F353E/F354E (maximum no. of I/O ports: 22)
  - General-purpose I/O ports (N-ch open drain) ..... : 3
  - General-purpose I/O ports (CMOS I/O) ..... : 18
  - General-purpose input port (CMOS input) ..... : 1

On-chip debug

- 1-wire serial control
- Serial writing supported (asynchronous mode)

Hardware/software watchdog timer

- Built-in hardware watchdog timer
- Built-in software watchdog timer

Low-voltage detection reset and interrupt circuit

- Built-in low-voltage detector

Clock supervisor counter

- Built-in clock supervisor counter function

Programmable port input voltage level

- CMOS input level / hysteresis input level

Dual operation Flash memory

- The erase/write operation and the read operation can be executed in different banks (upper bank/lower bank) simultaneously.

Flash memory security function

- Protects the content of the Flash memory

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1. Product Line-up

Part number / Parameter	MB95F352E	MB95F353E	MB95F354E	MB95F352L	MB95F353L	MB95F354L
Type	Flash memory product					
Clock supervisor counter	It supervises the main clock oscillation.					
Program ROM capacity	8 Kbyte	12 Kbyte	20 Kbyte	8 Kbyte	12 Kbyte	20 Kbyte
RAM capacity	240 bytes	496 bytes	496 bytes	240 bytes	496 bytes	496 bytes
Low-voltage detection reset	Yes			No		
Reset input	Selected through software			Dedicated		
CPU functions	Number of basic instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8 and 16 bits Minimum instruction execution time : 61.5 ns (with machine clock = 16.25 MHz) Interrupt processing time : 0.6 µs (with machine clock = 16.25 MHz)					
General-purpose I/O	I/O ports (Max): 22 CMOS I/O: 18 N-ch open drain: 3 CMOS input: 1			I/O ports (Max): 21 CMOS I/O: 18 N-ch open drain: 3		
Time-base timer	Interrupt cycle: 0.256 ms to 8.3 s (when external clock = 4 MHz)					
Hardware/software watchdog timer	Reset generation cycle - Main oscillation clock at 10 MHz: 105 ms (Min) The sub-CR clock can be used as the source clock of the hardware watchdog timer.					
Wild register	It can be used to replace three bytes of data.					
LIN-UART	A wide range of communication speeds can be selected by a dedicated reload timer. Clock-synchronous serial data transfer and clock-asynchronous serial data transfer is enabled. The LIN function can be used as a LIN master or a LIN slave.					
8/10-bit A/D converter	6 channels					
	8-bit resolution and 10-bit resolution can be chosen.					
8/16-bit composite timer	2 channels					
	The timer can be configured as an "8-bit timer x 2 channels" or a "16-bit timer x 1 channel". It has built-in timer function, PWC function, PWM function and input capture function. Count clock: it can be selected from internal clocks (seven types) and external clocks. It can output square wave.					
External interrupt	6 channels					
	Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.) It can be used to wake up the device from different standby modes.					
On-chip debug	1-wire serial control It supports serial writing. (asynchronous mode)					

(Continued)

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Part number / Parameter	MB95F352E	MB95F353E	MB95F354E	MB95F352L	MB95F353L	MB95F354L
UART/SIO	1 channel (The channel can be used either as a UART/SIO channel or as an I^2C channel.)					
	Data transfer with UART/SIO is enabled. It has a full duplex double buffer, variable data length (5/6/7/8 bits), a built-in baud rate generator and an error detection function. It uses the NRZ type transfer format. LSB-first data transfer and MSB-first data transfer are available to use. Clock-asynchronous (UART) serial data transfer and clock-synchronous (SIO) serial data transfer is enabled.					
I^2C	2 channels (One of the two channels can be used either as an I^2C channel or as a UART/SIO channel.)					
	Master/slave transmission and receiving It has the following functions: • bus error function • arbitration function • transmission direction detection function • wake-up function • functions of generating and detecting repeated START conditions.					
Watch prescaler	Eight different time intervals can be selected.					
Flash memory	It supports automatic programming, Embedded Algorithm, write/erase/erase-suspend/erase-resume commands. It has a flag indicating the completion of the operation of Embedded Algorithm. Number of write/erase cycles: 100000 Data retention time: 20 years Flash security feature for protecting the content of the Flash memory					
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode					
Package	FPT-24P-M34 FPT-24P-M10 LCC-32P-M19					

2. Packages and Corresponding Products

Part number / Package	MB95F352E	MB95F353E	MB95F354E	MB95F352L	MB95F353L	MB95F354L
FPT-24P-M34	O	O	O	O	O	O
FPT-24P-M10	O	O	O	O	O	O
LCC-32P-M19	O	O	O	O	O	O

O: Available

3. Differences Among Products and Notes On Product Selection

■ Current consumption

When using the on-chip debug function, take account of the current consumption of flash erase/write.
For details of current consumption, see “Electrical Characteristics”.

■ Package

For details of information on each package, see “Packages and Corresponding Products” and “Package Dimension”.

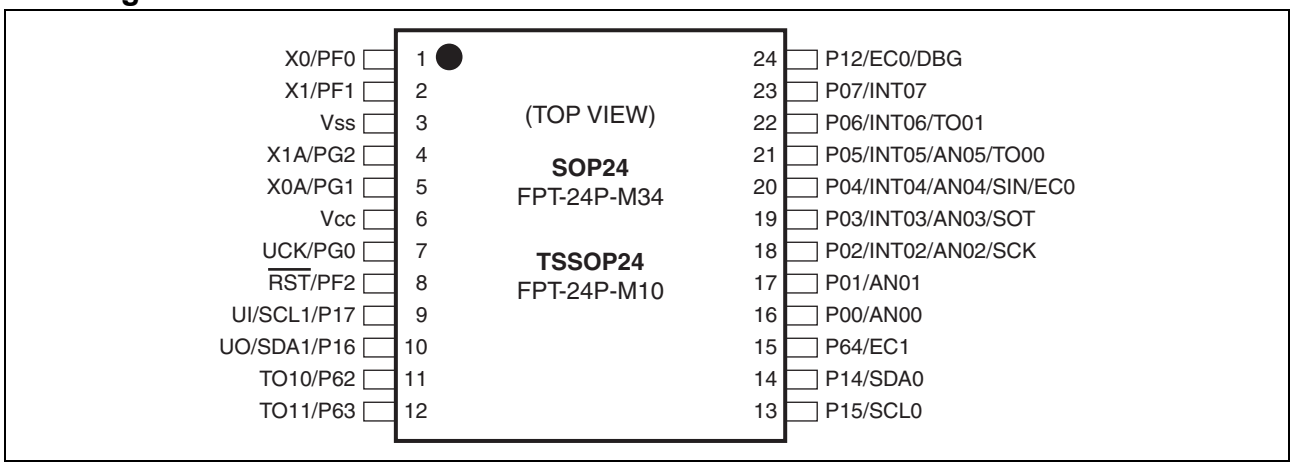
■ Operating voltage

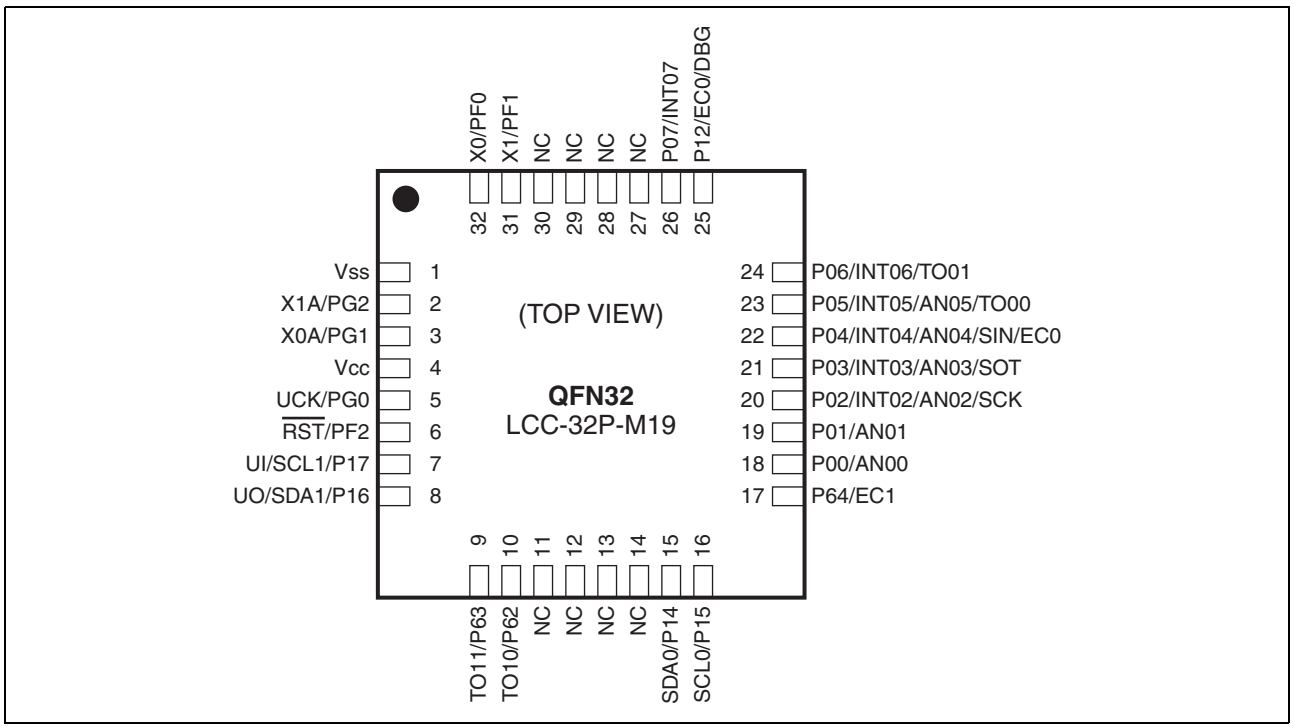
The operating voltage varies, depending on whether the on-chip debug function is used or not.
For details of the operating voltage, see “Electrical Characteristics”

■ On-chip debug function

The on-chip debug function requires that V_{CC}, V_{SS} and one serial wire be connected to an evaluation tool.

4. Pin Assignment





5. Pin Description (24-pin MCU)

Pin no.	Pin name	I/O circuit type*	Function
1	PF0	B	General-purpose I/O port
	X0		Main clock input oscillation pin
2	PF1	B	General-purpose I/O port
	X1		Main clock I/O oscillation pin
3	V_{SS}	—	Power supply pin (GND)
4	PG2	C	General-purpose I/O port
	X1A		Subclock I/O oscillation pin
5	PG1	C	General-purpose I/O port
	X0A		Subclock input oscillation pin
6	V_{CC}	—	Power supply pin
7	PG0	G	General-purpose I/O port
	UCK		UART/SIO clock pin
8	PF2	A	General-purpose input port
	$\overline{RST}$		Reset pin Dedicated reset pin on MB95F352L/F353L/F354L
9	P17	J	General-purpose I/O port
	SCL1		I^2C ch. 1 clock I/O pin
	UI		UART/SIO data input pin
10	P16	J	General-purpose I/O port
	SDA1		I^2C ch. 1 data I/O pin
	UO		UART/SIO data output pin
11	P62	D	General-purpose I/O port High-current pin
	TO10		8/16-bit composite timer ch. 1 output pin
12	P63	D	General-purpose I/O port High-current pin
	TO11		8/16-bit composite timer ch. 1 output pin
13	P15	I	General-purpose I/O port
	SCL0		I^2C ch. 0 clock I/O pin
14	P14	I	General-purpose I/O port
	SDA0		I^2C ch. 0 data I/O pin
15	P64	D	General-purpose I/O port
	EC1		8/16-bit composite timer ch. 1 clock input pin
16	P00	E	General-purpose I/O port
	AN00		A/D converter analog input pin

(Continued)

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Pin no.	Pin name	I/O circuit type*	Function
17	P01	E	General-purpose I/O port
	AN01		A/D converter analog input pin
18	P02	E	General-purpose I/O port
	INT02		External interrupt input pin
	AN02		A/D converter analog input pin
	SCK		LIN-UART clock I/O pin
19	P03	E	General-purpose I/O port
	INT03		External interrupt input pin
	AN03		A/D converter analog input pin
	SOT		LIN-UART data output pin
20	P04	F	General-purpose I/O port
	INT04		External interrupt input pin
	AN04		A/D converter analog input pin
	SIN		LIN-UART data input pin
	EC0		8/16-bit composite timer ch. 0 clock input pin
21	P05	E	General-purpose I/O port High-current pin
	INT05		External interrupt input pin
	AN05		A/D converter analog input pin
	TO00		8/16-bit composite timer ch. 0 output pin
22	P06	G	General-purpose I/O port High-current pin
	INT06		External interrupt input pin
	TO01		8/16-bit composite timer ch. 0 output pin
23	P07	G	General-purpose I/O port
	INT07		External interrupt input pin
24	P12	H	General-purpose I/O port
	EC0		8/16-bit composite timer ch. 0 clock input pin
	DBG		DBG input pin

*: For the I/O circuit types, see “I/O Circuit Type”.

6. Pin Description (32-pin MCU)

Pin no.	Pin name	I/O circuit type*	Function
1	V_{SS}	—	Power supply pin (GND)
2	PG2	C	General-purpose I/O port
	X1A		Subclock I/O oscillation pin
3	PG1	C	General-purpose I/O port
	X0A		Subclock input oscillation pin
4	V_{CC}	—	Power supply pin
5	PG0	G	General-purpose I/O port
	UCK		UART/SIO clock pin
6	PF2	A	General-purpose input port
	$\overline{RST}$		Reset pin Dedicated reset pin on MB95F352L/F353L/F354L
7	P17	J	General-purpose I/O port
	SCL1		I^2C ch. 1 clock I/O pin
	UI		UART/SIO data input pin
8	P16	J	General-purpose I/O port
	SDA1		I^2C ch. 1 data I/O pin
	UO		UART/SIO data output pin
9	P63	D	General-purpose I/O port High-current pin
	TO11		8/16-bit composite timer ch. 1 output pin
10	P62	D	General-purpose I/O port High-current pin
	TO10		8/16-bit composite timer ch. 1 output pin
11	NC	—	It is an internally connected pin. Always leave it unconnected.
12	NC	—	It is an internally connected pin. Always leave it unconnected.
13	NC	—	It is an internally connected pin. Always leave it unconnected.
14	NC	—	It is an internally connected pin. Always leave it unconnected.
15	P14	I	General-purpose I/O port
	SDA0		I^2C ch. 0 data I/O pin
16	P15	I	General-purpose I/O port
	SCL0		I^2C ch. 0 clock I/O pin
17	P64	D	General-purpose I/O port
	EC1		8/16-bit composite timer ch. 1 clock input pin
18	P00	E	General-purpose I/O port
	AN00		A/D converter analog input pin

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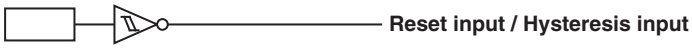
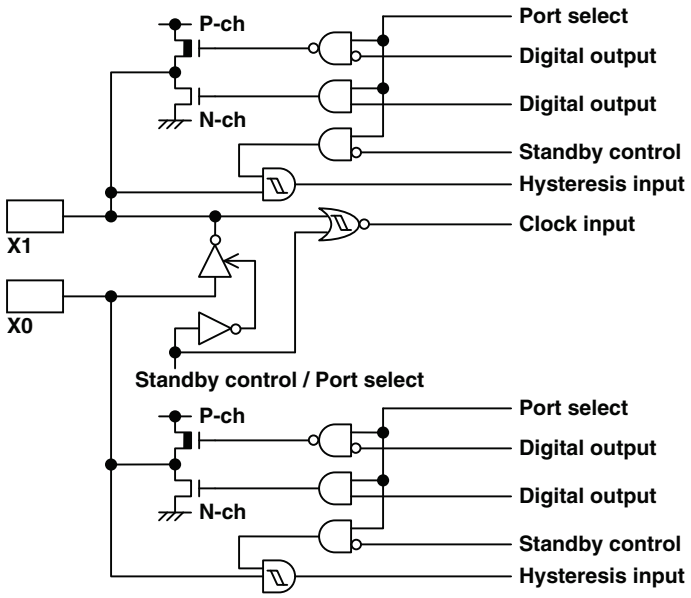
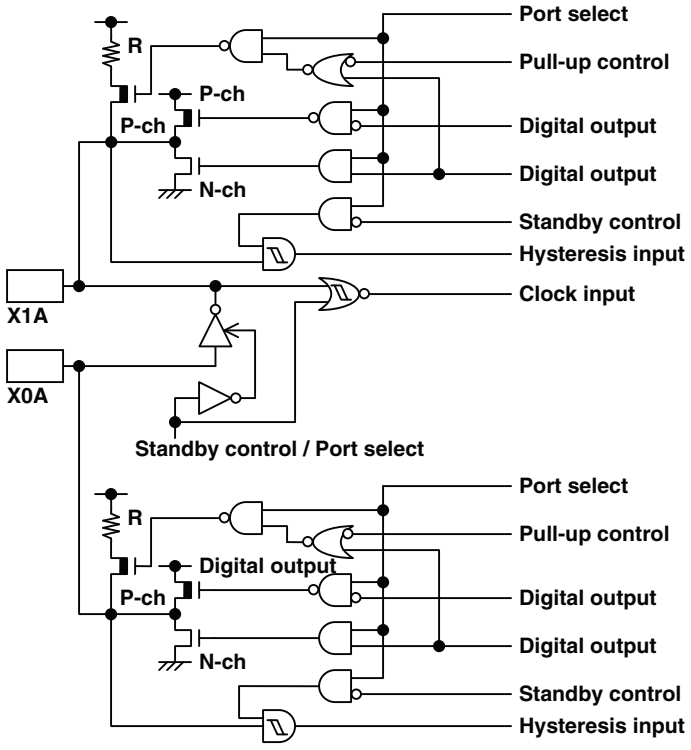
Pin no.	Pin name	I/O circuit type*	Function
19	P01	E	General-purpose I/O port
	AN01		A/D converter analog input pin
20	P02	E	General-purpose I/O port
	INT02		External interrupt input pin
	AN02		A/D converter analog input pin
	SCK		LIN-UART clock I/O pin
21	P03	E	General-purpose I/O port
	INT03		External interrupt input pin
	AN03		A/D converter analog input pin
	SOT		LIN-UART data output pin
22	P04	F	General-purpose I/O port
	INT04		External interrupt input pin
	AN04		A/D converter analog input pin
	SIN		LIN-UART data input pin
	EC0		8/16-bit composite timer ch. 0 clock input pin
23	P05	E	General-purpose I/O port High-current pin
	INT05		External interrupt input pin
	AN05		A/D converter analog input pin
	TO00		8/16-bit composite timer ch. 0 output pin
24	P06	G	General-purpose I/O port High-current pin
	INT06		External interrupt input pin
	TO01		8/16-bit composite timer ch. 0 output pin
25	P12	H	General-purpose I/O port
	EC0		8/16-bit composite timer ch. 0 clock input pin
	DBG		DBG input pin
26	P07	G	General-purpose I/O port
	INT07		External interrupt input pin
27	NC	—	It is an internally connected pin. Always leave it unconnected.
28	NC	—	It is an internally connected pin. Always leave it unconnected.
29	NC	—	It is an internally connected pin. Always leave it unconnected.
30	NC	—	It is an internally connected pin. Always leave it unconnected.
31	PF1	B	General-purpose I/O port
	X1		Main clock I/O oscillation pin
32	PF0	B	General-purpose I/O port
	X0		Main clock input oscillation pin

*: For the I/O circuit types, see “I/O Circuit Type”.

7. I/O Circuit Type

Type	Circuit	Remarks
A		■ Hysteresis input ■ Reset input
B		■ Oscillation circuit ■ High-speed side ■ Feedback resistance: approx. 1 MΩ ■ CMOS output ■ Hysteresis input
C		■ Oscillation circuit ■ Low-speed side ■ Feedback resistance: approx.10 MΩ ■ CMOS output ■ Hysteresis input ■ Pull-up control available

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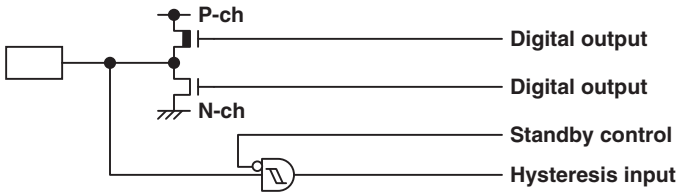
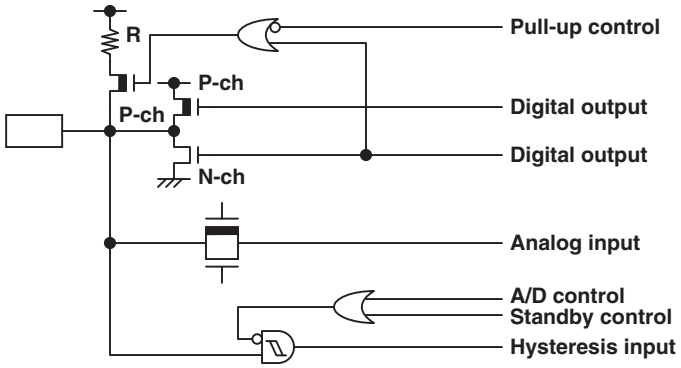
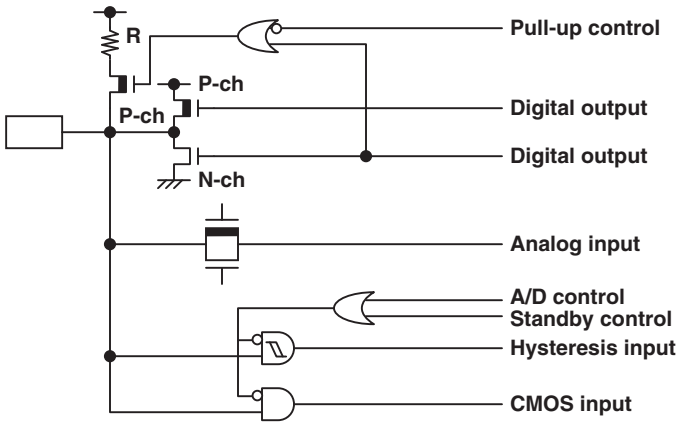
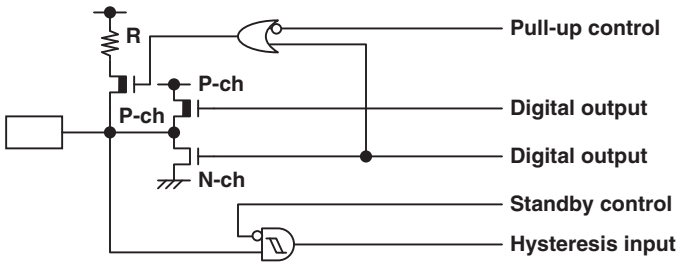
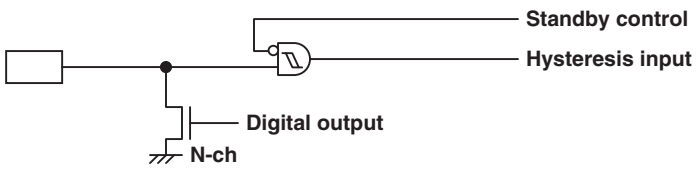
Type	Circuit	Remarks
D		■ CMOS output ■ Hysteresis input
E		■ CMOS output ■ Hysteresis input ■ Pull-up control available
F		■ CMOS output ■ Hysteresis input ■ CMOS input ■ Pull-up control available
G		■ CMOS output ■ Hysteresis input ■ Pull-up control available
H		■ N-ch open drain output ■ Hysteresis input

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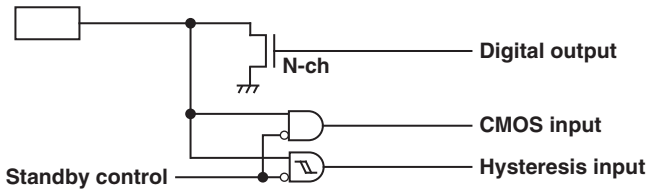
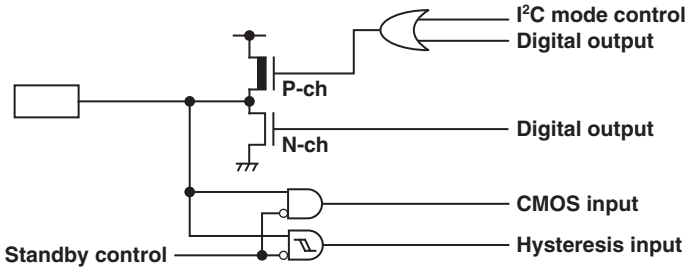
Type	Circuit	Remarks
I		■ N-ch open drain output ■ Hysteresis input ■ CMOS input
J		■ CMOS output ■ Hysteresis input ■ CMOS input ■ N-ch open drain output in I^2C mode

8. Notes On Device Handling

■ Preventing latch-ups

When using the device, ensure that the voltage applied does not exceed the maximum voltage rating.

In a CMOS IC, if a voltage higher than V_{CC} or a voltage lower than V_{SS} is applied to an input/output pin that is neither a medium-withstand voltage pin nor a high-withstand voltage pin, or if a voltage out of the rating range of power supply voltage mentioned in "14.1 Absolute Maximum Ratings" of "Electrical Characteristics" is applied to the V_{CC} pin or the V_{SS} pin, a latch-up may occur.

When a latch-up occurs, power supply current increases significantly, which may cause a component to be thermally destroyed.

■ Stabilizing supply voltage

Supply voltage must be stabilized.

A malfunction may occur when power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the V_{CC} power supply voltage.

As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in V_{CC} ripple (p-p value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard V_{CC} value, and the transient fluctuation rate does not exceed 0.1 V/ms at a momentary fluctuation such as switching the power supply.

■ Notes on using the external clock

When an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from subclock mode or stop mode.

9. Pin Connection

■ Treatment of unused pins

If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latch-ups. Always pull up or pull down an unused input pin through a resistor of at least 2 kΩ. Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.

■ Power supply pins

To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the V_{CC} pin and the V_{SS} pin to the power supply and ground outside the device. In addition, connect the current supply source to the V_{CC} pin and the V_{SS} pin with low impedance.

It is also advisable to connect a ceramic capacitor of approximately 0.1 µF as a bypass capacitor between the V_{CC} pin and the V_{SS} pin at a location close to this device.

■ DBG pin

Connect the DBG pin directly to an external pull-up resistor.

To prevent the device from unintentionally entering the debug mode due to noise, minimize the distance between the DBG pin and the V_{CC} or V_{SS} pin when designing the layout of the printed circuit board.

The DBG pin should not stay at "L" level after power-on until the reset is released.

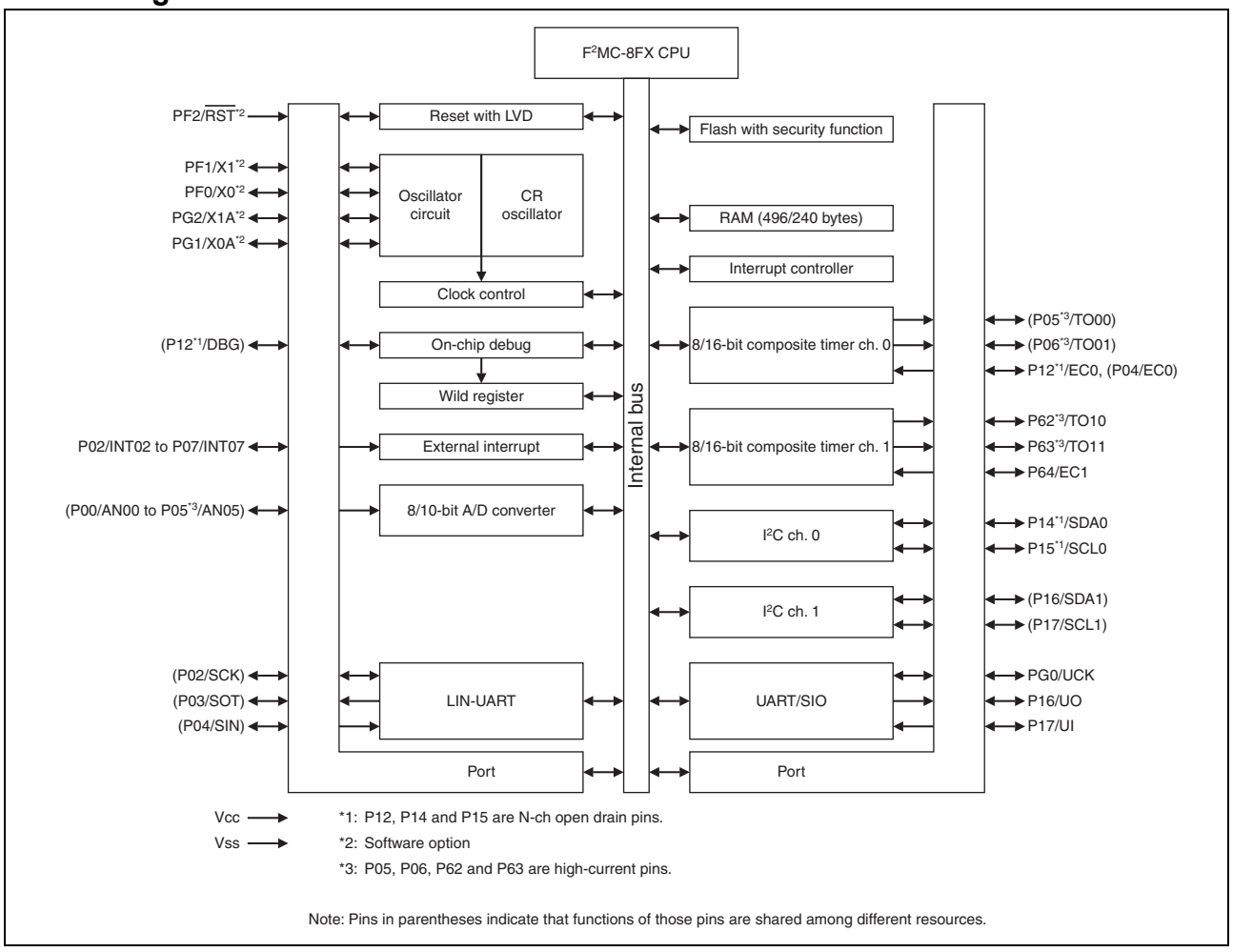
■ $\overline{\text{RST}}$ pin

Connect the $\overline{\text{RST}}$ pin directly to an external pull-up resistor.

To prevent the device from unintentionally entering the reset mode due to noise, minimize the distance between the $\overline{\text{RST}}$ pin and the V_{CC} or V_{SS} pin when designing the layout of the printed circuit board.

The PF2/$\overline{\text{RST}}$ pin functions as the reset input pin after power-on. The RSTEN bit in the SYSC register is used to switch the pin functions, the reset input function and the general-purpose I/O port function, of the PF2/$\overline{\text{RST}}$ pin. However, only on MB95F352E/F353E/F354E can the pin functions be changed.

10. Block Diagram

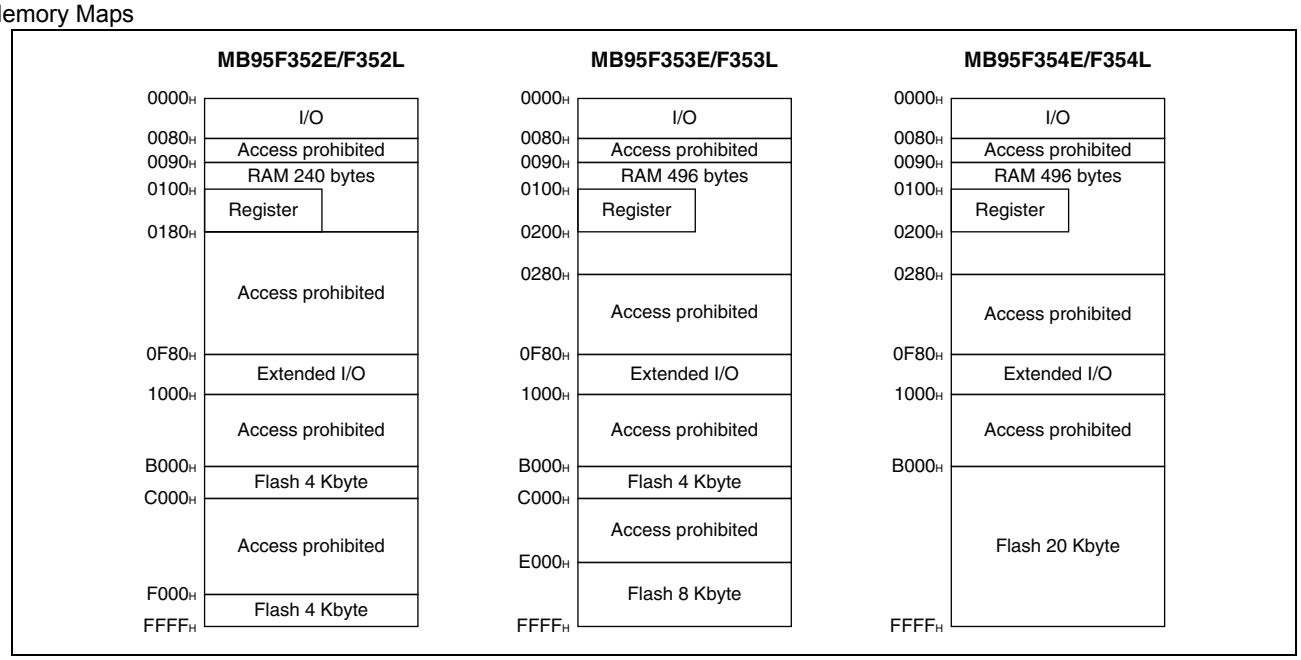


11. CPU Core

■ Memory Space

The memory space of the MB95350L Series is 64 Kbyte in size, and consists of an I/O area, a data area, and a program area. The memory space includes areas intended for specific purposes such as general-purpose registers and a vector table. The memory maps of the MB95350L Series are shown below.

■ Memory Maps



12. I/O Map

Address	Register abbreviation	Register name	R/W	Initial value
0000_H	PDR0	Port 0 data register	R/W	00000000_B
0001_H	DDR0	Port 0 direction register	R/W	00000000_B
0002_H	PDR1	Port 1 data register	R/W	00000000_B
0003_H	DDR1	Port 1 direction register	R/W	00000000_B
0004_H	—	(Disabled)	—	—
0005_H	WATR	Oscillation stabilization wait time setting register	R/W	11111111_B
0006_H	—	(Disabled)	—	—
0007_H	SYCC	System clock control register	R/W	$0000X011_B$
0008_H	STBC	Standby control register	R/W	$00000XXX_B$
0009_H	RSRR	Reset source register	R/W	XXXXXXXX_B
$000A_H$	TBTC	Time-base timer control register	R/W	00000000_B
$000B_H$	WPCR	Watch prescaler control register	R/W	00000000_B
$000C_H$	WDTC	Watchdog timer control register	R/W	$00XX0000_B$
$000D_H$	SYCC2	System clock control register 2	R/W	$XX100011_B$
$000E_H$ to 0015_H	—	(Disabled)	—	—
0016_H	PDR6	Port 6 data register	R/W	00000000_B
0017_H	DDR6	Port 6 direction register	R/W	00000000_B
0018_H to 0027_H	—	(Disabled)	—	—
0028_H	PDRF	Port F data register	R/W	00000000_B
0029_H	DDRF	Port F direction register	R/W	00000000_B
$002A_H$	PDRG	Port G data register	R/W	00000000_B
$002B_H$	DDRG	Port G direction register	R/W	00000000_B
$002C_H$	PUL0	Port 0 pull-up register	R/W	00000000_B
$002D_H$ to 0034_H	—	(Disabled)	—	—
0035_H	PULG	Port G pull-up register	R/W	00000000_B
0036_H	T01CR1	8/16-bit composite timer 01 status control register 1 ch. 0	R/W	00000000_B
0037_H	T00CR1	8/16-bit composite timer 00 status control register 1 ch. 0	R/W	00000000_B
0038_H	T11CR1	8/16-bit composite timer 11 status control register 1 ch. 1	R/W	00000000_B
0039_H	T10CR1	8/16-bit composite timer 10 status control register 1 ch. 1	R/W	00000000_B
$003A_H$ to 0048_H	—	(Disabled)	—	—
0049_H	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	00000000_B
$004A_H$	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	00000000_B
$004B_H$	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	00000000_B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
$004C_H$, $004D_H$	—	(Disabled)	—	—
$004E_H$	LVDR	LVD reset voltage selection ID register	R/W	00000000_B
$004F_H$	LVDC	LVD interrupt control register	R/W	$X000000X_B$
0050_H	SCR	LIN-UART serial control register	R/W	00000000_B
0051_H	SMR	LIN-UART serial mode register	R/W	00000000_B
0052_H	SSR	LIN-UART serial status register	R/W	00001000_B
0053_H	RDR/TDR	LIN-UART receive/transmit data register	R/W	00000000_B
0054_H	ESCR	LIN-UART extended status control register	R/W	00000100_B
0055_H	ECCR	LIN-UART extended communication control register	R/W	$000000XX_B$
0056_H	SMC10	UART/SIO serial mode control register 1 ch. 0	R/W	00000000_B
0057_H	SMC20	UART/SIO serial mode control register 2 ch. 0	R/W	00100000_B
0058_H	SSR0	UART/SIO serial status and data register ch. 0	R/W	00000001_B
0059_H	TDR0	UART/SIO serial output data register ch. 0	R/W	00000000_B
$005A_H$	RDR0	UART/SIO serial input data register ch. 0	R	00000000_B
$005B_H$ to $005F_H$	—	(Disabled)	—	—
0060_H	IBCR00	I^2C bus control register 0 ch. 0	R/W	00000000_B
0061_H	IBCR10	I^2C bus control register 1 ch. 0	R/W	00000000_B
0062_H	IBSR0	I^2C bus status register ch. 0	R	00000000_B
0063_H	IDDR0	I^2C data register ch. 0	R/W	00000000_B
0064_H	IAAR0	I^2C address register ch. 0	R/W	00000000_B
0065_H	ICCR0	I^2C clock control register ch. 0	R/W	00000000_B
0066_H	IBCR01	I^2C bus control register 0 ch. 1	R/W	00000000_B
0067_H	IBCR11	I^2C bus control register 1 ch. 1	R/W	00000000_B
0068_H	IBSR1	I^2C bus status register ch. 1	R	00000000_B
0069_H	IDDR1	I^2C data register ch. 1	R/W	00000000_B
$006A_H$	IAAR1	I^2C address register ch. 1	R/W	00000000_B
$006B_H$	ICCR1	I^2C clock control register ch. 1	R/W	00000000_B
$006C_H$	ADC1	8/10-bit A/D converter control register 1	R/W	00000000_B
$006D_H$	ADC2	8/10-bit A/D converter control register 2	R/W	00000000_B
$006E_H$	ADDH	8/10-bit A/D converter data register (upper)	R/W	00000000_B
$006F_H$	ADDL	8/10-bit A/D converter data register (lower)	R/W	00000000_B
0070_H	—	(Disabled)	—	—
0071_H	FSR2	Flash memory status register 2	R/W	00000000_B
0072_H	FSR	Flash memory status register	R/W	$000X0000_B$
0073_H	SWRE0	Flash memory sector write control register 0	R/W	00000000_B
0074_H	FSR3	Flash memory status register 3	R	00000000_B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0075_H	—	(Disabled)	—	—
0076_H	WREN	Wild register address compare enable register	R/W	00000000_B
0077_H	WROR	Wild register data test setting register	R/W	00000000_B
0078_H	—	Mirror of register bank pointer (RP) and mirror of direct bank pointer (DP)	—	—
0079_H	ILR0	Interrupt level setting register 0	R/W	11111111_B
$007A_H$	ILR1	Interrupt level setting register 1	R/W	11111111_B
$007B_H$	ILR2	Interrupt level setting register 2	R/W	11111111_B
$007C_H$	ILR3	Interrupt level setting register 3	R/W	11111111_B
$007D_H$	ILR4	Interrupt level setting register 4	R/W	11111111_B
$007E_H$	ILR5	Interrupt level setting register 5	R/W	11111111_B
$007F_H$	—	(Disabled)	—	—
$0F80_H$	WRARH0	Wild register address setting register (upper) ch. 0	R/W	00000000_B
$0F81_H$	WRARL0	Wild register address setting register (lower) ch. 0	R/W	00000000_B
$0F82_H$	WRDR0	Wild register data setting register ch. 0	R/W	00000000_B
$0F83_H$	WRARH1	Wild register address setting register (upper) ch. 1	R/W	00000000_B
$0F84_H$	WRARL1	Wild register address setting register (lower) ch. 1	R/W	00000000_B
$0F85_H$	WRDR1	Wild register data setting register ch. 1	R/W	00000000_B
$0F86_H$	WRARH2	Wild register address setting register (upper) ch. 2	R/W	00000000_B
$0F87_H$	WRARL2	Wild register address setting register (lower) ch. 2	R/W	00000000_B
$0F88_H$	WRDR2	Wild register data setting register ch. 2	R/W	00000000_B
$0F89_H$ to $0F91_H$	—	(Disabled)	—	—
$0F92_H$	T01CR0	8/16-bit composite timer 01 status control register 0 ch. 0	R/W	00000000_B
$0F93_H$	T00CR0	8/16-bit composite timer 00 status control register 0 ch. 0	R/W	00000000_B
$0F94_H$	T01DR	8/16-bit composite timer 01 data register ch. 0	R/W	00000000_B
$0F95_H$	T00DR	8/16-bit composite timer 00 data register ch. 0	R/W	00000000_B
$0F96_H$	TMCR0	8/16-bit composite timer 00/01 timer mode control register ch. 0	R/W	00000000_B
$0F97_H$	T11CR0	8/16-bit composite timer 11 status control register 0 ch. 1	R/W	00000000_B
$0F98_H$	T10CR0	8/16-bit composite timer 10 status control register 0 ch. 1	R/W	00000000_B
$0F99_H$	T11DR	8/16-bit composite timer 11 data register ch. 1	R/W	00000000_B
$0F9A_H$	T10DR	8/16-bit composite timer 10 data register ch. 1	R/W	00000000_B
$0F9B_H$	TMCR1	8/16-bit composite timer 10/11 timer mode control register ch. 1	R/W	00000000_B
$0F9C_H$ to $0FBB_H$	—	(Disabled)	—	—

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Address	Register abbreviation	Register name	R/W	Initial value
$0FBC_H$	BGR1	LIN-UART baud rate generator register 1	R/W	00000000_B
$0FBD_H$	BGR0	LIN-UART baud rate generator register 0	R/W	00000000_B
$0FBE_H$	PSSR0	UART/SIO dedicated baud rate generator prescaler select register ch. 0	R/W	00000000_B
$0FBF_H$	BRSR0	UART/SIO dedicated baud rate generator baud rate setting register ch. 0	R/W	00000000_B
$0FC0_H$ to $0FC2_H$	—	(Disabled)	—	—
$0FC3_H$	AIDRL	A/D input disable register (lower)	R/W	00000000_B
$0FC4_H$ to $0FE3_H$	—	(Disabled)	—	—
$0FE4_H$	CRTH	Main CR clock trimming register (upper)	R/W	$0XXXXXXX_B$
$0FE5_H$	CRTL	Main CR clock trimming register (lower)	R/W	$00XXXXXX_B$
$0FE6_H$, $0FE7_H$	—	(Disabled)	—	—
$0FE8_H$	SYSC	System configuration register	R/W	11000001_B
$0FE9_H$	CMCR	Clock monitoring control register	R/W	00000000_B
$0FEA_H$	CMDR	Clock monitoring data register	R	00000000_B
$0FEB_H$	WDTH	Watchdog timer selection ID register (upper)	R	XXXXXXXX_B
$0FEC_H$	WDTL	Watchdog timer selection ID register (lower)	R	XXXXXXXX_B
$0FED_H$	—	(Disabled)	—	—
$0FEE_H$	ILSR	Input level select register	R/W	00000000_B
$0FEF_H$ to $0FFF_H$	—	(Disabled)	—	—

R/W access symbols
- R/W : Readable / Writable
- R : Read only
- W : Write only

Initial value symbols
- 0 : The initial value of this bit is “0”.
- 1 : The initial value of this bit is “1”.
- X : The initial value of this bit is indeterminate.

Note: Do not write to an address that is “(Disabled)”. If a “(Disabled)” address is read, an indeterminate value is returned.

13. Interrupt Source Table

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower		
External interrupt ch. 4	IRQ00	$FFFA_H$	$FFFB_H$	L00 [1:0]	High
External interrupt ch. 5	IRQ01	$FFF8_H$	$FFF9_H$	L01 [1:0]	
External interrupt ch. 2	IRQ02	$FFF6_H$	$FFF7_H$	L02 [1:0]	
External interrupt ch. 6					
External interrupt ch. 3	IRQ03	$FFF4_H$	$FFF5_H$	L03 [1:0]	
External interrupt ch. 7					
LVD interrupt	IRQ04	$FFF2_H$	$FFF3_H$	L04 [1:0]	
UART/SIO ch. 0					
8/16-bit composite timer ch. 0 (lower)	IRQ05	$FFF0_H$	$FFF1_H$	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	$FFEE_H$	$FFEF_H$	L06 [1:0]	
LIN-UART (reception)	IRQ07	$FFEC_H$	$FFED_H$	L07 [1:0]	
LIN-UART (transmission)	IRQ08	$FFEA_H$	$FFEB_H$	L08 [1:0]	
—	IRQ09	$FFE8_H$	$FFE9_H$	L09 [1:0]	
I^2C ch. 1	IRQ10	$FFE6_H$	$FFE7_H$	L10 [1:0]	
—	IRQ11	$FFE4_H$	$FFE5_H$	L11 [1:0]	
—	IRQ12	$FFE2_H$	$FFE3_H$	L12 [1:0]	
—	IRQ13	$FFE0_H$	$FFE1_H$	L13 [1:0]	
8/16-bit composite timer ch. 1 (upper)	IRQ14	$FFDE_H$	$FFDF_H$	L14 [1:0]	
—	IRQ15	$FFDC_H$	$FFDD_H$	L15 [1:0]	
I^2C ch. 0	IRQ16	$FFDA_H$	$FFDB_H$	L16 [1:0]	
—	IRQ17	$FFD8_H$	$FFD9_H$	L17 [1:0]	
8/10-bit A/D converter	IRQ18	$FFD6_H$	$FFD7_H$	L18 [1:0]	
Time-base timer	IRQ19	$FFD4_H$	$FFD5_H$	L19 [1:0]	
Watch prescaler	IRQ20	$FFD2_H$	$FFD3_H$	L20 [1:0]	
—	IRQ21	$FFD0_H$	$FFD1_H$	L21 [1:0]	
8/16-bit composite timer ch. 1 (lower)	IRQ22	$FFCE_H$	$FFCF_H$	L22 [1:0]	
Flash memory	IRQ23	$FFCC_H$	$FFCD_H$	L23 [1:0]	Low

14. Electrical Characteristics

14.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} − 0.3	V_{SS} + 4.0	V	
Input voltage*1	V_{I1}	V_{SS} − 0.3	V_{SS} + 4.0	V	Other than P14 and P15*2
	V_{I2}	V_{SS} − 0.3	V_{SS} + 6.0	V	P14 and P15*2
Output voltage*1	V_O	V_{SS} − 0.3	V_{SS} + 4.0	V	*2
Maximum clamp current	I_{CLAMP}	−2	+2	mA	Applicable to specific pins*3
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to specific pins*3
"L" level maximum output current	I_{OL1}	—	15	mA	Other than P05, P06, P62 and P63
	I_{OL2}		15		P05, P06, P62 and P63
"L" level average current	I_{OLAV1}	—	4	mA	Other than P05, P06, P62 and P63 Average output current = operating current × operating ratio (1 pin)
	I_{OLAV2}		12		P05, P06, P62 and P63 Average output current = operating current × operating ratio (1 pin)
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
"L" level total average output current	ΣI_{OLAV}	—	50	mA	Total average output current = operating current × operating ratio (Total number of pins)
"H" level maximum output current	I_{OH1}	—	−15	mA	Other than P05, P06, P62 and P63
	I_{OH2}		−15		P05, P06, P62 and P63
"H" level average current	I_{OHAV1}	—	−4	mA	Other than P05, P06, P62 and P63 Average output current = operating current × operating ratio (1 pin)
	I_{OHAV2}		−8		P05, P06, P62 and P63 Average output current = operating current × operating ratio (1 pin)
"H" level total maximum output current	ΣI_{OH}	—	−100	mA	
"H" level total average output current	ΣI_{OHAV}	—	−50	mA	Total average output current = operating current × operating ratio (Total number of pins)
Power consumption	P_d	—	320	mW	
Operating temperature	T_A	−40	+85	°C	
Storage temperature	T_{stg}	−55	+150	°C	

(Continued)

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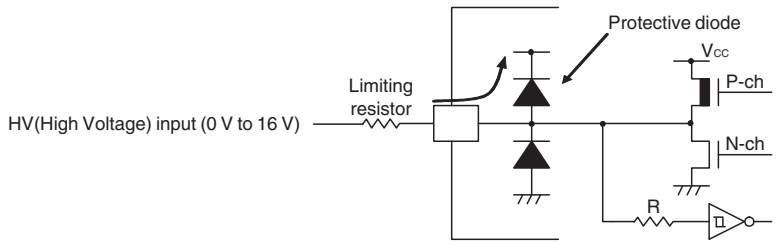
*1: The parameter is based on V_{SS} = 0.0 V.

*2: V_{I1}, V_{I2} and V_O must not exceed V_{CC} + 0.3 V. V_{I1} and V_{I2} must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the I_{CLAMP} rating is used instead of the V_{I1} and V_{I2} ratings.

*3: Applicable to the following pins: P00 to P07, P15, P16, P62 to P64, PF0, PF1, PG0 to PG2

- Use under recommended operating conditions.
- Use with DC voltage (current).
- The HV (High Voltage) signal is an input signal exceeding the V_{CC} voltage. Always connect a limiting resistor between the HV (High Voltage) signal and the microcontroller before applying the HV (High Voltage) signal.
- The value of the limiting resistor should be set to a value at which the current to be input to the microcontroller pin when the HV (High Voltage) signal is input is below the standard value, irrespective of whether the current is transient current or stationary current.
- When the microcontroller drive current is low, such as in low power consumption modes, the HV (High Voltage) input potential may pass through the protective diode to increase the potential of the V_{CC} pin, affecting other devices.
- If the HV (High Voltage) signal is input when the microcontroller power supply is off (not fixed at 0 V), since power is supplied from the pins, incomplete operations may be executed.
- If the HV (High Voltage) input is input after power-on, since power is supplied from the pins, the voltage of power supply may not be sufficient to enable a power-on reset.
- Do not leave the HV (High Voltage) input pin unconnected.
- Example of a recommended circuit

  • Input/Output equivalent circuit



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

14.2 Recommended Operating Conditions

(V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks	
		Min	Max			
Power supply voltage	V_{CC}	1.8*1*2*3	3.6	V	In normal operation, T_A = −10°C to +85°C	Other than on-chip debug mode
		2.0	3.6		In normal operation, T_A = −40°C to +85°C	
		1.5	3.6		Hold condition in stop mode	
		2.7	3.6		In normal operation	On-chip debug mode
		1.5	3.6		Hold condition in stop mode	
Operating temperature	T_A	−40	+85	°C	Other than on-chip debug mode	
		+5	+35		On-chip debug mode	

*1: This value varies depending on the operating frequency, the machine clock and the analog guaranteed range.

*2: This value is initially 2.03 V when the low-voltage detection reset is used.

*3: The threshold voltage can be set to 2.03 V, 2.55 V or 3.10 V by using the software.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

14.3 DC Characteristics

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHI1}	P04, P16, P17	*1	0.7 V_{CC}	—	V_{CC} + 0.3	V	When CMOS input level is selected
	V_{IHI2}	P14, P15	*1	0.7 V_{CC}	—	V_{SS} + 5.5	V	When CMOS input level is selected
	V_{IHS1}	P00 to P07, P12, P16, P17, P60 to P64, PF0, PF1, PG0 to PG2	*1	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
	V_{IHS2}	P14, P15	*1	0.8 V_{CC}	—	V_{SS} + 5.5	V	Hysteresis input
	V_{IHM}	PF2	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
"L" level input voltage	V_{IL}	P04, P14 to P17	*1	V_{SS} – 0.3	—	0.3 V_{CC}	V	When CMOS input level is selected
	V_{ILS}	P00 to P07, P12, P14 to P17, P62 to P64, PF0, PF1, PG0 to PG2	*1	V_{SS} – 0.3	—	0.2 V_{CC}	V	Hysteresis input
	V_{ILM}	PF2	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	Hysteresis input
Open-drain output application voltage	V_{D1}	P12	—	V_{SS} – 0.3	—	V_{SS} + 5.5	V	
	V_{D2}	P14, P15	—	V_{SS} – 0.3	—	V_{SS} + 5.5	V	
	V_{D3}	P16, P17	—	V_{SS} – 0.3	—	V_{SS} + 3.6	V	In I^2C mode
"H" level output voltage	V_{OH1}	Output pins other than P05, P06, P12, P62, P63	I_{OH} = –4 mA	V_{CC} – 0.5	—	—	V	
	V_{OH2}	P05, P06, P62 and P63	I_{OH} = –8 mA	V_{CC} – 0.5	—	—	V	
"L" level output voltage	V_{OL1}	Output pins other than P05, P06, P62, P63	I_{OL} = 4 mA	—	—	0.4	V	
	V_{OL2}	P05, P06, P62, P63	I_{OL} = 12 mA	—	—	0.4	V	
Input leak current (Hi-Z output leak current)	I_{LI}	All input pins	0.0 V < V_I < V_{CC}	–5	—	+5	µA	When pull-up resistance is disabled
Pull-up resistance	R_{PULL}	P00 to P07, PG1, PG2	V_I = 0 V	25	50	100	kΩ	When pull-up resistance is enabled
Input capacitance	C_{IN}	Other than V_{CC} and V_{SS}	f = 1 MHz	—	5	15	pF	

(Continued)

(V_{CC} = 1.8 V to 3.6 V, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ*3	Max		
Power supply current*2	I_{CC}	V_{CC} (External clock operation)	F_{CH} = 32 MHz F_{MP} = 16 MHz Main clock mode (divided by 2)	—	11.2	20	mA	Flash memory product (except writing and erasing)
				—	26.2	38	mA	Flash memory product (at writing and erasing)
				—	13.3	23.4	mA	At A/D conversion
	I_{CCS}		F_{CH} = 32 MHz F_{MP} = 16 MHz Main sleep mode (divided by 2)	—	5.2	9.6	mA	
	I_{CCL}		F_{CL} = 32 kHz F_{MPL} = 16 kHz Subclock mode (divided by 2) T_A = +25°C	—	15	35	µA	
	I_{CCLS}		F_{CL} = 32 kHz F_{MPL} = 16 kHz Subsleep mode (divided by 2) T_A = +25°C	—	5	15	µA	
	I_{CCT}		F_{CL} = 32 kHz Watch mode Main stop mode T_A = +25°C	—	1	10	µA	
	I_{CCMCR}	V_{CC}	F_{CRH} = 12.5 MHz F_{MP} = 12.5 MHz Main CR clock mode	—	9	15	mA	
	I_{CCSCR}		Sub-CR clock mode (divided by 2) T_A = +25°C	—	77	160	µA	
	I_{CCTS}	V_{CC} (External clock operation)	F_{CH} = 32 MHz Time-base timer mode	—	1.1	3	mA	
	I_{CCH}		Substop mode T_A = +25°C	—	0.1	5	µA	

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(V_{CC} = 1.8 V to 3.6 V, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ*3	Max		
Power supply current*2	I_{LVD}	V_{CC}	Current consumption for low-voltage detection circuit only	—	6.4	32	µA	
	I_{CRH}		Current consumption for the main CR oscillator	—	0.25	0.6	mA	
	I_{CRL}		Current consumption for the sub-CR oscillator oscillating at 100 kHz	—	20	72	µA	

*1: The input levels of P04 and P14 to P17 can be switched between “CMOS input level” and “hysteresis input level”. The input level selection register (ILSR) is used to switch between the two input levels.

*2: • The power supply current is determined by the external clock. When the low-voltage detection option is selected, the power-supply current will be the sum of adding the current consumption of the low-voltage detection circuit (I_{LVD}) to one of the value from I_{CC} to I_{CCH}. In addition, when both the low-voltage detection option and the CR oscillator are selected, the power supply current will be the sum of adding up the current consumption of the low-voltage detection circuit, the current consumption of the CR oscillators (I_{CRH}, I_{CRL}) and a specified value. In on-chip debug mode, the CR oscillator (I_{CRH}) and the low-voltage detection circuit are always enabled, and current consumption therefore increases accordingly.

- See "AC Characteristics: Clock Timing" for F_{CH} and F_{CL}.
- See "AC Characteristics: Source Clock/Machine Clock" for F_{MP} and F_{MPL}.

*3: V_{CC} = 3.0 V, T_A = +25°C

14.4 AC Characteristics

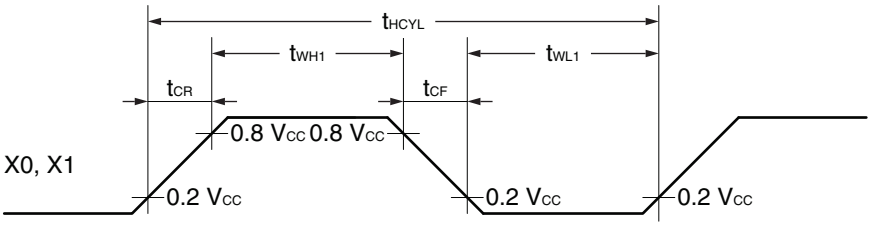
14.4.1 Clock Timing

(V_{CC} = 1.8 V to 3.6 V, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	1	—	16.25	MHz	When the main oscillation circuit is used
		X0	X1: open	1	—	12	MHz	When the main external clock is used
		X0, X1	*	1	—	32.5	MHz	
	F_{CRH}	—	—	12.25	12.5	12.75	MHz	When the main CR clock is used T_A = −10 °C to +85 °C
				9.8	10	10.2	MHz	
				7.84	8	8.16	MHz	
				0.98	1	1.02	MHz	
		—	—	12.1875	12.5	12.8125	MHz	When the main CR clock is used T_A = −40 °C to −10 °C
				9.75	10	10.25	MHz	
				7.8	8	8.2	MHz	
				0.975	1	1.025	MHz	
	F_{CL}	X0A, X1A	—	—	32.768	—	kHz	When the sub-oscillation circuit or the sub-external clock is used
	F_{CRL}	—	—	50	100	200	kHz	When the sub-CR clock is used
Clock cycle time	t_{HCYL}	X0, X1	—	61.5	—	1000	ns	When the main oscillation circuit is used
		X0	X1: open	83.4	—	1000	ns	When the main external clock is used
		X0, X1	*	30.8	—	1000	ns	
	t_{LCYL}	X0A, X1A	—	—	30.5	—	µs	When the sub-oscillation circuit or the sub-external clock is used
Input clock pulse width	t_{WH1} t_{WL1}	X0	X1: open	33.4	—	—	ns	When the external clock is used, the duty ratio should range between 40% and 60%.
		X0, X1	*	12.4	—	—	ns	
	t_{WH2} t_{WL2}	X0A	—	—	15.2	—	µs	
Input clock rise time and fall time	t_{CR} t_{CF}	X0	X1: open	—	—	5	ns	When the external clock is used
		X0, X1	*	—	—	5	ns	
CR oscillation start time	t_{CRHWK}	—	—	—	—	250	µs	When the main CR clock is used
	t_{CRLWK}	—	—	—	—	10	µs	When the sub-CR clock is used

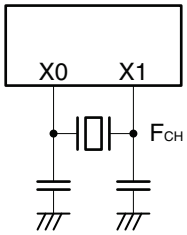
*: The external clock signal is input to X0 and the inverted external clock signal to X1.

- Input waveform generated when an external clock (main clock) is used

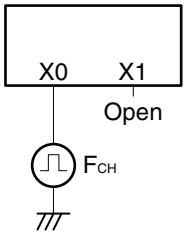


- Figure of main clock input port external connection

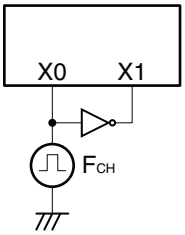
When a crystal oscillator or a ceramic oscillator is used



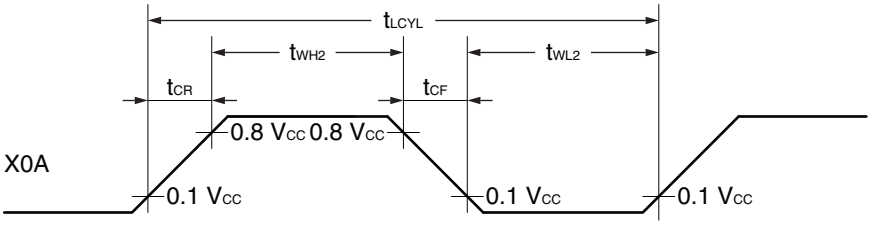
When the external clock is used (X1 is open)



When the external clock is used

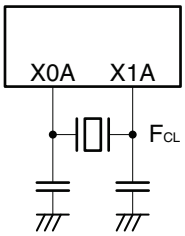


- Input waveform generated when an external clock (subclock) is used

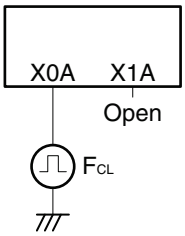


- Figure of subclock input port external connection

When a crystal oscillator or a ceramic oscillator is used



When the external clock is used



14.4.2 Source Clock/Machine Clock

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Source clock cycle time*1	t_{SCLK}	—	61.5	—	2000	ns	When the main external clock is used Min: F_{CH} = 32.5 MHz, divided by 2 Max: F_{CH} = 1 MHz, divided by 2
			80	—	1000	ns	When the main CR clock is used Min: F_{CRH} = 12.5 MHz Max: F_{CRH} = 1 MHz
			—	61	—	µs	When the sub-oscillation clock is used F_{CL} = 32.768 kHz, divided by 2
			—	20	—	µs	When the sub-CR clock is used F_{CRL} = 100 kHz, divided by 2
Source clock frequency	F_{SP}	—	0.5	—	16.25	MHz	When the main oscillation clock is used
			1	—	12.5	MHz	When the main CR clock is used
	F_{SPL}		—	16.384	—	kHz	When the sub-oscillation clock is used
			—	50	—	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz, divided by 2
Machine clock cycle time*2 (minimum instruction execution time)	t_{MCLK}	—	61.5	—	32000	ns	When the main oscillation clock is used Min: F_{SP} = 16.25 MHz, no division Max: F_{SP} = 0.5 MHz, divided by 16
			80	—	16000	ns	When the main CR clock is used Min: F_{SP} = 12.5 MHz Max: F_{SP} = 1 MHz, divided by 16
			61	—	976.5	µs	When the sub-oscillation clock is used Min: F_{SPL} = 16.384 kHz, no division Max: F_{SPL} = 16.384 kHz, divided by 16
			20	—	320	µs	When the sub-CR clock is used Min: F_{SPL} = 50 kHz, no division Max: F_{SPL} = 50 kHz, divided by 16
Machine clock frequency	F_{MP}	—	0.031	—	16.25	MHz	When the main oscillation clock is used
			0.0625	—	12.5	MHz	When the main CR clock is used
	F_{MPL}		1.024	—	16.384	kHz	When the sub-oscillation clock is used
			3.125	—	50	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz

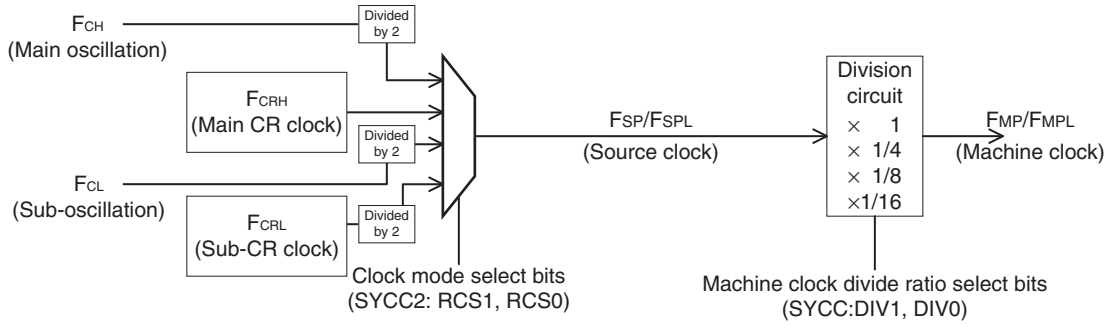
*1: This is the clock before it is divided according to the division ratio set by the machine clock division ratio selection bits (SYCC:DIV1, DIV0]). This source clock is divided to become a machine clock according to the division ratio set by the machine clock division ratio selection bits (SYCC:DIV1, DIV0]). In addition, a source clock can be selected from the following.

- Main clock divided by 2
- Main CR clock
- Subclock divided by 2
- Sub-CR clock divided by 2

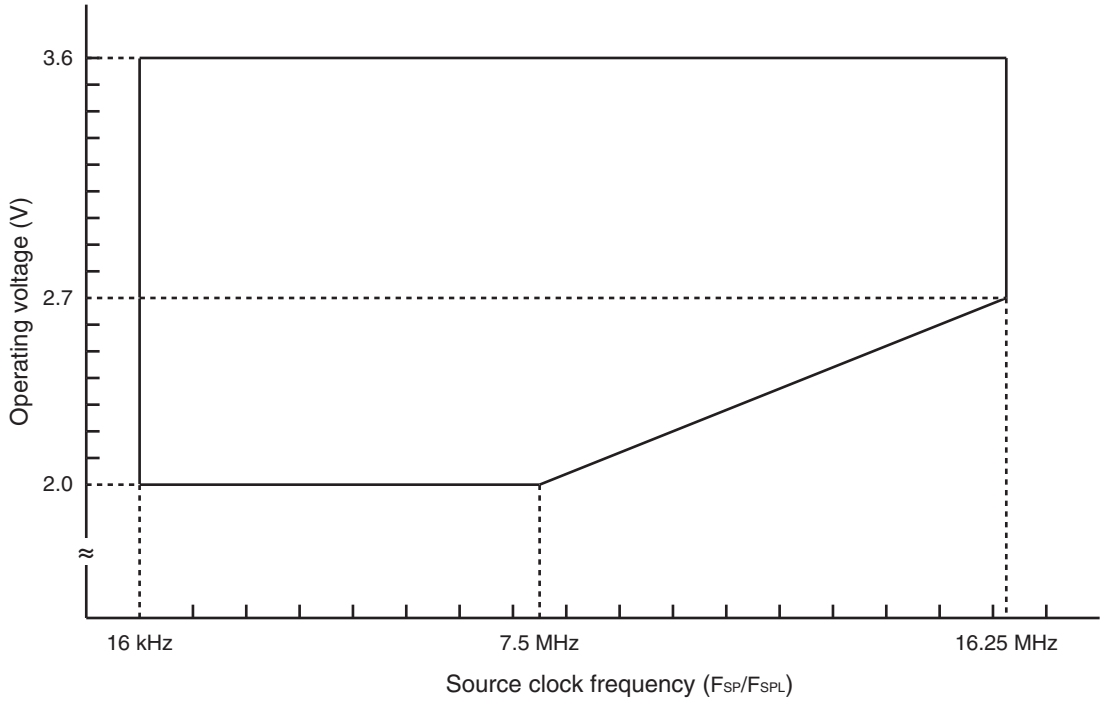
*2: This is the operating clock of the microcontroller. A machine clock can be selected from the following.

- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

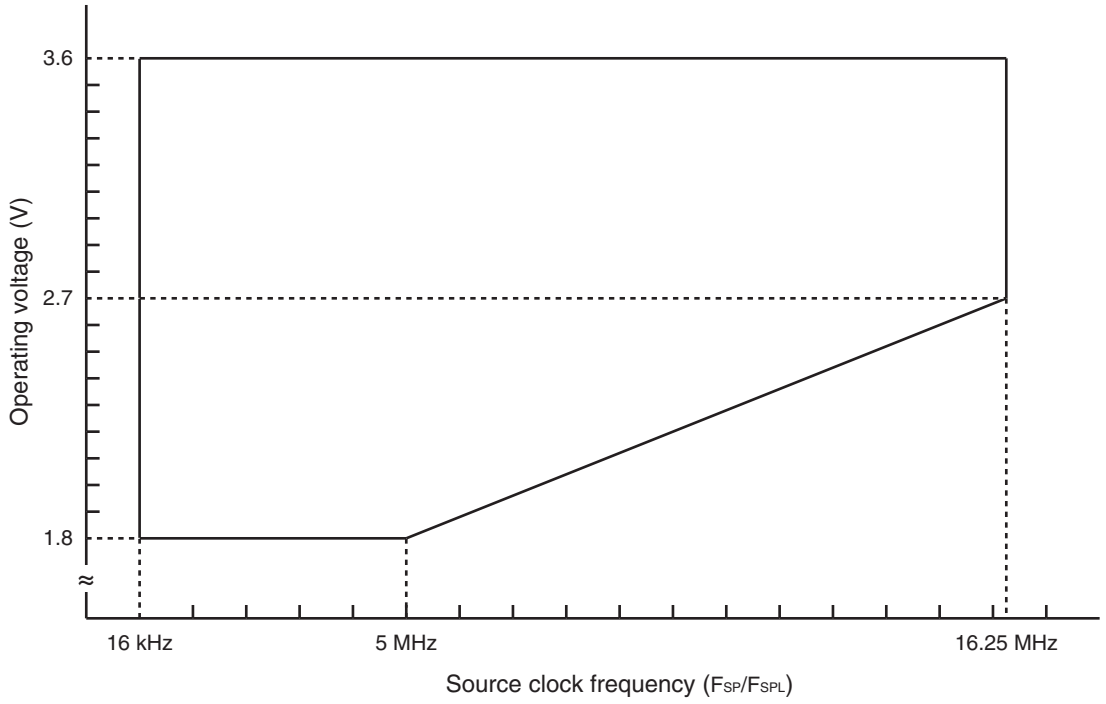
- Schematic diagram of the clock generation block



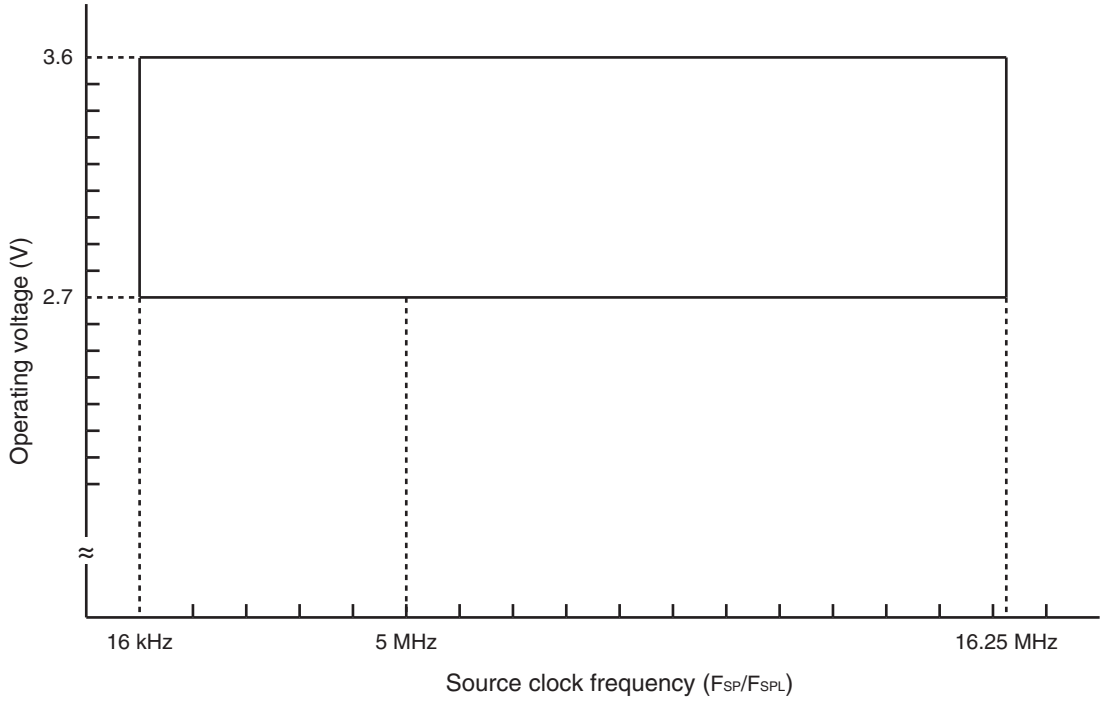
- Operating voltage - Operating frequency (When T_A = −40°C to +85°C)
  Without the on-chip debug function



- Operating voltage - Operating frequency (When T_A = −10°C to +85°C)
  Without the on-chip debug function



- Operating voltage - Operating frequency (When T_A = −40°C to +85°C)
  With the on-chip debug function



14.4.3 External Reset

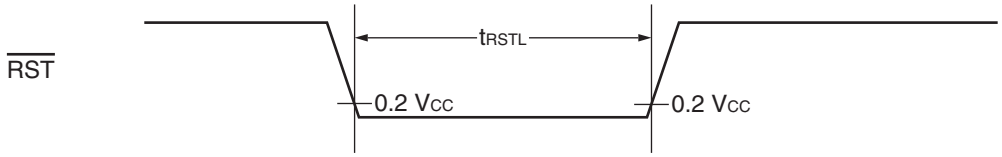
(V_{CC} = 3.0 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{RST}$ "L" level pulse width	t_{RSTL}	2 t_{MCLK}*1	—	ns	In normal operation
		Oscillation time of the oscillator*2 + 100	—	µs	In stop mode, subclock mode, sub-sleep mode, watch mode, and power-on
		100	—	µs	In time-base timer mode

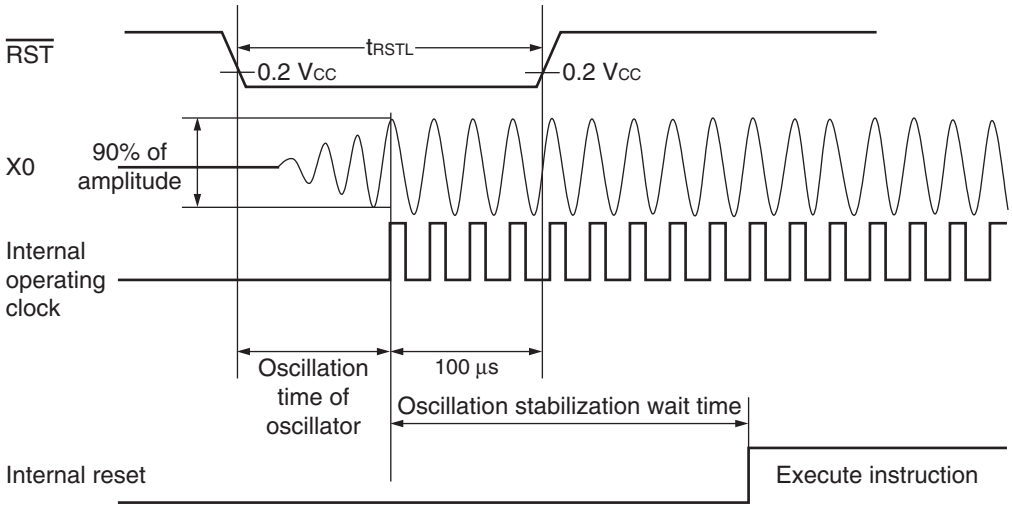
*1: See "Source Clock/Machine Clock" for t_{MCLK}.

*2: The oscillation time of an oscillator is the time for it to reach 90% of its amplitude. The crystal oscillator has an oscillation time of between several ms and tens of ms. The ceramic oscillator has an oscillation time of between hundreds of µs and several ms. The external clock has an oscillation time of 0 ms. The CR oscillator clock has an oscillation time of between several µs and several ms.

- In normal operation



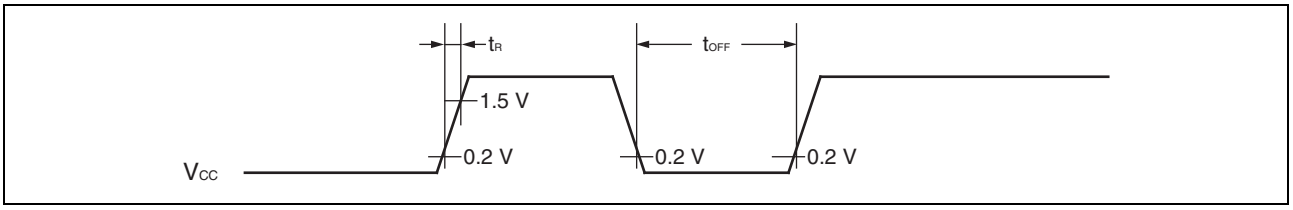
- In stop mode, subclock mode, subsleep mode, watch mode and power-on



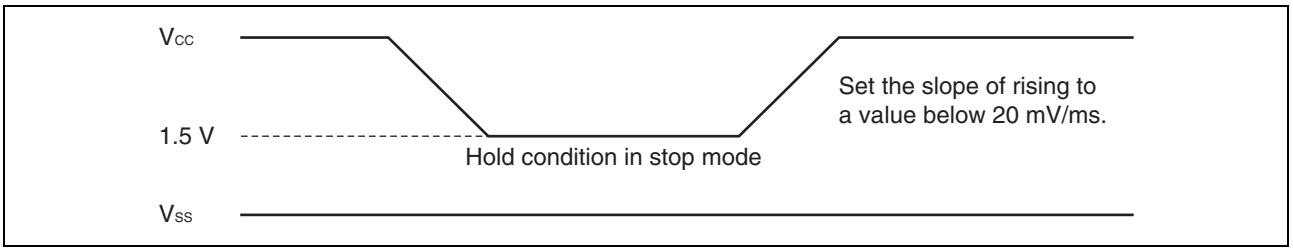
14.4.4 Power-on Reset

(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	—	—	50	ms	
Power supply cutoff time	t_{OFF}	—	1	—	ms	Wait time until power-on



Note: A sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during the operation, set the slope of rising to a value below within 20 mV/ms as shown below.

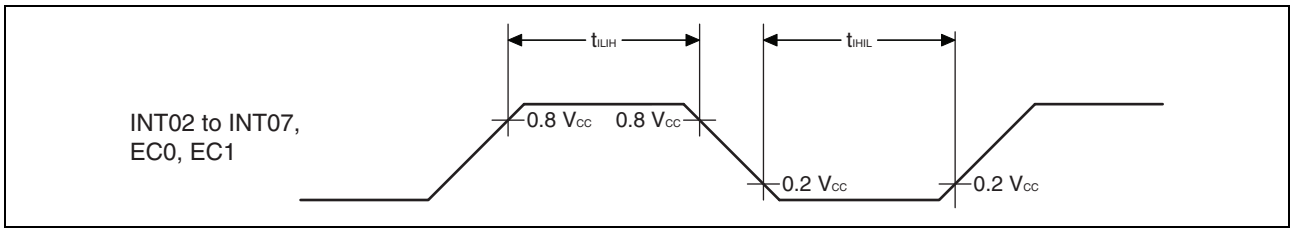


14.4.5 Peripheral Input Timing

(V_{CC} = 3.0 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Peripheral input “H” pulse width	t_{ILIH}	INT02 to INT07, EC0, EC1	2 t_{MCLK}*	—	ns
Peripheral input “L” pulse width	t_{IHIL}		2 t_{MCLK}*	—	ns

*: See “Source Clock/Machine Clock” for t_{MCLK}.



14.4.6 LIN-UART Timing

Sampling is executed at the rising edge of the sampling clock*1, and serial clock delay is disabled*2.
(ESCR register: SCES bit = 0, ECCR register: SCDE bit = 0)

(V_{CC} = 3.0 V to 3.6 V, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

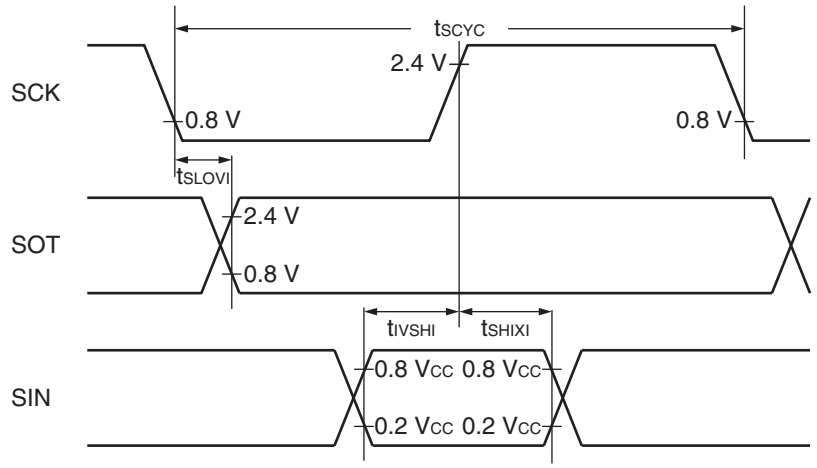
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK, SOT		−95	+95	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK	External clock operation output pin: C_L = 80 pF + 1 TTL	3 t_{MCLK}*3 − t_R	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK		t_{MCLK}*3 + 95	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCK, SOT		—	2 t_{MCLK}*3 + 95	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCK, SIN		190	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXE}	SCK, SIN		t_{MCLK}*3 + 95	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

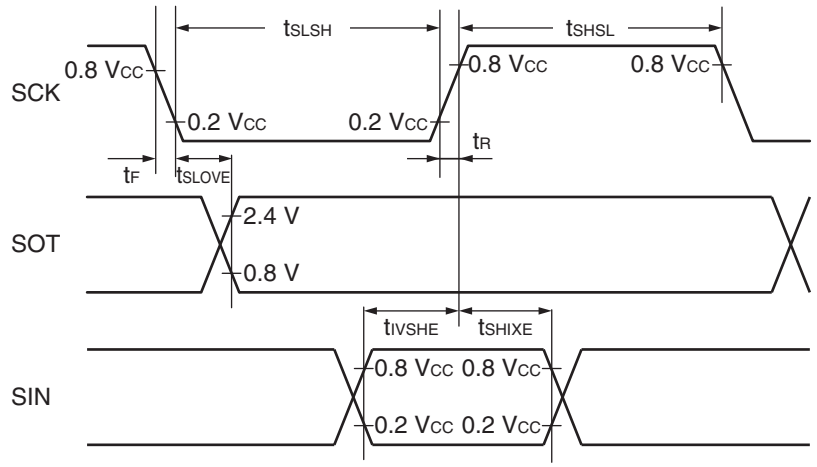
*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “Source Clock/Machine Clock” for t_{MCLK}.

- Internal shift clock mode



- External shift clock mode



Sampling is executed at the falling edge of the sampling clock*1, and serial clock delay is disabled*2.
(ESCR register: SCES bit = 1, ECCR register: SCDE bit = 0)

(V_{CC} = 3.0 V to 3.6 V, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

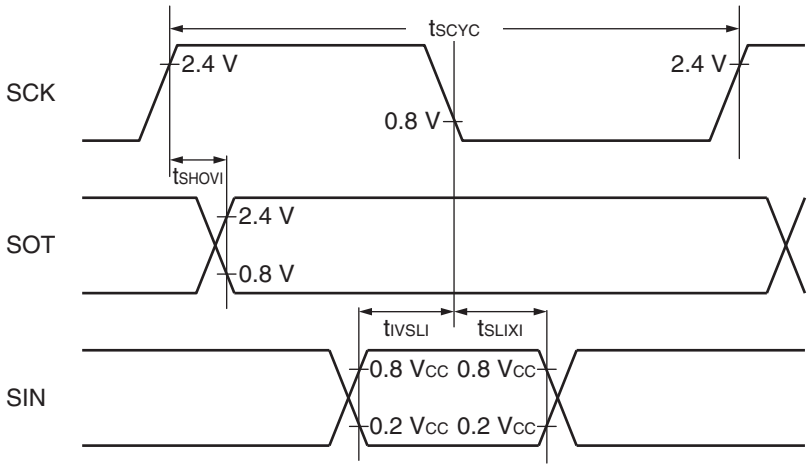
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK, SOT		−95	+95	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK	External clock operation output pin: C_L = 80 pF + 1 TTL	3 t_{MCLK}*3 − t_R	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK		t_{MCLK}*3 + 95	—	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCK, SOT		—	2 t_{MCLK}*3 + 95	ns
Valid SIN → SCK ↓	t_{IVSLE}	SCK, SIN		190	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXE}	SCK, SIN		t_{MCLK}*3 + 95	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

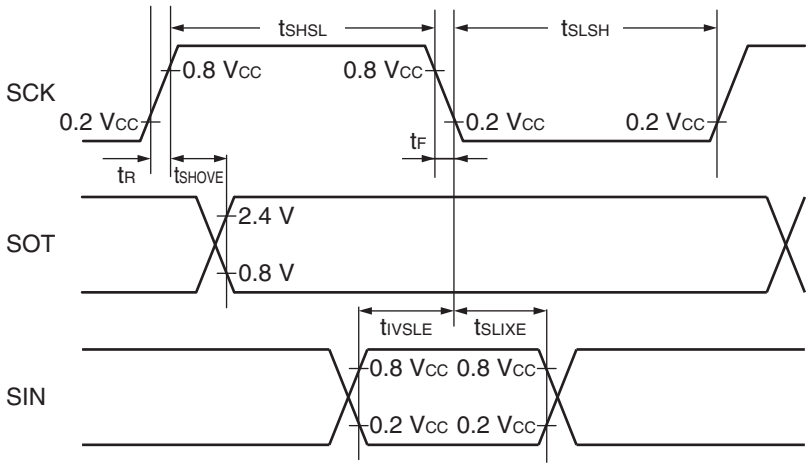
*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “Source Clock/Machine Clock” for t_{MCLK}.

- Internal shift clock mode



- External shift clock mode



Sampling is executed at the rising edge of the sampling clock*1, and serial clock delay is enabled*2.
(ESCR register: SCES bit = 0, ECCR register: SCDE bit = 1)

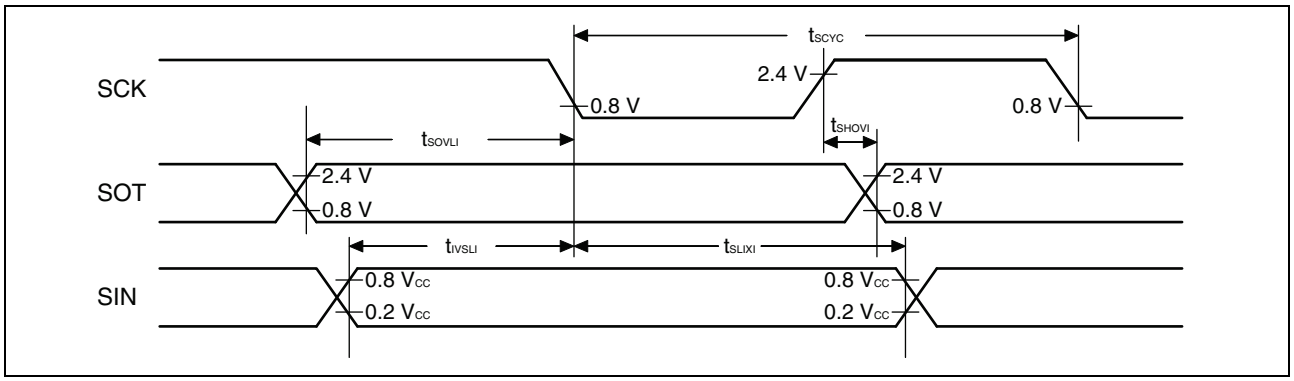
(V_{CC} = 3.0 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK, SOT		–95	+95	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCK, SOT		—	4 t_{MCLK}*3	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

*3: See “Source Clock/Machine Clock” for t_{MCLK}.



Sampling is executed at the falling edge of the sampling clock*1, and serial clock delay is enabled*2.
(ESCR register: SCES bit = 1, ECCR register: SCDE bit = 1)

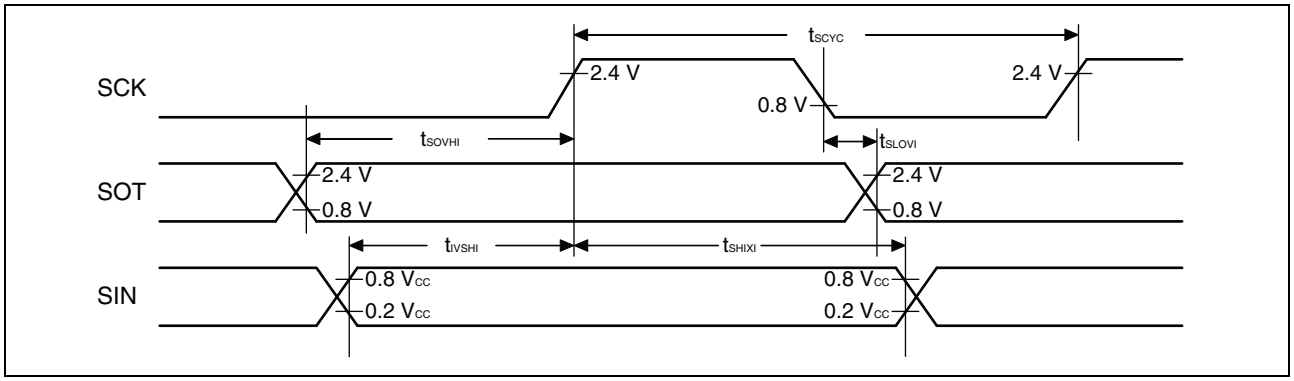
(V_{CC} = 3.0 V to 3.6 V, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK, SOT		−95	+95	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCK, SOT		—	4 t_{MCLK}*3	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

*3: See “Source Clock/Machine Clock” for t_{MCLK}.



14.4.7 Low-voltage Detection

(V_{SS} = 0.0 V, V_{CC} = 1.8 V to 3.6 V, T_A = –40°C to +85°C)

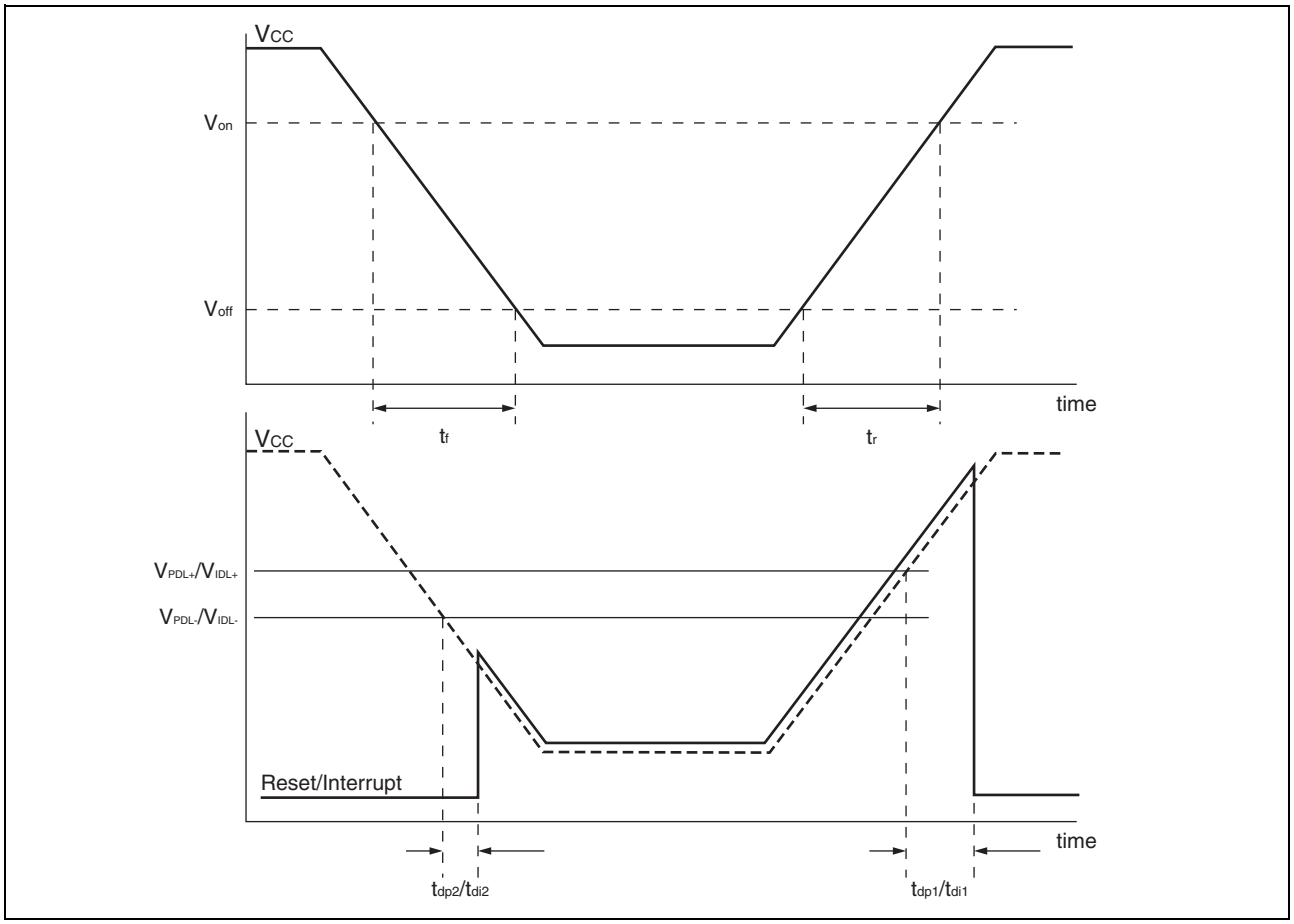
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power release voltage 0	V_{PDL0+}	1.83	1.93	2.03	V	At power supply rise
Power detection voltage 0	V_{PDL0-}	1.80	1.90	2.00	V	At power supply fall
Power release voltage 1	V_{PDL1+}	2.25	2.40	2.55	V	At power supply rise
Power detection voltage 1	V_{PDL1-}	2.20	2.35	2.50	V	At power supply fall
Power release voltage 2	V_{PDL2+}	2.80	2.95	3.10	V	At power supply rise
Power detection voltage 2	V_{PDL2-}	2.70	2.85	3.00	V	At power supply fall
Interrupt release voltage 0	V_{IDL0+}	2.03	2.18	2.33	V	At power supply rise
Interrupt detection voltage 0	V_{IDL0-}	2.00	2.15	2.30	V	At power supply fall
Interrupt release voltage 1	V_{IDL1+}	2.25	2.40	2.55	V	At power supply rise
Interrupt detection voltage 1	V_{IDL1-}	2.20	2.35	2.50	V	At power supply fall
Interrupt release voltage 2	V_{IDL2+}	2.46	2.61	2.76	V	At power supply rise
Interrupt detection voltage 2	V_{IDL2-}	2.40	2.55	2.70	V	At power supply fall
Interrupt release voltage 3	V_{IDL3+}	2.67	2.82	2.97	V	At power supply rise
Interrupt detection voltage 3	V_{IDL3-}	2.60	2.75	2.90	V	At power supply fall
Interrupt release voltage 4	V_{IDL4+}	2.90	3.10	3.30	V	At power supply rise
Interrupt detection voltage 4	V_{IDL4-}	2.80	3.00	3.20	V	At power supply fall
Power supply start voltage	V_{off}	—	—	1.8	V	
Power supply end voltage	V_{on}	3.3	—	—	V	
Power supply voltage change time (at power supply rise)	t_r	3000	—	—	µs	Slope of power supply that the reset release signal generates within the rating (V_{PDL+}/V_{IDL+})

(Continued)

(Continued)

(V_{SS} = 0.0 V, V_{CC} = 1.8 V to 3.6 V, T_A = –40°C to +85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage change time (at power supply fall)	t_f	3000	—	—	µs	Slope of power supply that the reset detection signal generates within the rating (V_{PDL-}/V_{IDL-})
Power reset release delay time	t_{dp1}	10	—	300	µs	
Power reset detection delay time	t_{dp2}	—	—	150	µs	
Interrupt reset release delay time	t_{di1}	10	—	200	µs	
Interrupt reset detection delay time	t_{di2}	—	—	150	µs	



14.4.8 I^2C Timing

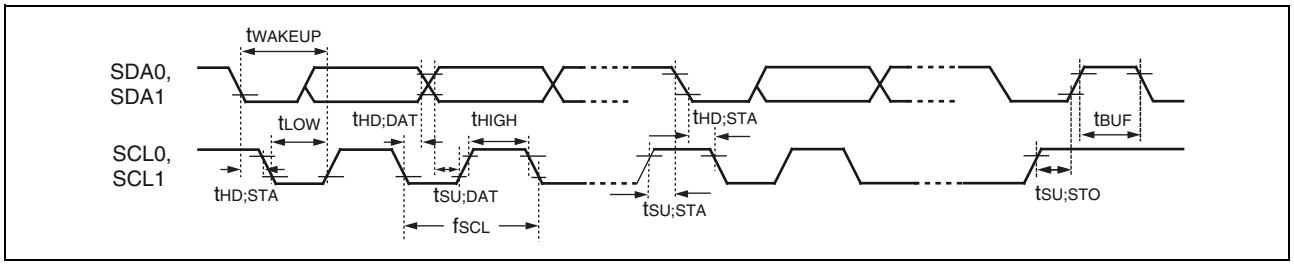
(V_{CC} = 3.0 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value				Unit
				Stan-dard-mode		Fast-mode		
				Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	SCL0, SCL1	R = 1.7 kΩ, C = 50 pF*1	0	100	0	400	kHz
(Repeated) START condition hold time SDA ↓ → SCL ↓	$t_{HD;STA}$	SCL0, SCL1, SDA0, SDA1		4.0	—	0.6	—	µs
SCL clock “L” width	t_{LOW}	SCL0, SCL1		4.7	—	1.3	—	µs
SCL clock “H” width	t_{HIGH}	SCL0, SCL1		4.0	—	0.6	—	µs
(Repeated) START condition hold time SCL ↑ → SDA ↓	$t_{SU;STA}$	SCL0, SCL1, SDA0, SDA1		4.7	—	0.6	—	µs
Data hold time SCL ↓ → SDA ↓↑	$t_{HD;DAT}$	SCL0, SCL1, SDA0, SDA1		0	3.45*2	0	0.9*3	µs
Data setup time SDA ↓↑ → SCL ↑	$t_{SU;DAT}$	SCL0, SCL1, SDA0, SDA1		0.25	—	0.1	—	µs
STOP condition setup time SCL ↑ → SDA ↑	$t_{SU;STO}$	SCL0, SCL1, SDA0, SDA1		4	—	0.6	—	µs
Bus free time between STOP condition and START condition	t_{BUF}	SCL0, SCL1, SDA0, SDA1		4.7	—	1.3	—	µs

*1: R represents the pull-up resistor of the SCL0/1 and SDA0/1 lines, and C the load capacitor of the SCL0/1 and SDA0/1 lines.

*2: The maximum $t_{HD;DAT}$ in the Standard-mode is applicable only when the time during which the device is holding the SCL signal at “L” (t_{LOW}) does not extend.

*3: A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system, provided that the condition of $t_{SU;DAT} \geq 250$ ns is fulfilled.



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(V_{CC} = 3.0 V to 3.6 V, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
SCL clock “L” width	t_{LOW}	SCL0, SCL1	R = 1.7 kΩ, C = 50 pF*1	$(2 + nm/2)t_{MCLK} - 20$	—	ns	Master mode
SCL clock “H” width	t_{HIGH}	SCL0, SCL1		$(nm/2)t_{MCLK} - 20$	$(nm/2)t_{MCLK} + 20$	ns	Master mode
START condition hold time	$t_{HD;STA}$	SCL0, SCL1, SDA0, SDA1		$(-1 + nm/2)t_{MCLK} - 20$	$(-1 + nm)t_{MCLK} + 20$	ns	Master mode Maximum value is applied when m, n = 1, 8. Otherwise, the minimum value is applied.
STOP condition setup time	$t_{SU;STO}$	SCL0, SCL1, SDA0, SDA1		$(1 + nm/2)t_{MCLK} - 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Master mode
START condition setup time	$t_{SU;STA}$	SCL0, SCL1, SDA0, SDA1		$(1 + nm/2)t_{MCLK} - 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Master mode
Bus free time between STOP condition and START condition	t_{BUF}	SCL0, SCL1, SDA0, SDA1		$(2\ nm + 4)t_{MCLK} - 20$	—	ns	
Data hold time	$t_{HD;DAT}$	SCL0, SCL1, SDA0, SDA1		$3\ t_{MCLK} - 20$	—	ns	Master mode
Data setup time	$t_{SU;DAT}$	SCL0, SCL1, SDA0, SDA1		$(-2 + nm/2)t_{MCLK} - 20$	$(-1 + nm/2)t_{MCLK} + 20$	ns	Master mode When assuming that “L” of SCL is not extended, the minimum value is applied to first bit of continuous data. Otherwise, the maximum value is applied.
Setup time between clearing interrupt and SCL rising	$t_{SU;INT}$	SCL0, SCL1		$(nm/2)t_{MCLK} - 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Minimum value is applied to interrupt at 9th SCL↓. Maximum value is applied to the interrupt at the 8th SCL↓.

(Continued)

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(V_{CC} = 3.0 V to 3.6 V, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Sym-bol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
SCL clock “L” width	t_{LOW}	SCL0, SCL1	R = 1.7 kΩ, C = 50 pF*1	4 t_{MCLK} − 20	—	ns	At reception
SCL clock “H” width	t_{HIGH}	SCL0, SCL1		4 t_{MCLK} − 20	—	ns	At reception
START condition detection	$t_{HD;STA}$	SCL0, SCL1, SDA0, SDA1		2 t_{MCLK} − 20	—	ns	Undetected when 1 t_{MCLK} is used at reception
STOP condition detection	$t_{SU;STO}$	SCL0, SCL1, SDA0, SDA1		2 t_{MCLK} − 20	—	ns	Undetected when 1 t_{MCLK} is used at reception
RESTART condition detection condition	$t_{SU;STA}$	SCL0, SCL1, SDA0, SDA1		2 t_{MCLK} − 20	—	ns	Undetected when 1 t_{MCLK} is used at reception
Bus free time	t_{BUF}	SCL0, SCL1, SDA0, SDA1		2 t_{MCLK} − 20	—	ns	At reception
Data hold time	$t_{HD;DAT}$	SCL0, SCL1, SDA0, SDA1		2 t_{MCLK} − 20	—	ns	At slave transmission mode
Data setup time	$t_{SU;DAT}$	SCL0, SCL1, SDA0, SDA1		t_{LOW} − 3 t_{MCLK} − 20	—	ns	At slave transmission mode
Data hold time	$t_{HD;DAT}$	SCL0, SCL1, SDA0, SDA1		0	—	ns	At reception
Data setup time	$t_{SU;DAT}$	SCL0, SCL1, SDA0, SDA1		t_{MCLK} − 20	—	ns	At reception
SDA↓ → SCL↑ (at wakeup function)	t_{WAKEUP}	SCL0, SCL1, SDA0, SDA1		Oscillation stabilization wait time +2 t_{MCLK} − 20	—	ns	

*1: R represents the pull-up resistor of the SCL0/1 and SDA0/1 lines, and C the load capacitor of the SCL0/1 and SDA0/1 lines.

*2:
- See “Source Clock/Machine Clock” for t_{MCLK}.
- m represents the CS4 bit and CS3 bit (bit4 and bit3) in the I^2C clock control register (ICCR0).
- n represents the CS2 bit to CS0 bit (bit2 to bit0) in the I^2C clock control register (ICCR0).
- The actual timing of I^2C is determined by the values of m and n set by the machine clock (t_{MCLK}) and the CS4 to CS0 bits in the ICCR0 register.
- Standard-mode:
  m and n can be set to values in the following range: 0.9 MHz < t_{MCLK} (machine clock) < 10 MHz.
  The usable frequencies of the machine clock are determined by the settings of m and n as shown below.
  (m, n) = (1, 8) : 0.9 MHz < $t_{MCLK} \leq$ 1 MHz
  (m, n) = (1, 22), (5, 4), (6, 4), (7, 4), (8, 4) : 0.9 MHz < $t_{MCLK} \leq$ 2 MHz
  (m, n) = (1, 38), (5, 8), (6, 8), (7, 8), (8, 8) : 0.9 MHz < $t_{MCLK} \leq$ 4 MHz
  (m, n) = (1, 98) : 0.9 MHz < $t_{MCLK} \leq$ 10 MHz
- Fast-mode:
  m and n can be set to values in the following range: 3.3 MHz < t_{MCLK} (machine clock) < 10 MHz.
  The usable frequencies of the machine clock are determined by the settings of m and n as shown below.
  (m, n) = (1, 8) : 3.3 MHz < $t_{MCLK} \leq$ 4 MHz
  (m, n) = (1, 22), (5, 4) : 3.3 MHz < $t_{MCLK} \leq$ 8 MHz
  (m, n) = (6, 4) : 3.3 MHz < $t_{MCLK} \leq$ 10 MHz

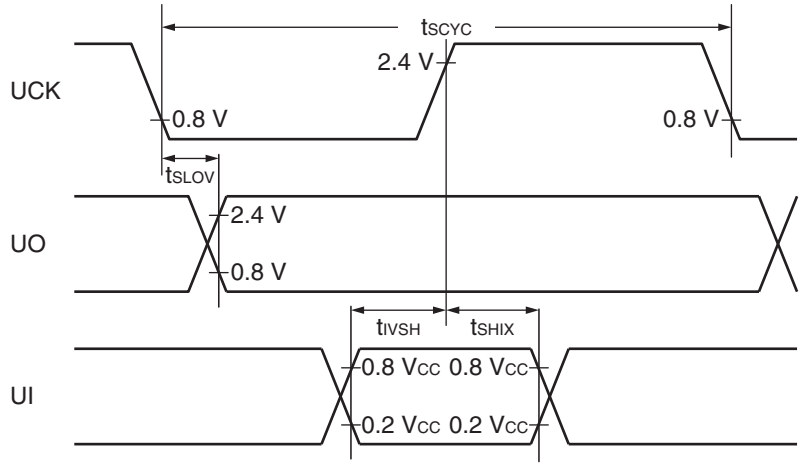
14.4.9 UART/SIO, Serial I/O Timing

(V_{CC} = 3.0 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

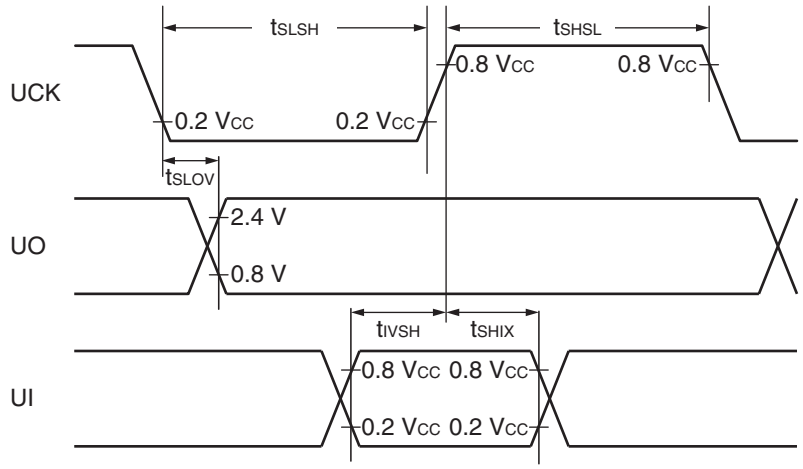
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	UCK	Internal clock operation	4 t_{MCLK}*	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK, UO		–190	+190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK, UI		2 t_{MCLK}*	—	ns
UCK ↑ → valid UI hold time	t_{SHIX}	UCK, UI		2 t_{MCLK}*	—	ns
Serial clock “H” pulse width	t_{SHSL}	UCK	External clock operation	4 t_{MCLK}*	—	ns
Serial clock “L” pulse width	t_{SLSH}	UCK		4 t_{MCLK}*	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK, UO		—	190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK, UI		2 t_{MCLK}*	—	ns
UCK ↑ → valid UI hold time	t_{SHIX}	UCK, UI		2 t_{MCLK}*	—	ns

*: See “Source Clock/Machine Clock” for t_{MCLK}.

- Internal shift clock mode



- External shift clock mode



14.5 A/D Converter

14.5.1 A/D Converter Electrical Characteristics

(V_{CC} = 1.8 V to 3.6 V, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

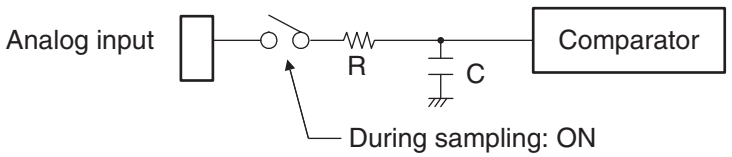
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		−3	—	+3	LSB	
Linearity error		−2.5	—	+2.5	LSB	
Differential linear error		−1.9	—	+1.9	LSB	
Zero transition voltage	V_{OT}	V_{SS} − 1.5 LSB	V_{SS} + 0.5 LSB	V_{SS} + 2.5 LSB	V	2.7 V ≤ V_{CC} ≤ 3.6 V
		V_{SS} − 0.5 LSB	V_{SS} + 1.5 LSB	V_{SS} + 3.5 LSB	V	1.8 V ≤ V_{CC} < 2.7 V
Full-scale transition voltage	V_{FST}	V_{CC} − 3.5 LSB	V_{CC} − 1.5 LSB	V_{CC} + 0.5 LSB	V	2.7 V ≤ V_{CC} ≤ 3.6 V
		V_{CC} − 2.5 LSB	V_{CC} − 0.5 LSB	V_{CC} + 1.5 LSB	V	1.8 V ≤ V_{CC} < 2.7 V
Compare time	—	1.3	—	140	µs	2.7 V ≤ V_{CC} ≤ 3.6 V
		20	—	140		1.8 V ≤ V_{CC} < 2.7 V
Sampling time	—	0.4	—	—	µs	2.7 V ≤ V_{CC} ≤ 3.6 V, with external impedance < 1.8 kΩ
		30	—	—	µs	1.8 V ≤ V_{CC} < 2.7 V, with external impedance < 14.8 kΩ
Analog input current	I_{AIN}	−0.3	—	+0.3	µA	
Analog input voltage	V_{AIN}	V_{SS}	—	V_{CC}	V	

14.5.2 Notes on Using the A/D Converter

■ External impedance of analog input and its sampling time

- The A/D converter has a sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the capacitor of the internal sample and hold circuit is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, considering the relationship between the external impedance and minimum sampling time, either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. In addition, if sufficient sampling time cannot be secured, connect a capacitor of about 0.1 µF to the analog input pin.

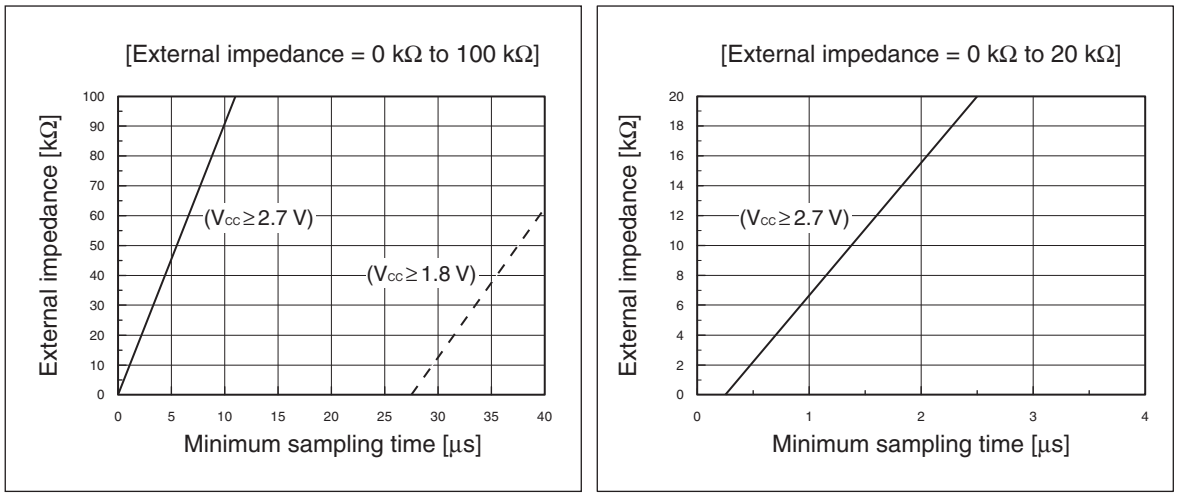
- Analog input equivalent circuit



V_{CC}	R	C
2.7 V ≤ V_{CC} ≤ 3.6 V	1.7 kΩ (Max)	14.5 pF (Max)
1.8 V ≤ V_{CC} < 2.7 V	84 kΩ (Max)	25.2 pF (Max)

Note: The values are reference values.

- Relationship between external impedance and minimum sampling time

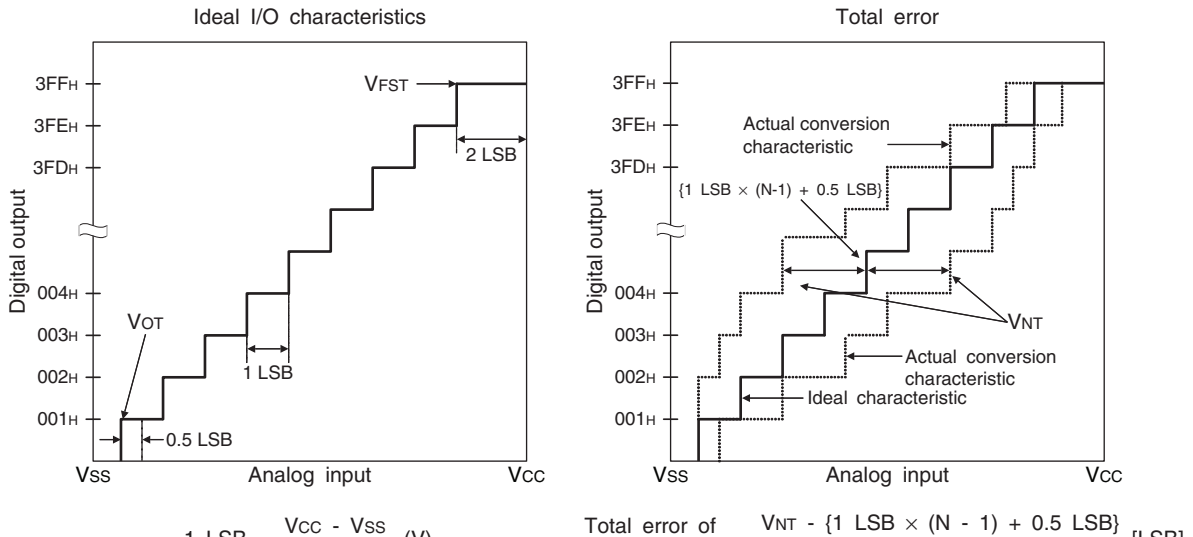


■ A/D conversion error

As $|V_{CC}–V_{SS}|$ decreases, the A/D conversion error increases proportionately.

14.5.3 Definitions of A/D Converter Terms

- Resolution
  It indicates the level of analog variation that can be distinguished by the A/D converter.
  When the number of bits is 10, analog voltage can be divided into 2^{10} = 1024.
- Linearity error (unit: LSB)
  It indicates how much an actual conversion value deviates from the straight line connecting the zero transition point (“00 0000 0000” ← → “00 0000 0001”) of a device to the full-scale transition point (“11 1111 1111” ← → “11 1111 1110”) of the same device.
- Differential linear error (unit: LSB)
  It indicates how much the input voltage required to change the output code by 1 LSB deviates from an ideal value.
- Total error (unit: LSB)
  It indicates the difference between an actual value and a theoretical value. The error can be caused by a zero transition error, a full-scale transition errors, a linearity error, a quantum error, or noise.



$$1\ \text{LSB} = \frac{V_{CC} - V_{SS}}{1024}\ (\text{V})$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

N : A/D converter digital output value

V_{NT} : Voltage at which the digital output transits from $(N - 1)_H$ to N_H

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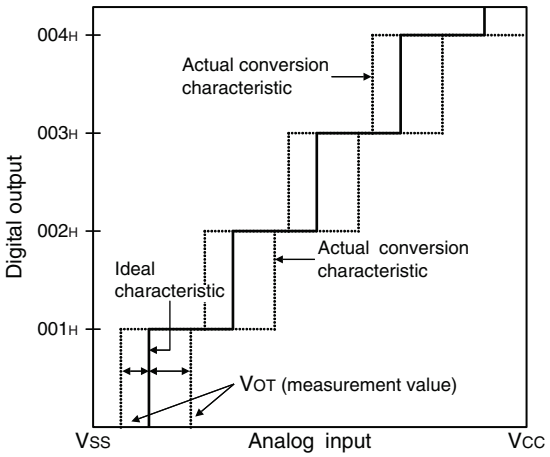
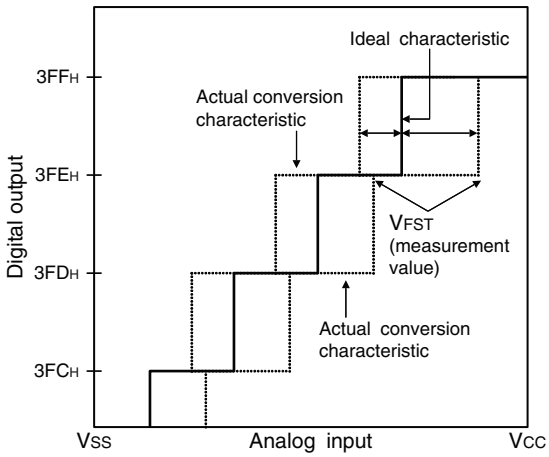
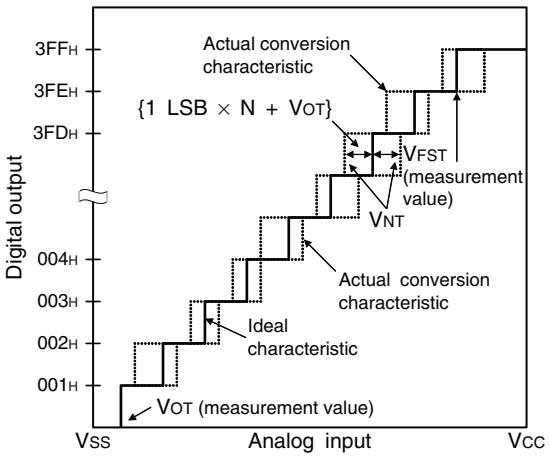
Zero transition error



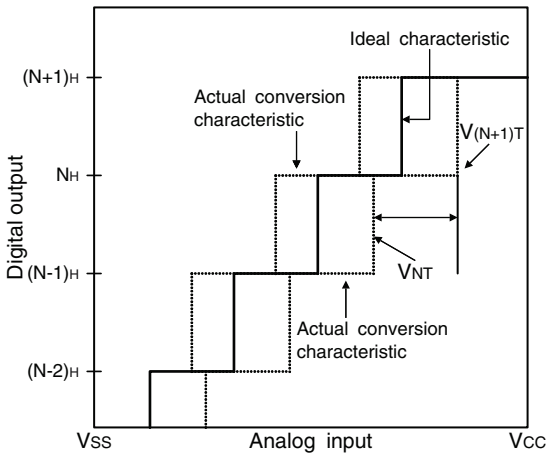
Full-scale transition error



Linearity error



Differential linearity error



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ LSB \times N + V_{OT}\}}{1\ LSB}$$

$$\text{Differential linear error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ LSB} - 1$$

N : A/D converter digital output value

V_{NT} : Voltage at which the digital output transits from $(N - 1)_H$ to N_H

V_{OT} (ideal value) = V_{SS} + 0.5 LSB [V]

V_{FST} (ideal value) = V_{CC} - 2 LSB [V]

14.6 Flash Memory Write/Erase Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time (2 Kbyte sector)	—	0.2*1	0.5*2	s	The time of writing 00_H prior to erasure is excluded.
Sector erase time (16 Kbyte sector)	—	0.5*1	7.5*2	s	The time of writing 00_H prior to erasure is excluded.
Byte writing time	—	21	6100*2	µs	System-level overhead is excluded.
Erase/write cycle	100000	—	—	cycle	
Power supply voltage at erase/write	2.7	3.0	3.6	V	
Flash memory data retention time	20*3	—	—	year	Average T_A = +85°C

*1: T_A = +25°C, V_{CC} = 3.0 V, 100000 cycles

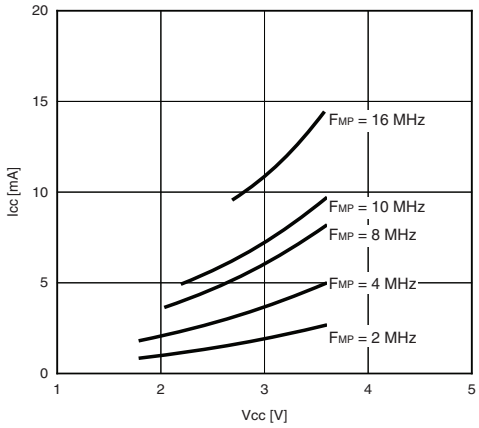
*2: T_A = +85°C, V_{CC} = 2.7 V, 100000 cycles

*3: This value is converted from the result of a technology reliability assessment. (The value is converted from the result of a high temperature accelerated test using the Arrhenius equation with the average temperature being +85°C).

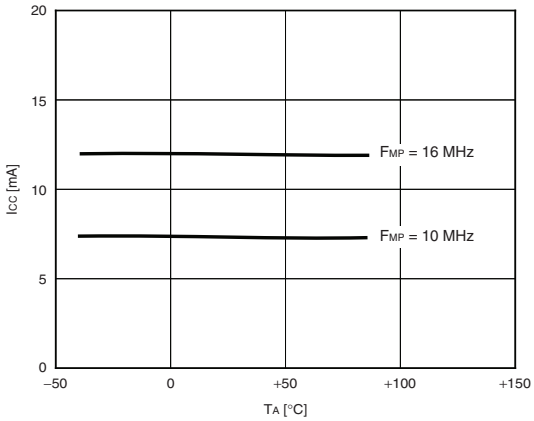
15. Sample Characteristics

■ Power supply current temperature characteristics

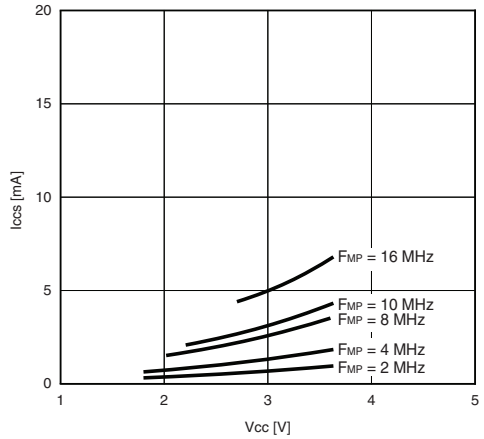
$I_{CC} - V_{CC}$
T_A = +25°C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



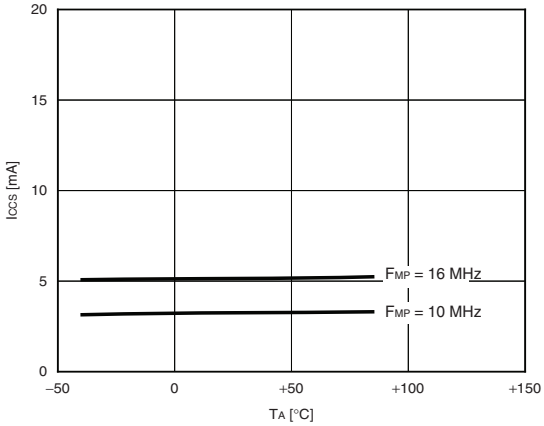
$I_{CC} - T_A$
V_{CC} = 3.0 V, F_{MP} = 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



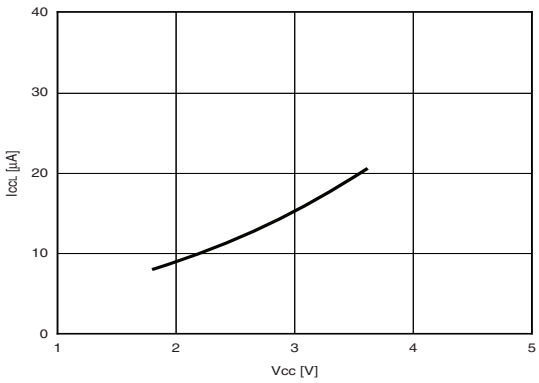
$I_{CCS} - V_{CC}$
T_A = +25°C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



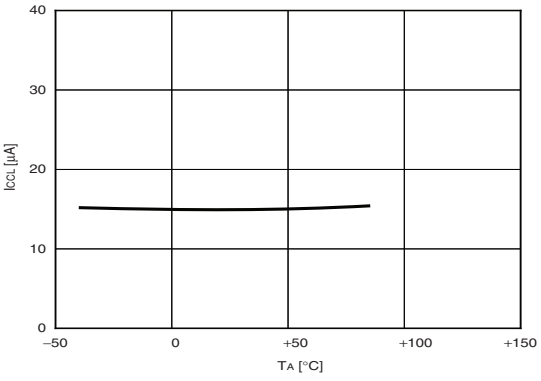
$I_{CCS} - T_A$
V_{CC} = 3.0 V, F_{MP} = 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



$I_{CCL} - V_{CC}$
T_A = +25°C, F_{MPL} = 16 kHz (divided by 2)
Subclock mode with the external clock operating



$I_{CCL} - T_A$
V_{CC} = 3.0 V, F_{MPL} = 16 kHz (divided by 2)
Subclock mode with the external clock operating



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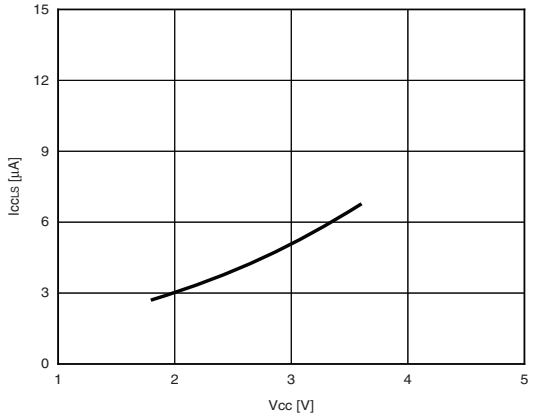
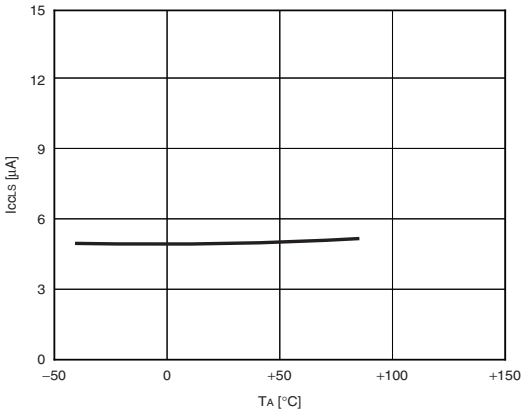
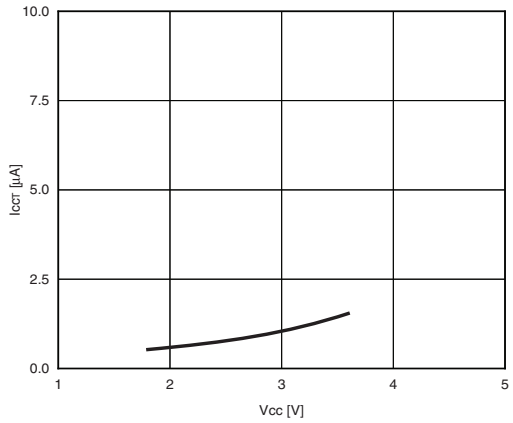
I_{CCLS} – V_{CC}
T_A = +25°C, F_{MPL} = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



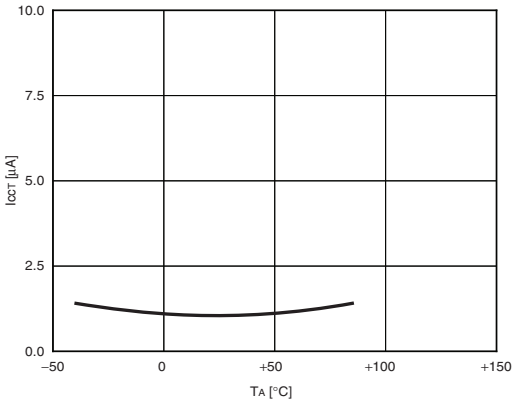
I_{CCLS} – T_A
V_{CC} = 3.0 V, F_{MPL} = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



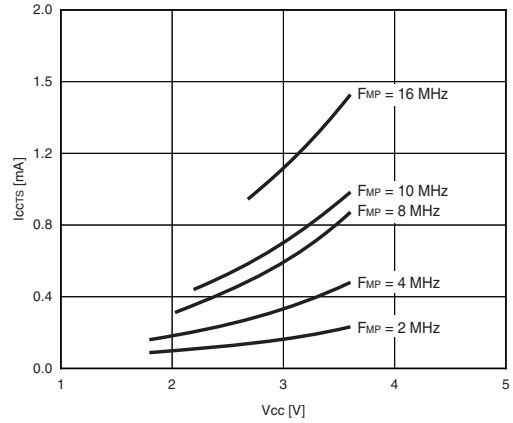
I_{CCT} – V_{CC}
T_A = +25°C, F_{MPL} = 16 kHz (divided by 2)
Watch mode with the external clock operating



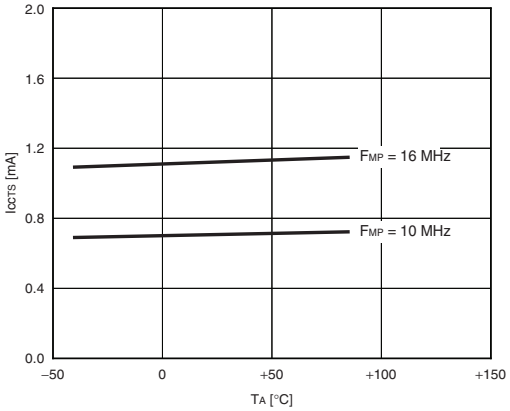
I_{CCT} – T_A
V_{CC} = 3.0 V, F_{MPL} = 16 kHz (divided by 2)
Watch mode with the external clock operating



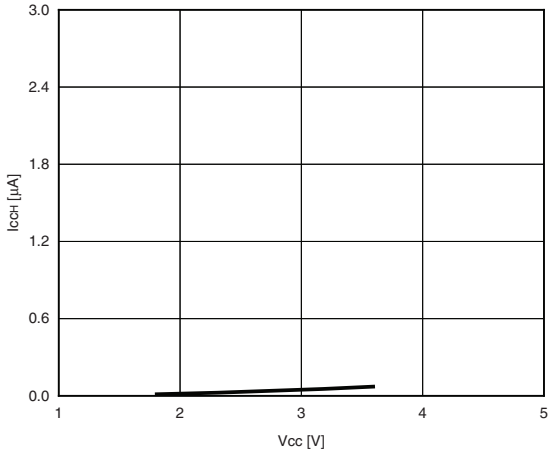
I_{CCTS} – V_{CC}
T_A = +25°C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating



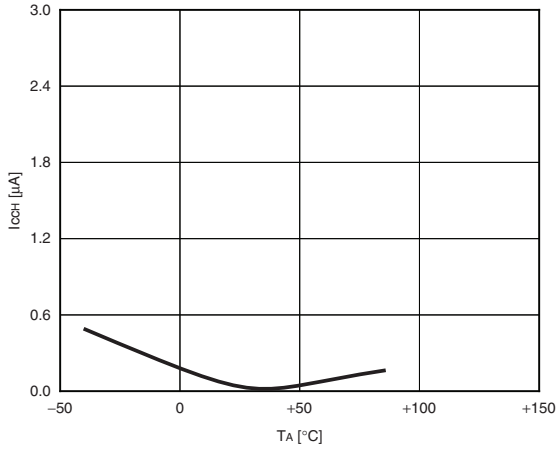
I_{CCTS} – T_A
V_{CC} = 3.0 V, F_{MP} = 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating



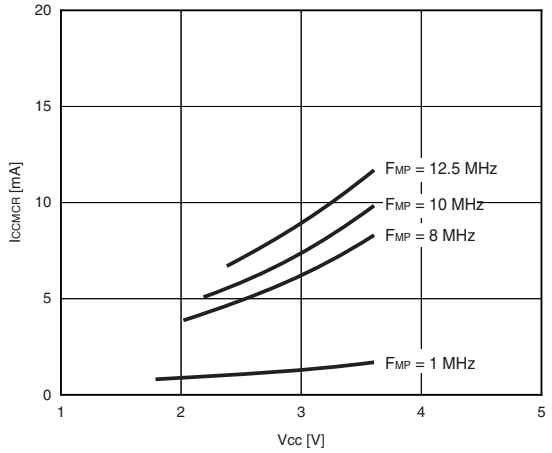
I_{CCH} – V_{CC}
T_A = +25°C, F_{MPL} = (stop)
Substop mode with the external clock stopping



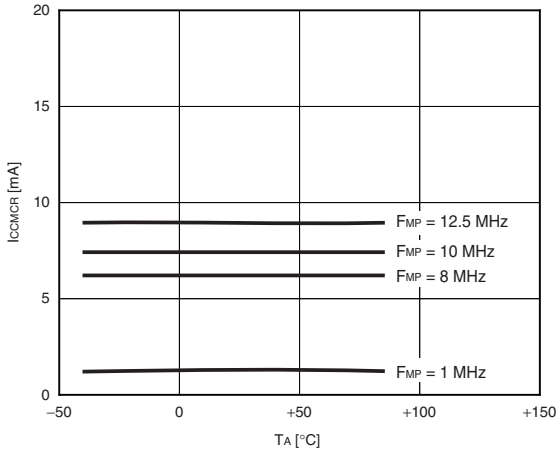
I_{CCH} – T_A
V_{CC} = 3.0 V, F_{MPL} = (stop)
Substop mode with the external clock stopping



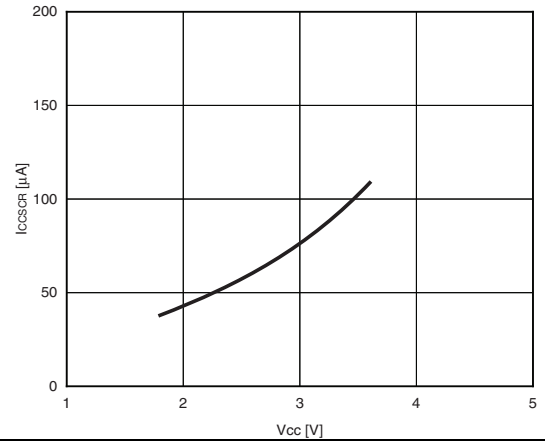
I_{CCMCR} – V_{CC}
T_A = +25°C, F_{MP} = 1, 8, 10, 12.5 MHz (no division)
Main clock mode with the main CR clock operating



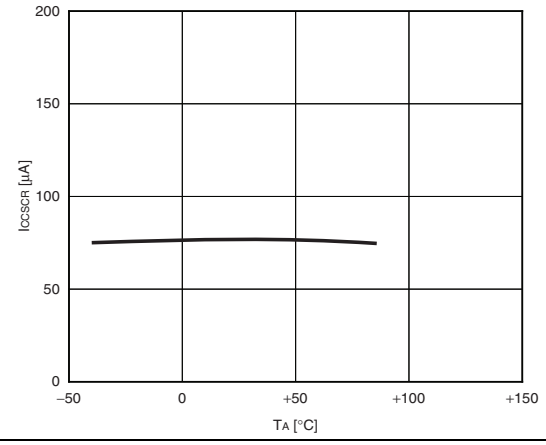
I_{CCMCR} – T_A
V_{CC} = 3.0 V, F_{MP} = 1, 8, 10, 12.5 MHz (no division)
Main clock mode with the main CR clock operating



I_{CCSCR} – V_{CC}
T_A = +25°C, F_{MPL} = 50 kHz (divided by 2)
Subclock mode with the sub-CR clock operating

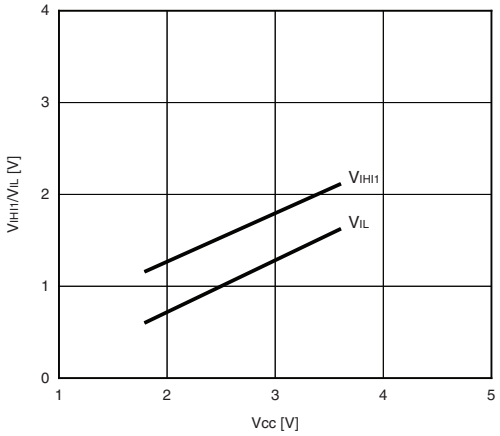


I_{CCSCR} – T_A
V_{CC} = 3.0 V, F_{MPL} = 50 kHz (divided by 2)
Subclock mode with the sub-CR clock operating

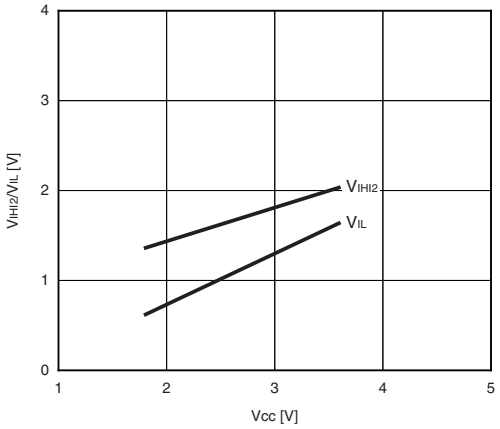


■ Input voltage characteristics

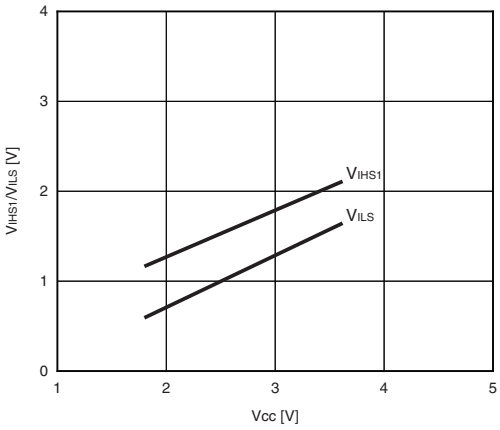
V_{IHI1} – V_{CC} and V_{IL} – V_{CC}
T_A = +25°C



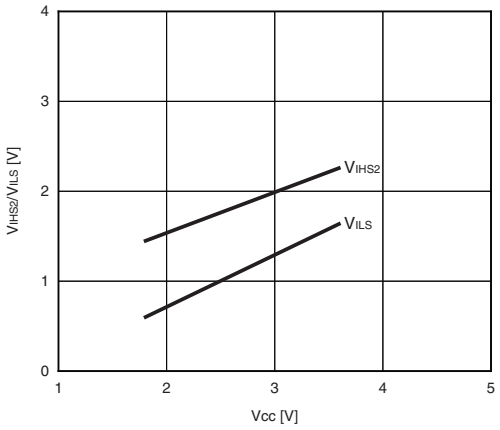
V_{IHI2} – V_{CC} and V_{IL} – V_{CC}
T_A = +25°C



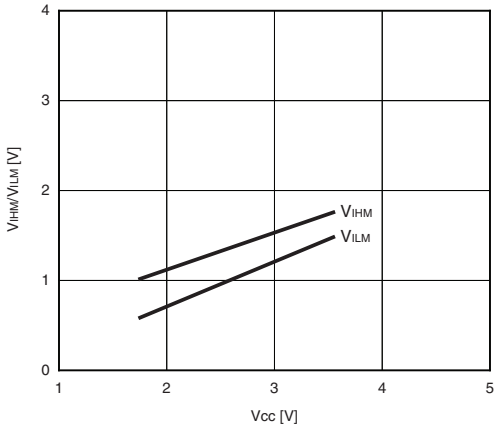
V_{IHS1} – V_{CC} and V_{ILS} – V_{CC}
T_A = +25°C



V_{IHS2} – V_{CC} and V_{ILS} – V_{CC}
T_A = +25°C

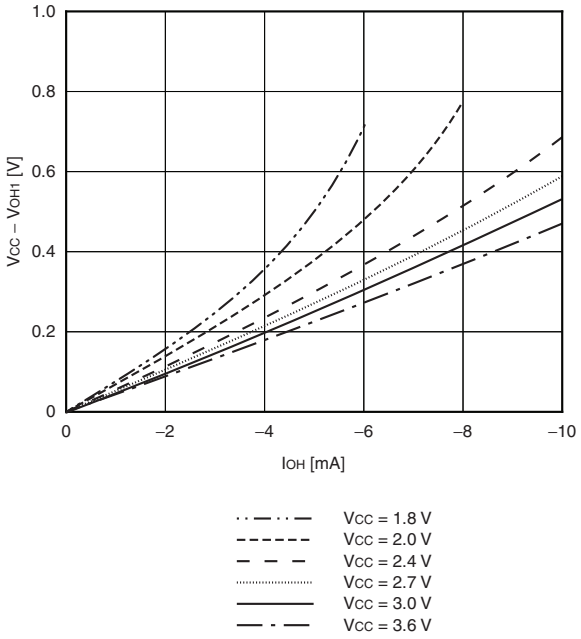


V_{IHM} – V_{CC} and V_{ILM} – V_{CC}
T_A = +25°C

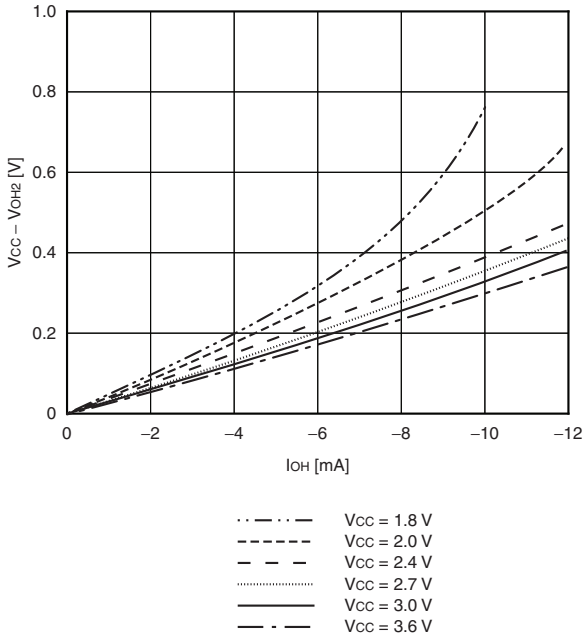


■ Output voltage characteristics

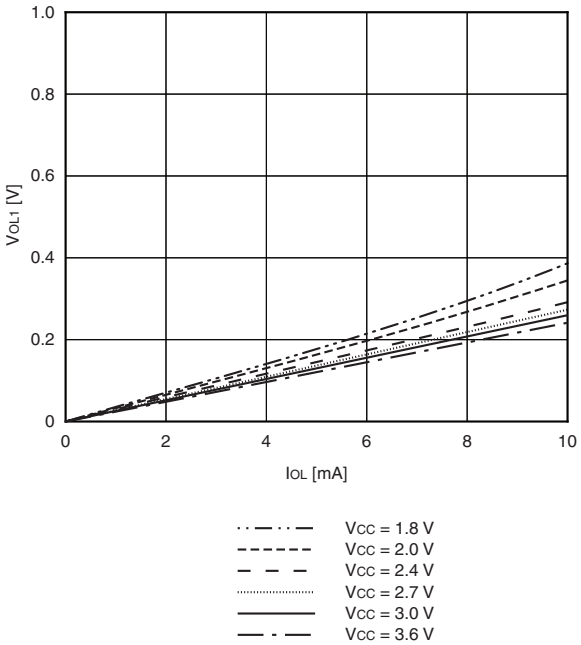
$(V_{CC} - V_{OH1}) - I_{OH}$
$T_A = +25°C$



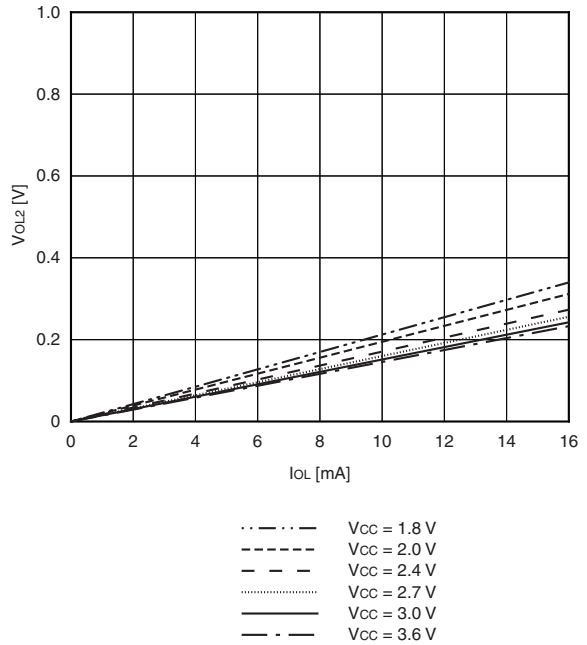
$(V_{CC} - V_{OH2}) - I_{OH}$
$T_A = +25°C$



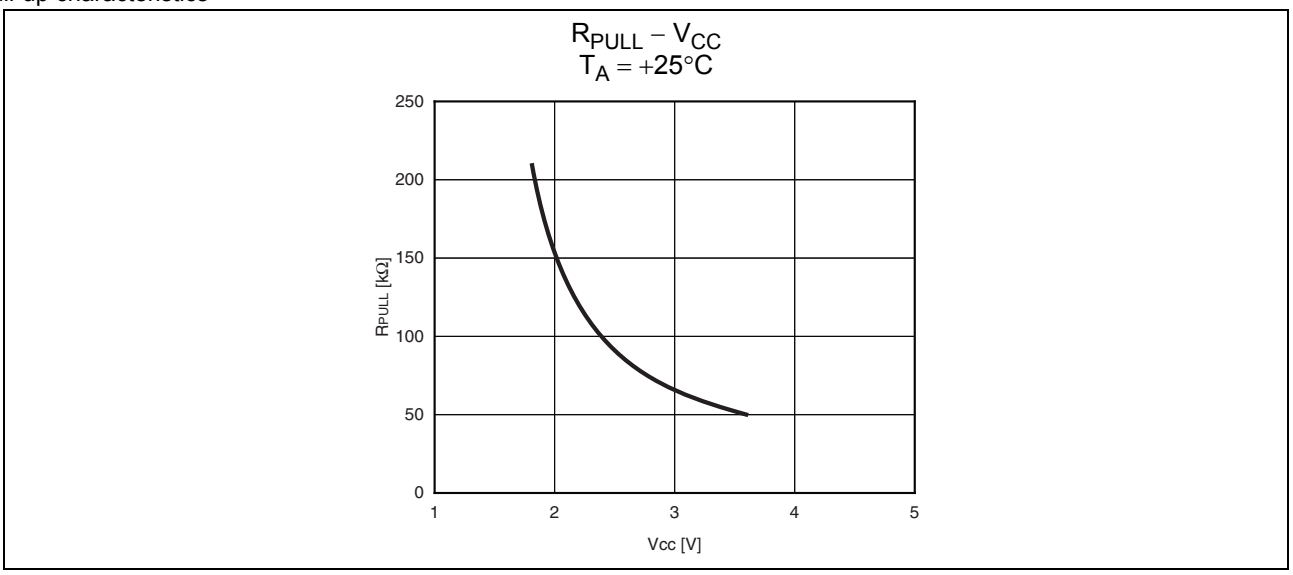
$V_{OL1} - I_{OL}$
$T_A = +25°C$



$V_{OL2} - I_{OL}$
$T_A = +25°C$



■ Pull-up characteristics



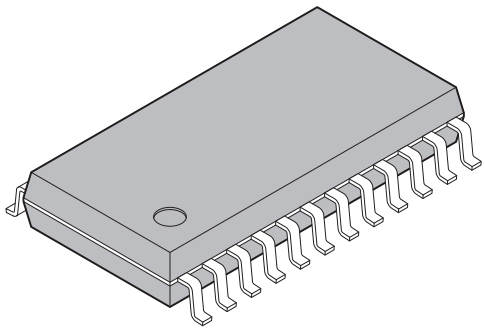
16. Mask Options

No.	Part Number	MB95F352E MB95F353E MB95F354E	MB95F352L MB95F353L MB95F354L
	Selectable/Fixed	Fixed	
1	Low-voltage detection reset	With low-voltage detection reset	Without low-voltage detection reset
2	Reset	Without dedicated reset input	With dedicated reset input

17. Ordering Information

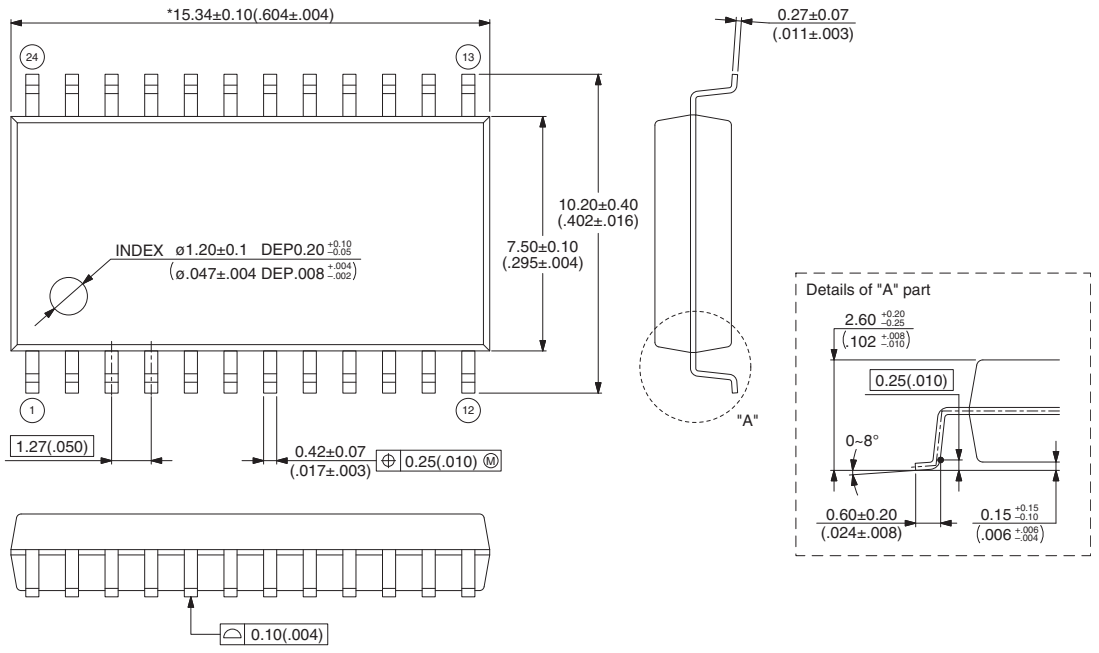
Part Number	Package
MB95F352EPF-G-SNE2 MB95F352LPF-G-SNE2 MB95F353EPF-G-SNE2 MB95F353LPF-G-SNE2 MB95F354EPF-G-SNE2 MB95F354LPF-G-SNE2	24-pin plastic SOP (FPT-24P-M34)
MB95F352EPFT-G-SNE2 MB95F352LPFT-G-SNE2 MB95F353EPFT-G-SNE2 MB95F353LPFT-G-SNE2 MB95F354EPFT-G-SNE2 MB95F354LPFT-G-SNE2	24-pin plastic TSSOP (FPT-24P-M10)
MB95F352EWQN-G-SNE1 MB95F352EWQN-G-SNERE1 MB95F352LWQN-G-SNE1 MB95F352LWQN-G-SNERE1 MB95F353EWQN-G-SNE1 MB95F353EWQN-G-SNERE1 MB95F353LWQN-G-SNE1 MB95F353LWQN-G-SNERE1 MB95F354EWQN-G-SNE1 MB95F354EWQN-G-SNERE1 MB95F354LWQN-G-SNE1 MB95F354LWQN-G-SNERE1	32-pin plastic QFN (LCC-32P-M19)

18. Package Dimension

24-pin plastic SOP		
 (FPT-24P-M34)	Lead pitch	1.27 mm
	Package width × package length	7.50 mm × 15.34 mm
	Lead shape	Gullwing
	Lead bend direction	Normal bend
	Sealing method	Plastic mold
	Mounting height	2.80 mm MAX
	Weight	0.44 g

24-pin plastic SOP
(FPT-24P-M34)

Note 1) * : These dimensions do not include resin protrusion.



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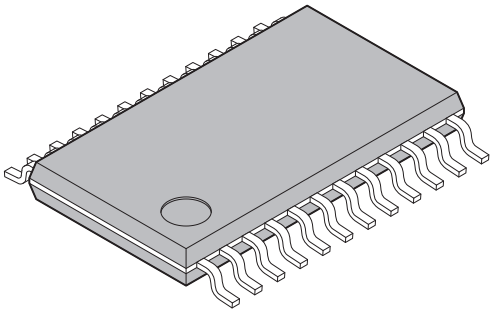
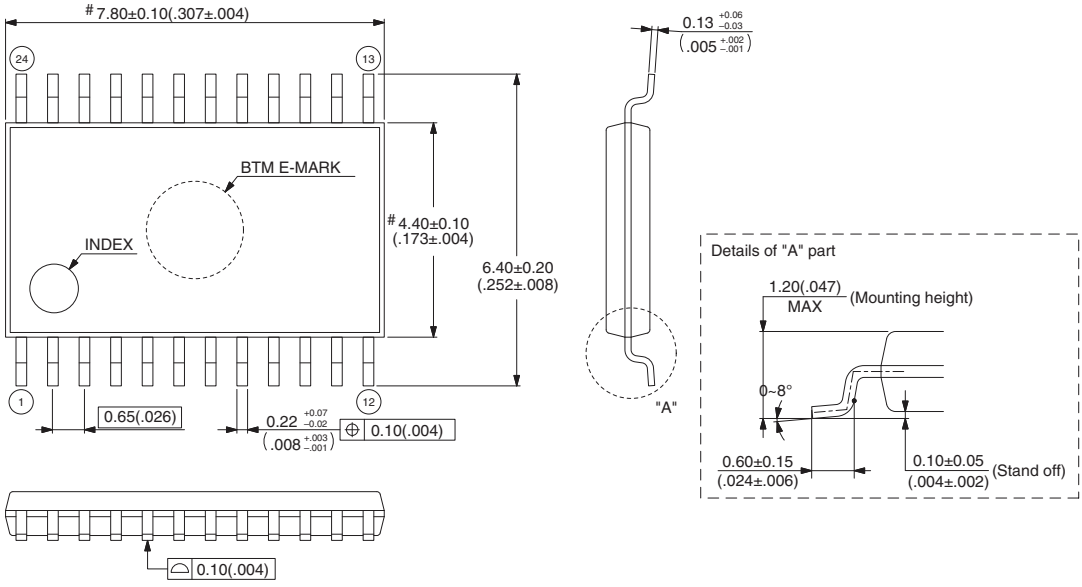
Dimensions in mm (inches).
Note: The values in parentheses are reference values.

(Continued)

24-pin plastic TSSOP		
 (FPT-24P-M10)	Lead pitch	0.65 mm
	Package width × package length	4.40 mm × 7.80 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.20 mm MAX
	Weight	0.10 g

24-pin plastic TSSOP
(FPT-24P-M10)

Note 1) Pins width and pins thickness include plating thickness.
Note 2) Pins width do not include tie bar cutting remainder.
Note 3) #: These dimensions do not include resin protrusion.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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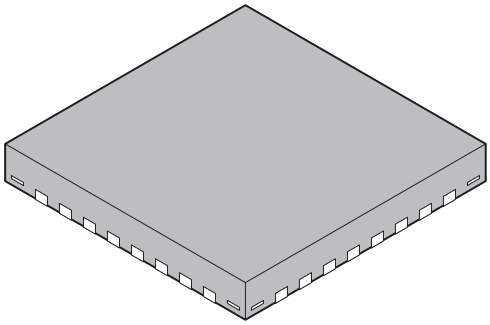
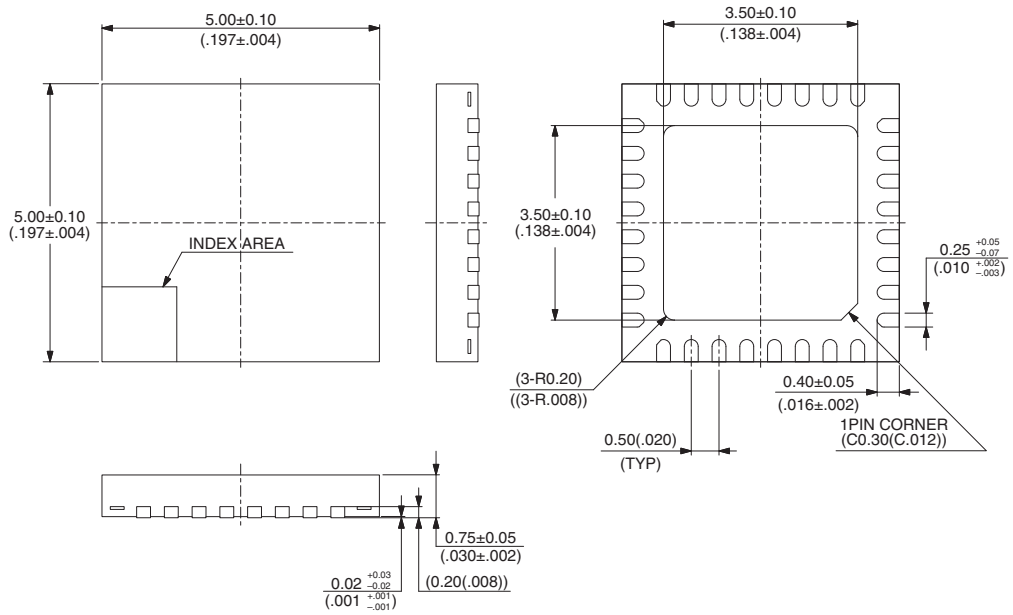
(Continued)

(Continued)

32-pin plastic QFN		
	Lead pitch	0.50 mm
	Package width × package length	5.00 mm × 5.00 mm
	Sealing method	Plastic mold
	Mounting height	0.80 mm MAX
	Weight	0.06 g
(LCC-32P-M19)		

32-pin plastic QFN
(LCC-32P-M19)



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Dimensions in mm (inches).
Note: The values in parentheses are reference values.

19. Major Changes

<table>
<tr><th>Page</th><th>Section</th><th>Details</th></tr>
<tr><td>7</td><td>Pin Assignment</td><td>Deleted the HCLK1 pin and the HCLK2 pin.</td></tr>
<tr><td>9</td><td>Pin Description (24-pin MCU)</td><td>Deleted the HCLK1 pin and the HCLK2 pin.</td></tr>
<tr><td>11</td><td>Pin Description (32-pin MCU)</td><td>Deleted the HCLK1 pin and the HCLK2 pin.</td></tr>
<tr><td>16</td><td>Block Diagram</td><td>Deleted the HCLK1 pin and the HCLK2 pin.</td></tr>
<tr><td>26</td><td>Electrical Characteristics
DC Characteristics</td><td>Changed the value of V_{CC} in the operating conditions.
3.0 V to 3.6 V → 2.7 V to 3.6 V</td></tr>
<tr><td>27</td><td></td><td>Changed the value of V_{CC} in the operating conditions.
3.6 V → 1.8 V to 3.6 V

Changed the typical (Typ) values and the maximum (Max) values of I_{CC}.
<table>
<tr><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Typ</th><th>Max</th></tr>
<tr><td>—</td><td>13.6</td><td>22.4</td><td>mA</td><td>Flash memory product (except writing and erasing)</td></tr>
<tr><td>—</td><td>38.1</td><td>44.9</td><td>mA</td><td>Flash memory product (at writing and erasing)</td></tr>
<tr><td>—</td><td>15.1</td><td>24.6</td><td>mA</td><td>At A/D conversion</td></tr>
</table>
→
<table>
<tr><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr>
<tr><th>Min</th><th>Typ*3</th><th>Max</th></tr>
<tr><td>—</td><td>11.2</td><td>20</td><td>mA</td><td>Flash memory product (except writing and erasing)</td></tr>
<tr><td>—</td><td>26.2</td><td>38</td><td>mA</td><td>Flash memory product (at writing and erasing)</td></tr>
<tr><td>—</td><td>13.3</td><td>23.4</td><td>mA</td><td>At A/D conversion</td></tr>
</table>
Changed the Typ value of I_{CCS}.
6.3 → 5.2

Changed the Typ value and the Max value of I_{CCL}.
Typ : 20 → 15
Max : 45 → 35

Changed the Typ value and the Max value of I_{CCLS}.
Typ : 6.3 → 5
Max : 30 → 15

Changed the Typ value and the Max value of I_{CCT}.
Typ : 2 → 1
Max : 22 → 10</td></tr>
</table>

(Continued)

(Continued)

Page	Section	Details
27	Electrical Characteristics DC Characteristics	Changed the Typ value of I_{CCMCR}. 11 → 9 Changed the Typ value of I_{CCSCR}. 110 → 77 Changed the Typ value of I_{CCTS}. 1.8 → 1.1 Changed the Typ value of I_{CCH}. 1 → 0.1
28		Changed the Typ value of I_{LVD}. 8 → 6.4 Changed the Typ value of I_{CRH}. 0.5 → 0.25 Added the following note: *3: V_{CC} = 3.0 V, T_A = +25°C
29	Electrical Characteristics AC Characteristics Clock Timing	Deleted all information about the HCLK1 pin and the HCLK2 pin in the table.
30		Deleted HCLK1 and HCLK2 in the "• Input waveform generated when an external clock (main clock) is used". Deleted the external connection diagram for the HCLK1 pin and HCLK2 pin in "• Figure of main clock input port external connection".
43	Electrical Characteristics AC Characteristics Low-voltage Detection	Deleted the following parameters: Power hysteresis width 0, Power hysteresis width 1, Power hysteresis width 2, Interrupt hysteresis width 0, Interrupt hysteresis width 1, Interrupt hysteresis width 2, Interrupt hysteresis width 3, Interrupt hysteresis width 4
44		Deleted V_{PHYS}/V_{IHYS} from the diagram.
54 to 59	Sample Characteristics	Added diagrams showing sample characteristics.
61	Ordering Information	Added the following part numbers for the 32-pin plastic QFN package (LCC-32P-M19): MB95F352EWQN-G-SNE1 MB95F352LWQN-G-SNE1 MB95F353EWQN-G-SNE1 MB95F353LWQN-G-SNE1 MB95F354EWQN-G-SNE1 MB95F354LWQN-G-SNE1

Document History

Document Title: MB95F352E/F352L/F353E/F353L/F354E/F354L CMOS F^{2}MC-8FX MB95350L Series 8-bit Microcontrollers Document Number: 002-07527				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	-	AKIH	04/13/2010	Migrated to Cypress and assigned document number 002-07527. No change to document contents or format.
*A	5183750	AKIH	03/31/2016	Updated to Cypress template
*B	5861657	YSAT	08/24/2017	Adapted new Cypress logo

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