CY91F467EA

32-bit FR60 Family CY91460E Series Microcontroller

CY91460E series is a line of general-purpose 32-bit RISC microcontrollers designed for embedded control applications which require high-speed real-time processing, such as consumer devices and on-board vehicle systems. This series uses the FR60 CPU, which is compatible with the FR family* of CPUs.

This series contains the LIN-USART and CAN controllers.

Features

FR60 CPU Core

- 32-bit RISC, load/store architecture, five-stage pipeline
- 16-bit fixed-length instructions (basic instructions)
- Instruction execution speed: 1 instruction per cycle
- Instructions including memory-to-memory transfer, bit manipulation, and barrel shift instructions: Instructions suitable for embedded applications
- Function entry/exit instructions and register data multi-load store instructions: Instructions supporting C language
- Register interlock function: Facilitating assembly-language coding
- Built-in multiplier with instruction-level support
  Signed 32-bit multiplication: 5 cycles
  Signed 16-bit multiplication: 3 cycles
- Interrupts (save PC/PS): 6 cycles (16 priority levels)
- Harvard architecture enabling program access and data access to be performed simultaneously
- Instructions compatible with the FR family

Internal Peripheral Resources

- General-purpose ports: Maximum 170 ports
- DMAC (DMA Controller)
  - Maximum of 5 channels able to operate simultaneously. (External to external: 1 channel)
  - 3 transfer sources (external pin/internal peripheral/software)
  - Activation source can be selected using software.
  - Addressing mode specifies full 32-bit addresses (increment/decrement/fixed)
  - Transfer mode (demand transfer/burst transfer/step transfer/block transfer)
  - Transfer data size selectable from 8-/16-/32-bit
  - Multi-byte transfer enabled (by software)
  - DMAC descriptor in I/O areas (200_H to 240_H, 1000_H to 1024_H)
- A/D converter (successive approximation type)
  - 10-bit resolution: 24 channels
  - Conversion time: minimum 1 µs
- External interrupt inputs: 14 channels
  - 8 channels shared with CAN RX or I2C pins
- Bit search module (for REALOS)
  - Function to search from the MSB (most significant bit) for the position of the first "0", "1", or changed bit in a word
- LIN-USART (full duplex double buffer): 5 channels
  - Clock synchronous/asynchronous selectable
  - Sync-break detection
  - Internal dedicated baud rate generator
- I^2C* bus interface (supports 400 kbps): 3 channels
  - Master/slave transmission and reception
  - Arbitration function, clock synchronization function
- CAN controller (C-CAN): 2 channels
  - Maximum transfer speed: 1 Mbps
  - 32 transmission/reception message buffers
- Stepper motor controller: 6 channels
  - 4 high current output to each channel
  - 2 synchronized PWMs per channel (8-/10-bit)
- Sound generator: 1 channel
  - Tone frequency: PWM frequency divide-by-two (reload value + 1)
- Alarm comparator: 1 channel
  - Monitor external voltage
  - Generate an interrupt in case of voltage lower/higher than the defined thresholds (reference voltage)
- 16-bit PPG timer: 12 channels
- 16-bit PFM timer: 1 channel
- 16-bit reload timer: 8 channels
- 16-bit free-run timer: 8 channels (1 channel each for ICU and OCU)
- Input capture: 8 channels (operates in conjunction with the free-run timer)
- Output compare: 4 channels (operates in conjunction with the free-run timer)
- Up/Down counter: 3 channels (3*8-bit or 1*16-bit + 1*8-bit)
- Watchdog timer
- Real-time clock
- Low-power consumption modes: Sleep/stop mode function

- Supply Supervisor: Low voltage detection circuit for external $V_{DD}5$ and internal 1.8 V core voltage
- Clock supervisor
  Monitors the sub-clock (32 kHz) and the main clock (4 MHz), and switches to a recovery clock (CR oscillator, etc.) when the oscillations stop.
- Clock modulator
- Clock monitor
- Sub-clock calibration

  Corrects the real-time clock timer when operating with the 32 kHz or CR oscillator
- Main oscillator stabilization timer

  Generates an interrupt in sub-clock mode after the stabilization wait time has elapsed on the 23-bit stabilization wait time counter
- Sub-oscillator stabilization timer

  Generates an interrupt in main clock mode after the stabilization wait time has elapsed on the 15-bit stabilization wait time counter

Shutdown Mode

- In low leakage shutdown mode, the internal main power supply is switched off. Only the following resources and meories remain active:
  - Standby RAM (16 KByte)
  - Real Time Clock
  - 4 MHz oscillator, 32 kHz oscillator, RC oscillator
  - Power management logic
  - Hardware Watchdog and Clock Supervisor

Package and Technology

- Package: LQFP-208 (low profile QFP)
- CMOS 0.18 μm technology
- Power supply range 3 V to 5 V (1.9 V/1.8 V internal logic provided by a step-down voltage converter)
- Operating temperature range: between – 40 °C and + 105 °C

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1. Product Lineup

Feature	CY91FV460B	CY91F467DA CY91F467DB	CY91F467EA
Max. core frequency (CLKB)	100 MHz	96 MHz	100 MHz
Max. resource frequency (CLKP)	50 MHz	48 MHz	50 MHz
Max. external bus freq. (CLKT)	50 MHz	48 MHz	50 MHz
Max. CAN frequency (CLKCAN)	50 MHz	48 MHz	50 MHz
Technology	0.18 µm	0.18 µm	0.18 µm
Software-Watchdog	yes	yes	yes
Hardware-Watchdog (RC osc. based)	yes (disengageable), can be activated in SLEEP/STOP	yes	yes, can be activated in SLEEP/STOP
Bit Search	yes	yes	yes
Reset input (INITX)	yes	yes	yes
Clock Modulator	yes	yes	yes
Clock Monitor	yes	yes	yes
Low Power Mode	yes	yes	yes
Shutdown Mode	no, emulation by software	no	yes
DMA	5 ch	5 ch	5 ch
MMU/MPU	MPU (16 ch) [1)]	MPU (8 ch) [1)]	MPU (8 ch) [1)]
Flash memory	2112 KByte or external emulation SRAM	1088 KByte	1088 KByte
Flash Protection	yes	yes	yes
D-RAM	64 KByte	32 KByte	64 KByte
ID-RAM	64 KByte	32 KByte	48 KByte
Standby RAM	no	no	16 KByte
Flash-Cache (F-cache)	16 KByte	8 KByte	8 KByte
Boot-ROM / BI-ROM	16 KByte Boot Flash	4 KByte	4 KByte
RTC	1 ch	1 ch	1 ch
Free Running Timer	8 ch	8 ch	8 ch
ICU	8 ch	8 ch	8 ch
OCU	8 ch	4 ch	4 ch
Reload Timer	8 ch	8 ch	8 ch
PPG 16-bit	16 ch	12 ch	12 ch
PFM 16-bit	1 ch	1 ch	1 ch
Sound Generator	1 ch	1 ch	1 ch
Up/Down Counter (8-/16-bit)	4 ch (8-bit) / 2 ch (16-bit)	3 ch (8-bit) / 1 ch (16-bit)	3 ch (8-bit) / 1 ch (16-bit)
C_CAN	6 ch (128 msg)	3 ch (32 msg)	2 ch (32 msg)

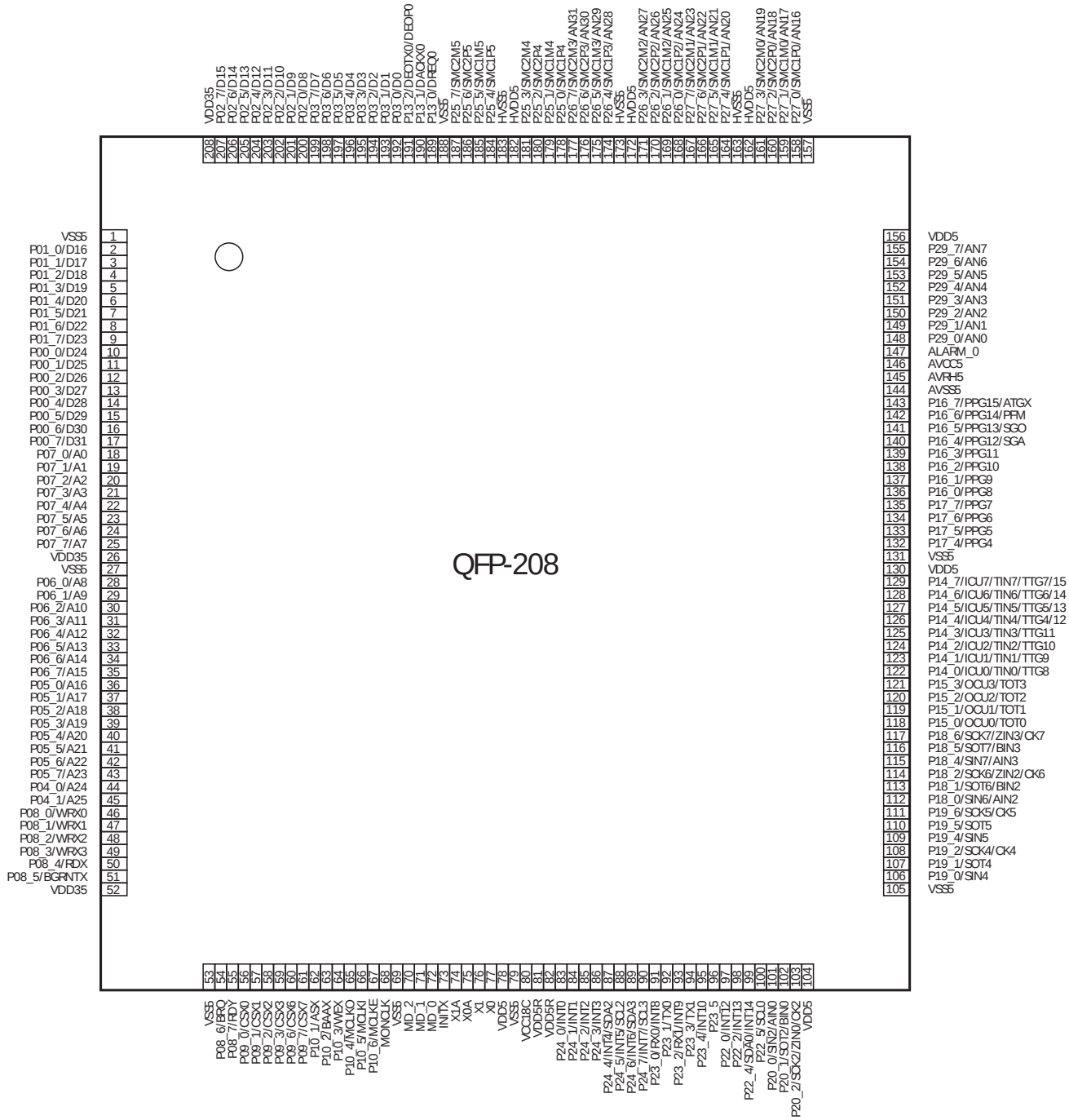
Feature	CY91FV460B	CY91F467DA CY91F467DB	CY91F467EA
LIN-USART	16 ch FIFO	1 ch + 4 ch FIFO	1 ch + 4 ch FIFO
I2C (400k)	8 ch	3 ch	3 ch
FR external bus	yes (32-bit addr, 32-bit data)	yes (26-bit addr, 32-bit data)	yes (26-bit addr, 32-bit data)
External Interrupts	32 ch	14 ch	14 ch
SMC	6 ch	6 ch	6 ch
ADC (10 bit)	32 ch, with Range Comparator	24 ch	24 ch, with Range Comparator
Alarm Comparator	2 ch	1 ch	1 ch
Supply Supervisor (low voltage detection)	yes	yes	yes
Clock Supervisor	yes	yes	yes
Main clock oscillator	4 MHz	4 MHz	4 MHz
Sub clock oscillator	32 kHz	32 kHz	32 kHz
RC Oscillator	100 kHz / 2 MHz	100 kHz / 2 MHz	100 kHz / 2 MHz
PLL	x 25	x 24	x 25
DSU4	yes	-	-
EDSU	yes (32 BP) [1]	yes (16 BP) [1]	yes (16 BP) [1]
Supply Voltage	1.8 V + 3 V / 5 V	3 V / 5 V	3 V / 5 V
Regulator	no	yes	yes
Power Consumption	n.a.	< 2 W	< 1.3 W
Temperatur Range (Ta)	0..70 C	-40..105 C	-40..105 C
Package	BGA896	QFP208	LQFP208
Power on to PLL run	< 20 ms	< 20 ms	< 20 ms
Flash Download Time	< 8 sec typical	< 6 sec typical	< 6 sec typical

1. MPU channels use EDSU breakpoint registers (shared operation between MPU and EDSU).

2. PIN ASSIGNMENT

2.1 CY91F467EA

(TOP VIEW)



LQR208

Note: Difference versus CY91460D series: At pins 95+96, RX2 and TX2 of CAN2 are removed.

3. Pin Description

3.1 CY91F467EA

Pin no.	Pin name	I/O	I/O circuit type [1]	Function
2 to 9	P01_0 to P01_7	I/O	A	General-purpose input/output ports
	D16 to D23			Signal pins of external data bus (bit16 to bit23)
10 to 17	P00_0 to P00_7	I/O	A	General-purpose input/output ports
	D24 to D31			Signal pins of external data bus (bit24 to bit31)
18 to 25	P07_0 to P07_7	I/O	A	General-purpose input/output ports
	A0 to A7			Signal pins of external address bus (bit0 to bit7)
28 to 35	P06_0 to P06_7	I/O	A	General-purpose input/output ports
	A8 to A15			Signal pins of external address bus (bit8 to bit15)
36 to 43	P05_0 to P05_7	I/O	A	General-purpose input/output ports
	A16 to A23			Signal pins of external address bus (bit16 to bit23)
44, 45	P04_0, P04_1	I/O	A	General-purpose input/output ports
	A24, A25			Signal pins of external address bus (bit24, bit25)
46 to 49	P08_0 to P08_3	I/O	A	General-purpose input/output ports
	WRX0 to WRX3			External write strobe output pins
50	P08_4	I/O	A	General-purpose input/output port
	RDX			External read strobe output pin
51	P08_5	I/O	A	General-purpose input/output port
	BGRNTX			External bus release reception output pin
54	P08_6	I/O	A	General-purpose input/output port
	BRQ			External bus release request input pin
55	P08_7	I/O	A	General-purpose input/output port
	RDY			External ready input pin
56 to 59	P09_0 to P09_3	I/O	A	General-purpose input/output ports
	CSX0 to CSX3			Chip select output pins
60, 61	P09_6, P09_7	I/O	A	General-purpose input/output ports
	CSX6, CSX7			Chip select output pins
62	P10_1	I/O	A	General-purpose input/output port
	ASX			Address strobe output pin
63	P10_2	I/O	A	General-purpose input/output port
	BAAX			Burst address advance output pin
64	P10_3	I/O	A	General-purpose input/output port
	WEX			Write enable output pin
65	P10_4	I/O	A	General-purpose input/output port
	MCLKO			Clock output pin for memory
66	P10_5	I/O	A	General-purpose input/output port
	MCLKI			Clock input pin for memory

Pin no.	Pin name	I/O	I/O circuit type [1]	Function
67	P10_6	I/O	A	General-purpose input/output port
	MCLKE			Clock enable signal pin for memory
68	MONCLK	O	M	Clock monitor pin
70	MD_2	I	G	Mode setting pins
71	MD_1	I	G	
72	MD_0	I	G	
73	INITX	I	H	External reset input pin
74	X1A	—	J2	Sub clock (oscillation) output
75	X0A	—	J2	Sub clock (oscillation) input
76	X1	—	J1	Clock (oscillation) output
77	X0	—	J1	Clock (oscillation) input
83 to 86	P24_0 to P24_3	I/O	A	General-purpose input/output ports
	INT0 to INT3			External interrupt input pins
87	P24_4	I/O	C	General-purpose input/output port
	INT4			External interrupt input pin
	SDA2			I^2C bus DATA input/output pin
88	P24_5	I/O	C	General-purpose input/output port
	INT5			External interrupt input pin
	SCL2			I^2C bus clock input/output pin
89	P24_6	I/O	C	General-purpose input/output port
	INT6			External interrupt input pin
	SDA3			I^2C bus DATA input/output pin
90	P24_7	I/O	C	General-purpose input/output port
	INT7			External interrupt input pin
	SCL3			I^2C bus clock input/output pin
91	P23_0	I/O	A	General-purpose input/output port
	RX0			RX input pin of CAN0
	INT8			External interrupt input pin
92	P23_1	I/O	A	General-purpose input/output port
	TX0			TX output pin of CAN0
93	P23_2	I/O	A	General-purpose input/output port
	RX1			RX input pin of CAN1
	INT9			External interrupt input pin
94	P23_3	I/O	A	General-purpose input/output port
	TX1			TX output pin of CAN1
95 [2]	P23_4	I/O	A	General-purpose input/output port
	INT10			External interrupt input pin
96 [2]	P23_5	I/O	A	General-purpose input/output port
97	P22_0	I/O	A	General-purpose input/output port
	INT12			External interrupt input pin

Pin no.	Pin name	I/O	I/O circuit type [1]	Function
98	P22_2	I/O	A	General-purpose input/output port
	INT13			External interrupt input pin
99	P22_4	I/O	C	General-purpose input/output port
	SDA0			I^2C bus data input/output pin
	INT14			External interrupt input pin
100	P22_5	I/O	C	General-purpose input/output port
	SCL0			I^2C bus clock input/output pin
101	P20_0	I/O	A	General-purpose input/output port
	SIN2			Data input pin of USART2
	AIN0			Up/down counter input pin
102	P20_1	I/O	A	General-purpose input/output port
	SOT2			Data output pin of USART2
	BIN0			Up/down counter input pin
103	P20_2	I/O	A	General-purpose input/output port
	SCK2			Clock input/output pin of USART2
	ZIN0			Up/down counter input pin
	CK2			External clock input pin of free-run timer 2
106	P19_0	I/O	A	General-purpose input/output port
	SIN4			Data input pin of USART4
107	P19_1	I/O	A	General-purpose input/output port
	SOT4			Data output pin of USART4
108	P19_2	I/O	A	General-purpose input/output port
	SCK4			Clock input/output pin of USART4
	CK4			External clock input pin of free-run timer 4
109	P19_4	I/O	A	General-purpose input/output port
	SIN5			Data input pin of USART5
110	P19_5	I/O	A	General-purpose input/output port
	SOT5			Data output pin of USART5
111	P19_6	I/O	A	General-purpose input/output port
	SCK5			Clock input/output pin of USART5
	CK5			External clock input pin of free-run timer 5
112	P18_0	I/O	A	General-purpose input/output port
	SIN6			Data input pin of USART6
	AIN2			Up/down counter input pin
113	P18_1	I/O	A	General-purpose input/output port
	SOT6			Data output pin of USART6
	BIN2			Up/down counter input pin

Pin no.	Pin name	I/O	I/O circuit type [1]	Function
114	P18_2	I/O	A	General-purpose input/output port
	SCK6			Clock input/output pin of USART6
	ZIN2			Up/down counter input pin
	CK6			External clock input pin of free-run timer 6
115	P18_4	I/O	A	General-purpose input/output port
	SIN7			Data input pin of USART7
	AIN3			Up/down counter input pin
116	P18_5	I/O	A	General-purpose input/output port
	SOT7			Data output pin of USART7
	BIN3			Up/down counter input pin
117	P18_6	I/O	A	General-purpose input/output port
	SCK7			Clock input/output pin of USART7
	ZIN3			Up/down counter input pin
	CK7			External clock input pin of free-run timer 7
118 to 121	P15_0 to P15_3	I/O	A	General-purpose input/output ports
	OCU0 to OCU3			Output compare output pins
	TOT0 to TOT3			Reload timer output pins
122 to 129	P14_0 to P14_7	I/O	A	General-purpose input/output ports
	ICU0 to ICU7			Input capture input pins
	TIN0 to TIN7			External trigger input pins of reload timer
	TTG8 to TTG11, TTG4/12 to TTG7/15			External trigger input pins of PPG timer
132 to 135	P17_4 to P17_7	I/O	A	General-purpose input/output ports
	PPG4 to PPG7			Output pins of PPG timer
136 to 139	P16_0 to P16_3	I/O	A	General-purpose input/output ports
	PPG8 to PPG11			PPG timer output pins
140	P16_4	I/O	A	General-purpose input/output port
	PPG12			Output pin of PPG timer
	SGA			SGA output pin of sound generator
141	P16_5	I/O	A	General-purpose input/output port
	PPG13			Output pin of PPG timer
	SGO			SGO output pin of sound generator
142	P16_6	I/O	A	General-purpose input/output port
	PPG14			Output pin of PPG timer
	PFM			Pulse frequency modulator output pin
143	P16_7	I/O	A	General-purpose input/output port
	PPG15			PPG timer output pin
	ATGX			A/D converter external trigger input pin
147	ALARM_0	I	N	Alarm comparator input pin

Pin no.	Pin name	I/O	I/O circuit type [1]	Function
148 to 155	P29_0 to P29_7	I/O	B	General-purpose input/output ports
	AN0 to AN7			Analog input pins of A/D converter
158	P27_0	I/O	F	General-purpose input/output port
	SMC1P0			Controller output pin of Stepper motor
	AN16			Analog input pin of A/D converter
159	P27_1	I/O	F	General-purpose input/output port
	SMC1M0			Controller output pin of Stepper motor
	AN17			Analog input pin of A/D converter
160	P27_2	I/O	F	General-purpose input/output port
	SMC2P0			Controller output pin of Stepper motor
	AN18			Analog input pin of A/D converter
161	P27_3	I/O	F	General-purpose input/output port
	SMC2M0			Controller output pin of Stepper motor
	AN19			Analog input pin of A/D converter
164	P27_4	I/O	F	General-purpose input/output port
	SMC1P1			Controller output pin of Stepper motor
	AN20			Analog input pin of A/D converter
165	P27_5	I/O	F	General-purpose input/output port
	SMC1M1			Controller output pin of Stepper motor
	AN21			Analog input pin of A/D converter
166	P27_6	I/O	F	General-purpose input/output port
	SMC2P1			Controller output pin of Stepper motor
	AN22			Analog input pin of A/D converter
167	P27_7	I/O	F	General-purpose input/output port
	SMC2M1			Controller output pin of Stepper motor
	AN23			Analog input pin of A/D converter
168	P26_0	I/O	F	General-purpose input/output port
	SMC1P2			Controller output pin of Stepper motor
	AN24			Analog input pin of A/D converter
169	P26_1	I/O	F	General-purpose input/output port
	SMC1M2			Controller output pin of Stepper motor
	AN25			Analog input pin of A/D converter
170	P26_2	I/O	F	General-purpose input/output port
	SMC2P2			Controller output pin of Stepper motor
	AN26			Analog input pin of A/D converter
171	P26_3	I/O	F	General-purpose input/output port
	SMC2M2			Controller output pin of Stepper motor
	AN27			Analog input pin of A/D converter

Pin no.	Pin name	I/O	I/O circuit type [1]	Function
174	P26_4	I/O	F	General-purpose input/output port
	SMC1P3			Controller output pin of Stepper motor
	AN28			Analog input pin of A/D converter
175	P26_5	I/O	F	General-purpose input/output port
	SMC1M3			Controller output pin of Stepper motor
	AN29			Analog input pin of A/D converter
176	P26_6	I/O	F	General-purpose input/output port
	SMC2P3			Controller output pin of Stepper motor
	AN30			Analog input pin of A/D converter
177	P26_7	I/O	F	General-purpose input/output port
	SMC2M3			Controller output pin of Stepper motor
	AN31			Analog input pin of A/D converter
178	P25_0	I/O	E	General-purpose input/output port
	SMC1P4			Controller output pin of Stepper motor
179	P25_1	I/O	E	General-purpose input/output port
	SMC1M4			Controller output pin of Stepper motor
180	P25_2	I/O	E	General-purpose input/output port
	SMC2P4			Controller output pin of Stepper motor
181	P25_3	I/O	E	General-purpose input/output port
	SMC2M4			Controller output pin of Stepper motor
184	P25_4	I/O	E	General-purpose input/output port
	SMC1P5			Controller output pin of Stepper motor
185	P25_5	I/O	E	General-purpose input/output port
	SMC1M5			Controller output pin of Stepper motor
186	P25_6	I/O	E	General-purpose input/output port
	SMC2P5			Controller output pin of Stepper motor
187	P25_7	I/O	E	General-purpose input/output port
	SMC2M5			Controller output pin of Stepper motor
189	P13_0	I/O	A	General-purpose input/output port
	DREQ0			DMA external transfer request input
190	P13_1	I/O	A	General-purpose input/output port
	DACKX0			DMA external transfer acknowledge output pin
191	P13_2	I/O	A	General-purpose input/output port
	DEOTX0			DMA external transfer EOT (End of Track) output pin
	DEOP0			DMA external transfer EOP (End of Process) output pin
192 to 199	P03_0 to P03_7	I/O	A	General-purpose input/output ports
	D0 to D7			Signal pins of external data bus (bit0 to bit7)
200 to 207	P02_0 to P02_7	I/O	A	General-purpose input/output ports
	D8 to D15			Signal pins of external data bus (bit8 to bit15)

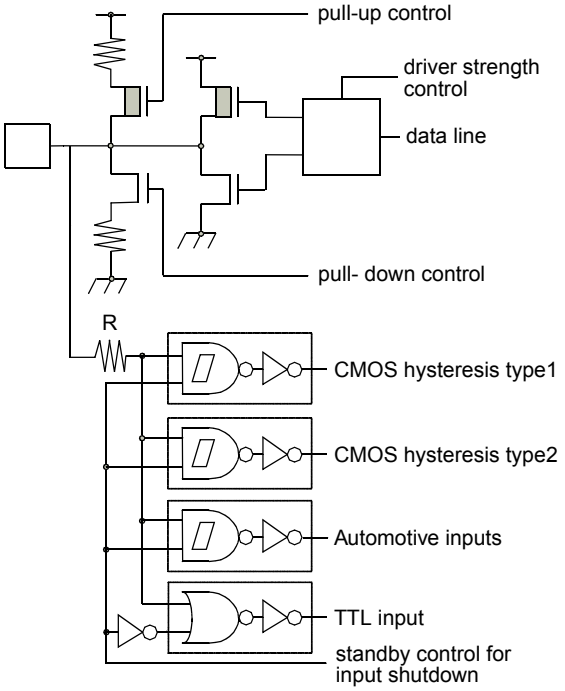
1. For information about the I/O circuit type, refer to I/O Circuit Types.

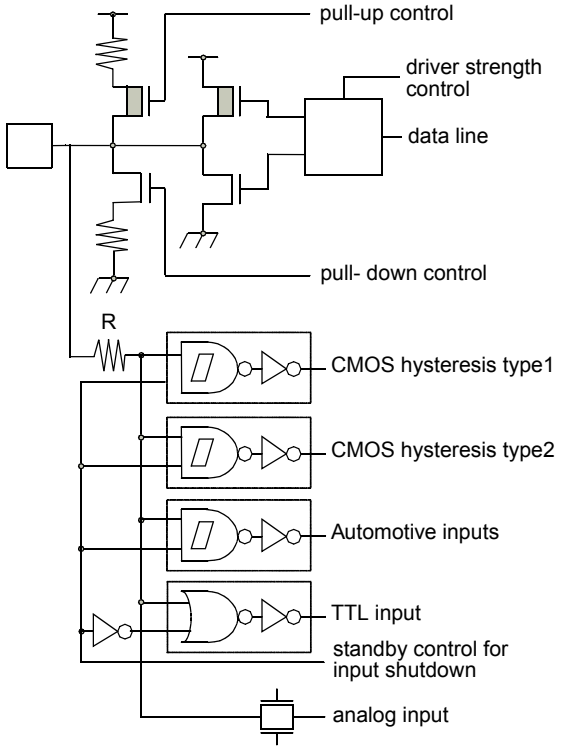
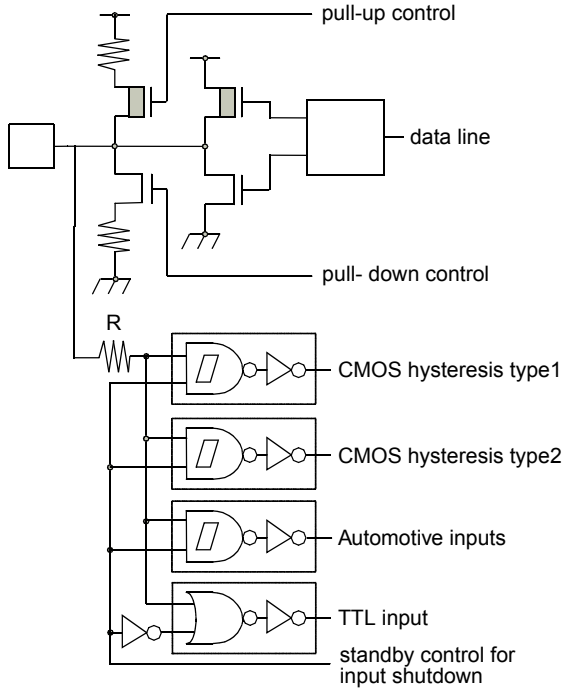
2. Difference versus CY91460D series: At pins 95+96, RX2 and TX2 of CAN2 are removed.

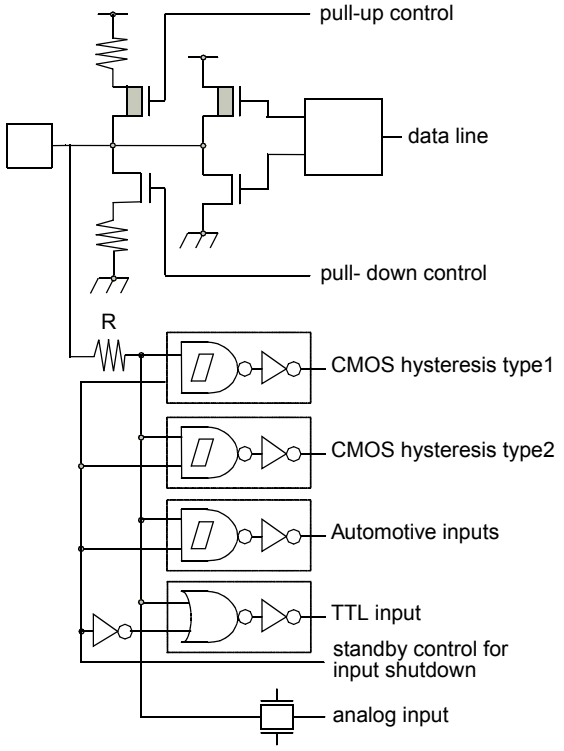
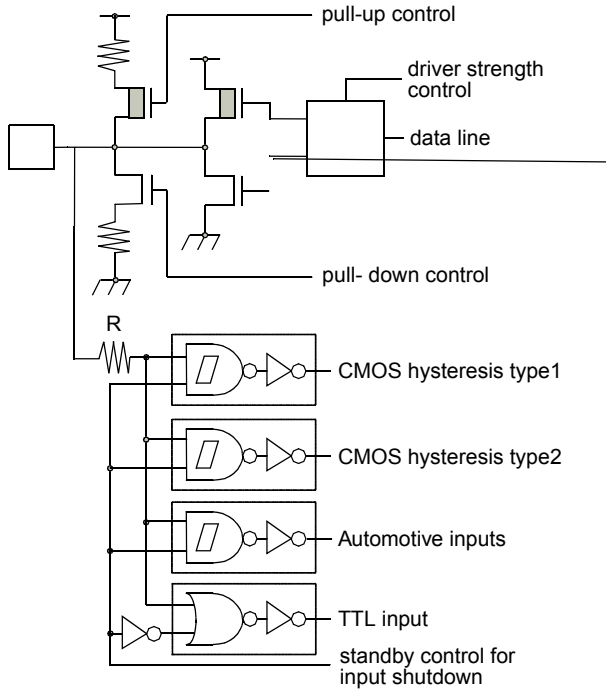
3.2 Power Supply/Ground Pins

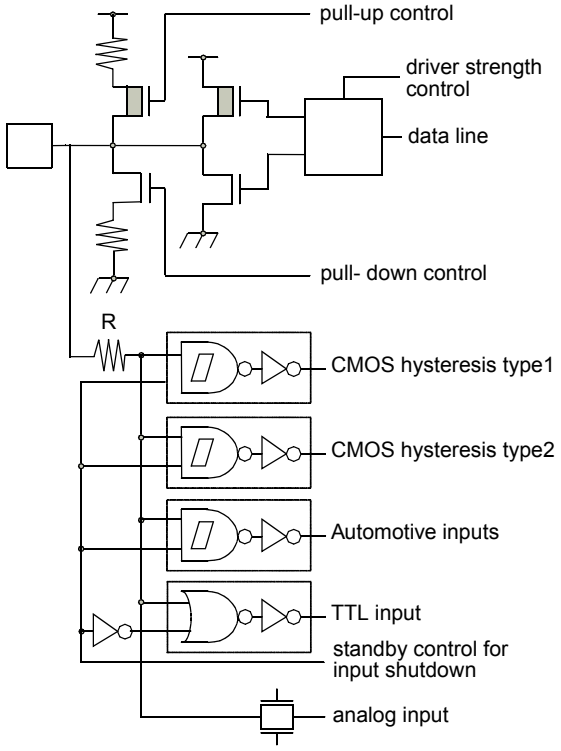
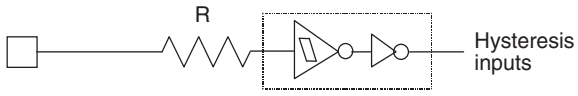
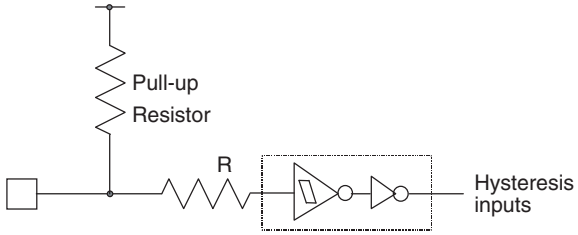
Pin no.	Pin name	I/O	Function
1, 27, 53, 69, 79, 105, 131, 157, 188	VSS5	Supply	Ground pins
163, 173, 183	HVSS5		Ground pins for Stepper motor controller
26, 52, 208	VDD35		Power supply pins for external data bus
78, 104, 130, 156	VDD5		Power supply pins
162, 172, 182	HVDD5		Power supply pins for Stepper motor controller
81, 82	VDD5R		Power supply pins for internal regulator
144	AVSS5		Analog ground pin for A/D converter
146	AVCC5		Power supply pin for A/D converter
145	AVRH5		Reference power supply pin for A/D converter
80	VCC18C		Capacitor connection pin for internal regulator

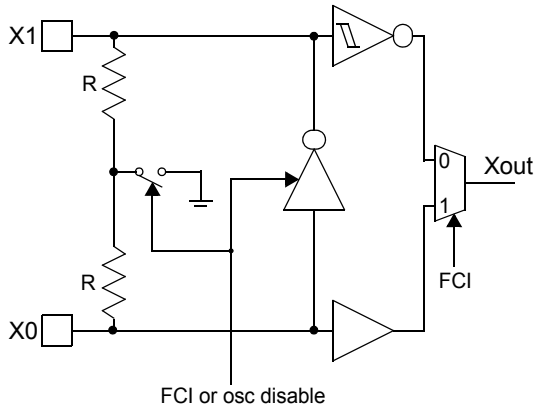
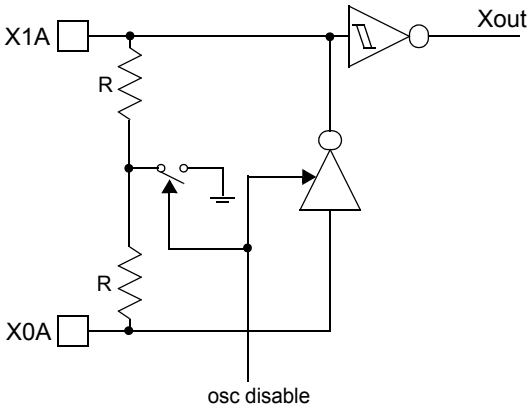
4. I/O Circuit Types

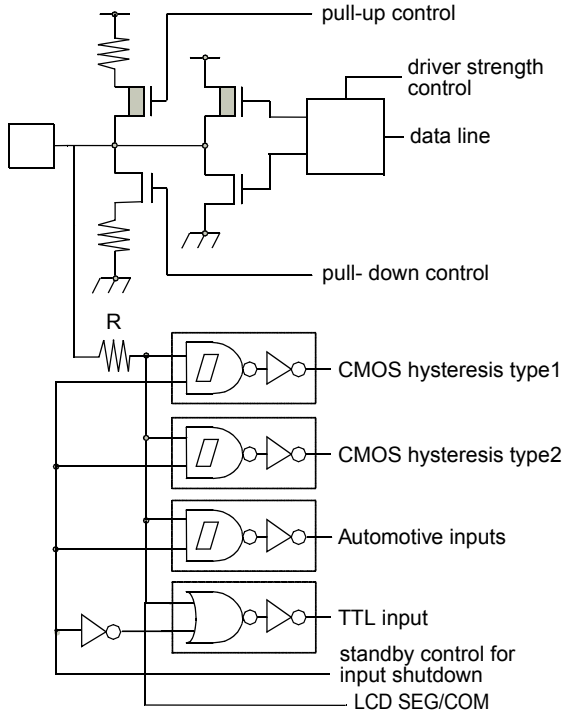
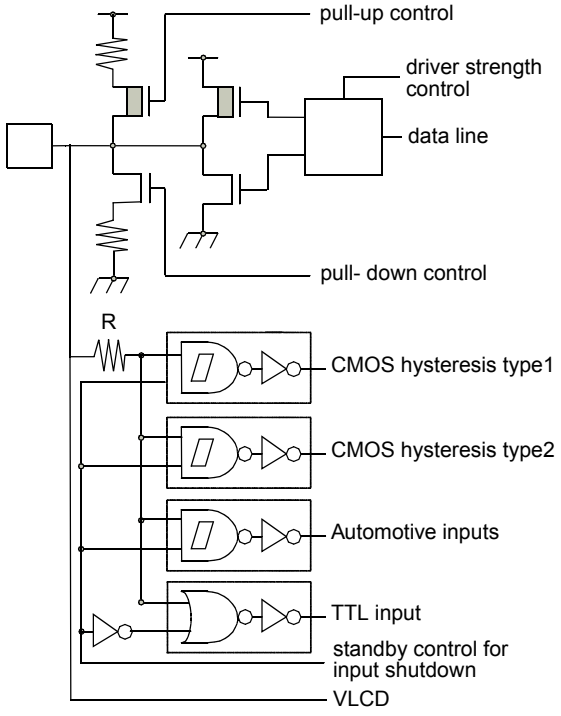
Type	Circuit	Remarks
A		CMOS level output (programmable I_{OL} = 5 mA, I_{OH} = -5 mA and I_{OL} = 2 mA, I_{OH} = -2 mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50 kΩ approx.

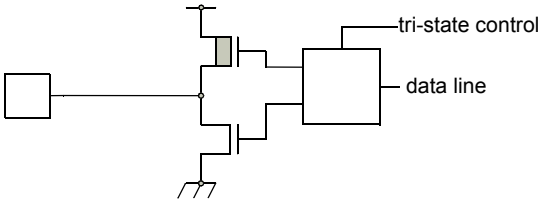
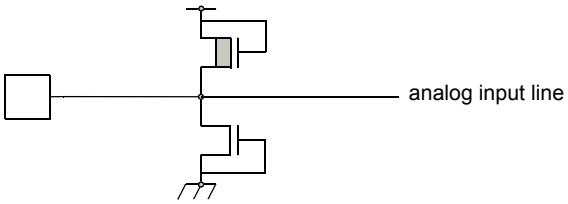
Type	Circuit	Remarks
B		CMOS level output (programmable I_{OL} = 5 mA, I_{OH} = -5 mA and I_{OL} = 2 mA, I_{OH} = -2 mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50 kΩ approx. Analog input
C		CMOS level output (I_{OL} = 3 mA, I_{OH} = -3 mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50 kΩ approx.

Type	Circuit	Remarks
D		CMOS level output (I_{OL} = 3 mA, I_{OH} = -3 mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50 kΩ approx. Analog input
E		CMOS level output (programmable I_{OL} = 5 mA, I_{OH} = -5 mA and I_{OL} = 2 mA, I_{OH} = -2 mA, and I_{OL} = 30 mA, I_{OH} = -30 mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50 kΩ approx.

Type	Circuit	Remarks
F		CMOS level output (programmable I_{OL} = 5 mA, I_{OH} = -5 mA and I_{OL} = 2 mA, I_{OH} = -2 mA, and I_{OL} = 30 mA, I_{OH} = -30 mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50 kΩ approx. Analog input
G		Mask ROM and EVA device: CMOS Hysteresis input pin Flash device: CMOS input pin 12 V withstand (for MD [2:0])
H		CMOS Hysteresis input pin Pull-up resistor value: 50 kΩ approx.

Type	Circuit	Remarks
J1		High-speed oscillation circuit: ■ Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) ■ Feedback resistor = approx. 2 * 0.5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode.
J2		Low-speed oscillation circuit: ■ Feedback resistor = approx. 2 * 5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled.

Type	Circuit	Remarks
K		CMOS level output (programmable I_{OL} = 5 mA, I_{OH} = -5 mA and I_{OL} = 2 mA, I_{OH} = -2 mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50 kΩ approx. LCD SEG/COM output
L		CMOS level output (programmable I_{OL} = 5 mA, I_{OH} = -5 mA and I_{OL} = 2 mA, I_{OH} = -2 mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50 kΩ approx. Analog input LCD Voltage input

Type	Circuit	Remarks
M		CMOS level tri-state output (I_{OL} = 5 mA, I_{OH} = -5 mA)
N		Analog input pin with protection

5. Handling Devices

5.1 Preventing Latch-up

Latch-up may occur in a CMOS IC if a voltage higher than ($V_{DD}5$, $V_{DD}35$ or $HV_{DD}5$) or less than ($V_{SS}5$ or $HV_{SS}5$) is applied to an input or output pin or if a voltage exceeding the rating is applied between the power supply pins and ground pins. If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Therefore, be very careful not to apply voltages in excess of the absolute maximum ratings.

5.2 Handling of Unused Input Pins

If unused input pins are left open, abnormal operation may result. Any unused input pins should be connected to pull-up or pull-down resistor (2 kΩ to 10 kΩ) or enable internal pullup or pulldown resisters (PPER/PPCR) before the input enable (PORTEN) is activated by software. The mode pins MD_x can be connected to $V_{SS}5$ or $V_{DD}5$ directly. Unused ALARM input pins can be connected to $AV_{SS}5$ directly.

5.3 Power Supply Pins

In CY91460 series, devices including multiple power supply pins and ground pins are designed as follows; pins necessary to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. All of the power supply pins and ground pins must be externally connected to the power supply and ground respectively in order to reduce unnecessary radiation, to prevent strobe signal malfunctions due to the ground level rising and to follow the total output current ratings. Furthermore, the power supply pins and ground pins of the CY91460 series must be connected to the current supply source via a low impedance.
It is also recommended to connect a ceramic capacitor of approximately 0.1 µF as a bypass capacitor between power supply pin and ground pin near this device.
This series has a built-in step-down regulator. Connect a bypass capacitor of 4.7 µF (use a X7R ceramic capacitator) to VCC18C pin for the regulator.

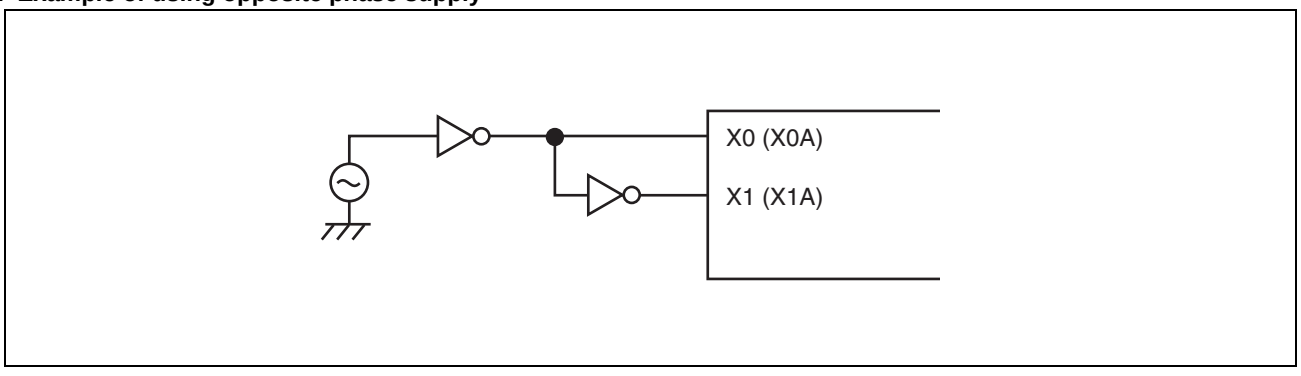
5.4 Crystal Oscillator Circuit

Noise in proximity to the X0 (X0A) and X1 (X1A) pins can cause the device to operate abnormally. Printed circuit boards should be designed so that the X0 (X0A) and X1 (X1A) pins, and crystal oscillator, as well as bypass capacitors connected to ground, are located near the device and ground.
It is recommended that the printed circuit board layout be designed such that the X0 and X1 pins or X0A and X1A pins are surrounded by ground plane for the stable operation.
Please request the oscillator manufacturer to evaluate the oscillational characteristics of the crystal and this device.

5.5 Notes on Using External Clock

When using the external clock, it is necessary to simultaneously supply the X0 (X0A) and the X1 (X1A) pins. In the described combination, X1 (X1A) should be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins. At X0 and X1, a frequency up to 16 MHz is possible.

Figure 1. Example of using opposite phase supply



5.6 Mode Pins (MD_x)

These pins should be connected directly to the power supply or ground pins. To prevent the device from entering test mode accidentally due to noise, minimize the lengths of the patterns between each mode pin and power supply pin or ground pin on the printed circuit board as possible and connect them with low impedance.

5.7 Notes on Operating in PLL Clock Mode

If the oscillator is disconnected or the clock input stops when the PLL clock is selected, the microcontroller may continue to operate at the free-running frequency of the self-oscillating circuit of the PLL. However, this self-running operation cannot be guaranteed.

5.8 Pull-up Control

The AC standard is not guaranteed in case a pull-up resistor is connected to the pin serving as an external bus pin.

5.9 Notes on PS Register

As the PS register is processed in advance by some instructions, when the debugger is being used, the exception handling may result in execution breaking in an interrupt handling routine or the displayed values of the flags in the PS register being updated.
As the microcontroller is designed to carry out reprocessing correctly upon returning from such an EIT event,
the operation before and after the EIT always proceeds according to specification.

The following behavior may occur if any of the following occurs in the instruction immediately after a DIV0U/DIV0S instruction:

(a) a user interrupt or NMI is accepted;
(b) single-step execution is performed;
(c) execution breaks due to a data event or from the emulator menu.

1. D0 and D1 flags are updated in advance.
2. An EIT handling routine (user interrupt/NMI or emulator) is executed.
3. Upon returning from the EIT, the DIV0U/DIV0S instruction is executed and the D0 and D1 flags are updated to the same values as those in 1.

The following behavior occurs when an ORCCR, STILM, MOV Ri,PS instruction is executed to enable a user interrupt or NMI source while that interrupt is in the active state.

1. The PS register is updated in advance.
2. An EIT handling routine (user interrupt/NMI or emulator) is executed.
3. Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as in 1.

6. Notes on Debugger

6.1 Execution of the RETI Command

If single-step execution is used in an environment where an interrupt occurs frequently, the corresponding interrupt handling routine will be executed repeatedly to the exclusion of other processing. This will prevent the main routine and the handlers for low priority level interrupts from being executed (For example, if the time-base timer interrupt is enabled, stepping over the RETI instruction will always break on the first line of the time-base timer interrupt handler).

Disable the corresponding interrupts when the corresponding interrupt handling routine no longer needs debugging.

6.2 Break Function

If the range of addresses that cause a hardware break (including event breaks) is set to the address of the current system stack pointer or to an area that contains the stack pointer, execution will break after each instruction regardless of whether the user program actually contains data access instructions.

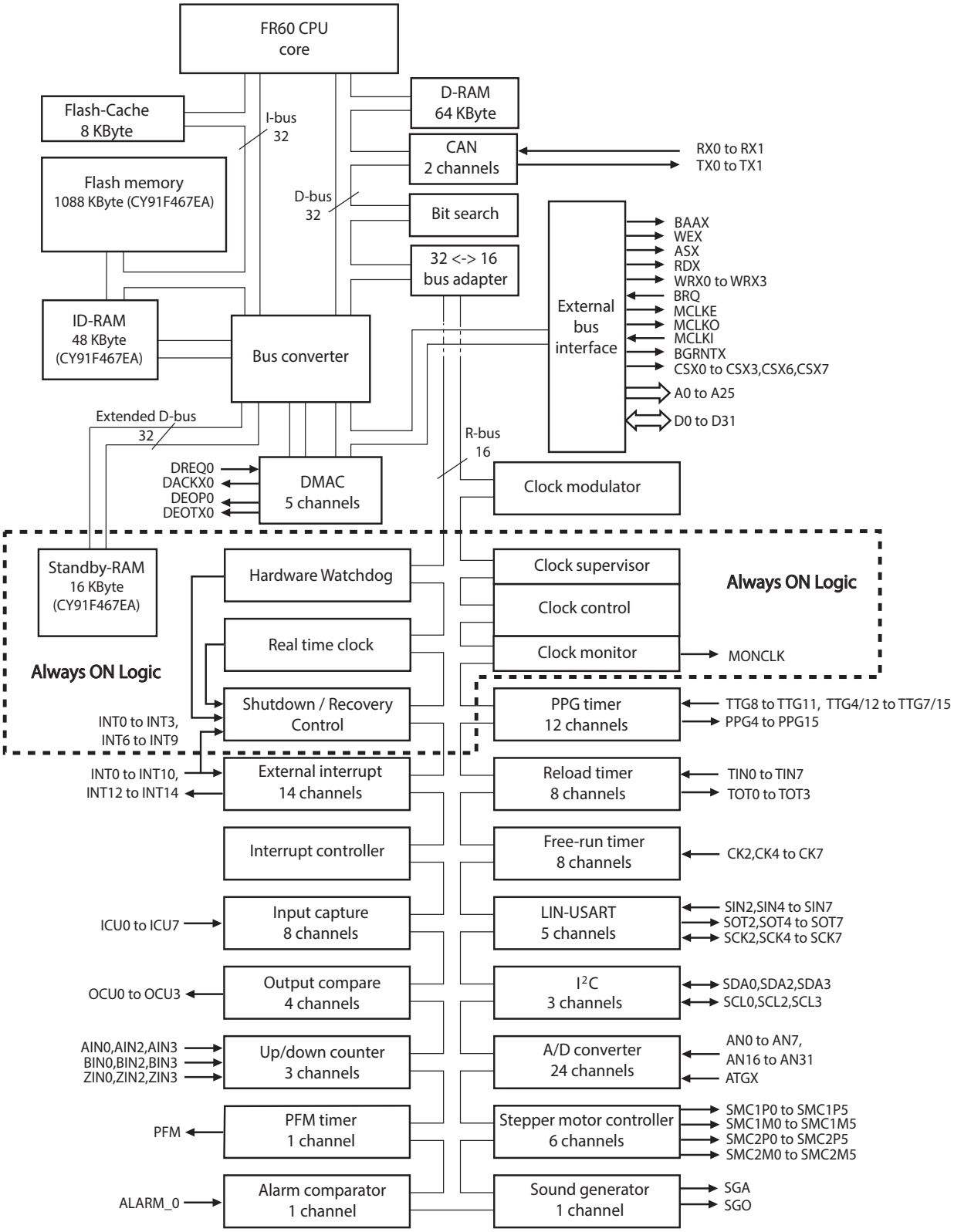
To prevent this, do not set (word) access to the area containing the address of the system stack pointer as the target of the hardware break (including an event breaks).

6.3 Operand Break

It may cause malfunctions if a stack pointer exists in the area which is set as the DSU operand break. Do not set the access to the areas containing the address of system stack pointer as a target of data event break.

7. Block Diagram

7.1 CY91F467EA



8. A/D Converter/Range Comparator

The new A/D Converter with Range Comparator is available on CY91FV460B and some new flash devices and is backward compatible to the A/D converter used on older devices. Beside the Range Comparator, 32 separated result data registers, a second interrupt flag and a new behaviour regarding reading the ADCS0.ACH[5:0] bits have been implemented.

There is one software incompatibility: Read-modify-write operation to the register ADCS0 is not allowed. See the description of the ADCS0.ACH[5:0] bits on page 31ff.

This chapter provides an overview of the A/D converter, describes the register structure and functions, and describes the operation of the A/D converter.

8.1 Overview of A/D Converter and A/D Range Comparator

The A/D converter converts analog input voltages into digital values and provides the following features. Any ADC cannel can be assigned to one of 4 Range Comparators.

8.1.1 Features of the A/D converter:

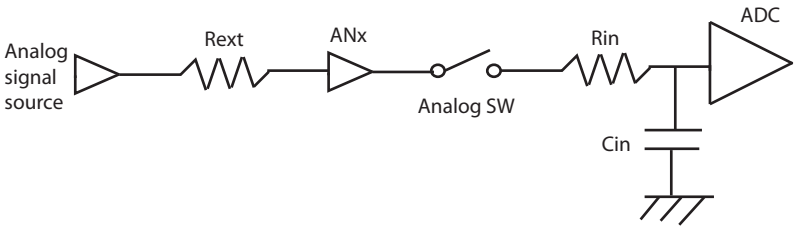
- Conversion time: minimum 1 µs per channel.
- RC type successive approximation conversion with sample & hold circuit
- 10-bit or 8-bit resolution
- Program section analog input from 32 channels
- 1 common result data register and 32 dedicated channel result data registers
- Single conversion mode:Convert the specified channel(s) only once.
- Continuous mode:Repeatedly convert the specified channels.
- Scan conversion mode: Continuous conversion of multiple channels, programmable for up to 32 channels
- Stop mode:Convert one channel, then temporarily halt until the next activation.
  (Enables synchronization of the conversion start timing.)
- A/D conversion can be followed by an A/D conversion interrupt request to CPU. This interrupt, an option that is ideal for continuous processing can be used to start a DMA transfer of the results of A/D conversion to memory.
- A/D conversion of all enabled channels (scan conversion) can be followed by an A/D End of Scan interrupt request to CPU. The data is stored into dedicated channel result registers, which can be read out using DMA transfer.
- Conversion startup may be by software, external trigger (falling edge) or timer (rising edge).

8.1.2 Features of the A/D Range Comparator (RCO):

- 4 conversion result Range Comparator channels, comparing the upper 8 bit of the conversion result with an upper and a lower threshold. The thresholds are programmable for the 4 comparators independendly.
- Any ADC channel can be assigned to one of the 4 range comparators.
- The comparision results will set “overflow” and “interrupt” flags per ADC channel, depending on the configuration. It is possible to configure the comparision for:
  - “out of range”: The flags are set if the A/D result is below the lower OR above the upper threshold.
  - “inside range”: The flags are set if the A/D result is above the lower AND below the upper threshold.
- The configuration can be set individually per ADC channel.
- Range comparision can be followed by an A/D Range Comparator interrupt request to CPU.

8.2 A/D Converter Input Impedance

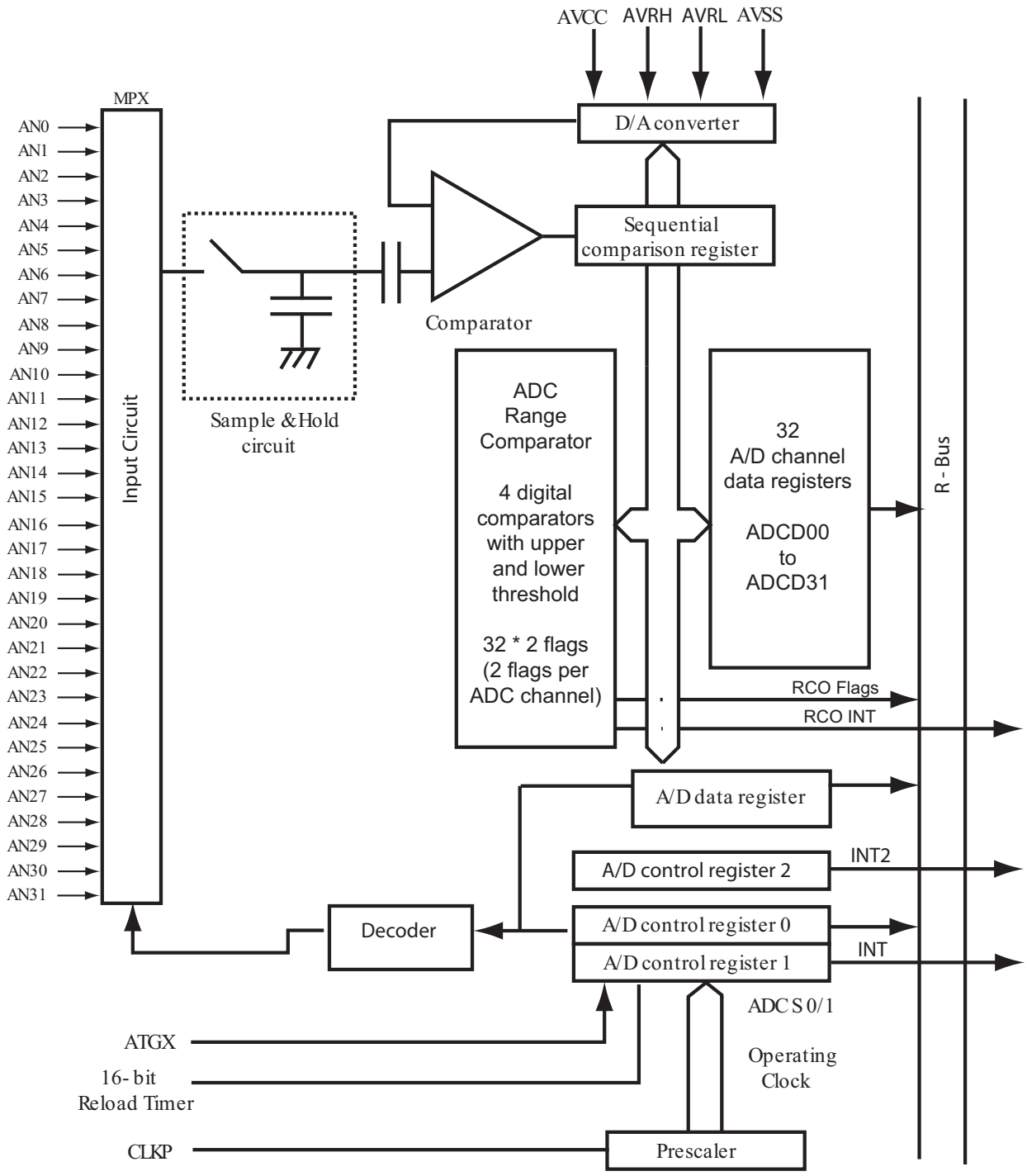
The following figure shows the sampling circuit of the A/D converter:



Do not set Rext over maximum sampling time (Tsamp).
Rext = Tsamp / (7*Cin) - Rin

8.3 Block Diagram of A/D Converter

The following figure shows block diagram of A/D converter.



8.4 Registers of the A/D Converter

The A/D converter with Range Comparator has the following registers:

Address (ADC0)	Address (ADC1 [1])	x=0 or 1 for ADC0, ADC1 [1] respectively				Register
		+0	+1	+2	+3	
$0001A0_H$	$0005E0_H$	ADxERH		ADxERL		A/D channel Enable register
$0001A4_H$	$0005E4_H$	ADxCS1	ADxCS0	ADxCR1	ADxCR0	A/D Control / Status register 0 + 1, A/D Conversion Result register
$0001A8_H$	$0005E8_H$	ADxCT1	ADxCT0	ADxSCH	ADxECH	Sampling timer setting register, Start Channel setting register, End Channel setting register
$0006B0_H$	$0006DC_H$	ADxCS2	-	-	-	A/D Control / Status register 2
000688_H	$0006B4_H$	RCOxH0	RCOxL0	RCOxH1	RCOxL1	Range Comparator 0,1 High/Low threshold registers
$00068C_H$	$0006B8_H$	RCOxH2	RCOxL2	RCOxH3	RCOxL3	Range Comparator 2,3 High/Low threshold registers
000690_H	$0006BC_H$	RCOxIRS				Range Comparator Inverted Range Select control
000694_H	$0006C0_H$	RCOxOF				Range Comparator Overflow flags
000698_H	$0006C4_H$	RCOxINT				Range Comparator Interrupt flags
$0006A0_H$	$0006CC_H$	ADxCC0	ADxCC1	ADxCC2	ADxCC3	Channel control for ch 0 to 7
$0006A4_H$	$0006D0_H$	ADxCC4	ADxCC5	ADxCC6	ADxCC7	Channel control for ch 8 to 16
$0006A8_H$	$0006D4_H$	ADxCC8	ADxCC9	ADxCC10	ADxCC11	Channel control for ch 16 to 23
$0006AC_H$	$0006D8_H$	ADxCC12	ADxCC13	ADxCC14	ADxCC15	Channel control for ch 24 to 31
$0006E0_H$	000720_H	ADCxD0		ADCxD1		ADC Channel Data register, channel 0,1
$0006E4_H$	000724_H	ADCxD2		ADCxD3		ADC Channel Data register, channel 2,3
$0006E8_H$	000728_H	ADCxD4		ADCxD5		ADC Channel Data register, channel 4,5
$0006EC_H$	$00072C_H$	ADCxD6		ADCxD7		ADC Channel Data register, channel 6,7
$0006F0_H$	000730_H	ADCxD8		ADCxD9		ADC Channel Data register, channel 8,9
$0006F4_H$	000734_H	ADCxD10		ADCxD11		ADC Channel Data register, channel 10,11
$0006F8_H$	000738_H	ADCxD12		ADCxD13		ADC Channel Data register, channel 12,13
$0006FC_H$	$00073C_H$	ADCxD14		ADCxD15		ADC Channel Data register, channel 14,15
000700_H	000740_H	ADCxD16		ADCxD17		ADC Channel Data register, channel 16,17
000704_H	000744_H	ADCxD18		ADCxD19		ADC Channel Data register, channel 18,19
000708_H	000748_H	ADCxD20		ADCxD21		ADC Channel Data register, channel 20,21
$00070C_H$	$00074C_H$	ADCxD22		ADCxD23		ADC Channel Data register, channel 22,23
000710_H	000750_H	ADCxD24		ADCxD25		ADC Channel Data register, channel 24,25
000714_H	000754_H	ADCxD26		ADCxD27		ADC Channel Data register, channel 26,27
000718_H	000758_H	ADCxD28		ADCxD29		ADC Channel Data register, channel 28,29
$00071C_H$	$00075C_H$	ADCxD30		ADCxD31		ADC Channel Data register, channel 30,31

1. On CY91F467E, ADC1 does not exist.

8.4.1 A/D Input Enable Register (ADER)

This register enables the analog input functions of the A/D converter. On CY91FV460B, additionally the bit **ADCHE** in PORTEN register influences the enabling of analog input.

■ **ADERH**: Access: Word, Half-word, Byte

31	30	29	28	27	26	25	24	Bit
ADE31	**ADE30**	**ADE29**	**ADE28**	**ADE27**	**ADE26**	**ADE25**	**ADE24**	
0	0	0	0	0	0	0	0	Initial value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute

23	22	21	20	19	18	17	16	Bit
ADE23	**ADE22**	**ADE21**	**ADE20**	**ADE19**	**ADE18**	**ADE17**	**ADE16**	
0	0	0	0	0	0	0	0	Initial value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute

■ **ADERL**: Access: Word, Half-word, Byte

15	14	13	12	11	10	9	8	Bit
ADE15	**ADE14**	**ADE13**	**ADE12**	**ADE11**	**ADE10**	**ADE9**	**ADE8**	
0	0	0	0	0	0	0	0	Initial value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute

7	6	5	4	3	2	1	0	Bit
ADE7	**ADE6**	**ADE5**	**ADE4**	**ADE3**	**ADE2**	**ADE1**	**ADE0**	
0	0	0	0	0	0	0	0	Initial value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute

[ADE31-0]: A/D Input Enable

ADEn	PORTEN.ADCHE	Function
0 [initial]	X	Analog input of A/D channel n is disabled. The ADC will not sample/convert this channel.
1	0 [initial]	Analog input of the channel n is enabled. Additionally, the port function register (PFR,EPFR) of the corresponding port must be set. The PFR/EPFR will switch the port to input direction (output driver = HiZ) and disable the digital input lines.
	1	Analog input of the channel n is enabled. Setting the port function register(s) is not necessary. ADEn will disable the digital input lines of the ports, but it does not change the port's direction.

❒ Software reset (RST) clears ADEn and PORTEN.ADCHE to 0.
❒ Be sure to set start channel and end channel to cover all enabled channels.

8.4.2 A/D Control Status Registers (ADCS2, ADCS1, ADCS0)

The A/D control status registers control and show the status of A/D converter. Do not overwrite ADCS0 register during A/D converting.

■ **ADCS2**: Access: Byte

15	14	13	12	11	10	9	8	Bit
BUSY	**INT**	**INTE**	**PAUS**	**-**	**-**	**INT2**	**INTE2**	
0	0	0	0	0	0	0	0	Initial value
R	R	R	R	R0	R0	R/W	R/W	Attribute

[bits 15:12] BUSY, INT, INTE, PAUS

These bits are a mirror of the corresponding bits in ADCS1, intended to quickly read out all status and interrupt information using only one register access. To write the bits, access them via ADCS1.

[bits 11:10] -

These bits do not exist. Read operation returns 0.

[bit 9] INT2 (End of Scan Flag)

The End of Scan flag is set when conversion data of the last channel is stored in ADCR, whereas the last channel is defined by ADECH register setting.

- If bit 8 (INTE2) is "1" when this bit is set, and the ADC runs in continous conversion mode, an End of Scan interrupt request is generated or, if activation of DMA is enabled, DMA is activated.
- Only clear this bit by writing "0" when A/D conversion is halted.
- Initialized to "0" by a reset.
- If DMA is used, this bit is cleared at the end of DMA transfer.
- Read-modify-write operations read this bit as “1”.

[bit 8] INTE2 (Enable End of Scan Interrupt)

INTE2 enables the End of Scan interrupt in continous conversion mode. In the other conversion modi, this bit has no effect.

Additionally, setting INTE2 changes the protect function of converted data (see description of ADCS1.PAUS).

INTE2	Function
0 [initial]	Disable End of Scan interrupt, ADC result protection protects the ADCR register data.
1	Enable End of Scan interrupt, ADC result protection protects the ADCD0...ADCD31 register data (in continuous conversion mode only)

■ **ADCS1**: Access: Half-word, Byte

15	14	13	12	11	10	9	8	Bit
BUSY	**INT**	**INTE**	**PAUS**	**STS1**	**STS0**	**STRT**	**reserved**	
0	0	0	0	0	0	0	0	Initial value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute

[bit 15] BUSY (busy flag and stop)

BUSY	Function
Reading	A/D converter operation indication bit. Set on activation of A/D conversion and cleared on completion.
Writing	Writing "0" to this bit during A/D conversion forcibly terminates conversion. Use to forcibly terminate in continuous and stop modes.

- Read-modify-write instructions read the bit as "1".
- Cleared on the completion of A/D conversion in single conversion mode.
- In continuous and stop mode, the flag is not cleared until conversion is terminated by writing "0".
- Initialized to "0" by a software reset (RST).

- Do not specify forcible termination and software activation (BUSY="0" and STRT="1") at the same time.

[bit 14] INT (End of Conversion Interrupt flag)

This bit is set when conversion data is stored in ADCR.

- If bit 5 (INTE) is "1" when this bit is set, an interrupt request is generated or, if activation of DMA is enabled, DMA is activated.
- Only clear this bit by writing "0" when A/D conversion is halted.
- Initialized to "0" by a software reset (RST).
- If DMA is used, this bit is cleared at the end of DMA transfer.

[bit 13] INTE (End of Conversion Interrupt enable)

This bit is enables or disables the conversion completion interrupt.

INTE	Function
0	Disable interrupt [Initial value]
1	Enable interrupt

- Cleared by a software reset (RST).

[bit 12] PAUS (A/D converter pause)

This bit is set when A/D conversion temporarily halts.

The A/D converter has one register to store the conversion result (ADCR) and additionally 32 ADC channel data registers. If a conversion is finished and the data of the previous conversion has not been read out before, previous data would be overwritten.

To avoid this problem, the next conversion data is not stored in the data registers until the previous value has been read out (e.g. by DMA). A/D conversion halts during this time. A/D conversion resumes when the ADC interrupt flag ADCR1.INT is cleared.

The register protection function depends on the conversion mode and the setting of ADCR2.INTE2:

Mode	INTE2	Function
Single, Stop	X	Protect ADCR (the common result register)
Continous	0	Protect ADCR (the common result register)
	1	Protect ADCD0...ADCD31 (the dedicated channel data registers)

- In continous mode with INTE2==1, PAUS is set when data of the **start channel** (set by ADSCH) is ready for writing to the registers, but IRQ2 (End of Scan interrupt) is active.
- In the other modes or if INTE2==0, PAUS is set when data of any channel is ready for writing to the registers, but IRQ (End of Conversion) is active.
- PAUS is cleared by writing "0" or by a reset. (Not cleared at the end of DMA transfer.) However when waiting condition of DMA transfer, this bit cannot be cleared.
- Regarding protect function of converted data, see Section “8.6 Operation of A/D Converter".

[bit 11, 10] STS1, STS0 (Start source select)

These bits select the A/D activation source.

STS1	STS0	Function
0	0	Software activation [Initial value]
0	1	External trigger pin activation and software activation
1	0	Timer activation and software activation
1	1	External trigger pin activation, timer activation and software activation

- These bits are initialized "00" by software reset (RST).
- In multiple-activation modes, the first activation to occur starts A/D conversion.
- The activation source changes immediately on writing to the register. Therefore care is required when switching activation mode during A/D operation.
- The A/D converter detects falling edges on the external trigger pin. When external trigger level is "L" and if these bits are changed to external trigger activation mode, A/D converting may starts.
- Selecting the timer selects the 16-bit reload timer 7.

[bit 9] STRT (Start)

Writing "1" to this bit starts A/D conversion (software activation).

- Write "1" again to restart conversion.
- Initialized to "0" by a software reset (RST).
- In continuous and stop mode, restarting is not occurred. Check BUSY bit before writing "1". (Activate conversion after clearing.)
- Do not specify forcible termination and software activation (BUSY="0" and STRT="1") at the same time.

[bit 8] reserved bit

Always write "0" to this bit.

■ **ADCS0**: Access: Half-word, Byte. Read-modify-write access is not allowed

7	6	5	4	3	2	1	0	Bit
MD1	**MD0**	**S10**	**ACH4**	**ACH3**	**ACH2**	**ACH1**	**ACH0 / ACHMD**	
0	0	0	0	0	0	0	0	Initial value
R/W	R/W	R/W	R	R	R	R	R,**W** [1]	Attribute

1. ACHMD is a new, control bit, see "[bit 0] ACHMD (ACH register mode, write-only)" on page 32.

[bit 7, 6] MD1, MD0 (A/D converter mode set)

These bits the operation mode.

MD1	MD0	Operating mode
0	0	Single mode 1 (Reactivation during A/D conversion is allowed)
0	1	Single mode 2 (Reactivation during A/D conversion is not allowed)
1	0	Continuous mode (Reactivation during A/D conversion is not allowed)
1	1	Stop mode (Reactivation during A/D conversion is not allowed)

- Single mode:A/D conversion is continously performed from the selected start channel (ADSCH) to the selected end channel (ADECH). The conversion stops once it has been done for all these channels.
- Continuous mode:A/D conversion is repeatedly performed from the selected start channel (ADSCH) to the selected end channel (ADECH) in a row.
- Stop mode:A/D conversion is performed from the selected start channel (ADSCH) to the selected end channel (ADECH), followed by a pause after each channel. The conversion is resumed upon activation.

When A/D conversion is started in continuous mode or stop mode, conversion operation continued until stopped by the BUSY bit.

Conversion is stopped by writing "0" to the BUSY bit.

On activation after forcibly stopping, conversion starts from the start channel, selected by ADSCH register.

Reactivation during A/D conversion is disabled for any of the timer, external trigger and software start sources in single mode 2, continuous and stop mode.

[bit 5] S10

This bit defines resolution of A/D conversion. If this bit set "0", the resolution is 10-bit. In the other case, resolution is 8-bit and the conversion result is stored to ADCR0 and in the lower 8 bits of the dedicated ADC result registers.

- Initialized to "0" by a reset.

[bit 4 to 0] ACH4-0 (Analog convert select channel, read-only)

These bits show the number of the currently or previously converted analog channel, depending on bit ACHMD (see below).

ACH4	ACH3	ACH2	ACH1	ACH0	Converted channel
0	0	0	0	0	AN0
0	0	0	0	1	AN1
...					...
1	1	1	1	0	AN30
1	1	1	1	1	AN31

- Writing these bits has no effect (bit 0 is writeable with special function ADCHMD).
- Initialized to "0000" by software reset (RST).

[bit 0] ACHMD (ACH register mode, write-only)

For reading out the ACH4-0 register bits (see below), there is a *direct* mode and a *latched* mode.

In direct mode, ACH4-0 shows the number of the ADC channel which is *currently in conversion*, e.g. the internal conversion channel pointer. This pointer is incremented immediately after a conversion is finished. On CY91460 series devices having the old ADC macro, ACH4-0 always show this mode.

In the new latched mode, ACH4-0 shows the number of the ADC channel whose conversion was *finished previously.* After a conversion is finished, the conversion channel pointer is latched and the latched data can be read in this mode. At the end of the next conversion, the latch is overwritten if no PAUSE condition exists.

ACHMD	Function
0	Direct ACH register mode [Initial value]
1	Latched ACH register mode

- ACHMD is a write-only bit.
- Read- or read-modify-write access returns the value of bit ACH0, that's why read-modify-write access is not allowed.
- Initial value is 0.

8.4.3 Common Data Register (ADCR1, ADCR0)

These registers store the conversion results of the A/D converter. ADCR0 stores lower 8-bit. ADCR1 stores upper 2-bit. The register values are updated at the completion of each conversion. The registers normally store the results of the previous conversion.

■ **ADCR1**: Access: Word, Half-word, Byte

15	14	13	12	11	10	9	8	Bit
-	-	-	-	-	-	**D9**	**D8**	
0	0	0	0	0	0	X	X	Initial value
R0, W0	R0, W0	R0, W0	R0, W0	R0, W0	R0, W0	R	R	Attribute

■ **ADCR0**: Access: Word, Half-word, Byte

7	6	5	4	3	2	1	0	Bit
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
X	X	X	X	X	X	X	X	Initial value
R	R	R	R	R	R	R	R	Attribute

■ Bit 15 to 10 of ADCR1 are read as "0".

■ The A/D converter has a conversion data protection function. See the "Operation" section for further information.

8.4.4 Dedicated A/D Channel Data Register (ADCD0 to ADCD31)

There are 32 ADC result data registers, one per channel. The registers are written by hardware at the end of conversion of the attached channel. ADCD0 is attached to channel 0, ADCD31 is attached to channel 31.

■ **ADCD0 ... ADCD31**: Access: Word, Half-word, Byte

15	14	13	12	11	10	9	8	Bit
-	-	-	-	-	-	**D9**	**D8**	
0	0	0	0	0	0	X	X	Initial value
R0	R0	R0	R0	R0	R0	R	R	Attribute

7	6	5	4	3	2	1	0	Bit
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
X	X	X	X	X	X	X	X	Initial value
R	R	R	R	R	R	R	R	Attribute

■ Bit 15 to 10 of the ADCD registers are read as "0".

■ The A/D converter has a conversion data protection function. In continous conversion mode, the protection function can be changed to protect the A/D Channel Data registers rather then the A/D Data Register (ADCR1). See section "8.6.6 Protection of the ADC Channel Data Registers" for further information.

8.4.5 Sampling Timer Setting Register (ADCT)

ADCT register controls the sampling time and comparison time of analog input. This register sets A/D conversion time. Do not update value of this register during A/D conversion operation.

■ **ADCT1**: Access: Word, Half-word, Byte

15	14	13	12	11	10	9	8	Bit
CT5	**CT4**	**CT3**	**CT2**	**CT1**	**CT0**	**ST9**	**ST8**	
0	0	0	1	0	0	0	0	Initial value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute

■ **ADCT0**: Access: Word, Half-word, Byte

7	6	5	4	3	2	1	0	Bit
ST7	**ST6**	**ST5**	**ST4**	**ST3**	**ST2**	**ST1**	**ST0**	
0	0	1	0	1	1	0	0	Initial value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute

[bit 15 to 10] CT5-0 (A/D comparison time set)

These bits specify clock division of comparison time.

- ❒ Setting "000001" means one division (=CLKP).
- ❒ Do not set these bits "000000".
- ❒ Initialized these bits to "000100" by software reset (RST).
- ❒ Comparison time = CT value * CLKP cycle * 10 + (4 * CLKP)
- ❒ Do not set comparison time over 500 µs.

[bit 9 to 0] ST9-0 (Analog input sampling time set)

These bits specify sampling time of analog input.

- ❒ Initialized these bits to "0000101100" by software reset (RST).
- ❒ Sampling time = ST value * CLKP cycle
- ❒ Do not set sampling time below 1.2 µs when AVCC is below 4.5 V.

Necessary sampling time and ST value are calculated by following.

- ❒ Necessary sampling time (Tsamp) = (Rext + Rin) * Cin * 7
- ❒ ST9 to ST0 = Tsamp / CLKP cycle

ST has to be set that sampling time is over Tsamp.
Example: CLKP = 32 MHz, AVCC >= 4.5 V, Rext = 200K-

Tsamp = (200 * 103 + 2.52 * 103) * 10.7 * 10-12 * 7 = 15.17 [us]
ST = 15.17-6 / 31.25-9 = 485.44
ST has to be set over 486_D (111100110_B).

Tsamp is decided by Rext. Thus conversion time should be considered together with Rext.

8.4.6 A/D Channel Setting Register (ADSCH, ADECH)

These registers specify the channels for the A/D converter to convert. Do not update these registers while the A/D converting is operating.

■ **ADSCH**: Access: Word, Half-word, Byte

15	14	13	12	11	10	9	8	Bit
-	**-**	**-**	**ANS4**	**ANS3**	**ANS2**	**ANS1**	**ANS0**	
-	-	-	0	0	0	0	0	Initial value
RX, W0	RX, W0	RX, W0	R/W	R/W	R/W	R/W	R/W	Attribute

■ **ADECH**: Access: Word, Half-word, Byte

7	6	5	4	3	2	1	0	Bit
-	**-**	**-**	**ANE4**	**ANE3**	**ANE2**	**ANE1**	**ANE0**	
-	-	-	0	0	0	0	0	Initial value
RX, W0	RX, W0	RX, W0	R/W	R/W	R/W	R/W	R/W	Attribute

These bits set the start and end channel for A/D converter.

- ❒ Setting of ANE4 to ANE0 the same channel as in ANS4 to ANS0 specifies conversion for that channel only. (Single conversion)
- ❒ In continuous or stop mode, conversion is performed up to the channel specified by ANE4 to ANE0. Conversion then starts again from the start channel specified by ANS4 to ANS0.
- ❒ If ANS > ANE, conversion starts with the channel specified by ANS, continuous up to channel 31, starts again from channel 0, and ends with the channel specified by ANE.
- ❒ Initialized to ANS="00000", ANE="00000" by a software reset (RST).

Example: Channel Setting ANS=30 ch, ANE=3 ch, single conversion mode

Operation: Conversion channel 30 ch -> 31 ch -> 0 ch -> 1 ch -> 2 ch -> 3 ch end

[bit 12 to 8] ANS4-0 (Analog start channel set)

[bit 4 to 0] ANE4-0 (Analog end channel set)

ANS4 ANE4	ANS3 ANE3	ANS2 ANE2	ANS1 ANE1	ANS0 ANE0	Start / End Channel
0	0	0	0	0	AN0
0	0	0	0	1	AN1
0	0	0	1	0	AN2
0	0	0	1	1	AN3
...					...
1	1	1	0	1	AN29
1	1	1	1	0	AN30
1	1	1	1	1	AN31

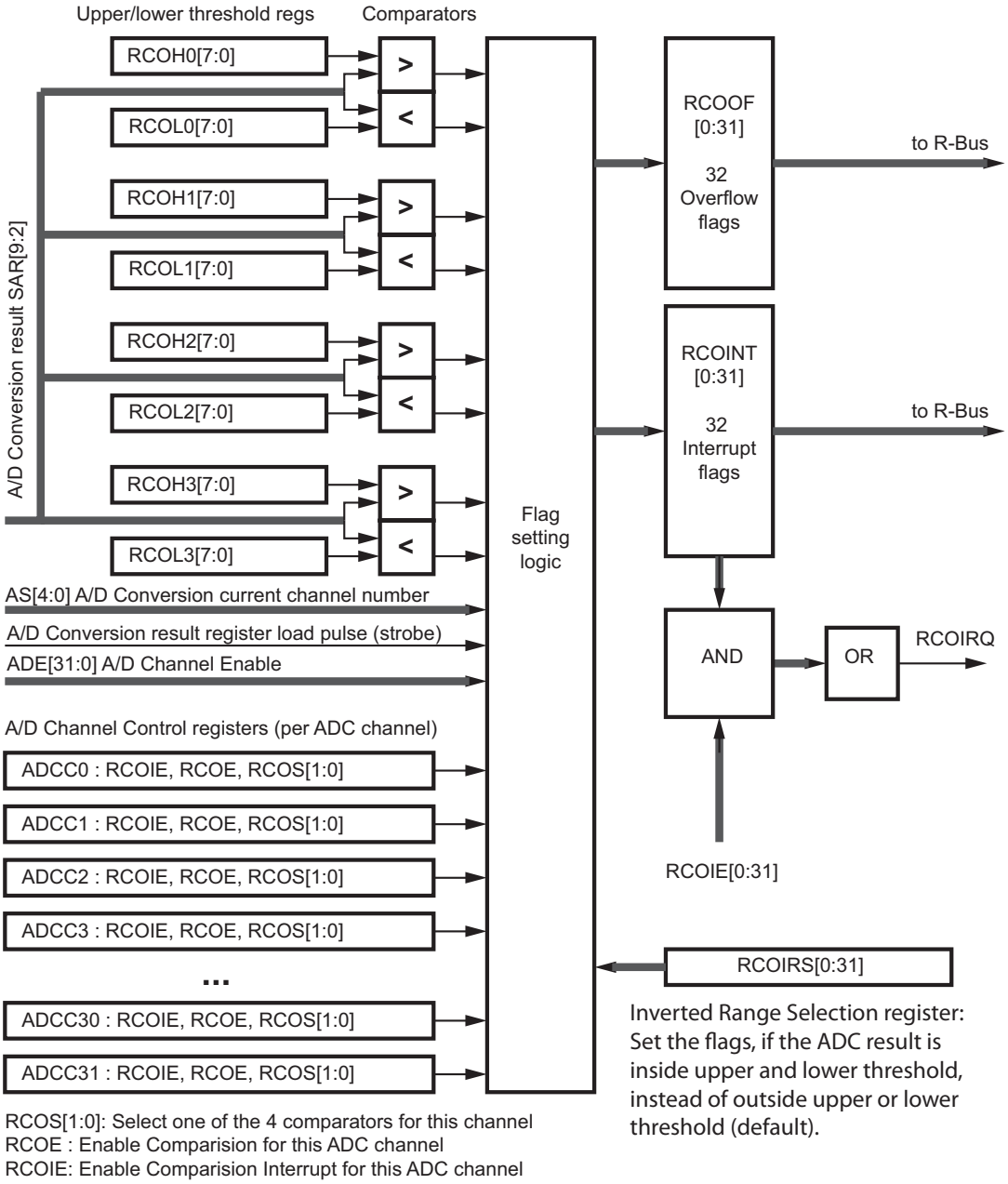
8.5 Range Comparator

8.5.1 Range Comparator Structure

The Range Comparator has 4 comparsion groups with an upper and a lower threshold register each. The 32 ADC channels can be enabled for range comparision and assigned to one of the 4 comparators individually. If enabled, the comparsision will set up to 2 flags for this ADC channel:

- An interrupt flag RCOINT, signalling that the ADC result is outside the range or, by “inverted” configuration, inside the range.
- An overflow flag RCOOF, showing that the range violation was an overflow and no underflow.

Furthermore, each ADC channel can be enabled to send an interrupt request to the CPU, if the RCOINT flag is set.



RCOS[1:0]: Select one of the 4 comparators for this channel
RCOE : Enable Comparision for this ADC channel
RCOIE: Enable Comparision Interrupt for this ADC channel

8.5.2 Range Comparator Registers

The Range Comparator (RCO) has the following registers:

- RCOHx[7:0]: Upper threshold register, one register per comparator block (x = 0...3)
- RCOLx[7:0]: Lower threshold register, one register per comparator block (x = 0...3)
- ADCCm[7:0]: ADC channel control, one register per 2 ADC channels (m = 0...15)
- RCOIRS[0:31]: RCO Inverted Range Selection, one bit per ADC channel
- RCOOF[0:31]: RCO Overflow Flags, one bit per ADC channel, read-only
- RCOINT[0:31]: RCO Interrupt Flags, one bit per ADC channel

Range Comparator Threshold registers (RCOH0/L0 to RCOH3/L3)

- **RCOH0-3**: Higher threshold, access: Word, Half-word, Byte

15	14	13	12	11	10	9	8	Bit
RCOH7	**RCOH6**	**RCOH5**	**RCOH4**	**RCOH3**	**RCOH2**	**RCOH1**	**RCOH0**	
1	1	1	1	1	1	1	1	Initial value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute

[bit 7:0] RCOH[7:0] (Range Comparator High threshold)

The RCOH bits define the higher comparision threshold of the Range Comparator channel.

The upper Range Comparator compares that the upper 8 bits of the ADC conversion result are higher then RCOH[7:0]

- **RCOL0-3**: Lower threshold, access: Word, Half-word, Byte

7	6	5	4	3	2	1	0	Bit
RCOL7	**RCOL6**	**RCOL5**	**RCOL4**	**RCOL3**	**RCOL2**	**RCOL1**	**RCOL0**	
0	0	0	0	0	0	0	0	Initial value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute

[bit 7:0] RCOL[7:0] (Range Comparator Low threshold)

The RCOL bits define the lower comparision threshold of the Range Comparator channel.

The lower Range Comparator compares that the upper 8 bits of the ADC conversion result are lower then RCOL[7:0]

A/D Converter Channel Control registers (ADCC0 to ADCC15)

The A/D channel control registers serve 2 ADC channels per register and control the range comparision for these channels.

ADCC0 register controls A/D channels 0 + 1,
ADCC1 register controls A/D channels 2 + 3,
...
ADCC15 register controls A/D channels 30 + 31

■ **ADCC0-15**: Access: Word, Half-word, Byte

7	6	5	4	3	2	1	0	Bit
RCOIE1	**RCOE1**	**RCOS11**	**RCOS10**	**RCOIE0**	**RCOE0**	**RCOS01**	**RCOS00**	
0	0	0	0	0	0	0	0	Initial value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute
Bits 7:4 control A/D channels 1,3,5,7,...31				Bits 3:0 control A/D channels 0,2,4,6,...,30				

[bit 7,3] RCOIE1, RCOIE0 (Range Comparator Interrupt enable)

The RCOIE bits enable the Range Comparator interrupt for the corresponding ADC channel.

RCOIE	Function
0	RCO interrupt for this ADC channel is disabled [default]
1	RCO interrupt for this ADC channel is enabled

[bit 6,2] RCOE1, RCOE0 (Range Comparator operation enable)

The RCOE bits enable the Range Comparision for the corresponding ADC channel:

RCOE	Function
0	RCO disabled, RCO flags for this ADC channel will not be set [default]
1	RCO enabled for this ADC channel

[bits 5:4,1:0] RCOS1[1:0], RCOS0[1:0] (converter channel select)

These bits select the A/D converter channel to be assigned to the Range Comparator channel:

RCOS[1:0]	Function
00	Select range comparator channel 0 for this ADC channel [default]
01	Select range comparator channel 1 for this ADC channel
10	Select range comparator channel 2 for this ADC channel
11	Select range comparator channel 3 for this ADC channel

Inverted Range Selection register

The RCOIRS register controlles that the comparision should check for “out of range” or “inside range”.
The 32 bits of RCOIRS is organized “per ADC channel”. ADC channel 0 is located on the MSB of the register and ADC channel 31 is on the LSB.

■ **RCOIRS**: Access: Word, Half-word, Byte

31	30	29	28	27	26	259	24	Bit
RCOIRS0	**RCOIRS1**	**RCOIRS2**	**RCOIRS3**	**RCOIRS4**	**RCOIRS5**	**RCOIRS6**	**RCOIRS7**	
0	0	0	0	0	0	0	0	Initial value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute
23	22	21	20	19	18	17	16	Bit
RCOIRS8	**RCOIRS9**	**RCOIRS10**	**RCOIRS11**	**RCOIRS12**	**RCOIRS13**	**RCOIRS14**	**RCOIRS15**	
0	0	0	0	0	0	0	0	Initial value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute
15	14	13	12	11	10	9	8	Bit
RCOIRS16	**RCOIRS17**	**RCOIRS18**	**RCOIRS19**	**RCOIRS20**	**RCOIRS21**	**RCOIRS22**	**RCOIRS23**	
0	0	0	0	0	0	0	0	Initial value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute
7	6	5	4	3	2	1	0	Bit
RCOIRS24	**RCOIRS25**	**RCOIRS26**	**RCOIRS27**	**RCOIRS28**	**RCOIRS29**	**RCOIRS30**	**RCOIRS31**	
0	0	0	0	0	0	0	0	Initial value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute

Note that bit[31] is assigned to ADC channel 0, bit[30] is assigned to ADC channel one and so on.

[bits 31:0] RCOIRS[0:31] (Inverted Range Select)

The RCOIRS bits control how the Range Comparator result flags are set.

- If the RCOIRS[n] is 0, the flags are set when the ADC result is above the upper threshold OR below the lower threshold. That is called “**out of range**” mode.
- If the RCOIRS[n] is 1, the flags are set when the ADC result is below or equal the upper threshold AND above or equal the lower threshold. That is called “**inside range**” mode.

RCOIRSn	Function
0	Range comparision for this ADC channel checks for “out of range” (default)
1	Range comparision for this ADC channel checks for “inside range”

Range Comparator Result Flags

The result of range comparision is stored in 2 flag registers:

- RCOINT[0:31]:Range comparision interrupt flags
- RCOOF[0:31]: Range comparision overflow flags

The Range Comparator Result flags are organized “per ADC channel”. There are 32 Range Comparator overflow flags and 32 interrupt flags. In case of a RCO interrupt, all interrupt flags can be read out by one 32-bit read operation and analyzed using the Bit Search Unit. The Bit Search Unit will return the number of the interrupting channel. Since bit search works from MSB to LSB (from left to right), ADC channel 0 is located on the MSB of the registers and ADC channel 31 is on LSB.

■ **RCOINT[0:31]**: Access: Word, Half-word, Byte

31	30	29	28	27	26	259	24	Bit
RCOINT0	**RCOINT1**	**RCOINT2**	**RCOINT3**	**RCOINT4**	**RCOINT5**	**RCOINT6**	**RCOINT7**	
0	0	0	0	0	0	0	0	Initial value
R/W0	R/W0	R/W0	R/W0	R/W0	R/W0	R/W0	R/W0	Attribute
23	22	21	20	19	18	17	16	Bit
RCOINT8	**RCOINT9**	**RCOINT10**	**RCOINT11**	**RCOINT12**	**RCOINT13**	**RCOINT14**	**RCOINT15**	
0	0	0	0	0	0	0	0	Initial value
R/W0	R/W0	R/W0	R/W0	R/W0	R/W0	R/W0	R/W0	Attribute
15	14	13	12	11	10	9	8	Bit
RCOINT16	**RCOINT17**	**RCOINT18**	**RCOINT19**	**RCOINT20**	**RCOINT21**	**RCOINT22**	**RCOINT23**	
0	0	0	0	0	0	0	0	Initial value
R/W0	R/W0	R/W0	R/W0	R/W0	R/W0	R/W0	R/W0	Attribute
7	6	5	4	3	2	1	0	Bit
RCOINT24	**RCOINT25**	**RCOINT26**	**RCOINT27**	**RCOINT28**	**RCOINT29**	**RCOINT30**	**RCOINT31**	
0	0	0	0	0	0	0	0	Initial value
R/W0	R/W0	R/W0	R/W0	R/W0	R/W0	R/W0	R/W0	Attribute

Note that bit[31] is assigned to ADC channel 0, bit[30] is assigned to ADC channel one and so on.

[bits 31:0] RCOINT[0:31] (Range Comparator Interrupt flags)

The RCOINT flags show that a “out of range” or “inside range” condition has been found on the ADC channel.

The bits are set under the following condition:

- the ADC channel is enabled ADER.ADE[i] is setand
- the range comparision for this channel is enabledADCCn.RCOE[i] is setand
- the conversion of the ADC channel is just finished and
- an interrupt condition was found (see the table on next page).

- The bits are cleared by writing 0 or by software reset (RST). Writing 1 has no effect.
- Read-modify-write operations read 1.

The interrupt condition depends on the comparision results and the RCOIRS setting for this channel:

Mode	RCOIRS	Upper threshold comparator	Lower threshold comparator	Interrupt condition
out of range	0	1	x	INT condition: above range, RCOOF is set
		0	0	-
		x	1	INT condition: below range, RCOOF is cleared

Mode	RCOIRS	Upper threshold comparator	Lower threshold comparator	Interrupt condition
inside range	1	1	x	-
		0	0	INT condition: inside range
		x	1	-

Note: The upper threshold comparator returns 1 if the upper 8 bits of the ADC result are greather then the threshold value in RCOH[7:0]. The lower threshold comparator returns 1 if the upper 8 bits of the ADC result are smaller then the threshold value in RCOL[7:0].

■ **RCOOF[0:31]**: Access: Read-only, Word, Half-word, Byte

31	30	29	28	27	26	259	24	Bit
RCOOF0	**RCOOF1**	**RCOOF2**	**RCOOF3**	**RCOOF4**	**RCOOF5**	**RCOOF6**	**RCOOF7**	
0	0	0	0	0	0	0	0	Initial value
R	R	R	R	R	R	R	R	Attribute

23	22	21	20	19	18	17	16	Bit
RCOOF8	**RCOOF9**	**RCOOF10**	**RCOOF11**	**RCOOF12**	**RCOOF13**	**RCOOF14**	**RCOOF15**	
0	0	0	0	0	0	0	0	Initial value
R	R	R	R	R	R	R	R	Attribute

15	14	13	12	11	10	9	8	Bit
RCOOF16	**RCOOF17**	**RCOOF18**	**RCOOF19**	**RCOOF20**	**RCOOF21**	**RCOOF22**	**RCOOF23**	
0	0	0	0	0	0	0	0	Initial value
R	R	R	R	R	R	R	R	Attribute

7	6	5	4	3	2	1	0	Bit
RCOOF24	**RCOOF25**	**RCOOF26**	**RCOOF27**	**RCOOF28**	**RCOOF29**	**RCOOF30**	**RCOOF31**	
0	0	0	0	0	0	0	0	Initial value
R	R	R	R	R	R	R	R	Attribute

Note that bit[31] is assigned to ADC channel 0, bit[30] is assigned to ADC channel one and so on.

[bits 31:0] RCOOF[0:31] (Range Comparator Overflow flag)

The RCOOF read-only flags store the output signal of the upper threshold comparator at the time when an interrupt condition (see above) appeared and the corresponding RCOINT flag was **not** set. So the RCOOF flags indicate the upper comparator state when the RCOINT flag had the last rising edge.

The RCOOF flag for a ADC channel is loaded with the upper threshold comparator output signal under the following condition:

- the corresponding RCOINT flag is not yet setand
- the corresponding RCOINT flag has a set condition in this cycle.

The flags are initialized by software reset (RST).

RCOOFn	Function
0	The output of the upper threshold comparator was 0 [default]
1	The output of the upper threshold comparator was 1

8.5.3 Range Comparator Interrupt request

The Range Comparator has one interrupt output line RCOIRQ. The interrupt output line becomes active if at least one of the Range Comparator interrupt flags RCOINT[31:0] is set and the corrsponding interrupt enable bit in the ADCC registers is set..

It is not possible to activate a DMA request from the range comparator interrupts.

8.6 Operation of A/D Converter

The A/D converter operates using the successive approximation method with 10-bit or 8-bit resolution. There is one 16-bit register provided to store conversion results (ADCR), which is updated each time conversion completes. Additionally, there is one ADC Channel Data register per channel (ADCD0...31), which is updated each time the assigned channel is converted. The Channel Data registers especially improve the continous conversion mode.
It is recommended to use the DMA service. The following describes the operation modes.

8.6.1 Single Mode

In single conversion mode, the analog input signals selected by the ANS bits and ANE bits are converted in order until the completion of conversion on the end channel determined by the ANE bits. A/D conversion then ends. If the start channel and end channel are the same (ANS=ANE), only a single channel conversion is performed.

Examples:

- ANS=00000b, ANE=00011b
  Start -> AN0 -> AN1 -> AN2 -> AN3 -> End
- ANS=00010b, ANE=00010b
  Start -> AN2 -> End

8.6.2 Continuous Mode

In continuous mode the analog input signals selected by the ANS bits and ANE bits are converted in order until the completion of conversion on the end channel determined by the ANE bits, then the converter returns to the ANS channel for analog input and repeats the process continuously. When the start and end channels are the same (ANS=ANE), conversion is performed continuously for that channel.

Examples:

- ANS=00000b, ANE=00011b
  Start -> AN0 -> AN1 -> AN2 -> AN3 -> AN0 ... -> repeat
- ANS=00010b, ANE=00010b
  Start -> AN2 -> AN2 -> AN2 ... -> repeat

  In continuous mode, conversion is repeated until '0' is written to the BUSY bit. (Writing '0' to the BUSY bit forcibly stops the conversion operation.) Note that forcibly terminating operation halts the current conversion during mid-conversion. (If operation is forcibly terminated, the value in the conversion register is the result of the most recently completed conversion.)

8.6.3 Stop Mode

In stop mode the analog input signal selected by the ANS bits and ANE bits are converted in order, but conversion operation pauses after each channel. The pause is released by applying another start signal.

At the completion of conversion on the end channel determined by the ANE bits, the converter returns to the ANS channel for analog input signal and repeats the conversion process continuously. When the start and end channel are the same (ANS=ANE), only a signal channel conversion is performed.

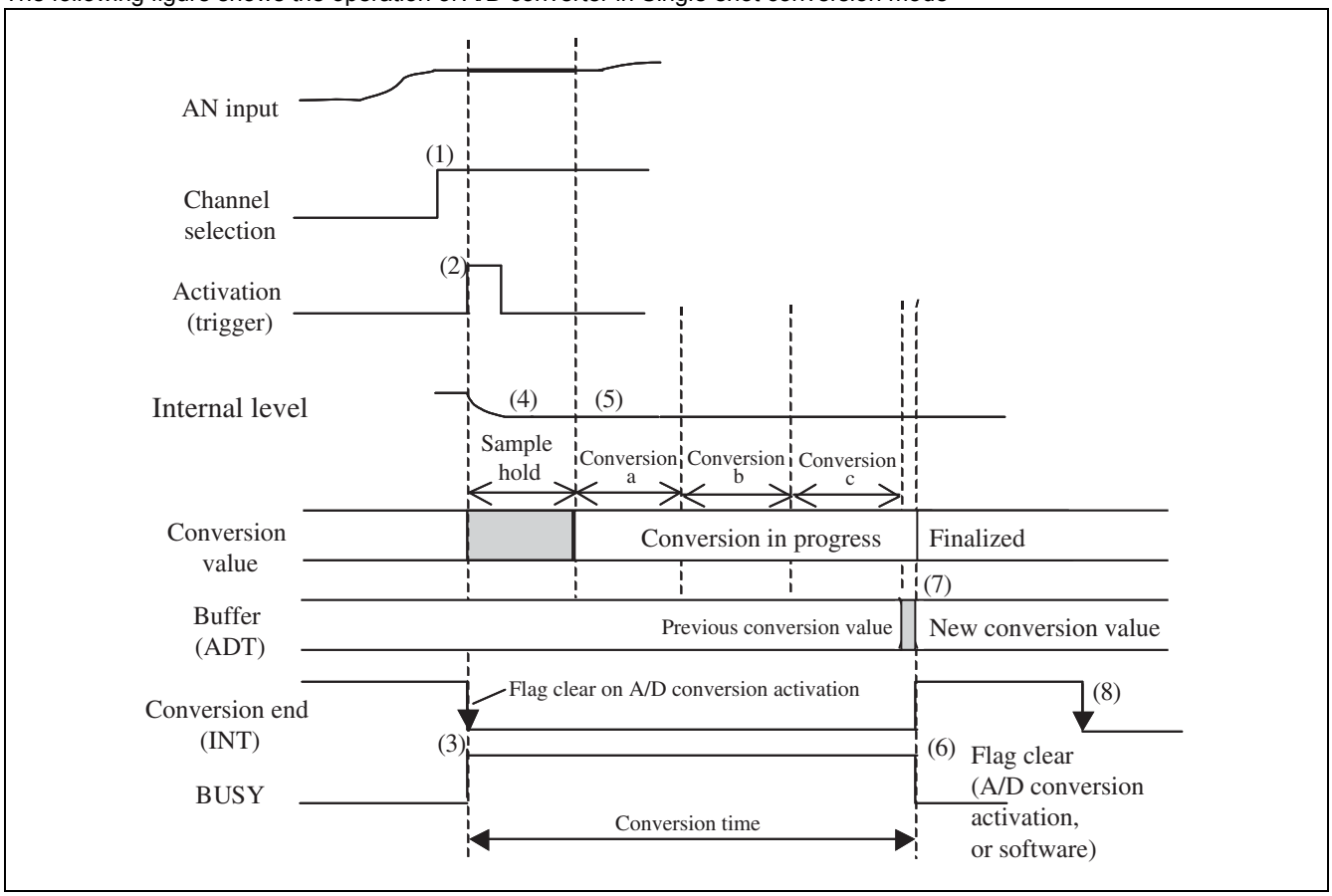
Examples:

- ANS=00000b, ANE=00011b
  Start -> AN0 -> stop -> start -> AN1 -> stop -> start -> AN2 -> stop -> start -> AN3 -> stop -> start -> AN0 ... -> repeat
- ANS=00010b, ANE=00010b
  Start -> AN2 -> stop -> start -> AN2 -> stop -> start -> AN2 ... -> repeat

  In stop mode the startup source is the source determined by the STS1, STS0 bits. This mode enables synchronization of the conversion start signal.

8.6.4 Single-shot Conversion

The following figure shows the operation of A/D converter in Single-shot conversion mode



(1)Channel selection

(2)A/D conversion activation (Trigger input: Software trigger/Reload timer/External trigger)

(3)INT flag clear, BUSY flag set

(4)Sample hold

(5)Conversion (Conversion a + Conversion b + Conversion c)

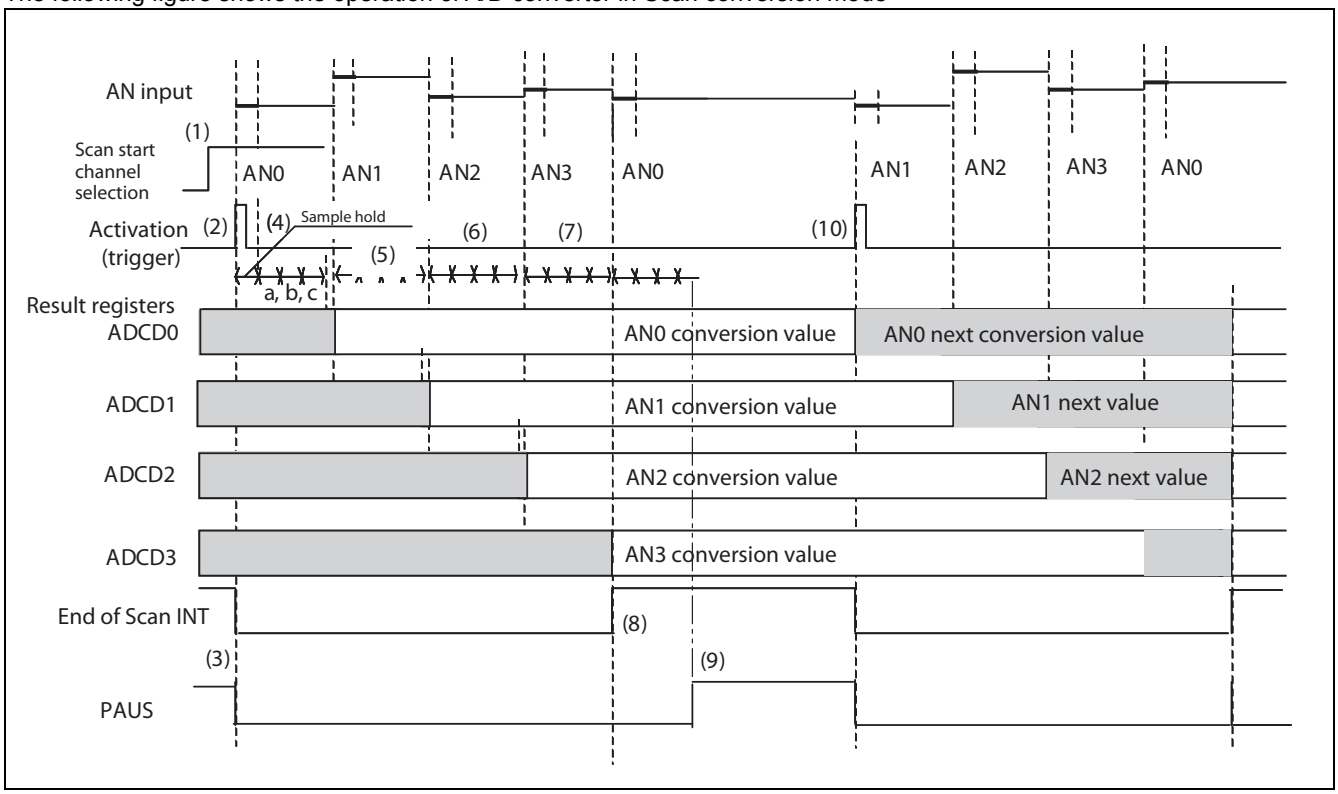
(6)Conversion end, INT flag set, BUSY flag clear

(7)Buffers the conversion value. Buffered data storage

(8)Software-based INT flag clear

8.6.5 Scan Conversion

The following figure shows the operation of A/D converter in Scan conversion mode



(1)Activation channel selection

(2)A/D activation (Trigger: Software trigger/Reload timer/External trigger)

(3)INT flag clear, PAUS flag clear

(4)AN0 conversion

a. Sample hold, conversion (conversion a + conversion b + conversion c)
b. Conversion end
c. Buffers the conversion value.

(5)AN1 conversion

(6)AN2 conversion

(7)AN3 conversion

(8)INT2 (End of Scan) flag is set, AN0 conversion starts

(9)Because INT2 has not been cleared yet, the ADC protects the result register of AN0 against overwriting and enters PAUSE state.

(10)INT2 flag cleared by DMA or by software, the ADC stores the result of AN0 and continues sampling AN1.

8.6.6 Protection of the ADC Channel Data Registers

There are 32 ADC result data registers, one register per channel. The registers are written by hardware at the end of conversion of the attached channel. ADCD0 is attached to channel 0, ADCD31 is attached to channel 31.

The CPU can read the data registers any time.

If a conversion is finished and the data of the previous conversion has not been read out before, previous data would be overwritten. To avoid this problem, the next conversion data is not stored in the data registers until the previous value has been read out (e.g. by DMA). A/D conversion halts during this time and the PAUS flag is set. A/D conversion restarts when the ADC interrupt flag ADCR1.INT is cleared.

The register protection function depends on the conversion mode and the setting of ADCR2.INTE2:

Mode	INTE2	Function
Single, Stop	X	Protection of ADCR
Continous	0	Protection of ADCR
	1	Protection of ADCD0...ADCD31

Protection of ADCD0...31

In continous mode with INTE2==1, PAUS is set when data of the **start channel (set by ADSCH)** is ready for writing to the registers, but IRQ2 (End of Scan interrupt) is already active.

Example: Start channel =4, end channel=7, continous mode, ADCS1.INTE=0, ADCS2.INTE2=1

Start by CPU --> convert channel 4 + safe data to ADCD4,
convert channel 5 + safe data to ADCD5,
convert channel 6 + safe data to ADCD6,
convert channel 7 + safe data to ADCD7 ---> End of Scan interrupt (IRQ2),
convert channel 4 + set PAUS (protect ADCD4...7).

After the CPU or DMA have read the data registers and cleared IRQ2, the scan conversion continues.

Protection of ADCR

In the other modes or if INTE2==0, PAUS is set when data of any channel is ready for writing to the registers, but IRQ (End of Conversion) is active. Because in this mode the protection function is active after each single conversion, the ADCR register is protected.

8.7 ADC Interrupt Generation and DMA Access

There are 2 ADC interrupt sources: End of Conversion and End of Scan.

8.7.1 End of Conversion

The End of Conversion (EoC) interrupt is enabled by ADCS1.INTE bit and is compatible to the A/D convertes in old devices of CY91460 series. If EoC is enabled, it appeares after any conversion cycle. It is recommended to use DMA transfer to read out the data from ADCR.

8.7.2 End of Scan

The End of Scan (EoS) interrupt is enabled by ADCS2.INTE2 bit. If EoS is enabled, it appeares after the conversion of the end channel, which is defined by the setting of ADECH register.

If the End of Conversion interrupt is enabled in parallel, both interrupt bits are set. In this case it is recommended that the interrupt routine reads out ADCS2 register (containing mirrored bits of ADCS1[7:4]) to check where the interrupt comes from.

8.7.3 DMA Transfer

DMA transfer can be triggered by End of Conversion interrupt or by End of Scan interrupt. The interrupts are assigned to separate DMA resource numbers (please refer to the Interrupt Vector Table).

The automatic interrupt clear after DMA transfer works for End of Conversion and for End of Scan separately.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

9. Hardware Watchdog (Extension)

This chapter describes a new feature of the Hardware Watchdog. For reference, please refer to chapter 21 Hardware Watchdog in the CY91460 series hardware manual.

9.1 Enabling the Hardware Watchdog in SLEEP and STOP State

The Hardware Watchdog can now be enabled in SLEEP and STOP state by software. On old devices, the watchdog is cleared in SLEEP and STOP and restarts counting at the transition to RUN mode.

Additionally, the restriction of CY91V460A about the settings ED1,ED0 = 01,10,11 has been removed.

9.1.1 HWWDE: Hardware watchdog timer duration register

The Hardware Watchdog Timer Duration register changes like following:

7	6	5	4	3	2	1	0	Bit
-	-	-	**STP_RUN**	-	-	ED1	ED0	
X	X	X	0	X	X	0	0	Initial value
RX, W0	RX, W0	RX, W0	R, W1	RX, W0	RX, W0	R, W	R, W	Attribute

■ Bit7-5: Reserved bits. Always write 0 to these bits.

■ Bit4: STP_RUN (Run in SLEEP/STOP mode):

- ❒ STP_RUN = 1 enables that the Hardware Watchdog continues running in SLEEP and STOP mode. The RC Oscillator will continue operation in SLEEP and STOP too.
- ❒ STP_RUN = 0 (default) the the Hardware Watchdog is cleared in SLEEP and STOP mode.
- ❒ STP_RUN can be set by CPU, but it cannot be cleared by the CPU
- ❒ STP_RUN is cleared by software reset (RST)

■ Bit3-2: Reserved bits. Always write 0 to these bits.

■ Bit1-0: ED (Elongate watchdog duration).]

ED1-0	Function
00	The watchdog period is 2^{16} CLKRC cycles [initial setting]
01	The watchdog period is 2^{17} CLKRC cycles
10	The watchdog period is 2^{18} CLKRC cycles
11	The watchdog period is 2^{19} CLKRC cycles

- ❒ These bits are cleared by software reset (RST) and can be written and read by CPU.

9.1.2 Caution

The section “Caution” changes as follows:

■ Software disabling is not possible.

The watchdog timer starts counting immediately after reset (release of INITX). Software cannot stop the counting.

■ Hardware disabling is only possible on the evaluation device CY91V460A **and CY91FV460B**.

The watchdog timer can be permanently disabled by setting the corresponding jumper of the evaluation board (this is not possible on flash devices with this watchdog timer). So always ensure correct configuration of the evaluation system to reflect the behaviour of the flash device.

■ Postponement of reset

In order to postpone the watchdog reset, the clearing of the watchdog timer is necessary. Whenever the CL bit of register is set to ‘0’ (there is no minimum writing limitation), the timer is cleared and the occurrence of reset is postponed. Just writing to the register without setting CL to ‘0’ does not clear the timer.

■ Timer stop and clear

In modes where the CPU does not work (SLEEP state, STOP state or STOP with RTC active state), the timer is cleared first then the counting is stopped. **If the bit HWWDE.STP_RUN is set, the counting continues, and the RC oscillator will continue too.**

■ During DMA transfer

During DMA transfer between D-bus modules, the writing e0f to CL bit is not possible. Thus, if the transfer timeis more than 328 ms (calculated from the fastest frequency of the RC oscillator as minimum period), a reset occurs.

■ Duration setting

Unlike on CY91V460 Rev.A it is possible to elongate the duration of the watchdog reset.

■ CLKRC frequency

Unlike on CY91V460 Rev.A it is possible to change the CLKRC frequency to 2 MHz. Even though the watchdog timer is always operated with a frequency of 100 kHz (10 µs) typical.

■ Difference between watchdog reset, external reset and Power-on reset

External reset pin (INITX), Clock Supervisor and Hardware Watchdog build a “reset chain”:

External reset pin / Power-On reset
- ❒ Clock Supervisor
- ❒ Hardware Watchdog
- ❒ Shutdown Controller [a]
- ❒ CPU

Each module in the chain transferes the incoming reset signal to its reset output.
External reset pin or Power-On will clear all the modules in the chain, but the Hardware Watchdog reset will not clear the Clock Supervisor.

a. Shutdown Controller is implemented on CY91F467E only.

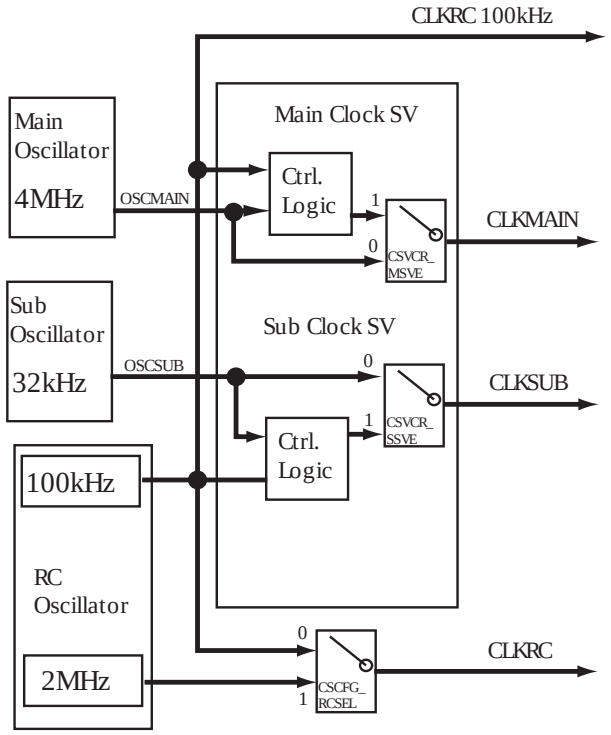
10. Clock Supervisor (New Feature)

This section gives an overview of the Clock Supervisor. Purpose of the Clock Supervisor is the supervision of the Main- and Sub oscillators. In case of oscillation (OSCMAIN or OSCSUB) failure the Clock Supervisor control logic will take action, i.e. switching to an internal RC-oscillation clock (CLKRC 100 kHz), depending on the operation mode set in the control register.

In CY91FV460B, CY91F467P and other new devices, an new Clock Supervisor version with extended functionality is implemented. This new feature is marked with the keyword "New feature".

10.1 Overview Clock Supervisor

Figure 10-1. Block diagram of the clock supervisor



The purpose of the clock supervisor is the supervision of the main and sub oscillation clocks. In case of a oscillation failure (OSCMAIN and/or OSCSUB) it can be replaced by an on-chip RC-oscillation clock (CLKRC 100 kHz), depending on the configuration.
If a clock the MCU currently uses, fails for a certain time (20-80 µs for *Main* clock / 160-640 µs for Sub clock) the MCU is reset by Setting Initialization Request (INIT) and the reset cause can be checked after reset vector fetch.
If the Sub clock is failing while the MCU is in Main clock mode, reset can be delayed until the transition to Sub clock mode or no reset will be initiated. The user can choose the behaviour with a control bit in the Clock Supervisor Control Register.
There are two independent supervisors, one for the Main clock and one for the Sub clock. They can be enabled/disabled separately. Main clock and Sub clock supervisor are disabled and re-enabled automatically if the corresponding oscillator is disabled and re-enabled.
If the MCU changes to STOP state, the RC-oscillator can be automatically disabled by a control bit. It will be enabled again upon wake-up from STOP state.
There are two status bits in the Clock Supervisor Control Register which indicate the failure of the Main clock and Sub clock. These bits can be available at two port pins (device dependent).
Single clock devices can use the CLKRC as Sub clock.

New feature: The two Clock Supervisor status bits can be cleared by CPU access, if the main and/or sub oscillator has resumed oscillation. The clock is switched back to OSCMAIN and/or OSCSUB in this case.

New feature: The RC oscillator is enabled in STOP mode automatically, if the Hardware Watchdog is configured to run during STOP. The RC oscillator can **only** be stopped in STOP mode, and then it depends on the Hardware Watchdog and the control bit in the Clock Supervisor Control Register.

10.2 Clock Supervisor Register

This section lists the Clock Supervisor Control Register and describes the function of each bit in detail.

10.2.1 Clock Supervisor Control Register (CSVCR)

The Clock Supervisor Control Register (CSVCR) sets the operation mode of the Clock Supervisor. Figure 10-2 shows the configuration of the Clock Supervisor Control Register.

Figure 10-2. Configuration Clock Supervisor Control Register (CSVCR)

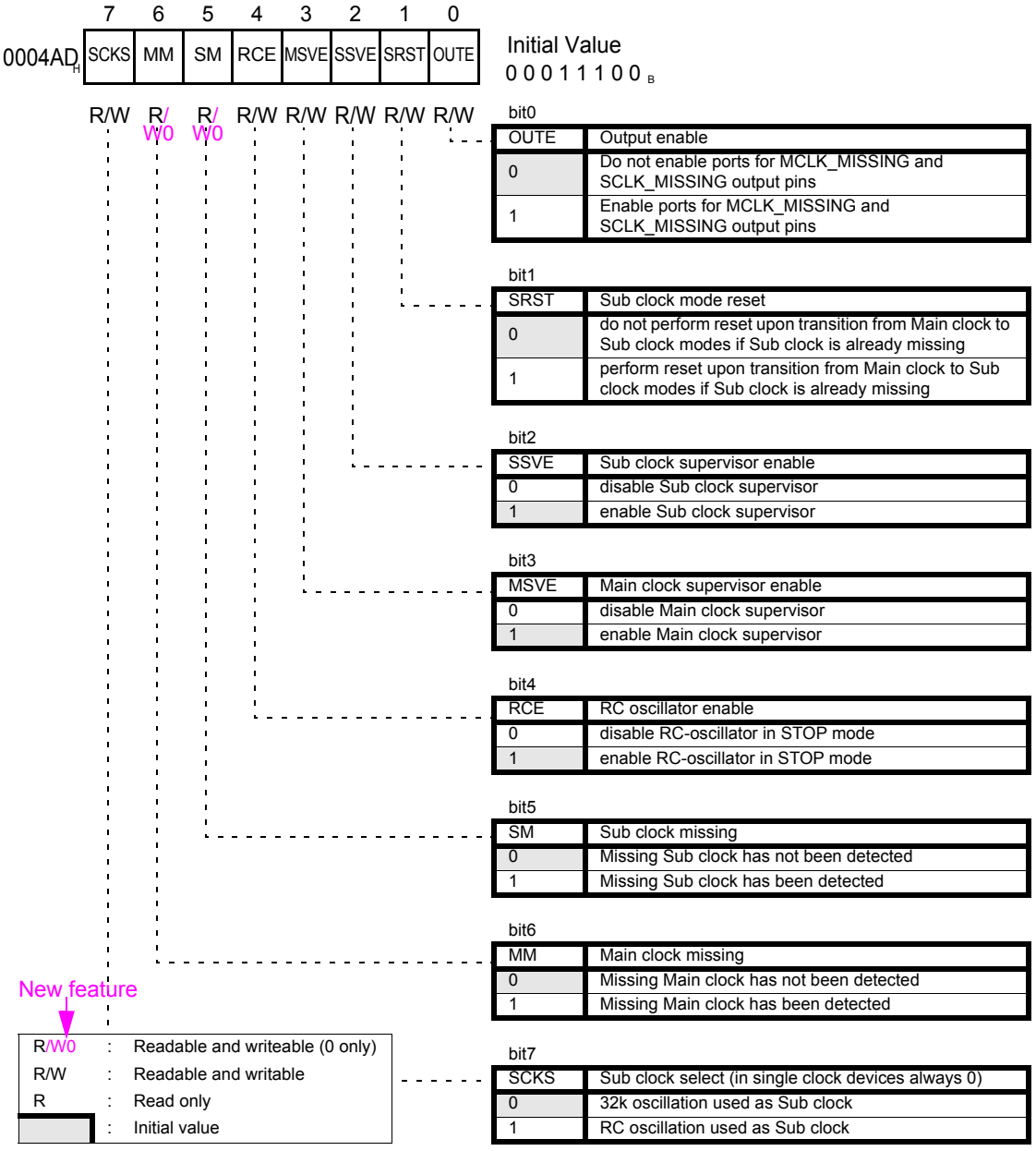


Table 10-1. describes the function of each bit of the Clock Supervisor Control Register (CSVCR).

Table 10-1. Functional Description of each bit of the Clock Supervisor Control Register

Bit	Name	Function
7	SCKS (Sub clock select)	This bit is to select between 32 kHz external oscillation and internal RC oscillation as Sub clock. If this bit is '0' then the external 32 kHz oscillation is used as Sub clock, if it's '1' then the internal RC oscillation is used as Sub clock. This bit is cleared to '0' by Power-On reset or external reset. Other types of reset will not affect this bit. Note: Don't change this bit while the CPU runs on Sub clock. First switch back to Main clock and then change SCKS!
6	MM (Main clock missing)	If this bit is 1, the Main clock supervisor has detected that the Main oscillation clock coming from X0, X1 is missing, e.g. by a broken crystal. If this bit is '0', a missing Main clock has not been detected. This bit is cleared to '0' by Power-On reset or external reset. Other types of reset will not affect this bit. New feature: This bit can be cleared by CPU access, if the main oscillator has resumed oscillation. If the main oscillator is still failing, the write access is ignored.
5	SM (Sub clock missing)	If this bit is 1, the Sub clock supervisor has detected that the sub oscillation clock coming from X0A, X1A is missing, e.g. by a broken crystal. If this bit is '0', a missing Sub clock has not been detected. This bit is cleared to '0' by Power-On reset or external reset. Other types of reset will not affect this bit. New feature: This bit can be cleared by CPU access, if the sub oscillator has resumed oscillation. If the sub oscillator is still failing, the write access is ignored.
4	RCE (RC-oscillator enable)	Setting this bit to '1' enables the RC-oscillator in STOP mode. Outside STOP mode, the RC-oscillator is always enabled. This bit is set to '1' by Power-On reset or external reset. Other types of reset will not affect this bit. New feature: If HWWDE.STP_RUN (=HWWDE[4]) is set in the Hardware Watchdog, then the RC oscillator is enabled and read and read-modify-write operations will return '1' independendly of RCE register setting. Effective RCE = RCE_Register or HWWDE.STP_RUN
3	MSVE (Main clock supervisor enable)	Setting this bit to '1' enables the Main clock supervisor. This bit is set to '1' by Power-On reset only. Other types of reset will not affect this bit.
2	SSVE (Sub clock supervisor enable)	Setting this bit to '1' enables the Sub clock supervisor. This bit is set to '1' by Power-On reset only. Other types of reset will not affect this bit.
1	SRST (Sub clock mode reset)	If this bit is set to '1', a reset is performed upon transition from Main/PLL clock mode to Sub clock mode if the Sub clock is already missing. If this bit is set to '0', no reset is performed in this case. This bit is cleared to '0' by Power-On reset or external reset. Other types of reset will not affect this bit.
0	OUTE (Output enable)	This bit can be used as an output enable to output the signals MCLK_MISSING (bit 3 of CSVCR) and SCLK_MISSING (bit 4 of CSVCR) to port pins. For more information about the pins see the corresponding Datasheet. If this bit is set to '1', the ports are enabled for MCLK_MISSING and SCLK_MISSING output. This bit is cleared to '0' by Power-On reset or external reset. Other types of reset will not affect this bit.

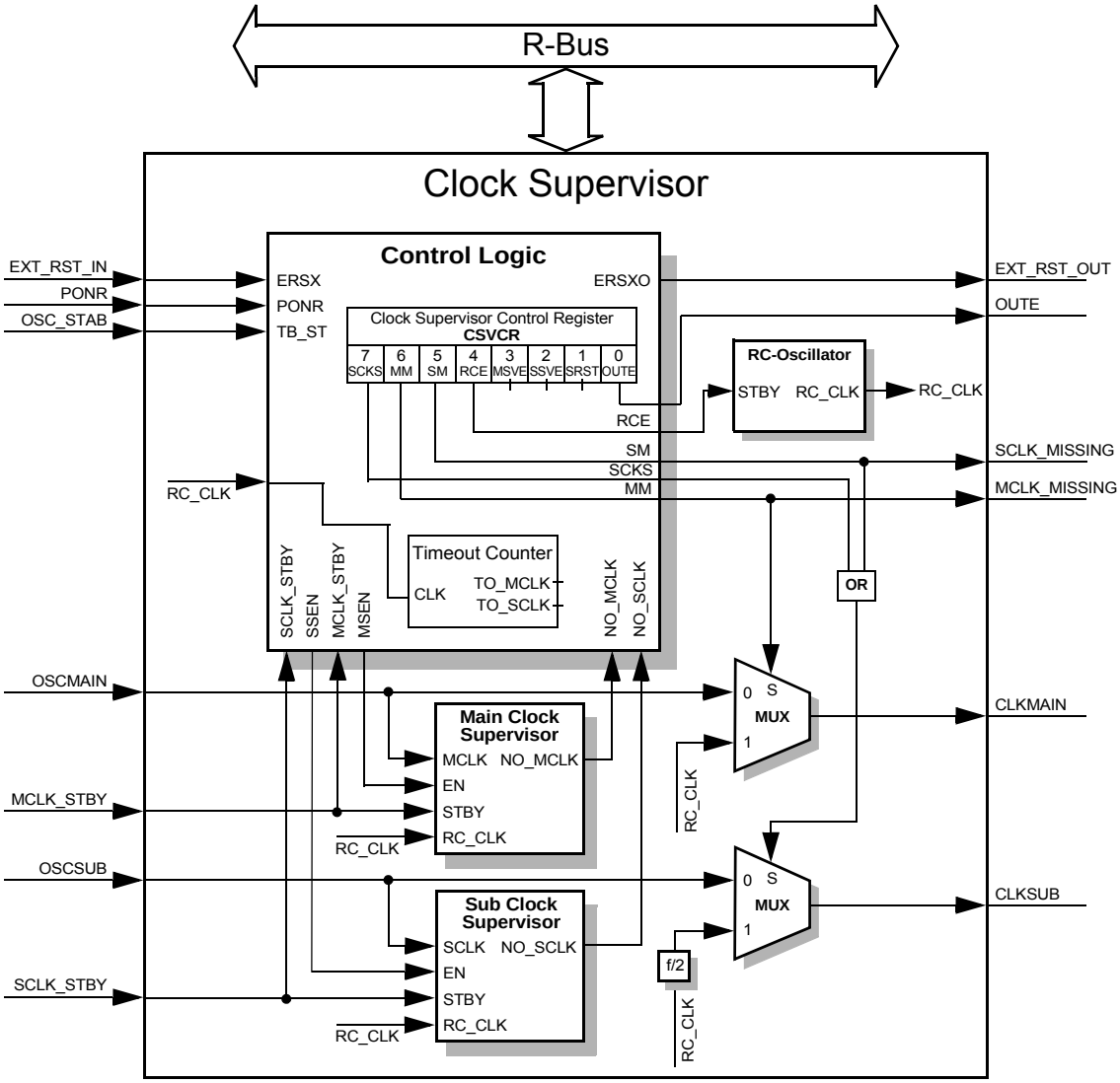
10.3 Block Diagram Clock Supervisor

This section presents a block diagram of the Clock Supervisor. The building blocks of the Clock Supervisor are:

- Main Clock Supervisor
- Sub Clock Supervisor
- Control Logic
- RC-Oscillator

10.3.1 Block Diagram Clock Supervisor

Figure 10-3. Bock Diagram of Clock Supervisor



SCLK_OUT and MCLK_OUT can be observed using the Clock Monitor Module. SCLK_MISSING and MCLK_MISSING can be programmed to device specific outputs (see the datasheet of the used device for the information which pins are used) by setting OUTE=1.

Signal EXT_RST_IN is the reset input, connected to the external INITX pin.
Signal EXT_RST_OUT is the reset output and causes Setting Initialization Request (INIT).

10.4 Operation Modes

This section describes all operation modes of the Clock Supervisor.

10.4.1 Operation mode with initial settings

In case the clock supervisor control register (CSVCR) is not configured at the beginning of the user program, the RC-oscillator, the Main clock supervisor and the Sub clock supervisor is enabled.

- The RC-oscillator is enabled at power-on.
- The Main clock supervisor is enabled after the 'oscillation stabilization wait time' or in case the Main clock is missing before the completion of the 'oscillation stabilization wait time', after the 'Main clock timeout' (TO_MCLK) from the timeout counter. The timeout counter is clocked with CLKRC. If the Main clock is missing from power-on, the power-on reset state is never left, which in this case is a safe state. The user must make sure with external pull-up/pull-down resistors that all relevant signal are pulled to the correct level.
- The Sub clock supervisor is enabled after the completion of the 'Sub clock timeout' (TO_SCLK) from the timeout counter. The timeout counter is clocked with CLKRC.
- If the Main clock stops while the Main clock supervisor is enabled, the Main clock is replaced with CLKRC 100 kHz, the MM bit is set to '1' and reset (EXT_RST_OUT) is asserted.
- If the Sub clock stops and the Sub clock supervisor is enabled, the behaviour depend on whether the MCU is in Main clock mode or in Sub clock mode. If the Sub clock stops in Sub clock mode, CLKRC divided by two substitutes the Sub clock, the SM bit is set to '1' and reset (EXT_RST_OUT) is asserted. If the Sub clock stops in Main clock mode, CLKRC divided by two substitutes the Sub clock, the SM bit is set to '1' and no reset occurs upon transition to Sub clock mode, since the SRST bit has its initial value of '0'. If the SRST bit is '1' a reset (INIT) occurs.

Figure 10-4. Timing Diagram: Initial settings, Main clock missing during power-on reset

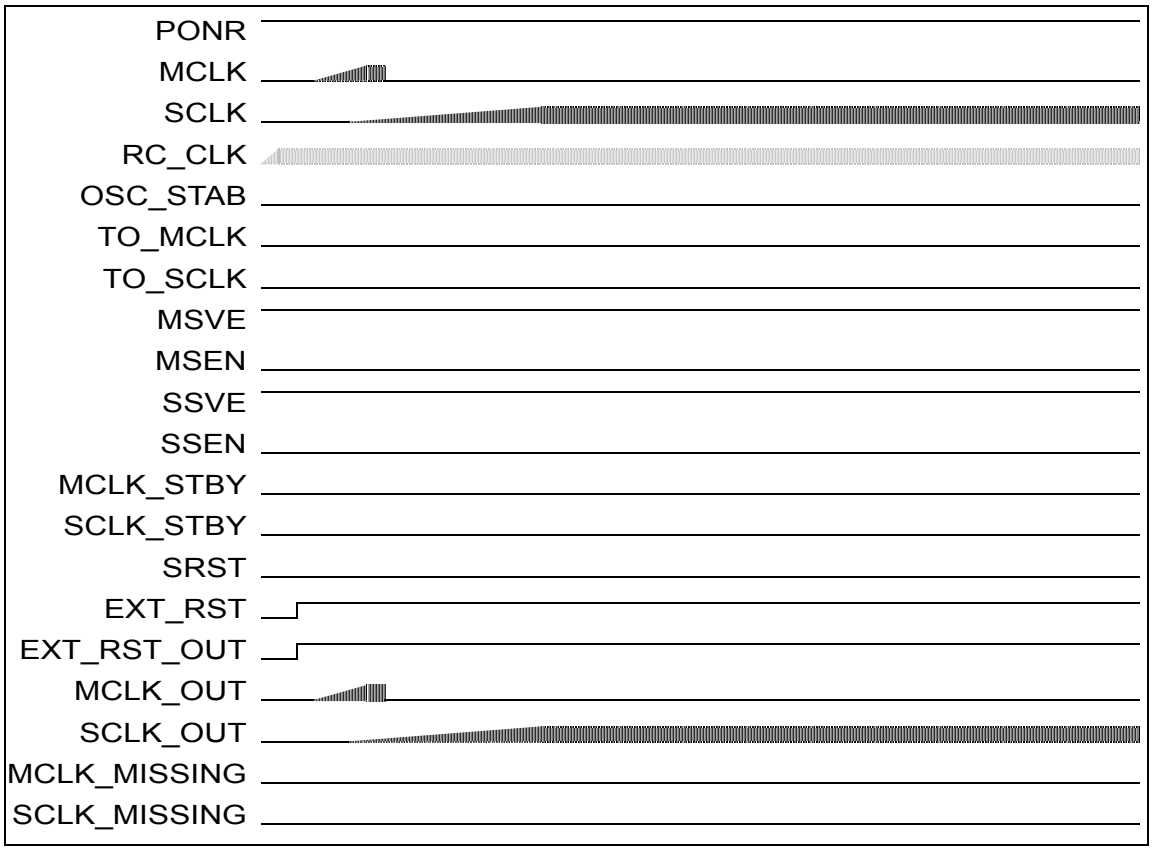


Figure 10-5. Timing Diagram: Initial settings, Main clock missing during 'oscillation stabilization wait time'

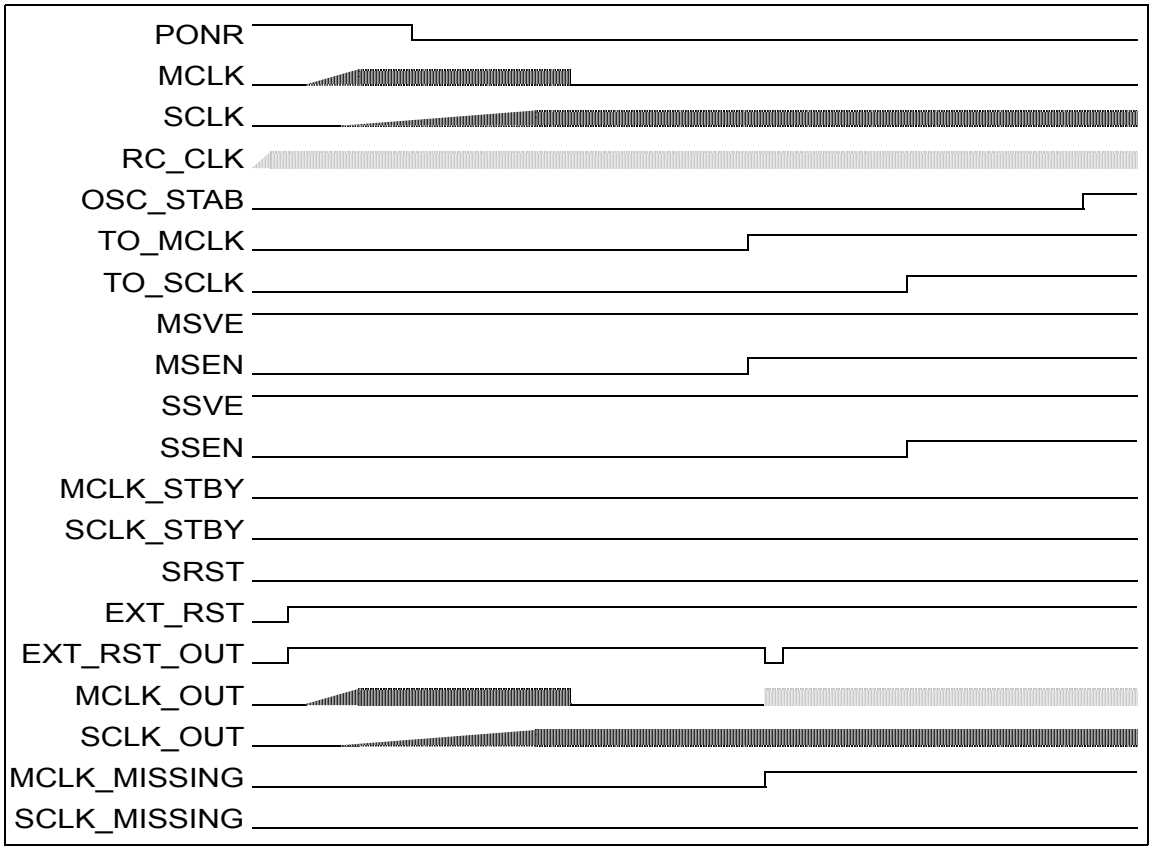


Figure 10-6. Timing Diagram: Initial settings, Main clock missing after 'oscillation stabilization wait time'

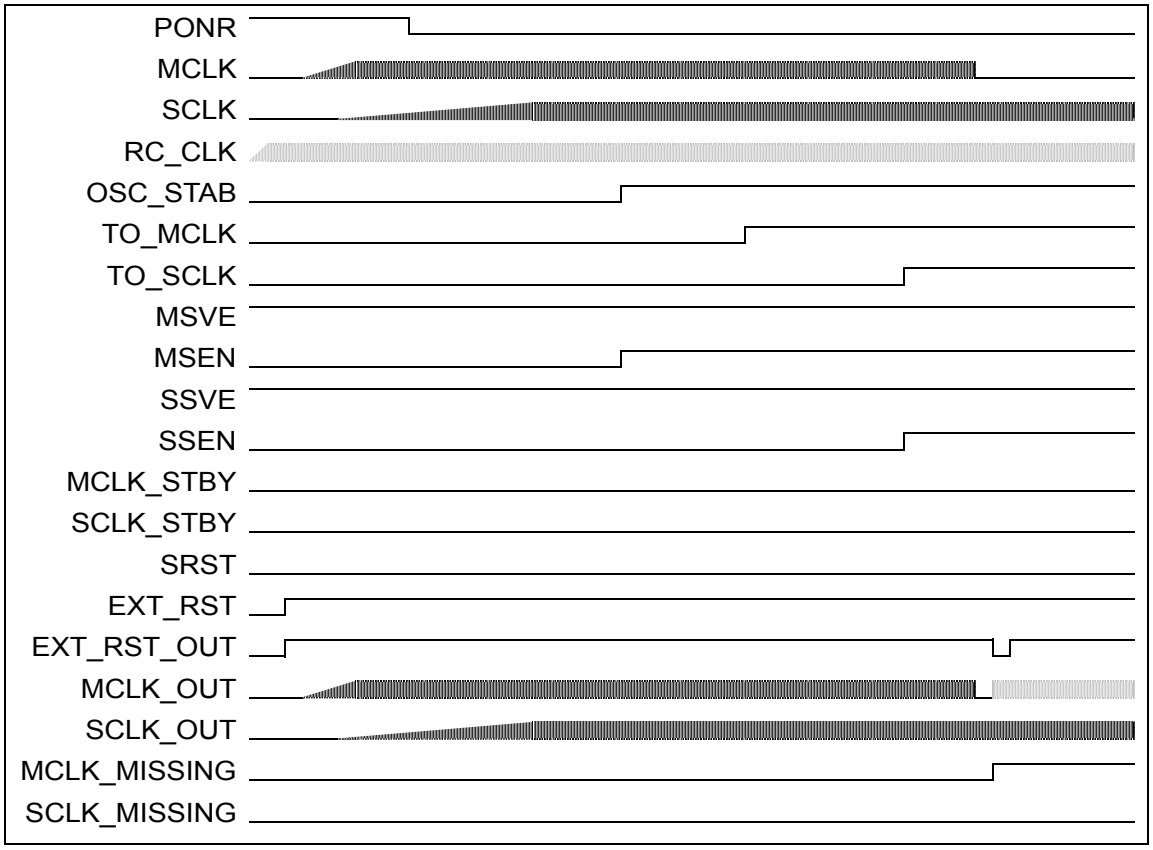


Figure 10-7. Timing Diagram: Initial settings, Sub clock missing before timeout

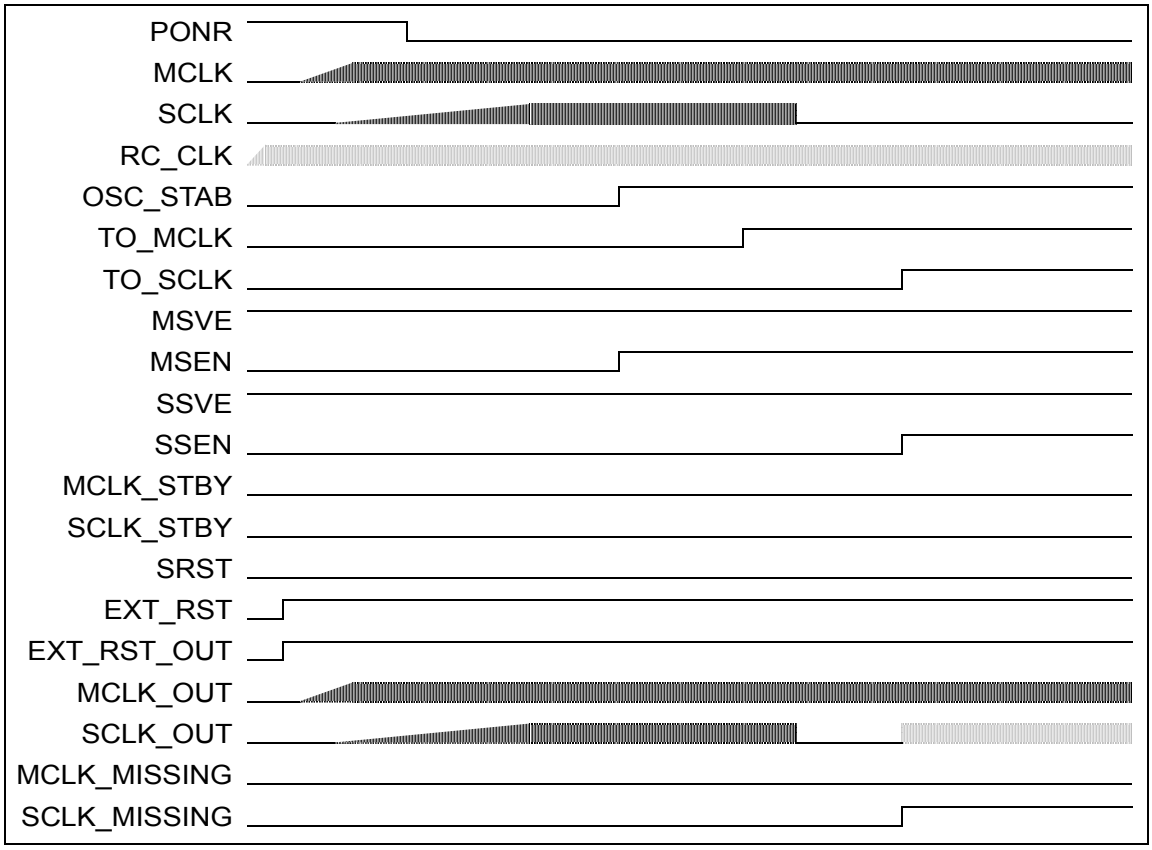
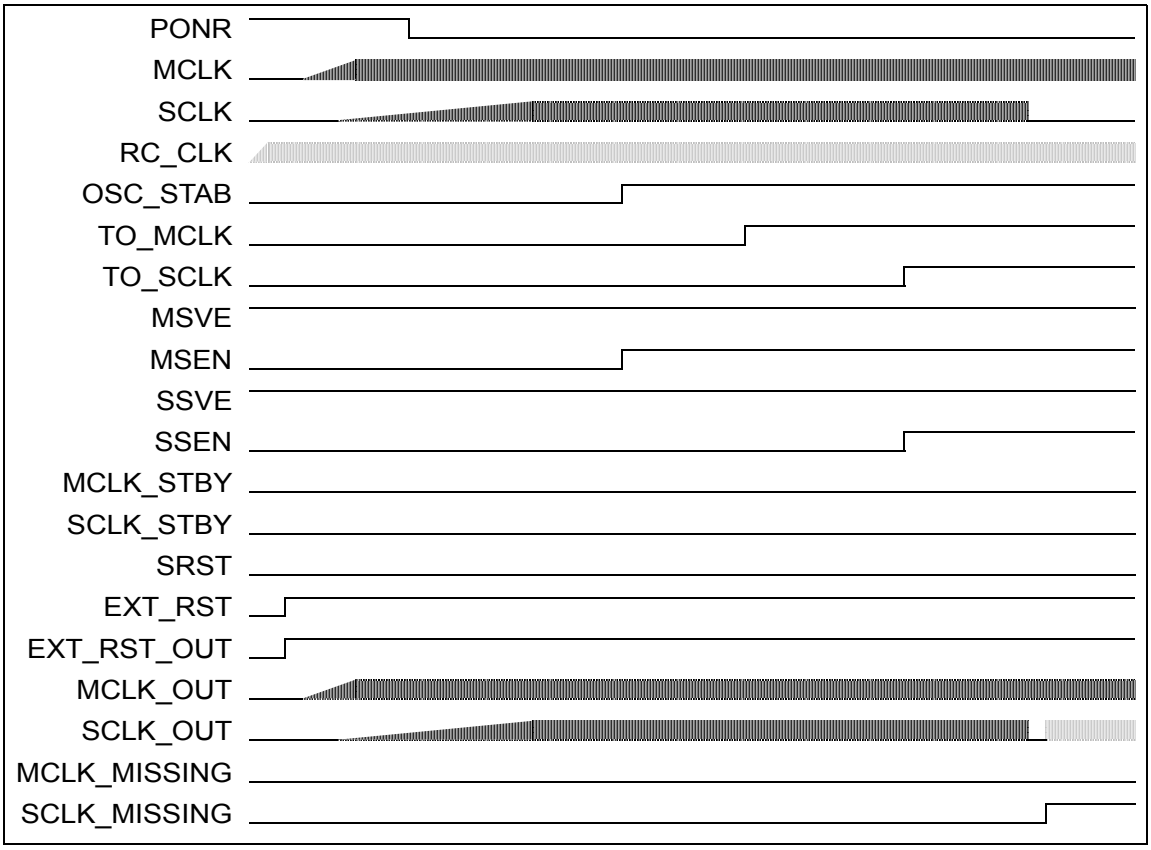


Figure 10-8. Timing Diagram: Initial settings, Sub clock missing after timeout



10.4.2 Disabling the RC-oscillator and the clock supervisors

The initial point of this scenario is that the RC-oscillator and Main clock or Sub clock supervisor is enabled.

- The RC-oscillator can be disabled only in STOP mode.

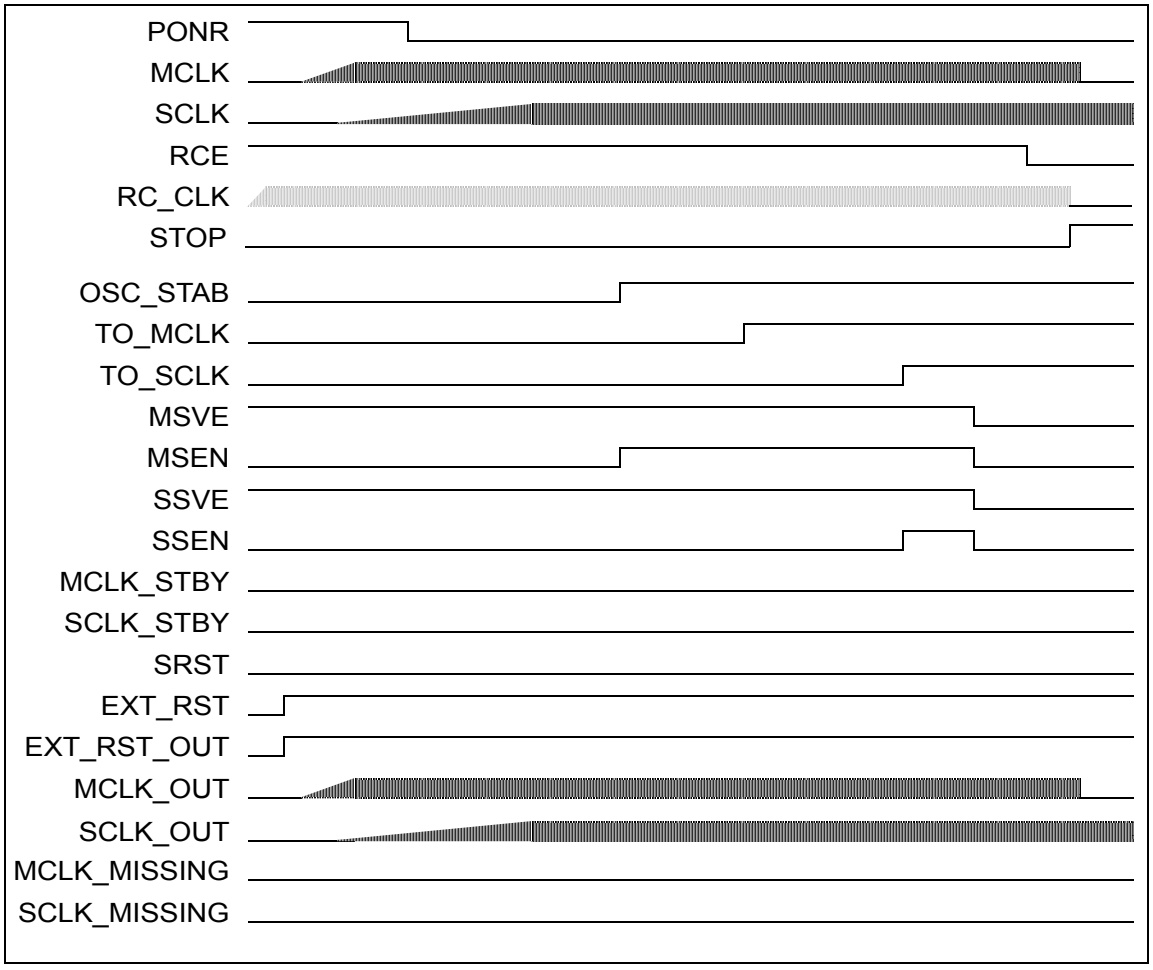
  First check that both SM and MM (bit 5 and bit 6 of CSVCR) are ’0’.
  Then disable the RC-oscillator by setting RCE to ’0’. If either SM or MM bit is ’1’, RCE must not be set to ’0’.

- New feature: If the Hardware Watchdog is to run in STOP mode (HWWDE.STP_RUN=’1’) then the RC-oscillator is enabled by hardware.

- The Main clock supervisor is disabled by setting MSVE (bit 3 of CSVCR) to ’0’.

- The Sub clock supervisor is disabled by setting SSVE (bit 2 of CVSVR) to ’0’.

Figure 10-9. Timing Diagram: Disabling the RC-oscillator and the clock supervisors

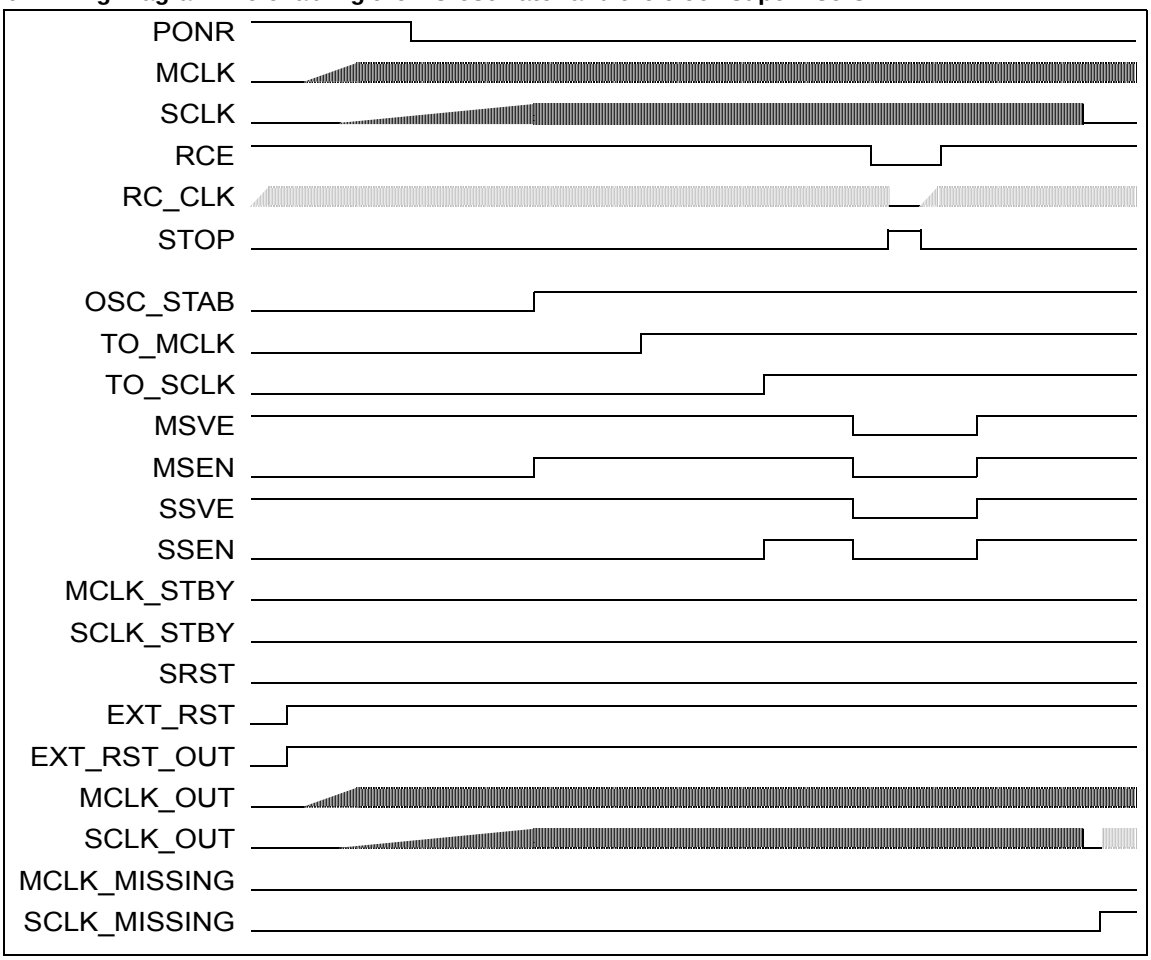


10.4.3 Re-enabling the RC-oscillator and the clock supervisors

The initial point of this scenario is that the RC-oscillator and both Main clock and Sub clock supervisor are disabled.

- The RC-oscillator is always enabled in RUN state. It can only be disabled in STOP, and after wakeup from STOP it will re-start automatically.
- The Main clock supervisor is enabled by setting MSVE (bit 3 of CSVCR) to ’1’.
- The Sub clock supervisor is enabled by setting SSVE (bit 2 of CSVCR) to ’1’.

Figure 10-10. Timing Diagram: Re-enabling the RC-oscillator and the clock supervisors



10.4.4 New feature: Switching back from RC to Main Oscillation

The initial point of this scenario is that the Main clock was missing, the Main clock supervisor has set the MM flag and switched to RC clock. The CPU already got reset (INIT) from clock supervisor and has detected MM=1 as reset source (See "Check if reset was asserted by the Clock Supervisor" on P. 65). The user is quite sure that the Main clock returned meanwhile or will return soon and wants to switch back to Main clock.

- The MM flag can be cleared by writing ‘0’ (bit 6 of CSVCR).
- If the Main clock is still missing during the write access, the write operation has no effect, the MM flag keeps ‘1’ value and the clock supervisor continues giving out RC clock.
- If the Main clock is operating during the write access, the MM flag is cleared and the clock is switched back to Main clock.
- It is possible to poll the MM flag until the Main clock is resumed:

```
            ldi             #_csvcr,r1
clear_CSV_loop:
            bandh           #0b1001,@r1 ;; Clear MM+SM
            btsth           #0b0110,@r1;; Check: Is one of them 1?
            bne             clear_CSV_loop
```

10.4.5 New feature: Switching back from RC to Sub Oscillation

The initial point of this scenario is that the CPU is running on Sub clock and Sub clock was missing. The Sub clock supervisor has set the SM flag and switched to RC clock (divided by 2). A clock supervisor reset was not generated because of CSVCR.SRST was ‘0’. Now the CPU is running user software on RC clock. The flag SM=1 was found by polling. The user is quite sure that the Sub oscillation returned meanwhile or will return soon and wants to switch back to Sub oscillation.

- The SM flag can be cleared by writing ‘0’ (bit 5 of CSVCR).
- If the Sub clock is still missing during the write access, the write operation has no effect, the SM flag keeps ‘1’ value and the clock supervisor continues giving out RC clock.
- If the Sub clock is operating during the write access, the SM flag is cleared and the clock is switched back to Sub clock.
- It is possible to poll the SM flag like described in the Main clock example above.

10.4.6 Sub clock modes

The Main clock supervisor is automatically disabled in Sub clock modes. The enable bit MSVE remains unchanged. At transition from Sub clock mode to Main clock mode the Main clock supervisor is enabled after the ’oscillation stabilization wait time’ or in case the Main clock is missing before the completion of the ’oscillation stabilization wait time’, after the ’Main clock timeout’ (TO_MCLK) from the timeout counter. The timeout counter is clocked with CLKRC.

10.4.7 Changing the behaviour upon transition to Sub clock mode if the Sub clock has already stopped in Main clock mode

If the Sub clock has stopped in Main clock mode and this was detected by the Sub clock supervisor, the behaviour upon transition to Sub clock mode depends on the state of the SRST bit.

- If SRST is set to ’0’ (initial value), reset is not asserted at the transition to Sub clock mode. The transition is performed using the RC-oscillation clock as Sub clock. In this case it is recommended to check the SM bit before the transition to Sub clock mode to get the information if Sub clock or CLKRC is used.
- If SRST is set to ’1’, reset is asserted at the transition to Sub clock mode.

The following timing diagrams (Figure 10-11, Figure 10-12, Figure 10-13) illustrate this behaviour.

Figure 10-11. Timing Diagram: Sub clock missing in Main clock mode, SRST=0

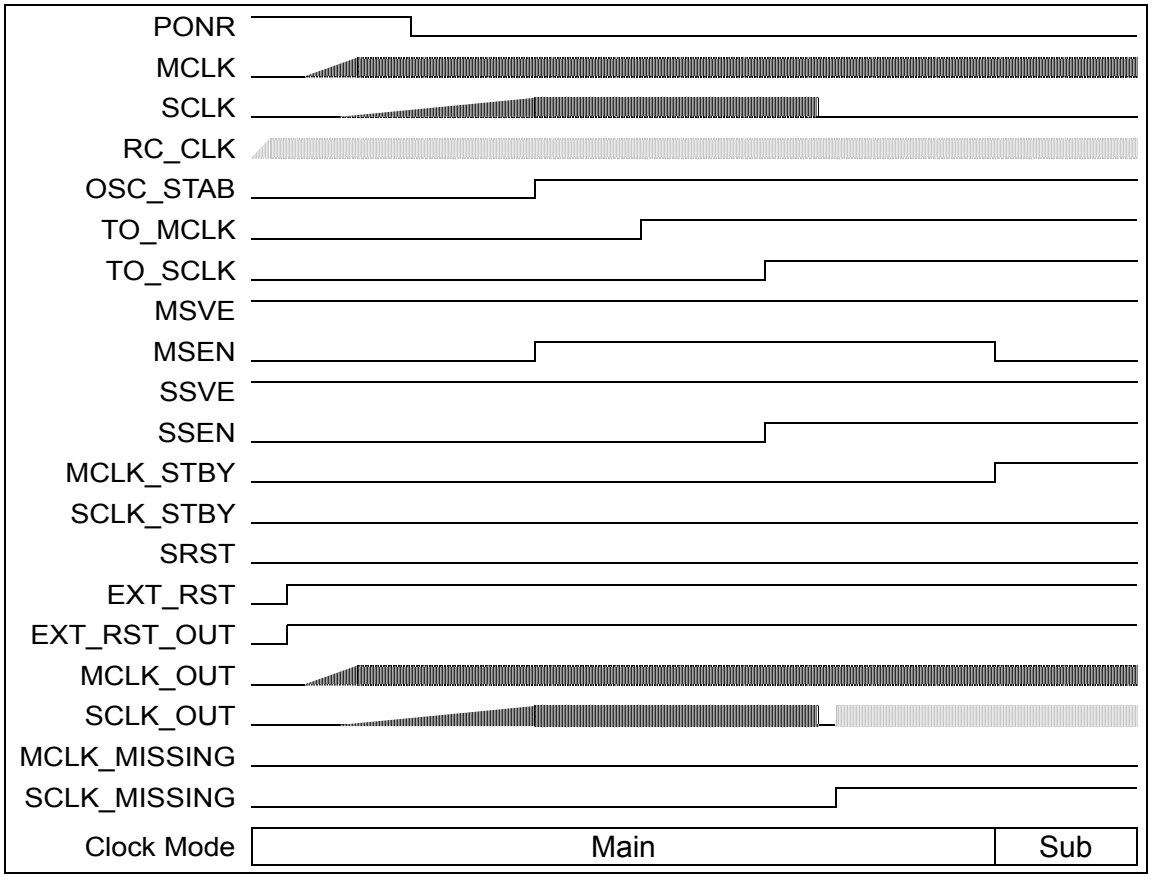


Figure 10-12. Timing Diagram: Sub clock missing in Main clock mode, SRST=1

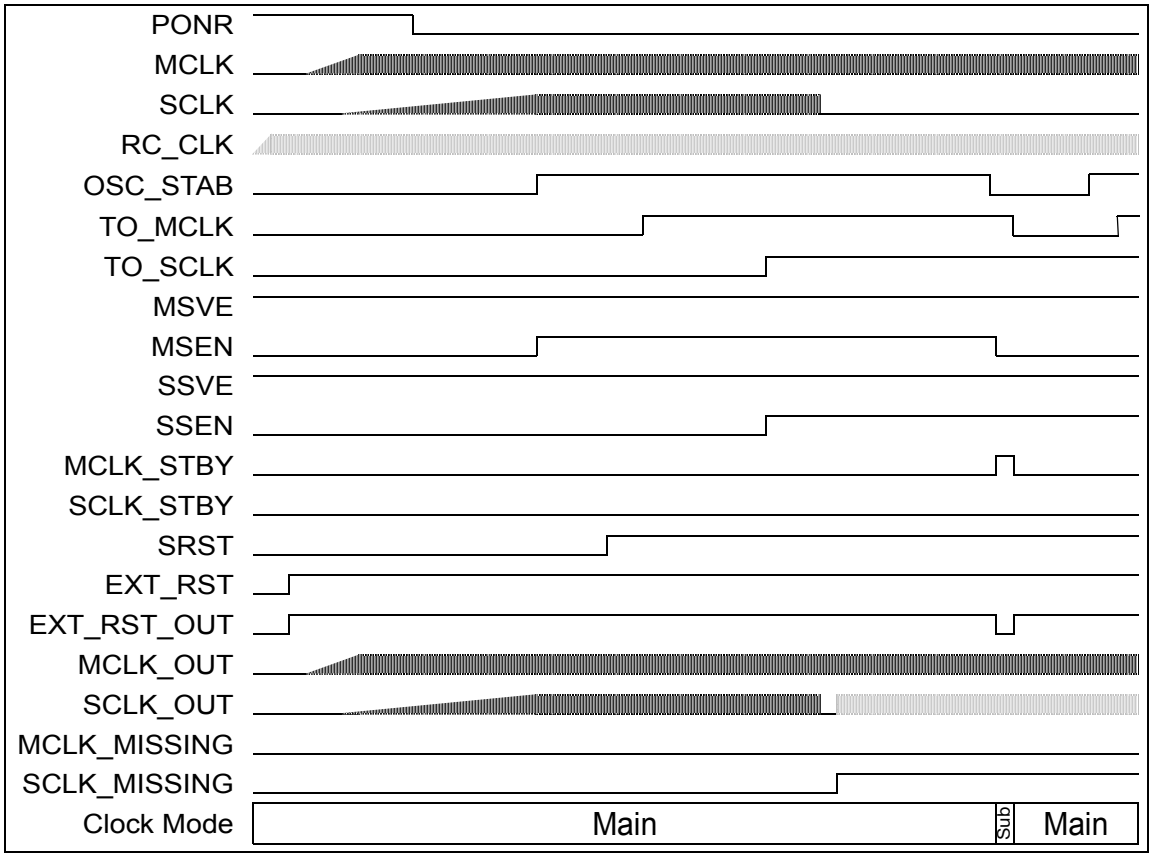
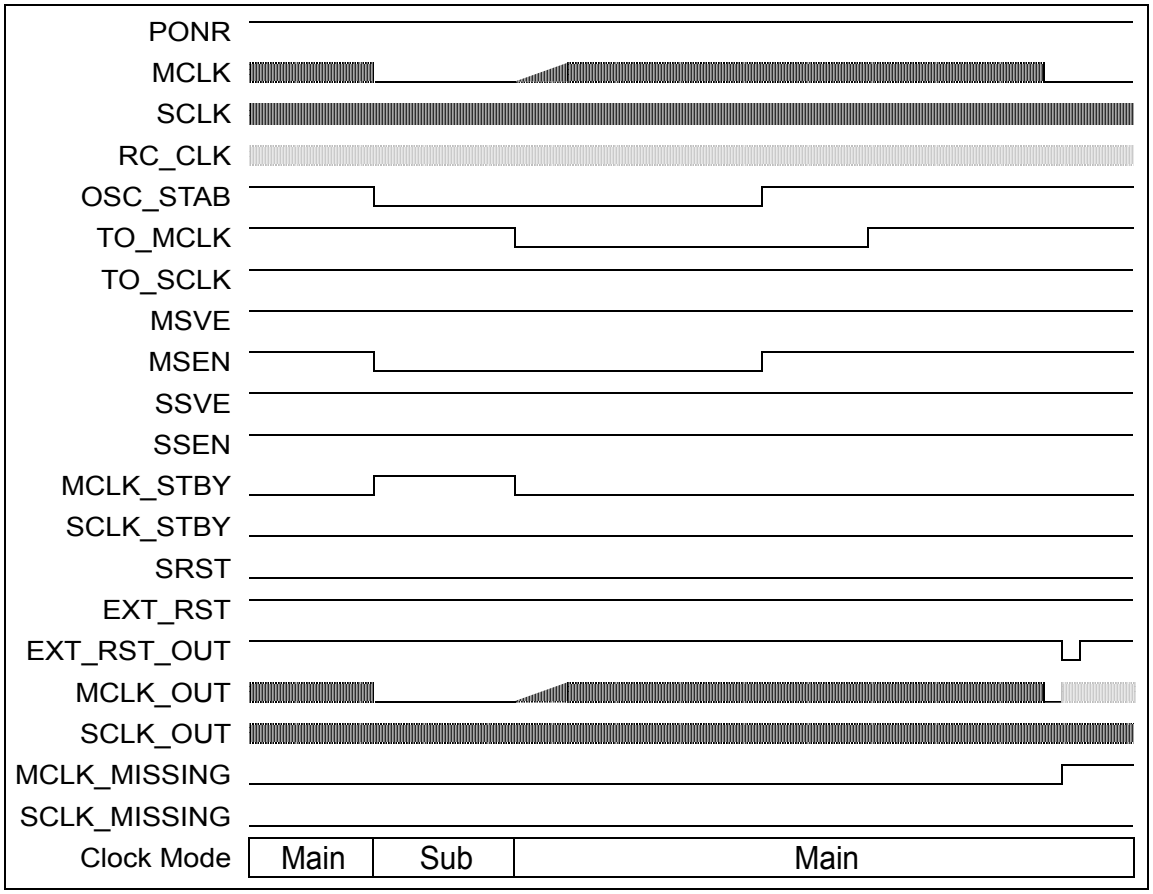


Figure 10-13. Timing Diagram: Waking up from Sub clock mode



10.4.8 STOP mode (with both oscillators disabled)

In this section, “STOP mode” means that the CPU is in STOP state and both oscillators are disabled by setting STCR.OSCD1=’1’ and STCR.OSCD2=’1’. The Clock Supervisor’s inputs MCLK_SBY and SCLK_SBY are connected to the oscillator disable lines OCSD1 and OSCD2, respectively.

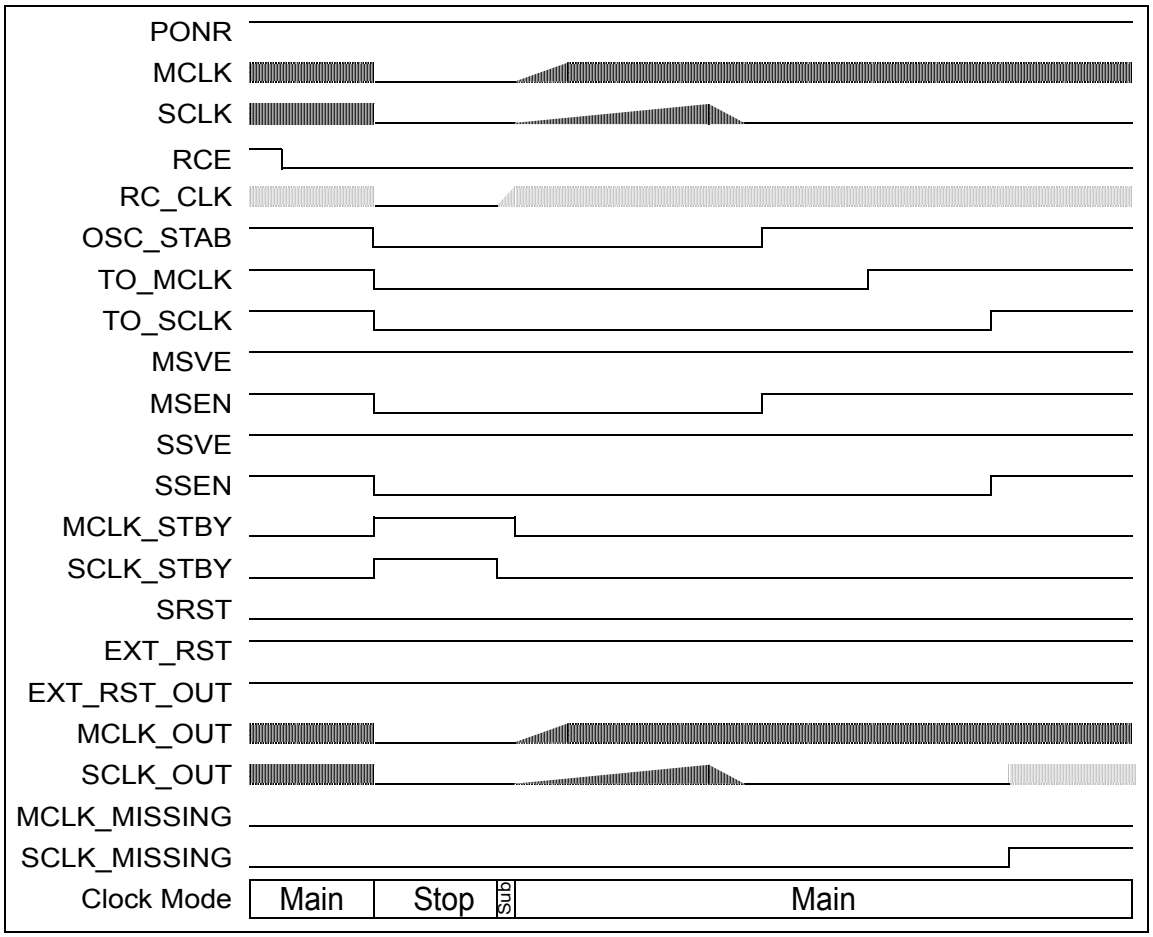
If Main clock and Sub clock supervisors are enabled, they will be automatically disabled at transition into STOP state. The corresponding enable bits in the clock supervisor control register remain unchanged. So after wake-up from STOP mode the clock supervisors will be enabled again. If the corresponding enable bits are set to ’0’, the clock supervisors will stay disabled after wake-up from STOP mode.

The RC-oscillator is disabled in STOP, if the RCE bit in the CSVCR register is cleared.

New feature: If the Hardware Watchdog is enabled in STOP state (HWWDE.STP_RUN=’1’), then the RC-oscillator is enabled by hardware during STOP. The RCE bit is unchanged, but read and read-modify-write operations return ‘1’.

- The RC-oscillator is enabled immediately after wake-up from STOP mode.
- The Main clock supervisor is enabled after the ’oscillation stabilization wait time’ or in case the Main clock is missing after wake-up from STOP mode, after the ’Main clock timeout’ (TO_MCLK) from the timeout counter. The timeout counter is clocked with CLKRC.
- The Sub clock supervisor is enabled after the ’Sub clock timeout’ (TO_SCLK) from the timeout counter which is clocked with the CLKRC.

Figure 10-14. Timing Diagram: Waking up from STOP state



10.4.9 RTC mode (STOP mode with Real Time Clock enabled)

In this section, “RTC mode” means that the CPU is in STOP state and one of the quartz oscillators is enabled by setting STCR.OSCD1=’0’ or STCR.OSCD2=’0’. The enabled oscillator clock is switched to the Real Time Clock to keep it running during STOP. The behavoiur of the Clock Supervisor depends on several settings.

■ If the RTC is connected to Main clock, the behaviour of the main clock supervisor is like described in Table 10-2.

Table 10-2. Main Clock Supervisor in RTC mode.

RC oscillator enable CSVCR.RCE	Main Oscillator disable STCR.OSCD1	Main clock supervisor enable SVCR.MSVE	Behaviour in STOP mode if Main clock fails and the RTC is connected to Main clock
1	1	X	Main clock fail cannot be seen because the Main oscillator is disabled. The Main clock supervisor is disabled because of the Main oscillator is disabled. The RTC will not run because of the same reason. Note: This is no RTC mode.
1	0	1	The clock supervisor will set MM flag, switch the Main clock to RC clock and generate an reset (INIT) to CPU. The STOP mode is cancelled by the reset. The RTC is initialized by the reset.
1	0	0	Main clock supervisor is disabled by MSVE=0. In case of Main clock fail, the RTC clock simply stopps.
0	X	X	Main clock supervisor is disabled because of it does not get RC clock. In case of Main clock fail, the RTC clock simply stopps.

Note New feature: RCE setting is valid if HWWDE.STP_RUN (HWWDE[4]) is ‘0’. Otherwise, RCE is overwritten to ‘1’.

■ If the RTC is connected to Sub clock, the behaviour of the sub clock supervisor is like described in Table 10-3.

Table 10-3. Sub Clock Supervisor in RTC mode.

RC oscillator enable CSVCR.RCE	Sub Oscillator disable STCR.OSCD2	Sub clock supervisor enable SVCR.SSVE	Behaviour in STOP mode if Sub clock fails and the RTC is connected to Sub clock
1	1	X	Sub clock fail cannot be seen because the Sub oscillator is disabled. The Sub clock supervisor is disabled because of the Sub oscillator is disabled. The RTC will not run because of the same reason. Note: This is no RTC mode.
1	0	1	The clock supervisor will set SM flag and switch the Sub clock to RC clock.The RTC continues running on RC clock. A reset is not generated because there is no transition from Main clock to Sub clock during STOP mode.
1	0	0	Sub clock supervisor is disabled by SSVE=0. In case of Sub clock fail, the RTC clock simply stopps.
0	X	X	Sub clock supervisor is disabled because of it does not get RC clock. In case of Sub clock fail, the RTC clock simply stopps.

Note New feature: RCE setting is valid if HWWDE.STP_RUN (HWWDE[4]) is ‘0’. Otherwise, RCE is overwritten to ‘1’.

■ The RC-oscillator is enabled immediately after wake-up from STOP state.

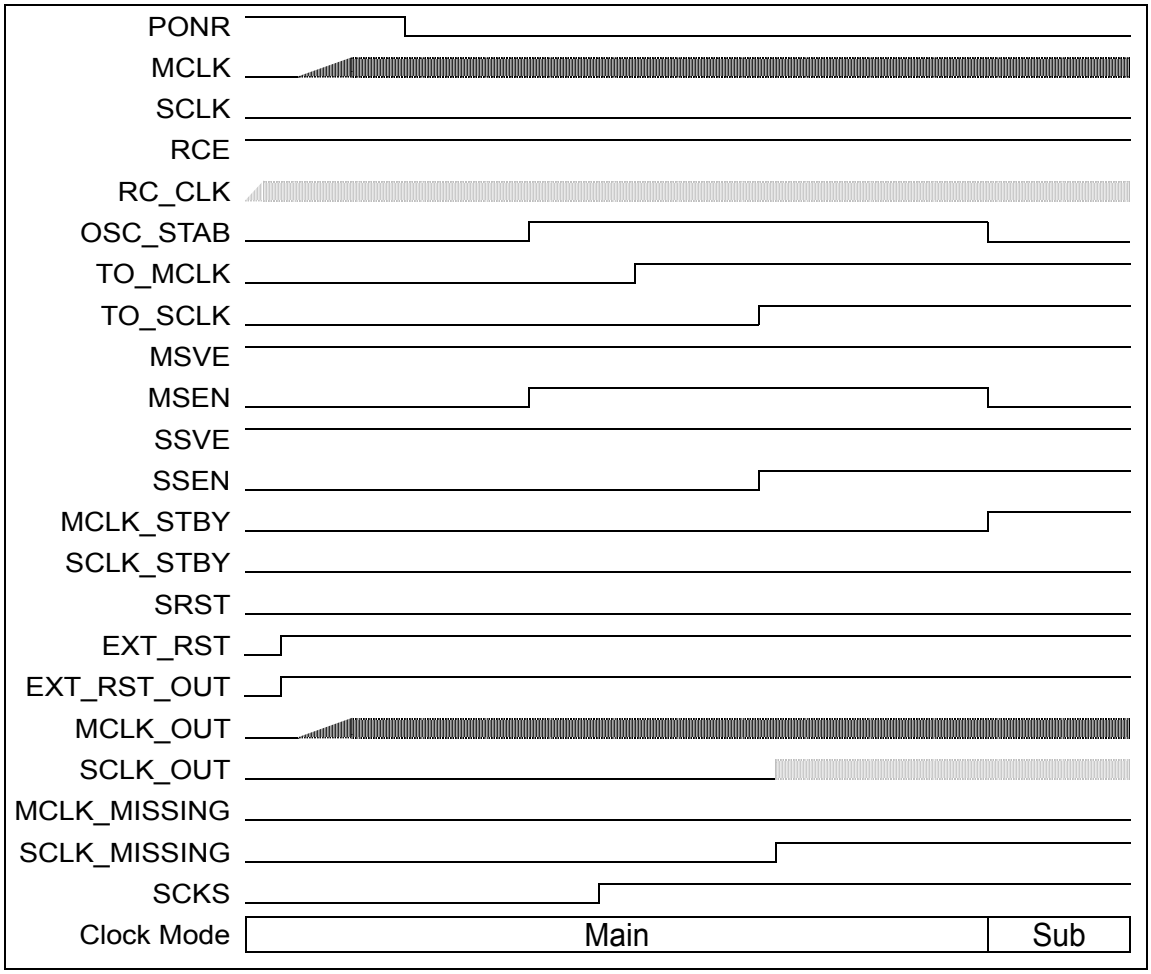
■ If the Main clock was disabled in STOP: The Main clock supervisor is enabled after the ’oscillation stabilization wait time’ or in case the Main clock is missing after wake-up from STOP state, after the ’Main clock timeout’ (TO_MCLK) from the timeout counter. The timeout counter is clocked with CLKRC.

■ IF the Sub clock was disabled in STOP: The Sub clock supervisor is enabled after the ’Sub clock timeout’ (TO_SCLK) from the timeout counter which is clocked with the CLKRC.

10.4.10 RC-Clock as Sub Clock

The Sub clock supervisor can provide the CLKRC as Sub clock. To enable this feature, SCKS bit (bit7 of CSVCR) must be set to ’1’.

Figure 10-15. Timing Diagram: Sub clock mode with single clock device



10.4.11 Check if reset was asserted by the Clock Supervisor

To find out whether the Clock Supervisor has asserted reset, the software must check the reset cause by reading the RSRR register (see the hardware manual "RSRR: Reset Cause Register" on P. 229). On the most flash devices, the RSRR register is read and cleared by the Boot ROM software. The content of RSRR can be found in CPU register R4[7:0] after Boot ROM is done.
If INIT (bit 7 of RSRR) is set, the cause was either external reset at the INITX pin or the clock supervisor or the hardware watchdog (HWWD). If neither SM bit nor MM bit (bit 5 and bit 6 of CSVCR) is set, reset cause was the external reset or the hardware watchdog. If SM is ’1’ the reset cause is a missing Sub clock and if MM is ’1’ the reset cause is a missing Main clock.

10.5 Cautions

After a Clock Supervisor reset, the CLKPLL is not usable as clk source, if the clock supervisor reset was caused by a missing OSCMAIN.

11. USART LIN/FIFO (Extension)

This chapter describes an extension of the USART (LIN/FIFO USART).
For reference, please refer to chapter 32 USART (LIN/FIFO) in the CY91460 series hardware manual.

11.1 USART End of Transmission Interrupt (ET)

The USART macros have been extended to generate an “End of Transmission” (ET) interrupt after the last bit of a transmission has been sent. If ET is enabled and there is no FIFO installed, the interrupt is generated after each transmission. If FIFO is installed, ET appeares after the transmission while the FIFO is empty.

The ET interrupt cannot request a DMA transfer.

The ET can be enabled and observed in the FSR (FIFO Status Register). Therefore, also USART modules which are not equipped with FIFO, have the FIFO Status Register.

11.1.1 USART Interrupts

With the ET interrupt, the list of USART interrupts extends to:

Reception/ transmission/ ICU	Interrupt request flag	Flag Register	Operation mode				Interrupt cause	Interrupt cause enable bit	How to clear the Interrupt Request
			0	1	2	3			
Reception	RDRF	SSR	x	x	x	x	receive data is written to RDR (FIFO level reached)	SSR:RIE	Receive data is read
	ORE	SSR	x	x	x	x	Overrun error		"1" is written to clear rec. error bit (SCR: CRE)
	FRE	SSR	x	x	[1]	x	Framing error		
	PE	SSR	x		[2]		Parity error		
	LBD	ESCR	x			x	LIN synch break detected	ESCR: LBIE	"0" is written to ESCR:LBD
	TBI & RBI	ESCR	x	x		x	no bus activity	ECCR:BIE	Receive data / Send data
Transmission	TDRE	SSR or FSR [3]	x	x	x	x	Empty transmission register	SSR:TIE	Transfer data is written
	ET	**FSR**	x	x	x	x	End of transmission [and FIFO empty [4]]	FSR:ETIE	"0" is written to FSR:ETINT
Input Capture Unit	ICP4	IPCP	x			x	1st falling edge of LIN synch field	IPCP:ICE	disable ICE temporary
	ICP4	IPCP	x			x	5th falling edge of LIN synch field	IPCP:ICE	disable ICE

1. Only available if ECCR04/SSM = 1
2. Only available if ECCR04/SSM = 1
3. FSR:TDRE is a read-only mirror of the SSR:TDRE bit
4. if FIFO is installed

X: Used

11.1.2 FSR: FIFO Status register for ET interrupt control

The FSR register ontrols and observes the ET interrupt and displays FIFO status (if FIFO is installed).

15	14	13	12	11	10	9	8	Bit
TDRE	**ETINT**	**ETIE**	**NVFD (Number of valid FIFO data)**					
X	X	0	0	0	0	0	0	Initial value
R	R,W0	R,W	R	R	R	R	R	Attribute

■ bit15: TDRE Transmission Data Register Empty flag (shadow)
- ❒ This is a read-only shadow of TDRE flag. Interrupt routines can determine the interrupt source (TDRE or ET) by just reading the FSR register.

■ bit 14: ETINT End of Transmission interrupt flag
- ❒ This flag is set when the ET condition has appeared:
  If no FIFO is installed, after the last bit of a transmission has been sent,
  if FIFO is installed, after the last bit of a transmission has been sent and the FIFO is empty.
- ❒ This flag is cleared by software reset (RST) or by writing 0.
- ❒ Writing 1 has no effect.
- ❒ Read - modify - write access always reads 1.

■ bit13: ETIE End of Transmission interrupt enable
- ❒ ETIE = 1 enables that the ET interrupt request is sent to the CPU when ETINT is set.
- ❒ ETIE = 0 (default) disables the ET interrupt request.
- ❒ This bit is cleared by software reset (RST) and can be written and read by CPU.

■ bit12-8: NVFD[4:0] Number of valid FIFO data
- ❒ These bits indicate the number of stored receptions (SVD=0) or pending transmissions (SVD=1) in the FIFO buffer.
- ❒ If no FIFO is installed, these bits return 0x00.

12. Shutdown Mode

12.1 Overview

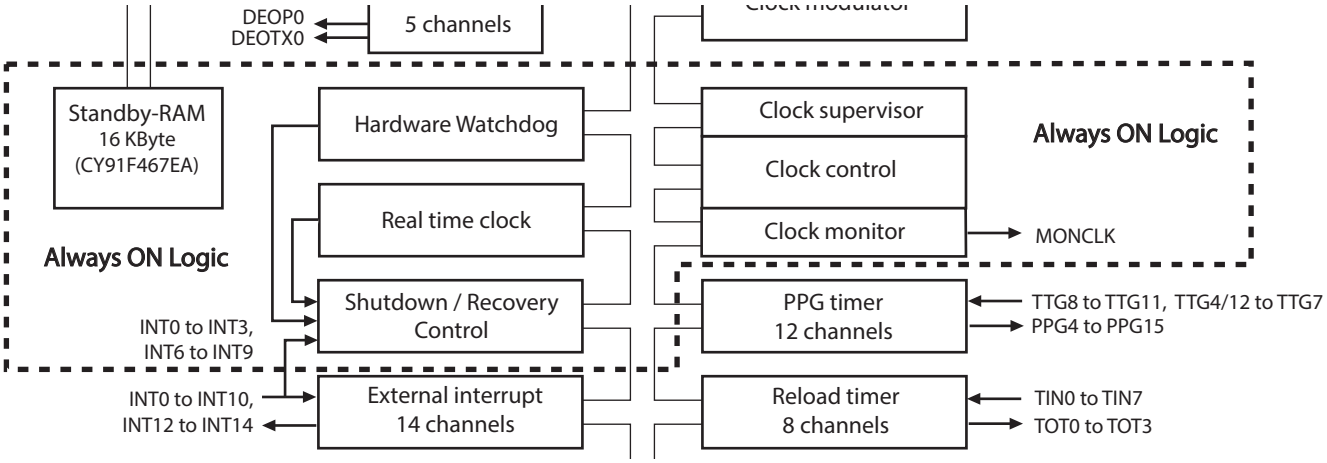
In Shutdown mode, the power supply of more then 80% of the internal logic and the main memories is switched off to minimize leakage.

This mode is a type of STOP state.
The device can enter this mode if it goes to STOP state when Shutdown is enabled.
During this mode, the oscillators can stop oscillating and the power is not supplied except for some logic.

The power continues to be supplied to the following circuits even in shutdown state:

- Standby RAM 16 KByte for data (address FFFAC000H to FFFAFFFH)
- Shutdown / recovery control circuit
- Clock control logic
- Real Time Clock
- 4 MHz oscillator + 32 kHz oscillator + RC oscillator
- Hardware Watchdog + Clock Supervisor

In the “Block Diagram” on page 23, this part of the device is called “Always ON Logic”:



The device will recover from Shutdown mode after the following events:

- Reset assertion by the INITX pin [a]
- External interrupt (8 sources)
- Real Time Clock interrupt
- Hardware watchdog reset
- Main Clock Supervisor reset

a. Reset by the INITX pin will kill the ShutDown state and restart the device like at power-on.

12.2 Standby RAM

CY91F467E containes a 16 KByte low-leakage RAM used as Standby RAM. The power supply of this RAM is not switched off in Shutdown state.

The Standby RAM is located at addresses FFFAC000H to FFFAFFFH.

To access it, to the RAM must be enabled by setting RAMEN bit in SHDE register. RAMEN is initialized by Software Reset (RST). If the RAM is to be accessed, make sure that no external bus Chip Select area overlaps the Standby RAM addresses.

The bit RAMEN is written using CLKP, while the Standby RAM is accessed with CLKB. If CLKP is slower then CLKB, make sure to have some wait time (at least 2 CLKP periods) between setting of RAMEN and first RAM access.

For the Standby RAM, low-leakage macros have been implemented. Read and write acces are performed with 1 wait cycle.

12.3 Shutdown Registers

12.3.1 Notes About the Reset Signals

The following register description mentiones different reset signals, which are explained shortly here. For more information, please refer to the CY91460 series hardware manual, “Chapter 9 Reset”.

■ Settings Initialization Reset (**INIT**):

initializes all the device’s control and clock settings. INIT can be triggered

- ❒ by low level on external INITX pin
- ❒ by low level on external HSTX pin (no hardware standby pin available in CY91460E series)
- ❒ by Hardware Watchdog Timer
- ❒ by Clock Supervisor
- ❒ by Software Watchdog Timer
- ❒ by Low Voltage Detection

■ Operation Initialization Reset (**RST**, “Software Reset”):

initializes CPU and peripherals and restarts the software. RST can be triggered

- ❒ by low level on external RSTX pin (not available in CY91460E series)
- ❒ by INIT (INIT always causes RST)
- ❒ by software (STCR.SRST=0)

■ Shutdown Recovery: The Shutdown state is released when a valid recovery factor is found. Shutdown recovery causes a Settings Initialization Reset (INIT) with some exceptions. For details, please refer to “Recovery from shutdown mode” on page 77.

12.3.2 SHDE: Shutdown control register

This register enables/disables the shutdown state as well as the Standby RAM.

■ **SHDE**: Address $0004D4_H$ Access: Byte

7	6	5	4	3	2	1	0	
SDENB	**-**	**-**	**-**	**-**	**-**	**-**	**RAMEN**	
0	X	X	X	X	X	X	0	Initial value [1]
retained	X	X	X	X	X	X	0	Initial value [2]
R/W	-	-	-	-	-	-	R/W	Attribute

1. Initial value after external pin INITX=0 or Shutdown Recovery
2. Initial value after Software Reset (RST)

[bit 7] SDENB: Shutdown enable

SDENB	Function
1	Enable shutdown state: On transition to STOP mode, the device enters Shutdown state.
0	Disable shutdown state: On transition to STOP mode, the device enters the normal STOP mode.

[bit 6 to bit 1] Reserved bits

■ The read value is undefined.

■ Always write 0 to these bits.

[bit 0] RAMEN: Standby RAM enable

RAMEN	Function
1	Enable the Standby RAM [1]: Read and write access to the Standby RAM is possible
0	Disable the Standby RAM: Read and write access to the Standby RAM is disabled.

1. The Standby RAM is located inside the address space of External Bus. If the Standby RAM is enabled, make sure that no chip select area of the External Bus overlaps the standby RAM area.

Note: RAMEN is cleared by INIT and by Software Reset because the chip select control registers (CSER, ACR0-7, ASR0-7, AWR0-7) are initialized by the same conditions. After both kinds of reset, chip select CS0 is enabled to cover all addresses of external bus area, which would overlap the Standby RAM address space.

Note: The bit RAMEN is written using CLKP, while the Standby RAM is accessed with CLKB. If CLKP is slower then CLKB, make sure to have some wait time (at least 2 CLKP periods) between setting of RAMEN and first RAM access.

12.3.3 EXTE: Shutdown recovery external interrupt enable register

This register enables external interrupts as the source for recovering from the shutdown state.

■ **EXTE**: Address $0004D6_H$ Access: Byte

7	6	5	4	3	2	1	0	
RX1	**RX0**	**INT7**	**INT6**	**INT3**	**INT2**	**INT1**	**INT0**	
0	0	0	0	0	0	0	0	Initial value [1]
retained	retained	retained	retained	retained	retained	retained	retained	Initial value [2]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute

1. Initial value after external pin INITX=0 or Shutdown Recovery
2. Initial value after Software Reset (RST)

Eight external interrupts that can be set as recovery sources are allocated to each bit, as shown in the table below:

bit	Pin No	Pin Name
7	93	P32_2/RX1/INT9
6	91	P23_0/RX0/INT8
5	90	P24_7/SCL3/INT7
4	89	P24_6/SDA3/INT6
3	86	P24_3/INT3
2	85	P24_2/INT2
1	84	P24_1/INT1
0	83	P24_0/INT0

[bit 7 to bit 0] Interrupt enable bits

Value	Function
1	Enable recovery interrupt
0	Disable recovery interrupt

❒ These bits can be read and written.
❒ External pin INITX=0 or Shutdown recovery clear these bits.

12.3.4 SHDINT: Shutdown recovery internal interrupt control and status register

The SHDINT register containes control bits and flags for enabling and indicating internal interrupts for recovery from shutdown mode.

■ **SHDINT**: Address $0004DB_H$ Access: Byte

7	6	5	4	3	2	1	0	
-	**-**	**-**	**-**	**HWWDF**	**HWWDE**	**RTCF**	**RTCE**	
X	X	X	X	0	0	0	0	Initial value [1]
X	X	X	X	retain	0	retain	0	Initial value [2]
X	X	X	X	retain	0	retain	retain	Initial value [3]
-	-	-	-	R(RM1)/ W0	R	R(RM1)/ W0	R/W	Attribute

1. Initial value after external pin INITX=0
2. Initial value after Shutdown Recovery
3. Initial value after Software Reset (RST)

[bit 7 to bit 4] Reserved bits

- The read value is undefined.
- Always write 0 to these bits.

[bit 3] HWWDF: Hardware Watchdog recovery flag

HWWDF	Function
1	Recovery factor from Hardware Watchdog found
0	No recovery factor from Hardware Watchdog found

- This bit is set in Shutdown mode, if HWWDE is set and if an INITX signal from Hardware Watchdog is detected.
- Writing "1" to this bit does not affect the operation.
- Writing "0" cleares the bit, external pin INITX=0 cleares the bit.
- "1" is read by a read-modify-write instruction.

[bit 2] HWWDE: Hardware Watchdog recovery enable (mirror of HWWDE.STP_RUN [a])

HWWDE	Function
1	Recovery reset from Hardware Watchdog is enabled, RC clock is enabled in STOP/Shutdown mode by hardware
0	Recovery reset from Hardware Watchdog is disabled, RC clock depends on CSVCR.RCE setting in STOP/Shutdown mode

- This bit is a read-only mirror of HWWDE.STP_RUN, which can be set only once after reset and cannot be cleared by CPU access.
- This bit is cleared by Software Reset (RST). Note that external pin INITX=0 or Shutdown recovery are always followed by a Software Reset RST.

[bit 1] RTCF: Real Time Clock recovery flag

RTCF	Function
1	Recovery factor from Real Time Clock found
0	No recovery factor from Real Time Clock found

- This bit is set in Shutdown mode, if RTCE is set and an interrupt signal from Real Time Clock is detected.
- Writing "1" to this bit does not affect the operation.
- Writing "0" cleares the bit, external pin INITX=0 cleares the bit.
- "1" is read by a read-modify-write instruction.

a. STP_RUN is bit HWWDE[4]

[bit 0] RTCE: Real Time Clock recovery enable

RTCE	Function
1	Recovery reset from Real Time Clock is enabled
0	Recovery reset from Real Time Clock is disabled

- This bit can be read and written.
- External pin INITX=0 or Shutdown recovery clear this bit.

12.3.5 EXTF: Shutdown recovery external interrupt source flags

This register indicates the recovery source for when a shutdown recovery external interrupt is used to recover.

■ **EXTF**: Address $0004D7_H$ Access: Byte

7	6	5	4	3	2	1	0	
RX1	**RX0**	**INT7**	**INT6**	**INT3**	**INT2**	**INT1**	**INT0**	
0	0	0	0	0	0	0	0	Initial value [1]
retained	retained	retained	retained	retained	retained	retained	retained	Initial value [2]
retained	retained	retained	retained	retained	retained	retained	retained	Initial value [3]
R(RM1)/ W0	R(RM1)/ W0	R(RM1)/ W0	R(RM1)/ W0	R(RM1)/ W0	R(RM1)/ W0	R(RM1)/ W0	R(RM1)/ W0	Attribute

1. Initial value after external pin INITX=0
2. Initial value after Shutdown Recovery
3. Initial value after Software Reset (RST)

The bit configuration is the same as for the EXTE register.

[bit 7 to bit 0] Interrupt factor flag bits

The bit corresponding to any input signal found to be valid as a recovery factor is set to "1."

Value	Function
1	Recovery factor found
0	No recovery factor found

- These bits are set in Shutdown mode, when the attached external interrupt channel is enabled by EXTE=1 and a recovery factor (level / edge) from the external interrupt channel is detected.
- Writing "1" to these bits does not affect the operation.
- Writing "0" cleares the bits, external pin INITX=0 cleares the bits.
- "1" is read by a read-modify-write instruction.

12.3.6 EXTLV1/2: Shutdown recovery external interrupt level selection register

This register sets the pin level for recovering from the shutdown state using an external interrupt.

■ **EXTLV1**: Address $0004D8_H$ Access: Halfword, Byte

15	14	13	12	11	10	9	8	
LB7	**LA7**	**LB6**	**LA6**	**LB5**	**LA5**	**LB4**	**LA4**	
0	0	0	0	0	0	0	0	Initial value [1]
retained	retained	retained	retained	retained	retained	retained	retained	Initial value [2]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute

1. Initial value after external pin INITX=0 or Shutdown Recovery
2. Initial value after Software Reset (RST)

■ **EXTLV2**: Address $0004D9_H$ Access: Halfword, Byte

7	6	5	4	3	2	1	0	
LB3	**LA3**	**LB2**	**LA2**	**LB1**	**LA1**	**LB0**	**LA0**	
0	0	0	0	0	0	0	0	Initial value [1]
retained	retained	retained	retained	retained	retained	retained	retained	Initial value [2]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute

1. Initial value after external pin INITX=0 or Shutdown Recovery
2. Initial value after Software Reset (RST)

Source levels of eight external interrupts that can be set as recovery sources are allocated to each bit, as shown in the table below.

bit	Pin No	Pin Name
15,14	93	P23_2/RX1/INT9
13,12	91	P23_0/RX0/INT8
11,10	90	P24_7/SCL3/INT7C
9,8	89	P24_6/SDA3/INT6D
7,6	86	P24_3/INT3
5,4	85	P24_2/INT2
3,2	84	P24_1/INT1
1,0	83	P24_0/INT0

[bit15 to bit0]: Interrupt level setting register

LBx	LAx	Interrupt Level
0	0	"L" level (initial value)
0	1	"H" level
1	0	Rising edge
1	1	Falling edge

Please refer to "External Interrupts: Level or Edge Setting" on page 76.

12.4 Shutdown Operation

12.4.1 Transition to shutdown state

Shutdown state is a special kind of the STOP state. During Shutdown, the settings in the STCR register for Oscillation Disable (STCR.OSCD1, STCR.OSCD2), Hi-Z mode (STCR.HIZ) and Oscillation Stabilization time (STCR.OS[1:0]) are valid the same kind as in normal STOP state. At recovery from Shutdown, STCR.OS[1:0] are not cleared to maintain the oscillator stabilisation time, while STCR.OSCD1, STCR.OSCD2 and STCR.HIZ are initialized by the recovery.

For transition into Shutdown, do the following:

- Enable at least one recovery condition (otherwise, recovery is only possible by external INITX pin)
- Enable the Shutdown mode
- Switch the device to STOP mode

The details are explained below.

Precautions

Before enabling Shutdown, consider the following:

- Data, which is needed after recovery from Shutdown, should be copied into the Standby RAM.
- The CPU should run on Main- or Sub-Oscillation, not on PLL. The PLL should be disabled.
- The Sub-Regulator can be set to 1.2 V in STOP mode by setting REGSEL.SUBSEL = 0x00
- Specify the levels of external interrupt signals used for recovery in EXTLV1/2 registers
- Enable the channels of external interrupt signals for recovery in EXTE register

Deep Shutdown Settings for maximal power saving

The following settings generate Shutdown without any activity on the device:

- Disable all pin pull-up/pull-down settings which are not required, or set the STCR.HIZ [a] bit when going to STOP.
- Set external bus pins to port mode / input direction (otherwise some pins will output constant values, see "I/O Behaviour in Shutdown" on page 80).
- Don't set Hardware Watchdog Run in STOP mode (HWWDE.STP_RUN [b] =0, this is default setting)
- Disable the RC oscillator in STOP mode (CSVCR.RCE=0)
- Disable the Low Voltage Detection in STOP mode (LVDET.LVEPD=1, LVDET.LVIPD=1)
- Disable the Main and the Sub oscillators in STOP mode (STCR.OSCD1=1, STCR.OSCD2=1)
- Set the Shutdown Enable bit SHDE.SDENB=1 to enable shutdown mode
- Go to STOP: set the STOP request STCR.STOP=1 and read back STCR two times.

Shutdown with Real Time Clock running

The following settings generate Shutdown with the RTC running on Main-Oscillation, Sub-Oscillation or RC clock, and with recovery by RTC enabled:

- Set the RTC prescaler values depending on the clock speed (WTBR register)
- If recovery by the RTC is needed:
  - Enable at least one of the the RTC interrupts (half-second, second, minute, hour or day) in WTCR and/or WTCE register
  - Enable RTC recovery: set SHDINT.RTCE=1
- If RTC uses Main Oscillation:
  - Disable the RC oscillator in STOP mode (CSVCR.RCE=0)
  - Disable the Sub oscillator in STOP mode (STCR.OSCD2=1) and keep Main oscillator running (OSCD1=0)
  - The RTC is connected to Main oscillation by default.
- If RTC uses Sub Oscillation:
  - Disable the RC oscillator in STOP mode (CSVCR.RCE=0)
  - Disable the Main oscillator in STOP mode (STCR.OSCD1=1) and keep Sub oscillator running (OSCD2=0)
  - Connect the RTC to Sub oscillator: set CSCFG.CSC[1:0]=01
- If RTC uses RC clock:
  - Enable the RC oscillator in STOP mode (CSVCR.RCE=1, this is default setting)

a. With STCR.HIZ=1, all pull-ups and pull-downs are disabled in STOP/Shutdown.
b. STP_RUN is bit [4] of HWWDE register. It enables running the Hardware Watchdog in STOP mode. STP_RUN can only be set by software, but not cleared. STP_RUN is cleared by INIT.

- Disable the Main and the Sub oscillators in STOP mode (STCR.OSCD1=1, STCR.OSCD2=1)
- Connect the RTC to RC oscillator: set CSCFG.CSC[1:0]=10

❒ Set the Shutdown Enable bit SHDE.SDENB=1 to enable shutdown mode
❒ Go to STOP: set the STOP request STCR.STOP=1 and read back STCR two times.

Hardware Watchdog in Shutdown

The Hardware Watchdog can run in STOP mode, if the bit HWWDE.STP_RUN [a] is set.

❒ Outside STOP mode, the Hardware Watchdog timeout will send an INIT signal to the CPU via the Shutdown control.
❒ In STOP mode without Shutdown, the Hardware Watchdog timeout will send an INIT signal to the CPU via the (inactive) Shutdown control, which cancelles the STOP mode immediately.
❒ In STOP mode with Shutdown enabled, the Hardware Watchdog timeout will set the SHDINT.HWWDF flag, causing a recovery from Shutdown.

The Hardware Watchdog can be enabled in Shutdown state like follows:

❒ Enable the Hardware Watchdog operation in STOP mode: set HWWDE.STP_RUN = 1
In parallel, this enables the RC oscillator by hardware, and the Hardware Watchdog recovery Enable bit SHDINT.HWWDE is set by hardware too.
❒ If RTC is needed, enable it like described in Shutdown with Real Time Clock running above.
❒ Specify the levels of external interrupt signals used for recovery in EXTLV1/2 registers
❒ Enable the channels of external interrupt signals for recovery in EXTE register
❒ Set the Shutdown Enable bit SHDE.SDENB=1 to enable shutdown mode
❒ Clear/restart the Hardware Watchdog: write 0 to bit HWWD.CL
❒ Go to STOP: set the STOP request STCR.STOP=1 and read back STCR two times.

If the timeout is reached, the Hardware Watchdog generates INIT, which cancelles the Shutdown state and forces recovery. The CPU will run on Main Oscillation after this recovery.

WARNING: If a Hardware Watchdog timeout INIT signal appeares just at the transition to Standby Mode, the device may enter an unpredictable state. Always make sure that the hardware Watchdog has been cleared just before entering Shutdown.

Clock Supervisor in Shutdown

The INITX pin, Clock Supervisor and Hardware Watchdog form the “external INIT chain”, like shown in the figure in section “Determining the Reset Source after Shutdown” on page 78. The Shutdown control is part of this chain.

An INIT signal from the Clock Supervisor will pass the Hardware Watchdog and arrive at the same Shutdown control input line as the INIT signal from Hardware Watchdog. Therefore, clock supervision in Shutdown mode is only possible if the Hardware Watchdog is operating in parallel.

If the Hardware Watchdog is disabled in Shutdown mode, an INIT signal from the Clock Supervisor is ignored in Shutdown.

The Clock Supervisor is enabled by default. In Shutdown mode, as long as the Main- and/or Sub-oscillator is running and the RC clock is not stopped, the CSV is supervising the Main- or Sub-oscillator, respectively.

❒ The Clock Supervisor needs the RC clock, so set CSVCR.RCE=1, this is default setting.
❒ If the Main-oscillator is not stopped (STCR.OSCD1=0), the Main clock supervisor is running.
❒ If the Main-oscillator fails, the Main Clock Supervisor generates INIT, which can cancel the Shutdown state and force recovery. The CPU runs on RC clock during and after the recovery.
❒ If the Sub-oscillator is not stopped (STCR.OSCD2=0), the Sub Clock Supervisor is running.
❒ If the Sub-oscillator fails, the Sub clock is switched to RC clock divided by 2. An INIT is not generated, and the Real Time Clock continues running on on RC clock divided by 2, if RTC is enabled.

To disable the Clock Supervisor, clear the bits CSVCR.MSVE and CSVCR.SSVE.

Low Voltage Detection in Shutdown

Low Voltage Detection is not supported in Shutdown mode. Always set the Low Voltage Detection into power down mode (LVDET.LVEPD=1, LVDET.LVIPD=1) before enabling Shutdown.

a. STP_RUN is bit [4] of HWWDE register. It enables running the Hardware Watchdog in STOP mode. STP_RUN can only be set by software, but not cleared. STP_RUN is cleared by INIT.

External Interrupts: Input Voltage Setting

The input voltages (CMOS-Schmitt, Automotive, TTL, CMOS-2) of the external interrupt lines are defined by the setting of PILR and EPILR of the appropriate ports. The PILR and EPILR settings for the 8 external recovery interrupt lines are maintained during Shutdown mode until they are cleared by the Software reset following the Recovery INIT.

EPILR	PILR	Pin No	Pin Name
EPILR23[2]	PILR23[2]	93	P23_2/RX1/INT9
EPILR23[0]	PILR23[0]	91	P23_0/RX0/INT8
EPILR24[7]	PILR24[7]	90	P24_7/SCL3/INT7C
EPILR24[6]	PILR24[6]	89	P24_6/SDA3/INT6D
EPILR24[3]	PILR24[3]	86	P24_3/INT3
EPILR24[2]	PILR24[2]	85	P24_2/INT2
EPILR24[1]	PILR24[1]	84	P24_1/INT1
EPILR24[0]	PILR24[0]	83	P24_0/INT0

External Interrupts: Level or Edge Setting

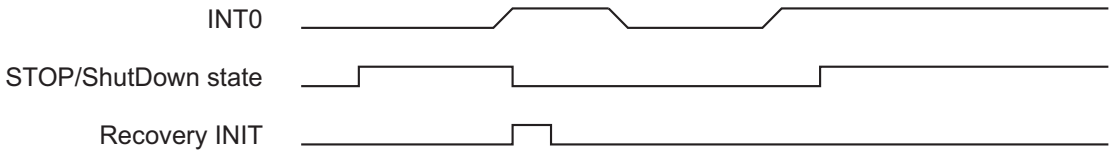
The registers EXTLV1 and EXTLV2 are used to set the interrupt level or edge for recovery per interrupt channel.

LBx	LAx	Interrupt Level
0	0	"L" level (initial value)
0	1	"H" level
1	0	Rising edge
1	1	Falling edge

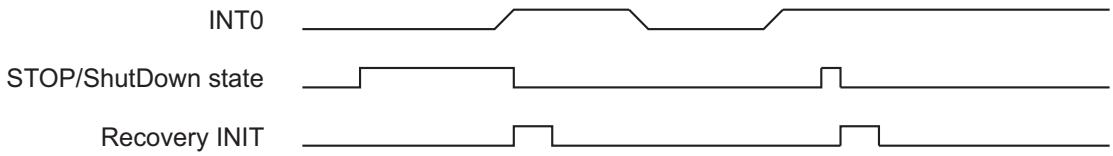
The settings “level” and “edge” generate different behaviour if the external source line is not changed back after recovery of if it changes to the sensitive level before Shutdown.

Examples:

- INT0 is enabled for recovery on **risong edge**. If a rising edge appeares during Shutdown state, recovery is performed. If a rising edge is outside Shutdown state, there will be no recovery:



- INT0 is enabled for recovery on **high level**. If INT0 changes to high level during Shutdown state, recovery is performed. If INT0 changes to high level already before Shutdown state, the Shutdown is recovered immediately because the high level on INT0 is valid. Note that, in this case, a complete shut-down/power-up sequence with recovery INIT is performed:



Note: If “H” level or “L” level is enabled for recovery, the level must be active for minimum 500 µs.

12.4.2 Recovery from shutdown mode

The following factors are available to recover from the shutdown state:

- Assert the reset signal at the INITX terminal for minimum 10 ms [a] [b]
- Input of a valid recovery request via an external interrupt terminal
- Real Ttime Clock Interrupt (when RTC interrupt is enabled)
- Hardware Watchdog reset (when HWWD is enabled in STOP mode)
- Main Clock Supervisor reset (when Main oscillator is running and Main Clock Supervisor is enabled and recovery by HWWD is enabled)

Shutdown state is released when a valid recovery factor is permitted. After the Shutdown state release, the device restarts with a settings initialization reset (INIT), just like power-up operation. Only the Real Time Clock, the Oscillation Stabilization settings in STCR register, and the recovery source flags in the Shutdown registers EXTF and SHDINT are not cleared.

The internal restart sequence is as follows:

1. Resume the internal power supply.
2. Reset and assert the initialization reset (INIT).
3. Wait for oscillation stabilization.
4. Start the reset sequence.

As the external interrupt source flags and the RTC flag are retained in EXTF and SHDINT registers, it is possible to determine whether it is power-up operation or recovery from shutdown state by checking the flags.

The Real Time Clock at Recovery from Shutdown

In normal operation, the registers and settings of the Real Rime Clock are initialized by Software Reset (RST).

At recovery from Shutdown, the RTC is **not** initialized:

- The prescaler, second, minute and hour counters continue counting also during the recovery INIT state.
- The clock selection for the RTC (by CSCFG.OSC1, CSCFG.OSC0) remains unchanged.
- The RTC interrupt enable bits and interrupt flags (in WTCR and WTCE registers) remain unchanged.

So at each recovery from Shutdown, the RTC continues running and the current time as well as the interrupt flags can be read from the RTC after recovery.

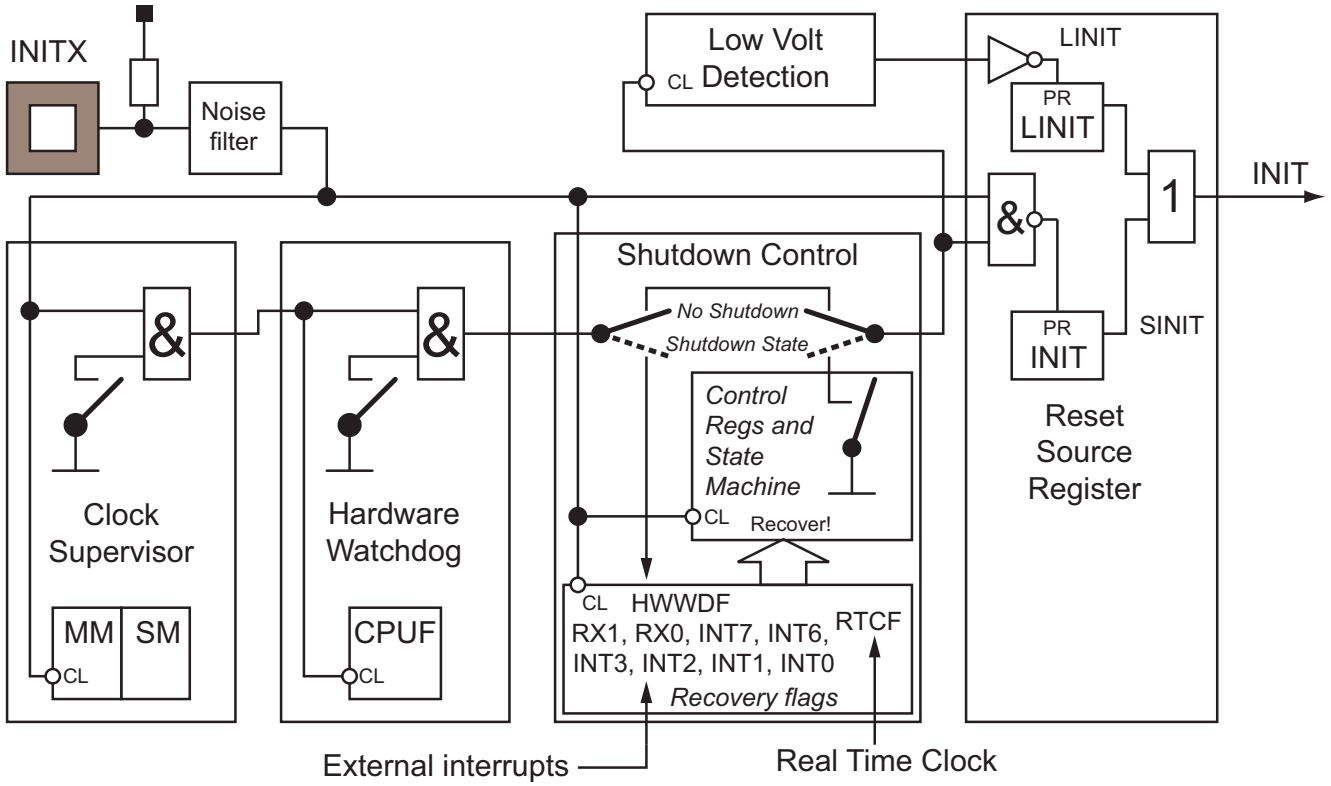
Note: The Interrupt Control Register for RTC (ICR58), the Interrupt Level Mask (ILM) register as well as the Condition Code Register (CCR, containing the I-Flag) are cleared by the recovery INIT, so that all interrupt processing is disabled.
If the software re-enables interrupt processing by setting ICR58, ILM and I-Flag, the software will process the pending RTC interrrupt immediately.

a. The minimum INTX=0 pulse length is determined by the time the main oscillator needs for stabilization.
b. Reset by INITX=0 will kill the ShutDown state and restart the device like at power-on.

12.4.3 Determining the Reset Source after Shutdown

The recovery from Shutdown is followed by an Setting Initialization Reset (INIT). Because INIT is always followed by a Software Reset (RST), the CPU fetches the Mode- and Reset-Vectors and jumps to the Reset Vector, which is located in the Boot ROM.

The following drawing shows how the Shutdown Control is located in the external INIT chain:



The following table lists the registers and flags for determination of the reset source, including Shutdown:

Register	Addr.	7	6	5	4	3	2	1	0
RSRR	**480_H** [1]	**INIT**	**HSTB**	**WDOG**	**ERST**	**SRST**	**LINIT**	*WT1*	*WT0*
EXTF	**$4D7_H$**	**RX1**	**RX0**	**INT7**	**INT6**	**INT3**	**INT2**	**INT1**	**INT0**
SHDINT	**$4DB_H$**	-	-	-	-	**HWWDF**	*HWWDE*	**RTCF**	*RTCE*
CSVCR	**$4AD_H$**	*SCKS*	**MM**	**SM**	*RCE*	*MSVE*	*SSVE*	*SRST*	*OUTE*
HWWD	**$4C7_H$**	-	-	-	-	*CL*	-	-	**CPUF**

1. RSRR is read and cleared by the Boot ROM software. After Boot ROM, the content of RSRR can be found in CPU register R4[7:0] and in a variable in memory.

Note:

RSRR: Reset Source register
EXTF: External shutdown recovery flags, see page page 72
SHDINT: Hardware Watchdog/ Real Time Clock recovery flags, see page page 71
CSVCR: CLock Supervisor Control / Status register
HWWD: Hardware Watchdog register
For details about RSRR, CSVCR and HWWD, please refer to the hardware manual.

Recovery from Shutdown will set the INIT bit in RSRR register. Because the INIT bit can also be set by external INIT (low level at INITX pin), Clock Supervisor or Hardware Watchdog, the flags in EXTF, SHDINT, CSVCR and HWWD should be checked for determining the reset source.

The recovery flags in EXTF and SHDINT are set **only** in Shutdown mode and **only** if recovery by this channel is enabled.

12.4.4 Registers which are not initialized by Shutdwon Recovery

As described above, recovery from Shutdown performes a settings initialization reset (INIT) followed by software reset (RST). This sequence will initialize the complete device with some exceptions, explained in the following table.

Registers which are not initialized by Shutdown Recovery:

Register	Address	non-initialized Bits	Reason
STCR	481_H	OS1, OS0	Keep oscillation stabilization time setting
CSVCR	$4AD_H$	all bits	Clock Supervisor is not initialized by recovery
CSCFG	$4AE_H$	all bits	Keep RTC and Calibration clock source settings
CMCFG	$4AF_H$	all bits	Keep Clock Monitor settings
WTCER	$4A1_H$	all bits	Real Time Clock to continue running
WTCR	$4A2_H$ - $4A3_H$		
WTBR	$4A5_H$ - $4A7_H$		
WTHR	$4A8_H$		
WTMR	$4A9_H$		
WTSR	$4AA_H$		
CUCR	$4B0_H$ - $4B1_H$	all bits	Subclock Calibration unit is part of RTC module
CUTD	$4B2_H$ - $4B3_H$		
CUTR1	$4B4_H$ - $4B5_H$		
CUTR2	$4B6_H$ - $4B7_H$		
HWWDE	$4C6_H$	all bits	Hardware Watchdog is not initialized by recovery
HWWD	$4C7_H$	all bits	
EXTF	$4D7_H$	all bits	Keep external recovery flags
SHDINT	$4DB_H$	HWWDF, RTCF	Keep hardware watchdog and RTC recovery flags

Note: If the ShutDown state is killed by external pin INITX=0, these registers are initialized like at normal power-on.

12.4.5 I/O Behaviour in Shutdown

During Shutdown mode, the I/O pins are switched into dedicated states:

Ports/Pins	Port function		Setting
P00_0 to P00_7, P01_0 to P01_7, P02_0 to P02_7, P03_0 to P03_7.	D[31:0]	External bus data I/O	The pins are switched to input direction, but it is not possible to input signals on these pins. If STCR.HIZ (HiZ mode in STOP) is not set, the pull-up/pull-down settings are maintained during shutdown. If STCR.HIZ is set, the pull-up and pull-down resistors are disabled.
P08_6, P08_7, P10_5, P13_0	BRQ, RDY, MCLKI, DREQ0	External bus control inputs	
P04_0 to P04_1, P05_0 to P05_7, P06_0 to P06_7, P07_0 to P07_7.	A[25:0]	External bus address outputs	
P08_0 to P08_5, P09_0 to P09_7, P10_1 to P10_4, P10_6, P13_1, P13_2	WRnX, RDX, BGRNTX, CSnX, ASX, BAAX, WEX, MCLKO, MCLKE	External bus control and clock outputs	If the pins were switched to output direction before shutdown (by PFR==1 or DDR==1), the pins will output '1' value and the driver strength is switched to 2 mA. Otherwise, the pins keep input direction, but it is not possible to input signals on these pins. If STCR.HIZ is not set, the pull-up/pull-down settings are maintained. If STCR.HIZ is set, the pull-up and pull-down resistors are disabled.
P24_0 to P24_3, P24_6, P24_7, P23_0, P23_2	INT0 to INT3, INT6, INT7, RX0/INT8, RX1/INT9	Pins used for Shutdown recovery	The pins are switched to input direction. If STCR.HIZ is not set, the pull-up/pull-down settings are maintained during shutdown. If STCR.HIZ is set, the pull-up and pull-down resistors are disabled. If external interrupt is enabled for recovery from Shutdown (Shutdown INTE=1), the input threshold setting (PILR, EPILR) is maintained during the shutdown mode and it is possible to input signals for recovery. After the first recovery factor is accepted, the port settings are initialized when the device proceeds to the reset (INIT/RST) sequence.
Pnn_m [1]	all other Ports not mentioned above		All other pins are switched to input direction, but it is not possible to input signals on these pins. If STCR.HIZ is not set, the pull-up/pull-down settings are maintained during Shutdown. If STCR.HIZ is set, the pull-up and pull-down resistors are disabled.
ALARM_0	ALARM analog input		The state of ALARM input is not changed in Shutdown state.
MD_0 to MD_2	Mode inputs		The state of MD[2:0] is not changed in Shutdown state
INITX	External INIT		The state of INITX is not changed in Shutdown state. The pull-up is enabled. It is possible to input external INITX signal during Shutdown.
VCC18C	Regulator capacitor pin		The capacitor connection pin for internal regulator shows the voltage which is applied to internal Always-ON domain.

1. nn = 14 to 29, m = 0 to 7

13. CPU and Control Unit

The FR family CPU is a high performance core that is designed based on the RISC architecture with advanced instructions for embedded applications.

13.1 Features

- Adoption of RISC architecture

  Basic instruction: 1 instruction per cycle

- General-purpose registers: 32-bit × 16 registers
- 4 Gbytes linear memory space
- Multiplier installed

  32-bit × 32-bit multiplication: 5 cycles
  16-bit × 16-bit multiplication: 3 cycles

- Enhanced interrupt processing function

  Quick response speed (6 cycles)
  Multiple-interrupt support
  Level mask function (16 levels)

- Enhanced instructions for I/O operation

  Memory-to-memory transfer instruction
  Bit processing instruction
  Basic instruction word length: 16 bits

- Low-power consumption

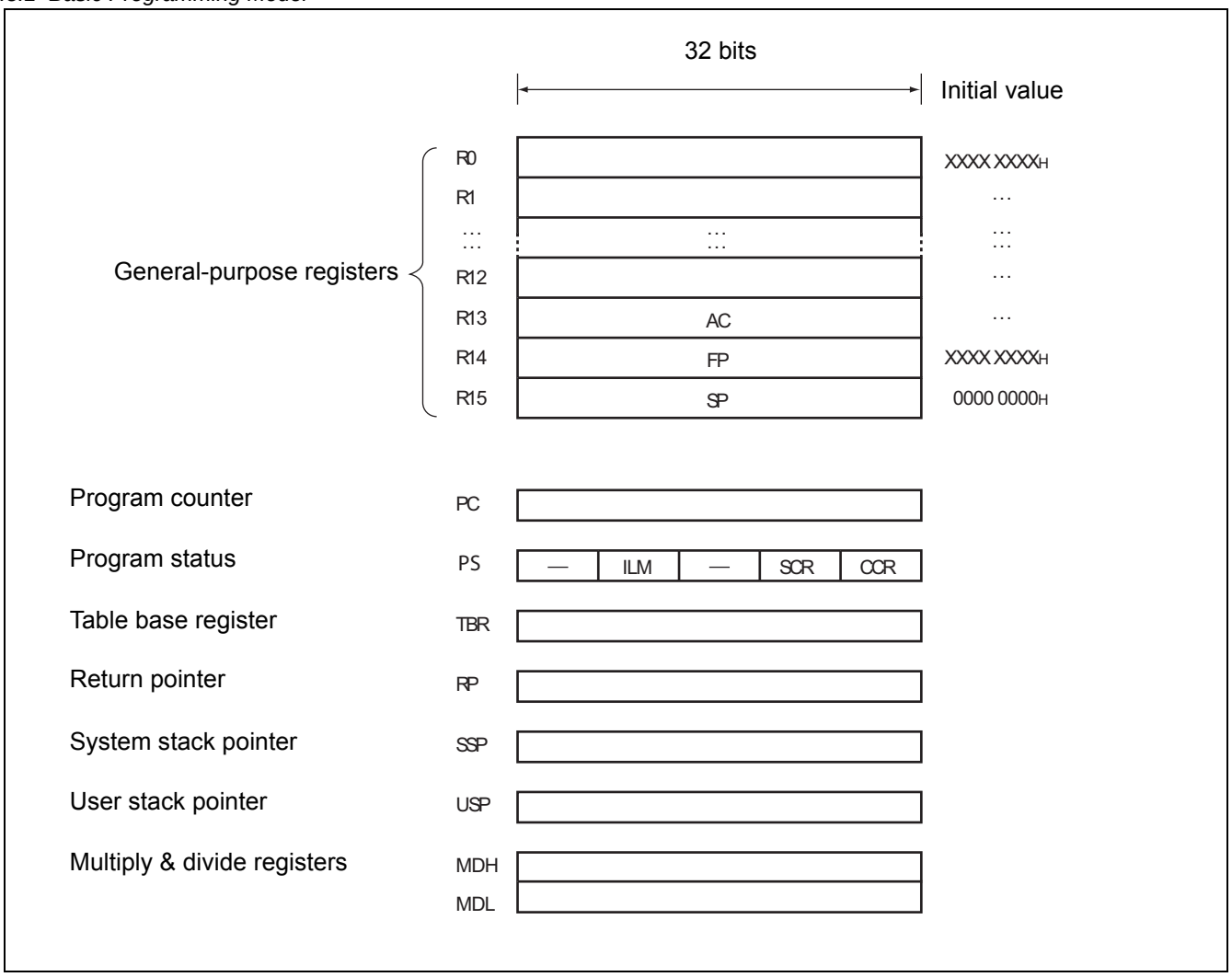
  Sleep mode/stop mode

13.2 Internal Architecture

- The FR family CPU uses the Harvard architecture in which the instruction bus and data bus are independent of each other.
- A 32-bit ↔ 16-bit buffer is connected to the 32-bit bus (D-bus) to provide an interface between the CPU and peripheral resources.
- A Harvard ↔ Princeton bus converter is connected to both the I-bus and D-bus to provide an interface between the CPU and the bus controller.

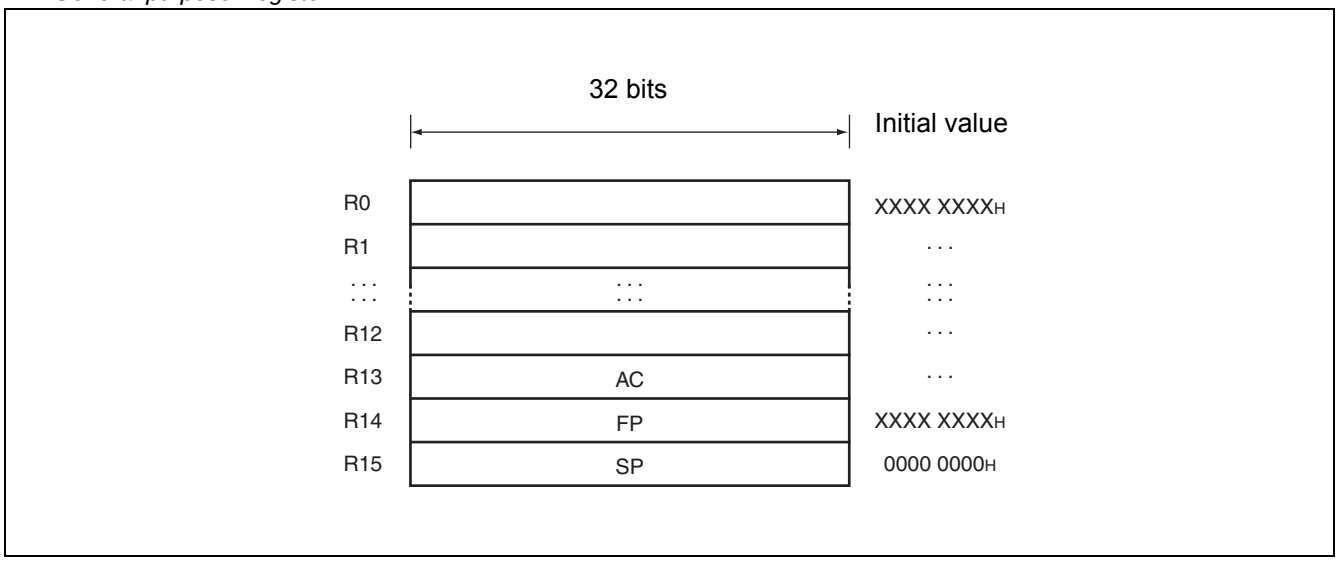
13.3 Programming Model

13.3.1 Basic Programming Model



13.4 Registers

13.4.1 General-purpose Register



Registers R0 to R15 are general-purpose registers. These registers can be used as accumulators for computation operations and as pointers for memory access.

Of the 16 registers, enhanced commands are provided for the following registers to enable their use for particular applications.

R13: Virtual accumulator

R14: Frame pointer

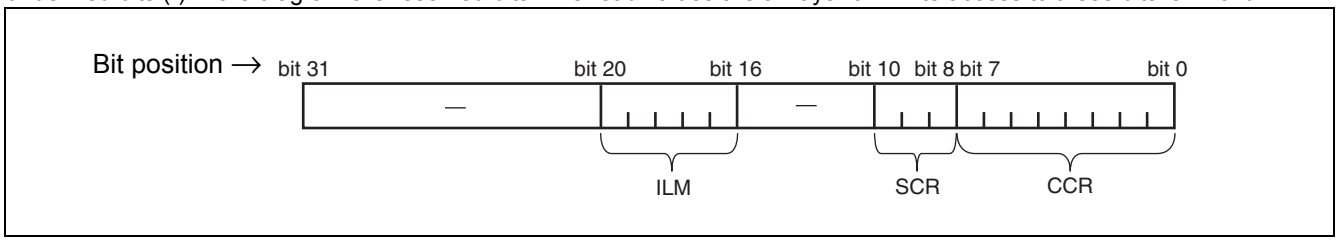
R15: Stack pointer

Initial values at reset are undefined for R0 to R14. The value for R15 is 00000000_H (SSP value).

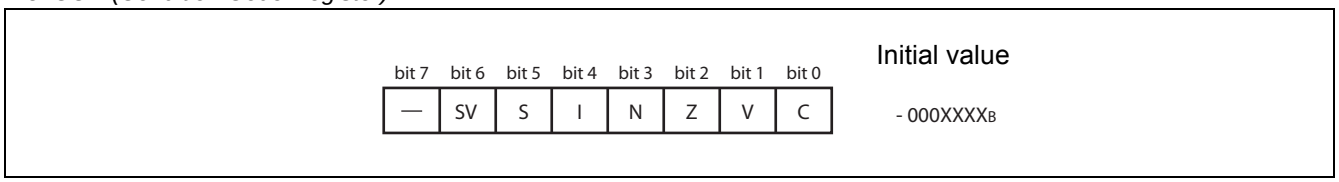
13.4.2 PS (Program Status)

This register holds the program status, and is divided into three parts, ILM, SCR, and CCR.

All undefined bits (-) in the diagram are reserved bits. The read values are always "0". Write access to these bits is invalid.



13.4.3 CCR (Condition Code Register)

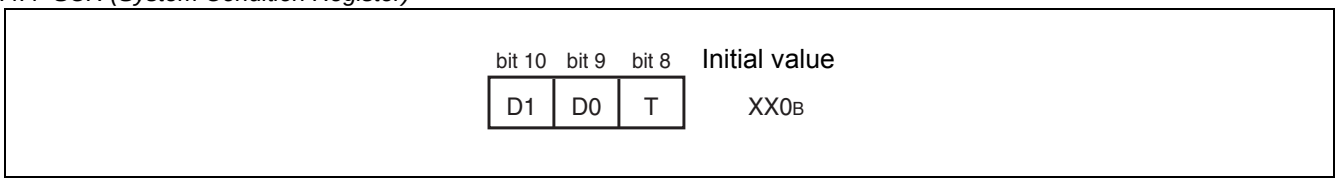


SV: Supervisor flag

S: Stack flag

I: Interrupt enable flag
N: Negative enable flag
Z: Zero flag
V: Overflow flag
C: Carry flag

13.4.4 SCR (System Condition Register)



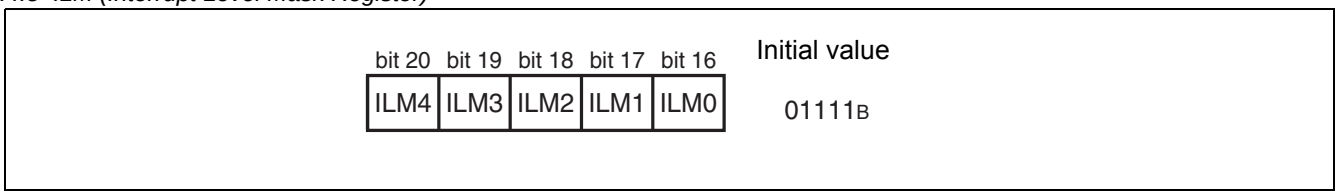
Flag for step division (D1, D0)

This flag stores interim data during execution of step division.

Step trace trap flag (T)

This flag indicates whether the step trace trap is enabled or disabled.
The step trace trap function is used by emulators. When an emulator is in use, it cannot be used in execution of user programs.

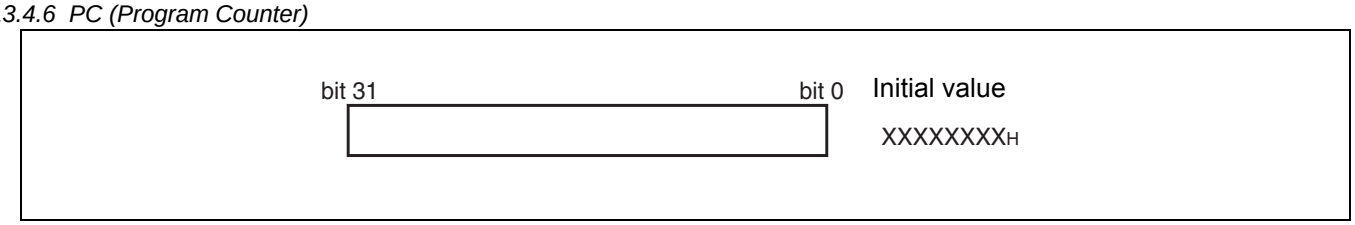
13.4.5 ILM (Interrupt Level Mask Register)



This register stores interrupt level mask values, and the values stored in ILM4 to ILM0 are used for level masking.

The register is initialized to value "01111_B" at reset.

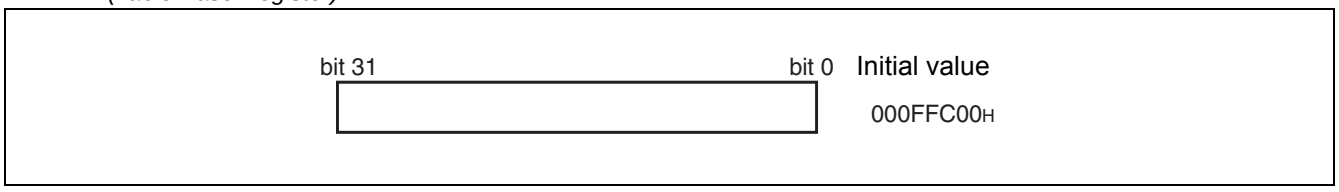
13.4.6 PC (Program Counter)



The program counter indicates the address of the instruction that is being executed.

The initial value at reset is undefined.

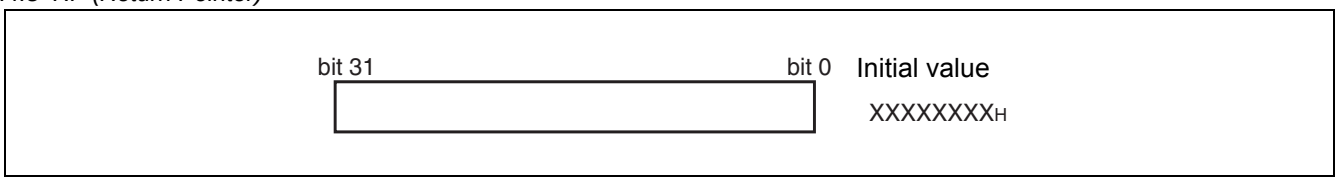
13.4.7 TBR (Table Base Register)



The table base register stores the starting address of the vector table used in EIT processing.

The initial value at reset is $000FFC00_H$.

13.4.8 RP (Return Pointer)



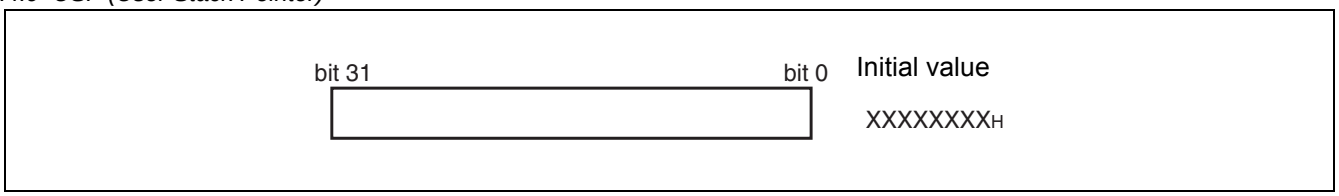
The return pointer stores the address for return from subroutines.

During execution of a CALL instruction, the PC value is transferred to this RP register.

During execution of a RET instruction, the contents of the RP register are transferred to PC.

The initial value at reset is undefined.

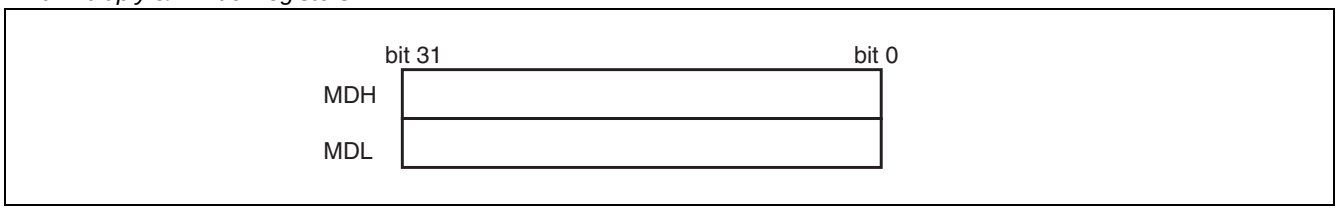
13.4.9 USP (User Stack Pointer)



The user stack pointer, when the S flag is “1”, this register functions as the R15 register.

- The USP register can also be explicitly specified.
  The initial value at reset is undefined.
- This register cannot be used with RETI instructions.

13.4.10 Multiply & Divide Registers



These registers are for multiplication and division, and are each 32 bits in length.

The initial value at reset is undefined.

14. Embedded Program/Data Memory (Flash)

14.1 Flash Features

- CY91F467EA: 1088 Kbytes (16 × 64 Kbytes + 8 × 8 Kbytes) = 8.5 Mbits
- Programmable wait state for read/write access
- Flash and Boot security with security vector at 0x0014:8000 - 0x0014:800F
- Boot security
- Basic specification: Same as MBM29LV400TC (except size and part of sector configuration)

14.2 Operation Modes

(1) 64-bit CPU mode:
- CPU reads and executes programs in word (32-bit) length units.
- Flash writing is not possible.
- Actual Flash Memory access is performed in d-word (64-bit) length units.

(2) 32-bit CPU mode:
- CPU reads, writes and executes programs in word (32-bit) length units.
- Actual Flash Memory access is performed in word (32-bit) length units.

(3) 16-bit CPU mode:
- CPU reads and writes in half-word (16-bit) length units.
- Program execution from the Flash is not possible.
- Actual Flash Memory access is performed in half-word (16-bit) length units.

Note: The operation mode of the flash memory can be selected using a Boot-ROM function. The function start address is 0xBF60. The parameter description is given in the Hardware Manual in chapter 54.6 "Flash Access Mode Switching".

14.3 Flash Access in CPU Mode

14.3.1 Flash Configuration

Figure 14-1. Flash memory map CY91F467EA

Address									
0014:FFFFh 0014:C000h	SA6 (8KB)				SA7 (8KB)				ROMS7
0014:BFFFh 0014:8000h	SA4 (8KB)				SA5 (8KB)				
0014:7FFFh 0014:4000h	SA2 (8KB)				SA3 (8KB)				
0014:3FFFh 0014:0000h	SA0 (8KB)				SA1 (8KB)				
0013:FFFFh 0012:0000h	SA22 (64KB)				SA23 (64KB)				ROMS6
0011:FFFFh 0010:0000h	SA20 (64KB)				SA21 (64KB)				
000F:FFFFh 000E:0000h	SA18 (64KB)				SA19 (64KB)				ROMS5
000D:FFFFh 000C:0000h	SA16 (64KB)				SA17 (64KB)				ROMS4
000B:FFFFh 000A:0000h	SA14 (64KB)				SA15 (64KB)				ROMS3
0009:FFFFh 0008:0000h	SA12 (64KB)				SA13 (64KB)				ROMS2
0007:FFFFh 0006:0000h	SA10 (64KB)				SA11 (64KB)				ROMS1
0005:FFFFh 0004:0000h	SA8 (64KB)				SA9 (64KB)				ROMS0
	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7	
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
32bit read/write	dat[31:0]				dat[31:0]				
64bit read	dat[63:0]								

14.3.2 Flash access timing settings in CPU mode

The following tables list all settings for a given maximum Core Frequency (through the setting of CLKB or maximum clock modulation) for Flash read and write access.

Table 14-1. Flash read timing settings (synchronous read)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 24 MHz	0	0	0	-	1	
to 48 MHz	0	0	1	-	2	
to 80 MHz	1	1	3	-	4	

Table 14-2. Flash write timing settings (synchronous write)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 32 MHz	1	-	-	0	4	
to 48 MHz	1	-	-	0	5	
to 64 MHz	1	-	-	0	6	
to 80 MHz	1	-	-	0	7	

14.3.3 Address mapping from CPU to parallel programming mode

The following tables show the calculation from CPU addresses to flash macro addresses which are used in parallel programming.

Table 14-3. Address mapping CY91F467EA

CPU Address (addr)	Condition	Flash sectors	FA (flash address) Calculation
14:0000h to 14:FFFFh	addr[2]==0	SA0, SA2, SA4, SA6 (8 Kbyte)	FA:= addr - addr%00:4000h + (addr%00:4000h)/2 - (addr/2)%4 + addr%4 - 05:0000h
14:0000h to 14:FFFFh	addr[2]==1	SA1, SA3, SA5, SA7 (8 Kbyte)	FA:= addr - addr%00:4000h + (addr%00:4000h)/2 - (addr/2)%4 + addr%4 - 05:0000h + 00:2000h
04:0000h to 13:FFFFh	addr[2]==0	SA8, SA10, SA12, SA14, SA16, SA18, SA20, SA22 (64 Kbyte)	FA:= addr - addr%02:0000 + (addr%02:0000h)/2 - (addr/2)%4 + addr%4 + 0C:0000h
04:0000h to 13:FFFFh	addr[2]==1	SA9, SA11, SA13, SA15, SA17, SA19, SA21, SA23 (64 Kbyte)	FA:= addr - addr%02:0000h + (addr%02:0000h)/2 - (addr/2)%4 + addr%4 + 0C:0000h + 01:0000h

Note: FA result is without 20:0000h offset for parallel Flash programming.
Set offset by keeping FA[21] = 1 as described in section “Parallel Flash programming mode”.

14.4 Parallel Flash Programming Mode

14.4.1 Flash configuration in parallel Flash programming mode

Parallel Flash programming mode (MD[2:0] = 111):

CY91F467EA

FA[21:0]	
003F:FFFFh 003F:0000h	SA23 (64KB)
003E:FFFFh 003E:0000h	SA22 (64KB)
003D:FFFFh 003D:0000h	SA21 (64KB)
003C:FFFFh 003C:0000h	SA20 (64KB)
003B:FFFFh 003B:0000h	SA19 (64KB)
003A:FFFFh 003A:0000h	SA18 (64KB)
0039:FFFFh 0039:0000h	SA17 (64KB)
0038:FFFFh 0038:0000h	SA16 (64KB)
0037:FFFFh 0037:0000h	SA15 (64KB)
0036:FFFFh 0036:0000h	SA14 (64KB)
0035:FFFFh 0035:0000h	SA13 (64KB)
0034:FFFFh 0034:0000h	SA12 (64KB)
0033:FFFFh 0033:0000h	SA11 (64KB)
0032:FFFFh 0032:0000h	SA10 (64KB)
0031:FFFFh 0031:0000h	SA9 (64KB)
0030:FFFFh 0030:0000h	SA8 (64KB)
002F:FFFFh 002F:E000h	SA7 (8KB)
002F:DFFFh 002F:C000h	SA6 (8KB)
002F:BFFFh 002F:A000h	SA5 (8KB)
002F:9FFFh 002F:8000h	SA4 (8KB)
002F:7FFFh 002F:6000h	SA3 (8KB)
002F:5FFFh 002F:4000h	SA2 (8KB)
002F:3FFFh 002F:2000h	SA1 (8KB)
002F:1FFFh 002F:0000h	SA0 (8KB)

	FA[1:0]=00	FA[1:0]=10
16bit write mode	DQ[15:0]	DQ[15:0]

Remark: Always keep FA[0] = 0 and FA[21] = 1

14.4.2 Pin Connections in Parallel Programming Mode

Resetting after setting the MD[2:0] pins to [111] will halt CPU functioning. At this time, the Flash memory's interface circuit enables direct control of the Flash memory unit from external pins by directly linking some of the signals to General Purpose Ports. Please see table below for signal mapping.

In this mode, the Flash memory appears to the external pins as a stand-alone unit. This mode is generally set when writing/erasing using the parallel Flash programmer. In this mode, all operations of the 8.5 Mbits Flash memory's Auto Algorithms are available.

Table 14-4. Correspondence between MBM29LV400TC and Flash Memory Control Signals

MBM29LV400TC External pins	FR-CPU mode	CY91F467EA external pins			Comment
		Flash memory mode	Normal function	Pin number	
—	INITX	—	INITX	73	
RESET	—	FRSTX	P09_6	60	
—	—	MD_2	MD_2	70	Set to '1'
—	—	MD_1	MD_1	71	Set to '1'
—	—	MD_0	MD_0	72	Set to '1'
RY/BY	FMCS:RDY bit	RY/BYX	P09_0	56	
BYTE	Internally fixed to 'H'	BYTEX	P09_2	58	
WE	Internal control signal + control via interface circuit	WEX	P13_2	191	
OE		OEX	P13_1	190	
CE		CEX	P13_0	189	
—		ATDIN	P25_7	187	Set to '0'
—		EQIN	P25_6	186	Set to '0'
—		TESTX	P09_3	59	Set to '1'
—		RDYI	P09_1	57	Set to '0'
A-1	Internal address bus	FA0	P25_5	185	Set to '0'
A0 to A3		FA1 to FA4	P27_0 to P27_3	158 to 161	
A4 to A7		FA5 to FA8	P27_4 to P27_7	164 to 167	
A8 to A11		FA9 to FA12	P26_0 to P26_3	168 to 171	
A12 to A15		FA13 to FA16	P26_4 to P26_7	174 to 177	
A16 to A19		FA17 to FA20	P25_0 to P25_3	178 to 181	
—		FA21	P25_4	184	Set to '1'
DQ0 to DQ7	Internal data bus	DQ0 to DQ7	P03_0 to P03_7	192 to 199	
DQ8 to DQ15		DQ8 to DQ15	P02_0 to P02_7	200 to 207	

14.5 Poweron Sequence in Parallel Programming Mode

The flash memory can be accessed in programming mode after a certain wait time, which is needed for Security Vector fetch:

- Minimum wait time after VDD5/VDD5R power on: 2.76 ms
- Minimum wait time after INITX rising: 1.0 ms

14.6 Flash Security

14.6.1 Vector addresses

Two Flash Security Vectors (FSV1, FSV2) are located parallel to the Boot Security Vectors (BSV1, BSV2) controlling the protection functions of the Flash Security Module:

FSV1: 0x14:8000 BSV1: 0x14:8004
FSV2: 0x14:8008 BSV2: 0x14:800C

14.6.2 Security Vector FSV1

The setting of the Flash Security Vector FSV1 is responsible for the read and write protection modes and the individual write protection of the 8 Kbytes sectors.

FSV1 (bit31 to bit16)

The setting of the Flash Security Vector FSV1 bits [31:16] is responsible for the read and write protection modes.

Table 14-5. Explanation of the bits in the Flash Security Vector FSV1 [31:16]

FSV1[31:19]	FSV1[18] Write Protection Level	FSV1[17] Write Protection	FSV1[16] Read Protection	Flash Security Mode
set all to "0"	set to "0"	set to "0"	set to "1"	Read Protection (all device modes, except INTVEC mode MD[2:0] = "000")
set all to "0"	set to "0"	set to "1"	set to "0"	Write Protection (all device modes, without exception)
set all to "0"	set to "0"	set to "1"	set to "1"	Read Protection (all device modes, except INTVEC mode MD[2:0] = "000") and Write Protection (all device modes)
set all to "0"	set to "1"	set to "0"	set to "1"	Read Protection (all device modes, except INTVEC mode MD[2:0] = "000")
set all to "0"	set to "1"	set to "1"	set to "0"	Write Protection (all device modes, except INTVEC mode MD[2:0] = "000")
set all to "0"	set to "1"	set to "1"	set to "1"	Read Protection (all device modes, except INTVEC mode MD[2:0] = "000") and Write Protection (all device modes except INTVEC mode MD[2:0] = "000")

FSV1 (bit15 to bit0)

The setting of the Flash Security Vector FSV1 bits [15:0] is responsible for the individual write protection of the 8 Kbytes sectors. It is only evaluated if write protection bit FSV1[17] is set.

Table 14-6. Explanation of the bits in the Flash Security Vector FSV1 [15:0]

FSV1 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV1[0]	SA0	set to "0"	set to "1"	
FSV1[1]	SA1	set to "0"	set to "1"	
FSV1[2]	SA2	set to "0"	set to "1"	
FSV1[3]	SA3	set to "0"	set to "1"	
FSV1[4]	SA4	set to "0"	—	Write protection is mandatory!
FSV1[5]	SA5	set to "0"	set to "1"	
FSV1[6]	SA6	set to "0"	set to "1"	
FSV1[7]	SA7	set to "0"	set to "1"	
FSV1[8]	—	set to "0"	set to "1"	not available

Table 14-6. Explanation of the bits in the Flash Security Vector FSV1 [15:0]

FSV1 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV1[9]	—	set to "0"	set to "1"	not available
FSV1[10]	—	set to "0"	set to "1"	not available
FSV1[11]	—	set to "0"	set to "1"	not available
FSV1[12]	—	set to "0"	set to "1"	not available
FSV1[13]	—	set to "0"	set to "1"	not available
FSV1[14]	—	set to "0"	set to "1"	not available
FSV1[15]	—	set to "0"	set to "1"	not available

Note: It is mandatory to always set the sector where the Flash Security Vectors FSV1 and FSV2 are located to write protected (here sector SA4). Otherwise it is possible to overwrite the Security Vector to a setting where it is possible to either read out the Flash content or manipulate data by writing.
See section "Flash access in CPU mode" for an overview about the sector organisation of the Flash Memory.

14.6.3 Security Vector FSV2

The setting of the Flash Security Vector FSV2 bits [31:0] is responsible for the individual write protection of the 64 Kbytes sectors. It is only evaluated if write protection bit FSV1 [17] is set.

Table 14-7. Explanation of the bits in the Flash Security Vector FSV2[31:0]

FSV2 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV2[0]	SA8	set to "0"	set to "1"	
FSV2[1]	SA9	set to "0"	set to "1"	
FSV2[2]	SA10	set to "0"	set to "1"	
FSV2[3]	SA11	set to "0"	set to "1"	
FSV2[4]	SA12	set to "0"	set to "1"	
FSV2[5]	SA13	set to "0"	set to "1"	
FSV2[6]	SA14	set to "0"	set to "1"	
FSV2[7]	SA15	set to "0"	set to "1"	
FSV2[8]	SA16	set to "0"	set to "1"	
FSV2[9]	SA17	set to "0"	set to "1"	
FSV2[10]	SA18	set to "0"	set to "1"	
FSV2[11]	SA19	set to "0"	set to "1"	
FSV2[12]	SA20	set to "0"	set to "1"	
FSV2[13]	SA21	set to "0"	set to "1"	
FSV2[14]	SA22	set to "0"	set to "1"	
FSV2[15]	SA23	set to "0"	set to "1"	
FSV2[31:16]	—	set to "0"	set to "1"	not available

Note: See section "Flash access in CPU mode" for an overview about the sector organisation of the Flash Memory.

15. Memory Space

The FR family has 4 Gbytes of logical address space (2^{32} addresses) available to the CPU by linear access.

■ Direct addressing area

The following address space area is used for I/O.

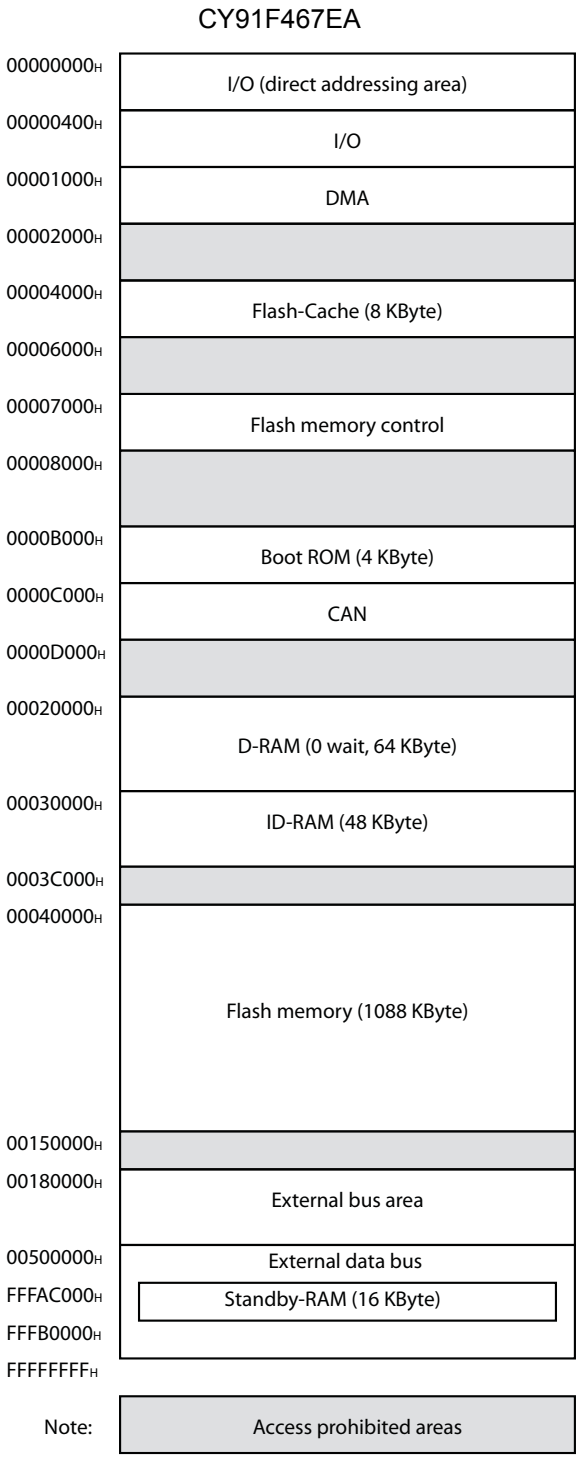
This area is called direct addressing area, and the address of an operand can be specified directly in an instruction.

The size of directly addressable area depends on the length of the data being accessed as shown below.

Byte data access:	000_H to $0FF_H$
Half word access:	000_H to $1FF_H$
Word data access:	000_H to $3FF_H$

16. Memory Maps

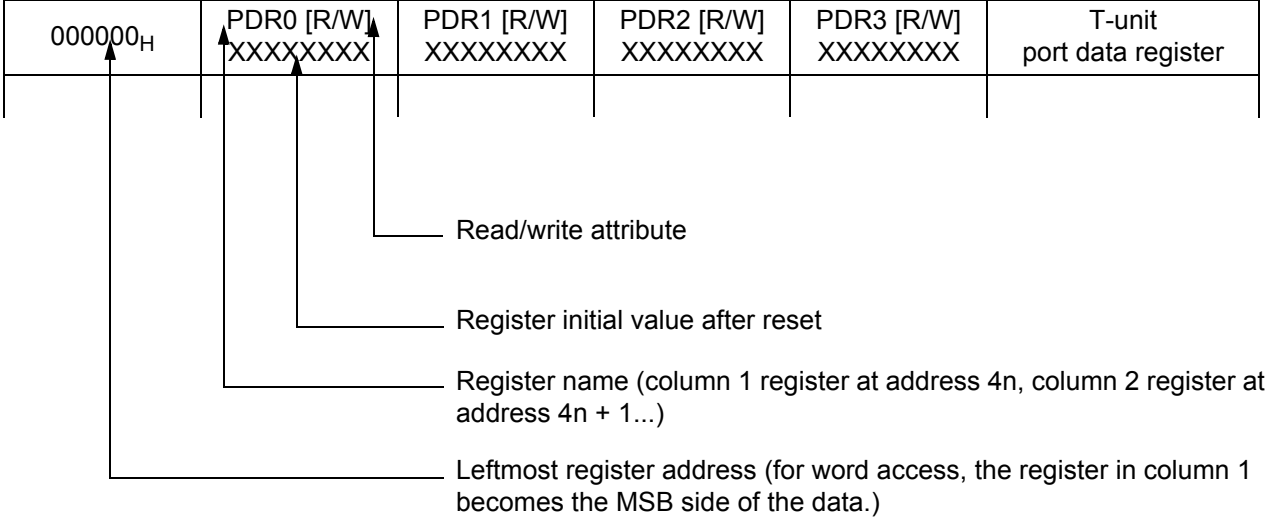
16.1 CY91F467EA



17. I/O Map

17.1 CY91F467EA

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000_H	PDR0 [R/W] XXXXXXXX	PDR1 [R/W] XXXXXXXX	PDR2 [R/W] XXXXXXXX	PDR3 [R/W] XXXXXXXX	T-unit port data register



Note: Initial values of register bits are represented as follows:

" 1 ": Initial value " 1 "
" 0 ": Initial value " 0 "
" X ": Initial value " undefined "
" - ": No physical register at this location
Access is barred with an undefined data access attribute.

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000_H	PDR00 [R/W] XXXXXXXX	PDR01 [R/W] XXXXXXXX	PDR02 [R/W] XXXXXXXX	PDR03 [R/W] XXXXXXXX	R-bus Port Data Register
000004_H	PDR04 [R/W] - - - - - - XX	PDR05 [R/W] XXXXXXXX	PDR06 [R/W] XXXXXXXX	PDR07 [R/W] XXXXXXXX	
000008_H	PDR08 [R/W] XXXXXXXX	PDR09 [R/W] XX - - XXXX	PDR10 [R/W] - XXXXXX -	Reserved	
$00000C_H$	Reserved	PDR13 [R/W] - - - - - XXX	PDR14 [R/W] XXXXXXXX	PDR15 [R/W] - - - - XXXX	
000010_H	PDR16 [R/W] XXXXXXXX	PDR17 [R/W] XXXX - - - -	PDR18 [R/W] - XXX - XXX	PDR19 [R/W] - XXX - XXX	
000014_H	PDR20 [R/W] - - - - - XXX	Reserved	PDR22 [R/W] - - XX - X - X	PDR23 [R/W] - - XXXXXX	
000018_H	PDR24 [R/W] XXXXXXXX	PDR25 [R/W] XXXXXXXX	PDR26 [R/W] XXXXXXXX	PDR27 [R/W] XXXXXXXX	
$00001C_H$	Reserved	PDR29 [R/W] XXXXXXXX	Reserved		

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000020_H to $00002C_H$	Reserved				Reserved
000030_H	EIRR0 [R/W] XXXXXXXX	ENIR0 [R/W] 00000000	ELVR0 [R/W] 00000000 00000000		External interrupt (INT 0 to INT 7)
000034_H	EIRR1 [R/W] XXXXXXXX	ENIR1 [R/W] 00000000	ELVR1 [R/W] 00000000 00000000		External interrupt (INT 8 to INT 10, INT 12 to INT 14)
000038_H	DICR [R/W] - - - - - - - 0	HRCL [R/W] 0 - - 11111	Reserved		Delay Interrupt
$00003C_H$ to $00004C_H$	Reserved				Reserved
000050_H	SCR02 [R/W, W] 00000000	SMR02 [R/W, W] 00000000	SSR02 [R/W, R] 00001000	RDR02/TDR02 [R/W] 00000000	LIN-USART 2
000054_H	ESCR02 [R/W] 00000X00	ECCR02 [R/W, R, W] -00000XX	FSR02 [RW/R] xx00 0000	Reserved	
000058_H, $00005C_H$	Reserved				Reserved
000060_H	SCR04 [R/W, W] 00000000	SMR04 [R/W, W] 00000000	SSR04 [R/W, R] 00001000	RDR04/TDR04 [R/W] 00000000	LIN-USART 4 with FIFO
000064_H	ESCR04 [R/W] 00000X00	ECCR04 [R/W, R, W] -00000XX	FSR04 [RW/R] xx00 0000	FCR04 [R/W] 0001 - 000	
000068_H	SCR05 [R/W, W] 00000000	SMR05 [R/W, W] 00000000	SSR05 [R/W, R] 00001000	RDR05/TDR05 [R/W] 00000000	LIN-USART 5 with FIFO
$00006C_H$	ESCR05 [R/W] 00000X00	ECCR05 [R/W, R, W] -00000XX	FSR05 [RW/R] xx00 0000	FCR05 [R/W] 0001 - 000	
000070_H	SCR06 [R/W, W] 00000000	SMR06 [R/W, W] 00000000	SSR06 [R/W, R] 00001000	RDR06/TDR06 [R/W] 00000000	LIN-USART 6 with FIFO
000074_H	ESCR06 [R/W] 00000X00	ECCR06 [R/W, R, W] -00000XX	FSR06 [RW/R] xx00 0000	FCR06 [R/W] 0001 - 000	
000078_H	SCR07 [R/W, W] 00000000	SMR07 [R/W, W] 00000000	SSR07 [R/W, R] 00001000	RDR07/TDR07 [R/W] 00000000	LIN-USART 7 with FIFO
$00007C_H$	ESCR07 [R/W] 00000X00	ECCR07 [R/W, R, W] -00000XX	FSR07 [RW/R] xx00 0000	FCR07 [R/W] 0001 - 000	
000080_H	Reserved				Reserved

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000084_H	BGR102 [R/W] 00000000	BGR002 [R/W] 00000000	Reserved		Baud rate Generator LIN-USART 2,4 to 7
000088_H	BGR104 [R/W] 00000000	BGR004 [R/W] 00000000	BGR105 [R/W] 00000000	BGR005 [R/W] 00000000	
$00008C_H$	BGR106 [R/W] 00000000	BGR006 [R/W] 00000000	BGR107 [R/W] 00000000	BGR007 [R/W] 00000000	
000090_H	PWC20 [R/W] - - - - - - XX XXXXXXXX		PWC10 [R/W] - - - - - - XX XXXXXXXX		Stepper Motor 0
000094_H	Reserved		PWS20 [R/W] -0000000	PWS10 [R/W] - -000000	
000098_H	PWC21 [R/W] - - - - - - XX XXXXXXXX		PWC11 [R/W] - - - - - - XX XXXXXXXX		Stepper Motor 1
$00009C_H$	Reserved		PWS21 [R/W] -0000000	PWS11 [R/W] - -000000	
$0000A0_H$	PWC22 [R/W] - - - - - - XX XXXXXXXX		PWC12 [R/W] - - - - - - XX XXXXXXXX		Stepper Motor 2
$0000A4_H$	Reserved		PWS22 [R/W] -0000000	PWS12 [R/W] - -000000	
$0000A8_H$	PWC23 [R/W] - - - - - - XX XXXXXXXX		PWC13 [R/W] - - - - - - XX XXXXXXXX		Stepper Motor 3
$0000AC_H$	Reserved		PWS23 [R/W] -0000000	PWS13 [R/W] - -000000	
$0000B0_H$	PWC24 [R/W] - - - - - - XX XXXXXXXX		PWC14 [R/W] - - - - - - XX XXXXXXXX		Stepper Motor 4
$0000B4_H$	Reserved		PWS24 [R/W] -0000000	PWS14 [R/W] - -000000	
$0000B8_H$	PWC25 [R/W] - - - - - - XX XXXXXXXX		PWC15 [R/W] - - - - - - XX XXXXXXXX		Stepper Motor 5
$0000BC_H$	Reserved		PWS25 [R/W] -0000000	PWS15 [R/W] - -000000	
$0000C0_H$	Reserved	PWC0 [R/W] -00000--	Reserved	PWC1 [R/W] -00000--	Stepper Motor Control 0 to 5
$0000C4_H$	Reserved	PWC2 [R/W] -00000--	Reserved	PWC3 [R/W] -00000--	
$0000C8_H$	Reserved	PWC4 [R/W] -00000--	Reserved	PWC5 [R/W] -00000--	
$0000CC_H$	Reserved				Reserved
$0000D0_H$	IBCR0 [R/W] 00000000	IBSR0 [R] 00000000	ITBAH0 [R/W] - - - - - - 00	ITBAL0 [R/W] 00000000	I^2C 0
$0000D4_H$	ITMKH0 [R/W] 00 - - - - 11	ITMKL0 [R/W] 11111111	ISMK0 [R/W] 01111111	ISBA0 [R/W] - 0000000	
$0000D8_H$	Reserved	IDAR0 [R/W] 00000000	ICCR0 [R/W] 00011111	Reserved	
$0000DC_H$ to 000100_H	Reserved				Reserved
000104_H	GCN11 [R/W] 00110010 00010000		Reserved	GCN21 [R/W] - - - - 0000	PPG Control 4 to 7

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000108_H	GCN12 [R/W] 00110010 00010000		Reserved	GCN22 [R/W] - - - - 0000	PPG Control 8 to 11
000110_H to $00012C_H$	Reserved				Reserved
000130_H	PTMR04 [R] 11111111 11111111		PCSR04 [R/W] XXXXXXXX XXXXXXXX		PPG 4
000134_H	PDUT04 [R/W] XXXXXXXX XXXXXXXX		PCNH04 [R/W] 0000000 -	PCNL04 [R/W] 000000 - 0	
000138_H	PTMR05 [R] 11111111 11111111		PCSR05 [R/W] XXXXXXXX XXXXXXXX		PPG 5
$00013C_H$	PDUT05 [R/W] XXXXXXXX XXXXXXXX		PCNH05 [R/W] 0000000 -	PCNL05 [R/W] 000000 - 0	
000140_H	PTMR06 [R] 11111111 11111111		PCSR06 [R/W] XXXXXXXX XXXXXXXX		PPG 6
000144_H	PDUT06 [R/W] XXXXXXXX XXXXXXXX		PCNH06 [R/W] 0000000 -	PCNL06 [R/W] 000000 - 0	
000148_H	PTMR07 [R] 11111111 11111111		PCSR07 [R/W] XXXXXXXX XXXXXXXX		PPG 7
$00014C_H$	PDUT07 [R/W] XXXXXXXX XXXXXXXX		PCNH07 [R/W] 0000000 -	PCNL07 [R/W] 000000 - 0	
000150_H	PTMR08 [R] 11111111 11111111		PCSR08 [R/W] XXXXXXXX XXXXXXXX		PPG 8
000154_H	PDUT08 [R/W] XXXXXXXX XXXXXXXX		PCNH08 [R/W] 0000000 -	PCNL08 [R/W] 000000 - 0	
000158_H	PTMR09 [R] 11111111 11111111		PCSR09 [R/W] XXXXXXXX XXXXXXXX		PPG 9
$00015C_H$	PDUT09 [R/W] XXXXXXXX XXXXXXXX		PCNH09 [R/W] 0000000 -	PCNL09 [R/W] 000000 - 0	
000160_H	PTMR10 [R] 11111111 11111111		PCSR10 [R/W] XXXXXXXX XXXXXXXX		PPG 10
000164_H	PDUT10 [R/W] XXXXXXXX XXXXXXXX		PCNH10 [R/W] 0000000 -	PCNL10 [R/W] 000000 - 0	
000168_H	PTMR11 [R] 11111111 11111111		PCSR11 [R/W] XXXXXXXX XXXXXXXX		PPG 11
$00016C_H$	PDUT11 [R/W] XXXXXXXX XXXXXXXX		PCNH11 [R/W] 0000000 -	PCNL11 [R/W] 000000 - 0	
000170_H	P0TMCSRH [R/W] - 0 - 000 - 0	P0TMCSRL [R/W] - - - 00000	P1TMCSRH [R/W] - 0 - 000 - 0	P1TMCSRL [R/W] - - - 00000	PFM
000174_H	P0TMRLR [W] XXXXXXXX XXXXXXXX		P0TMR [R] XXXXXXXX XXXXXXXX		
000178_H	P1TMRLR [W] XXXXXXXX XXXXXXXX		P1TMR [R] XXXXXXXX XXXXXXXX		
$00017C_H$	Reserved				Reserved

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000180_H	Reserved	ICS01 [R/W] 00000000	Reserved	ICS23 [R/W] 00000000	Input Capture 0 to 3
000184_H	IPCP0 [R] XXXXXXXX XXXXXXXX		IPCP1 [R] XXXXXXXX XXXXXXXX		
000188_H	IPCP2 [R] XXXXXXXX XXXXXXXX		IPCP3 [R] XXXXXXXX XXXXXXXX		
$00018C_H$	OCS01 [R/W] - - - 0 - - 00 0000 - - 00		OCS23 [R/W] - - - 0 - - 00 0000 - - 00		Output Compare 0 to 3
000190_H	OCCP0 [R/W] XXXXXXXX XXXXXXXX		OCCP1 [R/W] XXXXXXXX XXXXXXXX		
000194_H	OCCP2 [R/W] XXXXXXXX XXXXXXXX		OCCP3 [R/W] XXXXXXXX XXXXXXXX		
000198_H	SGCRH [R/W] 0000 - - 00	SGCRL [R/W] - - 0 - - 000	SGFR [R/W, R] XXXXXXXX XXXXXXXX		Sound Generator
$00019C_H$	SGAR [R/W] 00000000	Reserved	SGTR [R/W] XXXXXXXX	SGDR [R/W] XXXXXXXX	
$0001A0_H$	ADERH [R/W] 00000000 00000000		ADERL [R/W] 00000000 00000000		A/D Converter 0
0001A4	ADCS1 [R/W] 00000000	ADCS0 [R/W] 0000000**0 [R]** - - - - - - - **0 [W]**	ADCR1 [R] 000000XX	ADCR0 [R] XXXXXXXX	
$0001A8_H$	ADCT1 [R/W] 00010000	ADCT0 [R/W] 00101100	ADSCH [R/W] - - - 00000	ADECH [R/W] - - - 00000	
$0001AC_H$	Reserved	ACSR0 [R/W] - 11XXX00	Reserved		Alarm Comparator 0
$0001B0_H$	TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0
$0001B4_H$	Reserved		TMCSRH0 [R/W] - - - 00000	TMCSRL0 [R/W] 0 - 000000	
$0001B8_H$	TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		Reload Timer 1
$0001BC_H$	Reserved		TMCSRH1 [R/W] - - - 00000	TMCSRL1 [R/W] 0 - 000000	
$0001C0_H$	TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		Reload Timer 2 (PPG 4, PPG 5)
$0001C4_H$	Reserved		TMCSRH2 [R/W] - - - 00000	TMCSRL2 [R/W] 0 - 000000	
$0001C8_H$	TMRLR3 [W] XXXXXXXX XXXXXXXX		TMR3 [R] XXXXXXXX XXXXXXXX		Reload Timer 3 (PPG 6, PPG 7)
$0001CC_H$	Reserved		TMCSRH3 [R/W] - - - 00000	TMCSRL3 [R/W] 0 - 000000	

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$0001D0_H$	TMRLR4 [W] XXXXXXXX XXXXXXXX		TMR4 [R] XXXXXXXX XXXXXXXX		Reload Timer 4 (PPG 8, PPG 9)
$0001D4_H$	Reserved		TMCSRH4 [R/W] - - - 00000	TMCSRL4 [R/W] 0 - 000000	
$0001D8_H$	TMRLR5 [W] XXXXXXXX XXXXXXXX		TMR5 [R] XXXXXXXX XXXXXXXX		Reload Timer 5 (PPG 10, PPG 11)
$0001DC_H$	Reserved		TMCSRH5 [R/W] - - - 00000	TMCSRL5 [R/W] 0 - 000000	
$0001E0_H$	TMRLR6 [W] XXXXXXXX XXXXXXXX		TMR6 [R] XXXXXXXX XXXXXXXX		Reload Timer 6 (PPG 12, PPG 13)
$0001E4_H$	Reserved		TMCSRH6 [R/W] - - - 00000	TMCSRL6 [R/W] 0 - 000000	
$0001E8_H$	TMRLR7 [W] XXXXXXXX XXXXXXXX		TMR7 [R] XXXXXXXX XXXXXXXX		Reload Timer 7 (PPG 14, PPG 15) (A/D Converter)
$0001EC_H$	Reserved		TMCSRH7 [R/W] - - - 00000	TMCSRL7 [R/W] 0 - 000000	
$0001F0_H$	TCDT0 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS0 [R/W] 00000000	Free Running Timer 0 (ICU 0, ICU 1)
$0001F4_H$	TCDT1 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS1 [R/W] 00000000	Free Running Timer 1 (ICU 2, ICU 3)
$0001F8_H$	TCDT2 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS2 [R/W] 00000000	Free Running Timer 2 (OCU 0, OCU 1)
$0001FC_H$	TCDT3 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS3 [R/W] 00000000	Free Running Timer 3 (OCU 2, OCU 3)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000200_H	DMACA0 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204_H	DMACB0 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000208_H	DMACA1 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
$00020C_H$	DMACB1 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000210_H	DMACA2 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000214_H	DMACB2 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000218_H	DMACA3 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
$00021C_H$	DMACB3 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000220_H	DMACA4 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000224_H	DMACB4 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000228_H to $00023C_H$	Reserved				
000240_H	DMACR [R/W] 00 - - 0000	Reserved			
000244_H to $0002CC_H$	Reserved				Reserved
$0002D0_H$	Reserved	ICS045 [R/W] 00000000	Reserved	ICS67 [R/W] 00000000	Input Capture 4 to 7
$0002D4_H$	IPCP4 [R] XXXXXXXX XXXXXXXX		IPCP5 [R] XXXXXXXX XXXXXXXX		
$0002D8_H$	IPCP6 [R] XXXXXXXX XXXXXXXX		IPCP7 [R] XXXXXXXX XXXXXXXX		
$0002DC_H$ to $0002EC_H$	Reserved				Reserved
$0002F0_H$	TCDT4 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS4 [R/W] 00000000	Free Running Timer 4 (ICU 4, ICU 5)
$0002F4_H$	TCDT5 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS5 [R/W] 00000000	Free Running Timer 5 (ICU 6, ICU 7)
$0002F8_H$	TCDT6 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS6 [R/W] 00000000	Free Running Timer 6
$0002FC_H$	TCDT7 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS7 [R/W] 00000000	Free Running Timer 7

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000300_H	Reserved	UDRC0 [W] 00000000	Reserved	UDCR0 [R] 00000000	Up/Down Counter 0
000304_H	UDCCH0 [R/W] 00000000	UDCCL0 [R/W] 00001000	Reserved	UDCS0 [R/W] 00000000	
000308_H, $00030C_H$	Reserved				Reserved
000310_H	UDRC3 [W] 00000000	UDRC2 [W] 00000000	UDCR3 [R] 00000000	UDCR2 [R] 00000000	Up/Down Counter 2 to 3
000314_H	UDCCH2 [R/W] 00000000	UDCCL2 [R/W] 00001000	Reserved	UDCS2 [R/W] 00000000	
000318_H	UDCCH3 [R/W] 00000000	UDCCL3 [R/W] 00001000	Reserved	UDCS3 [R/W] 00000000	
$00031C_H$	Reserved				Reserved
000320_H	GCN13 [R/W] 00110010 00010000		Reserved	GCN23 [R/W] - - - - 0000	PPG Control 12 to 15
000324_H to $00032C_H$	Reserved				Reserved
000330_H	PTMR12 [R] 11111111 11111111		PCSR12 [R/W] XXXXXXXX XXXXXXXX		PPG 12
000334_H	PDUT12 [R/W] XXXXXXXX XXXXXXXX		PCNH12 [R/W] 0000000 -	PCNL12 [R/W] 000000 - 0	
000338_H	PTMR13 [R] 11111111 11111111		PCSR13 [R/W] XXXXXXXX XXXXXXXX		PPG 13
$00033C_H$	PDUT13 [R/W] XXXXXXXX XXXXXXXX		PCNH13 [R/W] 0000000 -	PCNL13 [R/W] 000000 - 0	
000340_H	PTMR14 [R] 11111111 11111111		PCSR14 [R/W] XXXXXXXX XXXXXXXX		PPG 14
000344_H	PDUT14 [R/W] XXXXXXXX XXXXXXXX		PCNH14 [R/W] 0000000 -	PCNL14 [R/W] 000000 - 0	
000348_H	PTMR15 [R] 11111111 11111111		PCSR15 [R/W] XXXXXXXX XXXXXXXX		PPG 15
$00034C_H$	PDUT15 [R/W] XXXXXXXX XXXXXXXX		PCNH15 [R/W] 0000000 -	PCNL15 [R/W] 000000 - 0	
000350_H to 000364_H	Reserved				Reserved
000368_H	IBCR2 [R/W] 00000000	IBSR2 [R] 00000000	ITBAH2 [R/W] - - - - - - 00	ITBAL2 [R/W] 00000000	I^2C 2
$00036C_H$	ITMKH2 [R/W] 00 - - - - 11	ITMKL2 [R/W] 11111111	ISMK2 [R/W] 01111111	ISBA2 [R/W] - 0000000	
000370_H	Reserved	IDAR2 [R/W] 00000000	ICCR2 [R/W] 00011111	Reserved	

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000374_H	IBCR3 [R/W] 00000000	IBSR3 [R] 00000000	ITBAH3 [R/W] - - - - - - 00	ITBAL3 [R/W] 00000000	I^2C 3
000378_H	ITMKH3 [R/W] 00 - - - - 11	ITMKL3 [R/W] 11111111	ISMK3 [R/W] 01111111	ISBA3 [R/W] - 0000000	
$00037C_H$	Reserved	IDAR3 [R/W] 00000000	ICCR3 [R/W] 00011111	Reserved	
000380_H to $00038C_H$	Reserved				Reserved
000390_H	ROMS [R] 11111111 00000000 (CY91F467EA)		Reserved		ROM Select Register
000394_H to $0003EC_H$	Reserved				Reserved
$0003F0_H$	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
$0003F4_H$	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0003F8_H$	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0003FC_H$	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400_H to $00043C_H$	Reserved				Reserved

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000440_H	ICR00 [R/W] ---11111	ICR01 [R/W] ---11111	ICR02 [R/W] ---11111	ICR03 [R/W] ---11111	Interrupt Controller
000444_H	ICR04 [R/W] ---11111	ICR05 [R/W] ---11111	ICR06 [R/W] ---11111	ICR07 [R/W] ---11111	
000448_H	ICR08 [R/W] ---11111	ICR09 [R/W] ---11111	ICR10 [R/W] ---11111	ICR11 [R/W] ---11111	
$00044C_H$	ICR12 [R/W] ---11111	ICR13 [R/W] ---11111	ICR14 [R/W] ---11111	ICR15 [R/W] ---11111	
000450_H	ICR16 [R/W] ---11111	ICR17 [R/W] ---11111	ICR18 [R/W] ---11111	ICR19 [R/W] ---11111	
000454_H	ICR20 [R/W] ---11111	ICR21 [R/W] ---11111	ICR22 [R/W] ---11111	ICR23 [R/W] ---11111	
000458_H	ICR24 [R/W] ---11111	ICR25 [R/W] ---11111	ICR26 [R/W] ---11111	ICR27 [R/W] ---11111	
$00045C_H$	ICR28 [R/W] ---11111	ICR29 [R/W] ---11111	ICR30 [R/W] ---11111	ICR31 [R/W] ---11111	
000460_H	ICR32 [R/W] ---11111	ICR33 [R/W] ---11111	ICR34 [R/W] ---11111	ICR35 [R/W] ---11111	
000464_H	ICR36 [R/W] ---11111	ICR37 [R/W] ---11111	ICR38 [R/W] ---11111	ICR39 [R/W] ---11111	
000468_H	ICR40 [R/W] ---11111	ICR41 [R/W] ---11111	ICR42 [R/W] ---11111	ICR43 [R/W] ---11111	
$00046C_H$	ICR44 [R/W] ---11111	ICR45 [R/W] ---11111	ICR46 [R/W] ---11111	ICR47 [R/W] ---11111	
000470_H	ICR48 [R/W] ---11111	ICR49 [R/W] ---11111	ICR50 [R/W] ---11111	ICR51 [R/W] ---11111	
000474_H	ICR52 [R/W] ---11111	ICR53 [R/W] ---11111	ICR54 [R/W] ---11111	ICR55 [R/W] ---11111	
000478_H	ICR56 [R/W] ---11111	ICR57 [R/W] ---11111	ICR58 [R/W] ---11111	ICR59 [R/W] ---11111	
$00047C_H$	ICR60 [R/W] ---11111	ICR61 [R/W] ---11111	ICR62 [R/W] ---11111	ICR63 [R/W] ---11111	
000480_H	RSRR [R/W] 10000000	STCR [R/W] 00110011	TBCR [R/W] 00XXX - 00	CTBR [W] XXXXXXXX	Clock Control
000484_H	CLKR [R/W] ---- 0000	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011	DIVR1 [R/W] 00000000	
000488_H	Reserved				Reserved
$00048C_H$	PLLDIVM [R/W] - - - - 0000	PLLDIVN [R/W] - - 000000	PLLDIVG [R/W] - - - - 0000	PLLMULG [W] 00000000	PLL Interface
000490_H	PLLCTRL [R/W] - - - - 0000	Reserved			
000494_H	OSCC1 [R/W] - - - - - 010	OSCS1 [R/W] 00001111	OSCC2 [R/W] - - - - - 010	OSCS2 [R/W] 00001111	Main/Sub Oscillator Control
000498_H	PORTEN [R/W] - - - - - - 00	Reserved			Port Input Enable Control
$00049C_H$	Reserved				Reserved

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0004A0$_H$	Reserved	WTCER [R/W] - - - - - - 00	WTCR [R/W] 00000000 000 - 00 - 0		Real Time Clock (Watch Timer)
0004A4$_H$	Reserved	WTBR [R/W] - - - XXXXX XXXXXXXX XXXXXXXX			
0004A8$_H$	WTHR [R/W] - - - 00000	WTMR [R/W] - - 000000	WTSR [R/W] - - 000000	Reserved	
0004AC$_H$	CSVTR [R/W] - - - 00010	CSVCR [R/W/W0] 00011100	CSCFG [R/W] 0X000000	CMCFG [R/W] 00000000	Clock-Supervisor / Selector / Monitor
0004B0$_H$	CUCR [R/W] - - - - - - - - - - - - 0 - - 00		CUTD [R/W] 10000000 00000000		Calibration of Sub Clock
0004B4$_H$	CUTR1 [R] - - - - - - - - 00000000		CUTR2 [R] 00000000 00000000		
0004B8$_H$	CMPR [R/W] - - 000010 11111101		Reserved	CMCR [R/W] - 001 - - 00	Clock Modulator
0004BC$_H$	CMT1 [R/W] 00000000 1 - - - 0000		CMT2 [R/W] - - 000000 - - 000000		
0004C0$_H$	CANPRE [R/W] 0 - - - 0000	CANCKD [R/W] - - - - - - 00 [1]	Reserved		CAN Clock Control
0004C4$_H$	LVSEL [R/W] 00000111	LVDET [R/W] 0000 0 - 00	HWWDE [R/W] - - - 0 - - 00 [2]	HWWD [R/W, W] 00011000	Low Voltage Detection/Hardware Watchdog
0004C8$_H$	OSCRH [R/W] 000 - - 001	OSCRL [R/W] - - - - - 000	WPCRH [R/W] 00 - - - 000	WPCRL [R/W] - - - - - - 00	Main-/Sub-Oscillation Stabilisation Timer
0004CC$_H$	OSCCR [R/W] - - - - - - 00 [3]	Reserved	REGSEL [R/W] - - 11 0110 [4]	REGCTR [R/W] - - - 0 - - 00	Main- Oscillation Standby Control Main-/Subregulator Control
0004D0$_H$	Reserved				Reserved
0004D4$_H$	SHDE [R/W] 0 - - - - - - 0	reserved	EXTE [R/W] 0000 0000	EXTF [R/W0] 0000 0000	Shutdown Control
0004D8$_H$	EXTLV [R/W] 0000 0000 0000 0000		reserved	SHDINT [R/W] - - - - 0000	
0004DC$_H$ to 00063C$_H$	Reserved				Reserved

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000640_H	ASR0 [R/W] 00000000 00000000		ACR0 [R/W] 1111**00 00100000 [5]		External Bus
000644_H	ASR1 [R/W] XXXXXXXX XXXXXXXX		ACR1 [R/W] XXXXXXXX XXXXXXXX		
000648_H	ASR2 [R/W] XXXXXXXX XXXXXXXX		ACR2 [R/W] XXXXXXXX XXXXXXXX		
$00064C_H$	ASR3 [R/W] XXXXXXXX XXXXXXXX		ACR3 [R/W] XXXXXXXX XXXXXXXX		
000650_H	ASR4 [R/W] XXXXXXXX XXXXXXXX		ACR4 [R/W] XXXXXXXX XXXXXXXX		
000654_H	ASR5 [R/W] XXXXXXXX XXXXXXXX		ACR5 [R/W] XXXXXXXX XXXXXXXX		
000658_H	ASR6 [R/W] XXXXXXXX XXXXXXXX		ACR6 [R/W] XXXXXXXX XXXXXXXX		
$00065C_H$	ASR7 [R/W] XXXXXXXX XXXXXXXX		ACR7 [R/W] XXXXXXXX XXXXXXXX		
000660_H	AWR0 [R/W] 01001111 11111011		AWR1 [R/W] XXXXXXXX XXXXXXXX		
000664_H	AWR2 [R/W] XXXXXXXX XXXXXXXX		AWR3 [R/W] XXXXXXXX XXXXXXXX		
000668_H	AWR4 [R/W] XXXXXXXX XXXXXXXX		AWR5 [R/W] XXXXXXXX XXXXXXXX		
$00066C_H$	AWR6 [R/W] XXXXXXXX XXXXXXXX		AWR7 [R/W] XXXXXXXX XXXXXXXX		
000670_H	MCRA [R/W] XXXXXXXX	MCRB [R/W] XXXXXXXX	Reserved		
000674_H	Reserved				
000678_H	IOWR0 [R/W] XXXXXXXX	IOWR1 [R/W] XXXXXXXX	IOWR2 [R/W] XXXXXXXX	IOWR3 [R/W] XXXXXXXX	
$00067C_H$	Reserved				
000680_H	CSER [R/W] 00000001	CHER [R/W] 11111111	Reserved	TCR [R/W] 0000**** [6]	
000684_H	RCRH [R/W] 00XXXXXX	RCRL [R/W] XXXX0XXX	Reserved		
000688_H	RCO0H0 [R/W] 11111111	RCO0L0 [R/W] 0000 0000	RCO0H1 [R/W] 1111111	RCO0L1 [R/W] 0000 0000	A/D Converter 0 Range Comparator
$00068C_H$	RCO0H2 [R/W] 1111111	RCO0L2 [R/W] 0000 0000	RCO0H3 [R/W] 1111111	RCO0L3 [R/W] 0000 0000	
000690_H	RCO0IRS [R/W] 00000000 00000000 00000000 00000000				
000694_H	RCO0OF [R] 00000000 00000000 00000000 00000000				
000698_H	RCO0INT [R/W0] 00000000 00000000 00000000 00000000				
$00069C_H$	reserved				

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0006A0$_H$	AD0CC0 [R/W] 0000 0000	AD0CC1 [R/W] 0000 0000	AD0CC2 [R/W] 0000 0000	AD0CC3 [R/W] 0000 0000	A/D Converter 0 Channel Control
0006A4$_H$	AD0CC4 [R/W] 0000 0000	AD0CC5 [R/W] 0000 0000	AD0CC6 [R/W] 0000 0000	AD0CC7 [R/W] 0000 0000	
0006A8$_H$	AD0CC8 [R/W] 0000 0000	AD0CC9 [R/W] 0000 0000	AD0CC10 [R/W] 0000 0000	AD0CC11 [R/W] 0000 0000	
0006AC$_H$	AD0CC12 [R/W] 0000 0000	AD0CC13 [R/W] 0000 0000	AD0CC14 [R/W] 0000 0000	AD0CC15 [R/W] 0000 0000	
0006B0$_H$	AD0CS2 [RW] 0000 - - 00	reserved			A/D Converter 0 Control register 2
0006B4$_H$ to 0006DC$_H$	Reserved				
0006E0$_H$	ADC0D0 [R] - - - - - - XX XXXXXXXX		ADC0D1 [R] - - - - - - XX XXXXXXXX		A/D Converter 0 Channel Data registers
0006E4$_H$	ADC0D2 [R] - - - - - - XX XXXXXXXX		ADC0D3 [R] - - - - - - XX XXXXXXXX		
0006E8$_H$	ADC0D4 [R] - - - - - - XX XXXXXXXX		ADC0D5 [R] - - - - - - XX XXXXXXXX		
0006EC$_H$	ADC0D6 [R] - - - - - - XX XXXXXXXX		ADC0D7 [R] - - - - - - XX XXXXXXXX		
0006F0$_H$	ADC0D8 [R] - - - - - - XX XXXXXXXX		ADC0D9 [R] - - - - - - XX XXXXXXXX		
0006F4$_H$	ADC0D10 [R] - - - - - - XX XXXXXXXX		ADC0D11 [R] - - - - - - XX XXXXXXXX		
0006F8$_H$	ADC0D12 [R] - - - - - - XX XXXXXXXX		ADC0D13 [R] - - - - - - XX XXXXXXXX		
0006FC$_H$	ADC0D14 [R] - - - - - - XX XXXXXXXX		ADC0D015 [R] - - - - - - XX XXXXXXXX		
000700$_H$	ADC0D16 [R] - - - - - - XX XXXXXXXX		ADC0D17 [R] - - - - - - XX XXXXXXXX		
000704$_H$	ADC0D18 [R] - - - - - - XX XXXXXXXX		ADC0D19 [R] - - - - - - XX XXXXXXXX		A/D Converter 0 Channel Data registers
000708$_H$	ADC0D20 [R] - - - - - - XX XXXXXXXX		ADC0D21 [R] - - - - - - XX XXXXXXXX		
00070C$_H$	ADC0D22 [R] - - - - - - XX XXXXXXXX		ADC0D23 [R] - - - - - - XX XXXXXXXX		
000710$_H$	ADC0D24 [R] - - - - - - XX XXXXXXXX		ADC0D25 [R] - - - - - - XX XXXXXXXX		
000714$_H$	ADC0D26 [R] - - - - - - XX XXXXXXXX		ADC0D27 [R] - - - - - - XX XXXXXXXX		
000718$_H$	ADC0D28 [R] - - - - - - XX XXXXXXXX		ADC0D29 [R] - - - - - - XX XXXXXXXX		
00071C$_H$	ADC0D30 [R] - - - - - - XX XXXXXXXX		ADC0D31 [R] - - - - - - XX XXXXXXXX		
000720$_H$ to 0007F8$_H$	Reserved				

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0007FC$_H$	Reserved	MODR [W] XXXXXXXX	Reserved		Mode Register
000800$_H$ to 000CFC$_H$	Reserved				Reserved
000D00$_H$	PDRD00 [R] XXXXXXXX	PDRD01 [R] XXXXXXXX	PDRD02 [R] XXXXXXXX	PDRD03 [R] XXXXXXXX	R-bus Port Data Direct Read Register
000D04$_H$	PDRD04 [R] - - - - - - XX	PDRD05 [R] XXXXXXXX	PDRD06 [R] XXXXXXXX	PDRD07 [R] XXXXXXXX	
000D08$_H$	PDRD08 [R] XXXXXXXX	PDRD09 [R] XX - - XXXX	PDRD10 [R] - XXXXXX -	Reserved	
000D0C$_H$	Reserved	PDRD13 [R] - - - - - XXX	PDRD14 [R] XXXXXXXX	PDRD15 [R] - - - - XXXX	
000D10$_H$	PDRD16 [R] XXXXXXXX	PDRD17 [R] XXXX - - - -	PDRD18 [R] - XXX - XXX	PDRD19 [R] - XXX - XXX	
000D14$_H$	PDRD20 [R] - - - - - XXX	Reserved	PDRD22 [R] - - XX - X - X	PDRD23 [R] - - XXXXXX	
000D18$_H$	PDRD24 [R] XXXXXXXX	PDRD25 [R] XXXXXXXX	PDRD26 [R] XXXXXXXX	PDRD27 [R] XXXXXXXX	
000D1C$_H$	Reserved	PDRD29 [R] XXXXXXXX	Reserved		
000D20$_H$ to 000D3C$_H$	Reserved				Reserved
000D40$_H$	DDR00 [R/W] 00000000	DDR01 [R/W] 00000000	DDR02 [R/W] 00000000	DDR03 [R/W] 00000000	R-bus Port Direction Register
000D44$_H$	DDR04 [R/W] - - - - - - 00	DDR05 [R/W] 00000000	DDR06 [R/W] 00000000	DDR07 [R/W] 00000000	
000D48$_H$	DDR08 [R/W] 00000000	DDR09 [R/W] 00 - - 0000	DDR10 [R/W] - 000000 -	Reserved	
000D4C$_H$	Reserved	DDR13 [R/W] - - - - - 000	DDR14 [R/W] 00000000	DDR15 [R/W] - - - - 0000	
000D50$_H$	DDR16 [R/W] 00000000	DDR17 [R/W] 0000 - - - -	DDR18 [R/W] - 000 - 000	DDR19 [R/W] - 000 - 000	
000D54$_H$	DDR20 [R/W] - - - - - 000	Reserved	DDR22 [R/W] - - 00 - 0 - 0	DDR23 [R/W] - - 000000	
000D58$_H$	DDR24 [R/W] 00000000	DDR25 [R/W] 00000000	DDR26 [R/W] 00000000	DDR27 [R/W] 00000000	
000D5C$_H$	Reserved	DDR29 [R/W] 00000000	Reserved		
000D60$_H$ to 000D7C$_H$	Reserved				Reserved

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000D80$_H$	PFR00 [R/W] 00000000 7	PFR01 [R/W] 00000000 7	PFR02 [R/W] 00000000 7	PFR03 [R/W] 00000000 7	R-bus Port Function Register
000D84$_H$	PFR04 [R/W] - - - - - - 00 7	PFR05 [R/W] 00000000 7	PFR06 [R/W] 00000000 7	PFR07 [R/W] 00000000 7	
000D88$_H$	PFR08 [R/W] 00000000 7	PFR09 [R/W] 00 - - 0000 7	PFR10 [R/W] - 000 000 - 7	Reserved	
000D8C$_H$	Reserved	PFR13 [R/W] - - - - - 000 7	PFR14 [R/W] 00000000	PFR15 [R/W] - - - - 0000	
000D90$_H$	PFR16 [R/W] 00000000	PFR17 [R/W] 0000 - - - -	PFR18 [R/W] - 000 - 000	PFR19 [R/W] - 000 - 000	
000D94$_H$	PFR20 [R/W] - - - - - 000	Reserved	PFR22 [R/W] - - 00 - 0 - 0	PFR23 [R/W] - - 000000	
000D98$_H$	PFR24 [R/W] 00000000	PFR25 [R/W] 00000000	PFR26 [R/W] 00000000	PFR27 [R/W] 00000000	
000D9C$_H$	Reserved	PFR29 [R/W] 00000000	Reserved		
000DA0$_H$ to 000DBC$_H$	Reserved				Reserved
000DC0$_H$	EPFR00 [R/W] - - - - - - - -	EPFR01 [R/W] - - - - - - - -	EPFR02 [R/W] - - - - - - - -	EPFR03 [R/W] - - - - - - - -	R-bus Extra Port Function Register
000DC4$_H$	EPFR04 [R/W] - - - - - - - -	EPFR05 [R/W] - - - - - - - -	EPFR06 [R/W] - - - - - - - -	EPFR07 [R/W] - - - - - - - -	
000DC8$_H$	EPFR08 [R/W] - - - - - - - -	EPFR09 [R/W] - - - - - - - -	EPFR10 [R/W] - - 00 - - - -	Reserved	
000DCC$_H$	Reserved	EPFR13 [R/W] - - - - - 0 - -	EPFR14 [R/W] 00000000	EPFR15 [R/W] - - - - 0000	
000DD0$_H$	EPFR16 [R/W] 0000 - - - -	EPFR17 [R/W] - - - - - - - -	EPFR18 [R/W] - 00 - - 00 -	EPFR19 [R/W] - 0 - - - 0 - -	
000DD4$_H$	EPFR20 [R/W] - - - - - 00 -	Reserved	EPFR22 [R/W] - - - - - - - -	EPFR23 [R/W] - - - - - - - -	
000DD8$_H$	EPFR24 [R/W] - - - - - - - -	EPFR25 [R/W] - - - - - - - -	EPFR26 [R/W] 00000000	EPFR27 [R/W] 00000000	
000DDC$_H$	Reserved	EPFR29 [R/W] - - - - - - - -	Reserved		
000DE0$_H$ to 000DFC$_H$	Reserved				Reserved

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$000E00_H$	PODR00 [R/W] 00000000	PODR01 [R/W] 00000000	PODR02 [R/W] 00000000	PODR03 [R/W] 00000000	R-bus Port Output Drive Select Register
$000E04_H$	PODR04 [R/W] - - - - - - 00	PODR05 [R/W] 00000000	PODR06 [R/W] 00000000	PODR07 [R/W] 00000000	
$000E08_H$	PODR08 [R/W] 00000000	PODR09 [R/W] 00 - - 0000	PODR10 [R/W] - 000000 -	Reserved	
$000E0C_H$	Reserved	PODR13 [R/W] - - - - - 000	PODR14 [R/W] 00000000	PODR15 [R/W] - - - - 0000	
$000E10_H$	PODR16 [R/W] 00000000	PODR17 [R/W] 0000 - - - -	PODR18 [R/W] - 000 - 000	PODR19 [R/W] - 000 - 000	
$000E14_H$	PODR20 [R/W] - - - - - 000	Reserved	PODR22 [R/W] - - 00 - 0 - 0	PODR23 [R/W] - - 000000	
$000E18_H$	PODR24 [R/W] 00000000	PODR25 [R/W] 00000000	PODR26 [R/W] 00000000	PODR27 [R/W] 00000000	
$000E1C_H$	Reserved	PODR29 [R/W] 00000000	Reserved		
$000E20_H$ to $000E3C_H$	Reserved				Reserved
$000E40_H$	PILR00 [R/W] 00000000	PILR01 [R/W] 00000000	PILR02 [R/W] 00000000	PILR03 [R/W] 00000000	R-bus Port Input Level Select Register
$000E44_H$	PILR04 [R/W] - - - - - - 00	PILR05 [R/W] 00000000	PILR06 [R/W] 00000000	PILR07 [R/W] 00000000	
$000E48_H$	PILR08 [R/W] 00000000	PILR09 [R/W] 00 - - 0000	PILR10 [R/W] - 000000 -	Reserved	
$000E4C_H$	Reserved	PILR13 [R/W] - - - - - 000	PILR14 [R/W] 00000000	PILR15 [R/W] - - - - 0000	
$000E50_H$	PILR16 [R/W] 00000000	PILR17 [R/W] 0000 - - - -	PILR18 [R/W] - 000 - 000	PILR19 [R/W] - 000 - 000	
$000E54_H$	PILR20 [R/W] - - - - - 000	Reserved	PILR22 [R/W] - - 00 - 0 - 0	PILR23 [R/W] - - 000000	
$000E58_H$	PILR24 [R/W] 00000000	PILR25 [R/W] 00000000	PILR26 [R/W] 00000000	PILR27 [R/W] 00000000	
$000E5C_H$	Reserved	PILR29 [R/W] 00000000	Reserved		
$000E60_H$ to $000E7C_H$	Reserved				Reserved

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$000E80_H$	EPILR00 [R/W] 00000000	EPILR01 [R/W] 00000000	EPILR02 [R/W] 00000000	EPILR03 [R/W] 00000000	R-bus Extra Port Input Level Select Register
$000E84_H$	EPILR04 [R/W] - - - - - - 00	EPILR05 [R/W] 00000000	EPILR06 [R/W] 00000000	EPILR07 [R/W] 00000000	
$000E88_H$	EPILR08 [R/W] 00000000	EPILR09 [R/W] 00 - - 0000	EPILR10 [R/W] - 000000 -	Reserved	
$000E8C_H$	Reserved	EPILR13 [R/W] - - - - - 000	EPILR14 [R/W] 00000000	EPILR15 [R/W] - - - - 0000	
$000E90_H$	EPILR16 [R/W] 00000000	EPILR17 [R/W] 0000 - - - -	EPILR18 [R/W] - 000 - 000	EPILR19 [R/W] - 000 - 000	
$000E94_H$	EPILR20 [R/W] - - - - - 000	Reserved	EPILR22 [R/W] - - 00 - 0 - 0	EPILR23 [R/W] - - 000000	
$000E98_H$	EPILR24 [R/W] 00000000	EPILR25 [R/W] 00000000	EPILR26 [R/W] 00000000	EPILR27 [R/W] 00000000	
$000E9C_H$	Reserved	EPILR29 [R/W] 00000000	Reserved		
$000EA0_H$ to $000EBC_H$	Reserved				Reserved
$000EC0_H$	PPER00 [R/W] 00000000	PPER01 [R/W] 00000000	PPER02 [R/W] 00000000	PPER03 [R/W] 00000000	R-bus Port Pull-Up/Down Enable Register
$000EC4_H$	PPER04 [R/W] - - - - - - 00	PPER05 [R/W] 00000000	PPER06 [R/W] 00000000	PPER07 [R/W] 00000000	
$000EC8_H$	PPER08 [R/W] 00000000	PPER09 [R/W] 00 - - 0000	PPER10 [R/W] - 000000 -	Reserved	
$000ECC_H$	Reserved	PPER13 [R/W] - - - - - 000	PPER14 [R/W] 00000000	PPER15 [R/W] - - - - 0000	
$000ED0_H$	PPER16 [R/W] 00000000	PPER17 [R/W] 0000 - - - -	PPER18 [R/W] - 000 - 000	PPER19 [R/W] - 000 - 000	
$000ED4_H$	PPER20 [R/W] - - - - - 000	Reserved	PPER22 [R/W] - - 00 - 0 - 0	PPER23 [R/W] - - 000000	
$000ED8_H$	PPER24 [R/W] 00000000	PPER25 [R/W] 00000000	PPER26 [R/W] 00000000	PPER27 [R/W] 00000000	
$000EDC_H$	Reserved	PPER29 [R/W] 00000000	Reserved		
$000EE0_H$ to $000EFC_H$	Reserved				Reserved

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$000F00_H$	PPCR00 [R/W] 11111111	PPCR01 [R/W] 11111111	PPCR02 [R/W] 11111111	PPCR03 [R/W] 11111111	R-bus Port Pull-Up/Down Control Register
$000F04_H$	PPCR04 [R/W] - - - - - - 11	PPCR05 [R/W] 11111111	PPCR06 [R/W] 11111111	PPCR07 [R/W] 11111111	
$000F08_H$	PPCR08 [R/W] 11111111	PPCR09 [R/W] 11 - - 1111	PPCR10 [R/W] - 111111 -	Reserved	
$000F0C_H$	Reserved	PPCR13 [R/W] - - - - - 111	PPCR14 [R/W] 11111111	PPCR15 [R/W] - - - - 1111	
$000F10_H$	PPCR16 [R/W] 11111111	PPCR17 [R/W] 1111 - - - -	PPCR18 [R/W] - 111 - 111	PPCR19 [R/W] - 111 - 111	
$000F14_H$	PPCR20 [R/W] - - - - - 111	Reserved	PPCR22 [R/W] - - 11 - 1 - 1	PPCR23 [R/W] - - 111111	
$000F18_H$	PPCR24 [R/W] 11111111	PPCR25 [R/W] 11111111	PPCR26 [R/W] 11111111	PPCR27 [R/W] 11111111	
$000F1C_H$	Reserved	PPCR29 [R/W] 11111111	Reserved		
$000F20_H$ to $000F3C_H$	Reserved				Reserved
001000_H	DMASA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004_H	DMADA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008_H	DMASA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00100C_H$	DMADA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010_H	DMASA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014_H	DMADA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018_H	DMASA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00101C_H$	DMADA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020_H	DMASA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024_H	DMADA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001028_H to $001FFC_H$	Reserved				Reserved
002000_H to $006FFC_H$	CY91F467EA Flash-cache size is 8 Kbytes: 004000_H to $005FFC_H$				Flash-cache / I-RAM area

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
007000_H	FMCS [R/W] 01101000	FMCR [R] - - - 00000	FCHCR [R/W] - - - - - - 00 10000011		Flash Memory/ Flash-cache/ I-RAM Control Register
007004_H	FMWT [R/W] 11111111 11111111		FMWT2 [R] - 001 - - - -	FMPS [R/W] - - - - - 000	
007008_H	FMAC [R] 00000000 00000000 00000000 00000000				
$00700C_H$	FCHA0 [R/W] - - - - - - - - - - - 00000 00000000 00000000				Flash-cache Non-cacheable area setting Register
007010_H	FCHA1 [R/W] - - - - - - - - - - - 00000 00000000 00000000				
007014_H to $007FFC_H$	Reserved				Reserved
008000_H to $00BFFC_H$	CY91F467EA Boot-ROM size is 4 Kbytes: $00B000_H$ to $00BFFC_H$ (instruction access is 1 wait cycle, data access is 1 wait cycle)				Boot ROM area
$00C000_H$	CTRLR0 [R/W] 00000000 00000001		STATR0 [R/W] 00000000 00000000		CAN 0 Control Register
$00C004_H$	ERRCNT0 [R] 00000000 00000000		BTR0 [R/W] 00100011 00000001		
$00C008_H$	INTR0 [R] 00000000 00000000		TESTR0 [R/W] 00000000 X0000000		
$00C00C_H$	BRPE0 [R/W] 00000000 00000000		Reserved		
$00C010_H$	IF1CREQ0 [R/W] 00000000 00000001		IF1CMSK0 [R/W] 00000000 00000000		CAN 0 IF 1 Register
$00C014_H$	IF1MSK20 [R/W] 11111111 11111111		IF1MSK10 [R/W] 11111111 11111111		
$00C018_H$	IF1ARB20 [R/W] 00000000 00000000		IF1ARB10 [R/W] 00000000 00000000		
$00C01C_H$	IF1MCTR0 [R/W] 00000000 00000000		Reserved		
$00C020_H$	IF1DTA10 [R/W] 00000000 00000000		IF1DTA20 [R/W] 00000000 00000000		CAN 0 IF 1 Register
$00C024_H$	IF1DTB10 [R/W] 00000000 00000000		IF1DTB20 [R/W] 00000000 00000000		
$00C028_H$, $00C02C_H$	Reserved				
$00C030_H$	IF1DTA20 [R/W] 00000000 00000000		IF1DTA10 [R/W] 00000000 00000000		
$00C034_H$	IF1DTB20 [R/W] 00000000 00000000		IF1DTB10 [R/W] 00000000 00000000		
$00C038_H$, $00C03C_H$	Reserved				

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$00C040_H$	IF2CREQ0 [R/W] 00000000 00000001		IF2CMSK0 [R/W] 00000000 00000000		CAN 0 IF 2 Register
$00C044_H$	IF2MSK20 [R/W] 11111111 11111111		IF2MSK10 [R/W] 11111111 11111111		
$00C048_H$	IF2ARB20 [R/W] 00000000 00000000		IF2ARB10 [R/W] 00000000 00000000		
$00C04C_H$	IF2MCTR0 [R/W] 00000000 00000000		Reserved		
$00C050_H$	IF2DTA10 [R/W] 00000000 00000000		IF2DTA20 [R/W] 00000000 00000000		
$00C054_H$	IF2DTB10 [R/W] 00000000 00000000		IF2DTB20 [R/W] 00000000 00000000		
$00C058_H$, $00C05C_H$	Reserved				
$00C060_H$	IF2DTA20 [R/W] 00000000 00000000		IF2DTA10 [R/W] 00000000 00000000		
$00C064_H$	IF2DTB20 [R/W] 00000000 00000000		IF2DTB10 [R/W] 00000000 00000000		
$00C068_H$ to $00C07C_H$	Reserved				
$00C080_H$	TREQR20 [R] 00000000 00000000		TREQR10 [R] 00000000 00000000		CAN 0 Status Flags
$00C084_H$ to $00C08C_H$	Reserved				
$00C090_H$	NEWDT20 [R] 00000000 00000000		NEWDT10 [R] 00000000 00000000		
$00C094_H$ to $00C09C_H$	Reserved				
$00C0A0_H$	INTPND20 [R] 00000000 00000000		INTPND10 [R] 00000000 00000000		
$00C0A4_H$ to $00C0AC_H$	Reserved				
$00C0B0_H$	MSGVAL20 [R] 00000000 00000000		MSGVAL10 [R] 00000000 00000000		
$00C0B4_H$ to $00C0FC_H$	Reserved				Reserved
$00C100_H$	CTRLR1 [R/W] 00000000 00000001		STATR1 [R/W] 00000000 00000000		CAN 1 Control Register
$00C104_H$	ERRCNT1 [R] 00000000 00000000		BTR1 [R/W] 00100011 00000001		
$00C108_H$	INTR1 [R] 00000000 00000000		TESTR1 [R/W] 00000000 X0000000		
$00C10C_H$	BRPE1 [R/W] 00000000 00000000		Reserved		

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$00C110_H$	IF1CREQ1 [R/W] 00000000 00000001		IF1CMSK1 [R/W] 00000000 00000000		CAN 1 IF 1 Register
$00C114_H$	IF1MSK21 [R/W] 11111111 11111111		IF1MSK11 [R/W] 11111111 11111111		
$00C118_H$	IF1ARB21 [R/W] 00000000 00000000		IF1ARB11 [R/W] 00000000 00000000		
$00C11C_H$	IF1MCTR1 [R/W] 00000000 00000000		Reserved		
$00C120_H$	IF1DTA11 [R/W] 00000000 00000000		IF1DTA21 [R/W] 00000000 00000000		
$00C124_H$	IF1DTB11 [R/W] 00000000 00000000		IF1DTB21 [R/W] 00000000 00000000		
$00C128_H$, $00C12C_H$	Reserved				CAN 1 IF 1 Register
$00C130_H$	IF1DTA21 [R/W] 00000000 00000000		IF1DTA11 [R/W] 00000000 00000000		
$00C134_H$	IF1DTB21 [R/W] 00000000 00000000		IF1DTB11 [R/W] 00000000 00000000		
$00C138_H$, $00C13C_H$	Reserved				
$00C140_H$	IF2CREQ1 [R/W] 00000000 00000001		IF2CMSK1 [R/W] 00000000 00000000		CAN 1 IF 2 Register
$00C144_H$	IF2MSK21 [R/W] 11111111 11111111		IF2MSK11 [R/W] 11111111 11111111		
$00C148_H$	IF2ARB21 [R/W] 00000000 00000000		IF2ARB11 [R/W] 00000000 00000000		
$00C14C_H$	IF2MCTR1 [R/W] 00000000 00000000		Reserved		
$00C150_H$	IF2DTA11 [R/W] 00000000 00000000		IF2DTA21 [R/W] 00000000 00000000		
$00C154_H$	IF2DTB11 [R/W] 00000000 00000000		IF2DTB21 [R/W] 00000000 00000000		
$00C158_H$, $00C15C_H$	Reserved				
$00C160_H$	IF2DTA21 [R/W] 00000000 00000000		IF2DTA11 [R/W] 00000000 00000000		
$00C164_H$	IF2DTB21 [R/W] 00000000 00000000		IF2DTB11 [R/W] 00000000 00000000		
$00C168_H$ to $00C17C_H$	Reserved				

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$00C180_H$	TREQR21 [R] 00000000 00000000		TREQR11 [R] 00000000 00000000		CAN 1 Status Flags
$00C184_H$ to $00C18C_H$	Reserved				
$00C190_H$	NEWDT21 [R] 00000000 00000000		NEWDT11 [R] 00000000 00000000		
$00C194_H$ to $00C19C_H$	Reserved				
$00C1A0_H$	INTPND21 [R] 00000000 00000000		INTPND11 [R] 00000000 00000000		CAN 1 Status Flags
$00C1A4_H$ to $00C1AC_H$	Reserved				
$00C1B0_H$	MSGVAL21 [R] 00000000 00000000		MSGVAL11 [R] 00000000 00000000		
$00C1B4_H$ to $00C1FC_H$	Reserved				
$00C200_H$ to $00EFFC_H$	Reserved				Resedved
$00F000_H$	BCTRL [R/W] -------- -------- 11111100 00000000				EDSU / MPU
$00F004_H$	BSTAT [R/W] -------- -----000 00000000 10--0000				
$00F008_H$	BIAC [R] -------- -------- 00000000 00000000				
$00F00C_H$	BOAC [R] -------- -------- 00000000 00000000				
$00F010_H$	BIRQ [R/W] -------- -------- 00000000 00000000				
$00F014_H$ to $00F01C_H$	Reserved				
$00F020_H$	BCR0 [R/W] -------- 00000000 00000000 00000000				
$00F024_H$	BCR1 [R/W] -------- 00000000 00000000 00000000				
$00F028_H$	BCR2 [R/W] -------- 00000000 00000000 00000000				
$00F02C_H$	BCR3 [R/W] -------- 00000000 00000000 00000000				
$00F030_H$ to $00F07C_H$	Reserved				Reserved

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$00F080_H$	BAD0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				EDSU / MPU
$00F084_H$	BAD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F088_H$	BAD2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F08C_H$	BAD3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F090_H$	BAD4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F094_H$	BAD5 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F098_H$	BAD6 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F09C_H$	BAD7 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				EDSU / MPU
$00F0A0_H$	BAD8 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0A4_H$	BAD9 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0A8_H$	BAD10 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0AC_H$	BAD11 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0B0_H$	BAD12 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0B4_H$	BAD13 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0B8_H$	BAD14 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0BC_H$	BAD15 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0C0_H$ to $01FFFC_H$	Reserved				Reserved
020000_H to $02FFFC_H$	CY91F467EA D-RAM size is 64 Kbytes: 020000_H to $02FFFC_H$ (data access is 0 wait cycles)				D-RAM area
030000_H to $03FFFC_H$	CY91F467EA ID-RAM size is 48 Kbytes: 030000_H to $03BFFC_H$ (instruction access is 0 wait cycles, data access is 1 wait cycle)				ID-RAM area

1. Depends on the number of available CAN channels.
2. HWWDE[4] is STP_RUN, see "Hardware Watchdog (Extension)" on page 46
3. OSCCR[1] is OSCDS2, see CY91460 series hardware manual
4. Main regulator default is 1.9 V, sub regulator 1.8 V (CY91F467D regulator defaults are 1.8 V/1.6 V)
5. ACR0 [11 : 10] depends on bus width setting in Mode vector fetch information.
6. TCR [3 : 0] INIT value = 0000, keeps value after RST
7. In internal vector fetch mode (MD[2:0]=000) PFR00 to PFR13 are initialized to 0x00 for GPIO mode.
   In external vector fetch mode (MD[2:0]=001) PFR00 to PFR13 are initialized to 0xFF to enable the external bus.

17.2 Flash Memory and External Bus Area

32bit read/write	dat[31:0]				dat[31:0]				
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
Address	Register								Block
	+ 0	+ 1	+ 2	+ 3	+ 4	+ 5	+ 6	+ 7	
040000_H to $05FFF8_H$	SA8 (64KB)				SA9 (64KB)				ROMS0
060000_H to $07FFF8_H$	SA10 (64KB)				SA11 (64KB)				ROMS1
080000_H to $09FFF8_H$	SA12 (64KB)				SA13 (64KB)				ROMS2
$0A0000_H$ to $0BFFF8_H$	SA14 (64KB)				SA15 (64KB)				ROMS3
$0C0000_H$ to $0DFFF8_H$	SA16 (64KB)				SA17 (64KB)				ROMS4
$0E0000_H$ to $0FFFF0_H$	SA18 (64KB)				SA19 (64KB)				ROMS5
$0FFFF8_H$	FMV [R] [1] $06\ 00\ 00\ 00_H$				FRV [R] [2] $00\ 00\ BF\ F8_H$				
100000_H to $11FFF8_H$	SA20 (64KB)				SA21 (64KB)				ROMS6
120000_H to $13FFF8_H$	SA22 (64KB)				SA23 (64KB)				
140000_H to $143FF8_H$	SA0 (8KB)				SA1 (8KB)				ROMS7
144000_H to $147FF8_H$	SA2 (8KB)				SA3 (8KB)				
148000_H to $14BFF8_H$	SA4 (8KB)				SA5 (8KB)				
$14C000_H$ to $14FFF8_H$	SA6 (8KB)				SA7 (8KB)				
150000_H to $17FFF8_H$	Reserved								

32bit read/write	dat[31:0]				dat[31:0]				
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
Address	Register								Block
	+ 0	+ 1	+ 2	+ 3	+ 4	+ 5	+ 6	+ 7	
180000_H to $1BFFF8_H$	External Bus Area								ROMS8
$1C0000_H$ to $1FFFF8_H$									ROMS9
200000_H to $27FFF8_H$									ROMS10
280000_H to $2FFFF8_H$									ROMS11
300000_H to $37FFF8_H$									ROMS12
380000_H to $3FFFF8_H$									ROMS13
400000_H to $47FFF8_H$									ROMS14
480000_H to $4FFFF8_H$									ROMS15
500000_H to $FFFABFF8_H$	External Bus Area								
$FFFAC000_H$ to $FFFAFFF8_H$	CY91F467EA Standby-RAM 16 KBytes (1 wait cycle)								Standby RAM
$FFFB0000_H$ to $FFFFFFF8_H$	External Bus Area								

1. Write operations to address $0FFFF8_H$ is not possible. When reading these addresses, the values shown above will be read.
2. Write operations to address $0FFFFC_H$ is not possible. When reading these addresses, the values shown above will be read.

18. Interrupt Vector Table

Interrupt	Interrupt number		Interrupt level [1]		Interrupt vector [2]		DMA Resource number
	Deci-mal	Hexa-de cimal	Setting Register	Register address	Offset	Default Vector address	
Reset	0	00	—	—	$3FC_H$	$000FFFFC_H$	—
Mode vector	1	01	—	—	$3F8_H$	$000FFFF8_H$	—
System reserved	2	02	—	—	$3F4_H$	$000FFFF4_H$	—
System reserved	3	03	—	—	$3F0_H$	$000FFFF0_H$	—
System reserved	4	04	—	—	$3EC_H$	$000FFFEC_H$	—
CPU supervisor mode (INT #5 instruction) [3]	5	05	—	—	$3E8_H$	$000FFFE8_H$	—
Memory Protection exception [3]	6	06	—	—	$3E4_H$	$000FFFE4_H$	—
System reserved	7	07	—	—	$3E0_H$	$000FFFE0_H$	—
System reserved	8	08	—	—	$3DC_H$	$000FFFDC_H$	—
System reserved	9	09	—	—	$3D8_H$	$000FFFD8_H$	—
System reserved	10	0A	—	—	$3D4_H$	$000FFFD4_H$	—
System reserved	11	0B	—	—	$3D0_H$	$000FFFD0_H$	—
System reserved	12	0C	—	—	$3CC_H$	$000FFFCC_H$	—
System reserved	13	0D	—	—	$3C8_H$	$000FFFC8_H$	—
Undefined instruction exception	14	0E	—	—	$3C4_H$	$000FFFC4_H$	—
NMI request	15	0F	F_H fixed		$3C0_H$	$000FFFC0_H$	—
External Interrupt 0	16	10	ICR00	440_H	$3BC_H$	$000FFFBC_H$	0, 16
External Interrupt 1	17	11			$3B8_H$	$000FFFB8_H$	1, 17
External Interrupt 2	18	12	ICR01	441_H	$3B4_H$	$000FFFB4_H$	2, 18
External Interrupt 3	19	13			$3B0_H$	$000FFFB0_H$	3, 19
External Interrupt 4	20	14	ICR02	442_H	$3AC_H$	$000FFFAC_H$	20
External Interrupt 5	21	15			$3A8_H$	$000FFFA8_H$	21
External Interrupt 6	22	16	ICR03	443_H	$3A4_H$	$000FFFA4_H$	22
External Interrupt 7	23	17			$3A0_H$	$000FFFA0_H$	23
External Interrupt 8	24	18	ICR04	444_H	$39C_H$	$000FFF9C_H$	—
External Interrupt 9	25	19			398_H	$000FFF98_H$	—
External Interrupt 10	26	1A	ICR05	445_H	394_H	$000FFF94_H$	—
Reserved	27	1B			390_H	$000FFF90_H$	—
External Interrupt 12	28	1C	ICR06	446_H	$38C_H$	$000FFF8C_H$	—
External Interrupt 13	29	1D			388_H	$000FFF88_H$	—
External Interrupt 14	30	1E	ICR07	447_H	384_H	$000FFF84_H$	—
Reserved	31	1F			380_H	$000FFF80_H$	—
Reload Timer 0	32	20	ICR08	448_H	$37C_H$	$000FFF7C_H$	4, 32
Reload Timer 1	33	21			378_H	$000FFF78_H$	5, 33
Reload Timer 2	34	22	ICR09	449_H	374_H	$000FFF74_H$	34
Reload Timer 3	35	23			370_H	$000FFF70_H$	35

Interrupt	Interrupt number		Interrupt level [1]		Interrupt vector [2]		DMA Resource number
	Deci-mal	Hexa-de cimal	Setting Register	Register address	Offset	Default Vector address	
Reload Timer 4	36	24	ICR10	$44A_H$	$36C_H$	$000FFF6C_H$	36
Reload Timer 5	37	25			368_H	$000FFF68_H$	37
Reload Timer 6	38	26	ICR11	$44B_H$	364_H	$000FFF64_H$	38
Reload Timer 7	39	27			360_H	$000FFF60_H$	39
Free Run Timer 0	40	28	ICR12	$44C_H$	$35C_H$	$000FFF5C_H$	40
Free Run Timer 1	41	29			358_H	$000FFF58_H$	41
Free Run Timer 2	42	2A	ICR13	$44D_H$	354_H	$000FFF54_H$	42
Free Run Timer 3	43	2B			350_H	$000FFF50_H$	43
Free Run Timer 4	44	2C	ICR14	$44E_H$	$34C_H$	$000FFF4C_H$	44
Free Run Timer 5	45	2D			348_H	$000FFF48_H$	45
Free Run Timer 6	46	2E	ICR15	$44F_H$	344_H	$000FFF44_H$	46
Free Run Timer 7	47	2F			340_H	$000FFF40_H$	47
CAN 0	48	30	ICR16	450_H	$33C_H$	$000FFF3C_H$	—
CAN 1	49	31			338_H	$000FFF38_H$	—
Reserved	50	32	ICR17	451_H	334_H	$000FFF34_H$	—
Reserved	51	33			330_H	$000FFF30_H$	—
Reserved	52	34	ICR18	452_H	$32C_H$	$000FFF2C_H$	—
Reserved	53	35			328_H	$000FFF28_H$	—
Reserved	54	36	ICR19	453_H	324_H	$000FFF24_H$	6, 48
Reserved	55	37			320_H	$000FFF20_H$	7, 49
Reserved	56	38	ICR20	454_H	$31C_H$	$000FFF1C_H$	8, 50
Reserved	57	39			318_H	$000FFF18_H$	9, 51
LIN-USART 2 RX	58	3A	ICR21	455_H	314_H	$000FFF14_H$	52
LIN-USART 2 TX **LIN-USART (FIFO) 2 EoT**	59	3B			310_H	$000FFF10_H$	53 --
Reserved	60	3C	ICR22	456_H	$30C_H$	$000FFF0C_H$	54
Reserved	61	3D			308_H	$000FFF08_H$	55
Reserved	62	3E	ICR23 [4]	457_H	304_H	$000FFF04_H$	—
Delayed Interrupt	63	3F			300_H	$000FFF00_H$	—
System reserved [5]	64	40	(ICR24)	(458_H)	$2FC_H$	$000FFEFC_H$	—
System reserved [5]	65	41			$2F8_H$	$000FFEF8_H$	—
LIN-USART (FIFO) 4 RX	66	42	ICR25	459_H	$2F4_H$	$000FFEF4_H$	10, 56
LIN-USART (FIFO) 4 TX **LIN-USART (FIFO) 4 EoT**	67	43			$2F0_H$	$000FFEF0_H$	11, 57 --
LIN-USART (FIFO) 5 RX	68	44	ICR26	$45A_H$	$2EC_H$	$000FFEEC_H$	12, 58
LIN-USART (FIFO) 5 TX **LIN-USART (FIFO) 5 EoT**	69	45			$2E8_H$	$000FFEE8_H$	13, 59 --
LIN-USART (FIFO) 6 RX	70	46	ICR27	$45B_H$	$2E4_H$	$000FFEE4_H$	60
LIN-USART (FIFO) 6 TX **LIN-USART (FIFO) 6 EoT**	71	47			$2E0_H$	$000FFEE0_H$	61 --

Interrupt	Interrupt number		Interrupt level [1]		Interrupt vector [2]		DMA Resource number
	Deci-mal	Hexa-de cimal	Setting Register	Register address	Offset	Default Vector address	
LIN-USART (FIFO) 7 RX	72	48	ICR28	$45C_H$	$2DC_H$	$000FFEDC_H$	62
LIN-USART (FIFO) 7 TX LIN-USART (FIFO) 7 EoT	73	49			$2D8_H$	$000FFED8_H$	63 --
I^2C 0 / I^2C 2	74	4A	ICR29	$45D_H$	$2D4_H$	$000FFED4_H$	—
I^2C 3	75	4B			$2D0_H$	$000FFED0_H$	—
Reserved	76	4C	ICR30	$45E_H$	$2CC_H$	$000FFECC_H$	64
Reserved	77	4D			$2C8_H$	$000FFEC8_H$	65
Reserved	78	4E	ICR31	$45F_H$	$2C4_H$	$000FFEC4_H$	66
Reserved	79	4F			$2C0_H$	$000FFEC0_H$	67
Reserved	80	50	ICR32	460_H	$2BC_H$	$000FFEBC_H$	68
Reserved	81	51			$2B8_H$	$000FFEB8_H$	69
Reserved	82	52	ICR33	461_H	$2B4_H$	$000FFEB4_H$	70
Reserved	83	53			$2B0_H$	$000FFEB0_H$	71
Reserved	84	54	ICR34	462_H	$2AC_H$	$000FFEAC_H$	72
Reserved	85	55			$2A8_H$	$000FFEA8_H$	73
Reserved	86	56	ICR35	463_H	$2A4_H$	$000FFEA4_H$	74
Reserved	87	57			$2A0_H$	$000FFEA0_H$	75
Reserved	88	58	ICR36	464_H	$29C_H$	$000FFE9C_H$	76
Reserved	89	59			298_H	$000FFE98_H$	77
Reserved	90	5A	ICR37	465_H	294_H	$000FFE94_H$	78
Reserved	91	5B			290_H	$000FFE90_H$	79
Input Capture 0	92	5C	ICR38	466_H	$28C_H$	$000FFE8C_H$	80
Input Capture 1	93	5D			288_H	$000FFE88_H$	81
Input Capture 2	94	5E	ICR39	467_H	284_H	$000FFE84_H$	82
Input Capture 3	95	5F			280_H	$000FFE80_H$	83
Input Capture 4	96	60	ICR40	468_H	$27C_H$	$000FFE7C_H$	84
Input Capture 5	97	61			278_H	$000FFE78_H$	85
Input Capture 6	98	62	ICR41	469_H	274_H	$000FFE74_H$	86
Input Capture 7	99	63			270_H	$000FFE70_H$	87
Output Compare 0	100	64	ICR42	$46A_H$	$26C_H$	$000FFE6C_H$	88
Output Compare 1	101	65			268_H	$000FFE68_H$	89
Output Compare 2	102	66	ICR43	$46B_H$	264_H	$000FFE64_H$	90
Output Compare 3	103	67			260_H	$000FFE60_H$	91
Reserved	104	68	ICR44	$46C_H$	$25C_H$	$000FFE5C_H$	92
Reserved	105	69			258_H	$000FFE58_H$	93
Reserved	106	6A	ICR45	$46D_H$	254_H	$000FFE54_H$	94
Reserved	107	6B			250_H	$000FFE50_H$	95
Sound Generator	108	6C	ICR46	$46E_H$	$24C_H$	$000FFE4C_H$	—
Phase Frequency Modulator	109	6D			248_H	$000FFE48_H$	—

Interrupt	Interrupt number		Interrupt level [1]		Interrupt vector [2]		DMA Resource number
	Deci-mal	Hexa-de cimal	Setting Register	Register address	Offset	Default Vector address	
Reserved	110	6E	ICR47 [4]	$46F_H$	244_H	$000FFE44_H$	—
Reserved	111	6F			240_H	$000FFE40_H$	—
Reserved	112	70	ICR48	470_H	$23C_H$	$000FFE3C_H$	15, 96
Reserved	113	71			238_H	$000FFE38_H$	97
Reserved	114	72	ICR49	471_H	234_H	$000FFE34_H$	98
Reserved	115	73			230_H	$000FFE30_H$	99
PPG4	116	74	ICR50	472_H	$22C_H$	$000FFE2C_H$	100
PPG5	117	75			228_H	$000FFE28_H$	101
PPG6	118	76	ICR51	473_H	224_H	$000FFE24_H$	102
PPG7	119	77			220_H	$000FFE20_H$	103
PPG8	120	78	ICR52	474_H	$21C_H$	$000FFE1C_H$	104
PPG9	121	79			218_H	$000FFE18_H$	105
PPG10	122	7A	ICR53	475_H	214_H	$000FFE14_H$	106
PPG11	123	7B			210_H	$000FFE10_H$	107
PPG12	124	7C	ICR54	476_H	$20C_H$	$000FFE0C_H$	108
PPG13	125	7D			208_H	$000FFE08_H$	109
PPG14	126	7E	ICR55	477_H	204_H	$000FFE04_H$	110
PPG15	127	7F			200_H	$000FFE00_H$	111
Up/Down Counter 0	128	80	ICR56	478_H	$1FC_H$	$000FFDFC_H$	—
Reserved	129	81			$1F8_H$	$000FFDF8_H$	—
Up/Down Counter 2	130	82	ICR57	479_H	$1F4_H$	$000FFDF4_H$	—
Up/Down Counter 3	131	83			$1F0_H$	$000FFDF0_H$	—
Real Time Clock	132	84	ICR58	$47A_H$	$1EC_H$	$000FFDEC_H$	—
Calibration Unit	133	85			$1E8_H$	$000FFDE8_H$	—
A/D Converter 0	134	86	ICR59	$47B_H$	$1E4_H$	$000FFDE4_H$	14, 112
Reserved	135	87			$1E0_H$	$000FFDE0_H$	—
Alarm Comparator 0	136	88	ICR60	$47C_H$	$1DC_H$	$000FFDDC_H$	—
Reserved	137	89			$1D8_H$	$000FFDD8_H$	—
Low Voltage Detection	138	8A	ICR61	$47D_H$	$1D4_H$	$000FFDD4_H$	—
SMC Comparator 0 to 5	139	8B			$1D0_H$	$000FFDD0_H$	—
Timebase Overflow	140	8C	ICR62	$47E_H$	$1CC_H$	$000FFDCC_H$	—
PLL Clock Gear	141	8D			$1C8_H$	$000FFDC8_H$	—
DMA Controller	142	8E	ICR63	$47F_H$	$1C4_H$	$000FFDC4_H$	—
Main/Sub OSC stability wait	143	8F			$1C0_H$	$000FFDC0_H$	—
Security vector	144	90	—	—	$1BC_H$	$000FFDBC_H$	—
Used by the INT instruction.	145 to 255	91 to FF	—	—	$1B8_H$ to 000_H	$000FFDB8_H$ to $000FFC00_H$	—

1. The Interrupt Control Registers (ICRs) are located in the interrupt controller and set the interrupt level for each interrupt request. An ICR is provided for each interrupt request.

2. The vector address for each EIT (exception, interrupt or trap) is calculated by adding the listed offset to the table base register value (TBR). The TBR specifies the top of the EIT vector table. The addresses listed in the table are for the default TBR value (000FFC00H). The TBR is initialized to this value by a reset. The TBR is set to 000FFC00H after the internal boot ROM is executed.
3. Memory Protection Unit (MPU) support
4. ICR23 and ICR47 can be exchanged by setting the REALOS compatibility bit (addr $0C03_H$: IOS[0])
5. Used by REALOS

19. Recommended Settings

19.1 PLL and Clockgear Settings

Please note that for CY91F467EA the core base clock frequencies are valid in the **1.9 V** operation mode of the Main regulator and Flash.

Recommended PLL Divider and Clockgear Settings

PLL Input (CLK) [MHz]	Frequency Parameter		Clockgear Parameter		PLL Output (X) [MHz]	Core Base Clock [MHz]	Remarks
	DIVM	DIVN	DIVG	MULG	MULG		
4	2	25	16	24	200	100	
4	2	24	16	24	192	96	.
4	2	23	16	24	184	92	
4	2	22	16	24	176	88	
4	2	21	16	20	168	84	
4	2	20	16	20	160	80	
4	2	19	16	20	152	76	
4	2	18	16	20	144	72	
4	2	17	16	16	136	68	
4	2	16	16	16	128	64	
4	2	15	16	16	120	60	
4	2	14	16	16	112	56	
4	2	13	16	12	104	52	
4	2	12	16	12	96	48	
4	2	11	16	12	88	44	
4	4	10	16	24	160	40	
4	4	9	16	24	144	36	
4	4	8	16	24	128	32	
4	4	7	16	24	112	28	
4	6	6	16	24	144	24	
4	8	5	16	28	160	20	
4	10	4	16	32	160	16	
4	12	3	16	32	144	12	

19.2 Clock Modulator Settings

The following table shows all possible settings for the Clock Modulator in a base clock frequency range from 32 MHz up to 98 MHz.

The Flash access time settings need to be adjusted according to Fmax while the PLL and clockgear settings should be set according to base clock frequency.

Clock Modulator Settings, Frequency Range and Supported Supply Voltage

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
1	3	026F	88	79.5	98.5	
1	3	026F	84	76.1	93.8	
1	3	026F	80	72.6	89.1	
1	5	02AE	80	68.7	95.8	
2	3	046E	80	68.7	95.8	
1	3	026F	76	69.1	84.5	
1	5	02AE	76	65.3	90.8	
1	7	02ED	76	62	98.1	
2	3	046E	76	65.3	90.8	
3	3	066D	76	62	98.1	
1	3	026F	72	65.5	79.9	
1	5	02AE	72	62	85.8	
1	7	02ED	72	58.8	92.7	
2	3	046E	72	62	85.8	
3	3	066D	72	58.8	92.7	
1	3	026F	68	62	75.3	
1	5	02AE	68	58.7	80.9	
1	7	02ED	68	55.7	87.3	
1	9	032C	68	53	95	
2	3	046E	68	58.7	80.9	
2	5	04AC	68	53	95	
3	3	066D	68	55.7	87.3	
4	3	086C	68	53	95	
1	3	026F	64	58.5	70.7	
1	5	02AE	64	55.3	75.9	
1	7	02ED	64	52.5	82	
1	9	032C	64	49.9	89.1	
1	11	036B	64	47.6	97.6	
2	3	046E	64	55.3	75.9	
2	5	04AC	64	49.9	89.1	
3	3	066D	64	52.5	82	
4	3	086C	64	49.9	89.1	
5	3	0A6B	64	47.6	97.6	
1	3	026F	60	54.9	66.1	
1	5	02AE	60	51.9	71	
1	7	02ED	60	49.3	76.7	
1	9	032C	60	46.9	83.3	
1	11	036B	60	44.7	91.3	
2	3	046E	60	51.9	71	

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
2	5	04AC	60	46.9	83.3	
3	3	066D	60	49.3	76.7	
4	3	086C	60	46.9	83.3	
5	3	0A6B	60	44.7	91.3	
1	3	026F	56	51.4	61.6	
1	5	02AE	56	48.6	66.1	
1	7	02ED	56	46.1	71.4	
1	9	032C	56	43.8	77.6	
1	11	036B	56	41.8	84.9	
1	13	03AA	56	39.9	93.8	
2	3	046E	56	48.6	66.1	
2	5	04AC	56	43.8	77.6	
2	7	04EA	56	39.9	93.8	
3	3	066D	56	46.1	71.4	
3	5	06AA	56	39.9	93.8	
4	3	086C	56	43.8	77.6	
5	3	0A6B	56	41.8	84.9	
6	3	0C6A	56	39.9	93.8	
1	3	026F	52	47.8	57	
1	5	02AE	52	45.2	61.2	
1	7	02ED	52	42.9	66.1	
1	9	032C	52	40.8	71.8	
1	11	036B	52	38.8	78.6	
1	13	03AA	52	37.1	86.8	
1	15	03E9	52	35.5	96.9	
2	3	046E	52	45.2	61.2	
2	5	04AC	52	40.8	71.8	
2	7	04EA	52	37.1	86.8	
3	3	066D	52	42.9	66.1	
3	5	06AA	52	37.1	86.8	
4	3	086C	52	40.8	71.8	
5	3	0A6B	52	38.8	78.6	
6	3	0C6A	52	37.1	86.8	
7	3	0E69	52	35.5	96.9	
1	3	026F	48	44.2	52.5	
1	5	02AE	48	41.8	56.4	
1	7	02ED	48	39.6	60.9	
1	9	032C	48	37.7	66.1	
1	11	036B	48	35.9	72.3	
1	13	03AA	48	34.3	79.9	

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
1	15	03E9	48	32.8	89.1	
2	3	046E	48	41.8	56.4	
2	5	04AC	48	37.7	66.1	
2	7	04EA	48	34.3	79.9	
3	3	066D	48	39.6	60.9	
3	5	06AA	48	34.3	79.9	
4	3	086C	48	37.7	66.1	
5	3	0A6B	48	35.9	72.3	
6	3	0C6A	48	34.3	79.9	
7	3	0E69	48	32.8	89.1	
1	3	026F	44	40.6	48.1	
1	5	02AE	44	38.4	51.6	
1	7	02ED	44	36.4	55.7	
1	9	032C	44	34.6	60.4	
1	11	036B	44	33	66.1	
1	13	03AA	44	31.5	73	
1	15	03E9	44	30.1	81.4	
2	3	046E	44	38.4	51.6	
2	5	04AC	44	34.6	60.4	
2	7	04EA	44	31.5	73	
2	9	0528	44	28.9	92.1	
3	3	066D	44	36.4	55.7	
3	5	06AA	44	31.5	73	
4	3	086C	44	34.6	60.4	
4	5	08A8	44	28.9	92.1	
5	3	0A6B	44	33	66.1	
6	3	0C6A	44	31.5	73	
7	3	0E69	44	30.1	81.4	
8	3	1068	44	28.9	92.1	
1	3	026F	40	37	43.6	
1	5	02AE	40	34.9	46.8	
1	7	02ED	40	33.1	50.5	
1	9	032C	40	31.5	54.8	
1	11	036B	40	30	59.9	
1	13	03AA	40	28.7	66.1	
1	15	03E9	40	27.4	73.7	
2	3	046E	40	34.9	46.8	
2	5	04AC	40	31.5	54.8	
2	7	04EA	40	28.7	66.1	
2	9	0528	40	26.3	83.3	

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
3	3	066D	40	33.1	50.5	
3	5	06AA	40	28.7	66.1	
3	7	06E7	40	25.3	95.8	
4	3	086C	40	31.5	54.8	
4	5	08A8	40	26.3	83.3	
5	3	0A6B	40	30	59.9	
6	3	0C6A	40	28.7	66.1	
7	3	0E69	40	27.4	73.7	
8	3	1068	40	26.3	83.3	
9	3	1267	40	25.3	95.8	
1	3	026F	36	33.3	39.2	
1	5	02AE	36	31.5	42	
1	7	02ED	36	29.9	45.3	
1	9	032C	36	28.4	49.2	
1	11	036B	36	27.1	53.8	
1	13	03AA	36	25.8	59.3	
1	15	03E9	36	24.7	66.1	
2	3	046E	36	31.5	42	
2	5	04AC	36	28.4	49.2	
2	7	04EA	36	25.8	59.3	
2	9	0528	36	23.7	74.7	
3	3	066D	36	29.9	45.3	
3	5	06AA	36	25.8	59.3	
3	7	06E7	36	22.8	85.8	
4	3	086C	36	28.4	49.2	
4	5	08A8	36	23.7	74.7	
5	3	0A6B	36	27.1	53.8	
6	3	0C6A	36	25.8	59.3	
7	3	0E69	36	24.7	66.1	
8	3	1068	36	23.7	74.7	
9	3	1267	36	22.8	85.8	
1	3	026F	32	29.7	34.7	
1	5	02AE	32	28	37.3	
1	7	02ED	32	26.6	40.2	
1	9	032C	32	25.3	43.6	
1	11	036B	32	24.1	47.7	
1	13	03AA	32	23	52.5	
1	15	03E9	32	22	58.6	
2	3	046E	32	28	37.3	
2	5	04AC	32	25.3	43.6	

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
2	7	04EA	32	23	52.5	
2	9	0528	32	21.1	66.1	
2	11	0566	32	19.5	89.1	
3	3	066D	32	26.6	40.2	
3	5	06AA	32	23	52.5	
3	7	06E7	32	20.3	75.9	
4	3	086C	32	25.3	43.6	
4	5	08A8	32	21.1	66.1	
5	3	0A6B	32	24.1	47.7	
5	5	0AA6	32	19.5	89.1	
6	3	0C6A	32	23	52.5	
7	3	0E69	32	22	58.6	
8	3	1068	32	21.1	66.1	
9	3	1267	32	20.3	75.9	
10	3	1466	32	19.5	89.1	

20. Electrical Characteristics

20.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply slew rate	—	—	50	V/ms	
Power supply voltage 1*1	$V_{DD}5R$	– 0.3	+ 6.0	V	
Power supply voltage 2*1	$V_{DD}5$	– 0.3	+ 6.0	V	
Power supply voltage 3*1	$HV_{DD}5$	– 0.3	+ 6.0	V	
Power supply voltage 4*1	$V_{DD}35$	– 0.3	+ 6.0	V	
Relationship of the supply voltages	$HV_{DD}5$	$V_{DD}5$-0.3	$V_{DD}5$+0.3	V	SMC mode
		$V_{SS}5$-0.3	$V_{DD}5$+0.3	V	General purpose port mode
	$AV_{CC}5$	$V_{DD}5$-0.3	$V_{DD}5$+0.3	V	At least one pin of the Ports 25 to 29 (SMC, ANn) is used as digital input or output.
		$V_{SS}5$-0.3	$V_{DD}5$+0.3	V	All pins of the Ports 25 to 29 (SMC, ANn) follow the condition of V_{IA}
Analog power supply voltage*1	$AV_{CC}5$	– 0.3	+ 6.0	V	*2
Analog reference power supply voltage*1	AVRH5	– 0.3	+ 6.0	V	*2
Input voltage 1*1	V_{I1}	Vss5 – 0.3	$V_{DD}5$ + 0.3	V	
Input voltage 2*1	V_{I2}	Vss5 – 0.3	$V_{DD}35$ + 0.3	V	External bus
Input voltage 3*1	V_{I3}	HVss5 – 0.3	$HV_{DD}5$ + 0.3	V	Stepper motor controller
Analog pin input voltage*1	V_{IA}	AVss5 – 0.3	AVcc5 + 0.3	V	
Output voltage 1*1	V_{O1}	Vss5 – 0.3	$V_{DD}5$ + 0.3	V	
Output voltage 2*1	V_{O2}	Vss5 – 0.3	$V_{DD}35$ + 0.3	V	External bus
Output voltage 3*1	V_{O3}	HVss5 – 0.3	$HV_{DD}5$ + 0.3	V	Stepper motor controller
Maximum clamp current	I_{CLAMP}	– 4.0	+ 4.0	mA	*3
Total maximum clamp current	$\Sigma \lvert I_{CLAMP} \rvert$	—	20	mA	*3
"L" level maximum output current*4	I_{OL}	—	10	mA	
		—	40	mA	Stepper motor controller
"L" level average output current*5	I_{OLAV}	—	8	mA	
		—	30	mA	Stepper motor controller
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
		—	360	mA	Stepper motor controller
"L" level total average output current*6	ΣI_{OLAV}	—	50	mA	
		—	230	mA	Stepper motor controller
"H" level maximum output current*4	I_{OH}	—	– 10	mA	
		—	– 40	mA	Stepper motor controller
"H" level average output current*5	I_{OHAV}	—	– 4	mA	
		—	– 30	mA	Stepper motor controller
"H" level total maximum output current	ΣI_{OH}	—	– 100	mA	
		—	– 360	mA	Stepper motor controller

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
"H" level total average output current*6	ΣI_{OHAV}	—	− 25	mA	
		—	− 230	mA	Stepper motor controller
Permitted power dissipation *7	P_D	—	1100 *8	mW	at $T_A \leq 85$ °C
		—	1100 *8	mW	at $T_A \leq 105$ °C, no Flash program/erase *9
		—	555 *8	mW	at $T_A \leq 105$ °C
Operating temperature	T_A	− 40	+ 105	°C	
Storage temperature	Tstg	− 55	+ 150	°C	

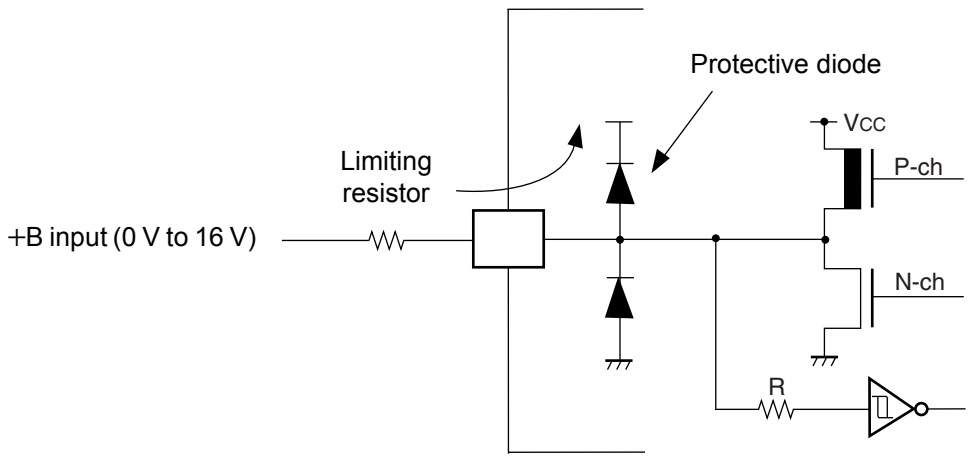
*1: The parameter is based on $V_{SS}5 = HV_{SS}5 = AV_{SS}5 = 0.0$ V.

*2: $AV_{CC}5$ and AVRH5 must not exceed $V_{DD}5 + 0.3$ V.

*3:

- Use within recommended operating conditions.
- Use with DC voltage (current).
- +B signals are input signals that exceed the $V_{DD}5$ voltage. +B signals should always be applied by connecting a limiting resistor between the +B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed the rated value at any time, either instantaneously or for an extended period, when the +B signal is input.
- Note that when the microcontroller drive current is low, such as in the low power consumption modes, the +B input potential can increase the potential at the power supply pin via a protective diode, possibly affecting other devices.
- Note that if the +B signal is input when the microcontroller is off (not fixed at 0 V), power is supplied through the +B input pin; therefore, the microcontroller may partially operate.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
- Do not leave +B input pins open.
- Example of recommended circuit:

• Input/output equivalent circuit



*4: Maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*5: Average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 100 ms period.

*6: Total average output current is defined as the value of the average current flowing through all of the corresponding pins for a 100 ms period.

*7:The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.
The actual power dissipation depends on the customer application and can be calculated as follows:

$P_D = P_{IO} + P_{INT}$

$P_{IO} = \Sigma (|V_{SS}-V_{OL}| * I_{OL} + |V_{DD}-V_{OH}| * I_{OH})$ (IO load power dissipation, sum is performed on all IO ports)

$P_{INT} = V_{DD}5R * I_{CC} + AV_{CC}5 * I_A + AVRH5 * I_R$ (internal power dissipation)

*8:Worst case value for the QFP package mounted on a 4-layer PCB at specified T_A without air flow.

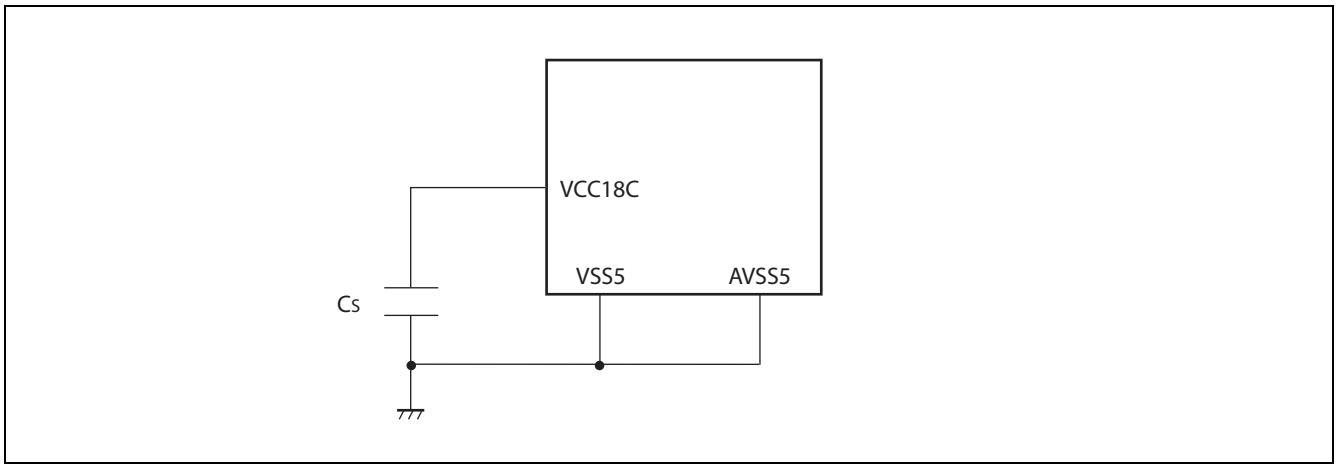
*9: Please contact Cypress for reliability limitations when using under these conditions.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

20.2 Recommended Operating Conditions

($V_{SS}5 = AV_{SS}5 = 0.0$ V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	$V_{DD}5$	3.0	—	5.5	V	
	$V_{DD}5R$	3.0	—	5.5	V	Internal regulator
	$V_{DD}35$	3.0	—	5.5	V	External bus
	$HV_{DD}5$	4.5	—	5.5	V	Stepper motor controller
		3.0	—	5.5	V	Stepper motor controller (when all pins are used as general-purpose ports)
	$AV_{CC}5$	3.0	—	5.5	V	A/D converter
Smoothing capacitor at VCC18C pin	C_S	—	4.7	—	µF	Use a X7R ceramic capacitor or a capacitor that has similar frequency characteristics.
Power supply slew rate		—	—	50	V/ms	
Operating temperature	T_A	− 40	—	+ 105	°C	
Stepper motor control slew rate			40		ns	Cload = 0 pF
Main Oscillation stabilisation time		10			ms	
Lock-up time PLL (4 MHz ->16 ...100 MHz)				0.6	ms	
ESD Protection (Human body model)	Vsurge	2			kV	$R_{discharge}$ = 1.5 kΩ $C_{discharge}$ = 100 pF
RC Oscillator	fRC100kHz	50	100	200	kHz	$VDD_{CORE} \geq 1.65$ V
	fRC2MHz	1	2	4	MHz	



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their Cypress representatives beforehand.

20.3 DC Characteristics

Note: In the following tables, "V_{DD}" means $V_{DD}35$ for pins of ext. bus or $HV_{DD}5$ for SMC pins or $V_{DD}5$ for other pins. In the following tables, "V_{SS}" means Hvss5 for ground Pins of the stepper motor and $V_{SS}5$ for the other pins.

($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40$ °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input "H" voltage	V_{IH}	—	Port inputs if CMOS Hysteresis 0.8/0.2 input is selected	$0.8 \times V_{DD}$	—	$V_{DD} + 0.3$	V	CMOS hysteresis input
		—	Port inputs if CMOS Hysteresis 0.7/0.3 input is selected	$0.7 \times V_{DD}$	—	$V_{DD} + 0.3$	V	$4.5\ V \le V_{DD} \le 5.5\ V$
				$0.74 \times V_{DD}$	—	$V_{DD} + 0.3$	V	$3\ V \le V_{DD} < 4.5\ V$
		—	AUTOMOTIVE Hysteresis input is selected	$0.8 \times V_{DD}$	—	$V_{DD} + 0.3$	V	
		—	Port inputs if TTL input is selected	2.0	—	$V_{DD} + 0.3$	V	
	V_{IHR}	INITX	—	$0.8 \times V_{DD}$	—	$V_{DD} + 0.3$	V	INITX input pin (CMOS Hysteresis)
	V_{IHM}	MD_2 to MD_0	—	$V_{DD} - 0.3$	—	$V_{DD} + 0.3$	V	Mode input pins
	V_{IHX0S}	X0, X0A	—	2.5	—	$V_{DD} + 0.3$	V	External clock in "Oscillation mode"
	V_{IHX0F}	X0	—	$0.8 \times V_{DD}$	—	$V_{DD} + 0.3$	V	External clock in "Fast Clock Input mode"
Input "L" voltage	V_{IL}	—	Port inputs if CMOS Hysteresis 0.8/0.2 input is selected	$V_{SS} - 0.3$	—	$0.2 \times V_{DD}$	V	
		—	Port inputs if CMOS Hysteresis 0.7/0.3 input is selected	$V_{SS} - 0.3$	—	$0.3 \times V_{DD}$	V	
		—	Port inputs if AUTOMOTIVE Hysteresis input is selected	$V_{SS} - 0.3$	—	$0.5 \times V_{DD}$	V	$4.5\ V \le V_{DD} \le 5.5\ V$
				$V_{SS} - 0.3$	—	$0.46 \times V_{DD}$	V	$3\ V \le V_{DD} < 4.5\ V$
		—	Port inputs if TTL input is selected	$V_{SS} - 0.3$	—	0.8	V	
	V_{ILR}	INITX	—	$V_{SS} - 0.3$	—	$0.2 \times V_{DD}$	V	INITX input pin (CMOS Hysteresis)
	V_{ILM}	MD_2 to MD_0	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	Mode input pins
	V_{ILXDS}	X0, X0A	—	$V_{SS} - 0.3$	—	0.5	V	External clock in "Oscillation mode"
Input "L" voltage	V_{ILXDF}	X0	—	$V_{SS} - 0.3$	—	$0.2 \times V_{DD}$	V	External clock in "Fast Clock Input mode"

($V_{DD}5 = AV_{CC}5$ = 3.0 V to 5.5 V, $V_{SS}5 = AV_{SS}5$ = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output “H" voltage	V_{OH2}	Normal outputs	4.5 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = – 2 mA	V_{DD} – 0.5	—	—	V	Driving strength set to 2 mA
			3.0 V ≤ V_{DD} ≤ 4.5 V, I_{OH} = – 1.6 mA					
	V_{OH5}	Normal outputs	4.5 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = – 5 mA	V_{DD} – 0.5	—	—	V	Driving strength set to 5 mA
			3.0 V ≤ V_{DD} ≤ 4.5 V, I_{OH} = – 3 mA					
	V_{OH3}	I^2C outputs	3.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = – 3 mA	V_{DD} – 0.5	—	—	V	
	V_{OH30}	High current outputs	4.5 V ≤ V_{DD} ≤ 5.5 V, T_A = -40 °C, I_{OH} = -40 mA	V_{DD} – 0.5			V	Driving strength set to 30 mA
			4.5 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = -30 mA					
			3.0 V ≤ V_{DD} ≤ 4.5 V, I_{OH} = -20 mA					
Output “L“ voltage	V_{OL2}	Normal outputs	4.5 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = + 2 mA	—	—	0.4	V	Driving strength set to 2 mA
			3.0 V ≤ V_{DD} ≤ 4.5 V, I_{OL} = + 1.6 mA					
	V_{OL5}	Normal outputs	4.5 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = + 5 mA	—	—	0.4	V	Driving strength set to 5 mA
			3.0 V ≤ V_{DD} ≤ 4.5 V, I_{OL} = + 3 mA					
	V_{OL3}	I^2C outputs	3.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = + 3 mA	—	—	0.4	V	
	V_{OL30}	High current outputs	4.5 V ≤ V_{DD} ≤ 5.5 V, T_A = -40 °C, I_{OL} = +40 mA			0.5	V	Driving strength set to 30 mA
			4.5 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = +30 mA					
			3.0 V ≤ V_{DD} ≤ 4.5 V, I_{OL} = +20 mA					
Input leakage current	I_{IL}	Pnn_m *1	3.0 V ≤ V_{DD} ≤ 5.5 V $V_{SS}5 < V_I < V_{DD}$ T_A=25 °C	– 1	—	+ 1	µA	
			3.0 V ≤ V_{DD} ≤ 5.5 V $V_{SS}5 < V_I < V_{DD}$ T_A=105 °C	– 3	—	+ 3		
Analog input leakage current	I_{AIN}	ANn *2	3.0 V ≤ V_{DD} ≤ 5.5 V T_A=25 °C	– 1	—	+ 1	µA	
			3.0 V ≤ V_{DD} ≤ 5.5 V T_A=105 °C	– 3	—	+ 3	µA	

($V_{DD}5 = AV_{CC}5$ = 3.0 V to 5.5 V, $V_{SS}5 = AV_{SS}5$ = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Sum input leakage current	ΣI_L	Pnn_m *3, ALARM_0	$V_{DD}5 \geq V_{IN} \geq V_{SS}5$, $AV_{CC}5 \geq V_{IN} \geq AV_{SS}5$ Σ (1 to n) [max($\lvert I_L Hi \rvert$, $\lvert I_L Li \rvert$)]	–	8	30	µA	n = number of IO = 65 GPIO + 1 ALARM $I_L H$: leakage at high level input; $I_L L$: leakage at low level input
Pull-up resistance	R_{UP}	Pnn_m *4 INITX	3.0 V ≤ V_{DD} ≤ 3.6 V	40	100	160	kΩ	
			4.5 V ≤ V_{DD} ≤ 5.5 V	25	50	100		
Pull-down resistance	R_{DOWN}	Pnn_m *5	3.0 V ≤ V_{DD} ≤ 3.6 V	40	100	180	kΩ	
			4.5 V ≤ V_{DD} ≤ 5.5 V	25	50	100		
Input capacitance	C_{IN}	All except $V_{DD}5$, $V_{DD}5R$, $V_{SS}5$, $AV_{CC}5$, AV_{SS}, AVRH5	f = 1 MHz	-	5	15	pF	
Power supply current CY91 F467EA	I_{CC}	$V_{DD}5R$	CY91F467EA: CLKB: 100 MHz CLKP: 50 MHz CLKT: 50 MHz CLKCAN: 50 MHz	–	110	140	mA	Code fetch from Flash
	I_{CCH}	$V_{DD}5R$ *6	T_A = + 25 °C	–	10	30	µA	ShutDown mode with RTC running on 32 kHz Sub clock *7
			T_A = + 85 °C	–	80	150	µA	
			T_A = + 105 °C	–	160	300	µA	
			T_A = + 25 °C	–	15	35	µA	ShutDown mode with RTC running on 100 kHz RC clock *8
			T_A = + 85 °C	–	85	160	µA	
			T_A = + 105 °C	–	170	320	µA	
			T_A = + 25 °C	–	30	100	µA	At STOP mode *9
			T_A = + 85 °C	–	450	1000	µA	
			T_A = + 105 °C	–	1000	2200	µA	
			T_A = + 25 °C	–	140	300	µA	RTC: 4 MHz mode *10
			T_A = + 85 °C	–	500	1200	µA	
			T_A = + 105 °C	–	1000	2400	µA	
			T_A = + 25 °C	–	120	200	µA	RTC: 100 kHz mode *11
			T_A = + 85 °C	–	500	1100	µA	
			T_A = + 105 °C	–	1000	2300	µA	
	I_{LVE}	$V_{DD}5$	–	–	70	150	µA	External low voltage detection
	I_{LVI}	$V_{DD}5R$	–	–	50	100	µA	Internal low voltage detection
	I_{OSC}	$V_{DD}5$	–	–	250	500	µA	Main clock (4 MHz)
			–	–	20	40	µA	Sub clock (32 kHz)

1. Pnn_m includes all GPIO pins. Analog (AN) channels and PullUp/PullDown are disabled.
2. ANn includes all pins where AN channels are enabled.

3. Pnn_m includes all GPIO pins beside the external bus pins (P00 to P13) and Stepper Motor pins (P25, P26, P27). Analog (AN) channels and PullUp/PullDown are disabled.
4. Pnn_m includes all GPIO pins. The pull up resistors must be enabled by PPER/PPCR setting and the pins must be in input direction.
5. Pnn_m includes all GPIO pins. The pull down resistors must be enabled by PPER/PPCR setting and the pins must be in input direction.
6. Current on regulator supply pin $V_{DD}5R$ does not include I_{OSC} and I_{CC} of the I/O ring.
7. ShutDown mode with standby RAM enabled, sub regulator set to 1.2 V, Low voltage detection disabled. Same current consumption if RTC and Sub oscillator are disabled.
8. ShutDown mode with standby RAM enabled, sub regulator set to 1.2 V, Low voltage detection disabled, RC oscillator enabled 100 kHz.
9. STOP mode, sub regulator set to 1.2 V, Low voltage detection disabled, RC oscillator disabled.
10. STOP mode, sub regulator set to 1.2 V, Low voltage detection disabled, RC oscillator disabled, Main oscillator enabled.
11. STOP mode, sub regulator set to 1.2 V, Low voltage detection disabled, RC oscillator enabled 100 kHz.

20.4 A/D Converter Characteristics

($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40$ °C to + 105 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	– 3	—	+ 3	LSB	
Nonlinearity error	—	—	– 2.5	—	+ 2.5	LSB	
Differential nonlinearity error	—	—	– 1.9	—	+ 1.9	LSB	
Zero reading voltage	V_{OT}	ANn	AVRL – 1.5 LSB	AVRL + 0.5 LSB	AVRL + 2.5 LSB	V	
Full scale reading voltage	V_{FST}	ANn	AVRH – 3.5 LSB	AVRH – 1.5 LSB	AVRH + 0.5 LSB	V	
Compare time	T_{comp}	—	0.6	—	t.b.d. [1]	µs	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V
			2.0	—	t.b.d. [1]	µs	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V
Sampling time	T_{samp}	—	0.4	—	—	µs	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V, R_{EXT} < 2 kΩ
			1.0	—	—	µs	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V, R_{EXT} < 1 kΩ
Conversion time	T_{conv}	—	1.0	—	—	µs	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V
			3.0	—	—	µs	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V
Input capacitance	C_{IN}	ANn	—	—	11	pF	
Input resistance	R_{IN}	ANn	—	—	2.6	kΩ	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V
			—	—	12.1	kΩ	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V
Analog input leakage current	I_{AIN}	ANn	– 1	—	+ 1	µA	T_A = + 25 °C
			– 3	—	+ 3	µA	T_A = + 105 °C
Analog input voltage range	V_{AIN}	ANn	AVRL	—	AVRH	V	
Offset between input channels	—	ANn	—	—	4	LSB	
Reference voltage range	AVRH	AVRH5	0.75 × $AV_{CC}5$	—	$AV_{CC}5$	V	
	AVRL	$AV_{SS}5$	$AV_{SS}5$	—	$AV_{CC}5 \times 0.25$	V	
Power supply current	I_A	$AV_{CC}5$	—	2.5	5	mA	A/D Converter active
	I_{AH}	$AV_{CC}5$	—	—	5	µA	A/D Converter not operated *1
Reference voltage current	I_R	AVRH5	—	0.7	1	mA	A/D Converter active
	I_{RH}	AVRH5	—	—	5	µA	A/D Converter not operated *2

1. Paramater is under re-evaluation.

Note: The accuracy gets worse as AVRH - AVRL becomes smaller

*1: Supply current at $AV_{CC}5$, if A/D converter and ALARM comparator are not operating, ($V_{DD}5 = AV_{CC}5 = AVRH = 5.0$ V)

*2: Input current at AVRH5, if A/D converter is not operating, ($V_{DD}5 = AV_{CC}5 = AVRH = 5.0$ V)

Sampling Time Calculation

$T_{samp} = (2.6\ kOhm + R_{EXT}) \times 11\ pF \times 7$; for $4.5\ V \le AV_{CC}5 \le 5.5\ V$

$T_{samp} = (12.1\ kOhm + R_{EXT}) \times 11\ pF \times 7$; for $3.0\ V \le AV_{CC}5 \le 4.5\ V$

Conversion Time Calculation

$T_{conv} = T_{samp} + T_{comp}$

20.4.1 Definition of A/D converter terms

■ Resolution

Analog variation that is recognizable by the A/D converter.

■ Nonlinearity error

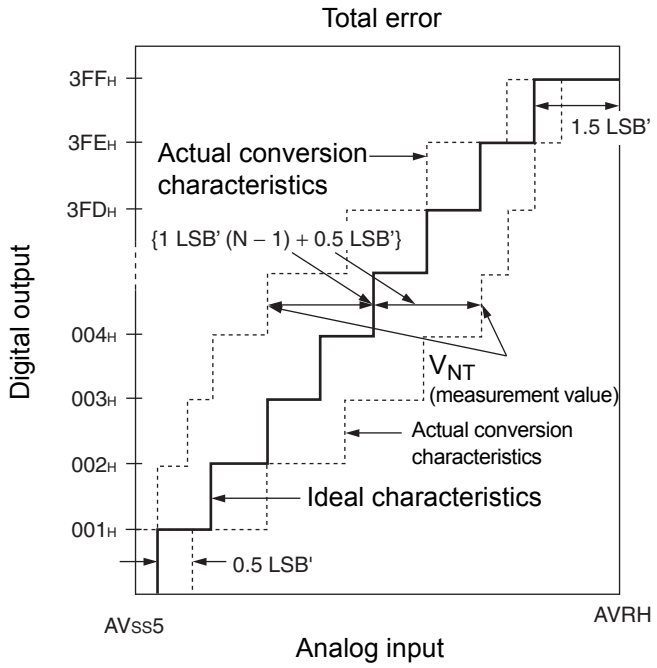
Deviation between actual conversion characteristics and a straight line connecting the zero transition point ($00\ 0000\ 0000_B \leftrightarrow 00\ 0000\ 0001_B$) and the full scale transition point ($11\ 1111\ 1110_B \leftrightarrow 11\ 1111\ 1111_B$).

■ Differential nonlinearity error

Deviation of the input voltage from the ideal value that is required to change the output code by 1 LSB.

■ Total error

This error indicates the difference between actual and theoretical values, including the zero transition error, full scale transition error, and nonlinearity error.



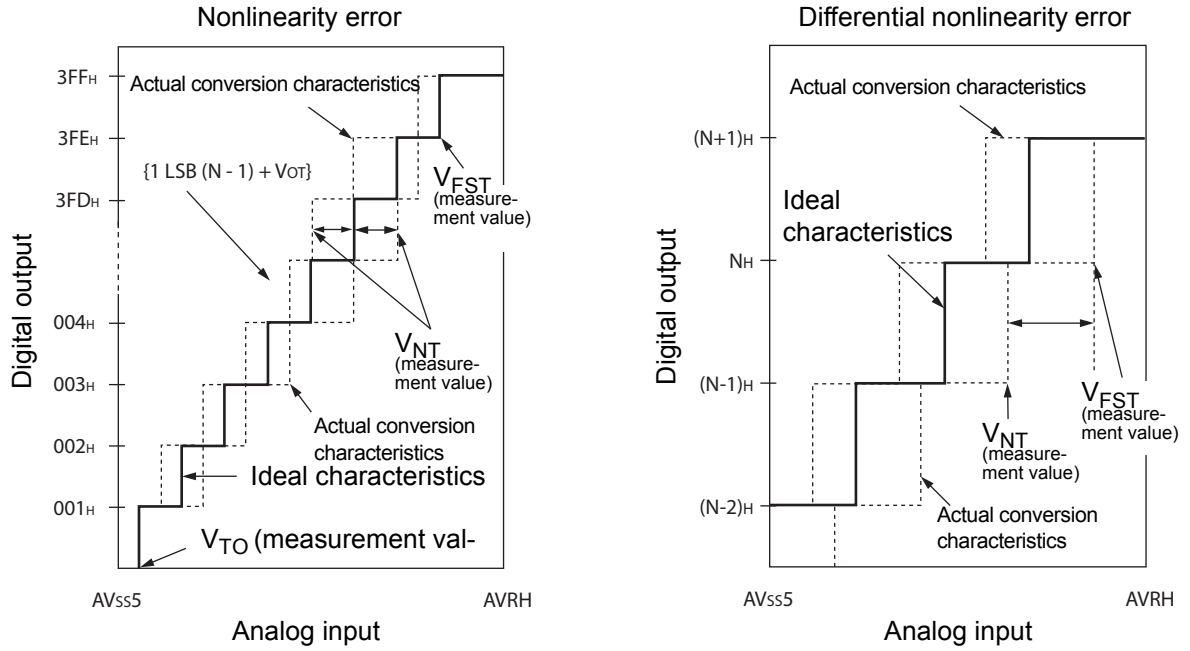
$$1\text{LSB' (ideal value)} = \frac{AVRH - AV_{SS}5}{1024}\ [V]$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB'} \times (N - 1) + 0.5\ \text{LSB'}\}}{1\ \text{LSB'}}$$

N : A/D converter digital output value
V_{OT}' (ideal value) = $AV_{SS}5 + 0.5$ LSB' [V]
V_{FST}' (ideal value) = AVRH – 1.5 LSB' [V]
V_{NT} : Voltage at which the digital output changes from $(N + 1)_H$ to N_H

(Continued)

(Continued)



$$\text{Nonlinearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{OT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential nonlinearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

N : A/D converter digital output value
V_{OT} : Voltage at which the digital output changes from 000_H to 001_H.
V_{FST} : Voltage at which the digital output changes from $3FE_H$ to $3FF_H$.

20.5 Alarm Comparator Characteristics

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Power supply current	I_{A5ALMF}	$AV_{CC}5$	—	25	40	µA	Alarm comparator enabled in fast mode (per channel) *1
	I_{A5ALMS}		—	7	10	µA	Alarm comparator enabled in normal mode (per channel) *1
	I_{A5ALMH}		—	—	5	µA	Alarm comparator disabled
ALARM pin input current	I_{ALIN}	ALARM_n	− 1	—	+ 1	µA	T_A=25 °C
			− 3	—	+ 3	µA	T_A=105 °C
ALARM pin input voltage range	V_{ALIN}		0	—	$AV_{CC}5$	V	
Alarm upper limit voltage	V_{IAH}		$AV_{CC}5 \times 0.78$ − 3%	$AV_{CC}5 \times 0.78$	$AV_{CC}5 \times 0.78$ + 3%	V	
Alarm lower limit voltage	V_{IAL}		$AV_{CC}5 \times 0.36$ − 5%	$AV_{CC}5 \times 0.36$	$AV_{CC}5 \times 0.36$ + 5%	V	
Alarm hysteresis voltage	V_{IAHYS}		50	—	250	mV	
Alarm input resistance	R_{IN}		5	—	—	MΩ	
Comparion time	t_{COMPF}		—	0.1	0.2	µs	Alarm comparator enabled in fast mode *1
	t_{COMPS}		—	1	2	µs	Alarm comparator enabled in normal mode *1

Note: *1:

The fast Alarm Comparator mode is enabled by setting ACSR.MD=1
Setting ACSR.MD=0 sets the normal mode.

20.6 FLASH Memory Program/Erase Characteristics

20.6.1 CY91F467EA

(T_A = 25°C, Vcc = 5.0 V)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.5	2.0	s	Erasure programming time not included
Chip erase time	-	n*0.5	n*2.0	s	n is the number of Flash sector of the device
Word (16 or 32-bit width) programming time	-	6	100	µs	System overhead time not included
Programme/Erase cycle	10 000			cycle	
Flash data retention time	20			year	*1

*1:This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85°C)

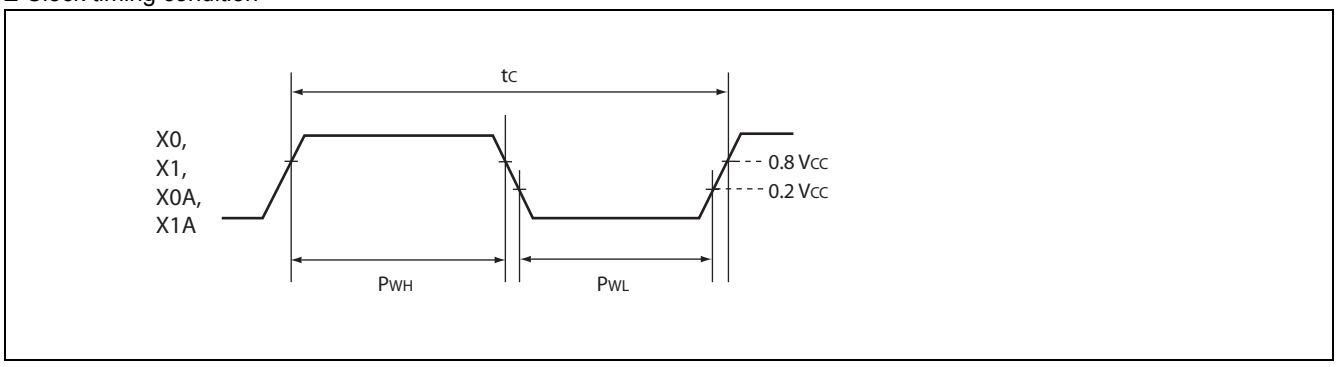
20.7 AC Characteristics

20.7.1 Clock Timing

($V_{DD}5$ = 3.0 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = −40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value			Unit	Condition
			Min	Typ	Max		
Clock frequency	f_C	X0 X1	3.5	4	16	MHz	Opposite phase external supply or crystal
			3.5	4	8	MHz	Opposite phase external supply or ceramic resonator
		X0A X1A	32	32.768	100	kHz	

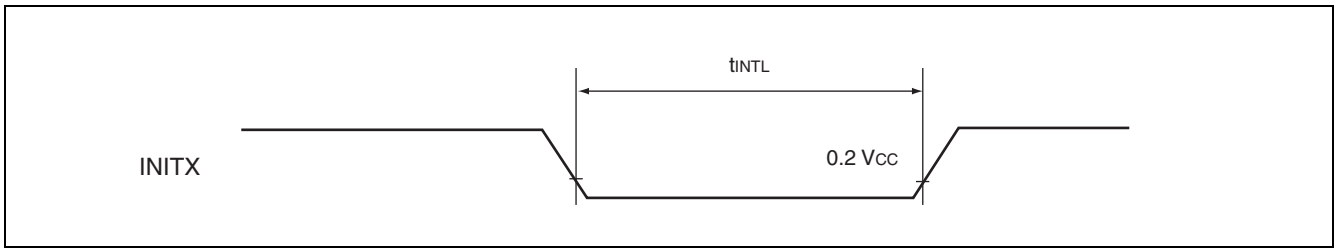
■ Clock timing condition



20.7.2 Reset Input Ratings

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
INITX input time (at power-on)	t_{INTL}	INITX	—	10	—	ms
INITX input time (other than the above)				20	—	µs



20.7.3 LIN-USART Timings at $V_{DD}5$ = 3.0 to 5.5 V

■ Conditions during AC measurements

■ All AC tests were measured under the following conditions:
- ❒ IO_{drive} = 5 mA
- ❒ $V_{DD}5$ = 3.0 V to 5.5 V, I_{load} = 3 mA
- ❒ $V_{SS}5$ = 0 V
- ❒ T_a = -40 °C to +105× °C
- ❒ C_l = 50 pF (load capacity value of pins when testing)
- ❒ VOL = 0.2 x $V_{DD}5$
- ❒ VOH = 0.8 x $V_{DD}5$
- ❒ EPILR = 0, PILR = 1 (Automotive Level = worst case)

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	$V_{DD}5$ = 3.0 V to 4.5 V		$V_{DD}5$ = 4.5 V to 5.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYCI}	SCKn	Internal clock operation (master mode)	4 t_{CLKP}	—	4 t_{CLKP}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKn SOTn		– 30	30	– 20	20	ns
SOT → SCK ↓ delay time	t_{OVSHI}	SCKn SOTn		m × t_{CLKP} – 30*	—	m × t_{CLKP} – 20*	—	ns
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCKn SINn		t_{CLKP} + 55	—	t_{CLKP} + 45	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}	SCKn SINn		0	—	0	—	ns

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	$V_{DD}5$ = 3.0 V to 4.5 V		$V_{DD}5$ = 4.5 V to 5.5 V		Unit
				Min	Max	Min	Max	
Serial clock "H" pulse width	t_{SHSLE}	SCKn	External clock operation (slave mode)	t_{CLKP} + 10	—	t_{CLKP} + 10	—	ns
Serial clock "L" pulse width	t_{SLSHE}	SCKn		t_{CLKP} + 10	—	t_{CLKP} + 10	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKn SOTn		—	2 t_{CLKP} + 55	—	2 t_{CLKP} + 45	ns
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCKn SINn		10	—	10	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXE}	SCKn SINn		t_{CLKP} + 10	—	t_{CLKP} + 10	—	ns
SCK rising time	t_{FE}	SCKn		—	20	—	20	ns
SCK falling time	t_{RE}	SCKn		—	20	—	20	ns

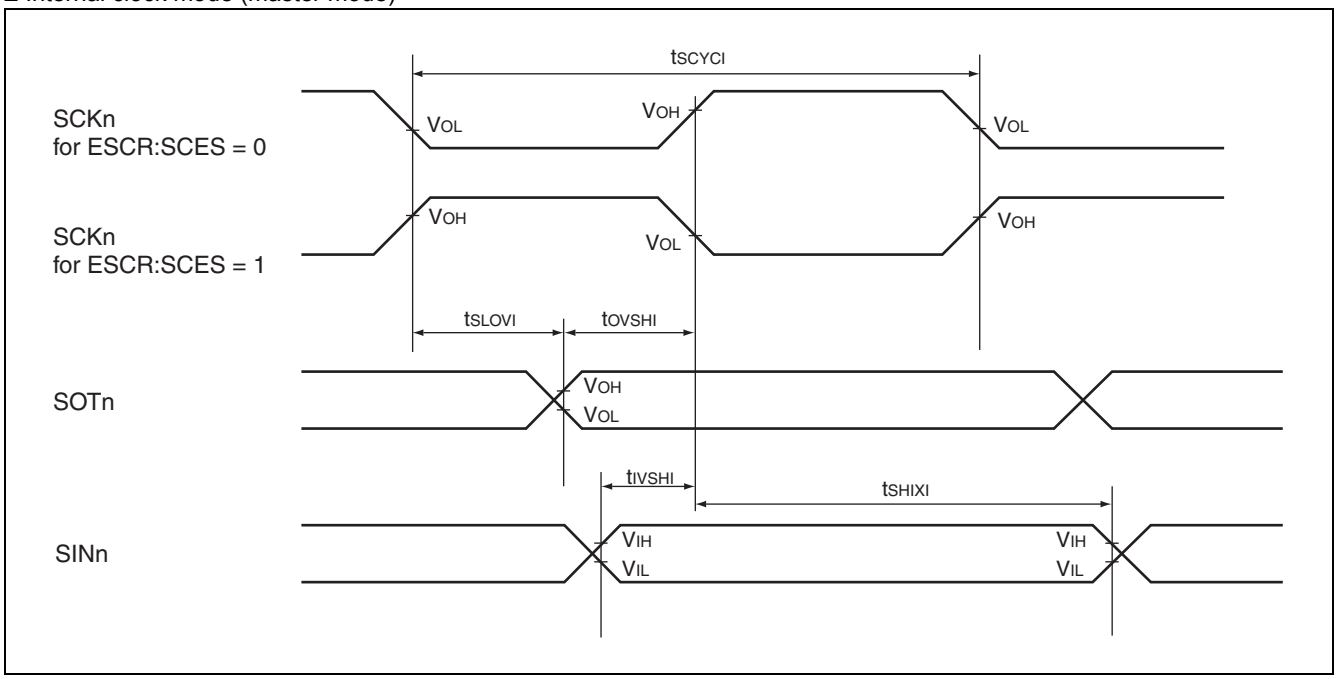
*: Parameter m depends on t_{SCYCI} and can be calculated as:

- if t_{SCYCI} = 2*k*t_{CLKP}, then m = k, where k is an integer > 2
- if t_{SCYCI} = (2*k + 1)*t_{CLKP}, then m = k + 1, where k is an integer > 1

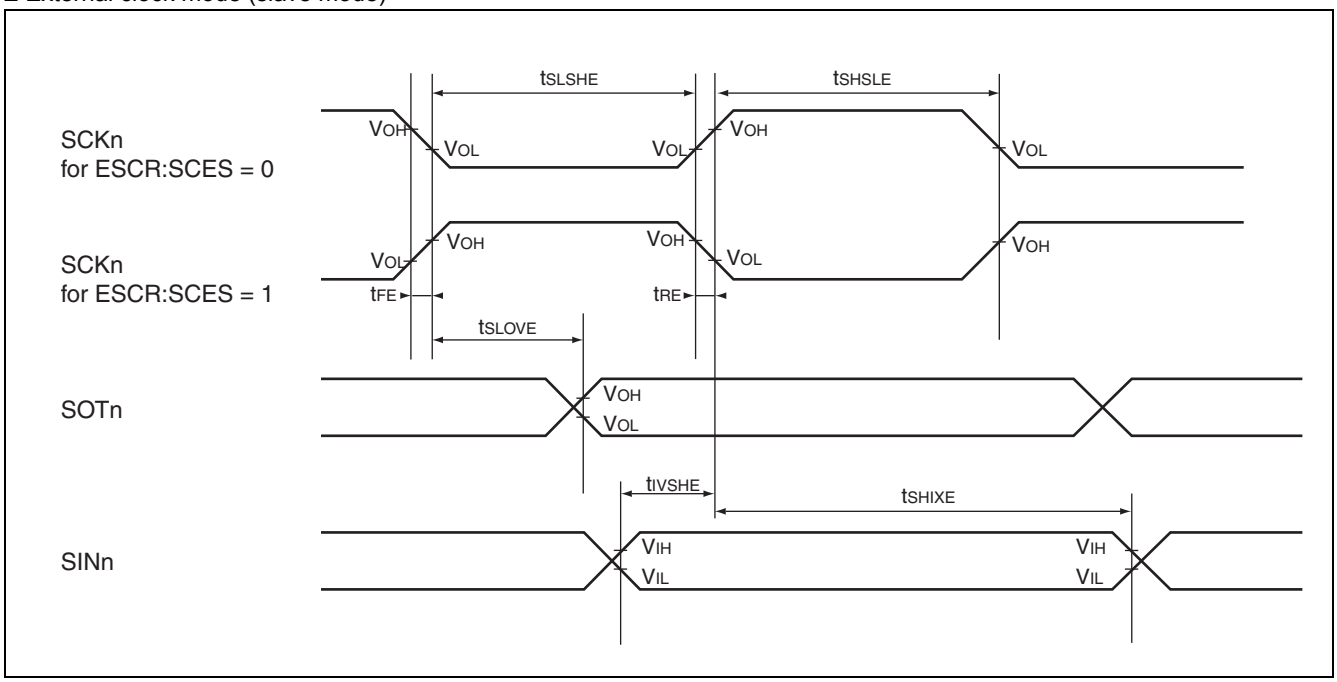
Notes:

- The above values are AC characteristics for CLK synchronous mode.
- t_{CLKP} is the cycle time of the peripheral clock.

■ Internal clock mode (master mode)



■ External clock mode (slave mode)



20.7.4 I^2C AC Timings at $V_{DD}5$ = 3.0 to 5.5 V

■ Conditions during AC measurements

All AC tests were measured under the following conditions:

- ❒ IO_{drive} = 3 mA
- ❒ $V_{DD}5$ = 3.0 V to 5.5 V, I_{load} = 3 mA
- ❒ $V_{SS}5$ = 0 V
- ❒ Ta = – 40 °C to + 105 °C
- ❒ C_l = 50 pF
- ❒ VOL = 0.3 × $V_{DD}5$
- ❒ VOH = 0.7 × $V_{DD}5$
- ❒ EPILR = 0, PILR = 0 (CMOS Hysteresis 0.3 × $V_{DD}5$/0.7 × $V_{DD}5$)

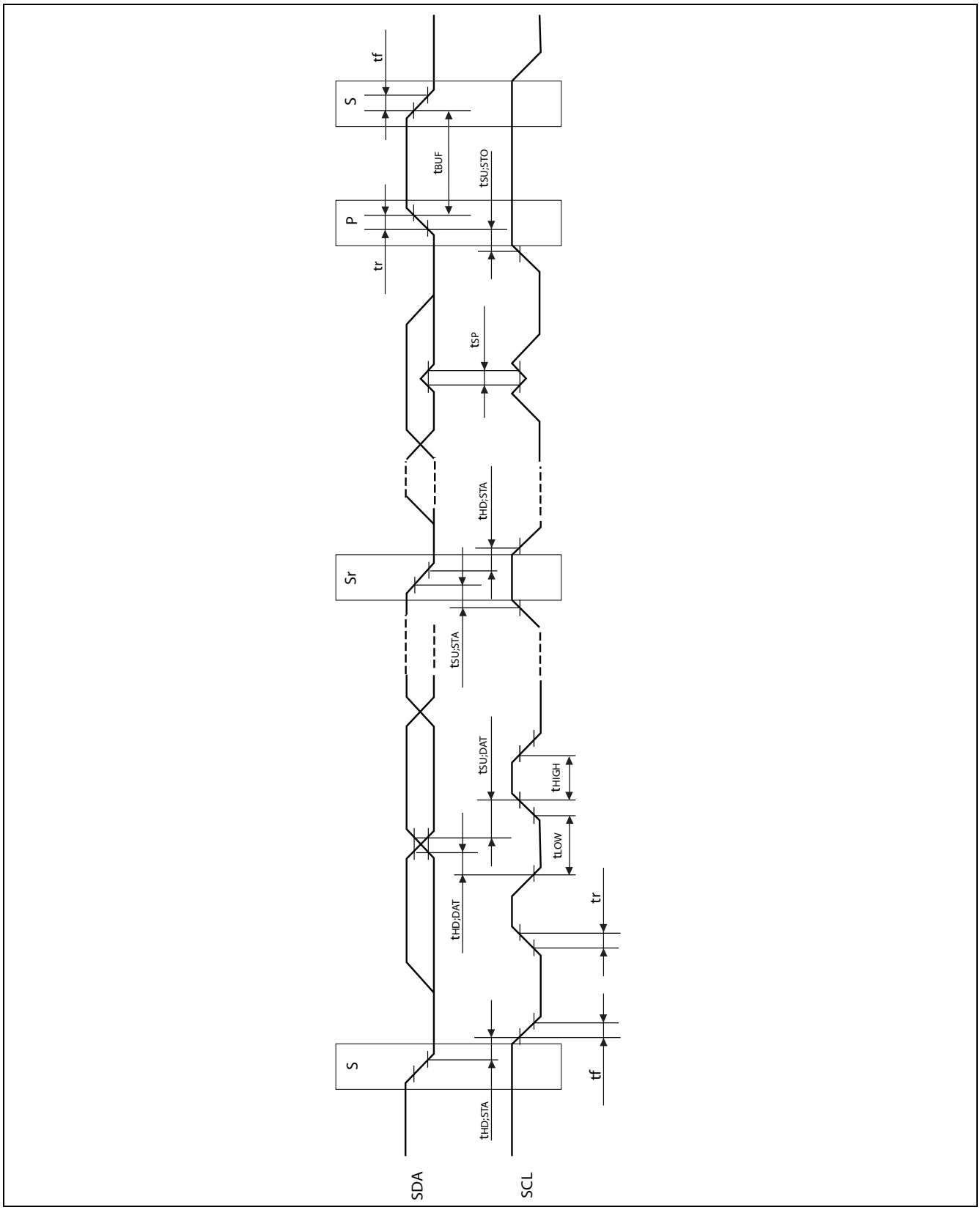
Fast Mode:

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit	Remark
			Min	Max		
SCL clock frequency	f_{SCL}	SCLn	0	400	kHz	
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	SCLn, SDAn	0.6	—	µs	
LOW period of the SCL clock	t_{LOW}	SCLn	1.3	—	µs	
HIGH period of the SCL clock	t_{HIGH}	SCLn	0.6	—	µs	
Setup time for a repeated START condition	$t_{SU;STA}$	SCLn, SDAn	0.6	—	µs	
Data hold time for I^2C-bus devices	$t_{HD;DAT}$	SCLn, SDAn	0	0.9	µs	
Data setup time	$t_{SU;DAT}$	SCLn SDAn	100	—	ns	
Rise time of both SDA and SCL signals	t_r	SCLn, SDAn	20 + 0.1Cb	300	ns	
Fall time of both SDA and SCL signals	t_f	SCLn, SDAn	20 + 0.1Cb	300	ns	
Setup time for STOP condition	$t_{SU;STO}$	SCLn, SDAn	0.6	—	µs	
Bus free time between a STOP and START condition	t_{BUF}	SCLn, SDAn	1.3	—	µs	
Capacitive load for each bus line	C_b	SCLn, SDAn	—	400	pF	
Pulse width of spike suppressed by input filter	t_{SP}	SCLn, SDAn	0	(1..1.5) × t_{CLKP}	ns	*1

1. The noise filter will suppress single spikes with a pulse width of 0ns and between (1 to 1.5) cycles of peripheral clock, depending on the phase relationship between I2C signals (SDA, SCL) and peripheral clock

Note: t_{CLKP} is the cycle time of the peripheral clock.

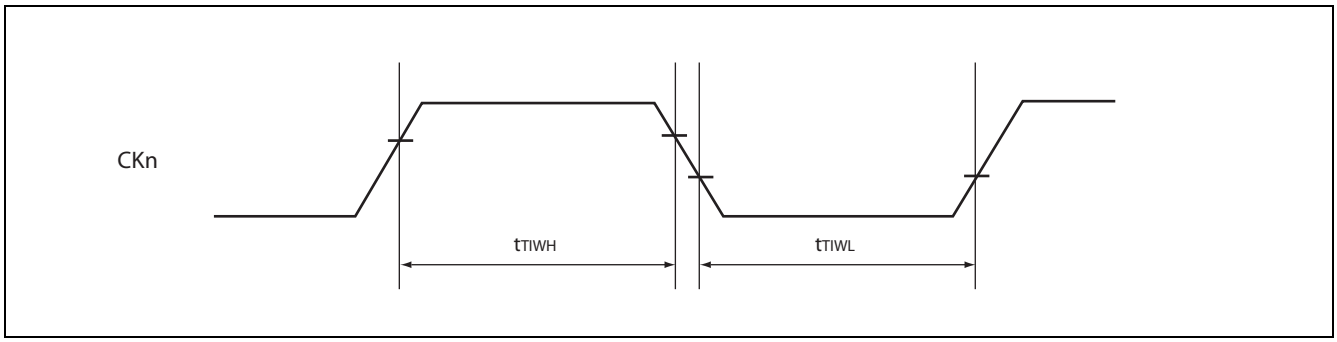

tf
S
tBUF
tSU;STO
P
tr
tSP
tHD;STA
Sr
tSU;STA
tSU;DAT
tHIGH
tLOW
tHD;DAT
tr
S
tf
tHD;STA
SDA
SCL

20.7.5 Free-run Timer Clock

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	CKn	—	$4t_{CLKP}$	—	ns

Note: t_{CLKP} is the cycle time of the peripheral clock.

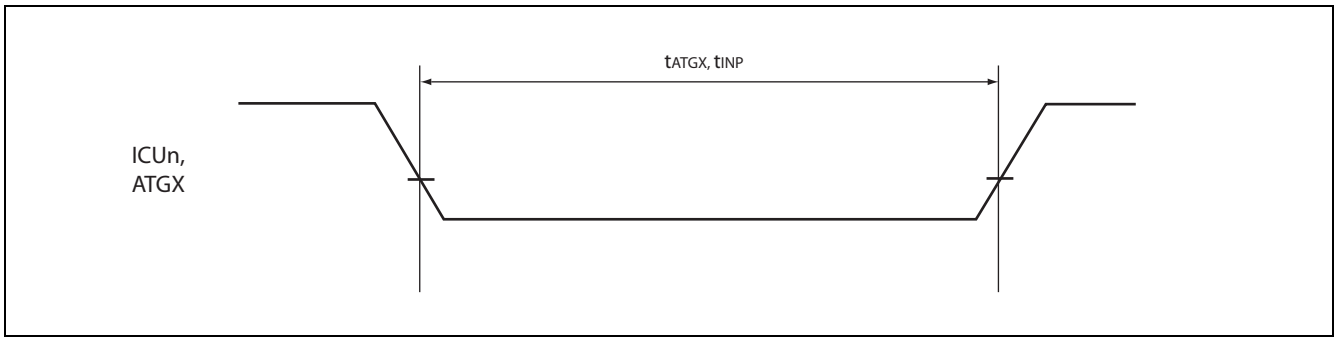


20.7.6 Trigger Input Timing

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input capture input trigger	t_{INP}	ICUn	—	$5t_{CLKP}$	—	ns
A/D converter trigger	t_{ATGX}	ATGX	—	$5t_{CLKP}$	—	ns

Note: t_{CLKP} is the cycle time of the peripheral clock.



20.7.7 External Bus AC Timings at $V_{DD}35$ = 4.5 to 5.5 V

■ Conditions during AC measurements

All AC tests were measured under the following conditions:

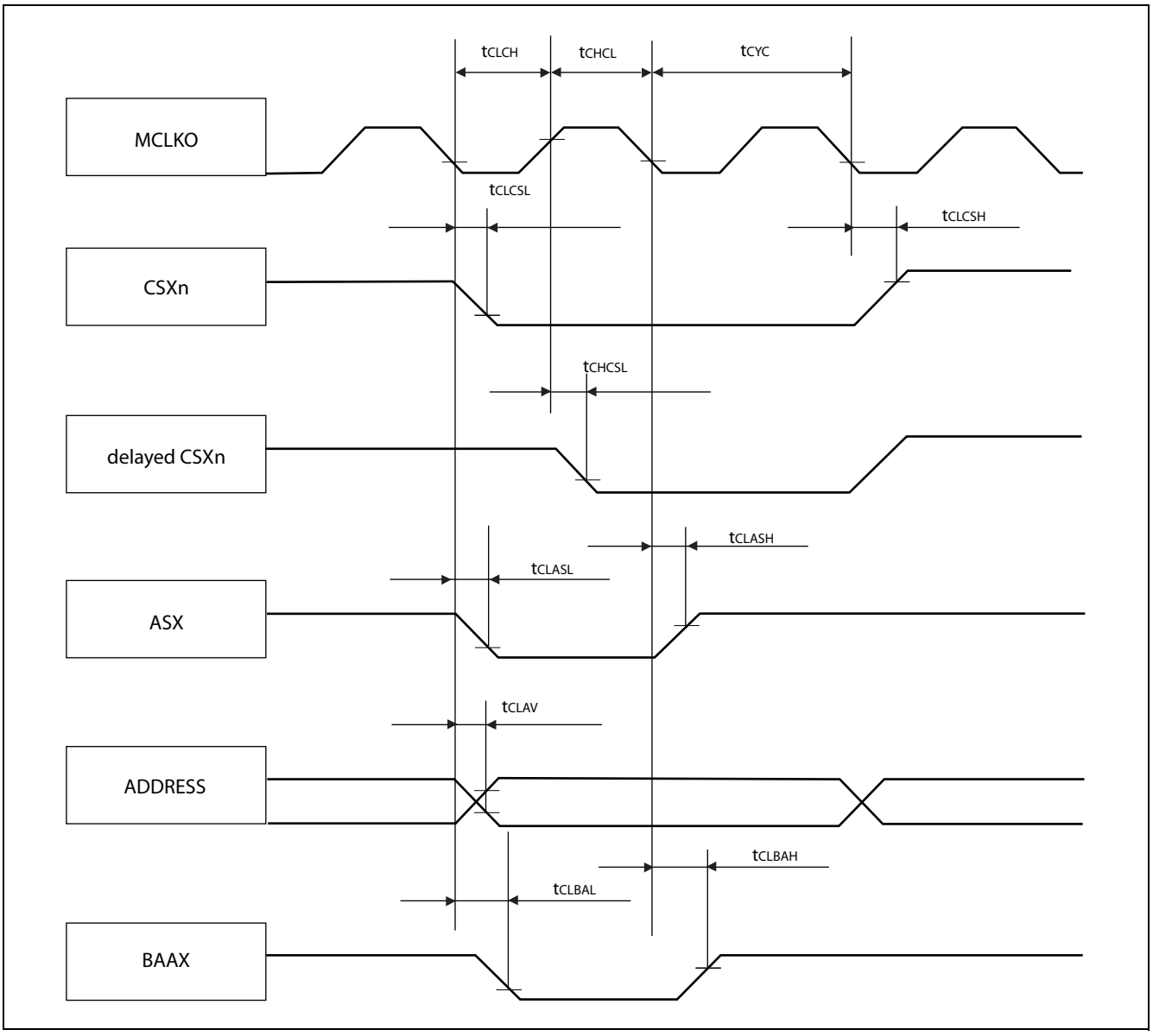
- ❒ IO_{drive} = 5 mA
- ❒ $V_{DD}35$ = 4.5 V to 5.5 V, I_{load} = 5 mA
- ❒ $V_{SS}5$ = 0 V
- ❒ Ta = – 40 °C to + 105 °C
- ❒ C_l = 50 pF
- ❒ VOL = 0.5 × $V_{DD}35$
- ❒ VOH = 0.5 × $V_{DD}35$
- ❒ EPILR = 0, PILR = 1 (Automotive Level = worst case)

Basic Timing

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO	t_{CLCH}	MCLKO	1/2 x t_{CLKT} – 2	1/2 × t_{CLKT} + 2	ns
	t_{CHCL}		1/2 × t_{CLKT} – 2	1/2 × t_{CLKT} + 2	ns
MCLKO ↓ to CSXn delay time	t_{CLCSL}	MCLKO CSXn	–	7	ns
	t_{CLCSH}		–	7	ns
MCLKO ↑ to CSXn delay time (Addr → CS delay)	t_{CHCSL}		– 1	+ 6	ns
MCLKO ↓ to ASX delay time	t_{CLASL}	MCLKO ASX	–	7	ns
	t_{CLASH}		–	7	ns
MCLKO ↓ to BAAX delay time	t_{CLBAL}	MCLKO BAAX	–	7	ns
	t_{CLBAH}		2	–	ns
MCLKO ↓ to Address valid delay time	t_{CLAV}	MCLKO A25 to A0	–	8	ns

Note: t_{CLKT} is the cycle time of the external bus clock.

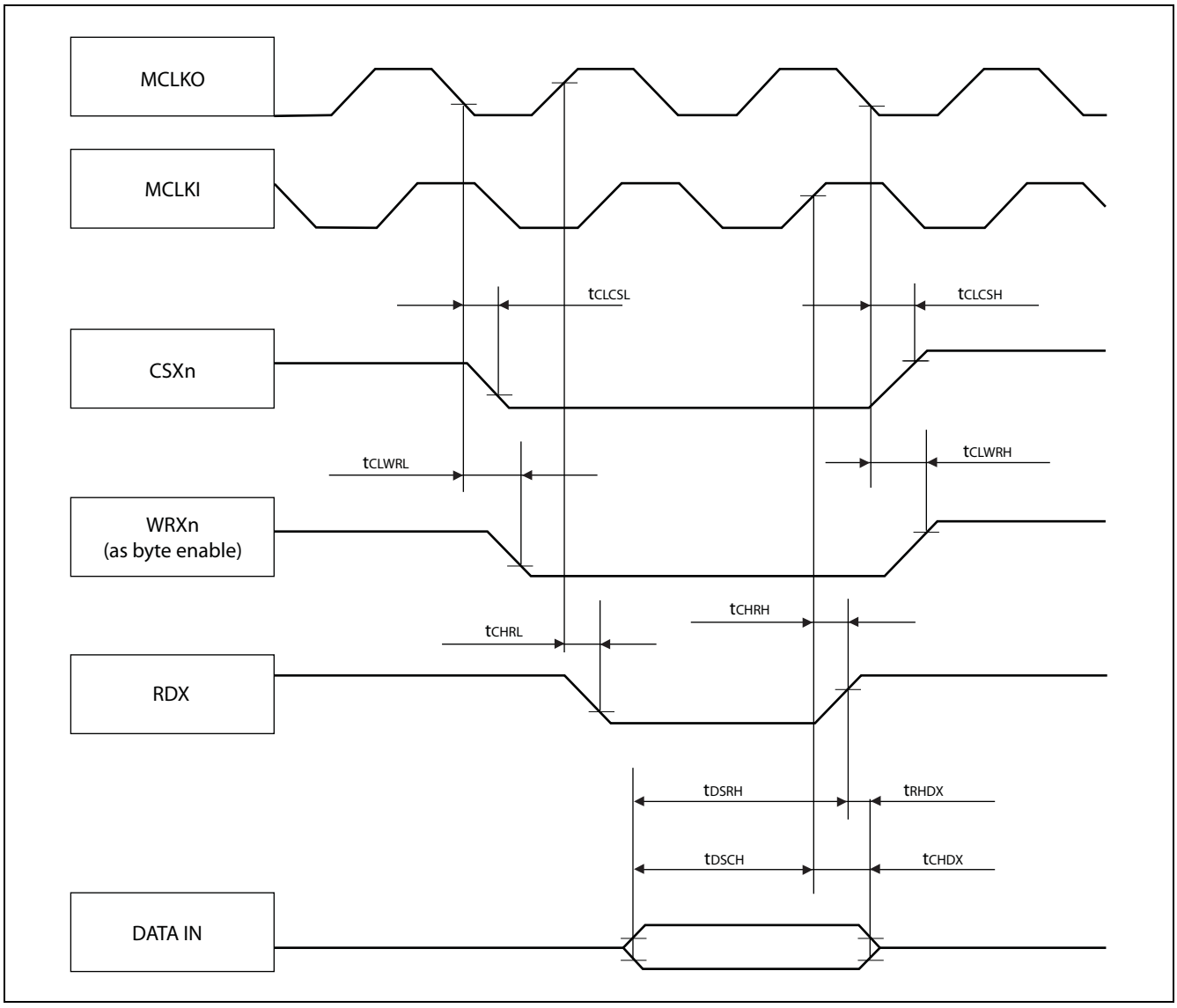

tCLCH
tCHCL
tCYC
MCLKO
tCLCSL
tCLCSH
CSXn
tCHCSL
delayed CSXn
tCLASH
tCLASL
ASX
tCLAV
ADDRESS
tCLBAH
tCLBAL
BAAX

Synchronous/Asynchronous Read Access with External MCLKI Input

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↑ /MCLKI ↑ to RDX delay time	t_{CHRL}	MCLKO RDX	– 1	6	ns
	t_{CHRH}	MCLKI RDX	8	16	ns
Data valid to RDX ↑ setup time	t_{DSRH}	RDX D31 to D0	19	—	ns
RDX ↑ to Data valid hold time (external MCLKI input)	t_{RHDX}	RDX D31 to D0	0	—	ns
Data valid to MCLKI ↑ setup time	t_{DSCH}	MCLKI D31 to D0	3	—	ns
MCLKI ↑ to Data valid hold time	t_{CHDX}	MCLKI D31 to D0	1	—	ns
MCLKO ↓ to WRXn (as byte enable) delay time	t_{CLWRL}	MCLKO WRXn	—	9	ns
	t_{CLWRH}		– 1	—	ns
MCLKO ↓ to CSXn delay time	t_{CLCSL}	MCLKO CSXn	—	7	ns
	t_{CLCSH}		—	7	ns

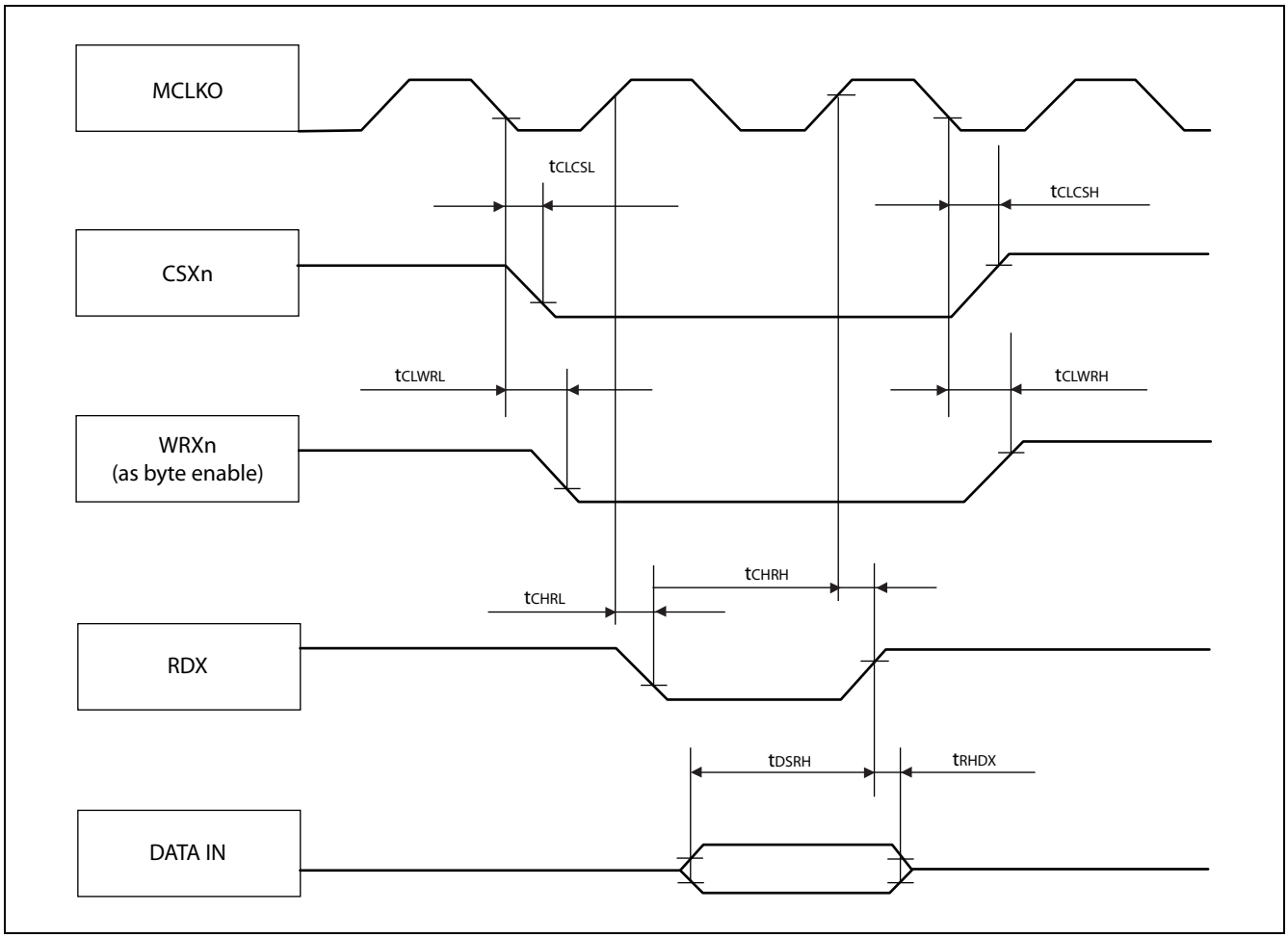
Note: The usage of the external feedback from MCLKO to MCLKI is not recommended.


MCLKO
MCLKI
tCLCSL
tCLCSH
CSXn
tCLWRL
tCLWRH
WRXn
(as byte enable)
tCHRH
tCHRL
RDX
tDSRH
tRHDX
tDSCH
tCHDX
DATA IN

Synchronous/Asynchronous Read Access with Internal MCLKO --> MCLKI Feedback

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

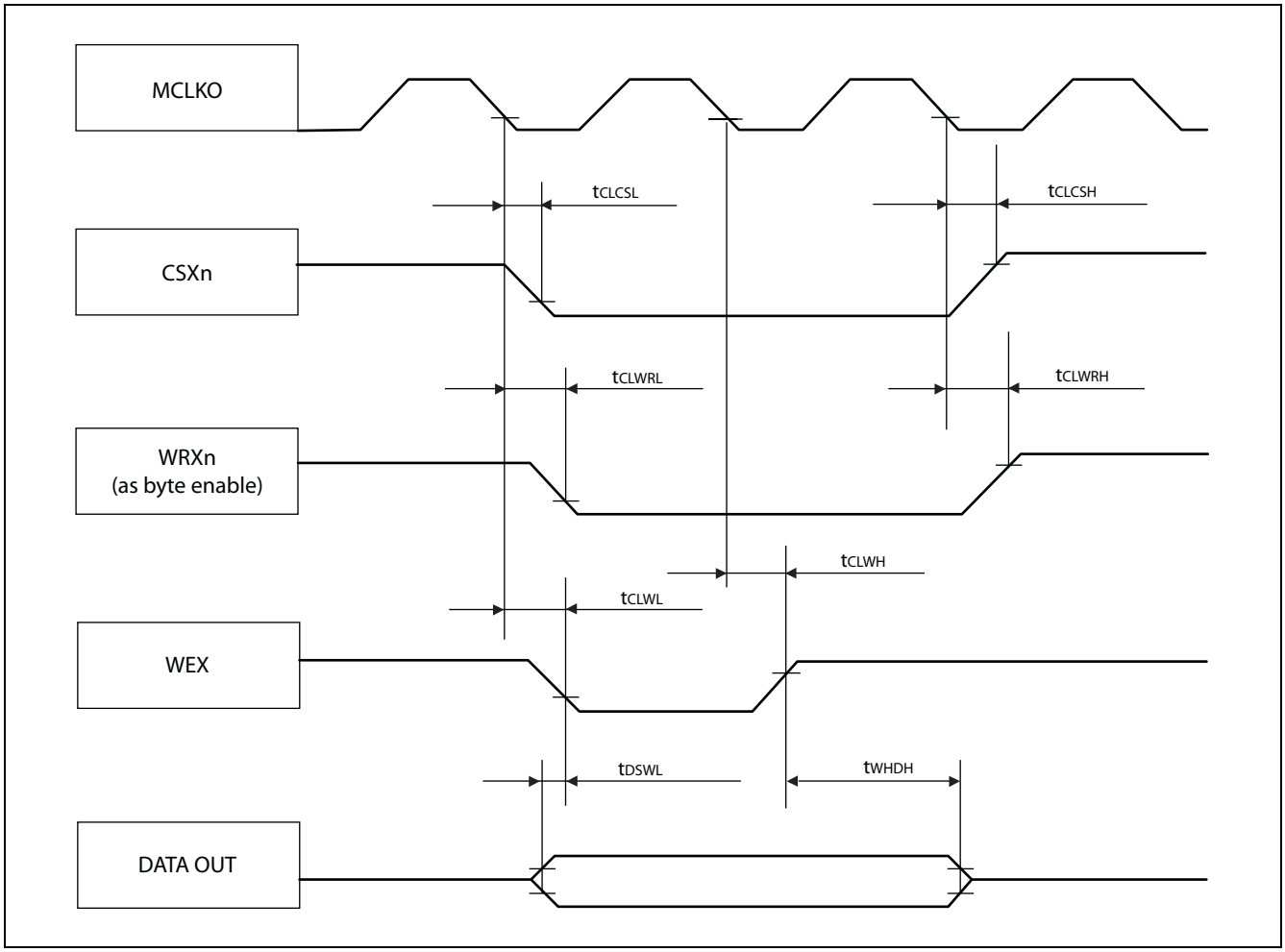
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↑ to RDX delay time	t_{CHRL}	MCLKO RDX	– 1	6	ns
	t_{CHRH}		– 1	7	ns
Data valid to RDX ↑ setup time	t_{DSRH}	RDX D31 to D0	16	—	ns
RDX ↑ to Data valid hold time (internal MCLKO → MCLKI / /MCLKI feedback)	t_{RHDX}	RDX D31 to D0	0	—	ns
MCLKO ↓ to WRXn (as byte enable) delay time	t_{CLWRL}	MCLKO WRXn	—	9	ns
	t_{CLWRH}		– 1	—	ns
MCLKO ↓ to CSXn delay time	t_{CLCSL}	MCLKO CSXn	—	7	ns
	t_{CLCSH}		—	7	ns



Synchronous Write Access - Byte Control Type

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

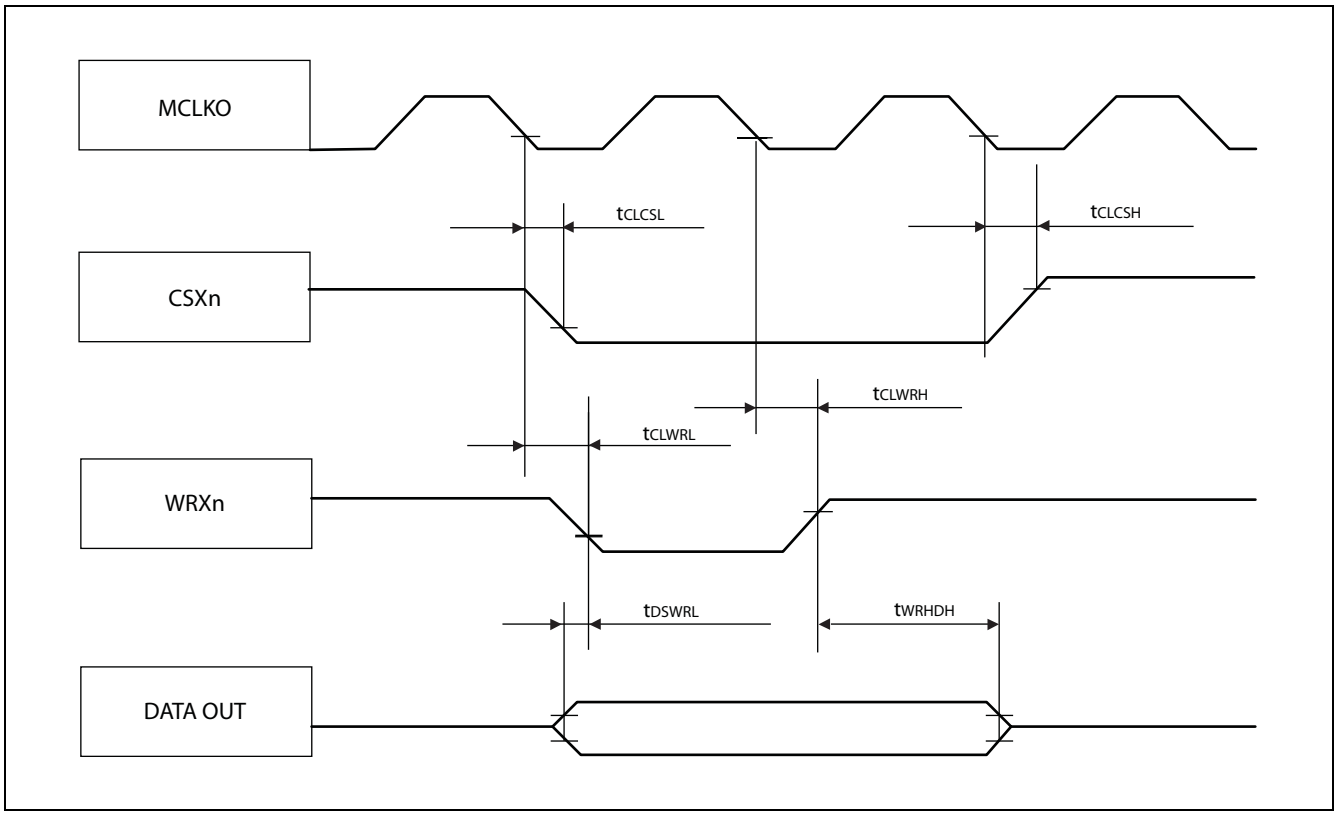
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↓ to WEX delay time	t_{CLWL}	MCLKO WEX	–	7	ns
	t_{CLWH}		2	–	ns
Data valid to WEX ↓ setup time	t_{DSWL}	WEX D31 to D0	– 4	–	ns
WEX ↑ to Data valid hold time	t_{WHDH}	WEX D31 to D0	t_{CLKT} – 5	–	ns
MCLKO ↓ to WRXn (as byte enable) delay time	t_{CLWRL}	MCLKO WRXn	–	9	ns
	t_{CLWRH}		– 1	–	ns
MCLKO ↓ to CSXn delay time	t_{CLCSL}	MCLKO CSXn	–	7	ns
	t_{CLCSH}		–	7	ns



Synchronous Write Access - No Byte Control Type

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

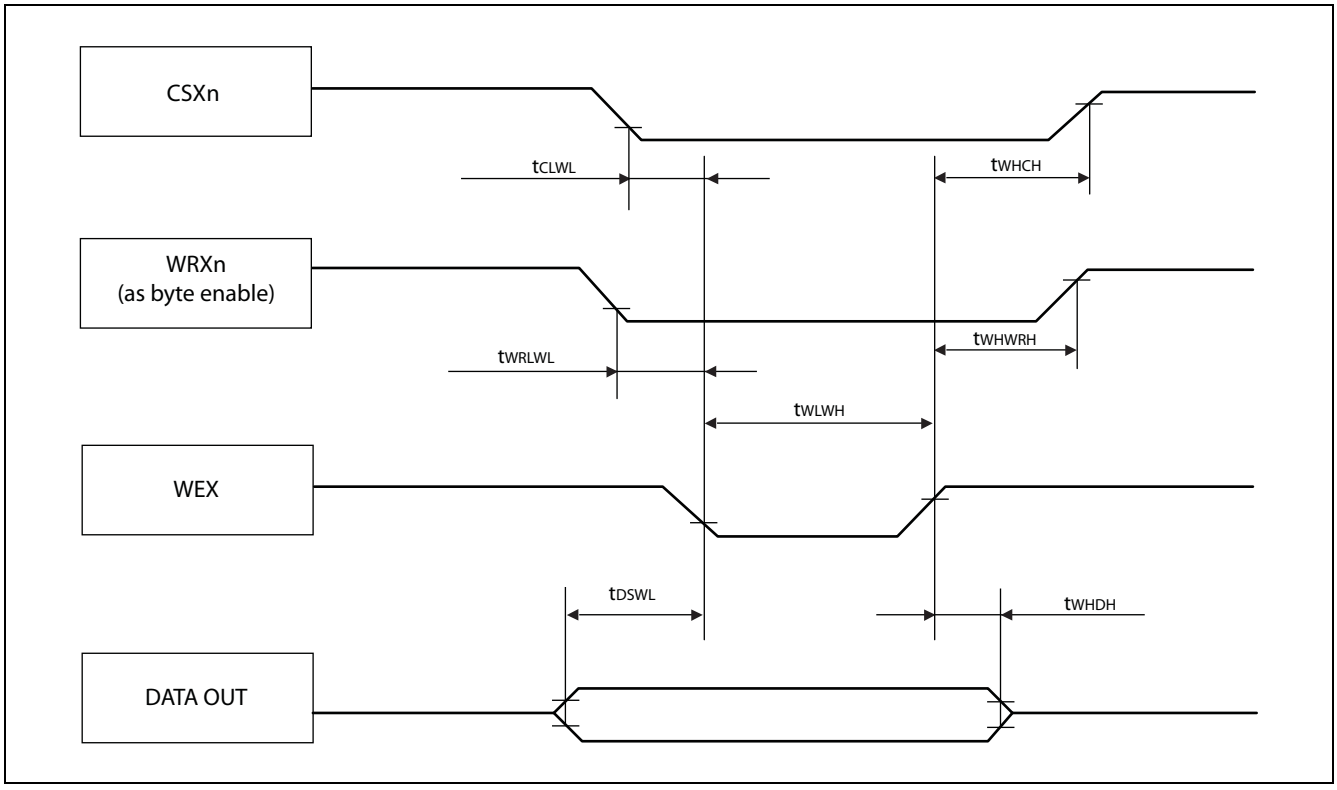
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↓ to WRXn delay time	t_{CLWRL}	MCLKO WRXn	—	9	ns
	t_{CLWRH}		– 1	—	ns
Data valid to WRXn ↓ setup time	t_{DSWRL}	WRXn D31 to D0	– 6	—	ns
WRXn ↑ to Data valid hold time	t_{WRHDH}	WRXn D31 to D0	t_{CLKT} – 6	—	ns
MCLKO ↓ to CSXn delay time	t_{CLCSL}	MCLKO CSXn	—	7	ns
	t_{CLCSH}		—	7	ns



Asynchronous Write Access - Byte Control Type

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

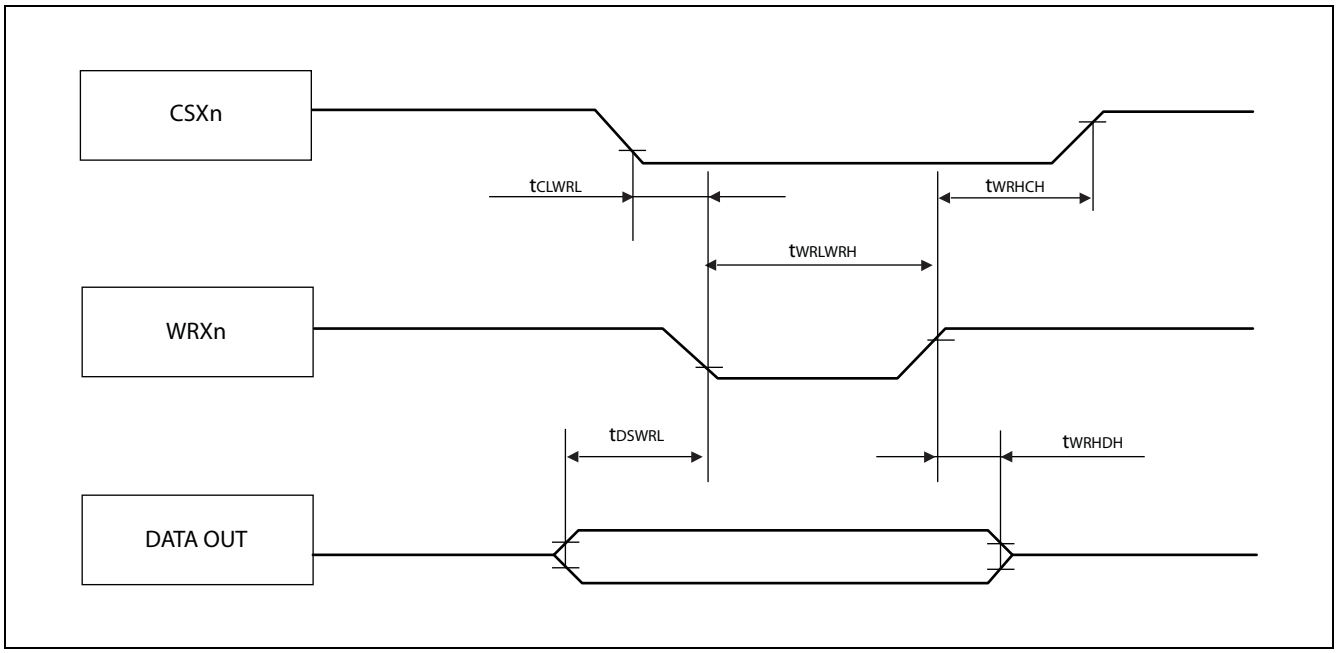
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
WEX ↓ to WEX ↑ pulse width	t_{WLWH}	WEX	$t_{CLKT} - 2$	—	ns
Data valid to WEX ↓ setup time	t_{DSWL}	WEX D31 to D0	$1/2 \times t_{CLKT} - 16$	—	ns
WEX ↑ to Data valid hold time	t_{WHDH}	WEX D31 to D0	$1/2 \times t_{CLKT} - 6$	—	ns
WEX to WRXn delay time	t_{WRLWL}	WEX WRXn	—	$1/2 \times t_{CLKT} + 2$	ns
	t_{WHWRH}		$1/2 \times t_{CLKT} - 1$	—	ns
WEX to CSXn delay time	t_{CLWL}	WEX CSXn	—	$1/2 \times t_{CLKT} + 1$	ns
	t_{WHCH}		$1/2 \times t_{CLKT} - 1$	—	ns



Asynchronous Write Access - No Byte Control Type

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

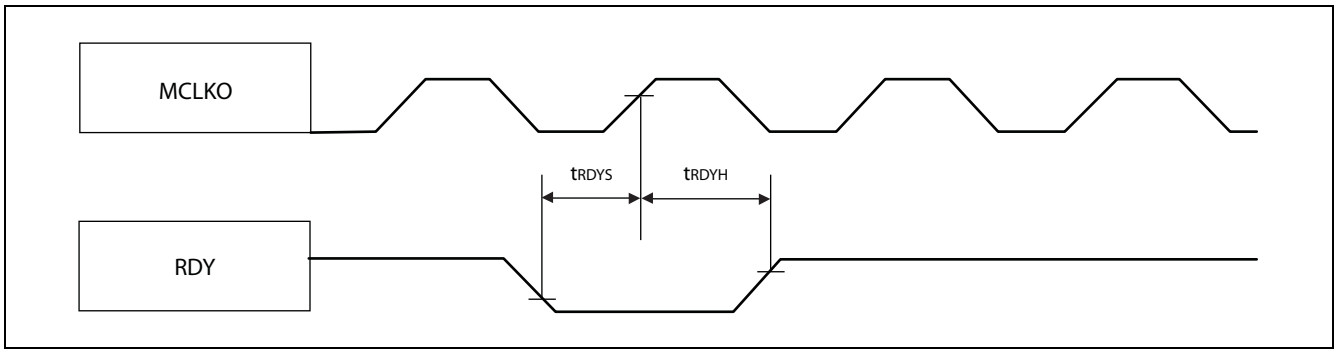
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
WRXn ↓ to WRXn ↑ pulse width	t_{WRLWRH}	WRXn	$t_{CLKT} - 1$	—	ns
Data valid to WRXn ↓ setup time	t_{DSWRL}	WRXn D31 to D0	$1/2 \times t_{CLKT} - 6$	—	ns
WRXn ↑ to Data valid hold time	t_{WRHDH}	WRXn D31 to D0	$1/2 \times t_{CLKT} - 6$	—	ns
WRXn to CSXn delay time	t_{CLWRL}	WRXn CSXn	—	$1/2 \times t_{CLKT} - 1$	ns
	t_{WRHCH}		$1/2 \times t_{CLKT} - 2$	—	ns



RDY Waitcycle Insertion

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
RDY setup time	t_{RDYS}	MCLKO RDY	12	—	ns
RDY hold time	t_{RDYH}	MCLKO RDY	0	—	ns



Bus Hold Timing

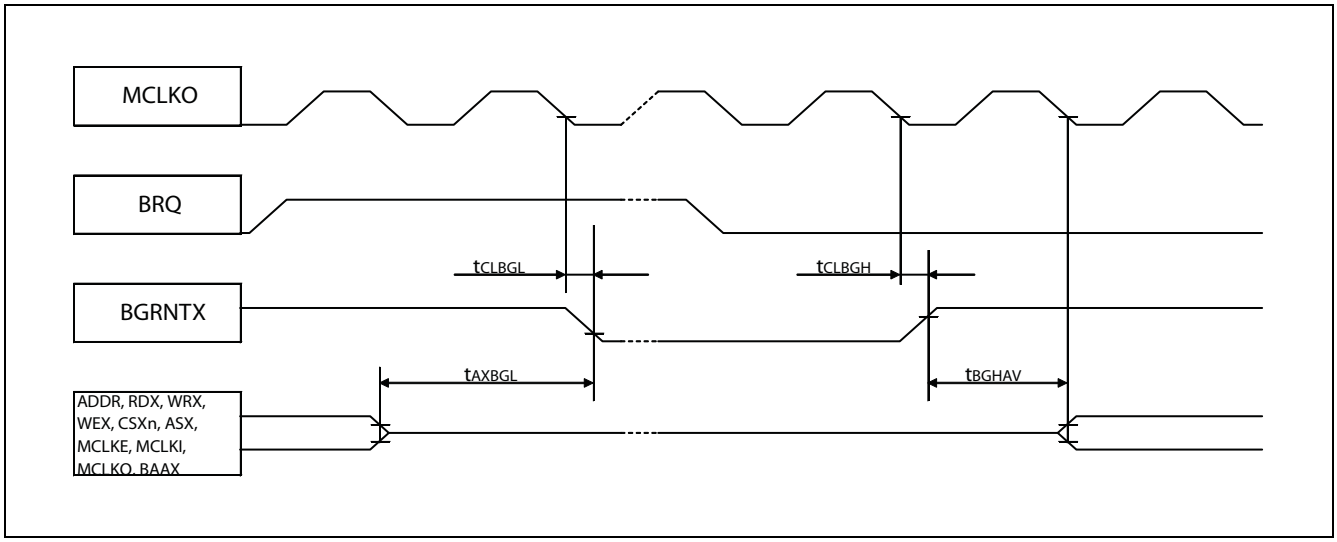
($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↓ to BGRNTX delay time	t_{CLBGL}	MCLKO BGRNTX	–	5	ns
	t_{CLBGH}		–	6	ns
Bus HIZ to BGRNTX ↓	t_{AXBGL}	BGRNTX MCLK* A0 to An RDX, ASX WRXn,WEX CSXn,BAAX	t_{CLKT} + 5	–	ns
BGRNTX ↑ to Bus drive	t_{BGHAV}		t_{CLKT} + 6	–	ns

Note: BRQ must be kept High until the bus is granted (this is acknowledged by the falling edge of BGRNTX). It must be kept High as long as the bus shall be hold. After releasing the bus (BRQ set to Low) this is acknowledged by the rising edge of BGRNTX.

Note: Condition for t_{AXBGL} and t_{BGHAV}:

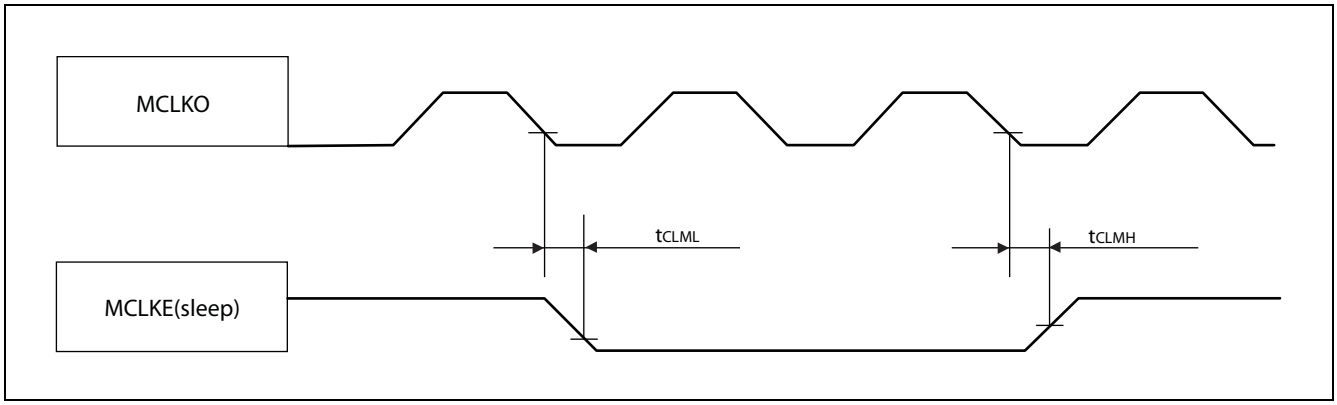
- VOL = 0.2 × $V_{DD}35$
- VOH = 0.8 × $V_{DD}35$



Clock Relationships

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↓ to MCLKE (in sleep mode)	t_{CLML}	MCLKO MCLKE	–	7	ns
	t_{CLMH}		– 1	–	ns

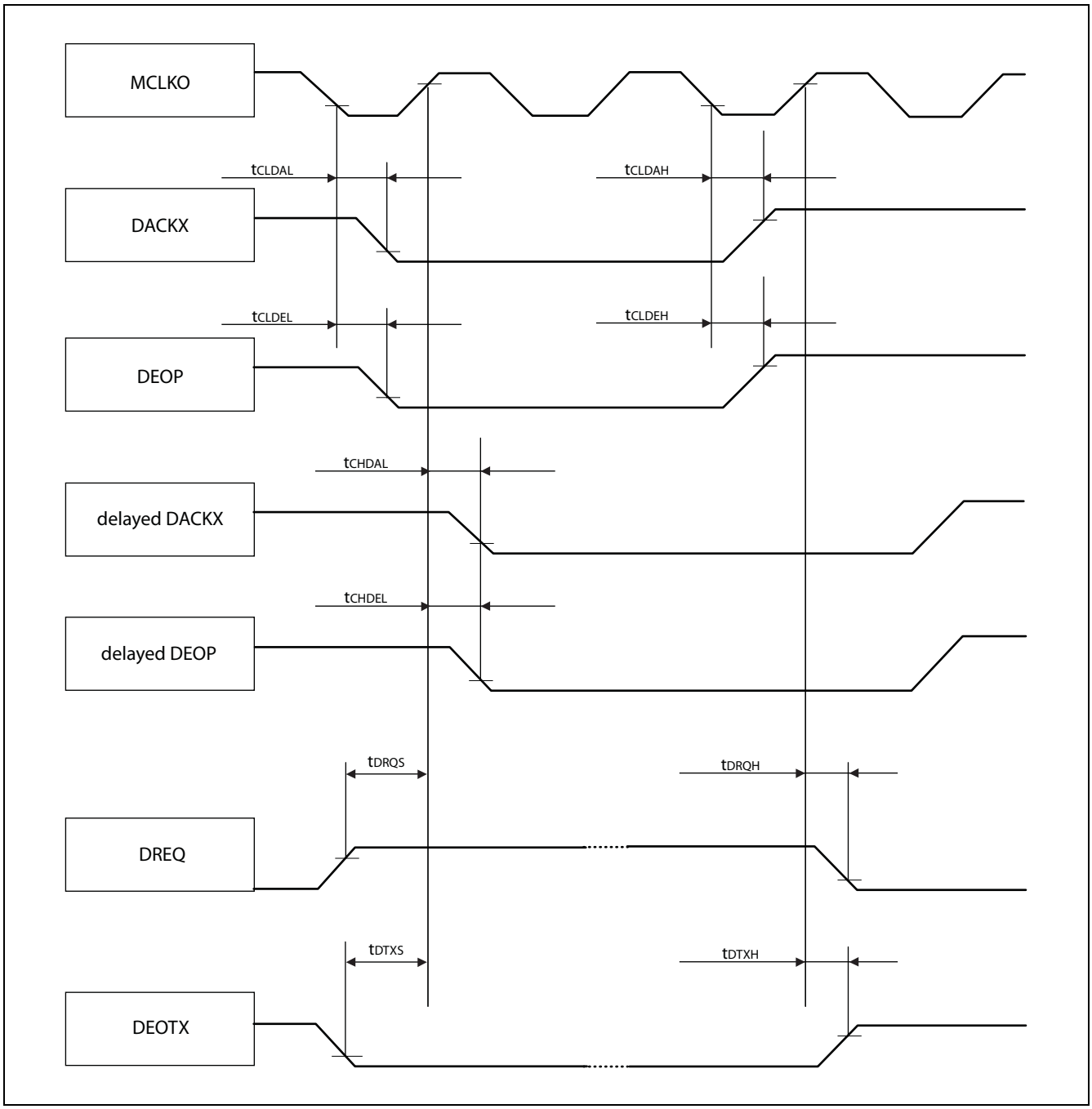


DMA Transfer

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↓ to DACKX delay time	t_{CLDAL}	MCLKO DACKXn	–	7	ns
	t_{CLDAH}		–	7	ns
MCLKO ↓ to DEOP delay time	t_{CLDEL}	MCLKO DEOPn	–	9	ns
	t_{CLDEH}		–	9	ns
MCLKO ↑ to DACKX delay time (ADDR → delayed CS)	t_{CHDAL}	MCLKO DACKXn	1	6	ns
MCLKO ↑ to DEOP delay time (ADDR → delayed CS)	t_{CHDEL}	MCLKO DEOPn	1	8	ns
DREQ setup time	t_{DRQS}	MCLKO DREQn	12	–	ns
DREQ hold time	t_{DRQH}	MCLKO DREQn	0	–	ns
DEOTXn setup time	t_{DTXS}	MCLKO DEOTXn	12	–	ns
DEOTXn hold time	t_{DTXH}	MCLKO DEOTXn	0	–	ns

Note: DREQ and DEOTX must be applied for at least $5 \times t_{CLKT}$ to ensure that they are really sampled and evaluated. Under best case conditions (DMA not busy) only setup and hold times are required.


MCLKO
tCLDAL
tCLDAH
DACKX
tCLDEL
tCLDEH
DEOP
tCHDAL
delayed DACKX
tCHDEL
delayed DEOP
tDRQS
tDRQH
DREQ
tDTXS
tDTXH
DEOTX

20.7.8 External Bus AC Timings at $V_{DD}35$ = 3.0 to 4.5 V

■ Conditions during AC measurements

All AC tests were measured under the following conditions:

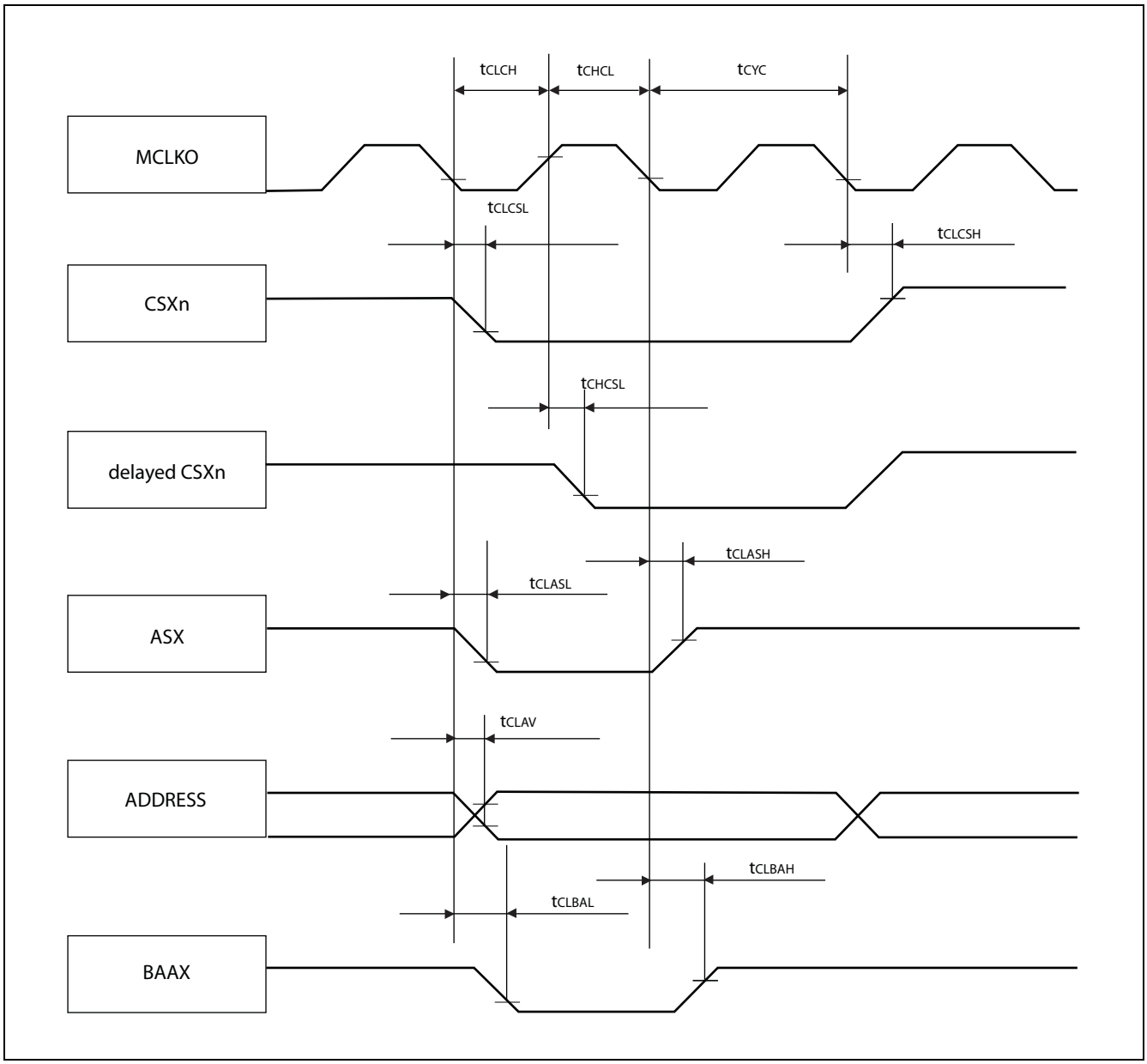
- ❒ IO_{drive} = 5 mA
- ❒ $V_{DD}35$ = 3.0 V to 4.5 V, I_{load} = 3 mA
- ❒ $V_{SS}5$ = 0 V
- ❒ Ta = – 40 °C to + 105 °C
- ❒ C_l = 50 pF
- ❒ VOL = 0.5 × $V_{DD}35$
- ❒ VOH = 0.5 × $V_{DD}35$
- ❒ EPILR = 0, PILR = 1 (Automotive Level = worst case)

Basic Timing

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO	t_{CLCH}	MCLKO	1/2 × t_{CLKT} – 2	1/2 × t_{CLKT} + 4	ns
	t_{CHCL}		1/2 × t_{CLKT} – 4	1/2 × t_{CLKT} + 2	ns
MCLKO ↓ to CSXn delay time	t_{CLCSL}	MCLKO CSXn	–	6	ns
	t_{CLCSH}		–	8	ns
MCLKO ↑ to CSXn delay time (Addr → CS delay)	t_{CHCSL}		– 1	+ 5	ns
MCLKO ↓ to ASX delay time	t_{CLASL}	MCLKO ASX	–	7	ns
	t_{CLASH}		–	9	ns
MCLKO ↓ to BAAX delay time	t_{CLBAL}	MCLKO BAAX	–	7	ns
	t_{CLBAH}		2	–	ns
MCLKO ↓ to Address valid delay time	t_{CLAV}	MCLKO A25 to A0	–	13	ns

Note: t_{CLKT} is the cycle time of the external bus clock.

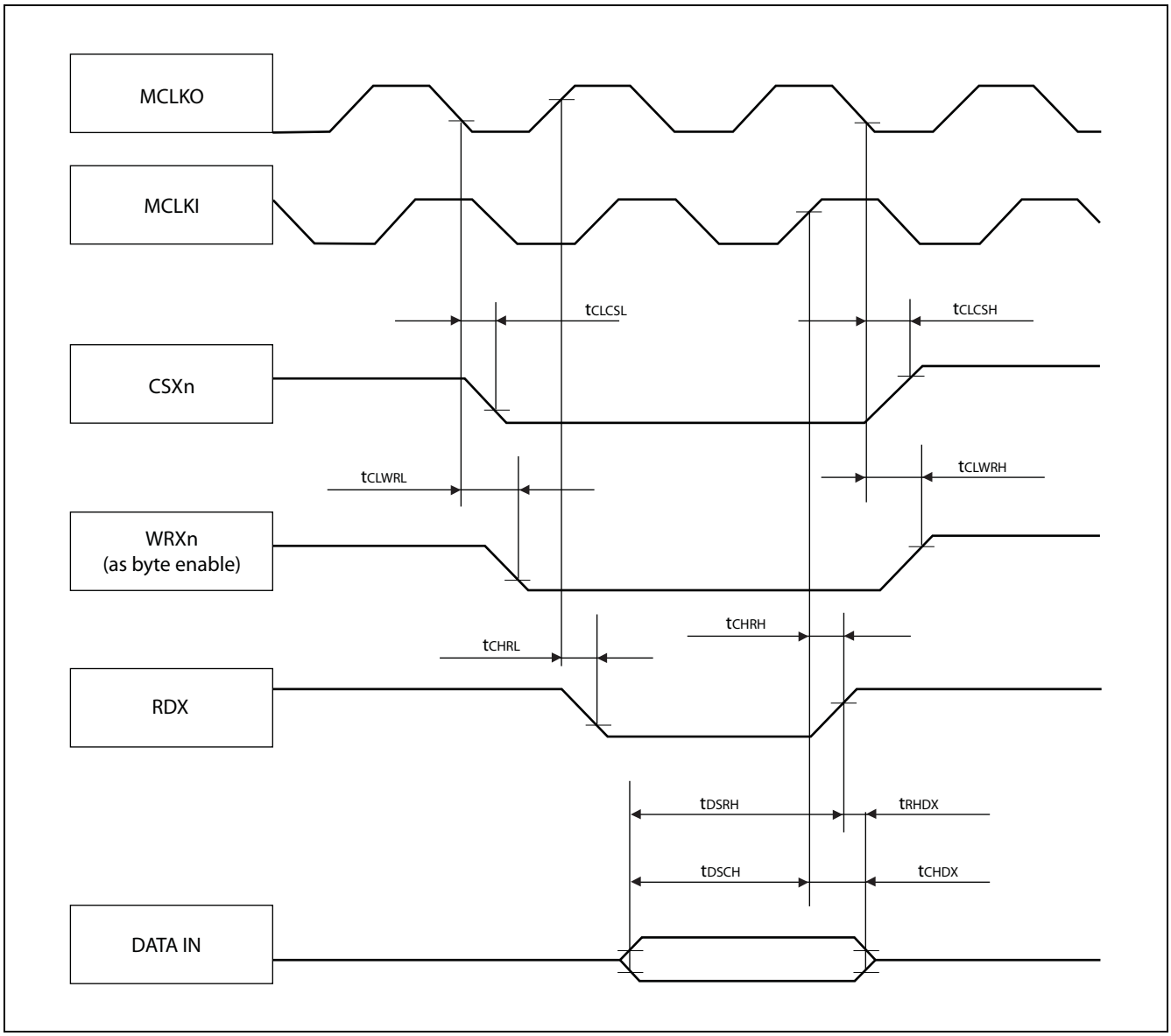

tCLCH
tCHCL
tCYC
MCLKO
tCLCSL
tCLCSH
CSXn
tCHCSL
delayed CSXn
tCLASH
tCLASL
ASX
tCLAV
ADDRESS
tCLBAH
tCLBAL
BAAX

Synchronous/Asynchronous Read Access with External MCLKI Input

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↑/MCLKI ↑ to RDX delay time	t_{CHRL}	MCLKO RDX	– 1	5	ns
	t_{CHRH}	MCLKI RDX	8	16	ns
Data valid to RDX ↑ setup time	t_{DSRH}	RDX D31 to D0	19	—	ns
RDX ↑ to Data valid hold time (external MCLKI input)	t_{RHDX}	RDX D31 to D0	0	—	ns
Data valid to MCLKI ↑ setup time	t_{DSCH}	MCLKI D31 to D0	3	—	ns
MCLKI ↑ to Data valid hold time	t_{CHDX}	MCLKI D31 to D0	1	—	ns
MCLKO ↓ to WRXn (as byte enable) delay time	t_{CLWRL}	MCLKO WRXn	—	12	ns
	t_{CLWRH}		0	—	ns
MCLKO ↓ to CSXn delay time	t_{CLCSL}	MCLKO CSXn	—	6	ns
	t_{CLCSH}		—	9	ns

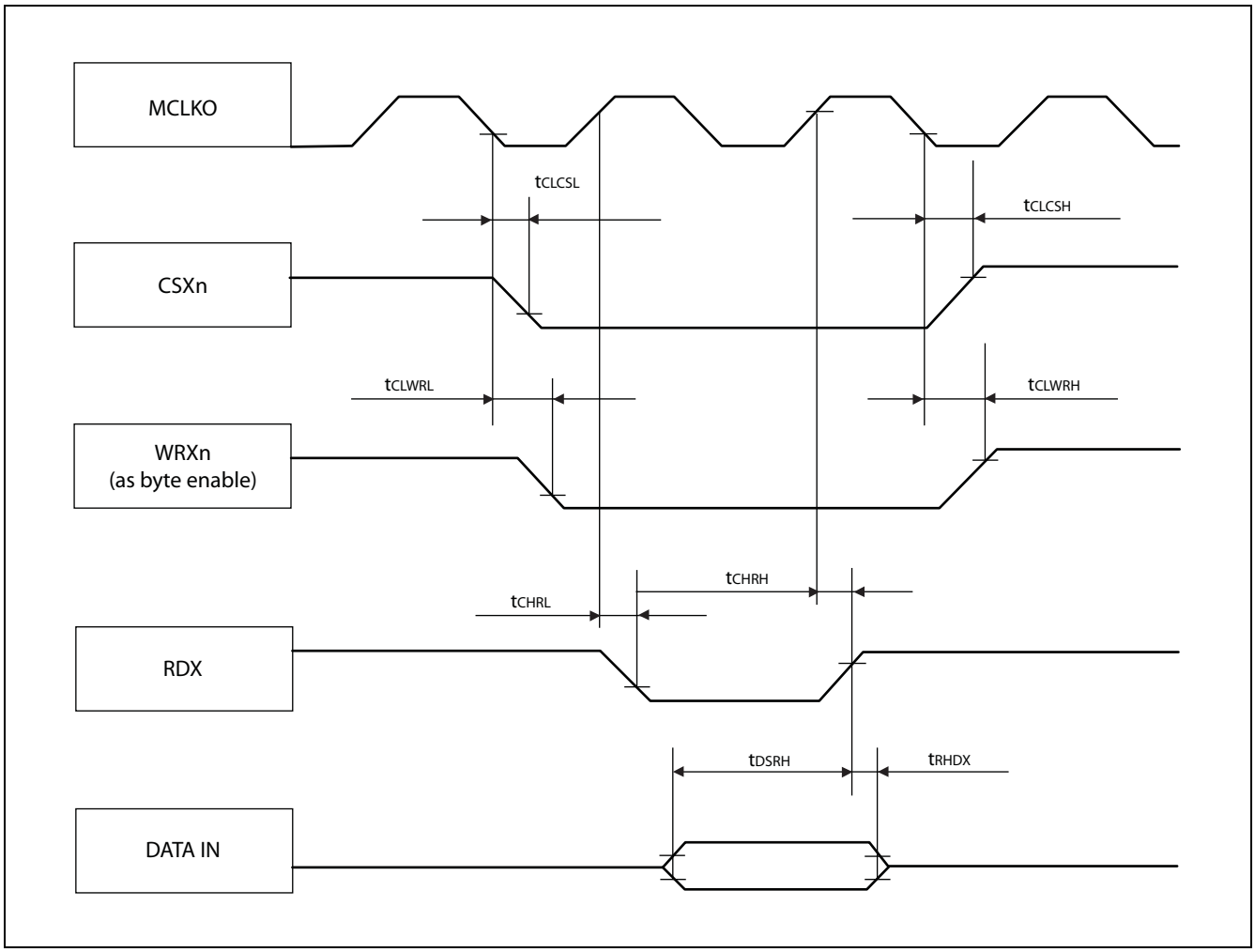
Note: The usage of the external feedback from MCLKO to MCLKI is not recommended.


MCLKO
MCLKI
tCLCSL
tCLCSH
CSXn
tCLWRL
tCLWRH
WRXn
(as byte enable)
tCHRH
tCHRL
RDX
tDSRH
tRHDX
tDSCH
tCHDX
DATA IN

Synchronous/Asynchronous Read Access with Internal MCLKO --> MCLKI Feedback

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

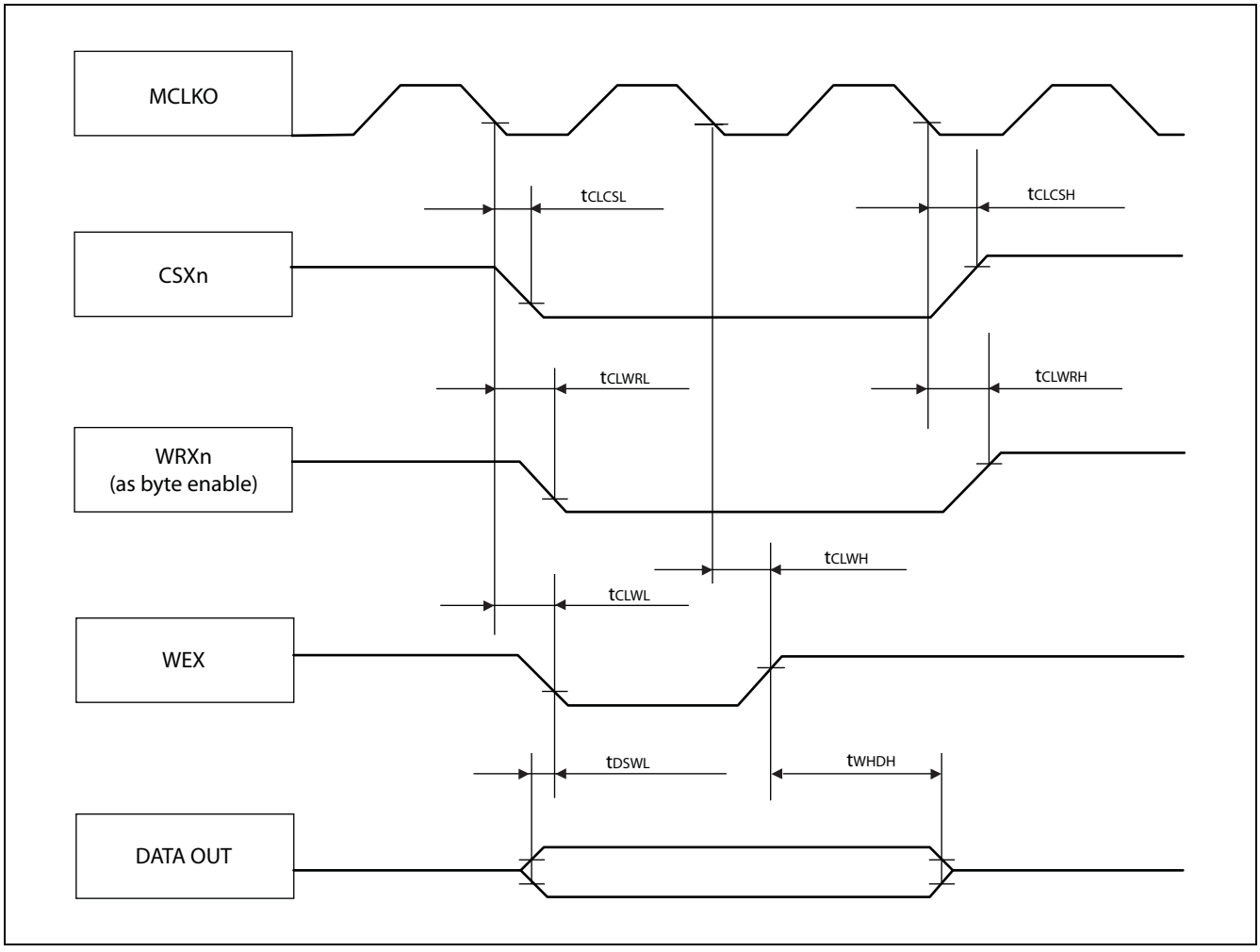
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↑ to RDX delay time	t_{CHRL}	MCLKO RDX	– 1	5	ns
	t_{CHRH}		– 1	7	ns
Data valid to RDX ↑ setup time	t_{DSRH}	RDX D31 to D0	18	—	ns
RDX ↑ to Data valid hold time (internal MCLKO → MCLKI / /MCLKI feedback)	t_{RHDX}	RDX D31 to D0	0	—	ns
MCLKO ↓ to WRXn (as byte enable) delay time	t_{CLWRL}	MCLKO WRXn	—	12	ns
	t_{CLWRH}		0	—	ns
MCLKO ↓ to CSXn delay time	t_{CLCSL}	MCLKO CSXn	—	6	ns
	t_{CLCSH}		—	8	ns



Synchronous Write Access - Byte Control Type

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

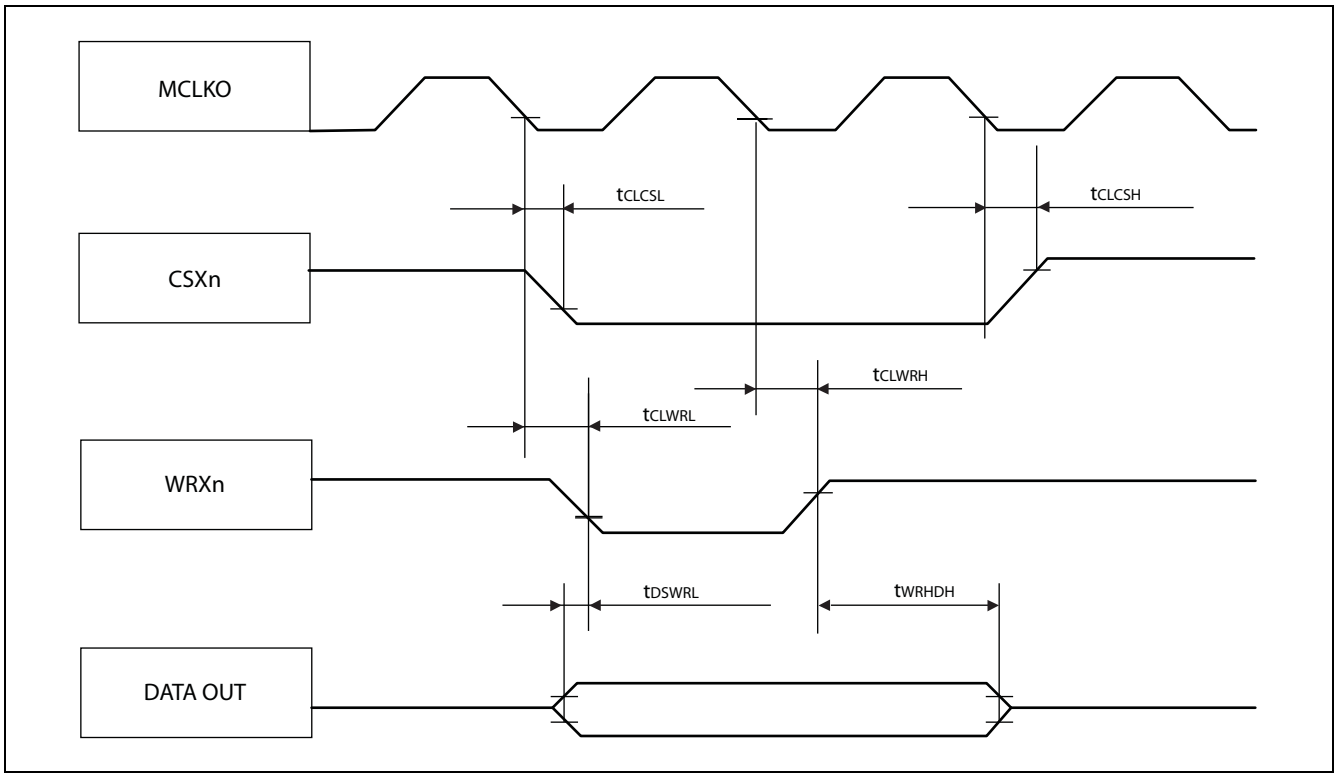
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↓ to WEX delay time	t_{CLWL}	MCLKO WEX	–	7	ns
	t_{CLWH}		1	–	ns
Data valid to WEX ↓ setup time	t_{DSWL}	WEX D31 to D0	– 11	–	ns
WEX ↑ to Data valid hold time	t_{WHDH}	WEX D31 to D0	t_{CLKT} – 5	–	ns
MCLKO ↓ to WRXn (as byte enable) delay time	t_{CLWRL}	MCLKO WRXn	–	12	ns
	t_{CLWRH}		0	–	ns
MCLKO ↓ to CSXn delay time	t_{CLCSL}	MCLKO CSXn	–	6	ns
	t_{CLCSH}		–	8	ns



Synchronous Write Access - No Byte Control Type

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

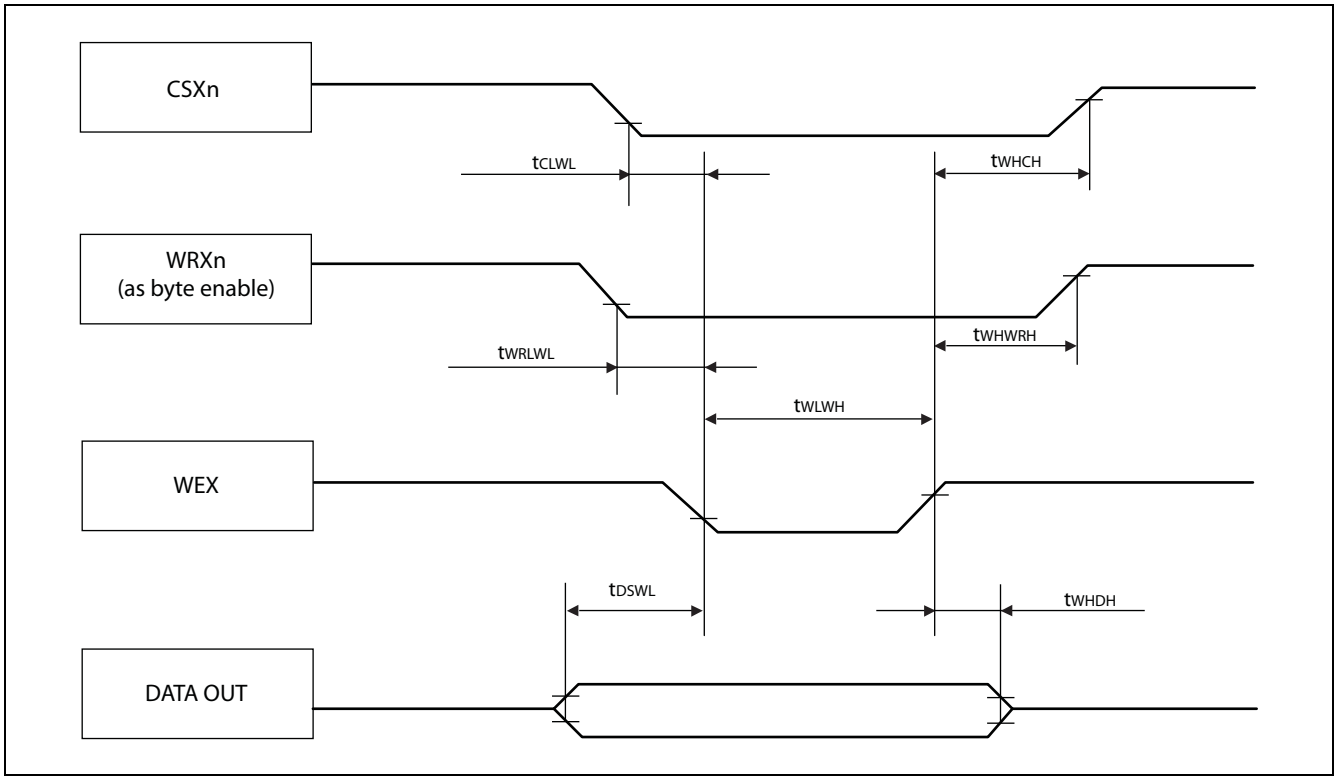
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↓ to WRXn delay time	t_{CLWRL}	MCLKO WRXn	–	12	ns
	t_{CLWRH}		0	–	ns
Data valid to WRXn ↓ setup time	t_{DSWRL}	WRXn D31 to D0	– 11	–	ns
WRXn ↑ to Data valid hold time	t_{WRHDH}	WRXn D31 to D0	t_{CLKT} – 6	–	ns
MCLKO ↓ to CSXn delay time	t_{CLCSL}	MCLKO CSXn	–	6	ns
	t_{CLCSH}		–	8	ns



Asynchronous Write Access - Byte Control Type

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

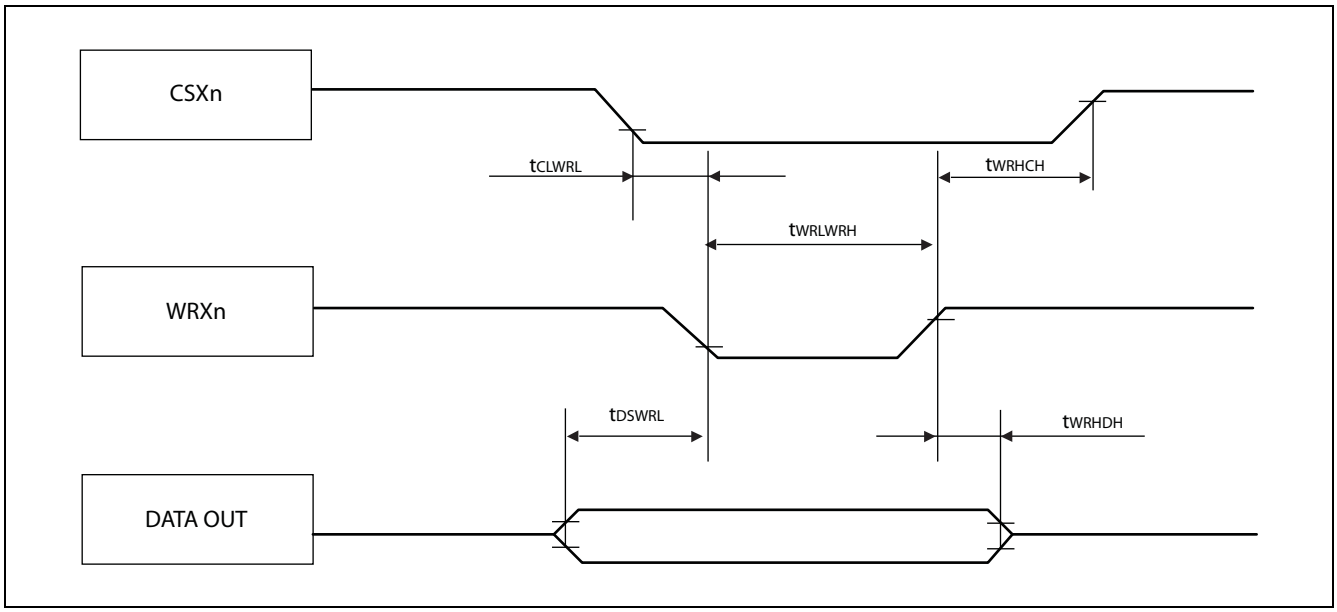
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
WEX ↓ to WEX ↑ pulse width	t_{WLWH}	WEX	$t_{CLKT} - 2$	—	ns
Data valid to WEX ↓ setup time	t_{DSWL}	WEX D31 to D0	$1/2 \times t_{CLKT} - 11$	—	ns
WEX ↑ to Data valid hold time	t_{WHDH}	WEX D31 to D0	$1/2 \times t_{CLKT} - 6$	—	ns
WEX to WRXn delay time	t_{WRLWL}	WEX WRXn	—	$1/2 \times t_{CLKT} + 3$	ns
	t_{WHWRH}		$1/2 \times t_{CLKT} - 3$	—	ns
WEX to CSXn delay time	t_{CLWL}	WEX CSXn	—	$1/2 \times t_{CLKT} - 3$	ns
	t_{WHCH}		$1/2 \times t_{CLKT} - 3$	—	ns



Asynchronous Write Access - No Byte Control Type

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

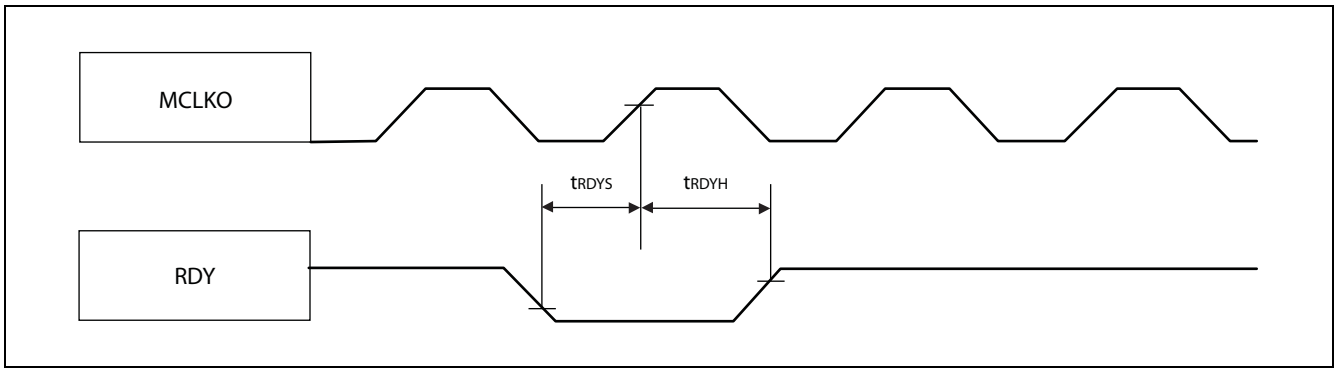
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
WRXn ↓ to WRXn ↑ pulse width	t_{WRLWRH}	WRXn	$t_{CLKT} - 2$	—	ns
Data valid to WRXn ↓ setup time	t_{DSWRL}	WRXn D31 to D0	$1/2 \times t_{CLKT} - 11$	—	ns
WRXn ↑ to Data valid hold time	t_{WRHDH}	WRXn D31 to D0	$1/2 \times t_{CLKT} - 6$	—	ns
WRXn to CSXn delay time	t_{CLWRL}	WRXn CSXn	—	$1/2 \times t_{CLKT} - 2$	ns
	t_{WRHCH}		$1/2 \times t_{CLKT} - 3$	—	ns



RDY Waitcycle Insertion

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
RDY setup time	t_{RDYS}	MCLKO RDY	14	—	ns
RDY hold time	t_{RDYH}	MCLKO RDY	0	—	ns



Bus Hold Timing

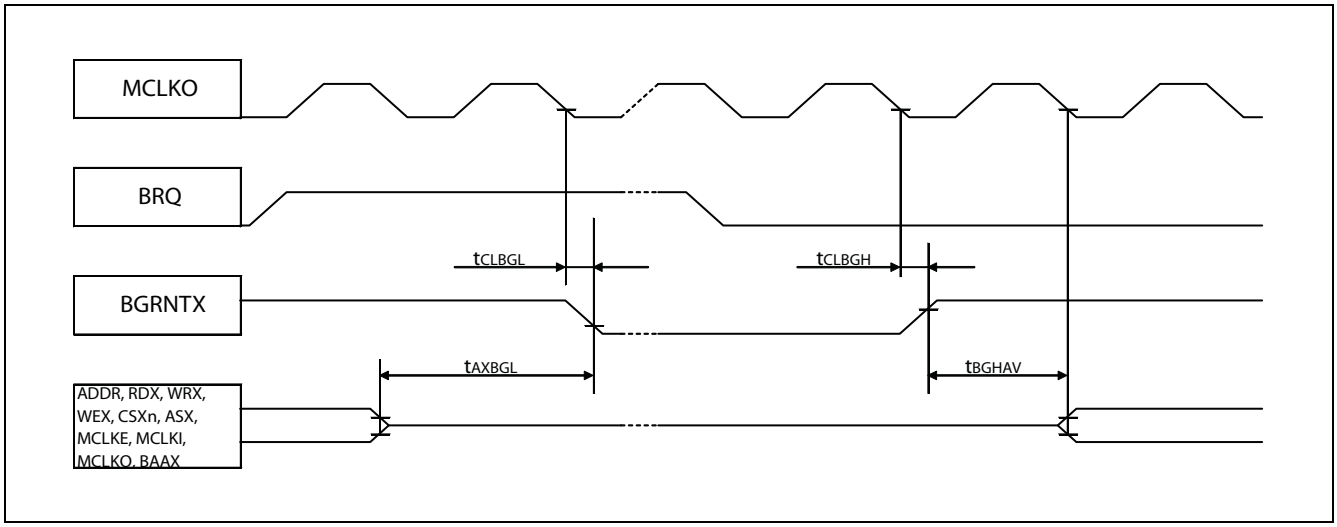
($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↓ to BGRNTX delay time	t_{CLBGL}	MCLKO BGRNTX	–	5	ns
	t_{CLBGH}		–	6	ns
Bus HIZ to BGRNTX ↓	t_{AXBGL}	BGRNTX MCLK* A0 to An RDX, ASX WRXn,WEX CSXn,BAAX	t_{CLKT} + 8	–	ns
BGRNTX ↑ to Bus drive	t_{BGHAV}		t_{CLKT} + 1	–	ns

Note: BRQ must be kept High until the bus is granted (this is acknowledged by the falling edge of BGRNTX). It must be kept High as long as the bus shall be hold. After releasing the bus (BRQ set to Low) this is acknowledged by the rising edge of BGRNTX.

Note: Condition for t_{AXBGL} and t_{BGHAV}:

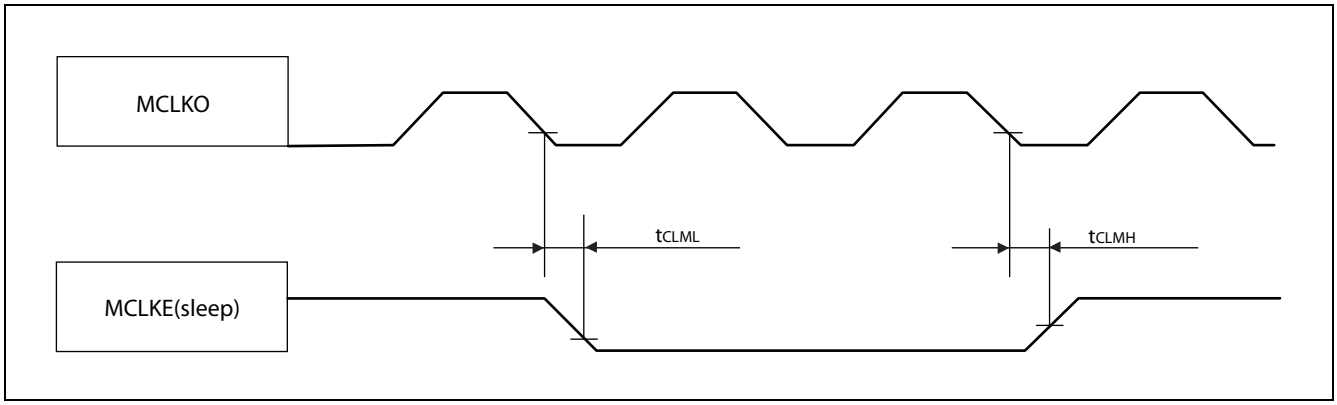
- VOL = 0.2 × $V_{DD}35$
- VOH = 0.8 × $V_{DD}35$



Clock Relationships

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↓ to MCLKE (in sleep mode)	t_{CLML}	MCLKO MCLKE	–	3	ns
	t_{CLMH}		0	–	ns

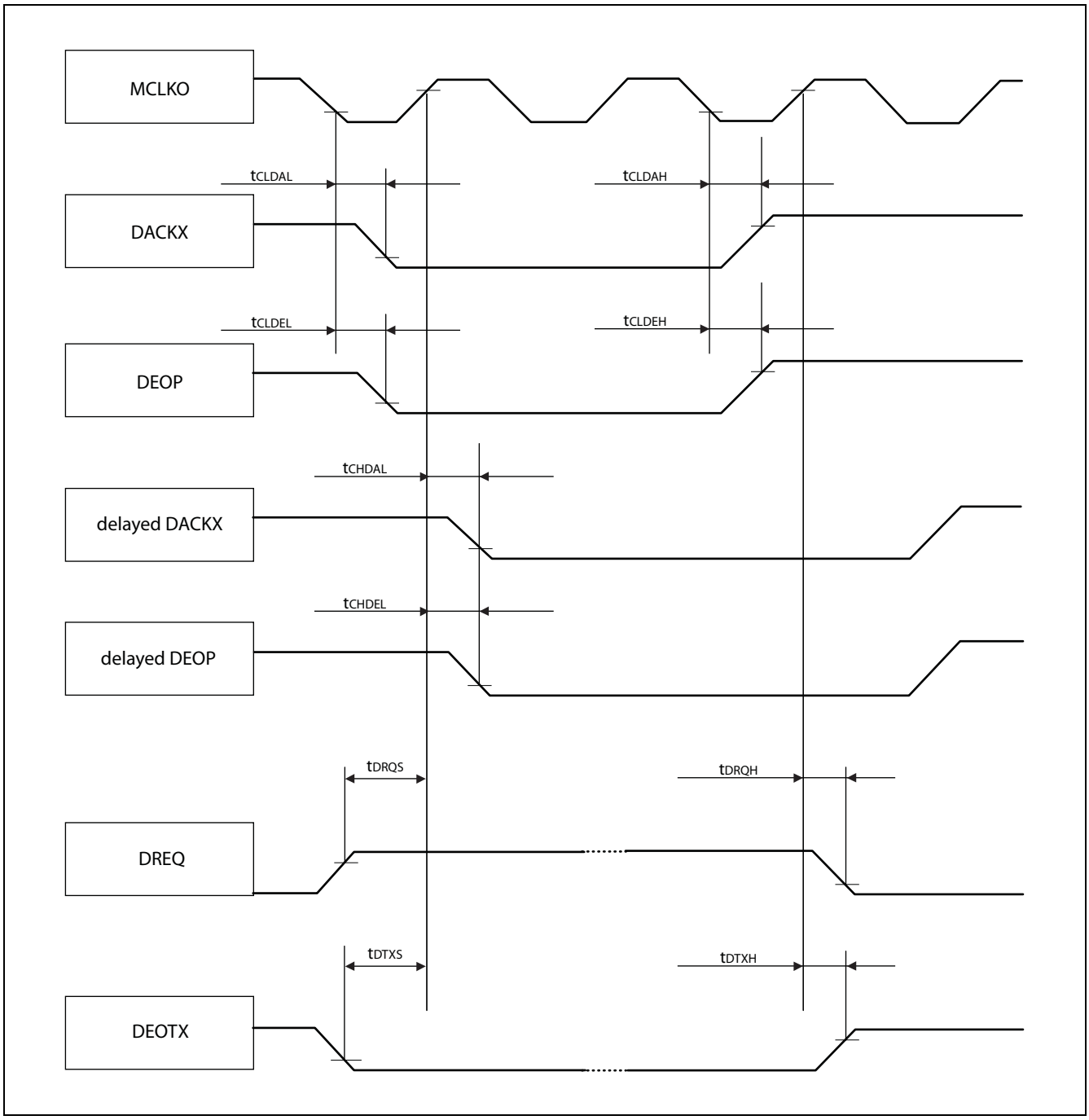


DMA Transfer

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↓ to DACKX delay time	t_{CLDAL}	MCLKO DACKXn	—	7	ns
	t_{CLDAH}		—	8	ns
MCLKO ↓ to DEOP delay time	t_{CLDEL}	MCLKO DEOPn	—	7	ns
	t_{CLDEH}		—	11	ns
MCLKO ↑ to DACKX delay time (ADDR → delayed CS)	t_{CHDAL}	MCLKO DACKXn	– 1	4	ns
MCLKO ↑ to DEOP delay time (ADDR ⟶ delayed CS)	t_{CHDEL}	MCLKO DEOPn	— 1	6	ns
DREQ setup time	t_{DRQS}	MCLKO DREQn	16	—	ns
DREQ hold time	t_{DRQH}	MCLKO DREQn	0	—	ns
DEOTXn setup time	t_{DTXS}	MCLKO DEOTXn	16	—	ns
DEOTXn hold time	t_{DTXH}	MCLKO DEOTXn	0	—	ns

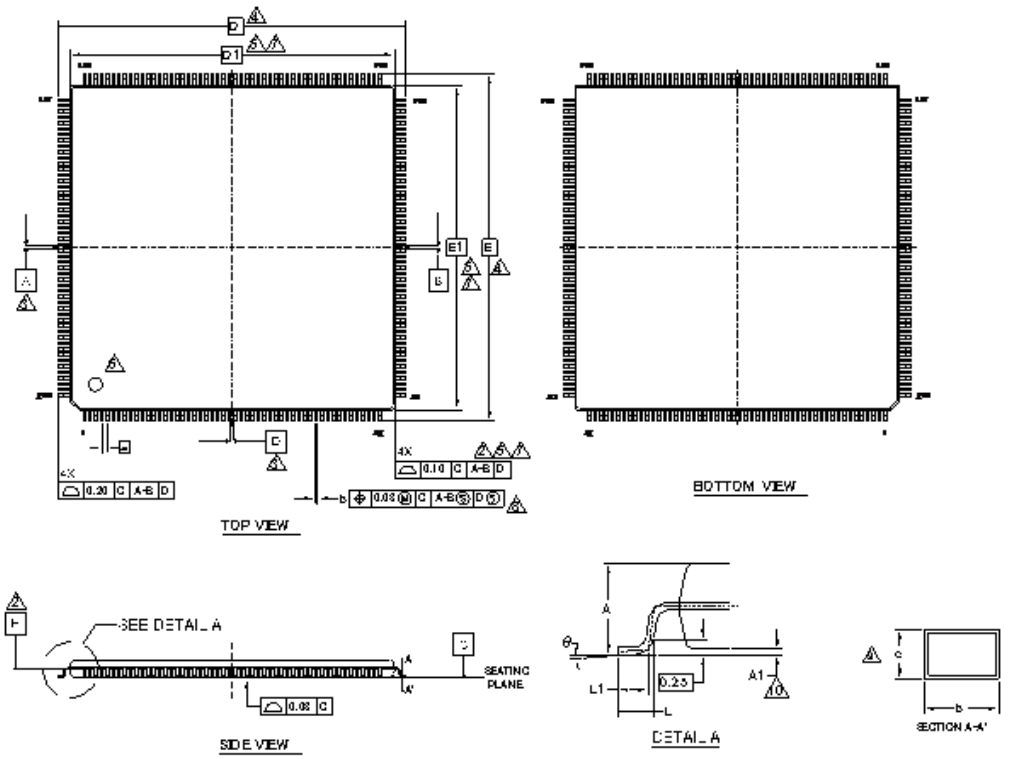
Note: DREQ and DEOTX must be applied for at least 5 × t_{CLKT} to ensure that they are really sampled and evaluated. Under best case conditions (DMA not busy) only setup and hold times are required.


MCLKO
tCLDAL
tCLDAH
DACKX
tCLDEL
tCLDEH
DEOP
tCHDAL
delayed DACKX
tCHDEL
delayed DEOP
tDRQS
tDRQH
DREQ
tDTXS
tDTXH
DEOTX

21. Ordering Information

Part number	Package	Remarks
CY91F467EAPMC-GS-UJE2	208-pin low profile QFP (LQR208)	Lead-free package

22. Package Dimension



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.09	—	0.20
D	30.00 BSC		
D1	28.00 BSC		
e	0.50 BSC		
E	30.00 BSC		
E1	28.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDED BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY

002-15151 **

PACKAGE OUTLINE, 208 LEAD LQFP
28.00x28.00x1.7 MM LQR208 REV**

23. Appendix

23.1 Revision History

Version/Date	Page	Section	Change Results
Ver. 0.01 2009-04-16	-	-	Initial version based on MB91F467D
Ver. 0.2 2009-07-03	all	all	Various updates following the proof read results on other MB91460 series datasheets
	page 68	Shutdown Mode	Chapter “Shutdown Mode” added
Ver. 0.3 2009-08-03	page 4	Product Lineup	Corrected that the software watchdog cannot be activated in SLEEP/STOP
	page 68-page 81	Chapter Shutdown Mode	Total update
	page 105	IO Map; SHDINT register	Removed bits [3:2]
	page 131	ELECTRICAL CHARACTERISTICS, Absolute maximum ratings	Permitted power dissipation (calculated) added
	page 136	DC Characteristics	Added Sum input leakage current
	page 138	A/D converter characteristics; Zero reading voltage, Full scale reading voltage	Changed the units from “LSB” into “V” and the values from <value>+<n> into <value>+<n LSB>
	page 143	AC Characteristics	Removed the AC specification temporary
	page 178	Package Dimension	Updated the the drawing of FPT-208P-M04 into FPT-208P-M06, updated the URL for download
Ver. 0.4 2009-08-04	all	Total update after first spec review	No change bars in this revision!
Ver. 0.5 2009-08-19	page 66	USART LIN/FIFO (Extension)	This chapter added for “End of Transmission” IRQ
	page 95	I/O Map	Marked all differences versus MB91F467D with colors
	page 120	Interrupt Vector Table	Added the USART “End of Transmission” IRQs

Version/Date	Page	Section	Change Results
Ver. 0.6 2009-09-08	page 76	Shutdown mode: External Interrupts: Level or Edge Setting	Added this section
	page 76	Shutdown mode: Input Voltage Selection	Added this section
	page 71	Shutdown mode: SHDINT register	Re-added bits [3:2] HWWDF, HWWDE for hardware watchdog
	page 69	Shutdown mode: All registers	Updated the bit descriptions of all flags, updated the reset conditions of all registers
	page 78	Shutdown mode: Determining the reset source	Figure updated, Hardware watchdog + Clock supervisor updated
	page 75	Shutdown mode: Hardware watchdog	Updated the parts about Hardware watchdog, Clock Supervisor completely
	page 75	Shutdown mode: Clock Supervisor	
Ver. 0.8 2009-10-19	page 69	Shutdwon Mode: Standby RAM	Changed: 1 wait cycle for read, 0 wait cycles for write
	78	Hardware Watchdog: Caution	Updated “Difference between watchdog reset, external reset and Power-on reset”
	page 74	Shutdown Mode: Precautions	Add setting of EXTE and EXTLV; removed this from Deep Shutdown settings
	page 79	Shutdown Mode: Registers which are not initialized by Shutdown Recovery	Added this section
	page 23	Block Diagram	Corrected the connection of Standby RAM (to extended D-bus)
Ver. 0.9 2009-11-24	56	Clock Supervisor, CSVCR register	Added note that bit SCKS must not be changed during CPU runs in Sub clock.
Ver. 1.0 2009-12-15	all	Header	Changed from “Preliminary Short Specification” into “Preliminary Datasheet”
	3	Features	Removed the note about PHILIPS I2C license
	page 13	Pin Description: Power supply/Ground pins	Added pin 208 to the list of VDD35 pins
	page 69	Shutdown Mode: Standby RAM	StandBy RAM 1 wait state for read and write
	page 109	I/O Map	Added note about external bus PFR initial values
	page 119	I/O Map	StandBy RAM 1 wait state for read and write
	page 120	Interrupt Vector Table	Re-arranged the table to set correct page breaks
	page 178	Package Dimension	Link to package database corrected

Ver-sion/Date	Page	Section	Change Results
Ver. 1.1 2010-01-21	page 67	USART LIN/FIFO (Extension): FIFO status register for End of Transmission interrupt control	Bits [12:8] of FSR register named NVFD[5:0] (Number of valid FIFO data), name is needed for Softune header file.
	page 69	Shutdown Mode: Standby RAM	Added notes that, if CLKP is slower then CLKB, there must be a wait time between setting RAMEN and Standby RAM access.
	page 69	Shutdown Mode: SHDE Register	
	page 68	Shutdown Mode: Overview	Added notes that reset by external pin INITX=0 will kill the Shutdown state and restart the device like at power-on.
	page 77	Shutdown Mode: Recovery	
	page 79	Shutdown Mode: Registers which are not initialized by Shutdown Recovery	
Ver 1.11 2010-06-02	page 4	Product Lineup	Changed max. CLKB frequency to 100 MHz
	page 124	Recommended Settings PLL and Clockgear settings	Enabled / allowed the settings which reach CLKB up to 100 MHz
	page 124	Recommended Settings Clock modulator settings	
	page 136	Electrical Characteristics DC Characteristics	Changed Icc max for CLKB:P:T:CAN = 100:50:50:50 MHz; Updated all current consumption characteristics
	page 143	Electrical Characteristics AC Characteristics	Chapter AC Characteristics added

DS705-00002-1v2-E		2010-08-15
Page	**Section**	**Changes**
1	■ DESCRIPTION	Fujitsu Microelectronics --> Fujitsu Semiconductor
21	■ HANDLING DEVICES 5.3 Power Supply Pins	Changed “MB91460D series” --> “MB91460 series”
49	■ CLOCK SUPERVISOR 10.2.1 Clock Supervisor Control Register (CSVCR)	Description of SCKS bit: On single clock devices always 0
50	■ CLOCK SUPERVISOR 10.3 Block Diagram Clock Supervisor	Changed input EXT_RST ---> EXT_RST_IN in the drawing
65	■ CLOCK SUPERVISOR 10.4.11 Check if reset was asserted by the Clock Super-visor	Changed the cross reference text “RSRR: Reset Cause Register" so that the hardware manual is mentioned.
136	■ ELECTRICAL CHARACTERISTICS 20.3 DC Characteristics Sum input leakage current	Changed from max. 40µA to max. 30µA
136	■ ELECTRICAL CHARACTERISTICS 20.3 DC Characteristics Power supply current CY91 F467EA	Updated all IccH values according to evaluation results
138	■ ELECTRICAL CHARACTERISTICS 20.4 A/D Converter Characteristics Compare time	Changed T_{comp} max from 16,500 µs to “t.b.d.” because this parameter is under re-evaluation.

DS705-00002-1v2-E		2010-08-15
Page	**Section**	**Changes**
150 163	■ ELECTRICAL CHARACTERISTICS 20.7 AC Characteristics 20.7.7 External Bus AC Timings at VDD35 = 4.5 to 5.5 V 20.7.8 External Bus AC Timings at VDD35 = 3.0 to 4.5 V	Changed all symbol names from upper case strings to the commonly used style. Example: Changed TCLCH into t_{CLCH}
150	■ ELECTRICAL CHARACTERISTICS 20.7 AC Characteristics 20.7.7 External Bus AC Timings at VDD35 = 4.5 to 5.5 V	Updated all timing information according to the evaluation results
163	■ ELECTRICAL CHARACTERISTICS 20.7 AC Characteristics 20.7.8 External Bus AC Timings at VDD35 = 3.0 to 4.5 V	Updated all timing information according to the evaluation results
177	■ ORDERING INFORMATION	Removed the remark that the "device is under development"

23.2 Major Changes

DS705-00002-1v3-E		2010-10-01
Page	**Section**	**Changes**
150 163	■ ELECTRICAL CHARACTERISTICS 7. AC characteristics 20.7.7 External Bus AC Timings at VDD35 = 4.5 to 5.5 V 20.7.8 External Bus AC Timings at VDD35 = 3.0 to 4.5 V	Corrected the condition of VOL from $0.2 \times V_{DD}35$ into $0.5 \times V_{DD}35$ VOH from $0.8 \times V_{DD}35$ into $0.5 \times V_{DD}35$
160 173	■ ELECTRICAL CHARACTERISTICS 7. AC characteristics Bus Hold Timing Bus Hold Timing	Added note about condition for t_{AXBGL} and t_{BGHAV}: -VOL = $0.2 \times V_{DD}35$ -VOH = $0.8 \times V_{DD}35$
177	■ ORDERING INFORMATION	Corrected the product number from MB91F467EAPFVS-GSE2 into MB91F467EAPMC-GSE2

NOTE: Please see “Document History” about later revised information.

Page	Section	Changes
Rev *A		
-	Updated to Cypress template	
-	Marketing Part Numbers changed from an MB prefix to a CY prefix.	
6 177 178	2. PIN ASSIGNMENT 21. Ordering Information 22. Package Dimension	Package description modified to JEDEC description. (Before) FPT-208P-M06 (After) LQR208
177	21. Ordering Information	Revised the following parts number. (Before) MB91F467EAPMC-GSE2 (After) CY91F467EAPMC-GS-UJE2

Document History

Document Title: CY91F467EA, 32-bit FR60 Family CY91460E Series Microcontroller Document Number: 002-09308				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	-	GSHI	03/24/2014	Initial release. Migrated Fujitsu datasheet “DS705-00002-1v3-E” into Cypress Template. Revised the following items:
*A	6331966	GSHI	10/04/2018	Marketing Part Numbers changed from an MB prefix to a CY prefix. 2. PIN ASSIGNMENT 21.Ordering Information 22.Package Dimension For details, please see 23.2.Major Changes

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