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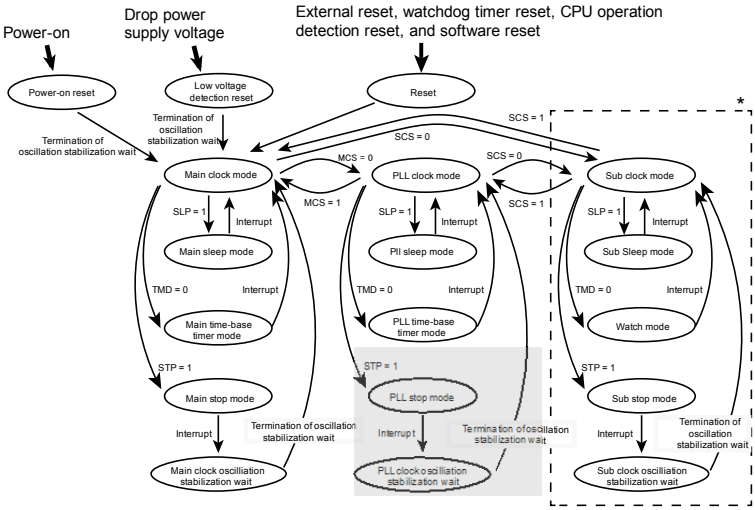
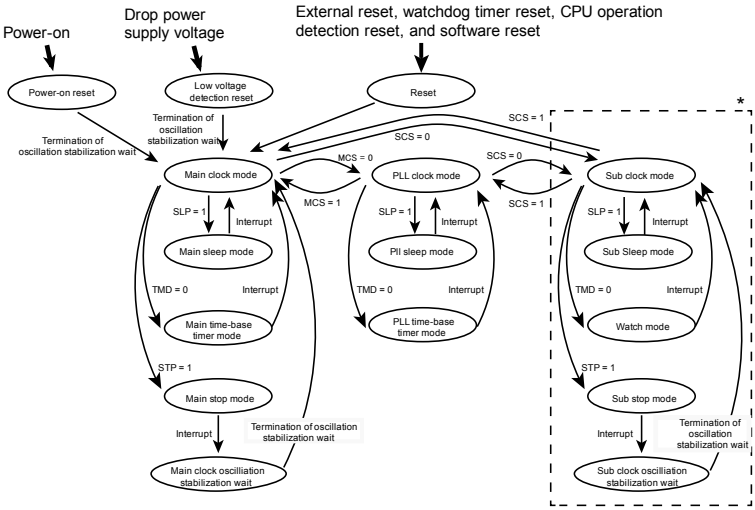
MB90920 Series

16-BIT Microcontroller
F^2MC-16LX
Hardware Manual

Errata Sheet

Page	Section	Description
Original document code: CM44-10142-5E		
Revision 1.0 February 2, 2015		
127	5.3	Table 5.3-1 Functions of Clock Selection Register (CKSCR) (1 / 3) of WS1 and WS0 bits were corrected to delete the description concerned with PLL stop mode as shown the shading below. (Error) When the switching from the main clock mode to PLL clock mode is executed, the oscillation stabilization wait time is fixed at 2^{14}/HCLK (during operation at an oscillation clock frequency of 4 MHz: approx. 4.1 ms). When the CPU switches from sub clock mode to PLL clock mode or when it returns from PLL stop mode to PLL clock mode, the oscillation stabilization wait time follows the values specified in these bits. Since the PLL clock oscillation stabilization wait time requires 2^{14}/HCLK or more, for switching from sub clock mode to PLL clock mode and transiting to PLL stop, set these bits to 10_B or 11_B. (Correct) When the switching from the main clock mode to PLL clock mode is executed, the oscillation stabilization wait time is fixed at 2^{14}/HCLK (during operation at an oscillation clock frequency of 4 MHz: approx. 4.1 ms). When the CPU switches from sub clock mode to PLL clock mode , the oscillation stabilization wait time follows the values specified in these bits. Since the PLL clock oscillation stabilization wait time requires 2^{14}/HCLK or more, for switching from sub clock mode to PLL clock mode , set these bits to 10_B or 11_B.
158	6.5.4	The Note was added for the transition to the stop mode as follows. ・The transition to the stop mode must be set at Main clock and Sub clock mode.
159	6.5.4	The Note was corrected to delete the description concerned with PLL stop mode as shown the shading below. •In PLL stop mode, the main clock and PLL multiplier circuit remain stopped. When the CPU returns from PLL stop mode, therefore, it is necessary to secure the main clock oscillation stabilization wait time and PLL clock oscillation stabilization wait time. The oscillation stabilization wait time in this case bases upon the values set in the oscillation stabilization wait time selection bit in the clock selection register (CKSCR:WS1, WS0), and the main clock oscillation stabilization wait time and PLL clock oscillation stabilization wait time will be counted together. Therefore, set a value to the "CKSCR:WS1, WS0" bit in line with the longest one of the oscillation stabilization wait times. However, because 2^{14}/HCLK or more is needed for the PLL clock oscillation stabilization wait time, set 10_B or 11_B to the "CKSCR: WS1, WS0" bit.

Page	Section	Description
161	6.6	Figure 6.6-1 State Transition Diagram was corrected to delete the description concerned with PLL stop mode and PLL clock oscillation stabilization wait as shown below figure. (Error)  *: These modes can be used with the dual clock product only. (Correct)  *: These modes can be used with the dual clock product only.

<table>
<tr><th>Page</th><th>Section</th><th>Description</th></tr>
<tr><td>162</td><td>6.6</td><td>Table 6.6-1 Operation States in the Low-power Consumption Mode was corrected the description concerned with PLL stop mode as shown the shading below table.

(Error)
<table>
<tr><th>Operation state</th><th>Main clock</th><th>Sub clock</th><th>PLL clock</th><th>CPU</th><th>Peripheral</th><th>Watch</th><th>Time-base timer</th><th>Clock source</th></tr>
<tr><td>PLL</td><td rowspan="3">Operating</td><td rowspan="3">Operating</td><td rowspan="3">Operating</td><td>Operating</td><td rowspan="2">Operating</td><td rowspan="3">Operating</td><td rowspan="3">Operating</td><td rowspan="4">PLL clock</td></tr>
<tr><td>PLL sleep</td><td rowspan="3">Stopped</td></tr>
<tr><td>PLL time-base timer*1</td><td rowspan="2">Stopped</td></tr>
<tr><td>PLL stop</td><td>Stopped</td><td>Stopped</td><td>Stopped</td><td>Stopped</td><td>Stopped</td></tr>
<tr><td>PLL oscillation stabilization wait</td><td>Operating</td><td>Operating</td><td>Operating</td><td>Stopped</td><td>Operating</td><td>Operating</td></tr>
</table>
(Correct)
<table>
<tr><th>Operation state</th><th>Main clock</th><th>Sub clock</th><th>PLL clock</th><th>CPU</th><th>Peripheral</th><th>Watch</th><th>Time-base timer</th><th>Clock source</th></tr>
<tr><td>PLL</td><td rowspan="3">Operating</td><td rowspan="3">Operating</td><td rowspan="3">Operating</td><td>Operating</td><td rowspan="2">Operating</td><td rowspan="3">Operating</td><td rowspan="3">Operating</td><td rowspan="4">PLL clock</td></tr>
<tr><td>PLL sleep</td><td rowspan="3">Stopped</td></tr>
<tr><td>PLL time-base timer*1</td><td rowspan="2">Stopped</td></tr>
<tr><td>PLL oscillation stabilization wait</td><td>Operating</td><td>Operating</td><td>Operating</td><td>Operating</td><td>Operating</td></tr>
</table></td></tr>
<tr><td>165</td><td>6.8</td><td>6.8 Notes on Using the Low-power Consumption Mode was corrected to add the description concerned with transiting stop mode as shown the shading below.

Take notice of the following points when using the low-power consumption mode.
• Transition to the standby mode and interrupts
• Notes on the transition to the standby mode
• Releasing the standby mode by an interrupt
• At transiting the stop mode
• At releasing the stop mode
• Oscillation stabilization wait time
• Switching the clock mode
• Notes on accessing to the low-power consumption mode control register (LPMCR) for the transition to the standby mode.

■ At Transiting the Stop Mode
The transition to the stop mode must be set at Main clock and Sub clock mode.
If the mode is transited to the stop mode during PLL clock mode,set the stop mode after transiting Main clock mode once.</td></tr>
<tr><td>166</td><td>6.8</td><td>6.8 Notes on Using the Low-power Consumption Mode was corrected to delete the description concerned with PLL stop mode as shown the shading below.

■ Oscillation Stabilization Wait Time
● PLL clock oscillation stabilization wait time
In PLL stop mode, the main clock and PLL multiplier circuit remain stopped. When the CPU returns from PLL stop mode, therefore, it is necessary to secure the main clock oscillation stabilization wait time and PLL clock oscillation stabilization wait time. The oscillation stabilization wait time in this case bases upon the values set in the oscillation stabilization wait time selection bit in the clock selection register (CKSCR:WS1, WS0), and the main clock oscillation stabilization wait time and PLL clock oscillation stabilization wait time will be counted together. Therefore, set a value to the "CKSCR:WS1, WS0" bit in line with the longest one of the oscillation stabilization wait times. However, because 2^{14}/HCLK or more is needed for the PLL clock oscillation stabilization wait time, set 10_B or 11_B to the "CKSCR: WS1, WS0" bit.</td></tr>
</table>

Page	Section	Description
263	9.3.2	9.3.2 Time-base Timer Control Register (TBTC) of TOBF was corrected to delete the description concerned with PLL stop mode as shown the shading below. (Error) The TBOF bit is cleared by the conditions listed below. • Writing "0" • Transition to main stop mode • Transition to PLL stop mode • Transition from sub clock mode to main clock mode • Transition from sub clock mode to PLL clock mode • Transition from main clock mode to PLL clock mode • Writing "0" to the TBR bit • Reset Writing "1" has no effect. Reading by read-modify-write (RMW) instructions always reads "1". (Correct) The TBOF bit is cleared by the conditions listed below. • Writing "0" • Transition to main stop mode • Transition from sub clock mode to main clock mode • Transition from sub clock mode to PLL clock mode • Transition from main clock mode to PLL clock mode • Writing "0" to the TBR bit • Reset Writing "1" has no effect. Reading by read-modify-write (RMW) instructions always reads "1".

<table>
<tr><th>Page</th><th>Section</th><th>Description</th></tr>
<tr><td>270</td><td>9.4.2</td><td>
9.4.2 Operation of Time-base Timer was corrected to delete the description concerned with PLL stop mode as shown the shading below.

(Error)
■ Operation of Time-base Timer
The time-base timer consists of an 18-bit counter and uses a main clock as the count clock. While a main clock is input, count operation continues.
Time-base counter is cleared by the following conditions:
• Power-on reset
• Transition to main stop mode
• Transition to PLL stop mode
• Transition from main clock mode to PLL clock mode
• Transition from sub clock mode to main clock mode
• Transition from sub clock mode to PLL clock mode
• Setting the TBR bit in the TBTC register to "0".
The watchdog timer and interval interrupt functions, which use the output of the time-base timer, are affected by clearing the time-base timer.

(Correct)
■ Operation of Time-base Timer
The time-base timer consists of an 18-bit counter and uses a main clock as the count clock. While a main clock is input, count operation continues.
Time-base counter is cleared by the following conditions:
• Power-on reset
• Transition to main stop mode
• Transition from main clock mode to PLL clock mode
• Transition from sub clock mode to main clock mode
• Transition from sub clock mode to PLL clock mode
• Setting the TBR bit in the TBTC register to "0".
The watchdog timer and interval interrupt functions, which use the output of the time-base timer, are affected by clearing the time-base timer.
</td></tr>
<tr><td>272</td><td>9.4.2</td><td>
Table 9.4-2 Clearing the Time-base Timer Counter and Oscillation Stabilization Wait Time was corrected the description concerned with PLL stop mode as shown the shading below table.

(Error)
<table>
<tr><th>Operation</th><th>Counter clear</th><th>TBOF clear</th><th>Oscillation stabilization wait time</th></tr>
<tr><td>Writing "0" to TBR bit in TBTC</td><td>Y</td><td>Y</td><td>-</td></tr>
<tr><td>Power-on reset</td><td>Y</td><td>Y</td><td>Main clock oscillation stabilization wait time</td></tr>
<tr><td>Releasing main stop mode
Releasing PLL stop mode</td><td>Y</td><td>Y</td><td>Main clock oscillation stabilization wait time</td></tr>
<tr><td>Releasing sub stop mode</td><td>N</td><td>N</td><td>Sub clock oscillation stabilization wait time</td></tr>
</table>

(Correct)
<table>
<tr><th>Operation</th><th>Counter clear</th><th>TBOF clear</th><th>Oscillation stabilization wait time</th></tr>
<tr><td>Writing "0" to TBR bit in TBTC</td><td>Y</td><td>Y</td><td>-</td></tr>
<tr><td>Power-on reset</td><td>Y</td><td>Y</td><td>Main clock oscillation stabilization wait time</td></tr>
<tr><td>Releasing main stop mode</td><td>Y</td><td>Y</td><td>Main clock oscillation stabilization wait time</td></tr>
<tr><td>Releasing sub stop mode</td><td>N</td><td>N</td><td>Sub clock oscillation stabilization wait time</td></tr>
</table>
</td></tr>
</table>