

PSOC™ Control C3 – Device power modes

Customer training workshop

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Overview

Overview

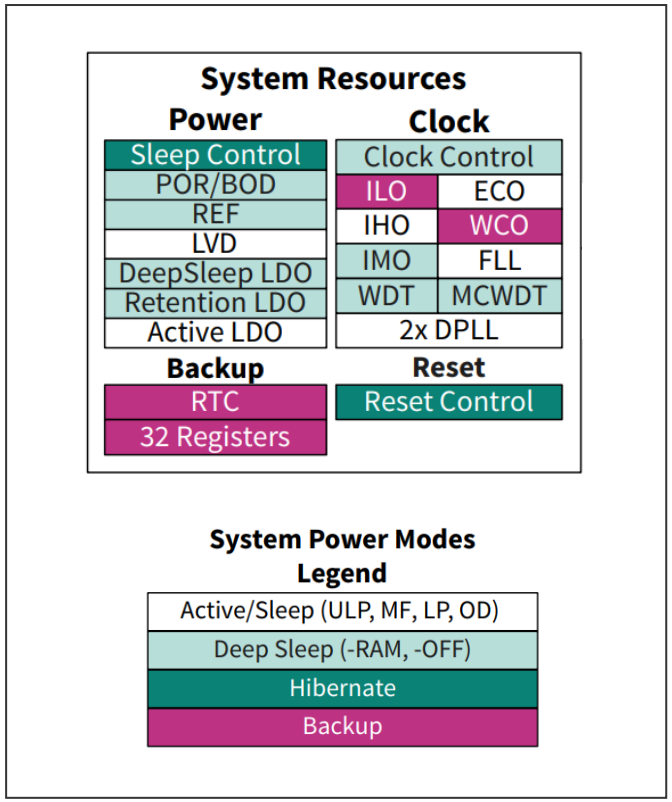
Features

Power modes in decreasing power consumption order:

- Active/Sleep
- Deep Sleep
- Deep Sleep RAM
- Deep Sleep Off
- Hibernate

Benefits

The PSOC™ Control C3 supports six low-power modes to achieve the best compromise between low power consumption, short start-up time, available peripherals, and available wake-up sources.



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Features and capabilities

Active/Sleep
- Active: all peripherals and CPU are available
- Sleep: all peripherals remain available except the CPU

Deep Sleep
- Active logic is frozen but low-speed functions remain available
- Most configuration and memory states are retained
- High-speed clock sources are turned off
- Wake-up returns the processors to its previous state

Deep Sleep RAM
- The CPU is turned off, but 64 KB of SRAM is retained for a warm boot after wake up

Deep Sleep Off
- Same as Deep Sleep RAM, except RAM is also turned off. Wake up requires a “cold” boot

Hibernate
- Lowest power mode where VDDD remains active
- Device and I/O states are frozen, and the device resets on wake up

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See the architecture reference manual:

Section 18: Device power modes, and **Section 18.2: Architecture**

for more details.

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Features and capabilities (contd.)

Power mode features

- Software can use power modes to optimize power consumption in an application
- Deep Sleep mode: Supports multiple wake-up sources and retains full SRAM
- Hibernate mode: Wakes up from I/O, LPComp, RTC, and timer alarms

Methods to control power consumption in different power modes

- Enable or disable clocks to peripherals
- Powering on/off clock sources
- Powering on/off peripherals and internal components of PSOC™ Control C3

User-selectable core voltage in Active mode

The power management unit operates in the following mode selections:

- Ultra Low Power (ULP) mode: 0.9 V, CPU at 50 MHz
- Mid Frequency (MF) mode: 1.0 V, CPU at 70 MHz
- Low Power (LP) mode: 1.1 V, CPU at 150 MHz
- Over Drive (OD) mode: 1.2 V, CPU at 180 MHz

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See the architecture reference manual:

Section 18.1: Features

for more details.

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Device power modes

Power mode: Active and Sleep

Active

- Normal operating power mode; All device resources used by the system are active and clocked
- LPActive/LPSleep: Low-power profiles implemented as register configurations within Active/Sleep modes
- The CPU executes code along with all logic and remains memory-powered
- All the peripherals are available for use in Active mode

Sleep

- CPU clock is turned off; CPU halts code execution and enters sleep
- All peripherals available in Active mode remain available in Sleep mode
- Peripheral activity can continue; if the CPU is required, it can be reactivated via clock gating instantaneously
- Any unmasked interrupt can wake up the CPU to Active mode

Power mode	Description	Entry condition	Wake-up source	Wake-up action
Active	Primary mode of operation; all peripherals and CPU are available	Wake-up from sleep, all deep sleep modes, hibernate reset, or any other reset	Not applicable	Not applicable
Sleep	CPU is in Sleep mode; all other peripherals are available	Register write from Active mode or wake up from Deep Sleep through a debugger	Any interrupt to CPU	Interrupt

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See the architecture reference manual:

Section 18.2.1.1: Active and Sleep

for more details.

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Power mode: Deep Sleep

- Low-power mode where Active logic is frozen, but low-speed functions remain available
- GPIO states are frozen; high-speed clock sources are turned off
- System state is fully preserved, allowing seamless resumption of operation; stack and critical parameters are retained
- Wake-up restores the processor to its previous execution point
- Ideal for applications where the processor does not need to run code, but peripherals must operate at speeds lower than the system clock

Power mode	Description	Entry condition	Wake-up source	Wake-up action
Deep Sleep	All high-frequency clocks and peripherals are turned off. Low-frequency clocks and low-power analog and digital peripherals are available for operation and as wake-up sources	Register write from active	GPIO interrupt, low-power comparator, SCB-instance, watchdog timer, RTC alarms, and debugger	Interrupt or debug

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See the architecture reference manual:

Section 18.2.1.2: Deep Sleep

for more details.

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Power mode: Deep Sleep RAM

- Active mode logic is not retained, which requires a processor reset upon wake-up
- In Deep Sleep RAM mode, the entire SRAM is retained. The software can store key information in SRAM to enable a "warm“ reboot, allowing the application to return to its previous state faster than a full "cold" reboot
- Deep Sleep logic is remains active and functional, but only SRAM is retained. Wake up results in a reset (warm reboot)

Power mode	Description	Entry condition	Wake-up source	Wake-up action
Deep Sleep RAM	It’s like Deep Sleep, except most configuration state is not retained. Wake-up causes the processors to reboot. The software can use the retained SRAM contents (programmable) to more quickly recover the application state, that is perform a “warm” reboot	Register write from active	GPIO interrupt, low-power comparator, SCB-instance, watchdog timer, RTC alarms	Warm reboot

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See the architecture reference manual:

Section 18.2.1.3: Deep Sleep RAM

for more details.

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Power mode: Deep Sleep Off

- Active mode logic and memories are not retained at all. This requires a full "cold" reboot to restore the application to its previous state
- Deep Sleep logic is turned on and functional, but Active logic and SRAM are powered off. Wake-up results in a reset (cold reboot)
- SRAM retention is unavailable

Power mode	Description	Entry condition	Wake-up source	Wake-up action
Deep Sleep Off	A low-power mode, like Deep Sleep, except most configuration state and memories are not retained. Wake-up causes the processors to "cold" reboot	Register write from active	GPIO interrupt, low-power comparator, SCB-instance, watchdog timer, RTC alarms	Cold reboot

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See the architecture reference manual:

Section 18.2.1.4: Deep Sleep Off

for more details.

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Power mode: Deep Sleep states

Deep Sleep state	After wake up
Deep Sleep	Wake up from WFI/WFE
Deep Sleep RAM	Warm reboot
Deep Sleep Off	Cold reboot

Application

Deep Sleep states are used in applications where the processor does not need to execute code, but peripherals must continue operating at speeds lower than the system clock.

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See the architecture reference manual:

Section 18.2.1.4: Deep Sleep Off

for more details.

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Power mode: Hibernate

- The lowest power mode when external supplies are present and XRES is de-asserted
- Comparators can be used in this mode, but at the cost of increased low-speed comparator current
- Wake-up requires the device to go through Reset
- Dedicated wake-up pins (P2.0 and P9.0) and a low-power comparator output
- Debug functionality is lost; the debugger disconnects on entering Hibernate mode

Application

Useful for handheld or battery-powered applications where the system can enter a low-power state while preserving essential state information.

Power mode	Description	Entry condition	Wake-up source	Wake-up action
Hibernate	GPIO states are frozen; all high-frequency clocks and peripherals are switched off. Low-frequency clocks, and WCO can function. Device resets on wake-up event	Register write from active	Wake-up pins, low-power comparator, RTC alarm, and watchdog timer	Hibernate reset

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See the architecture reference manual:

Section 18.2.1.5: Hibernate

for more details.

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Other operational states

- Additionally, there are two states: **Reset** and **Off**
- Reset and Off states are determined by the external power supply and XRES conditions
- Entering these modes does not require any firmware action, and exiting them does not require an interrupt or wake-up event
- The Reset and Off states are discussed for completeness, covering all possible modes and states the device can enter
  - Reset state (XRES): Occurs when an external reset (XRES pin pulled low) is applied or when Power-on reset/Brownout detection is asserted
  - Off state (OFF): Represents the device state with no power is applied

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See the architecture reference manual:

Section 18.2.2: Other operation states

for more details.

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Wake-up parameters, resource management

Power modes and wake-up parameters

	Active/Sleep	Deep Sleep	Deep Sleep RAM	Deep Sleep Off	Hibernate	Off
Parameters						
Wake source	Any interrupt	DS peripherals	DS peripherals	DS peripherals	RTC/HIB peripherals	Power on
Wake action	Resume	Resume	Warm Boot	Reset/cold boot	Reset	Reset
Wake time	1 CPU cycle	< 20 µs	Deep Sleep + warm boot	Deep Sleep + cold boot	POR + cold boot < 1 ms	
Resources						
ECO	On/Off	On/Off	On/Off	On/Off	Off	Off
IHO	On	Off	Off	Off	Off	Off
IMO	On	On	On	On	Off	Off
ILO	On/Off	On/Off	On/Off	On/Off	Off	Off
WCO	On/Off	On/Off	On/Off	On/Off	On/Off	Off
CPU	On/Sleep	Retention	Off	Off	Off	Off
SRAM	On	On	On/Off*	Off	Off	Off

* Full SRAM powered on or off.

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See the architecture reference manual:

Section 18.4: Summary

for more details.

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Power modes and resource availability

Block	Power mode				
	Active	Sleep	Deep Sleep	Hibernate	Backup
CPUSS					
CPU	Y	N	N	N	N
NVIC	Y	Y	N	N	N
WIC	Y	Y	Y	Y	N
Flash	Y	Y	N	N	N
SRAM	Y	Y	Y	N	N
DMA	Y	Y	N	N	N
Programmable digital					
Smart IO	Y	Y	Y	N	N
Fixed-function digital					
TCPWM	Y	Y	N	N	N
SCB	Y	Y	Y	N	N
CAN FD	Y	Y	N	N	N

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See the architecture reference manual:

Section 18.4: Summary

for more details.

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Power modes and resource availability (contd.)

Block	Power mode				
	Active	Sleep	Deep Sleep	Hibernate	Backup
Special function					
CORDIC	Y	Y	N	N	N
Programmable analog					
LPC	Y	Y	Y	Y	N
SAR	Y	Y	N	N	N
CSG	Y	Y	N	N	N
IO					
GPIO	Y	Y	Y	Y *	N
Backup					
RTC	Y	Y	Y	Y	Y
Registers	Y	Y	Y	Y	Y

* Only hibernate_wake-up pins (P2.0 and P9.0) are operational and capable of waking up the device from Hibernate mode.

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See the architecture reference manual:

Section 18.4: Summary

for more details.

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Revision history

Document revision	Date	Description of change
**	2026-01-14	Initial release.

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