

PSOC™ Control C3 architecture (PSC3P2x, PSC3M3x, PSC3M5x, PSC3P5x) - TCPWM and Analog subsystems

Customer training workshop (CTW)

February 2026

public

Prerequisites

- Basic hands-on with ModusToolbox™
- Basic understanding of PSOC™ Control C3 device architecture

- Required development tools
  - ModusToolbox™ Tools Package v3.5 or later
  - Eclipse IDE for ModusToolbox™ v2025.8.0 or later
  - ModusToolbox™ Programming Tools v1.6 or later
    - Recommended installation via ModusToolbox™ Setup tool
  - PSOC™ Control C3M5 Evaluation Kit (KIT_PSC3M5_EVK)

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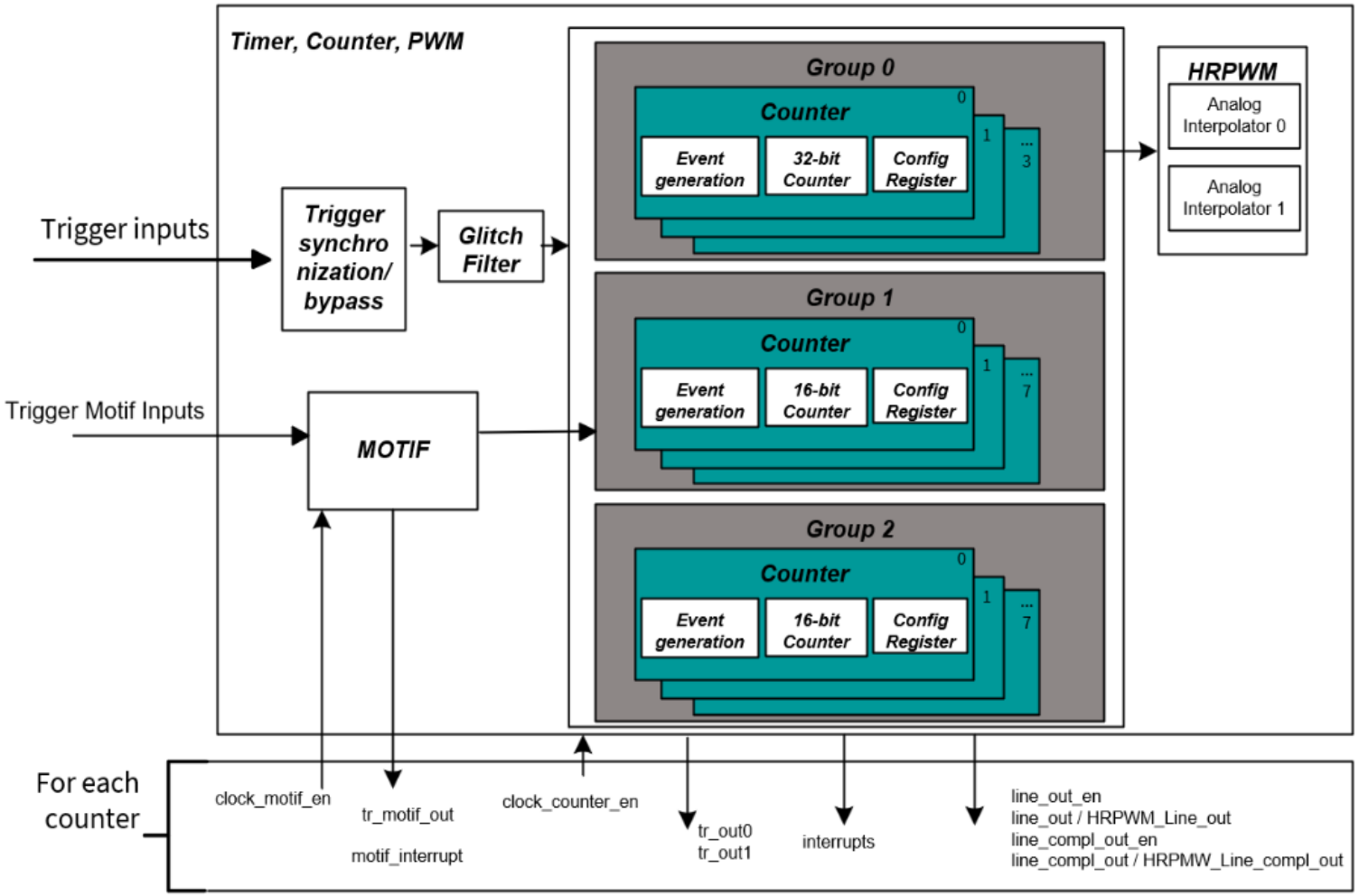
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Timer, counter, and pulse-width modulator (TCPWM)

Block diagram



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Features

- Three counter groups
  - 16-bit group1 and group 2: support eight counters each
  - 32-bit group 0: support four counters only
- High-resolution (HR) PWM supports with 32-bit group 0 only
- HRPWM supports PWM and PWM_DT modes
- A configurable motion interface (MOTIF) only with group 1
- Independent control of clock pre-scaling and dead time
- Connect the block to the CPU subsystem via the AHB-5 interface
- Interrupt request for each counter based on TC, and CC0/CC1 match events
- Signal interface of the counter with input trigger and trigger out generated as trigger events for other peripherals
- Independent line polarity setting for PWM signal during Kill event

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Counters

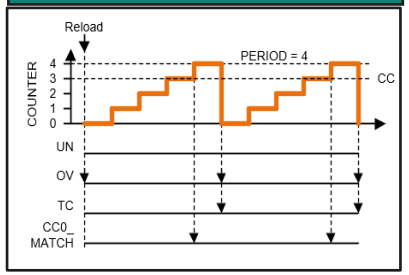
- 16-bit or 32-bit counters, depending on the specific group, with two compare/capture and period registers
- Counter can run in one of the available modes - timer, capture, PWM, PWM_DT, MOTIF (Hall, Quad decoder/multi-channel) and HRPWM
- Support various counting modes
  - One-shot mode and continuous mode (up/down/up-down)
- Each counter can produce two output signals with programmable dead time
  - Line_out
  - Line_compl_out
- Symmetric/asymmetric PWM output control with programmable dead time
- Two output trigger signals for each counter to indicate underflow, overflow, and capture/compare events
- Counter control signals (reload, start, stop) are manipulated by the input trigger signals or the software commands
  - Group trigger (timer) and one-to-one trigger (GPIO and ADC channels)
  - Constant 1 or 0 is also used as an input trigger
- Synchronous operation of multiple counters is possible
- Support one interrupt output for each counter
- Each counter has independent control of clock enable and clock pre-scaling (1x,2x…..128x)

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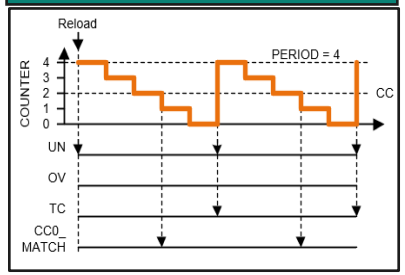
TCPWM: Counters (contd.)

– Counting modes

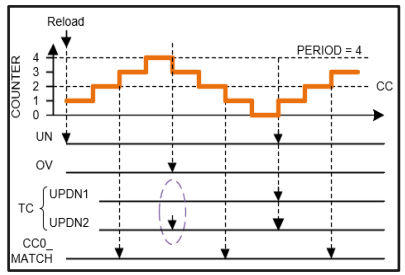
Counter UP



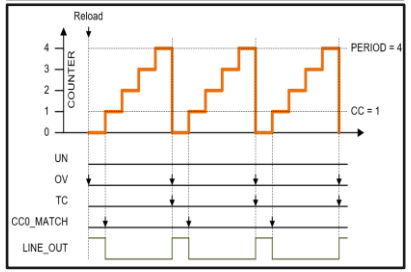
Counter Down



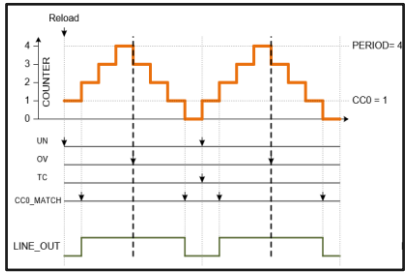
Counter UP-DOWN



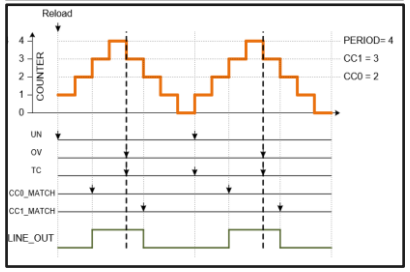
Edge aligned- Cont



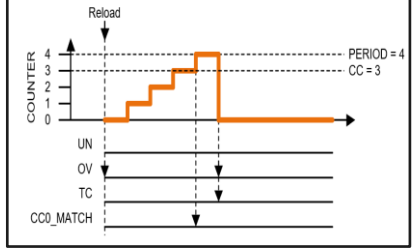
Centre aligned-Sym.

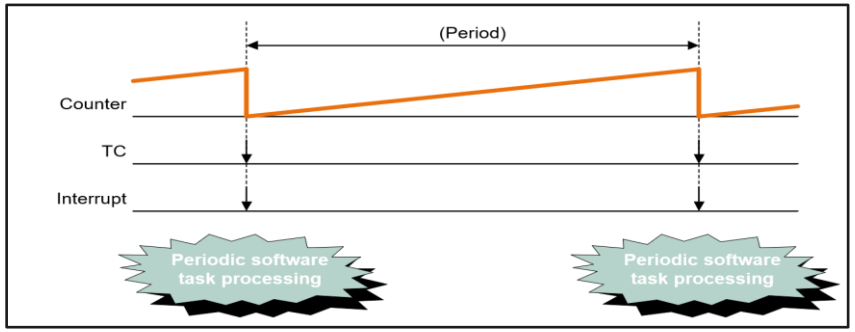


Centre aligned-Asym.



Single Shot

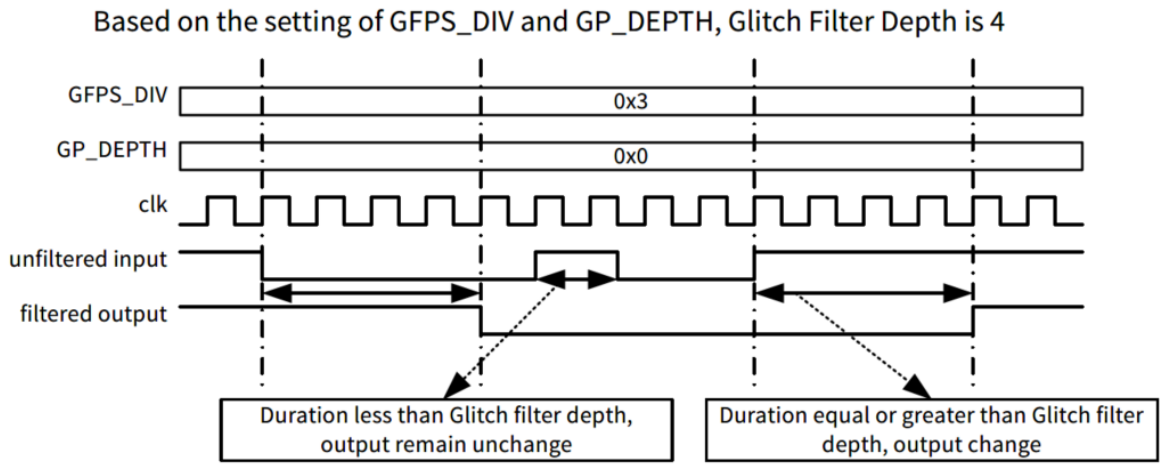




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Glitch filter

- Glitch filtering is the process of removing unwanted pulses from a digital input signal that is usually HIGH or LOW
- Glitch filter can be inserted into the general purpose triggers and specific one-to-one triggers
- The glitch filter runs on clk_peri
- Independent configuration with selectable depth of 0-512
- The figure below shows how the output of the glitch filter changes with the duration of the filter depth
- Glitch filter supported on general purpose triggers and one-to-one triggers for the counter



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Trigger output and interrupt generation

- Each counter has two trigger outputs (TR_OUT0/1) and an interrupt
- TR_OUT0 and TR_OUT1 can be routed through Trigger Mux to other peripherals

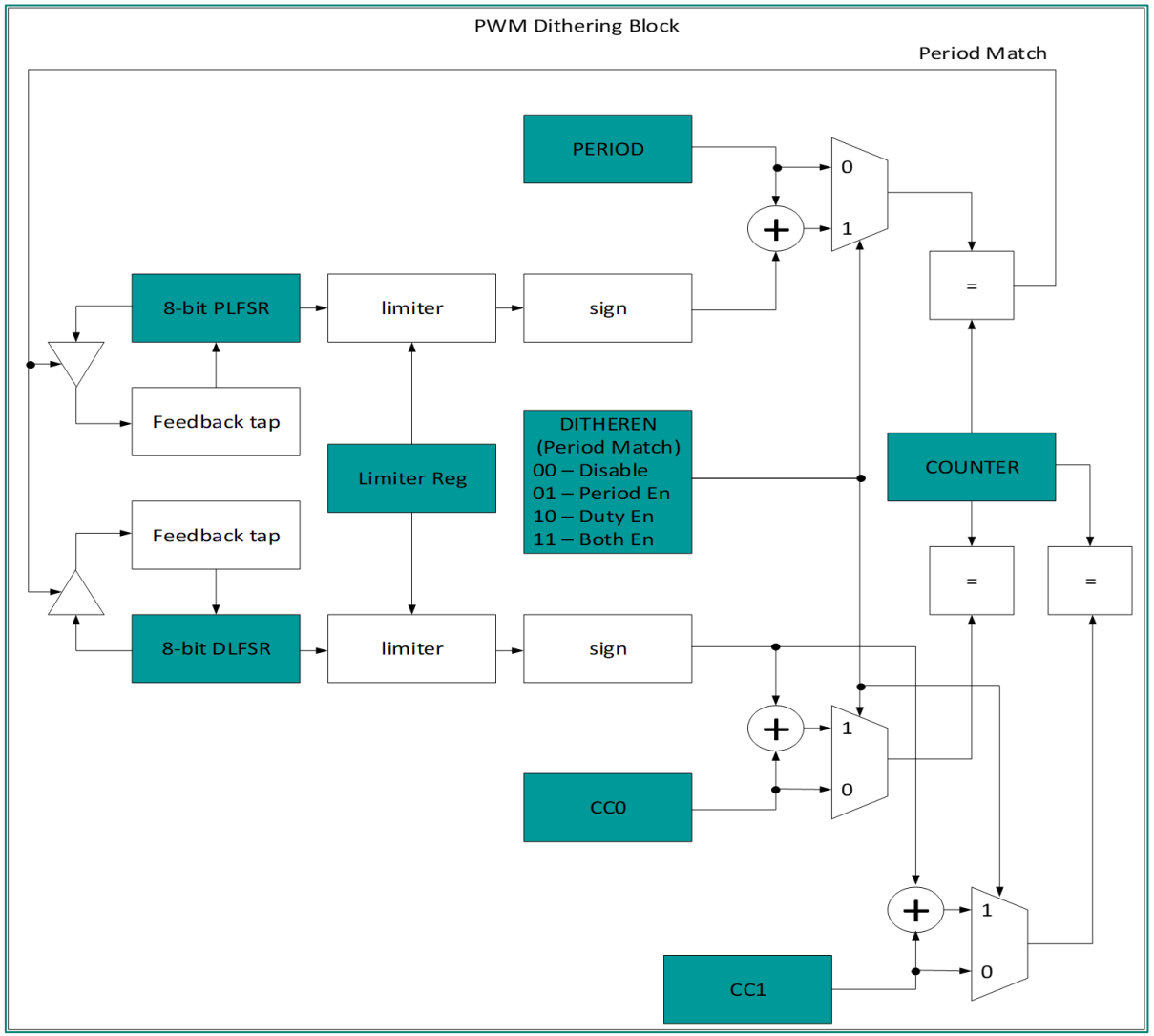
Factor	Description	TR_OUT0/1[1]	Interrupt
Overflow (OV)	An overflow event indicates that in an up-counting mode, COUNTER equals PERIOD register, and is changed to a different value	✓	–
Underflow (UN)	An underflow event indicates that in a down counting mode, COUNTER equals 0, and is changed to a different value	✓	–
Terminal ount (TC)	A TC event is the logical OR of the underflow and overflow events	✓	✓
CC0/1_MATCH	This event is generated when the counter is running and one of the following conditions occur: - Counter equals the compare value - A capture event occurs and the CC0/1 and CC0/1_BUFF registers are updated	✓	✓
CC0_CC1_MATCH	This event is triggered when either CC0_MATCH or CC1_MATCH occurs	✓	–
LINE_OUT	PWM output signal	✓	–

[1] TR_OUT0/1 is disabled.

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Dithering mode

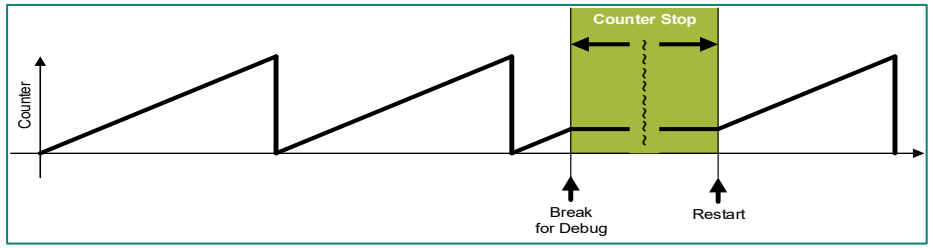
- The dithering feature is available on group 1 and group 2. The dithering feature is added in these counter groups for PWM and PWM_DT mode
- Dithering can be turned on for a period and duty cycle independently
  - Period dithering - pseudo random number generated from an LFSR is added or subtracted from the period value
  - Duty cycle dithering - pseudo random number generated from LFSR is added or subtracted from the CC0/CC1 value
- Value in PLFSR/DLFSR register is hanged based on an 8-bit LFSR taps polynomial
- Software can control the magnitude of the LFSR value to be added or subtracted by programming the LFSR.Limiter bits



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Debug mode

- The TCPWM counters support debugging through CTRL.DBG_FREEZE_EN and CTRL.DBG_SUS_EN bits
- It can be configured per counter if the counter operation continues or pauses in debug state (for example, after running to a break point). This feature is especially intended when using a TCPWM counter as an OS timer
- Freeze TCPWM in debug mode, not only set DBG_FREEZE_EN and DBG_SUS_EN, debug signal(tr_debug_freeze) also need to be set. tr_debug_freeze is from DEBUG600 System Cross Trigger Interface (CTI)



	DBG_FREEZE_EN	DBG_SUS_EN
Counter operation continues	0	0
Counter operation pauses immediately	1	0
Counter operation pauses after tc event and enter passive state. Passive state is controlled through CTRL.KILL_LINE_POLARITY	0	1
Counter operation pauses immediately and enters passive state. Passive state is controlled through CTRL.KILL_LINE_POLARITY. STATUS.RUNNING bit set to '0'	1	1

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Motion interface (MOTIF)

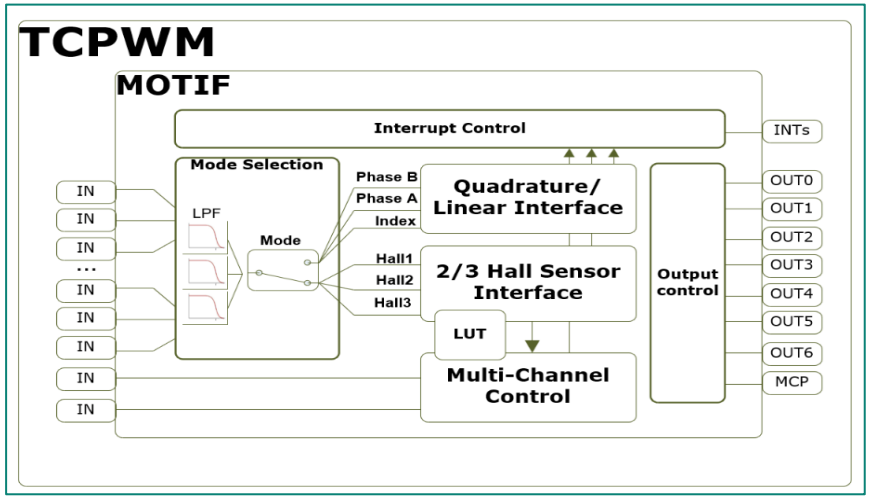
Key features

- Interface for linear or quadrate rotary encoder
- Hall sensors interface mode
- Standalone multi-channel control
- Look up table (LUT) support with hall sensor and standalone multi-channel control
- Auto hall fault selection

Highlights

Motion interface (MOTIF) is an ideal solution for motor control applications it is a flexible and powerful component integrated in TCPWM that enables incremental encoder or hall sensors as motor control feedback input

- MOTIF is available only in TCPWM group #1
- MOTIF can be configured by the user to support any of the three available operation modes :
  - Quadrature encoder
  - HALL interface
  - Standalone multi-channel
- Each MOTIF module is connected to a dedicated channel counter group



Customer benefits

- Application-tailored motor position and velocity measurement
- Hall Interface for direct connection to Hall sensors
- Simple built-in mode for brushless DC motor control
- Perform multi-level modulation for PWM
- Flexibility to develop complex modulation schemes
- Hardware lookup table (LUT) for advanced motor control feedback loop operation
- Input and output look-up table for automatic modulation control, reduces the software complexity, and CPU load

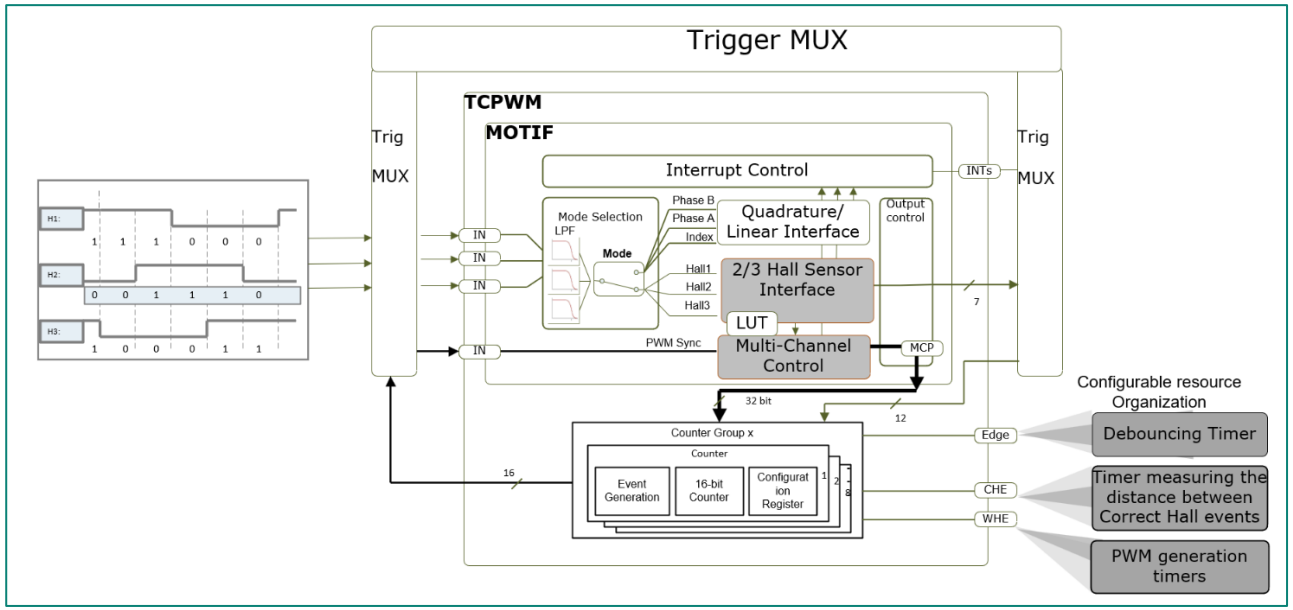
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Motion interface (MOTIF) Hall sensor mode

Key feature

- Hall sensor interface with current and expected pattern can be easily updated via SW or LUT
- Hall sensor mode can also operate in look-up table mode (LUT) in a semi-autonomous way
- Support for input signal filtering with program delay times via low-pass filters
- Flexible input signal debouncing /filtering via a timer
- Time measurement between **c**orrect **h**all events
- Programmable error handling (**w**rong **h**all **e**vent)
- Synchronisation with the PWM generation
- Hall fault detections with auto-loading of pre-configured values for a specific safe operation

MOTIF interface to Hall sensor



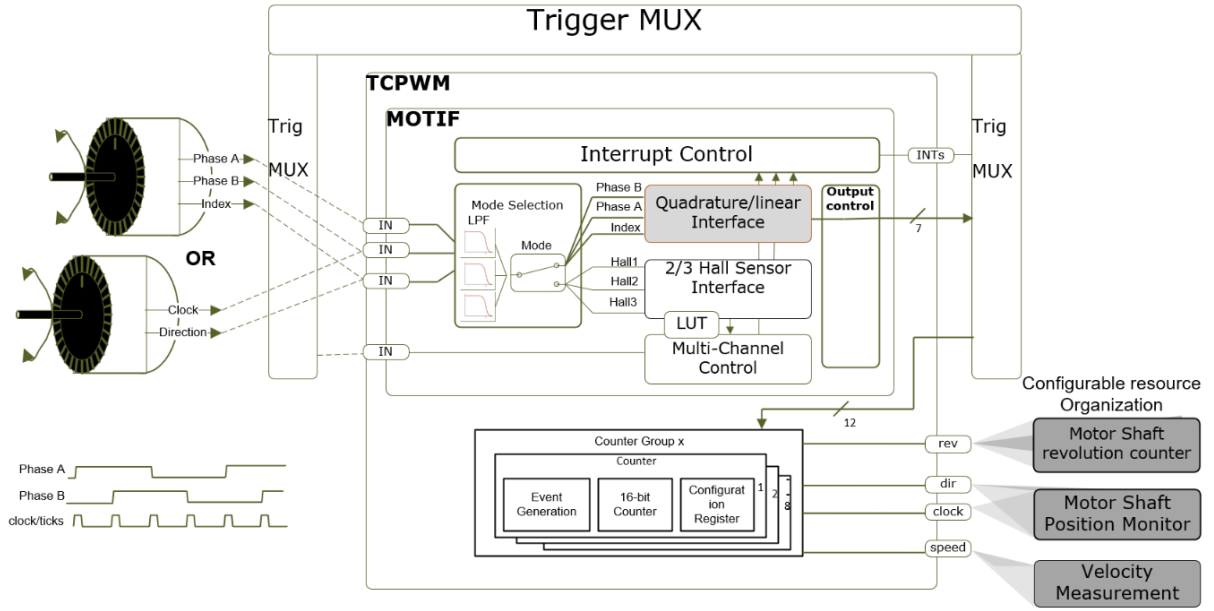
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Motion interface (MOTIF) Quadrature encoder mode

Key feature

- Linear or quadrature interface
- Support for input signal filtering with programmable delay times via low-pass filters
- Positon monitoring (tick counting + direction)
- Velocity monitoring (time between ticks/elapsed time for a number of ticks)
- Revolution monitoring
- Interrupt sources for phase error, motor revolution, direction change and error on phase decoding
- Quadrature decoder mode can be used in parallel with the standalone multichannel mode

MOTIF interface to encoder



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High-resolution PWM (HRPWM)

Key feature

- Complementary high-resolution PWM outputs with <100ps resolution
- Configurable PWM control scheme

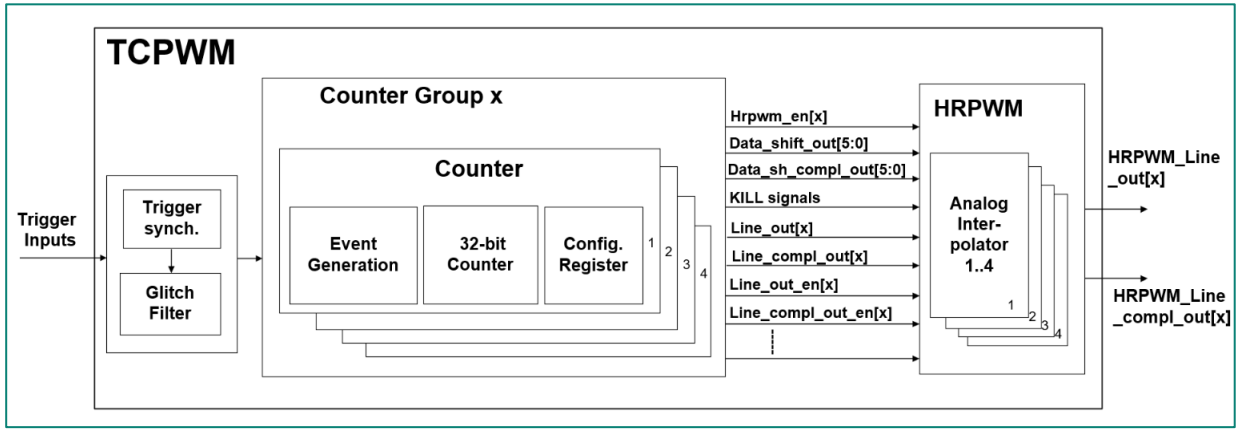
Highlights

TCPWM supports High-resolution PWM (HRPWM) functionality to enable an in-cycle control loop of higher switching frequency (up to 200 KHz, depending on the algorithm)

- 4x32-bit TCPWM counters support HRPWM functionality; HRPWM is available in Group 0
- HRPWM generation feature is supported in both PWM and PWM_DT mode
- HRPWM allows PWM signal adjustments in the steps of <100ps (target 66ps) with 64 steps (6-bit fractional value in 26-bit integer)
- High resolution PWM support for period, duty, and dead time
- Each 32-bit counter is connected to a delay element (Analog Interpolator) to output HRPWM out and HRPWM complementary

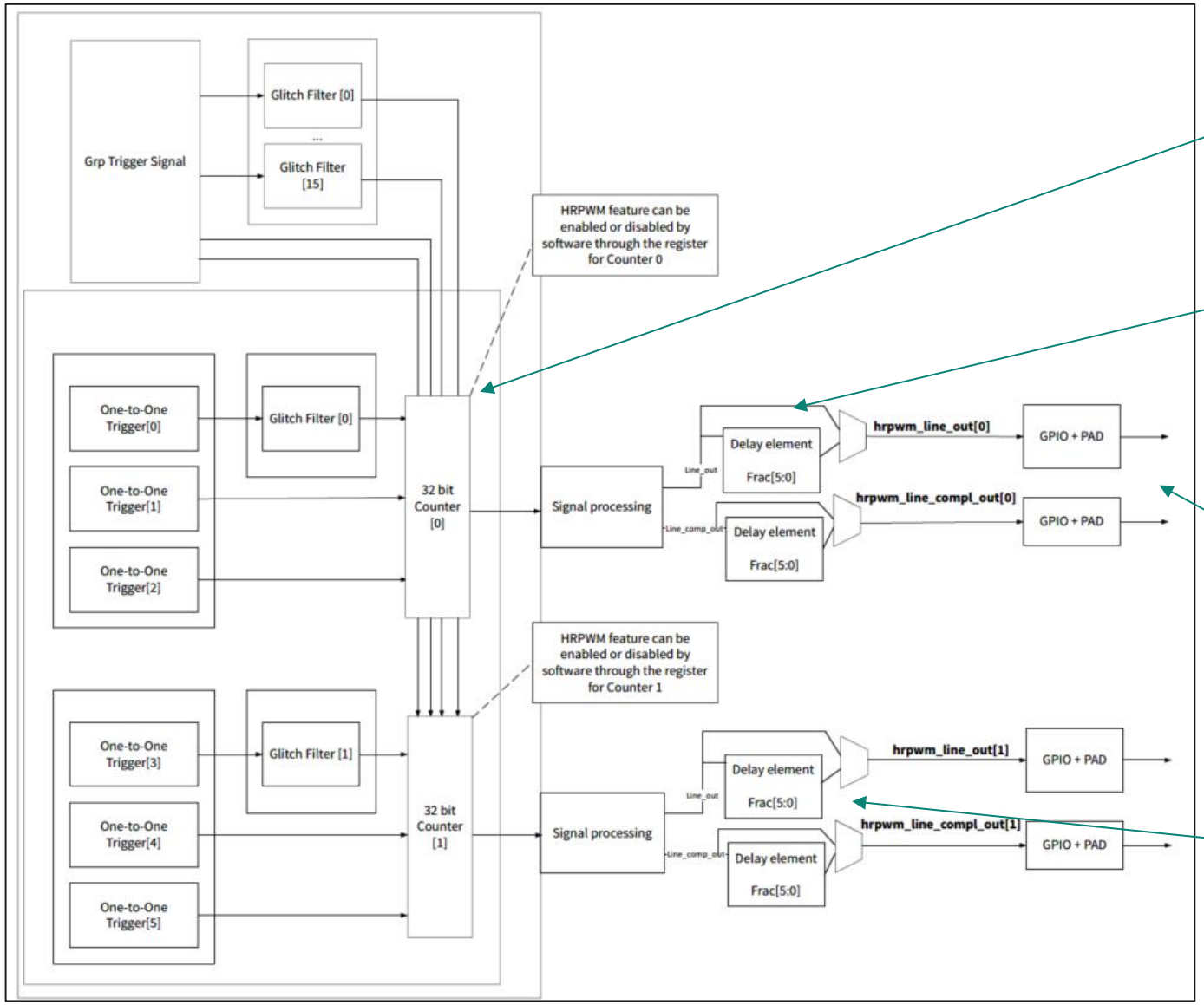
User benefits

- HRPWM enables more accurate control for real-time applications enabling higher switching frequencies, lower ripple and higher system efficiency
- Easy configuration for controlling various SMPS topologies: Half bridge, full bridge, resonant, and phase shift



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HRPWM block diagram



HRPWM features is supported in 32 bit counter TCPWM group

In PWM or PWM_DT mode – HRPWM is enabled
LSBs value = fractional or micro ticks for delay lines for period, duty and dead time

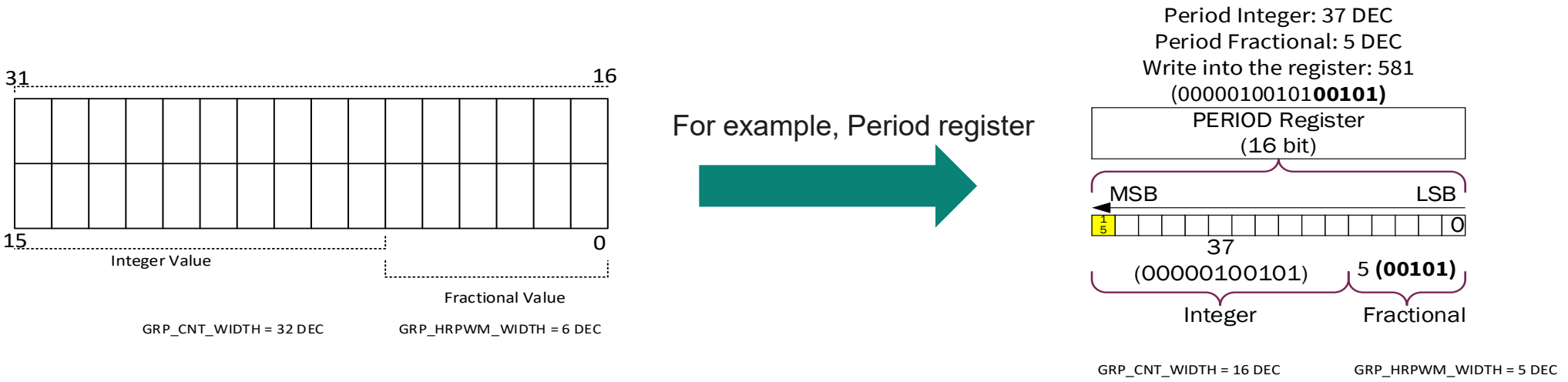
PWM output mode in HRPWM support :
Right Align , left align , center align , center align asymmetric

Each TCPWM counter with HRPWM capability has:
2 delay elements – one for delaying rising-falling edges of line out and another for line_compl_out

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HRPWM function- register handling

- HRPWM in the PWM mode
  - The LSBs 6-bit are used for fractional or micro ticks for delaying the line_out and line_compl_out outputs
    - PERIOD/PERIOD_BUFF, CC0/CC0_BUFF, and CC1/CC1_BUFF and DT/DT_BUFF
  - The MSBs for integer value are used for by the TCPWM counter

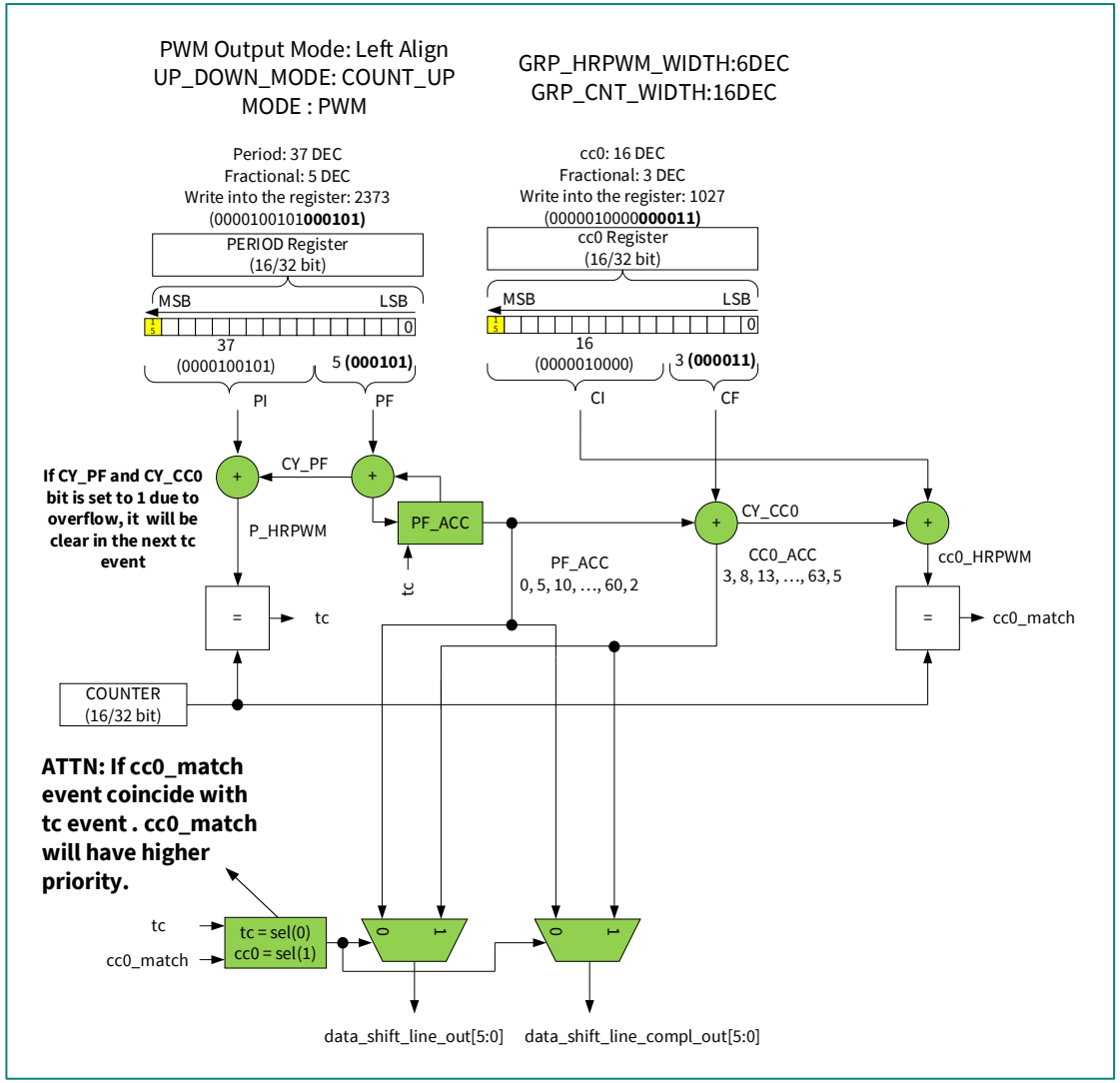


  - Analog interpolator consists of X number of delay elements, where X = 2^(GRP_HRPWM_WIDTH). For PSCO C3, X = 64. The delay (d) introduced by each delay element = PERIOD (clk_out)/X, for PSOC™ C3 with clk_out=240 MHz, d = 65.1ps

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HRPWM function in PWM mode

- Computation
  - Fractional delay is inserted by a delay element, resulting in hrpwm_line_out and hrpwm_line_compl_out of the delay element
- Period Register
  - PERIOD register contains fractional value >0, it is added into PF_ACC
  - When the PF_ACC value overflows, the carry is added into the integer value (PI) of the PERIOD register
  - Carry is cleared at the next TC event
- CCx Register
  - PF_ACC is also added fractional value configured into the CC0/ CC1 Register
  - When the added value CC0_ACC or CC1_ACC overflows
  - Carry is added to the corresponding CC0/CC1 register integer value for the interval of one TC event
  - Carry is cleared at the next TC event



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Calculation of period with HRPWM

- For example,
  Configure TCPWM CNT[0] with HRPWM0_CH0 to generate Output PWM with the following parameters:

  - fOUT = 200.52 KHz (PERIOD)
  - Output duty cycle (DT) = 0,65
  - TCPWM channel clock Source
    CLK_HF3 = 240 MHz
  - TCLK = 4.16ns (@240 MHz)
  - HRES_STEPS = 64
  - tHRES = 65,1ps (240 MHz/HRES_STEPS)
  - TOUT = 1/ fOUT
    = 1/200.52*10^3
    = 4.98703us or 4987.03ns

  - TOUT(Ticks) = TOUT /Tclk (Where Tclk = 1/ fclk_HF3)
  - TOUT(Ticks) = 4987.03ns/4.16ns = 1198,805

  - PERIOD_int[31:6] = Integer(TOUT(Ticks))
    = 1198(0x4AE)

    PERIOD[31:6] = 0x4AE
  - PERIOD_Fract[5:0] = Nearest_Integer[Fraction(TOUT(Ticks)) * HRES_STEPS]
    = Nearest_Interest[0,805*64]
    = Nearest_Interest[51,52]

    Period_Fract[5:0] = ~51(0x33)

  - PERIOD[31:0] = (PERIOD_int[31:6] << 0x6)|(PERIOD_Fract[5:0])
    PERIOD[31:0] = 0b..1 0010 1011 1011 0011 = 0x1 0x2BB3

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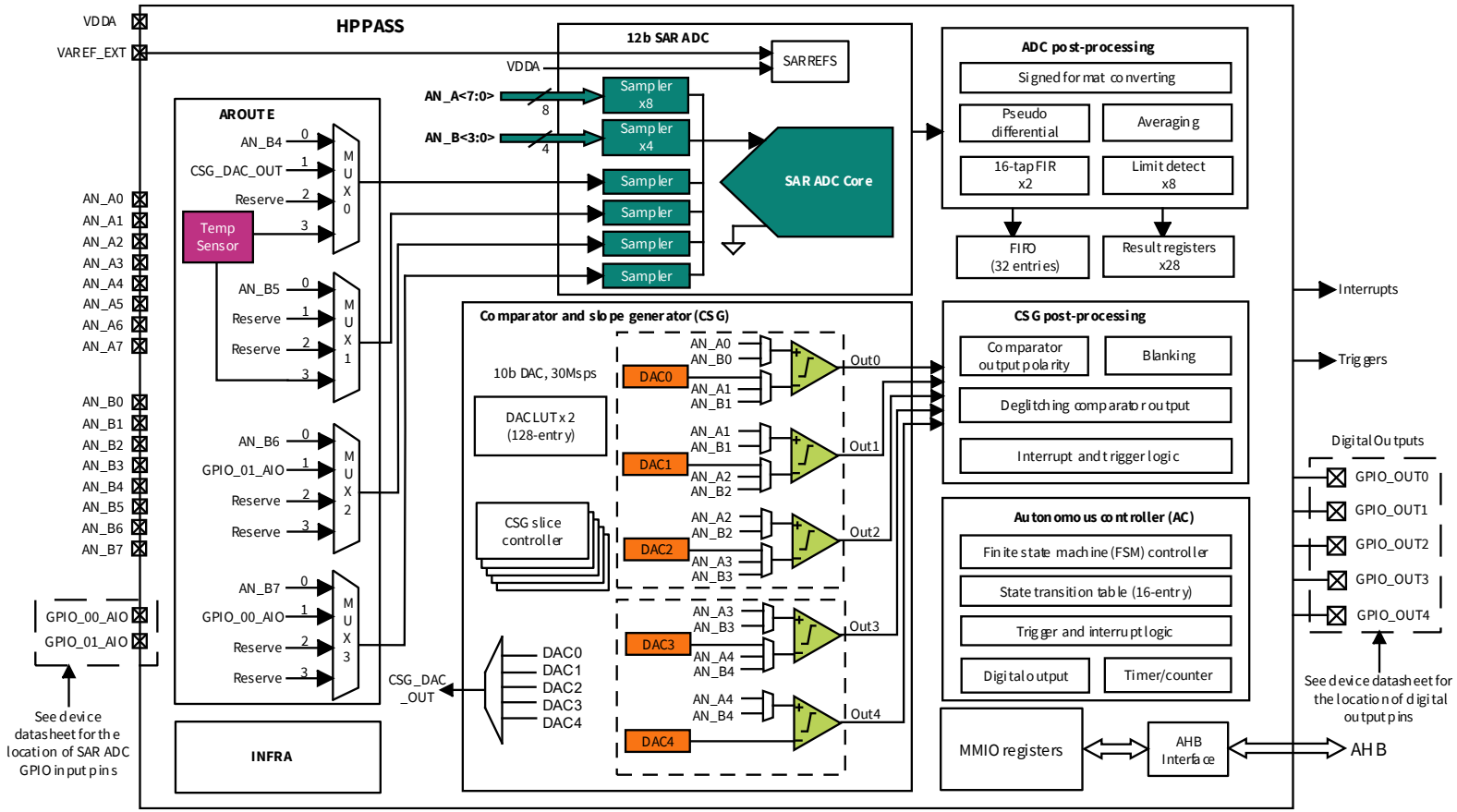
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High-performance programmable analog subsystem (HPPASS)

Block diagram



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Features

- 12-bit SAR ADC
  - When operating in a single-channel, the maximum speed of the ADC is 12 Msps
  - 16 samplers, of which 12x direct and 4x multiplexed. Each generates a simultaneous sampling of an external analog signal. All samplers support gains of 1, 3, 6, 12
  - Up to sixteen dedicated analog pads, connected to up to 16 parallel sample stages
  - Two additional GPIOs can be used as analog inputs by AMUX
  - Two internal voltage signals (temperature sensor and DAC output voltage) can be connected to a muxed sampler by AMUX
  - AMUX can be controlled by a SAR sequencer, firmware, or autonomous controller (AC)
  - 21 channels: Sixteen channels for dedicated analog inputs, two channels for additional GPIOs, and three channels for internal voltage signals
  - Post processing
  - SAR sequencer
  - Self-calibration support for offset, linearity and gain
  - Interrupt generation
  - Four FIFO level triggers, which can trigger other on-chip peripherals (such as DMA, GPIO, TCPWM)
  - On-chip temperature sensor

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Features (contd.)

- Five comparator and slope generators (CSG)
  - Each CSG slice consists of a 10-bit 30Msps DAC to generate the comparator reference
  - Each comparator positive input can select one of two analog inputs
  - Each comparator negative input can select the DAC output or one of two analog inputs
  - Two 128-entry waveform look-up tables (LUT)
  - DAC support direct write mode, buffered mode, hysteretic mode, slope generation mode and LUT waveform generation mode
  - DAC start can be triggered by firmware, triggered from other peripherals or an autonomous controller
  - DAC update can be triggered by firmware, triggered from other peripherals, autonomous controller or comparator output
  - Comparator post processing
    - Configurable comparator output polarity
    - Blanking the comparator
    - Deglitching the comparator output
    - Generate configurable comparator interrupt and or AC trigger
    - Ability to select the comparator output or inverted comparator as an update trigger
  - DAC output can be routed to ADC by AMUX
  - Interrupt generation: comparator output, DAC hardware started, DAC slope done and buffer empty

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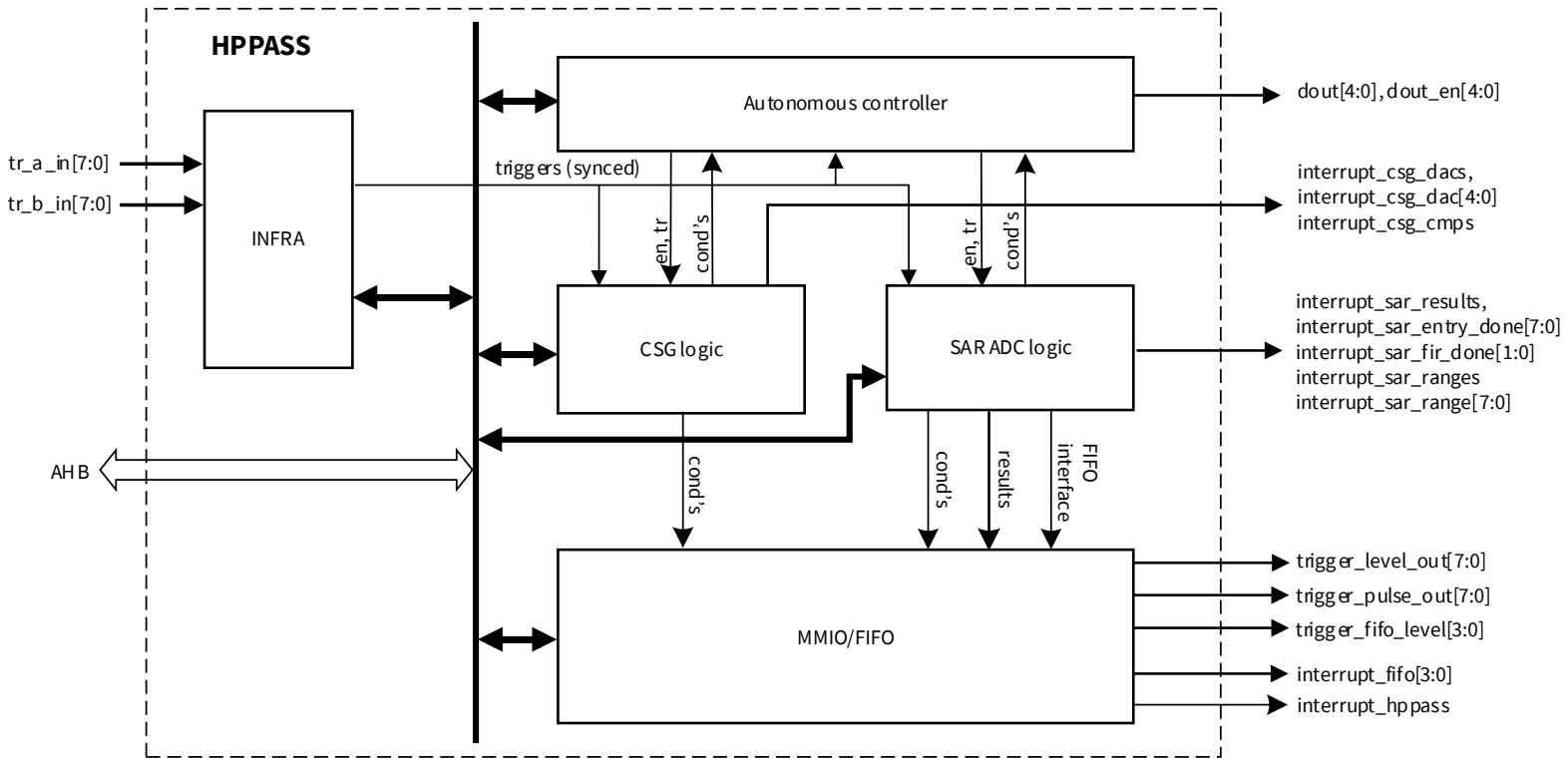
Features (contd.)

- Autonomous controller (AC) is a finite-state machine (FSM) sequencer that works with a sixteen-entry state transition table to transition appropriately through various pre-defined states, based on timer, and/or events. An autonomous controller can perform the following functions:
  - Enable and disable internal blocks (SAR ADC, and CSG), provide a BLOCK_READY status to firmware
  - Hardware or firmware trigger to execute programmed actions
  - Trigger any of the internal blocks
  - Implement hardware delays
  - Periodic action (for example, triggering) in a timed loop
  - Receive conditions from the internal blocks and act on those events
  - Generate an AC-based interrupt to the CPU
  - Digital output to as many as five GPIOs
- Eight input triggers, which can be configured to a firmware-level trigger, a firmware pulse trigger, hardware trigger A (multiplexer trigger), or hardware trigger B (one-to-one trigger)
- Eight output level triggers, each of which can select a CSG comparator output and a SAR ADC limit detection output
- Eight output pulse triggers, each of which can select one pulse trigger from the ADC group, FIR done, and the AC trigger

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Top-level diagram

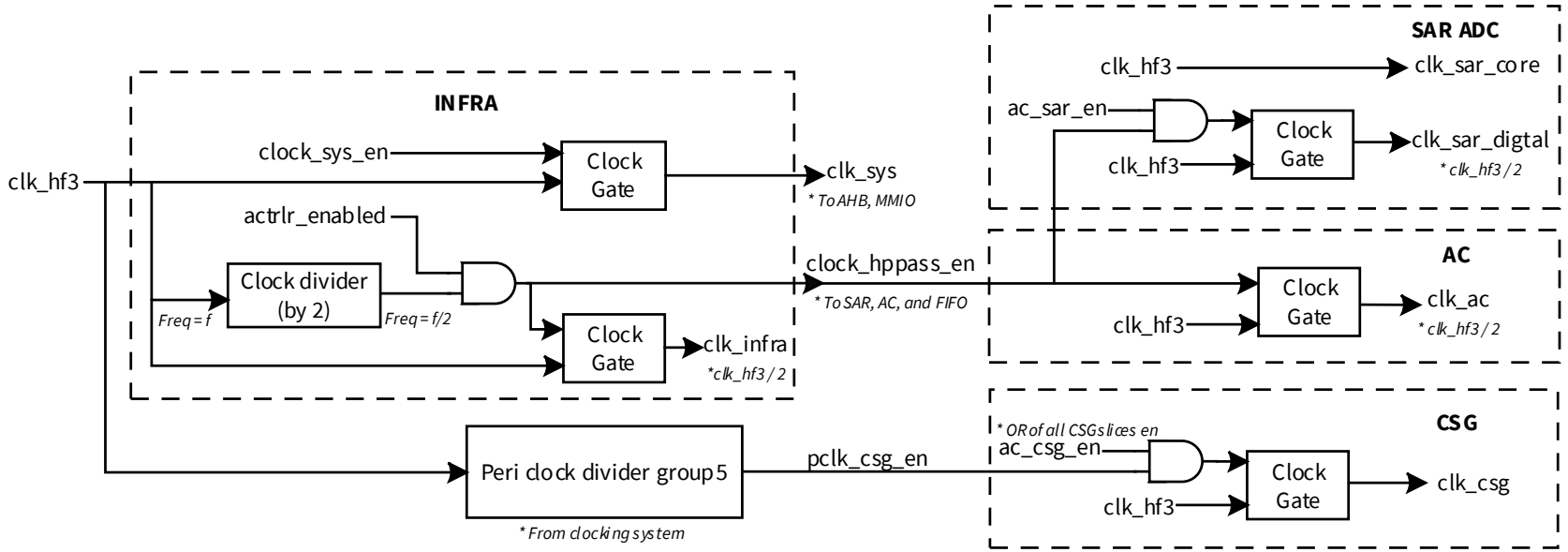
– The figure shows the top-level structure of the HPPASS digital system



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Clock

- HPPASS requires only one clock CLK_HF3, the frequency rang of CLK_HF3 from 60 MHz to 240 MHz
  - SAR ADC core clock directly use CLK_HF3 clock
  - SAR ADC digital part, AC, INFRA clocks are fixed at CLK_HF3/2
  - CSG clock can be configured separately by the peripheral clock divider group 5, so that the source clock comes from CLK_HF3, ranging from 10 MHz to 120 MHz



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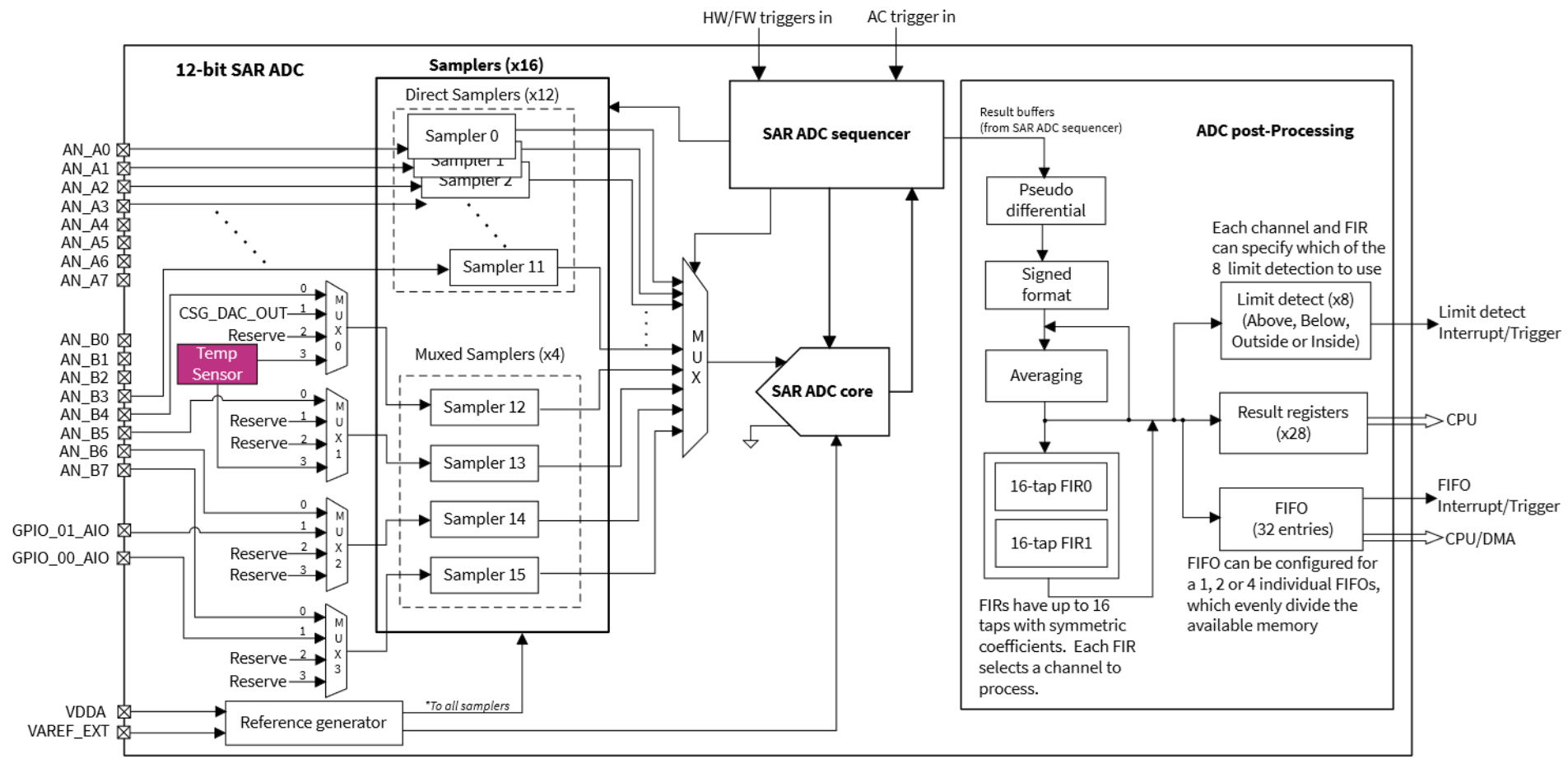
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SAR ADC

Overview - Block diagram

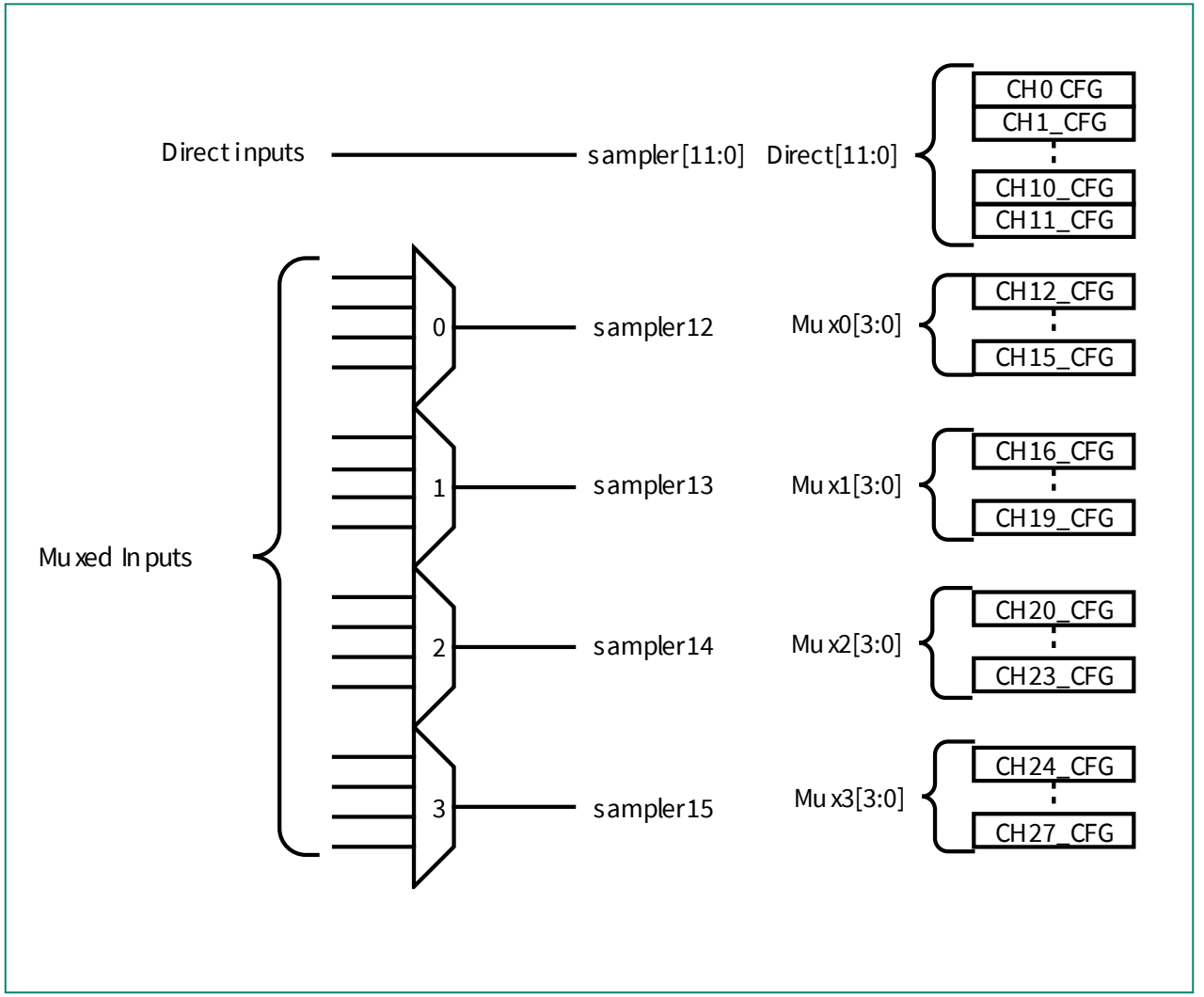
– It consists of a SAR sequencer, samplers, SAR ADC core, and post-processing blocks



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Channels

- Contains twelve direct samplers and four muxed samplers
- All samplers support gains of 1, 3, 6, 12
- Contains 28 SAR channel configurations. However, some of the multiplexed inputs are reserved; the actual channel mapping is listed in the table on the following slide



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Channels (contd.)

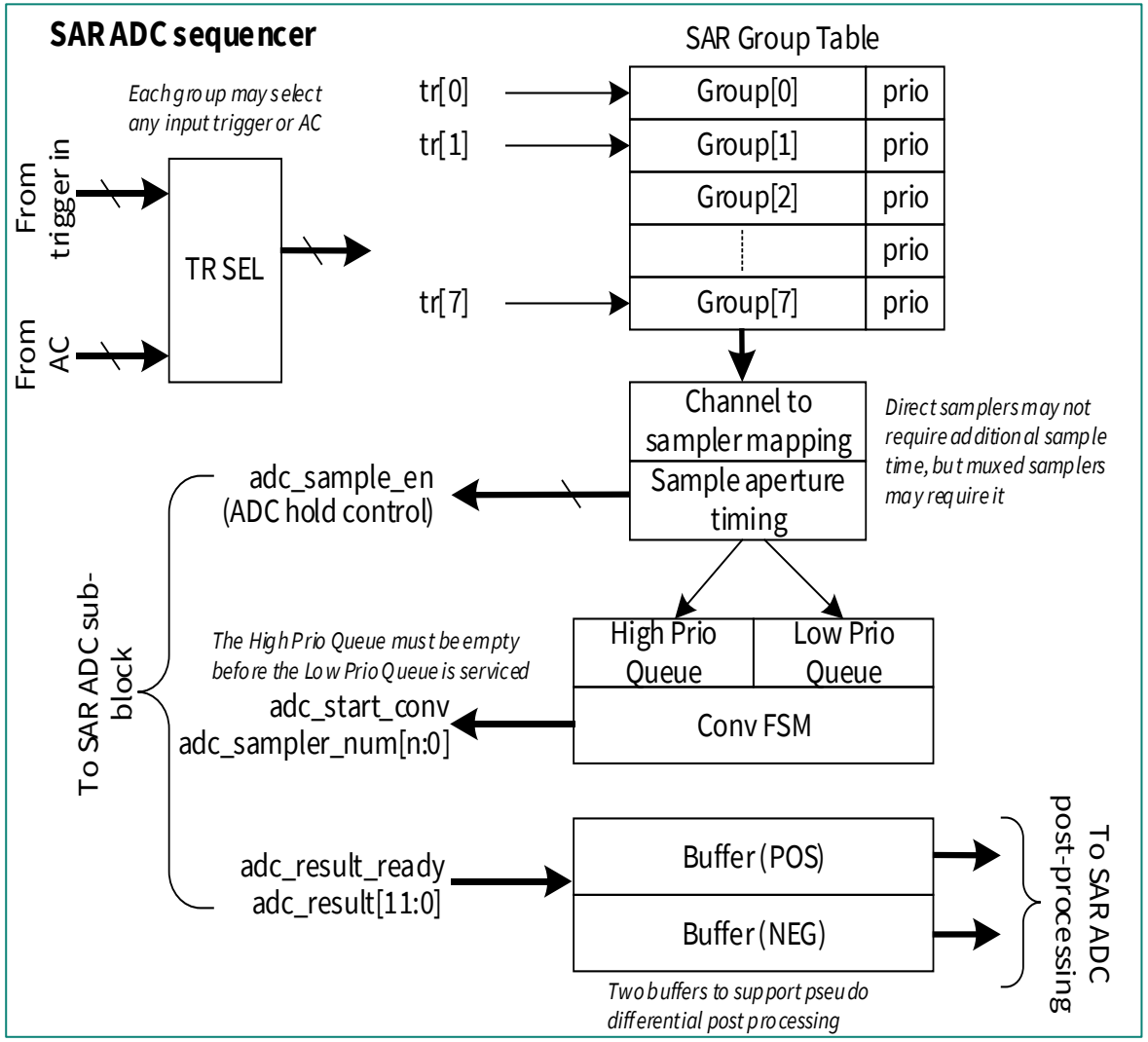
Channel num.	Sampler	Type	Input
0	Sampler 0	Direct	AN_A0
1	Sampler 1	Direct	AN_A1
2	Sampler 2	Direct	AN_A2
3	Sampler 3	Direct	AN_A3
4	Sampler 4	Direct	AN_A4
5	Sampler 5	Direct	AN_A5
6	Sampler 6	Direct	AN_A6
7	Sampler 7	Direct	AN_A7
8	Sampler 8	Direct	AN_B0
9	Sampler 9	Direct	AN_B1
10	Sampler 10	Direct	AN_B2
11	Sampler 11	Direct	AN_B3

Channel num.	Sampler	Type	Input
12	Sampler 12 for MUX 0	MUX0 select 0	AN_B4
13		MUX0 select 1	CSG DAC OUT
14		MUX0 select 2	Reserve
15		MUX0 select 3	Temp sensor
16	Sampler 13 for MUX 1	MUX1 select 0	AN_B5
17		MUX1 select 1	Reserve
18		MUX1 select 2	Reserve
19		MUX1 select 3	Temp sensor
20	Sampler 14 for MUX 2	MUX2 select 0	AN_B6
21		MUX2 select 1	GPIO_01_AIO
22		MUX2 select 2	Reserve
23		MUX2 select 3	Reserve
24	Sampler 15 for MUX 3	MUX3 select 0	AN_B7
25		MUX3 select 1	GPIO_00_AIO
26		MUX3 select 2	Reserve
27		MUX3 select 3	Reserve

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Sequencer

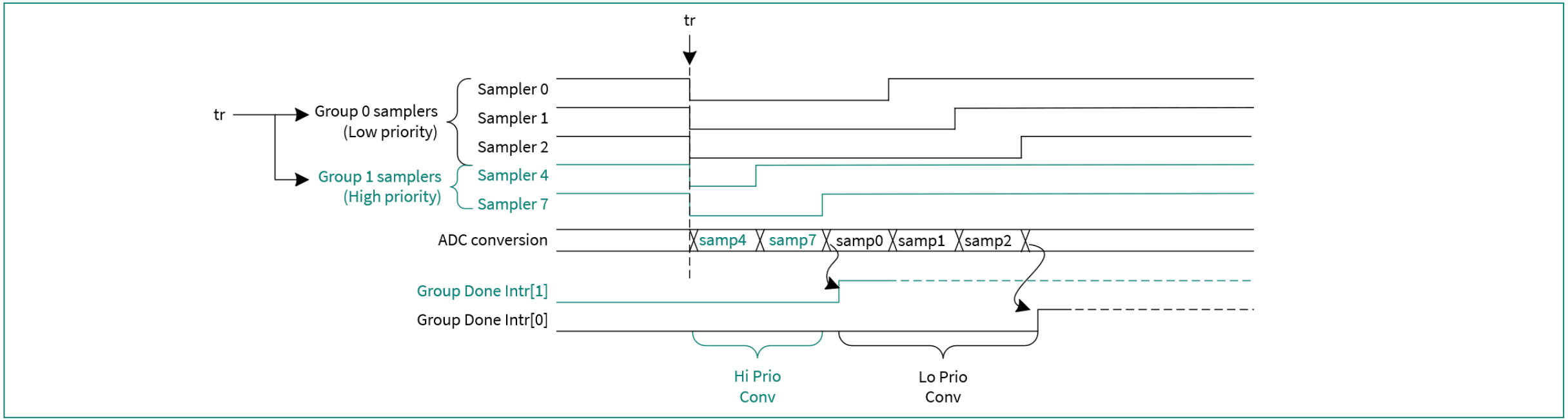
- Sequencer is controlled by a SAR group table, which consists of eight entries
- In a given group, up to sixteen samplers can be enabled for simultaneous sampling
- Each group can select a different input from each muxed samplers
- Every group can be triggered by firmware, triggered from other peripherals (TCPWM and GPIO) or AC
- Every group can select one of three available programmable sample times
- Two priorities: LOW or HIGH programmable per group
- Every group supports continuous mode



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Illustration of triggering, sampling and conversion priority

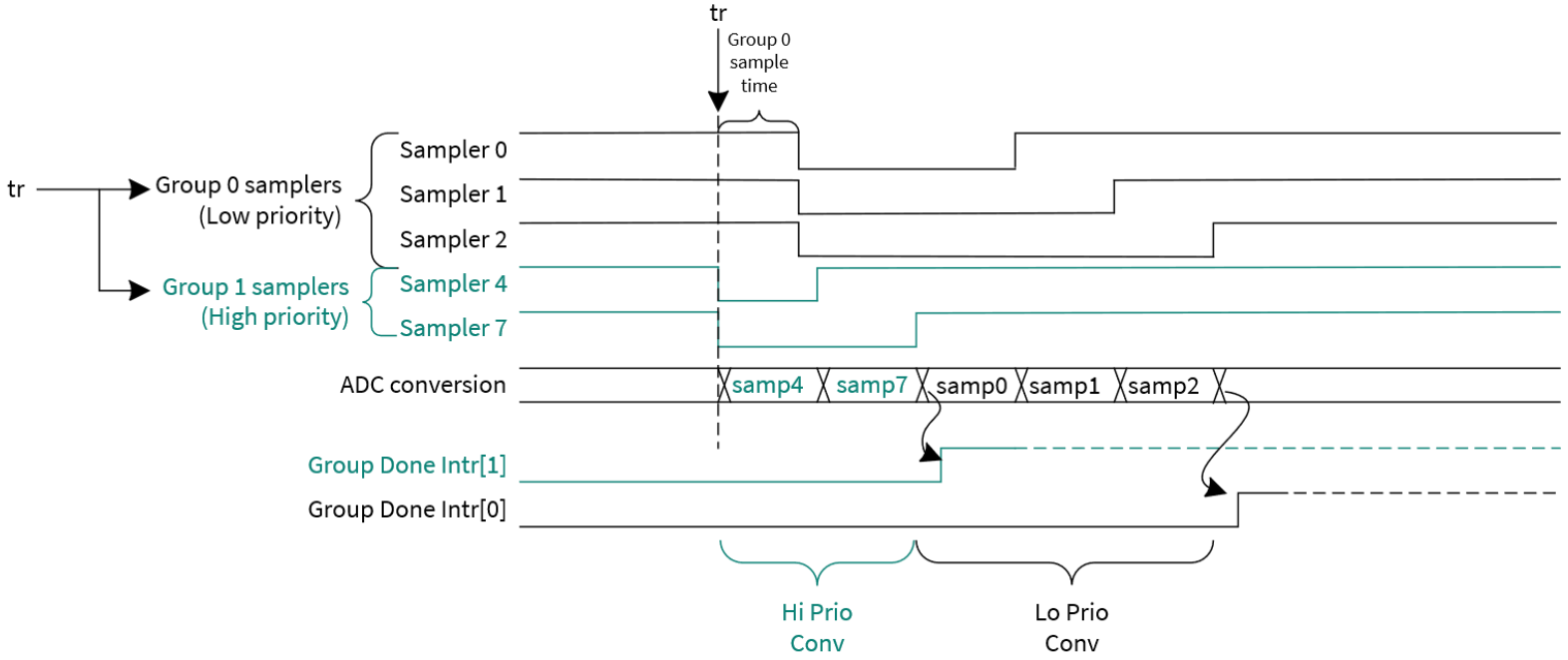
– Simple trigger scenario: the figure shows the simple case of one trigger routed to two groups with different priorities



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Illustration of triggering, sampling and conversion priority (contd.)

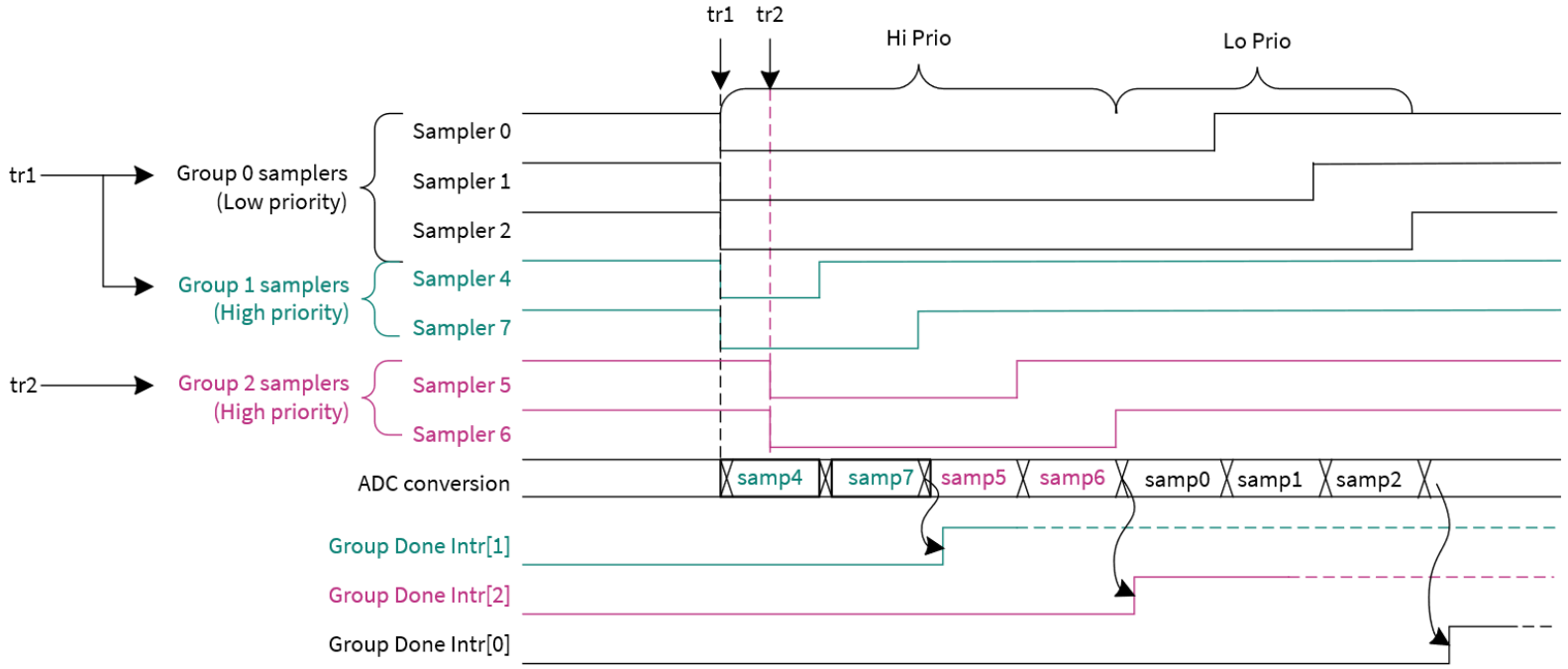
– Simple trigger scenario with sampling time: the following diagram shows the same case, but where Group 0 has a programmed sampling time greater than '0'



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Illustration of triggering, sampling and conversion priority (contd.)

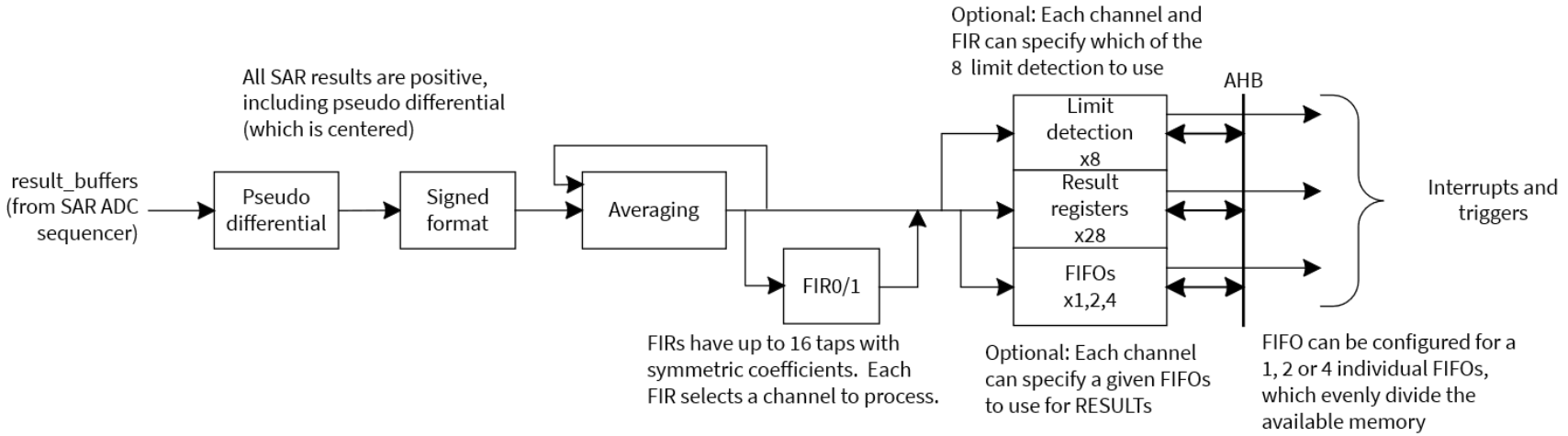
– Multiple trigger scenario: a new trigger is asserted for different groups, while the channels of a previously triggered group or groups are being held or converted



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Post-processing

- The post-processing has the following features:
  - Pseudo-differential hardware subtraction
  - Signed format
  - Accumulation/Averaging (N result, where N is 2,4,8,16)
  - FIR processing
  - Limit detection



Note: The pseudo-differential mode is enabled for a given channel; the averaging mode of this channel must be set to disable.

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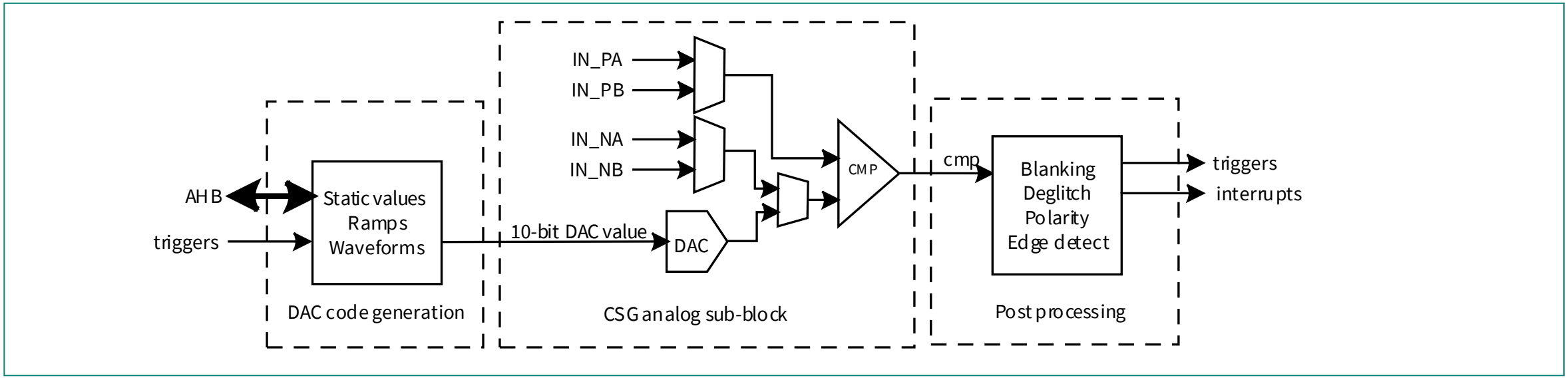
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Comparator and slope generator (CSG)

Overview

- Compares a 10-bit 30-Msps DAC value with a selected analog input signal, or compares two analog inputs
  - DAC is only used as an internal reference and cannot be measured outside of the chip; however, ADC can measure it



- The figure is considered a slice, and the PSOC™ Control C3 MCU supports five slices

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Inputs

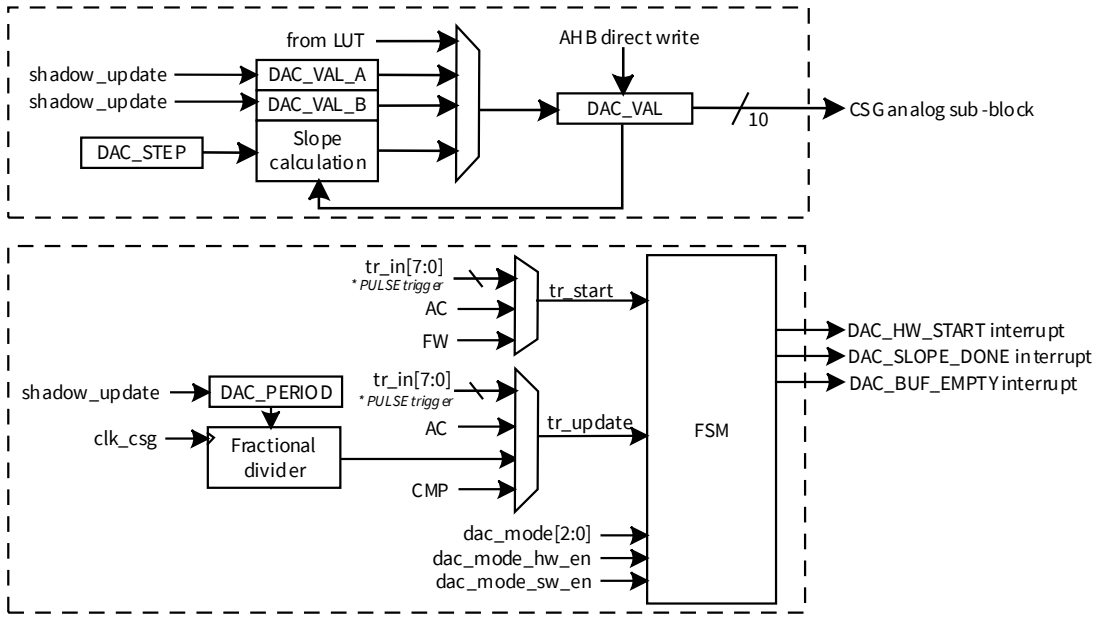
– The table lists comparators of all inputs for every slice

Slice	Comparator positive inputs	Comparator negative inputs
Slice 0	AN_A0/AN_B0	DAC0/AN_A1/AN_B1
Slice 1	AN_A1/AN_B1	DAC1/AN_A2/AN_B2
Slice 2	AN_A2/AN_B2	DAC2/AN_A3/AN_B3
Slice 3	AN_A3/AN_B3	DAC3/AN_A4/AN_B4
Slice 4	AN_A4/AN_B4	DAC4

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10-bit DAC

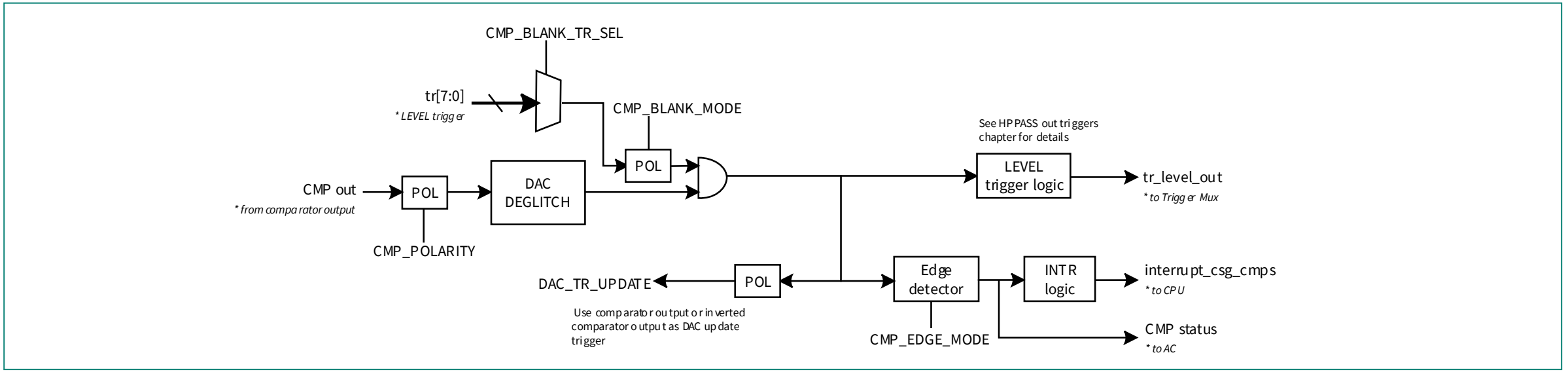
- There are various modes of generating and controlling the DAC codes. It contains the following modes:
  - Direct firmware control of DAC code
  - Buffered firmware control of DAC code
  - Two-value (Hysteretic) control of DAC code
  - Automatic DAC ramp generation
  - Look-up table (LUT) for DAC arbitrary waveform generation



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Post-processing

- The main features are as follows:
  - Configuring the comparator output polarity
  - Blanking the comparator, gating it to ‘0’ with an input level trigger
  - Deglitching the comparator output that may occur due to a DAC code change; the comparator output is latched for a programmable number of clock cycles
  - Generating a configurable comparator interrupt and or AC status
  - Ability to select the comparator output or inverted comparator output as an update trigger (only used for hysteresis mode)



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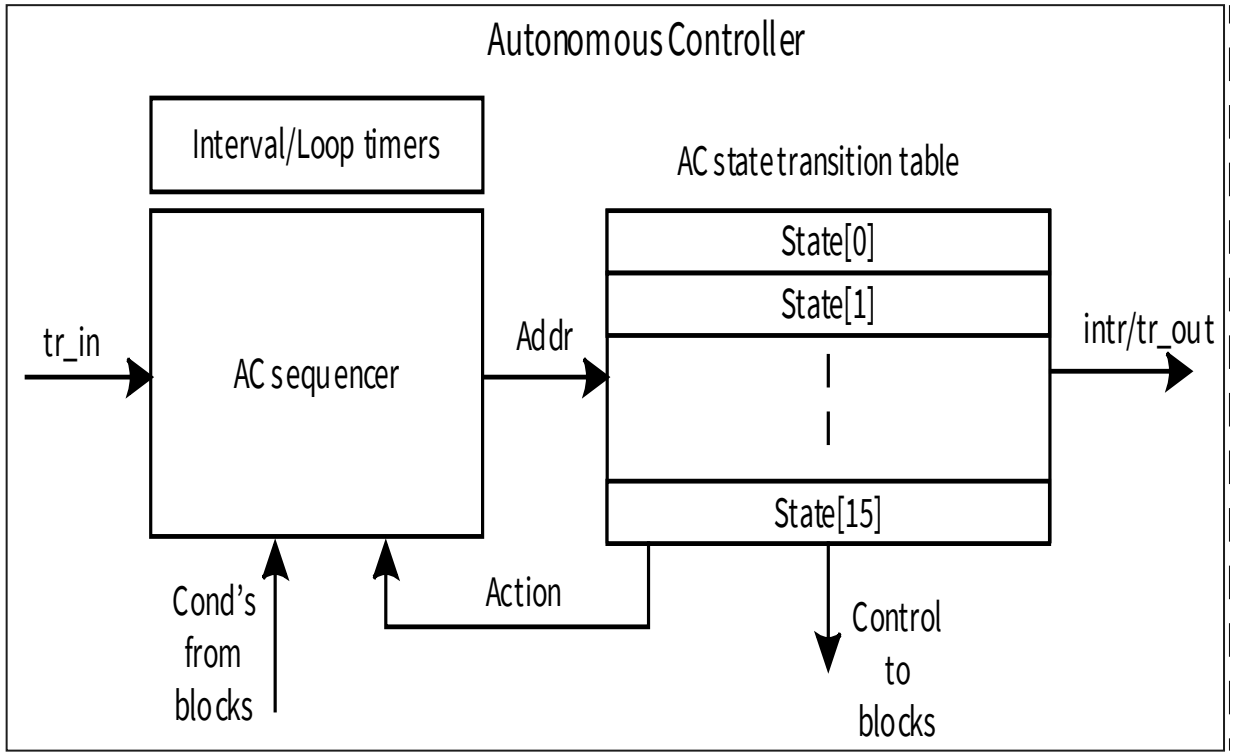
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Autonomous controller (AC)

Overview

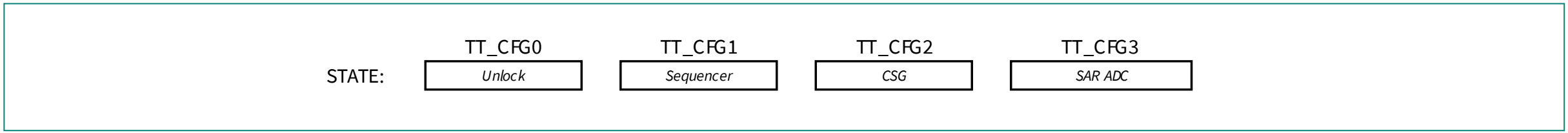
- The AC is a programmable state machine; it consists of a memory-based state transition table ("timer table"), sequencer, and timers
- It has the following capabilities:
  - Enabling and disabling of blocks, providing BLOCK_READY status to the firmware
  - Ability to be triggered by hardware/firmware and execute programmed actions
  - Triggering any of the HPPASS internal blocks (SAR groups, CSG slices)
  - Implementing hardware delays
  - Taking periodic action (for example, triggering) in a timed loop
  - Receiving conditions from the HPPASS internal blocks and acting on those events
  - Generating an AC-based interrupt to the CPU
  - Monitoring the SAR ADC limit detection condition and taking action based on the status



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State transition table

- The AC program is stored in a RAM table (called a state transition table), which consists of 16 states (or programming instructions)
- Each instruction state spans four registers (TT_CFG0, TT_CFG1, TT_CFG2, TT_CFG3) with the following organization



  - Unlock: If you unlock a given block enabled in a given state, it's only in that state that the enable is updated. This prevents inadvertent mode transitions in the normal course of AC program execution
  - Sequencer: This is the brain of the AC. In this register, the actual program flow is specified with delays, loops, branches, and condition checking
  - CSG: Used to enable and optionally trigger the CSG slices
  - SAR ADC: Used to enable the SAR ADC and optionally trigger SAR ADC groups, and control AROUTE

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Example

- If averaging (accumulation) by N is configured for channels in a given group, only one result is generated every N triggers for that ADC group
- The following routine waits for an HPPASS internal trigger (can be an external hardware or firmware trigger), then triggers the indicated SAR ADC group 16 times, each time waiting for SAR ADC group conversion done (SAR_ENTRY_DONE) condition, and then jumps back to wait for the next HPPASS trigger

```
STATE:TOP
  ACTION=WAIT_FOR  COND=HW_TR0_IN

STATE:TR_SAR
  SAR_TR=0x01  ACTION=WAIT_FOR  COND=SAR_ENTRY0_DONE

STATE:
  ACTION=BRANCH_IF_FALSE  BR_ADDR=TR_SAR  COND=CNT_DONE  CNT=15

STATE:
  ACTION=BRANCH_IF_TRUE  BR_ADDR=TOP  COND=TRUE
```


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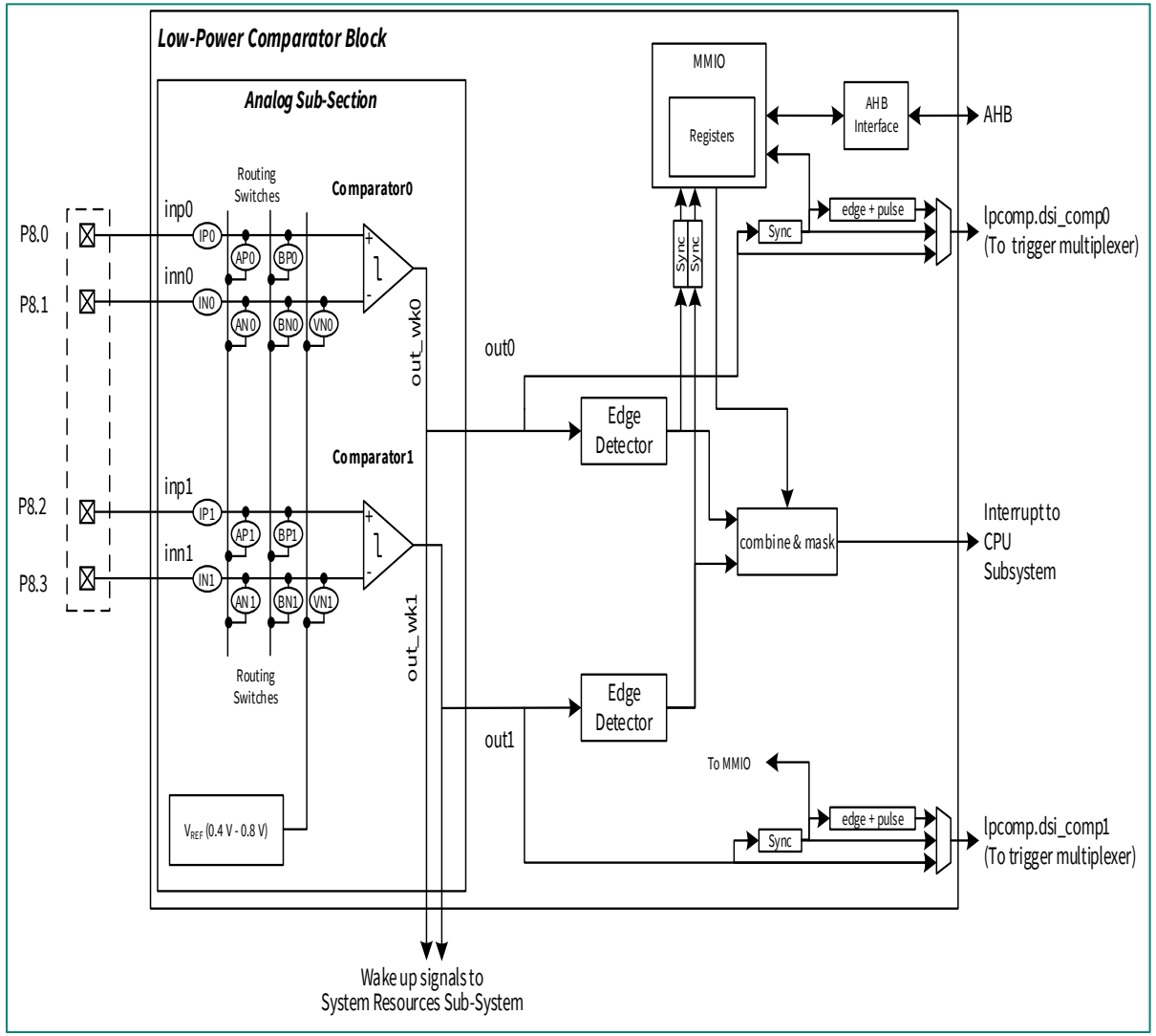
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Low-power comparator (LPCOMP)

Features

- Programmable power and speed
- Ultra-low-power mode support
- Each comparator features a one-sided hysteresis option
- Rising edge, falling edge, and combined rising and falling edge detection at the comparator output
- Local reference voltage generation
- Wake-up source from low-power modes



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Input and output configuration

- Low-power comparator operates with the following input options, and the internal routing can be configured by setting the LPCOMP_CMPx_SW and LPCOMP_CMPx_SW_CLEAR registers
  - Compare two voltages from external pins
  - Compare external signals with a locally generated reference voltage

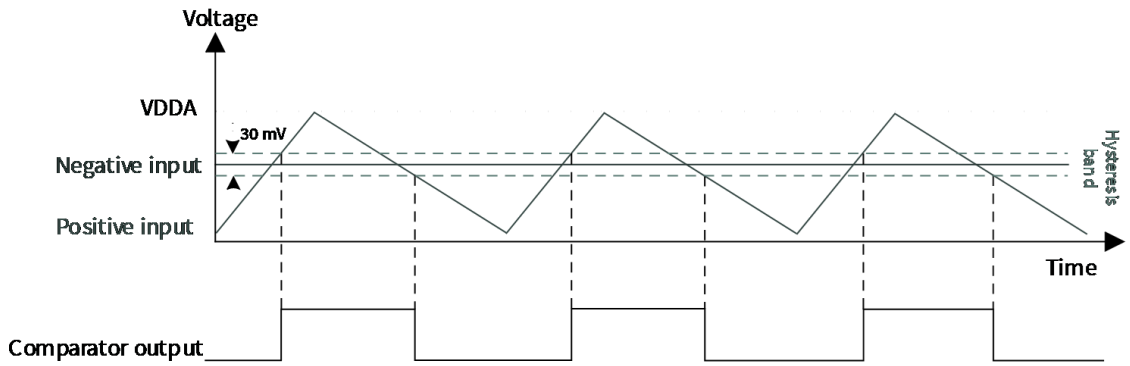
  Note: this voltage is not a calibrated reference and can vary from 0.4 V to 0.8 V. Ensure that the external analog input voltage is less than 0.4 V or greater than 0.8 V when compared against the internal reference.

- Comparator output can be configured to one of the following options by DSI_BYPASSx and DSI_LEVELx bits of the LPCOMP_CMPx_CTRL register
  - Direct comparator output
  - Synchronous comparator output - level
  - Synchronous comparator output – pulse
- Comparator output can be routed to GPIOs and other on-chip peripherals (DMA/TCPWM) by trigger multiplexer
- Comparator output is connected to an edge detector block. This block determines the edge that triggers the interrupt. The edge selection is configured using the INTTYPEx bit of the LPCOMP_CMPx_CTRL register

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Power mode and hysteresis

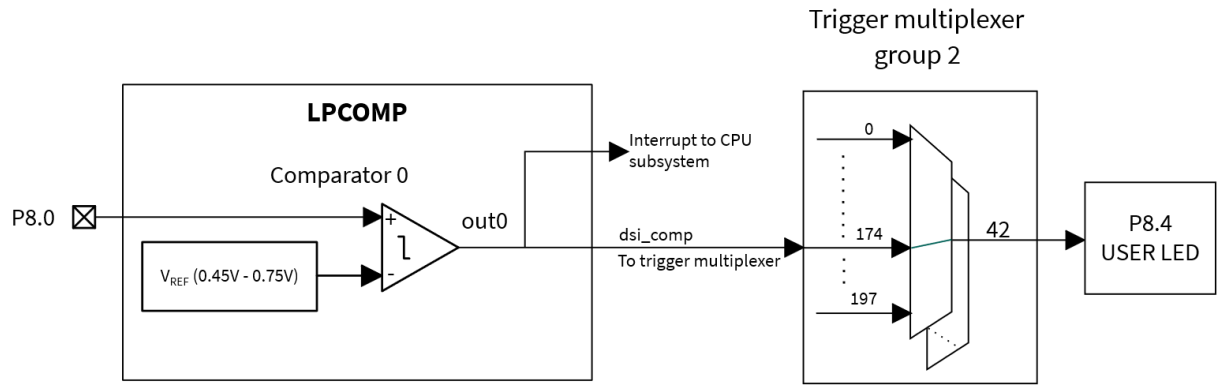
- Provides three power modes, it is configured using the MODEx bit of the LPCOMP_CMPx_CTRL register
  - Normal
  - Low-power
  - Ultra-low-power
- Normal/Low-power modes can only be used in the Active and Sleep modes; Utra-low-power mode is allowed only in Deep Sleep and Hibernate modes
- Hysteresis helps to avoid oscillations at the comparator output when the signals are noisy
  - Enabled/disabled it by using the HYSTx bit in the LPCOMP_CMPx_CTRL register
  - The figure shows the waveform of the comparator output with hysteresis enabled



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Wake up from low-power modes

- Operational in the device's low-power modes (Sleep, Deep Sleep, and Hibernate)
- Have the following restrictions when operating in Deep Sleep and Hibernate modes
  - Comparators should be operated in Ultra-low-power mode
  - Input to the comparator should come from the dedicated pins. The internal reference VREF is available and can be connected to the negative inputs of the comparator
- The following drawing shows the comparison of an external input voltage (P8.0) with an internal reference voltage to wakeup MCU from Deep Sleep mode, LED P8.4 is used to indicate the comparison result



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Lab 1 – Generate PWM signals to control the brightness of LEDs

Lab 1 – Generate PWM signals to control the brightness of LEDs

- PWM_Square_Wave example demonstrates how to use PWM signals to control the brightness of LEDs on Infineon's PSOC™ Control C3M5 Evaluation Kit

- What will we learn?
  - Configuring TCPWM and GPIO interrupt
  - The GPIO interrupt changes the PWM duty cycle to achieve variations in LED brightness

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Lab 2 - Read the voltage from a potentiometer (POT)

Lab 2 - Read the voltage from a potentiometer (POT)

- HPPASS ADC basic example demonstrates how to use the SAR ADC to measure the external input voltage from a potentiometer in Infineon's PSOC™ Control C3M5 Evaluation Kit

- What will we learn?
  - Configuring analog subsystem and SAR ADC
  - Reading voltage from ADC RESULT register

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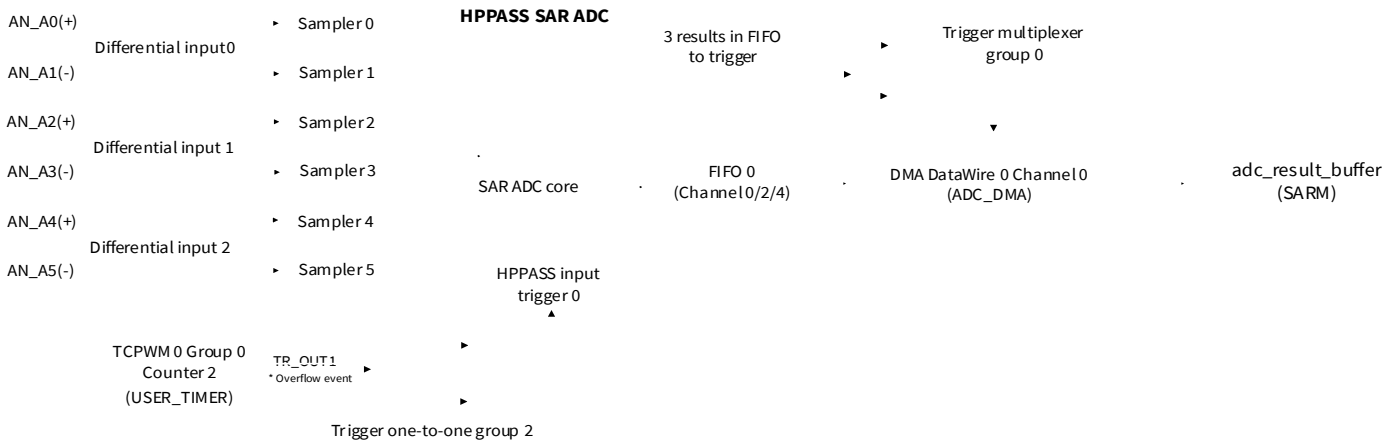
9 **Lab 3 - Use the TCPWM timer to trigger ADC conversions and read the resulting ADC values 66**

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Lab 3 - Use the TCPWM timer to trigger ADC conversions and read the resulting ADC values

Lab 3 - Use the TCPWM timer to trigger ADC conversions and read the resulting ADC values

– HPPASS SAR ADC differential measurement example demonstrates how to use HPASS SAR ADC pseudo-differential feature to measure the differential input voltage and use the TCPWM timer to trigger ADC conversion in Infineon's PSOC™ Control C3M5 Evaluation Kit



– What will we learn?
  – Triggering ADC conversion by TCPWM timer
  – Differential input voltage measurement by SAR ADC pseudo-differential function
  – Getting ADC result by SAR ADC FIFO and DMA

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Revision history

Document revision	Date	Description of change
**	2026-02-09	Initial release

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