

PSOC™ control C3 (PSC3M3x,PSC3P2x, PSC3M5x,PSC3P5x) GPIO/SmartIO and serial communication block (SCB)

Customer training workshop (CTW)

February 2026

public

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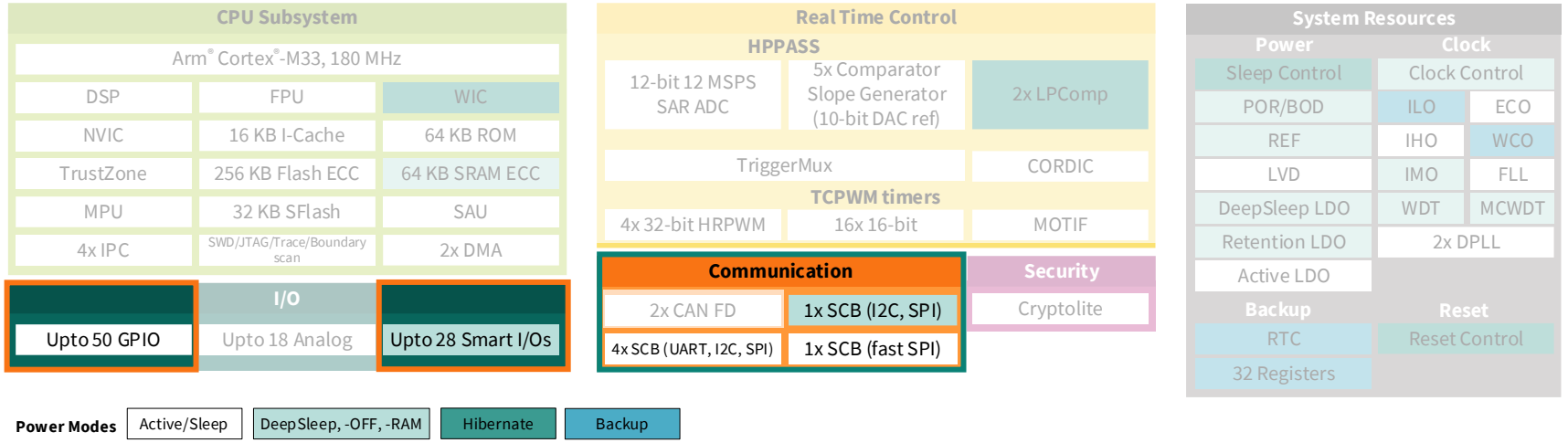
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PSOC™ Control C3 GPIO/SmartIO

I/O subsystem : GPIO/SmartIO



Features

- Each IO can be individually configurable to one of the eight drive modes, input trigger modes or slew rate
- Programmable slew rate control
- Hold mode for latching the previous state
- Support a multiplexing network called High-speed I/O matrix
- Smart IO supporting Boolean functions in the I/O signal path
- Edge-triggered interrupts rising, falling, and both on all GPIO Secure aware GPIO configurations

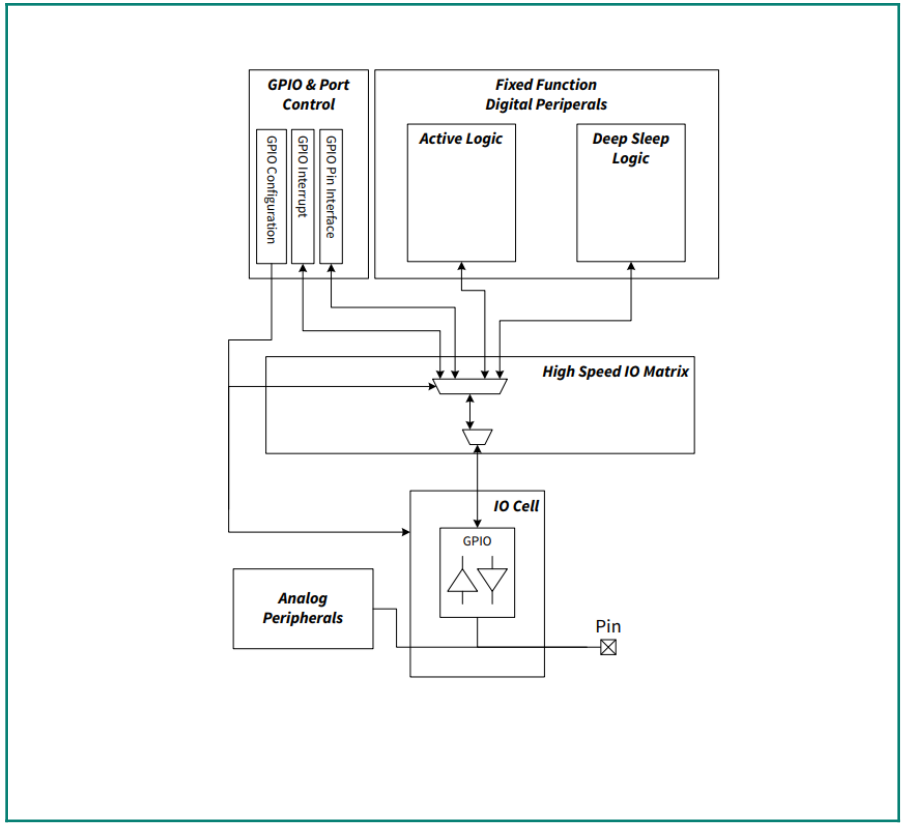
Benefit

- Flexibility for the user to adapt to the different usage situations of GPIOs
- Slower slew rate support in reducing EMI and crosstalk for low-frequency signals
- Advantage of reducing power consumption while keeping the last IO driver state in Low-power mode
- Allow GPIOs to be shared with multiple functions and multiplex the pin connection to a particular peripheral selected by the user

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I/O system block diagram

- GPIO pins are connected to I/O cells
- I/O configuration through the registers
- GPIO and port control I/O cell feature
  - Digital input
  - Digital output drive modes
  - Slew rate control
  - GPIO SMC (Stepper mode control)
  - High-speed I/O
  - Interrupt
  - Behavior in low-power modes
- Digital peripherals connect to IO cells via high- speed I/O matrix (HSIOM)
- HSIOM allows GPIOs to be shared with multiple functions
- Sixteen dedicated analog pins



Hint bar

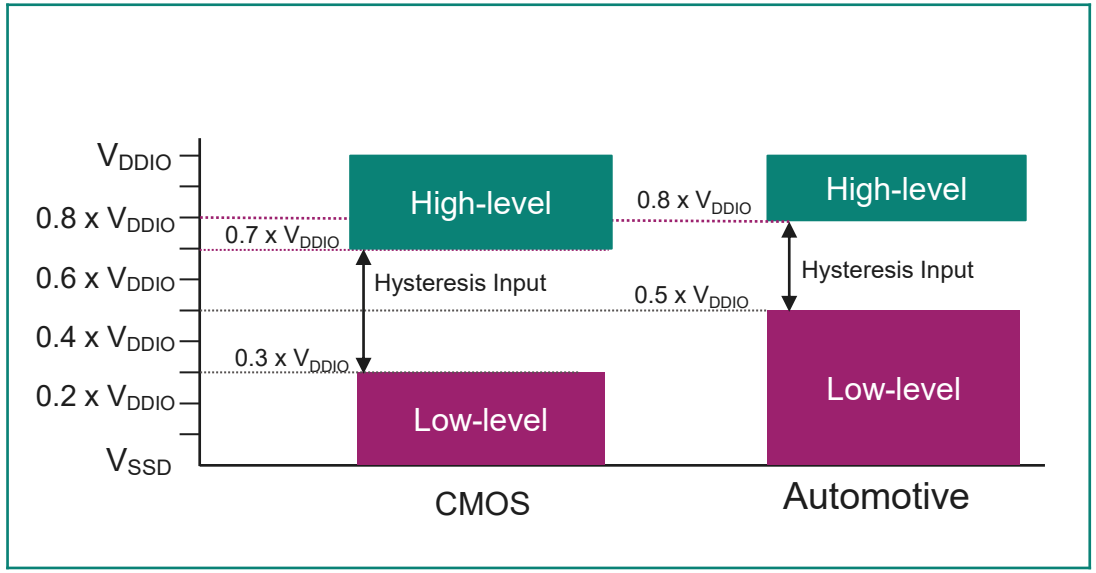
See the architecture reference manual, Architecture (section 23.2), for additional details.

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Digital input

- Each pin's input buffer trip point is configurable for the following modes:
  - CMOS (default)
    - VIH: 0.7 × VDDIO
    - VIL: 0.3 × VDDIO
  - TTL
    - VIH: 2.0 V
    - VIL: 0.8 V

Input spec



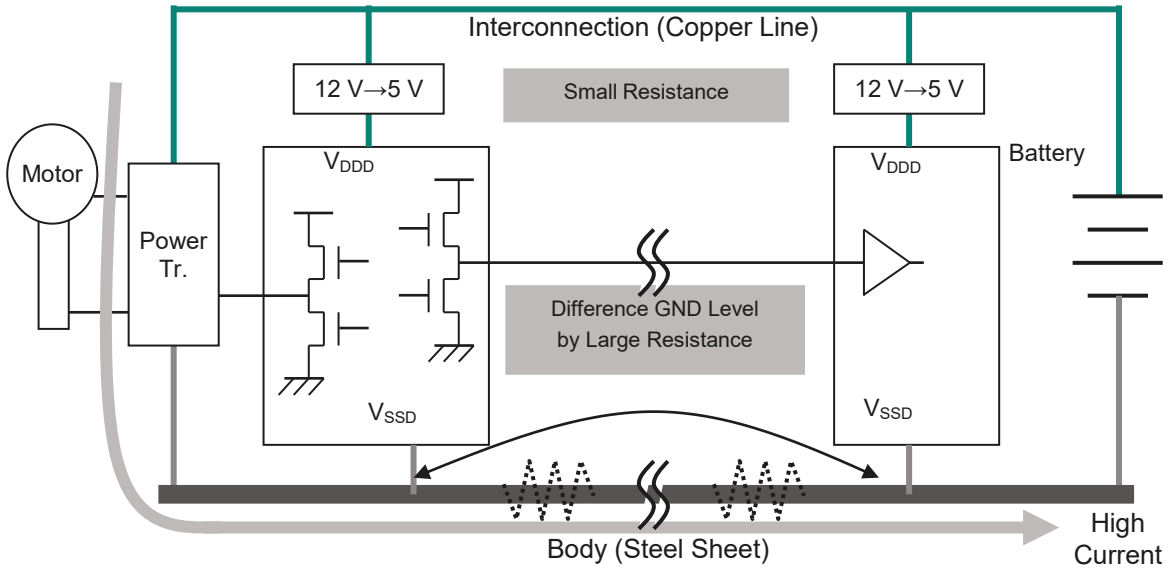
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See the architecture reference manual, Digital input buffer (section 23.3.1), for additional details.

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Digital input (contd.)

Use case



– Supports higher threshold input for GND variation that occurs due to high current in the electronic control unit (ECU)

Hint bar

See the architecture reference manual, Digital input buffer (section 23.3.1), for additional details.

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Digital output

- Each I/O is individually configurable to one of eight drive modes by software[1]
- Default pin reset is high-impedance (High-Z) drive mode with input buffer disabled
- Use case
  - 0: Analog/digital input/unused
  - 1: Resistive pull up and down at the same time for SMC- Not Supported
  - 2-3: Interface with open-drain drive lines
  - 4: Signal is externally pulled up (for example, I^2C)
  - 5: The signal is externally pulled down
  - 6: Digital output signal or drive external devices
  - 7: Be driven by other signals

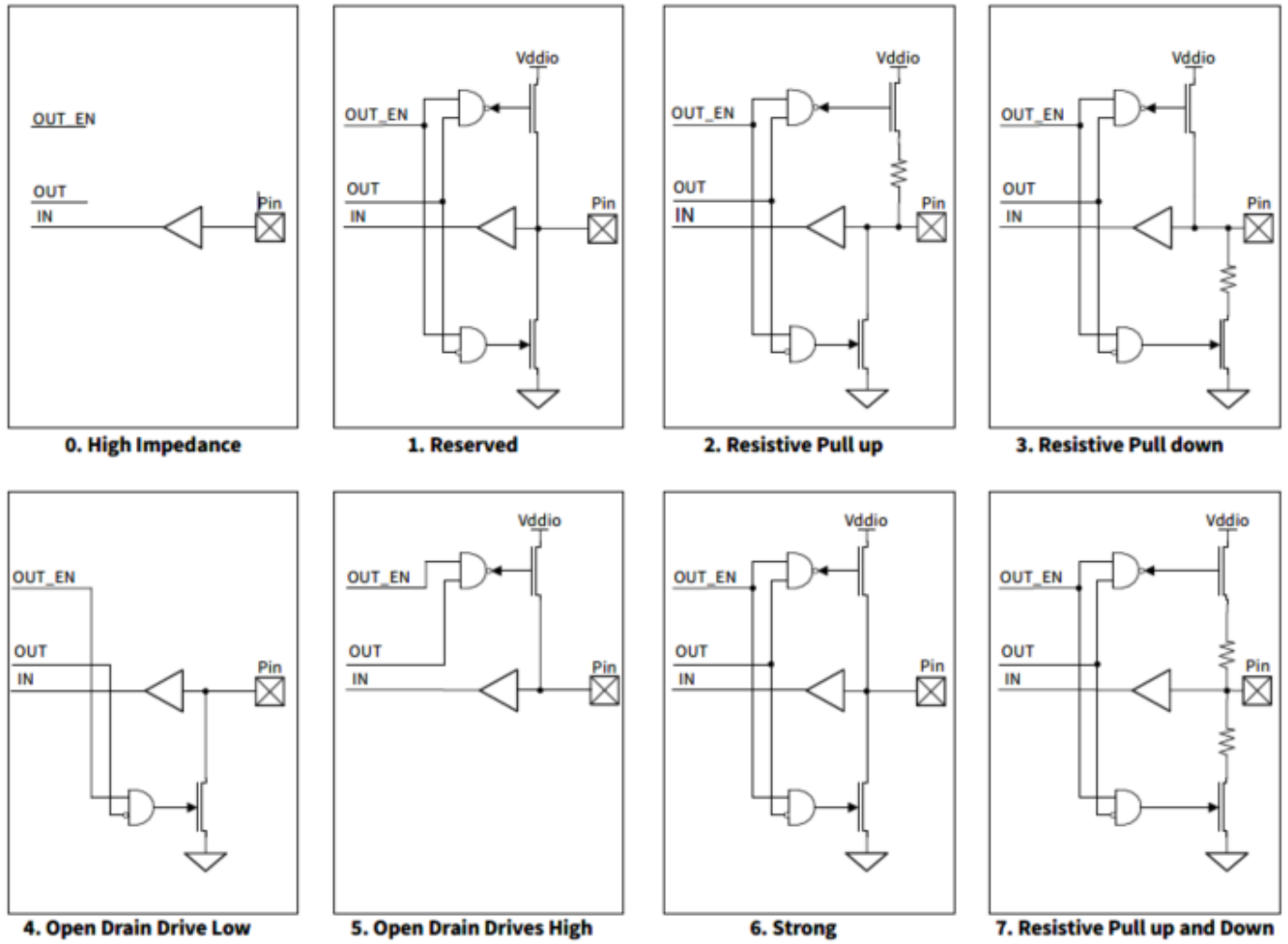
Hint bar

See the architecture reference manual, Drive mode (section 23.3.2.3), for additional details.

[1] See the Register reference manual (GPIO_PRTx_CFG) for additional details.

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Digital output (contd.)



Hint bar

See the architecture reference manual, Drive mode (section 23.3.2.3), for additional details.

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GPIO drive strength and slew rate control

- Programmable output driver configuration for some GPIO pins1
  - Fast slew rate
    - Full drive strength: drive select 0, 1 (current)
    - 1/2 drive strength: drive select 2
    - 1/4 drive strength: drive select 3
  - Slow slew rate
    - Full drive strength: 0

Spec	Slew rate mode	Min	Max	Conditions
Tr/Tf	Fast, full drive Strength = 0	–	2.5 ns	10%/90% 15 pF load
	Slow, full drive Strength = 0	42-48 ns	93-102 ns	

- Advantage
  - Slower slew rate can reduce EMI and crosstalk
- Use case
  - Slower slew rate is used for low-frequency signals or signals without strict timing constraints

Hint bar

See the architecture reference manual, Slew rate control (section 23.3.2.1), for additional details.

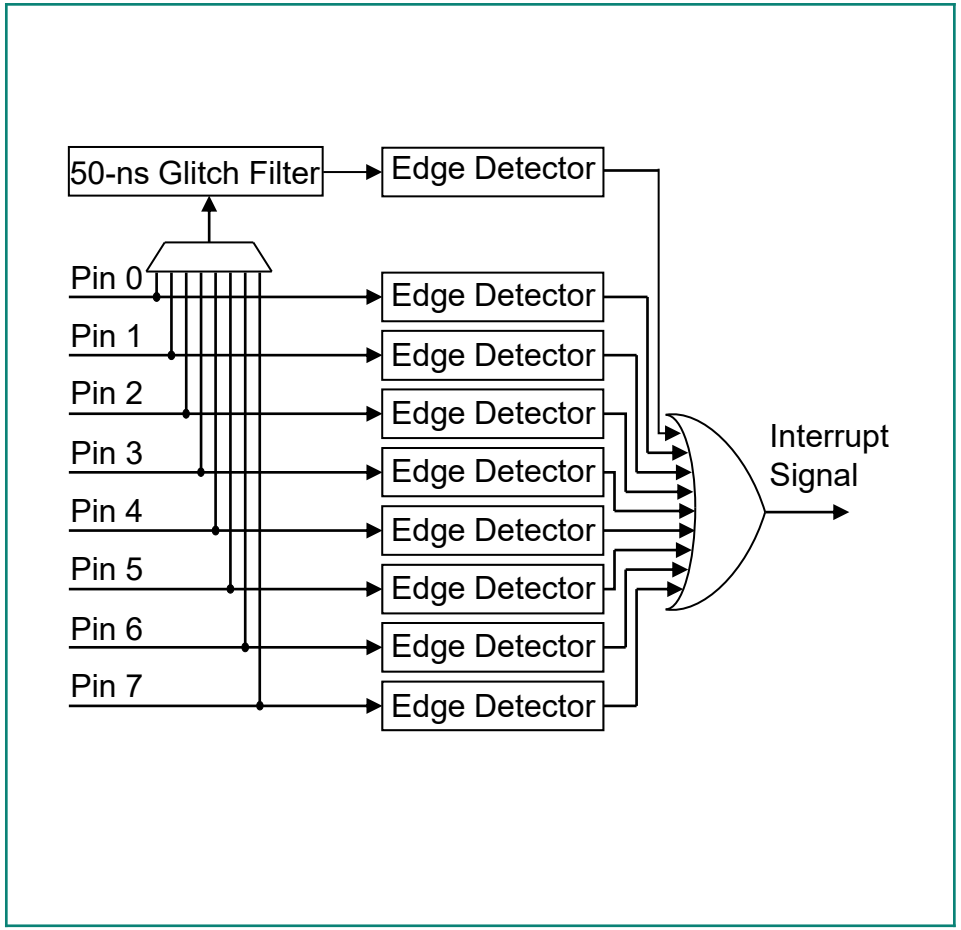
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GPIO interrupt

- All port pins can generate GPIO interrupts and status registers[1]
- A GPIO interrupt signal is generated by one per port
- Edge detector supports rising, falling, and both edges in all power modes[2]
- Glitch filter can be used by one pin per port[3]

- Use case
  - Wakeup interrupt from low-power mode (for example, CAN wakeup)
  - Detect the input signal state change (for example, switch)

Note: Not all ports have eight I/O pins.



Hint bar

See the architecture reference manual, Interrupt (section 23.3.4), for additional details.

[1] See the Register reference manual (GPIO_PRTx_INTR) for additional details.
[2] See the Register reference manual (GPIO_PRTx_INTR_CFG) for additional details.
[3] If a longer pulse suppression width is necessary, use Smart I/Os.

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GPIO behavior in each state

State	Status
Reset	– All GPIOs are in high-impedance analog state, and the input buffers are disabled
Sleep	– GPIO pins are active – Input buffers are active – Can be driven by most peripherals, such as TCPWM and SCB – Any GPIO can be used to wake the device
Deep Sleep	– GPIO pins connected to the DeepSleep domain peripheral are functional – All other pins are hold/frozen and will maintain the last output driver state and I/O configuration – GPIO interrupts are functional on all I/Os and can be used to wake the device
Hibernate	– Only select I/Os can be used to wake the device[1] – All other pins are on hold/frozen and will maintain the last output driver state and I/O configuration

Advantages

- Reduces power consumption while keeping the last I/O driver state
- Any I/O can be used as wakeup interrupt except in Hibernate mode

Hint bar

See the architecture reference manual, Behavior in low power mode (section 23.2.4), for additional details.

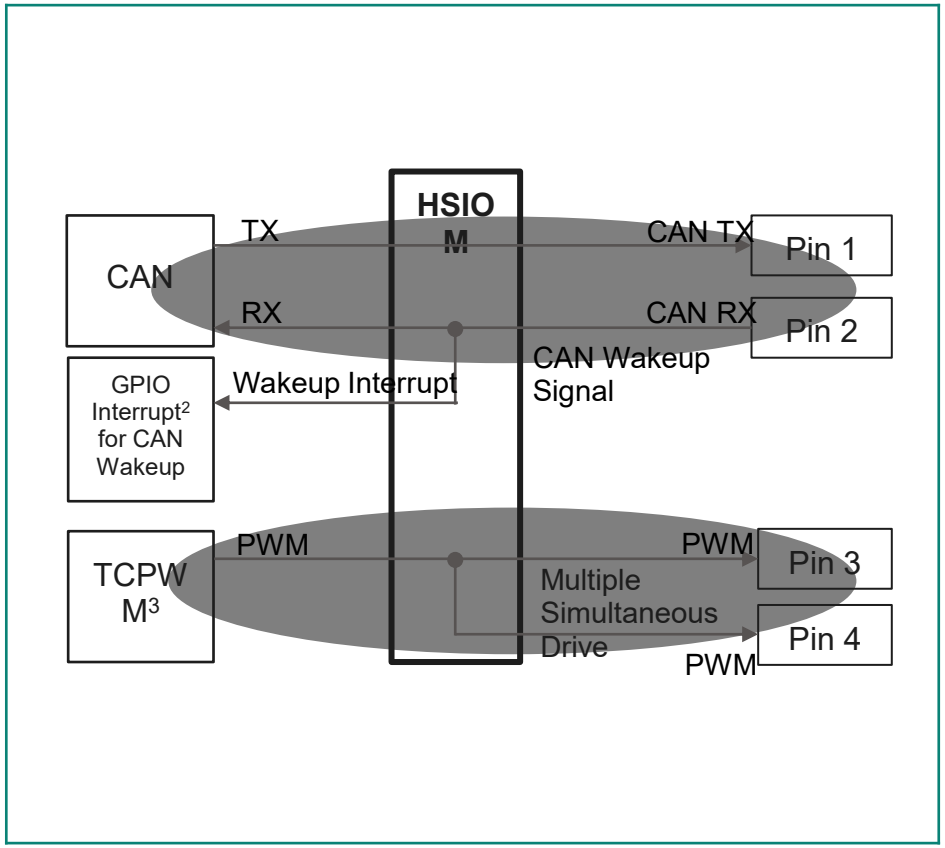
[1] PSOC Control C3 supports up to two GPIO pin interrupts for wake up (P2.0 and P9.0)

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High-speed I/O matrix (HSIOM)

- Routing internal peripheral signals to and from GPIOs
- GPIOs can be shared with multiple functions
- Multiplexes the pin connection to a user-selected peripheral[1]
- GPIO interrupt has no dependency on HSIOM configuration[2]

- Use case
  - CAN Wakeup[2]
  - Multiple simultaneous drive by PWM output[3]



Hint bar

See the architecture reference manual, HSIO to map alternate functions on GPIO (section 23.2.2), for additional details.

[1] See the Register reference manual (HSIOM_PRTx_PORT_SELx) for additional details.
[2] Do not change the HSIOM configuration before going to low power mode.
[3] It depends on the pin assignment. For details on pin assignment, refer to the device datasheet.

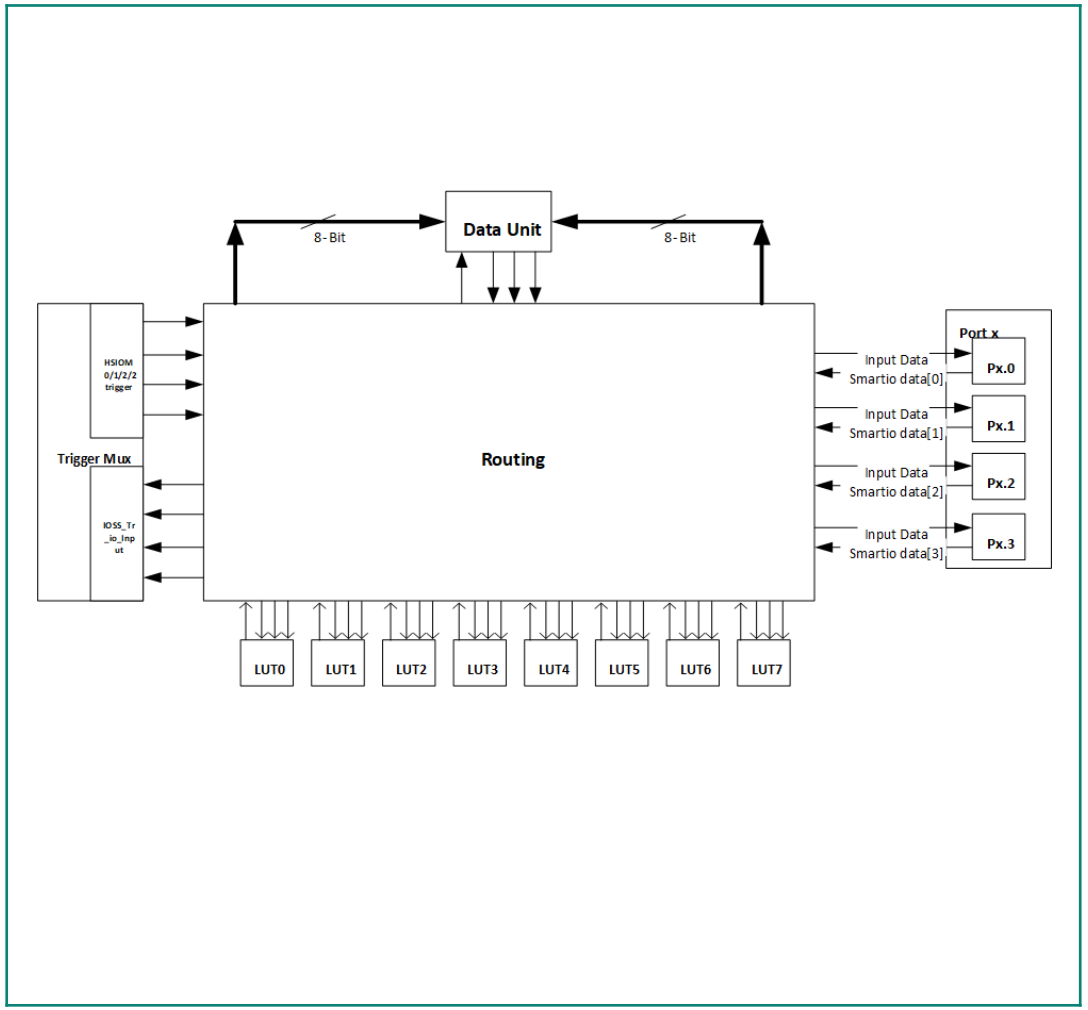
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Smart I/O

Overview

Smart I/O blocks on PSOC™ C3 devices add programmable logic to the GPIO ports. Each Smart I/O instance provides:

- Eight 3-Input Look-Up-Tables (LUT) describing the logical operations to be performed on these inputs. 4 LUTs are connected to respective ports, and the remaining four LUTs are floating to be used for the logical combination of internally routed signals
- Single data unit (DU) consisting of a simple 8-bit data path. It is capable of performing simple increment, decrement, shift, and AND/OR operations
- Flexible connectivity of inputs and outputs from/to trigger multiplexer



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Smart I/O (contd.)

Key features

- LUT-based, combinatorial and programmable logic for combining internal and external signals, with options for cascading and synchronisation
- Single data unit with 8-bit data path per Smart I/O instance

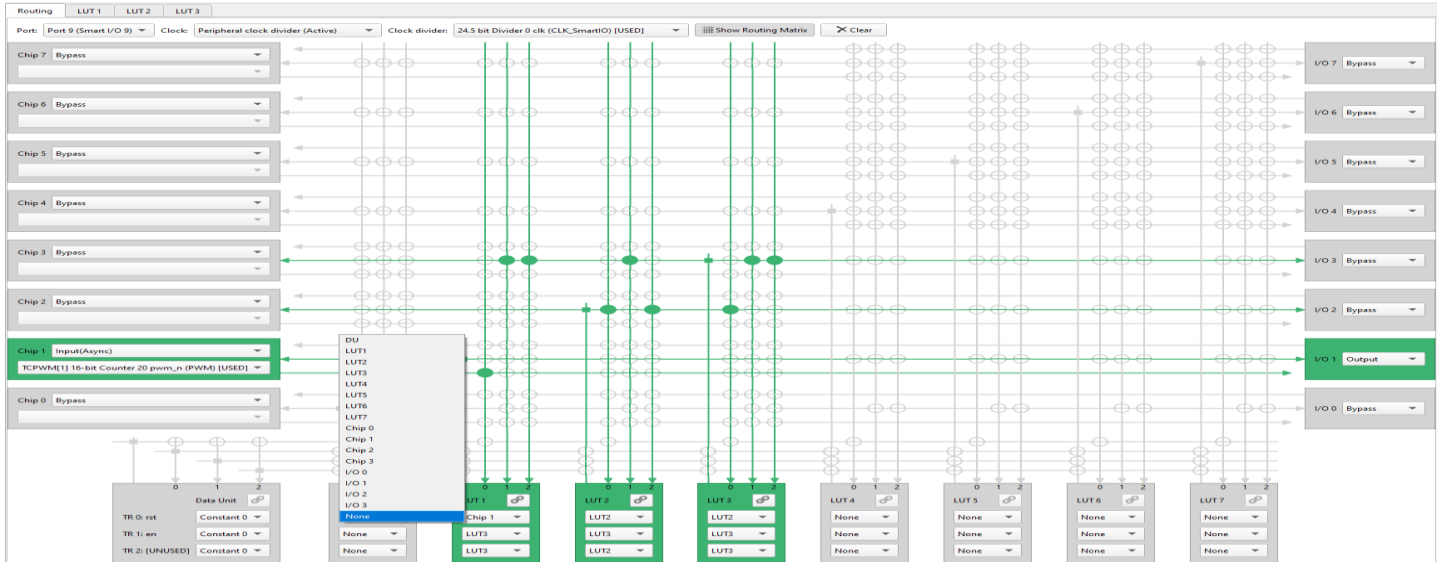
User benefits

- Logical combinations of signals and events for internal or external use
- Signal processing on external inputs or internal signals

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Smart I/O features

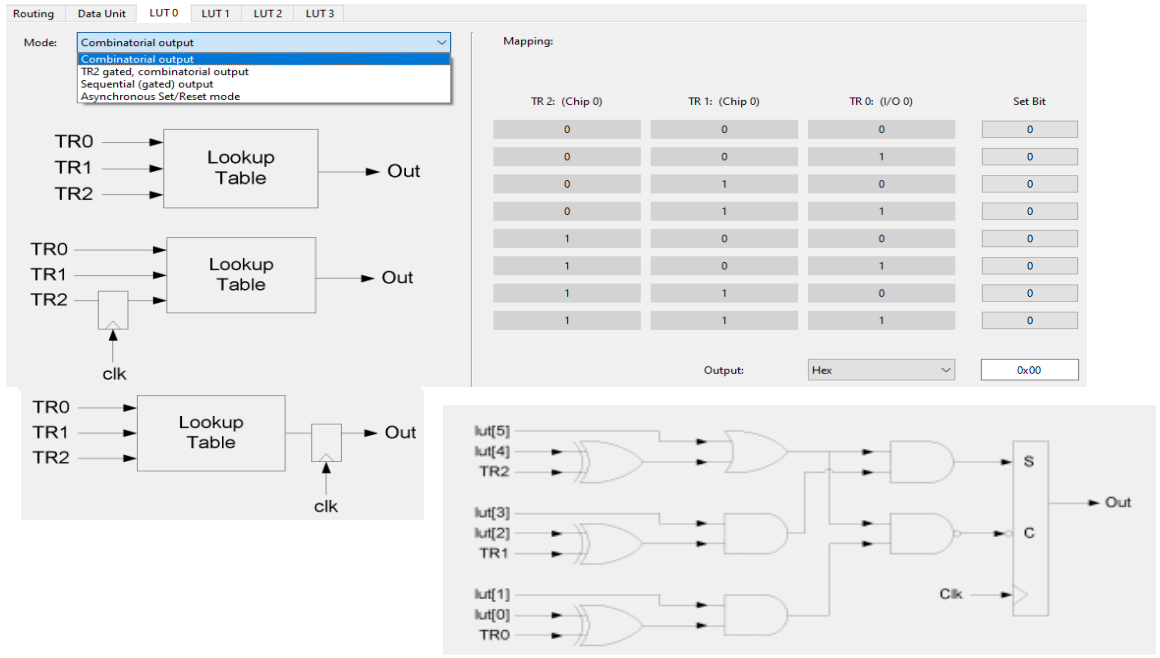
Configure the programmable logic between an I/O port positioned and fixed function peripherals/ CPU and so on.



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Smart I/O features (contd.)

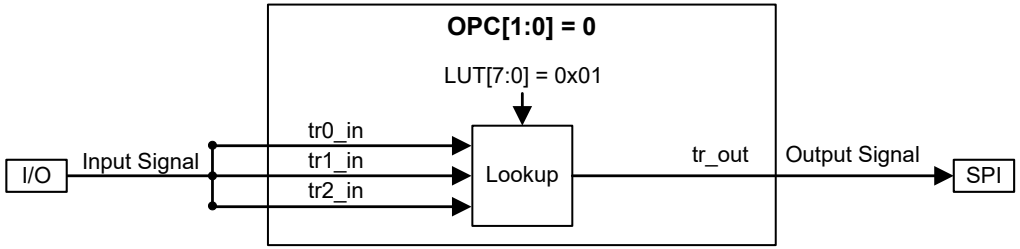
- Combinatorial Boolean logic set by a truth table
- Rising/Falling Edge and level detection
- Data Unit with ALU operations
- Combinatorial mode, Clock gating on in- or output signals, and Asynchronous Set/Reset



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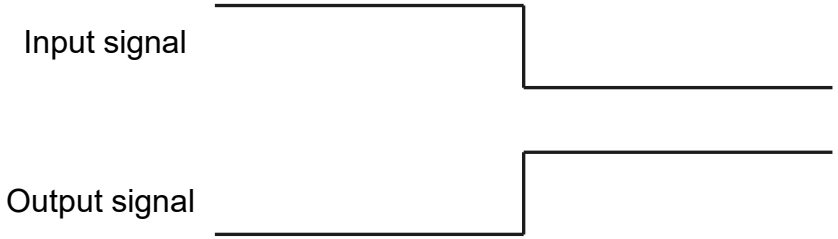
Use case 1: Invert SPI signal polarity

– Use as an inverter by setting only OPC[1:0] = 0, LUT[7:0] = 0x01



LUT[7:0] = 0x01

tr2_in	tr1_in	tr0_in	tr_out
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0



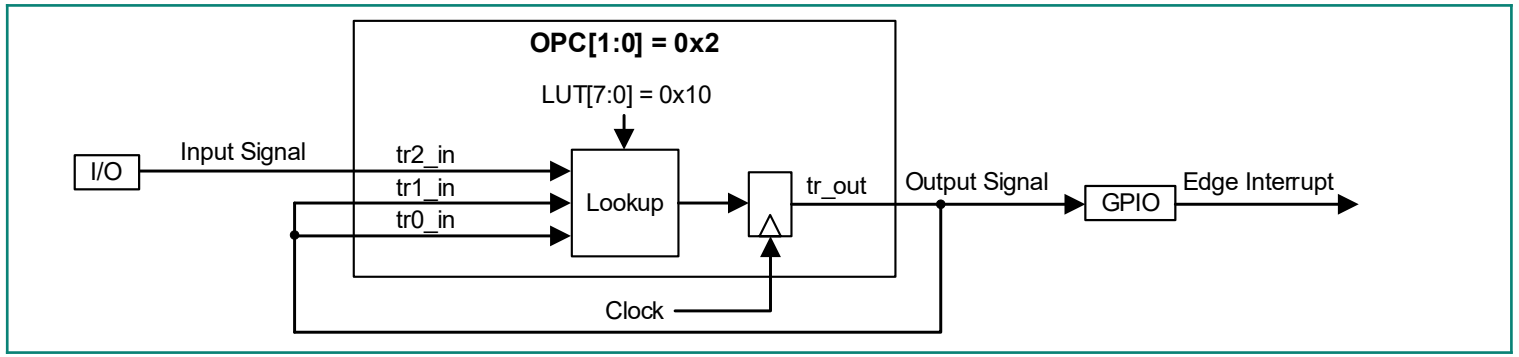
Hint bar

See the architecture reference manual, Block components (section 23.4.2), for additional details.

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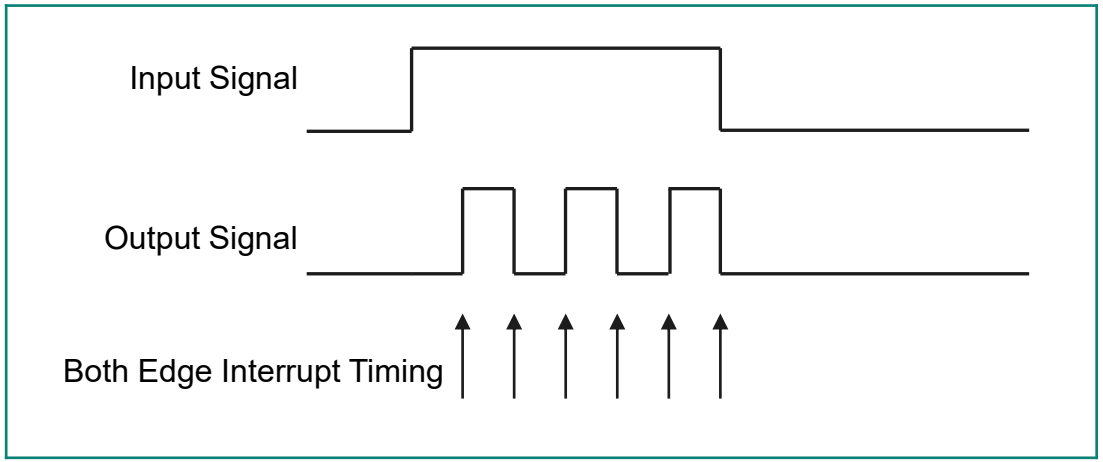
Use case 2: High-level detection interrupt

– Use as a high-level detection interrupt by using a GPIO edge interrupt and setting LUT to OPC[1:0] = 0x2, LUT[7:0] = 0x10



LUT[7:0] = 0x10

tr2_in	tr1_in	tr0_in	tr_out
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0



Hint bar

See the architecture reference manual, Block components (section 23.4.2), for additional details.

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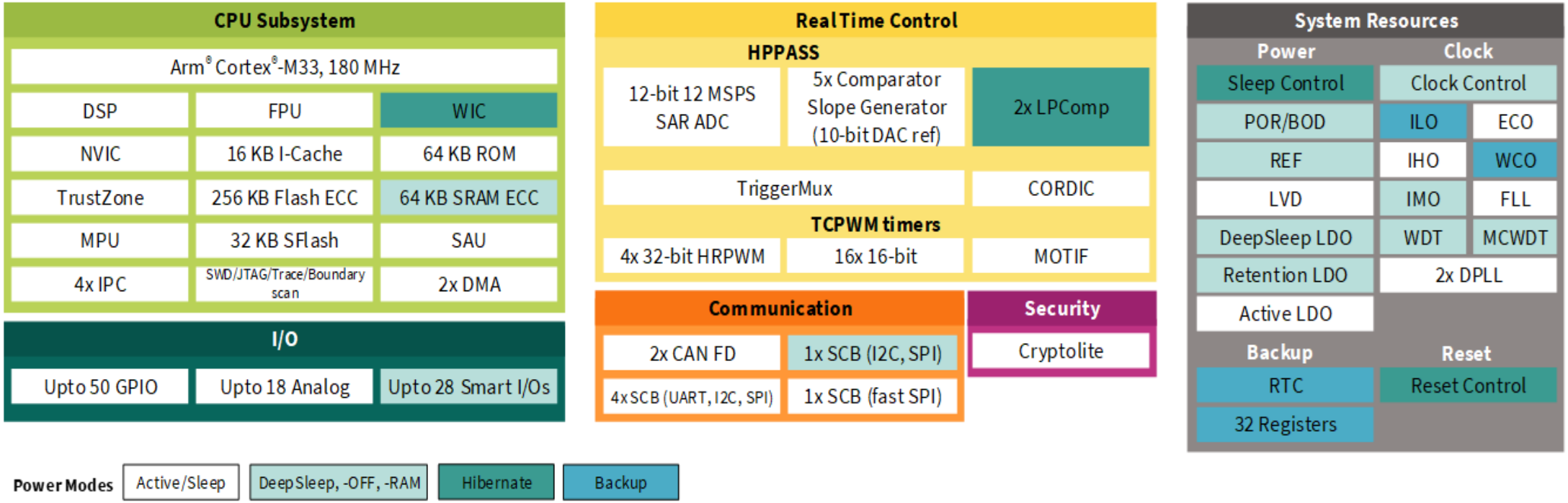
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Serial communication block (SCB)

Serial communication block (SCB)



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Serial communication block (SCB) (contd.)

Features

- Supported serial communication protocols are I2C,SPI, UART
- Supports slave operation in Deep Sleep for SPI and I2C interfaces
- One SCB has fast SPI support of up to 50 MHz
- Supports single wire half-duplex mode for UART
- Six independent run-time-reconfigurable SCBs; each is software configurable as master or slave for I2C,SPI, or UART in Active power mode

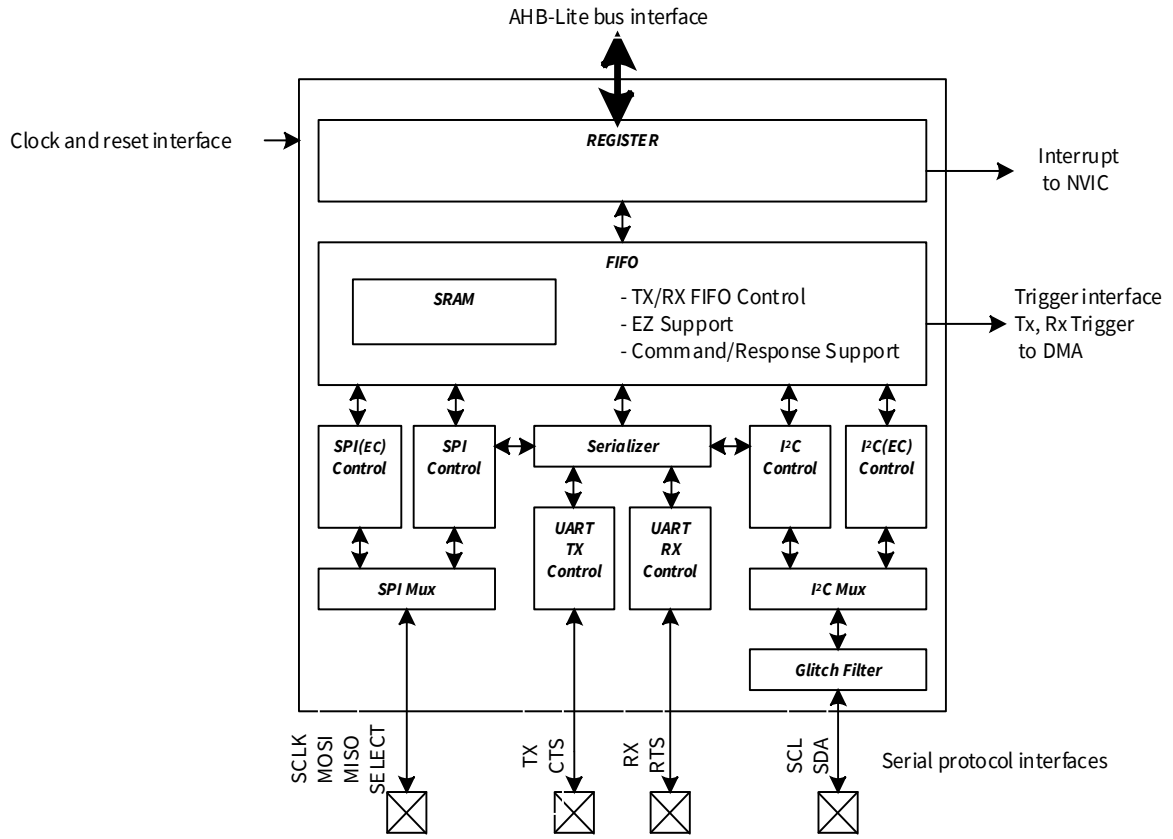
Benefits

- Allows users to select various supported flavours of SPI, I2C, and UART
- Allows users to configure frame size, adjust FIFO size, baud rates, and so on
- Enables communication with standard external devices supporting single-wire protocol
- SPI/I2C slave communication possible in the Deep Sleep power saving mode
- All SCB blocks support DMA transfers

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Serial communication block diagram

Block diagram



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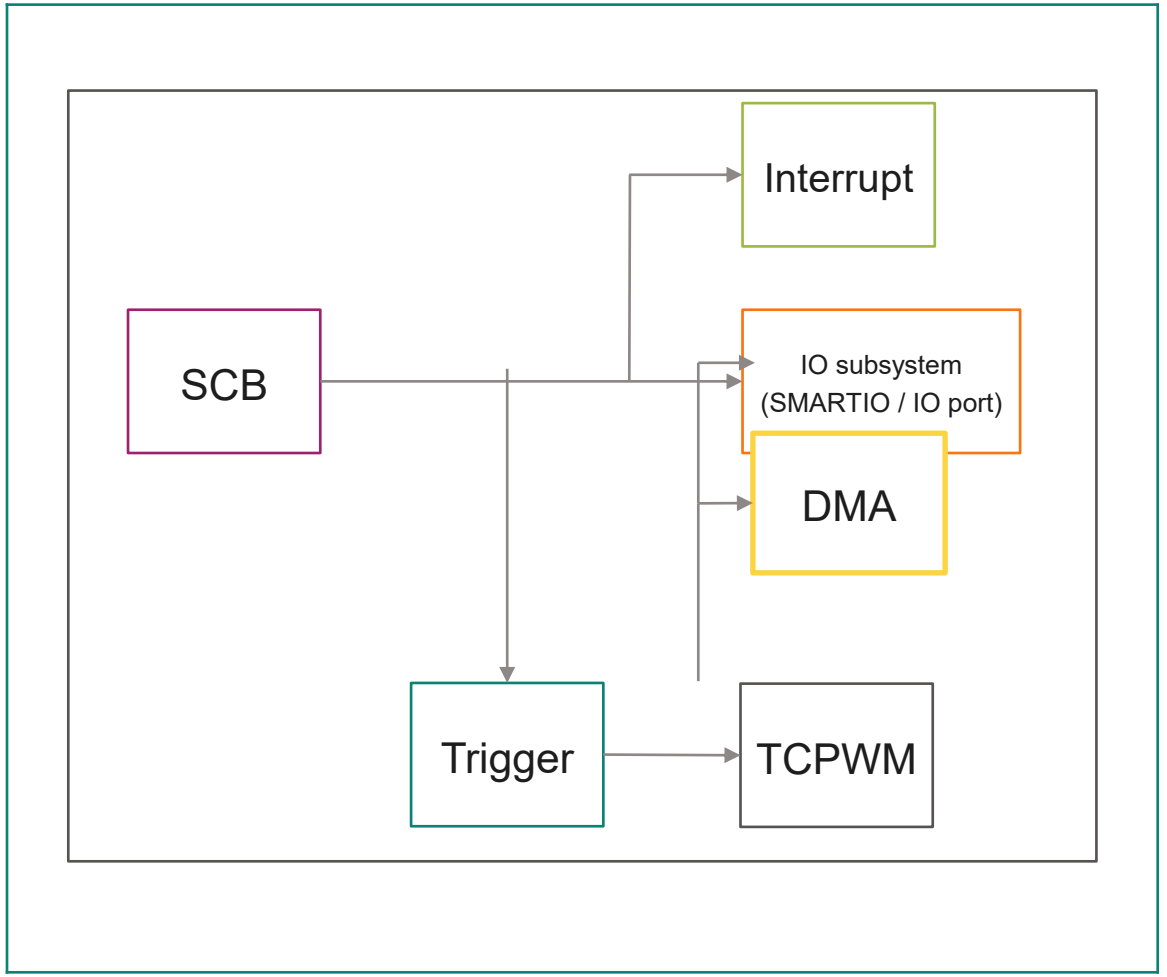
See the architecture reference manual, Serial communication block (section 26), for additional details.

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System integration

SCB is interconnected with several modules in the MCU system

- Interrupt – To generate an interrupt
- IO subsystem – Signal connection to the input and output pins, using SMARTI/O to redirect the SCB pin to other peripherals or loopback
- Trigger Mux – If SCB does not have a direct connection to a peripheral, the signal can be mapped to the Trigger Mux module and connected to SCB. Use Tigger Mux to start/stop/reset the peripherals
- TCPWM – Input signal to TCPWM module through trigger mux
- DMA – To transfer data without CPU intervention



Target applications

- Connectivity/communication

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Serial communication block overview (1/3)

- Supports three serial interface protocols
  - Serial peripheral interface (SPI)
  - Universal asynchronous receiver/transmitter (UART)
  - Inter-integrated circuit (I2C)

- SPI features
  - Supports master and slave functionality
  - Supports three SPI protocols (Motorola, Texas Instruments, National Semiconductor)
  - Supports up to four slave select lines
  - Programmable data frame size from 4 bits to 32 bits
  - Supports FIFO mode, EZSPI mode and CMD_RESP mode (slave only) of operation
  - Wake-up interrupt cause activated on slave selection (SCB[0] only)
  - SPI Master/slave support till 25 MHz, Fast SPI support on one SCB till 50 MHz
  - Programmable oversampling and local loopback control

Hint bar

See the architecture reference manual, Features (section 26.3.1), for additional details.

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Serial communication block overview (2/3)

- UART features
- Supports protocols
  - Standard UART
  - Multi-processor mode
  - Half duplex mode
  - SmartCard interface (ISO7816), IrDA protocol, and local interconnect network (LIN) submodes
- Programmable data frame size from 4 to 16 bits
- Programmable number of STOP bits (can set half-bit periods between 1 and 4)
- Programmable oversampling
- Hardware flow control

Hint bar

See the architecture reference manual, Features (section 26.4.1), for additional details.

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Serial communication block overview (3/3)

- I2C features
  - Master and slave mode
  - Three types of data-rate modes
  - Standard mode (100 KHz), Fast mode (400 kHz), Fast mode Plus (1 MHz)
  - 7-bit slave addressing
  - 10-bit addressing supported through software
  - Multi-master modes and bus arbitration
  - Clock stretching and Collision detection
  - Analog and digital glitch filter – up to 50 ns

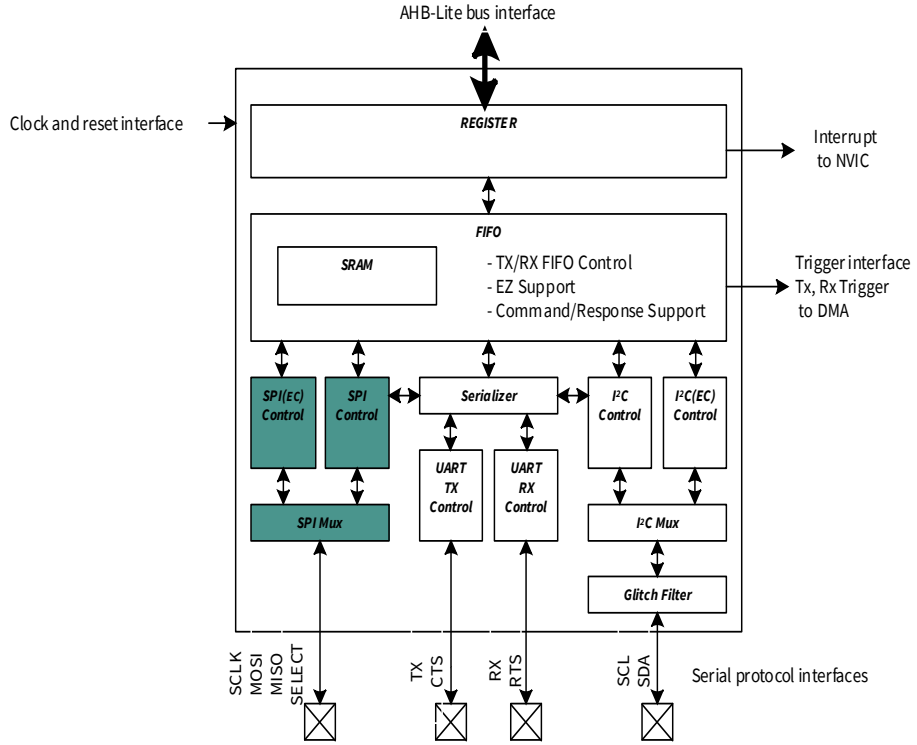
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See the architecture reference manual, Features (section 26.5.1), for additional details.

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SPI serial communication block components

- Supports up to four slave select lines
- Supports three SPI protocols
- SPI buffer mode
  - FIFO mode
  - EZSPI mode
  - Command-Response mode



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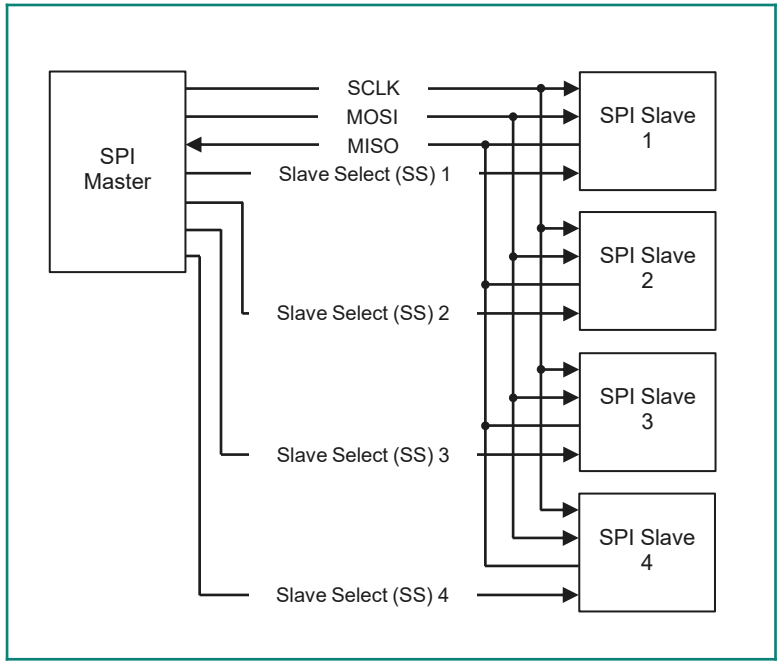
See the architecture reference manual, Serial peripheral interface (SPI) (section 26.3), for additional details.

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SPI slave select lines

- The standard SPI interface consists of four signals
  - SCLK: Serial clock (clock output from the master, input to the slave)
  - MOSI: Master-out-slave-in (data output from the master, input to the slave)
  - MISO: Master-in-slave-out (data input to the master, output from the slave)
  - Slave Select (SS): Typically, an active-low signal (output from the master, input to the slave)

- **Advantage**
  - Can communicate with multiple external ICs using the same bus



Hint bar

See the architecture reference manual, General description (section 26.3.2) for additional details.

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SPI protocols

Three SPI protocols[1]

- The Motorola SPI[2] protocol has four clock modes
  - Data is driven and captured by clock polarity and clock phase
- Texas Instruments SPI[2]
  - The Texas Instruments SPI protocol redefines the use of the SS signal to indicate the start of a data transfer
- National Semiconductor SPI[3]
  - The National Semiconductor SPI protocol alternates transmission and reception

Hint bar

See the architecture reference manual, Features (section 26.3.1), for additional details.

[1] See the register reference manual (SCBx_SPI_CTRL) for additional details.
[2] Full duplex.
[3] Half duplex.

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SPI interrupt

– Interrupt events in SPI ode

Event type	Event
TX	SPI master transfer done
RX	SPI Bus Error
TX	TX FIFO is not full
TX	TX FIFO is empty
TX	TX FIFO overflows
TX	TX FIFO underflows
TX	SPI slave deselected after a write EZSPI transfer occurred
TX	SPI slave deselected after any EZSPI transfer occurred
RX	RX FIFO is full
RX	RX FIFO is not empty
RX	RX FIFO overflows
RX	RX FIFO underflows

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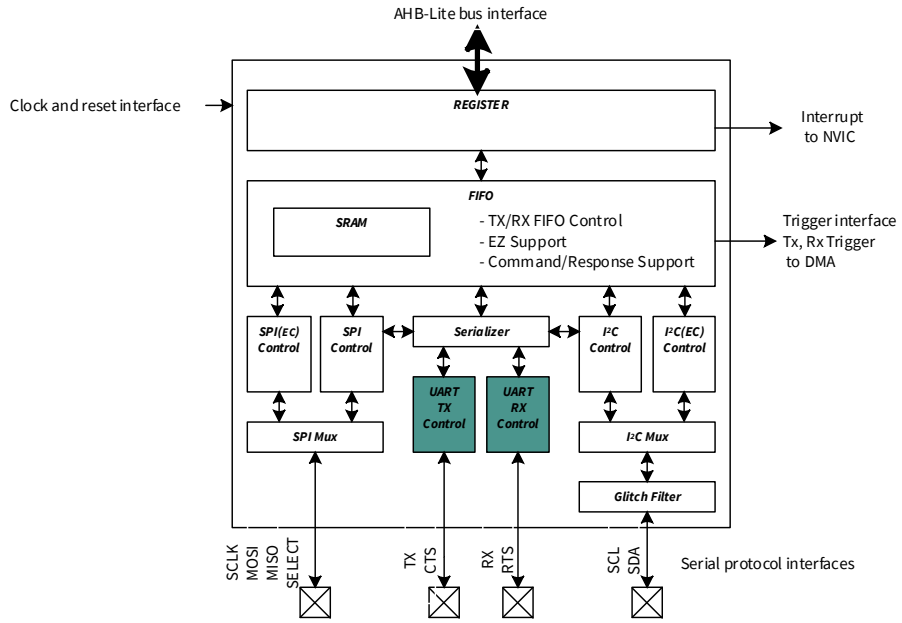
See the architecture reference manual, SPI interrupt (section 26.6.1), for additional details.

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UART serial communications block

The UART in the SCB block supports the following:

- Standard UART
- Half duplex
- Multi-processor mode
- Start skipping function
- Oversampling
- Break detection



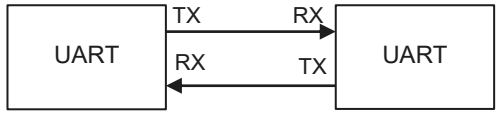
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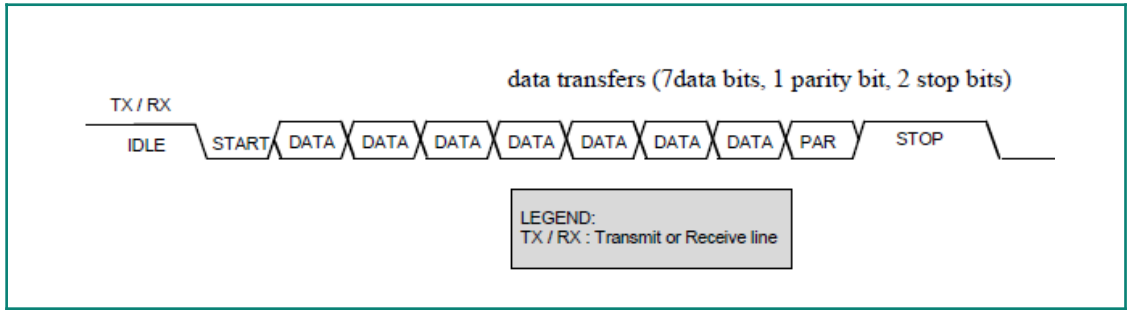
See the architecture reference manual, UART (section 26.4), for additional details.

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UART standard UART

- Standard UART
  - TX and RX connection
  - Buffer mode only uses FIFO mode
  - Typical UART transfer frame components
  - Start bit
  - Data bits (programmable from 4 to16 bits)
  - Parity bit (optional)
  - Stop bit (can be set to half-bit periods between 1 and 4)





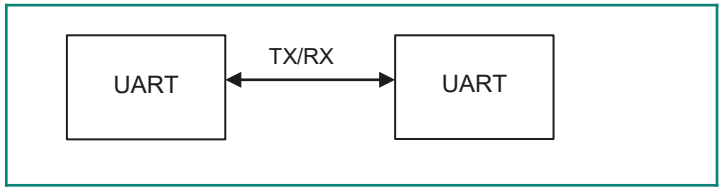
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See the architecture reference manual, Standard protocol (section 26.4.3.1), for additional details.

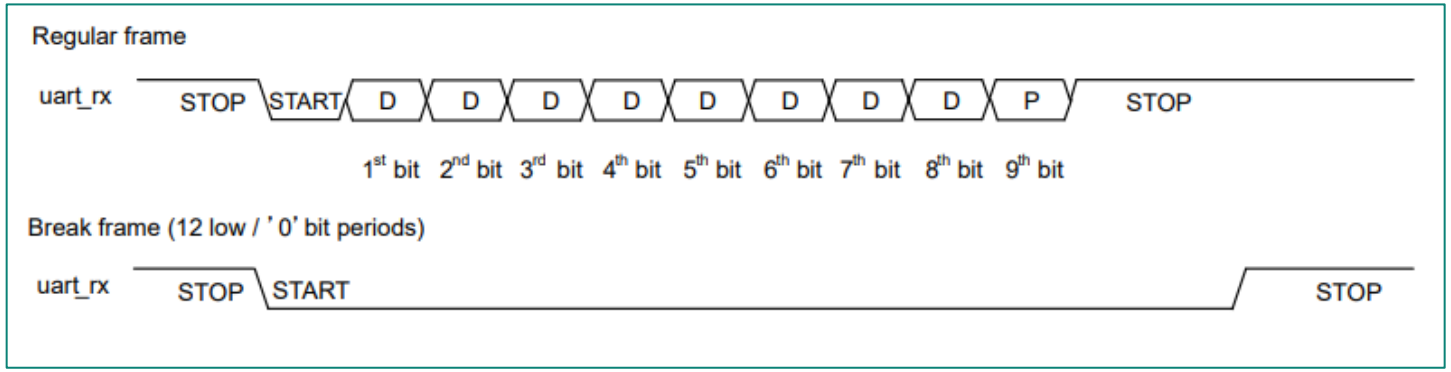
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UART half duplex mode and break detection

- UART half-duplex
  - From the protocol point of view, all features of standard UART sub-mode are supported except the parallel transmission and reception, which is caused by the single transmission line



- Break detection
  - Break detection detects when UART_RX is LOW ’0’ for more than BREAK_WIDTH bit periods.
  - A break is used by the transmitter to signal a special condition to the receiver.
  - This condition may result in a reset, shut down, or initialisation sequence at the receive



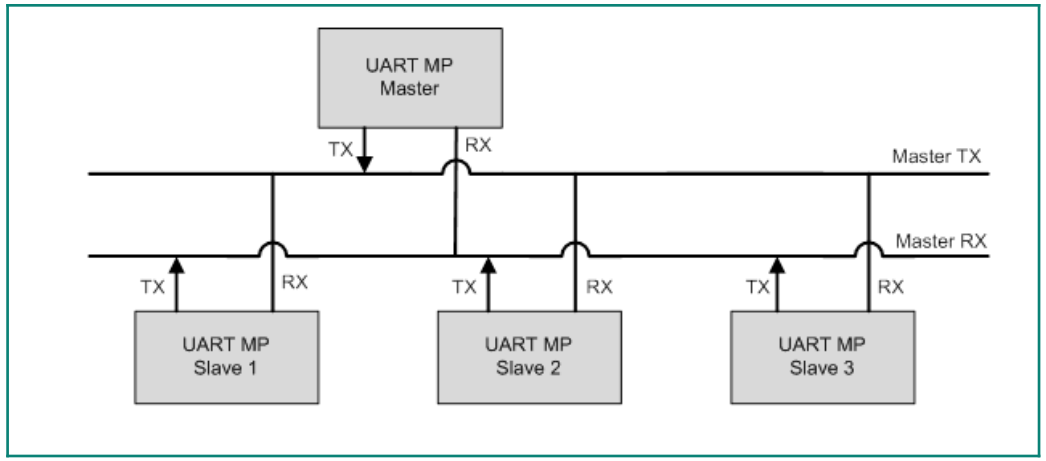
Hint bar

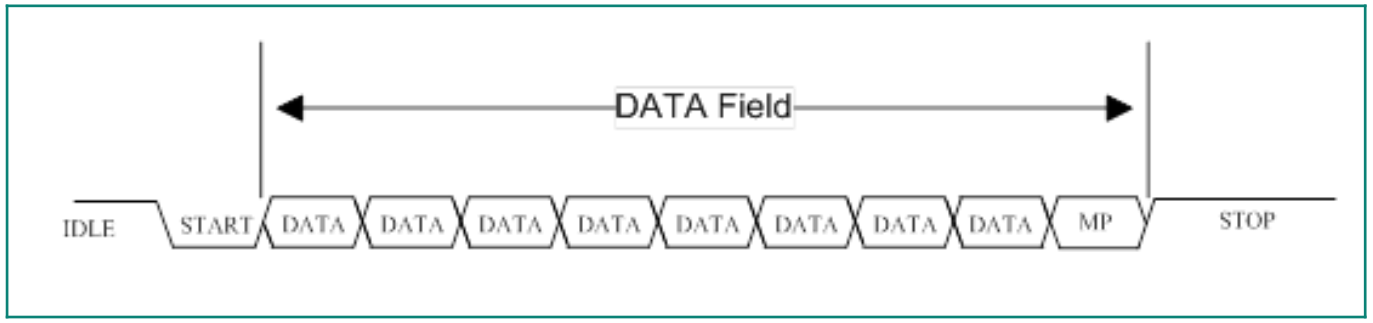
See the architecture reference manual, Half duplex mode (section 26.4.3.1.3), for additional details.

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UART multi-processor mode

- UART_MP (multi-processor) mode
- Single-master-multi-slave connection
- UART_MP mode properties
- Each slave is identified by a unique address
- Uses a 9-bit data field
  - Ninth bit as address/data flag (MP bit)
- Parity bit is disabled





- **Advantage**
  - Can communicate with multiple external ICs using the same bus

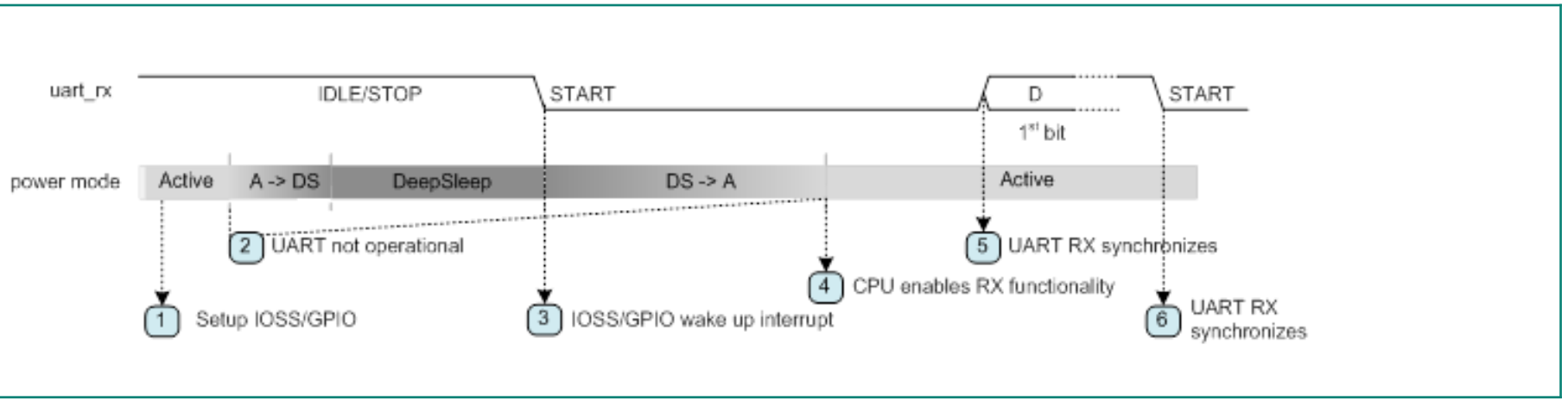
Hint bar

See the architecture reference manual, Multi-processor mode (section 26.4.3.1.6), for additional details.

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UART start skipping function

– Use Start Skipping to wake up from Deep Sleep mode
  1. The GPIO is set as an interrupt to the UART RX line transition ‘1’ to ‘0’ (START bit).
  2. The UART receiver is not functional during Deep Sleep mode transition.
  3. When the GPIO interrupt is activated, the system transitions from Deep Sleep to Active mode.
  4. The CPU enables UART receive functionality.
  5. The UART receiver synchronises with the received data frame.
  6. The UART receiver proceeds with normal operation.



– **Advantage**
  – UART can receive data immediately upon MCU wakeup from Deep Sleep

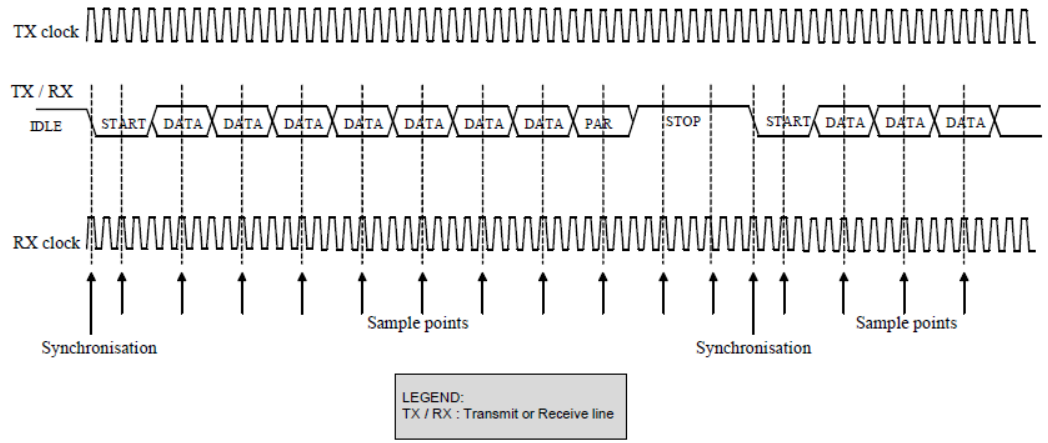
Hint bar

See the architecture reference manual, start skipping (section 26.4.3.1.2), for additional details.

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UART oversampling

- The receiver oversamples the incoming signal
- The sampling clock can select from 8 to 16 clock cycles by software
- The value of the sample point1 in the middle of the bit transfer period is used for transmitter and receiver clock synchronization



- **Advantage**
  - Can be used to synchronise the receiver with the transmitter clock

Hint bar

See the architecture reference manual, clocking and oversampling (section 26.4.4), for additional details.

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UART interrupt events in UART mode

Event type	Event
TX	TX done
RX	Frame error in received data frame
RX	Parity error in received data frame
RX	LIN baud rate detection is completed
RX	LIN break detection is successful
TX	TX FIFO is not full
TX	TX FIFO is empty
TX	TX FIFO overflows
TX	TX FIFO underflows
TX	TX received a NACK in SmartCard mode
TX	Arbitration lost
TX	TX trigger level
RX	RX trigger level
RX	RX FIFO is full
RX	RX FIFO is not empty
RX	RX FIFO overflows
RX	RX FIFO underflows

Hint bar

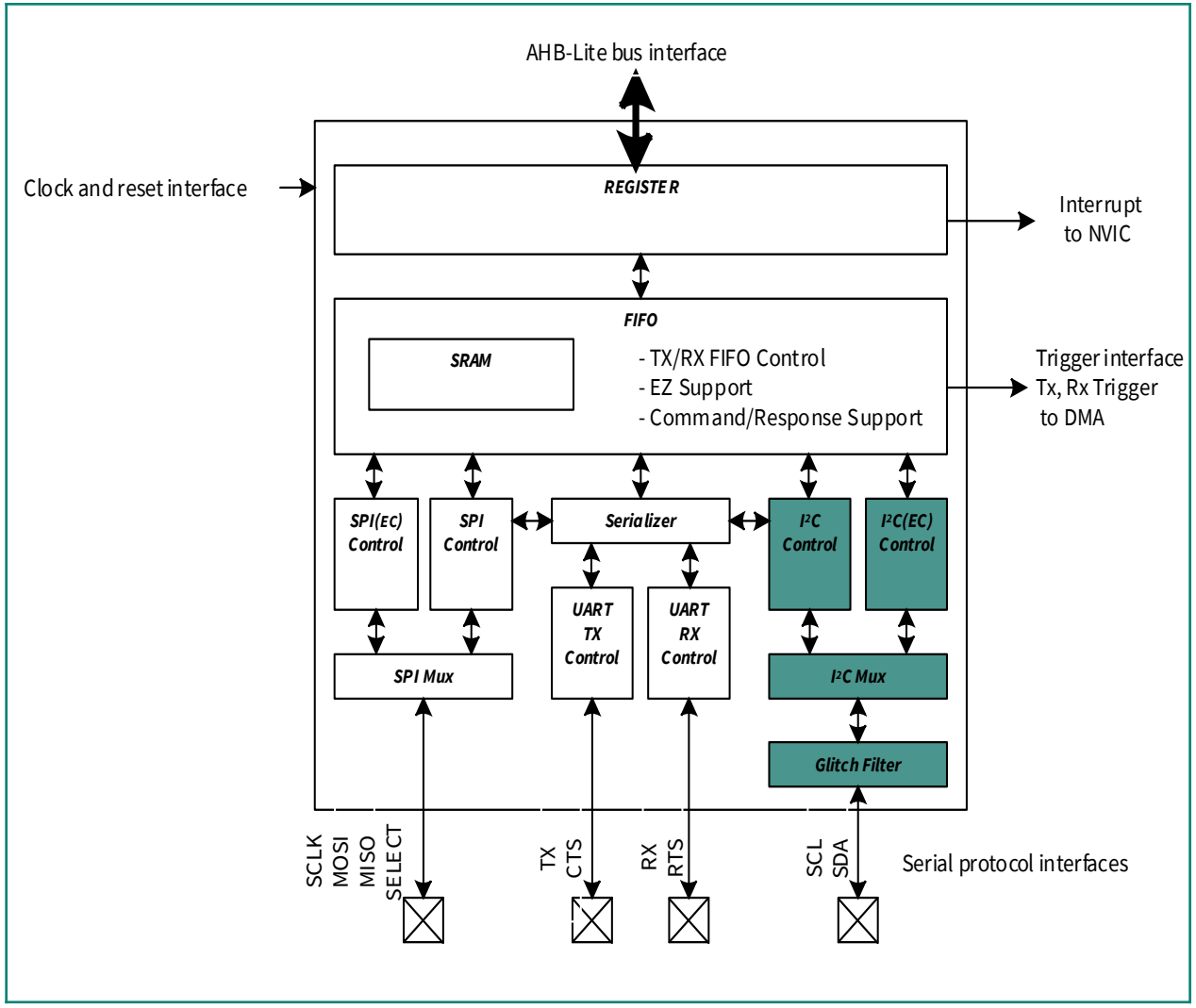
See the architecture reference manual, UART interrupts (section 26.6.2), for additional details.

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I2C serial communications block

I2C supports the following:

- Standard I2C
- I2C Buffer mode
  - FIFO mode1
  - EZI2C mode
  - Command-Response mode
- Glitch filtering



Hint bar

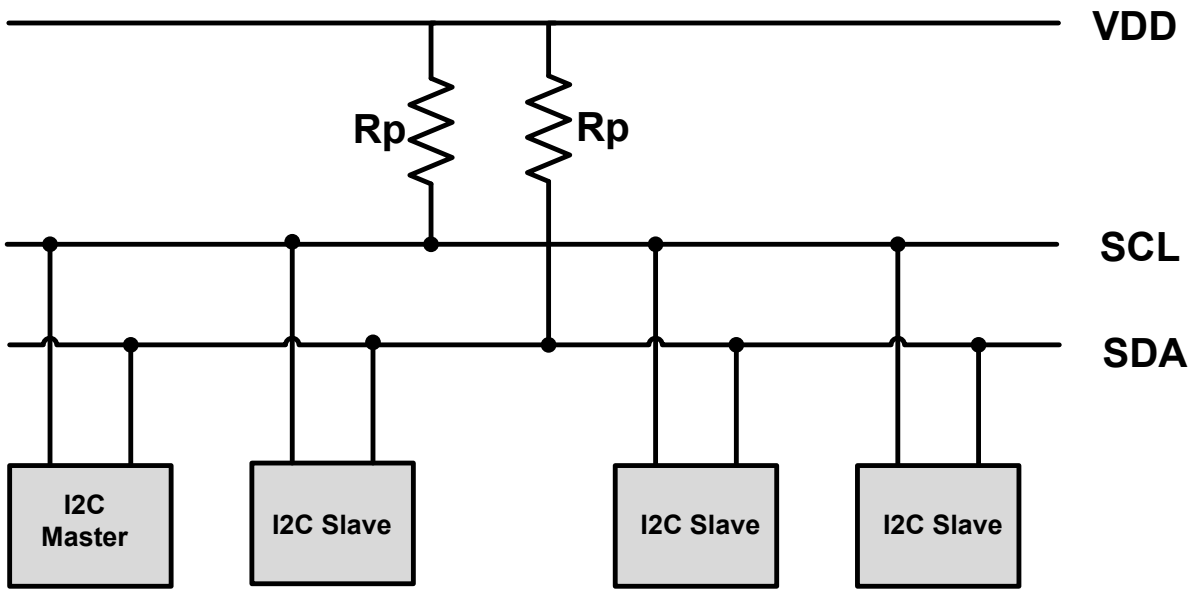
See the architecture reference manual, Inter-integrated circuit I2C (section 26.5), for additional details

[1] FIFO mode has the same features as SPI

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I2C standard

- The standard I2C bus is a two-wire interface with these lines
  - Serial data (SDA)
  - Serial clock (SCL)
- I2C devices are connected to these lines through pull-up
- Masters and slaves can operate as either transmitter or receiver



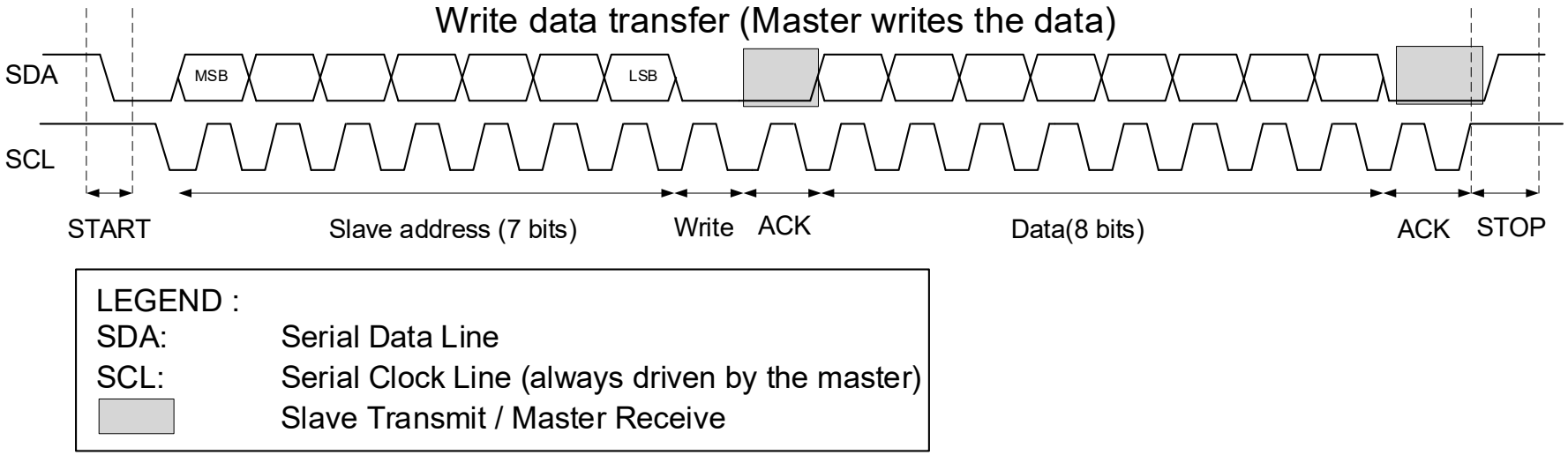
Hint bar

See the architecture reference manual, General description (section 26.5.2), for additional details.

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I2C write transfer

- The master sends data to the slave via a typical write transfer
- Generate START condition
- 7-bit I2C slave address and a write indicator ‘0’ bit
- The addressed slave transmits an acknowledgement
- If the master receives an acknowledgement, it transmits data (8 bits) to the bus
- When the transfer is complete, the master generates a STOP condition



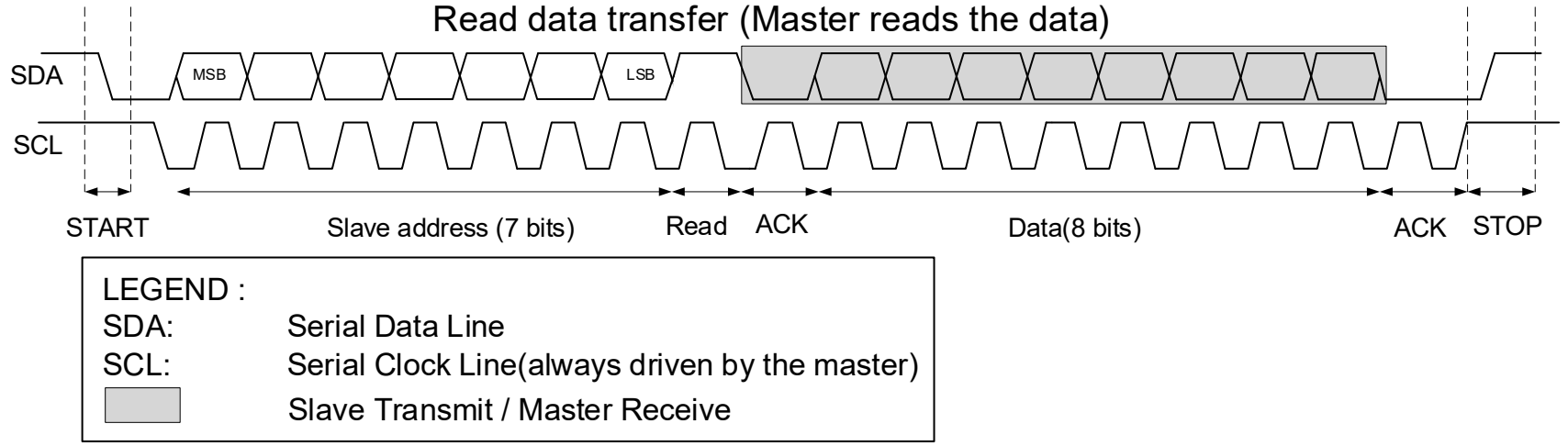
Hint bar

See the architecture reference manual, Write transfer (section 26.5.4.1), for additional details.

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I2C read transfer

- The master receives data from the slave via a typical read transfer
- Generate START condition
- 7-bit I2C slave address and a read indicator ‘1’ bit
- If the slave acknowledges the acknowledgement signal from the master, it starts transmitting data after the acknowledgement signal
- The master transmits an acknowledgement to confirm
- When the transfer is complete, the master generates a STOP condition



Hint bar

See the architecture reference manual, Read transfer (section 26.5.4.2), for additional details.

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I2C glitch filtering

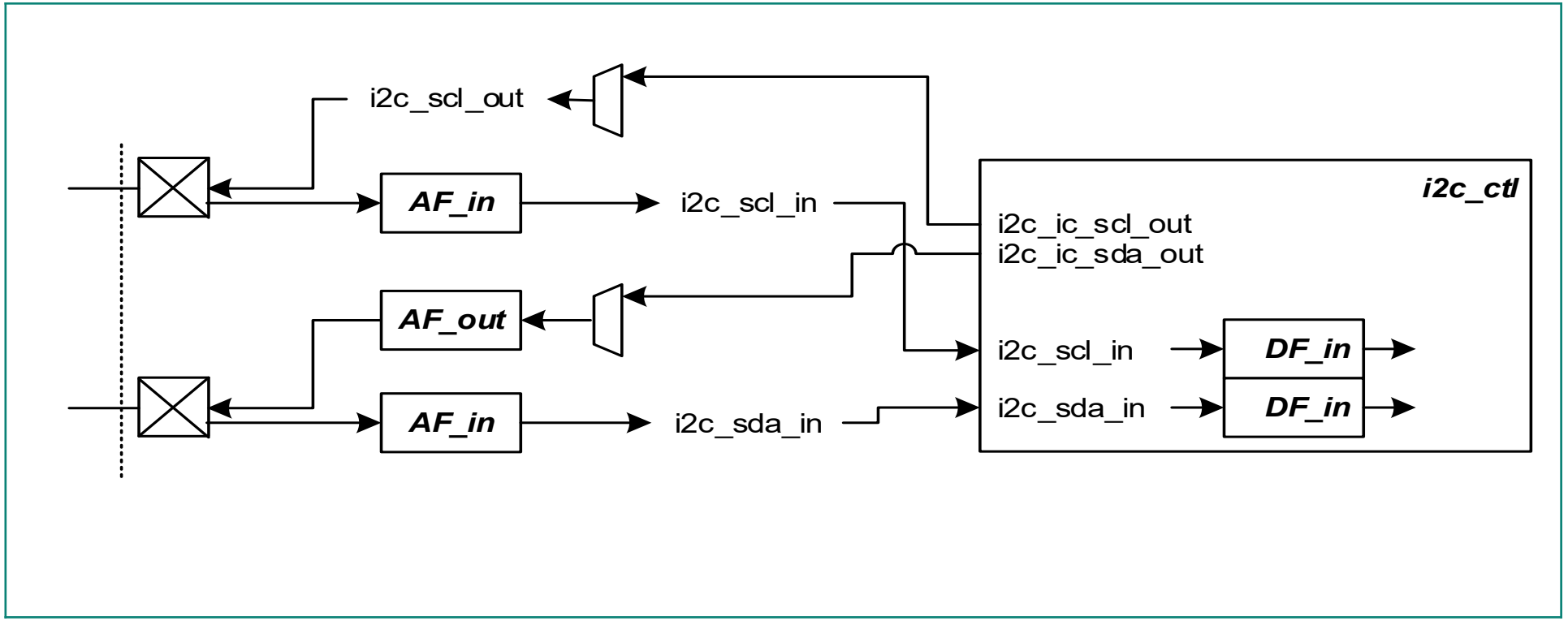
- The PSOC C3 SCB I2C has analog and digital glitch filters
- Analog glitch filters (AF_in, AF_out) are applied in the following:
  - i2c_scl_in
  - i2c_sda_in
  - i2c_sda_out
- Analog glitch filters are applied to filter glitches of up to 50 ns
- Digital glitch filters (DF_in) are applied in the following:
  - i2c_scl_in
  - i2c_sda_in
- Digital glitch filters are 3-tap median filters

Hint bar

See the architecture reference manual, Glitch filtering (section 26.5.6.1), for additional details.

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I2C glitch filtering (contd.)



Hint bar

See the architecture reference manual, Glitch filtering (section 26.5.6.1), for additional details.

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I2C interrupt

Interrupt events in I2C mode

Event type	Event
TX	I²C master lost arbitration
RX	I²C master received NACK
RX	I²C master received ACK
TX	I²C master sent STOP
RX	I²C master bus error (unexpected stop/start condition detected)
TX	I²C slave lost arbitration
RX	I²C slave received NACK
RX	I²C slave received ACK
RX	I²C slave received STOP
RX	I²C slave received START

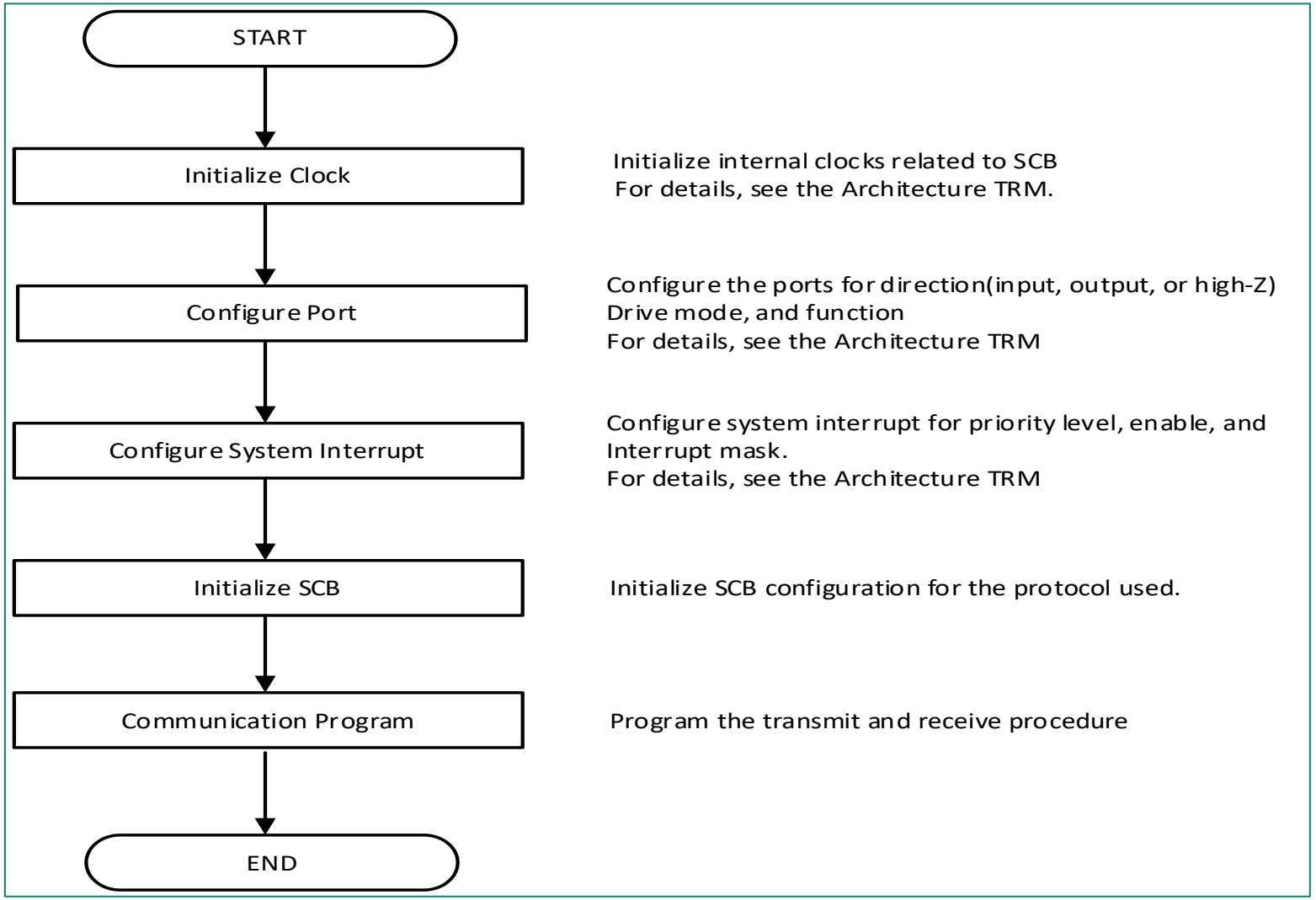
Event type	Event
RX	I²C slave address matched
RX	I²C slave bus error (unexpected stop/start condition detected)
TX	TX FIFO is not full
TX	TX FIFO is empty
TX	TX FIFO overflows
TX	TX FIFO underflows
RX	RX FIFO is full
RX	RX FIFO is not empty
RX	RX FIFO overflows
RX	RX FIFO underflows

Hint bar

See the architecture reference manual, I2C interrupts (section 26.6.3), for additional details.

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SCB common settings



Hint bar

See the reference manual, Serial communication block (section 26), for additional details.

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Lab activity

Lab 1: Hello world blinky

Lab 2: I2C master slave communication

Lab 3: UART transmit and receive

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4 **Revision history** **54**

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Revision history

Document revision	Date	Description of change
**	2026-02-06	Initial release

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