Customer training workshop
32-bit Arm® Cortex®-M7 microcontroller - XMC7000 Watchdog Timer

Target products

› Target product list for this training material:

Family category	Series	Code flash memory size
XMC7200	XMC7200-8M	Up to 8384 KB
XMC7100	XMC7100-4M	Up to 4160 KB

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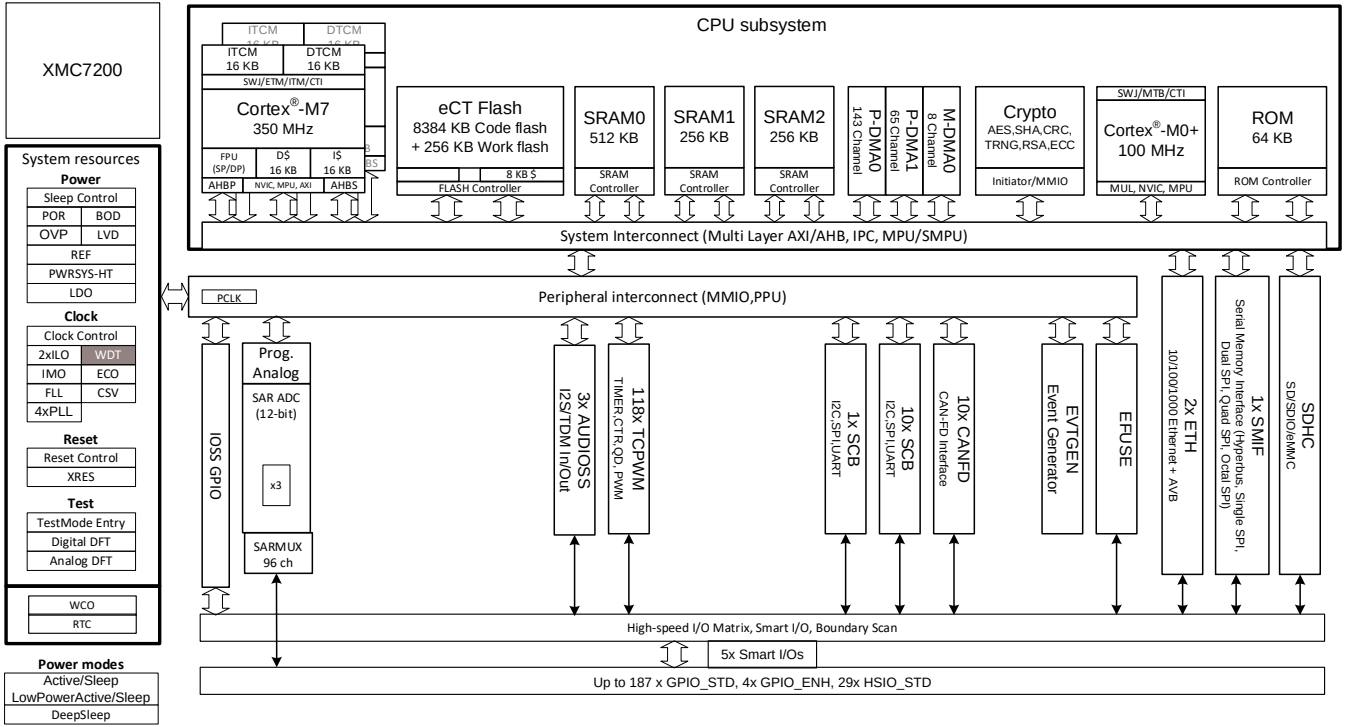
XMC7200 - 8M family

Introduction to XMC7200 – 8M

› Watchdog timer (WDT) is part of system resources



Hint Bar

Review TRM chapter 20 for additional details

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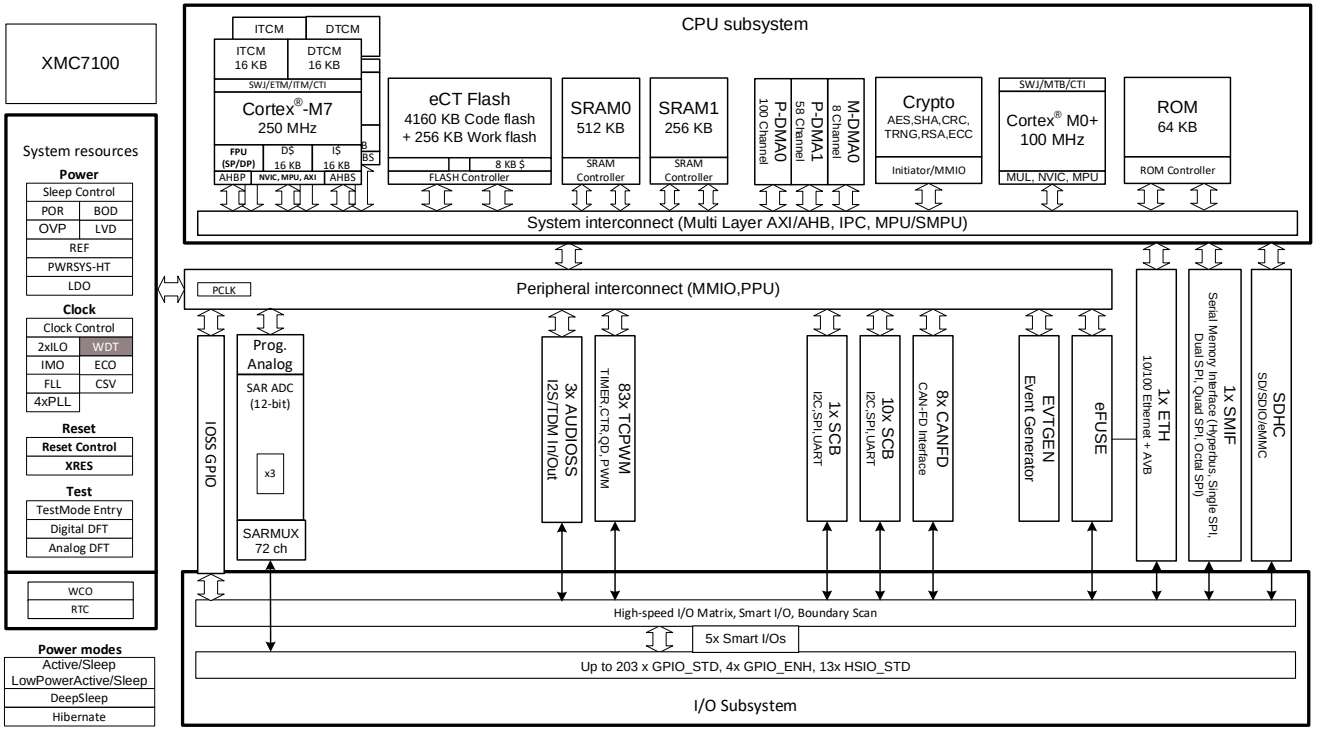
XMC7100 - 4M family

Introduction to XMC7100 – 4M

- Watchdog timer (WDT) is part of system resources



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Review TRM chapter 20 for additional details

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WDT overview

- A hardware timer that automatically resets the device in the event of an unexpected software execution path and provides warning interrupts and faults for multi-counter WDT (MCWDT)
- Two types of WDT
  - Basic WDT
  - MCWDT
- Features
  - Basic WDT: One 32-bit free-running counter
  - MCWDT: Two 16-bit counters and one 32-bit counter
  - Both WDT types support:
    - Window mode
    - Running and freezing timers during DeepSleep mode
    - Debug mode
    - Interrupt generation

Hint Bar

Review TRM section 20.1 for additional details

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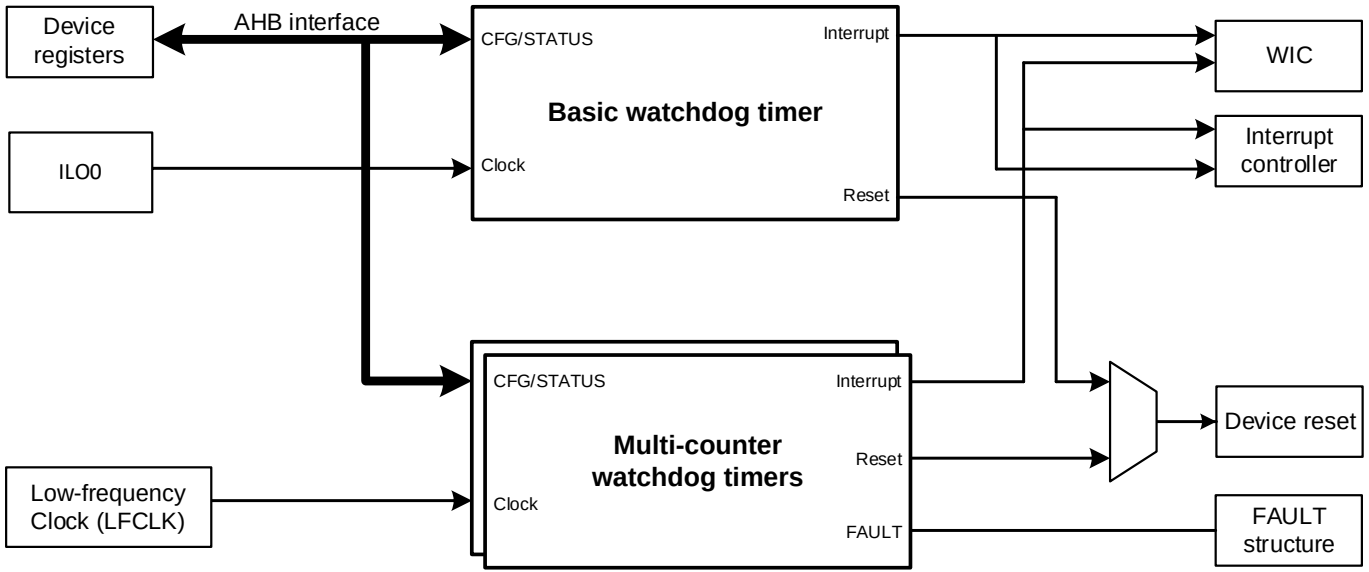
Watchdog timer block diagram



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Review TRM section 20.1 for additional details

Refer to the Clock System training section for additional Clock details

Refer to the Interrupts training section for additional WIC details

Refer to the Fault Structures training section for additional Fault Structure details

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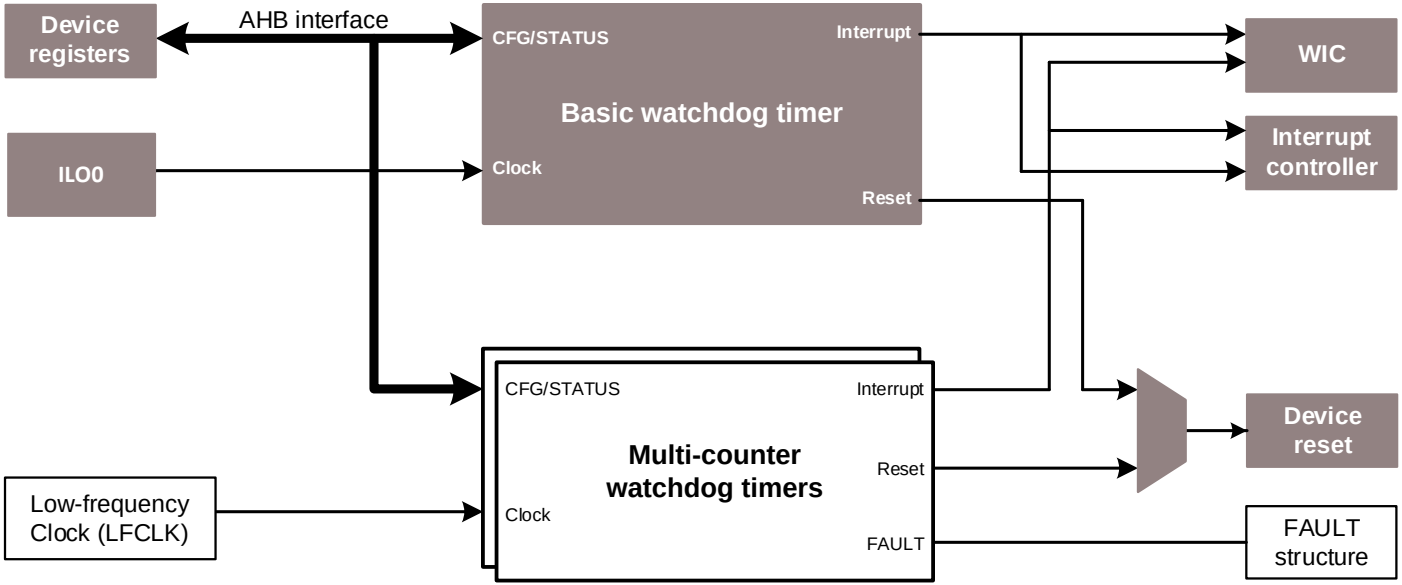
Basic watchdog timer block diagram



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Review TRM section 20.3 for additional details

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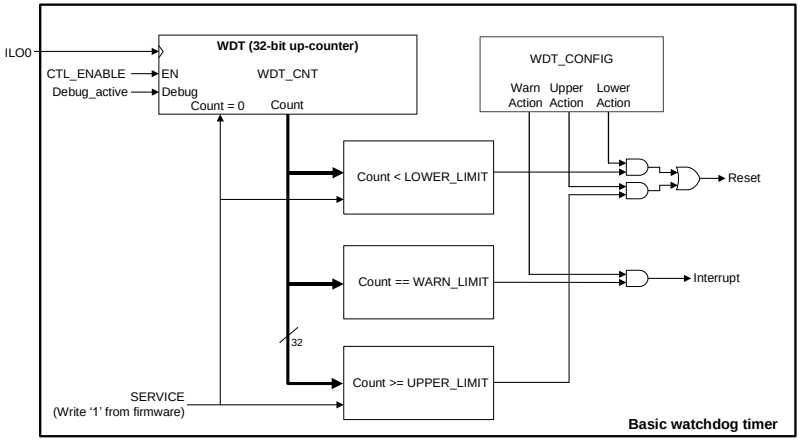
Basic WDT overview

- Features
  - 32-bit free-running counter supporting Window mode
  - Device reset and interrupt
  - Input clock source: ILO0
  - Enabled after power-on
  - Programmable LOWER_LIMIT, WARN_LIMIT, and UPPER_LIMIT
  - Registers that are protected and require an unlock sequence
  - WARN_LIMIT that generates an interrupt to request servicing
  - Device reset that occurs when UPPER_LIMIT is reached in the Window mode or when the counter is cleared before LOWER_LIMIT
  - Four power modes
    - Active
    - Sleep
    - DeepSleep
    - Hibernate[1]



[1] In Hibernate mode, any interrupt to wake up the device results in reset

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Review TRM section 20.3.1 for additional details

Internal Low-speed Oscillator (ILO)

Refer to the Device Power Modes training section for additional power modes details

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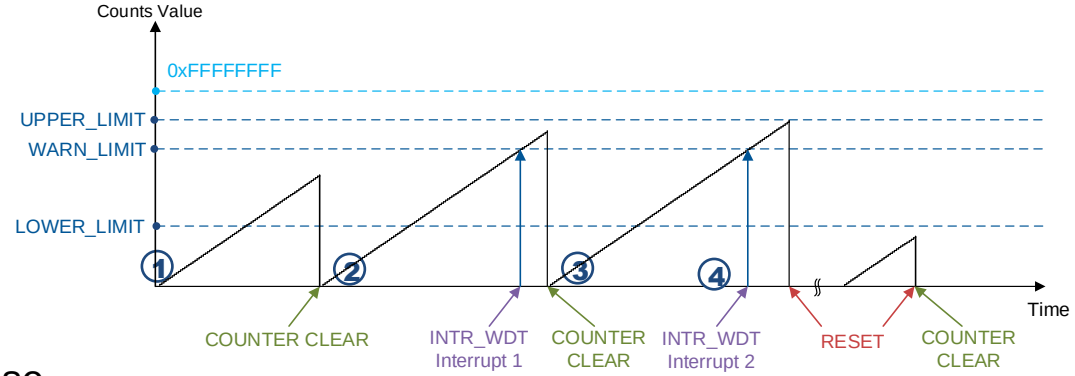
Basic WDT operation

1. Counter is cleared between LOWER_LIMIT and WARN_LIMIT
   No WARN interrupt is issued and no RESET is done
2. Counter is cleared between WARN_LIMIT and UPPER_LIMIT
   A WARN interrupt is issued but no RESET is done
3. When the counter reaches the UPPER_LIMIT, a reset is executed
4. A reset is issued if the counter is cleared before the LOWER_LIMIT is reached



› Use case
  - LOWER_LIMIT and UPPER_LIMIT are used to activate the Window function
  - By using WARN_LIMIT, the interrupt can be used to debug before reset

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Review Register TRM and TRM section 20.3.2 for additional details

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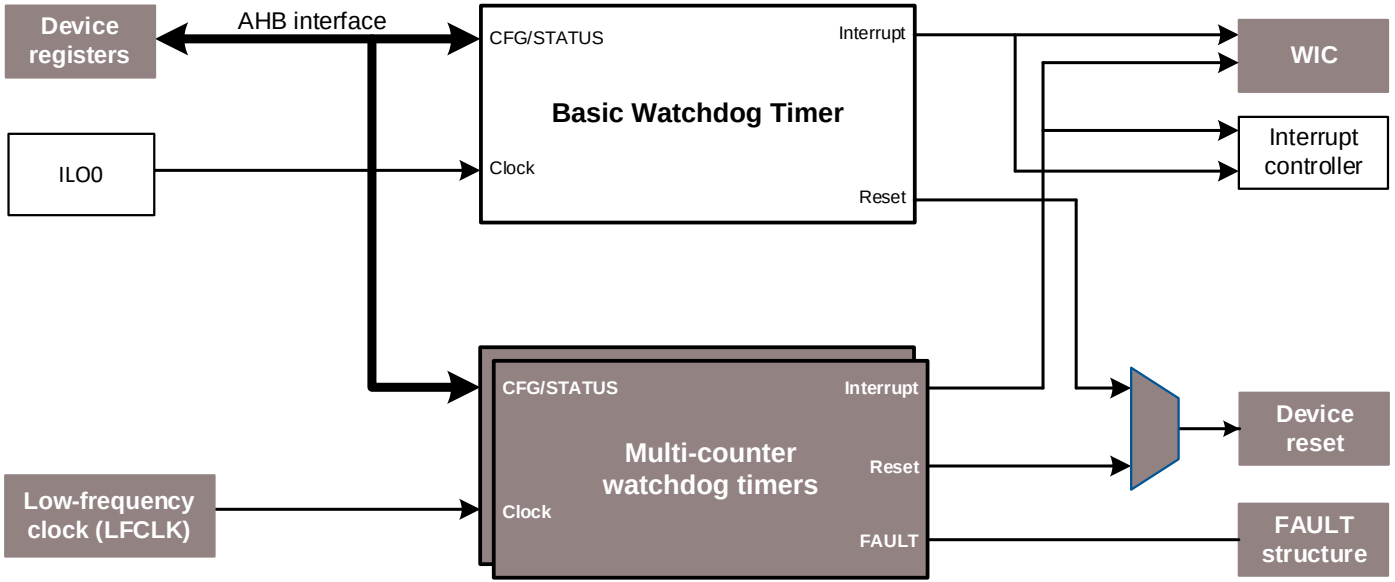
Multi-counter WDT block diagram



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Review TRM section 20.4 for additional details

XMC7000 devices support three units of MCWDT

Depending on the device, up to four units are supported

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Multi-counter WDT overview

- Features
  - Three independent counters
    - Two 16-bit counters that support:
      - Window mode
      - Interrupt mode with enabled/disabled AUTO_SERVICE
    - One 32-bit counter that supports:
      - Interrupt generation
    - Input clock source: LFCLK (ILO0, ILO1, ECO, and WCO)
  - Can operate in three power modes
    - Active
    - Sleep
    - DeepSleep
  - Disabled after power-on
  - Registers that are protected and require an unlock sequence
  - Device reset that occurs if the FAULT is not handled within two LFCLK cycles

Hint Bar

Review TRM section 20.4 for additional details

Refer to the Clock System training section for additional ILO, ECO, and WCO details

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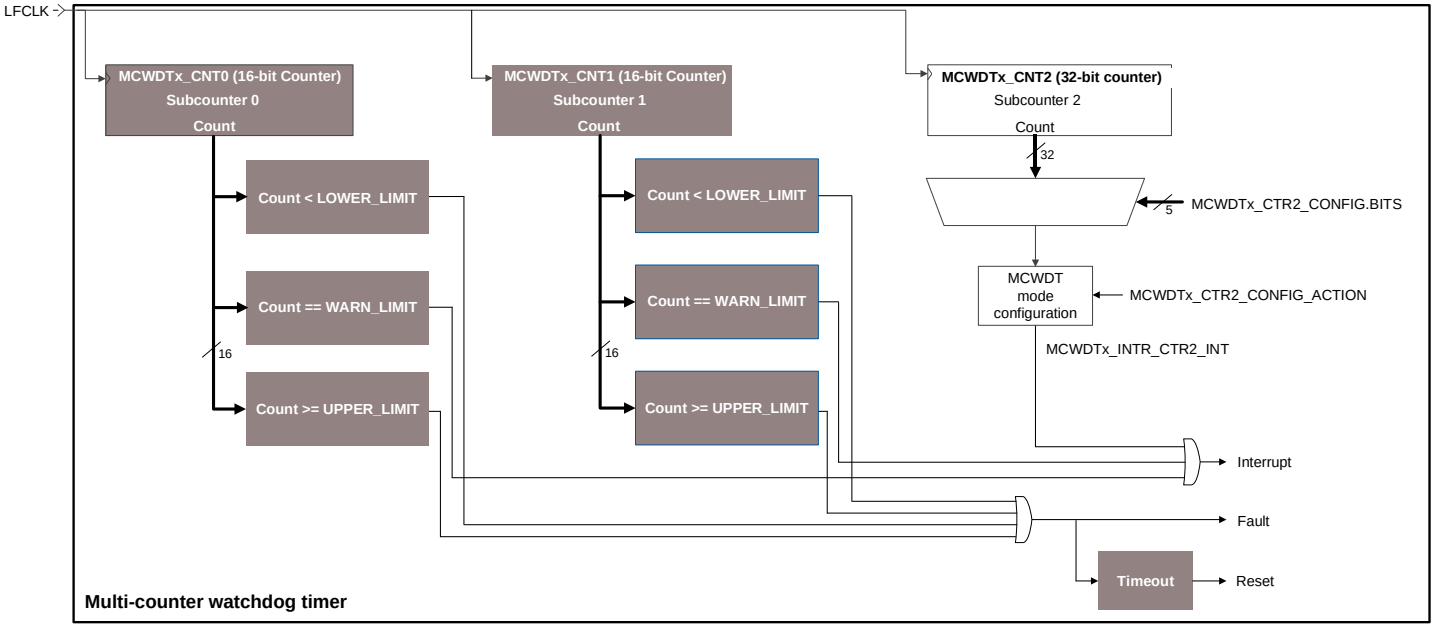
Subcounter 0/1 operation (1/5)

- Subcounter 0 (MCWDTx_CNT0) 1 and Subcounter 1 (MCWDTx_CNT1) are independent 16-bit up-counters



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Review Register TRM and TRM section 20.4.2.1 for additional details

[1] Prefix "x" in MCWDTx represents the number of MCWDT. The number of MCWDT varies by device. It starts with 0.

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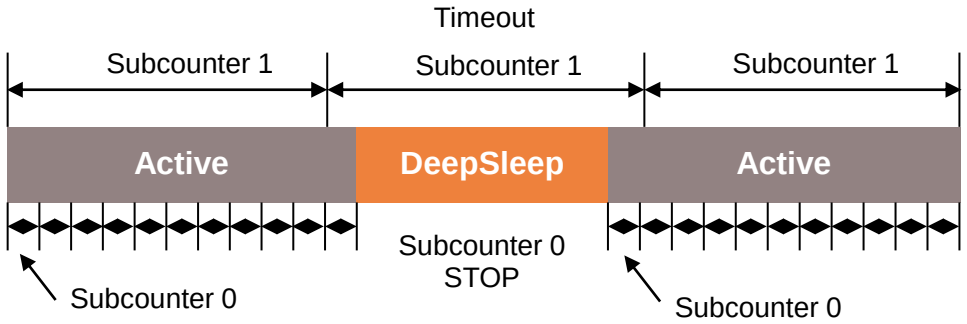
Subcounter 0/1 operation (2/5)

- MCWDT does not change limits for DeepSleep mode entry or exit automatically
- To get a behavior similar to DeepSleep, subcounters 0 and 1 can work together through SW configuration[1]
- Use case
  - Subcounter 0: Can be configured with a timeout threshold that protects running SW and configured to stop during DeepSleep
  - Subcounter 1: Can be configured with a longer timeout that continues to operate during DeepSleep



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Review TRM section 20.4.5 for additional details

[1] One MCWDT block can be associated to one CPU. This selects which CPU SLEEPDEEP signal is used for SLEEPDEEP_PAUSE

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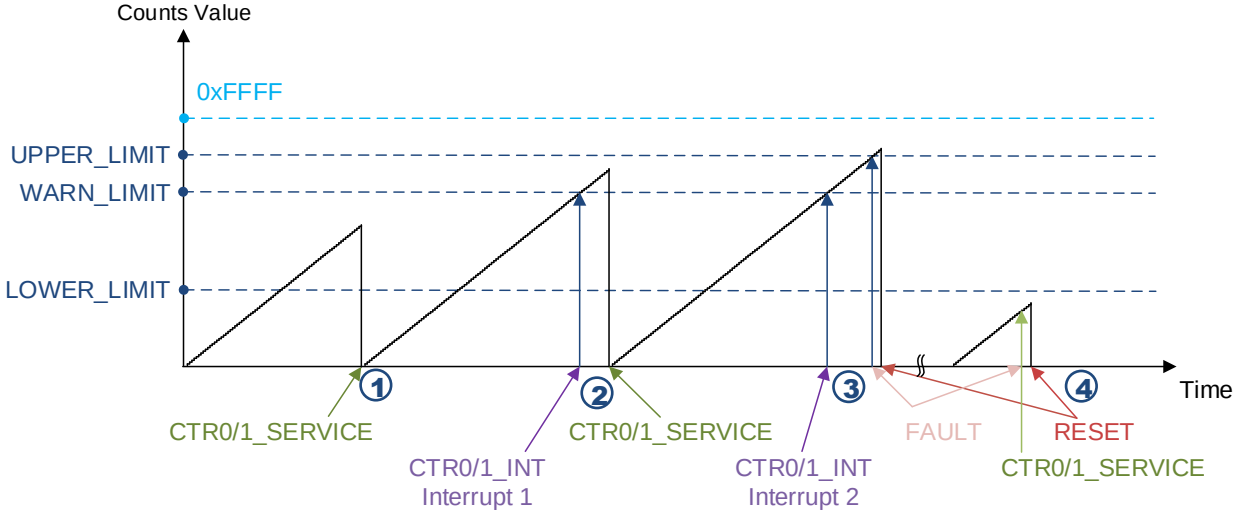
Subcounter 0/1 operation (3/5)

› Sequence of scenarios in Window mode



① Counter is cleared between LOWER_LIMIT and WARN_LIMIT.
No WARN interrupt and no RESET

② Counter is cleared between WARN_LIMIT and UPPER_LIMIT.
WARN interrupt is issued but no RESET

③ When the counter reaches the UPPER_LIMIT a FAULT is issued. A RESET can be issued in case the FAULT is not handled in time by the software

④ Counter is cleared before the LOWER_LIMIT is reached. A FAULT is issued. A RESET can be issued if the FAULT is not handled in time by the software.

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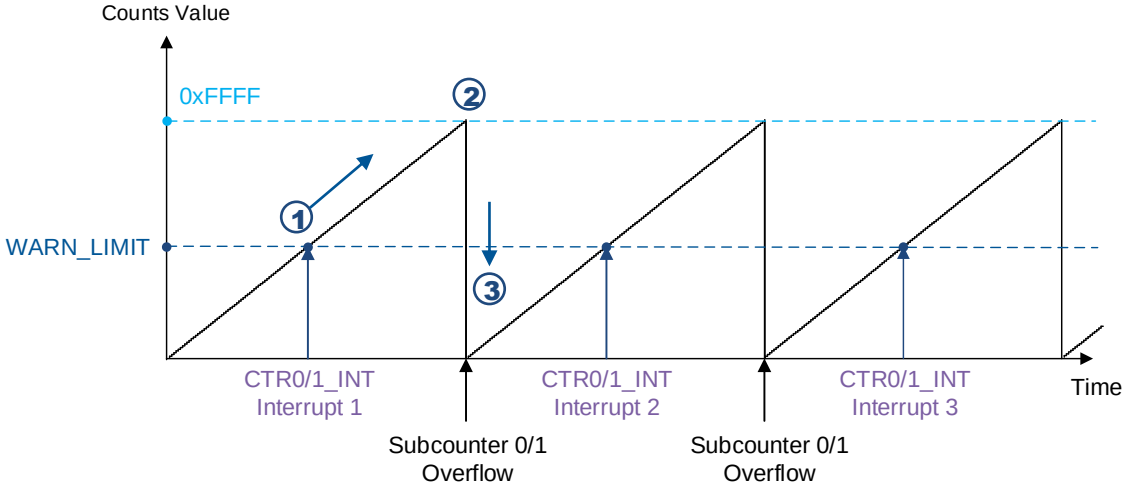
Subcounter 0/1 operation (4/5)

› 16-bit subcounters with WARN interrupt only (AUTO_SERVICE = 0) operate as follows:



① Counter continues to increment after the counter value matches the WARN_LIMIT

② Counter continues to count up until the 16-bit maximum value is reached

③ Counter overruns and restarts at zero

Hint Bar

Review TRM section 20.4.2.1 for additional details

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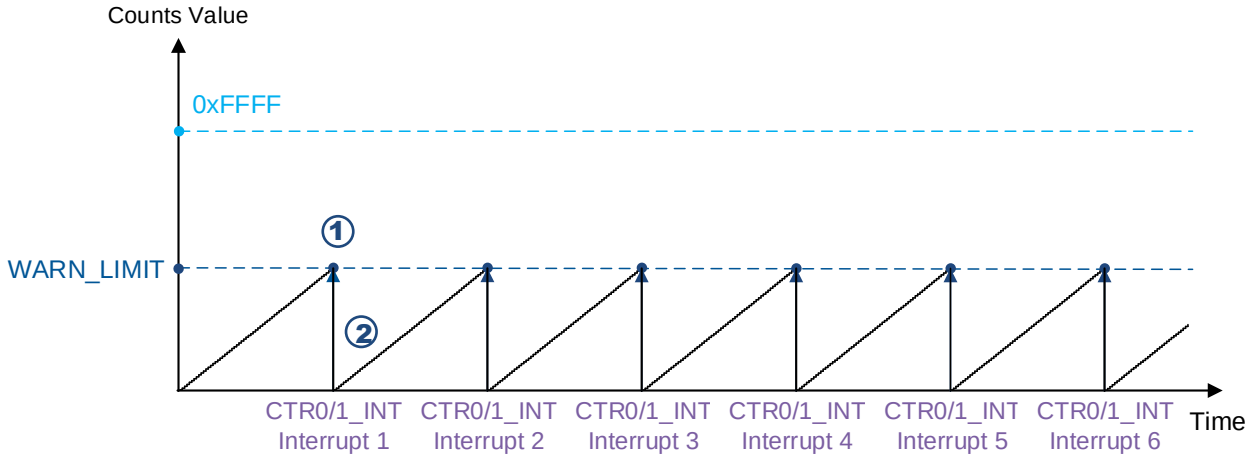
Subcounter 0/1 operation (5/5)

› 16-bit subcounters with WARN interrupt only with enabled automatic service (AUTO_SERVICE = 1) operate as follows:



① When the counter matches the WARN_LIMIT, an interrupt is issued

② The AUTO_SERVICE function clears the counter on any match event

Hint Bar

Review TRM section 20.4.2.1 for additional details

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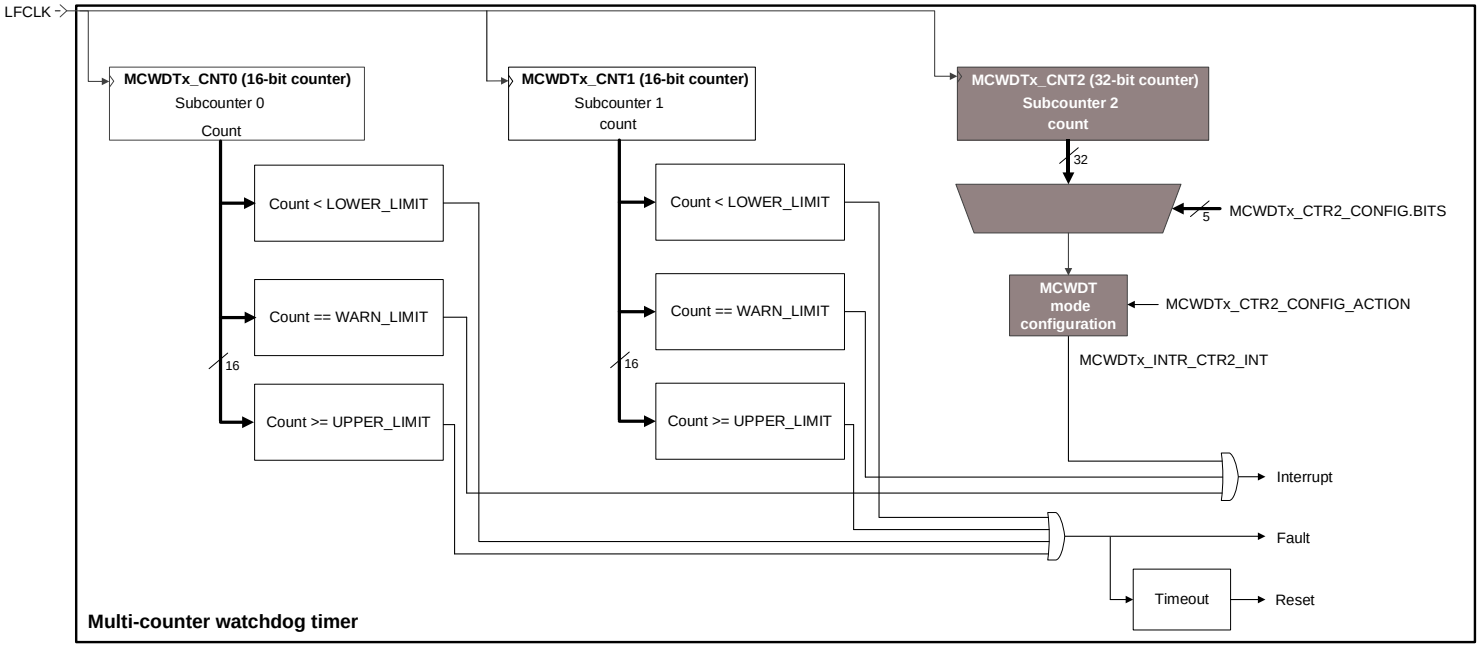
32-bit counter operation (1/2)

- Subcounter 2 (MCWDTx_CNT2) is a 32-bit free-running counter that can be configured to generate an interrupt when one of the counter bits toggle
- Does not support Window mode



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Review TRM section 20.4.2.2 for additional details

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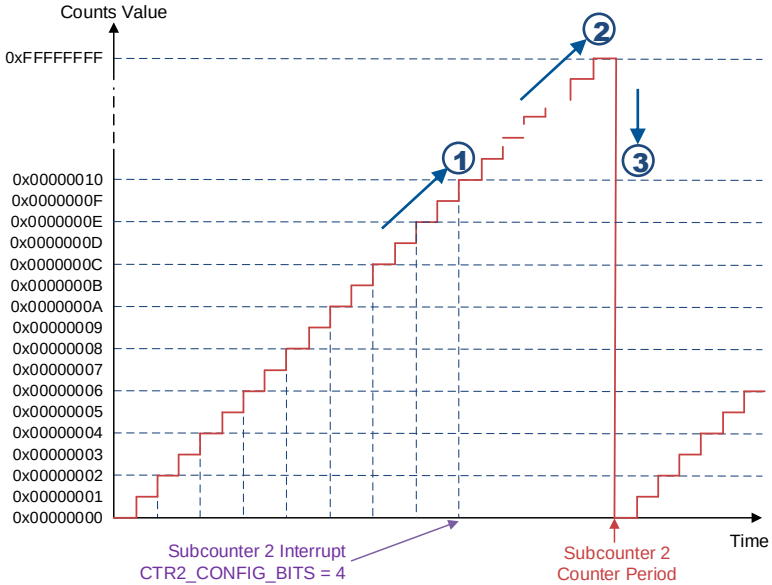
32-bit counter operation (2/2)



Hint Bar

Review Register TRM and TRM section 20.4.2.2 for additional details

› When BIT = 4 is selected on the register, Subcounter 2 operates as follows:

1. Counter counts up and interrupt[1] is generated on each toggle of the corresponding bit
2. Counter continues to count up until the 32-bit maximum value is reached
3. Counter overflows and restarts

[1] The interrupt generated is a warning interrupt

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Enabling and disabling WDT

- WDT counters can be enabled and disabled by setting the registers
- Basic WDT
  - Enabled by setting the ENABLE[31] bit in the WDT_CTL register
  - Disabled by clearing the setting
- MCWDT counters
  - Enabled by setting the ENABLE[31] bit in the MCWDTx_ CTRy_CTL and MCWDTx_CTR2_CTL registers
  - Disabled by clearing the setting
- Advantage
  - Settings can be configured according to your system requirements

Hint Bar

Review Register TRM and chapter 20.4 for additional details

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WDT Lock feature

- Basic WDT
  - Locked by default
  - When the WDT_LOCK bits are not equal to ‘0’, write access to the following registers is prohibited:
    - CTL, LOWER_LIMIT, WARN_LIMIT, UPPER_LIMIT, CNT, and SERVICE
- MCWDT counters
  - Unlocked by default
  - When the MCWDT2_LOCK bits are not equal to ‘0’, write access to some registers is prohibited[1]
- When registers are locked, software writes are always ignored
- Advantage
  - Protection through lock feature is for the functional safety of the system

Hint Bar

Review Register TRM and TRM chapter 20 for additional details

[1] Refer to the Appendix for the registers list

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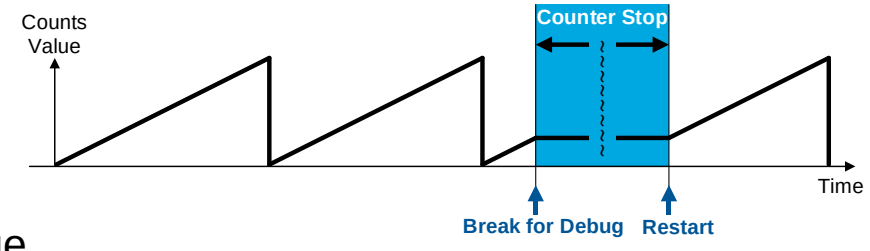
Debug mode

- Both Basic WDT and MCWDT support debug mode
- Depending on DEBUG_TRIGGER_EN and DEBUG_RUN bit configuration, there are three options in debug mode
  - Counter is stopped when a debugger is connected
  - Counter is stopped only when a debugger is connected and the CPU is halted during a breakpoint
  - Counter is running when a debugger is connected. No reset is issued when the CPU is halted during a breakpoint but the counter is not stopped



- Advantage
  - Even if you break for debugging, you can debug with the same counter operation as the actual operation

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Review Register TRM and TRM chapter 20.6 for additional details

It may take up to two clk_hf cycles for the counter to pause and another two cycles to resume, due to the internal synchronization

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Reset cause detection

- Reset generated by the WDT counters are indicated by the bit in the RES_CAUSE register
  - Basic WDT
    - RESET_WDT [0] bit
  - MCWDT counters
    - RESET_MCWDT0 [5], RESET_MCWDT1 [6], RESET_MCWDT2 [7], and RESET_MCWDT3 [8] bits
- The bits remain set until cleared or until a power-on reset (POR), brownout reset (BOD), or external reset (XRES) occurs

Hint Bar

Review TRM section 20.5 for additional details

Refer to Reset System training section for additional reset details

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Appendix

Register list - Basic WDT

Lockable	Register	Name	Description
✔	WDT_CTL	Watchdog Control Register	Control register for the Basic WDT
✔	WDT_LOWER_LIMIT	WDT Lower Limit Register	Lower limit for the Basic WDT
✔	WDT_UPPER_LIMIT	WDT Upper Limit Register	Upper limit for the Basic WDT
✔	WDT_WARN_LIMIT	WDT Warn Limit Register	Warn limit for the Basic WDT
✔	WDT_CONFIG	WDT Configuration Register	Configuration for the Basic WDT. Includes the ACTION configuration for UPPER, LOWER, and WARN limits, auto-servicing and pause settings in low-power and debug modes
✔	WDT_CNT	WDT Count Register	Count value for the Basic WDT
	WDT_LOCK	WDT Lock Register	Lock or unlock the Basic WDT registers
✔	WDT_SERVICE	WDT Service Register	Clears the Basic WDT counter
	WDT_INTR	WDT Interrupt Register	Interrupt signal from Basic WDT
	WDT_INTR_SET	WDT Interrupt Set Register	Can be used to set interrupts for firmware testing
	WDT_INTR_MASK	WDT Interrupt Mask Register	Controls whether interrupt is forwarded to CPU. All masks block the interrupt when 0 and forward the interrupt when 1
	WDT_INTR_MASKED	WDT Interrupt Masked Register	Bitwise AND between the interrupt request and mask registers so firmware can read the status of all mask-enabled interrupt causes with a single load operation

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Register list - MCWDT (1/2)

Lockable	Register	Name	Description
✓	MCWDTx_CTRy_CTL	MCWDT Subcounter 0/1 Control Register	Control register for MCWDT subcounter
✓	MCWDTx_CTRy_LOWER_LIMIT	MCWDT Subcounter 0/1 Lower Limit Register	Lower limit for this MCWDT subcounter
✓	MCWDTx_CTRy_UPPER_LIMIT	MCWDT Subcounter 0/1 Upper Limit Register	Upper limit for this MCWDT subcounter
✓	MCWDTx_CTRy_WARN_LIMIT	MCWDT Subcounter 0/1 Warn Limit Register	Warn limit for this MCWDT subcounter
✓	MCWDTx_CTRy_CONFIG	MCWDT Subcounter 0/1 Configuration Register	Configuration for MCWDT subcounter. Includes the ACTION configuration for Upper, Lower, and Warn limits
✓	MCWDTx_CTRy_CNTy	MCWDT Subcounter 0/1 Count Register	Count value for this MCWDT subcounter
✓	MCWDTx_CTR2_CTL	MCWDT Subcounter 2 Control Register	Control register for MCWDT subcounter 2
✓	MCWDTx_CTR2_CONFIG	MCWDT Subcounter 2 Configuration Register	Configuration for MCWDT subcounter 2
✓	MCWDTx_CTR2_CNT	MCWDT Subcounter 2 Count Register	Count value for this MCWDT subcounter 2
	MCWDTx_LOCK	MCWDT Lock Register	Lock or unlock the respective configuration registers of subcounters 0/1/2 of this MCWDT
✓	MCWDTx_SERVICE	MCWDT Service Register	Includes service bits to clear subcounter 0/1 of this MCWDT

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Register list - MCWDT (2/2)

Lockable	Register	Name	Description
	MCWDTx_INTR	MCWDT Interrupt Register	Interrupt status register for subcounters 0/1/2 for this MCWDT
	MCWDTx_INTR_SET	MCWDT Interrupt Set Register	This register can be used to trigger an interrupt for firmware testing
	MCWDTx_INTR_MASK	MCWDT Interrupt Mask Register	This register controls whether a subcounter interrupt is forwarded to the corresponding processor. All masks block the interrupt when 0 and forward the interrupt when 1
	MCWDTx_INTR_MASKED	MCWDT Interrupt Masked Register	Bitwise AND between the interrupt request and mask registers so firmware can read the status of all mask enabled interrupt causes with a single load operation
	CLK_SELECT	Clock Selection Register	Clock source selection register
	CLK_ILO0_CONFIG	ILO0 Configuration	ILO0 configuration
	RES_CAUSE	Reset Cause Observation Register	Reset cause observation register

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Revision History

Revision	ECN	Submission Date	Description of Change
**	7759734	2022-05-06	Initial release

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