Customer training workshop

32-bit Arm® Cortex®-M7 microcontroller XMC7000 Trigger Multiplexer



Target products

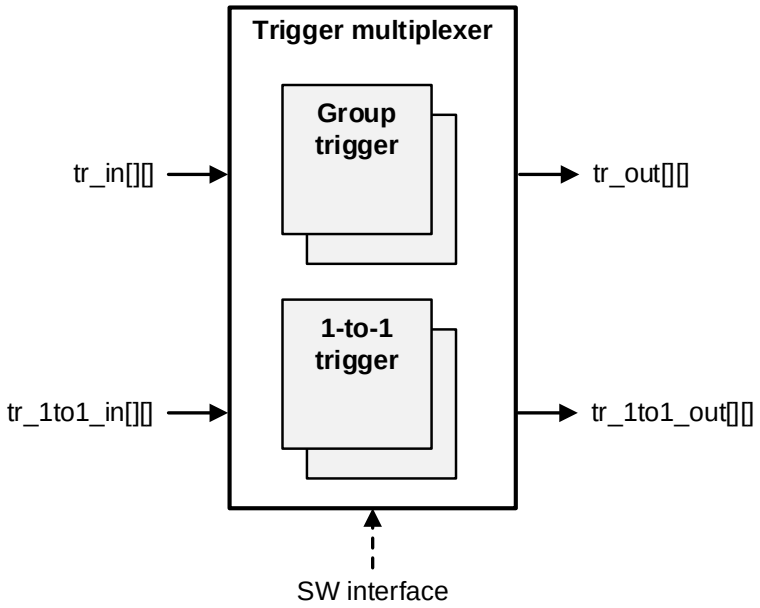
› Target product list for this training material:

Family category	Series	Code flash memory size
XMC7200	XMC7200-8M	Up to 8384 KB
XMC7100	XMC7100-4M	Up to 4160 KB

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Trigger multiplexer overview

- The trigger multiplexer helps the user route triggers from a source peripheral block to a destination
- Features
  - Ability to connect any trigger signal from one peripheral to another
  - Up to 16 multiplexer-based trigger groups
  - Up to 16 one-to-one trigger groups
  - Software (SW) trigger support to trigger any signal in the block
  - Ability to configure a trigger multiplexer with trigger manipulation feature in HW such as inversion and edge /Level detection



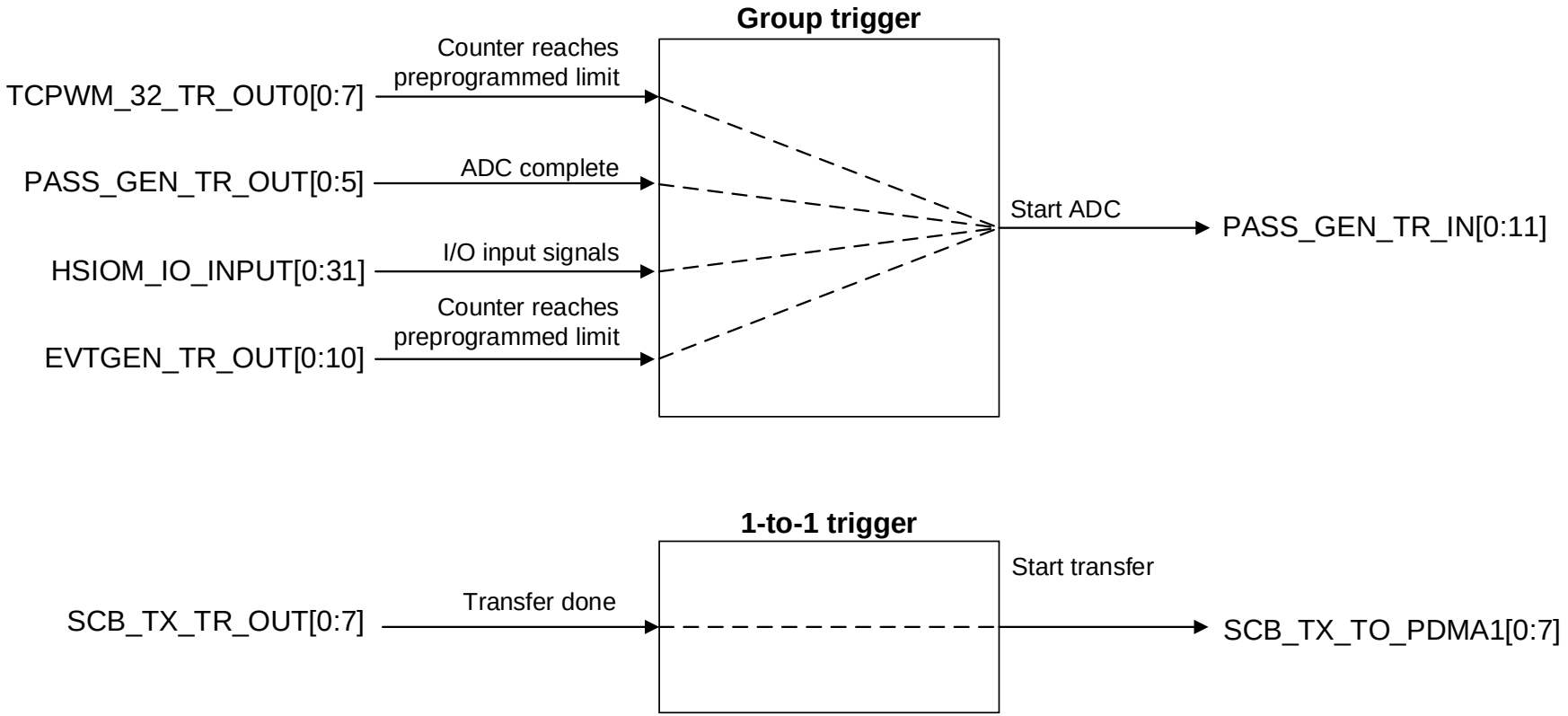
Hint Bar

Review TRM section 28.1 for additional details

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Trigger multiplexing

- A trigger input signal indicates the completion of a peripheral action or a peripheral event
- A trigger output signal initiates a peripheral action



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Review TRM section 28.4 for additional details

Refer to the datasheet for the trigger list for each device

Trigger input:

- Level sensitive: FIFO empty

- Edge sensitive: ADC channel done

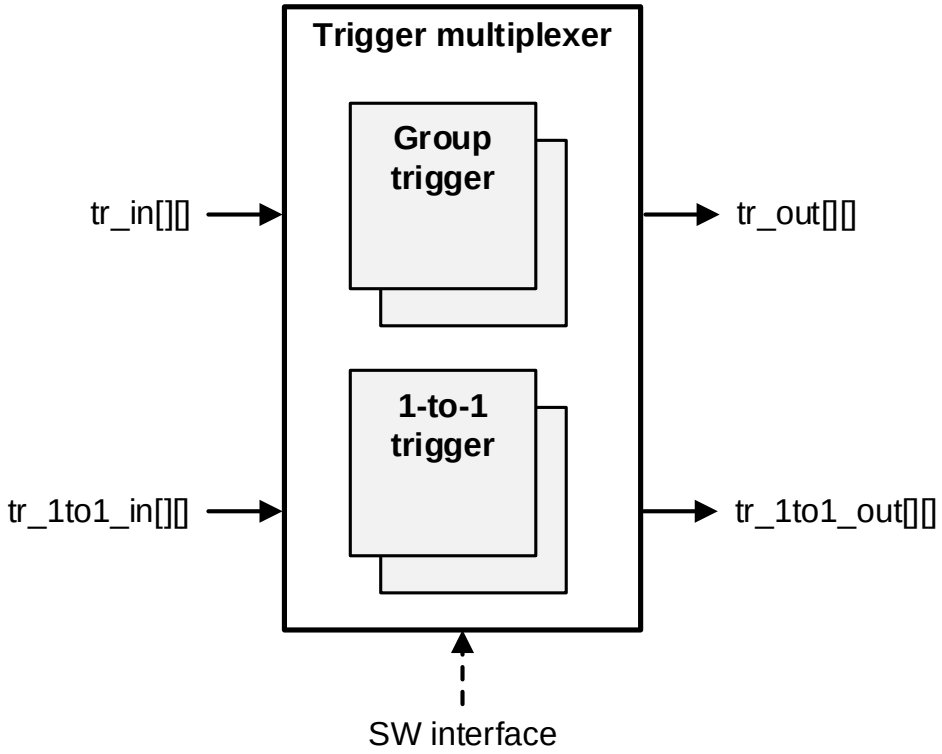
Trigger output:

- Invert

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Trigger multiplexer block diagram

- A trigger multiplexer consists of multiple trigger groups, which are of two types:
  - Group trigger
  - 1-to-1 trigger



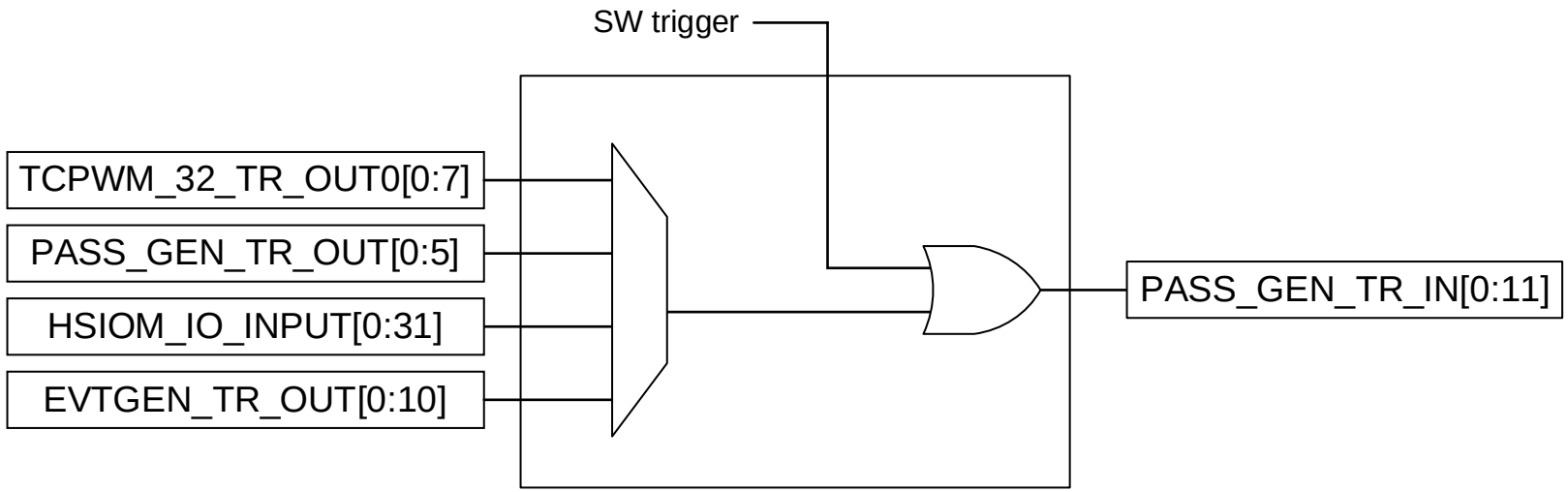
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Review TRM section 28.3 for additional details

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Group trigger

- Functionalities
  - Connects a peripheral input trigger to multiple peripheral output triggers
  - Generates a SW trigger



Example of group trigger

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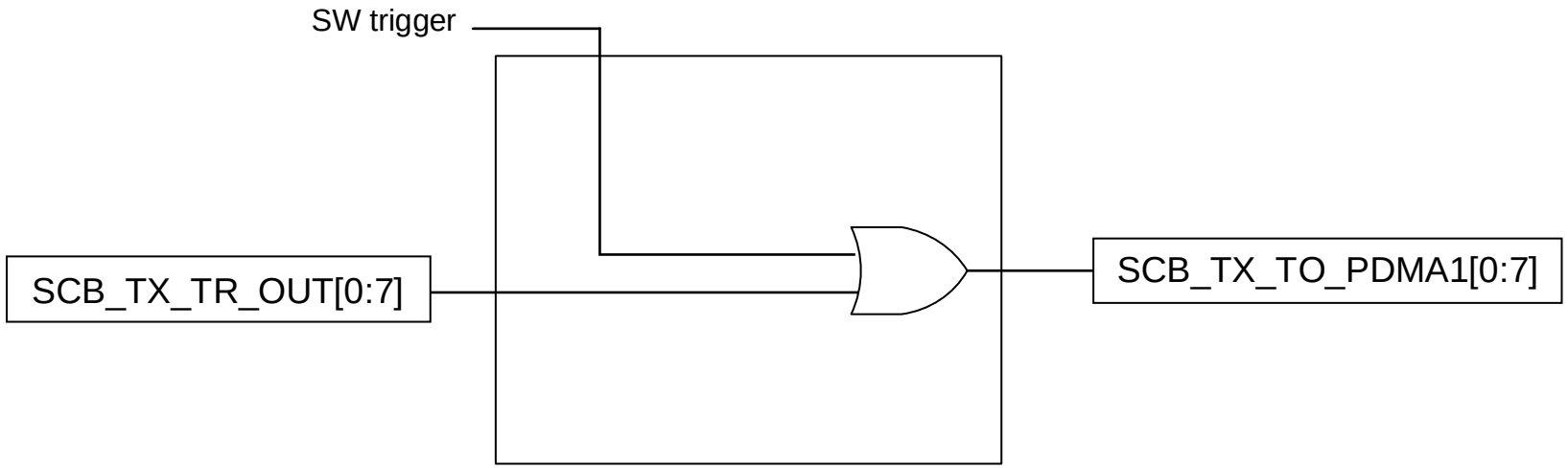
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Multiple peripheral output triggers are selected by the software

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1-to-1 trigger

- Functionalities
  - Connects a peripheral input trigger to a specific peripheral output trigger
  - Generates a SW trigger



Example of 1 - to- 1 trigger

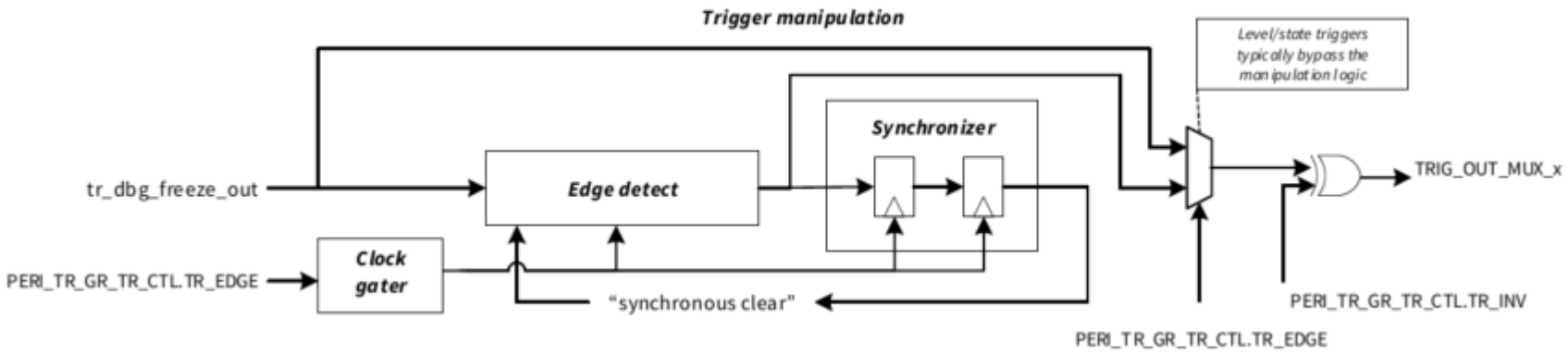
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Trigger Manipulation

- Functionalities
  - Trigger manipulation logic provides asynchronous edge detection
  - Synchronization of the trigger signal to the peripheral clock domain
  - Hardware trigger signal level inversion



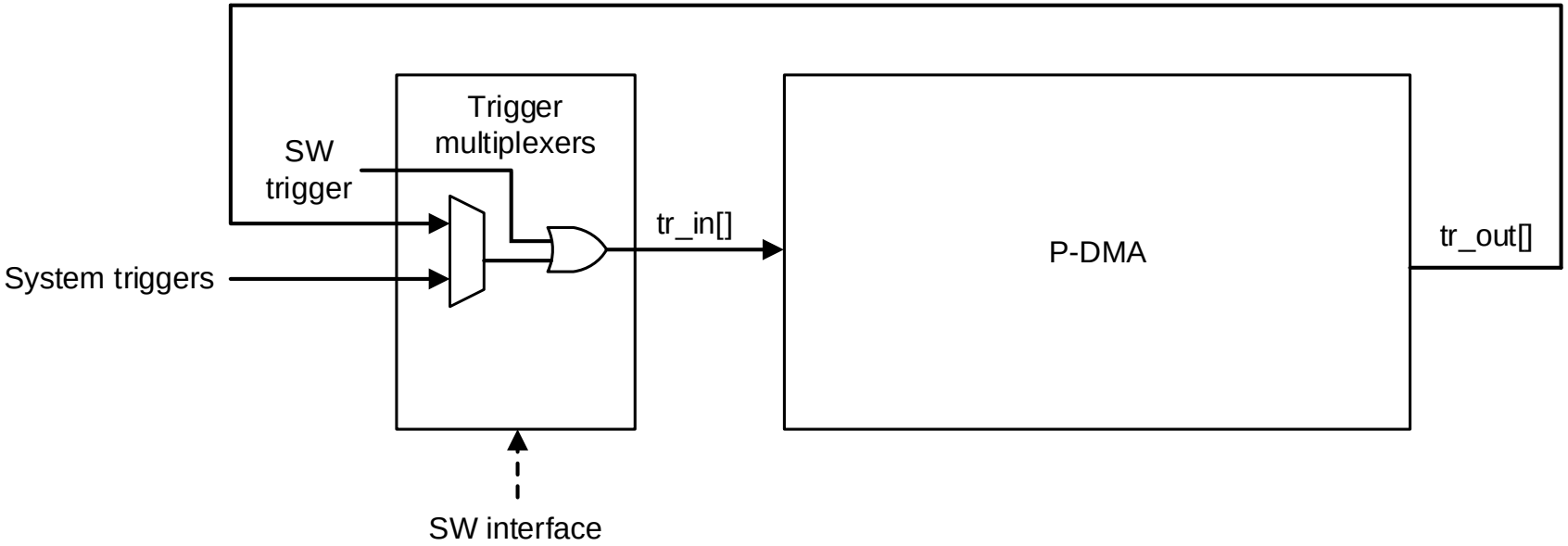
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Use case: SW trigger

- SW trigger is written as one of the system triggers of a bit-encoded interrupt in P-DMA
  - P-DMA activation made through the SW trigger can enable the initial CRC on program data



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Review TRM section 28.5 for additional details

Refer to the Direct Memory Access Training section for additional details on P-DMA

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Revision history

Revision	ECN	Submission Date	Description of Change
*	7760347	2022-05-09	Initial release

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