

XMC7000 Timer/counter/pulse-width modulator (TCPWM)

Customer training workshop (CTW)

January 2026

public

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Target products

Target product list for this training material:

Family category	Series	Code flash memory size
XMC7200	XMC7200-8M	Up to 8384 KB
XMC7100	XMC7100-4M	Up to 4160 KB

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XMC7200 - 8M family



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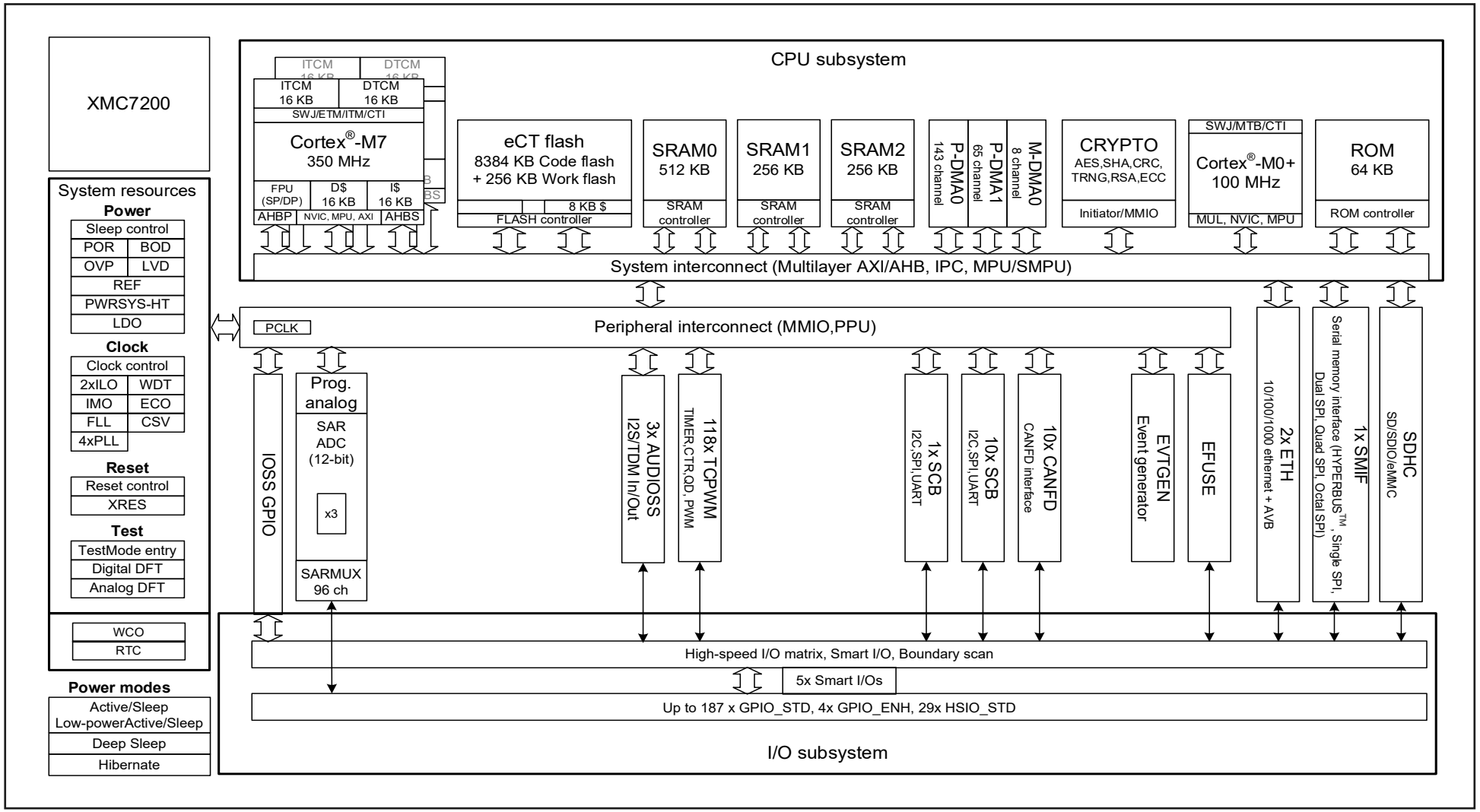
Introduction to XMC7200 - 8M

– TCPWM is located in the peripheral blocks



Hint bar

See the architecture reference manual, Top level architecture (section 1.2), for additional details specific to the CPUSS.

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XMC7100 - 4M family



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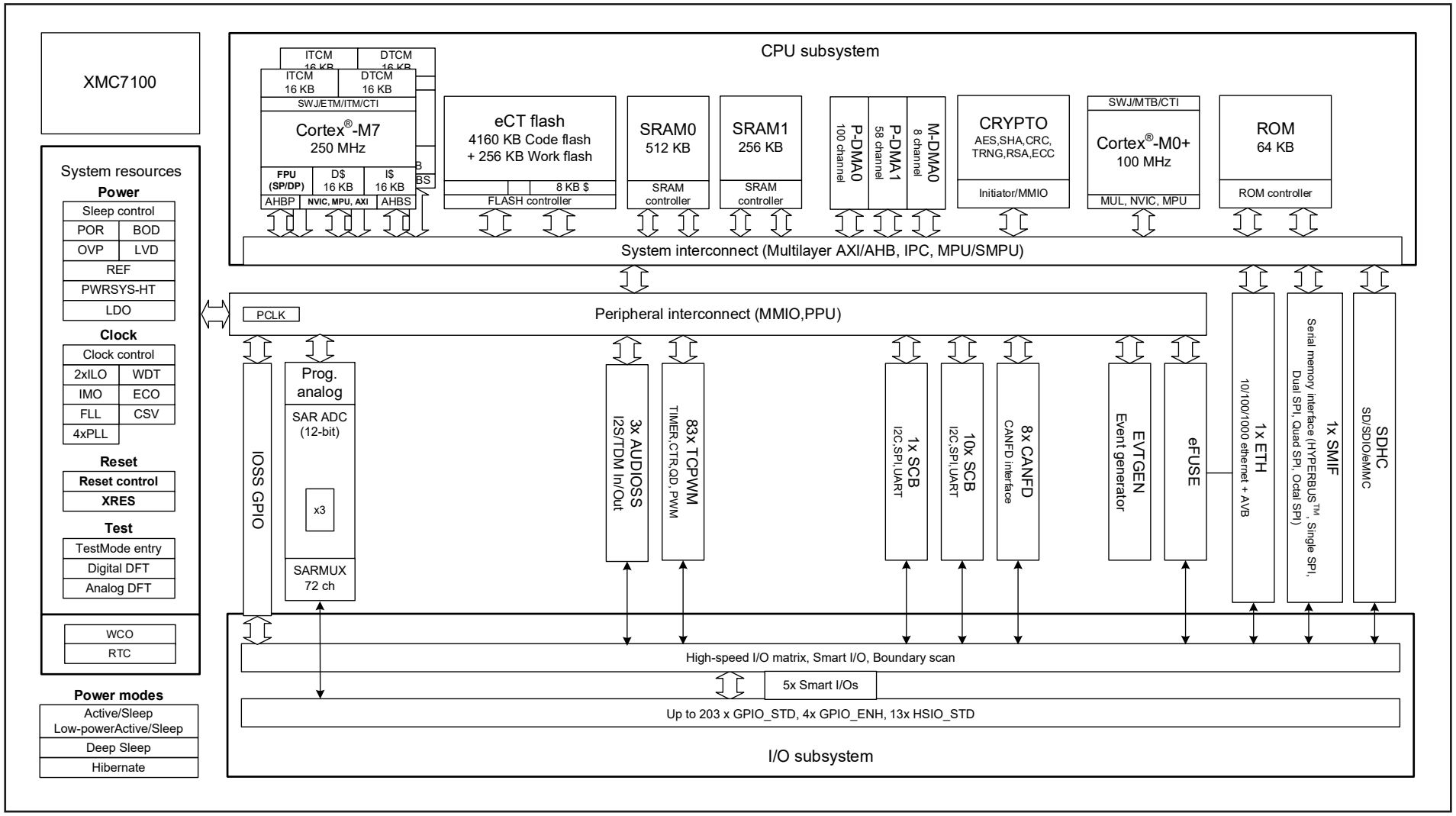
Introduction to XMC7100 - 4M

– TCPWM is located in the peripheral blocks



Hint bar

See the architecture reference manual, Support (section 2.1), for additional details specific to the CPUSS.

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Timer counter pulse width modulator (TCPWM)



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Overview

The Timer/counter/pulse-width modulator (TCPWM) block in XMC7000 implements the following functionality:

- Timer
- Capture
- Quadrature decoder
- Pulse-width modulation (PWM)
- PWM with dead time insertion (PWM_DT)
- PWM pseudo-random (PWM_PR)
- Shift register (SR)

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See the architecture reference manual, TCPWM (chapter 25), for additional details.

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Features

Counter specification

- Supports up to four counter groups (device-specific1)
- Each counter group consists of up to 256 counters (counter group-specific1)

Each counter

- Can run in one of the seven function modes
- Supports various counting modes
  - One-shot mode and Continuous mode (Up/Down/Up-down)
- Selects input signals
  - Start, Reload, Stop, Count, and two Capture event signals
- Generates output signals
  - Two output triggers, PWM output, and interrupt
- Supports debug mode

Hint bar

See the architecture reference manual, TCPWM (chapter 25), for additional details.

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Features (contd.)

- Motor control functions are supported only in the 16-bit for motor counter group
- Asymmetric PWM output control
  - This function has a different compare value when counting up and down
- PWM output selection for stepper motor
  - Two PWM output signals (line_out and line_compl_out) can be output by selecting one of the following values:
    - Constant low (0) or high (1)
    - PWM signal / Inverted PWM signal
    - Z (high impedance)
- Extend dead time
  - Dead time can be extended from 8 bits to 16 bits

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See the architecture reference manual, TCPWM (chapter 25), for additional details.

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Block components



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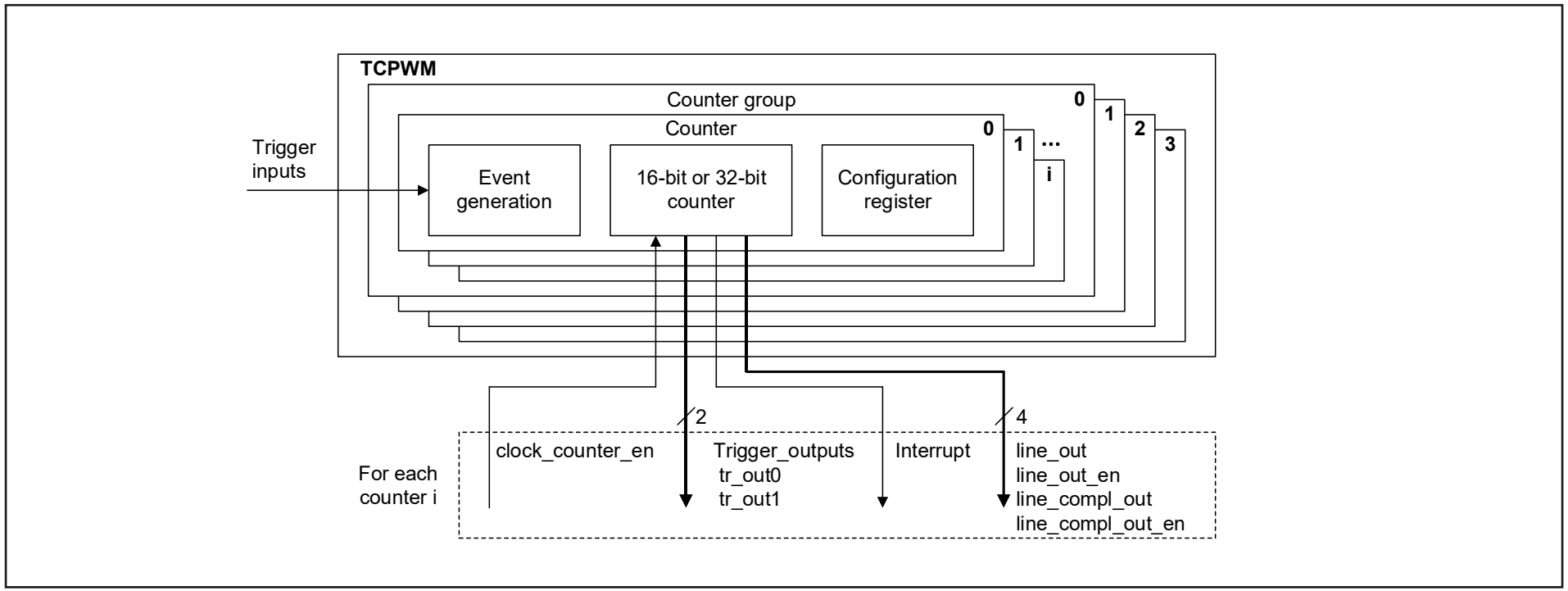
Components (1/42)

- TCPWM components
  - Event generation
- 16-bit or 32-bit counter



Hint bar

- See the architecture reference manual, TCPWM (chapter 25), for additional details
- See the features list in datasheet for additional details

[1] XMC7200 (272-pin) supports three counter groups. Refer to the respective device datasheet for the number of counter groups supported by each device.
- Counter Group 0: 87 ch (16 bit)
- Counter Group 1: 15 ch (16 bit for motor)
- Counter Group 2: 16 ch (32 bit)
- Counter Group 3: Not available

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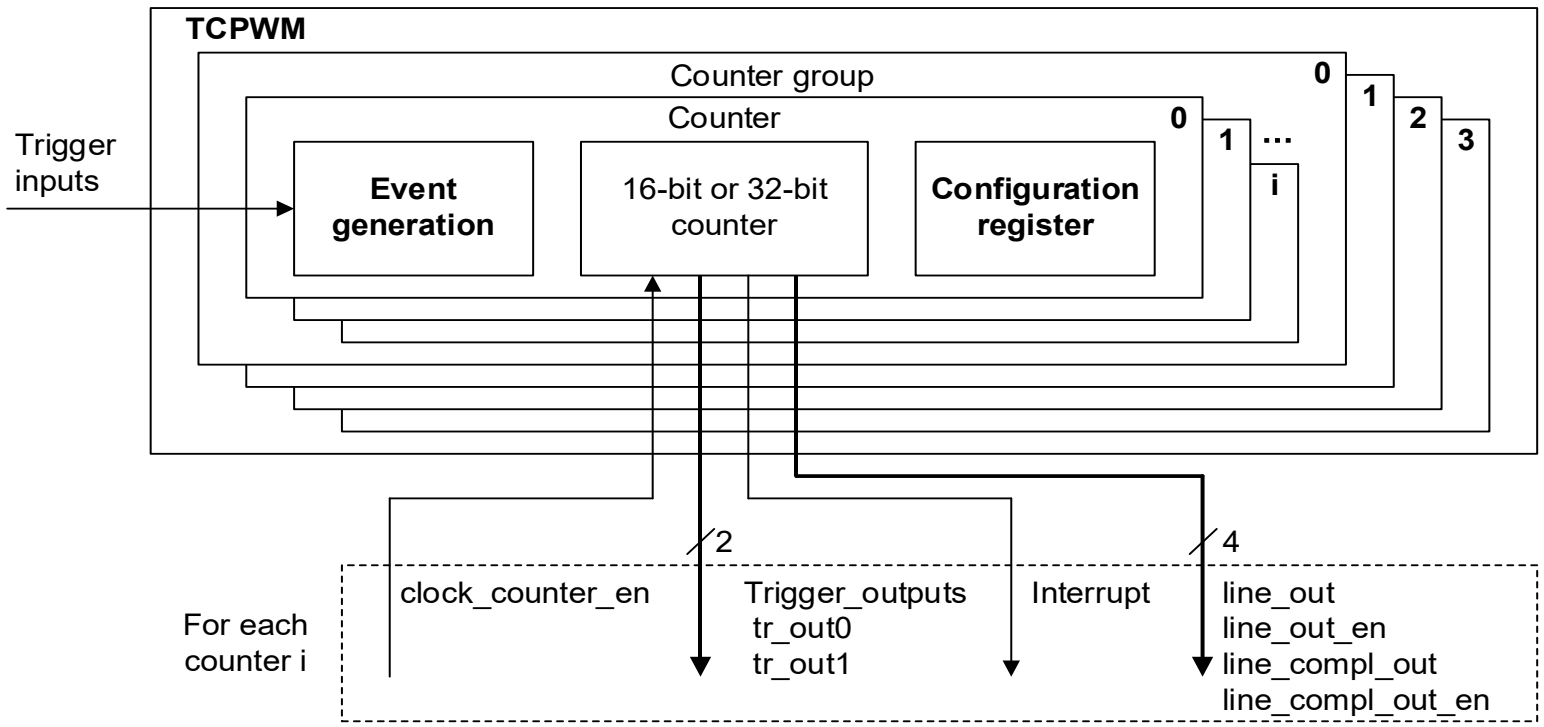
Components (2/42)

Event generation functions

– Input trigger selection
– Event detection



Hint bar

See the architecture reference manual, TCPWM (chapter 25), for additional details.

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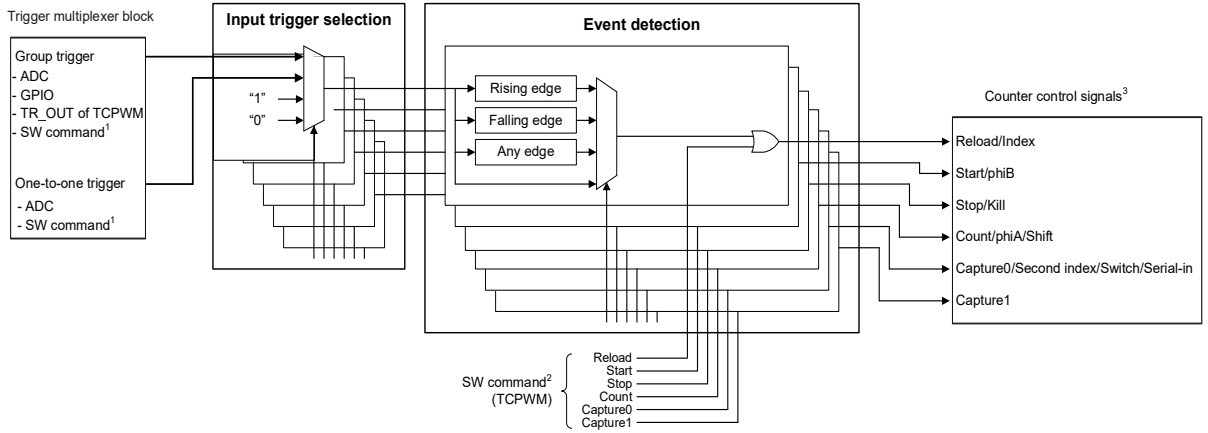
Components (3/42)

Input trigger selection and event detection

The counter control signals have the following features:

- Selects input signals from two types of trigger multiplexer signals
  - Group trigger (for example, timer) and one-to-one trigger (for example, GPIO inputs, ADC channels)
  - The constants ‘1’ and ‘0’ are also used as input triggers
- Detects the selected edge from four types
  - Rising edge, falling edge, any edge, and no edge
- Supports software (SW) commands
  - SW command of trigger multiplexer/SW command of TCPWM



[1] SW command (trigger multiplexer)
This signal can be synchronized to the counter clock.
[2] SW command (TCPWM)
This signal is asynchronous to the counter clock.
[3] The name of the counter control signal is changed by the counter function.

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See the architecture reference manual, TCPWM (chapter 25), for additional details.

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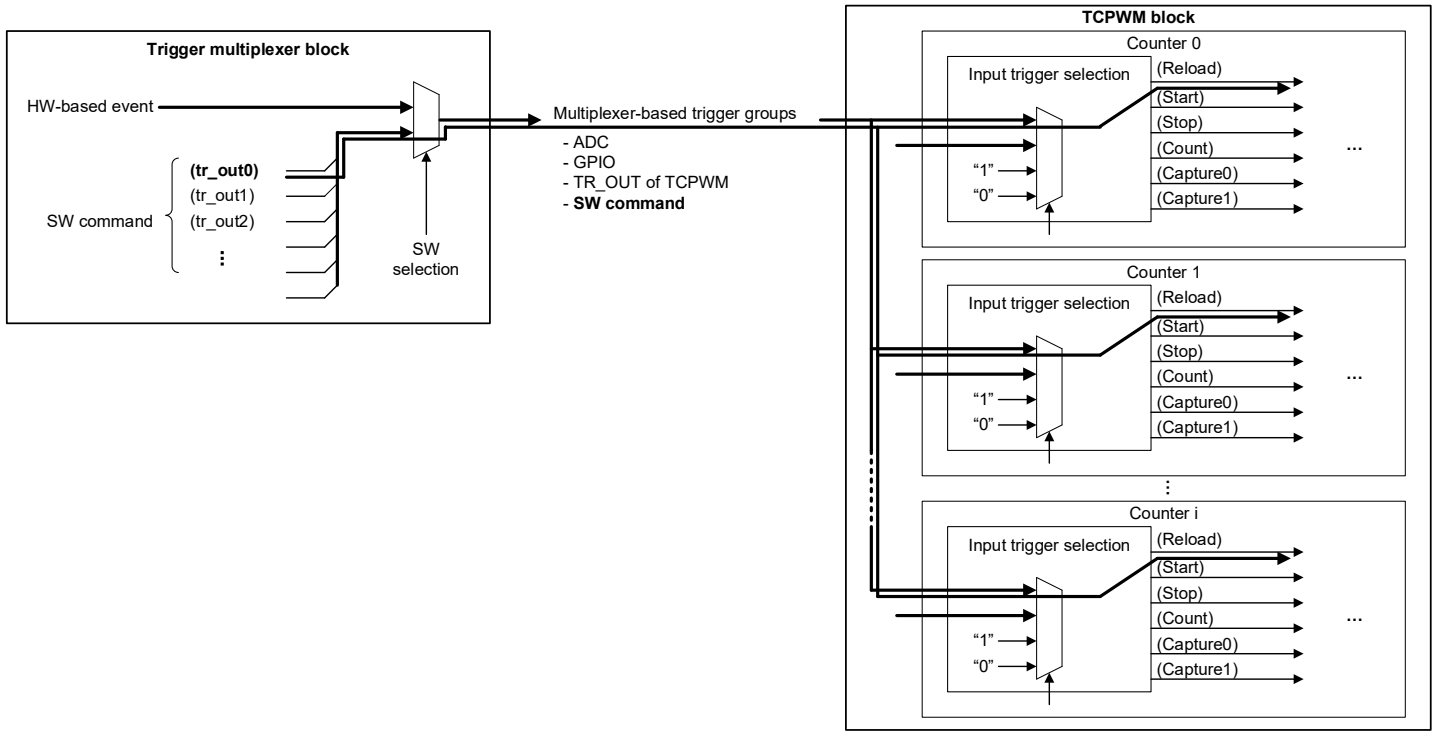
Components (4/42)

Simultaneous activation

- Advantage
  - When a trigger multiplexer block SW command is used, the TCPWM counters can also be activated at the same time



Hint bar

See the architecture reference manual, TCPWM (chapter 25), for additional details.

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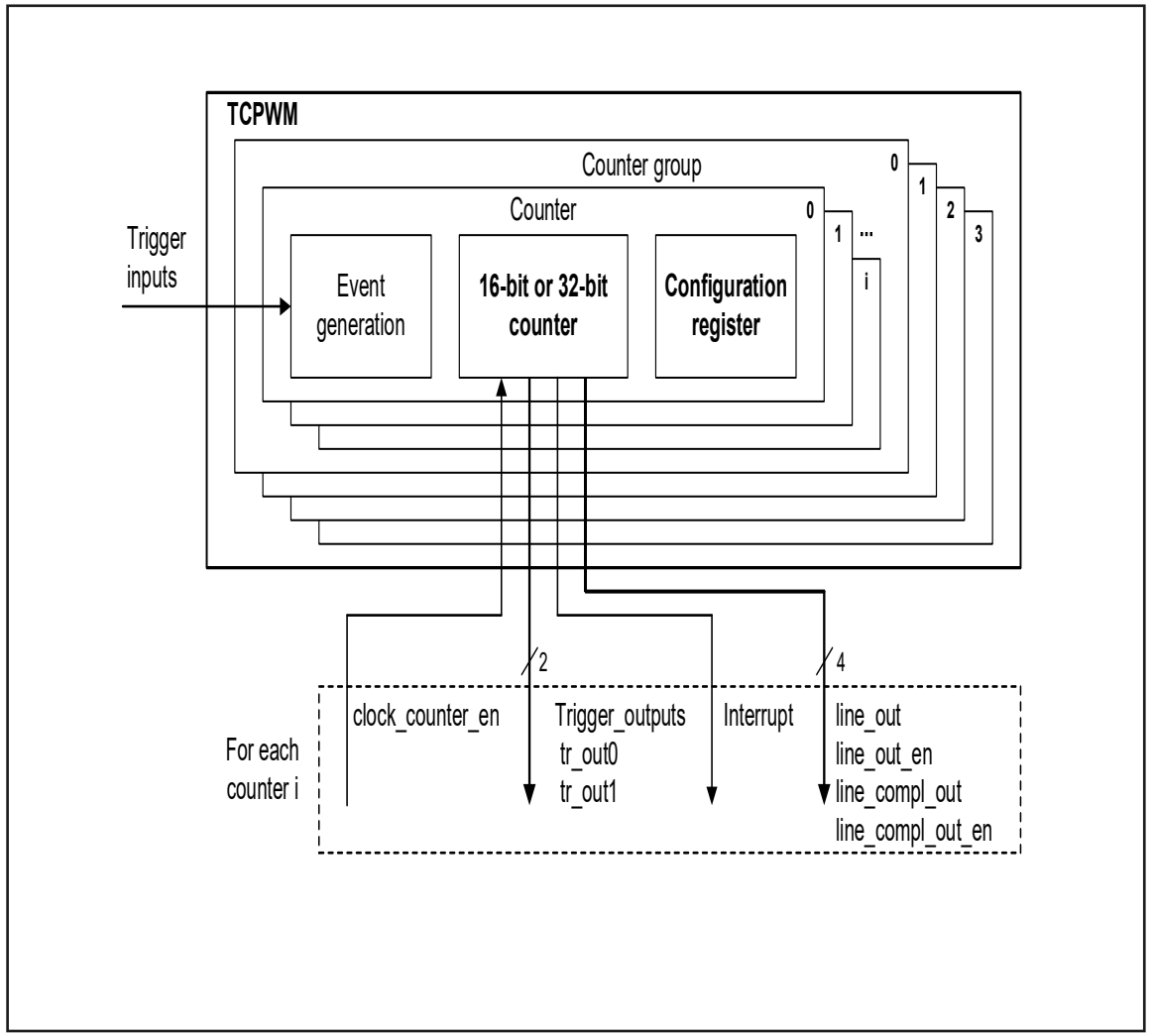
Components (5/42)

16-bit or 32-bit counter

- Functions
  - Timer
  - Capture
  - Quadrature decode
  - PWM
  - PWM_DT
  - PWM_PR
  - SR
- Trigger output and interrupt generation
- Clock enable
- Line output
- Debug mode



Hint bar

See the architecture reference manual, TCPWM (chapter 25), for additional details.

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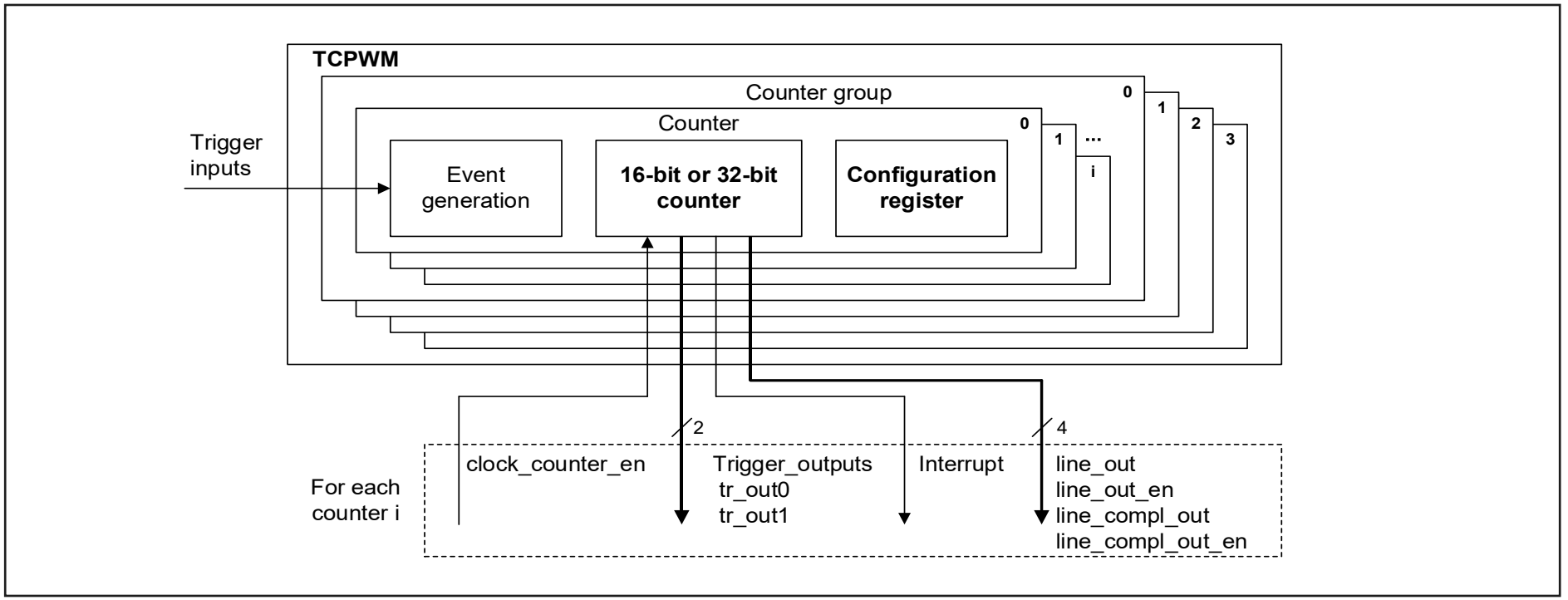
Components (6/42)

Trigger output and interrupt generation features

Each counter has trigger outputs (TR_OUT0/1) and an interrupt:

- Overflow (OV)
- Underflow (UN)
- Terminal Count (TC)
- CC0/1_MATCH
- LINE_OUT



Hint bar

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Components (7/42)

Trigger output and interrupt generation

– TR_OUT 0/1 and the interrupt are selected by SW

Factor	Description	TR_OUT0/1[1]	Interrupt
Overflow (OV)	An overflow event indicates that in an up counting mode, COUNTER equals PERIOD register, and is changed to a different value	✓	–
Underflow (UN)	An underflow event indicates that in a down counting mode, COUNTER equals 0, and is changed to a different value	✓	–
Terminal Count (TC)	A TC event is the logical OR of the underflow and overflow events	✓	✓
CC0/1_MATCH	This event is generated when the counter is running and one of the following conditions occur: – Counter equals the compare value – A capture event occurs and the CC0/1 and CC0/1_BUFF registers are updated	✓	✓
LINE_OUT	PWM output signal	✓	–

– TR_OUT can be routed through the trigger multiplexer to other peripherals on the device

[1] TR_OUT0/1 can also be disabled.

Hint bar

See the architecture reference manual, Trigger outputs (section 25.2.5), for additional details.

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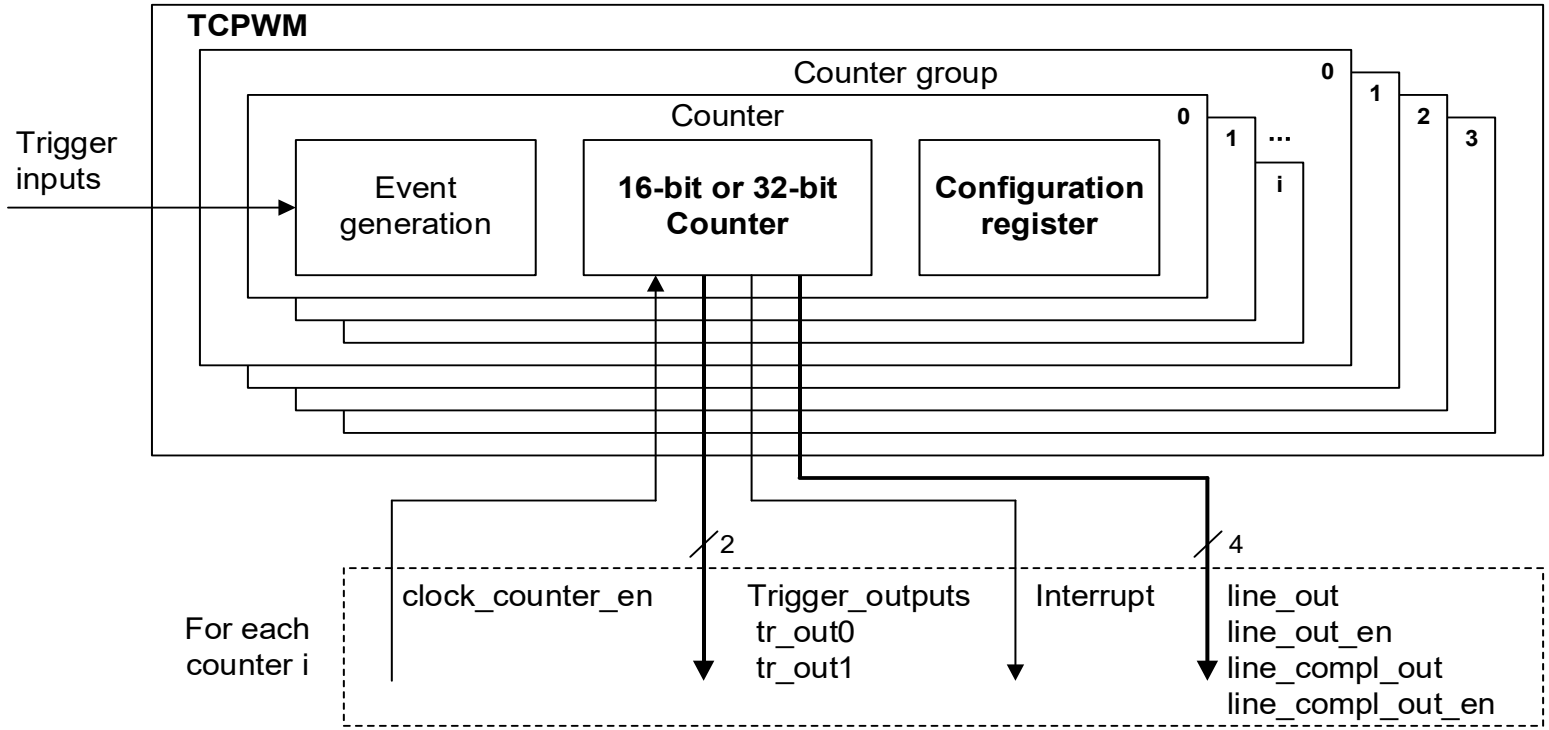
Components (8/42)

Clock enable

– A counter increments or decrements by ‘1’ for every counter clock cycle in which a count event is detected



Hint bar

See the architecture reference manual, TCPWM Clocking (section 25.2.2), for additional details.

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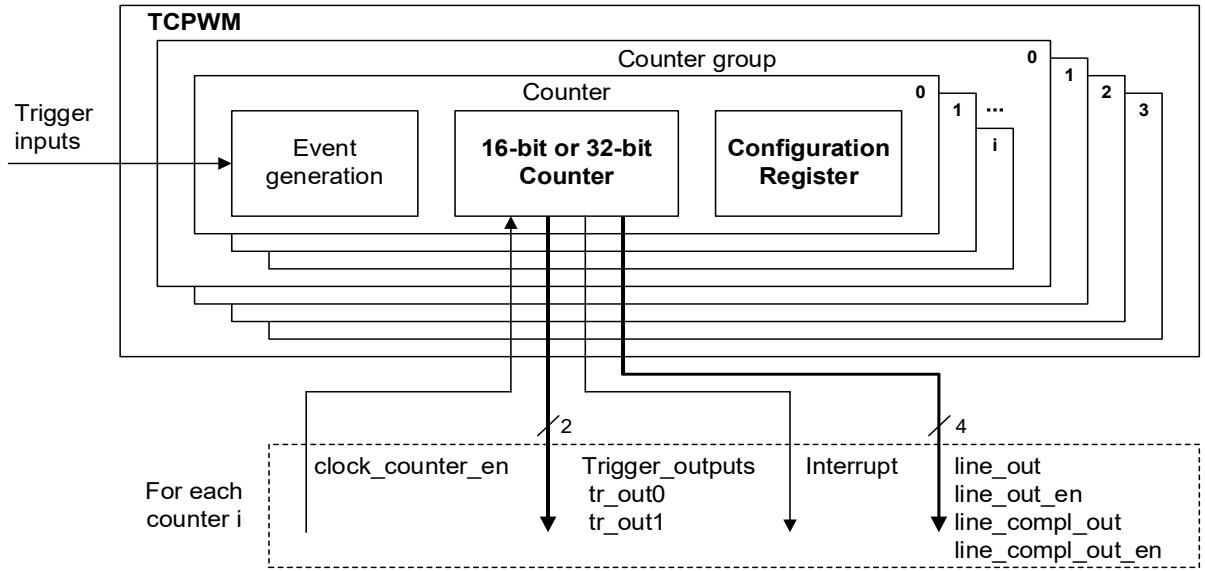
Components (9/42)

Line output

- Each counter can produce two output signals
  - Line_out
  - Line_compl_out
- These signals are supported in PWM, PWM_DT, PWM_PR, and SR functionality
- Output signal condition depends on two signals
  - Line_out_en
  - Line_compl_out_en



Hint bar

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Components (10/42)

Timer
– The timer mode is commonly used to measure the time an event occurs or to measure the time difference between two events

Event generation
– SW selects the input triggers (Reload[1], Start[2], Stop[3], Count[4])

16-bit or 32-bit counter
– Auto reload
  – CC0/1 and CC0/1_BUFF are exchanged on a CC0/1_MATCH event

Counter operation
– One-shot mode and Continuous mode
– Up/Down modes (COUNT_UP/COUNT_DOWN/COUNT_UPDN1/2)

Signal output
– TR_OUT0: OV, UN, TC, CC0_MATCH, CC1_MATCH
– TR_OUT1: OV, UN, TC, CC0_MATCH, CC1_MATCH
– Interrupt: TC, CC0_MATCH, CC1_MATCH

Hint bar

See the architecture reference manual, TCPWM (chapter 25), for additional details.

[1] Reload: Initializes and starts the counter.
[2] Start: Starts the counter.
[3] Stop: Stops the counter.
[4] Count: Count event (increments/decrements the counter).

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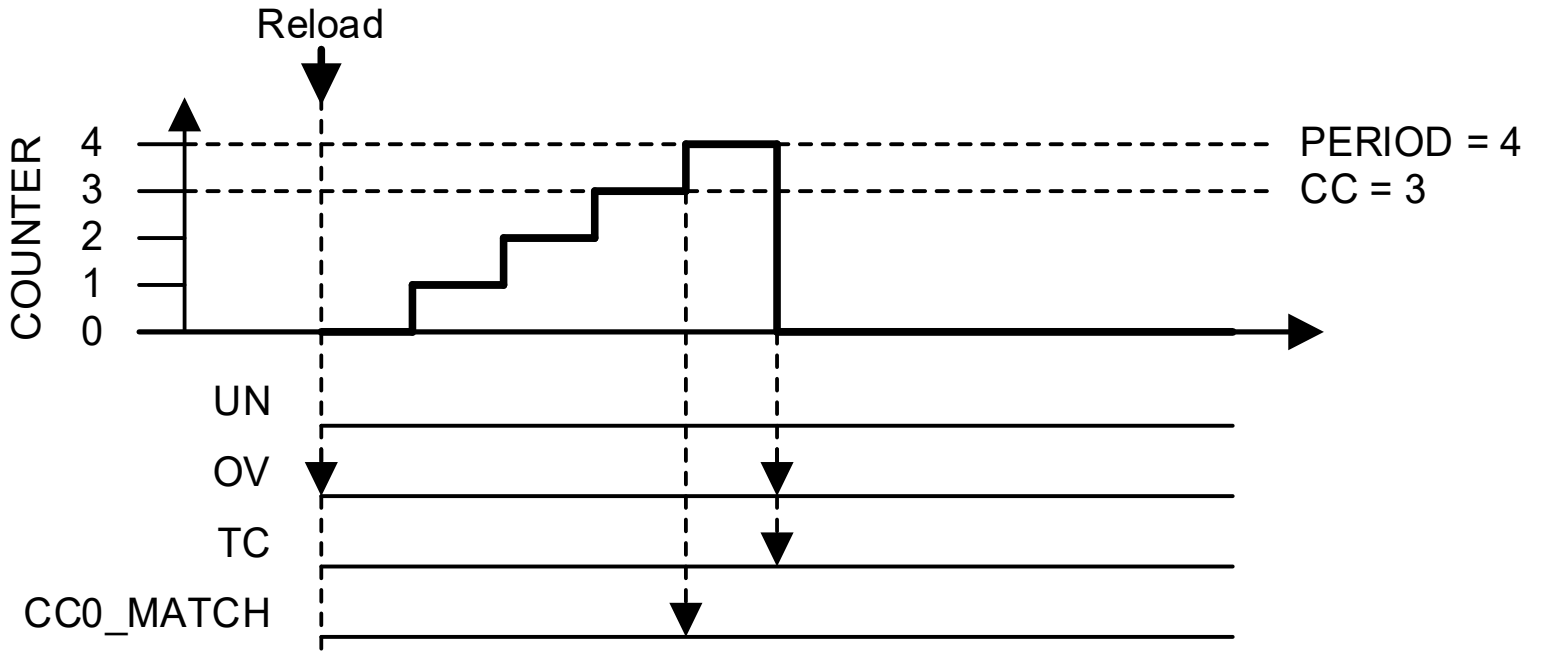
Components (11/42)

Timer operation: One-shot mode



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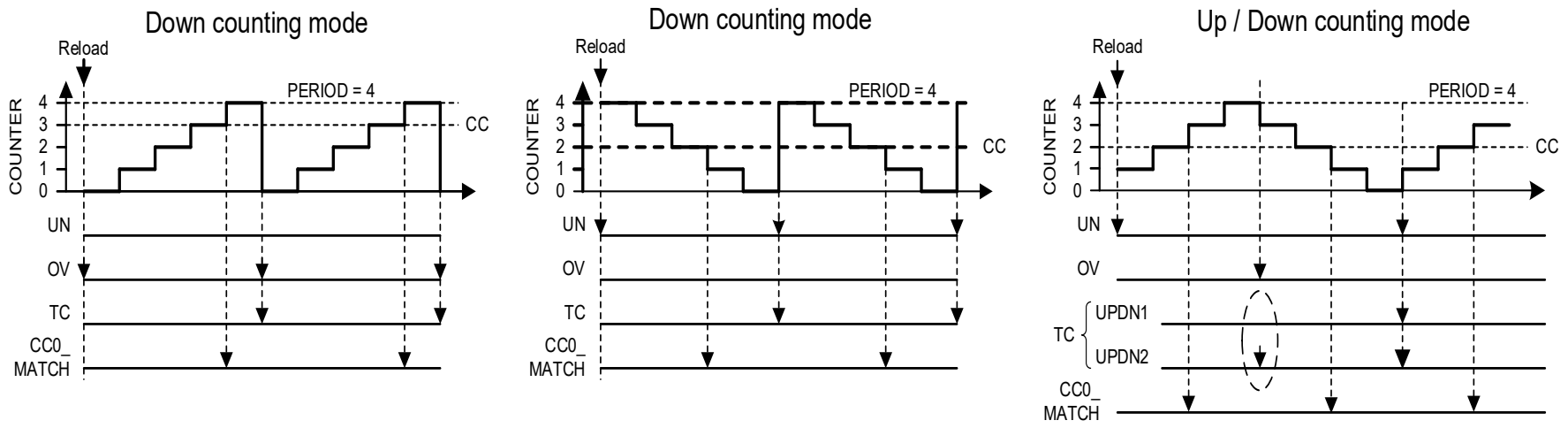
Components (12/42)

Timer operation: Up/down modes (Continuous mode)



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See the architecture reference manual, TCPWM (chapter 25), for additional details.

[1] In COUNT_UPDN2, TC is output when the counter overflows and underflows.

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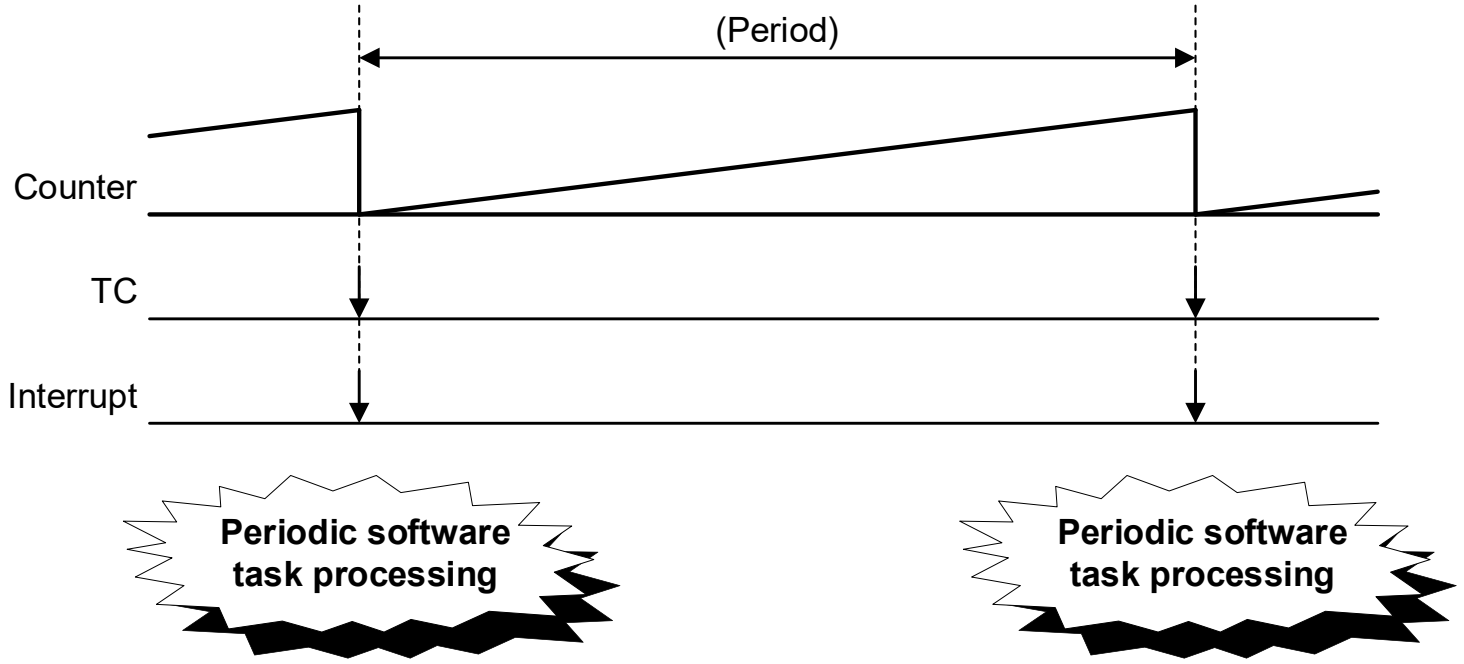
Components (13/42)

Timer use case

– Generate periodic interrupt for software task processing



Hint bar

See the architecture reference manual, TCPWM (chapter 25), for additional details.

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Components (14/42)

Capture
– Capture functionality uses the value of the counter to measure the width and period of the input pulse

Event generation
– SW selects input triggers (Reload[1], Start[2], Stop[3], Count[4], Capture0/1[5])

16-bit or 32-bit counter
– Counter operation
  – One-shot mode and Continuous mode
  – Up/Down modes (COUNT_UP/COUNT_DOWN/COUNT_UPDN1/2)

Signal output
– TR_OUT0: OV, UN, TC, CC0_MATCH, CC1_MATCH
– TR_OUT1: OV, UN, TC, CC0_MATCH, CC1_MATCH
– Interrupt: TC, CC0_MATCH, CC1_MATCH

Hint bar

See the architecture reference manual, TCPWM (chapter 25), for additional details.

[1] Reload: Initializes and starts the counter.
[2] Start: Starts the counter.
[3] Stop: Stops the counter.
[4] Count: Count event increments/decrements the counter.
[5] Capture0/1: Copies the counter value to CC0/1 and CC0/1 to CC0/1_BUFF.

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Components (15/42)

Capture operation:

Capture using Capture 0/1 signal

- Measure between falling edges of Capture 0 signal

Advantage

- Provides the following measurement functions:
  - H pulse width/L pulse width
  - Rising cycle/falling cycle
  - Edge-to-edge measurement

Use case

- Measure the input pulse period (vehicle speed pulse)

Hint bar

See the architecture reference manual, TCPWM Capture mode (section 25.3.2), for additional details.

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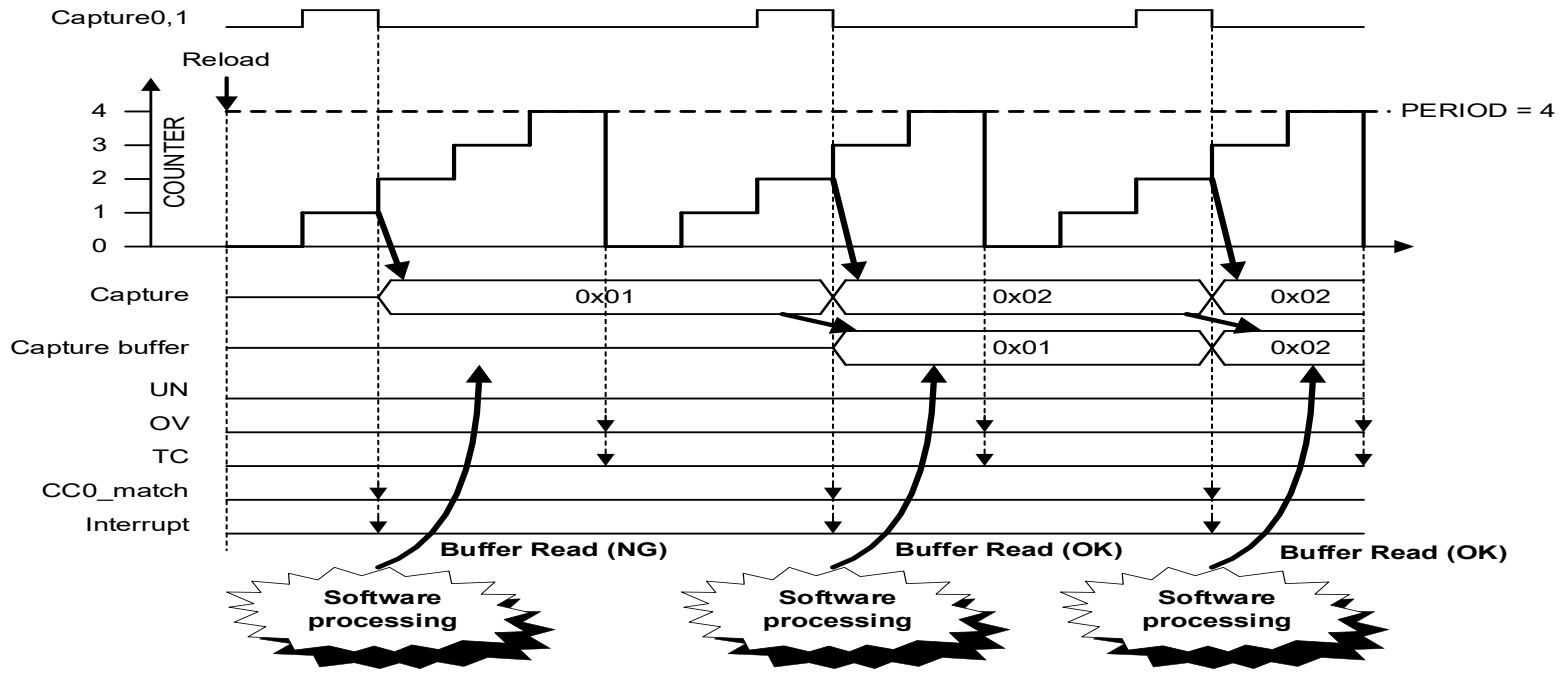
Components (16/42)

Capture operation



Hint bar

See the architecture reference manual, TCPWM Capture mode (section 25.3.2), for additional details.

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Components (17/42)

Quadrature decoder
– The Quadrature decoder has four range modes and four encoding modes

Range modes
– QUAD_RANGE0
– QUAD_RANGE0_CMP
– QUAD_RANGE1_CMP
– QUAD_RANGE1_CAPT

Encoding modes
– X1 encoding
– X2 encoding
– X4 encoding
– Up/down rotary count mode

Each range mode has:
– Four encoding modes
– Different input trigger for each range mode

Hint bar

See the architecture reference manual, TCPWM Quadrature decoder mode (section 25.3.3), for additional details.

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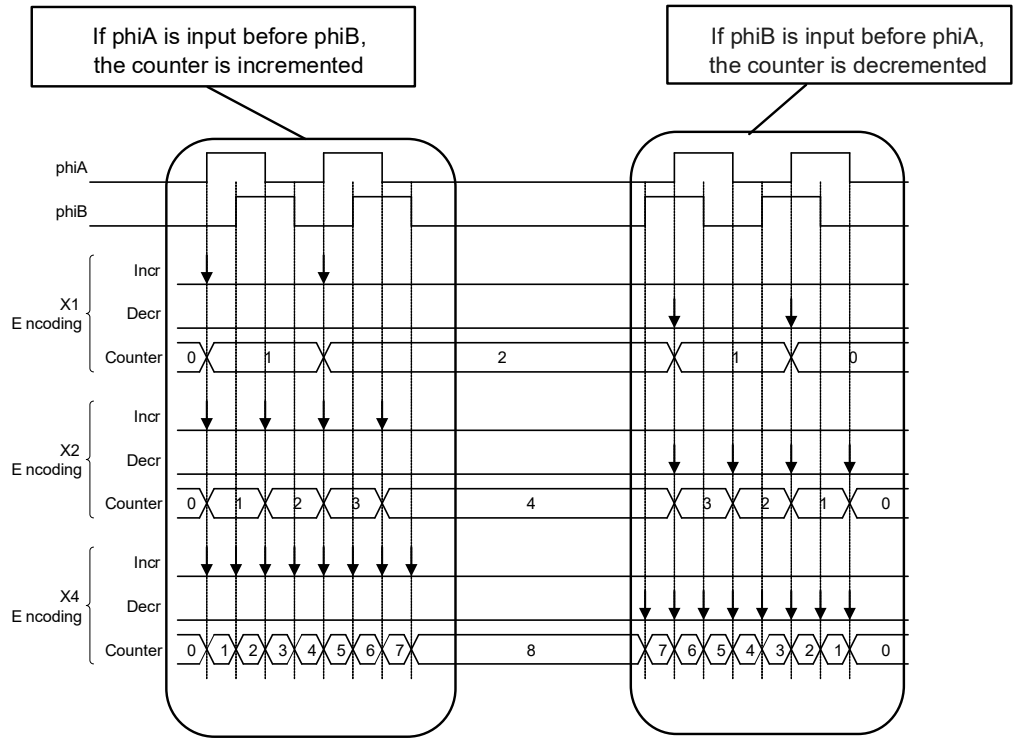
Components (18/42)

Encoding modes

– X1, X2, and X4 encoding modes



Hint bar

See the architecture reference manual, TCPWM Quadrature decoder mode (section 25.3.3), for additional details.

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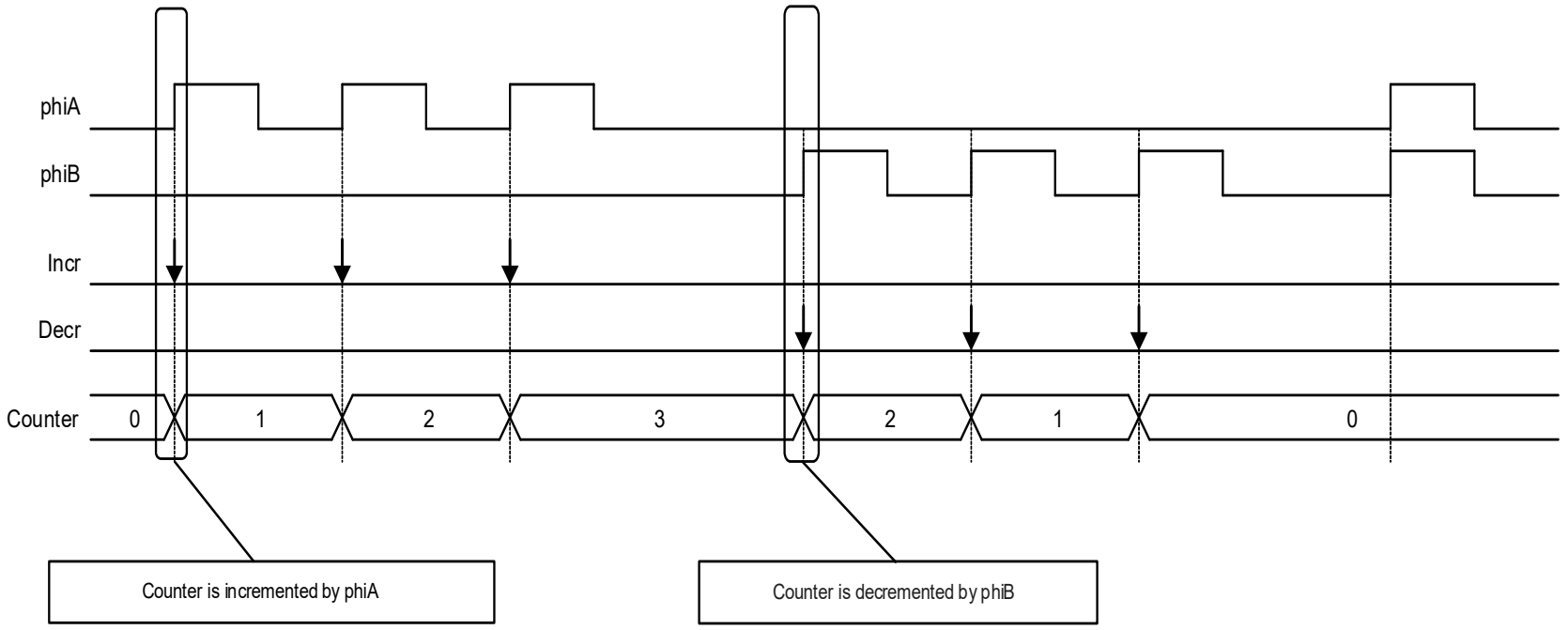
Components (19/42)

Encoding modes

– Up / down rotary count mode



Hint bar

See the architecture reference manual, TCPWM Quadrature decoder mode (section 25.3.3), for additional details.

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Components (20/42)

Range modes

Range modes supported	Counter range	Counter initial value	Copy the counter value[1]	Compare event[1]	Capture event[1]
QUAD_RANGE0	0x0000 to 0xFFFF/0xFFFFFFFF	0x8000	✓	–	–
QUAD_RANGE0_CMP	0x0000 to 0xFFFF/0xFFFFFFFF	0x8000	✓	✓	–
QUAD_RANGE1_CMP	0x0000 to PERIOD	0x0000	–	✓	–
QUAD_RANGE1_CAPT[2]	0x0000 to PERIOD	0x0000	–	✓	✓

Advantage

– Output of the quadrature encoder can be decoded without external circuits

Hint bar

See the architecture reference manual, TCPWM (chapter 25), for additional details.

[1] For details about each item, see the respective time chart on the following pages - 30, 32, 34, 36.
[2] QUAD_RANGE1_CAPT mode provides the same functionality as the QUAD_RANGE1_CMP; the only difference is that capture functions are available instead of compare functions.

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Components (21/42)

QUAD_RANGE0

Event generation

– SW selects the input triggers (index[1], phiB[2], Stop[3], phiA[4])

16-bit or 32-bit counter

– Counter operation
  – Four encoding modes can be used (X1, X2, X4, and up/down rotary count mode)

Signal output

– TR_OUT0: TC, CC0_MATCH
– TR_OUT1: TC, CC0_MATCH
– Interrupt: TC, CC0_MATCH

Hint bar

See the architecture reference manual, TCPWM (chapter 25), for additional details.

[1] index: Initializes and starts the counter.
[2] phiB: Quadrature phiB input.
[3] Stop: Stops the quadrature functionality.
[4] phiA: Quadrature phiA input.

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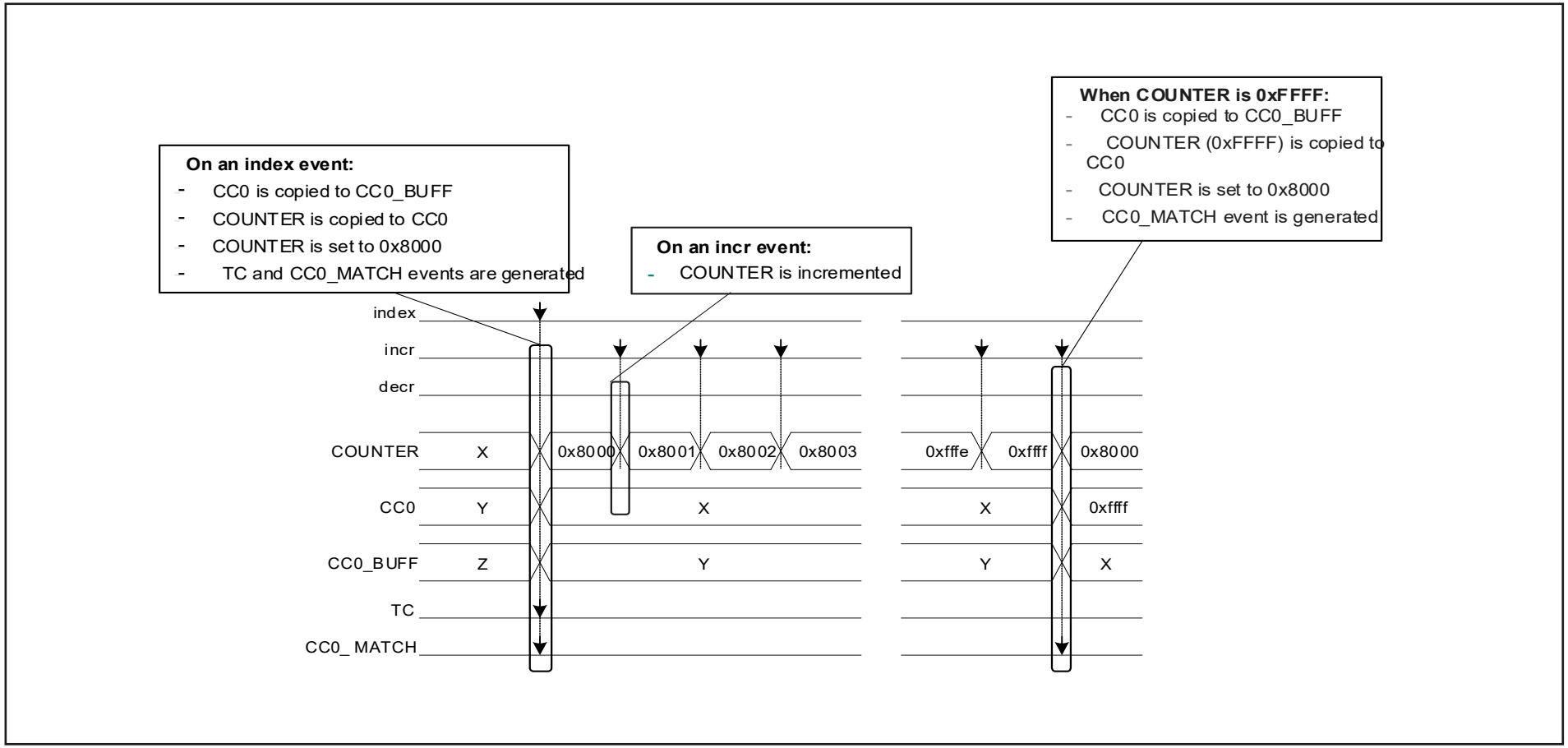
Components (22/42)

QUAD_RANGE0 operation

– Operation example (X1 encoding mode)



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See the architecture reference manual, TCPWM Quadrature QUAD_RANGE0 mode (section 25.3.3.1) for additional details.

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Components (23/42)

QUAD_RANGE0_CMP

Event generation

– SW selects the input triggers (index[1], phiB[2], Stop[3], phiA[4], second index[5])

16-bit or 32-bit counter

– Counter operation
  – Four encoding modes can be used (X1, X2, X4, and up/down rotary count mode)

Signal output

– TR_OUT0: TC, CC0_MATCH, CC1_MATCH
– TR_OUT1: TC, CC0_MATCH, CC1_MATCH
– Interrupt: TC, CC0_MATCH, CC1_MATCH

Hint bar

See the architecture reference manual, TCPWM (chapter 25), for additional details.

[1] index: Initializes and starts the counter.
[2] phiB: Quadrature phiB input.
[3] Stop: Stops the quadrature functionality.
[4] phiA: Quadrature phiA input.
[5] Second index: This event acts as a second quadrature index input. It has the same function as the index event.

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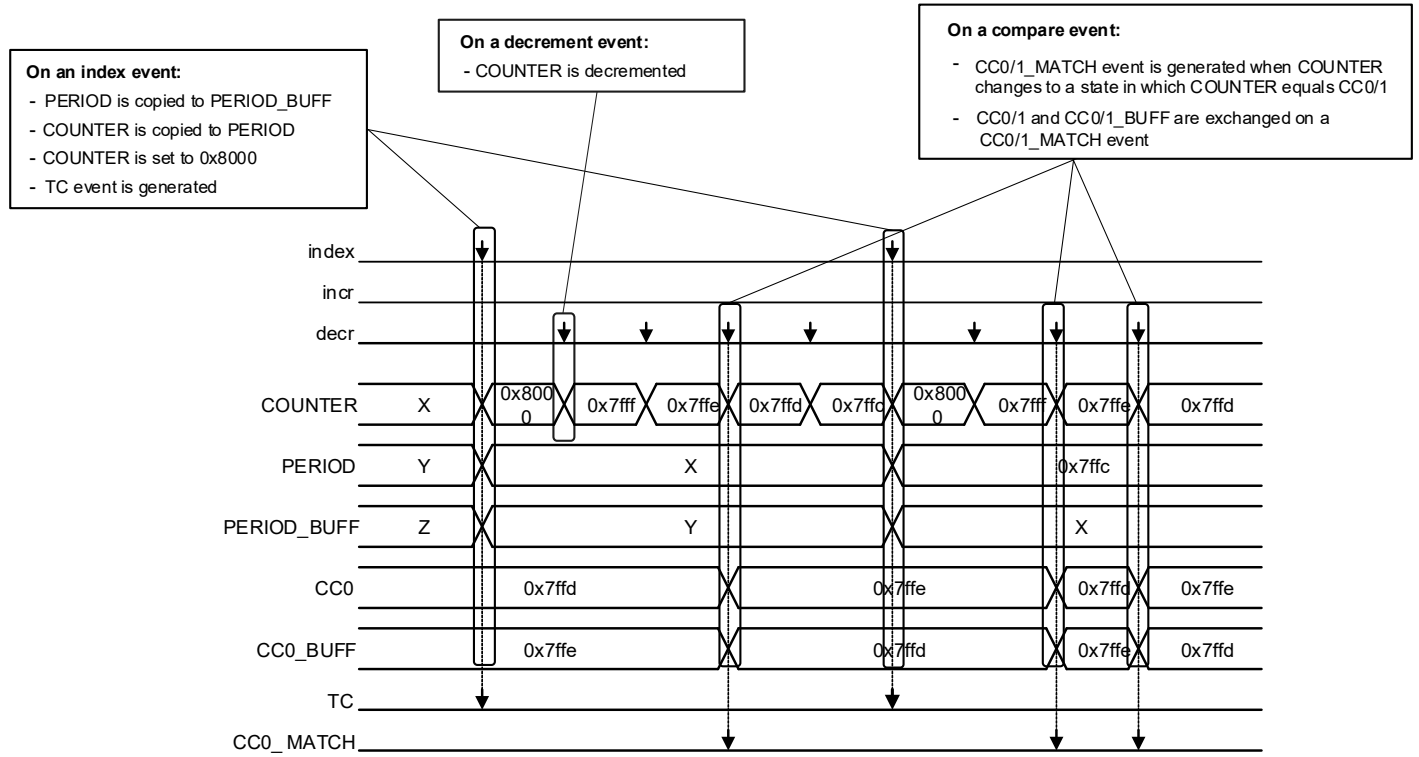
Components (24/42)

QUAD_RANGE0_CMP operation

– Operation example (X1 encoding mode)



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Components (25/42)

QUAD_RANGE1_CMP

Event generation

– SW selects the input triggers (index[1], phiB[2], Stop[3], phiA[4])

16-bit or 32-bit counter

– Counter operation
  – Four encoding modes can be used (X1, X2, X4, and up/down rotary count mode)

Signal output

– TR_OUT0: OV, UN, TC, CC0_MATCH, CC1_MATCH
– TR_OUT1: OV, UN, TC, CC0_MATCH, CC1_MATCH
– Interrupt: TC, CC0_MATCH, CC1_MATCH

Hint bar

See the architecture reference manual, TCPWM (chapter 25), for additional details.

[1] index: Initializes and starts the counter.
[2] phiB: Quadrature phiB input.
[3] Stop: Stops the quadrature functionality.
[4] phiA: This event acts as a quadrature phiA input.

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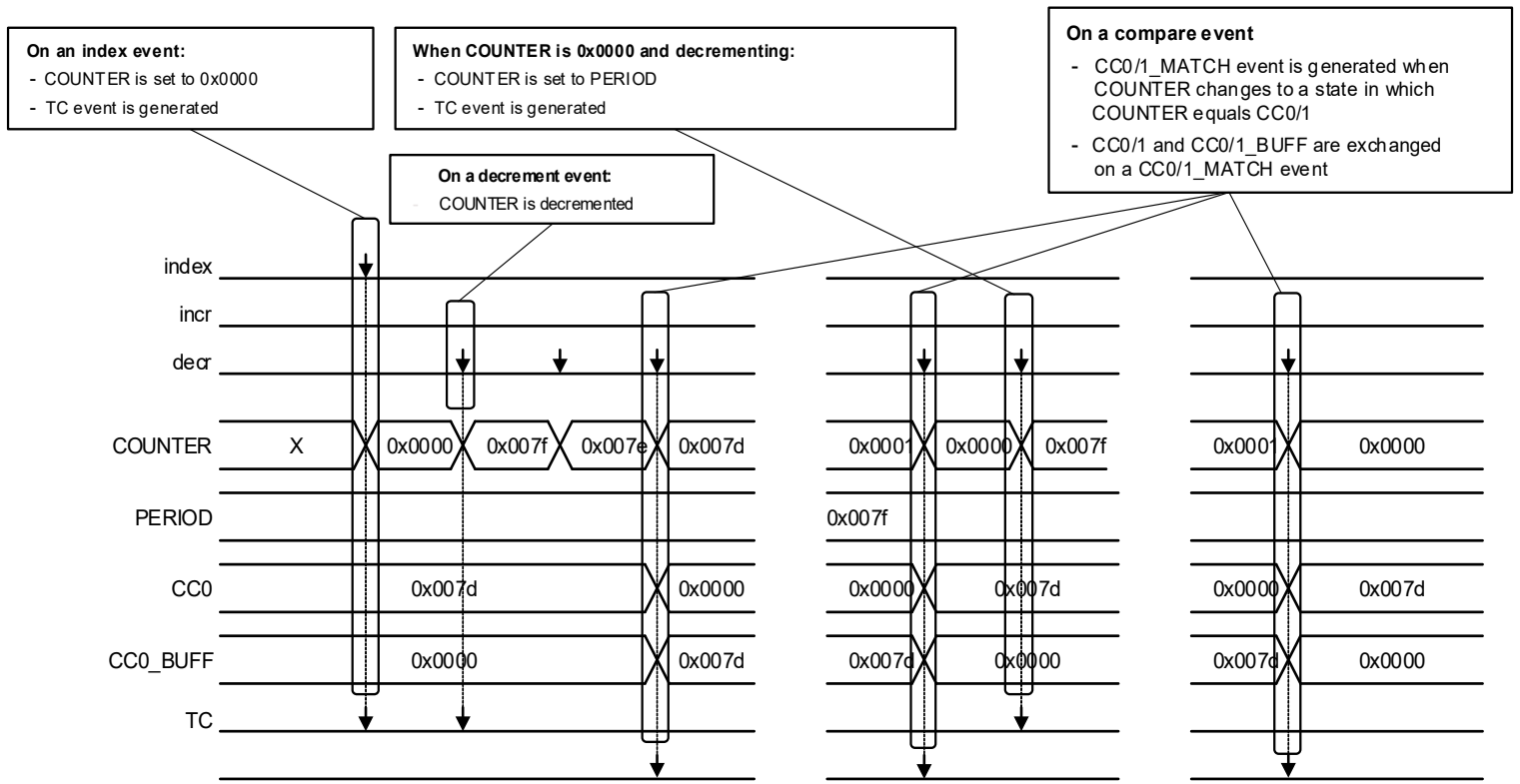
Components (26/42)

QUAD_RANGE1_CMP operation

– Operation example (X1 encoding mode)



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Components (27/42)

QUAD_RANGE1_CAPT

Event generation

- SW selects the input triggers (index[1], phiB[2], Stop[3], phiA[4], Capture0[5]/1[6])

16-bit or 32-bit counter

- Counter operation
  - Four encoding modes can be used (X1, X2, X4, and up/down rotary count mode)

Signal output

- TR_OUT0: OV, UN, TC, CC0_MATCH, CC1_MATCH
- TR_OUT1: OV, UN, TC, CC0_MATCH, CC1_MATCH
- Interrupt: TC, CC0_MATCH, CC1_MATCH

Hint bar

See the architecture reference manual, TCPWM (chapter 25), for additional details.

[1] index: Initializes and starts the counter.
[2] phiB: Quadrature phiB input.
[3] Stop: Stops the quadrature functionality.
[4] phiA: This event acts as a quadrature phiA input.
[5] Capture0: Capture event to copy COUNTER to CC0, CC0 to CC0_BUFF.
[6] Capture1: Second capture event to copy COUNTER to CC1, CC1 to CC1_BUFF.

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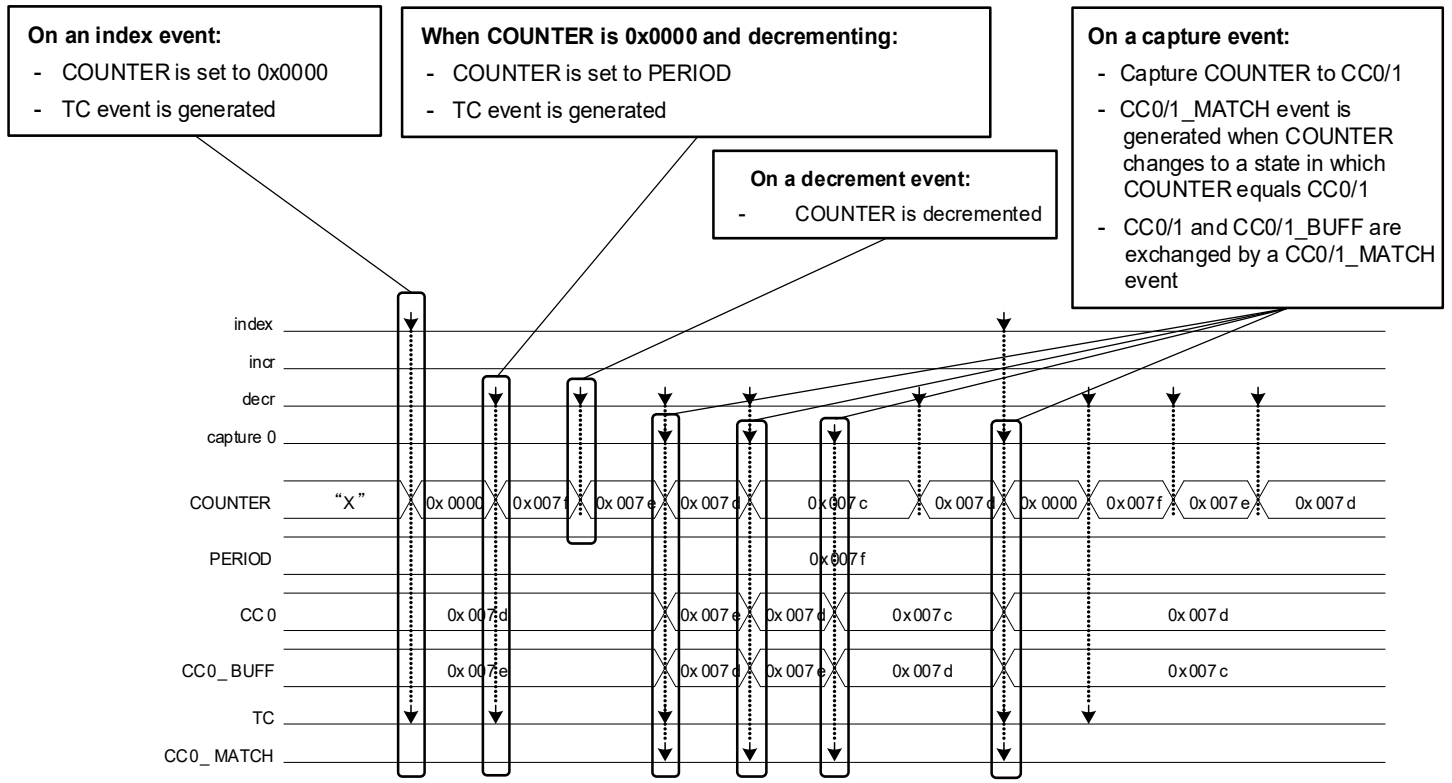
Components (28/42)

QUAD_RANGE1_CAPT operation

– Operation example (X1 encoding mode)



Hint bar

See the architecture reference manual, TCPWM (chapter 25), for additional details.

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Components (29/42)

PWM
– The comparison output is a PWM signal whose period depends on the period register value and whose duty cycle depends on the compare and period register values

Event generation
– SW selects the input triggers (Reload[1], Start[2], Stop/Kill[3], Count[4], Capture0[5], Stop1/Kill1[6])

16-bit or 32-bit counter
– Auto reload
  – CC0/1 and CC0/1_BUFF are exchanged on a CC0/1_MATCH event
  – PERIOD and PERIOD_BUFF are exchanged on a switch event and TC event
– Counter operation
  – One-shot mode and Continuous mode
  – Up/Down modes (COUNT_UP/COUNT_DOWN/COUNT_UPDN1/2)

Signal output
– TR_OUT0: OV, UN, TC, CC0_MATCH, CC1_MATCH, LINE_OUT[7]
– TR_OUT1: OV, UN, TC, CC0_MATCH, CC1_MATCH, LINE_OUT[7]
– Interrupt: TC, CC0_MATCH, CC1_MATCH

Hint bar

See the architecture reference manual, TCPWM (chapter 25), for additional details.

[1] Reload: Sets the counter value and starts the counter.
[2] Start: Starts the counter.
[3] Stop/kill: Stops the counter. Different stop/kill modes exist.
[4] Count: Count event incr/decr the counter.
[5] Capture0: This event acts as a switch event.
[6] Stop1/kill1: This event acts as a second stop/kill event.
[7] LINE_OUT can be output with inverted polarity.

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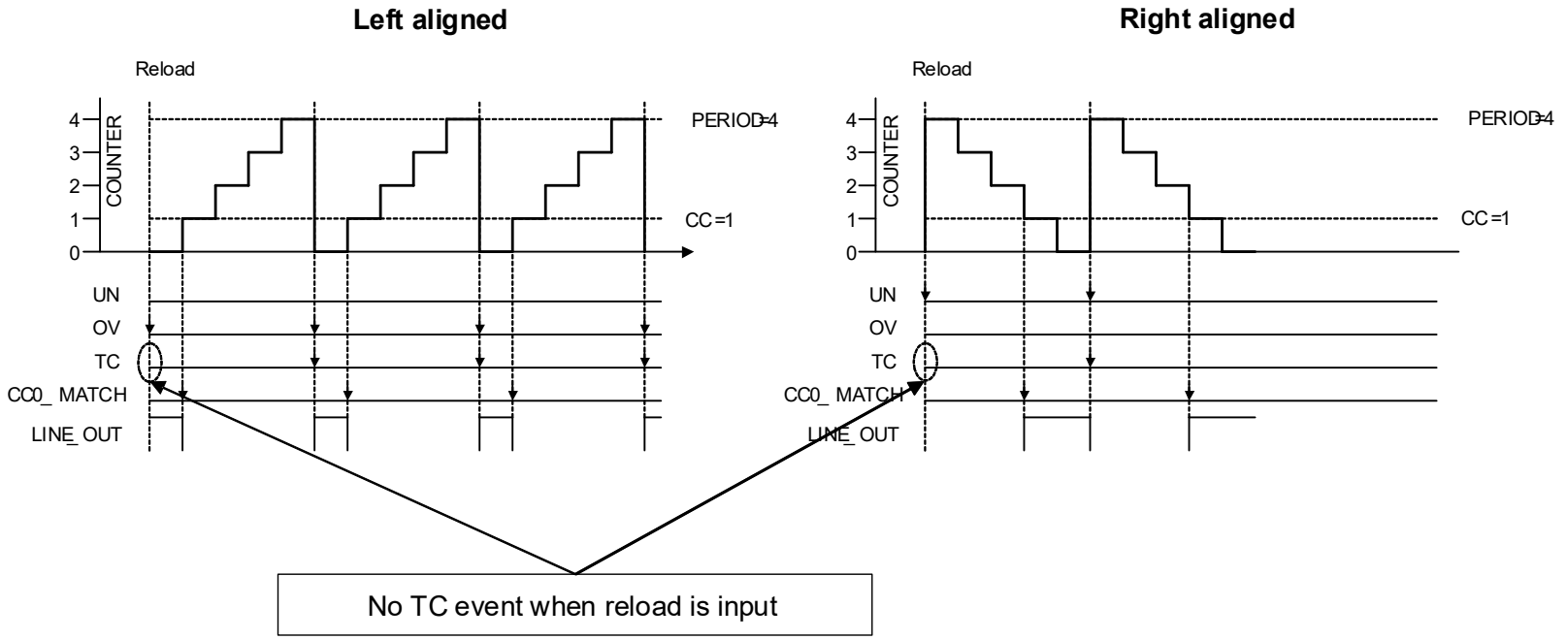
Components (30/42)

PWM operation

– Operation example (Continuous mode, COUNT_UP/DOWN)



Hint bar

See the architecture reference manual, TCPWM (chapter 25), for additional details.

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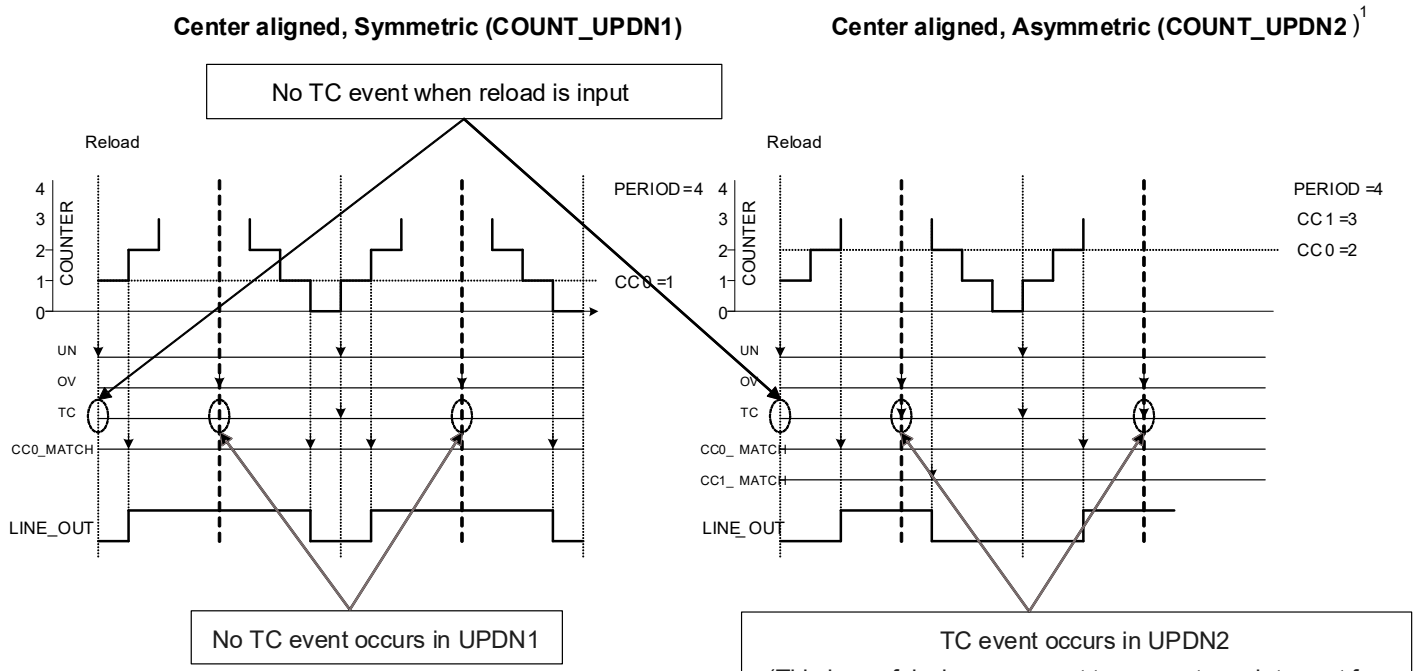
Components (31/42)

PWM operation

– Operation example (Continuous mode)



Hint bar

See the architecture reference manual, TCPWM (chapter 25), for additional details.

[1] Asymmetric PWM signals can be generated using the COUNT_UPDN2 mode.

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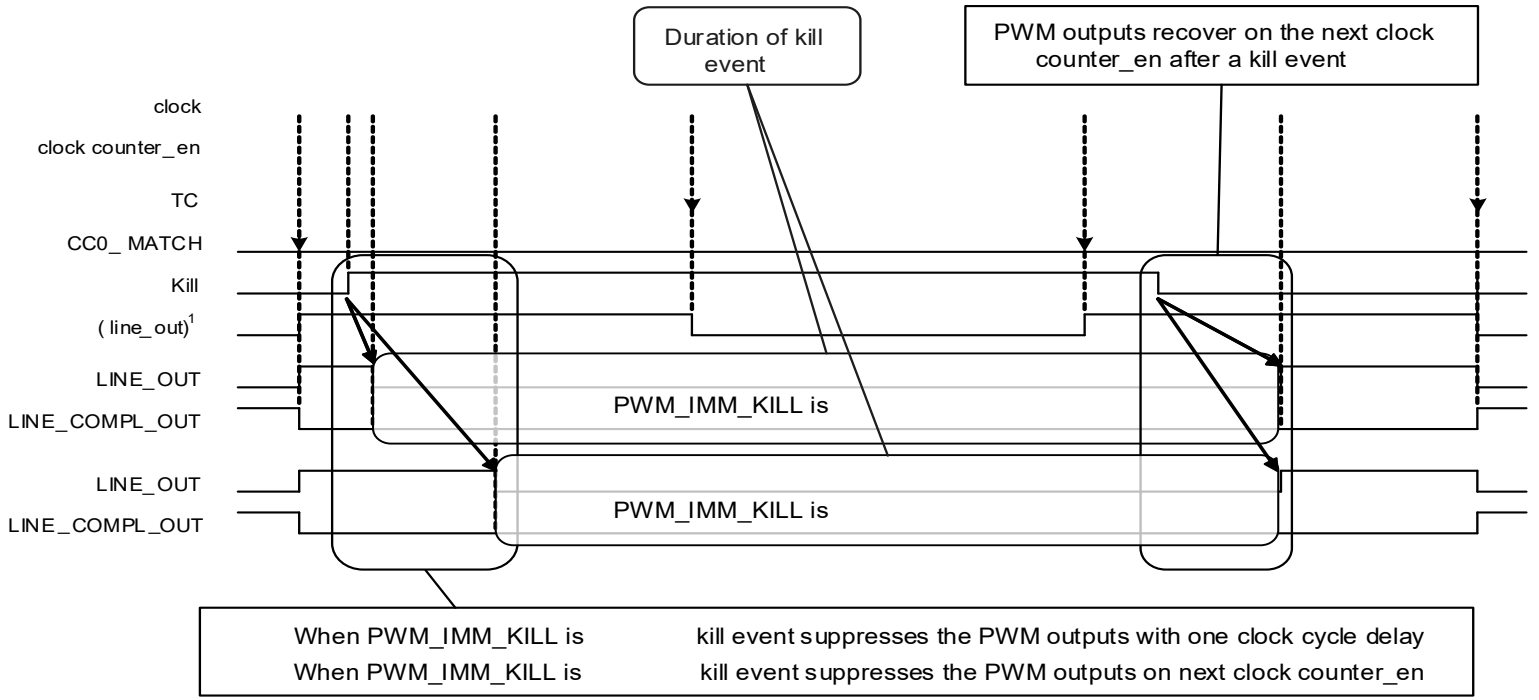
Components (32/42)

PWM operation

Operation example:

– Kill event



[1] line_out is the signal when the kill event does not occur.

Hint bar

See the architecture reference manual, TCPWM (chapter 25), for additional details.

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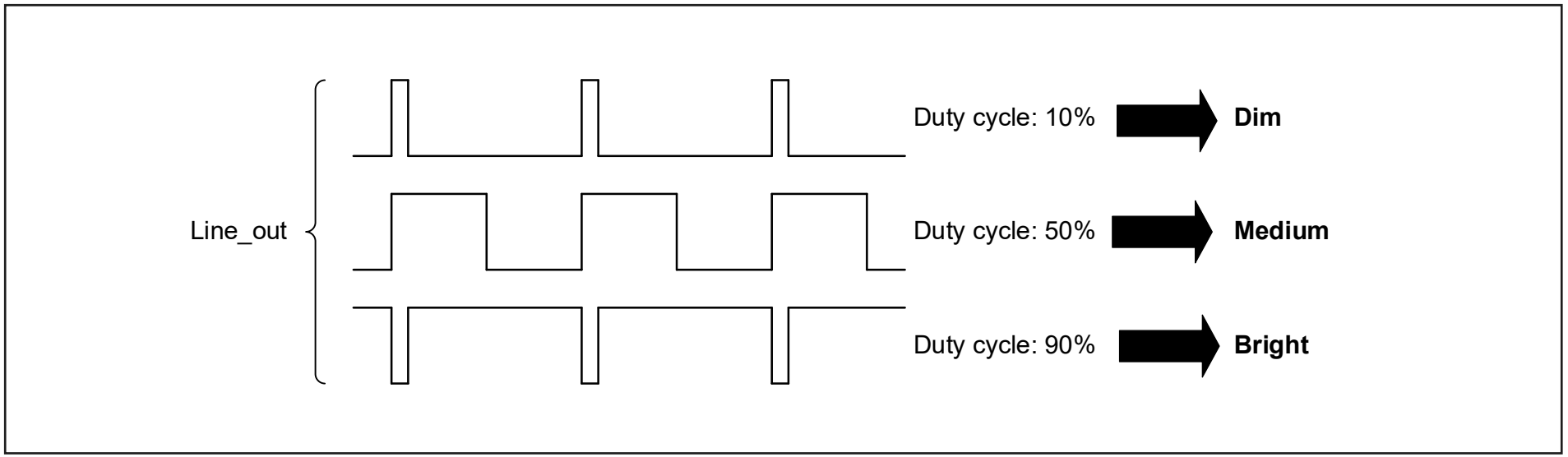
Components (33/42)

PWM use case

Control LED brightness:

– Control brightness of the LED with duty cycle of the PWM signal



– The line output signal can be output with 0% and 100% duty, except in the following cases:
  – COUNT_UP mode:
    – To get 100% duty cycle, CC0 must be set to a value higher than the period. If period is 0xFFFF (for 16-bit counter) or 0xFFFFFFFF (for 32-bit counter), 100% duty cycle cannot be achieved
  – COUNT_DOWN mode:
    – To get 0% duty cycle, CC0 must be set to a value higher than the period. If period is 0xFFFF (for 16-bit counter) or 0xFFFFFFFF (for 32-bit counter), 0% duty cycle cannot be achieved

Hint bar

See the architecture reference manual, TCPWM (chapter 25), for additional details.

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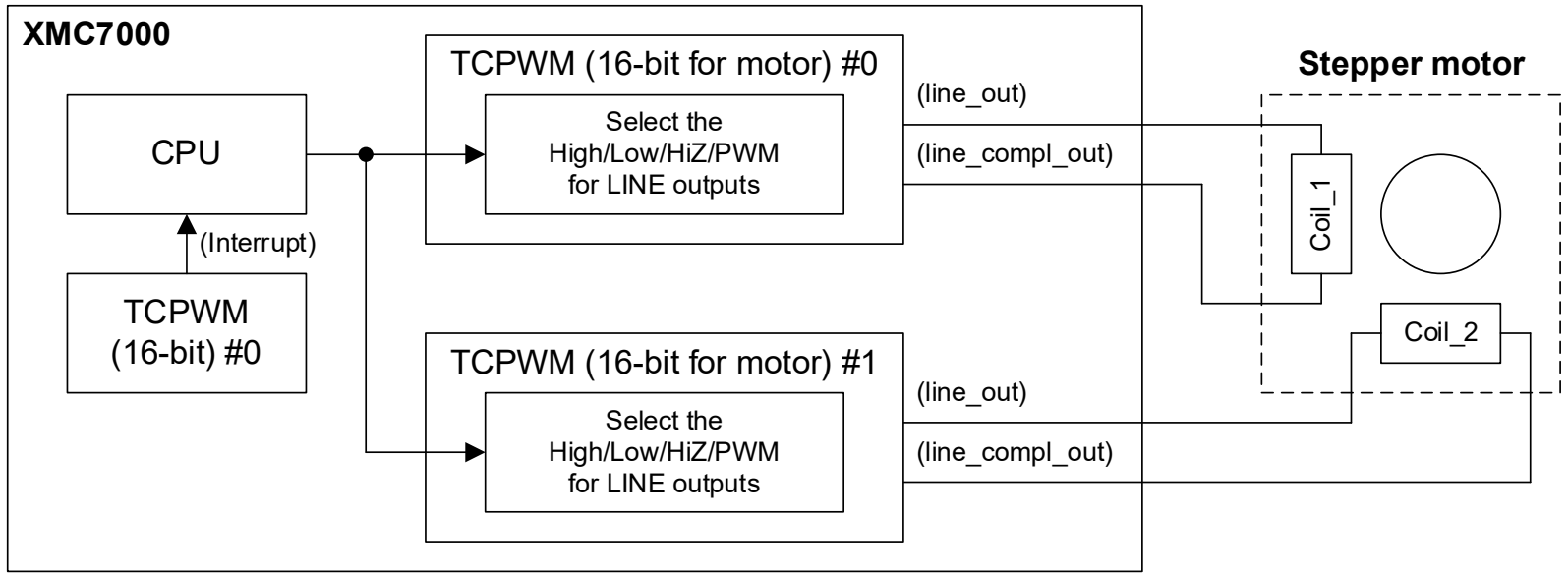
Components (34/42)

PWM use case

Stepper Motor Control (SMC)

- TCPWM supports **PWM Output Selection** for stepper motors, including micro stepper control
- TCPWM (16-bit) #0: Generates the interrupt signal for motor control period
- TCPWM (16-bit for Motor) #0/1: Generates the SMC signals



Note: XMC7000 does not contain high current GPIO_SMC port pins to drive Stepper motor directly.

Hint bar

See the architecture reference manual, TCPWM (chapter 25), for additional details.

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Components (35/42)

PWM_DT
– PWM_DT functionality is the same as PWM functionality, except that dead time can be inserted and clock pre-scaling is not provided

Event generation
– SW selects the input triggers (Reload[1], Start[2], Stop/kill[3], Count[4], Capture0[5], Stop1/kill1[6])

16-bit or 32-bit counter
– Auto reload
  – CC0/1 and CC0/1_BUFF are exchanged on a CC0/1_MATCH event
  – PERIOD and PERIOD_BUFF are exchanged on a switch event and TC event
– Counter operation
  – One-shot mode and Continuous mode
  – Up/Down modes (COUNT_UP/COUNT_DOWN/COUNT_UPDN1/2)
– Dead time insertion
  – Range is 0 to 65535 counter clock cycles (16-bit, only for Counter Group 2)
  – Range is 0 to 255 (8-bit)

Signal output
– TR_OUT0: OV, UN, TC, CC0_MATCH, CC1_MATCH, LINE_OUT[7]
– TR_OUT1: OV, UN, TC, CC0_MATCH, CC1_MATCH, LINE_OUT[7]
– Interrupt: TC, CC0_MATCH, CC1_MATCH

Hint bar

See the architecture reference manual, TCPWM (chapter 25), for additional details.

[1] Reload: Sets the counter value and starts the counter.
[2] Start: Starts the counter.
[3] Stop/kill: Stops the counter. Different stop/kill modes exist.
[4] Count: Count event incr/decr the counter.
[5] Capture0: This event acts as a switch event.
[6] Stop1/kill1: This event acts as a second stop/kill event.
[7] LINE_OUT can be output with inverted polarity.

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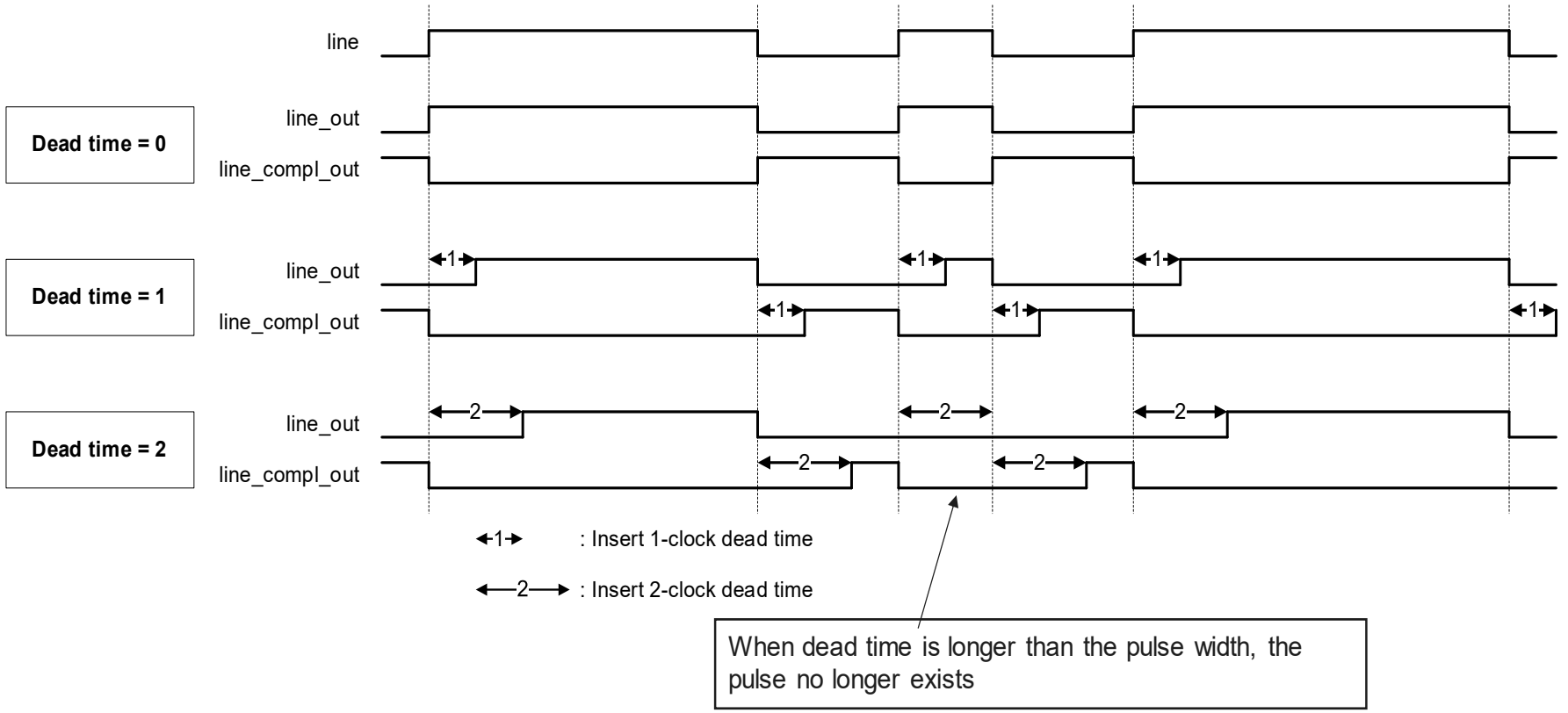
Components (36/42)

Dead time insertion

Example: Dead time insertion: 0-clock, 1-clock, 2-clock

– To prevent a short circuit due to switching element delay, insert the dead time



Hint bar

See the architecture reference manual, TCPWM (chapter 25), for additional details.

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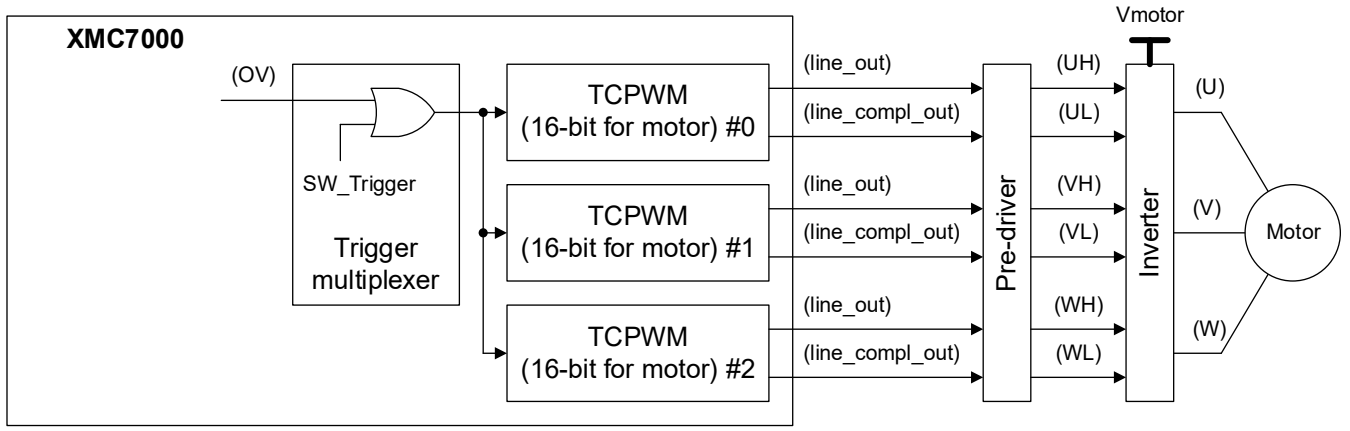
Components (37/42)

PWM_DT use case

- Three-phase motor control:
  - By using three TCPWMs, a three-phase motor can be controlled using a PWM signal with dead time
  - TCPWM (16 bit) #0: Generates the motor control period
  - TCPWM (16 bit for motor) #0/1/2: Generates the motor control signals
- Three TCPWMs can be activated simultaneously using overflow of TCPWM or SW command of trigger multiplexer



[1] Reload: Sets the counter value and starts the counter.
[2] Start: Starts the counter.
[3] Stop/kill: Stops the counter. Different stop/kill modes exist.
[4] Count: Count event incr/decr the counter.
[5] Capture0: This event acts as a switch event.
[6] Stop1/kill1: This event acts as a second stop/kill event.
[7] LINE_OUT can be output with inverted polarity.

Hint bar

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Components (38/42)

PWM_PR

The PWM PR functionality changes the counter value using the linear feedback shift register (LFSR)

Event generation

- SW selects the input triggers (Reload[1], Start[2], Stop/kill[3], Capture0[4]/1[5])

16-bit or 32-bit counter

- Auto reload
  - CC0/1 and CC0/1_BUFF are exchanged on a CC0/1_MATCH event
  - PERIOD and PERIOD_BUFF are exchanged on a switch event and TC event
  - LINE_SEL and LINE_SEL_BUFF are exchanged on a switch event and TC event
- Counter operation
  - One-shot mode and Continuous mode
- Generate a pseudo-random number sequence
- The generated signal has different frequency/noise characteristics than a regular PWM signal
- Programmable LFSR length

Signal output

- TR_OUT0: OV, UN, TC, CC0_MATCH, CC1_MATCH, LINE_OUT[6]
- TR_OUT1: OV, UN, TC, CC0_MATCH, CC1_MATCH, LINE_OUT[6]
- Interrupt: TC, CC0_MATCH, CC1_MATCH

[1] Reload: Same behavior as start event.
[2] Start: Starts the counter.
[3] Stop/kill: Stops the counter. Different stop/kill modes exist.
[4] Capture0: Switch event.
[5] Capture1: Second stop/kill event.
[6] LINE_OUT can be output with inverted polarity.

Hint bar

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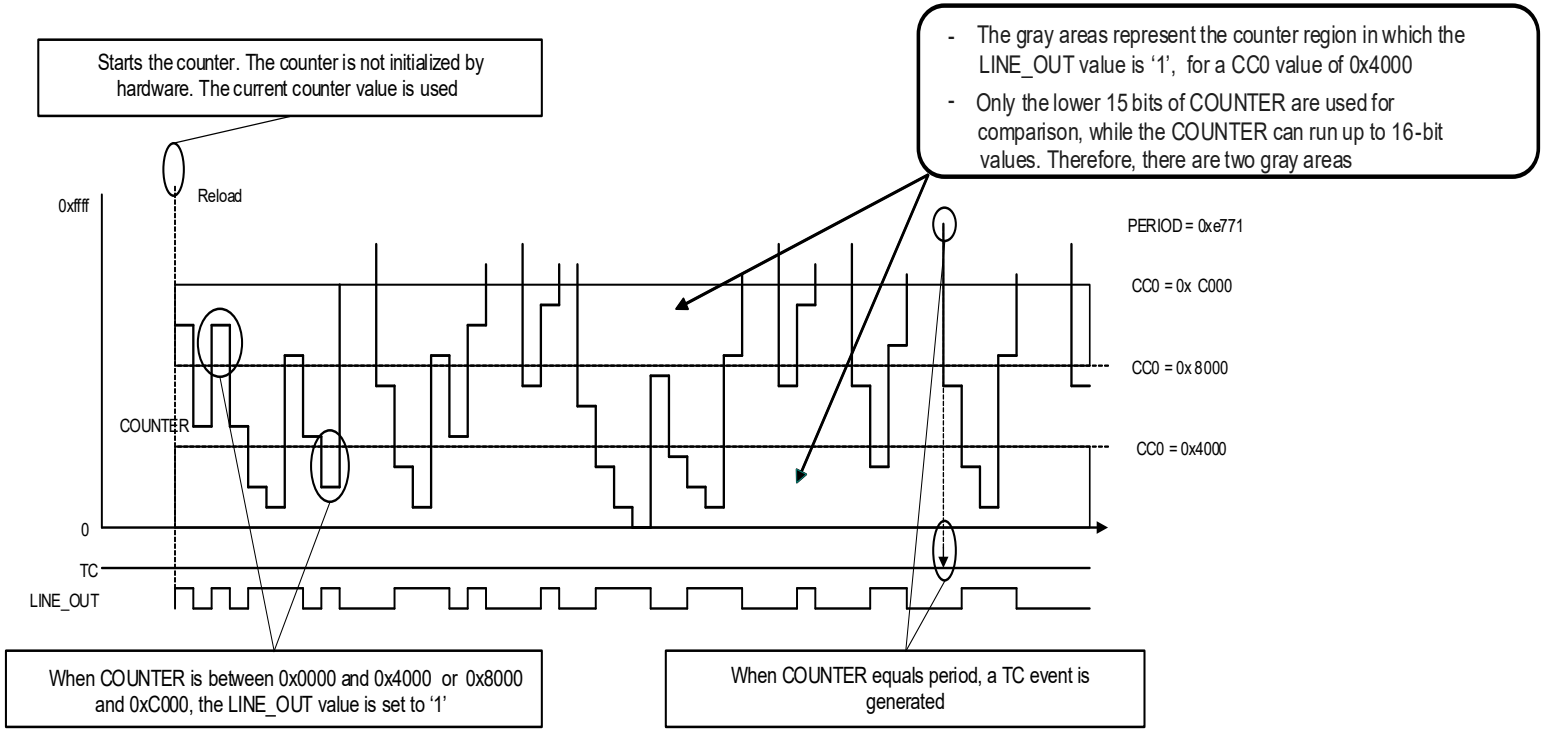
Components (39/42)

PWM_PR operation

Operation example: Continuous mode, generate a pseudo-random number



Hint bar

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Components (40/42)

Shift Register
– Shift Register (SR) functionality shifts the counter value to the right

Event generation
– SW selects the input triggers (Reload[1], Start[2], Stop[3], Shift[4], Serial-in[5])

16-bit or 32-bit counter
– Auto reload
  – CC0/1 and CC0/1_BUFF are exchanged on a CC0/1_MATCH event
– Counter shift
  – The counter value is shifted to the right

Signal output
– TR_OUT0: CC0_MATCH, CC1_MATCH, LINE_OUT[6]
– TR_OUT1: CC0_MATCH, CC1_MATCH, LINE_OUT[6]
– Interrupt: CC0_MATCH, CC1_MATCH

Hint bar

See the architecture reference manual, TCPWM (chapter 25), for additional details.

[1] Reload: Sets the counter value to “0” and starts the counter shift operation.
[2] Start: Starts the counter shift operation.
[3] Stop: Stops the counter.
[4] Shift: Shifts the counter in right direction.
[5] Serial-in: Serial input to the MSB of the counter.
[6] LINE_OUT can be output with inverted polarity.

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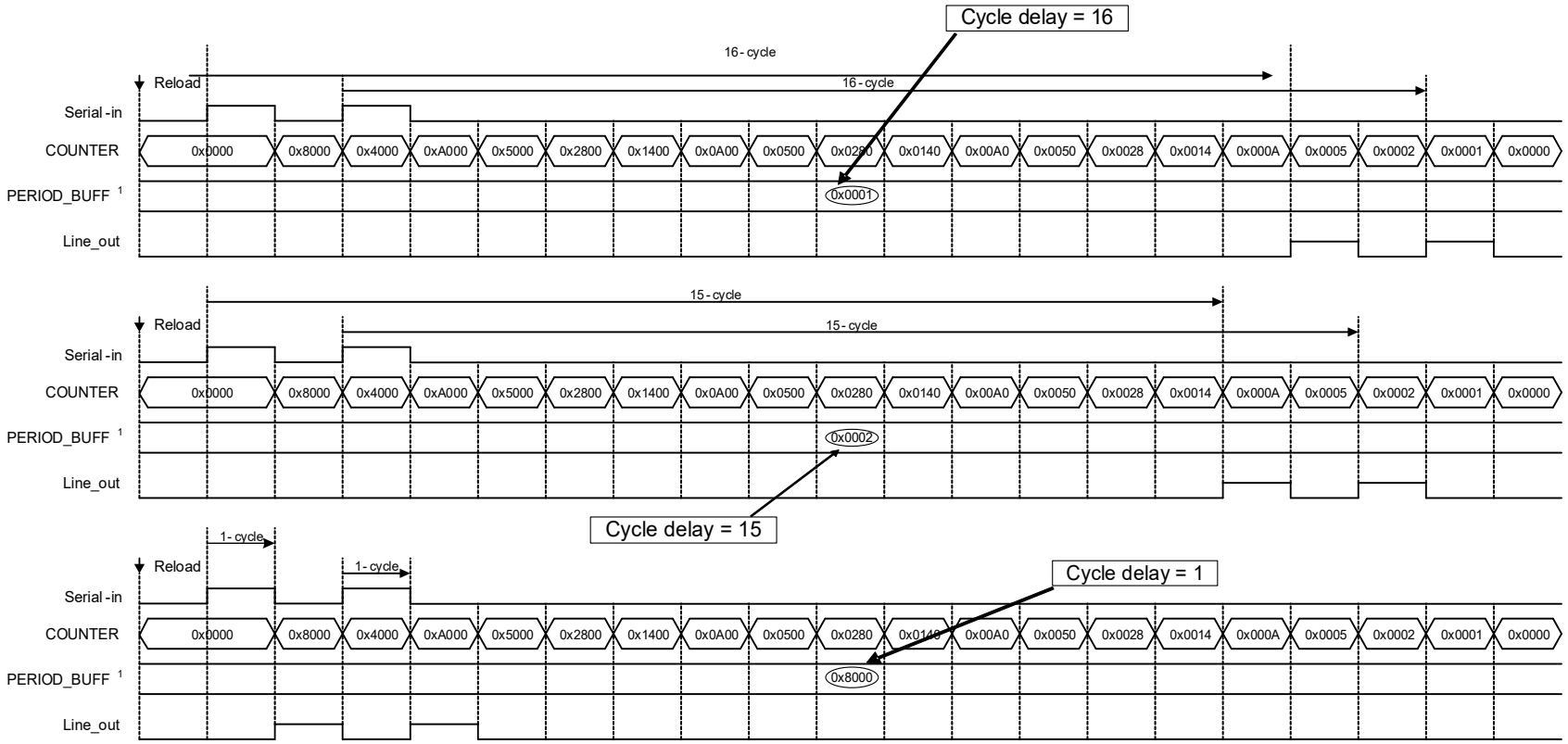
Components (41/42)

SR operation

– Operation example: Counter shift to the right



Hint bar

See the architecture reference manual, TCPWM (chapter 25), for additional details.

[1] The set value of the PERIOD_BUFF refers to the delay cycle number of the shift register. The period buffer needs to be set so that only one of the delay taps is valid.

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Components (42/42)

Debug mode

TCPWM counters support Debug mode

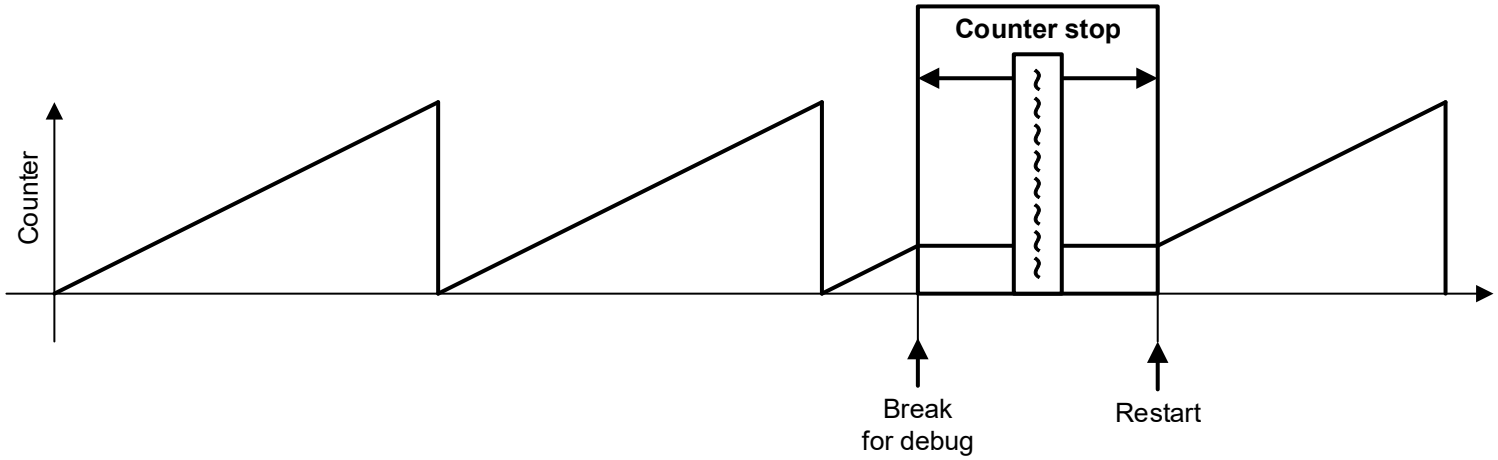
– Can be configured per counter if counter operation continues or pauses in debug state

Use case

– Counter operation is paused

Advantage

– Even if you break for debugging, you can debug with the same counter operation as the actual operation



Hint bar

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Revision history

Document revision	Date	Description of change
**	2022-05-17	Initial release.
*A	2026-01-05	Migrated to the latest empower training presentation template.

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