

XMC7000 SDHC host controller

Customer training workshop (CTW)

January 2026

public

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Target products

Target product list for this training material:

Family category	Series	Code flash memory size
XMC7200	XMC7200-8M	Up to 8384 KB
XMC7100	XMC7100-4M	Up to 4160 KB

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XMC7200 - 8M family



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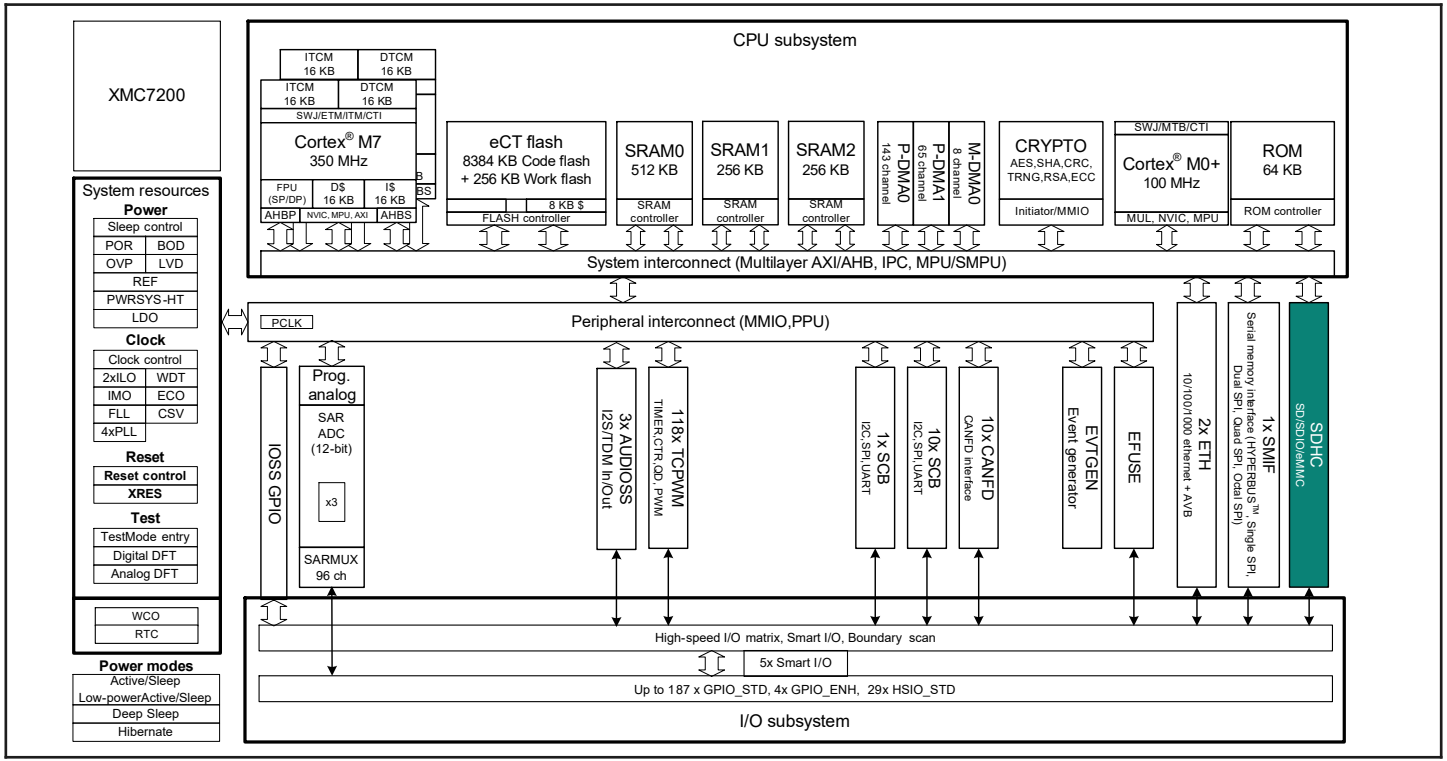
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Introduction to XMC7200 - 8M

SDHC host controller is located in the peripheral blocks.



Hint bar

See the XMC architecture reference manual, SDHC host controller, (chapter 31), for additional details.

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XMC7100 - 4M family



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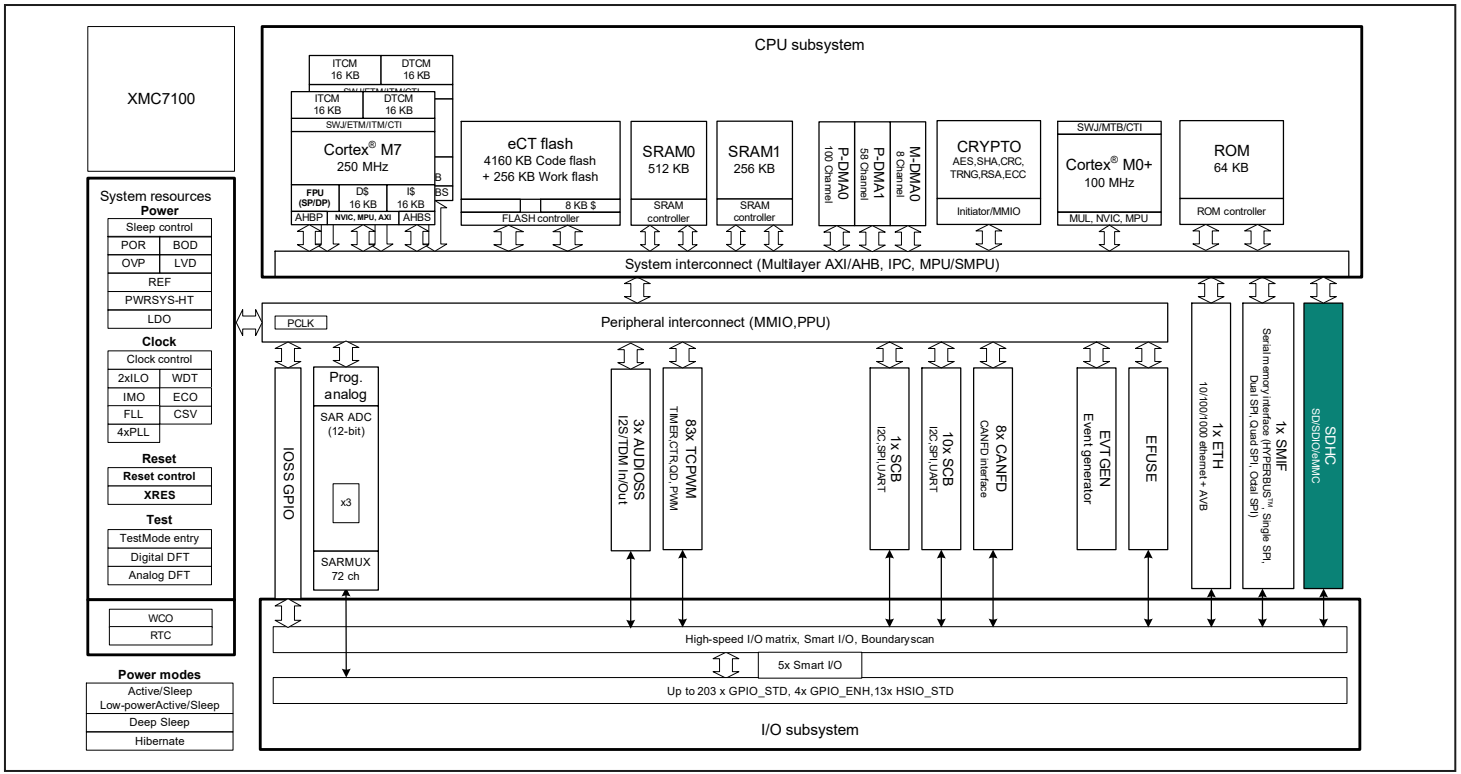
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Introduction to XMC7100 - 4M

SDHC host controller is located in the peripheral blocks.



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See the XMC architecture reference manual, SDHC host controller, (chapter 31), for additional details.

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Secure digital high capacity (SDHC)

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Overview

- SDHC host controller enables interface with the following:
  - Secure digital (SD) cards
  - Secure digital input output (SDIO) cards or Wi-Fi products (for example, CYW4343W)
  - Embedded multimedia card (eMMC)-based memory devices

Hint bar

See the following documents for additional details.

- Datasheet
- XMC architecture reference manual chapter 31
- SD specification's part 1 of physical layer specification version 6.00
- SD specification's part A2 of SD host controller standard specification version 4.20
- SD specification's part E1 of SDIO specifications version 4.10
- Embedded multi-media card (eMMC) electrical standard 5.1

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Features

- SD 6.0, SDIO 4.10, and eMMC 5.1 standards
- Host controller interface (HCI) 4.2
- eMMC/SD/SDIO interface for 3.3 V
- Three DMA modes
- I/O interfaces
  - Card detection
  - Mechanical write protection

Hint bar

See the following documents for additional details.

- Datasheet
- XMC architecture reference manual chapter 31
- SD specification's part 1 of physical layer specification version 6.00
- SD specification's part A2 of SD host controller standard specification version 4.20
- SD specification's part E1 of SDIO specifications version 4.10
- Embedded multi-media card (eMMC) electrical standard 5.1

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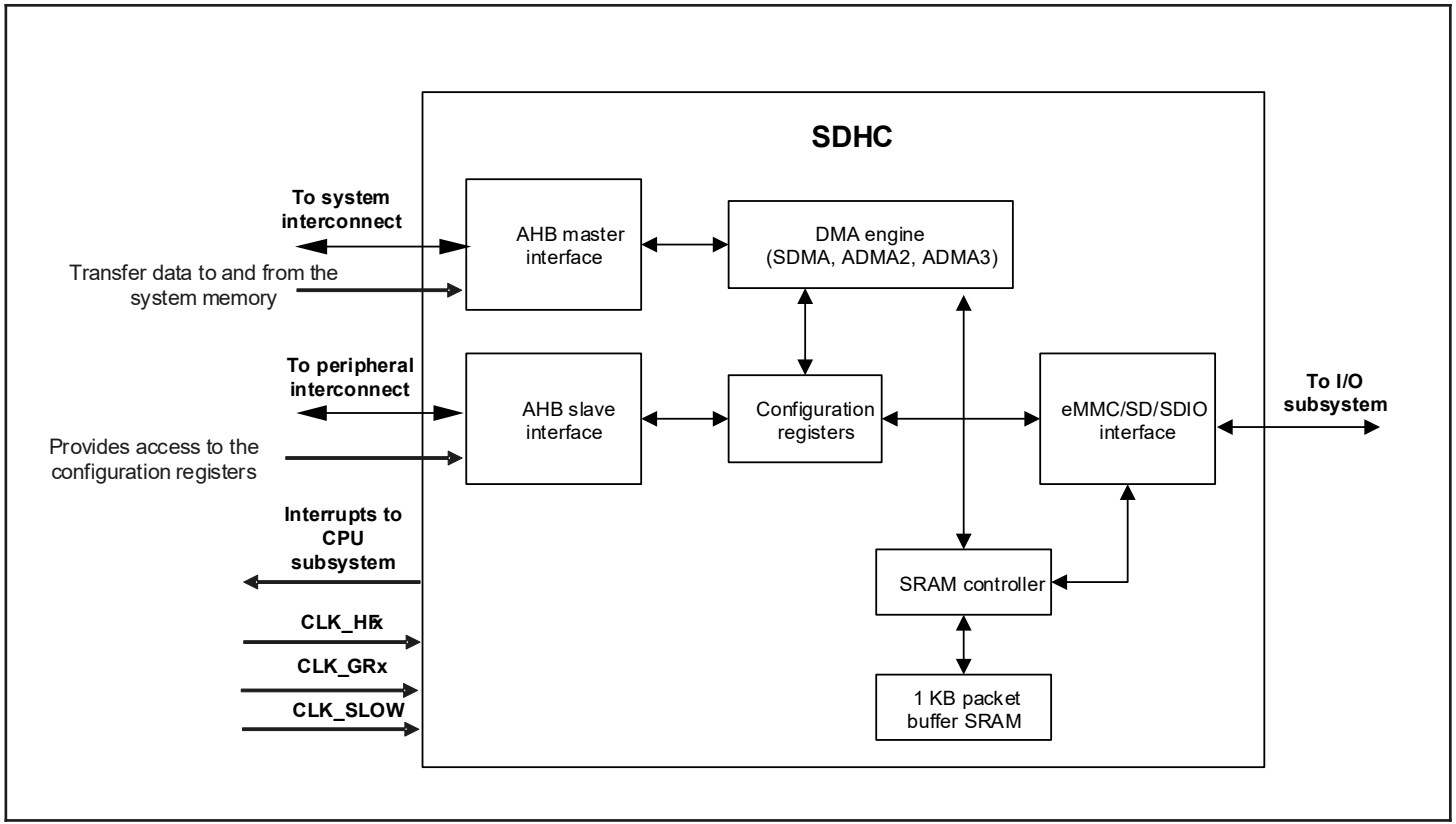
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SDHC components

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Block diagram



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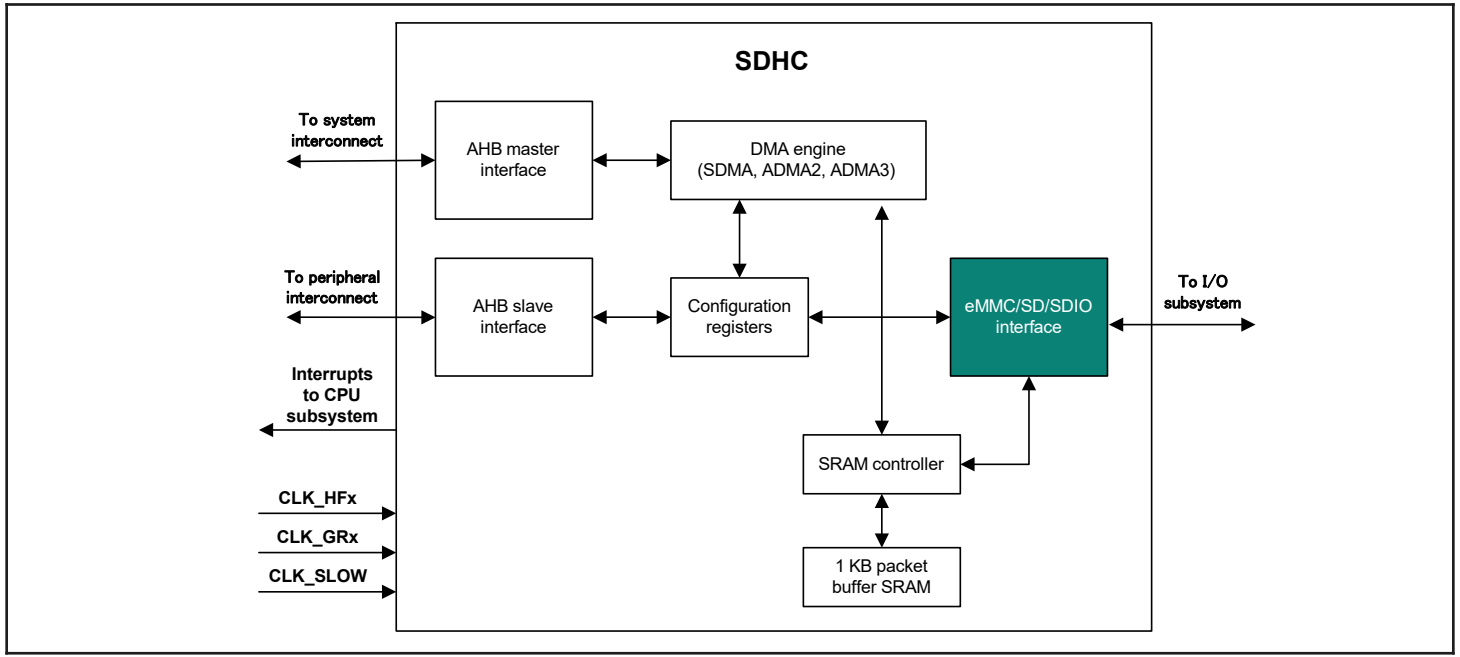
See the XMC architecture reference manual, block diagram (chapter 31.2), for additional details.

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Host controller components (1/24)

SDHC host controller components include:

- eMMC/SD/SDIO bus protocol
- eMMC/SD/SDIO interface



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See the XMC architecture reference manual, Features (chapter 31.1), for additional details.

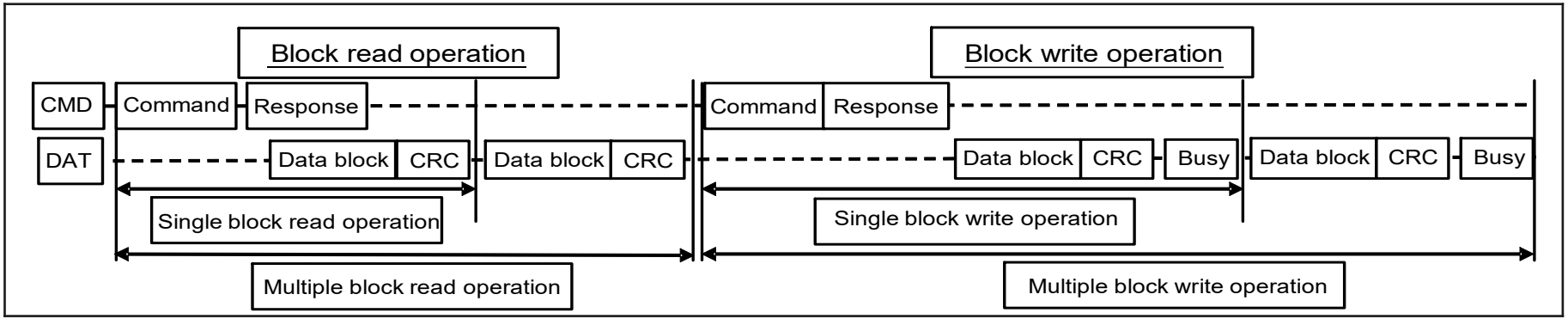
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Host controller components (2/24)

eMMC/SD/SDIO bus protocol

Each message is represented by one of the following tokens

- **Command**: Command is a token that is sent from the host to the card for the operation to start
- **Response:** Response is a token that is sent from the card to the host as an answer to a previously received command
- **Data:** Data is transferred via the data line
- **Busy:** Block write operation uses a simple busy signalling of the write operation on the DAT0 line



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Host controller components (3/24)

eMMC/SD/SDIO interface: Data bus and speed modes

–	eMMC	SD	SDIO
Data bus	1-bit 4-bit 8-bit	1-bit 4-bit	
Max. Speed Modes	Legacy: 26 MBps @ 26 MHz, 8-bit High-speed SDR: 52 MBps @ 52 MHz, 8-bit High-speed DDR: 104 MBps @ 52 MHz, 8-bit	Default speed (DS): 12.5 MBps @ 25 MHz, 4-bit High speed (HS): 25.0 MBps @ 50 MHz, 4-bit	

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See the XMC architecture reference manual, I/O interface (sections 31.1, 31.7), and register reference manual for additional details.

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Host controller components (4/24)

eMMC/SD/SDIO interface: I/O interface

Signal	Function	eMMC	SD	SDIO
SDHC_CLK_CARD	Clock output	Yes	Yes	Yes
SDHC_CARD_CMD	Command (bi-directional)	Yes	Yes	Yes
SDHC_CARD_DAT_3TO0_[3:0]	Data (bi-directional)	Yes	Yes	Yes
SDHC_CARD_DAT_7TO4_[7:4]	Data (bi-directional)	Yes	-	-
SDHC_CARD_DETECT_N[1]	Card detect signal input, active LOW	-	Yes	-
SDHC_CARD_MECH_WRITE_PROT[1]	Mechanical write protect signal input, active LOW	-	Yes	-
SDHC_CARD_IF_PWR_EN	Card interface power enable output	Yes	Yes	Yes

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See the XMC architecture reference manual, I/O interface (sections 31.1, 31.7), and register reference manual for additional details.

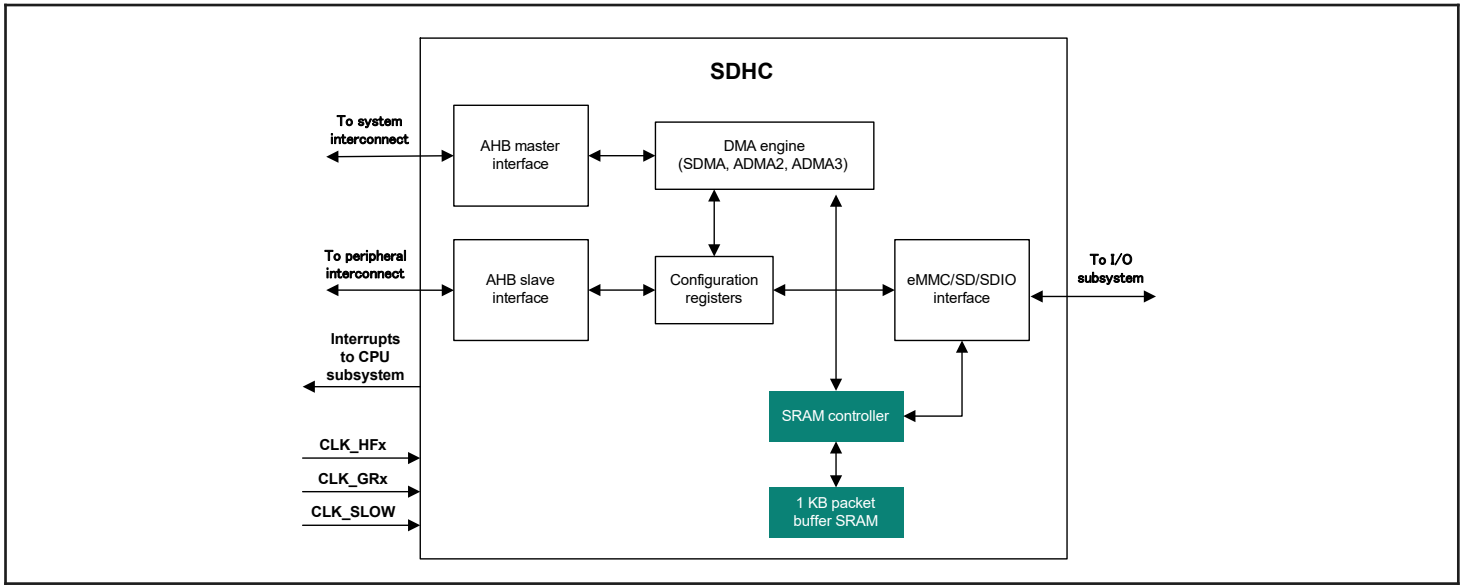
[1] SDHC_CARD_DETECT_N and SDHC_CARD_MECH_WRITE_PROT should be connected to ground if an eMMC or an embedded SDIO device is connected.

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Host controller components (5/24)

SDHC host controller components includes:

- SRAM
  - SRAM controller
  - Packet buffer SRAM



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See the XMC architecture reference manual, Packet buffer SRAM chapter (31.8), for additional details.

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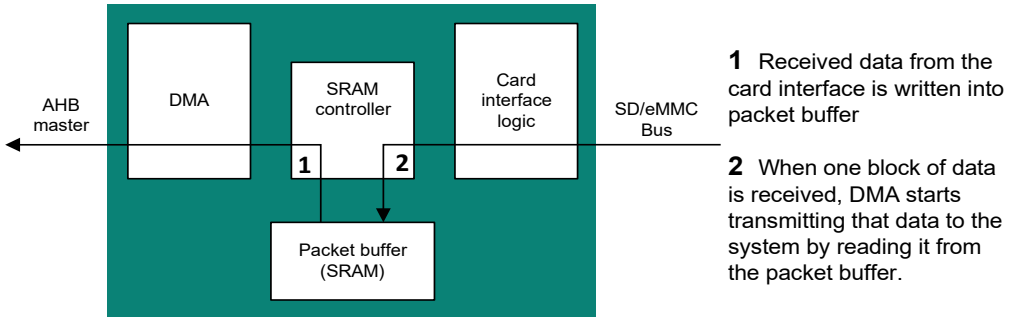
Host controller components (6/24)

Packet buffer SRAM: Packet buffer SRAM stores the data packets while carrying out data transfer to and from the card.

– SRAM size is 1KB to support buffering of two 512-byte blocks

–**Read transfer**

Data flow in read transfer



1 Received data from the card interface is written into packet buffer

2 When one block of data is received, DMA starts transmitting that data to the system by reading it from the packet buffer.

– **Write transfer:** DMA writes data into a packet buffer that is subsequently read by the card interface

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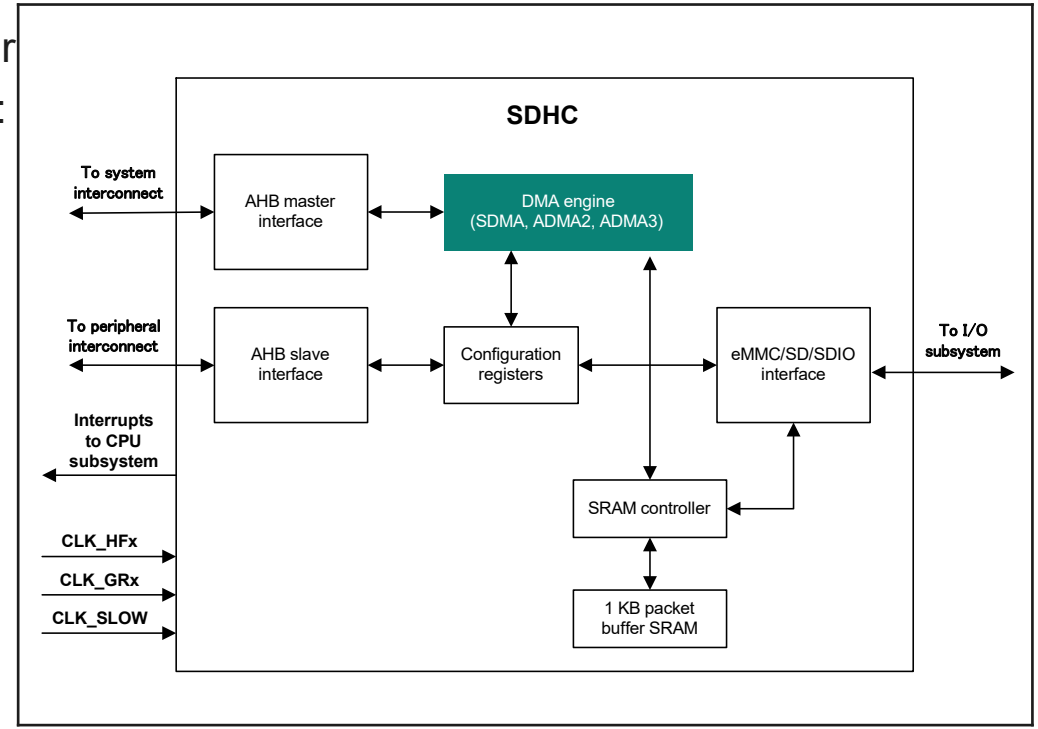
See the XMC architecture reference manual, Packet buffer SRAM chapter (31.8), for additional details.

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Host controller components (7/24)

SDHC host controller components include:

- DMA engine
  - SDMA
  - ADMA2
  - ADMA3



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See the XMC architecture reference manual, DMA engine section (31.9), for additional details

- Single operation DMA (SDMA)
- Advanced DMA (ADMA)

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Host controller components (8/24)

DMA engine

DMA engine handles data transfer between SDHC and system memory

Features

– Supports SDMA, ADMA2, and ADMA3 modes

Modes	Description	Max. transfer size
SDMA	SDMA transfers a data boundary by a read/write command	512KB
ADMA2	ADMA2 transfers multiple data boundaries by a read/write command	4GB
ADMA3	ADMA3 performs multiple ADMA2 operations	4GB

– DMA engine enables new task descriptor fetches[1] while DMA is moving data during task execution[2]

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See the XMC architecture reference manual, (section 31.9), for additional details

– Single operation DMA (SDMA)

– Advanced DMA (ADMA)

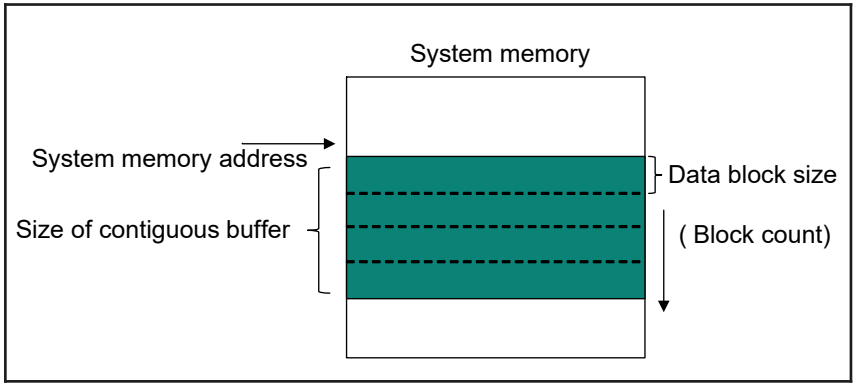
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Host controller components (9/24)

SDMA operation

SDMA transfers a data boundary by a read/write command

- Writing to the command register[1] triggers SDMA transfer
- Configuration registers for transfer
  - System memory address or block count[2]: SDMA uses ADMA System Address Register[3] when Block Count is specified[4]
  - Data block size[5]: 1 byte to 2048 bytes
  - Size of contiguous buffer[6]: 4 KB, 8 KB, 16 KB, 32 KB, 64 KB, 128 KB, 256 KB, and 512 KB



[1] CMD_R
[2] SDMASA_R.BLOCKCNT_SDMASA
[3] ADMA_SA_LOW_R
[4] When HOST_CTRL2_R.HOST_VER4_ENABLE = 1
[5] BLOCKSIZE_R.XFER_BLOCK_SIZE
[6] BLOCKSIZE_R.SDMA_BUF_BUF_BDARY

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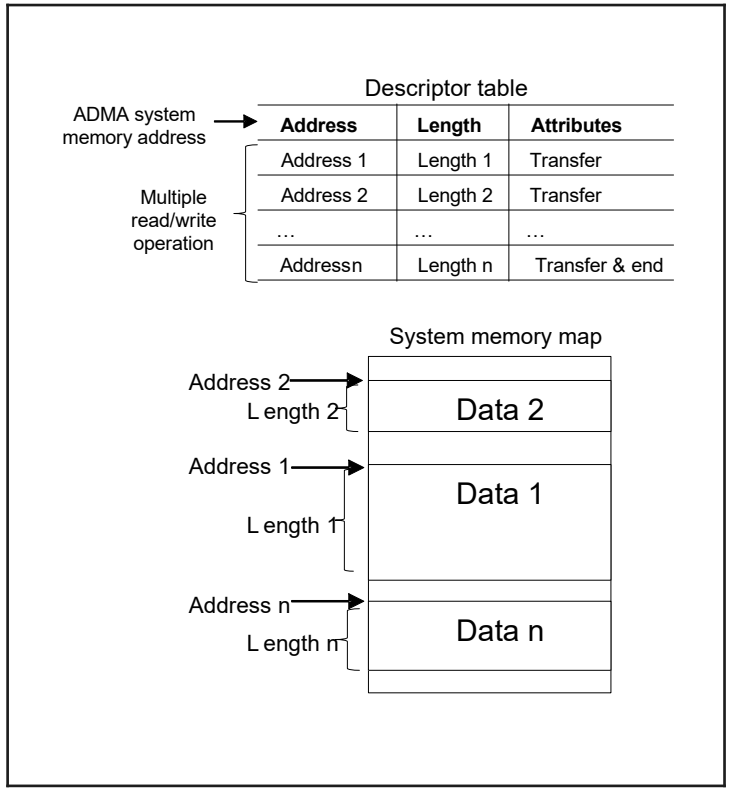
Host controller components (10/24)

ADMA2 operation

ADMA2 transfers multiple data boundaries by a read/write command

- Procedure:
  1. Setting ADMA System memory address[1] (see the figure) for descriptor table start address
  2. Writing to the command register[2] triggers the ADMA2 transfer
  3. ADMA2 fetches one descriptor line and executes it in the Descriptor table
  - This is repeated until the end of the descriptor is found[3] (see third step of the procedure)
- Data address and length
  - Minimum unit of address: 4 bytes
  - Maximum data length of each descriptor line: less than 64 KB

[1] ADMA_SA_LOW_R
[2] CMD_R
[3] End = 1 in attribute



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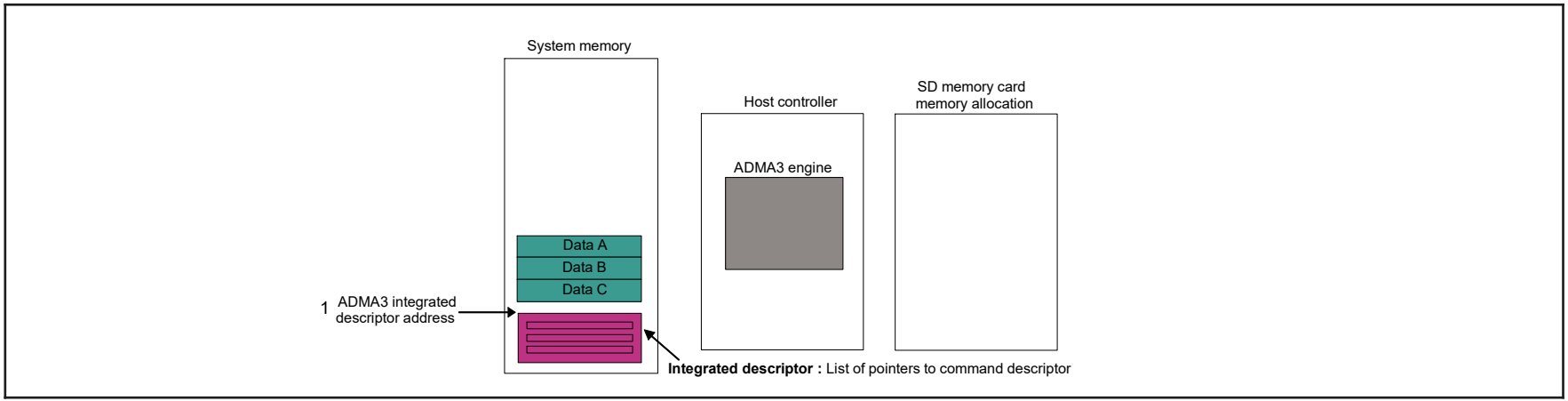
Host controller components (11/24)

ADMA3 operation: Writing to the Integrated Address register

ADMA3 performs multiple ADMA2 operations. The following slides describe each of the operations.

– Procedure:

1. Writing to the ADMA3 integrated address register[1] triggers ADMA3



[1] ADMA_ID_LOW_R

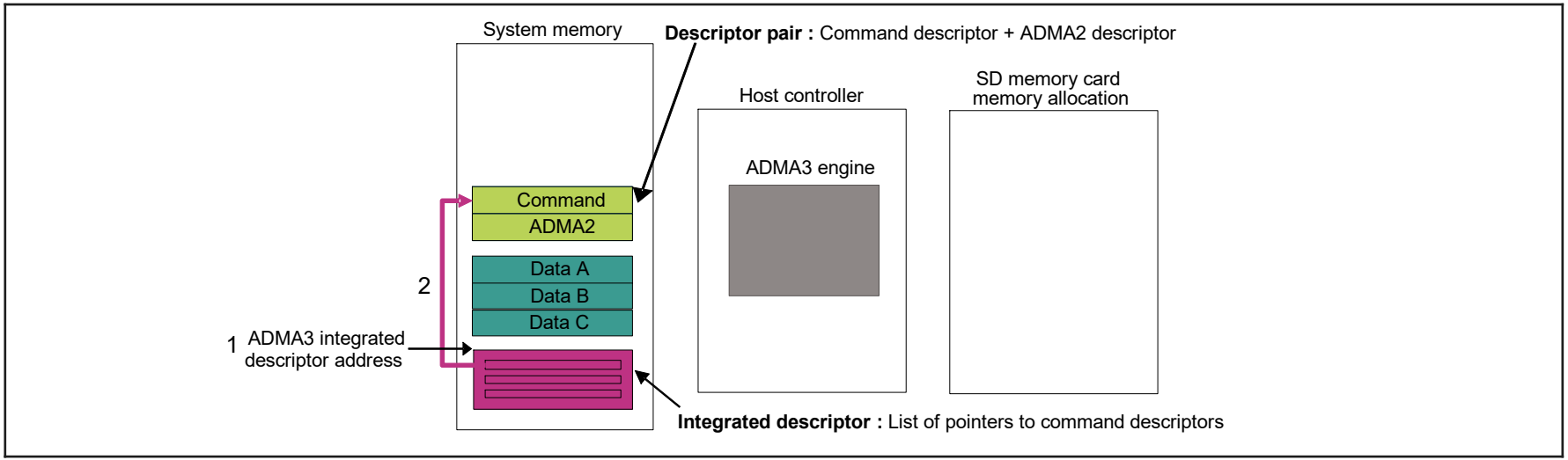
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Host controller components (12/24)

ADMA3 operation: Fetching pointer in descriptor

– Procedure:

2. ADMA3 fetches pointers one by one in the integrated descriptor and executes descriptors designated by the pointer



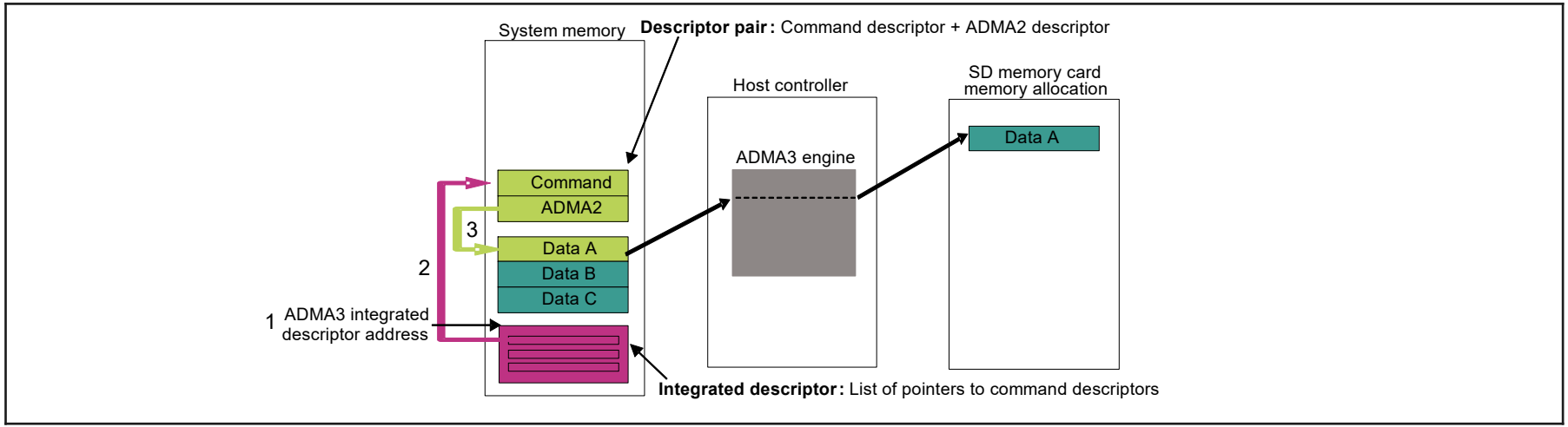
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Host controller components (13/24)

ADMA3 operation: Issuing a command

– Procedure:

3. ADMA3 writes the Command descriptor contents to the host controller registers to issue a command and then executes the ADMA2 descriptor



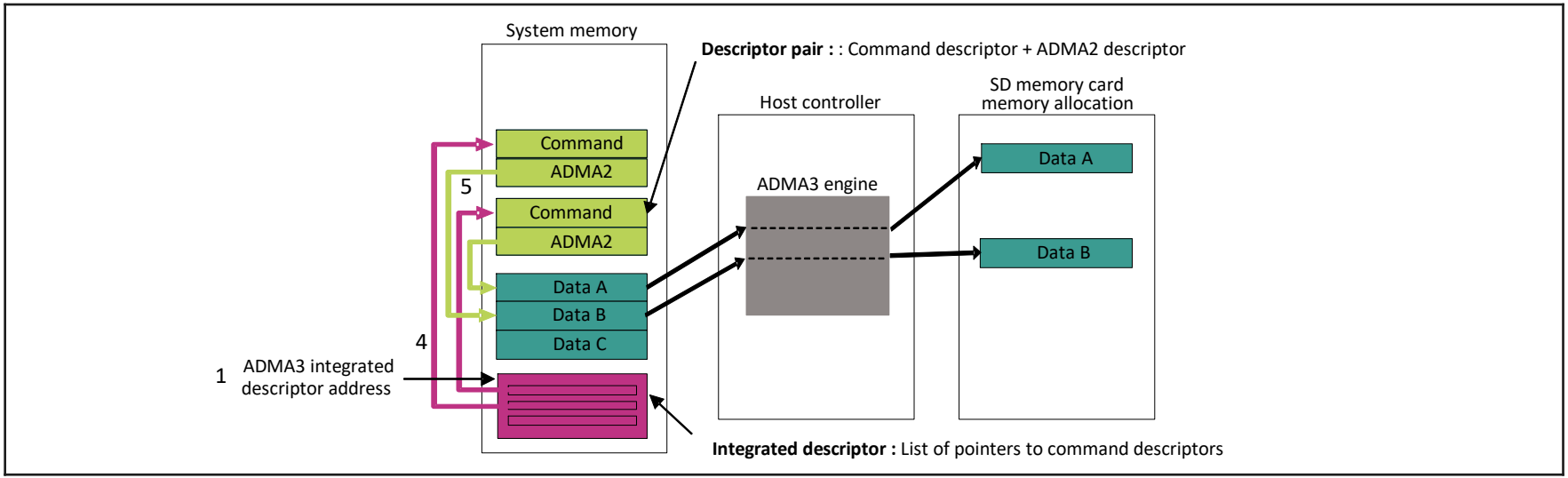
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Host controller components (14/24)

ADMA3 operation: Executing next descriptor

– Procedure:

4. ADMA3 fetches the next pointer in the Integrated descriptor and executes descriptors designated by the pointer



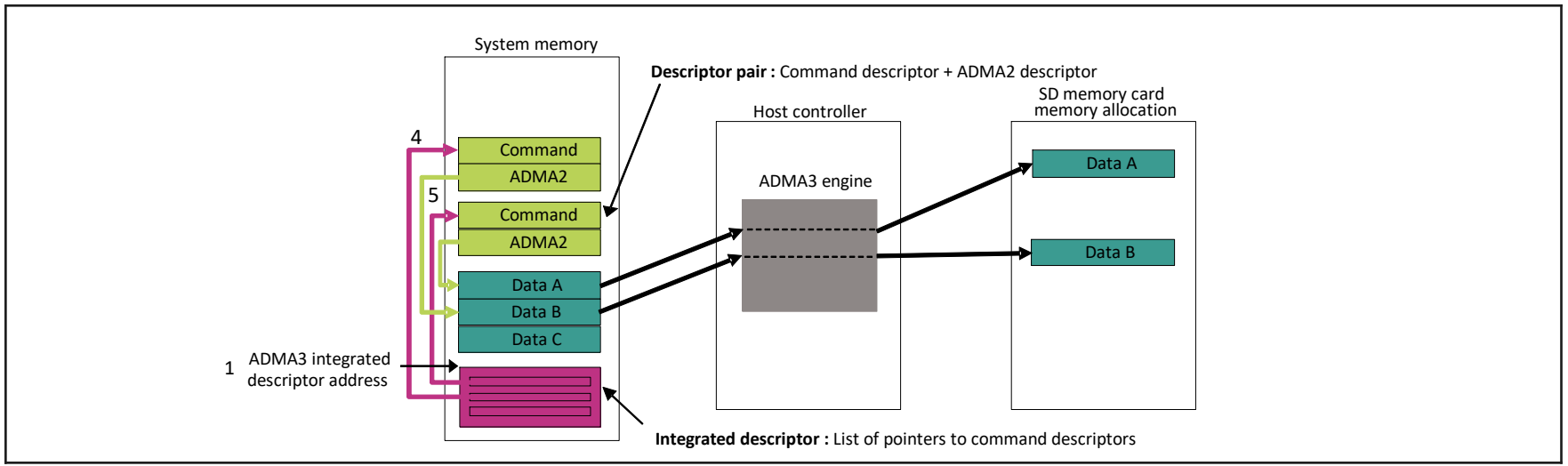
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Host controller components (15/24)

ADMA3 operation: Executing next descriptor

– Procedure:

5. ADMA3 writes the next Command descriptor contents to the host controller registers to issue a command and then executes the ADMA2 descriptor



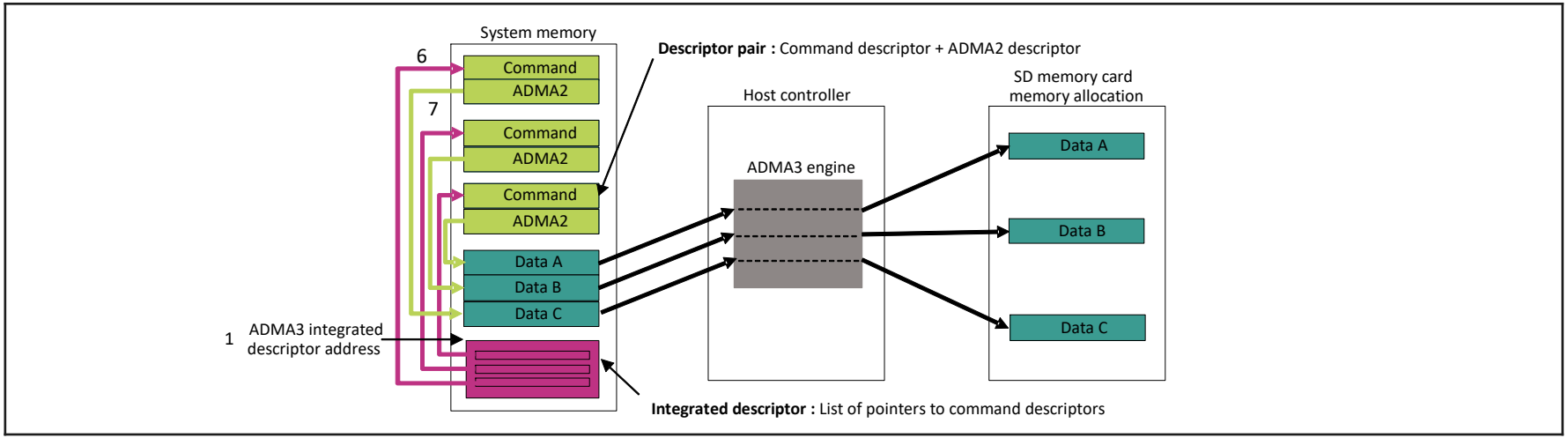
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Host controller components (16/24)

ADMA3 operation: Executing until the end of the descriptor

– Procedure:

6. ADMA3 fetches the next pointer in the Integrated descriptor and executes descriptors designated by the pointer until the end of the Command descriptor[2]



[2] CDEnd = 1 in attribute

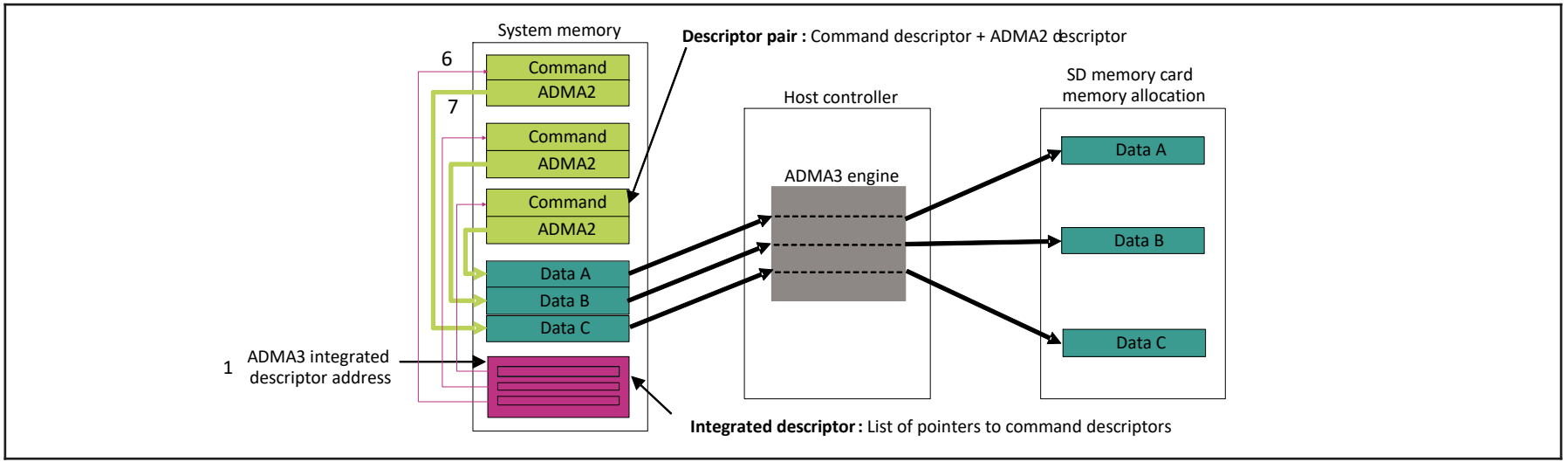
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Host controller components (17/24)

ADMA3 operation: Executing until the end of the descriptor

– Procedure:

7. ADMA3 writes the end of the Command descriptor contents to the host controller registers to issue a command, and then executes the ADMA2 descriptor

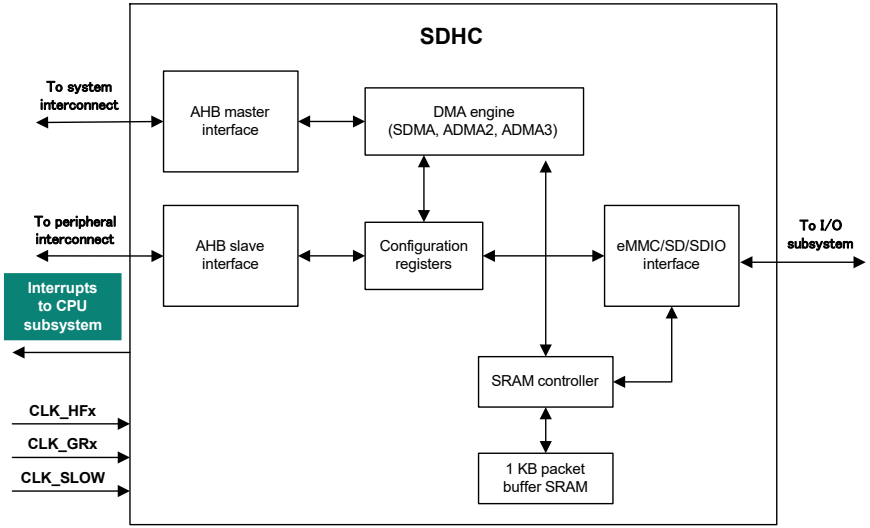


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Host controller components (18/24)

SDHC host controller components

- Interrupts
  - Wakeup interrupts
  - General interrupts



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See the XMC architecture reference manual, Interrupts to CPU (chapter 31.6), for additional details.

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Host controller components (19/24)

Wakeup interrupts (only for SD/SDIO mode)

Wakeup the SDHC host controller from Active/Sleep mode.

Wakeup interrupt	Set condition
SD card insertion	Card insertion
SD card removal	Card removal
SDIO card interrupt	DAT[1] = 1

Hint bar

See the XMC architecture reference manual, (section 31.6), and register reference manual for additional details

- Wakeup the interrupts cannot wake up from Deep Sleep and Hibernate mode
- In Deep Sleep mode, only CTL register is retained

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Host controller components (20/24)

General interrupts (for eMMC/SD/SDIO mode)

Triggered on all other events, in either normal conditions or error conditions.

Normal interrupt	Set condition
Command complete	Command complete
Transfer complete	Command execution is completed
Block gap event	Transaction stopped at block gap
DMA interrupt	DMA Interrupt is generated
Buffer write ready	Ready to write buffer
Buffer read ready	Ready to read buffer
Card insertion (SD mode only)	Card inserted
Card removal (SD mode only)	Card removed
Card interrupt (SDIO mode only)	DAT[1] = 1

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Host controller components (21/24)

General interrupts (for eMMC/SD/SDIO mode)

Triggered on all other events, in either normal conditions or error conditions.

Normal interrupt	**Set condition**
FX event	R[14] = 1 (Response register) and Response type R1/R5 = 0 (Transfer mode register)
Command queuing engine event	Command queuing related event has occurred (depends on command queuing interrupt status register)
Error interrupt	**Set condition**
Command timeout error	No response is returned within 64 SD clock cycles from the end bit of the command
Command CRC error	Command CRC error occurred
Command end bit error	Detected that the end bit of a command response is ‘0’
Command index error	Command index error occurred in the command response
Data timeout error	Detected one of the following timeout conditions: – Busy timeout for R1b, R5b type – Busy timeout after Write CRC status – Write CRC status timeout – Read data timeout

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Host controller components (22/24)

General interrupts (for eMMC/SD/SDIO mode)

Triggered on all other events, in either normal conditions or error conditions.

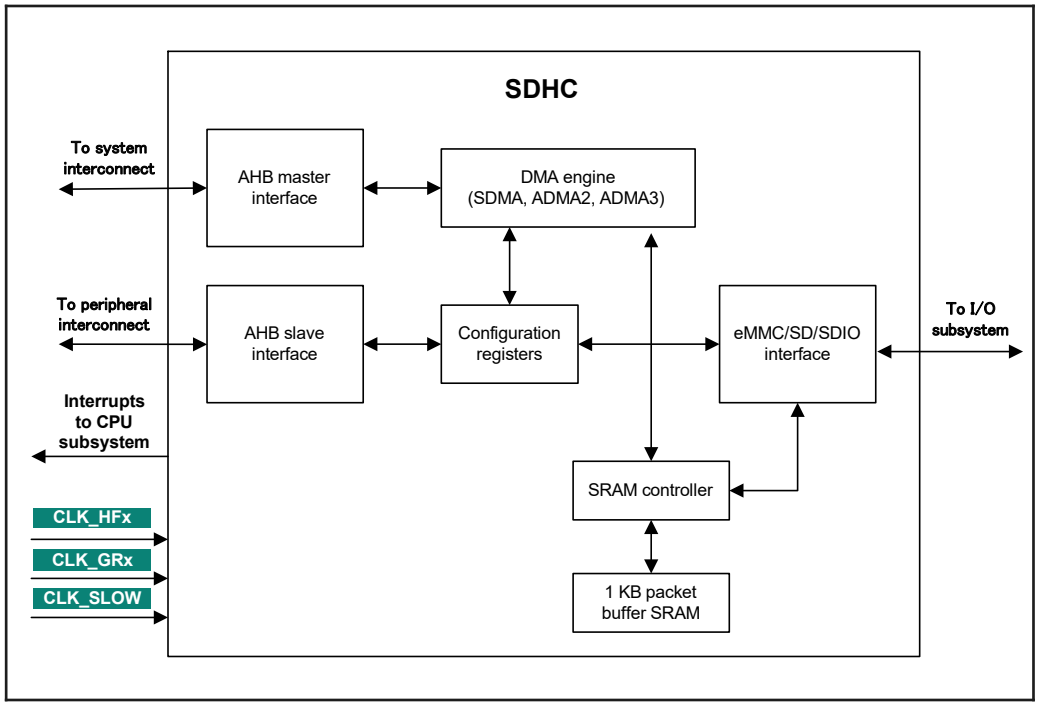
Error interrupt	Set condition
Data CRC error	Detected CRC error when transferring read data, which uses the DAT line, when detecting the write CRC status having a value of other than 010 or when write CRC status timeout occurs.
Data End Bit error	Detected 0 at the end bit position of read data that uses the DAT line or at the end bit position of the CRC status.
Current Limit error	Power fail occurred
Auto CMD error	Detected that any of the bits D00 to D05 in Auto CMD error status register have changed from 0 to 1.
ADMA error	ADMA error occurred
Response error (SD/SDIO mode only)	An error is detected in a response

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Host controller components (23/24)

SDHC host controller components:

- Clocks
  - CLK_HFx[1]
  - CLK_GRx[2]
  - CLK_SLOW



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See the XMC architecture reference manual, chapter 31.3, for additional details.

[1] It is connected to CLK_HF6 in the XMC7000. For other devices, see the respective device datasheet.
[2] It is connected to CLK_GR4 in the XMC7000. For other devices, see the respective device datasheet.

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Host controller components (24/24)

Clocks

The following clocks are used in the SDHC host controller block:

Source	SDHC clock	Function
CLK_SLOW	Core SDHC clock	Used for core SDHC functions including the packet buffer SRAM; it is sourced from the slow clock (CLK_SLOW); it must be ≥ AHB slave clock.
	AHB Master Interface clock	Used by the AHB master interface; it is sourced from the slow clock (CLK_SLOW); it must be ≥ AHB slave clock.
CLK_GRx	AHB Slave Interface clock	Used by the AHB slave interface; it is clocked by the PERI group clock (CLK_GRx); it must be ≥ CLK_CARD.
CLK_HFx	Base clock / Card clock	Used for sourcing the SD/eMMC interface clock (CLK_CARD); it is derived from CLK_HFx; it must be set to 100 MHz to be compatible with the capabilities register[1].
	Timer clock	Used for command and data timeout functions; it is derived from CLK_HFx.

CLK_SLOW ≥ CLK_GRx ≥ CLK_CARD

[1] This register provides the Host driver with information specific to the Host controller.

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See the XMC architecture reference manual, chapter 31.3, for additional details and the register reference manual for additional information.

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Appendix

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Unsupported features

- SD/SDIO operation in UHS-II mode
- Command queuing engine (CQE)
- eMMC boot operation in dual data rate mode
- Read wait operation by DAT[2] signaling in an SDIO card
- Suspend/resume operation in an SDIO card
- Interrupt input pins for embedded SD systems
- SPI protocol mode of operation
- SD UHS-I mode using 1.8 V signal voltage: SDR, SDR25, SDR50, and DDR50

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Revision history

Document revision	Date	Description of change
**	2022-10-19	Initial release.
*A	2026-01-02	Migrated to the latest empower training presentation template.

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