

XMC7000 Reset system

Customer training workshop (CTW)

November 2025

public

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Target products

Target product list for this training material:

Family category	Series	Code flash memory size
XMC7200	XMC7200-8M	Up to 8384 KB
XMC7100	XMC7100-4M	Up to 4160 KB

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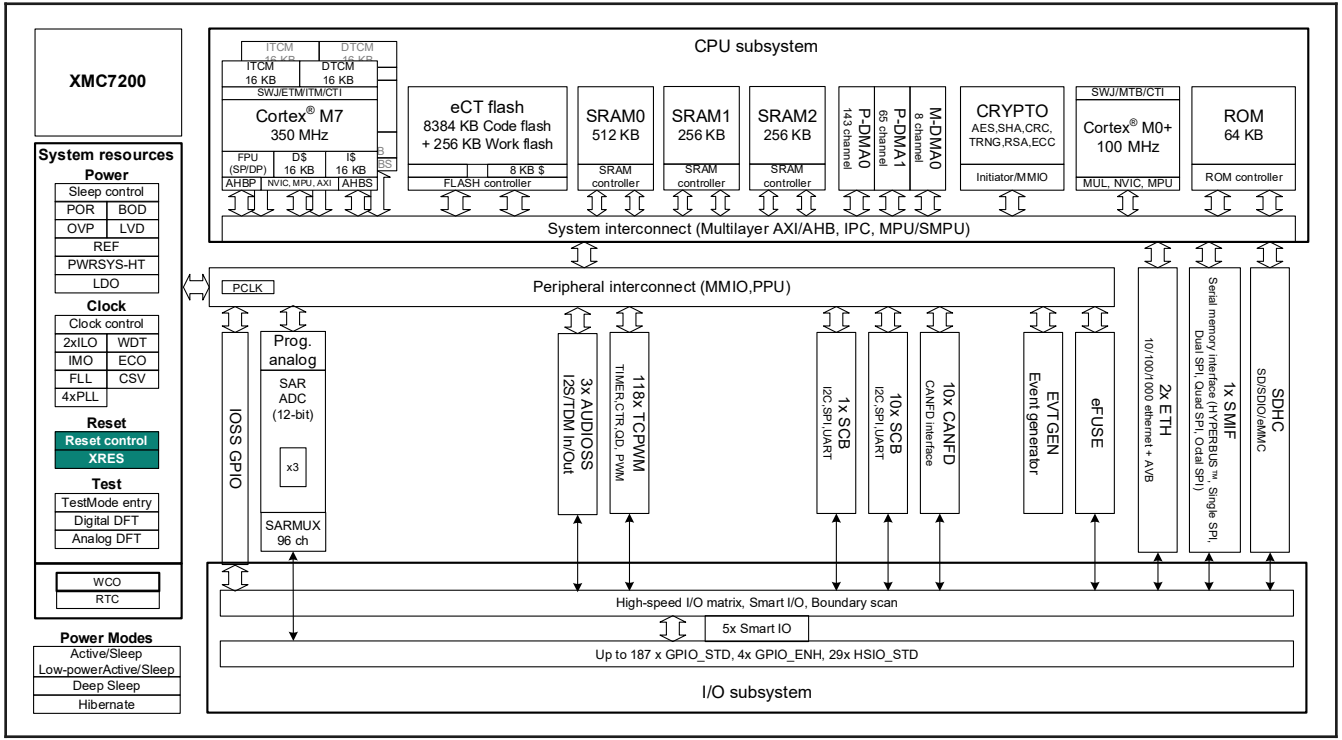
XMC7200 - 8M family



public

Introduction to XMC7200- 8M

The reset system is part of System resources.



Hint bar

See the architecture reference manual chapter 19, Reset system and the Registers reference manual for additional details.

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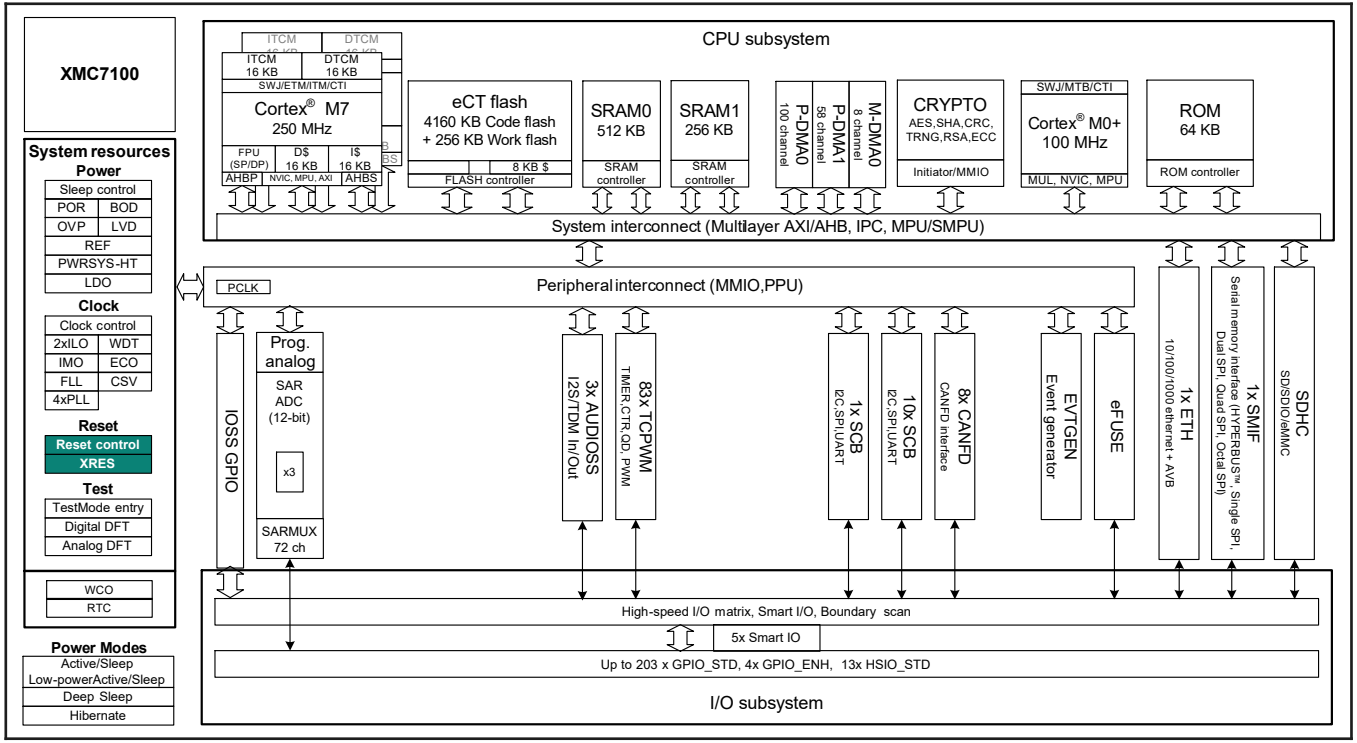
XMC7100 - 4M family



public

Introduction to XMC7100- 4M

The reset system is part of System resources.



Hint bar

See the architecture reference manual chapter 19, Reset system and the Registers reference manual for additional details.

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Reset system



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Overview

- XMC7000 supports several types of resets to ensure error-free operation during power-up and allow the device to reset based on user-supplied external hardware or internal software reset signals
- Resets are asserted (triggered) asynchronously and deasserted (released) synchronously on a positive edge of the related clock

Hint bar

- See the architecture reference manual chapter 16 Power supply and monitoring for additional POR, BOD, OVD, and OCD details
- See the Watchdog timer training section for additional WDT and MCWDT details
- See the Device power mode training section for additional Hibernate details
- See the Fault subsystem training section for additional Fault details
- See the Clock system training section for additional CSV details

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Overview (contd.)

Reset sources:

- POR[1], BOD[2], OVD[3], OCD[4]
- External reset (XRES_L)
- WDT[5], MCWDT[6]
- Hibernate wakeup reset
- Internal system reset
- Fault
- CSV[7]

[1] Power-on reset
[2] Brownout detection
[3] Overvoltage protection
[4] Overcurrent protection
[5] Watchdog timer
[6] Multi-counter watchdog timer
[7] Clock supervision

Hint bar

- See the architecture reference manual chapter 16 Power supply and monitoring for additional POR, BOD, OVD, and OCD details
- See the Watchdog timer training section for additional WDT and MCWDT details
- See the Device power mode training section for additional Hibernate details
- See the Fault subsystem training section for additional Fault details
- See the Clock system training section for additional CSV details

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Sources

Reset source	Description
POR	POR holds the device in reset until the supply voltage V_{DDD} reaches a sufficient level to initialize the startup circuits
BOD	BOD generates a reset if V_{DDD} or V_{DDA} or V_{CCD} fall below their voltage threshold
OVD	OVD generates a reset if V_{DDD} or V_{DDA} or V_{CCD} rise above their voltage threshold
OCD	OCD generates a reset if the load current of a regulator is over the regulator limit
XRES_L	XRES_L is a reset triggered by an external reset pin
WDT	WDT reset causes a reset if WDT is not serviced by the software within a specified time limit or it is serviced too early in window mode

Hint bar

- See the Power supply and Monitoring training section 19 for additional POR, BOD, OVD, and OCD details
- See the Watchdog timer training section for additional WDT and MCWDT details
- See the Device power mode training section for additional Hibernate details
- See the Fault subsystem training section for additional Fault details
- See the Clock system training section for additional CSV details

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Sources (contd.)

Reset source	Description
Hibernate Wakeup reset	Hibernate wakeup reset occurs when a wakeup source triggers an exit from Hibernate mode
MCWDT	MCWDT reset causes a reset if MCWDTs are not serviced by the software within a specified time limit or they are serviced too early in window mode
Internal system reset (Software reset)	The internal system reset is a mechanism that allows software running on any of the CPUs or a connected debugger to request a system reset
Fault detection reset	Fault detection reset is generated if certain faults occur
CSV	CSV initiates a reset when a monitored clock stops or is outside the configured relationship to a reference clock
Test controller or debugger reset	Test controller or debugger asserted reset only resets the debug domain

Hint bar

- See the Power supply and Monitoring training section 19 for additional POR, BOD, OVD, and OCD details
- See the Watchdog timer training section for additional WDT and MCWDT details
- See the Device power mode training section for additional Hibernate details
- See the Fault subsystem training section for additional Fault details
- See the Clock system training section for additional CSV details

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Types and cause bits

Reset type	Reset source	Reset cause register [bit][1]	Clearing source of reset cause register	Block or not block recording of other reset causes	Available power mode
High-voltage (HV)	POR	SRSS_RES_CAUSE [30]	Software	Not block recording of other HV causes	All power modes
	BOD	SRSS_RES_CAUSE [19:17]	Software or POR	Block recording of other HV causes except POR	All power modes except Hibernate mode
	OVD	SRSS_RES_CAUSE [22:20]			
	OCD	SRSS_RES_CAUSE [24:23]			
	XRES_L	SRSS_RES_CAUSE [16]			All power modes
	WDT	SRSS_RES_CAUSE [0]			All power modes
	Hibernate wakeup reset	PWR_HIBERNATE [7:0] PWR_HIB_DATA [31:0] [2]	Software or POR or XRES	Not block recording of other causes	Hibernate mode

Hint bar

- See the Power supply and Monitoring training section 19 for additional POR, BOD, OVD, and OCD details
- See the Watchdog timer training section for additional WDT and MCWDT details
- See the Device power mode training section for additional Hibernate details
- See the Fault subsystem training section for additional Fault details
- See the Clock system training section for additional CSV details

[1] Reset occurs if the source triggers during Deep Sleep.
[2] Yes, if orderly shutdown of the RAM is done.

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Types and cause bits (contd.)

Reset type	Reset source	Reset cause register [bit][1]	Clearing source of reset cause register	Block or not block recording of other reset causes	Available power mode
Low-voltage (LV)	MCWDT	SRSS_RES_CAUSE [8:5]	Software or HV resets	Not block recording of other causes	All power modes except Hibernate mode
	Software reset	SRSS_RES_CAUSE [4]			Active mode
	Fault detection reset	SRSS_RES_CAUSE [2:1]			All power modes except Hibernate mode
	CSV	SRSS_RES_CAUSE2 [16:0]			
	Test controller or debugger reset	SRSS_RES_CAUSE [3]			

Hint bar

- See the Power supply and Monitoring training section 19 for additional POR, BOD, OVD, and OCD details
- See the Watchdog timer training section for additional WDT and MCWDT details
- See the Device power mode training section for additional Hibernate details
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- See the Clock system training section for additional CSV details

[1] Reset occurs if the source triggers during Deep Sleep.

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Distribution

Mapping of reset sources to the corresponding destinations that are affected by a reset event

Reset type	Reset source	HV reset causes in RES_CAUSE	LV reset causes in RES_CAUSE	Data registers in fault	Debug unit	Hibernate registers	RTC	CPUs	SRAM retention
High-Voltage (HV)	POR	X	X	X	X	X	X	X	No
	BOD	–	X	X	X	X	–	X	No
	OVD	–	X	X	X	X	–	X	No
	OCD	–	X	X	X	X	–	X	No
	XRES_L	–	X	X	X	X	–	X	No
	WDT	–	X	X	X	X	–	X	Yes[6]
	Hibernate wakeup reset	–	X	X	X	–	–	X	No

Hint bar

See the architecture reference manual section 19.1, Reset sources for additional details.

[6] Yes, if orderly shutdown of the RAM is done only during a warning interrupt.

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Distribution (contd.)

Mapping of reset sources to the corresponding destinations that are affected by a reset event

Reset type	Reset source	HV reset causes in RES_CAUSE	LV reset causes in RES_CAUSE	Data registers in fault	Debug unit	Hibernate registers	RTC	CPUs	SRAM retention
Low-Voltage (LV)	MCWDT	–	–	–	X[1]	–	–	X	Yes[2]
	Software reset	–	–	–		–	–	X	Yes[2]
	Fault Detection Reset	–	–	–	X[1]	–	–	X	Yes[2]
	CSV_HF[4]	–	–	–		–	–	X	Yes[3]
	CSV_REF[5]	–	–	–		–	–	X	No

Hint bar

See the architecture reference manual section 19.1, Reset sources for additional details.

[1] Reset occurs if the source triggers during Deep Sleep.
[2] Yes, if orderly shutdown of the RAM is done.
[3] Yes, if orderly shutdown of the RAM is done and the CSV resets are not from CSV_HF0.
[4] Clock supervision for High-frequency clock.
[5] Clock supervision for Reference clock.

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Revision history

Document revision	Date	Description of change
**	2022-03-24	Initial release
*A	2025-11-05	Migrated to the latest empower training presentation template

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