

XMC7000 Protection units

Customer training workshop (CTW)

January 2026

public

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Target products

Target product list for this training material:

Family category	Series	Code flash memory size
XMC7200	XMC7200-8M	Up to 8384 KB
XMC7100	XMC7100-4M	Up to 4160 KB

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XMC7200 - 8M family



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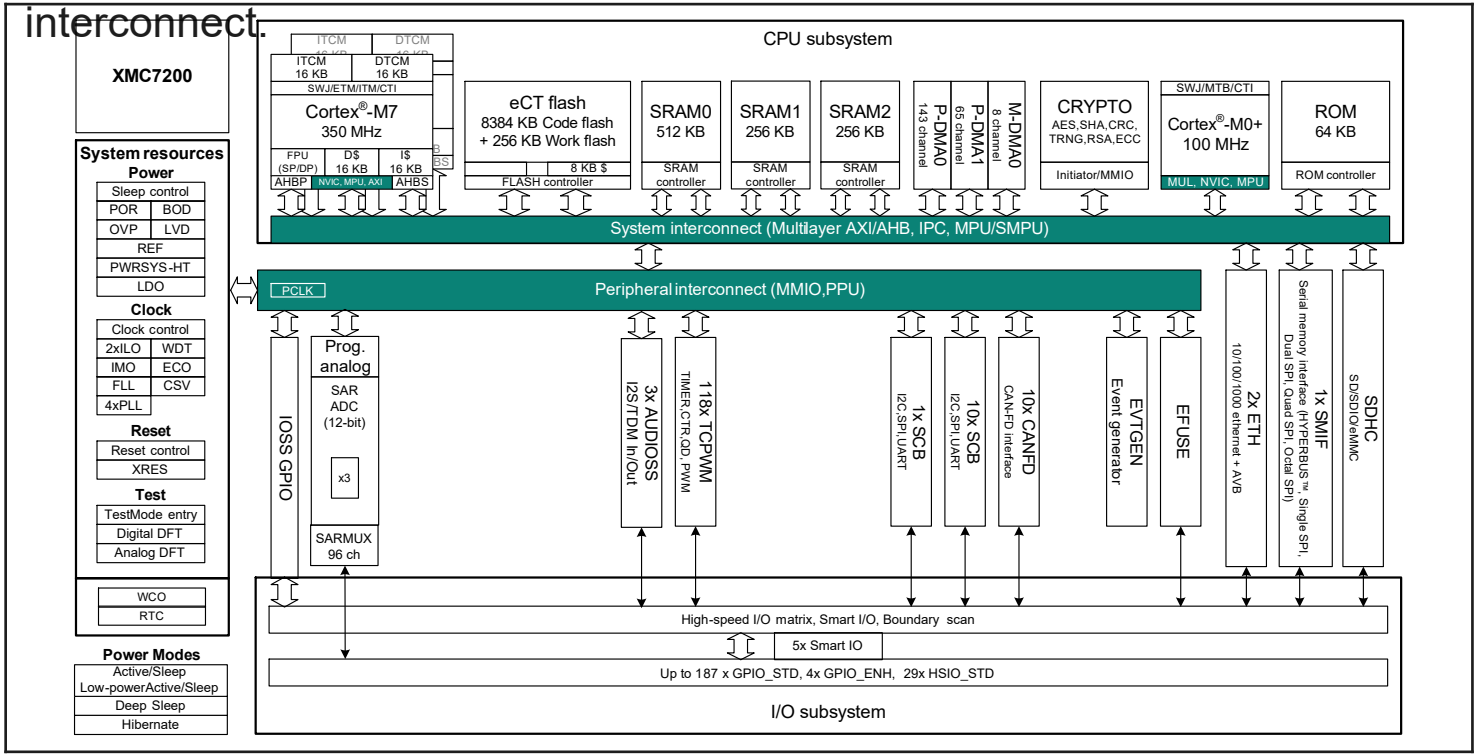
Introduction to XMC7200-8M

Protection units (MPU/SMPU/PPU) are in CPUSS and peripheral interconnect.



Hint bar

See the XMC7000 MCU family architecture reference manual chapter 6 and the XMC7200 MCU registers reference manual for additional details.

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XMC7100 - 4M family



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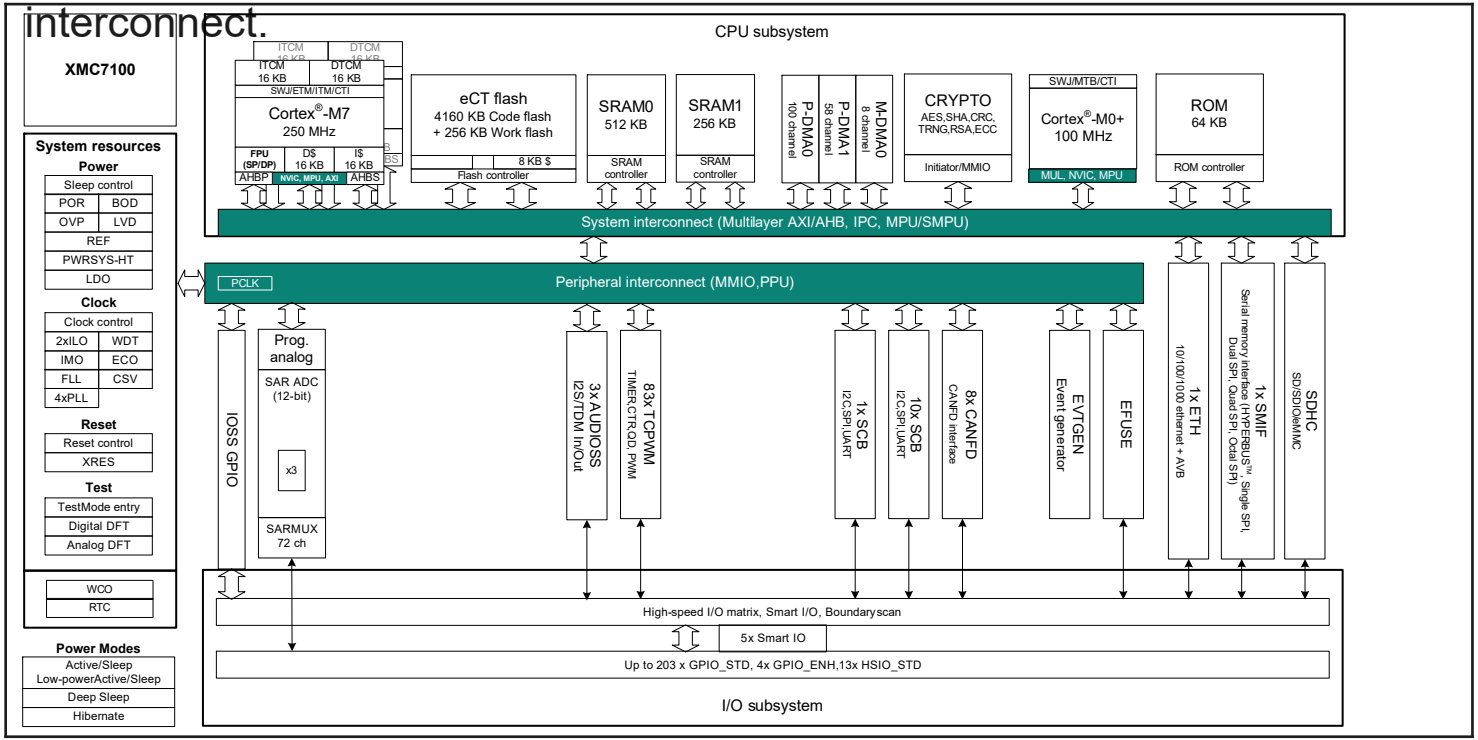
Introduction to XMC7100-4M

Protection units (MPU/SMPU/PPU) are in CPUSS and peripheral interconnect.



Hint bar

See the XMC7000 MCU family architecture reference manual chapter 6 and the XMC7200 MCU registers reference manual for additional details.

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Protection unit overview

Overview

- Allows/restricts bus transfers on the bus infrastructure
- Includes four protection units (MPU/SMPU/PPU/SWPU)

Features

- Supports various access attributes
  - Address range (Start address and region size)
  - Read/Write
  - Execute (code or data)
  - Privileged/unprivileged
  - Secure/non-secure
  - Protection context (PC)

Hint bar

- See the XMC7000 MCU family architecture reference manual chapter 6 and the XMC7200 MCU registers reference manual for additional details
- See the XMC7000 microcontroller CPU subsystem, chapter CPUSS for additional details

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Protection unit overview (contd.)

Features (continuation)

- Protects protection structures
- Captures protection violations in fault report structure

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- See the XMC7000 MCU family architecture reference manual chapter 6 and the XMC7200 MCU registers reference manual for additional details
- See the XMC7000 microcontroller CPU subsystem, chapter CPUSS for additional details

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Protection context

- Protection context (PC) is an access attribute of the protection units
- The PC prevents erroneous writing from accessing the unintended PC to memory, and peripherals
- The PC helps to apply different protection attributes without changing the SMPU, PPU, and SWPU settings
  - XMC7000 supports eight PCs
  - Used as the PC attribute for bus transfers
  - Access to memory and peripherals is allowed or restricted by SMPU, PPU, and SWPU
  - Changed by reprogramming the PC field in MSx_CTL
  - PC0 and PC1 are hardware-controlled and not available to the user; PC2 to PC7 are available

Hint bar

- See the XMC7000 MCU family architecture reference manual chapter 6 and the XMC7200 MCU registers reference manual for additional details
- See the XMC7000 microcontroller CPU subsystem, chapter CPUSS for additional details

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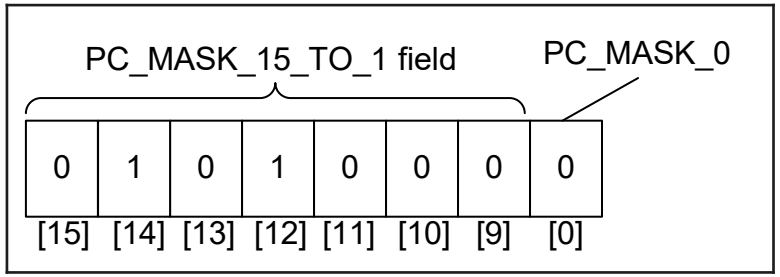
Protection context programming and restrictions

PC programming

- Main CPU[1], secondary CPU[2], and test controller bus master have a PC field[3]
- A PC attribute is changed by reprogramming the PC field
- The PC is used as the access attribute for all bus transfers by the master
- The SMPUs, PPUs, and SWPUs allow/restrict bus transfers based on the PC attribute



[1] The main CPU refers to the Cortex®-M7 CPU in the MCU.
[2] The secondary CPU refers to the Cortex®-M0+ CPU in the MCU.
[3] The PC field is located in the MPU_MSx_CTL register.
[4] PC_MASK field is located in the SMPU_MSx_CTL register. PC_MASK_0 is always **0** and cannot set any master.
[5] PCs 4 and 6 are configurable; other PCs are nonconfigurable.

Hint bar

See the XMC7000 MCU family architecture reference manual chapter 6.3 and the XMC7200 MCU registers reference manual for additional details.

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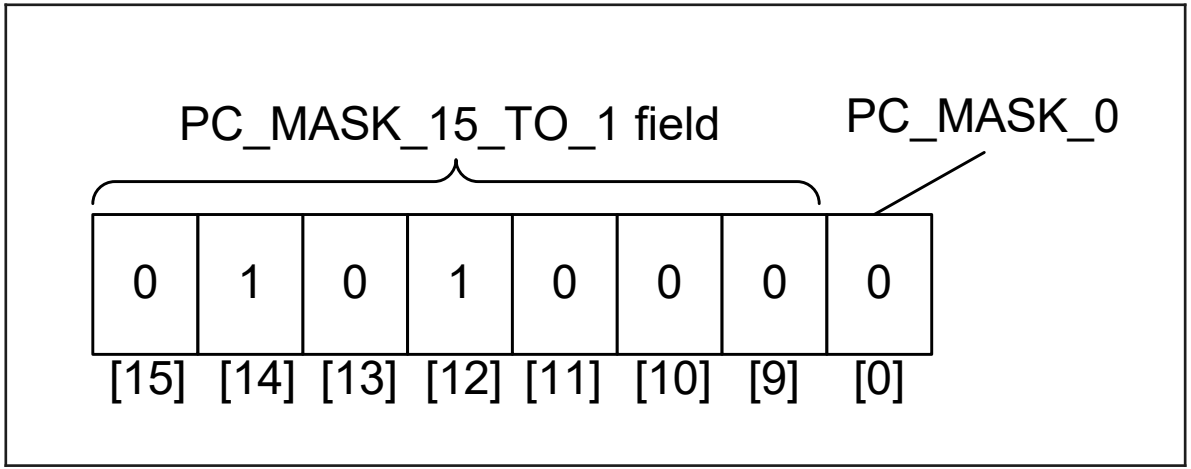
Protection context programming and restrictions (contd.)

PC programming restrictions

- Changes to the PC can be restricted by the PC_MASK[4] field
- Controlled by a secure CPU (Cortex®-M0+)



[1] The main CPU refers to the Cortex®-M7 CPU in the MCU.
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[3] The PC field is located in the MPU_MSx_CTL register.
[4] PC_MASK field is located in the SMPU_MSx_CTL register. PC_MASK_0 is always **0** and cannot set any master.
[5] PCs 4 and 6 are configurable; other PCs are nonconfigurable.

Hint bar

See the XMC7000 MCU family architecture reference manual chapter 6.3 and the XMC7200 MCU registers reference manual for additional details.

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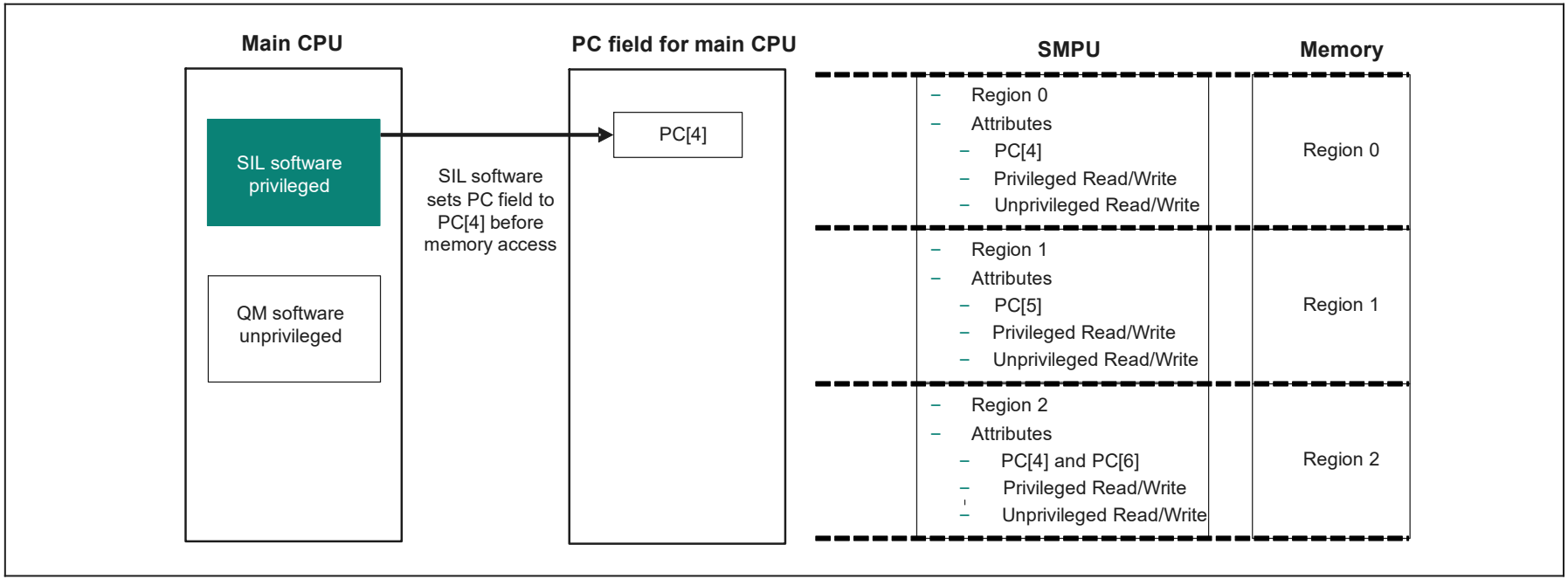
Use case 1

– Software separation between SIL[1] and QM[2]



[1] SIL: Safety integrity level. This software function has safety requirements
[2] QM: Quality management. This software function does not have safety requirements

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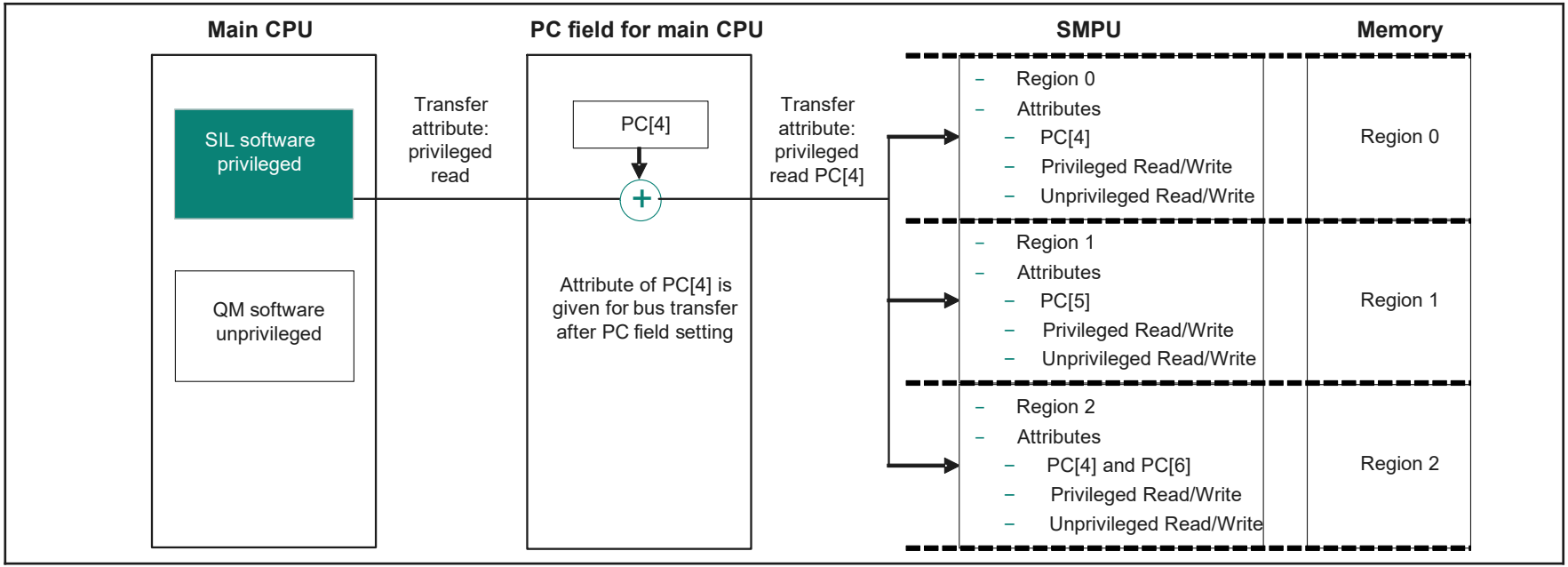
Use case 2

- Software separation between SIL[1] and QM[2]
- Assign PC[4] to SIL[1] software



[1] SIL: Safety integrity level. This software function has safety requirements
[2] QM: Quality management. This software function does not have safety requirements

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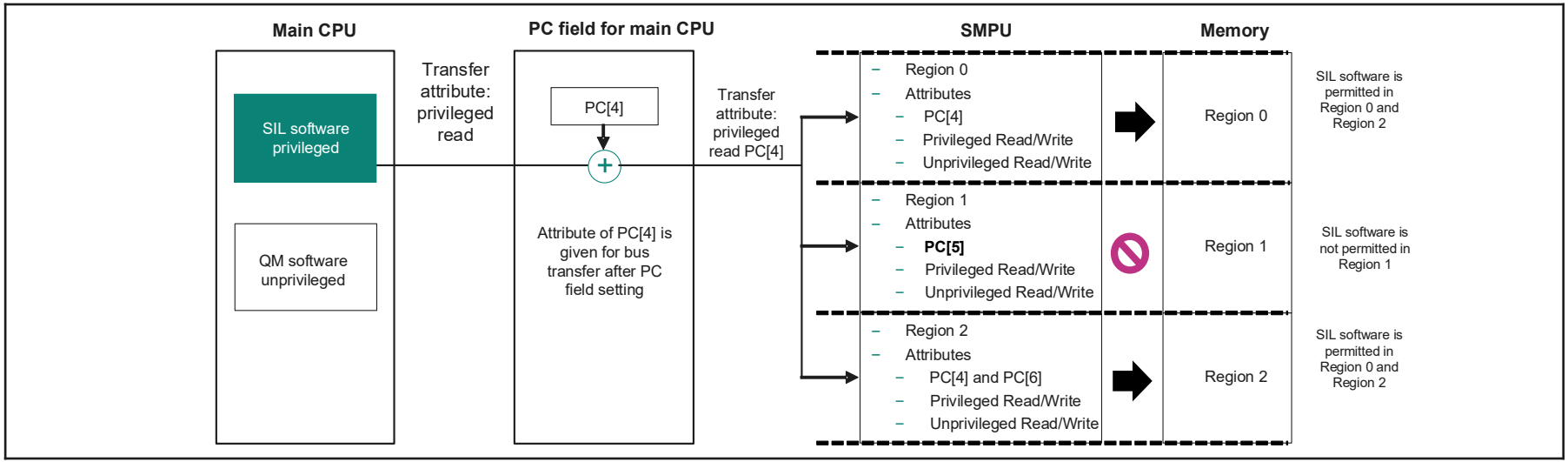
Use case 3

- Software separation between SIL[1] and QM[2]
- Assign PC[4] to SIL[1] software
- Restrict memory access between PCs with SMPU



[1] SIL: Safety integrity level. This software function has safety requirements.
[2] QM: Quality management. This software function does not have safety requirements.

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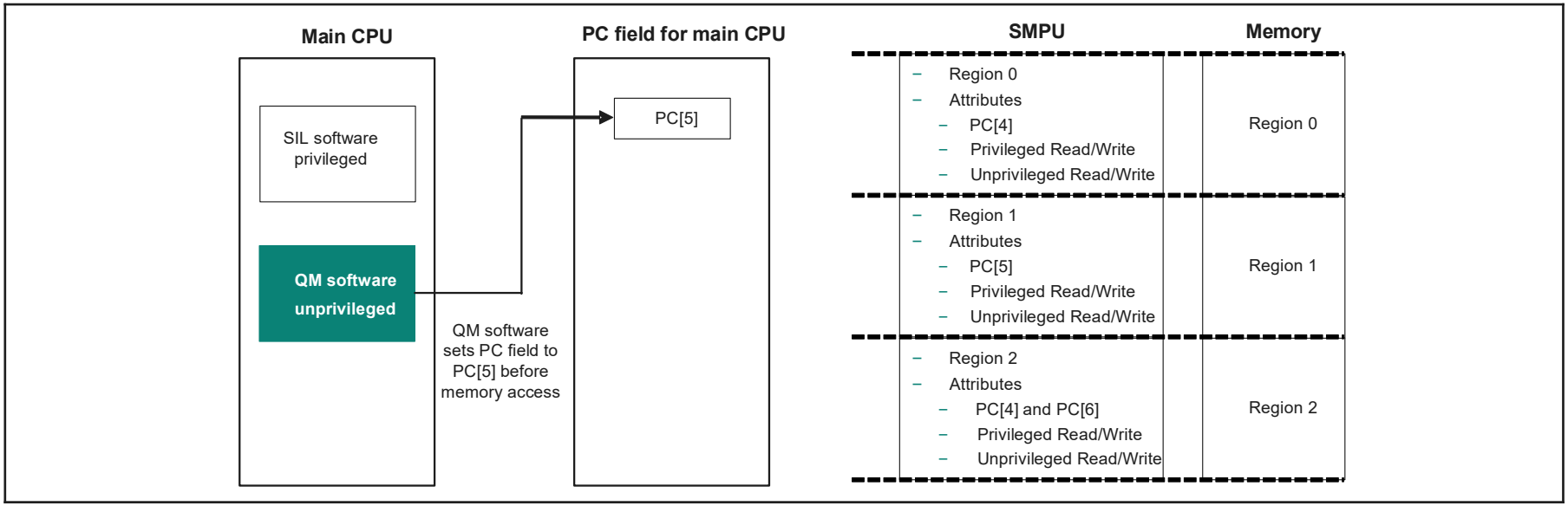
Use case 4

– Software separation between SIL[1] and QM[2]



[1] SIL: Safety integrity level. This software function has safety requirements.
[2] QM: Quality management. This software function does not have safety requirements.

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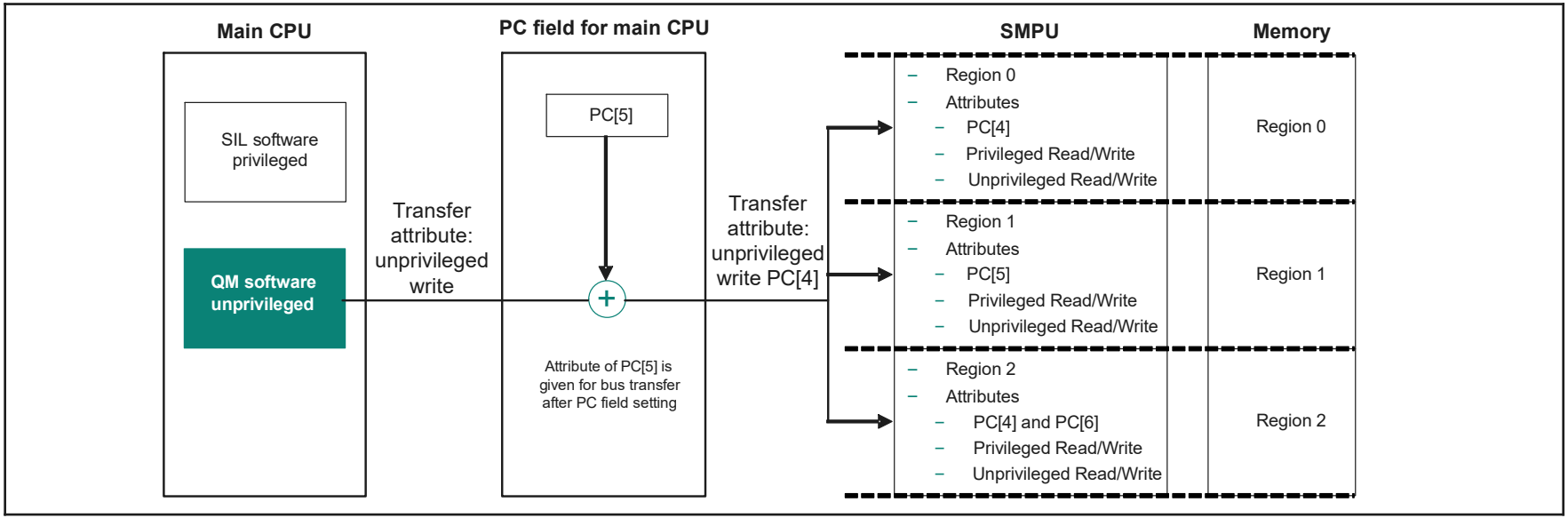
Use case 5

- Software separation between SIL[1] and QM[2]
- Assign PC[5] to QM software



[1] SIL: Safety integrity level. This software function has safety requirements.
[2] QM: Quality management. This software function does not have safety requirements.

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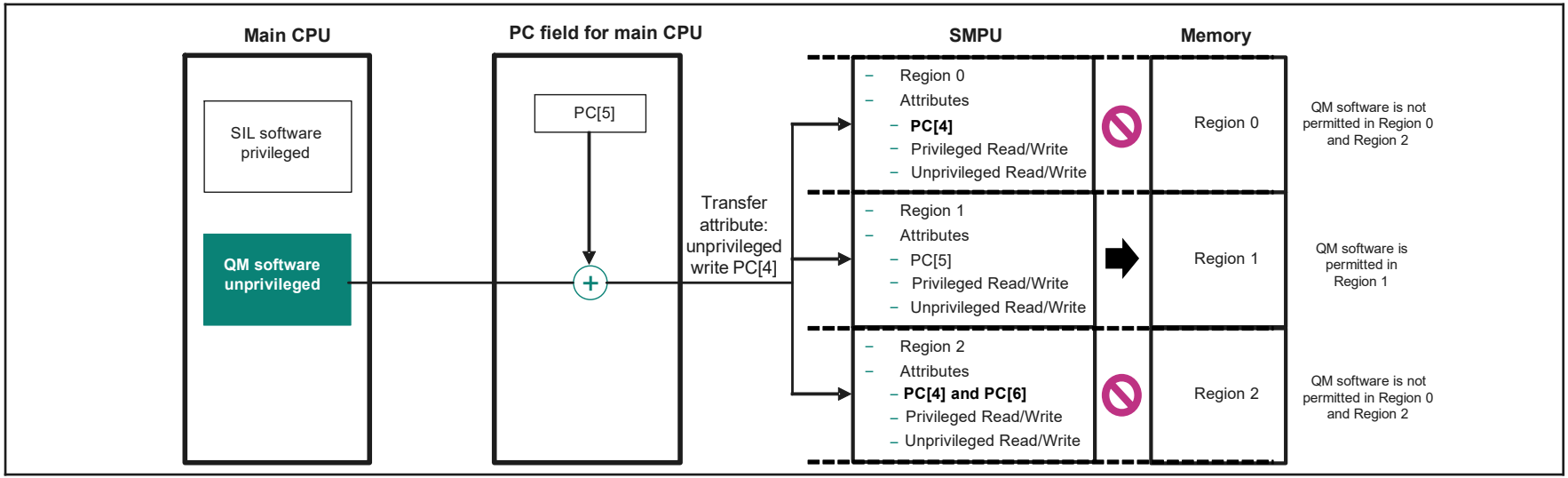
Use case 6

- Software separation between SIL[1] and QM[2]
- Assign PC[5] to QM[2] software
- Restrict memory access between PCs with SMPU



[1] SIL: Safety integrity level. This software function has safety requirements.
[2] QM: Quality management. This software function does not have safety requirements.

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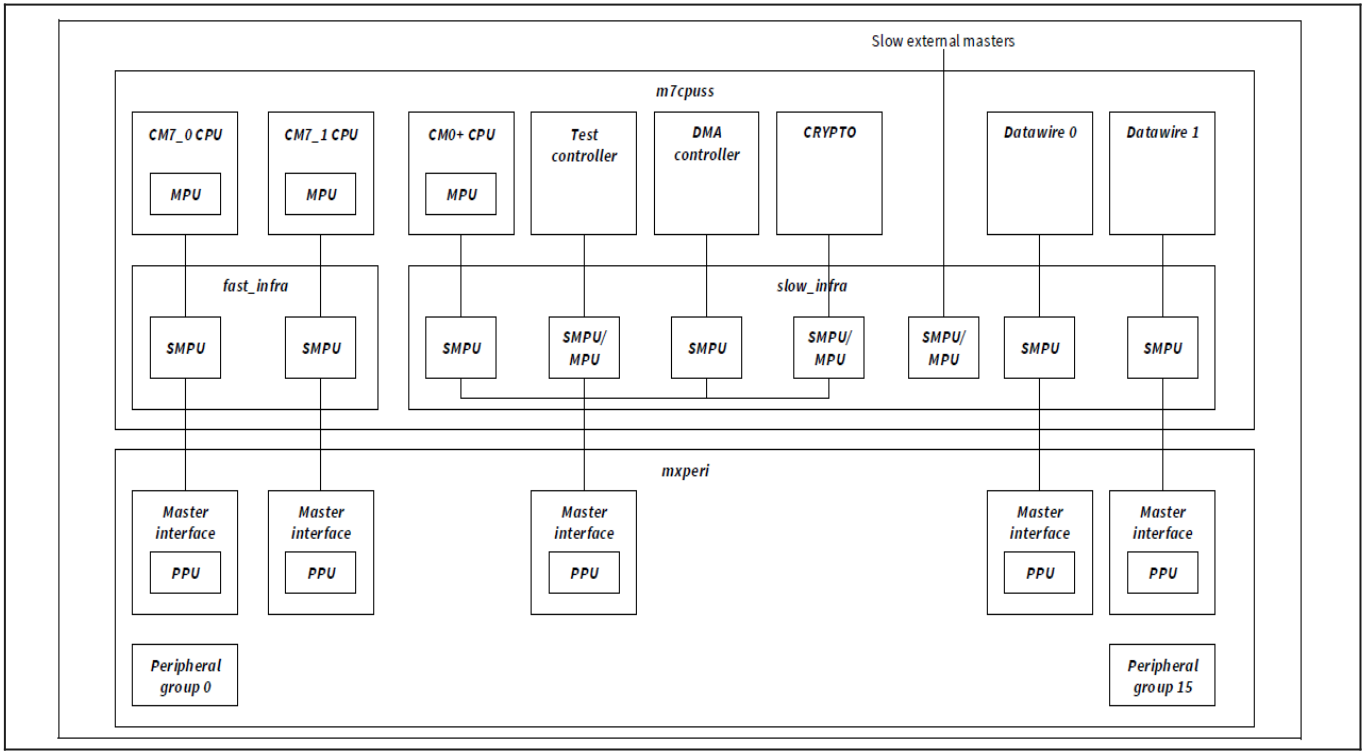
Block diagram of protection unit

Protection unit consists of the following components:



Hint bar

Arm® provides additional supporting material on their webpage at: http://infocenter.arm.com

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Components of protection unit

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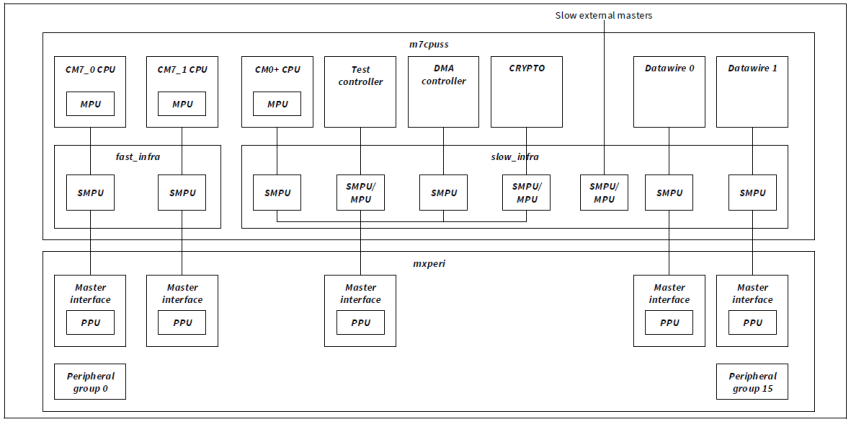
MPU block diagram

MPU

- Provides memory protection
- Associated with a single master
  - Each CPU can independently give different roles
  - P-DMA, M-DMA, and CRYPTO inherit the attribute of programmed transfer
- Up to sixteen regions for XMC7200
- Up to eight regions for XMC7100



Hint bar

- Arm® provides additional supporting material on their webpage at: http://infocenter.arm.com
- See the XMC7000 MCU family architecture reference manual chapter 6 and the XMC7200 MCU registers reference manual for additional details
- See the XMC7000 microcontroller CPU subsystem for additional details
- XMC7200: 16 regions
  XMC7100: 8 regions

[1] The definition of MPU aspect of bus infrastructure follows the Arm® MPU definition.
[2] The test controller is connected to the external debugger.

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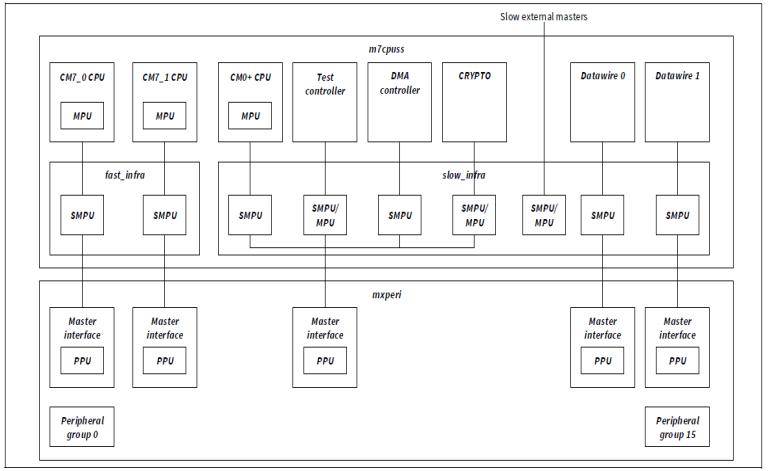
MPU block diagram (contd.)

MPU

- Two types of MPU:
  - Arm® Cortex® -M7 and Cortex® -M0+ CPU
  - Bus infrastructure[1] for the test controller[2]
- Access restriction:
  - Address range, Read/Write, Execute, and Privileged/Unprivileged
- The region is equally divided into eight subregions



Hint bar

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  XMC7100: 8 regions

[1] The definition of MPU aspect of bus infrastructure follows the Arm® MPU definition.
[2] The test controller is connected to the external debugger.

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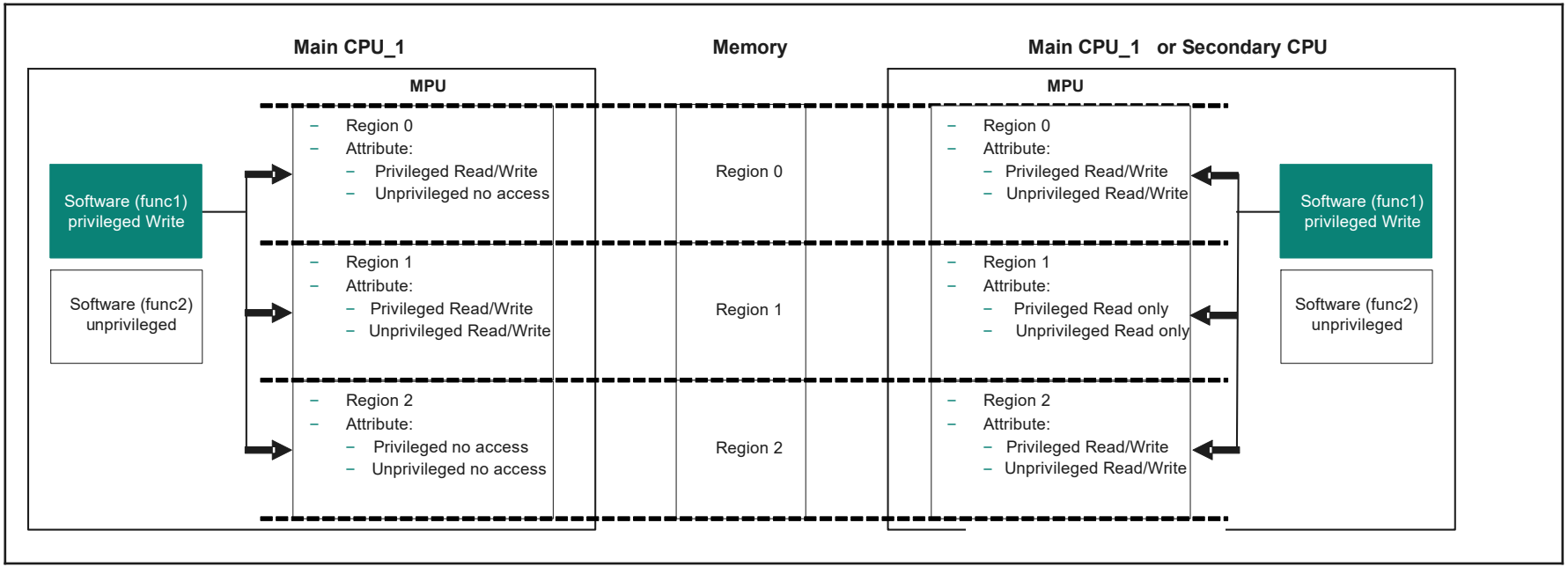
Use case 1

– Software (func1) of both CPUs accesses to memory with privileged write



[1] Main CPU_0 is the Cortex® - M7_0 in XMC7000
[2] Main CPU_1 is the Cortex® - M7_1 in XMC7000

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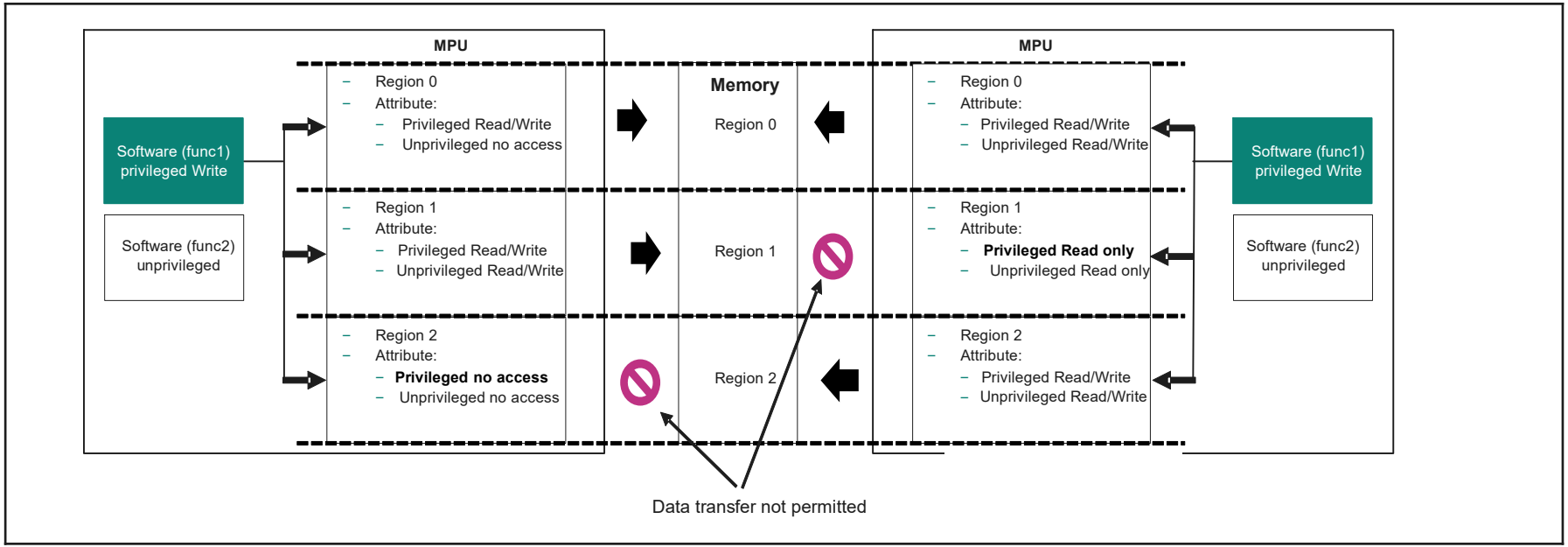
Use case 1 (contd.)

- Software (func1) of Main CPU_0 is allowed access to Region 0 and Region 1
- Software (func1) of Main CPU_1 or secondary CPU is allowed access to Region 0 and Region 2



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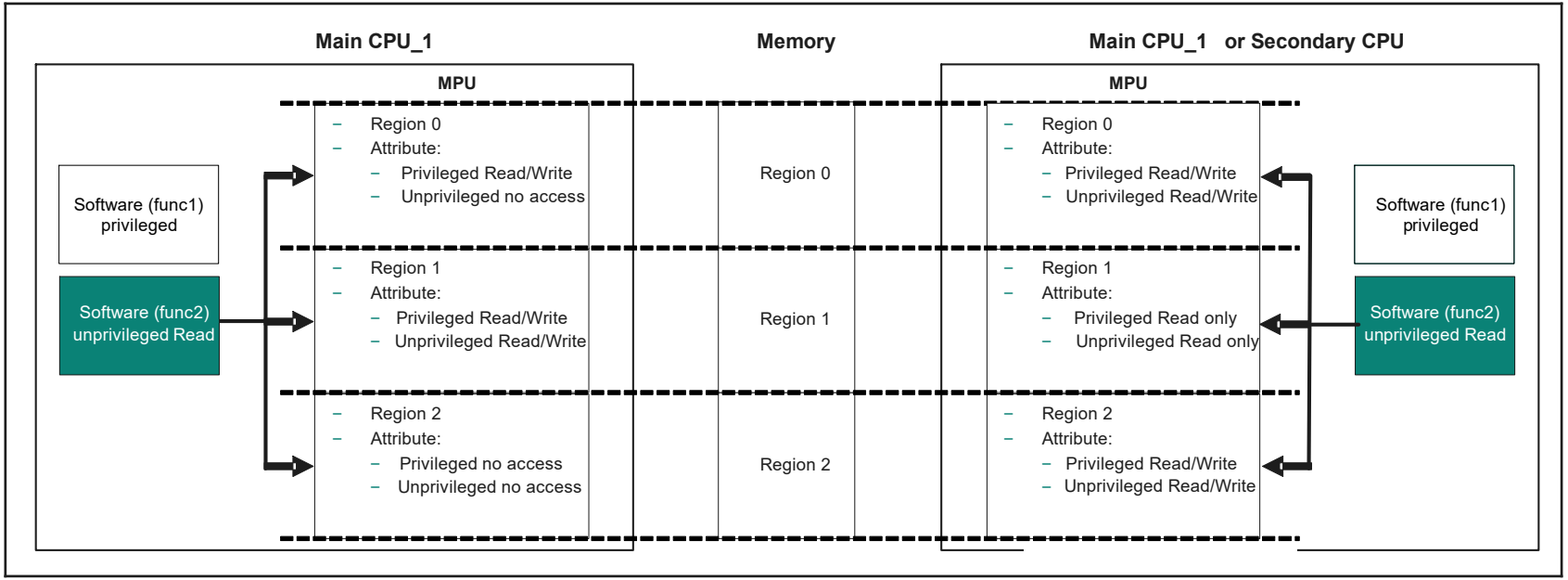
Use case 2

– Software (func2) of both CPUs accesses memory with unprivileged read



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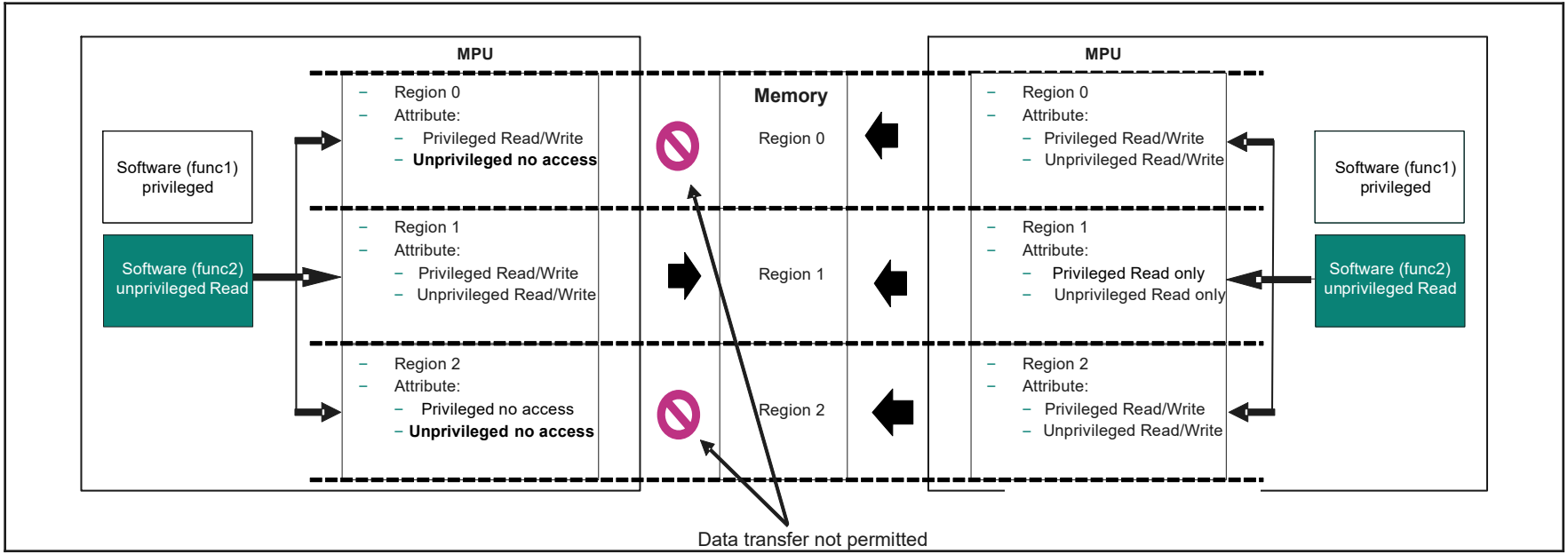
Use case 2 (contd.)

- Software (func2) of Main CPU_0 is allowed access to Region 1
- Software (func2) of Main CPU_1 or secondary CPU is allowed access to all regions



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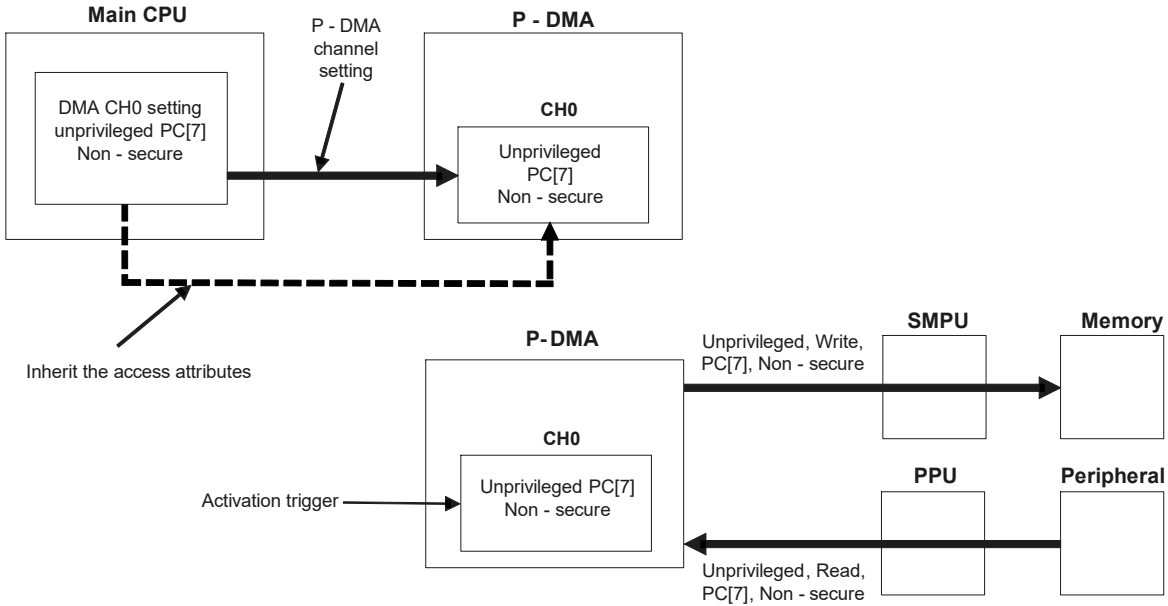
P-DMA/M-DMA/Crypto access attribute

Inherit the access control attributes of the programmed bus transfer for these bus transfer attributes.



Hint bar

See the XMC7000 MCU family architecture reference manual chapter 6 for additional details.

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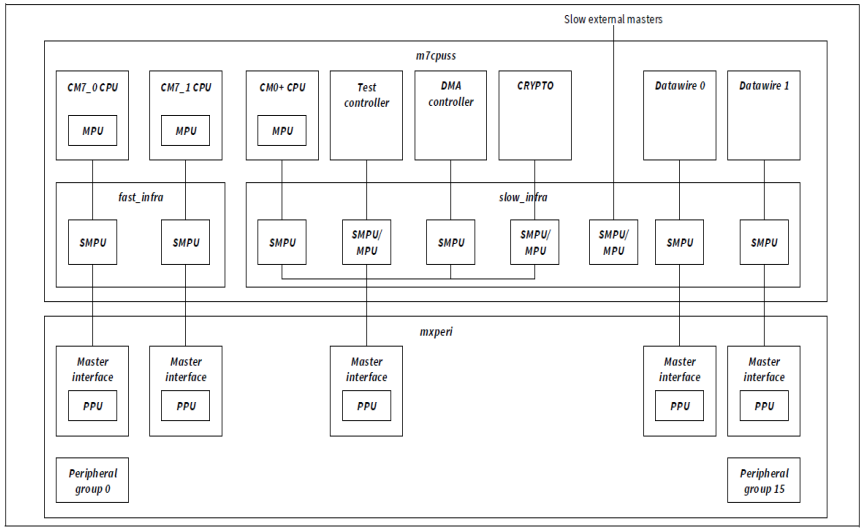
SMPU block diagram

SMPU

- Provides memory protection
- Shared by all bus masters
- Includes 16 regions
- Access restriction to:
  - Address range
  - Read/Write
  - Execute
  - Privileged/unprivileged
  - Secure/non-secure
  - Protection context
- The region is equally divided into eight subregions
- Protection pair: slave and master protection structures



Hint bar

- See the XMC7000 MCU family architecture reference manual chapter 6 and the XMC7200 MCU registers reference manual for additional details
- See the XMC7000 microcontroller CPU subsystem for additional details

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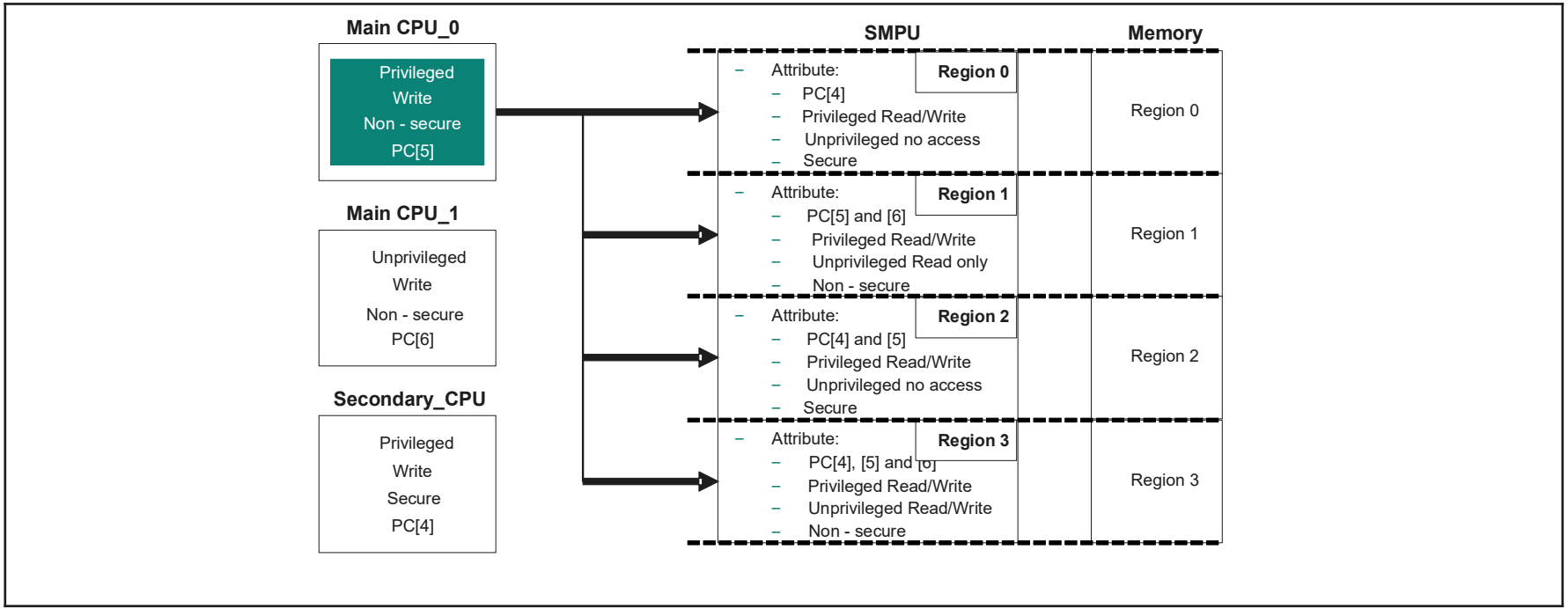
Use case 1

Main CPU_0 software accesses memory with privileged write, non-secure, and PC[5].



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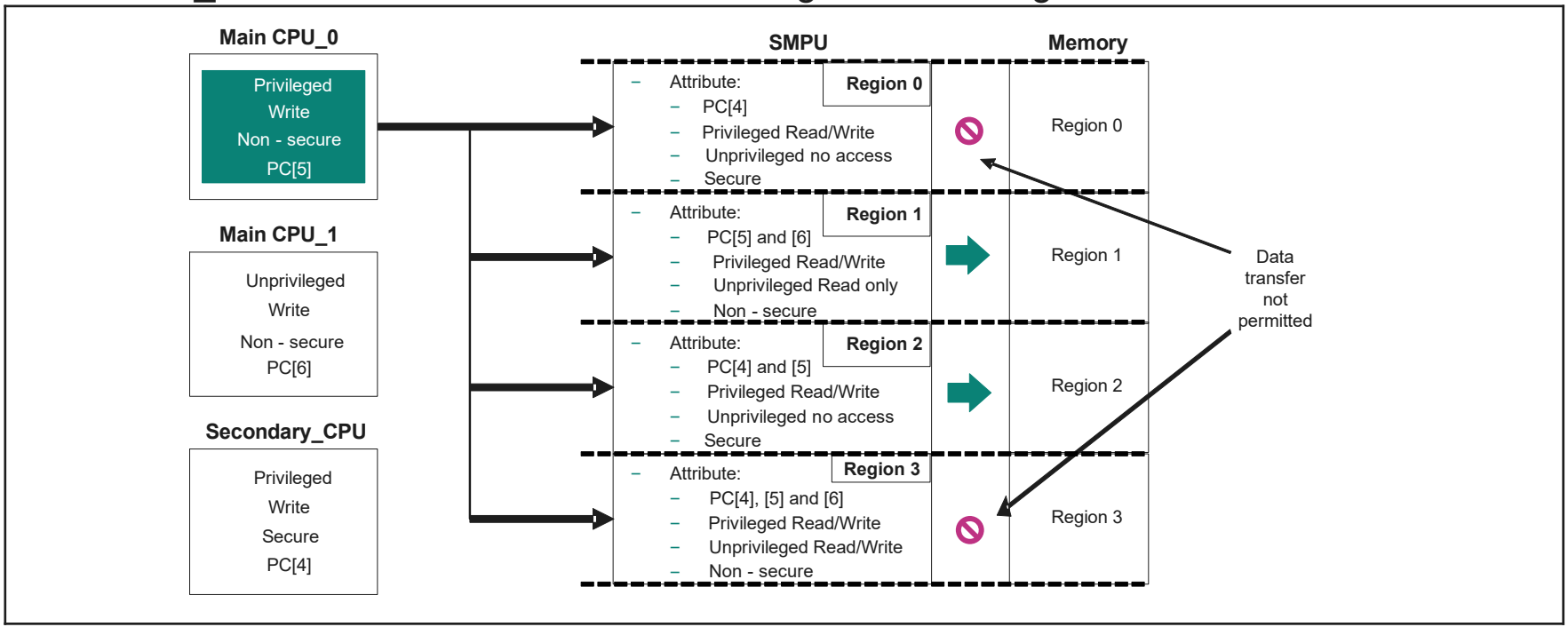
Use case 1 (contd.)

Main CPU_0 software is allowed access to Region 1 and Region 3.



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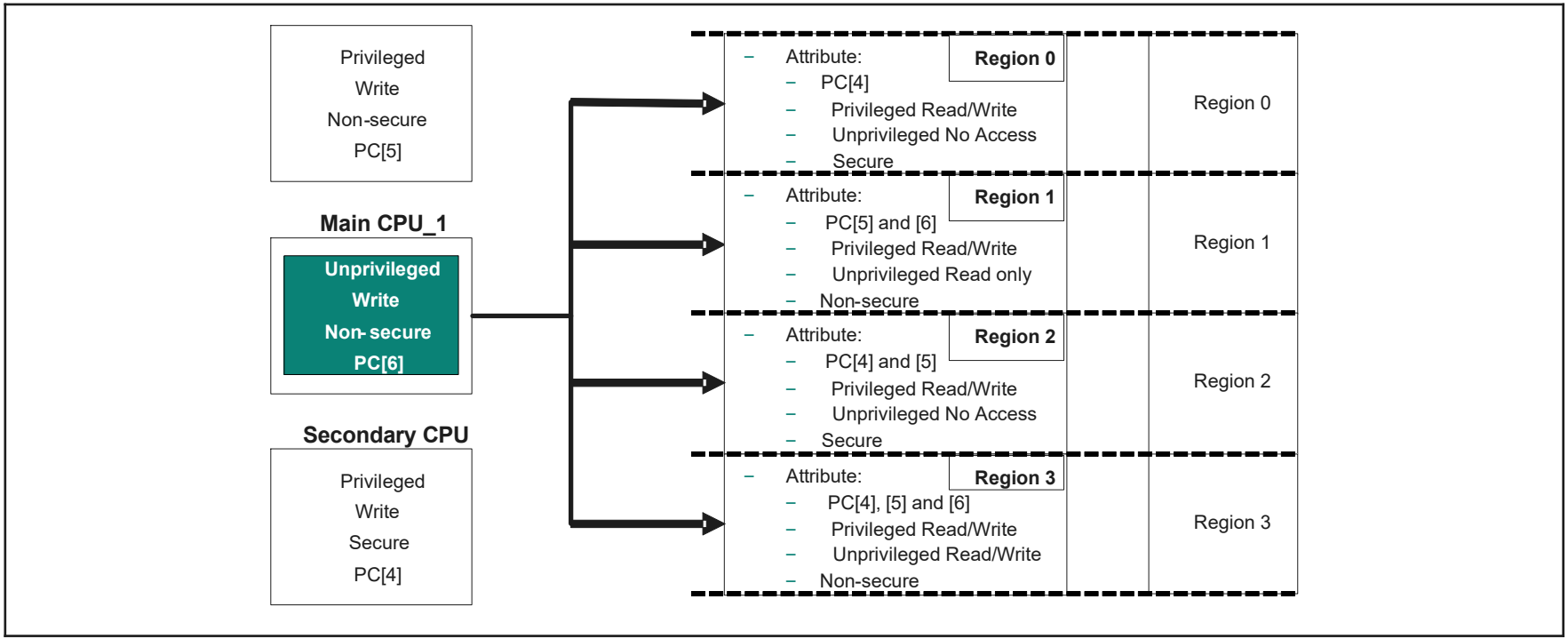
Use case 2

Main CPU_1 software accesses to memory with unprivileged write, non-secure, and PC[6].



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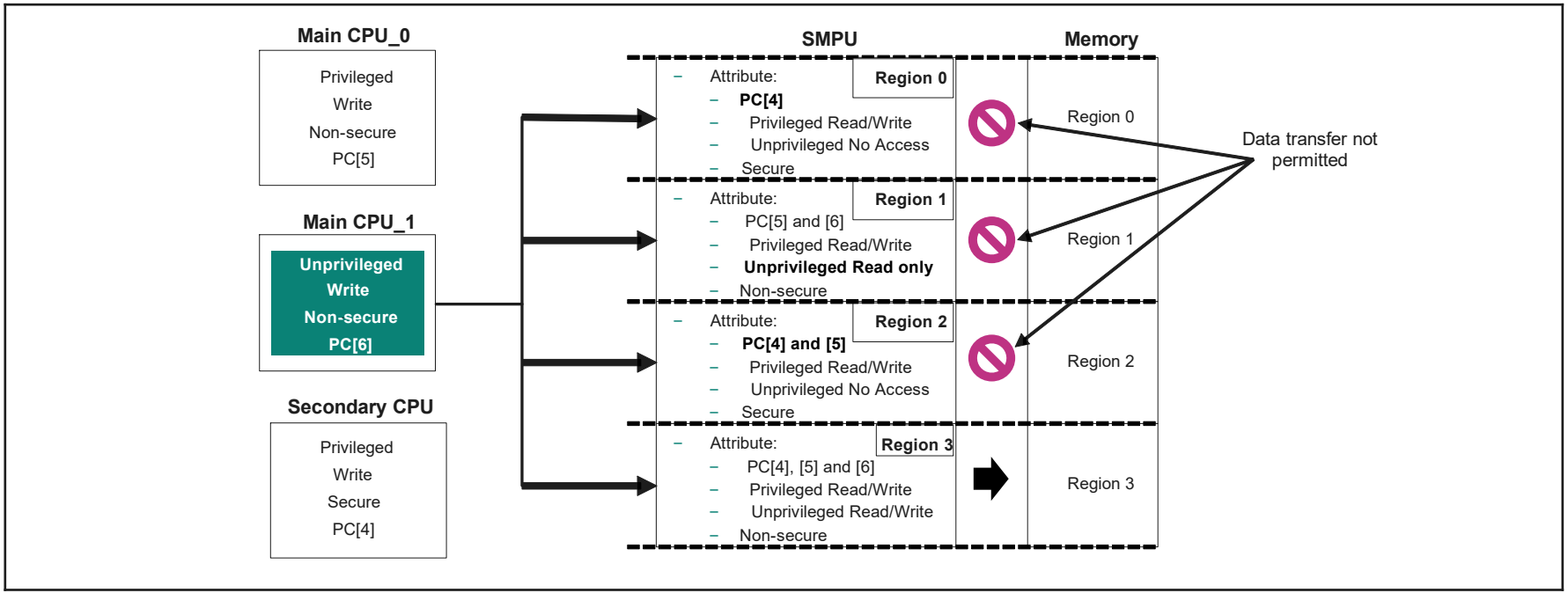
Use case 2 (contd.)

Main CPU_1 software is allowed access to Region 3.



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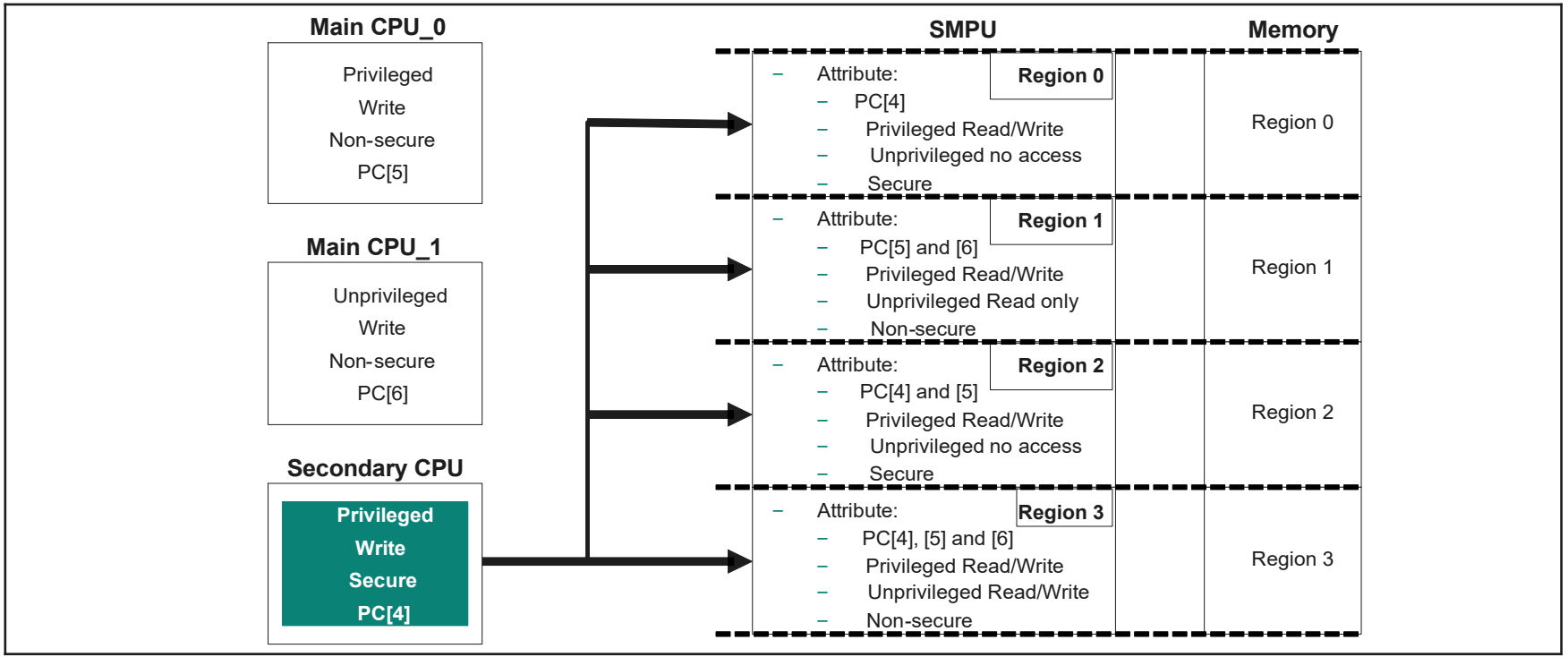
Use case 3

Secondary CPU software accesses to memory with privileged write, Secure, and PC[4].



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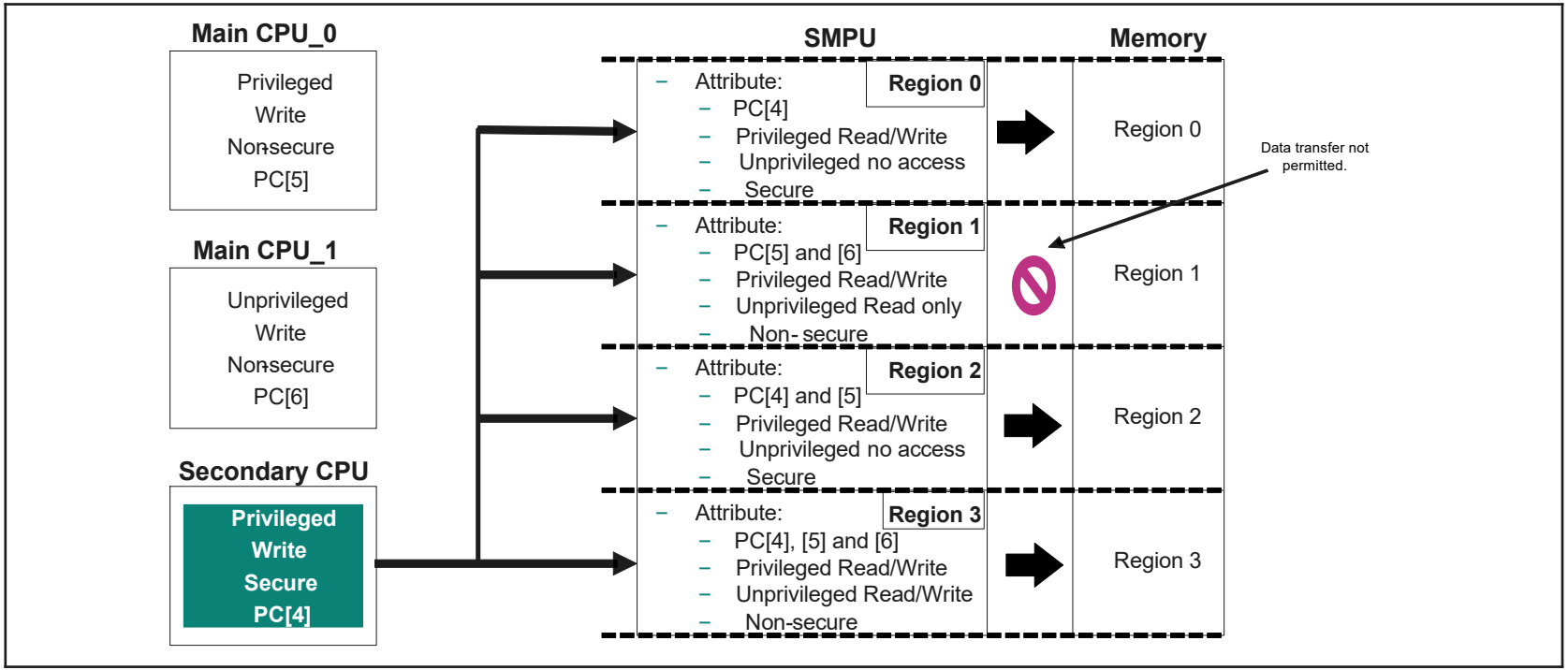
Use case 3 (contd.)

Secondary CPU software is allowed access to Region 0, Region 2, and Region 3.



Note: Non-secure attribute allows both non-secure and secure access.

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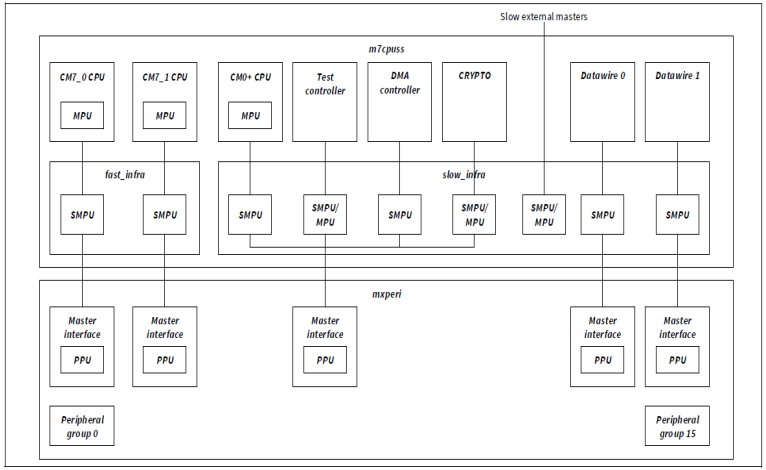
PPU block diagram

PPU

- Provides peripheral protection
- Shared by all bus masters
- Two PPU types:
  - Fixed PPU structure[1]
  - Programmable PPU structure[2]
- Access restriction to:
  - Address range
    (restricted to programmable PPU)
  - Read/Write
  - Privileged/unprivileged
  - Secure/non-secure
  - Protection context
  - Applies different setting for each PC

[1] Protects the address range of known resources.
[2] Protects the address range of specific resources.



Hint bar

- See the XMC7000 MCU family architecture reference manual chapter 6 and chapter 6.4.7 (PPU), for more details on SRAM and ECC and XMC7200 MCU registers reference manual for additional details
- Fixed structures take precedence over programmable structures

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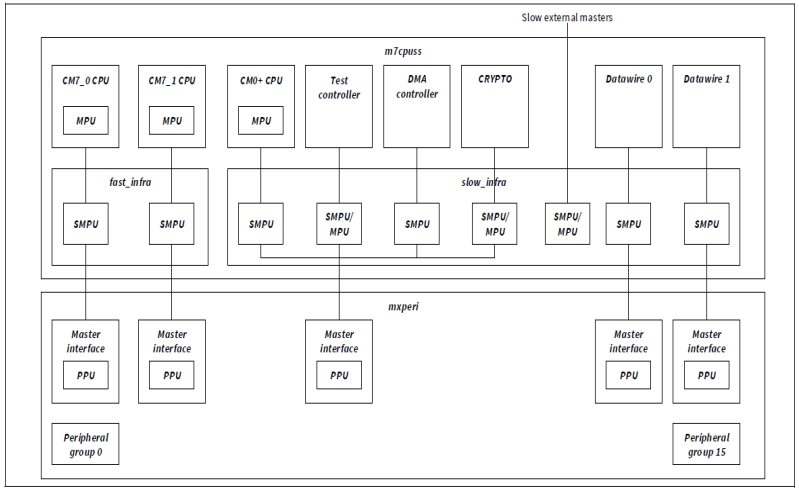
PPU block diagram (contd.)

- Protection pair: slave and master protection structures
- Protection information uses a single SRAM with ECC



[1] Protects the address range of known resources.
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- Fixed structures take precedence over programmable structures

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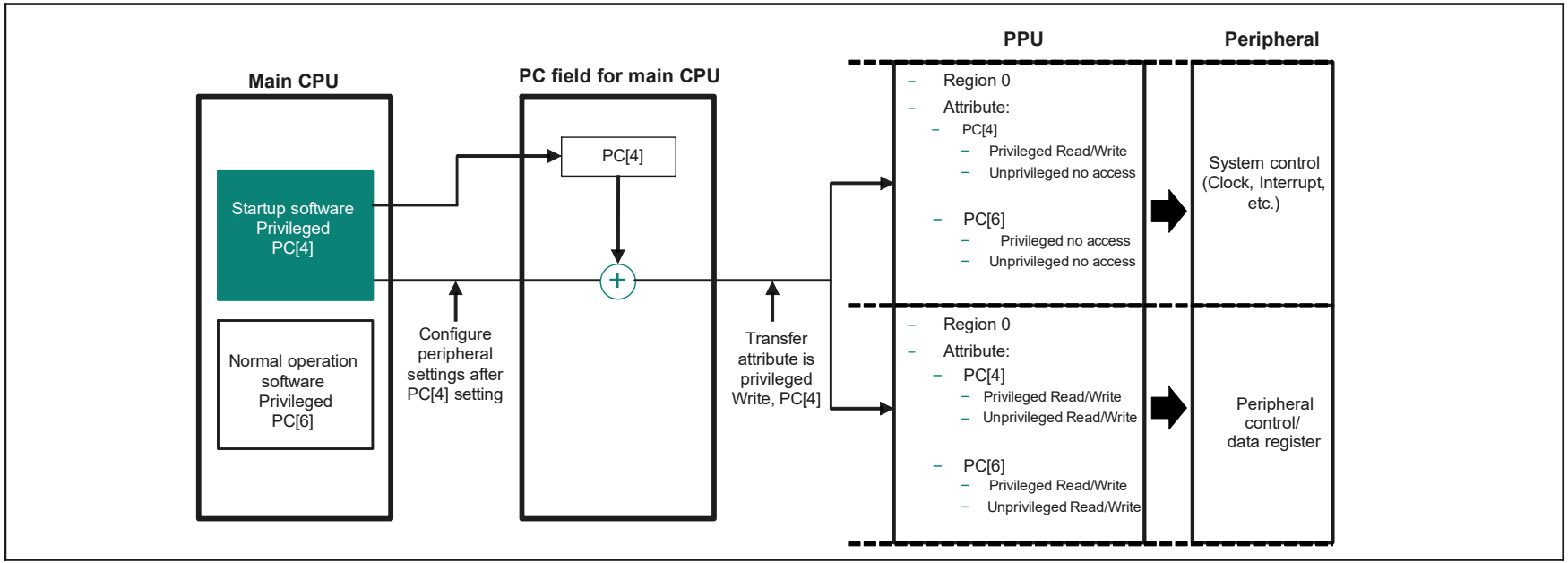
Use cases

- Execute system settings such as clock and initial setting of peripheral in startup software at power-up
- Startup software: Privileged, PC[4] access to peripheral



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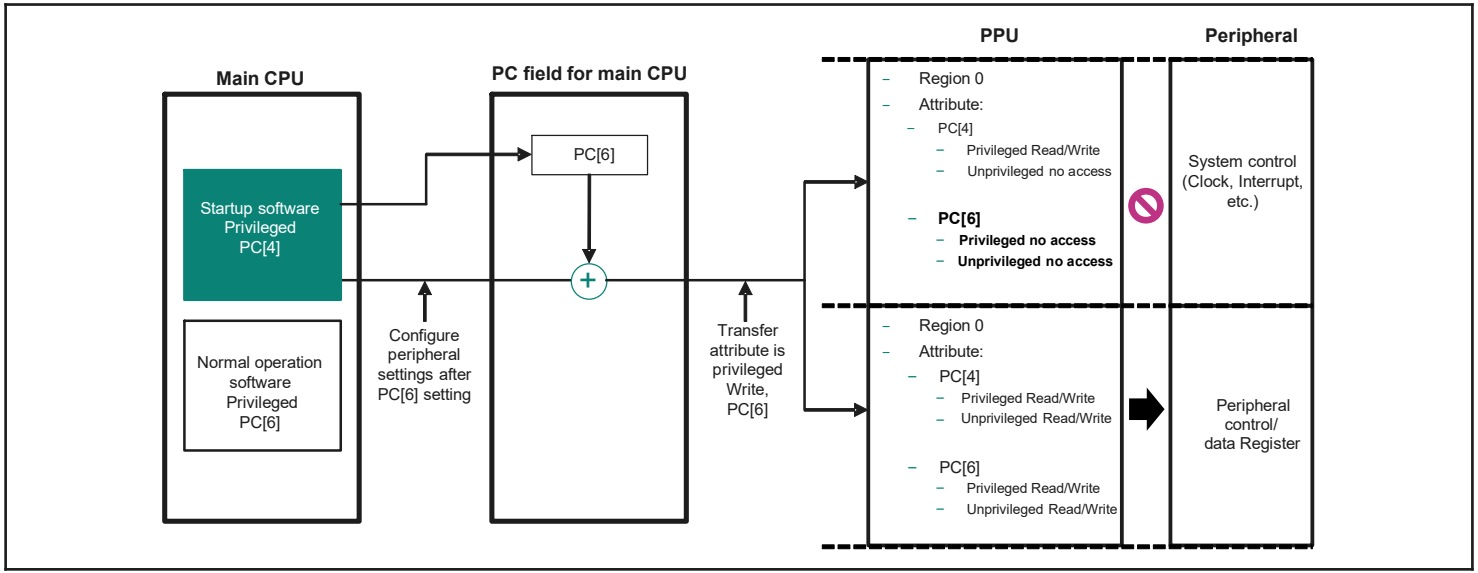
Use cases (contd.)

- Transfer to normal operation software after initial setting and startup software is not executed
- Normal operation software: Privileged, PC[6] access to peripheral



Hint bar

Advantage:

Prevents erroneous change of system settings by applying different access attributes between the initial setting and normal setting.

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SWPU

SWPU is used to access restrictions to flash (write[1]) and eFuse (read/write)

- SWPU prevents malicious or unintended access to flash or eFuse
- SWPU has three protection units:
  - FWPU: Flash Write Protection Unit. (Up to 16 regions)
  - ERPU: eFuse Read Protection Unit. (Up to 4 regions)
  - EWPU: eFuse Write Protection Unit. (Up to 4 regions)
- SWPU has two configuration parts
  - Boot protection: It cannot be updated
  - Application protection: It is additional access restrictions specific to the application
- SWPU is read during the boot process from SFlash and stores it in RAM

Hint bar

See the XMC7000 MCU family architecture reference manual chapter 6.5 for additional details.

[1] Program and Erase

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SWPU (contd.)

- Access restriction for the following:
  - Address range
  - Read/Write
  - Privileged/unprivileged
  - Secure/non-secure
  - Protection context
- Protection pair, slave and master protection structures

Hint bar

See the XMC7000 MCU family architecture reference manual chapter 6.5 for additional details.

[1] Program and Erase

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SWPU structure (application protection)

SWPU is stored in SFlash

SWPU	Field Name	Size	Description
	Object Size	4 bytes	Number of configured elements
FWPU	N_FWPU	4 bytes	Number of FWPU objects. Up to 16 regions
	FWPU0_SL_ADDR	4 bytes	Configures the FWPU0 base address
	FWPU0_SL_SIZE	4 bytes	Configures the FWPU0 region size and FWPU0 enable
	FWPU0_SL_ATT	4 bytes	Configures the FWPU0 slave attribute
	FWPU0_MS_ATT	4 bytes	Configures the FWPU0 master attribute
	:	4 bytes	
ERPU	N_ERPU	4 bytes	Number of ERPU objects. ERPU has up to four regions.
	ERPU0_SL_OFFSET	4 bytes	Configures the ERPU0 base address offset
	ERPU0_SL_SIZE	4 bytes	Configures the ERPU0 region size and ERPU0 enable
	ERPU0_SL_ATT	4 bytes	Configures the ERPU0 slave attribute
	ERPU0_MS_ATT	4 bytes	Configures the ERPU0 master attribute
	:		
EWPU	N_EWPU	4 bytes	Number of EWPU objects. EWPU has up to four regions.
	EWPU0_SL_OFFSET	4 bytes	Configures the EWPU0 base address offset
	EWPU0_SL_SIZE	4 bytes	Configures the EWPU0 region size and ERPU0 enable
	EWPU0_SL_ATT	4 bytes	Configures the EWPU0 slave attribute
	WPU0_MS_ATT	4 bytes	Configures the EWPU0 master attribute
	:		

Hint bar

See the XMC7000 MCU family architecture reference manual chapter 6.5 for additional details.

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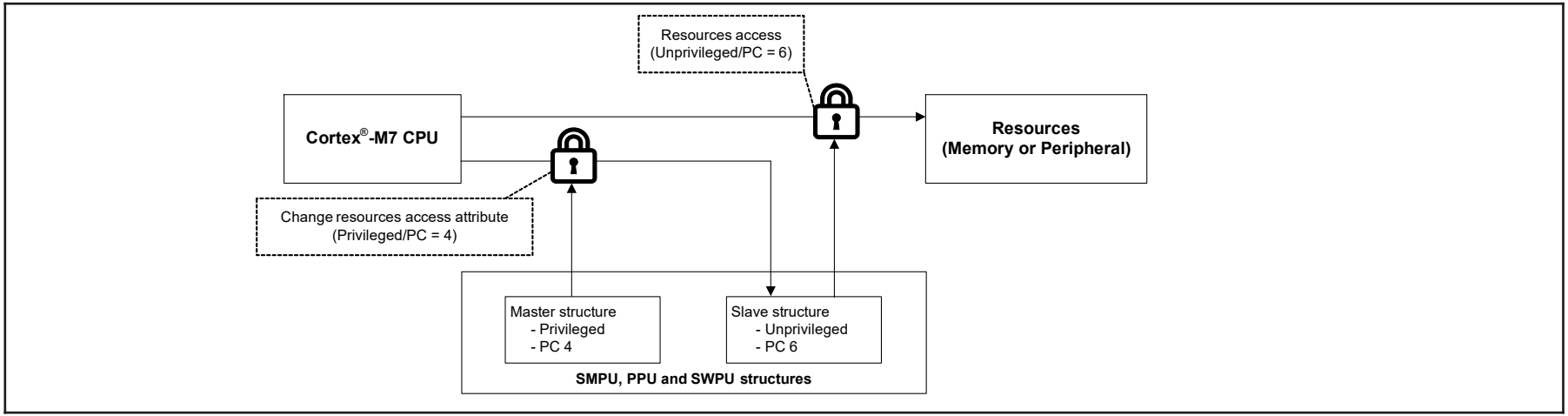
Protection pair

SMPU, PPU, and SWPU have a protection pair for protection of protection structures

- Master structure: Protection of slave structure
- Slave structure: Protection of resources
- Change slave setting attributes by master setting attributes



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Protection violation

MPU, SMPU, and PPU detect a restricted transfer; the bus transfer results in a bus error.

- Access is evaluated by each protection unit in the following order:
  - MPU (High) > SMPU > PPU (Low)
- The slave address regions in programmable PPU may overlap with other slave address regions. In this case, access is evaluated by the PPU in the following order:
  - PPU master structure (High) > Programmable slave structures > Fixed slave structure (Low)
- The bus transfer will not reach its target

Violation information is reported to the fault reporting structure.

- Violation address
- Bus transfer attribute
- Accessed bus master

Hint bar

See the Fault structure training section references for additional details.

Advantage

- Prevents erroneous writing by not allowing transfer
- Possible analysis of violation transfer

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Revision history

Document revision	Date	Description of change
**	2022-03-24	Initial release.
*A	2026-01-02	Migrated to the latest empower training presentation template.

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