Customer training workshop

XMC7000 microcontroller– Program and debug interface

Target products

Target product list for this training material:

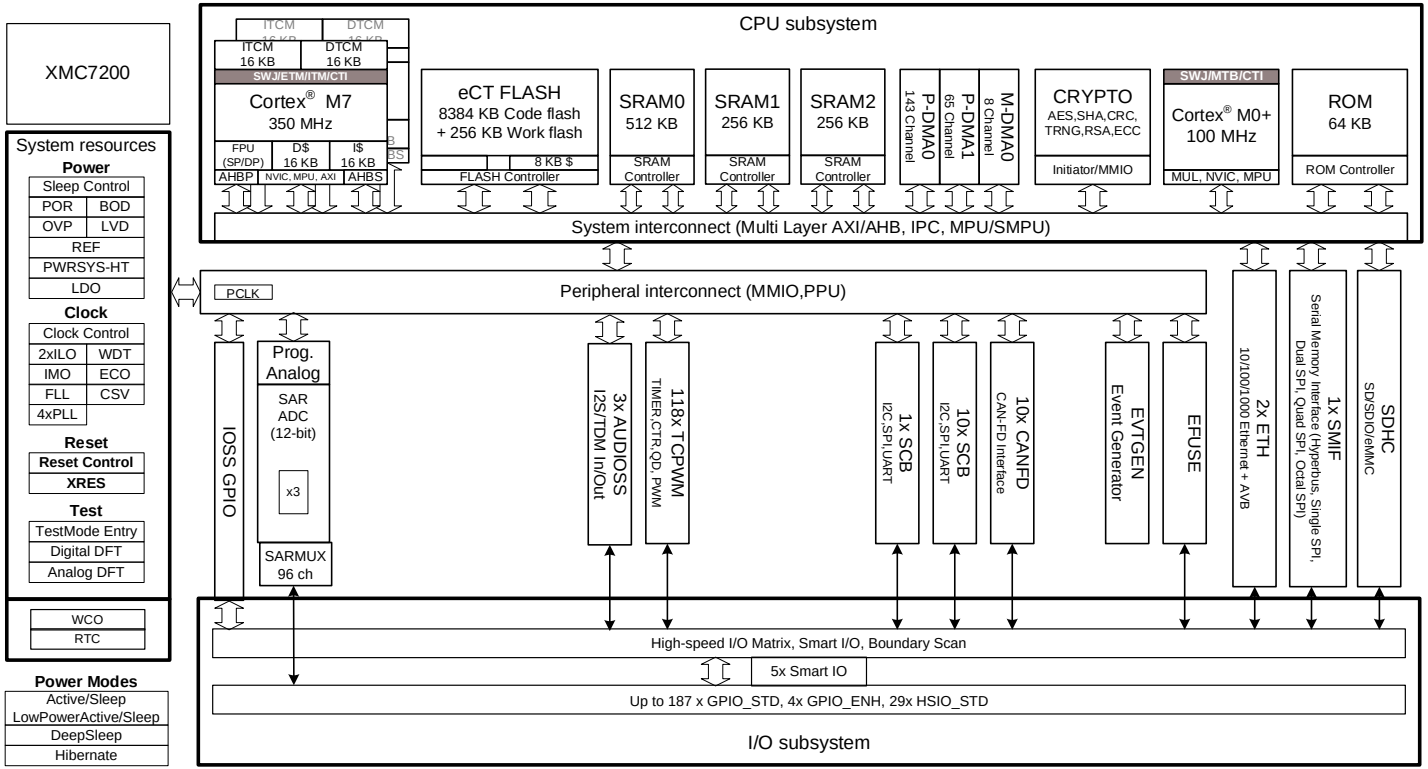
Family category	Series	Code flash memory size
XMC7200	XMC7200-8M	Up to 8384 KB
XMC7100	XMC7100-4M	Up to 4160 KB

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XMC7200 - 8M family

Introduction to XMC7200-8M

› The program and debug interface is part of the CPU subsystem



Hint Bar

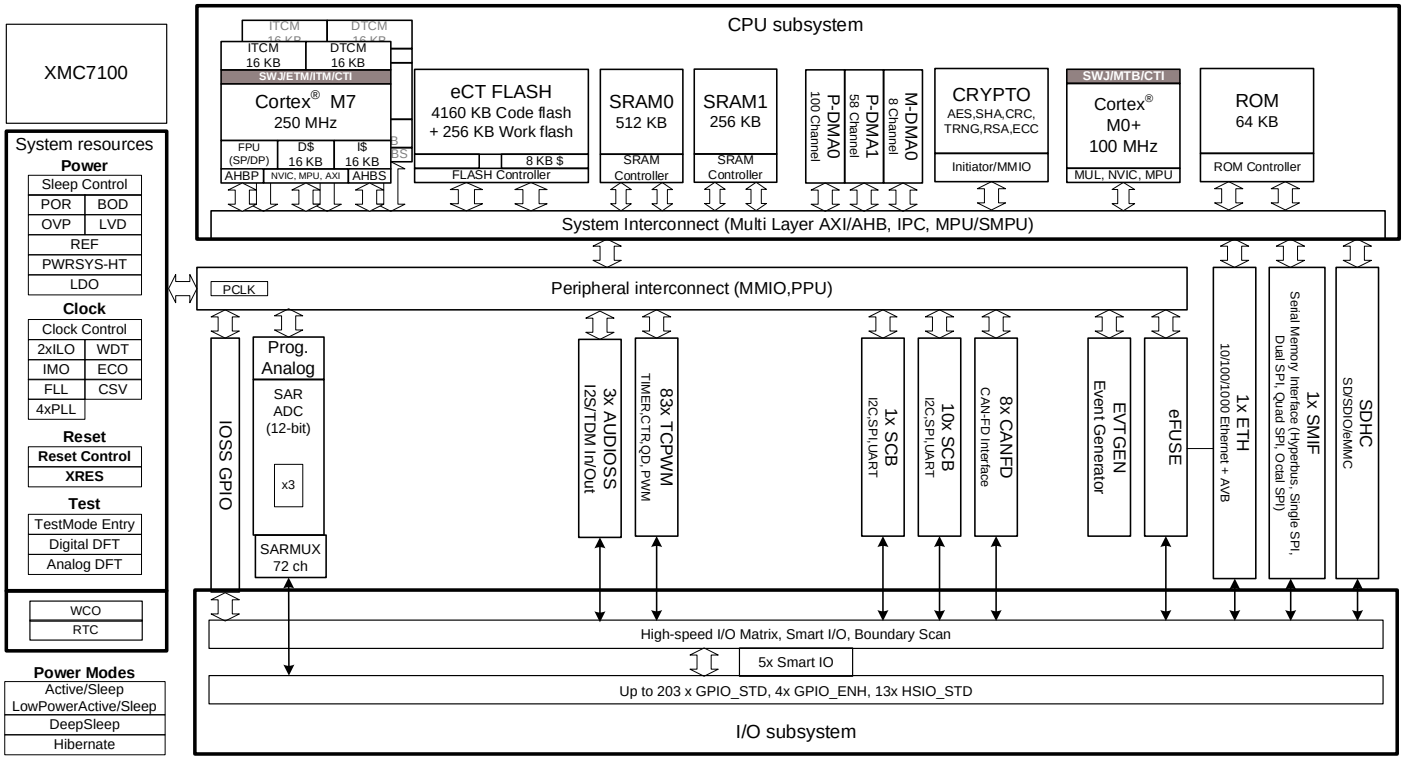
Review XMC7000 TRM chapter 34 for additional details

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XMC7100 - 4M family

Introduction to XMC7100-4M

› The program and debug interface is part of the CPU subsystem



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Review XMC7000 TRM chapter 34 for additional details

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Program and debug interface overview

- The program and debug interface is a communication gateway for an external device to perform programming and debugging
- The external device includes a
  - Infineon-supplied programmer
  - Third-party programmer and debugger
- Communication protocol between the external device and XMC7000 microcontroller is supplied by
  - Serial wire debug (SWD)
  - Joint Test Action Group (JTAG)

Hint Bar

Review TRM chapter 34 and CoreSight documentation for additional details

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Multi-core debug for XMC7000

- Arm® Cortex®-M0+ Core debug components
  - Cross-triggering interface (CTI), four hardware breakpoints, and two watchpoints
- Arm® Cortex®-M7 Core debug components
  - CTI, six hardware breakpoints, and four watchpoints
- Enables multi-core debug
  - Three CTIs connected via cross-triggering matrix (CTM)
  - Start or stop CM0+/CM7 at the same time
  - Start or stop instruction tracing based on whether or not the trace buffer is full, or on the break
- Debug and access port (DAP) security
  - Four access ports (APs) each can be independently disabled
  - eFuse (permanent)
  - System AP is protected by MPU

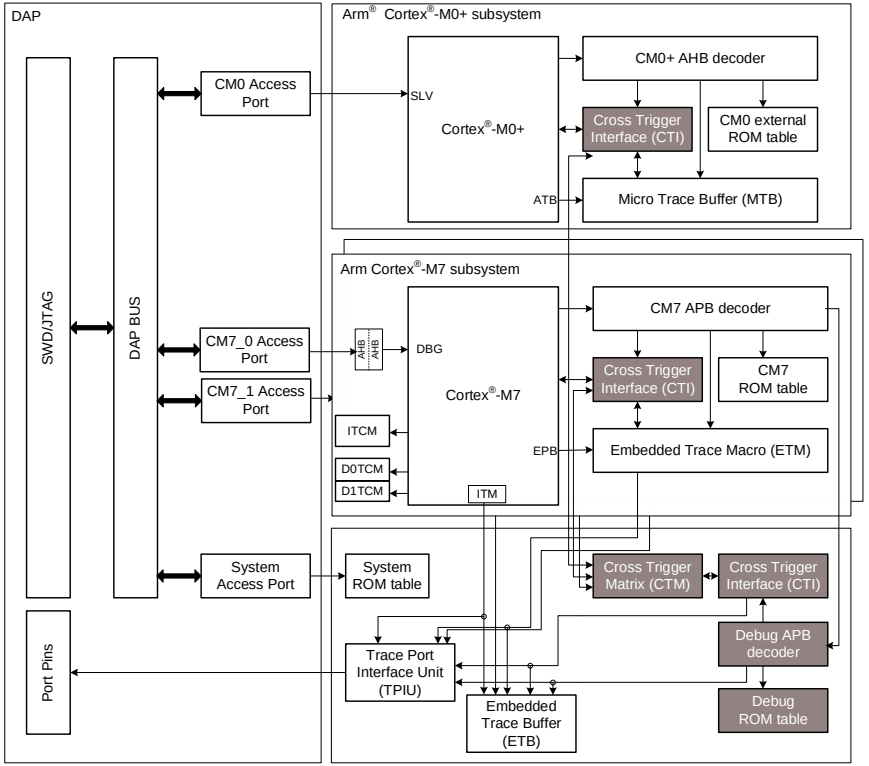
Hint Bar

Review TRM chapter 34 and CoreSight documentation for additional details

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Multi-core debug for XMC7000

Program and debug interface



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Review TRM chapter 34 and CoreSight documentation for additional details

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Tracing for XMC7000

- Arm® Cortex®-M0+
  - Micro trace buffer (MTB) for tracing and storing instructions
- Arm® Cortex®-M7
  - Embedded trace macrocell (ETM) for tracing instructions
  - Embedded trace buffer (ETB) for tracing instructions and storing them in a local SRAM
  - Instrumentation trace macrocell (ITM) for tracing output
  - Trace port interface unit (TPIU) for tracing information from the chip to an external trace port analyzer
    - Parallel (4 pins, multiplexed with GPIO and clock pin)

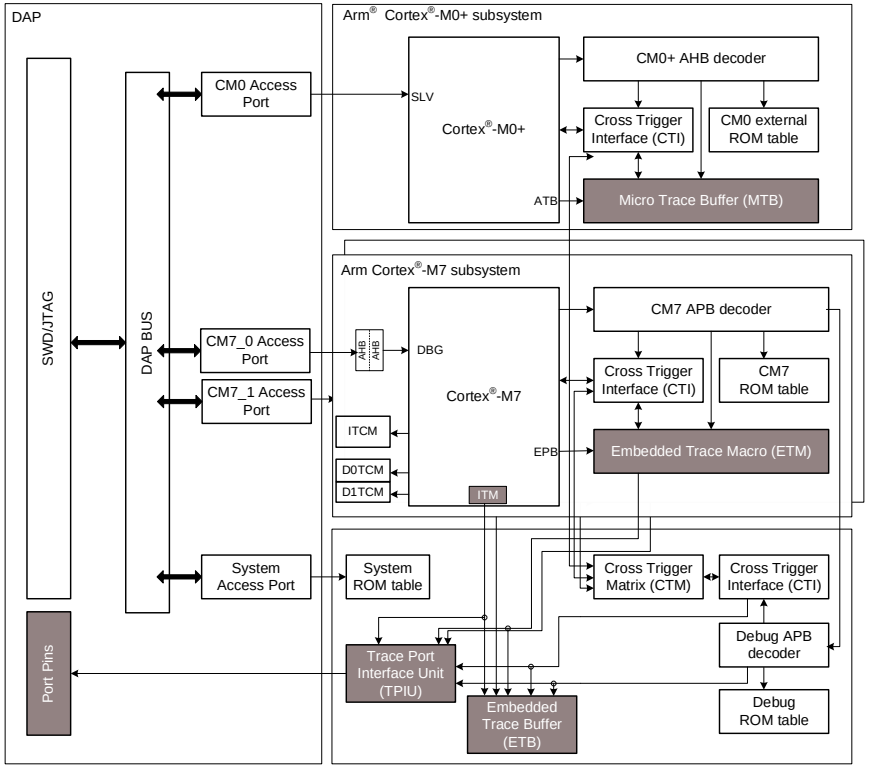
Hint Bar

Review TRM chapter 34

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Tracing for XMC7000

Program and debug interface



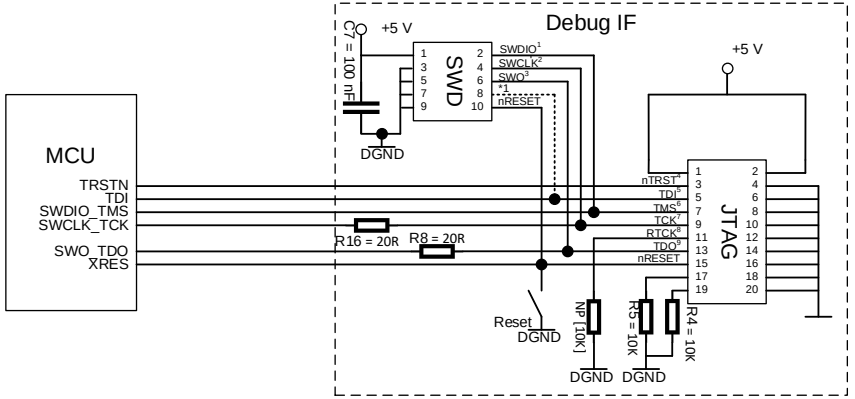
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Review TRM chapter 36 and CoreSight Documentations for additional details

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Serial wire debug (SWD) and JTAG interface

- The SWD protocol is a packet-based serial transaction protocol
- The JTAG controller and interface are compliant to IEEE-1149.1-2001
  - The test access port (TAP) interface is used to control the values in the boundary scan cells
  - Boundary scan test supported



*1: Only needed if SWD connector should also provide JTAG lines

[1] Serial wire data I/O
[2] Serial wire clock
[3] Serial wire output
[4] Test reset
[5] Test data in
[6] Test mode select
[7] Test clock
[8] Return test clock
[9] Test data out

Debug interface pin configuration on Boot ROM

After reset, the debug pins remain in high-impedance mode until Boot ROM initializes them as follows:

Pin name	Input enable	Drive mode
swj_trstn	Yes	Internal Pull-up
swj_swo_tdo	Yes	Strong (output)
swj_swdoe_tdi	Yes	Internal Pull-up
swj_swdio_tms	Yes	Internal Pull-up
swj_swclk_tclk	Yes	Internal Pull-down

Hint Bar

Review the Program and Debug Interface TRM chapter for additional details

Section 34.5

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Programmer and IDEs for XMC7000

› Flash programmer

Vendor	Flash programmer	Software	Notes
Infineon	KitProg3	ModusToolbox™ software	
	MiniProg4	ModusToolbox™ software	

› Integrated design environment (IDE)

Vendor	Debugger	Compiler
IAR	I -JET	Embedded Workbench for Arm® (8.42.x)
MTB	MiniProg4	J-link GCC

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Revision History

Revision	ECN	Submission Data	Description of Change
**	7736119	2022-03-24	Initial release

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