

XMC7000 I/O system

Customer training workshop (CTW)

January 2026

public

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Target products

Target product list for this training material:

Family category	Series	Code flash memory size
XMC7200	XMC7200-8M	Up to 8384 KB
XMC7100	XMC7100-4M	Up to 4160 KB

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XMC7200 - 8M family



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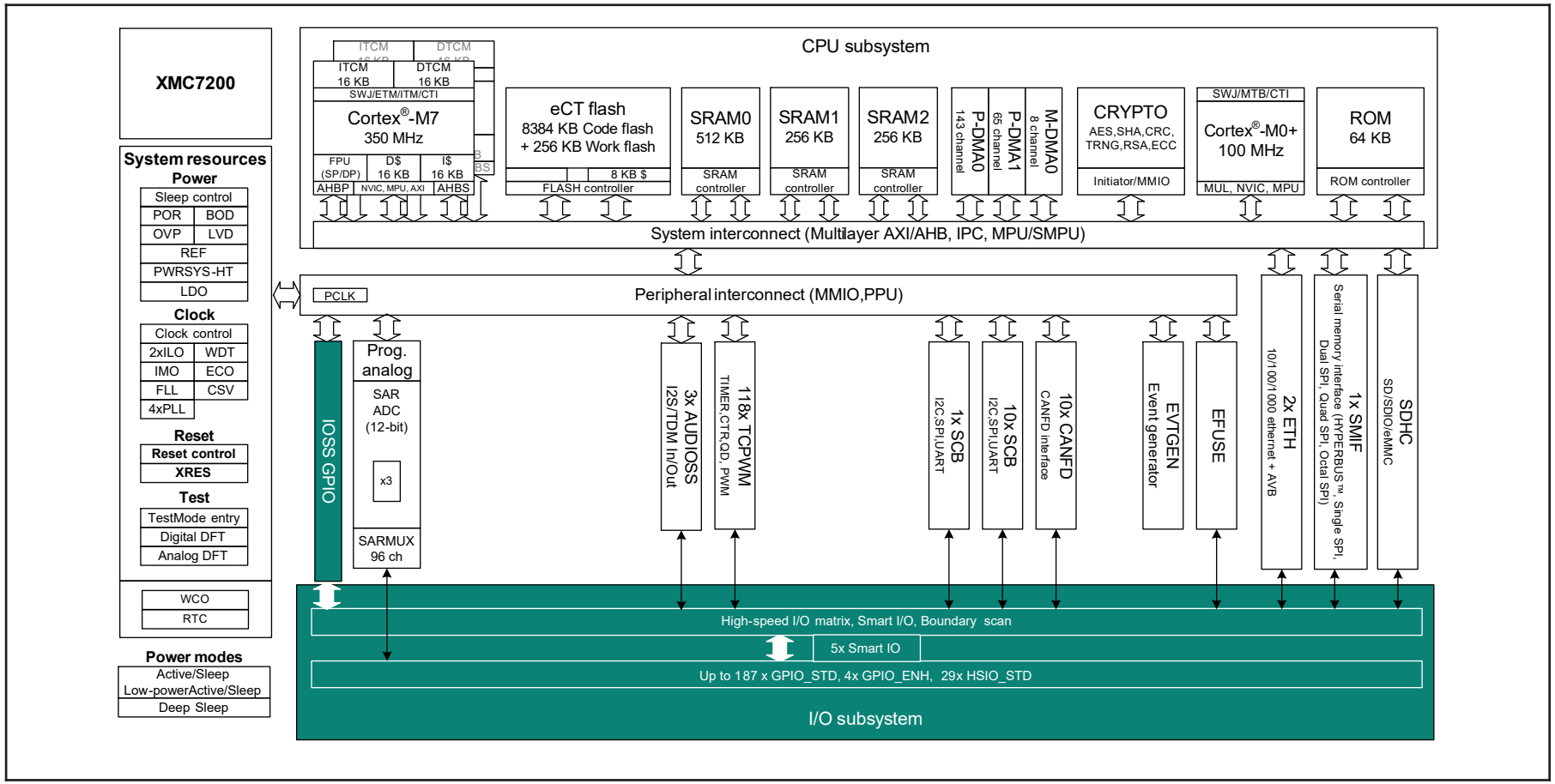
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Introduction to XMC7200-8M

The I/O system includes GPIO, HSIOM, and Smart I/O functions.



Hint bar

See the XMC7000 MCU family architecture reference manual, I/O system (chapter 22), for additional details.

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XMC7100 - 4M family



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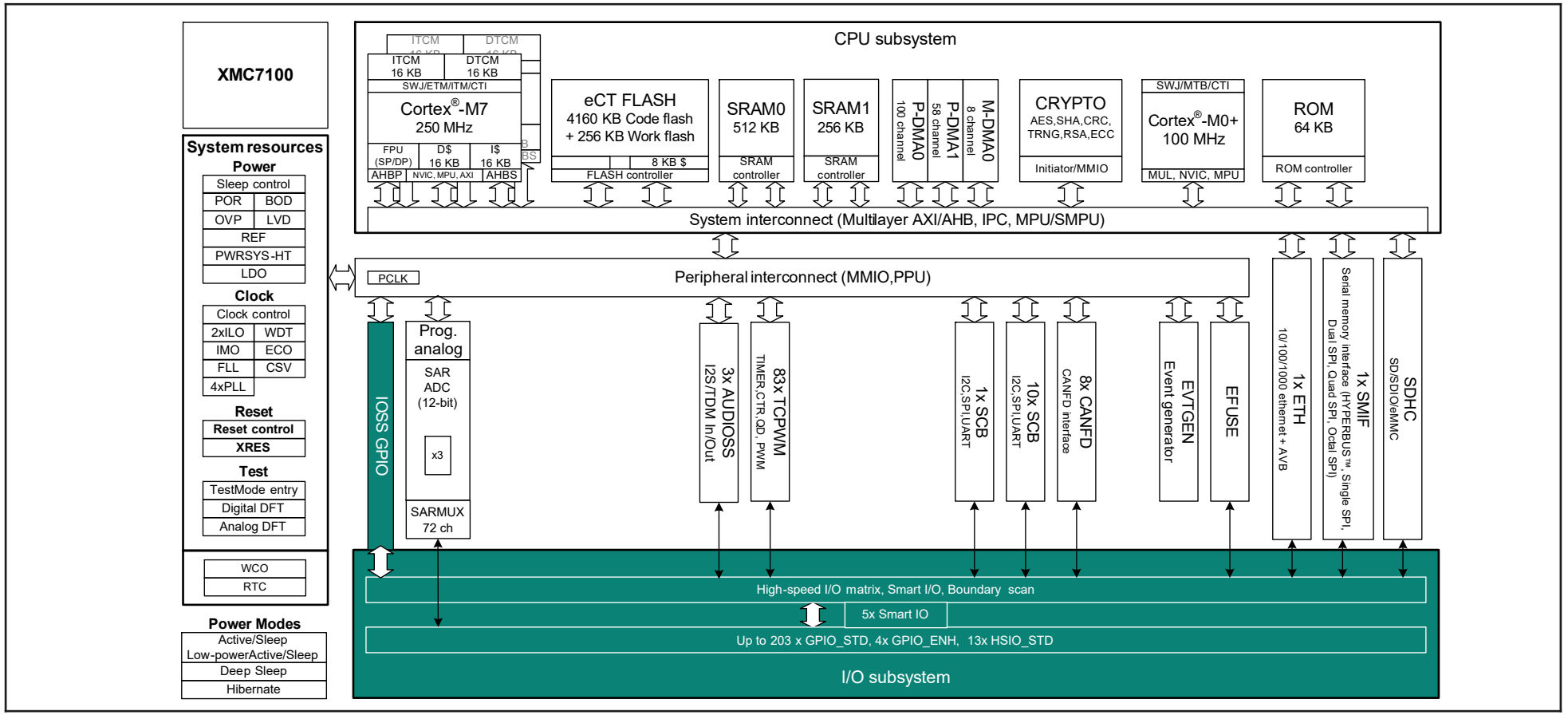
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Introduction to XMC7100-4M

The I/O system includes GPIO, HSIOM, and smart I/O functions.



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See the XMC7000 MCU family architecture reference manual, I/O system (chapter 22), for additional details.

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I/O system overview

Interface between CPU and peripheral components to the outside world.

Features

- Analog and digital input and output capabilities
- Eight drive modes
- Slew rate control
- High-speed I/O matrix (HSIOM)
- Edge-triggered interrupts on all GPIOs
- Hold I/O state in DeepSleep mode
- Smart I/O

Hint bar
See the XMC7000 MCU family architecture reference manual, Features (chapter 22.1), for additional details.

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I/O system components



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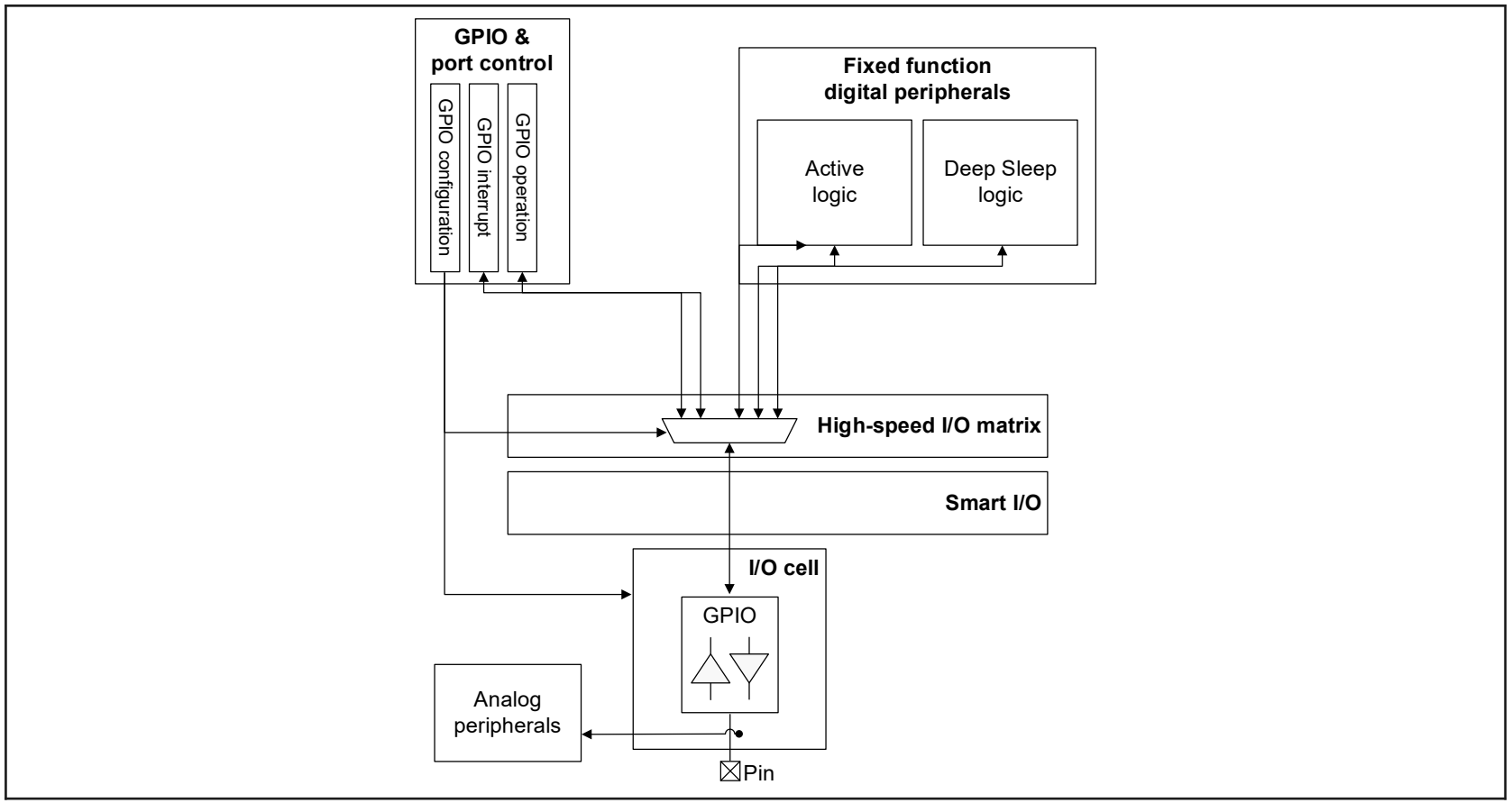
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I/O system block diagram

I/O system components



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See the XMC7000 MCU family architecture reference manual, GPIO interface overview (chapter 22.2), for additional details.

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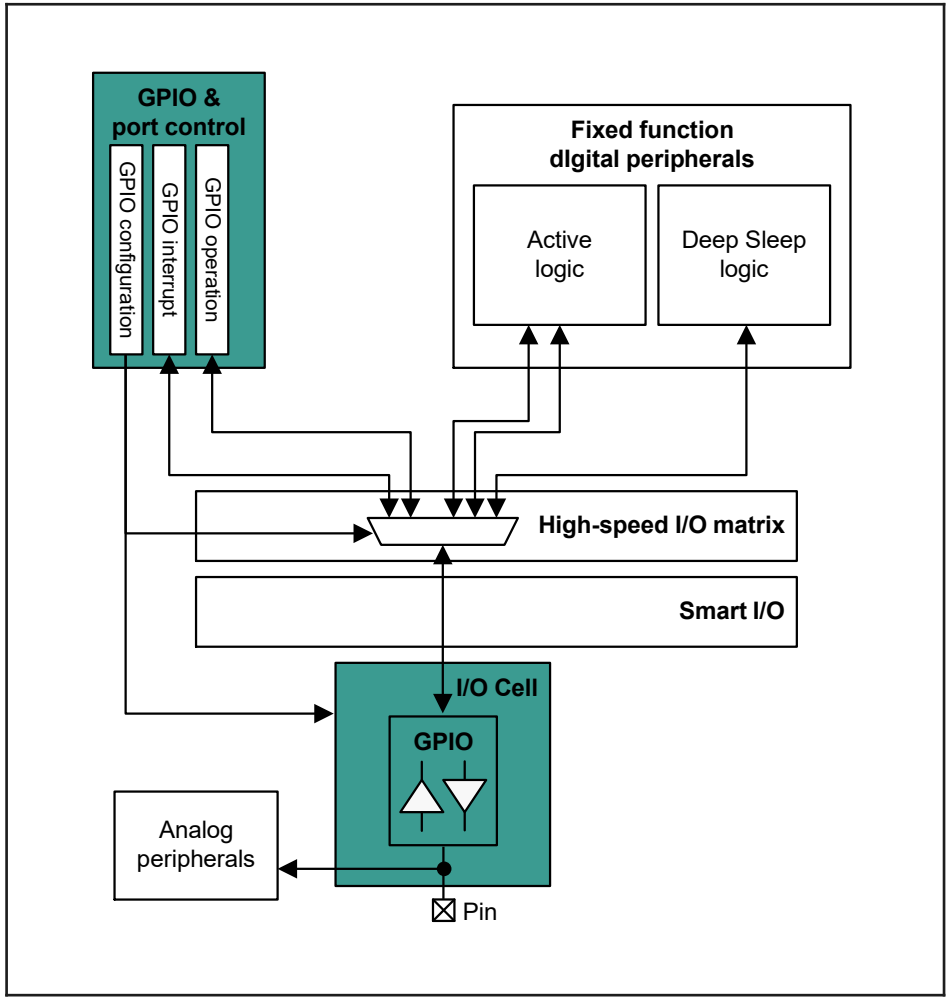
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GPIO and port control I/O cell

GPIO and port control I/O cell includes the following:

- Digital input
- +B input support
- Digital output drive modes
- Slew rate control
- GPIO SMC
- High-speed I/O
- Interrupt
- Behavior in low-power modes



Hint bar

See the XMC7000 MCU family architecture reference manual, GPIO interface overview (chapter 22.2), for additional details.

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Digital input

Each pin’s input buffer trip point is configurable for the following modes:

CMOS (Default)

- VIH: 0.7 × VDDIO
- VIL: 0.3 × VDDIO

TTL

- VIH: 2.0 V
- VIL: 0.8 V

Industrial

- VIH: 0.8 × VDDIO
- VIL: 0.5 × VDDIO

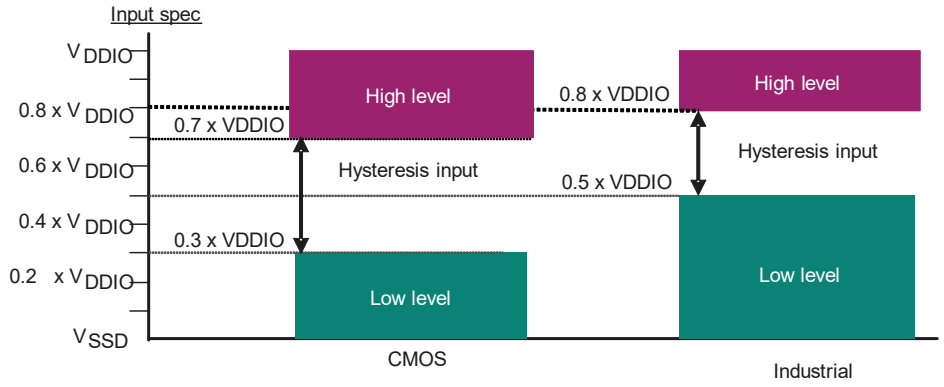
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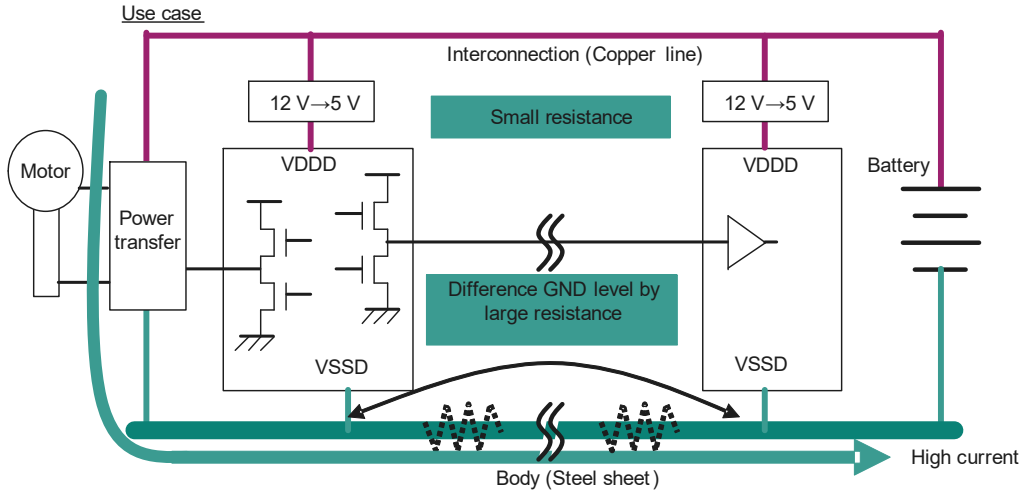
- See the XMC7000 MCU family architecture reference manual, Digital input buffer (section 22.5), for additional details
- See figure 22-3 in XMC7000 MCU family architecture reference manual

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Use case for trip point

Supports a higher threshold input for GND variation that occurs due to high current in the electronic control unit (ECU).

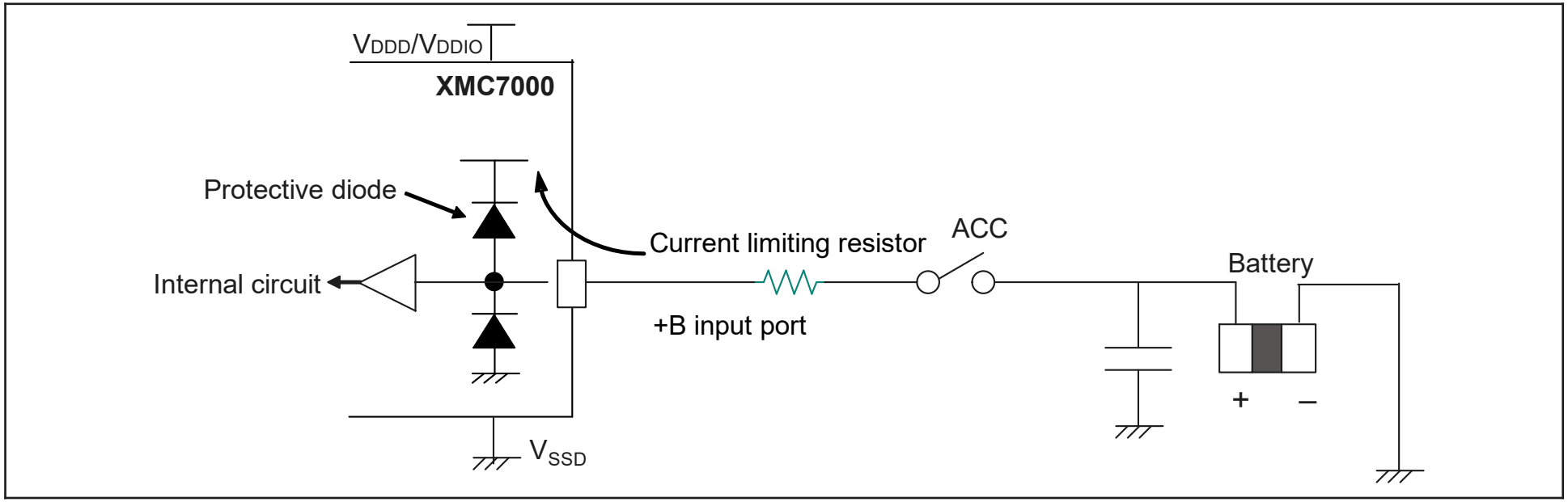




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+B input support

- Supports +B input to GPIO by adding the current limiting resistor
- Reduces the external parts and PCB footprint



Hint bar

- See the XMC7200, XMC7200D XMC7200 microcontroller 32-bit Arm® Cortex®-M7 datasheet for additional details
- For more details, see XMC7100 microcontroller 32-bit Arm® Cortex®-M7 datasheet, figure 26-1

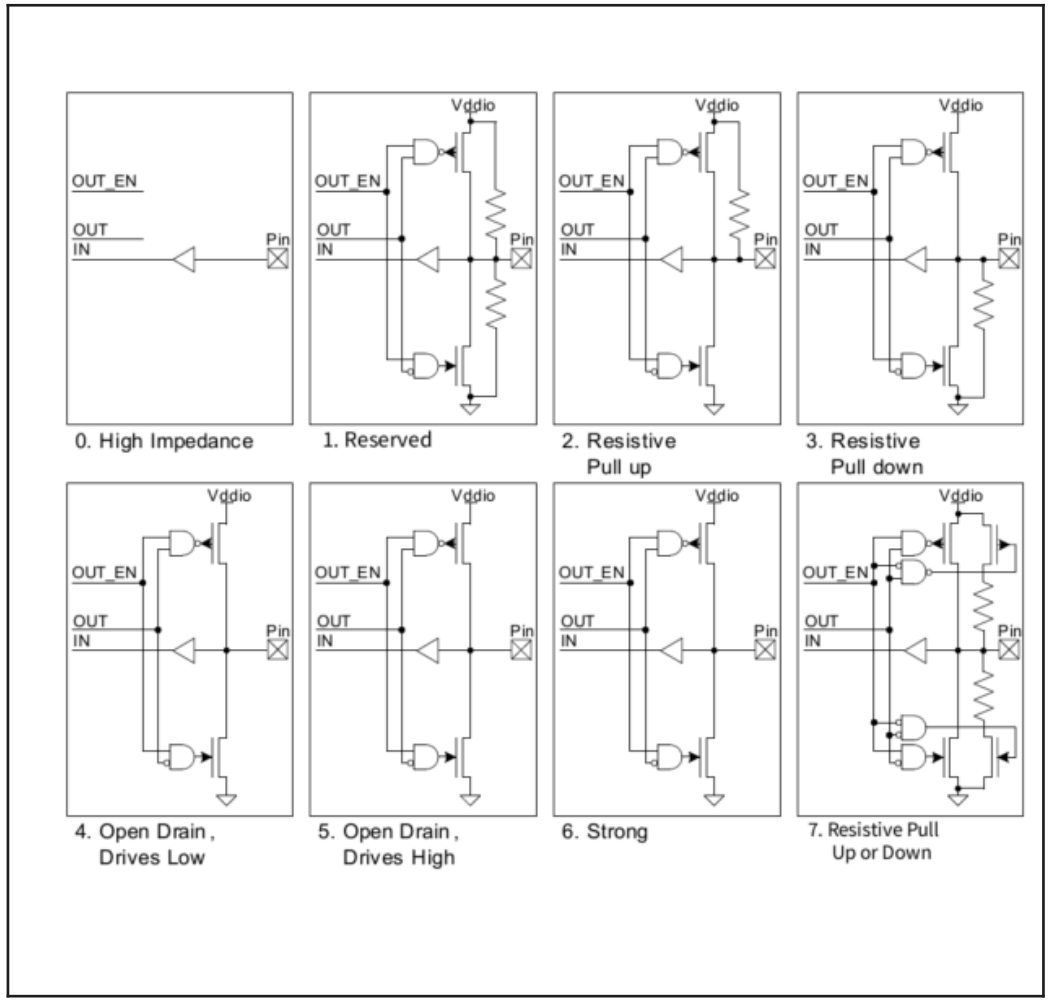
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Digital output drive modes

Each I/O is individually configurable to one of eight drive modes by software.[1]

Use case

1. Analog/digital input/unused [0] (see the figure for High impedence)
2. Resistive pull up and down at the same time for SMC- Not Supported [1] (see the figure for Reserved)
3. Interface with open drain drive lines [2-3] (see the figure for Resistive pull-up and pull-down)
4. Signal is externally pulled up (for example, I^2C) [4] (see the figure for Open drain, drives low)
5. Signal is externally pulled down [5](see the figure for Open drain, drives high)
6. Digital output signal or drive external devices [6] (see the figure for Strong)
7. Be driven by other signals [7](see see the figure for Resistive pull-up or down)



Hint bar

See the XMC7000 MCU family architecture reference manual, chapter 22.6.1, for additional details.

[1] See the register reference manual (GPIO_PRTx_CFG) for additional details.

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GPIO_STD/ENH drive strength

Drive strength can be set to one of four levels, shown in the table:

Spec	Strength (DRIVE_SEL)	V_{DDIO} or V_{DDD}		Conditions	
		2.7 V to 4.5 V	4.5 V to 5.5 V		
IOL	0,1	2 mA	5 mA (6 mA)	GPIO_STD	V_{OL} = 400 mV (600 mV)
		2 mA	5 mA	GPIO_ENH	V_{OL} = 400 mV
		6 mA		GPIO_ENH	V_{OL} = 600 mV
	2	1 mA	2 mA	GPIO_STD, GPIO_ENH	V_{OL} = 400 mV
	3	0.5 mA	1 mA	GPIO_STD, GPIO_ENH	V_{OL} = 400 mV
IOH	0,1	-2 mA	-5 mA	GPIO_STD, GPIO_ENH	V_{OH} = (V_{DDIO} or V_{DDD}) – 500 mV
	2	-1 mA	-2 mA	GPIO_STD, GPIO_ENH	V_{OH} = (V_{DDIO} or V_{DDD}) – 500 mV
	3	-0.5 mA	-1 mA	GPIO_STD, GPIO_ENH	V_{OH} = (V_{DDIO} or V_{DDD}) – 500 mV

Hint bar

See the device datasheet and architecture reference manuals section 22.6.2 for additional details.

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GPIO_STD/ENH slew rate control

Programmable output driver configuration for some GPIO pins[1]

Fast slew rate

- Full drive strength: 0, 1
- 1/2 drive strength: 2
- 1/4 drive strength: 3

Slow slew rate (GPIO_ENH only)

- Full drive strength: 0

Spec	Slew rate mode	Min	Max	Conditions
Tr/Tf	Fast, Strength = 0 (GPIO_STD, GPIO_ENH)	1 ns	10 ns	10%/90% 20-pF load
	Slow, Strength = 0 (GPIO_ENH)	20 ns x (V_{DDD}/5.5)	160 ns	

Advantage

- Slower slew rate can reduce EMI and crosstalk

Use case

- Slower slew rate is used for low-frequency signals or signals without strict timing constraints

Hint bar

- See the datasheet and architecture reference manual section 22.6.2 for additional details
- See XMC7100 /7200 datasheet, Table 26-6 for more details

[1] See the register reference manual (GPIO_PRTx_CFG_OUT) for additional details. Slew rate control is not available on all GPIO ports.

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High-speed I/O standard (HSIO_STD)1

Supports 3.3 V high-speed interfaces

- Serial memory interface
  - Single, Dual, Quad, or Octal serial peripheral interface (SPI)
  - HYPERBUS™
- Secure digital host controller (SDHC) interface
  - Secure digital (SD) cards
  - Secure digital input output (SDIO) cards
  - Embedded multimedia card (eMMC) based memory devices
- Ethernet
  - Media independent interface (MII)
  - Reduced media independent interface (RMII)
  - Reduced gigabit media independent interface (RGMII)

Drive select

DRIVE_SEL[0:1]	Description
00	HSIO default mode
01	GPIO Full drive strength
10	GPIO 1/2 drive strength
11	GPIO 1/4 drive strength

Hint bar

See the datasheet and architecture reference manual section 22.4 for additional details

HSIO_STD does not support:

- Slew rate control
- Deep Sleep operation
- Analog connections

[1] Not all devices supports HSIO_STD functionality. See to the specific device datasheet for availability of HSIO_STD and the specifications of each drive strength.

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High-speed I/O standard low noise (HSIO_STD_LN)1

- Supports clocking and signaling up to 133 MHz for BGA packages and 100 MHz for TEQFP packages
- Supports high-speed interfaces
  - Graphics input / output
  - Ethernet and Serial memory interface

Drive select [2]

DRIVE_SEL_EXT[0:2]	Mode supported	Slew rate control	Slew rate (V/ns)	Voltage range	Frequency (MHz)	Load (pF)
000	xSPI-266	0	1.37	3.0 V to 3.6 V	133	15
		1	1.25	3.0 V to 3.6 V	125	15
001	xSPI-200	0	1.03	3.0 V to 3.6 V	100	15
		1	0.9	3.0 V to 3.6 V	90	15
010	Graphics	0	0.43	3.0 V to 3.6 V	80	15
		1	0.3	3.0 V to 3.6 V	60	15
111	Graphics 64 MHz Ethernet 50 MHz	0	0.31	3.0 V to 3.6 V	64	15
		1	0.24	3.0 V to 3.6 V	50	15
		0/1	0.43	4.5 V to 5.5 V	80	15
100	SPI 12 MHz GPIO support	0/1	0.11	3.0 V to 3.6 V	12	20
		0/1	0.15	4.5 V to 5.5 V	20	20
101, 110, 111	Unused	N/A	N/A	N/A	N/A	N/A

Hint bar

See the datasheet and architecture reference manual section 22.6 for additional details.

[1] Not all devices support HSIO_STD_LN functionality. See to the specific device datasheet for availability of HSIO_STD_LN.
[2] This table consists only parameter target values for orientation. The device specification is only mentioned in the appropriate device datasheet.

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High-speed I/O enhanced

Supports high-speed interfaces

- High-speed I/O enhanced (HSIO_ENH)[1]
  - Supports signaling up to 200 MHz for high-speed interface
    - xSPI400(1.8V), xSPI333(3.3V), xSPI266(3.3V)

Drive select[2]

DS_TRIM[0:2]	Description	Voltage support	Mode supported	Package support	Memory support
000	Default (50 Ω)	N/A	N/A	N/A	N/A
001	120 Ω	3.3 V	xSPI-266	TQFP	Single
010	90 Ω	N/A	N/A	N/A	N/A
011	60 Ω	3.3 V	xSPI-266	TQFP	Dual
100	50 Ω	1.8 V	xSPI-400	BGA	Single
101	30 Ω	3.3 V	xSPI-333	BGA	Single
110	20 Ω	1.8 V	xSPI-400	BGA	Dual
111	15 Ω	3.3 V	xSPI-333	BGA	Single

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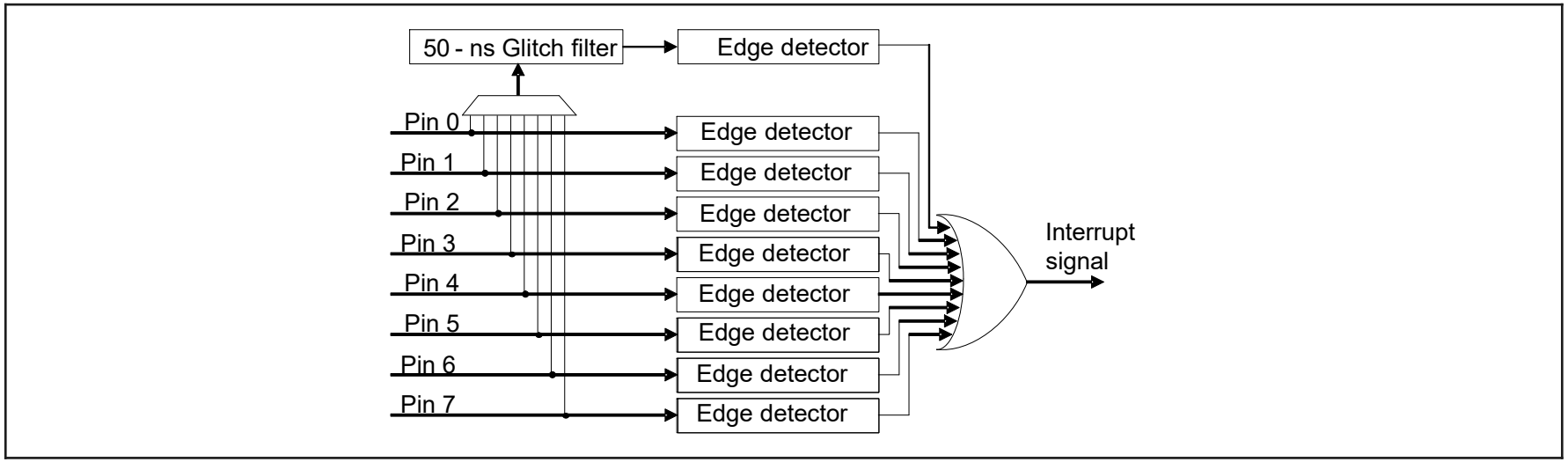
See the datasheet and architecture reference manual section 22.6 for additional details.

[1] Not all devices support HSIO_ENH functionality. See to the specific device datasheet for availability of HSIO_ENH .
[2] This table consists only parameter target values for orientation. The device specification is only mentioned in the appropriate device datasheet.

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GPIO interrupt

- All port pins can generate GPIO interrupts and status registers[1]
- GPIO interrupt signal is generated by one per port
- Edge detector supports rising, falling, and both edges in all power modes[2]
- Glitch filter can be used by one pin per port[3]



Use case

- Wakeup interrupt from low-power mode (e.g., CAN wakeup)
- Detect the input signal state change (e.g., switch)

[1] See the registers reference manual (GPIO_PRTx_INTR) for additional details.
[2] See the registers reference manual (GPIO_PRTx_INTR_CFG) for additional details.
[3] If more longer pulse suppression width is necessary, use Smart I/Os.

Hint bar

See the architecture reference manual, chapter 22.10, for additional details.

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Behavior in each state

State	Status
Reset	– All GPIOs are in high-impedance analog state, and the input buffers are disabled
Sleep	– GPIO pins are active – Can be driven by most peripherals, such as TCPWM and SCB – Any GPIO can be used to wake the device
Deep Sleep	– GPIO pins connected to the Deep Sleep domain peripheral (SCB[0]) are functional – All other pins are hold/frozen and will maintain the last output driver state and I/O configuration – GPIO interrupts are functional on all I/Os and can be used to wake the device
Hibernate	– Only select I/Os can be used to wake the device[1] – All other pins are on hold/frozen and will maintain the last output driver state and I/O configuration

Advantages

– Reduces power consumption while keeping the last I/O driver state
– Any I/O can be used as wakeup interrupt except in Hibernate mode

Hint bar

– See the architecture reference manual, section 22.9, for additional details
– See the Device power modes training section for details on the device power modes

[1] XMC7000 supports up to two GPIO interrupts.

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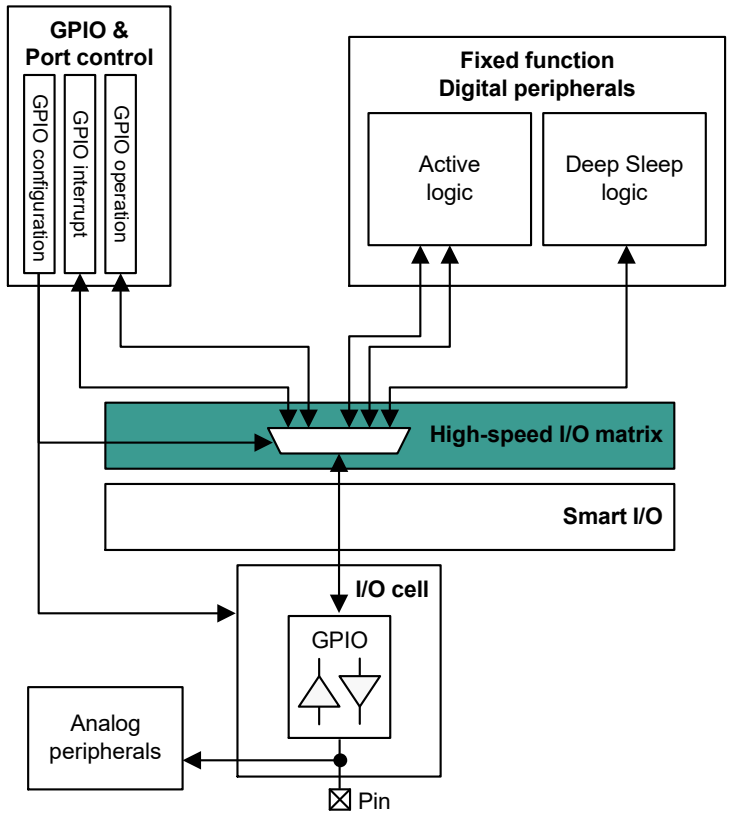
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High-speed I/O matrix (HSIOM)

Routing internal CPU and peripheral signals to and from the GPIOs.



Hint bar

See the XMC7000 MCU family architecture reference manual, chapter 22.7, for additional details.

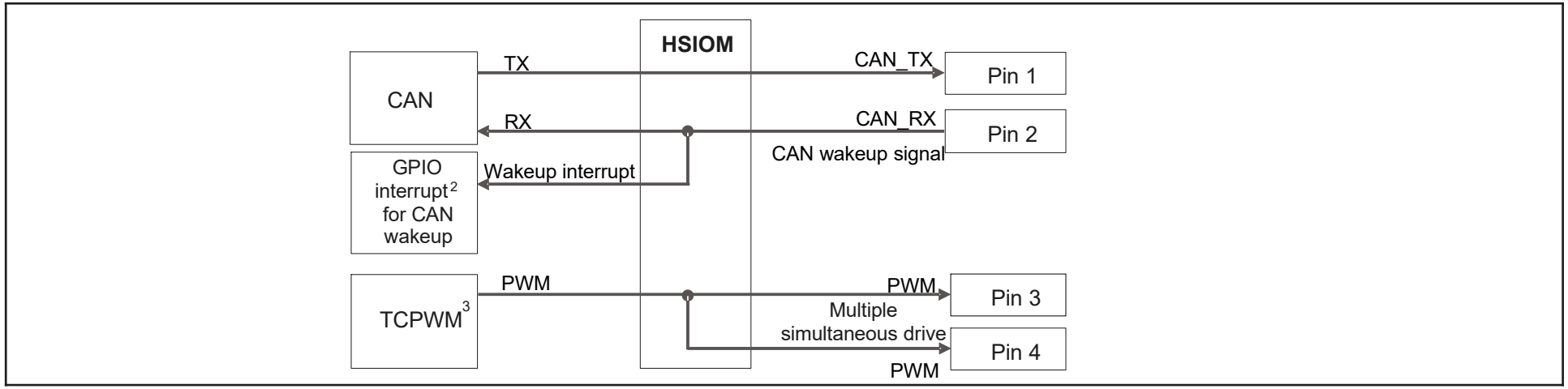
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High-speed I/O matrix (HSIOM) (contd.)

- Routing internal peripheral signals to and from GPIOs
- GPIOs can be shared with multiple functions
- Multiplexes the pin connection to a user-selected peripheral[1]
- GPIO interrupt has no dependency on HSIOM configuration[2]

Use case

- CAN Wakeup[2]
- Multiple simultaneous drive by PWM output[3]



Hint bar

See the datasheet and architecture reference manual, section 22.7, for additional details.

[1] See the registers reference manual (HSIOM_PORT_SELx) for additional details.
[2] Do not change the HSIOM configuration before going to Low-power mode.
[3] It depends on the pin assignment. For details on pin assignment, refer to the device datasheet.

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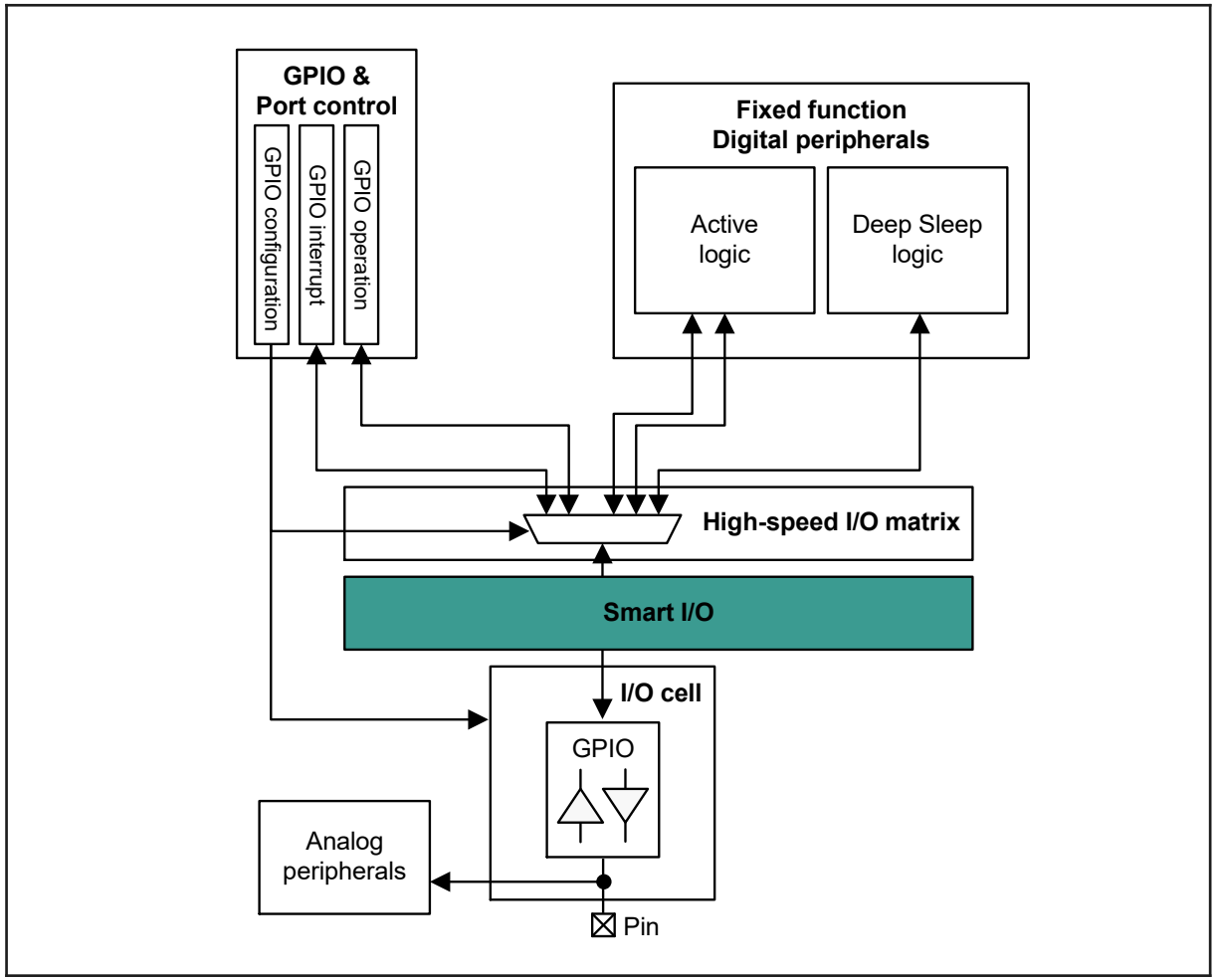
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Smart I/O

Smart I/O

- Smart I/O signal paths
- Block components
- Routing



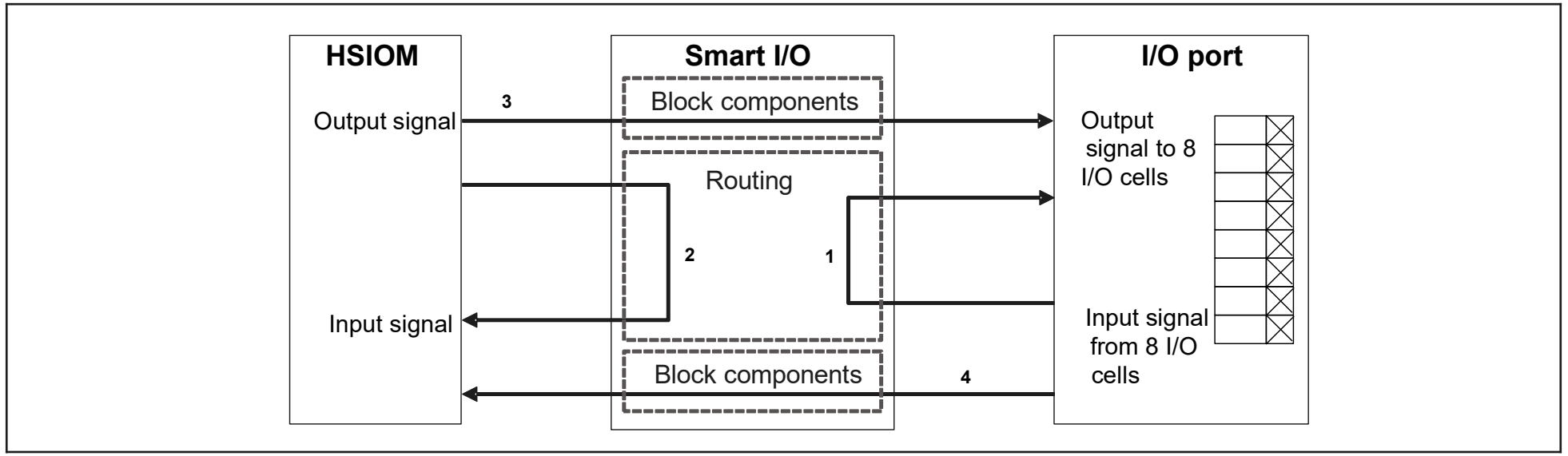
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See the XMC7000 MCU family architecture reference manual, section 22.12, for additional details.

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Smart I/O signal paths

1. Observe input signals directly and control output signals directly
2. Operate on and modify HSIOM output signals and route the modified signals to HSIOM input signals
3. Operate on and modify HSIOM output signals and route the modified signals to the output signals
4. Operate on and modify input signals and route the modified signals to HSIOM input signals



Use cases

1. Simple logic control without CPU involvement
2. Communication peripheral loopback test
3. Inverting SPI output signal polarity
4. Inverting SPI input signal polarity or as a glitch filter for the input signal

Hint bar

- See the XMC7000 MCU family architecture reference manual, section 22.12, for additional details
- See the Block components and Routing for additional details

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Block components (1/3)

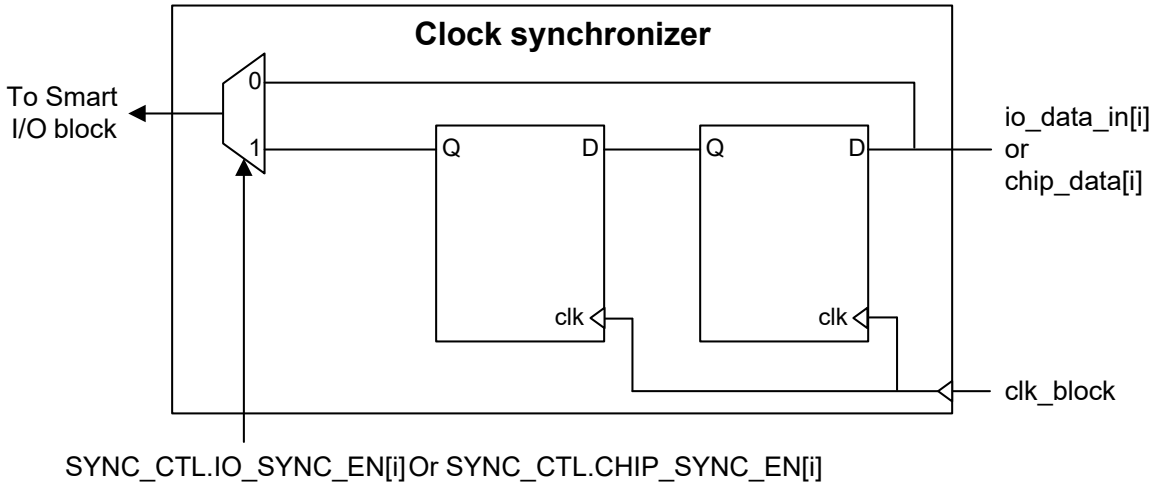
Internal Smart I/O logic components

- Clock and reset
  - Used for all components
- Data unit
  - Consists of a simple 8-bit data path

Synchronizers

Each GPIO input signal and device input signal (HSIOM input) can be used either asynchronously or synchronously

- To use the signals synchronously, a double flip-flop synchronizer is placed on both the signal paths to synchronise the signal to the Smart I/O clock (clk_block)



Hint bar

See the architecture reference manual, section 22.12.2 and the registers reference manual for additional details.

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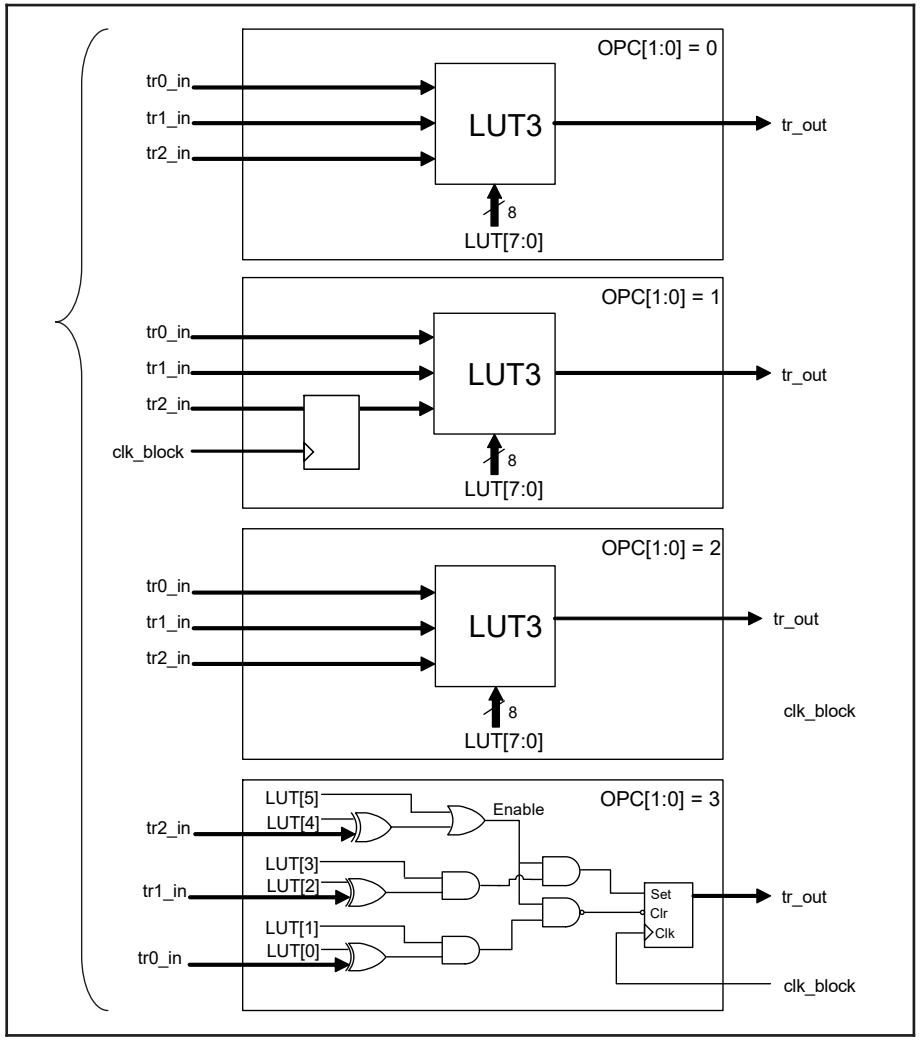
Block components (2/3)

Three-input lookup table (LUT3)

- Each Smart I/O block contains eight lookup table (LUT3) components
- An LUT3 component consists of a three-input LUT and a flip-flop
- OPC[1:0][1] determines the usage of flip-flop
- LUT[7:0][2] is used as a lookup table for three input signals

tr2_in[2]	tr1_in[2]	tr0_in[2]	tr_out
0	0	0	LUT[0]
0	0	1	LUT[1]
0	1	0	LUT[2]
0	1	1	LUT[3]
1	0	0	LUT[4]
1	0	1	LUT[5]
1	1	0	LUT[6]
1	1	1	LUT[7]

[1] See the registers reference manual (SMARTIO_LUT_CTL) for additional details.
[2] Their inputs are defined by the SMARTIO_LUT_SEL register.



Hint bar

See the XMC7000 MCU family architecture reference manual section 22.12.2 and the XMC7100 MCU registers reference manual for additional details.

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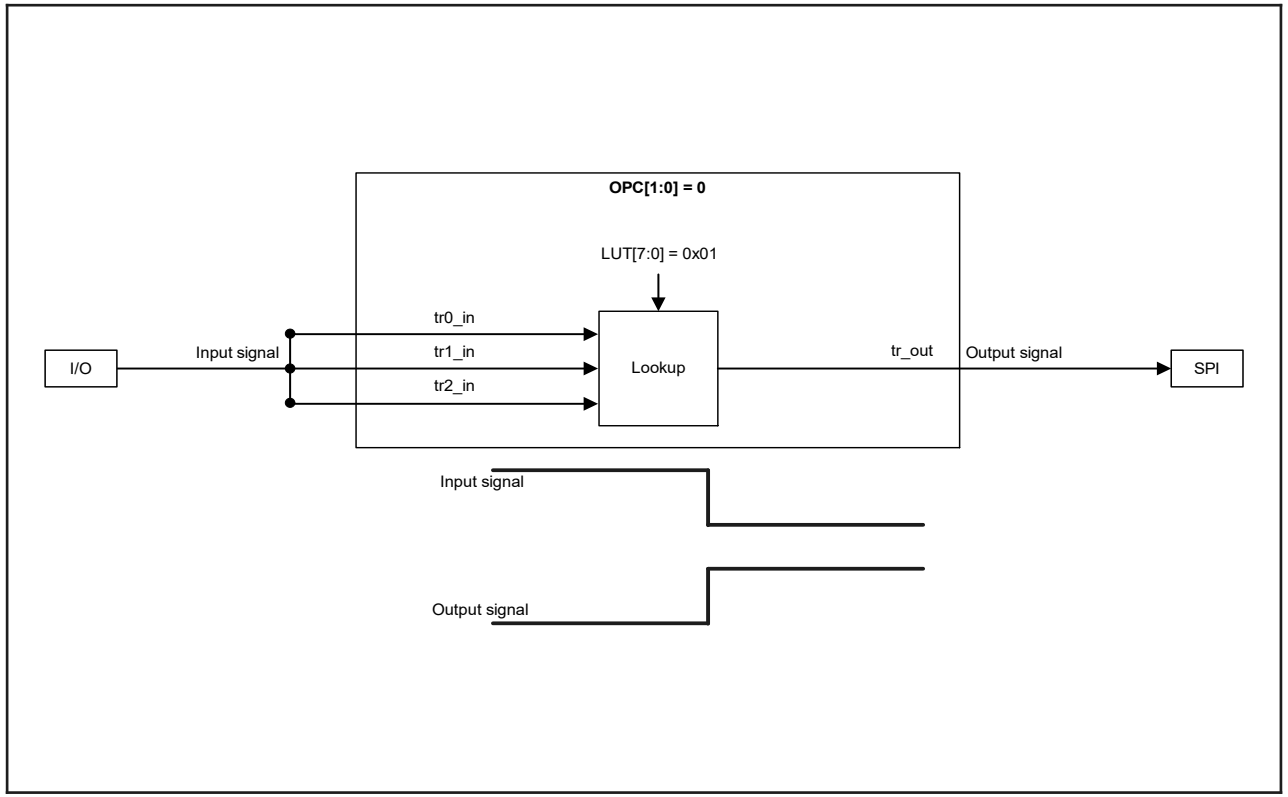
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Use case 1: Invert SPI signal polarity

Use as an inverter by setting only OPC[1:0] = 0, LUT[7:0] = 0x01

LUT[7:0] = 0x01

tr2_in	tr1_in	tr0_in	tr_out
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0



Hint bar

See the XMC7000 MCU family architecture reference manual, section 22.12, and the XMC7100 MCU registers reference manual for additional details.

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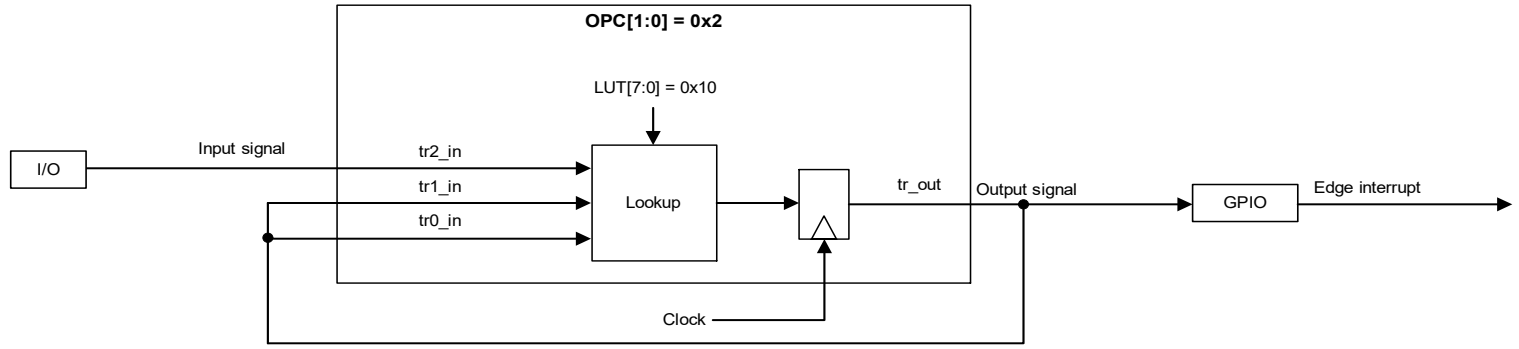
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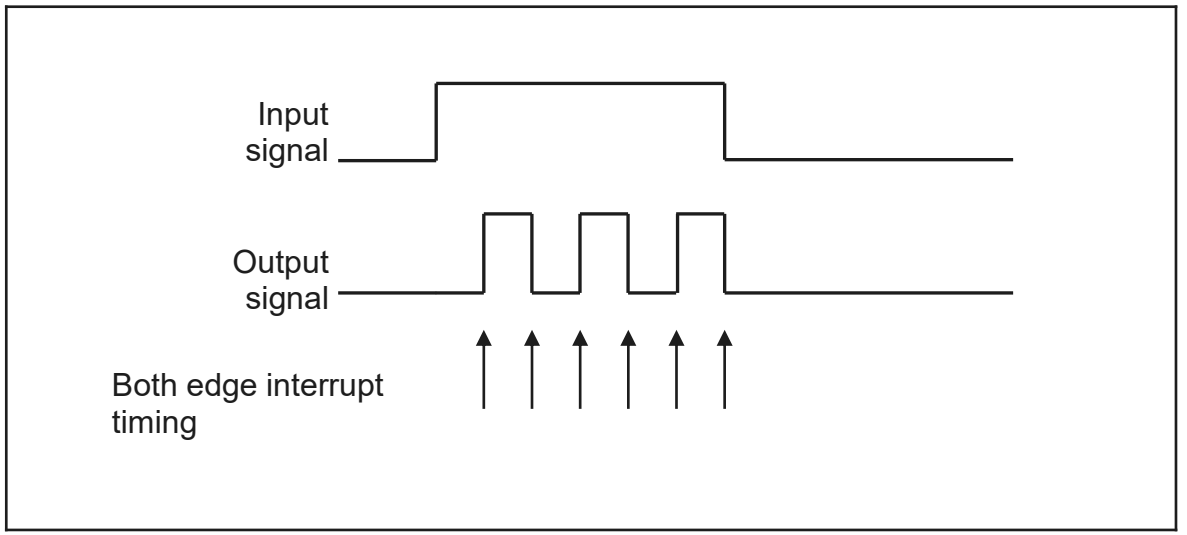
Use case 2: High-level detection interrupt

Use as a high-level detection interrupt by using a GPIO edge interrupt and setting LUT3 to OPC[1:0] = 0x2, LUT[7:0] = 0x10



LUT[7:0] = 0x10

tr2_in	tr1_in	tr0_in	tr_out
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0



Hint bar

See the XMC7000 MCU family architecture reference manual, section 22.12.2 and the XMC7100 MCU registers reference manual for additional details.

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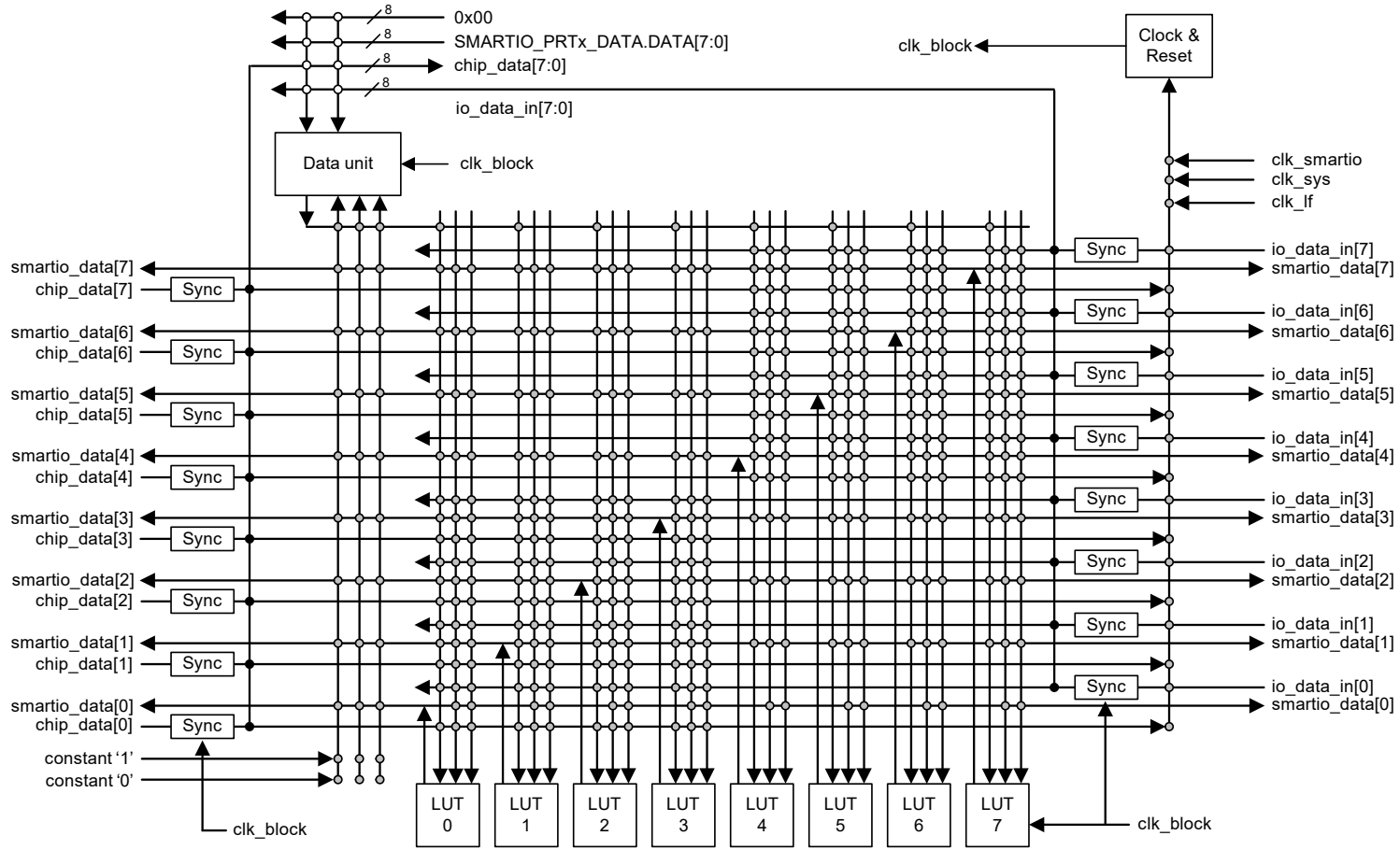
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Routing

Routing is used to route signals in and out of the block and between various components inside the block.



Hint bar

- See the XMC7000 MCU family architecture reference manual, section 22.12.3 and the XMC7100 MCU registers reference manual for additional details
- Additional reference material is available on the web page at: PSOC™ Creator smart I/O component datasheet

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Revision history

Document revision	Date	Description of change
**	2022-04-04	Initial release.
*A	2026-01-07	Migrated to the latest empower training presentation template.

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