Customer training workshop

XMC7000 microcontroller: Interrupts

Target products

Target product list for this training material

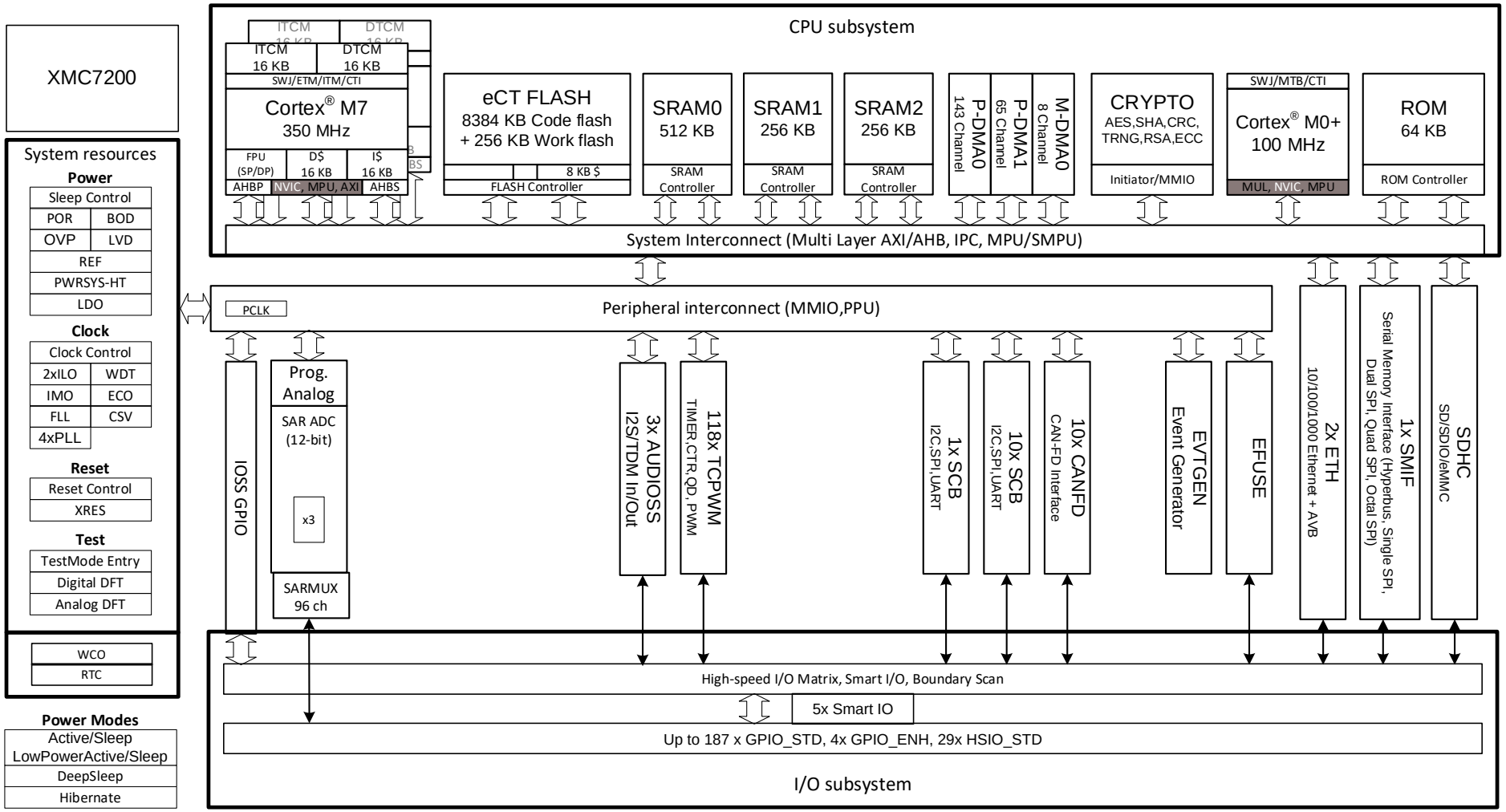
Family category	Series	Code flash memory size
XMC7200	XMC7200-8M	Up to 8384KB
XMC7100	XMC7100-4M	Up to 4160KB

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XMC7200 - 8M family

Introduction to XMC7200-8M

› The interrupt controller is in the CPUSS block



Hint Bar

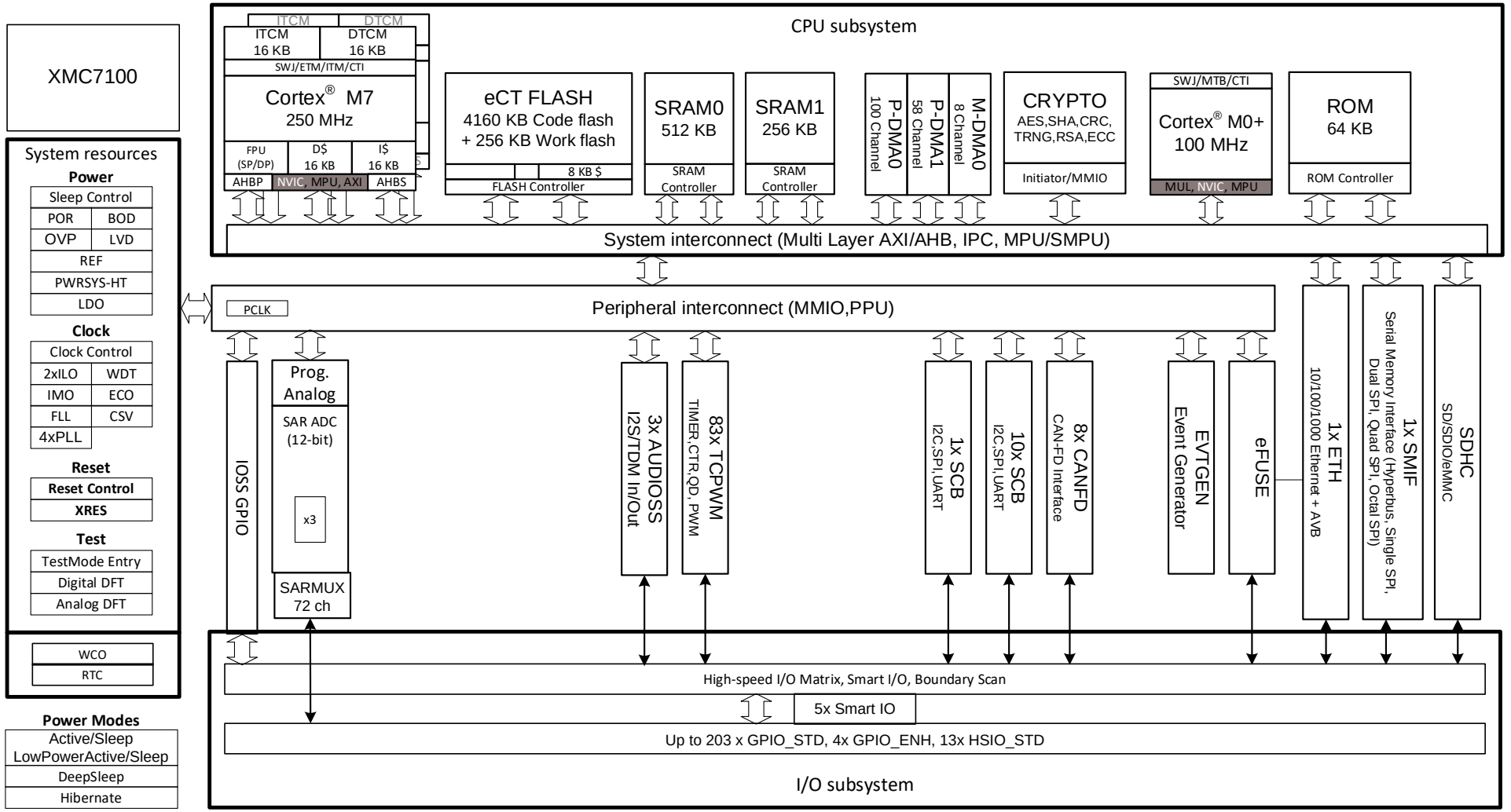
Review TRM chapter 12 for additional details

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XMC7100 - 4M family

Introduction to XMC7100-4M

› The interrupt controller is in the CPUSS block



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Review TRM chapter 12 for additional details

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Interrupts overview

- Interrupts are events generated by peripherals of each CPU
- Exceptions are events generated by each CPU

- Features
  - Up to 1023[1] system interrupts
  - Any of the system interrupts can be mapped to each CPU NMI (up to four)
  - Vector table is placed in either flash or SRAM
  - Configurable priority levels (eight levels for Cortex®-M7 and four levels for Cortex®-M0+) for each interrupt
  - All the available system interrupt sources are usable in Active power mode and wake up from Sleep power mode
  - Wakeup interrupts are capable of waking the device from DeepSleep power mode

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Review TRM section 12.1 for additional details specific to Interrupts

Refer to each device datasheet for the list of system interrupts

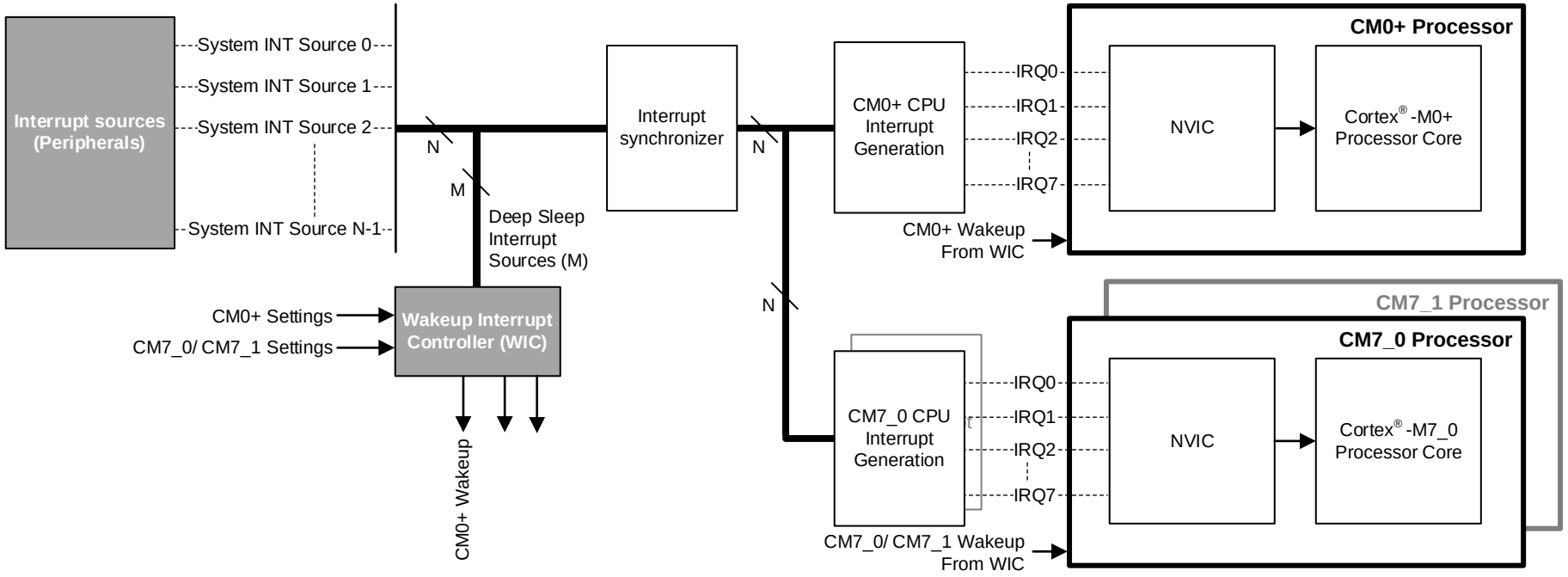
Refer to the CPUSS Training Section for additional Vector Table Relocation details

[1] The total number of system interrupts varies depending on the device

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Components in interrupt architecture

› The interrupt architecture consists of the following components.



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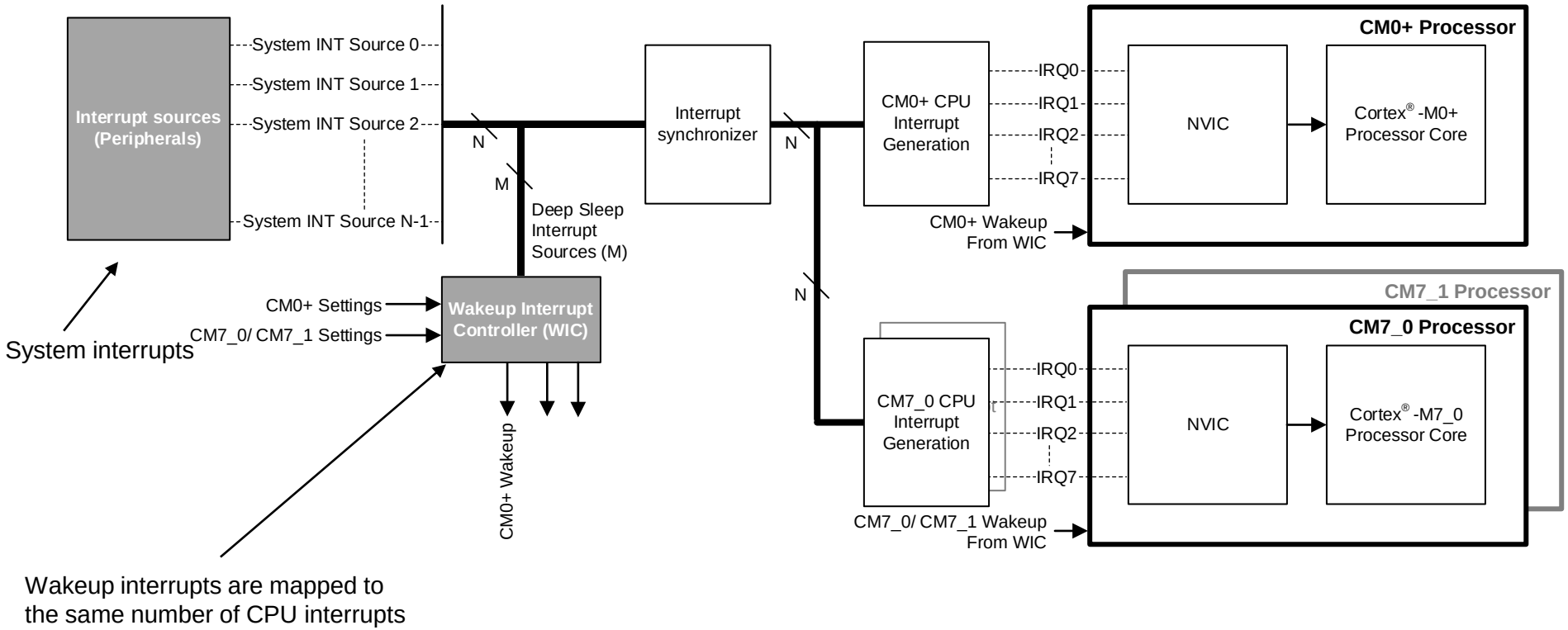
Nested Vectored Interrupt Controller (NVIC)

Interrupt request (IRQ)

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Interrupt architecture block diagram

- Interrupt architecture components
  - Interrupt sources
  - System interrupts
  - Wakeup interrupts



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Number of system interrupts (N)

Number of wakeup interrupts (M)

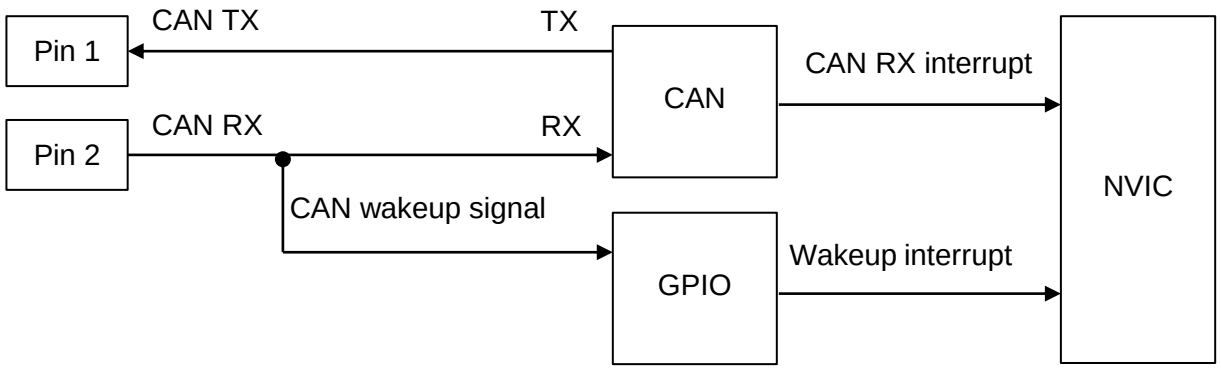
Refer to the Appendix for the number of system interrupts, listed by device

Refer to each device datasheet for the list of system interrupts

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Interrupt sources

- System interrupts
  - Originate from peripheral interrupts
  - Include wakeup interrupts
- Wakeup interrupts
  - Wakes CPU up from DeepSleep mode
- Use case
  - The GPIO can be used as a CAN wakeup interrupt



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Review TRM section 12.5 for additional details about system interrupts

Refer to each device datasheet for the list of system interrupts

Review TRM section 12.10 for additional details about wakeup interrupts

Wakeup from DeepSleep mode involves the WIC

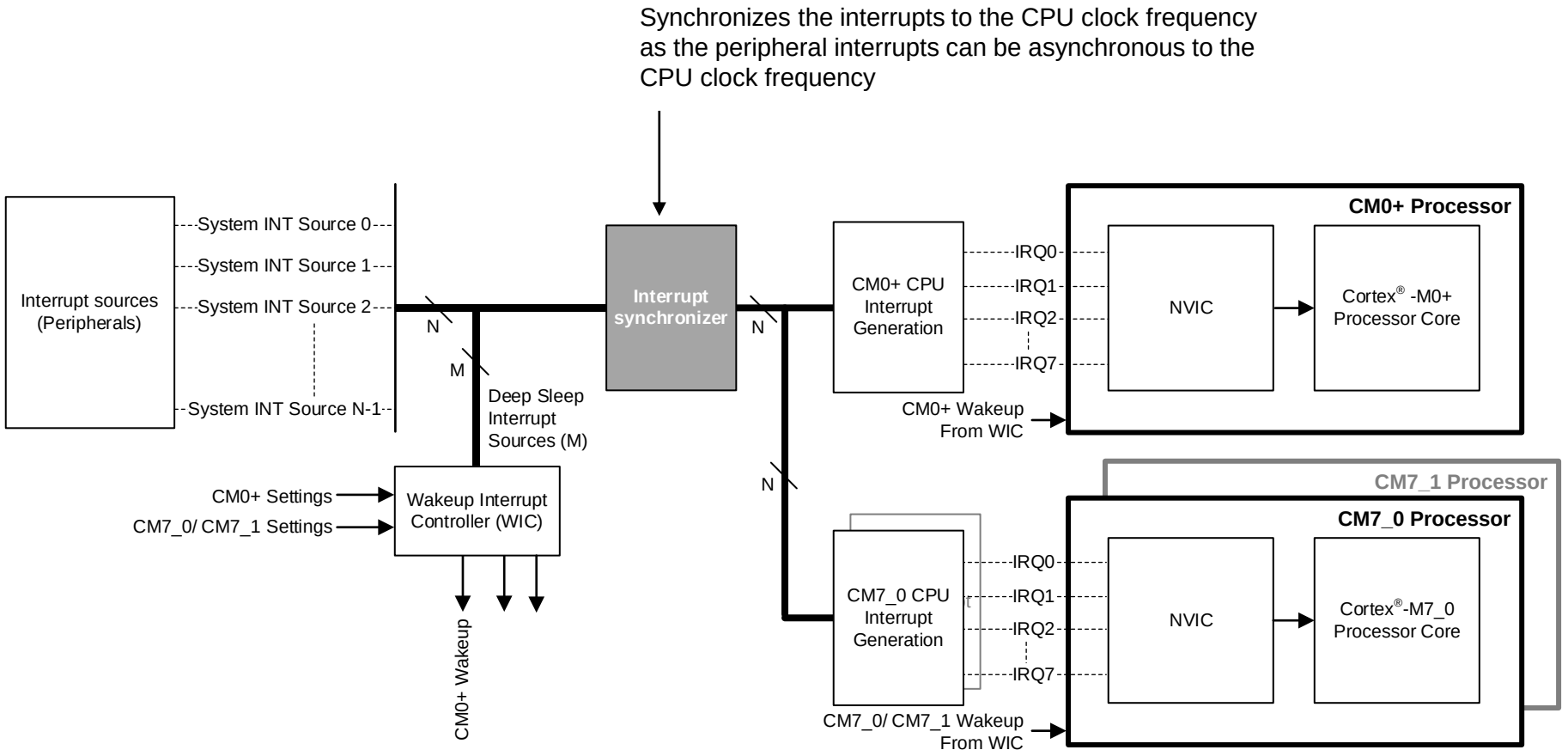
Review TRM section 12.10 for additional details specific to WIC

Review the Device Power Modes training section for additional Wakeup Interrupts details

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Interrupt synchronizer

- Interrupt architecture components
  - Interrupt synchronizer



Hint Bar

Review TRM section 12.5 for additional details about system interrupts

Refer to each device datasheet for the list of system interrupts

Review TRM section 12.10 for additional details about wakeup interrupts

Wakeup from DeepSleep mode involves the WIC

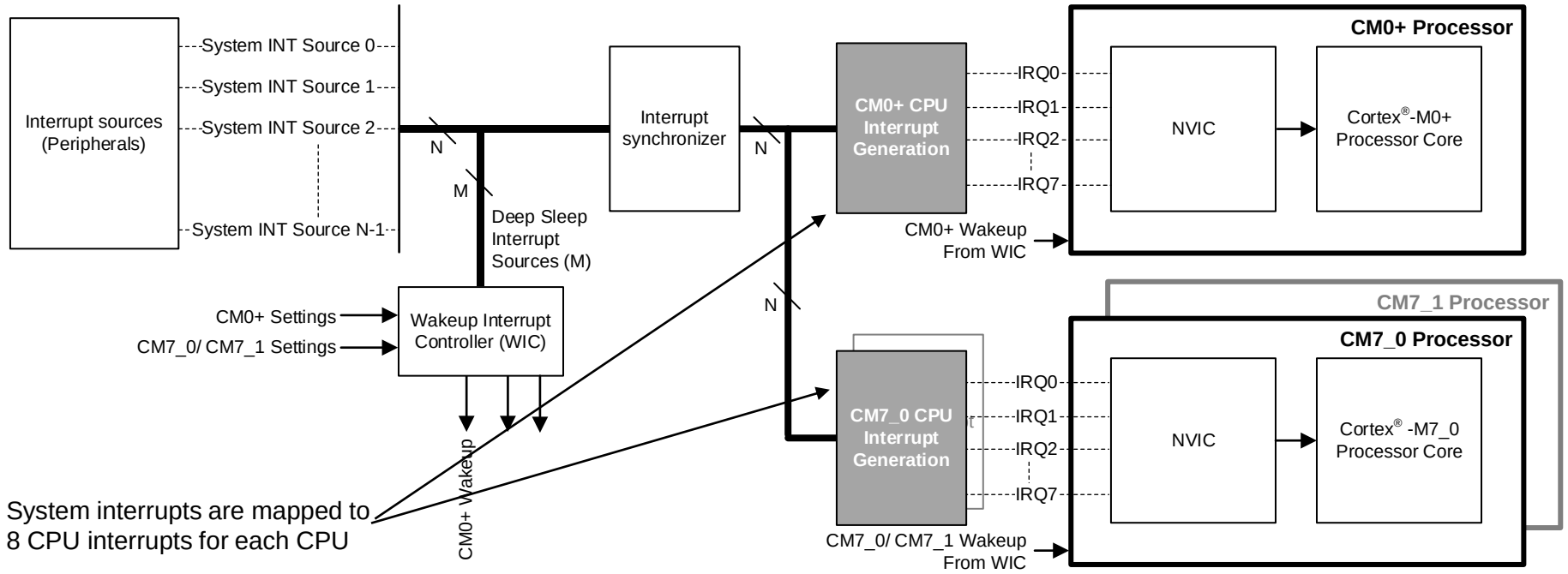
Review TRM section 12.10 for additional details specific to WIC

Review the Device Power Modes training section for additional Wakeup Interrupts details

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CPU interrupt

- Interrupt architecture components
  - CPU interrupt
    - Each system interrupt can be mapped to exactly one CPU interrupt of each core
    - Achieved using the register setting
      - CM0/CM7_0/CM7_1_SYSTEM_INT_CTL.CPU_INT_IDX[2:0]
      - CM0/CM7_0/CM7_1_SYSTEM_INT_CTL.CPU_INT_VALID



Hint Bar

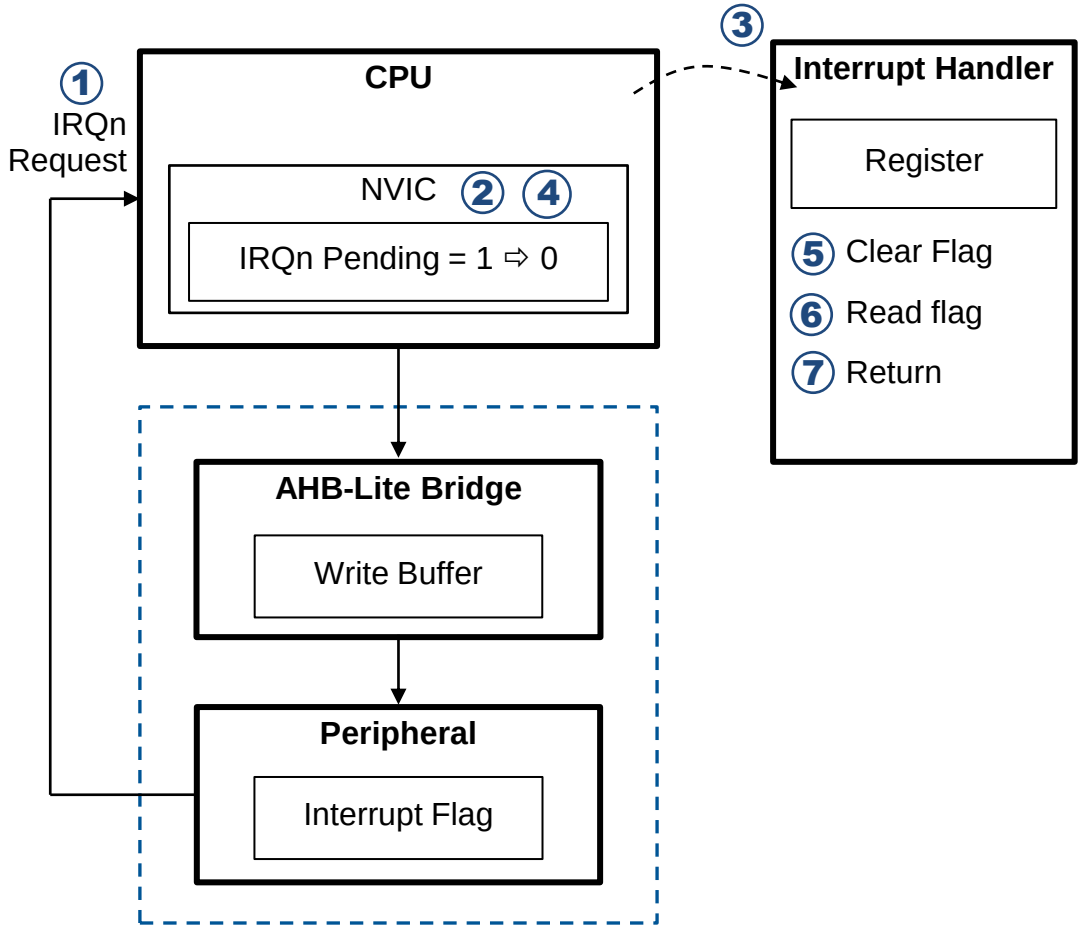
Refer to each device datasheet for the list of system interrupts

CM7_0 and CM7_1 represent the first and the second CM7 core in the CYT4 device, respectively

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Interrupt handler processing (1/3)

- Sequence of a normal interrupt request handling
  - ① Interrupt request asserts IRQn
  - ② When the IRQn request can be accepted, the NVIC sets the pending status
  - ③ Jumps to the interrupt handler
  - ④ Entering the interrupt handler clears the pending status
  - ⑤ Clears the interrupt flag of the peripheral register
  - ⑥ Reads the interrupt flag of the peripheral register to drain the Write Buffer
  - ⑦ Return



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Interrupt handler processing (2/3)

- The CPU interrupt handler uses the SYSTEM_INT_IDX field to index a system interrupt lookup table and jump to the system interrupt handler
- Read after write (RAW) is important in the interrupt handler processing to ensure completion of the write buffer

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Review TRM section 12.5 for additional details

The lookup table is usually located in one of the system memories

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Interrupt handler processing (3/3)

› The following code illustrates the sequence:

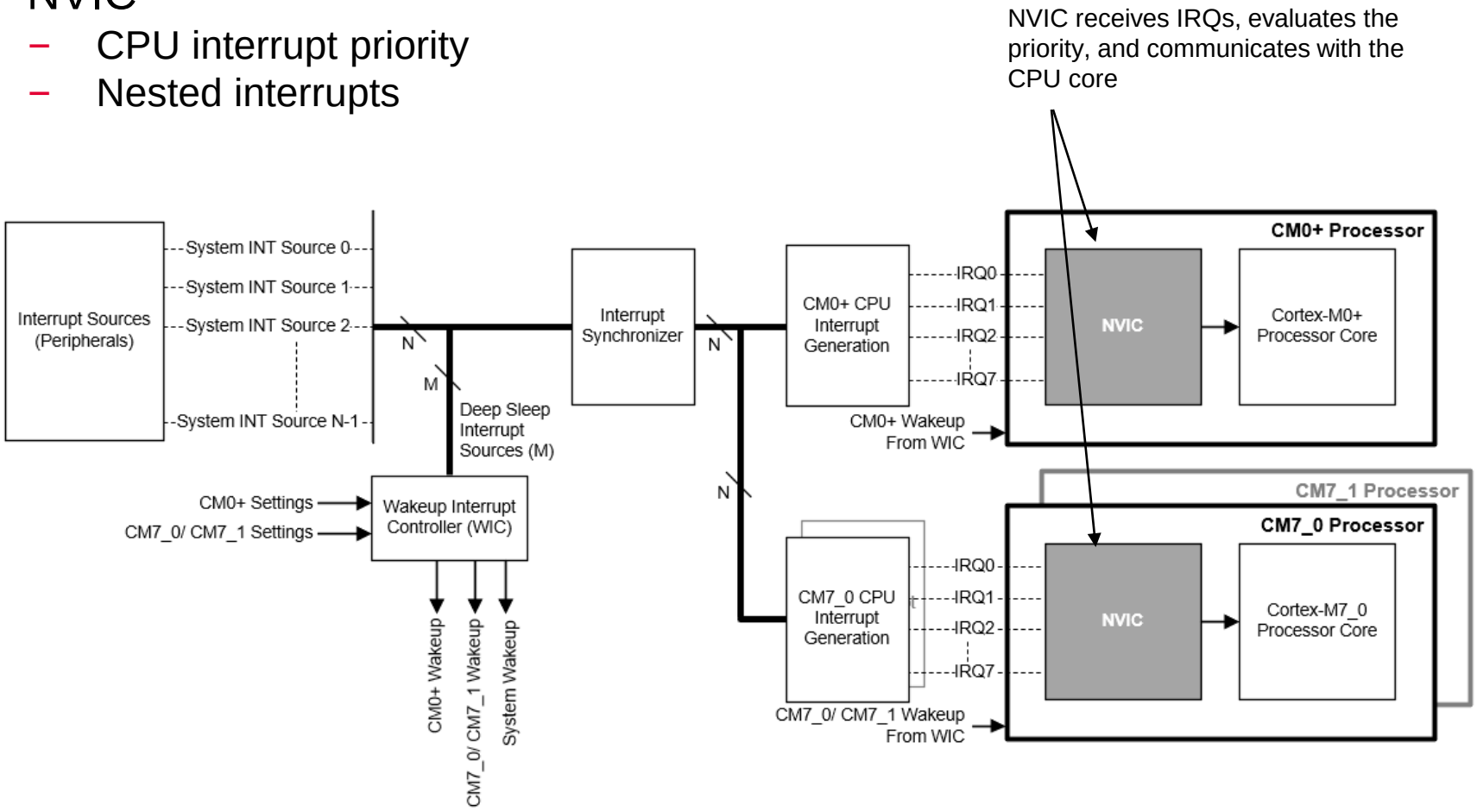
```
void CM7_0/CM7_1_CpuIntr0_Handler (void)
{
uint32_t system_int_idx;
SystemIntr_Handler handler;
if(CPUSS_CM7_0/CM7_1_INT_STATUS[0].SYSTEM_INT_VALID)
{
system_int_idx = CPUSS_CM7_0/CM7_1_INT_STATUS[0].SYSTEM_INT_IDX;
handler = SystemIntr_Table[system_int_idx];
handler(); // jump to system interrupt handler
}
else
{
// Triggered by software or because software cleared a peripheral interrupt flag
// but did not clear the Pending flag at NVIC
}
}
…
void CM7_0/CM7_1_CpuIntr7_Handler (void)
{
uint32_t system_int_idx;
SystemIntr_Handler handler;
if(CPUSS_CM7_0/CM7_1_INT_STATUS[7].SYSTEM_INT_VALID)
{
system_int_idx = CPUSS_CM7_0/CM7_1_INT_STATUS[7].SYSTEM_INT_IDX;
handler = SystemIntr_Table[system_int_idx];
handler(); // jump to system interrupt handler
}
else
{
// Triggered by software or because software cleared a peripheral interrupt flag
// but did not clear the Pending flag at NVIC
}
}
```

```
void CM7_0/CM7_1_SystemIntr0_Handler (void)
{
// Clear the peripheral interrupt request flag by register write
// Read back the register, to ensure completion of register write access
// Handle system interrupt 0.
}
…
void CM7_0/CM7_1_SystemIntr1022_Handler (void)
{
// Clear the peripheral interrupt request flag by register write
// Read back the register, to ensure completion of register write access
// Handle system interrupt 1022.
}
```


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NVIC

- Interrupt architecture components
  - NVIC
    - CPU interrupt priority
    - Nested interrupts



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Arm® provides additional reference material on their webpage at:
infocenter.arm.com

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Exception vector table (1/2)

› The exception vector tables store the entry point addresses for all exception handlers in Cortex®-M0+, and Cortex® M7 cores

Cortex®-M0+ Exception Vector Table

Exception #	Exception	Exception Priority	Vector Address
–	Initial stack pointer value	Not applicable (N/A)	Start_Address = 0x0000 or CM0P_SCS_VTOR[1]
1	Reset	–3, highest priority	Start_Address + 0x04
2	Non-maskable Interrupt (NMI)	–2	Start_Address + 0x08
3	Hard fault	–1	Start_Address + 0x0C
4–10	Reserved	N/A	Start_Address + 0x10 to Start_Address + 0x28
11	Supervisory call (SVCall)	Configurable (0–3)	Start_Address + 0x2C
12–13	Reserved	N/A	Start_Address + 0x30 to Start_Address + 0x34
14	Pend supervisory (PendSV)	Configurable (0–3)	Start_Address + 0x38
15	System tick timer (SysTick)	Configurable (0–3)	Start_Address + 0x3C
16	External interrupt (IRQ0)	Configurable (0–3)	Start_Address + 0x40
…	…	…	…
23	External interrupt (IRQ7)	Configurable (0–3)	Start_Address + 0x5C
24	Internal (SW only) interrupt (IRQ8)	Configurable (0-3)	Start_Address + 0x60
…	…	…	…
31	Internal (SW only) interrupt (IRQ15)	Configurable (0-3)	Start_Address + 0x7C

[1] Start Address = 0x0000 on reset and is later modified in the user code by updating the CM0P_SCS_VTOR register

Hint Bar

Review TRM section 12.3.3 for additional details

IRQ0-IRQ7 are connected to the System Interrupt generation logic

IRQ8-IRQ15 can be triggered by software only and are not connected to any peripheral

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Exception vector table (2/2)

Cortex®-M7 Exception vector table

Exception #	Exception	Exception priority	Vector address
–	Initial stack pointer value	–	Start_Address = 0x0000 or CM7_0/CM7_1_SCS_VTOR[1]
1	Reset	–3, highest priority	Start _Address + 0x0004
2	Non-maskable Interrupt (NMI)	–2	Start _Address + 0x0008
3	Hard fault	–1	Start _Address + 0x000C
4	Memory management fault	Configurable (0–7)	Start _Address + 0x0010
5	Bus fault	Configurable (0–7)	Start _Address + 0x0014
6	Usage fault	Configurable (0–7)	Start _Address + 0x0018
7–10	Reserved	–	–
11	Supervisory call (SVCall)	Configurable (0–7)	Start _Address + 0x002C
12–13	Reserved	–	–
14	Pend supervisory (PendSV)	Configurable (0–7)	Start _Address + 0x0038
15	System tick timer (SysTick)	Configurable (0–7)	Start _Address + 0x003C
16	External interrupt (IRQ0)	Configurable (0–7)	Start _Address + 0x0040
...	...	...	...
23	External interrupt (IRQ7)	Configurable (0–7)	Start _Address + 0x005C
24	Internal (SW only) interrupt (IRQ8)	Configurable (0–7)	Start _Address + 0x60
...	...	...	...
31	Internal (SW only) interrupt (IRQ15)	Configurable (0-7)	Start _Address + 0x7C

[1] Start Address = 0x0000 on reset and is later modified by the user code by updating the CM7_0/CM7_1_SCS_VTOR register

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Review TRM section 12.3.3 for additional details

IRQ0-IRQ7 are connected to the System Interrupt generation logic

IRQ8-IRQ15 can be triggered by software only and are not connected to any peripheral

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CPU interrupt priority

- The priority of each interrupt can be configured to eight levels for Cortex® M7 and four levels for Cortex®-M0+
- Use case for CPU interrupt priority
  - Example of priority levels and interrupts for application

High

Priority Level

Low

-2	:	Fault	NMI exception, protection violation
0	:	GPIO	Ignition detection, wakeup use
1	:	CAN	Communication with other ECU
2	:	LIN/UART	Communication with other ECU
3	:	SCB	Communication with external IC
4	:	TCPWM	Task management
5	:	Event Generator	Wakeup use
6	:	ADC	Sensor data acquisition
7	:	RTC	Real-time clock alarm

Main routine

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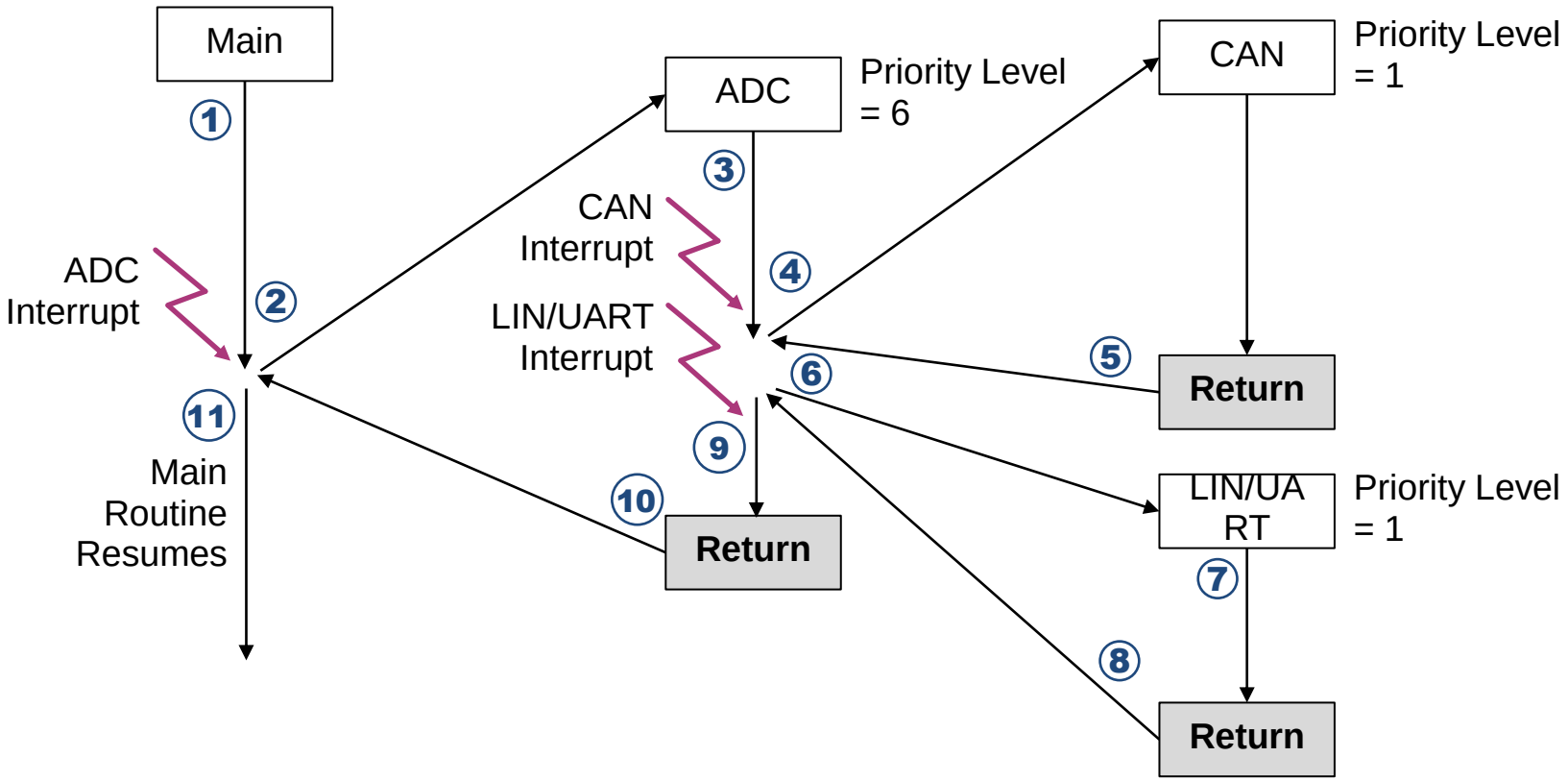
Review TRM section 12.5 for additional details

Refer to each device datasheet for the list of system interrupts

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Nested interrupts

- Depending on the interrupt priority level, nested interrupts are possible
- Use case for nested interrupts



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CAN is serviced before LIN based on the index order of system interrupts

Refer to each device datasheet for the list of system interrupts

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Enabling and disabling interrupts

- The NVICs of CM0+ and CM7 cores provide registers to individually enable and disable the CPU interrupts in software
- CM0+ and CM7 interrupts are enabled and disabled using the ISER and ICER
- If an interrupt is not enabled, the NVIC will not process the interrupt requests on that interrupt line
- CM0+ and CM7 provide additional registers to control the activation of exceptions/interrupts based on their priority
  - PRIMASK: Prevent activation of exceptions having configurable priority
  - FAULTMASK: Prevent activation of all exceptions other than NMI
  - BASEPRI: Prevent activation of exceptions having the same or lower priority than the BASEPRI

Hint Bar

Review TRM section 12.7 for additional details

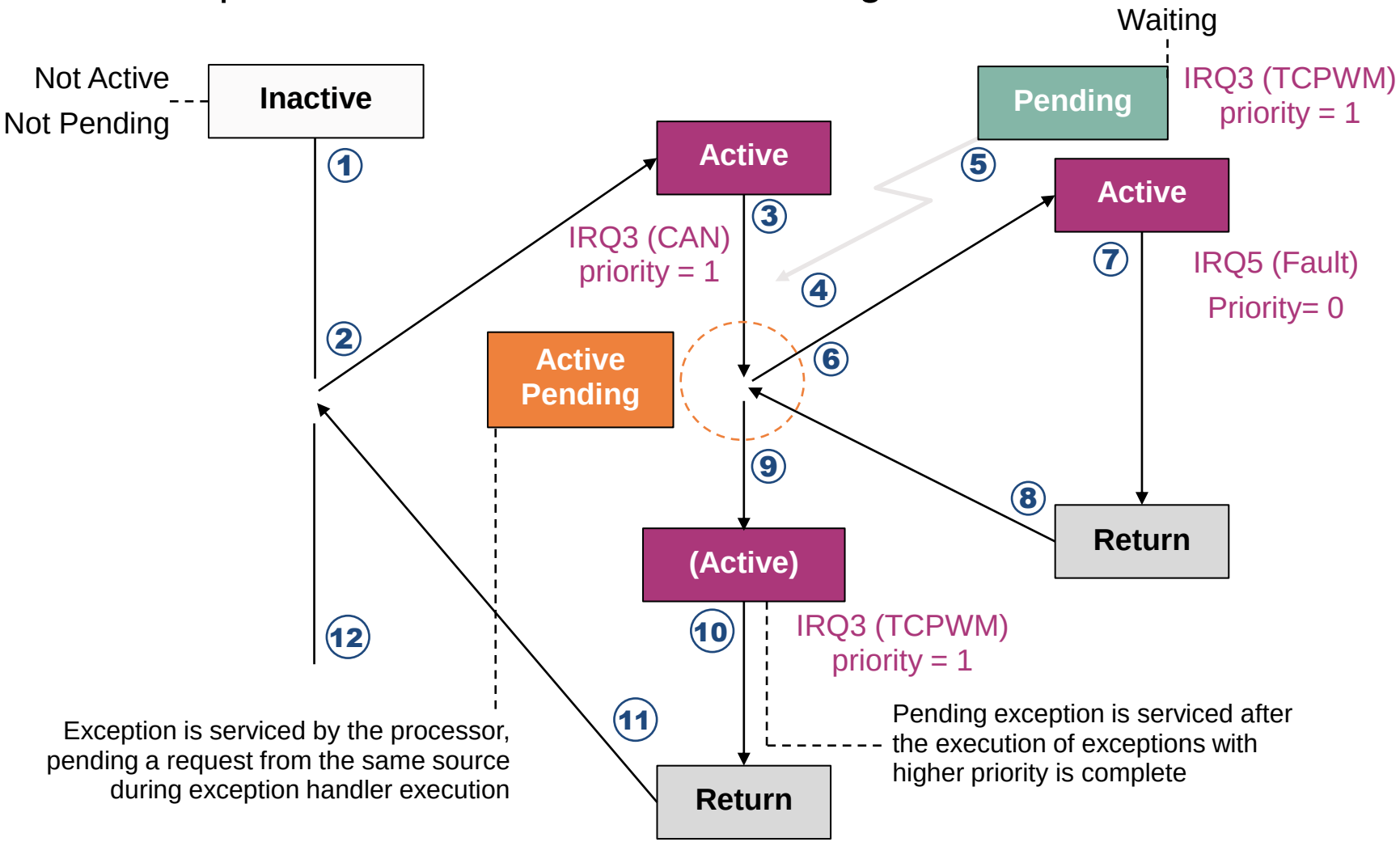
Interrupt Set-Enable Register (ISER)

Interrupt Clear-Enable Register (ICER)

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Exception states

› Each exception can be in one of the following states:



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Review TRM section 12.8 for additional details.

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Appendix

Number of interrupts

- Maximum number of system interrupts and wakeup interrupts varies by device.

Series	Maximum number of system interrupts	Maximum number of wakeup interrupts
XMC7200	567	51
XMC7100	567	51

Hint Bar

Refer to each device datasheet for the list of system interrupts

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Revision history

Revision	ECN	Submission date	Description of change
**	7736175	2022-03-24	Initial release

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