Customer training workshop

XMC7000 Microcontroller Flash

Target products

Target product list for this training material

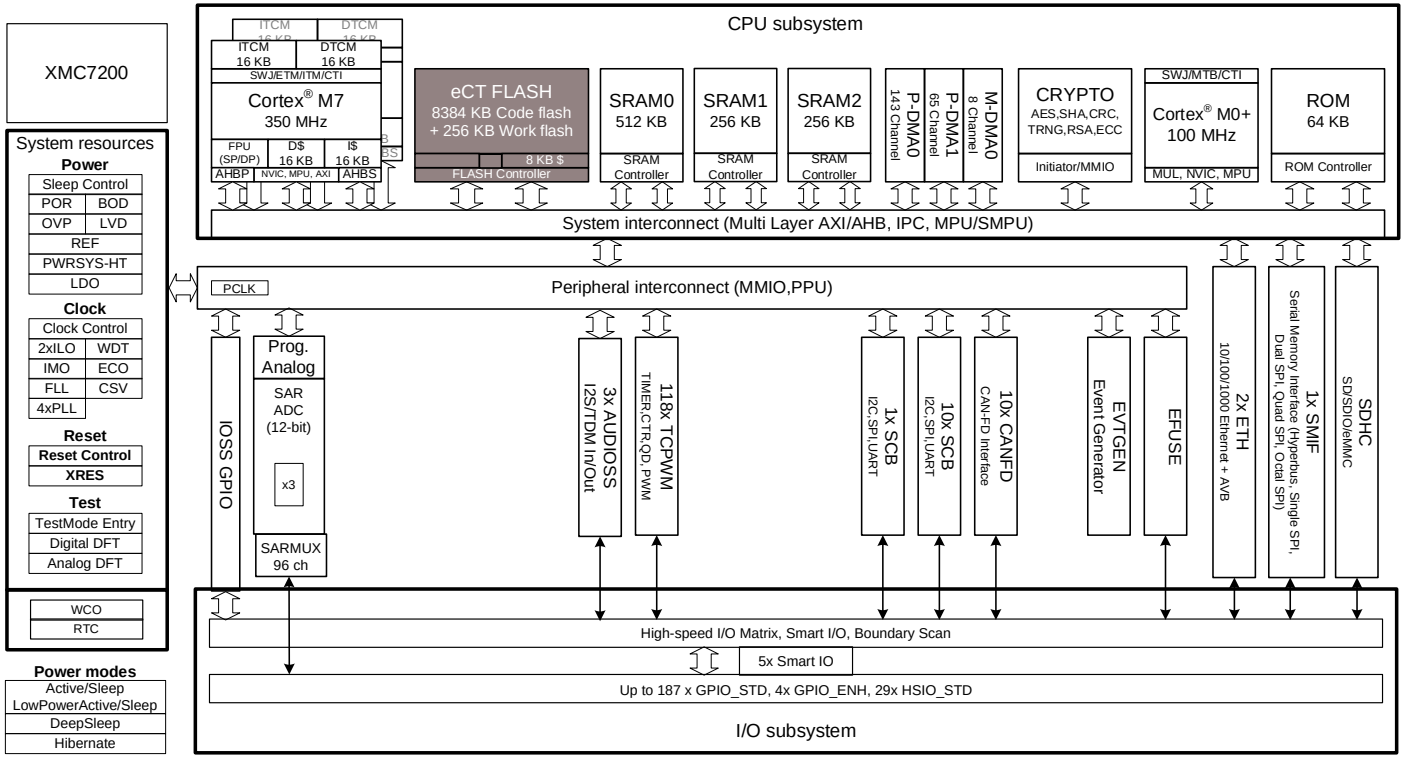
Family category	Series	Code flash memory size
XMC7200	XMC7200-8M	Up to 8384KB
XMC7100	XMC7100-4M	Up to 4160KB

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XMC7200 - 8M family

Introduction to XMC7200-8M

› Flash is part of the CPU subsystem



Hint Bar

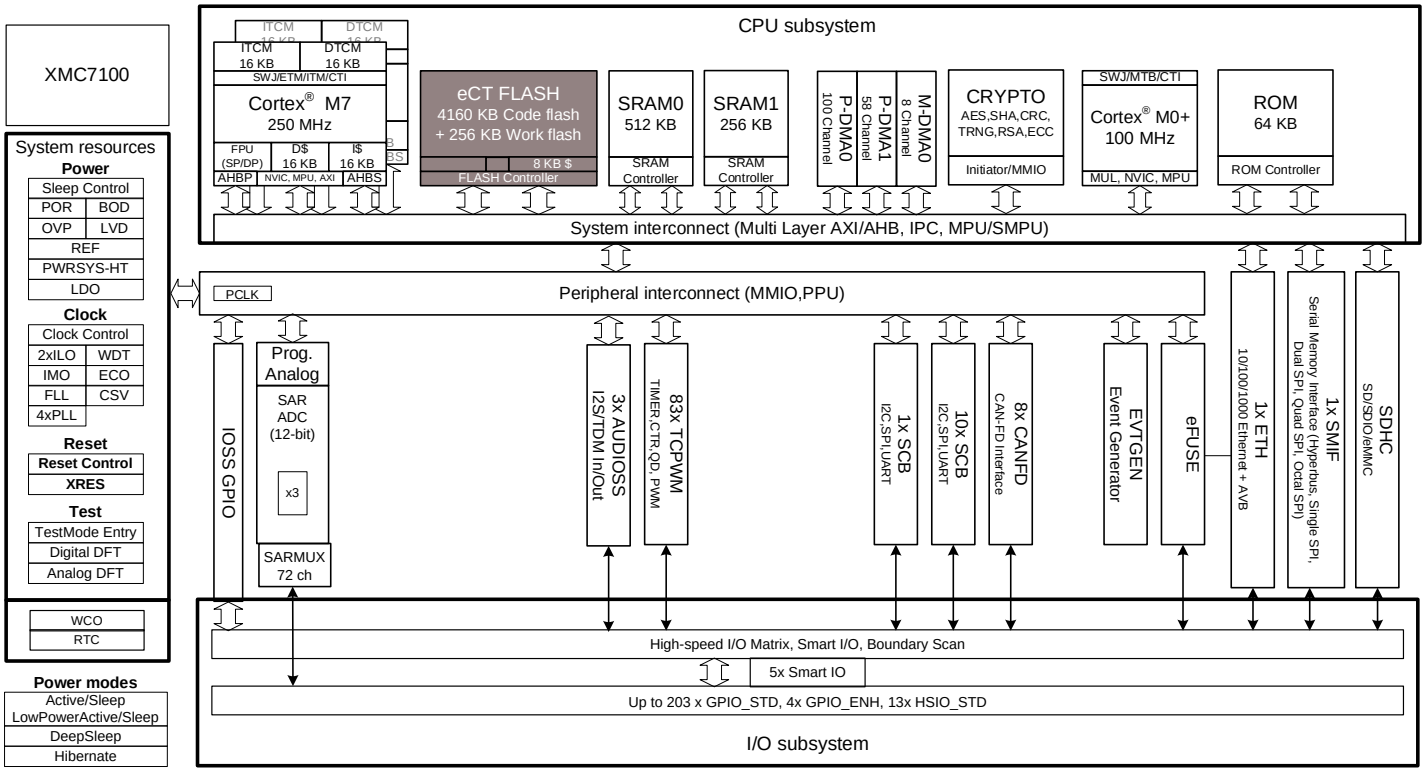
Review TRM chapters 8 and 9 for additional details

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XMC7100 - 4M family

Introduction to XMC7100-4M

› Flash is part of the CPU subsystem



Hint Bar

Review TRM chapters 8 and 9 for additional details

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Flash overview

- XMC7200/XMC7100 have Code flash and Work flash
  - Code flash is used for user program code
  - Work flash is used for long-term data retention
- Cache
  - XMC7200/XMC7100
    - CM0+: 8KB cache in flash; read-only capacity with an LRU replacement scheme
    - CM7: CPU has its own caches (16KB I-cache/16KB D-cache)
- Flash wait states
  - XMC7200/XMC7100
    - 0 wait cycle for CLK_MEM2 ≤ 100 MHz
    - 1 wait cycle for 100 MHz < CLK_MEM ≤ 200 MHz

Hint Bar

XMC7200: Review Datasheet chapters 3 and 4 for additional details

XMC7100: Review Datasheet chapters 4

[1] High-frequency clock
[2] Memory clock. This clock is a divided version of CLK_HF.

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Flash overview

Feature	Code Flash		Work Flash	
	XMC7200	XMC7100	XMC7200	XMC7100
Memory size	8384 KB (8128 KB + 256 KB)	4160 KB (4032 KB + 128 KB)	256 KB (192 KB + 64 KB)	
Program size	64bit, 256 bit, 4096-bit		32-bit	
ECC function	64-bit + 8-bit Single-error correction/double-error detection (SECDED)		32-bit + 7-bit Single-error correction/double-error detection (SECDED)	
Erase sector size	32KB for large sector and 8KB for small sector		2KB for large sector and 128 bytes for small sector	
Security	Supported		Supported	
Single bank and dual bank modes	Supported		Supported	
Reading while programming/erasing	Supported		Supported	
Program/Erase cycles/ data retention time @ 85 °C	1,000/20 years		250,000/10 years	

Hint Bar

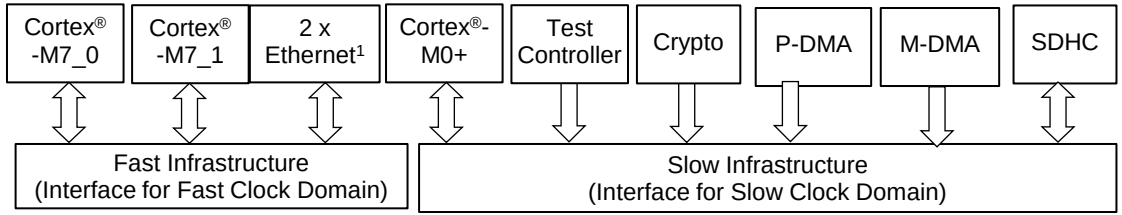
Review TRM Sections 8 and 9

Review the Device Security section for additional details on security

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Block diagram for XMC7000 family

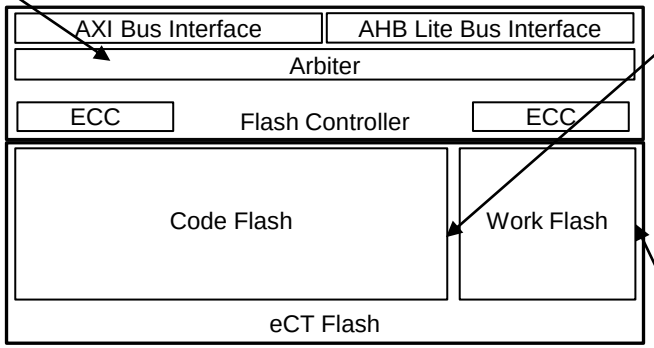
› Cortex®-M7_0, Cortex®-M7_1, and Cortex®-M0+ cores can access code flash and work flash via fast/slow infrastructure



The Arbiter component performs priority-based arbitration according to the master identifier (listed in the table below)

Master Identifier	Bus Master
0	Cortex®-M0+ CPU
1	Cryptography Component
2	P-DMA0
3	P-DMA1
4	M-DMA
5	SDHC
9	Ethernet 0[1]
10	Ethernet 1[1]
13	Cortex®-M7_1 CPU
14	Cortex®-M7_0 CPU
15	Test Controller

[1]XMC7200: 2ch, XMC7100: 1ch (Ethernet 0 only)



*This figure is an example of some blocks only. Refer to the TRM for details.

- XMC7200: Up to 8384 KB (8128 KB + 256 KB)
- XMC7100: UP to 4160 KB (4032 KB + 128 KB)
- Single/Dual Bank Mode Supported
- ECC: 64-bit Data + 8 ECC bit
- Program/Erase Cycle/Retention Time: 1,000/20 Years

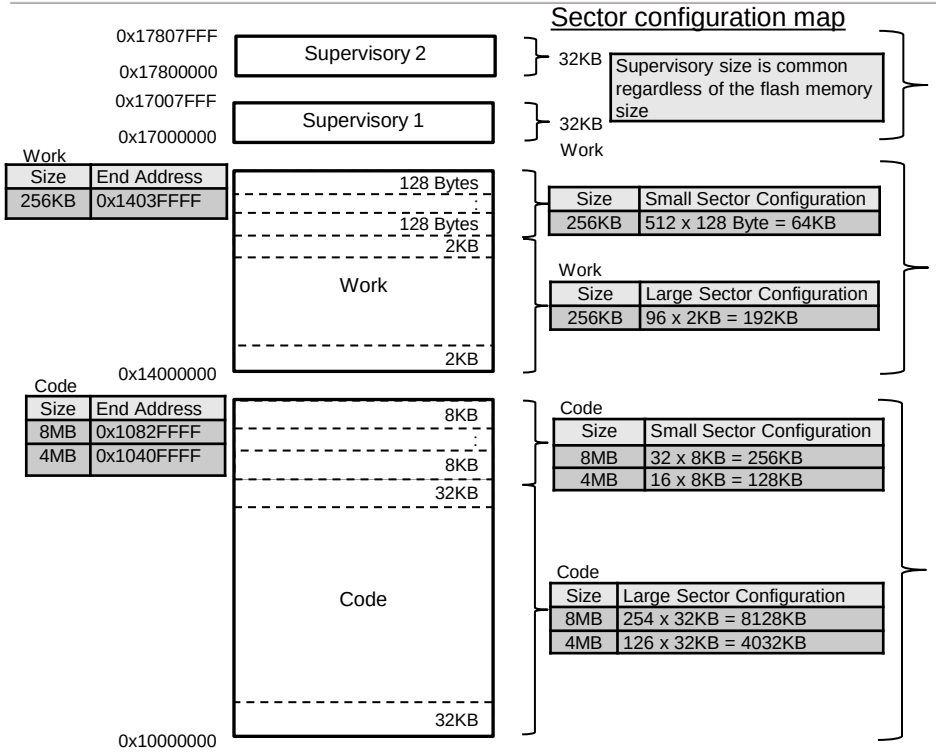
- XMC7000: Up to 256 KB (192 KB + 64 KB)
- Single/Dual Bank Mode Supported
- ECC: 32-bit Data + 7 ECC Bit
- Program/Erase Cycle/Retention Time: 250,000/10 Years

Hint Bar

Review Datasheet Chapter 4

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Sector configuration



Sector configuration map

32KB — Supervisory size is common regardless of the flash memory size

32KB

Work

Size	Small Sector Configuration
256KB	512 x 128 Byte = 64KB

Work

Size	Large Sector Configuration
256KB	96 x 2KB = 192KB

Code

Size	Small Sector Configuration
8MB	32 x 8KB = 256KB
4MB	16 x 8KB = 128KB

Code

Size	Large Sector Configuration
8MB	254 x 32KB = 8128KB
4MB	126 x 32KB = 4032KB

Supervisory Region
Stores trim parameters for hard IP, system configuration parameters, protection and security settings, boot scripts, etc.
Read access to this region is permitted but program/erase access is prohibited.

Work Flash: Stores data or critical parameters
256 KB (192 KB + 64 KB) for both XMC7200 and XMC7100
Optimized to be reprogrammed multiple times by small sector 128 bytes

Code Flash: Stores programs
Up to 8384KB (XMC7200)
Up to 4160KB (XMC7100)

Product Name	Flash Memory Size (Code Flash + Work Flash)
XMC7200	Up to 8384KB (8128KB + 256KB) + 256KB (192KB + 64KB)
XMC7100	Up to 4160KB (4032KB + 128KB) + 256KB (192KB + 64KB)

Example of 8MB/6MB/4MB. For other products, refer to the respective TRMs.

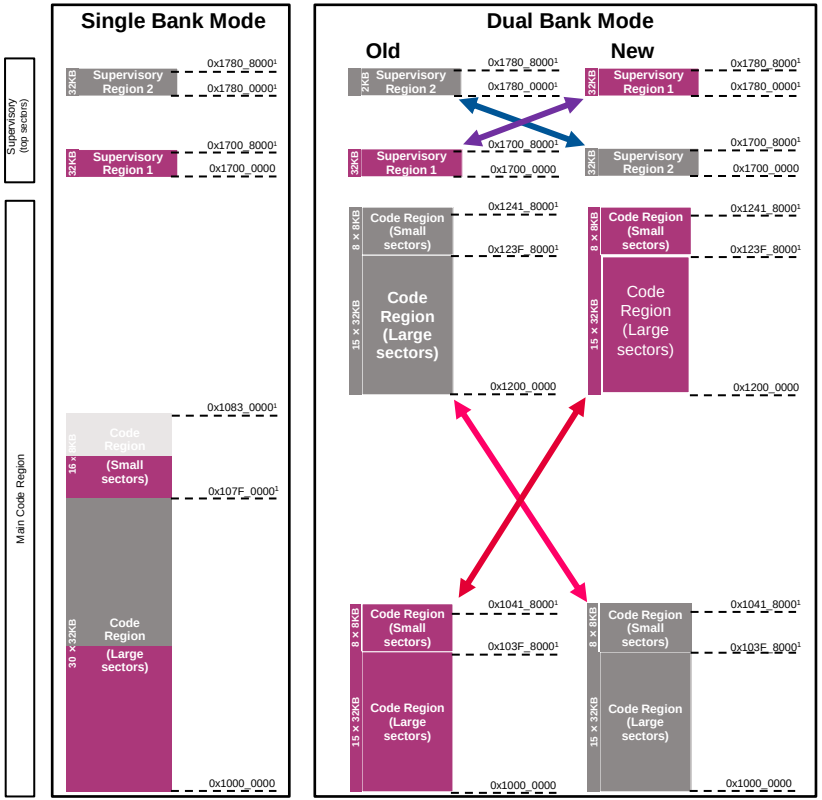
Hint Bar

Review TRM chapters 8 and 9 for additional details

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Bank modes

Representative Product: XMC 7200 (8MB Code Flash)



- Single Bank mode: Entire code and supervisory logical regions are mapped as single contiguous address regions
- Dual Bank mode: Split into two halves, and each half is presented as a separate address region. Can be swapped to support same-location firmware upgrades
  - Old: CPU executes from a current software (pink region) while the higher sectors are programmed with a new software image (gray region)
  - New: When the CPU reboots, the user code changes the main map field, such that the CPU is executed from the new region
- Dual Bank mode enables writing to the other bank while executing flash
- Work flash and code flash both support Dual Bank mode
- Mapping of work flash is independent of mapping of code flash

Hint Bar

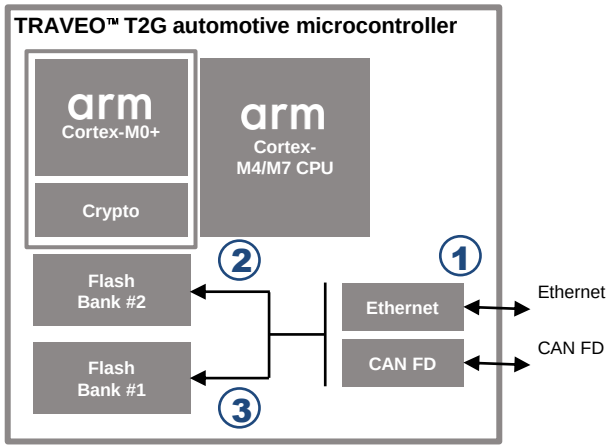
Review TRM chapters 8 and 9 for additional details

[1] Example of 8MB. The end address is different for other code flash memory sizes. For details, refer to the TRM.

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Remap functionality

- Software can control the remap functionality, which enables writing during flash execution in both bank modes
  - The higher and lower physical banks are swapped in the main flash region
- Use case
  - FOTA[1]: The CPU executes from a current software image in the lower bank while the higher bank is programmed with a new software image. When the CPU reboots, the ROM boot code changes the REMAP field such that the CPU executed from the new image is on the higher bank



1. Software update data is received via any communication interface
2. Updated data can be stored in the internal Flash Bank #2. The vehicle sends a command to switch to the new software version at the next ignition cycle. The new software version is activated
3. The previous version is still available in the internal Flash Bank #1 and can be reused as a roll-back solution

Hint Bar

Review TRM chapters 8 and 9 for additional details

[1] Firmware-Over-The-Air

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Error-correcting code (ECC)

- ECC implements single-error correction/double-error detection (SECDED)
  - Default setting of ECC checking for code flash and work flash interface is “Enable”
  - Double-error detection
    - For CPU bus transfers, notify with bus error generation[1]
    - For non-CPU bus transfers, notify with bus error generation
  - Code flash: 64-bit data + 8 ECC bits
  - Work flash: 32-bit data + 7 ECC bits
- Fault report structure
  - Both correctable and non-correctable ECC errors are reported to the fault structure in the same way. All data correction and recovery are left to the ISR. There is no hardware support for writing corrected data back to flash
  - Use case
    - SEC report: Log the error counts
    - DED report: Report to NMI
- Error injection
  - It is possible to generate an ECC error by providing an error injection address and error injection data register
  - Use case
    - As initial diagnosis of ECC before running the application
    - To test the error recovery routines

Hint Bar

Review TRM chapters 8, 9, and 15 for additional details

Interrupt service routine (ISR)

Nonmaskable interrupt (NMI)

[1] It depends on FLASH_CTL register, MAIN_ERR_SILENT bit

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Appendix

Comparison between XMC7200 and XMC7100

Features	XMC 7200	XMC 7100
Code flash memory size	8384KB (8128KB + 256KB)	4160 KB (4032 KB + 128 KB)
Work flash memory size	256KB (192KB + 64KB)	
Bus interface	AXI, AHB-Lite	
Cache	CM0+: Cache inside flash CM7: CPU has own caches (I-Cache, D-Cache)	
Flash wait states	0 wait cycle for CLK_MEM2 ≤ 100 MHz 1 wait cycle for 100 MHz < CLK_MEM ≤ 200 MHz	0 wait cycle for CLK_MEM2 ≤ 100 MHz 1 wait cycle for 100 MHz < CLK_MEM ≤ 160 MHz
Bus master priority of arbiter	0: Cortex®-M0+ CPU 1: Cryptography component 2: P-DMA0 3: P-DMA1 4: M-DMA 5: SDHC 9: Ethernet 0 10: Ethernet 1 13: Cortex®-M7_1 CPU 14: Cortex®-M7_0 CPU 15: Test controller	0: Cortex®-M0+ CPU 1: Cryptography component 2: P-DMA0 3: P-DMA1 4: M-DMA 9: Ethernet 0 13: Cortex®-M7_1 CPU 14: Cortex®-M7_0 CPU 15: Test controller
ECC (SEC/DED)	Code flash: 64-bit + 8-bit and Work flash: 32-bit + 7-bit	
Bank modes	Supported	
Reading while programming/erasing	Supported	
Security	Supported	
Program/Erase cycles/ data retention time @ 85 °C	Code flash: 1,000 cycles/20 years Work flash: 250,000 cycles/10 years	

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Revision History

Revision	ECN	Submission Data	Description of Change
*	7736201	2022-03-24	Initial Release

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