Customer training workshop

XMC7000 MCU fault subsystem

Target products

› Target product families for this training material

Family category	Series	Code Flash Memory Size
XMC7200	XMC7200-8M	Up to 8384KB
XMC7100	XMC7100-4M	Up to 4160KB

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Fault subsystem overview

- Stores fault information
- Supports the following signaling interfaces: reset, interrupt, trigger, or output
- Fault sources:
  - MPU/SMPU/PPU violations
  - Peripheral-specific errors
    - For example: WDT, CSV, and BOD on VDDA, OVD on VDDA and LVD
  - Memory-controller-specific errors
    - For example: SRAM ECC errors and Flash ECC errors
- Communicated as either a bus error or a fault in the fault report structure
- Functionality is available only in Active/Sleep power modes

Hint Bar

Review TRM chapter 15 for additional details

See each device datasheet for Fault Sources

Memory protection unit (MPU)

Shared memory protection unit (SMPU)

Peripheral protection unit (PPU)

Error-correction code (ECC)

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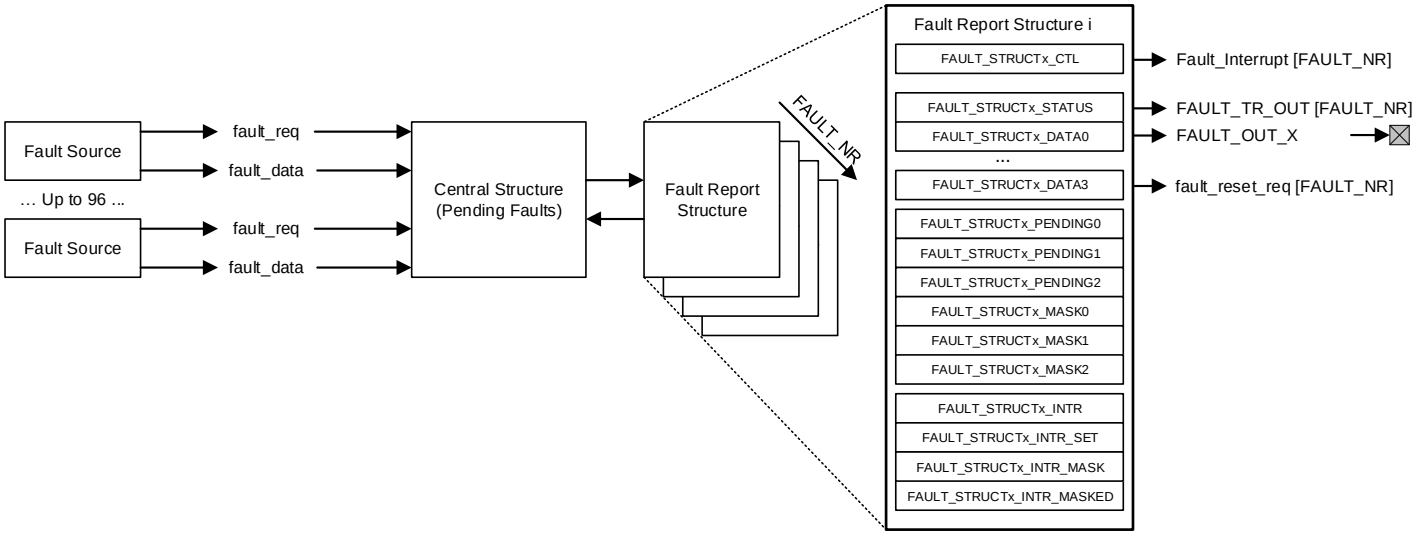
Fault subsystem block diagram

› Fault subsystem components



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Review TRM section 15.1 for additional details

See each device datasheet for Fault Sources

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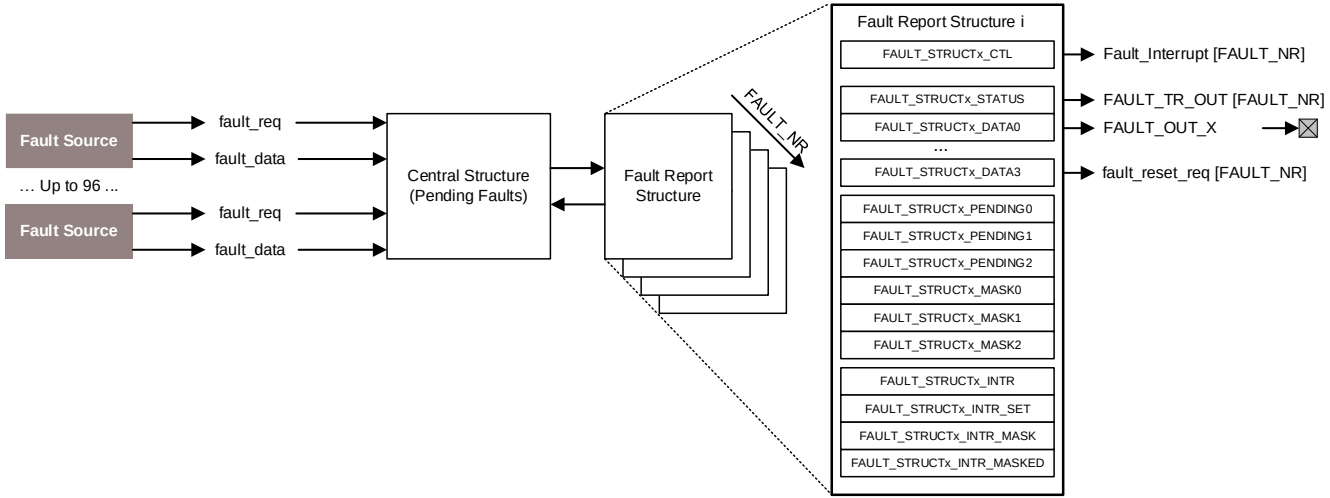
Fault sources

- MPU/SMPU/PPU violations
- Peripheral-specific errors
  - Example: WDT, CSV, and BOD on VDDA, OVD on VDDA, LVD
- Memory-controller-specific errors
  - Examples: SRAM ECC errors, Flash and Flash ECC errors



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Review TRM chapter 15 for additional details

See each device datasheet for Fault Sources

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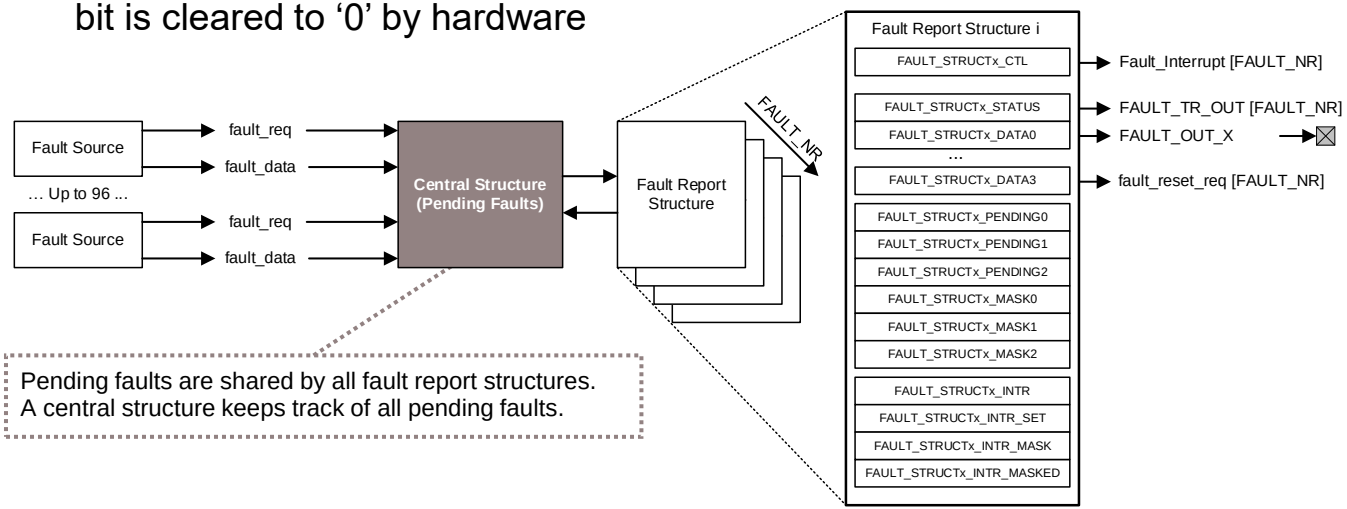
Central structure

- Pending faults are shared by all fault report structures
- Central structure keeps track of all the pending faults
  - FAULT_STRUCTx_PENDINGy[1] registers reflect which of the fault sources are pending
  - When a pending fault is captured by a fault structure, the associated pending bit is cleared to ‘0’ by hardware



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Review TRM section 15.1 and Register TRM for additional details

[1] FAULT_STRUCTx, 'x' signifies the fault structure instance and 'y' in FAULT_STRUCTx_PENDINGy varies from 0 through 2

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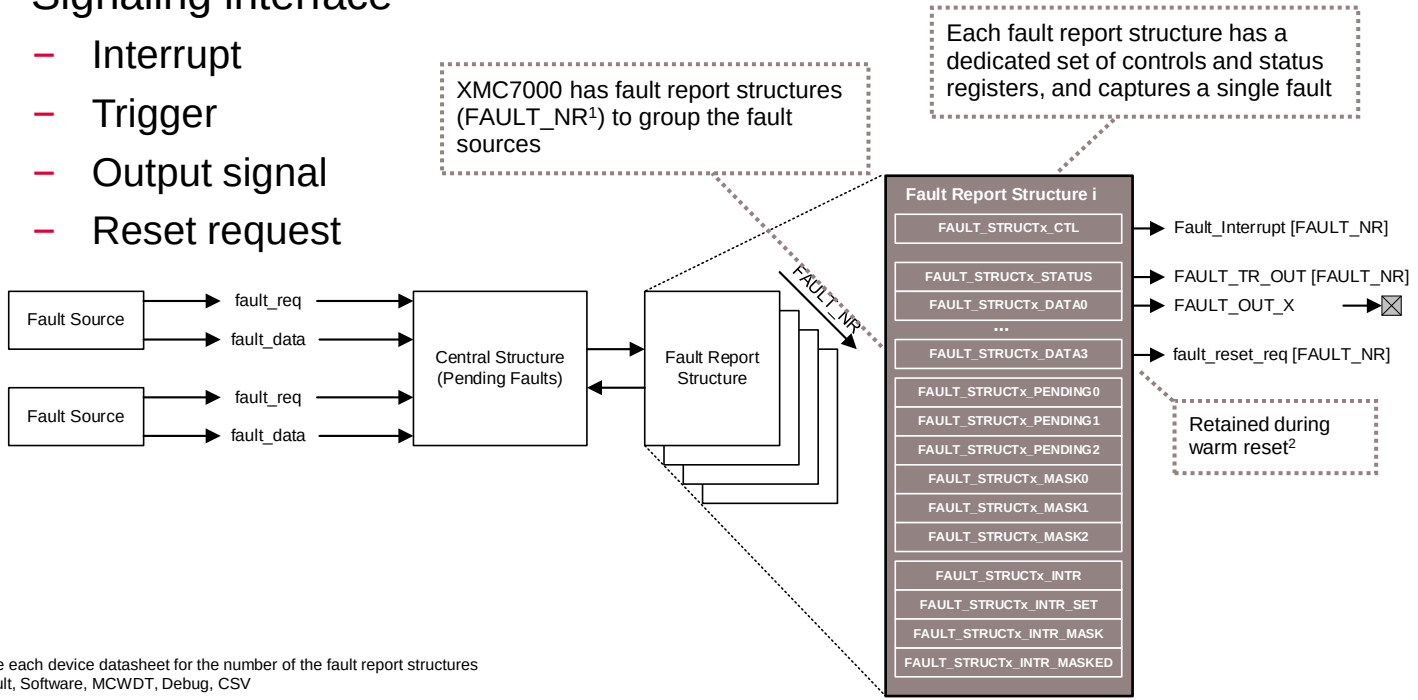
Fault report structure

- Captures fault information
- Signaling interface
  - Interrupt
  - Trigger
  - Output signal
  - Reset request



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Review TRM section 15.1 and Register TRM for additional details

[1] See each device datasheet for the number of the fault report structures
[2] Fault, Software, MCWDT, Debug, CSV

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Captured fault information

- Each fault report structure has a dedicated set of controls and status registers and captures a single fault
- The captured fault information includes:
  - A validity bit field that indicates that a fault is captured
  - A fault index that identifies the fault source
  - Additional fault information
    - Changes depending on the fault source

Fault sources	Additional fault information				
	Fault block	Syndrome	Violating address	Master ID	Access information
MPU/SMPU/PPU/CAN ECC			✓	✓	✓
SRAM/Flash ECC		✓	✓		
Flash bus error			✓	✓	
WDT/CSV/BOD/OVD/LVD	✓				

Hint Bar

Review TRM section 15.1 and Register TRM for additional details

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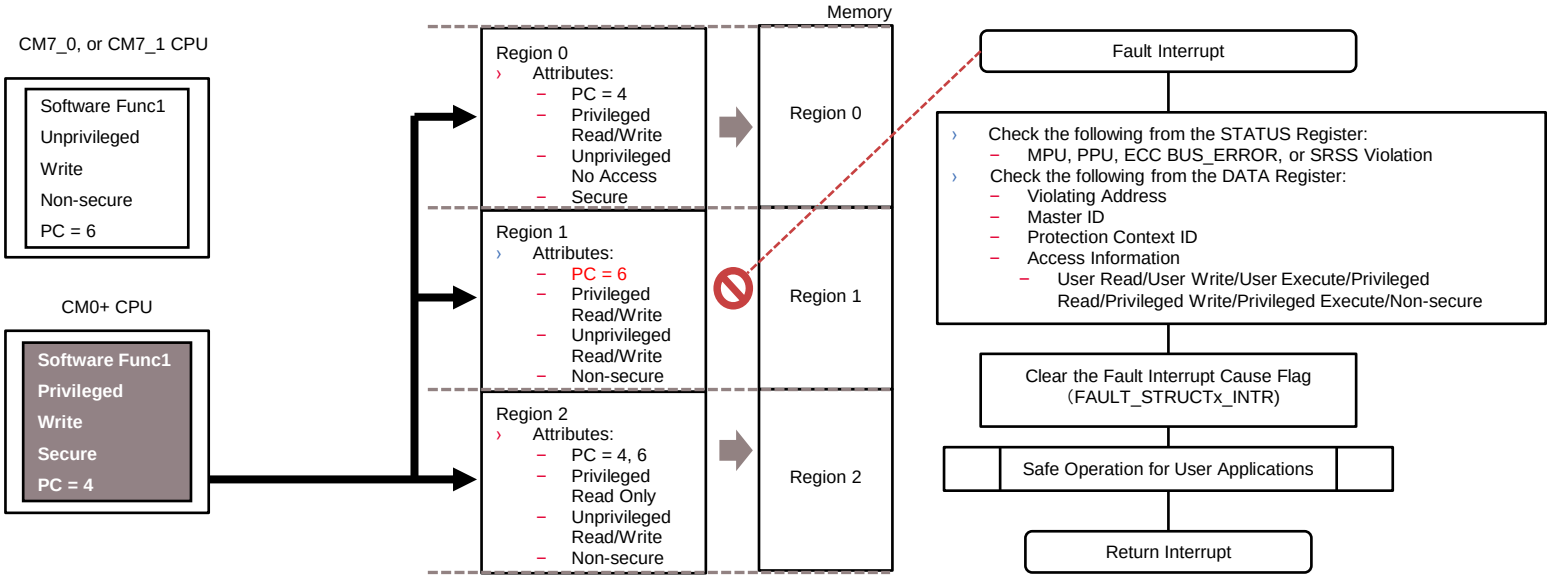
Fault and protection

- Use a fault Interrupt when an SMPU violation is detected
  - Enable Fault Source 0 (CM0+ MPU/SMPU violation) of the MASK register and INTR_MASK to generate the interrupt
- When CM0+ accesses three memory regions (Region 0, 1, 2), as shown below, a fault interrupt occurs
  - Privileged, Write, Secure, Protection Context (PC) = 4, Access to Region 0, 1, 2



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Signaling interface

- The fault subsystem supports a signaling interface that notifies the CPU or the external system that there is a fault
- The following signals are enabled by software:
  - A fault interrupt (“Fault_Interrupt”)
  - A trigger (“FAULT_TR_OUT”)
  - A chip output pin (“FAULT_OUT_X”)
  - A fault reset request (“fault_reset_req”)
- Use Case:

Fault	Signaling interface	Purpose
MPU/SMPU/PPU violation	Interrupt	Check the master and address
ECC correctable error (SEC)	Trigger connects to TCPWM	Log the error counts
LVD/CSV violation	Output pin	Send alarm to system and stop the MCU
MCWDT timeout	Reset request	Recover from abnormal operation

- Advantage
  - Centralizes fault information management and handles each fault according to system requirements

Hint Bar

Review TRM section 15.1 and Register TRM for additional details

Review the Trigger Multiplexer training section for additional trigger details

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Revision History

Revision	ECN	Submission Date	Description of Change
**	7729831	2022-03-17	Initial release

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