# Customer training workshop

# XMC7000 MCU family overview

# Target products

## Target product list for this training material

| Family category | Series | Code flash memory size |
|---|---|---|
| XMC7200 | XMC7200-8M | Up to 8384 KB |
| XMC7100 | XMC7100-4M | Up to 4160 KB |

# XMC7200 - 8M family

# Overview

- Includes Arm® dual Cortex®-M7 and M0+ CPUs, manufactured using a high-performance 40-nm process
- Target applications
  - Industrial drives, robotics, transportation (eBikes, LEVs) , eV chargers
- Features
  - 32-bit CPU subsystem:
    - Two 350-MHz 32-bit Cortex®-M7 CPUs, each with single-cycle multiply, single/double-precision floating point unit (FPU), and memory protection units (MPU)
    - 100-MHz 32-bit Cortex®-M0+ CPU with MPU
  - 8384KMB of code flash along with 256KB of work flash:
    - Dual Bank Mode support for firmware over-the-air (FOTA)
  - SRAM: 1024KB (SRAM0 -512KB, SRAM1 -256 KB , SRAM2 -256KB)
  - Internal 8-MHz (±1%) main oscillator (IMO) and internal low-speed (32-kHz) oscillator (ILO)
  - Internal (up to 300 mA) power supply: $V_{DDD}$ = 2.7 V to 5.5 V
  - External (up to 600 mA) power supply: $V_{DDD}$ = 2.7 V to 5.5 V and $V_{CCD}$ = 1.15 V (1.1 V to 1.2 V)

**Hint Bar**

**Review datasheet and TRM chapter 1 for additional details**

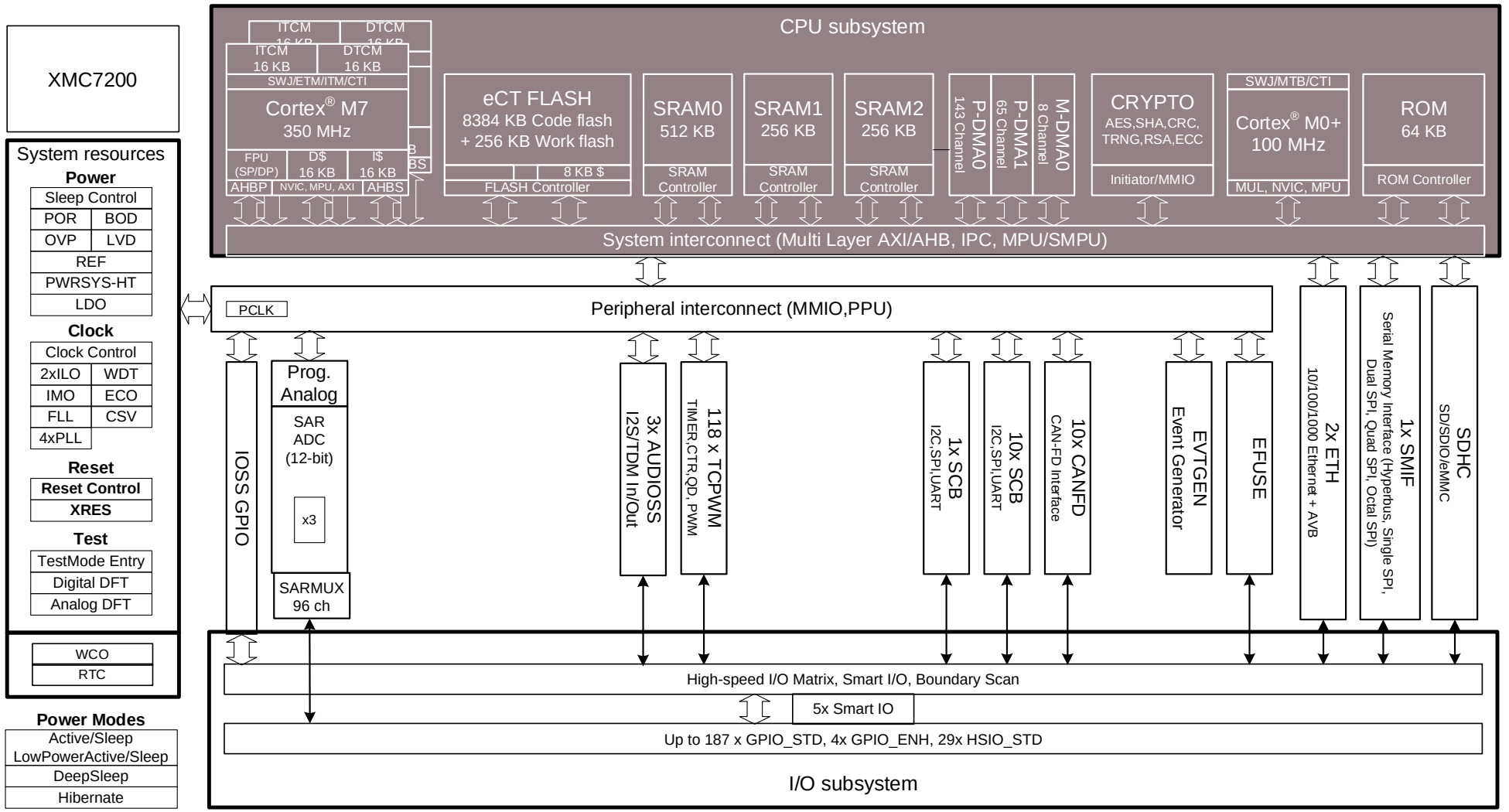
# Overview

- Features (continued)
  - Enhanced Secure Hardware Extension (eSHE) and Hardware Secure Module (HSM) support
  - Debugging is supported over SWD, JTAG controller, and interface-compliant IEEE-1149.1-2001, and flash programming through SWD/JTAG interface
  - Packages:
    - 176-TEQFP, 272-FBGA

**Hint Bar**

**Review datasheet and TRM chapter 1 for additional details**

# XMC7200 architecture diagrams:
# CPU subsystem

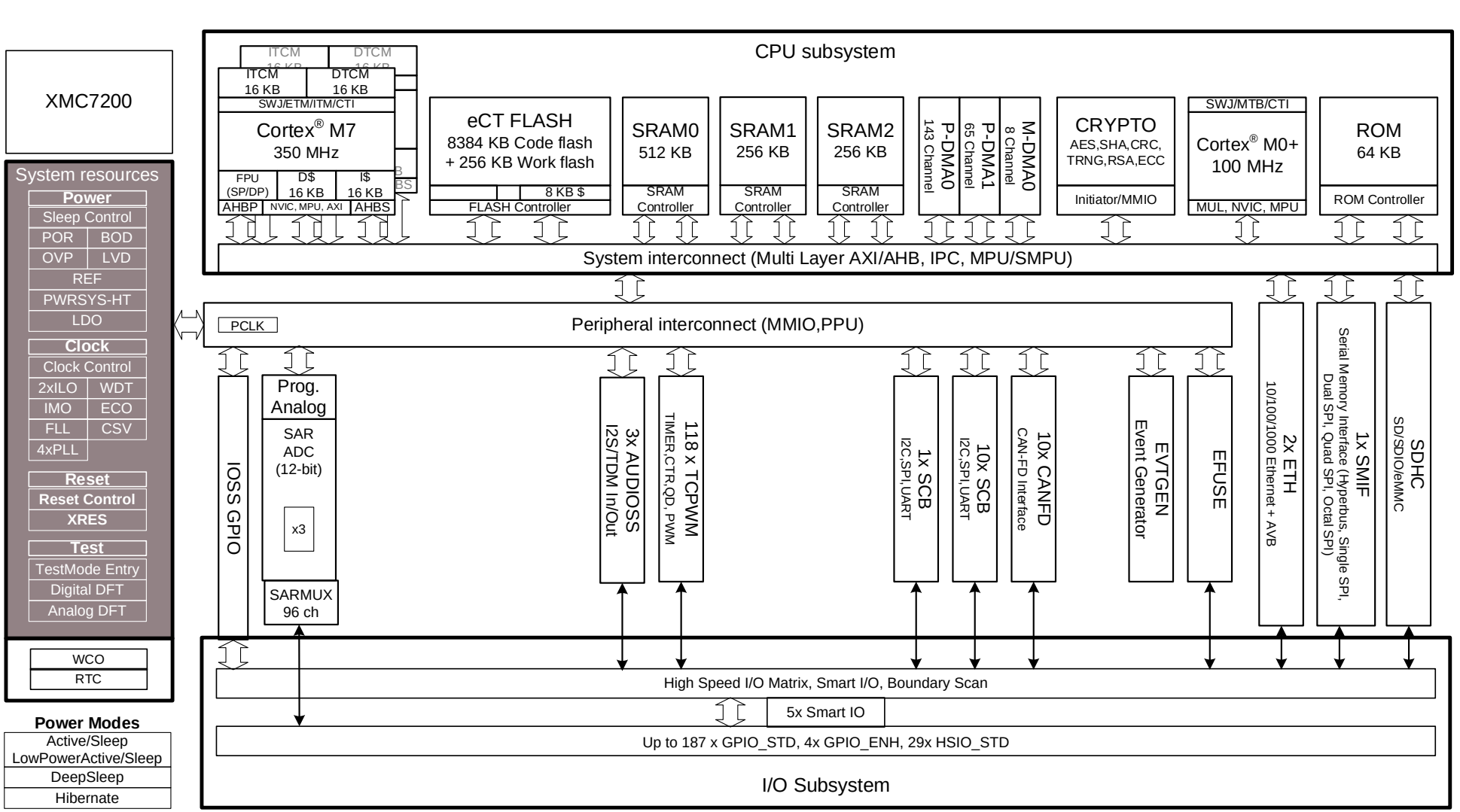



## Hint Bar

**Training section reference**

- **CPU Subsystem**
- **Direct Memory Access (DMA)**
- **Flash**
- **SRAM Interface**
- **Boot (ROM)**
- **Device Security (Crypto)**

# XMC7200 architecture diagrams:
# System resources

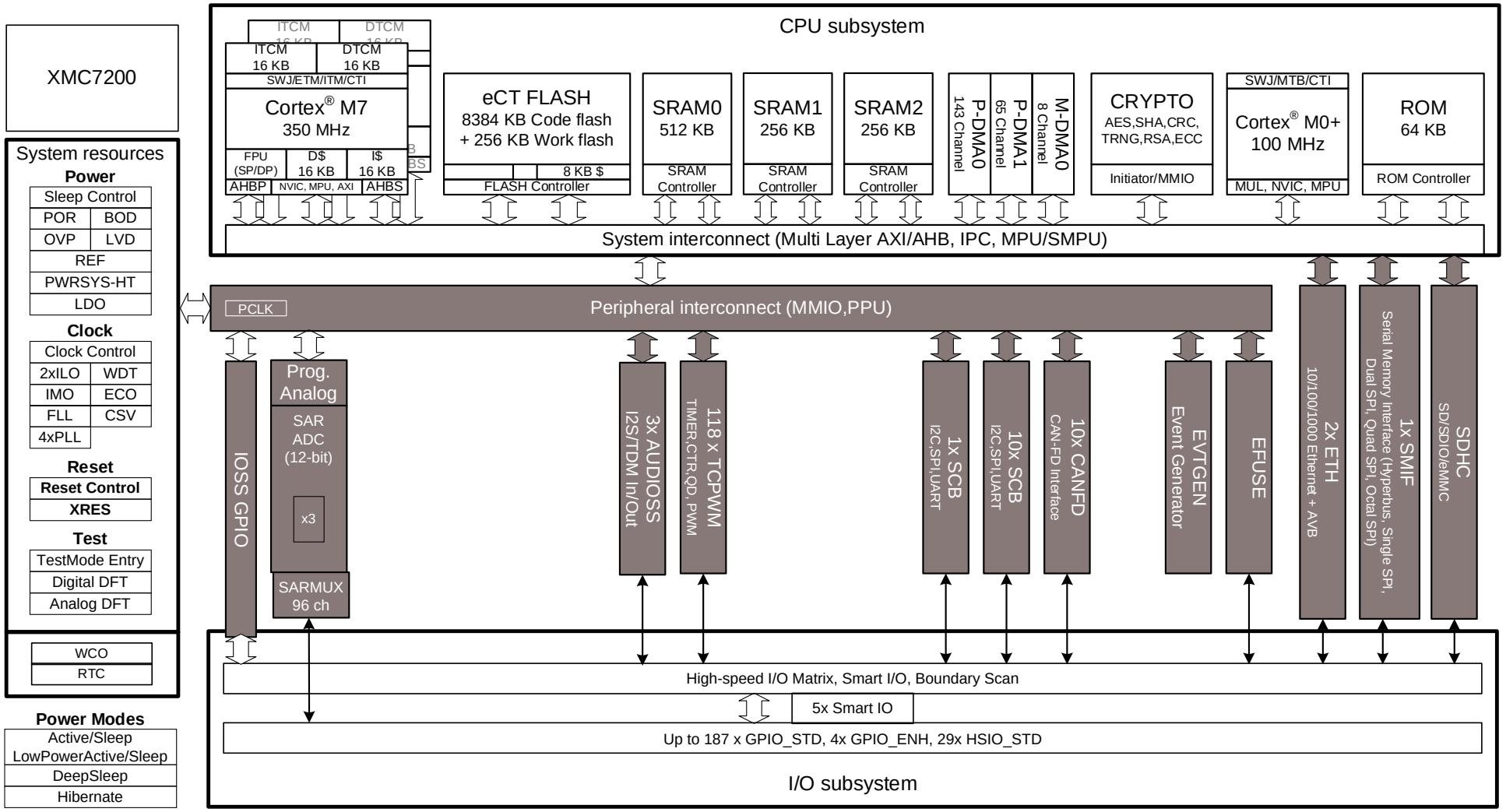



## Hint Bar

**Training section reference**

- **Power Supply and Monitoring**
- **Clock System**
- **Watchdog Timer**
- **Reset System**

# XMC7200 architecture diagrams:
# Peripheral blocks

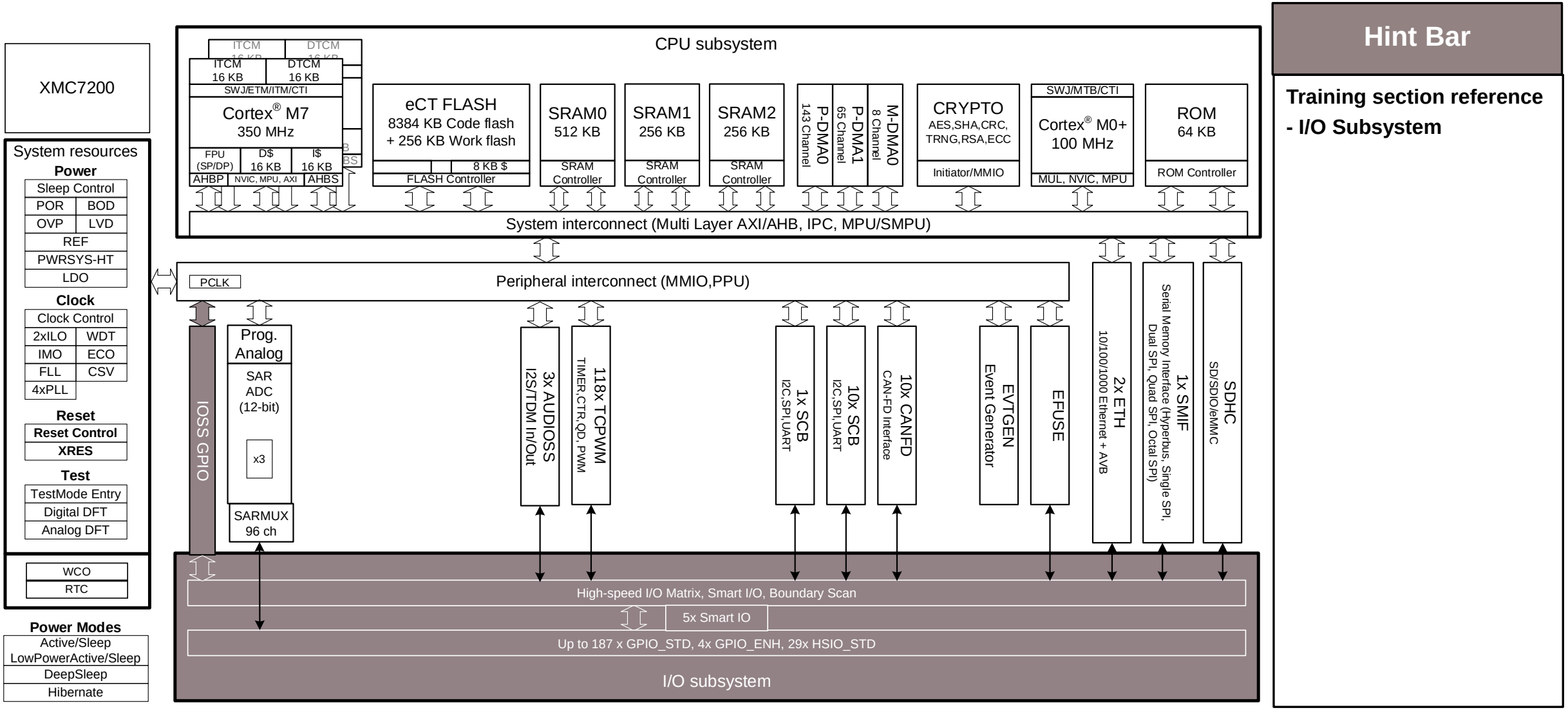



## Hint Bar

**Training section reference**

- **SAR ADC**
- **TCPWM (Timer/Counter/Pulse-Width Modulator)**
- **Serial Communication Blocks (SCB)**
- **CAN FD**
- **Event Generator**
- **CXPI**

# XMC7200 architecture diagrams:
# I/O subsystem




## Hint Bar

**Training section reference**

**- I/O Subsystem**

# XMC7100 - 4M family

# Overview

- Includes Arm® dual Cortex®-M7 and M0+ CPUs, manufactured using a high-performance 40-nm process
- Target applications
  - Industrial drives, transportations (eBikes, LEV), eV chargers
- Features
  - 32-bit CPU subsystem:
    - One or two 250-MHz 32-bit Cortex® -M7 CPUs, each with single-cycle multiply, single/double-precision floating point unit (FPU), and memory protection units (MPU)
    - 100-MHz 32-bit Cortex® -M0+ CPU with MPU
  - 4160KB of code flash along with 256KB of work flash:
    - Dual bank mode support for firmware over-the-air (FOTA)
  - SRAM: 768KB (SRAM0 -512KB, SRAM1-256KB)
  - Internal 8-MHz (±1%) main oscillator (IMO) and internal low-speed (32-kHz) oscillator (ILO)
  - Internal (up to 300 mA) power supply: $V_{DDD}$ = 2.7 V to 5.5 V
  - External (up to 600 mA) power supply: $V_{DDD}$ = 2.7 V to 5.5 V and $V_{CCD}$ = 1.15 V (1.1 V to 1.2 V)

**Hint Bar**

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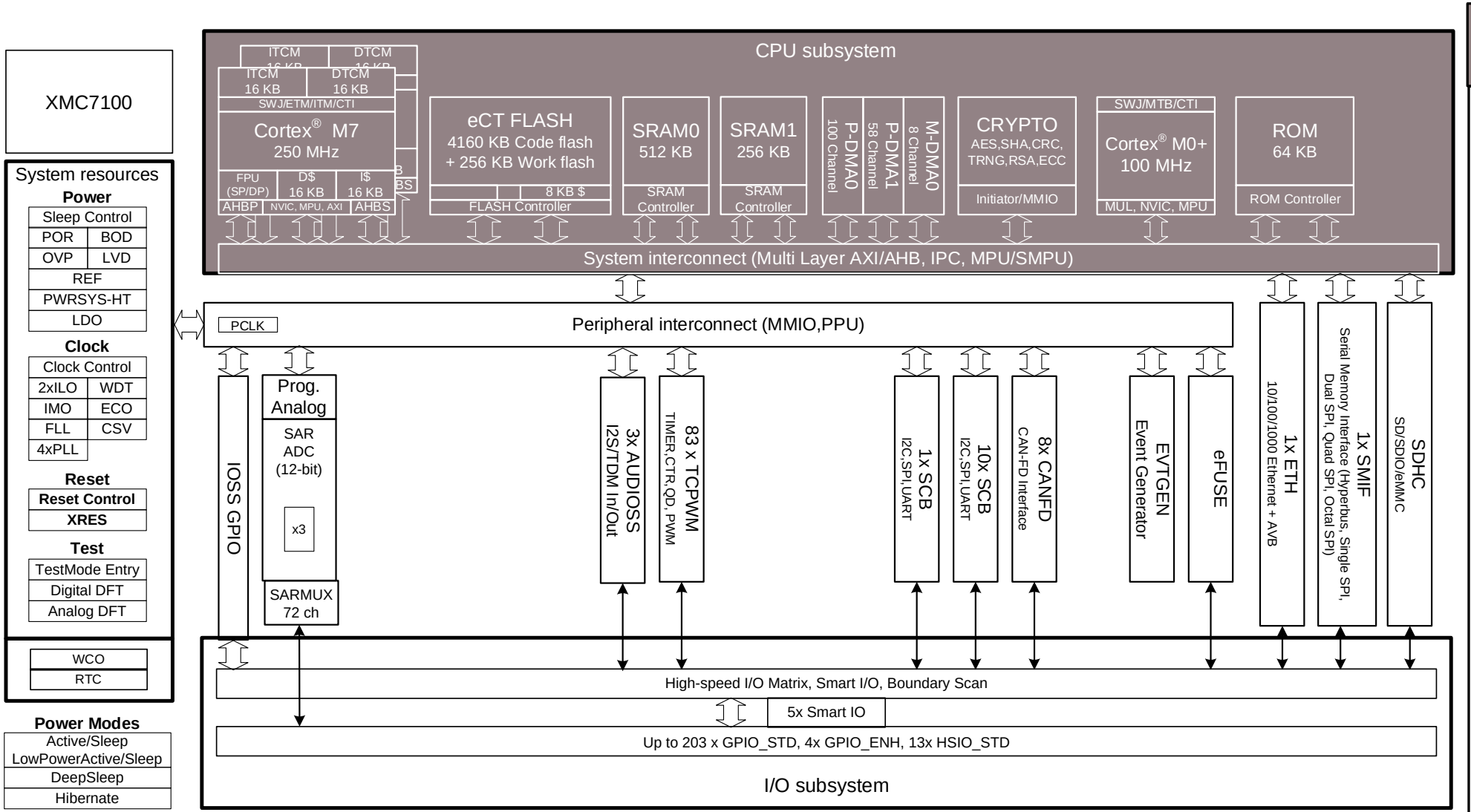
# Overview

- Features (continued)
  - Enhanced Secure Hardware Extension (eSHE) and Hardware Secure Module (HSM) support
  - Debugging is supported over SWD, JTAG controller, and interface-compliant IEEE-1149.1-2001, and Flash programming through SWD/JTAG interface
  - Packages:
    - 100-/144-/176-TEQFP, 272-FBGA

**Hint Bar**

**Review datasheet and TRM chapter 1 for additional details**

# XMC7100 architecture diagrams:
# CPU subsystem

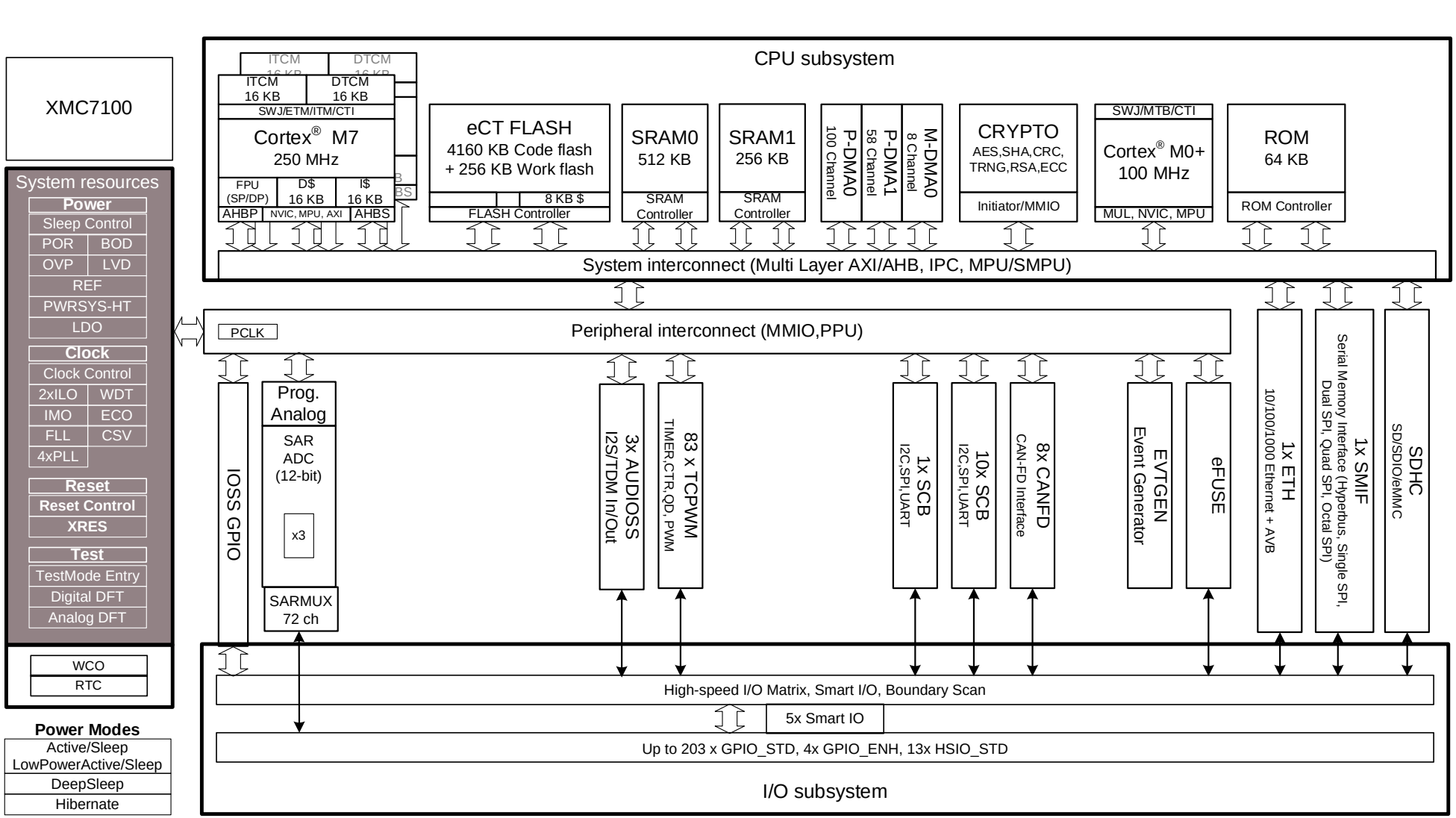



## Hint Bar

**Training section reference**

- **CPU Subsystem**
- **Direct Memory Access (DMA)**
- **Flash**
- **SRAM Interface**
- **Boot (ROM)**
- **Device Security (Crypto)**

# XMC7100 architecture diagrams:
# System resources




## Hint Bar

**Training section reference**

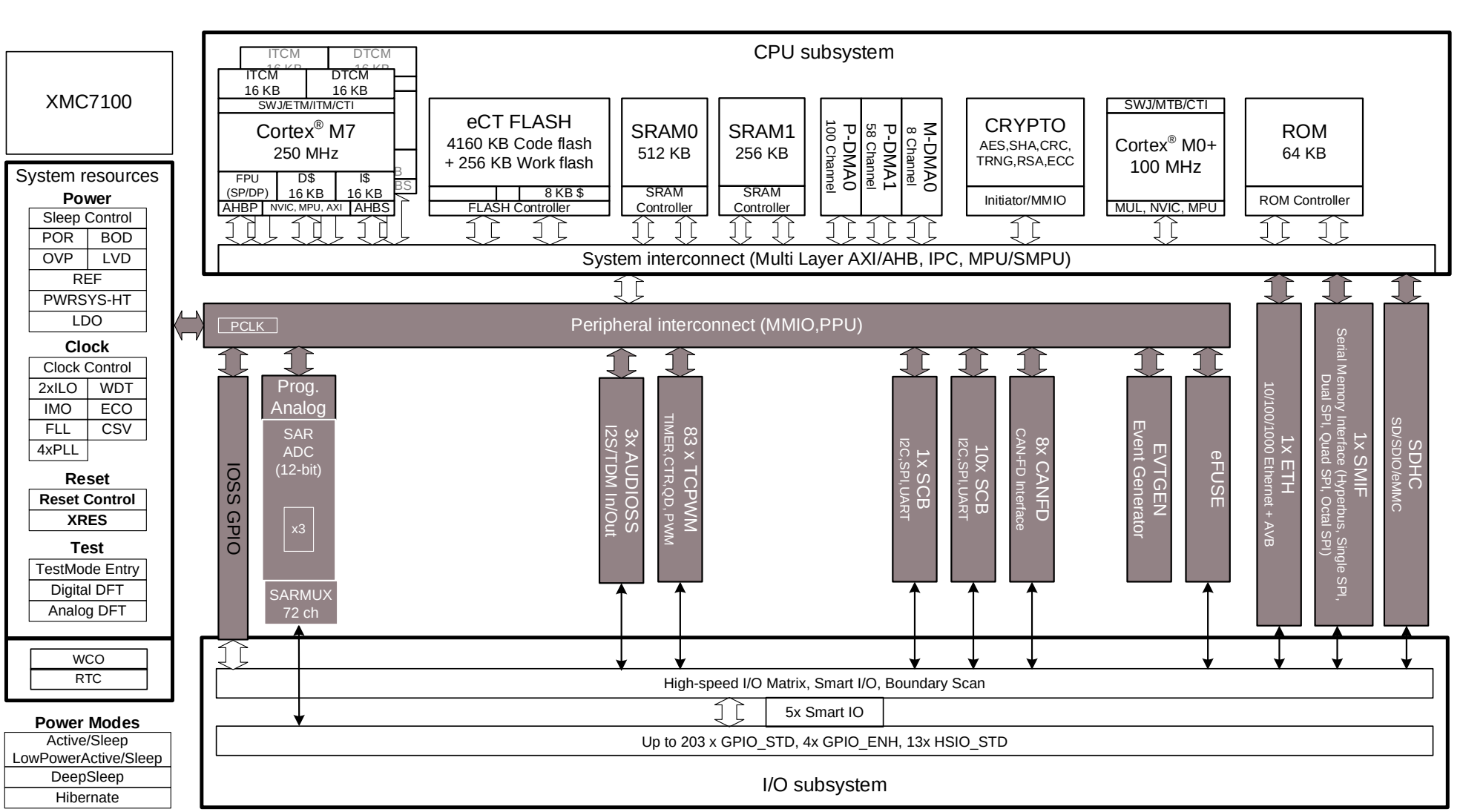
**- Power Supply and Monitoring**

**- Clock System**

**- Watchdog Timer**

**- Reset System**

# XMC7100 architecture diagrams:
# Peripheral blocks

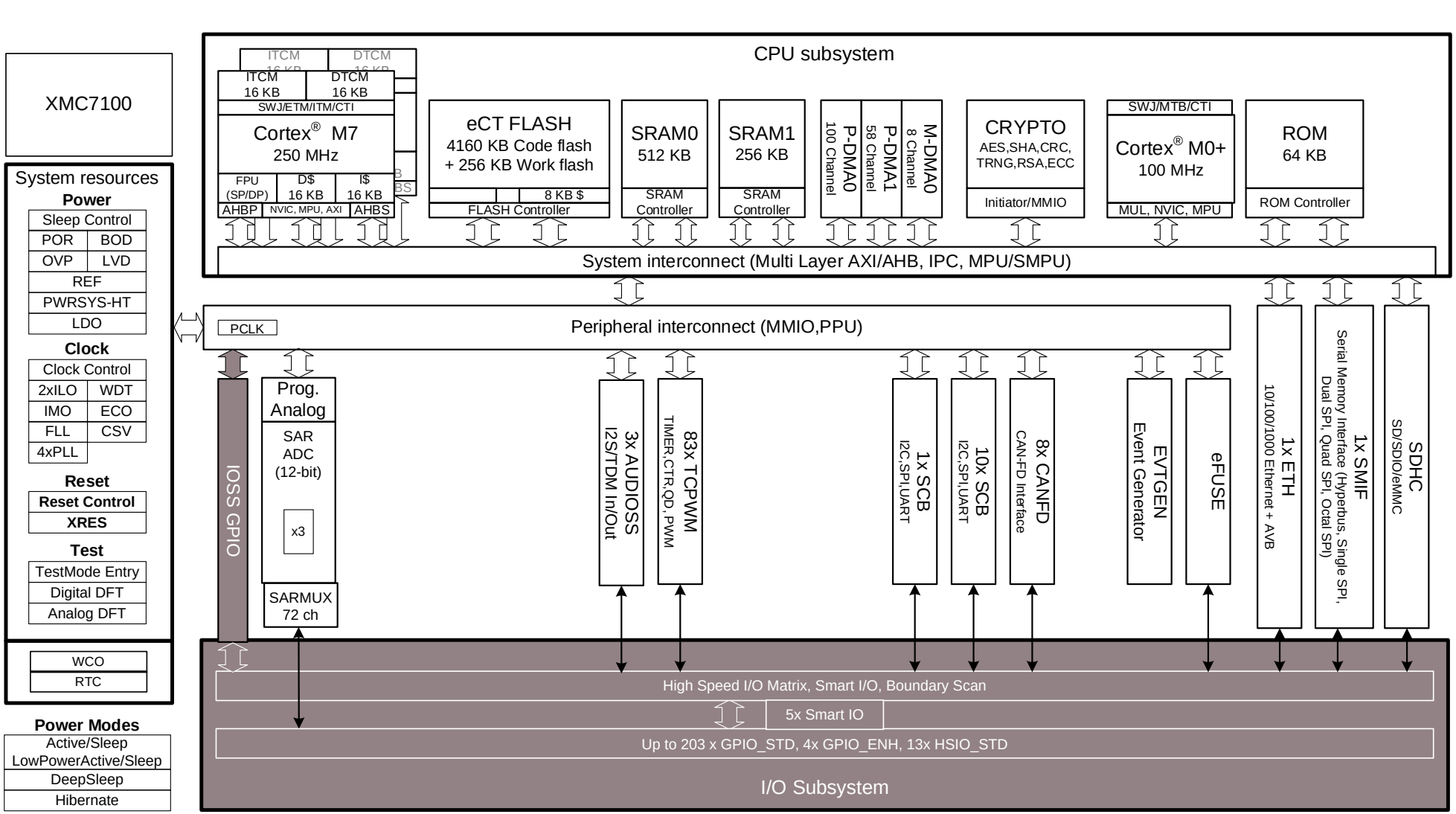



## Hint Bar

**Training section reference**

- **SAR ADC**
- **TCPWM (Timer/Counter/Pulse-Width Modulator)**
- **Serial Communication Blocks (SCB)**
- **Local Interconnect Network (LIN)**
- **CAN FD**
- **Event Generator**
- **CXPI**

# XMC7100 architecture diagrams:
# I/O subsystem




## Hint Bar

**Training section reference**

**- I/O Subsystem**

# Appendix

## Comparison between XMC7200 and XMC7100

# Feature comparison between XMC7200/XMC7100(1/4)

| Features | | XMC7200-8M | XMC7100-4M |
|---|---|---|---|
| CPU subsystem | Main CPU | One or Two Cortex-M7 CPUs and a 32 bit Arm Cortex M0+ CPU | |
| | Frequency | 350Mhz | 250Mhz |
| | FPU | Single(32bit)/double(64 bit)-precision | |
| | Cache | 16 KB instruction, 16 KB data | |
| | MPU | Same | |
| | System Tick Timer | Same | |
| Inter-processor communication (IPC) | | Same | |
| Protection unit | | Same | |
| Direct memory access | | Same | |
| Flash | Bus interface | AXI, AHB-Lite | |
| | ECC (SEC/DED) | Same | |
| | Bank modes | Same | |
| SRAM interface | Bus interface | AXI, AHB-Lite | |
| | ECC (SEC/DED) | Same | |
| | TCM | 16 KB ITCM, 16 KB DTCM | |
| Boot | | Same | |
| Interrupts | | Same | |
| Device security with Crypto | | Same | |
| Chip operational modes | | Same | |
| Fault subsystem | | Same | |

# Feature comparison between XMC7200/XMC7100 (2/4)

| Features | | XMC7200-8M | XMC7100-4M |
|---|---|---|---|
| Power supply and monitoring | Power supply | $V_{DDD}$ = 2.7 V to 5.5 V (up to 300 mA by internal regulator)<br>$V_{DDD}$ = 2.7 V to 5.5 V and $V_{CCD}$ = 1.15 V (exceeds 300 mA) | |
| | 5.0 V I/O power supply | $V_{DDIO_1}$, $V_{DDIO_2}$ | |
| | 3.3 V I/O power supply | $V_{DDIO_3}$, $V_{DDIO_4}$ | $V_{DDIO_3}$ |
| | 1.8 V I/O power supply | N/A | |
| | Analog power supply | $V_{DDA}$ (2.7V-5.5V) | |
| | Active/DeepSleep regulator | Same | |
| | External transistor control | Available | |
| | External PMIC control | Available | |
| | BOD/OVD/LVD | Same | |
| Device power modes | | Same | |
| Clock system | Internal clock sources (IMO, ECO) | Same (operates at 8 MHz ±1%) | |
| | External clock sources (ECO, WCO, EXT_CLK) | Same | |
| | FLL | Same | |
| | PLL without SSCG and fractional operation | Same | |
| | PLL with SSCG and fractional operation | Available | |
| | Clock supervision (CSV) | Same | |
| | Clock calibration counter | Same | |
| Reset system | | Same | |

# Feature comparison between XMC7200/XMC7100 (3/4)

| Features | | XMC7200-8M | XMC7100-4M |
|---|---|---|---|
| Watchdog timer | | Same | |
| Real time clock | | Same | |
| I/O system | GPIO input modes (CMOS/TTL/Industrial) | Same | |
| | Eight output drive modes | Same | |
| | Drive strength (Full, 1/2, 1/4) | Same | |
| | Slew rate control (only for GPIO_ENH) | Same | |
| | GPIO interrupt | Same | |
| | Smart I/O | Same | |
| | High-speed I/O | HSIO_STD - 29 | HSIO_STD - 13 |
| CAN FD | | 10 Ch | 8 Ch |
| Serial communications block | | Same | |
| TCPWM | | 118 Ch | 83 Ch |
| SAR ADC | | 96 Ch | 72 Ch |
| Event generator | | Same | |
| Trigger multiplexer | | Same | |
| Serial memory interface | | Same | |
| Ethernet MAC | | 2 Ch (10/100/1000) | 1Ch (10/100) |

# Feature comparison between XMC7200/XMC7100 (4/4)

| Features | XMC7200-8M | XMC7100-4M |
|---|---|---|
| SDHC host controller | Available | |
| Audio subsystem | Available | |
| Flash security ( Program /work read protection) | Same | |
| Debug trace | Same | |
| Program and debug interface | Same | |
| Nonvolatile memory programming | Same | |
| Packages | 176-TEQFP/ 272-BGA | 100-TEQFP /144-TEQFP /176-TEQFP/ 272-BGA |

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# Revision History

| Revision | ECN | Submission Date | Description of Change |
|---|---|---|---|
| ** | 7728864 | 2022-03-16 | Initial release |