

XMC7000 Event generator

Customer training workshop (CTW)

January 2026

public

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Target products

Target product list for this training material:

Family category	Series	Code flash memory size
XMC7200	XMC7200-8M	Up to 8384 KB
XMC7100	XMC7100-4M	Up to 4160 KB

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XMC7200 - 8M family



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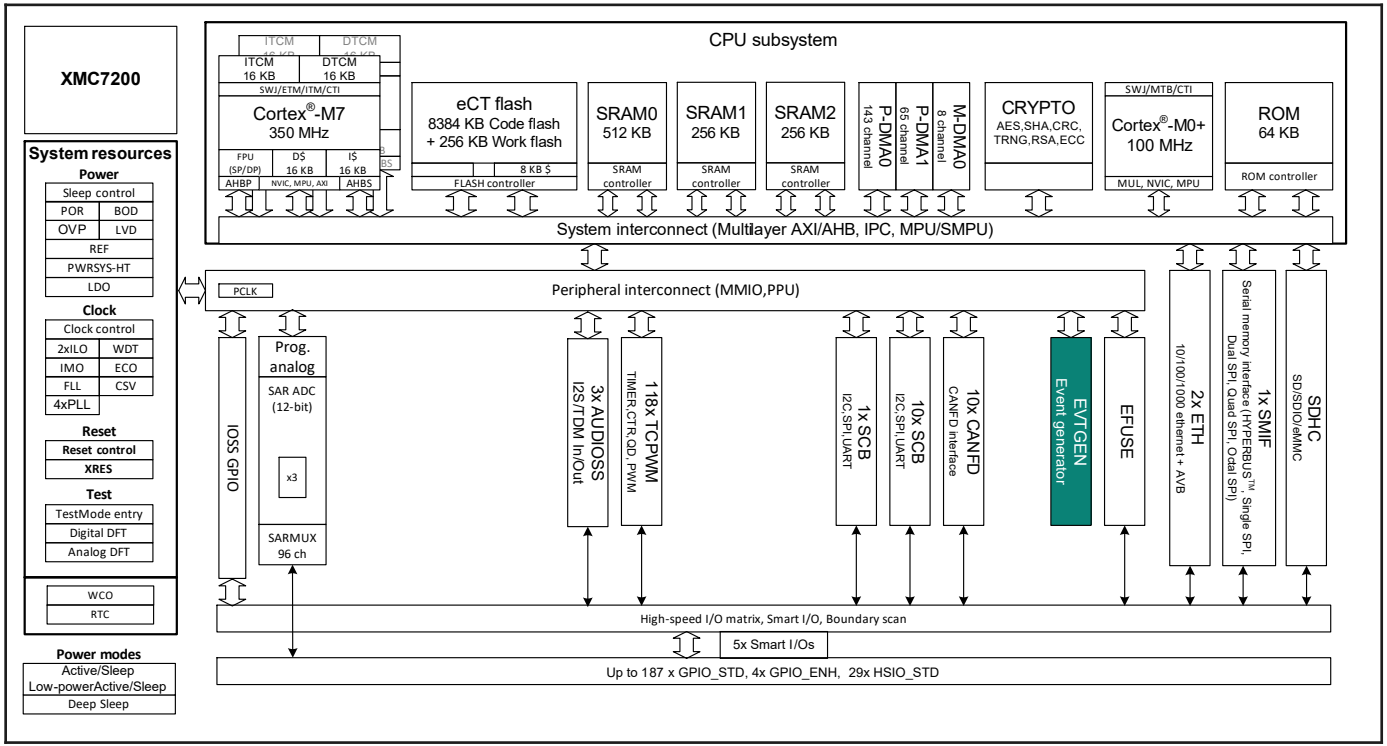
Introduction to XMC7200 – 8M

The event generator (EVTGEN) is a part of the peripheral blocks.



Hint bar

See the architecture reference manual Event generator (chapter 27) for additional details.

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XMC7100 - 4M family



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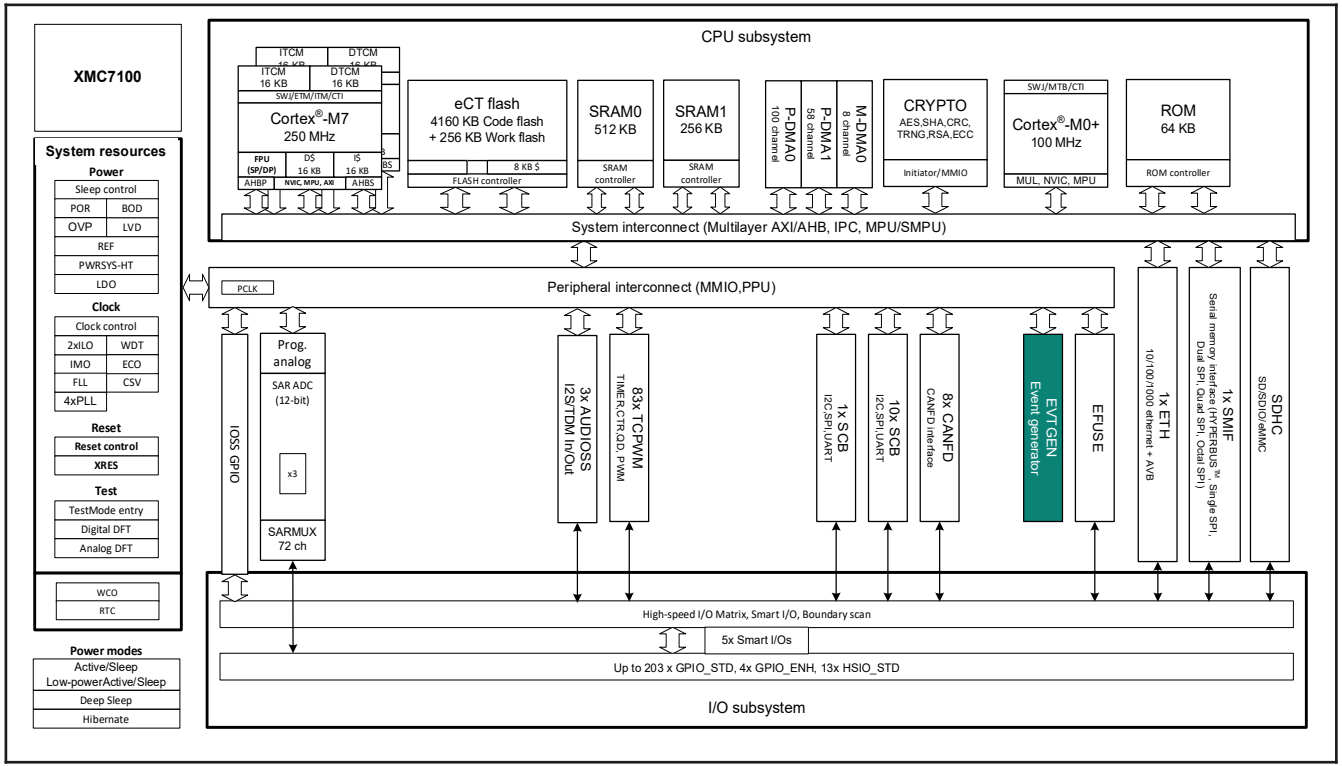
Introduction to XMC7100 – 4M

The event generator (EVTGEN) is a part of the peripheral blocks.



Hint bar

See the architecture reference manual Event generator (chapter 27) for additional details.

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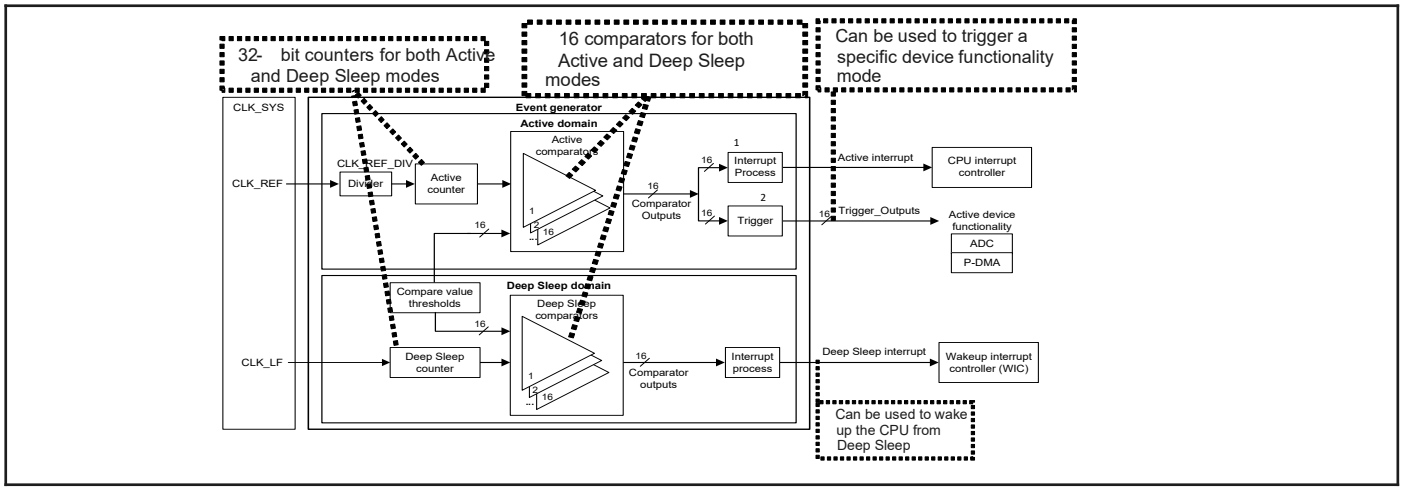
Overview

32-bit counters, one each for Deep Sleep and Active power modes.

Interval range

- 30 ns to 76 hours (Active mode)
- 31 µs to 36 hours (Deep Sleep mode)

Generates interrupts or triggers



[1] This interrupt can be used like a normal interval timer.
[2] This trigger activates ADC.

Hint bar

- See the architecture reference manual, Event generator (chapter 27) for additional details
- See the trigger multiplexer training section for additional trigger details
- See the Interrupt training section for additional interrupt details

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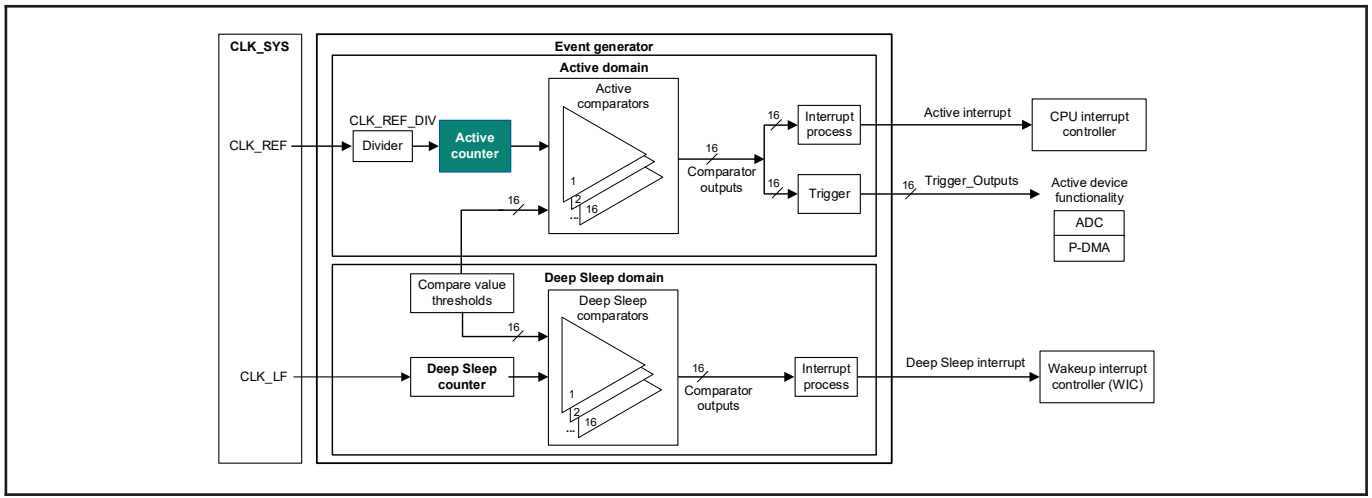
Counters

Active counter

- Works on the divided CLK_REF_DIV[1] (IMO[2] or ECO[3])
- Restarts from ‘0’ after overflow
- Enables read by software in Active mode
- Not retained in Deep Sleep power mode



[1] Reference clock (IMO or ECO)
[2] IMO: Internal main oscillator
[3] ECO: External crystal oscillator

Hint bar

- See the architecture reference manual Event generator (chapter 27.2.2) for additional details
- See the Clock training section for additional clock details
- See the datasheet for each clock frequency

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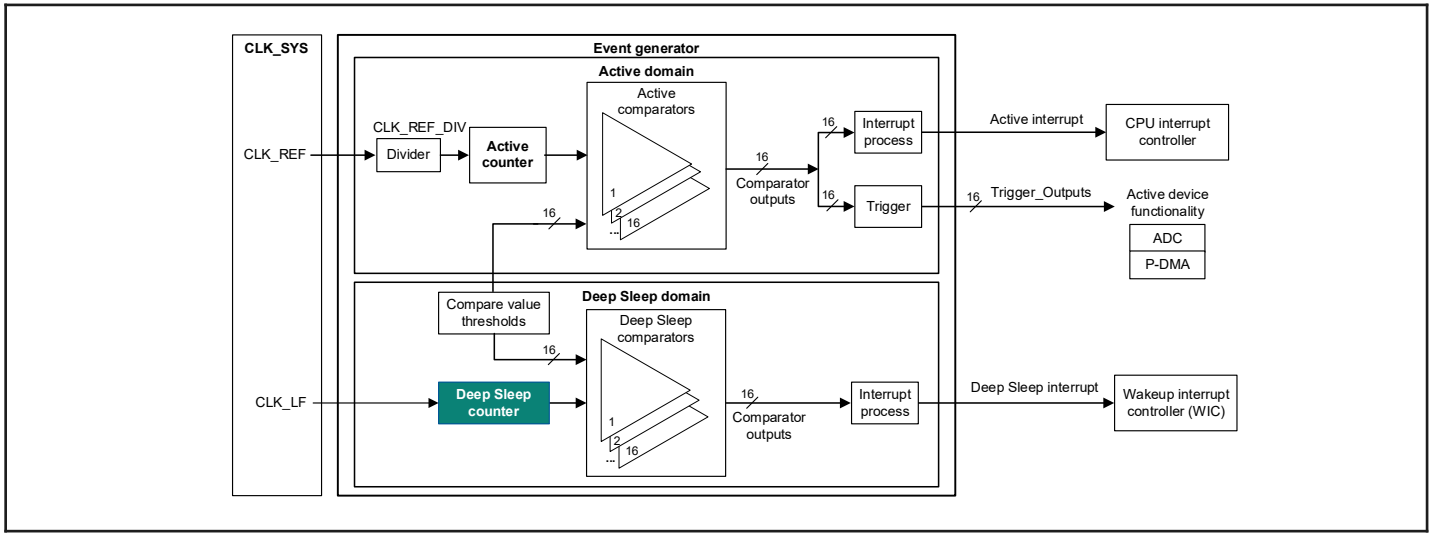
Counters (contd.)

Deep Sleep counter

- Works on the CLK_LF[4] (ILO[5] or WCO[6])
- Cannot be read by software in Active or Deep Sleep mode



Hint bar

- See the architecture reference manual Event generator (chapter 27.2.2) for additional details
- See the clock training section for additional clock details
- See the datasheet for each clock frequency

[4] Low-frequency clock (ILO or WCO)
[5] ILO: Internal low-speed oscillator
[6] WCO: Watch crystal oscillator

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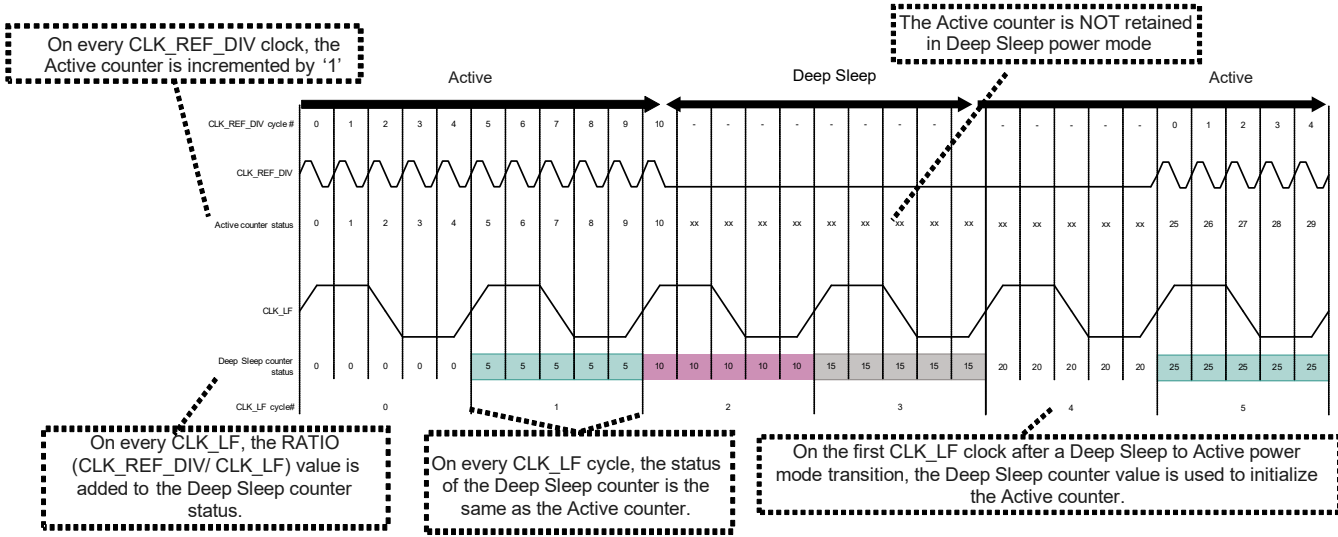
Relation of Active and Deep Sleep counter

Active and Deep Sleep counter status with RATIO = 5 (CLK_REF_DIV is 5 times as fast as CLK_LF)

– Active and Deep Sleep counters are always in sync



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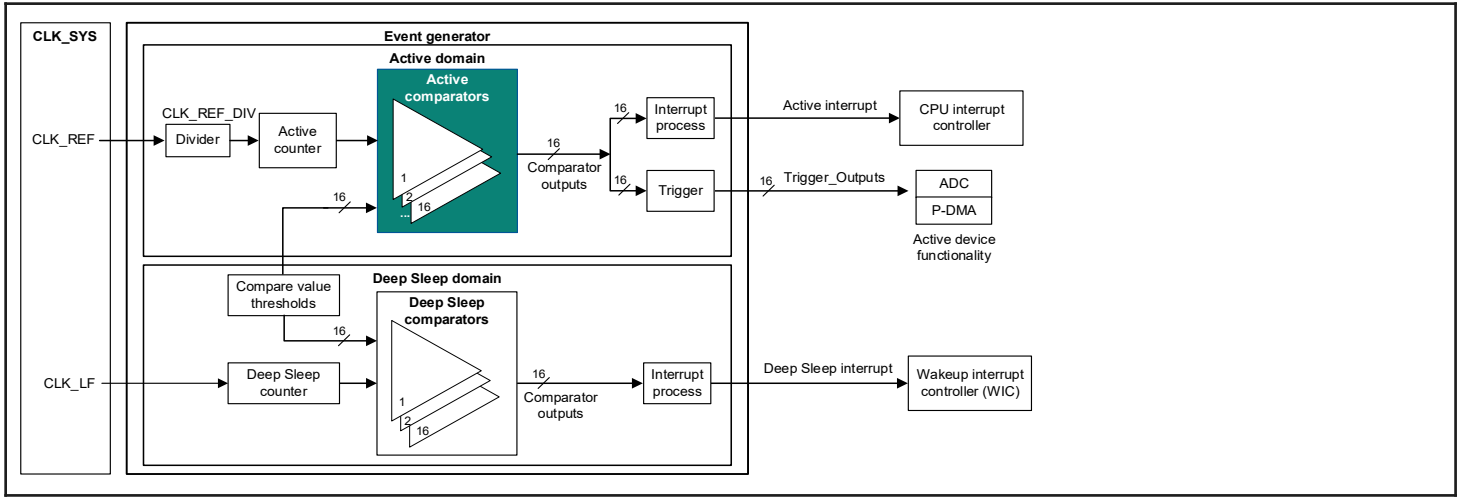
Comparators

Active comparators

- 16 (maximum): COMP0 [31:0]
  - 30 ns (minimum); ECO: 33.34 MHz
  - 76 hours (minimum); ECO: 4 MHz/256[1]
- Compares to Active counter
- Generates triggers and interrupts



[1] CLK_REF_DIV range is 1 to 256

Hint bar

- See the register reference manual Event generator (chapter 27.2.4) for additional details
- See the datasheet for each clock frequency

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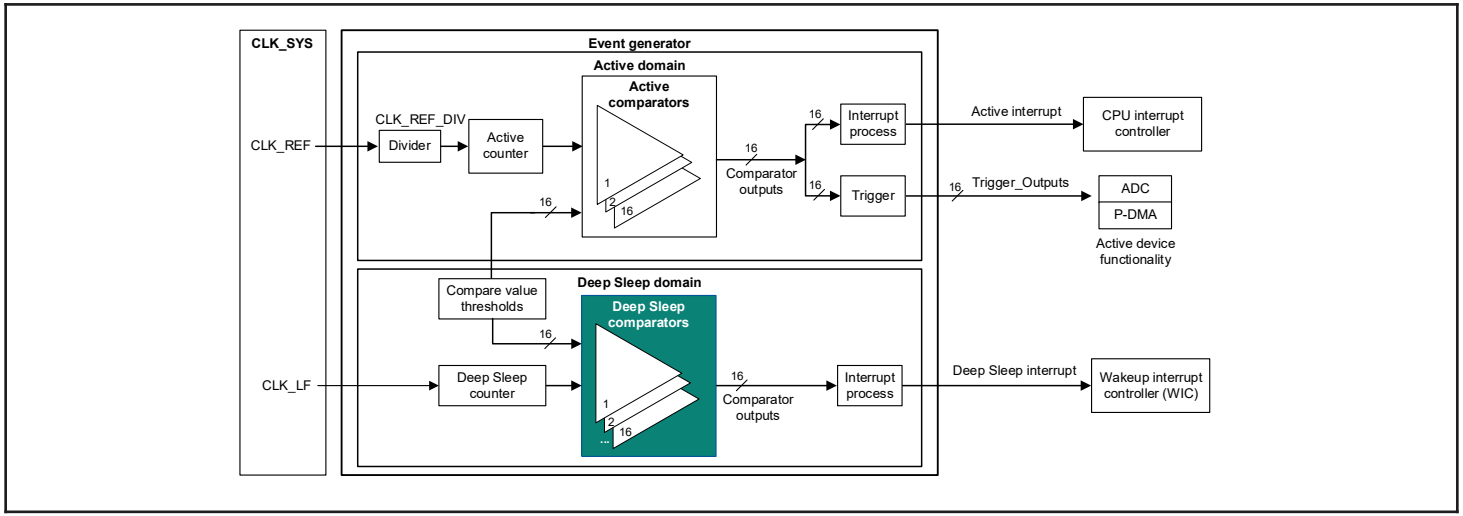
Comparators (contd.)

Deep Sleep comparators

- 16 (maximum): COMP1 [31:0]
  - 31 µs (minimum); ILO: 32.768 kHz
  - 36 hours (maximum); ILO: 32.768 kHz
- Compares to the Deep Sleep counter
- Generates a wakeup interrupt



[1] CLK_REF_DIV range is 1 to 256.

Hint bar

- See the register reference manual Event generator (chapter 27.2.4.5) for additional details
- See the datasheet for each clock frequency

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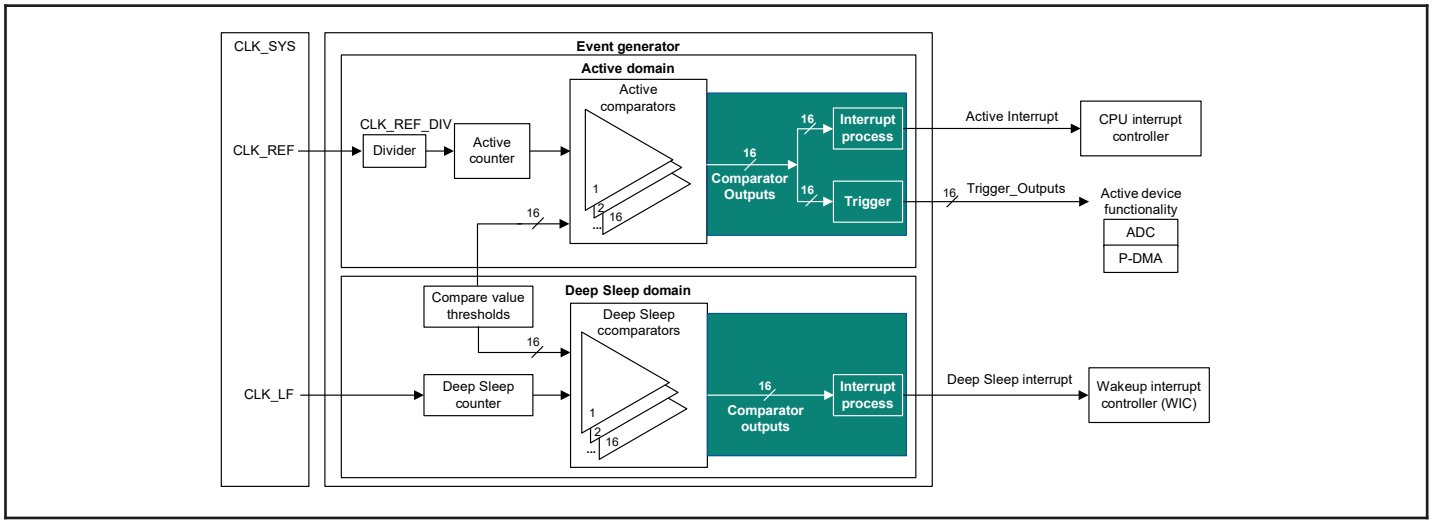
Comparator outputs

Interrupts

- An Active interrupt is generated when the Active counter is ≥ COMP0
  - Use case: Periodic waveform
- Deep Sleep interrupt occurs when the Deep Sleep counter is ≥ COMP1
  - Use Case: Wake up from Deep Sleep mode



Hint bar

- See the reference manual section Event generator (chapter 27.2.5) and Comparator structures / 27.2.6 Interrupts for additional details
- See the trigger multiplexer training section for additional trigger details

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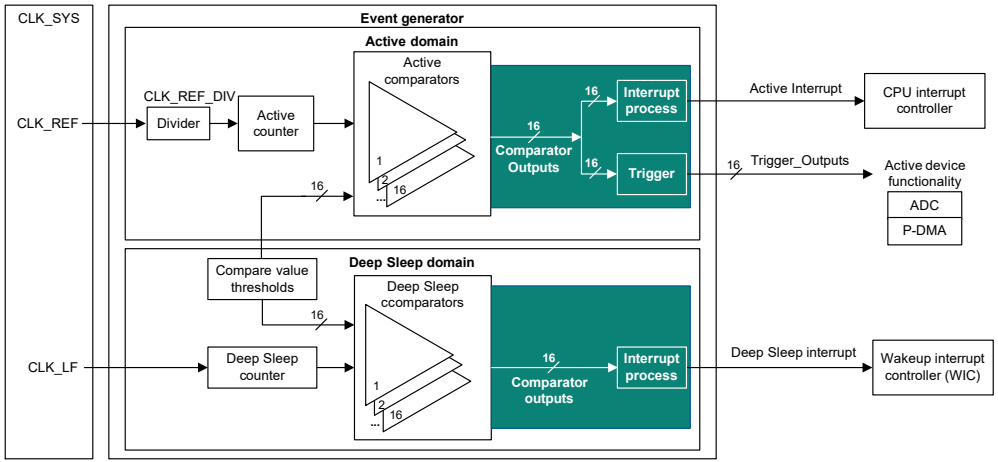
Comparator outputs (contd.)

Trigger

- Available only in Active power mode
- Generated when the Active counter is ≥ COMP0
  - Use case: Periodic task management



Hint bar

- See the reference manual Event generator (chapter 27.2.5) and Comparator structures / 27.2.6 Interrupts for additional details
- See the trigger multiplexer training section for additional trigger details

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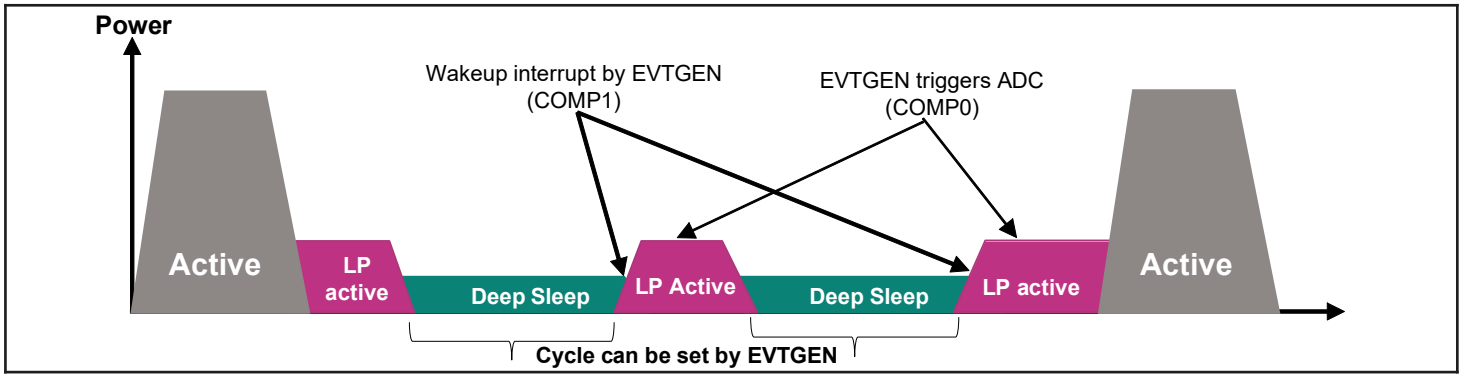
Cyclic wakeup operation

- Enables periodic ADC sensing with low power
- Periodic wakeup from Deep Sleep mode by using the Deep Sleep comparator (using COMP1)
- After Cortex®-M0+ or Cortex®-M7 wakes up (in LP Active mode), EVTGEN can generate a trigger for ADC (using COMP0)



Use case

- Cyclic touch detection on the switch module of the control unit
- Cyclic sensor sensing

Hint bar

- See the reference manual Event generator (chapter 27.2.6 / 27.2.6) and Interrupts for additional details
- See the power modes training section for additional low-power details
- See the trigger multiplexer training section for additional trigger details
- See the Cyclic Wakeup Sequence for Sensing by ADC section for additional cyclic wakeup sequence details

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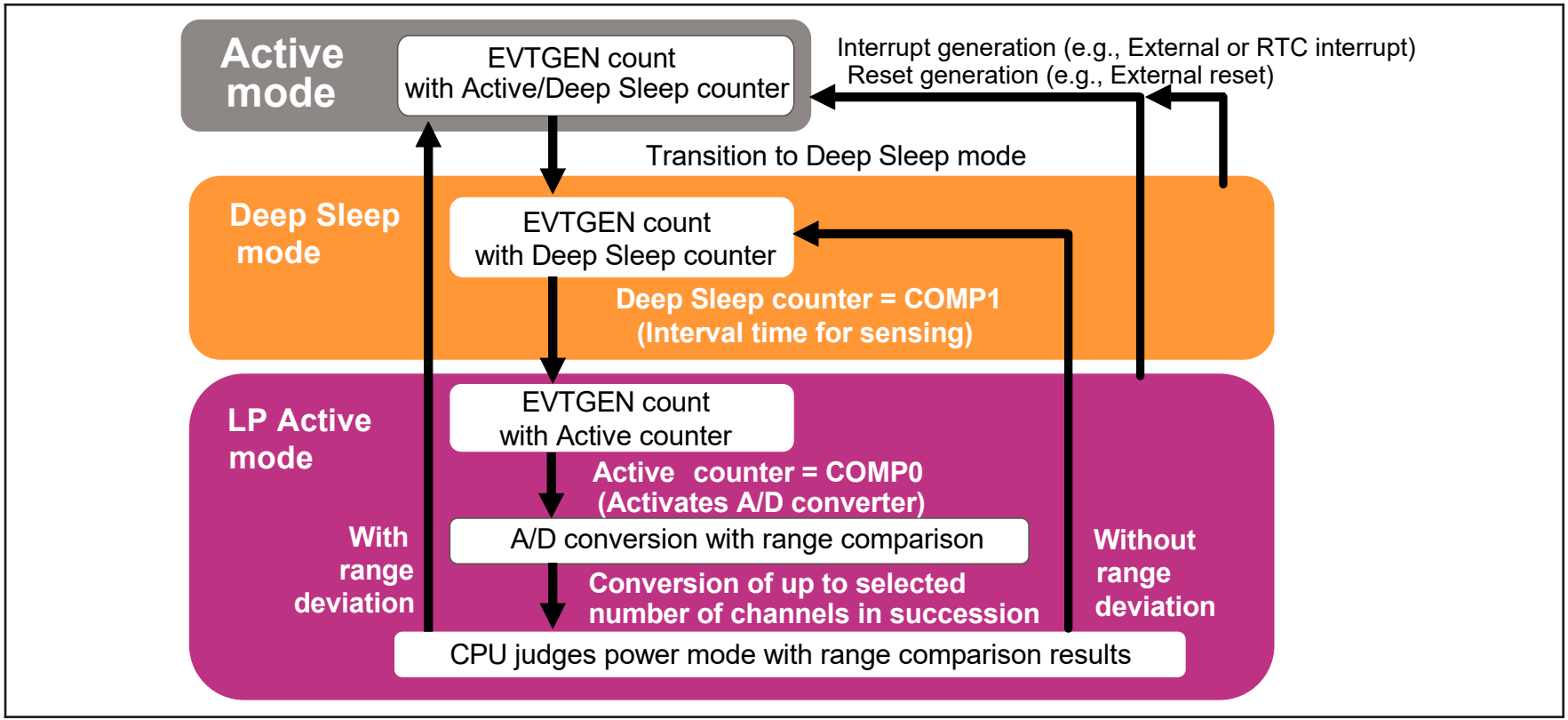
Cyclic wakeup sequence for sensing by ADC



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9 **Revision history** **26**

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Revision history

Document revision	Date	Description of change
**	2022-09-05	Initial release.
*A	2026-01-05	Migrated to the latest empower training presentation template.

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