

XMC7000 Ethernet MAC

Customer training workshop (CTW)

March 2026

Public

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Target products

Target product list for this training material:

Family category	Series	Code flash memory size
XMC7200	XMC7200 - 8M	Up to 8384 KB
XMC7100	XMC7100 - 4M	Up to 4160 KB

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XMC7200 - 8M family



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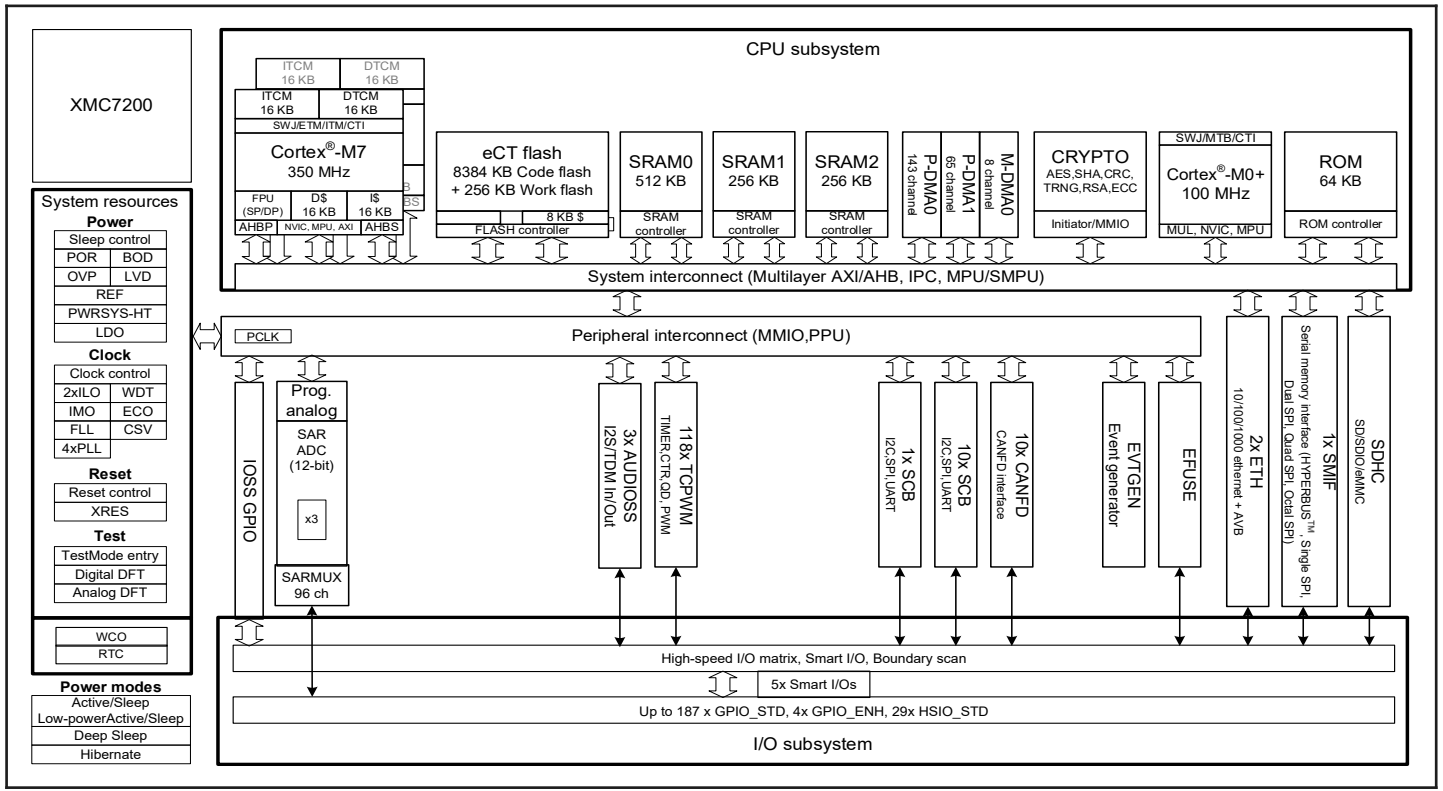
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Introduction to XMC7200 – 8M

– Ethernet MAC is located in the peripheral blocks



Hint bar

See the architecture reference manual, Ethernet MAC (section 29), for additional details.

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XMC7100 - 4M family



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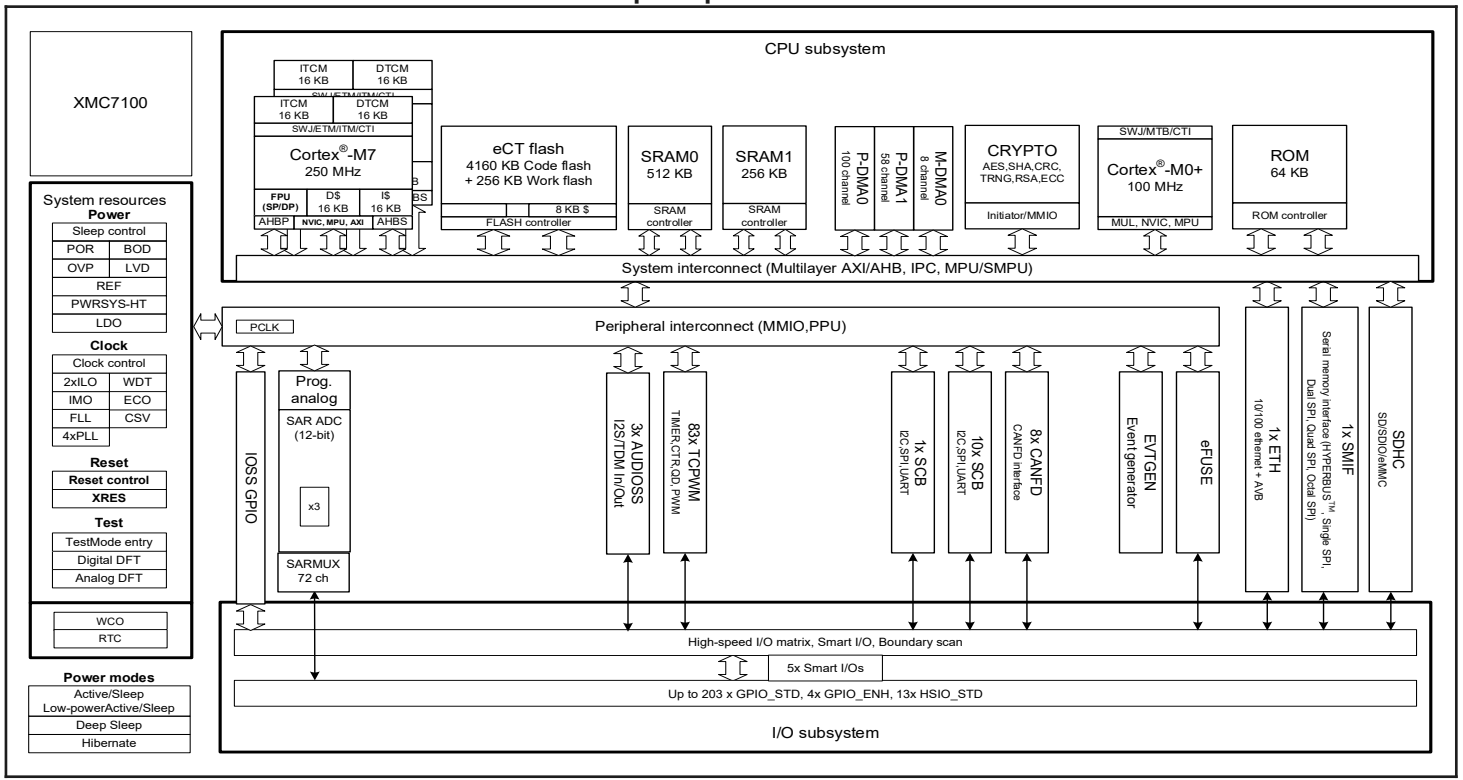
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Introduction to XMC7100 – 4M

– Ethernet MAC is located in the peripheral blocks



Hint bar

See the architecture reference manual, Ethernet MAC (section 29), for additional details.

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Ethernet MAC

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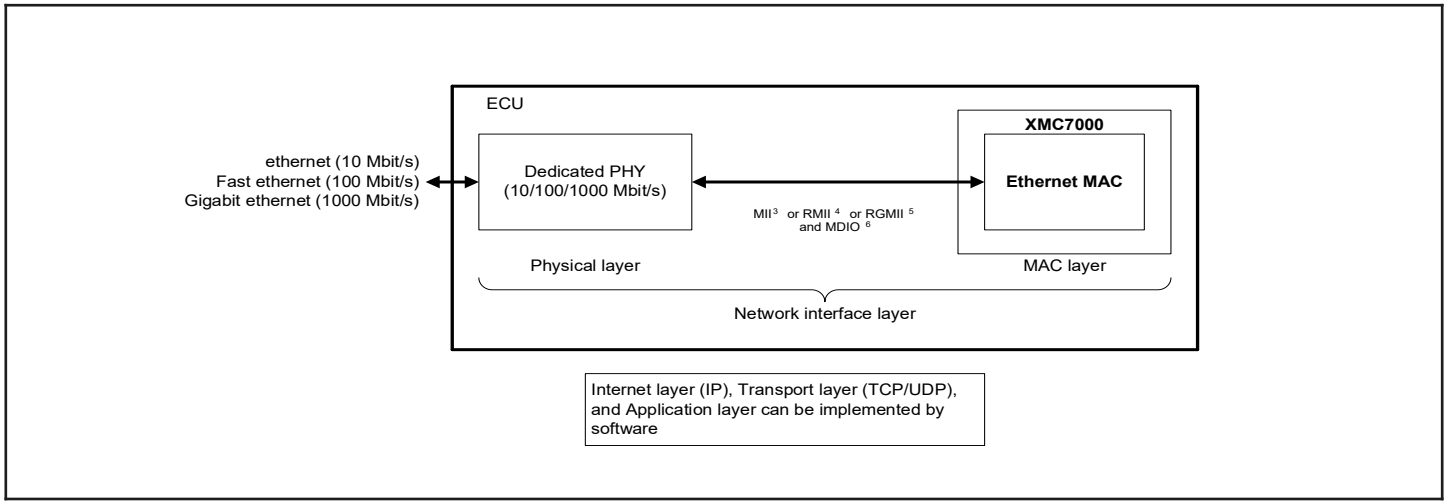
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Overview

– The Ethernet MAC[1] module transmits and receives IEEE 802.3 frames by connecting with the PHY[2] device



[1] MAC: Media access control.
[2] PHY: Physical layer.
[3] MII: Media independent interface.
[4] RMII: Reduced media independent interface.
RMII is the standard for reducing the number of signals needed to connect the PHY to the MAC compared to MII.
[5] RGMII: Reduced gigabit media independent interface. Only supported by XMC7200.
RGMII is the standard for reducing the number of signals needed to connect the PHY to the MAC compared to GMII.
[6] MDIO: Management data Input/Output.

Hint bar

– See the architecture reference manual, overview (section 29.1), for additional details

– See the device-specific datasheet to confirm which PHY interfaces are supported in the device

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Features

- MII, RMII, and RGMII PHY interface
- MDIO interface for PHY management
- XMC7200: 10/100/1000 Mbps Ethernet MAC compatible with IEEE 802.3
- XMC7100: 10/100 Mbps Ethernet MAC compatible with IEEE 802.3
- Full-duplex
- Jumbo frame[1] (Max 1536 bytes)
- IEEE 802.1Q: Virtual LAN (VLAN)
- IEEE 802.3: Pause frame
- IEEE 802.1Qav: Forwarding and queuing enhancements for time-sensitive streams
- IEEE Std 802.1Qbb: Priority based flow control
- IEEE 802.1AS: Timing and synchronization for time-sensitive applications in bridged LANs
- IEEE 1588: Precision time protocol

Hint bar

- See the architecture reference manual, overview (section 29.1), for additional details
- See the device-specific datasheet to confirm which PHY interfaces are supported in the device

[1] Jumbo frame is not standardized by IEEE.

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Components

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Components (1/24)

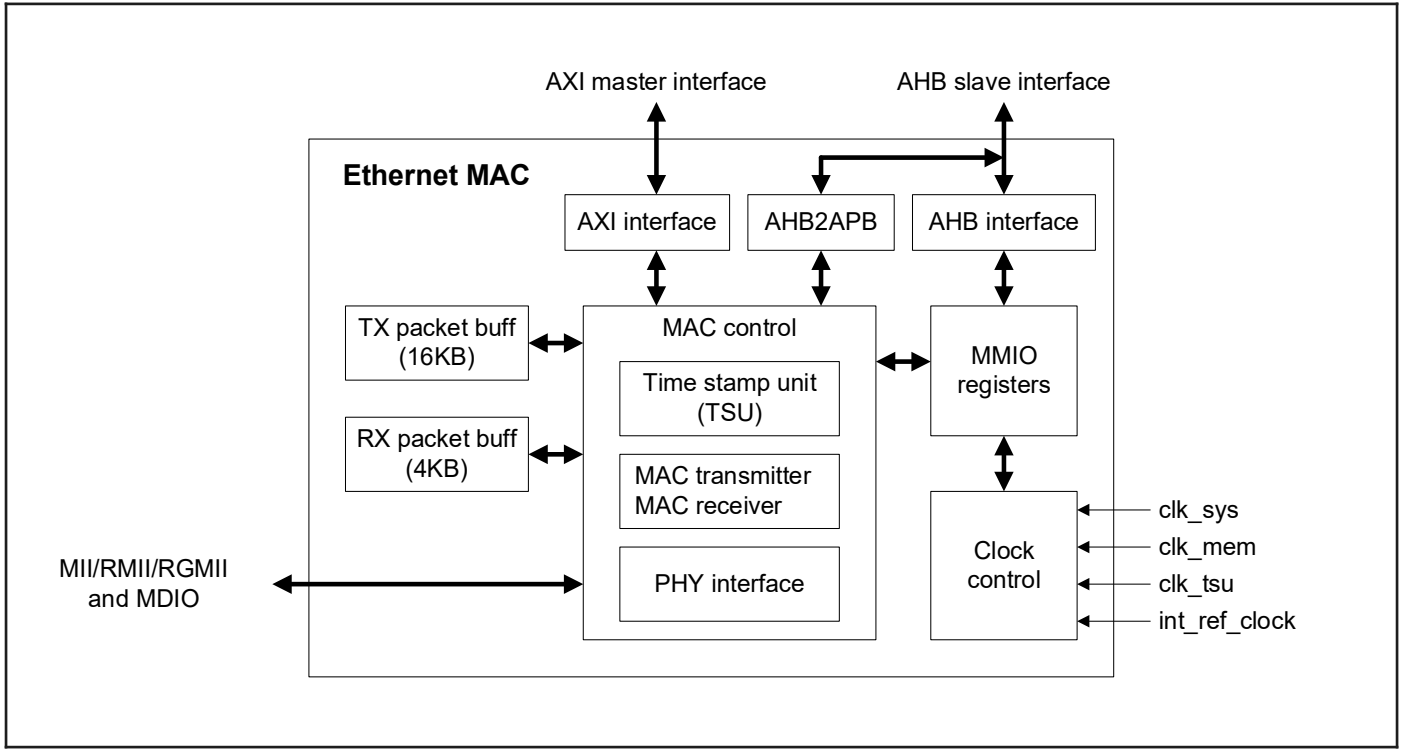
- MAC control
  - PHY interface
  - MAC transmitter/receiver
  - Time stamp unit
- TX/RX packet memory
- CLK control

Hint bar

- See the architecture reference manual, block diagram (section 29.2), for additional details
- See the features list in the datasheet for additional details
- See the device-specific datasheet to confirm which PHY interfaces are supported in the device

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Components (2/24)



Hint bar

- See the architecture reference manual, block diagram (section 29.2), for additional details
- See the features List in the datasheet for additional details
- See the device-specific datasheet to confirm which PHY interfaces are supported in the device

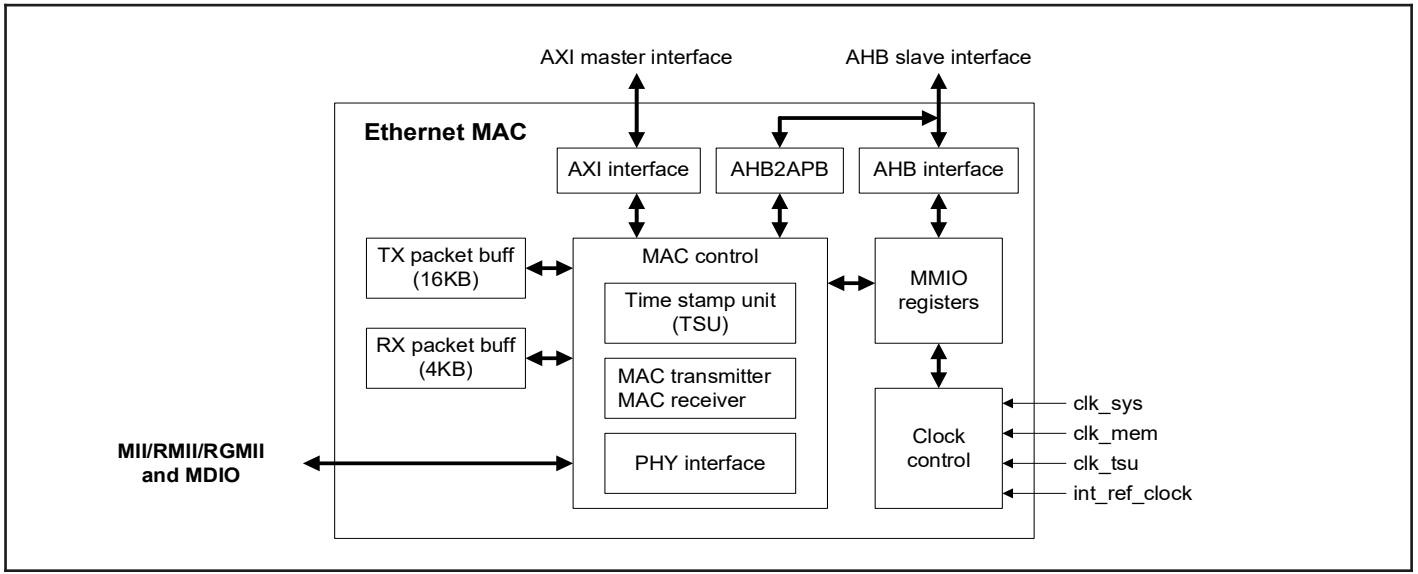
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Components (3/24)

PHY interface

– Supports MII/RMII/RGMII[1] PHY interface

– Supports MDIO interface



[1] Only supported by XMC7200.

Hint bar

– See the architecture reference manual, media independent interfaces (section 29.3.14), for additional details

– See the device-specific datasheet to confirm which PHY interfaces are supported in the device

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Components (4/24)

PHY interface types

– Supports the following interface types and transfer rates

Interface type	Transfer rate		
	10 Mbps	100 Mbps	1000 Mbps
MII	✓	✓	–
RMII	✓	✓	–
RGMII	✓	✓	✓

Hint bar

– See the architecture reference manual, RMII (section 29.3.14.3), for additional details

– See the device-specific datasheet to confirm which PHY interfaces are supported in the device

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Components (5/24)

MII/RMII/RGMII interface

– Supported signals: Transmitter/Receiver signals

Pin name	Function of signals	MII	RMII	RGMII
TXD[1:0]	Transmit data [1:0]	✓	✓	✓
TXD[3:2]	Transmit data [3:2]	✓	–	✓
TXD[7:4]	Transmit data [7:4]	–	–	–
TX_CTL	Transmit enable	✓	✓	✓
TX_ER	Transmit error	✓	–	–
TX_CLK	Transmit clock	✓	✓	✓
RXD[1:0]	Receive data [1:0]	✓	✓	✓
RXD[3:2]	Receive data [3:2]	✓	–	✓
RXD[7:4]	Receive data [7:4]	–	–	–
RX_CTL	Receive data valid	✓	✓	✓
RX_ER	Receive error	✓	✓	–
RX_CLK	Receive clock	✓	–	✓
REF_CLK	Operation clock out	–	✓	✓
–	Operation clock in	–	✓	✓

Hint bar

– See the architecture reference manual, media independent interfaces (section 29.3.14), for additional details

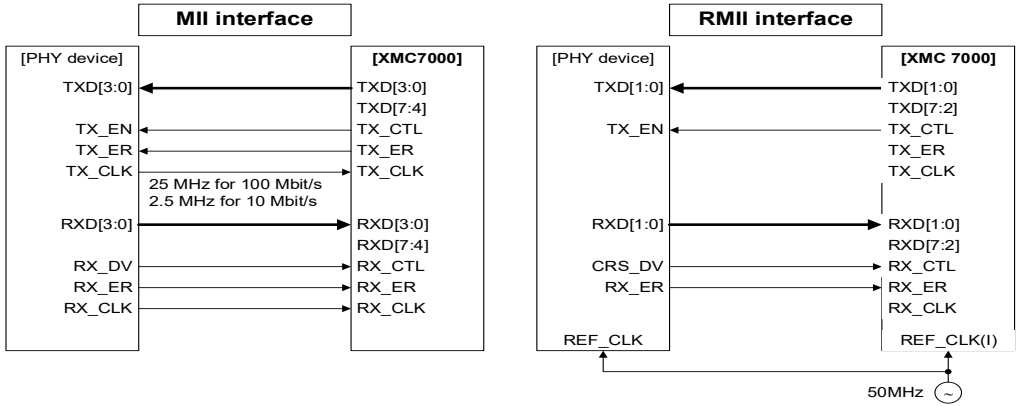
– See the package pin list and alternate functions in the datasheet for additional details

– See the device-specific datasheet to confirm which PHY interfaces are supported in the device

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Components (6/24)

Use Case: MII/RMII interface



TX and RX clocks are supplied from external PHY

TX and RX clock sources can be supplied from either the internal reference clock or the external clock source

ETH_CTRL register must be used to select the reference clock source from the internal reference clock or from HSIO

Hint bar

- See the architecture reference manual, media independent interfaces (section 29.3.14), for additional details
- See the device-specific datasheet to confirm which PHY interfaces are supported in the device

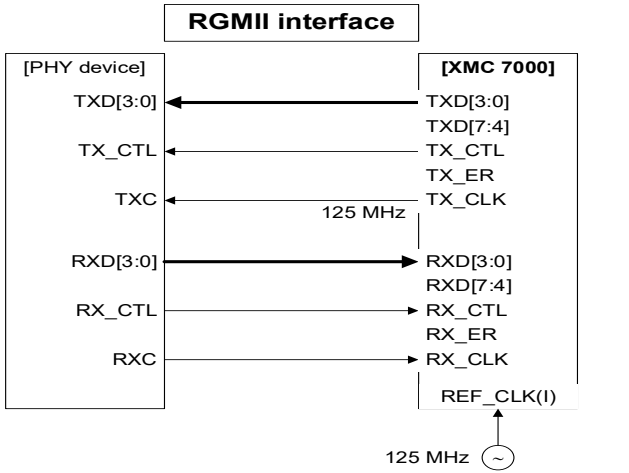
Register info

- ETH_CTRL(REFCLK_SRC_SEL)

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Components (7/24)

Use Case: MII/RMII interface



TX clock source can be selected either from the internal clock source or from HSIO

ETH_CTRL register must be used to select the reference clock source from the internal reference clock or from HSIO

Hint bar

- See the architecture reference manual, media independent interfaces (section 29.3.14), for additional details
- See the device-specific datasheet to confirm which PHY interfaces are supported in the device

Register info

- ETH_CTRL (REFCLK_SRC_SEL)

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Components (8/24)

MDIO interface

Supported signals:

Pin name	Direction	Function of signals
MDIO	I/O	Management data Input/Output
MDC	O	Management data clock

- MDIO is a single bi-directional tristate signal between Ethernet MAC and PHY
- MDC is a clock for MDIO
  - MDC is generated by dividing CLK_SYS
  - MDC should not toggle faster than 2.5 MHz (minimum period of 400 ns), as defined by the IEEE 802.3az

Hint bar

See the architecture reference manual, MDIO interface (section 29.3.12), for additional details.

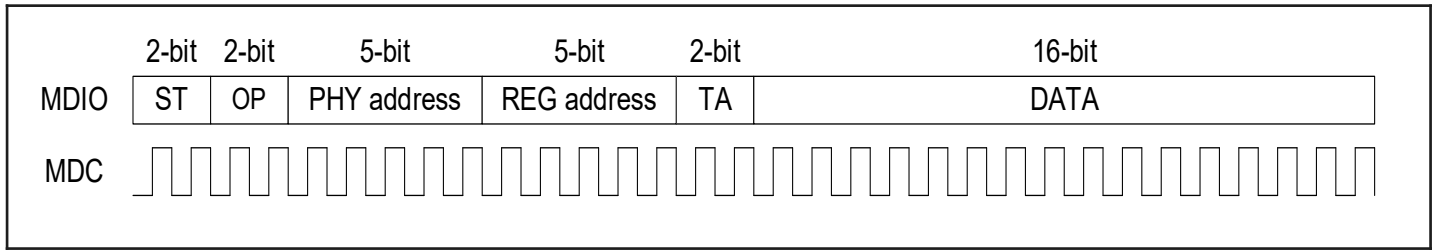
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Components (9/24)

MDIO interface

Use case:

- ETH_phy_management register is implemented as a shift register
- Writing to this register starts a shift operation and outputs to the MDIO pin



Hint bar

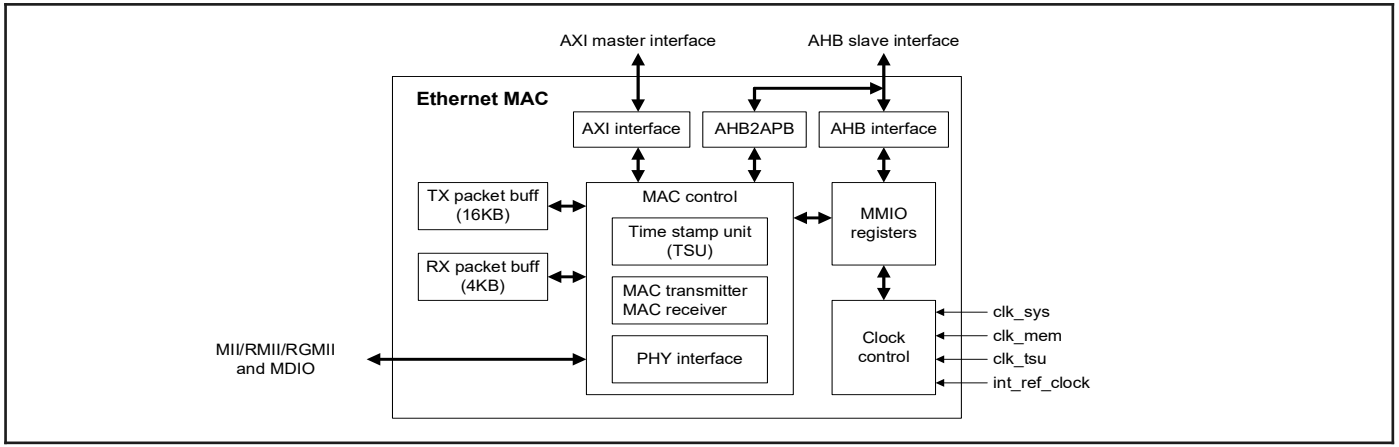
See the architecture reference manual, MDIO interface (section 29.3.12), for additional details.

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Components (10/24)

MAC transmitter/receiver, TSU, and packet buff

- MAC transmitter/receiver and TX/RX packet buff
  - Supports transfer of packets between physical layer and MAC layer, and stores data in the TX/RX packet buffer
- Time Stamp Unit (TSU)
  - Generates a time stamp for the transmit data and checks the time stamp for the receive data



Hint bar

See the architecture reference manual, transmit scheduling algorithm (section 29.3.2) and MAC receiver (section 29.3.4), for additional details.

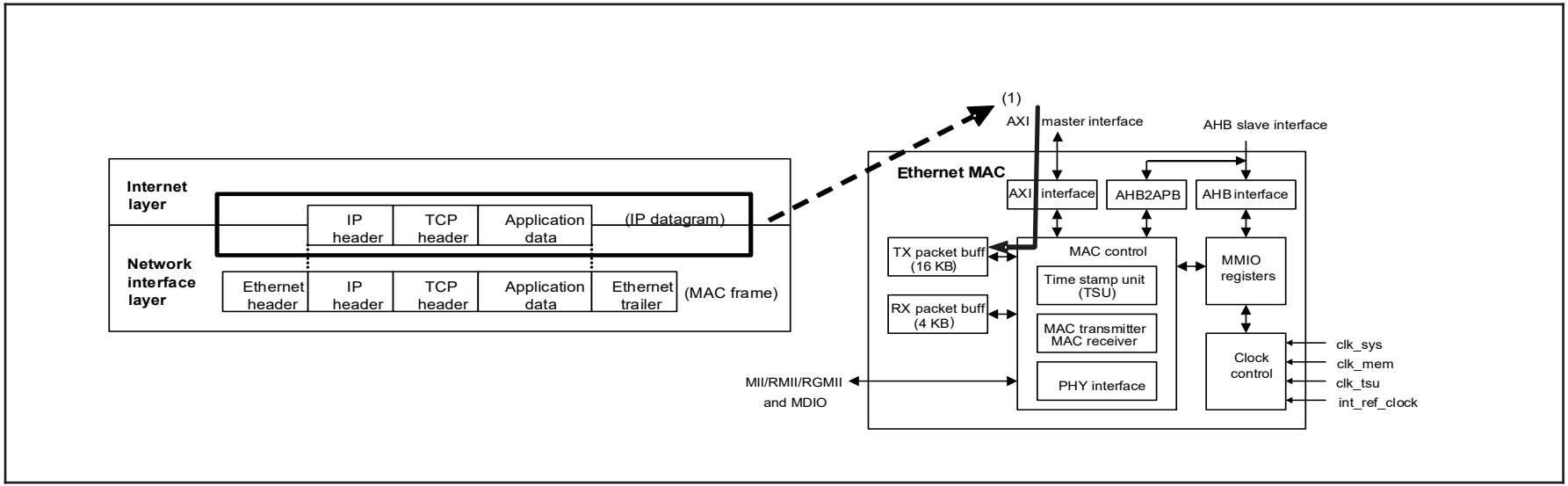
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Components (11/24)

MAC transmitter

Procedure:

1. IP datagrams are transferred to the TX packet memory via AXI[1]



[1] Support to DMA transfer. DMAC is implemented in the MAC control.

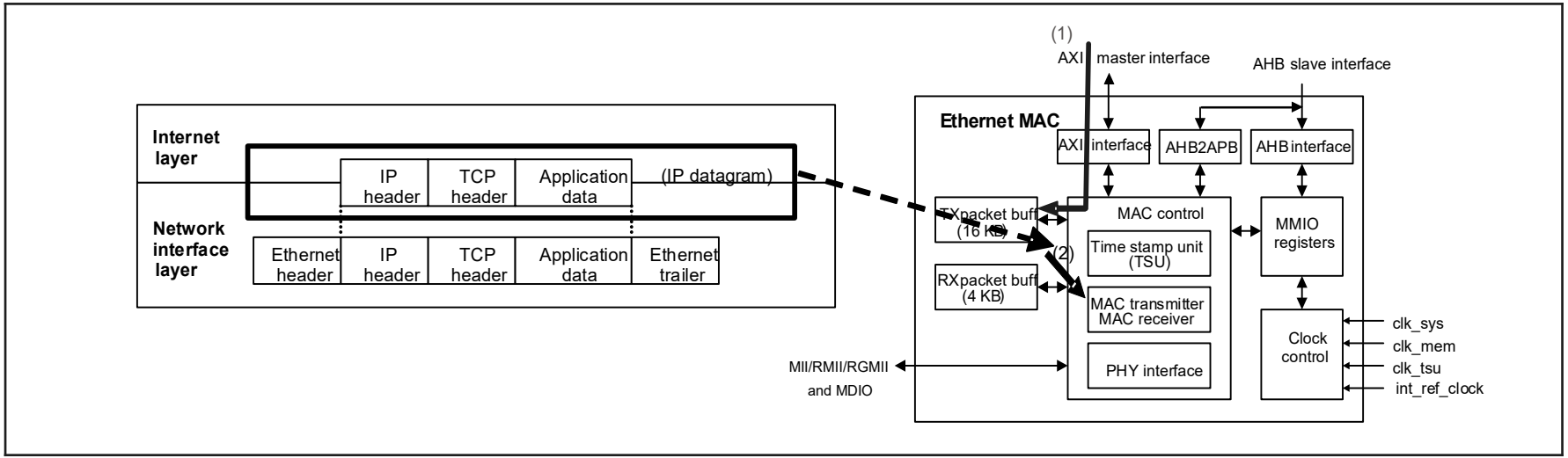
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Components (12/24)

MAC transmitter

Procedure:

1. IP datagrams are transferred to the TX packet memory via AXI[1]
2. IP datagram is transferred to the MAC transceiver[1]



[1] Support to DMA transfer. DMAC is implemented in the MAC control.

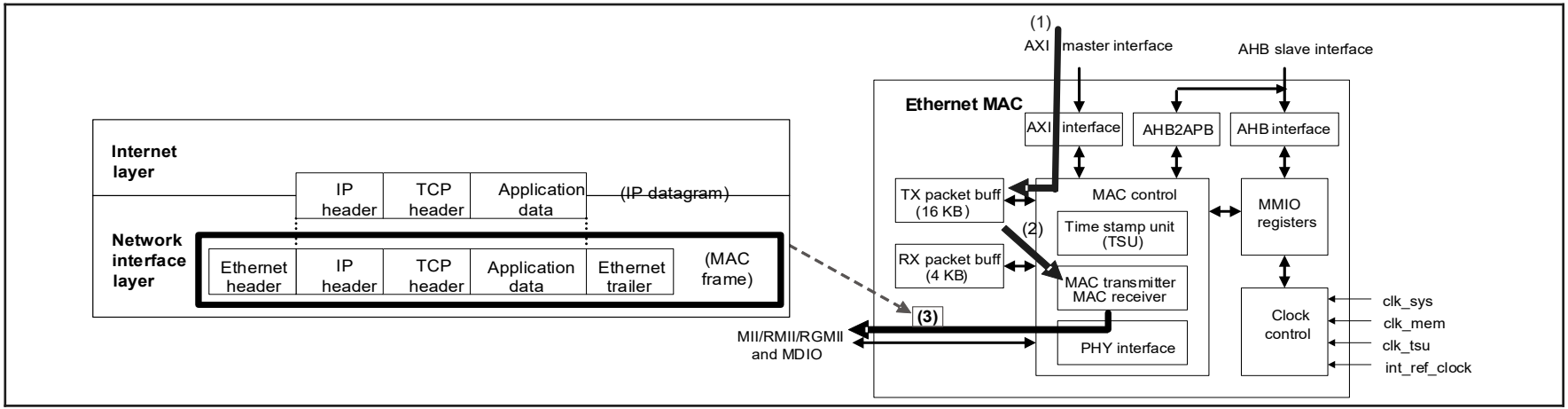
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Components (13/24)

MAC transmitter

Procedure:

1. IP datagrams are transferred to the TX packet memory via AXI[1]
2. IP datagram is transferred to the MAC transceiver[1]
3. MAC frame is multiplexed and transmitted by the hardware



[1] Support to DMA transfer. DMAC is implemented in the MAC control.

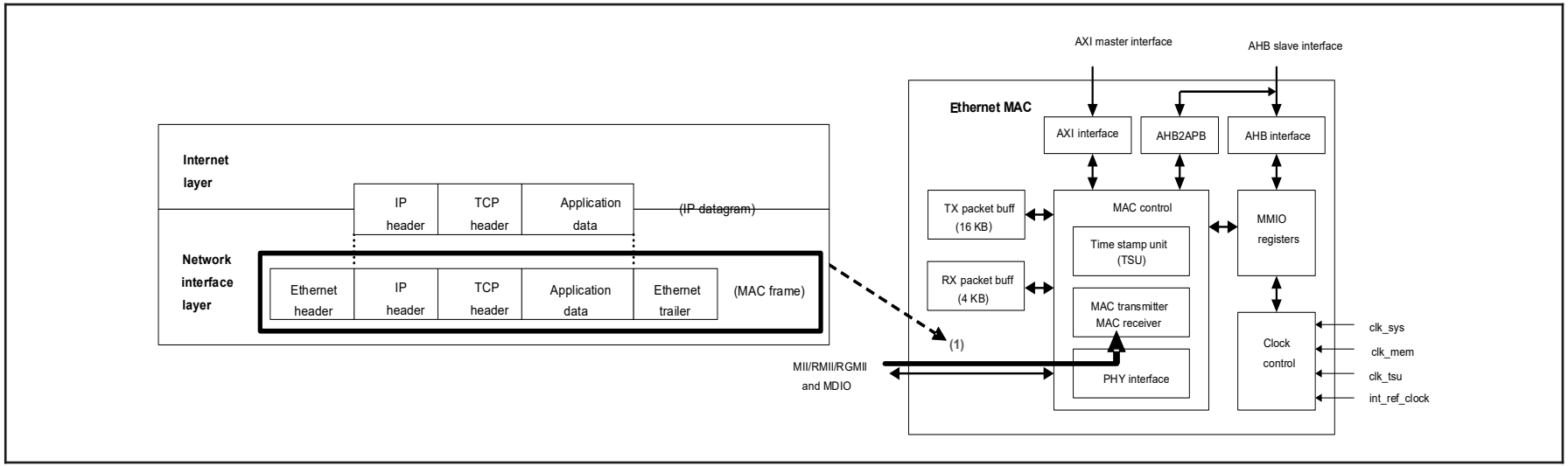
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Components (14/24)

MAC receiver

Procedure:

1. MAC frame is checked and demultiplexed by the hardware



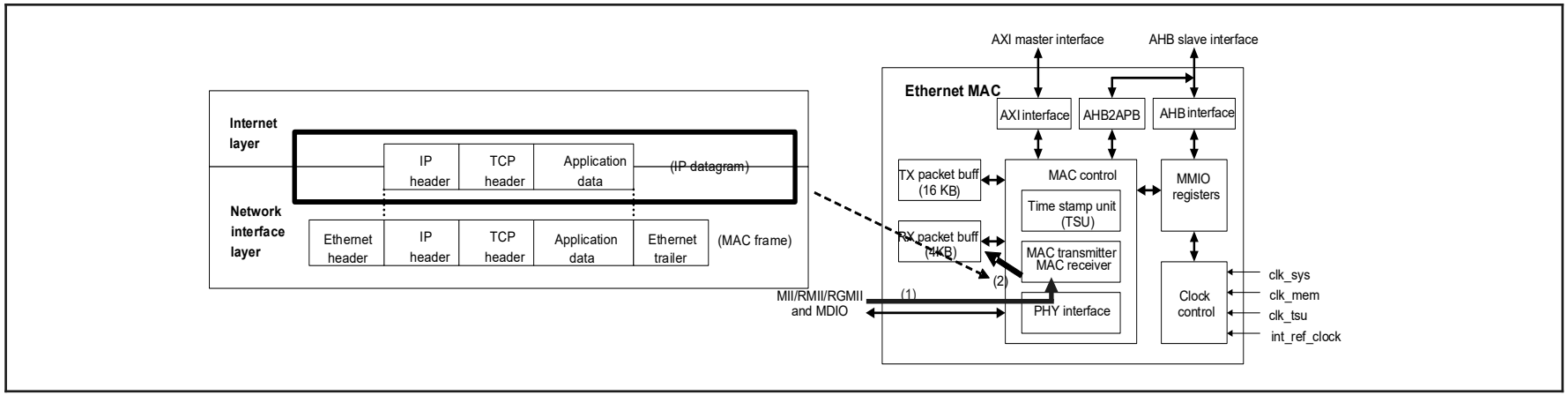
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Components (15/24)

MAC receiver

Procedure:

1. MAC frame is checked and demultiplexed by the hardware
2. IP datagram is transferred to the RX packet memory[1]



[1] Support to DMA transfer. DMAC is implemented in the MAC control.

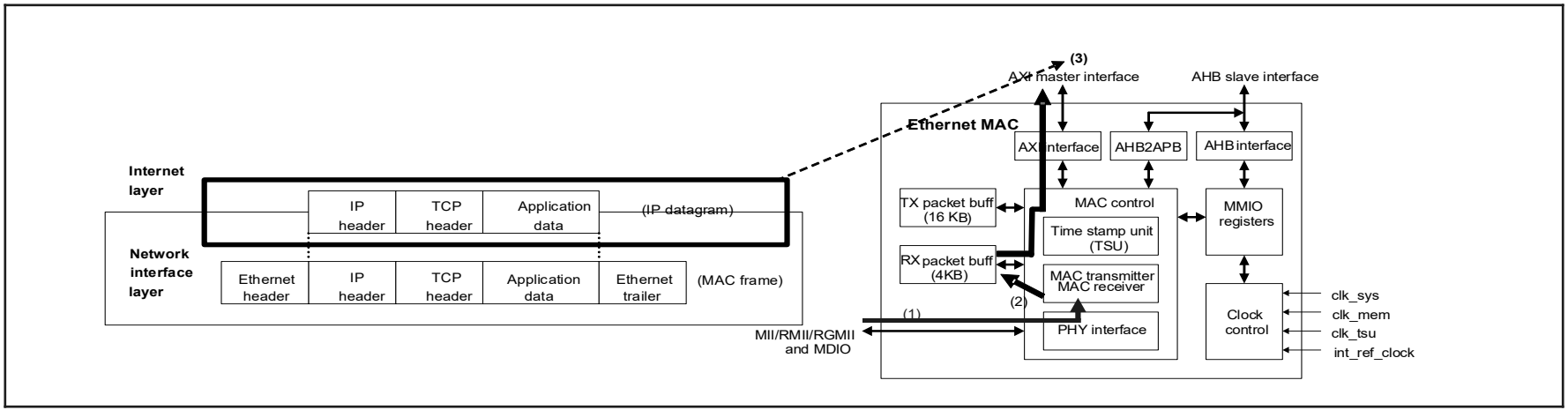
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Components (16/24)

MAC receiver

Procedure:

1. MAC frame is checked and demultiplexed by the hardware
2. IP datagram is transferred to the RX packet memory[1]
3. IP datagram is transferred to the internal memory via the AXI bus[1]



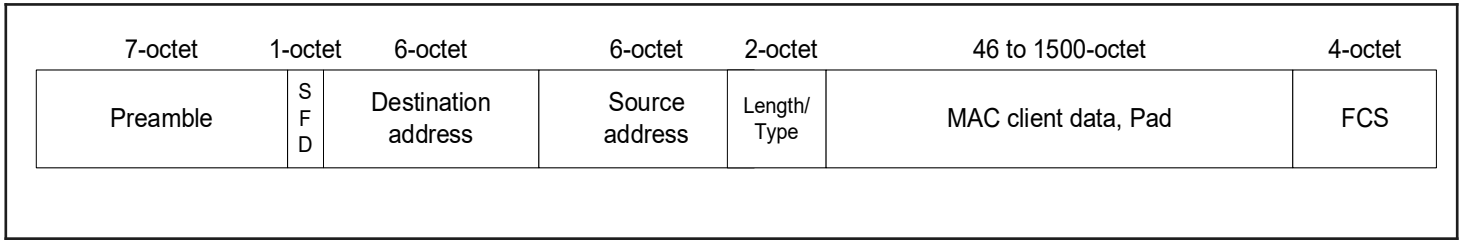
[1] Support to DMA transfer. DMAC is implemented in the MAC control.

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Components (17/24)

MAC frame

– Frame format



Notes

– SFD: Start of frame delimiter

– FCS: Flag check sequence

Hint bar

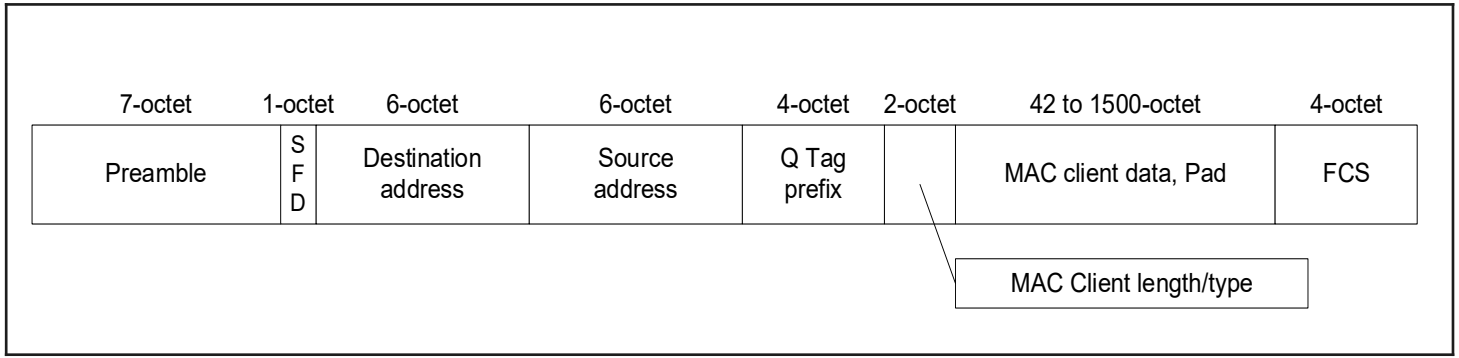
See the architecture reference manual for additional details.

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Components (18/24)

MAC frame

– Basic frame



Hint bar

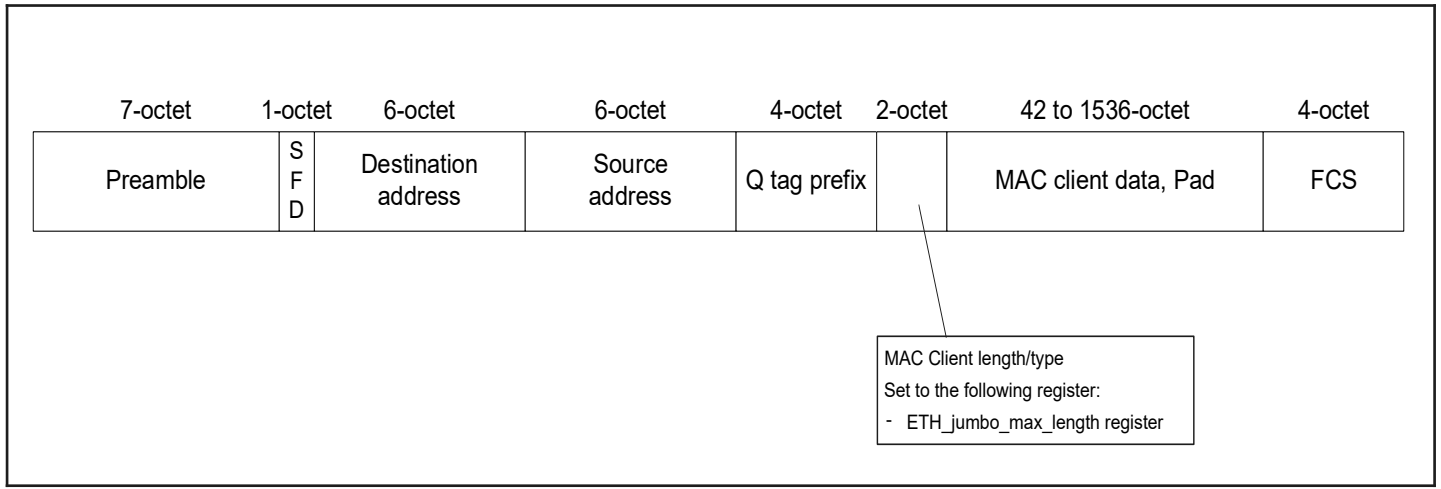
See the architecture reference manual for additional details.

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Components (19/24)

Jumbo frame support

– The maximum length of the XMC7000 jumbo frame payload is 1536 bytes



Hint bar

– See the architecture reference manual for additional details

Register Info

– ETH_jumbo_max_length

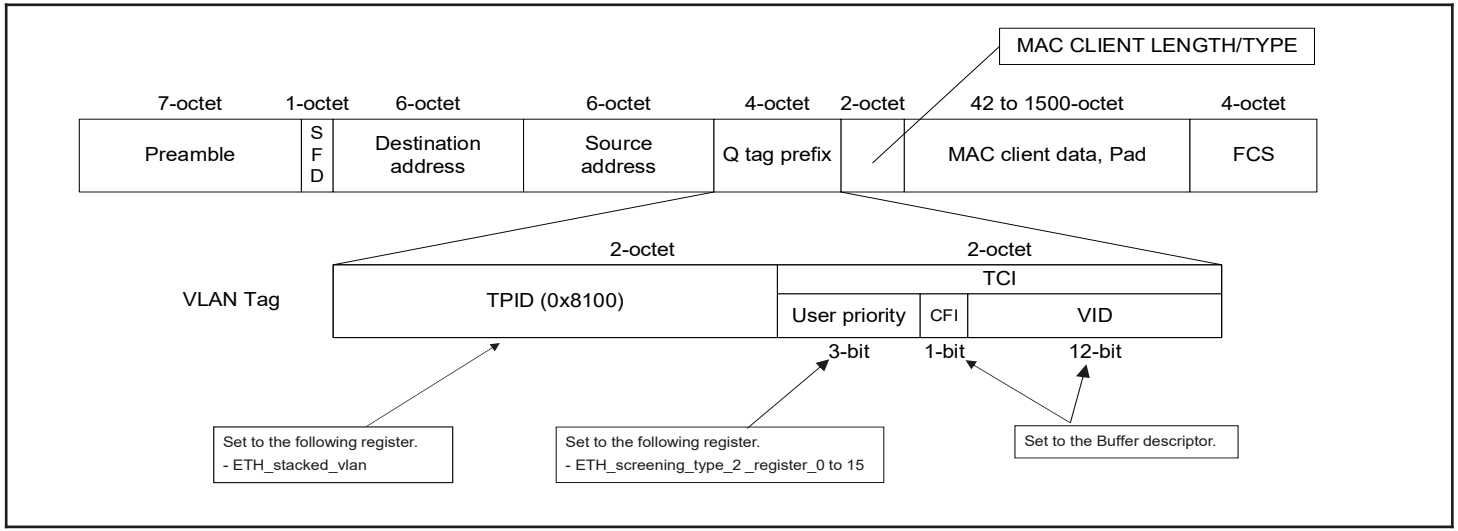
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Components (20/24)

VLAN support

– Provides a virtual LAN group in the network by VLAN tag

– VLAN tag is inserted into the Q-tagged frame



[1] TPID: Tag protocol identifier.
[2] TCI: Tag control information.
[3] CFI: Canonical format indicator.
[4] VID: VLAN identifier.

Hint bar

– See the architecture reference manual for additional details

Register info

– ETH_network_config

– ETH_stacked_vlan

– ETH_dma_config

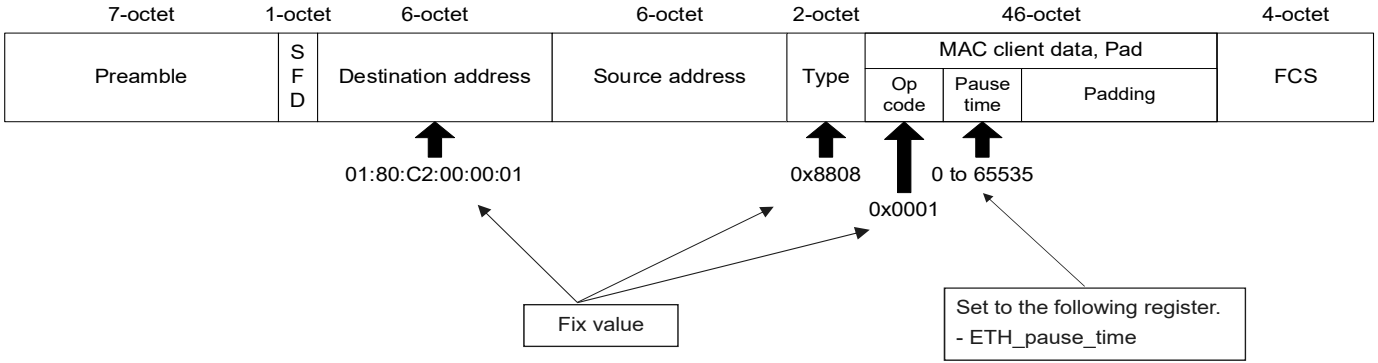
– ETH_screening_type_2 _register_0 to 15

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Components (21/24)

Pause frame support

– Pause frame is used to prevent self-buffer overflow



Hint bar

– See the architecture reference manual for additional details

Register info

– ETH_network_config

– ETH_pause_time

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Components (22/24)

Audio video bridging systems support

- Supports the timing and synchronization (IEEE 802.1AS)
- Supports the TSU[1]
  - Ethernet MAC has a TSU compatible to IEEE 1588
- Supports the FQTSS[2] (IEEE 802.1Qav)
  - Ethernet MAC has registers to support FQTSS
  - FQTSS is controlled by software using registers and supports priority control of transmission data

Hint bar

See the architecture reference manual for additional details.

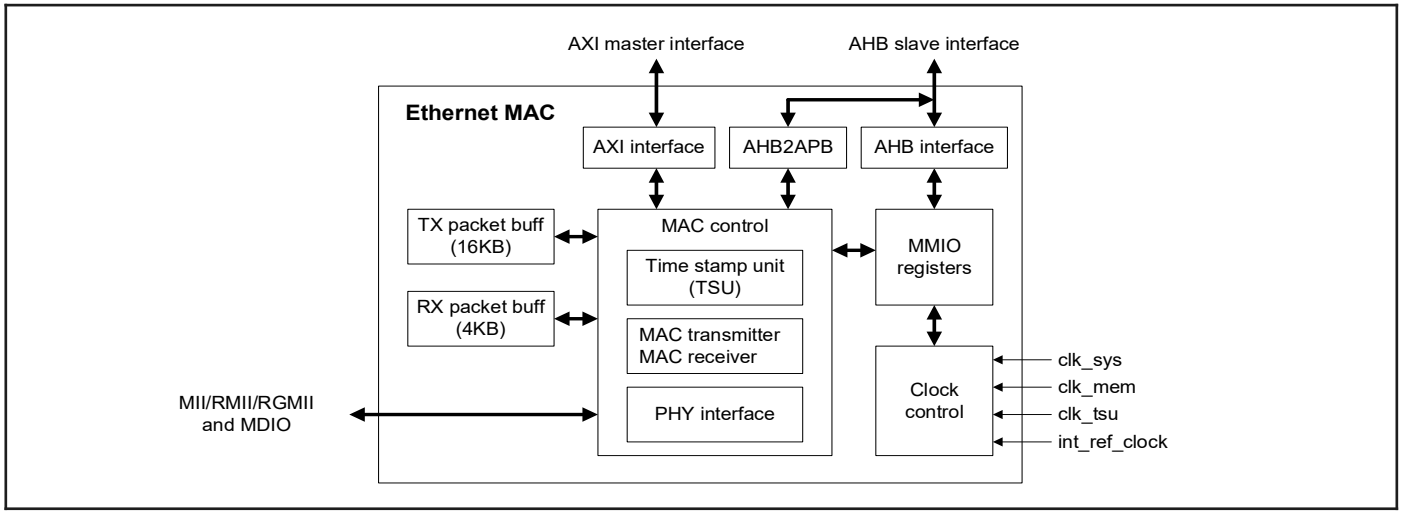
[1] TSU: Time stamp unit.
[2] FQTSS: Forwarding and queuing enhancements for time-sensitive streams.

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Components (23/24)

Clock control

- The following clocks are needed to execute the internal operation of Ethernet MAC
  - clk_sys
  - clk_mem
  - clk_tsu
  - int_ref_clock



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See the architecture reference manual, clocks to EMAC (section 29.3.15), for additional details.

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Components (24/24)

Clock sources

Usage of each clock is listed here:

Clock	Function
clk_sys	To generate MDC clock and for AHB operation, clk_sys is derived from CLK_PERI
clk_tsu	TSU clock for TSU timer
clk_mem	Fast clock for AXI operation
int_ref_clock	Internal reference clock supplied from PLL

Hint bar

See the architecture reference manual, clocks to EMAC (section 29.3.15), for additional details.

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Revision history

Document revision	Date	Description of change
**	2022-05-13	Initial release.
*A	2026-03-13	Migrated to the latest empower training presentation template.

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