

XMC7000 Device power modes

Customer training workshop (CTW)

November 2025

public

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Target products

Target product list for the following training materials:

Family category	Series	Code flash memory size
XMC7200	XMC7200-8M	Up to 8384 KB
XMC7100	XMC7100-4M	Up to 4160 KB

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XMC7200 - 8M family



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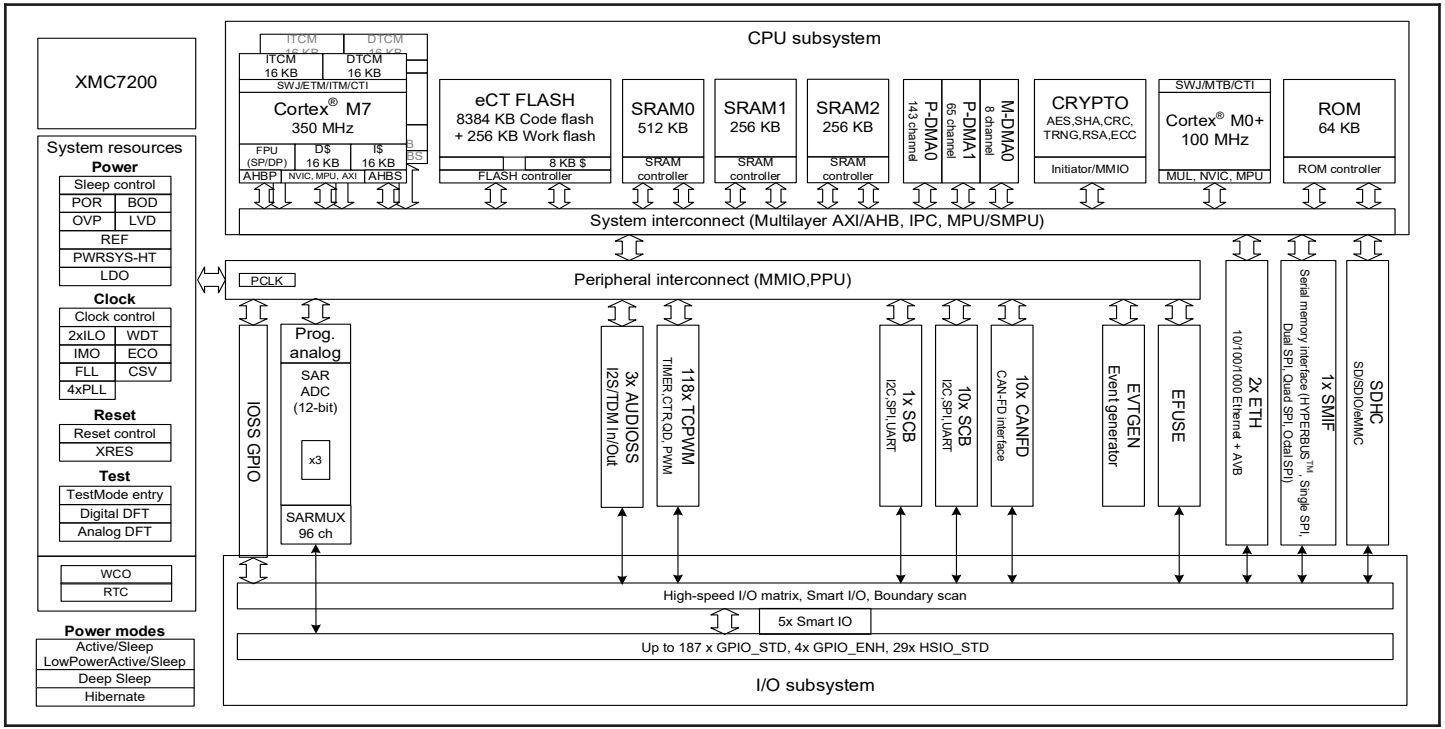
Introduction to XMC7200 - 8M

– Device power modes are controlled by sleep control in the System resources



Hint bar

See the architecture reference manual, chapter 17 device power modes for additional details.

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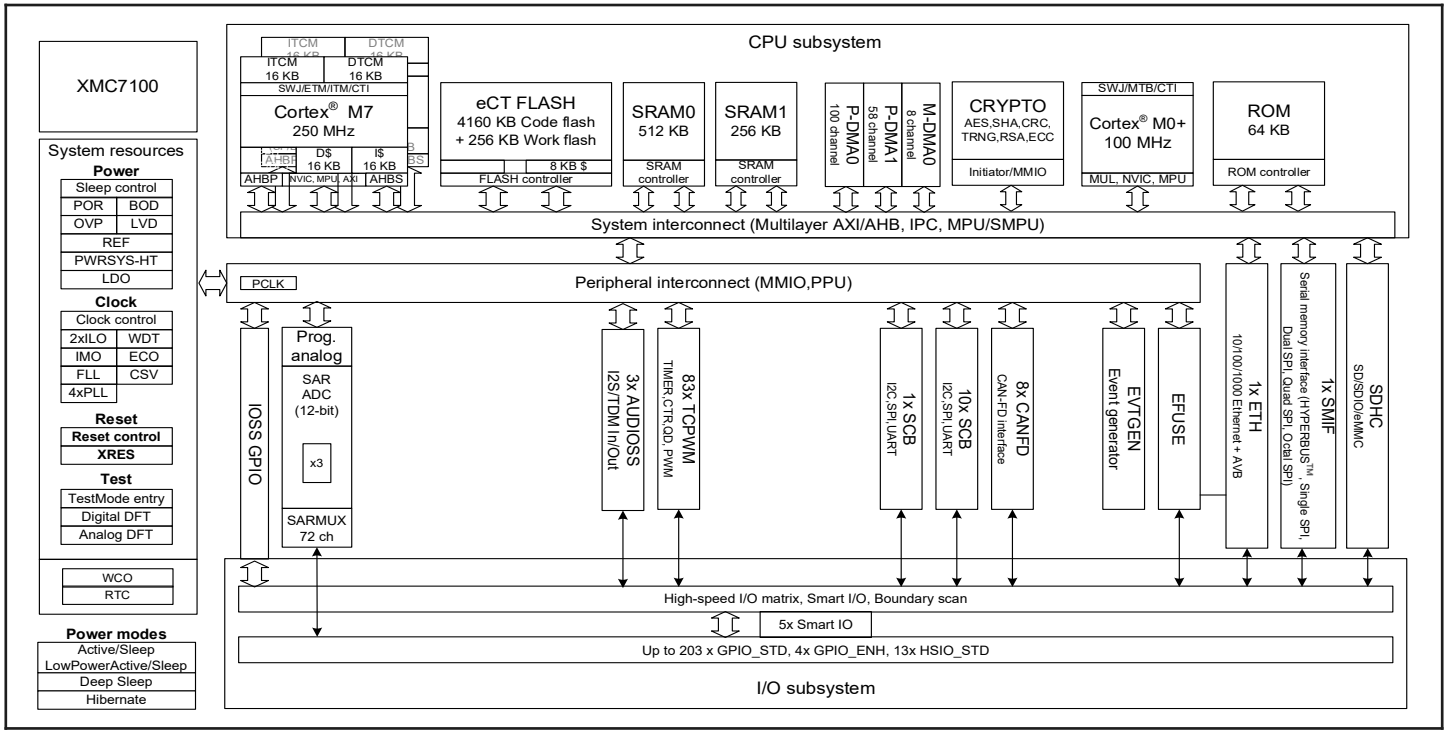
XMC7100 - 4M family



public

Introduction to XMC7100 - 4M

– Device power modes are controlled by sleep control in the system resources



Hint bar

See the reference manual chapter 17 device power modes for additional details.

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Device power modes

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Overview

XMC7000 supports the following power modes:

- Active mode (high-power consumption)
- Sleep mode (medium or high-power consumption)
- Deep Sleep mode (medium or low-power consumption)
- Hibernate mode (medium or low-power consumption)

Advantage

- Supports the device power modes to optimize power consumption for user applications

Hint bar

See the reference manual chapter 17 device power modes for additional details.

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Types of device power modes

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Active mode

- The device enters the Active mode upon device reset
- All the logic, memory, and peripherals are available
- The software can decide to enable or disable specific peripherals and power domains

Hint bar

- See the device power modes reference manual chapter section 17.4 summary for additional details
- In Active mode, power consumption can be reduced using software control (such as clock settings and power on/off). The software setting is available in the low-power profiles (LPACTIVE)
- See the XMC7100 and XMC7200 datasheet for the current consumption details

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Active mode (contd.)

–	Component	State	Component	State
Core function	CPU	ON	High-speed clock (IMO/ECO/PLL)	ON
	P-DMA/M-DMA	ON	ILO/WCO/LPECO[1]	ON
	SRAM	ON	Power-on-Reset (POR)	ON
	Flash	ON	LVD/BOD/OVD/OCD	ON
	CSV	ON	–	–
Peripherals	ADC	ON	RTC	ON
	TCPWM	ON	SCB	ON
	GPIO	ON	–	–
	EVTGEN	ON	M_TTCAN	ON
	WDT/MCWDT	ON	Others	ON

Hint bar

- See the device power modes reference manual chapter section 17.4 summary for additional details
- In Active mode, power consumption can be reduced using software control (such as clock settings and power on/off). The software setting is available in the low-power profiles (LPACTIVE)
- See the XMC7100 and XMC7200 datasheet for the current consumption details

[1] See the device-specific datasheet to check if LPECO is supported.

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Sleep mode

- The CPU enters the Sleep mode when the CPU clock is turned OFF
- All the other peripherals are available
- Any peripheral interrupt can wake up the CPU in the Active mode

Hint bar

- See the device power modes reference manual chapter for additional details
- In Sleep mode, power consumption can be reduced using software control (such as clock settings and power on/off). The software setting is available in the low-power profiles (LPSLEEP)
- See the XMC7100 and XMC7200 datasheet for the current consumption details

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Sleep mode (contd.)

–	Component	State	Component	State
Core function	CPU	Sleep	High-speed clock (IMO/ECO/PLL)	ON
	P-DMA/M-DMA	ON	ILO/WCO/LPECO[1]	ON
	SRAM	ON	Power-on-reset (POR)	ON
	Flash	ON	LVD/BOD/OVD/OCD	ON
	CSV	ON	–	–
Peripherals	ADC	ON	RTC	ON
	TCPWM	ON	SCB	ON
	GPIO	ON	–	–
	EVTGEN	ON	M_TTCAN	ON
	WDT/MCWDT[2]	ON	Others	ON

Hint bar

- See the device power modes reference manual chapter for additional details
- In Sleep mode, power consumption can be reduced using software control (such as clock settings and power ON/OFF). The software setting is available in the low-power profiles (LPSLEEP)
- See the XMC7100 and XMC7200 datasheet for the current consumption details

[1] See the device-specific datasheet to check if LPECO is supported.
[2] WDT/MCWDT operation can be disabled before switching to low-power mode. If WDT/MCWDT is used in low-power mode, CPU must wake up to clear the WDT/MCWDT.

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Deep Sleep mode

- Only low-frequency peripherals are available in the Deep Sleep mode
- SRAM data is retained[1]
- LVD/BOD/OVD/OCD monitors power lines in low-power mode
- Specific peripheral (WDT, RTC, EVTGEN, SCB#0, and GPIO) interrupts can wake up the CPU to Active mode
- In Debug mode, an attempt to enter Deep Sleep results in a transition to Sleep mode instead, with all power and clocks active. Upon terminating the debug session, the device will automatically transition to Deep Sleep mode

Hint bar

- See the device power modes reference manual chapter for additional details
- See the XMC7100 and XMC7200 datasheet for the current consumption details

[1] This is not retained by default. It must be configured by software.

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Deep Sleep mode (contd.)

–	Component	State	Component	State
Core function	CPU	Retention[3]	High-speed clock (IMO/ECO/PLL)	OFF
	P-DMA/M-DMA	Retention[3]	ILO/WCO/LPECO[2]	ON
	SRAM	Retention[3]	Power-on-Reset (POR)	ON
	Flash	OFF	LVD/BOD/OVD/OCD	ON
	CSV	ON	–	–
Peripherals	ADC	Retention[3]	RTC	ON
	TCPWM	OFF	SCB	ON (only 0ch)
	GPIO	ON/Freeze	–	–
	EVTGEN	ON	M_TTCAN	Retention[3]
	WDT/MCWDT[4]	ON	Others	Retention[3]

Hint bar

- See the device power modes reference manual chapter for additional details
- Specific peripheral (WDT, RTC, EVTGEN, SCB#0, and GPIO) interrupts can wake up the CPU to Active mode
- In Debug mode, an attempt to enter Deep Sleep results in a transition to Sleep mode instead, with all power and clocks active. Upon terminating the debug session, the device will automatically transition to Deep Sleep mode
- See the XMC7100 and XMC7200 datasheet for the current consumption details

[2] See the device-specific datasheet to check if LPECO is supported.
[3] Specific registers of CPU, DMA, and peripherals are retained while other parts are powered off.
[4] WDT/MCWDT operation can be disabled before switching to low-power mode. If WDT/MCWDT is used in low-power mode, CPU must wake up to clear WDT/MCWDT.

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Hibernate mode

- I/O states, RTC, WDT, and POR are retained; everything else is in the OFF mode
- Device resets on wakeup
- Wakeup event: RTC or GPIO (up to four pins[1] in total) or WDT

Hint bar

- See the device power modes reference manual chapter section 17.4 summary for additional details
- See the XMC7100 and XMC7200 datasheet for the current consumption details

[1] In the XMC7000 device, only two pins support this wakeup functionality. The datasheet contains additional details.

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Hibernate mode

–	Component	State	Component	State
Core function	CPU	OFF	High-speed clock (IMO/ECO/PLL)	OFF
	P-DMA/M-DMA	OFF	ILO/WCO/LPECO[2]	ON
	SRAM	OFF	Power-on-Reset (POR)	ON
	Flash	OFF	LVD/BOD/OVD/OCD	OFF
	CSV[3]	ON	–	–
Peripherals	ADC	OFF	RTC	ON
	TCPWM	OFF	SCB	OFF
	GPIO	FREEZE[4]	–	–
	EVTGEN	OFF	M_TTCAN	OFF
	WDT/MCWDT[5]	ON (only WDT)	Others	OFF

Hint Bar

- See the device power modes reference manual chapter section 17.4 summary for additional details
- See the XMC7100 and XMC7200 datasheet for the current consumption details

[2] See the device-specific datasheet to check if LPECO is supported.
[3] See the device-specific datasheet to check if CSV function is available in Hibernate mode.
[4] The I/O state must be frozen before going into Hibernate mode and unfrozen after Reset, to complete the transition to Active mode.
[5] WDT/MCWDT operation can be disabled before switching to low-power mode. If WDT/MCWDT is used in low-power mode, CPU must wake up to clear WDT/MCWDT.

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Power mode transitions

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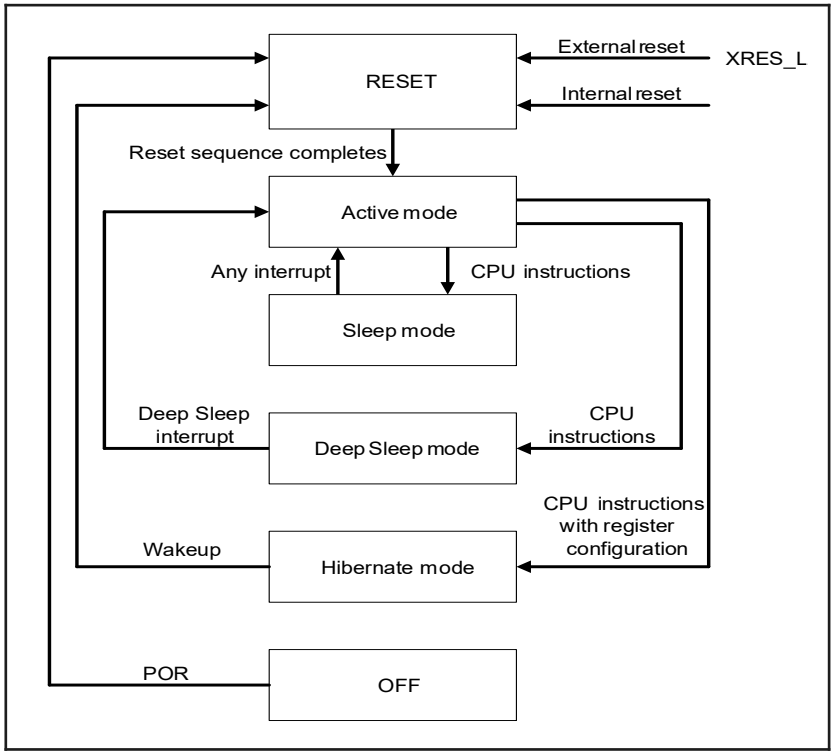
Power mode transitions

Device state and low-power mode transitions

- RESET/OFF state transitions
- Low-power mode transitions
  - Sleep mode
  - Deep Sleep mode
  - Hibernate mode



Hint bar

See the device power modes reference manual chapter section 17.3 power mode transitions for additional details.

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RESET/OFF state transitions

OFF state

- Represents the state with no power applied
- Enters RESET when power-up is above POR level (POR event)

RESET state

- Detects reset events: POR, external reset, and internal reset[1]
- Enters Active mode after reset sequence completion
- Starts IMO

Hint bar

- See the device power modes reference manual chapter for additional details
- See the reset sources training section 17.3 power mode transitions for additional details

[1] Internal reset refers to reset by all factors except external reset (XRES_L).

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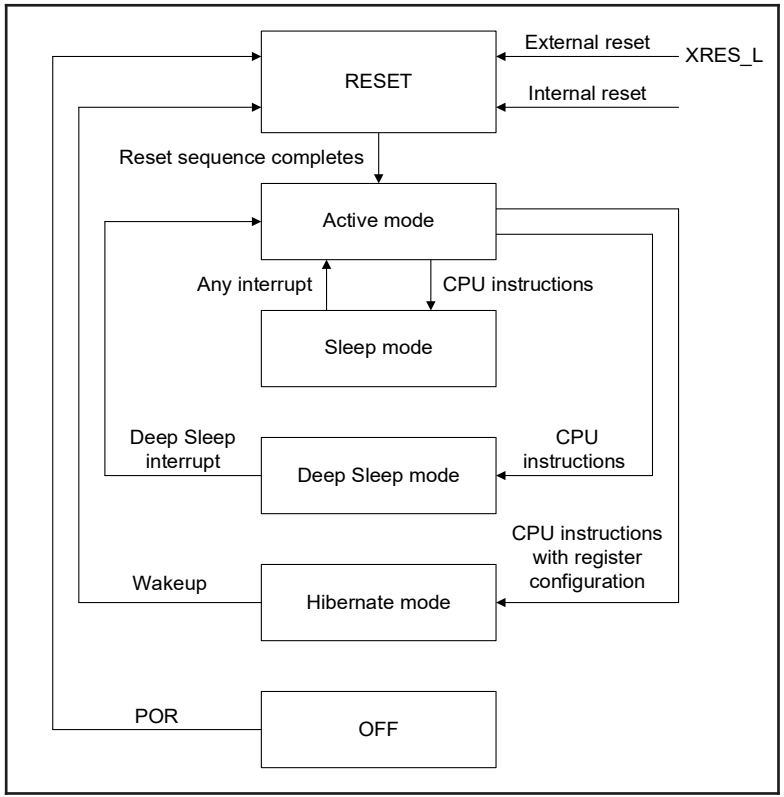
RESET/OFF state transitions (contd.)

- Assertion of XRES_L during any of the power modes, transitions the device to RESET



Hint bar

- See the device power modes reference manual chapter for additional details
- See the reset sources training section 17.3 power mode transitions for additional details

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Sleep mode transitions

Enter Sleep mode[1]

- Set the interrupt controller for application-specific wakeup interrupt
- Clears the SLEEPDEEP in SCR[2] register of both CPUs
- Execute WFI[3] instruction on both CPUs

Wakeup

- Wakeup of application-specific interrupt occurs
- The CPU transition from Sleep mode to Active mode and executes the interrupt handler

Note:

- When transitioning from Active mode to Sleep mode, the LPACTIVE profile is inherited
- When transitioning from Sleep mode to Active mode, the LPSLEEP profile is inherited

Hint bar

- See the device power modes reference manual chapter section 17.3.2 low-power mode transition for additional details
- Arm® provides additional supporting material on their webpage: infocenter.arm.com

[1] Device will enter Sleep mode only when both cores are in sleep state.
[2] The SCR register is CPU-specific.
[3] Wait for interrupt. Forces processor to suspend execution until Interrupt events.

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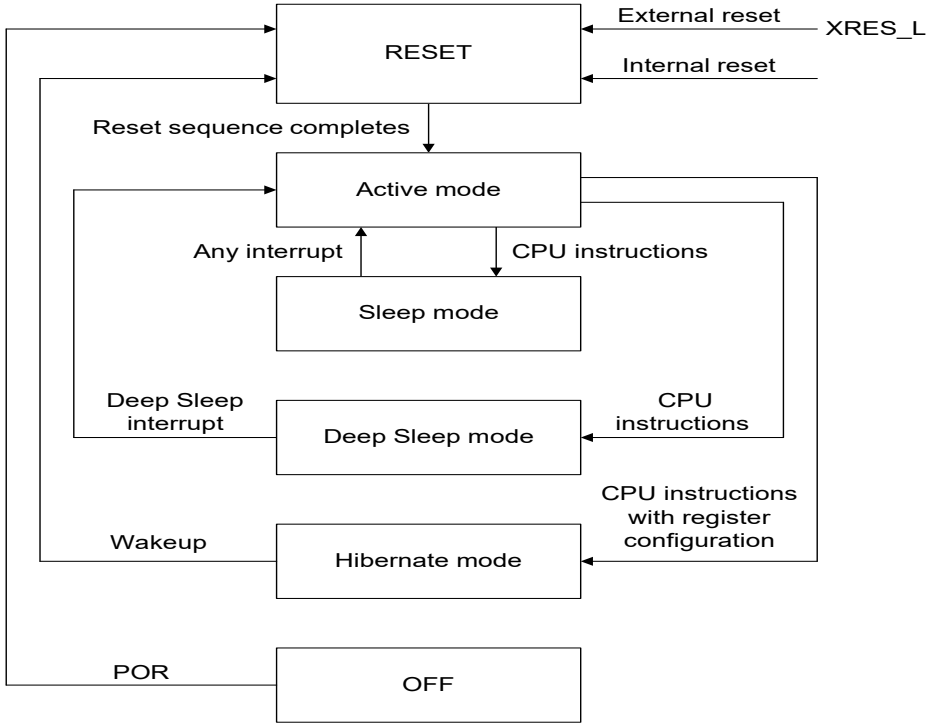
Sleep mode transitions (contd.)



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Deep Sleep mode transitions

Enter Deep Sleep mode

- Check if low-power functions are ready[1]
- Sets the wakeup interrupt controller (WIC) for application-specific wakeup interrupt
- Sets the SLEEPDEEP in the SCR register for both CPUs
- Executes the WFI instructions on both CPUs

Wakeup

- Wakeup interrupt from Deep Sleep peripherals or GPIOs
- Device transitions to Active mode
- CPU exits the Deep Sleep mode and executes the interrupt handler

Hint bar

- See the device power modes reference manual chapter Section 17.3.2 low-power mode transition for additional details
- If an attempt is made to transition to Deep Sleep mode while low-power circuits are not ready or the debugger is connected, the device will enter Sleep mode temporarily and automatically transition to Deep Sleep mode when both conditions are satisfied

[1] See the reference manual for additional PWR_CTL.LPM_READY details.

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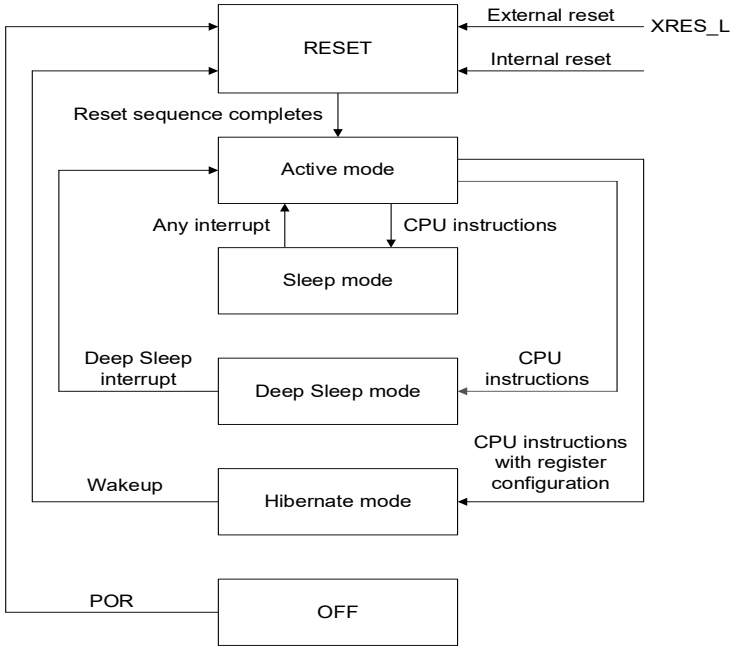
Deep Sleep mode transitions (contd.)



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[1] See the reference manual for additional PWR_CTL.LPM_READY details.

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Hibernate mode transitions

Enter Hibernate mode

- Sets the PWR_HIBERNATE[1] and PWR_HIB_DATA[1] registers based on the wakeup requirement
- Sets the FREEZE bit [17] of the PWR_HIBERNATE register to freeze the I/O pins
- Sets the HIBERNATE bit [31] of the PWR_HIBERNATE register to enter Hibernate mode
- Reads the PWR_HIBERNATE register to make sure that the write has taken effect
- Executes the WFI instruction on both CPUs

Wakeup

- Wakeup event from RTC, designated GPIOs, or WDT
- Enters RESET state
- Transitions to Active mode after reset sequence completion[2]

Hint bar

- See the device power modes reference manual chapter section 17.3.2 low-power mode transition for additional details
- XMC7000 offers four 32-bit registers in the backup domain to hold the data during Hibernate mode
- Hibernate wakeup is implemented as transition to active mode through reset

[1] The reference manual provides additional details of PWR_HIBERNATE and PWR_HIB_DATA.
[2] Unfreeze the I/Os after reaching Active state to complete transition.

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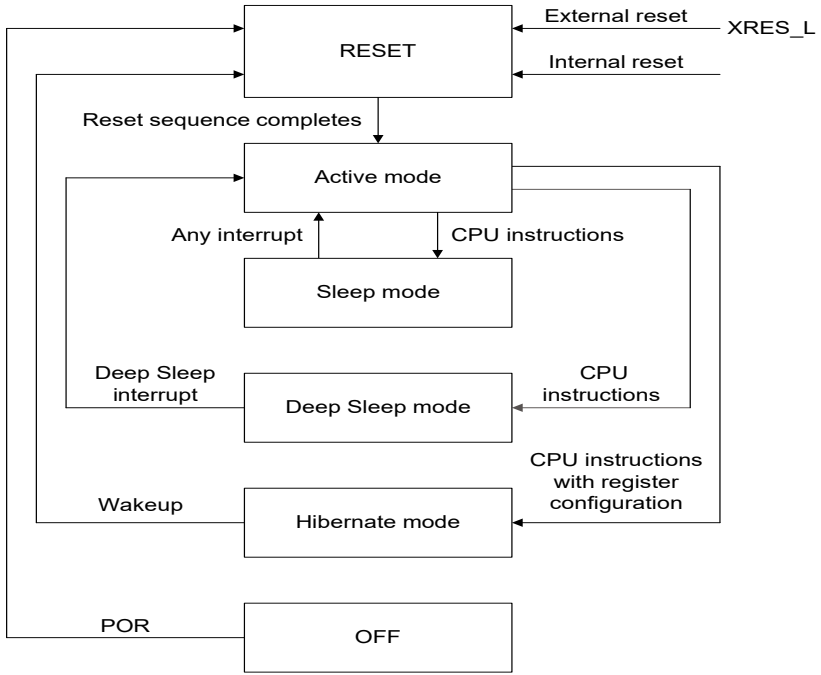
Hibernate mode transitions (contd.)



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Revision history

Document revision	Date	Description of change
**	2022-03-24	Initial release
*A	2025-11-07	Migrated to the latest empower training presentation template

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