Customer training workshop

XMC7000 microcontroller CPU subsystem

Target products

Target product list for this training material

Family category	Series	Code flash memory size
XMC7200	XMC7200-8M	Up to 8384KB
XMC7100	XMC7100-4M	Up to 4160KB

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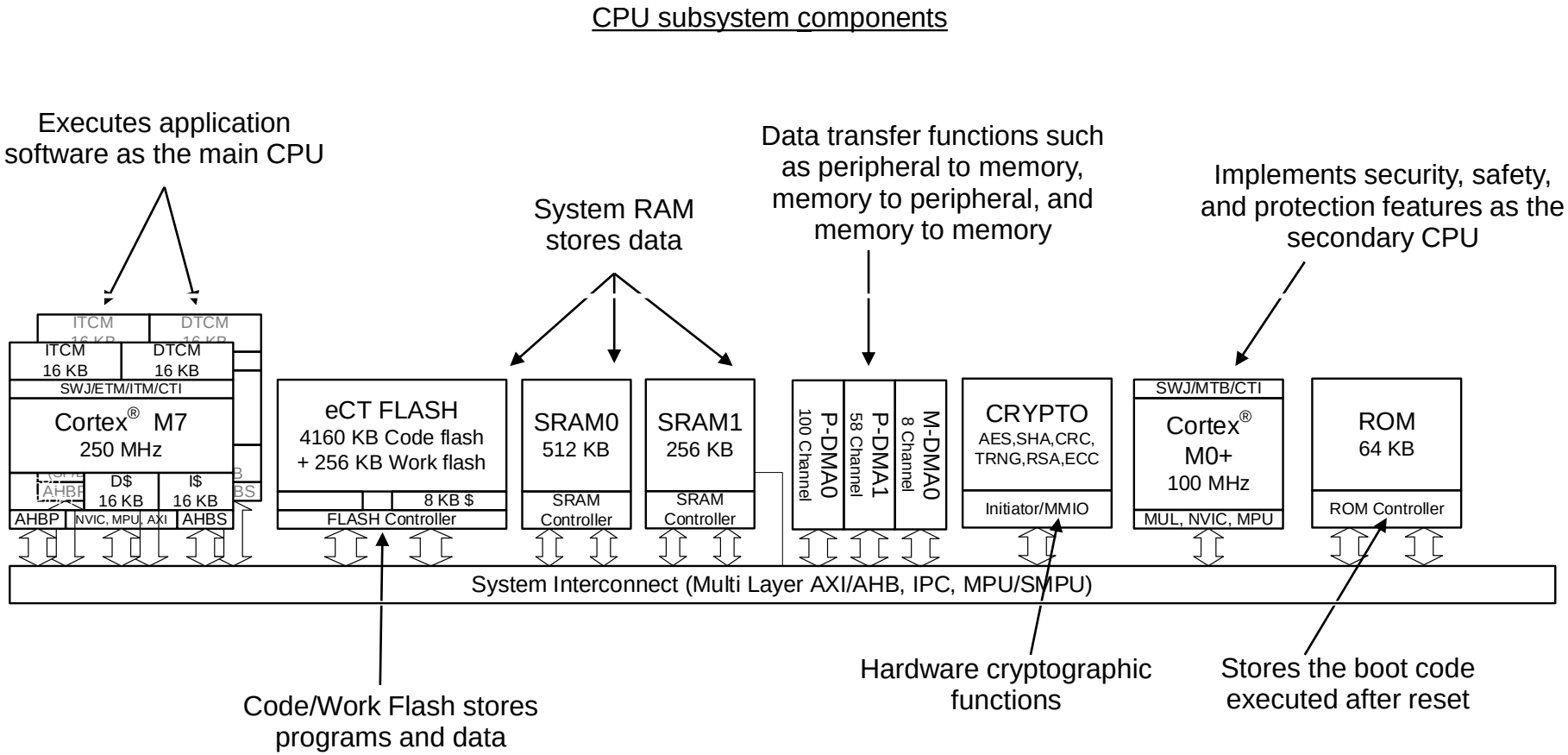
XMC7200 - 8M family

CPU subsystem overview

- The CPU subsystem (CPUSS) is based on dual 32-bit Arm® Cortex® CPUs



XMC7200 has two Arm® Cortex®-M7 CPUs for primary processing

Hint Bar

Section 2: Blocks and functionality in the XMC7200 datasheet

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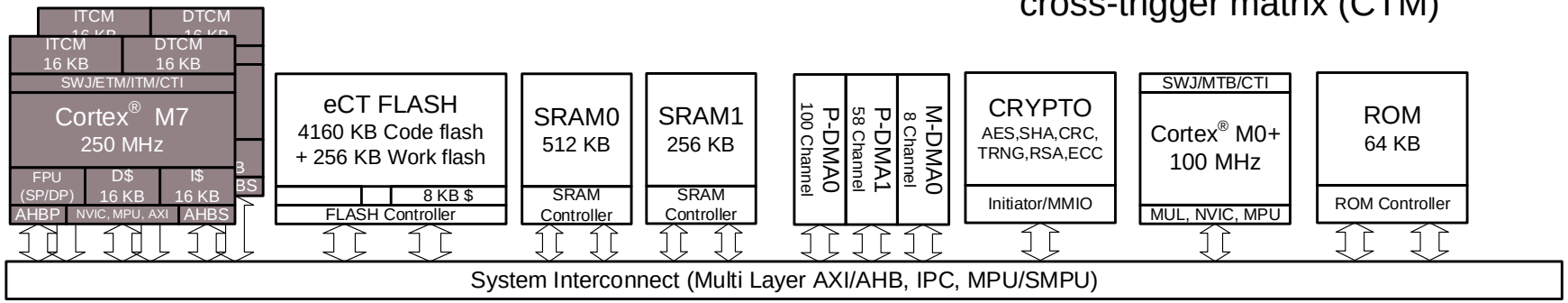
Cortex®-M7 features summary

- Main CPU
  - Two Cortex®-M7 CPUs[1]
  - Execution of application software
  - Up to 350-MHz operation (XMC7200)[2]
- Tightly-coupled memories (ITCM and DTCM) and instruction and data caches[3]
- System tick (SysTick) timer
- Floating-point unit (FPU)
  - Single and double precision
  - Compliant with the ANSI/IEEE Std 754-2008 IEEE Standard for Binary Floating-Point Arithmetic
- Memory protection unit (MPU)
  - Sixteen protection regions
  - Privileged/unprivileged, read/write attributes
- Nested vector interrupt controller (NVIC)
  - Eight external system interrupts, eight internal software interrupts, eight interrupt levels, and one non-maskable interrupt
  - Wakeup interrupt controller (WIC) support
  - Vector table relocation (VTOR)
- Debug components
  - Supports SWD and JTAG interface (SWJ)
  - Tracing components (ETM/ITM over ETB/TPIU)
  - Cross-triggering component (CTI) and cross-trigger matrix (CTM)

Cortex®-M7 block



[1] XMC7200 has two Arm® Cortex®-M7 CPUs for primary processing
[2] See the device datasheet for operation frequency of target product.
[3] See the device data sheet for supported capacity of ITCM, DTCM and caches.

Hint Bar

Arm provides additional reference material on their webpage at: infocenter.arm.com

Training section references:

- Interrupts

- Program and Debug Interface

- Protection Units

- SRAM Interface

Combined SWD/JTAG interface (SWJ)

Embedded trace macrocell (ETM)

Instrumentation trace macrocell (ITM)

Cross-triggering interface (CTI)

Embedded trace buffer (ETB)

Trace port interface Unit (TPIU)

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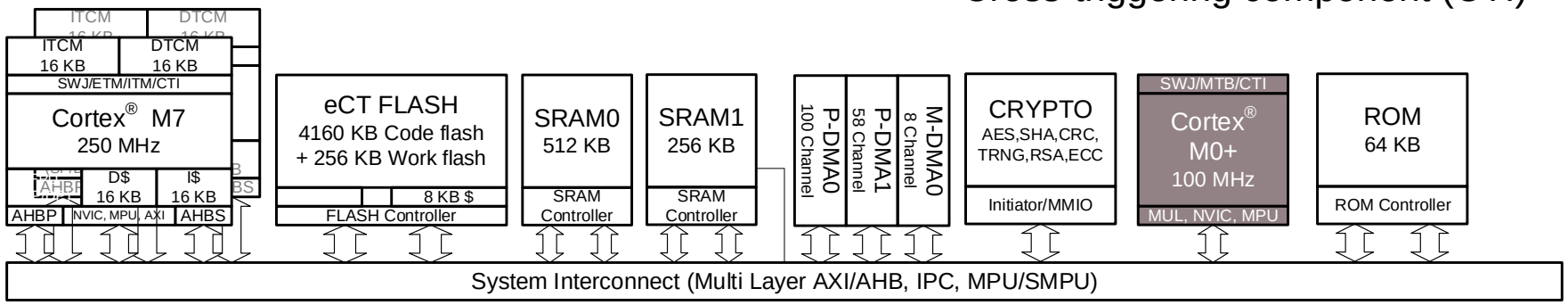
Cortex®-M0+ features summary

- Secondary CPU
  - Execution of boot process
  - Secure master in secure system to establish a root-of-trust
  - Up to 100-MHz operation
- SysTick timer
- Memory protection unit (MPU)
  - Eight protection regions
  - Privileged/unprivileged access attributes
- Nested vector interrupt controller (NVIC)
  - Eight external system interrupts, eight internal software interrupts, four interrupt levels, and one non-maskable interrupt
  - Wakeup interrupt controller (WIC) support
  - Vector table relocation (VTOR)
- Debug components
  - Supports SWD and JTAG interface (SWJ)
  - Tracing component (ETM over MTB)
  - Cross-triggering component (CTI)

Cortex®-M0+ block



Hint Bar

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infocenter.arm.com

Training section references:

- Interrupts

- Program and Debug Interface

- Protection Units

Combined SWD/JTAG interface (SWJ)

Micro trace buffer (MTB)

Embedded trace macrocell (ETM)

Cross-triggering interface (CTI)

[2] See the device datasheet for operation frequency of target product

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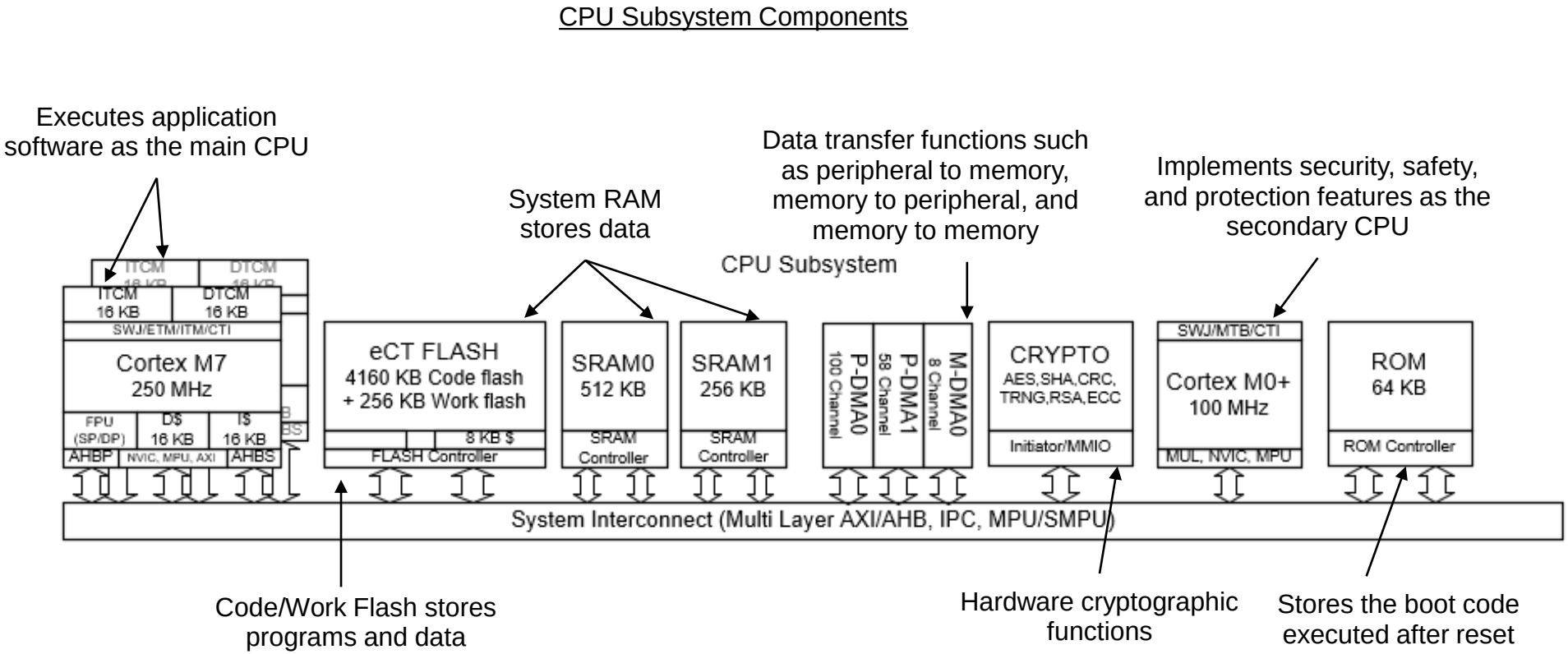
XMC7100 - 4M family

CPU subsystem overview

› The CPU subsystem (CPUSS) is based on dual 32-bit Arm® Cortex® CPUs



Hint Bar

Section 2: Blocks and functionality in the XMC7100 datasheet

XMC7100 has two Arm® Cortex®-M7 CPUs for primary processing

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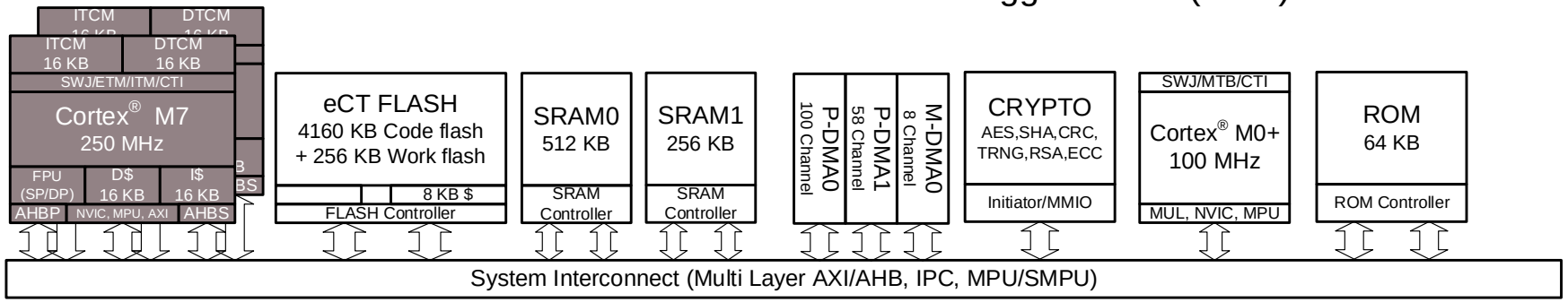
Cortex®-M7 features summary

- Main CPU
  - Two Cortex-M7 CPUs[1]
  - Execution of application software
  - Up to 250-MHz operation (XMC7100)[2]
- Tightly-coupled memories (ITCM and DTCM) and instruction and data caches[3]
- System tick (SysTick) timer
- Floating-point unit (FPU)
  - Single and double precision
  - Compliant with the ANSI/IEEE Std 754-2008 IEEE Standard for Binary Floating-Point Arithmetic
- Memory protection unit (MPU)
  - Sixteen protection regions
  - Privileged/unprivileged, read/write attributes
- Nested vector interrupt controller (NVIC)
  - Eight external system interrupts, eight internal software interrupts, eight interrupt levels, and one non-maskable interrupt
  - Wakeup interrupt controller (WIC) support
  - Vector table relocation (VTOR)
- Debug components
  - Supports SWD and JTAG interface (SWJ)
  - Tracing components (ETM/ITM over ETB/TPIU)
  - Cross-triggering component (CTI) and cross-trigger matrix (CTM)

Cortex®-M7 block



[1] XMC7100 has two Arm® Cortex®-M7 CPUs for primary processing
[2] See the device datasheet for operation frequency of target product.
[3] See the device data sheet for supported capacity of ITCM, DTCM and caches.

Hint Bar

Arm provides additional reference material on their webpage at: infocenter.arm.com

Training section references:

- Interrupts

- Program and Debug Interface

- Protection Units

- SRAM Interface

Combined SWD/JTAG interface (SWJ)

Embedded trace macrocell (ETM)

Instrumentation trace macrocell (ITM)

Cross-triggering interface (CTI)

Embedded trace buffer (ETB)

Trace port interface Unit (TPIU)

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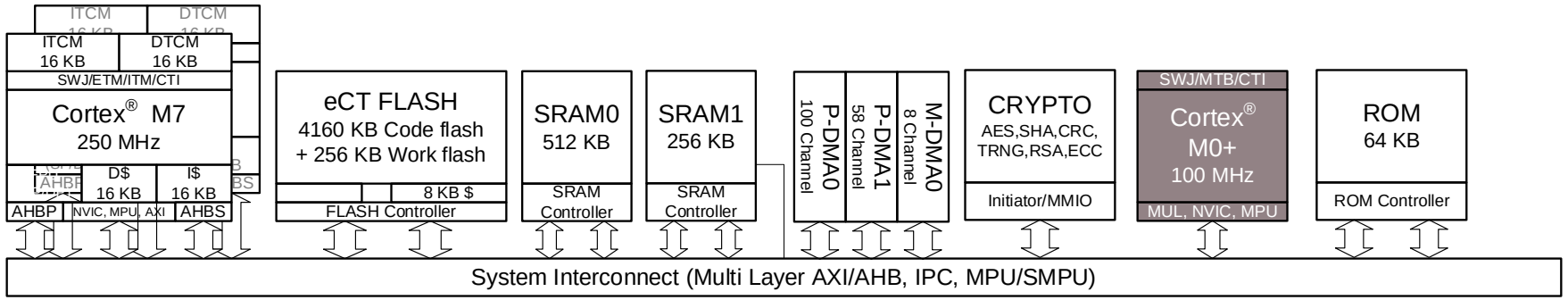
Cortex®-M0+ features summary

- Secondary CPU
  - Execution of boot process
  - Secure master in secure system to establish a root-of-trust
  - Up to 100-MHz operation
- SysTick timer
- Memory protection unit (MPU)
  - Eight protection regions
  - Privileged/unprivileged access attributes
- Nested vector interrupt controller (NVIC)
  - Eight external system interrupts, eight internal software interrupts, four interrupt levels, and one non-maskable interrupt
  - Wakeup interrupt controller (WIC) support
  - Vector table relocation (VTOR)
- Debug components
  - Supported SWD and JTAG interface (SWJ)
  - Tracing component (ETM over MTB)
  - Cross-triggering component (CTI)

Cortex®-M0+ block



Hint Bar

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infocenter.arm.com

Training section references:

- Interrupts

- Program and Debug Interface

- Protection Units

Combined SWD/JTAG interface (SWJ)

Micro trace buffer (MTB)

Embedded trace macrocell (ETM)

Cross-triggering interface (CTI)

[2] See the device datasheet for operation frequency of target product

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CPUSS dedicated master identifier

- Each bus master has a dedicated master identifier, which is used for:
  - Bus arbitration
  - IPC lock acquire functionality
  - Violation access information by MPU, SMPU, and PPU

Master Identifier[1]	XMC7200	XMC7100
0	Cortex®-M0+	Cortex®-M0+
1	Crypto	Crypto
2	P-DMA 0	P-DMA 0
3	P-DMA 1	P-DMA 1
4	M-DMA0	M-DMA0
5	SDHC	SDHC
9	Ethernet 0	Ethernet 0
10	Ethernet 1	-
13	Cortex-M7_1	Cortex-M7_1
14	Cortex-M7_0	Cortex-M7_0
15	Tap Controller	Test Controller

Hint Bar

Bus Master: Section 23

Inter processor communication (IPC)

Memory protection unit (MPU)

Shared memory protection unit (SMPU)

Peripheral protection unit (PPU)

[1] See the device datasheet for master identifier number and regarding peripherals of target product.

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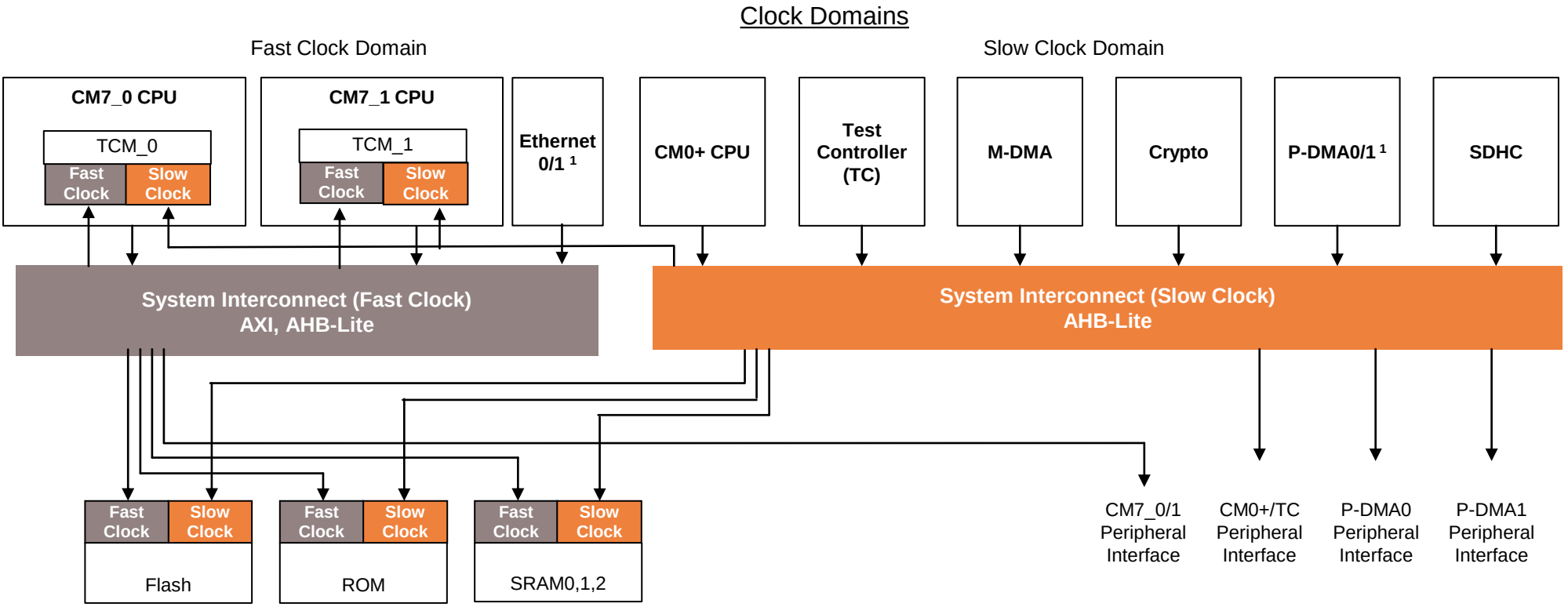
CPUSS bus infrastructure

- AHB-Lite and AXI bus infrastructure
- Bus clock domains
  - Fast/slow clock domains
  - Each memory interface has both domains
- Bus competition
  - CPUSS has multiple bus masters
  - Design a system that considers bus competition by simultaneous access



[1] See the device datasheet for master identifier number and regarding peripherals of target product.

Hint Bar

Sys Interface in CM7 can only access peripherals

Code Interface in CM7 can only access memory controllers

Training section references:

- Clock System

- SRAM interface

- Flash

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CPU features

- **Cortex®-M7**
  - 5 CoreMark/MHz and 2.14 DMIPS/MHz
  - ISA support (Thumb/Thumb-2)
  - 6-stage superscalar + branch prediction pipeline
  - Interconnect
    - AXI master
    - AHB peripheral port (AHBP/AHBS)
    - Tightly-coupled memory (ITCM/DTCM)
  - Instruction and data cache
  - DSP extensions
    - Single-cycle 16/32-bit MAC, single-cycle dual 16-bit MAC
    - 8/16-bit SIMD arithmetic
  - Floating point unit (FPU)
  - Memory protection unit (MPU)
  - Nested vector interrupt controller (NVIC)
    - Vector table relocation (VTOR)
  - Wake-up interrupt controller(WIC)
  - SysTick Timer

- **Cortex®-M0+**
  - 1.99 CoreMark/MHz and 0.9 DMIPS/MHz
  - ISA support (Thumb/Thumb-2)
  - 2-stage pipeline
  - Interconnect
    - AHB - Lite
  - Memory protection unit (MPU)
  - Nested vector interrupt controller (NVIC)
    - Vector table relocation (VTOR)
  - Wake-up interrupt controller(WIC)
  - SysTick Timer

Hint Bar

Arm provides additional reference material on their webpage at:
infocenter.arm.com

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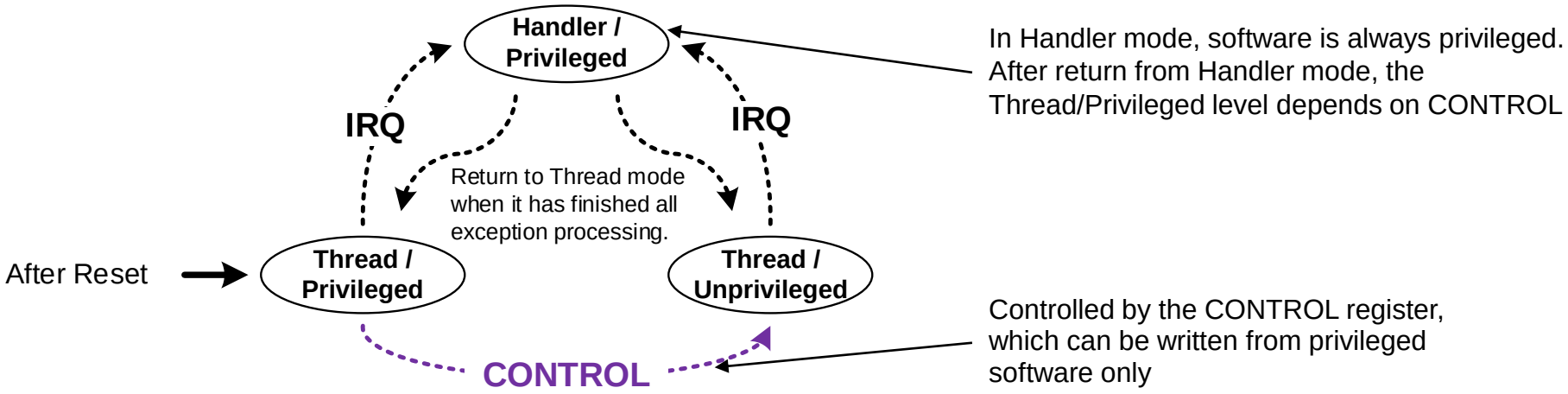
CPU mode transition

- Both CPUs support two operating modes and two privilege levels
  - Operating mode
    - Thread mode executes application software
    - Handler mode handles exceptions
  - Privilege levels
    - Unprivileged: Software has limited access to MSR/MRS instructions (uses CPS instructions), system timer, NVIC, system control block, and memory/peripherals
    - Privileged: Software can use all instructions and has access to all resources
    - Transition from Thread/Privileged to Thread/Unprivileged by CONTROL register[1]
    - Transition from Thread/Unprivileged to Thread/Privileged via SVC[2]



Hint Bar

Review TRM section 4.4 for additional details specific to CPU modes

Arm provides additional reference material on their webpage at: infocenter.arm.com

Move to system coprocessor register from the Arm register (MSR)

Move the contents of program status register to a general-purpose register (MRS)

Change processor state (CPS)

[1] The CONTROL register is a CPU-specific register. It defines privileged/unprivileged, stack pointer, and FPU extension.
[2] Supervisor calls are used to request privileged operations

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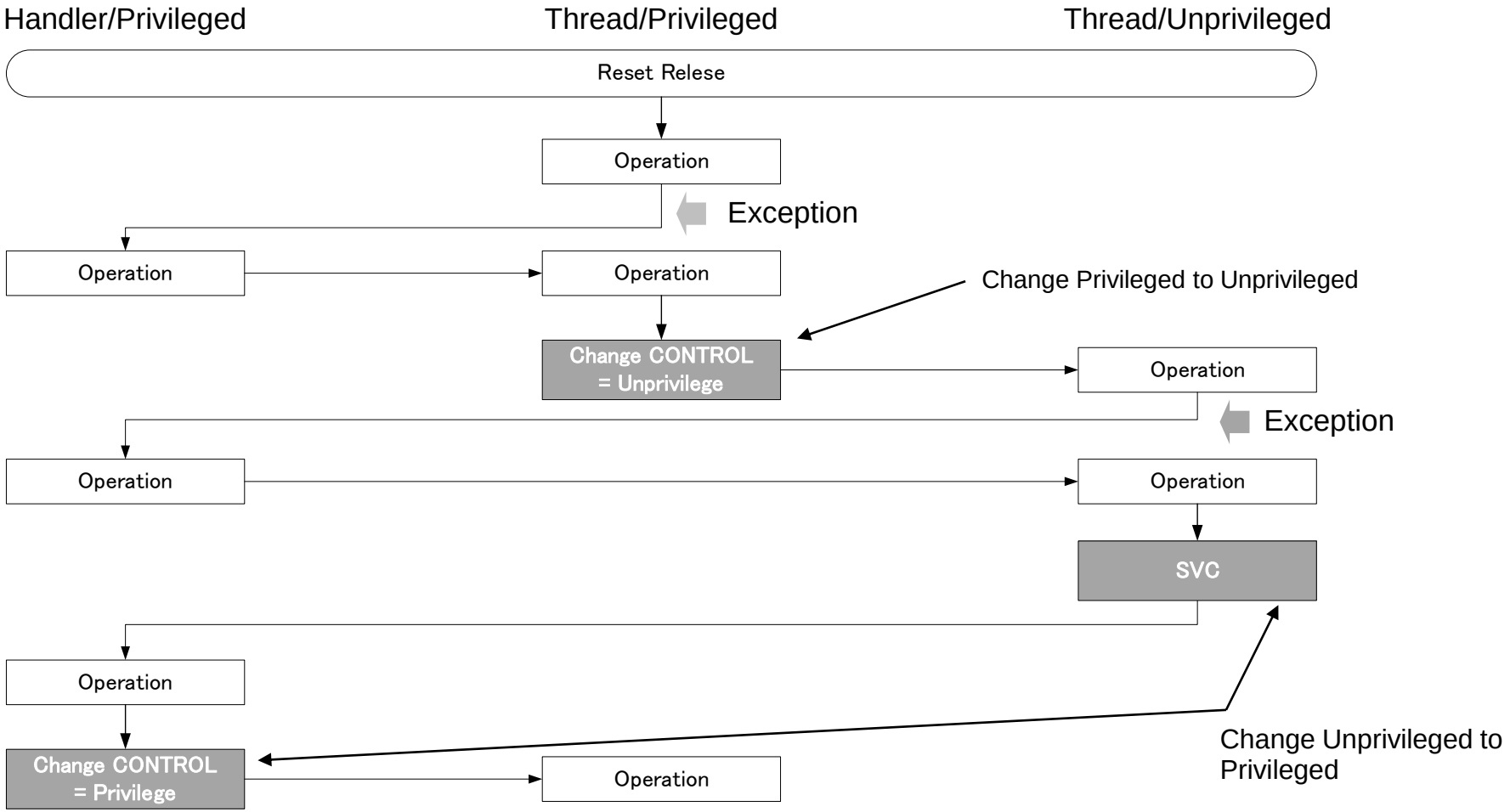
Operation modes transition

› Use case: Changing privileged/unprivileged mode



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Arm provides additional reference material on their webpage at:
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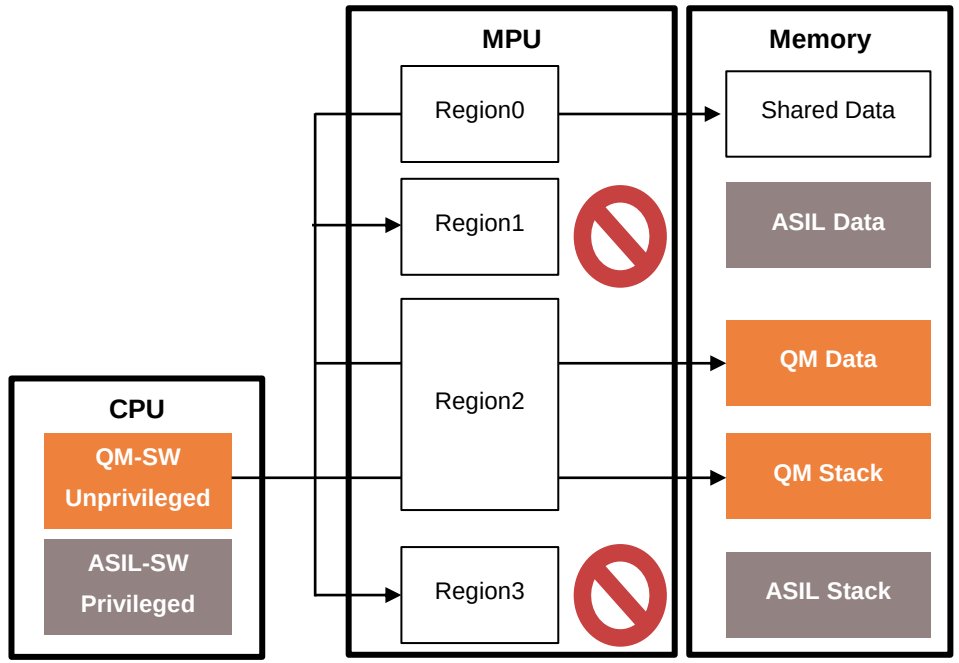
Memory protection

- Each CPU has a memory protection unit (MPU)[1] that:
  - Realizes software separation freedom of interface
  - Includes address range, read/write, and privileged/unprivileged attributes
  - Features sixteen protection regions
- Use case
  - Software partitioning of SIL and QM in functional safety

Example of MPU Operation



Hint Bar

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[1] MPU registers are written by privileged software and are only one part of the protection concept. For details, refer to the Protection Units training section.

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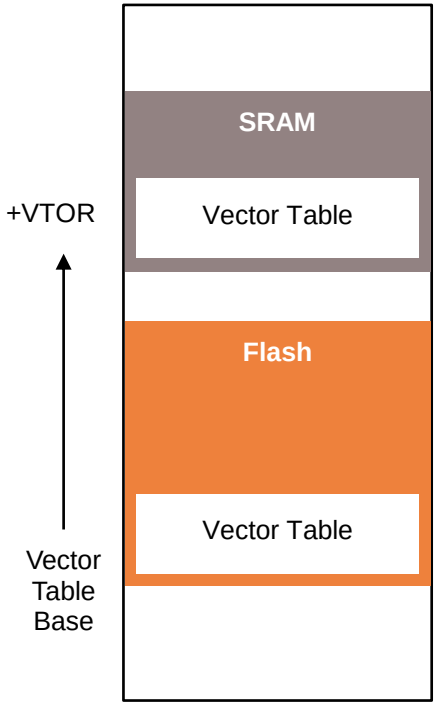
Vector table relocation

- **Vector Table Offset Register (VTOR)[1]**
  - Defines the location of the vector table of each core. There is a VTOR for each CM7 and another one for CM0.
  - Can be used to relocate the vector table from Flash to SRAM, allowing the interrupt handlers to change dynamically
  - VTOR is written from privileged software only
  - Use the following registers to set VTOR for both cores:
    - CM0_VECTOR_TABLE_BASE: By default set to beginning of Flash by Boot ROM
    - CM7_0/1_VECTOR_TABLE_BASE: Set by CM0+ application before releasing the CPU core CM7_0/1 from reset
  - After boot, each core copies the vector table to SRAM and updates VTOR with the address of the new location
- **Use cases**
  - Execute the program with RAM only, for Flash programming or performance improvement
  - Use different vectors depending on software level or system mode, such as normal and reprogramming

VTOR Operation



Hint Bar

Arm provides additional supporting material on their webpage at: infocenter.arm.com

See the Register TRM for additional details

[1] The VTOR register is a CPU-specific register

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System tick generation

- Each CPU supports a SysTick timer to measure time duration, which provides:
  - A 24-bit down counter
  - A selectable internal CPU clock or external clock
  - Active and Sleep mode operation
  - SysTick interrupt generation
- SysTick registers can be written from Privileged software only

- Use cases
  - RTOS tick timer
  - Alarm timer to alert when an action is not completed within a particular duration
  - Software completion time measurement

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Arm provides additional supporting material on their webpage at: infocenter.arm.com

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CPU subsystem memory feature summary

- TCM
  - ITCM and DTCM (instruction/data tightly coupled memory) for CM7
  - Size 16KB: ITCM/16KB: DTCM(XMC7000)
  - Error-correction code (ECC) function (SEC/DED)
- SRAM
  - Data storage and code execution
  - Size: up to 1024KB (XMC7200)
  - Size: up to 768KB (XMC7100)
  - Each CPU sharing
  - ECC function
- Flash
  - Code and Work Flash
  - Size: up to 8483KB: Code/ 256KB: Work (XMC7200) [1]
  - Size: up to 4160KB: Code/ 256KB: Work (XMC7100) [1]
  - ECC function
  - Instruction cache for each CPU
  - APIs for Flash programming
- ROM
  - Boot code for CM0+
  - API[2] function implementation

Hint Bar

TRM sections:

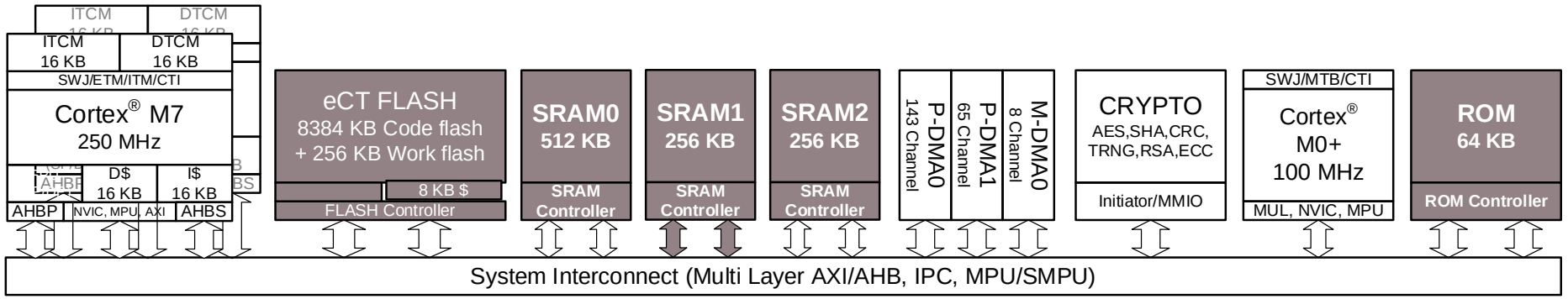
- Flash

- SRAM interface

- Boot

- XMC7200 address map

- XMC7100 address map



[1] See the device datasheet for memory size of target product.
[2] No user access to read or modify SROM code

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P-DMA/M-DMA feature summary

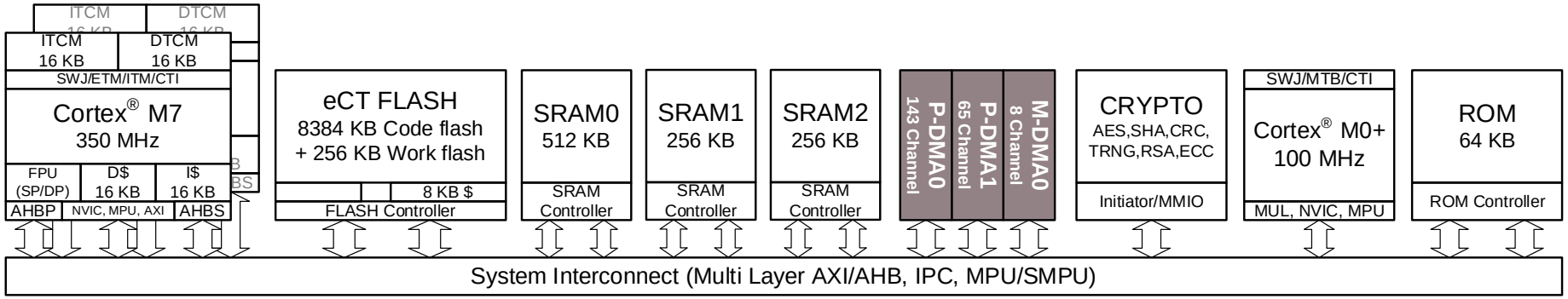
- Peripheral DMA (P-DMA)
  - Single transfer engine shared for all channels
  - Focuses on low-latency transfer
  - Transfer modes:
    - Single, 1D, 2D, and CRC
- Memory DMA (M-DMA)
  - Dedicated transfer engine for each channel
  - Focuses on high-memory bandwidth
  - Transfer modes:
    - Single, 1D, 2D, Memory Copy, and Scatter

Hint Bar

Training section references:

Direct Memory Access

P-DMA/M-DMA block



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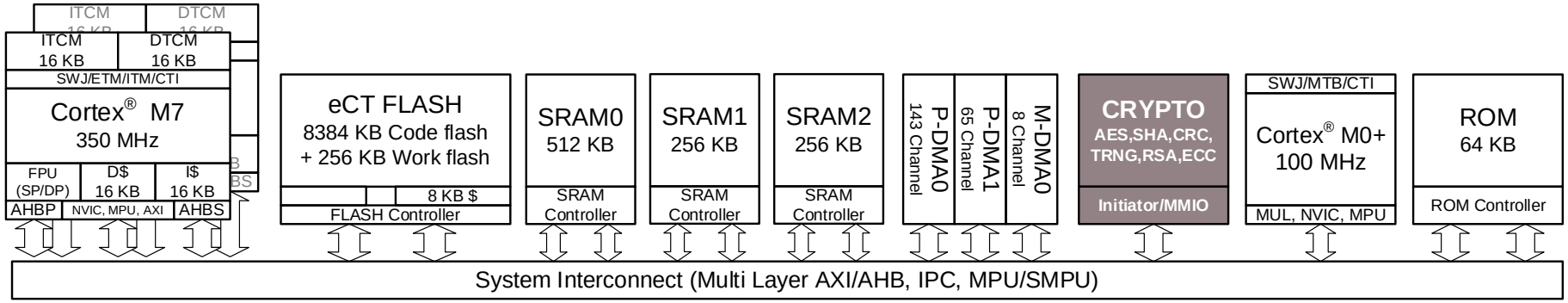
Cryptographic (Crypto) feature summary

- Hardware crypto functions[1]
  - Symmetric key encryption and decryption
  - Hashing
  - Message authentication
  - Random number generation
  - Cyclic redundancy checking
  - Asymmetric key cryptography

Crypto block



Hint Bar

Training section references:

- Device Security

[1] Access limited to the secure master (CM0+)

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Appendix

Comparison between families

Features		XMC7200 – 8M	XMC7100 – 4M
Main CPU	CPU	One/Two Cortex-M7 CPUs	
	Operating Frequency	350 MHz for the XMC7200	250 MHz for the XMC7100
	FPU	Single/double-precision	
	Cache	16KB instruction, 16KB data	
	MPU	Cortex-M7: 16 regions	
	Interrupt Structure	NVIC+WIC	
	System Tick Timer	Supported	
Secondary CPU	CPU	Cortex-M0+ CPU	
	Operating Frequency	Same (Up to 100 MHz)	
	MPU	Cortex-M0+: 8 regions	
	Interrupt Structure	NVIC+WIC	
	System Tick Timer	Supported	
Flash	Bus Interface	AXI, AHB-Lite	
	ECC (SEC/DED)	Supported	
	Bank Modes	Supported	
	Size (Code/Work)	8483KB / 256KB	4160KB/ 256KB
SRAM	Bus Interface	AXI, AHB-Lite	
	ECC (SEC/DED)	Support	
	TCM Size	16KB ITCM, 16KB DTCM	
	SRAM Size	1024KB	768KB
Boot		Supported	
Device Security with Crypto		Supported	
Direct Memory Access	P-DMA	Supported	
	M-DMA	Supported	

[1] This functionality is for debug purposes

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Revision History

Revision	ECN	Submission Date	Description of Change
**	7729812	2022-03-17	Initial release

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