

XMC7000 CAN FD controller

Customer training workshop (CTW)

November 2025

public

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Target products

Target product list for this training material:

Family category	Series	Code flash memory size
XMC7200	XMC7200-8M	Up to 8384 KB
XMC7100	XMC7100-4M	Up to 4160 KB

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XMC7200 - 8M family



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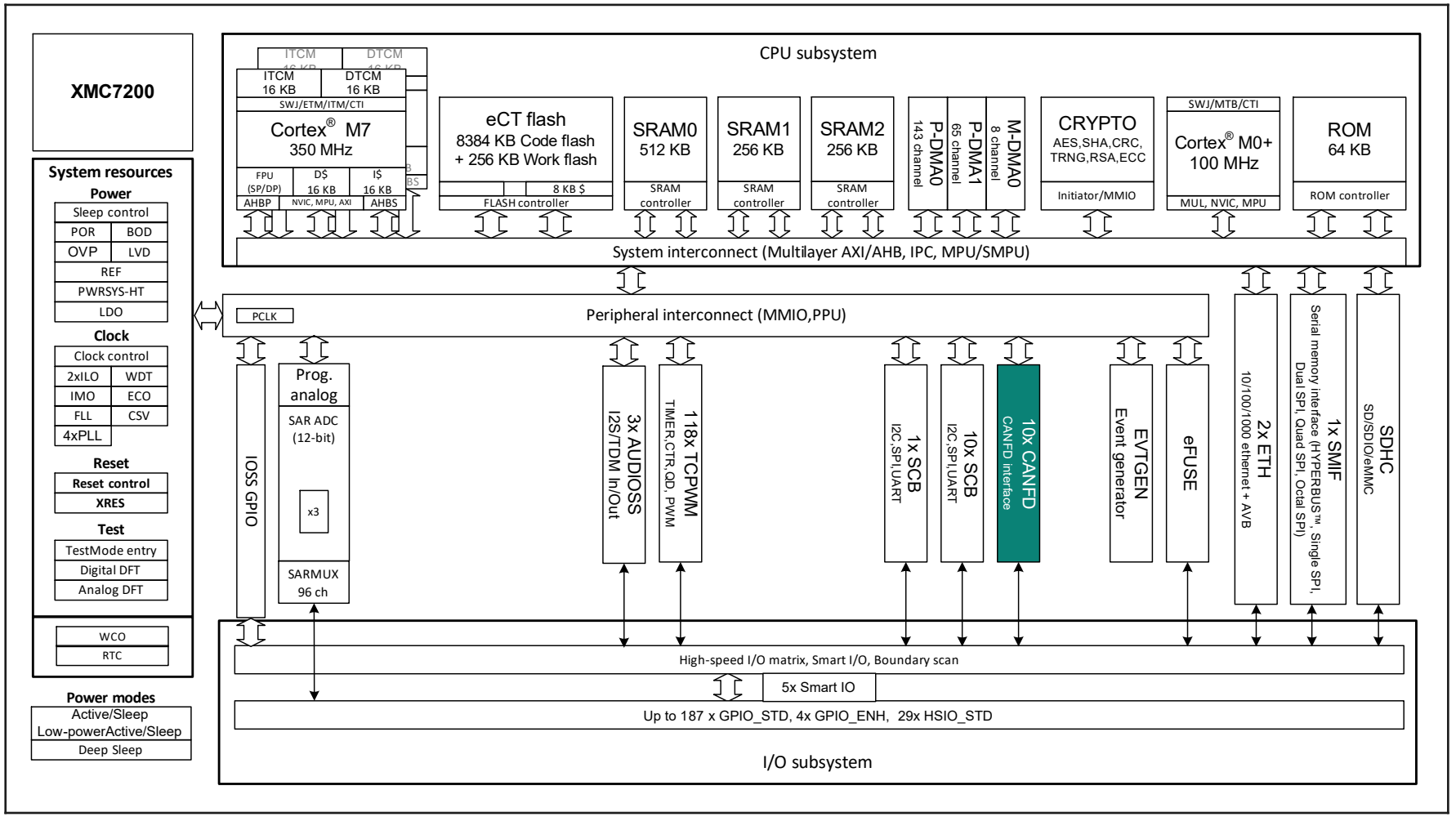
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Introduction to XMC7200-8M

CAN FD is part of the peripheral blocks.



Hint bar

See the XMC7000 architectural reference manual (CAN FD controller) chapter 6 and the registers reference manual for additional details.

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XMC7100 - 4M family



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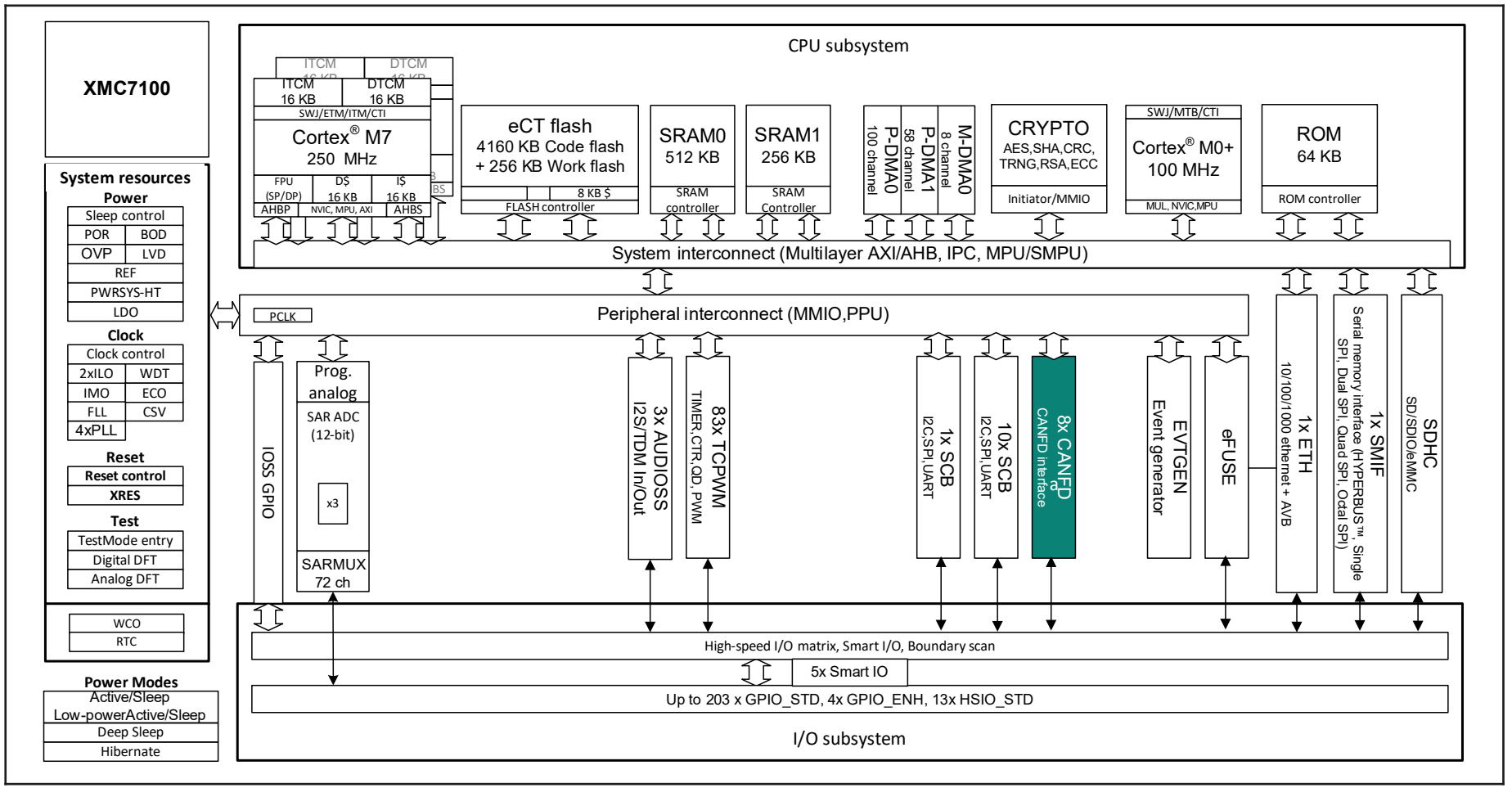
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Introduction to XMC7100-4M

CAN FD is part of the peripheral blocks.



Hint bar

See the CAN FD controller architectural reference manual chapter 24 and the register reference manual for additional details.

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CAN FD controller overview

Overview

- ISO11898-1:2015 standard
- Supports up to 8 Mbps

Features

- Flexible data rate (FD) with up to 64 data bytes per message
- Time-triggered (TT) communication on CAN (ISO 11898-4: 2004)
- Programmable loopback test mode
- Shared timestamp counter
- Acceptance filtering
- Receive FIFO top pointer
- Enables DMA access on the FIFO
- Shared message RAM (MRAM)
- Error-correcting code (ECC) generator and checker

Hint bar

See the datasheet and section 24 of the CAN FD controller architectural reference manual chapter for additional details.

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CAN FD controller architecture

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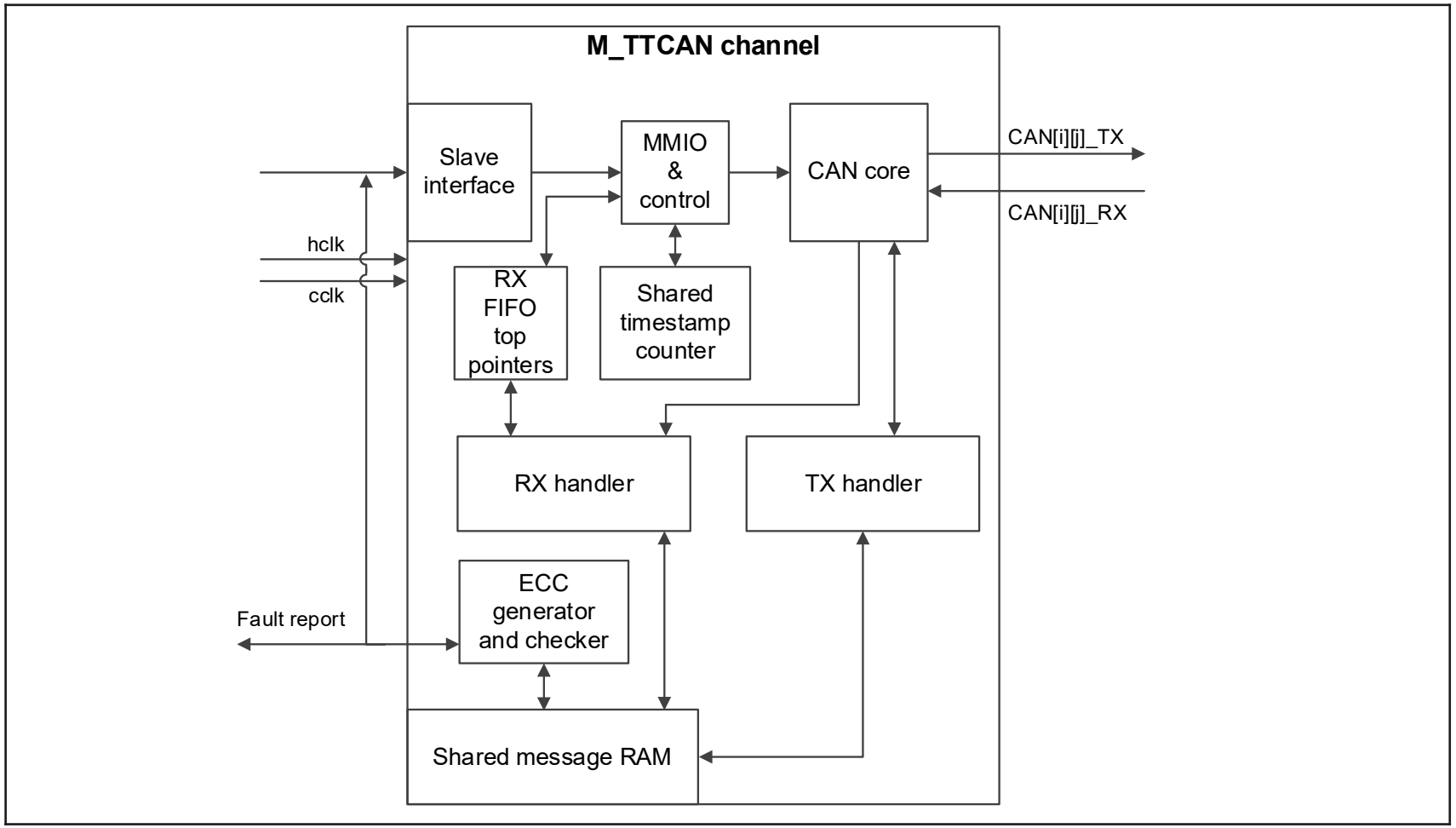
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Block diagram

CAN FD controller components.



Hint bar

See the section 24.2.1, Block diagram of the CAN FD controller architectural reference manual chapter for additional details.

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CAN core

Classic CAN and CAN FD operation

– Supports standard and extended ID

Transmitter delay compensation

– Supports the transmitter delay measurement and offset setting

Power down

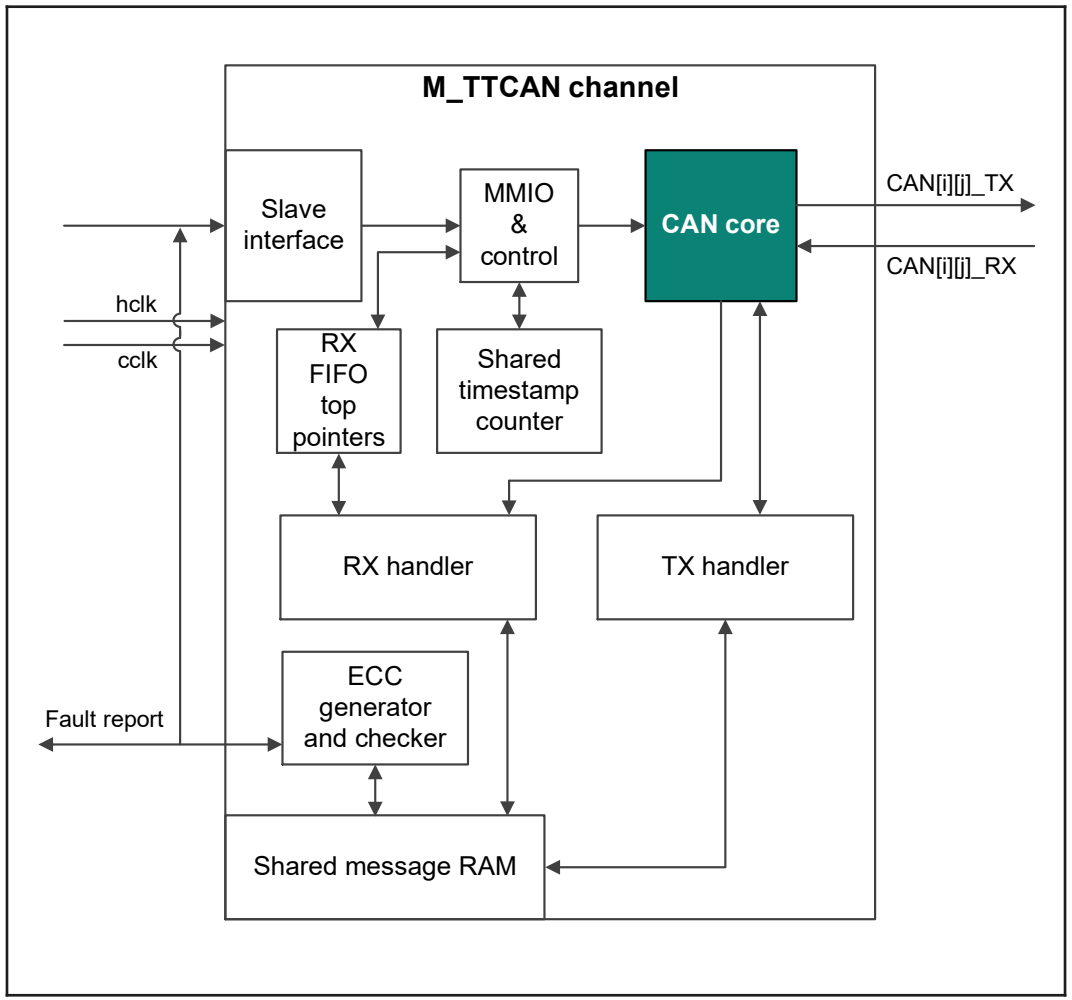
– Supports Sleep mode

Test mode

– Supports loopback mode

Interrupt

– Supports two types of interrupts



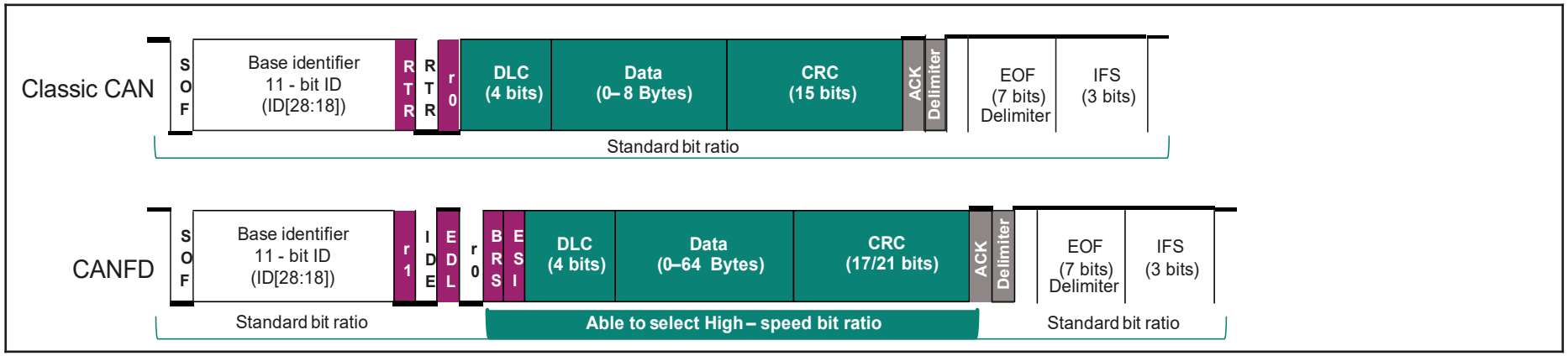
Hint bar

See the section 24.3, Functional description of the CAN FD controller architectural reference manual chapter for additional details.

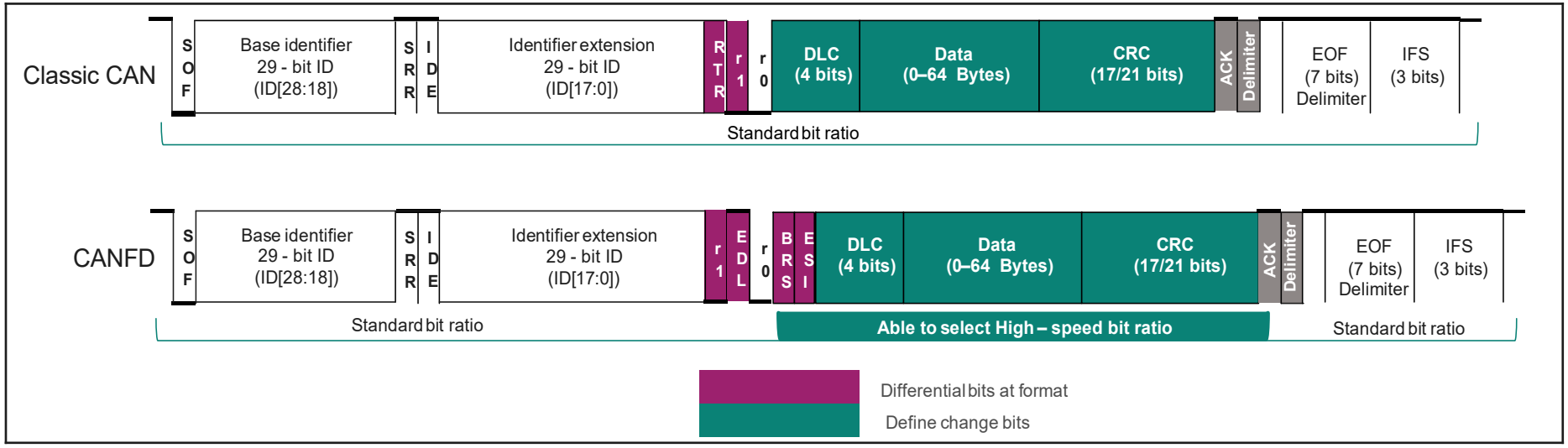
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Classic CAN and CAN FD operation

– Standard format (11-bit ID)



– Extended format (29-bit ID)



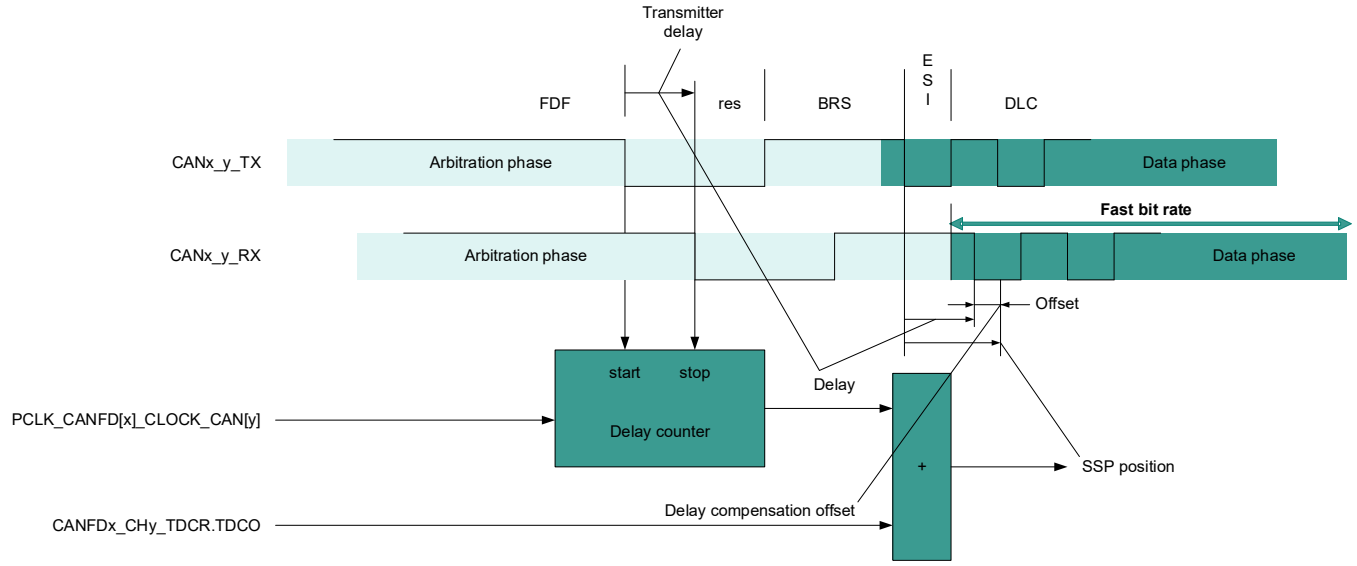
Hint bar

See the section 24.3, functional description of the CAN FD controller architectural reference manual and Register reference manual for additional details.

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Transmitter delay compensation

- Supports the transmitter delay measurement and offset setting
- When transmitting via CANx_y_TX, the CAN FD controller receives the transmitted data from its local CAN transceiver via CANx_y_RX
- The received data is delayed by the transmitter delay. If this delay is greater than TSEG1[1], a bit error is detected
- To enable a data phase bit time that is even shorter than the transmitter delay, the delay compensation is introduced



Hint bar

See the section 24.3.1.4, Transmitter delay compensation of the CAN FD controller architectural reference manual and register reference manual for additional details.

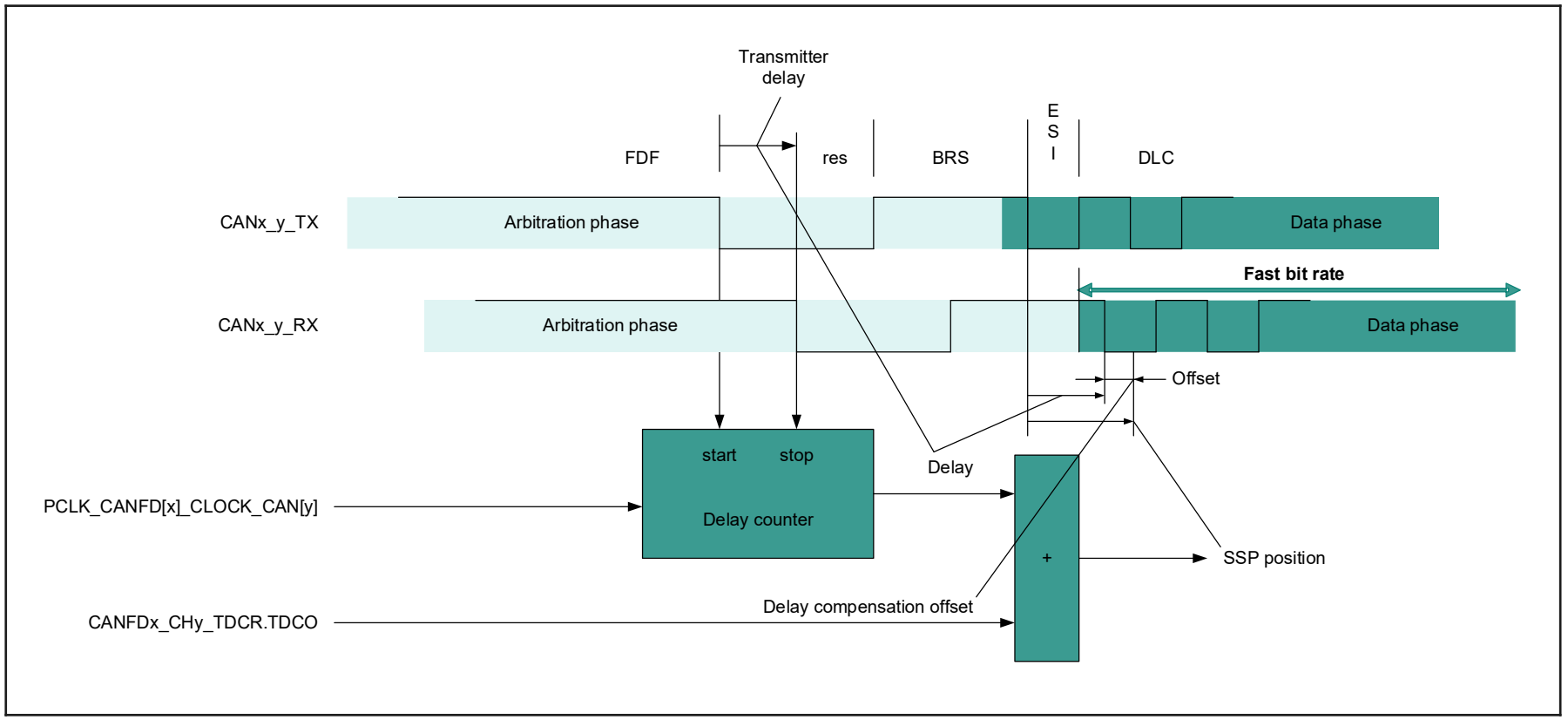
[1] Time segment before the sample point.

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Transmitter delay compensation (contd.)

Advantage

– Enables transmission with higher bit rates during the CAN FD data phase, independent of the delay of a specific CAN transceiver



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See the section 24.3.1.4, Transmitter delay compensation of the CAN FD controller architectural reference manual chapter and register reference manual for additional details.

[1] Time segment before sample point.

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Power down (Sleep mode)

- A clock provided to the CAN channel can be stopped by raising a clock stop request through the CTL.STOP_REQ bit
- After receiving an acknowledgment from the CAN channel, the hardware automatically stops the clock
- Clearing CTL.STOP_REQ allows exit from the Power down mode[1]
- All CAN configurations and MRAM except the timestamp counter are retained during Deep Sleep mode

Advantage

- Unlike older approaches, software does not have to wait for an acknowledgment and can be used for other functionalities
- Power down (stopping clock) reduces power consumption when the CAN bus is idle

Hint bar

See the section 24.3.1.8, Power down (Sleep mode) of the CAN FD controller architectural reference manual chapter and register reference manual for additional details.

[1] CTL.STOP_REQ must not be cleared before receiving an acknowledge from the CAN channel.

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Test mode

External loopback mode

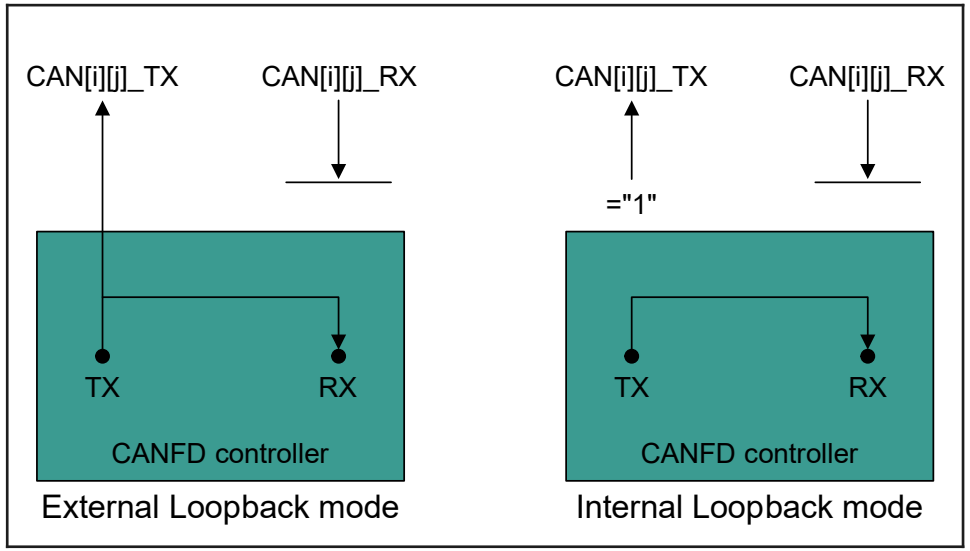
- Ignores acknowledgement errors (recessive bit sampled in the acknowledge slot of a data/remote frame) in loopback mode
- Performs an internal feedback from TX output to RX input
- Transmitted messages can be monitored at the CAN[i][j]_TX pin

Internal loopback mode

- Tests without affecting a running CAN system connected to the CAN[i][j]_TX and CAN[i][j]_RX pins

Use case

- CAN diagnosis without the influence of external ECU[1] by using the Internal loopback mode



Hint bar

See the section 24.3.1.9, Test mode of the CAN FD controller architectural reference manual chapter and register reference manual for additional details.

[1] Electrical control unit.

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Interrupt

- Each interrupt source in the M_TTCAN channel can be separately enabled or disabled using the IE register
- Each enabled interrupt from the channel can be routed either to the interrupt 0 or interrupt 1 line using the ILS and ILE registers. By default, all interrupts are routed to the interrupt 0 line

Hint bar

- See the section 24.2.3, Interrupt lines of the CAN FD controller architectural reference manual chapter and register reference manual for additional details
- The description of the IE register in the Register reference manual provides a list of all possible interrupt sources

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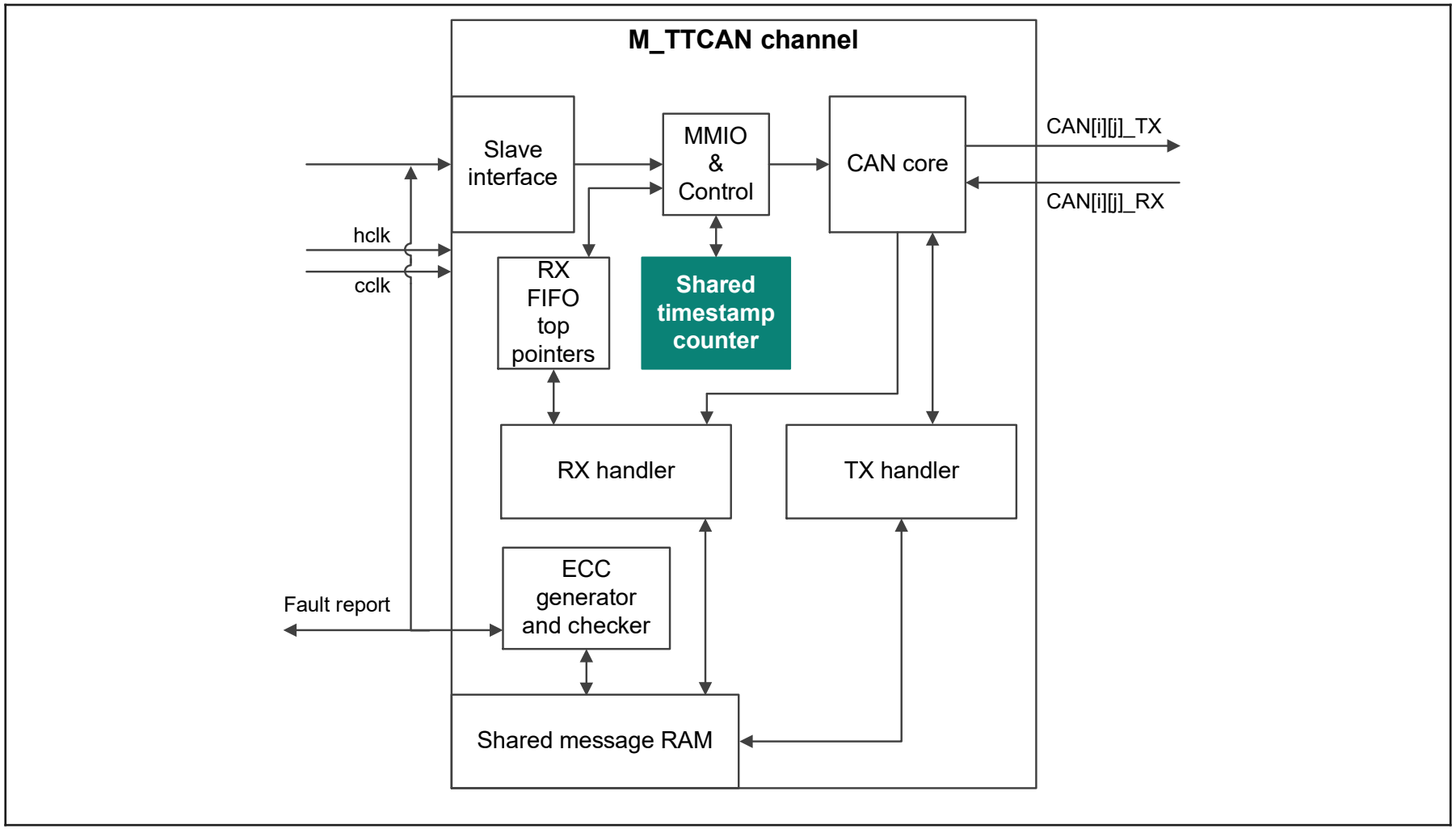
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Shared timestamp counter

Supports a 16-bit timestamp value.



Hint bar

See the section 24.3.2, Timestamp generation of the CAN FD controller architectural reference manual chapter for additional details.

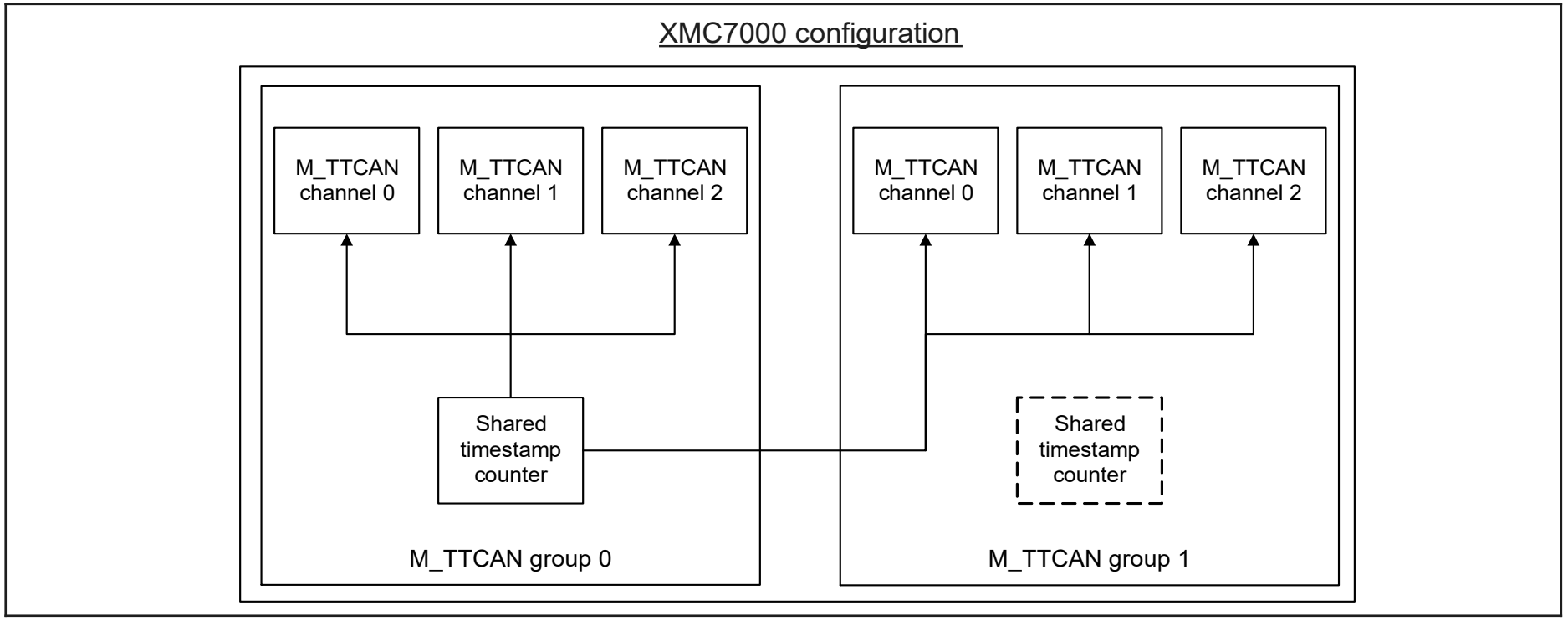
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Shared timestamp counter (contd.)

- The timestamp counter records a 16-bit timestamp value when messages are sent or received
- The captured timestamp value is stored in the respective buffer or FIFO element

Advantage

- To make event ordering global in the device, the 16-bit timestamp counter is shared among all M_TTCAN channels



Hint bar

See the section 24.3.2, Timestamp generation of the CAN FD controller architectural reference manual chapter and register reference manual for additional details.

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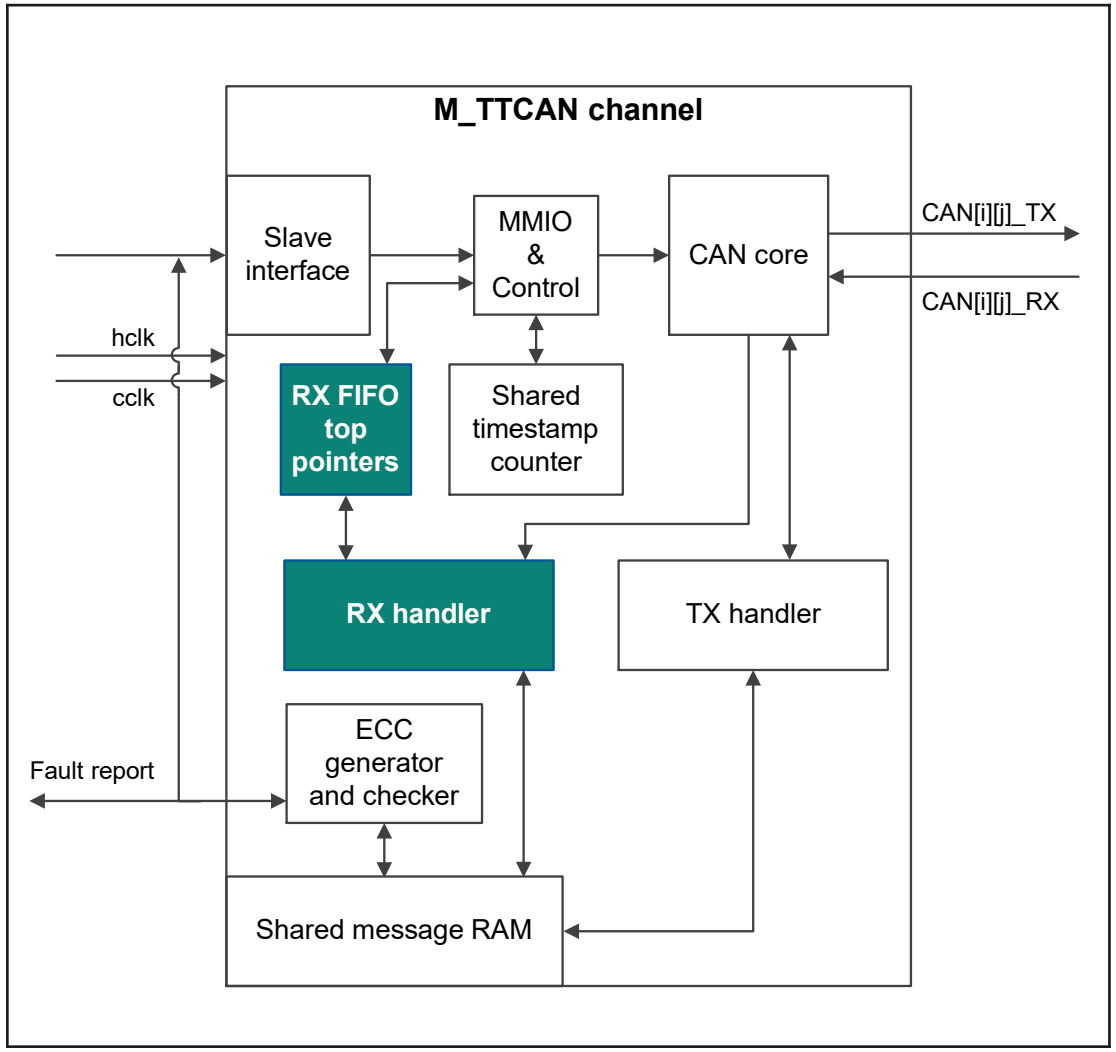
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RX handler

CAN FD controller components

- RX handler
  - Acceptance filtering
  - Dedicated RX buffers
  - RX FIFOs
- RX FIFO top pointers



Hint bar

See the section 24.3.4, RX handling of the CAN FD controller architectural reference manual chapter for additional details.

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Acceptance filtering

Two sets of acceptance filters

- Standard identifiers
- Extended identifiers

Features

- Each filter element[1] can be configured as follows:
  - Range filter (from - to)
  - Filter for one or two dedicated IDs
  - Classic bit mask filter
- Each filter element supports configurable acceptance or rejection filtering
- Each filter element can be enabled or disabled individually
- Filters are checked sequentially from element #0 until the first match

Hint bar

See the section 24.3.4.1, Acceptance filtering of the CAN FD controller architectural reference manual chapter and register reference manual for additional details.

[1] A filter element is a condition of the filtering list. There can be up to 192 filter elements.

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Dedicated RX buffers

Up to 64 dedicated RX buffers

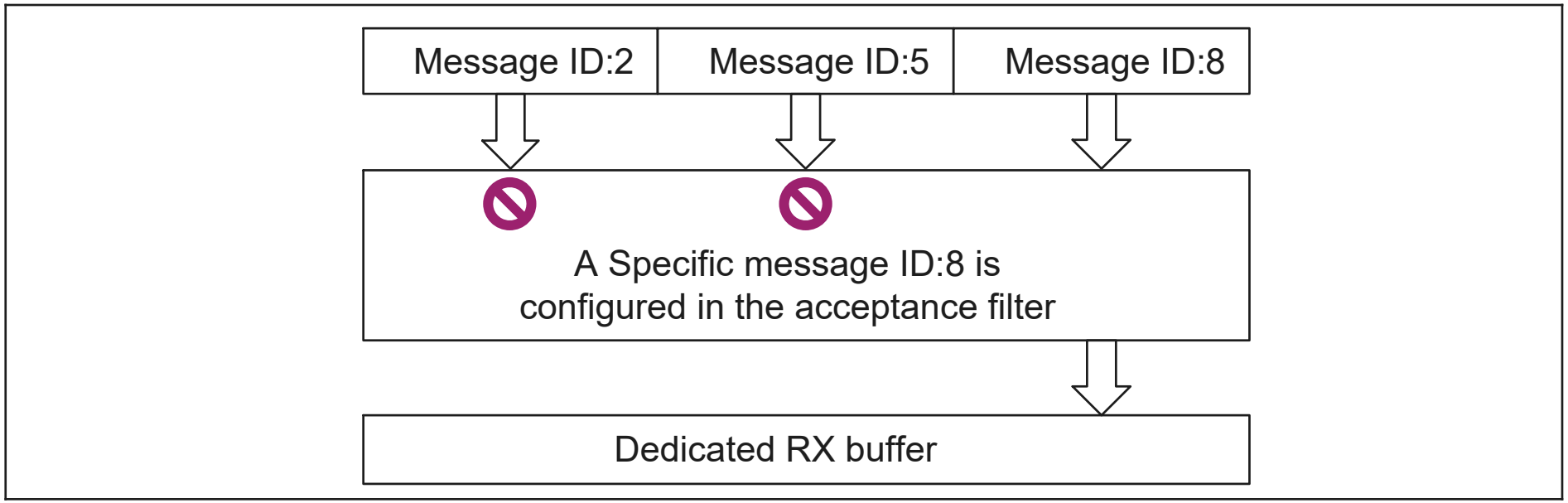
– After a received message is accepted by a filter element, the message is stored in the RX Buffer in the message RAM referenced by the filter element

Use case

– Receive only the specific message ID (8) with the dedicated RX buffer and acceptance filter

Advantage

– Accepts frames only with a specific message IDs



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See the section 24.3.4.3, Dedicated RX buffers of the CAN FD controller architectural reference manual chapter and register reference manual for additional details.

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RX FIFOs

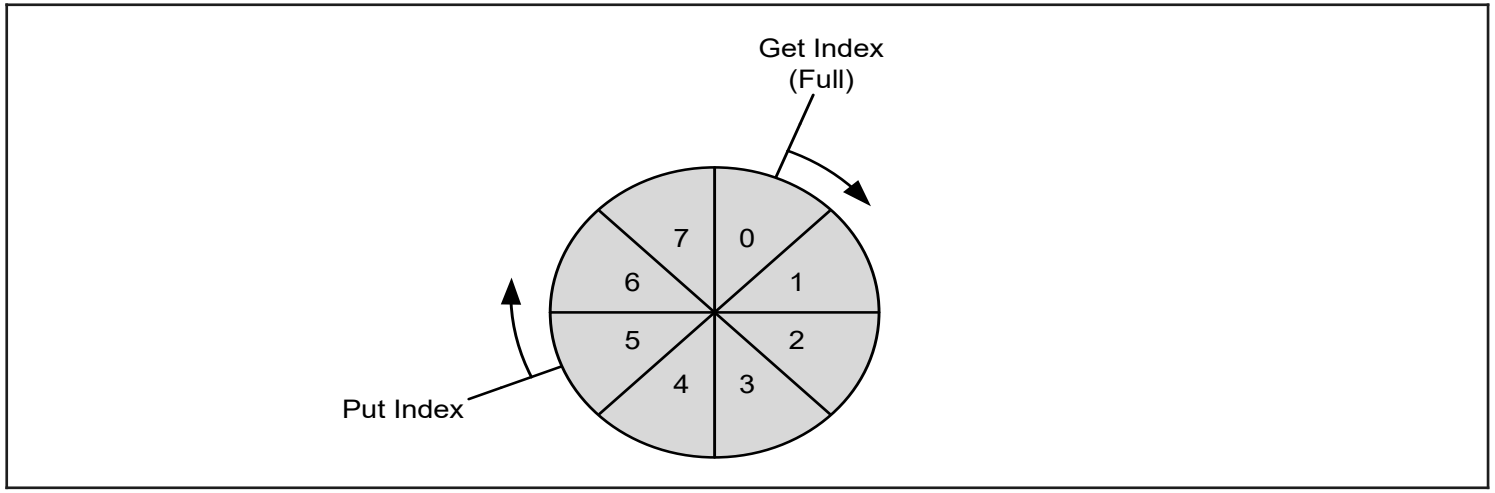
- RX FIFOs are configured to hold up to 64 elements each
- Received messages that pass acceptance filtering are transferred to the RX FIFO as configured by the matching filter element
- When the RX FIFO Put Index reaches the RX FIFO Get Index, the RX FIFO Full condition interrupt flag is set

Watermark interrupt

- To prevent RX FIFO overflow, the RX FIFO watermark interrupt is used

Use case

- The RX FIFO watermark interrupt flag is used to trigger DMA



Hint bar

See the section 24.3.4.2, RX FIFOs of the CAN FD controller architectural reference manual chapter and register reference manual for additional details.

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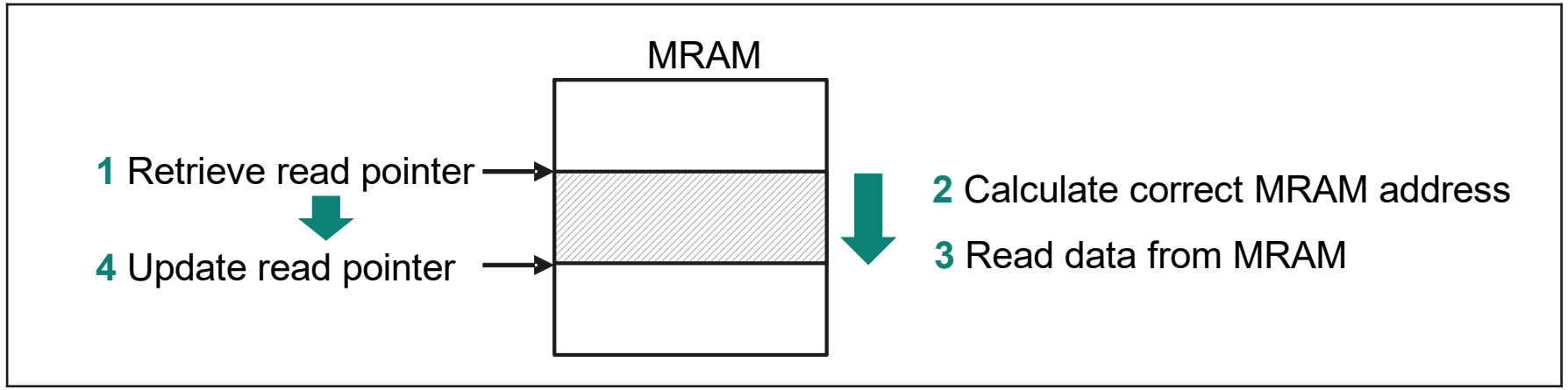
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RX FIFO top pointer

– Tracks the number of message data words read and updates the pointer information after reading the last word



– Provides a single location[1] to read the data

Advantages

– Reduces the software process to retrieve the read pointer, calculates the correct MRAM address, and updates the read pointer
– Reduces the bus load and latency
– Enables DMA on FIFOs

Hint bar

See the section 24.3.4.2, RX FIFOs of the CAN FD controller architectural reference manual chapter and register reference manual for additional details.

[1] RXFTOP0_DATA for RX FIFO0, RXFTOP1_DATA for RX FIFO1.

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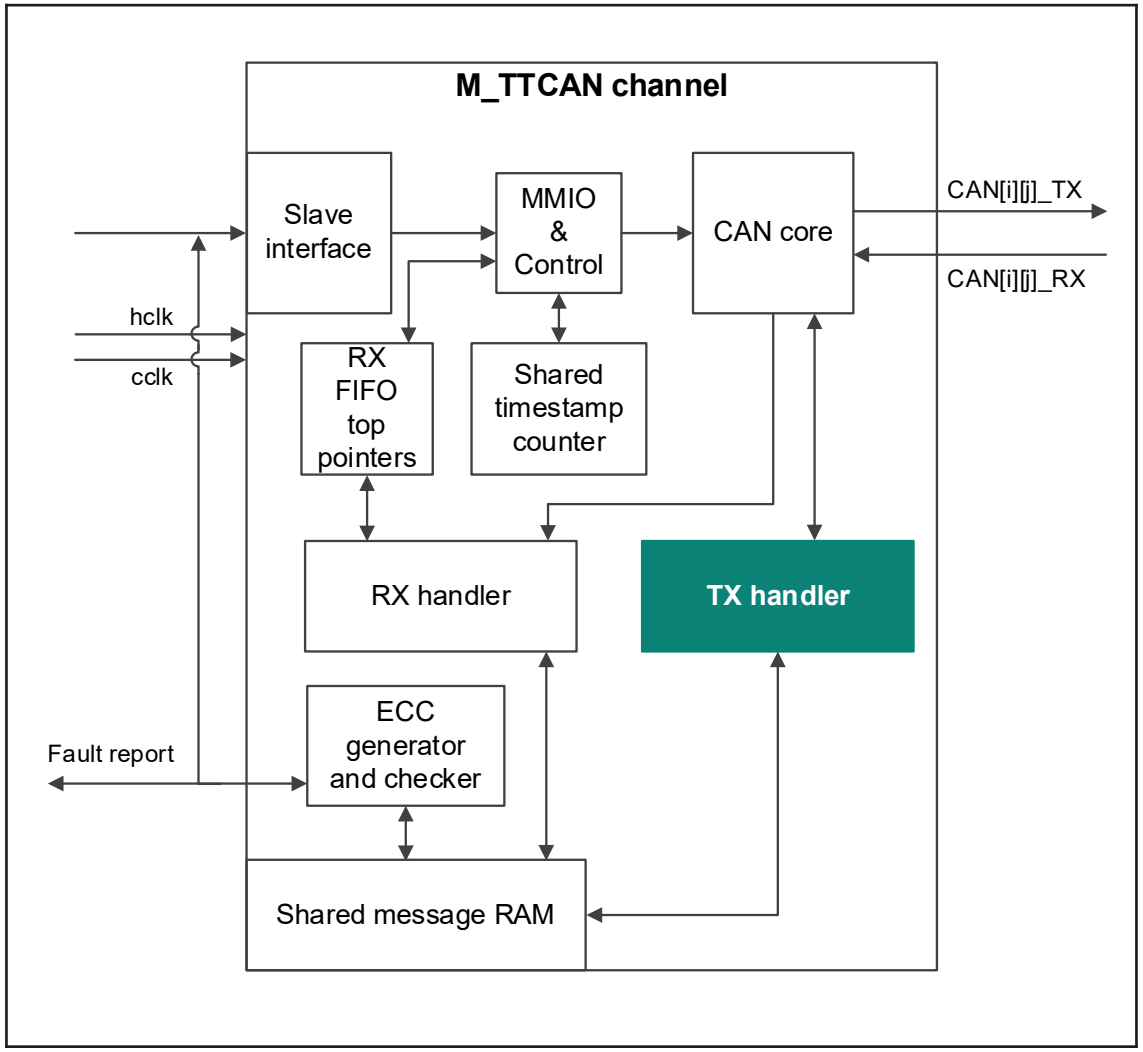
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TX handler

CAN FD TX handler controller component:

- Dedicated TX buffers
- TX FIFO and TX queue
- Mixed dedicated TX buffers/TX queue
- Mixed dedicated TX buffers/TX queue
- TX event FIFO



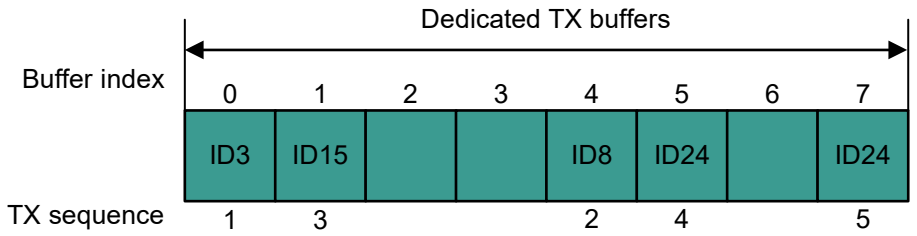
Hint bar

See the section 24.3.5, TX handling of the CAN FD controller architectural reference manual chapter for additional details.

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Dedicated TX buffers

- Each 32-bit dedicated TX buffer is configured with a specific Message ID
- If multiple TX buffers are configured with the same Message ID, the TX buffer with the lowest buffer number is transmitted first



- Dedicated TX buffers allocate “Element Size” 32-bit words in the MRAM

TX buffer/FIFO/queue Element Size

Data field [bytes]	Element size [RAM words]
8	4
12	5
16	6
20	7
24	8
32	10
48	14
64	18

Hint bar

See the section 3.5.2, Dedicated TX buffers of the CAN FD controller architectural reference manual chapter and register reference manual (TXESC.TBDS) for additional details.

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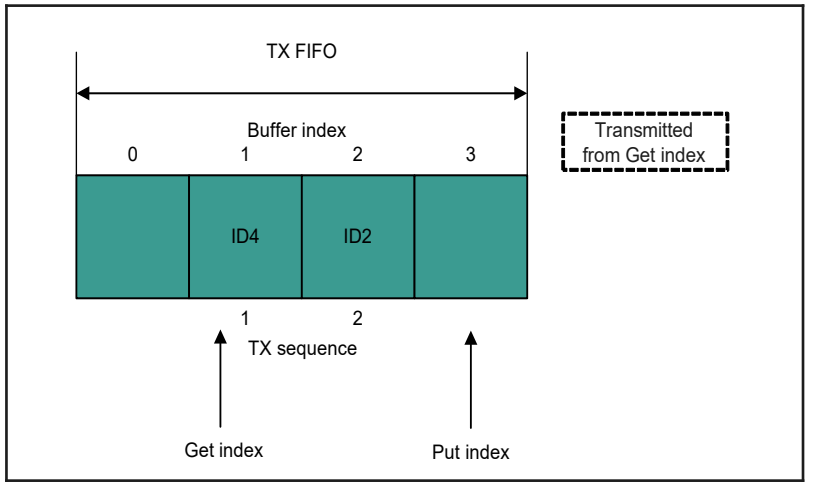
TX FIFO and TX queue

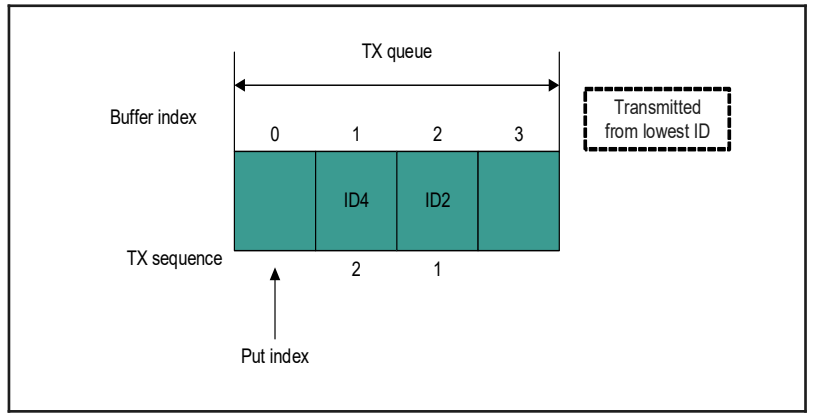
TX FIFO

- Messages stored in TX FIFO are transmitted starting with the message referenced by the Get Index[1]
- After each transmission, the Get Index is incremented cyclically until the TX FIFO is empty

TX Queue

- Messages stored in the TX queue are transmitted starting with the message with the lowest Message ID (highest priority)
- If multiple TX queues are configured with the same Message ID, the TX queue with the lowest buffer number is transmitted first





Hint bar

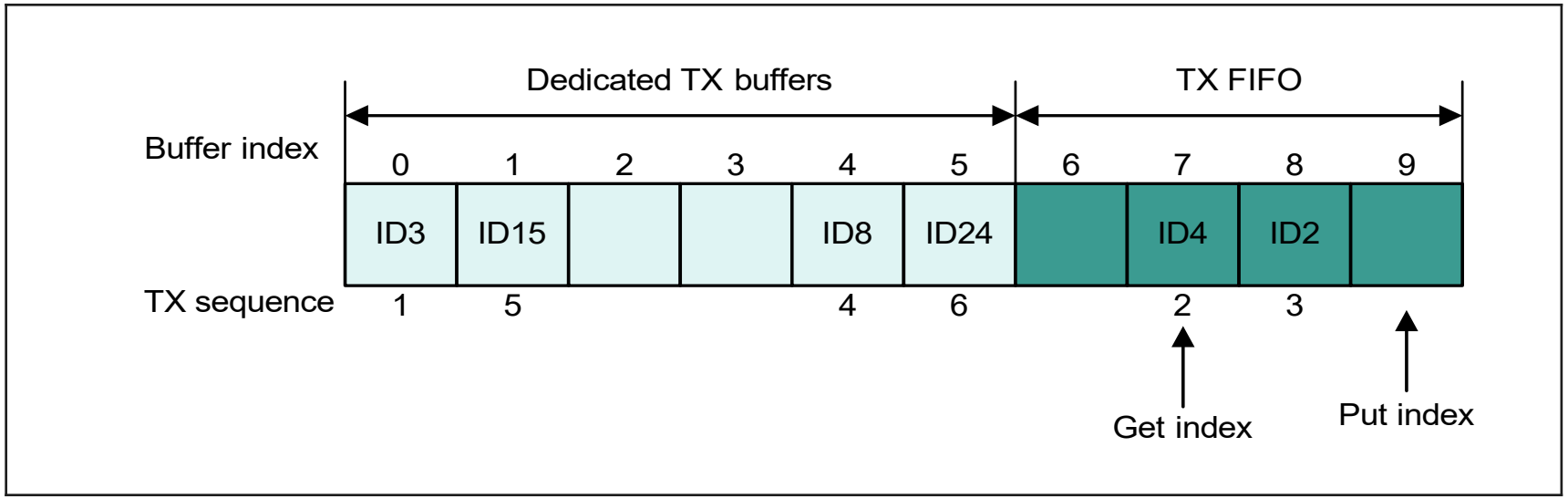
See the section 24.3.5.3 (TX FIFOs), 24.3.5.4 (TX queue) of the CAN FD controller architectural reference manual chapter and register reference manual for additional details.

[1] TXFQS.TFGI

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Mixed dedicated TX buffers/TX FIFO

– The MRAM TX buffer section is subdivided into a set of dedicated TX buffers and TX FIFO



TX prioritization

– Scan dedicated TX buffers and the oldest pending TX FIFO buffer (referenced by Get index)

– The TX buffer with the lowest message ID has the highest priority and is transmitted next

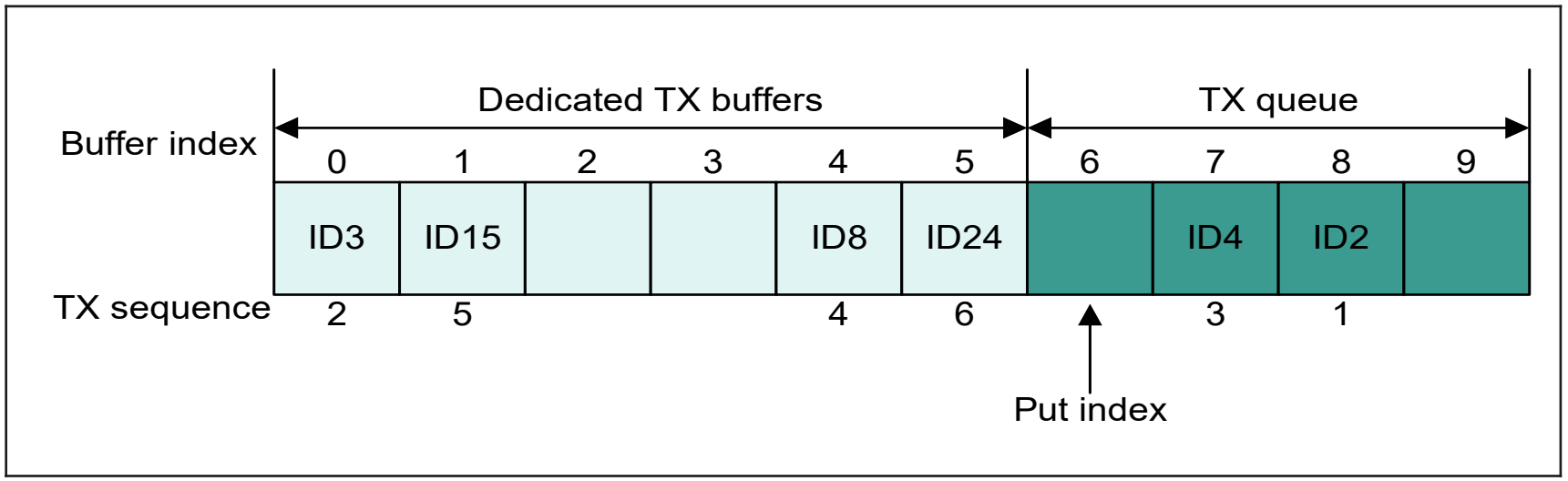
Hint bar

See the section 24.3.5.5, Mixed dedicated TX buffers/TX FIFO of the CAN FD controller architectural reference manual chapter and register reference manual for additional details.

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Mixed dedicated TX buffers/TX queue

– The MRAM TX buffer section is subdivided into a set of dedicated TX buffers and a TX queue



TX prioritization

– Scan all TX buffers with an activated transmission request

– The TX buffer with the lowest Message ID has the highest priority and is transmitted next

Hint bar

See the section 24.3.5.6, Mixed dedicated TX buffers/TX queue of the CAN FD controller architectural reference manual chapter and register reference manual for additional details.

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TX Event FIFO

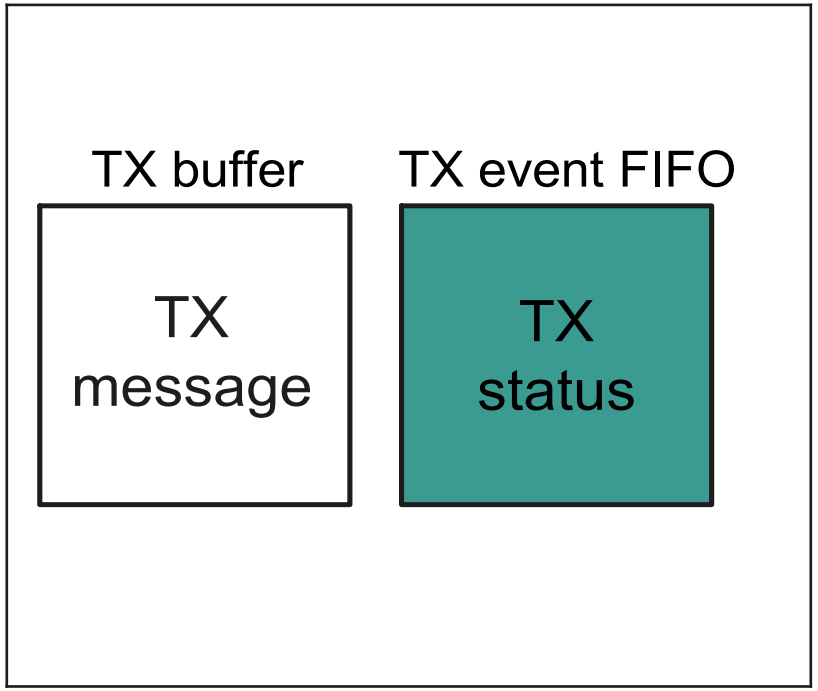
- Message ID and timestamp are stored in the TX Event FIFO element
- Configured to a maximum of 32 elements

Use case

- A TX buffer holds only the message to be transmitted, while the transmit status is stored separately in the TX Event FIFO

Advantage

- When operating a dynamically managed transmit queue, a TX buffer can be used for a new message immediately after successful transmission
- It is not necessary to save transmit status information from a TX buffer before overwriting that TX buffer



Hint bar

See the section 24.3.5.8, TX event handling of the CAN FD controller architectural reference manual chapter and register reference manual for additional details.

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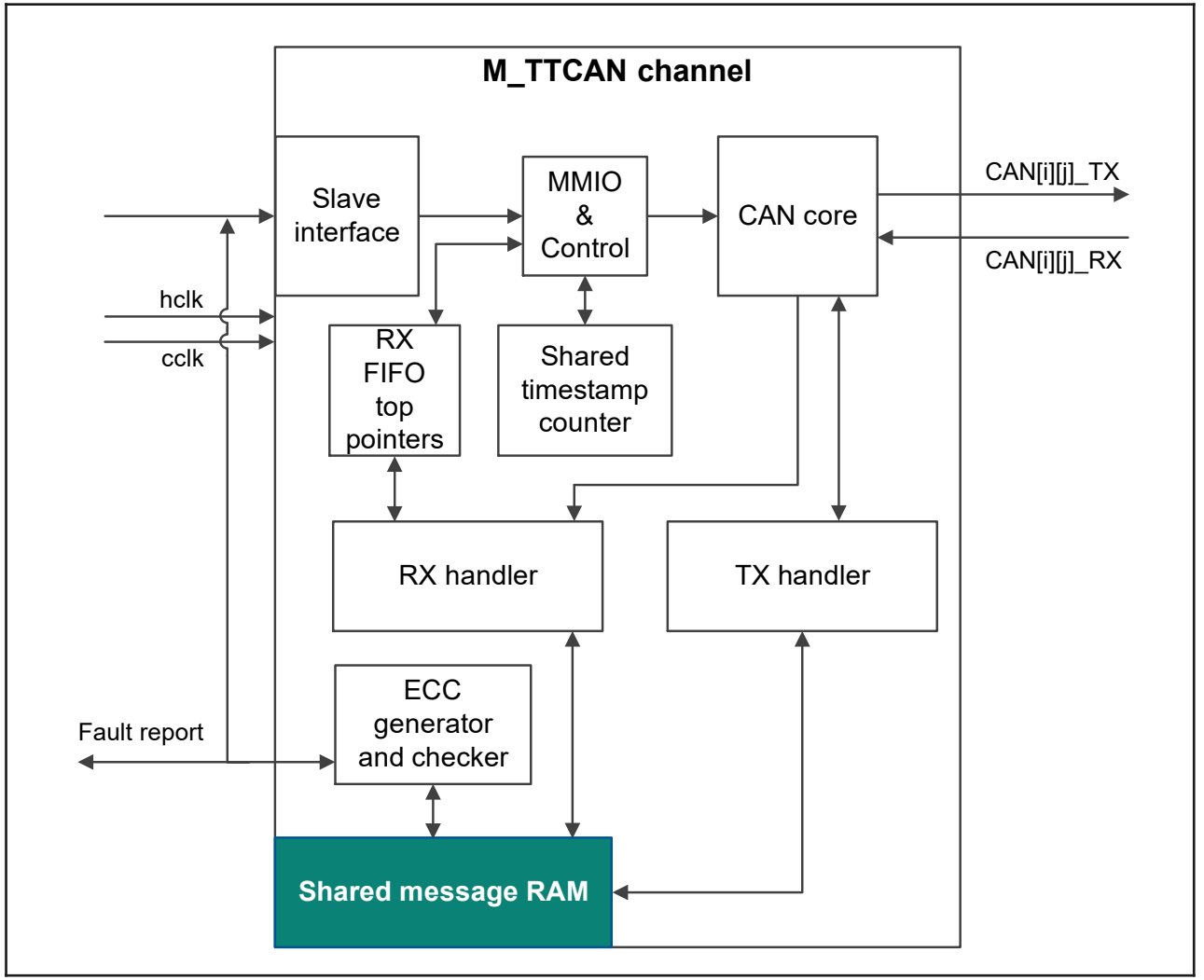
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Shared message RAM

CAN FD controller components

- Shared message RAM
  - Message RAM configuration
- The following slides provide more information on shared message RAM



Hint bar

See the section 24.4, Message RAM of the CAN FD controller architectural reference manual chapter and Register reference manual for additional details.

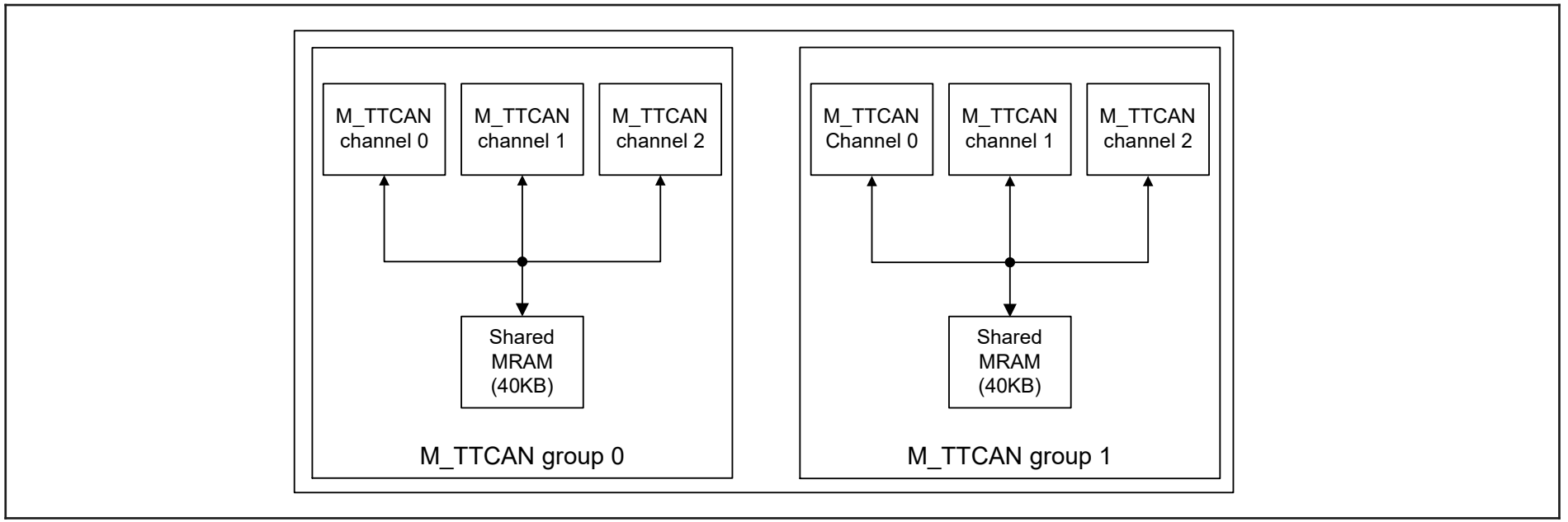
Note: Message RAM cannot be used for system RAM.

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Shared message RAM (contd.)

Message RAM in the XMC7000 family devices is shared among multiple M_TTCAN channels in the M_TTCAN group

XMC7000 Message RAM[1]



Advantage

– Each M_TTCAN channel in the module is configured to require the message RAM according to the needs of the application

Hint bar

See the section 24.4, Message RAM of the CAN FD controller architectural reference manual chapter and register reference manual for additional details.

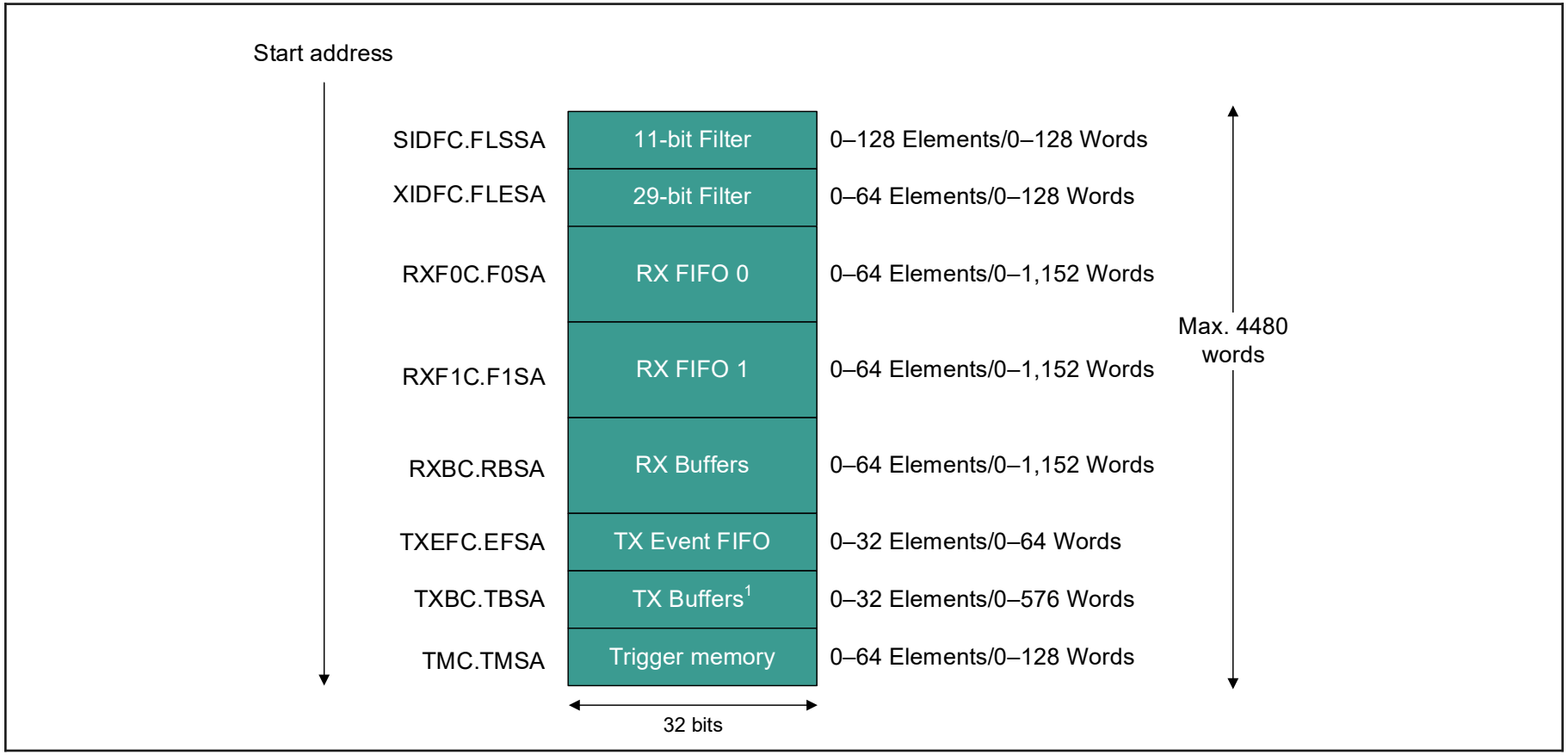
Note: Message RAM cannot be used for system RAM.

[1] XMC7000: 40 KB among five channels

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Message RAM configuration

- Filter and messages are managed separately
- Sent and received messages are managed separately



Hint bar

See the section 24.4.1, Message RAM configuration of the CAN FD controller architectural reference manual chapter and register reference manual for additional details.

[1] The TX buffer section can be configured to hold dedicated TX buffers as well as a TX FIFO/TX queue.

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Turning message RAM OFF

- Message RAM can be turned off to save power by setting the CTL.MRAM_OFF bit
- Default value of this bit is ‘0’ and MRAM is retained in this configuration during Deep Sleep power mode
- All M_TTCAN channels must be powered down before setting the MRAM_OFF bit

Hint bar

See the section 24.4.9, Message RAM OFF of the CAN FD controller architectural reference manual chapter and register reference manual for additional details.

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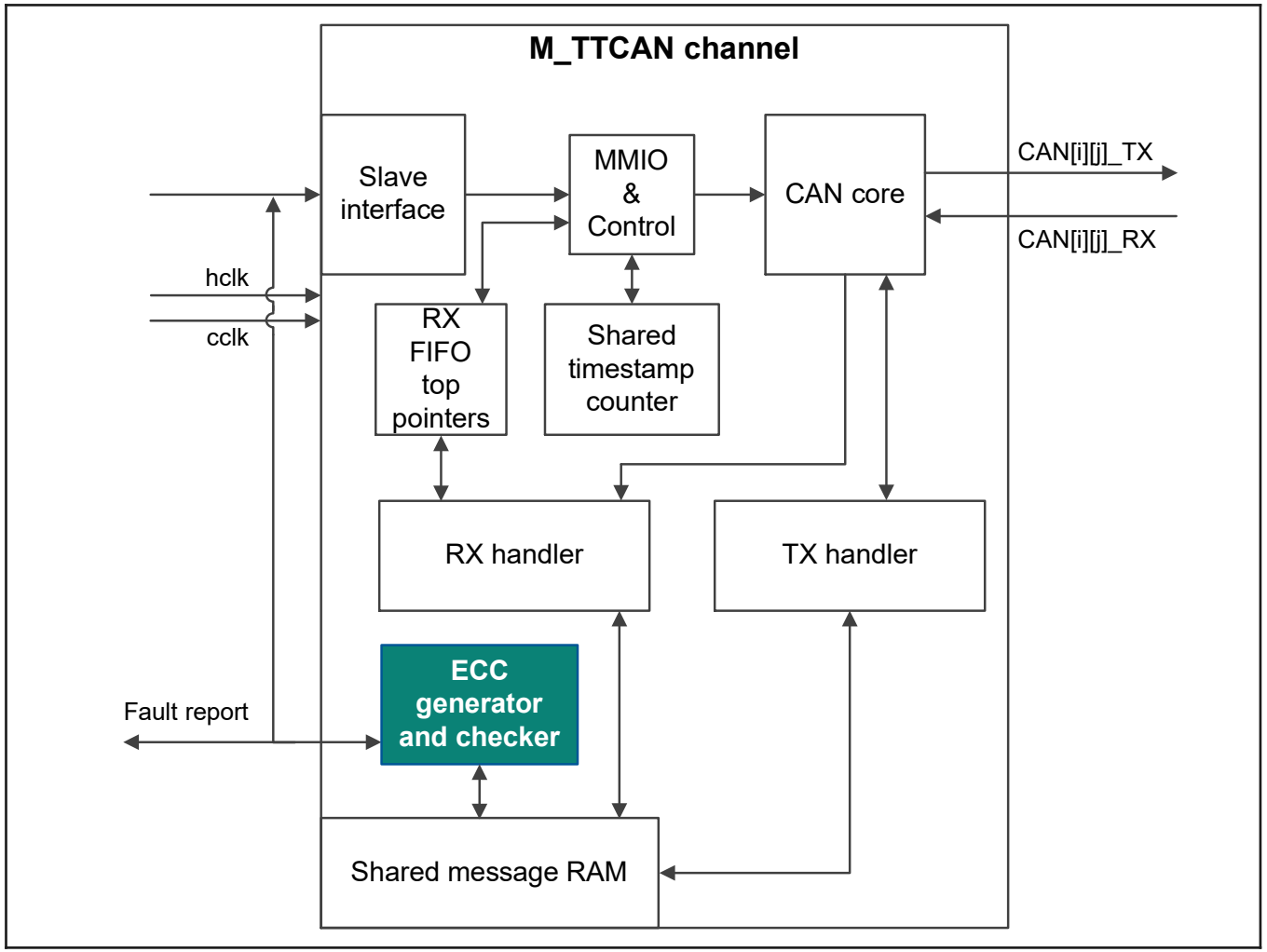
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ECC generator and checker (1/3)

CAN FD components

- ECC generator and checker
  - Single-error correction
  - Double-error detection
  - ECC-error injection
  - Address error



Hint bar

See the section 24.4.8, ECC for message RAM of the CAN FD controller architectural reference manual chapter and register reference manual for additional details.

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ECC generator and checker (2/3)

Single-bit error correction and double-bit error detection (SECDED)

- SEC report action:
  - Report to the fault subsystem

DED report action

- Report to the master
  - In the case of an AHB master, a bus error occurs
  - In the case of an M_TTCAN channel, the M_TTCAN channel shuts down immediately
- Interrupt
- Reports to the fault subsystem

Software ECC error injection support

Use case

- SEC report: Not needed because a single-bit error is corrected automatically
- DED report: Use for failsafe operation, such as stop system control
- ECC error injection: Use for initial diagnosis of ECC before application running

Hint bar

See the section 24.4.8, ECC for message RAM of the CAN FD controller architectural reference manual chapter and register reference manual for additional details.

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ECC generator and checker (3/3)

- Address error
- Detects when TTCAN or MCU is trying to access out-of-range MRAM[1]
- Unlike ECC errors, this can happen for both writes and reads

Report action

- Read from M_TTCAN master
  - To prevent sending corrupt data, shutdown the M_TTCAN channel immediately
  - Interrupt
- Read from the AHB interface
  - Bus error
- Any case (read, write, and any master)
  - Report to the fault subsystem

Advantage

- Makes software debugging easier

Hint bar

See the section 24.4.8.3 of the CAN FD controller architectural reference manual chapter and register reference manual for additional details.

[1] XMC7000: 40KB

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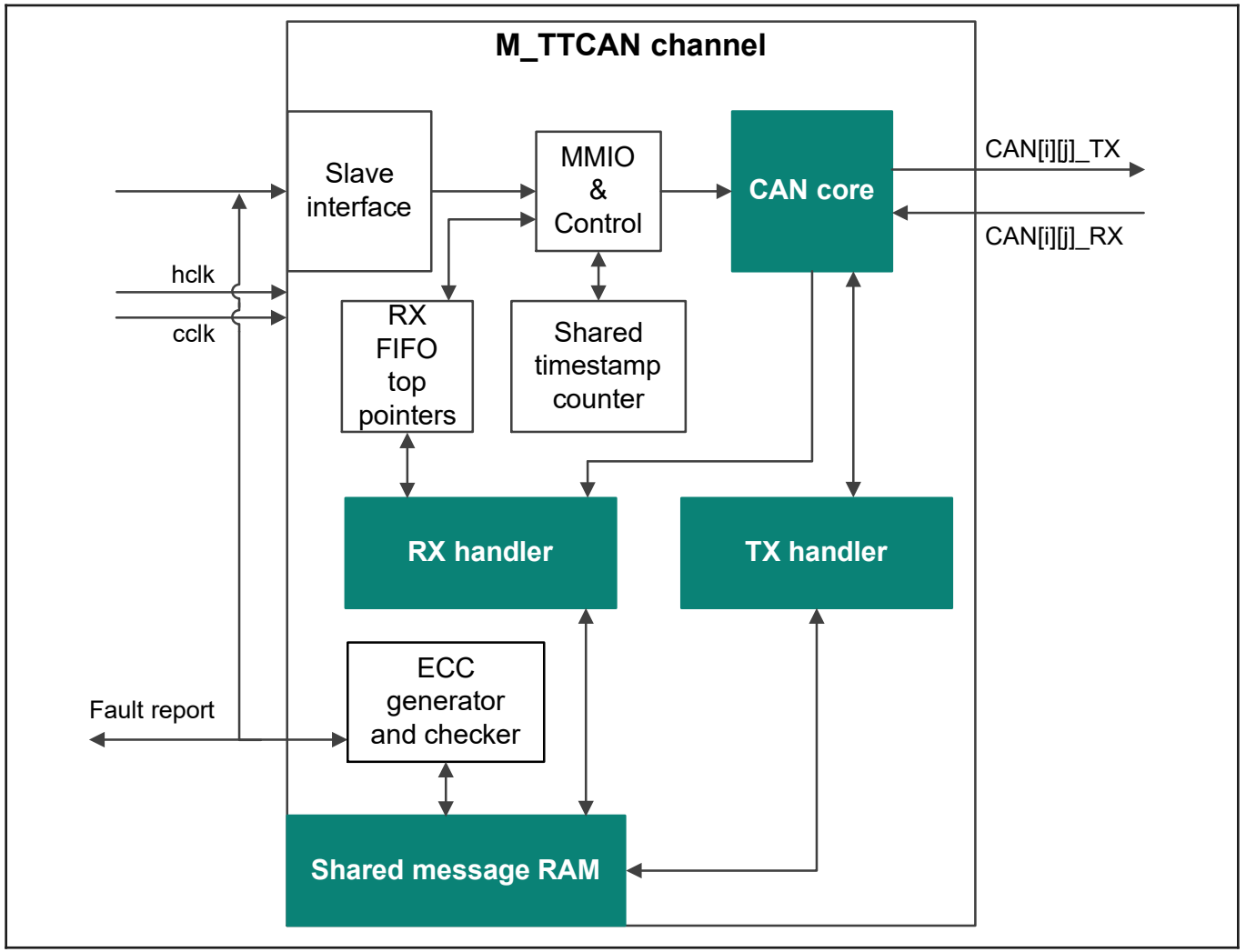
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TTCAN channel operation

- Reference message
- Message scheduling
- Trigger memory
- Schedule initialization
- TTCAN gap control
- Stopwatch
- TTCAN error level
- TTCAN message handling



Hint bar

See the section 24.5, TTCAN operation of the CAN FD controller architectural reference manual chapter and register reference manual for additional details.

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Reference message

- A data frame characterized by a specific CAN identifier
- Received and accepted by all nodes except the time master (sender of the reference message)
- Level 1
  - Data length must be at least one
- Level 0, 2
  - Data length must be at least four
- Extended by other data up to the sum of eight CAN data bytes
- All bits of the identifier except the three LSBs characterize the message as a reference message
- The last three bits specify the priorities of up to eight potential time masters

Hint bar

See the section 24.5.1, Reference message of the CAN FD controller architectural reference manual chapter for additional details.

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Message scheduling

- TTOCF.TM controls whether M_TTCAN operates as a potential time master or as a time slave
- If it is a potential time master, the three LSBs of the reference message's identifier, TTRMC.RID, define the master priority as follows:
  - 0: Highest priority
  - 7: Lowest priority

Hint bar

See the section 24.5.2.2, Message scheduling of the CAN FD controller architectural reference manual chapter and register reference manual for additional details.

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Trigger memory

- Trigger memory is a part of the Message RAM
- Stores up to 64 trigger elements
- A trigger memory element consists of:
  - Time mark (TM)
  - Cycle code (CC)
  - Trigger type (TYPE)
  - Filter type (FTYPE)
  - Message number (MNR)
  - Message status count (MSC)
  - Time mark event internal (TMIN)
  - Time mark event external (TMEX)
  - Asynchronous serial communication (ASC)

Hint bar

See the section 24.5.2.3, Trigger memory and 24.4.7, Trigger memory element CAN FD controller architectural reference manual chapter for additional details.

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TTCAN schedule initialization

- Synchronization to M_TTCAN’s message schedule starts when CCCR.INIT is reset
- M_TTCAN operates strictly time-triggered (TTOCF.GEN = ‘0’) or external event-synchronized time-triggered (TTOCF.GEN = ‘1’)
- All nodes start with cycle time zero at the beginning of their trigger list with TTOST.SYS = 00 (out of synchronization), no transmission is enabled except the reference message

Hint bar

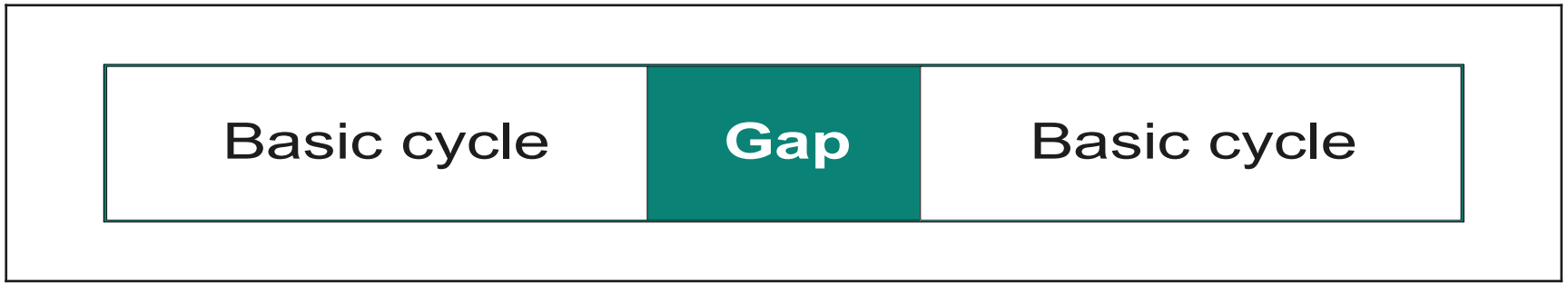
See the section 24.5.2.4, TTCAM schedule initialization of the CAN FD controller architectural reference manual chapter and register reference manual for additional details.

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TTCAN gap control

All functions related to gap control apply only when M_TTCAN is operated in external event-synchronized time-triggered mode (TTOCF.GEN = ‘1’)

- TTCAN message schedule can be interrupted by inserting gaps between basic cycles of the system matrix
- During a gap, all transmissions are stopped, and the CAN bus remains idle
- A gap is finished when the next reference message starts a new basic cycle
- A gap starts at the end of a basic cycle that itself was started by a reference message with bit Next_is_Gap = ‘1’



Use case

- Gaps are initialized by the current time master

Hint bar

See the section 24.5.3, TTCAN gap control of the CAN FD controller architectural reference manual chapter and register reference manual for additional details.

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Stopwatch

- The stopwatch function enables capturing of M_TTCAN internal time values (local time, cycle time, or global time) triggered by an external event
- To enable the stopwatch function, the application program must first define local time, cycle time, or global time as the stopwatch source via TTOCN.SWS

Hint bar

See the section 24.5.4, Stop watch of the CAN FD controller architectural reference manual chapter and register reference manual for additional details.

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TTCAN error level

ISO 11898-4 specifies four levels of error severity, as follows:

- **S0: No error**
- **S1: Warning**
- Only notification of application; reaction is application-specific
- **S2: Error**
- Notification of application, all transmissions in exclusive or arbitrating time windows are disabled (no data or remote frames may be started)
- The potential time masters transmit reference messages with the reference trigger offset TTOST.RTO set to the maximum value of 127
- **S3: Severe error**
- Notification of application, all the CAN bus operations are stopped (transmission of dominant bits is not allowed), and CCCR.MON is set
- The S3 error condition remains active until the application updates the configuration (set CCCR.CCE)

Hint bar

See the section 24.5.7, TTCAN error level of the CAN FD controller architectural reference manual chapter and register reference manual for additional details.

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TTCAN message handling

Reference message

- For potential time masters, the identifier of the reference message is configured via TTRMC.RID
- No dedicated TX buffer is required for transmission of the reference message
- When a reference message is transmitted, the first data byte (TTCAN Level 1) corresponding to the first four data bytes (TTCAN Level 0 and Level 2) provided by the Frame Synchronization Entry (FSE)[1]

Message reception

- Message reception is done via the two RX FIFOs, similar to event-driven CAN communication

Message transmission

- For time-triggered message transmission, M_TTCAN supplies 32 dedicated TX buffers
- TX FIFO or TX queue is not available when M_TTCAN is configured for time-triggered operation (TTOCF.OM = 01 or 10)

Hint bar

See the section 24.5.8, TTCAN message handling of the CAN FD controller architectural reference manual chapter and register reference manual for additional details.

[1] Frame synchronization event (FSE) occurs at the sample point of each Start-of-Frame (SoF) bit.

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Revision history

Document revision	Date	Description of change
**	2022-04-05	Initial release
*A	2025-11-05	Migrated to the latest empower training presentation template

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