XMC4000 Errata

32-bit Arm® Cortex®-M4

About this document

Scope and purpose

This document describes the errata for XMC4000 product family.

Intended audience

This document is intended for the users who plan to use XMC4000 devices in an application.

Table of contents

About this document 1
Table of contents 2
1 Errata 3
1.1 Cold start issue in XMC44xx/XMC45xx devices 3
Revision history 5
Disclaimer 6

1 Errata

This document describes the errata for XMC4000 product family detailing the problem, root cause, and a recommended software workaround.

For more details, contact Infineon support.

1.1 Cold start issue in XMC44xx/XMC45xx devices

Problem statement

Under certain low-temperature conditions, a small percentage (less than 0.2%) of XMC44xx and XMC45xx devices may fail to start correctly during the initial power-up (cold start).

Affected devices

- XMC4400
- XMC4402
- XMC4500
- XMC4502
- XMC4504

Technical description

The XMC4000 family includes a memory subsystem with an internal Prefetch Unit (PFU) designed to accelerate program execution from flash memory by providing an instruction buffer (cache). Flash memory can be accessed either directly or through the PFU using different address ranges for the same physical flash array.

During normal startup, the first read access to the cached flash area (typically starting at 0x0800 0000) transfers instructions from flash to the instruction buffer. Simultaneously, the CPU executes the first instruction directly, bypassing the buffer. Under certain conditions during initial power-up (cold start, typically around -30°C…0°C), corrupted data may be written to the instruction buffer during the first transfer of instructions from a cached flash address into the instruction buffer of the PMU. If these corrupted instructions are later fetched and executed, the system may exhibit erroneous behavior during boot.

Root cause

The corruption occurs during the initial transfer of instructions to the PFU after power-up. This can lead to various faults such as Memory Management Fault, Hard Fault, Bus Fault, or Usage Fault, preventing proper system startup.

Scope of impact

- Memory bytes are corrupted only during the initial loading of instructions to cache line after power-up
- Subsequent transfers to the same cache line are unaffected
- Code executed from non-cached space (0x0C00 0000) is not impacted
- The issue does not occur after a system reset or external reset via the PORST pin

Workaround

To mitigate the issue, the entire memory of the PFU should be filled with a sequence of Jump and NOP instructions during the execution of the startup file. The sequence must be structured so that the Jump instructions are always the first in each row and are executed directly (bypassing the Prefetch Buffer), while the NOP instructions serve only to fill the Prefetch Buffer without being executed. After this initialization, the Prefetch Buffer will be replaced by normal program code during subsequent execution.

During a Cache Miss (i.e., when an instruction to be fetched is not yet present in the instruction buffer), a complete cache line is loaded from Flash starting at the address of the requested instruction. At the same time, the first instruction of this transfer is presented directly to the CPU and executed, without being read from the PFU buffer. By preloading the instruction buffer with a sequence of JMP and NOP commands—where only the first JMP instruction is executed, and the potentially corrupted NOP instructions are never executed, the entire instruction cache can be initialized without executing code from it. This approach prevents any adverse effects of corrupted PFU data during the first write operation. After this initial operation, normal program flow resumes, and the instruction buffer is overwritten with valid program code in the usual manner.

Because the proposed workaround requires filling the entire instruction cache without executing code from it, flash memory equivalent to the instruction buffer size (i.e., 4 KB) is necessary.

The only impact of this workaround is an additional 4 KB of Flash memory usage.

Fix status

The next revision of the `mtb-xmclib-cat3-4.7.0` library will include this fix within the startup files.

Revision history

Document revision	Date	Description of changes
V1.0	2025-12-04	Initial release

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2025-12-04

Published by

Infineon Technologies AG

81726 Munich, Germany

© 2025 Infineon Technologies AG

All Rights Reserved.

Do you have a question about any aspect of this document?

Email: erratum@infineon.com

Document reference
IFX-mlb1764777900264

Important notice

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

Warnings

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.