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September 13, 2017

FM3 Family Notification on Return from TIMER/STOP Mode Transition by Interrupts

In 32-bit microcontroller FM3 family, it has found that the MCU may not be able to return from the TIMER/STOP mode after transiting into the lower power consumption mode (TIMER/STOP mode).
This document describes the root case and the workaround.

Applicable Devices

Series Name	Part Number
MB9B500 Series	MB9BF504N, MB9BF505N, MB9BF506N, MB9BF504R, MB9BF505R, MB9BF506R
MB9B400 Series	MB9BF404N, MB9BF405N, MB9BF406N, MB9BF404R, MB9BF405R, MB9BF406R
MB9B300 Series	MB9BF304N, MB9BF305N, MB9BF306N, MB9BF304R, MB9BF305R, MB9BF306R
MB9B100 Series	MB9BF102N, MB9BF104N, MB9BF105N, MB9BF106N, MB9BF102R, MB9BF104R, MB9BF105R, MB9BF106R
MB9A100 Series	MB9AF102N, MB9AF104N, MB9AF105N, MB9AF102R, MB9AF104R, MB9AF105R

1 Details

In the following interrupts, the MCU may not be able to return from the TIMER/STOP mode after transiting into the TIMER/STOP mode.

Applicable interrupts

1. External interrupt
2. Non-maskable interrupt (NMI)
3. USB wakeup interrupt
4. Low-voltage detection interrupt (LVD)
5. Timer counter interrupt
6. Hardware watch dog timer interrupt

1.1 Mechanism

The MCU in FM3 family transits to the RUN mode from the TIMER/STOP mode by interrupts.
The circuit which receives the interrupt requests is called the stand-by return signal generator. The Figure 1 shows the circuit structure.
The interrupt requests are retained once at each latch circuits. Then, they are input to the OR circuit as the asynchronous return interrupt as shown in the Figure 1.

When the rising edge of the output of OR circuit (SIG.B signal) is detected, the stand-by return signal (SIG.Q signal in the Figure 1) is generated to transit to the RUN mode.

When the MCU transits to the RUN mode from the TIMER/STOP mode, there is a period, which the MCU cannot accept any interrupt request. The period is 3 x CLKLC (CLKLC: internal low speed CR clock).
If the interrupts are requested in the period, then the stand-by return signal generator cannot detect them. Moreover, any software cannot clear the interrupt requests.

As a result, the MCU transits to the TIMER/STOP mode with asserting the output of the OR circuit in the Figure 1 (SIG.B signal). That is, even if the interrupts to return form the TIMER/STOP mode is requested, the MCU cannot transit to the RUN mode from the TIMERE/STOP mode because the raising edge of the output of OR circuit (SIG.B signal) cannot be detected.
Figure 2 shows the timing waveform at normal operation. Figure 3 shows the internal timing waveform which the MCU cannot return from the stand-by mode. (restricted operation)

Figure 1. Circuit Structure of stand-by return signal generator

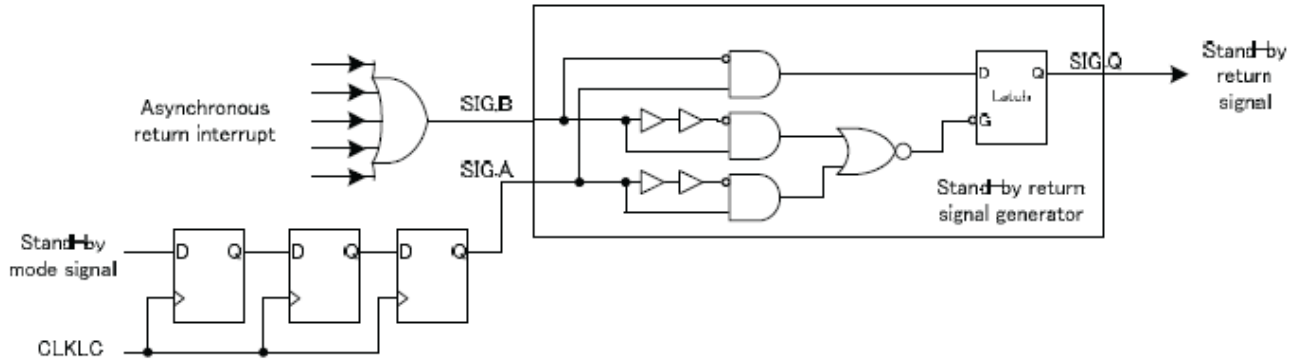


Figure 2. Timing Waveform at Normal Operation

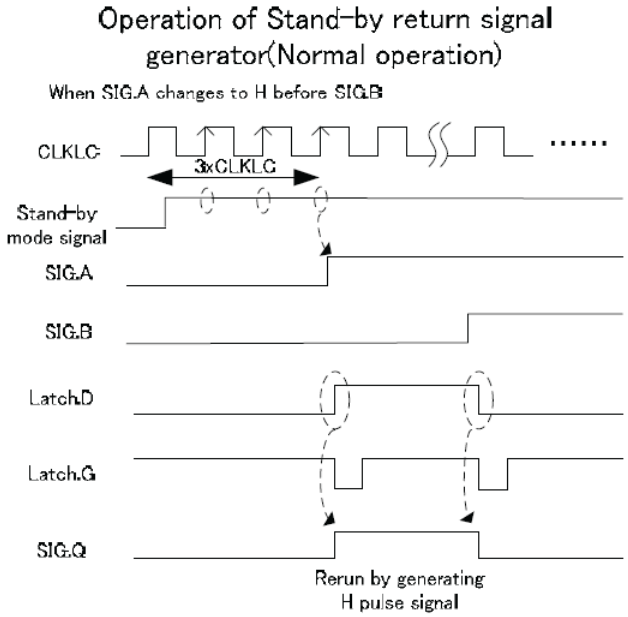
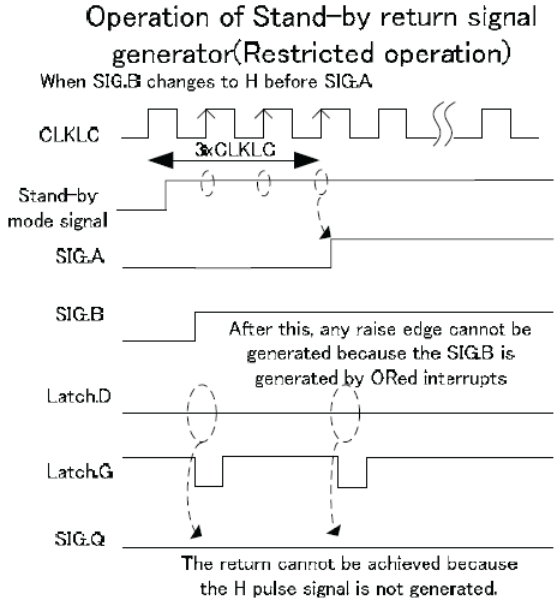


Figure 3. Timing Waveform at Restricted Operation



In the Figure 1, the stand-by mode signal (SIG.A signal) must change to the High level before the output of OR circuit (SIG.B signal) to complete the return operation.
The CPU transits to the stand-by mode after the WFI or WFE command is executed.
However, for whole MCU, 3*CLKLC is required to transit the TIMER/STOP mode (until SIG.A becomes High level.)

In the restricted operation, if the interrupts are requested in the period (3*CLKLC), the SIG.B changes to High level before SIG.A. As a result, the SIG.Q cannot be generated because the Latch.D signal cannot change to High level.
Moreover, if asynchronous return interrupt requests are ORed, then the MCU cannot return form the stand-by mode because the interrupt edge cannot be generated after that.

This phenomenon occurs in the low speed CR, the sub mode, and the stop mode in the timer mode. The high speed CR, the main, and the standby return generator of PLL mode in the timer mode is not applicable.

2 Workaround

Notes described in the Section 3 Operations of CPU Operation Modes of the CHAPTER 5 : Low Power Consumption mode in the MB9Axxx/MB9Bxxx Series Peripheral Manual shall be kept.

(Extracts from the Peripheral manual)
“Before transiting to the timer mode, ensure that NMI interrupt, External interrupt, Hardware watchdog timer interrupt, USB wake up interrupt, Clock counter interrupt and Low voltage detection interrupt causes are not set. If these interrupt causes are set, clear them.

Additionally, the following workaround shall be performed.

Additionally, the following workaround shall be performed.

2.1 External Interrupt

2.1.1 Return from TIMER mode

The external interrupt cannot be used for the return from the following TIMER modes.
- Low speed CR TIMER mode
- Sub TIMER mode

2.1.2 Return from STOP mode

The external interrupt cannot be used for the return from the STOP mode.

2.2 Non-Maskable Interrupt (NMI)

2.2.1 Return from TIMER mode

The Non-maskable interrupt (NMI) cannot be used for the return from the following TIMER modes.
- Low speed CR TIMER mode
- Sub TIMER mode

2.2.2 Return from STOP mode

The Non-maskable interrupt (NMI) cannot be used for the return from the STOP mode.
The Non-maskable interrupt (NMI) cannot be used for the return from the STOP mode.

2.3 USB Wakeup Interrupt

2.3.1 Return from TIMER mode

The USB wakeup interrupt cannot be used for the return from the following TIMER modes.
- Low speed CR TIMER mode
- Sub TIMER mode

2.3.2 Return from STOP mode

The USB wakeup interrupt cannot be used for the return from the STOP mode.

2.4 Low-voltage detection interrupt

2.4.1 Return from TIMER mode

The low-voltage detection interrupt cannot be used for the return from the following TIMER modes.
- Low speed CR TIMER mode
- Sub TIMER mode

2.4.2 Return from STOP mode

The low-voltage detection interrupt cannot be used for the return from the STOP mode.

2.5 Watch Counter Interrupt

In transiting to the TIMER mode, confirm if the timer interrupt is not generated until the transition to the TIMER mode is completed, by checking the value in the underflow interrupt counter of the timer counter.

2.5.1 Setting at TIMER mode transition

TIMER mode setting procedure in the Section 3.2 Operations of TIMER modes (high speed CR timer, main timer, PLL timer, low speed CR timer, and sub timer modes) of the CHAPTER 5: Low Power Consumption mode in the MB9Axxx/MB9Bxxx Series Peripheral Manual shall be kept.

(Extracts from the Peripheral manual)

“Execute the following steps to change to TIMER mode.

1. Write "0x1ACC" to the KEY bit and "0b00" to the STM bit of the Standby Mode Control Register (STB_CTL). Use the SPL bit to set the status of each pin in TIMER mode.
2. Set “1” to the SLEEPDEEP bit of the Cortex-M3 System Control Register.
3. Execute the WFI or WFE instruction.

The system changes to the appropriate TIMER mode according to the current clock mode indicated in the RCM bit of the System Clock Mode Control Register (SCM_CTL).”

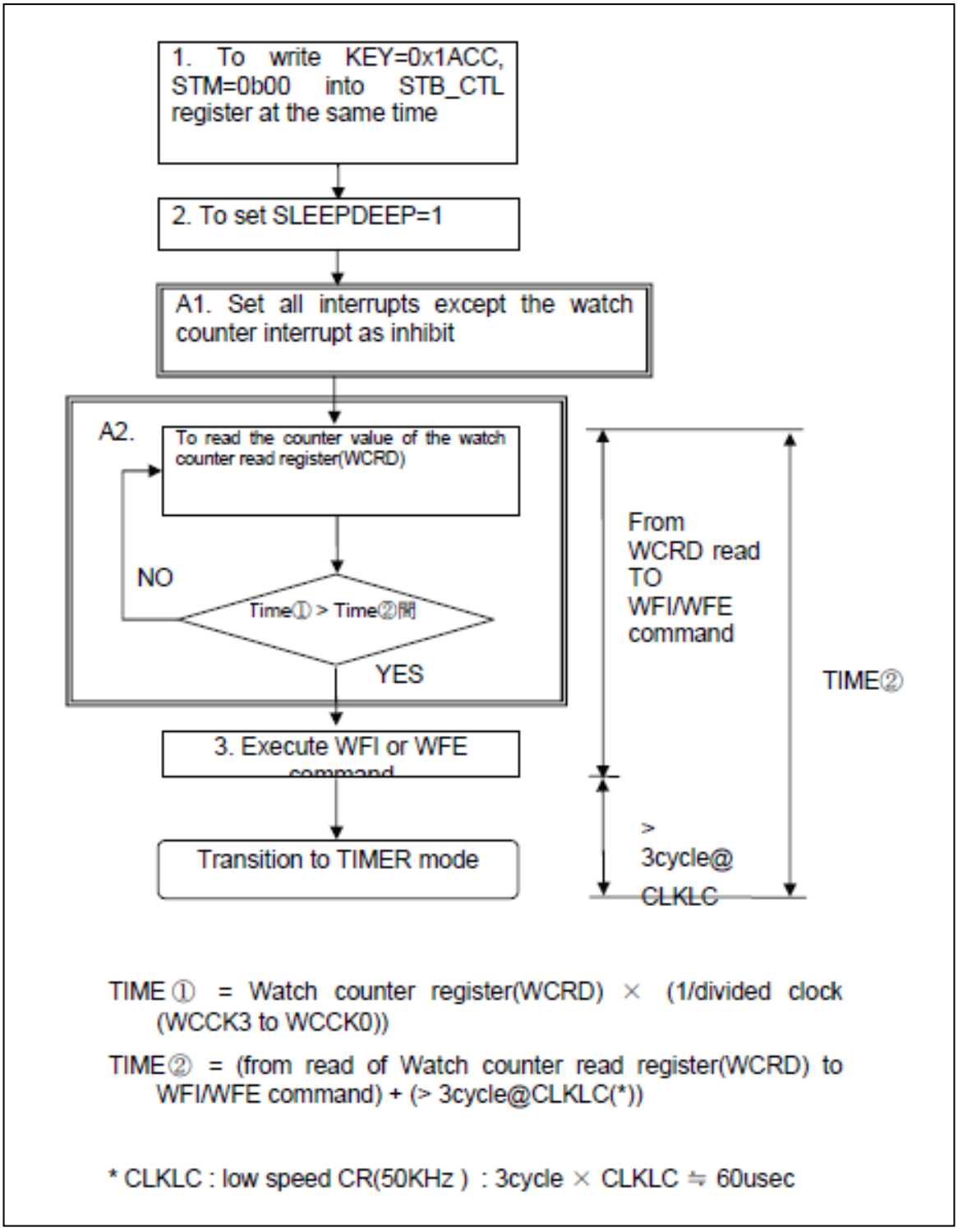
Additionally, the following setting shall be performed before 3. Execute the WFI or WFE instruction.

Additional setting 1: Set all interrupts except the watch counter interrupt as inhibit.

Additional setting 2: Check the value of the watch counter re-load register (WCRD).

Furthermore, check if the period between the WFI or WFE command execution and the TIMER mode transition is satisfied.

2.5.2 Example of Setting for Watch counter in TIMER mode transition



2.5.3 Notes

If the value of the watch counter reload counter (WCRL) is shorter than the time until the TIMER mode transition, the watch counter interrupt cannot be used for the return from the TIMER mode.
In this case, set the watch counter interrupt request (WCIE = 0 of watch counter control register: WCCR) as inhibit.

2.6 Hardware Watchdog Timer

When the MCU transits to the TIMER mode, do not generate the hardware watchdog interrupt until the transition to the TIMER mode is completed, by executing the reload of the hardware watch dog timer counter.

2.6.1 Notes on TIMER mode transition

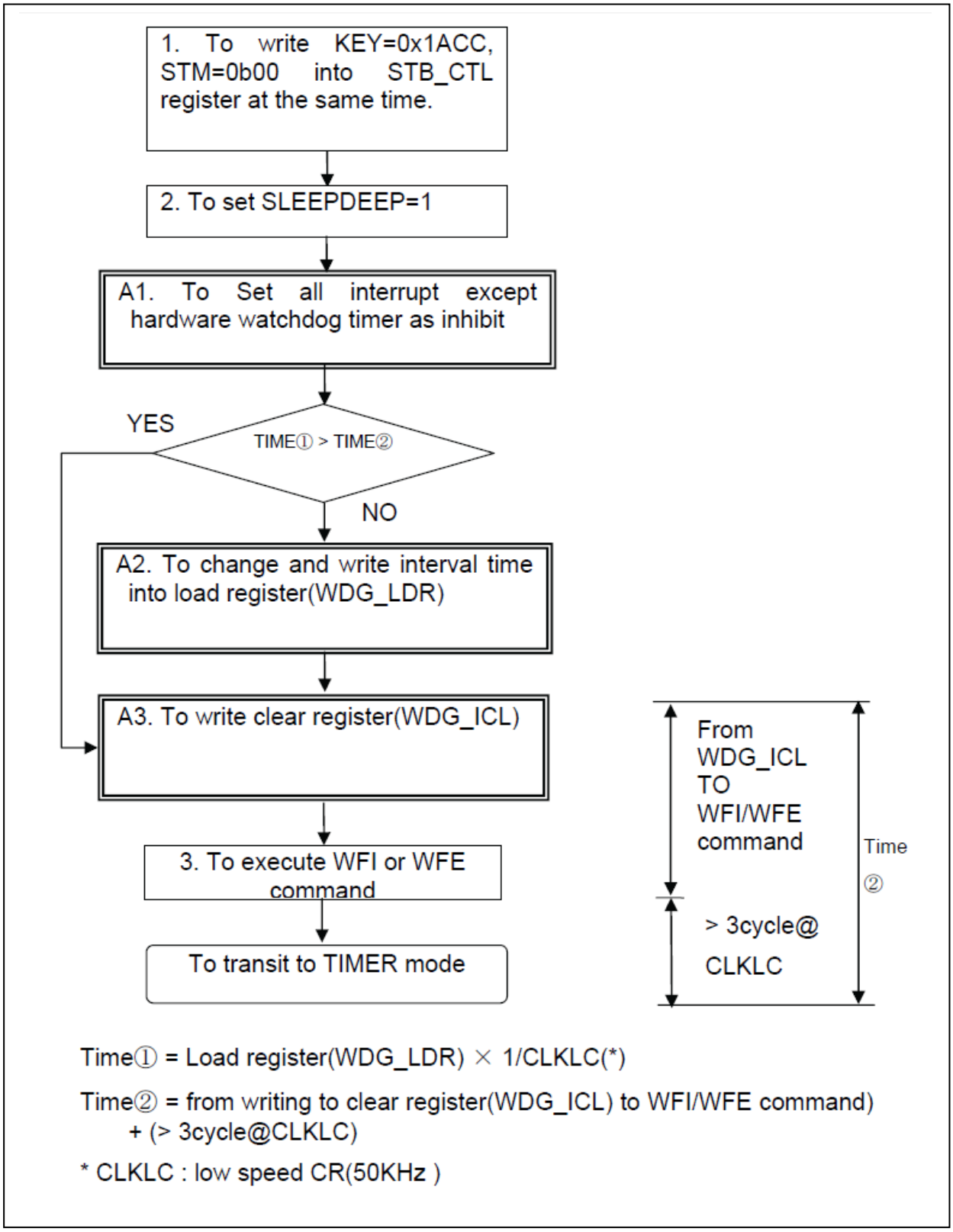
When the MCU transits to the TIMER mode, clear the counter of the hardware watchdog timer to avoid the generation of the hardware watchdog interrupt in the TIMER mode transition.

How to reload the Hardware Watchdog Counter
The following setting shall be performed before the WFI or WFE command is executed.

A1. Set all interrupt except the watch counter as inhibit.
A2. Write the interval time to the load register (WDG_LDR).
A3. Write the clear register (WDG_ICL).

For details, refer to the Figure 4-2 Setting procedure example of hardware watchdog timer in the CHAPTER 11: Watchdog timer of MB9Axxx/MB9Bxxx Series Peripheral Manual.

2.6.2 Example of setting Hardware Watchdog timer in TIMER mode



Appendix-1

Status on each interrupts

Interrupts	TIMER mode					Stop
	High speed CR	Main	PLL	Low speed CR	Sub	
External interrupt 0 to 15	○	○	○	×	×	×
NMI	○	○	○	×	×	×
USB	○	○	○	×	×	×
Low-voltage detection	○	○	○	×	×	×
Watch counter	△	△	△	△	△	-
Hardware Watchdog Timer	△	△	△	△	△	-

Remarks

- ○ : Not applicable
- △ : Avoidance by software should be reviewed.
- × : Applicable. Phenomenon described in this document may occur.
- - : Not applicable as the timer counter is stopped in the STOP mode.

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