my-d™ move lean and my-d™ move lean NFC

Extended datasheet

Intelligent 64 byte EEPROM with contactless interface compliant to ISO/IEC 14443-3 Type A and support of NFC Forum Type 2 Tag operation

Key features

Contactless interface

- Physical interface and anticollision compliant to ISO/IEC 14443 Type A
  - Operation frequency 13.56 MHz
  - Data rate 106 kbit/s in both direction
  - Contactless transmission of data and supply energy
  - Anticollision logic: Several cards may be operated in the field simultaneously
- Unique identification number (7 byte double-size UID) according to ISO/IEC 14443-3 Type A
- Read and write distance up to 10 cm and more (influenced by external circuitry i.e. reader and inlay design)

64 byte EEPROM

- Organized in 16 blocks of 4 bytes each
- 48 bytes freely programmable user memory
- 16 bytes of service area reserved for UID, LOCK bytes, OTP block
- Programming time per block < 4 ms
- Endurance minimum 10,000 erase/write cycles[1)]
- Data retention minimum 5 years[1)]

Privacy features

- 32-bit of One Time Programmable (OTP) memory area
- Locking mechanism for each block

Data protection

- Data integrity supported by 16-bit CRC, parity bit, command length check
- Anti-tearing mechanism for OTP

NFC Forum operation

- Compliant to NFC Forum Type 2 Tag operation
- Support of static memory structure according to NFC Forum Type 2 Tag operation
- SLE 66R01L: UNINITIALIZED state, may be configured to INITIALIZED state
- SLE 66R01LN: Pre-configured NFC memory with empty NDEF message (INITIALIZED state, non-reversible)

Electrical characteristics

- On-chip capacitance 17 pF ± 5%
- ESD protection minimum 2 kV
- Ambient temperature (T_A) -25°C … +70°C (for the chip)

1 Values are temperature dependent.

About this document

Scope and purpose

This Extended datasheet describes features, functionality and operational characteristics of SLE 66R01L(N).

Intended audience

This document is primarily intended for system and application developers.

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1 Sales codes and delivery forms

This chapter provides information about available delivery forms and pin/pad descriptions.

Table 1 Sales codes and delivery forms

Sales codes	Package	Total memory/user memory[1)]
SLE 66R01L TSNP	PG-TSNP-2-3	64/48 bytes
SLE 66R01L C	Wafer sawn/unsawn	
SLE 66R01L NB	NiAu Bumped (sawn wafer)	
SLE 66R01LN TSNP	PG-TSNP-2-3	
SLE 66R01LN C	Wafer sawn/unsawn	
SLE 66R01LN NB	NiAu Bumped (sawn wafer)	

1) Total memory size includes the service area whereas user memory size is freely programmable for user data.

Note: The ordering codes for the individual sales code and package combinations are available on request.

1.1 Bare die

For more details (die dimensions, pad size, pad location, etc..,), please refer to the wafer specification document [7].

1.1.1 Pin description bare die

The my-d™ move lean/my-d™ move lean NFC provides a contactless interface. Table 2 lists pin/pad definitions and pin/pad functions.

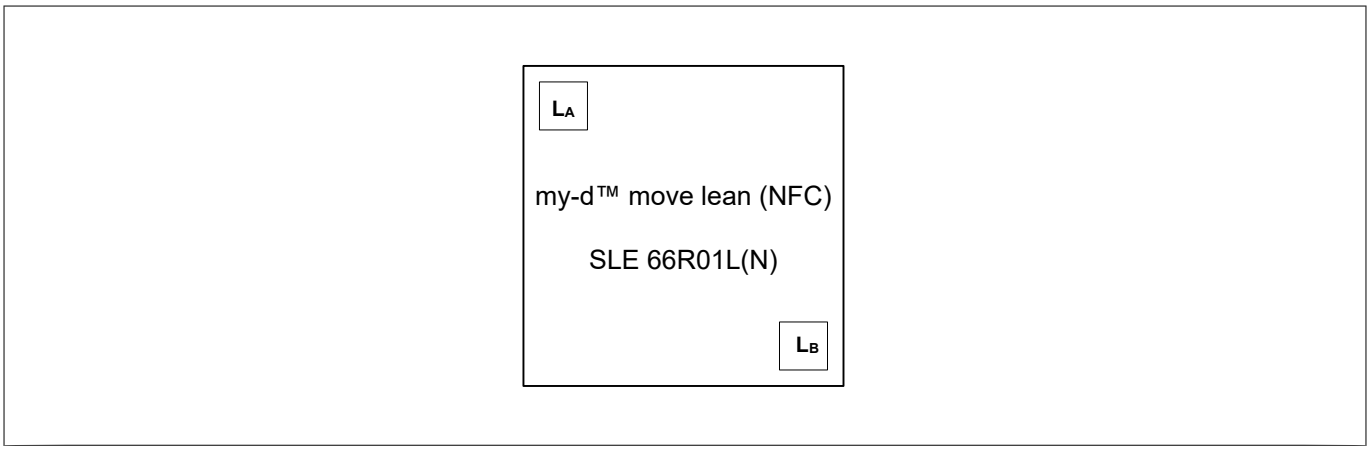

Figure 1 Pin configuration bare die

Table 2 Pin/pad description and function

Symbol	Function
L_A	Antenna connection
L_B	Antenna connection

1.2 SMD package

The following package is available:

- PG-TSNP-2-3

Table 3 Pad/pin description

Pad number	Pin description
1	Antenna connection
2	Antenna connection

The figures in the sections below show the following aspects of the package:

- Package outline and pin layout: It shows the package dimensions of the device in the individual packages
- Package footprint: It shows footprint recommendations
- Tape and reel packing
- Sample marking pattern: It describes the productive sample marking pattern on the package

Notes:

1. *The drawings are for information only and not drawn to scale. More detailed information about package characteristics and assembly instructions is available on request.*

2. *Unless specified otherwise, all figure dimensions are given in mm.*

1.2.1 Package outline and pin layout

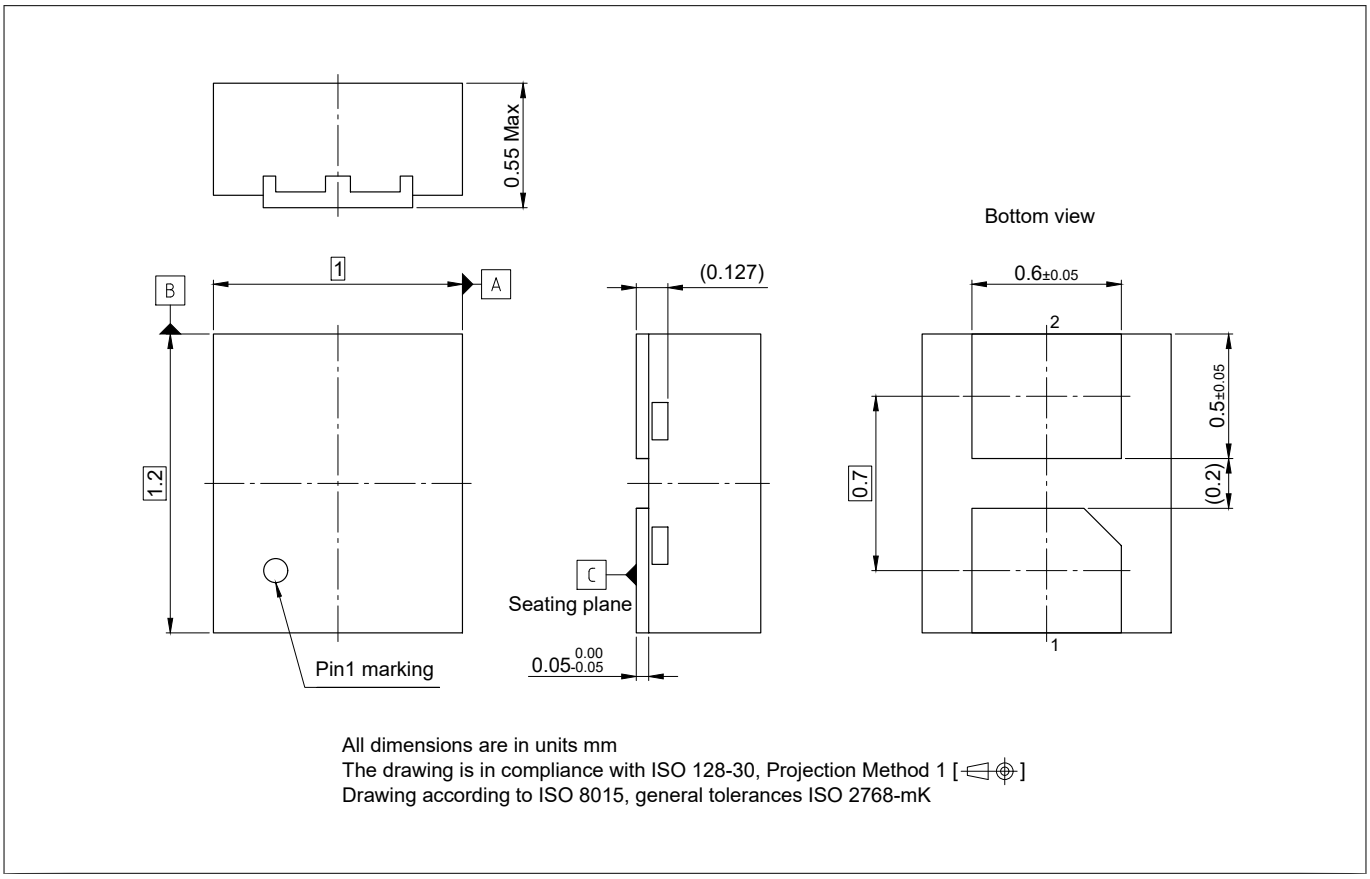

Figure 2 PG-TSNP-2-3 package outline and pin layout

1.2.2 Package footprint

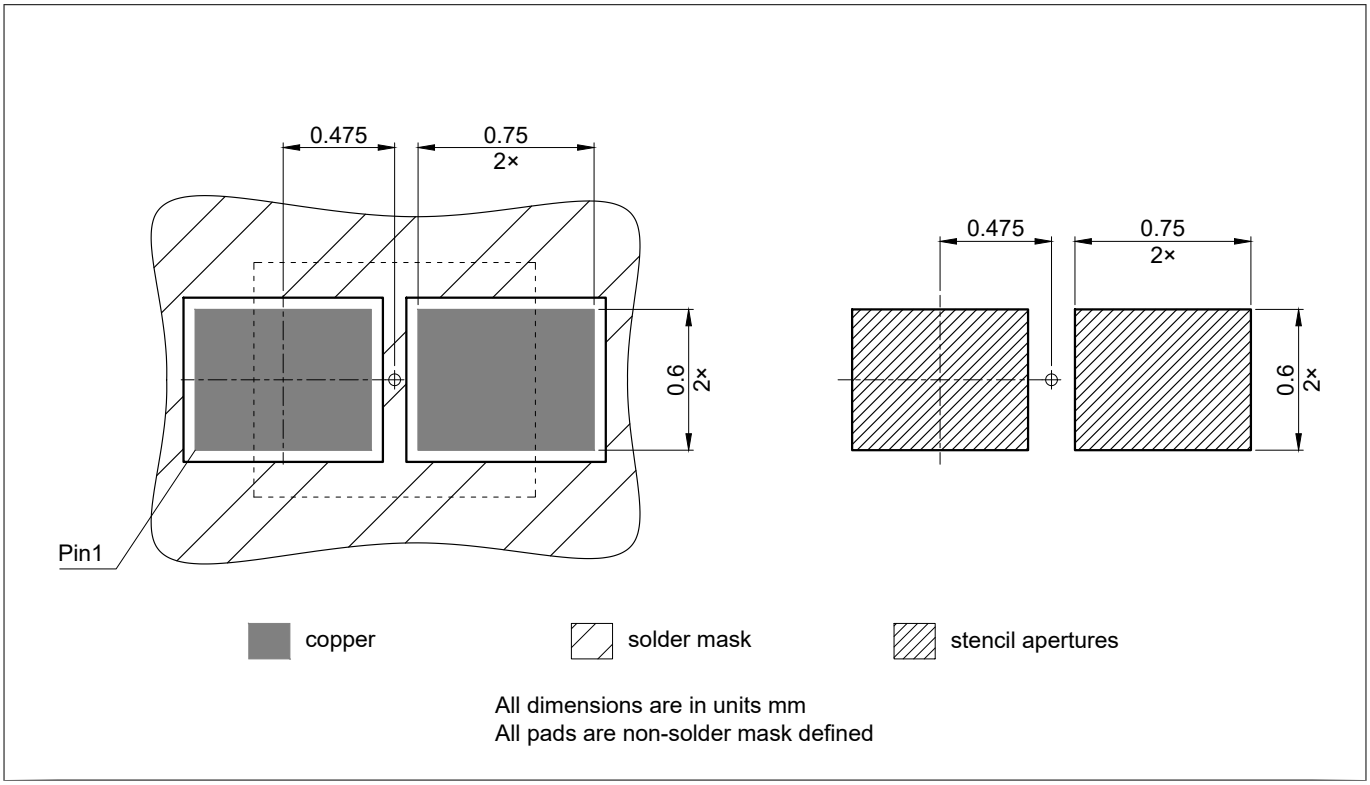

Figure 3 PG-TSNP-2-3 package footprint

1.2.3 Tape and reel packing

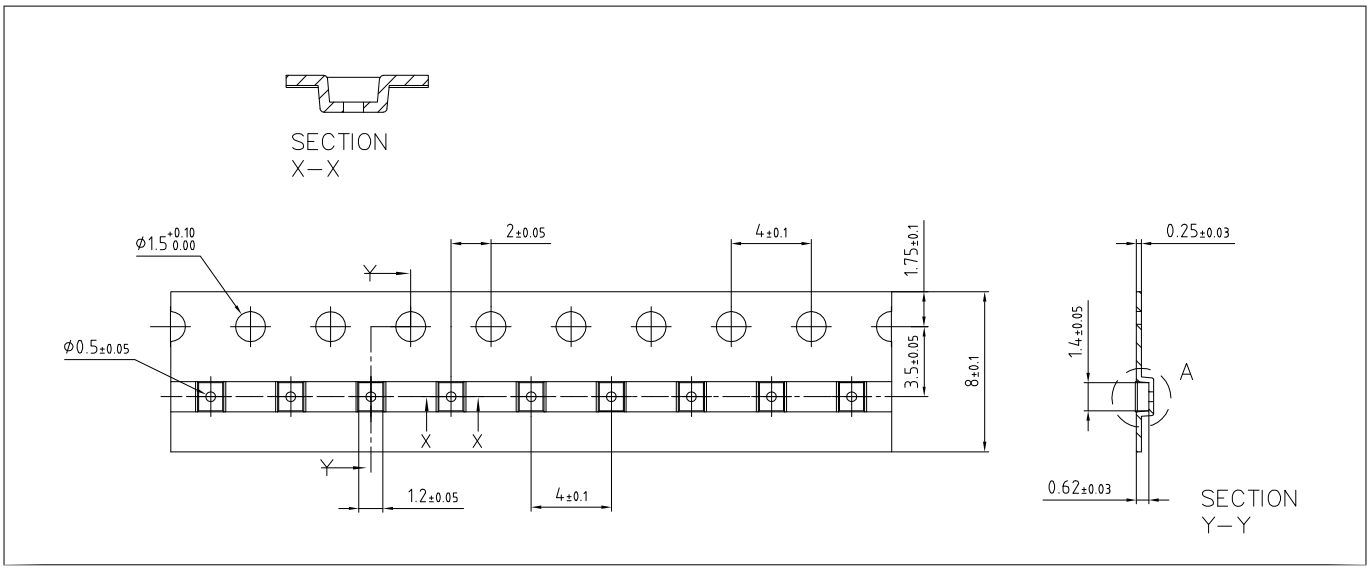

Figure 4 PG-TSNP-2-3 tape and reel packing

1.2.4 Production sample marking pattern

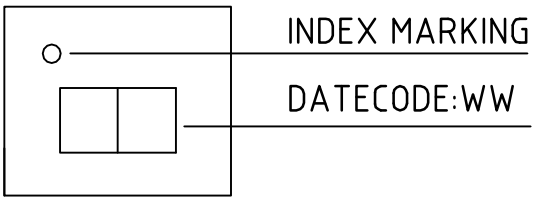

Figure 5 PG-TSNP-2-3 sample marking pattern

Table 4 Marking pattern

Indicator	Description
□□	Datecode
<WW>	Production week[1)]

1) It is inserted during fabrication

2 my-d™ product family

my-d™ products are available both in plain mode with open memory access and in secure mode with memory access controlled by authentication procedures. The my-d™ product family provides users with different memory sizes, features NFC Forum Type 2 Tag functionality and incorporates security features to enable considerable flexibility in the application design.

Flexible controls within the my-d™ devices start with plain mode operation featuring individual page locking; for more complex applications various settings in secure mode can be set for multi-user/multi-application configurations.

In plain mode access to the memory is supported by both 4 byte blocks as well as 8 byte page structure.

In secure mode a cryptographic algorithm based on a 64-bit key is available. Mutual authentication, message authentication codes (MAC) and customized access conditions protect the memory against unauthorized access.

The functional architecture, meaning the memory organization and authentication of my-d™ products is the same for both my-d™ proximity (ISO/IEC 14443) and my-d™ vicinity (ISO/IEC 18000-3 mode 1 or ISO/IEC 15693). This eases the system design and allows simple adaptation between applications.

Configurable value counters featuring anti-tearing functionality are suitable for value token applications, such as limited use transportation tickets.

Architectural interoperability of my-d™ products enables easy migration from simple to more demanding applications.

The my-d™ move lean family is designed for cost-optimized applications and its implemented command set eases the usage in existing applications and infrastructures.

2.1 my-d™ move lean and my-d™ move lean NFC

The my-d™ move lean and my-d™ move lean NFC are part of Infineon's my-d™ product family and are designed to meet the requirements of the increasing NFC market demanding smart memories. They are compliant with ISO/IEC 14443 Type A, ISO/IEC 18092 and NFC Forum Type 2 Tag operation.

48 bytes of memory can be arranged in static memory structures for NFC applications.

Based on SLE 66R01L, SLE 66R01LN already contains a pre-configuration of the NFC memory indicating the INITIALIZED state according to the definition of the NFC Forum Type 2 Tag life cycle. Due to that, the my-d™ move lean NFC is ready to be used in NFC infrastructures.

my-d™ move lean and my-d™ move lean NFC products are suited for a broad range of applications like public transport, event ticketing or smart posters.

2.2 Application segments

my-d™ products are optimized for personal and object identification. Please find in the following table some dedicated examples are as follows:

Table 5 my-d™ family product overview

Product	Application
my-d™ move-SLE 66R01P	Public transport, smart posters, NFC device pairing
my-d™ move NFC-SLE 66R01PN	Public transport, smart posters, NFC device pairing
my-d™ move lean-SLE 66R01L	Public transport, smart posters, NFC device pairing
my-d™ move lean NFC-SLE 66R01LN	Public transport, smart posters, NFC device pairing
my-d™ vicinity plain-SRF 55VxxP	Factory automation, healthcare, ticketing, access control
my-d™ vicinity plain HC-SRF 55VxxP HC	Ticketing, brand protection, loyalty schemes, Ski passes
my-d™ vicinity secure-SRF 55VxxS	Ticketing, brand protection, loyalty schemes, access control
my-d™ vicinity secure-SRF 55VxxS HC	Supply chain management, library management, product authentication, amusement ticketing, access control

3 System overview

The system consists of a host system, one or more SLE 66R01L/SLE 66R01LN Tags or other ISO/IEC 14443 Type A compliant cards and an ISO/IEC 14443 Type A compatible contactless reader. Alternatively, since the SLE 66R01L and SLE 66R01LN can be used in NFC Forum Type 2 Tag memory structures, an NFC Forum device in card reader/writer mode can be used to operate the chip.

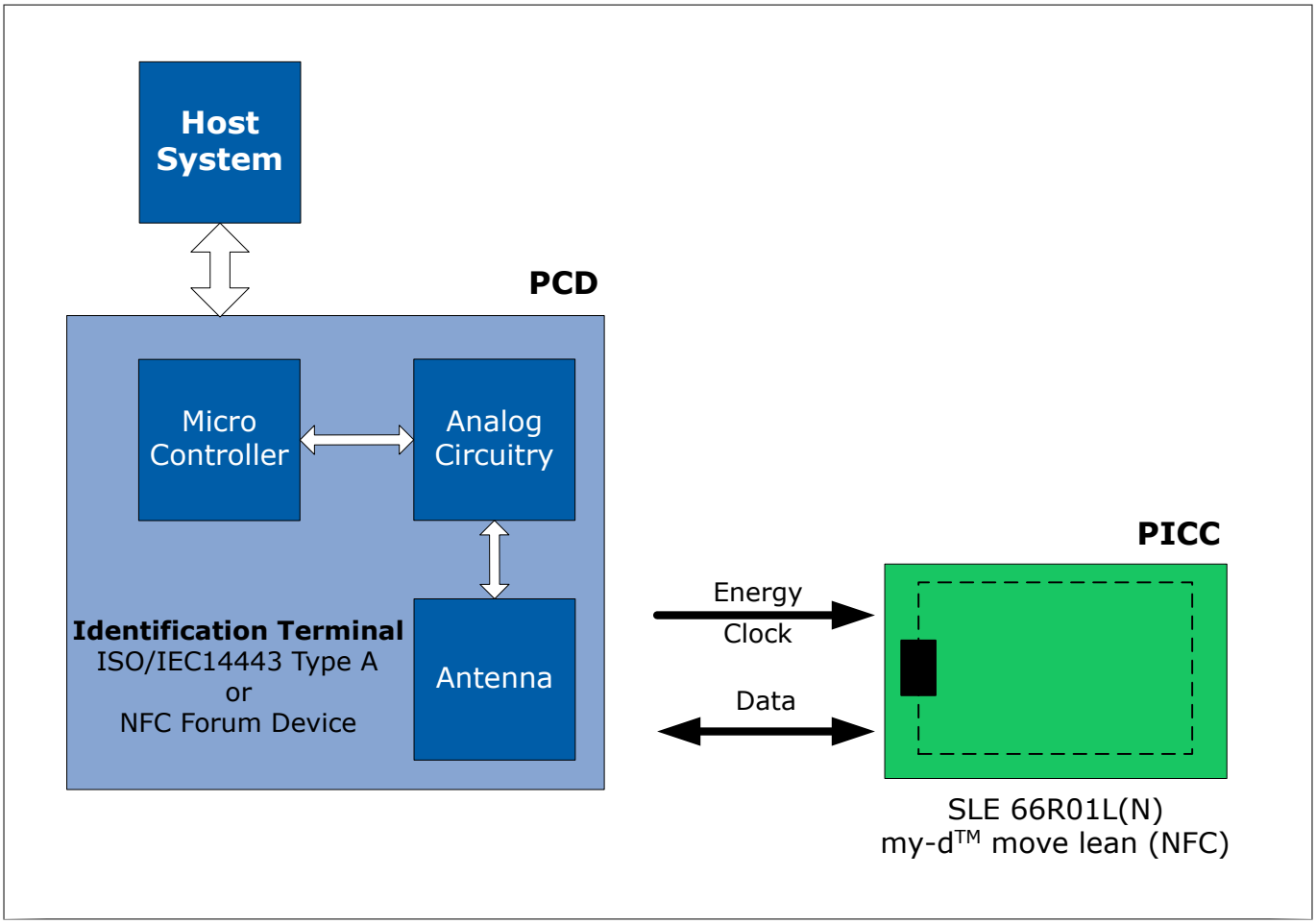

Figure 6 SLE 66R01L and SLE 66R01LN contactless system overview

4 Product overview

The SLE 66R01L and SLE 66R01LN are part of the Infineon my-d™ product family and support Infineon's transport and ticketing strategy and are designed to meet the requirements of NFC applications.

They are compliant with ISO/IEC 14443 Type A and NFC Forum Type 2 Tag operation.

4.1 Circuit description

The SLE 66R01L and SLE 66R01LN are made up of an EEPROM memory unit, an analog interface for contactless operation, a data transmission path and a control unit. Figure 7 illustrates the main blocks of the SLE 66R01L and SLE 66R01LN.

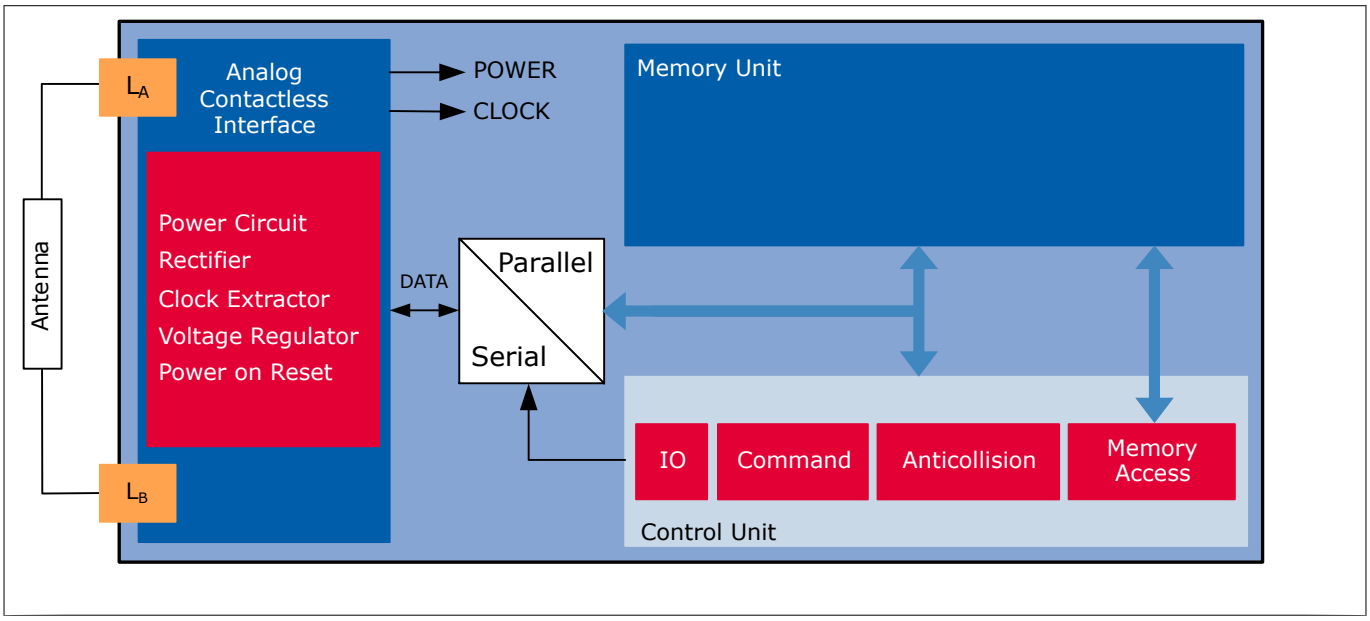

Figure 7 Block diagram of the SLE 66R01L and SLE 66R01LN

The SLE 66R01L and SLE 66R01LN comprise the following three parts:

- **Analog contactless interface**
  - The analog contactless interface contains the voltage rectifier, voltage regulator and system clock to supply the IC with appropriate power. Additionally, the data stream is modulated and demodulated
- **Memory unit**
  - The memory unit consists of 16 blocks of 4 bytes each
- **Control unit**
  - The control unit decodes and executes all commands. Additionally, the control unit is responsible for the correct anticollision flow

4.2 Memory overview

The total amount of addressable memory is 64 bytes organized in blocks of 4 bytes each.

The general structure comprises Service Areas as well as User Areas:

- 16 bytes of service and administration data (located in Service Area 1 and 2) reserved for:
  - 7 byte double-size UID
  - Configuration data
  - LOCKx bytes
  - OTP memory
- 48 bytes of user memory (located in User Area 1 and 2) reserved for:
  - User data

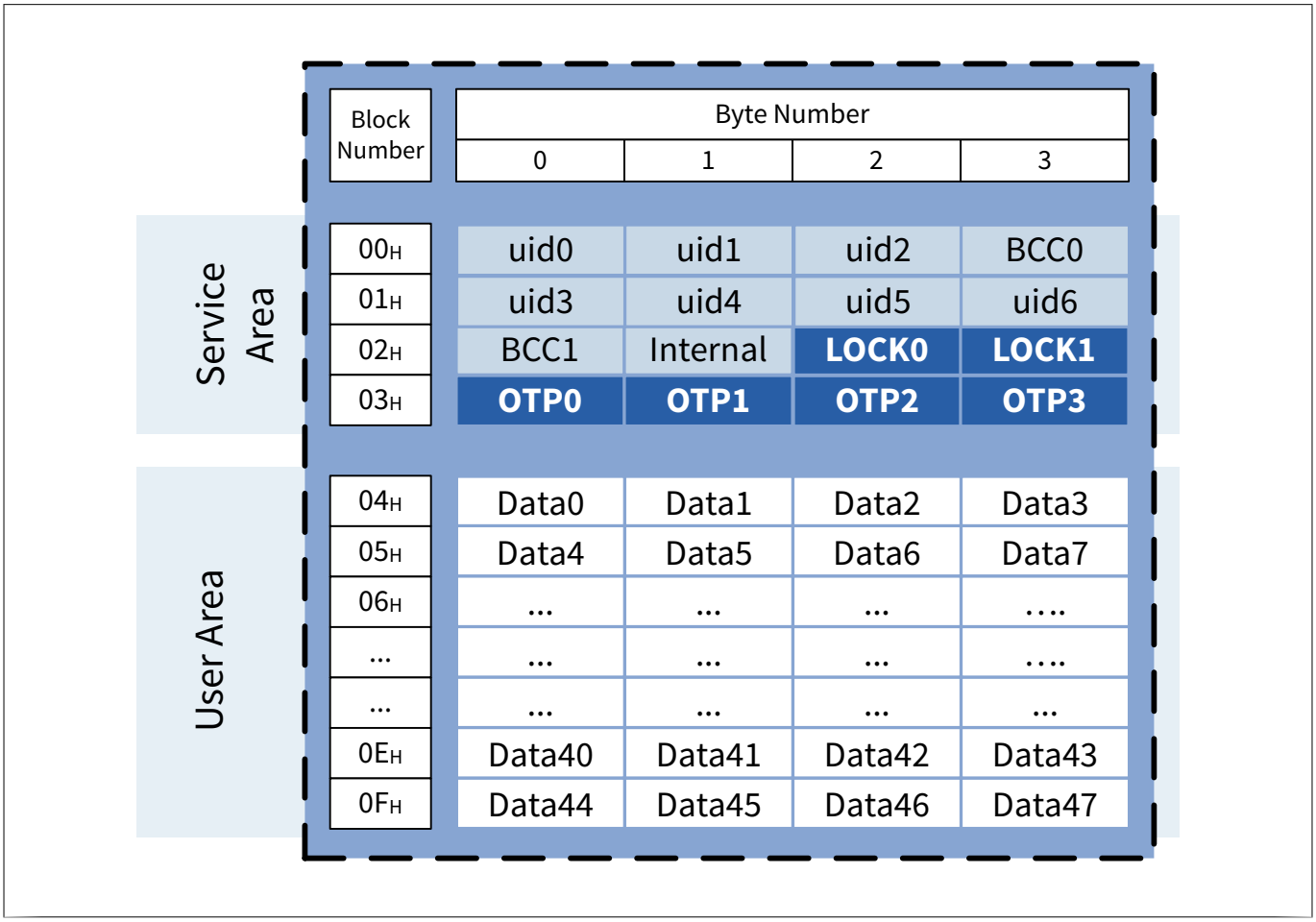

Figure 8 SLE 66R01L and SLE 66R01LN memory overview

4.3 Memory overview for NFC Forum Type 2 Tag

The memory organization is configurable according to the NFC Forum Type 2 Tag operation specification. Static memory structures are supported.

Figure 9 illustrates the principle of the SLE 66R01L and SLE 66R01LN as an NFC Forum Type 2 Tag compatible chip. The memory can be accessed with NFC Forum Type 2 Tag commands.

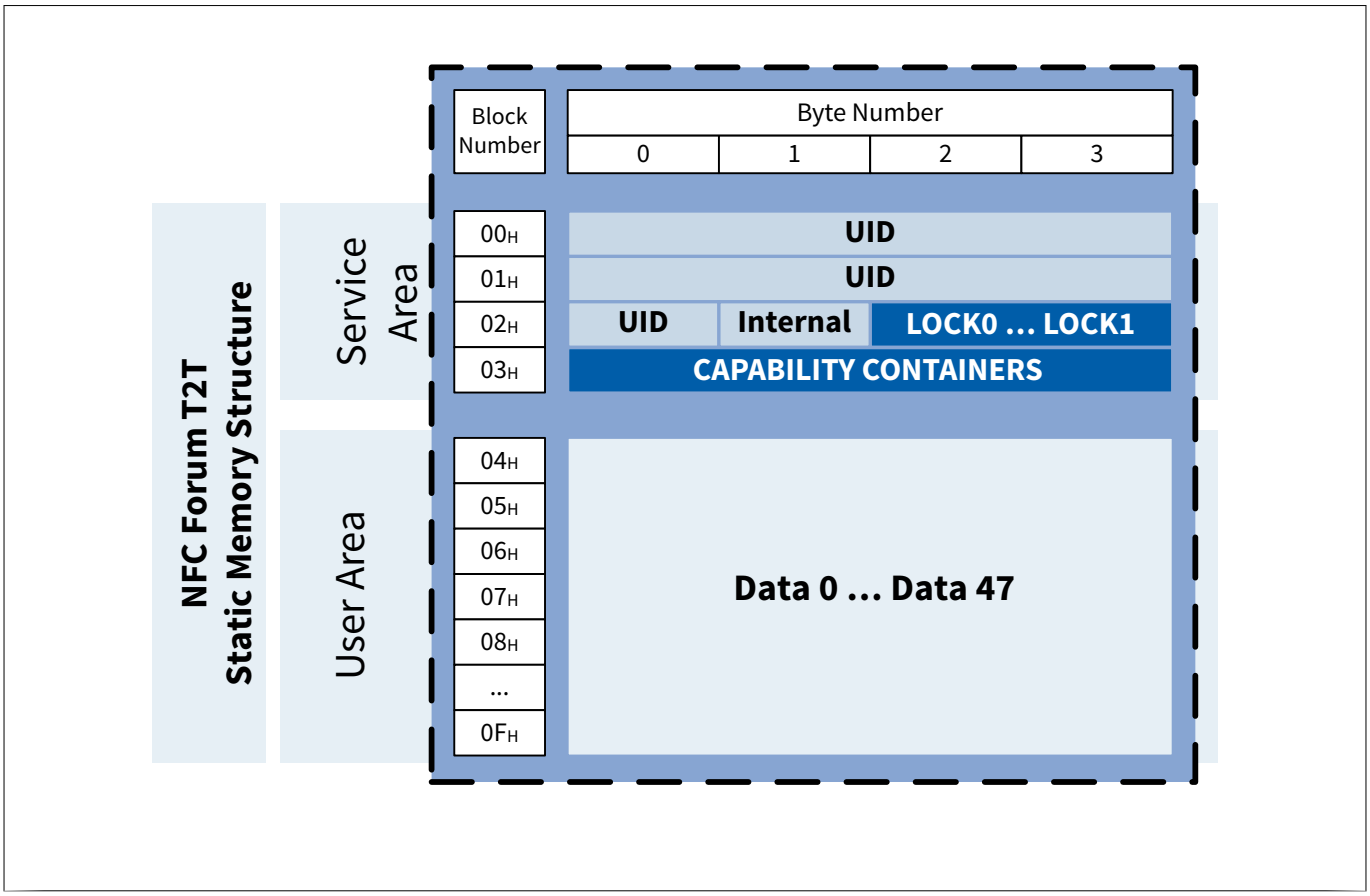

Figure 9 SLE 66R01L and SLE 66R01LN NFC Forum Type 2 Tag memory structure

Based on SLE 66R01L and SLE 66R01LN already contains a pre-configuration of the NFC memory indicating the INITIALIZED state according to the definition of the NFC Forum Type 2 Tag life cycle. With this pre-configuration the my-d™ move lean NFC can be immediately used in NFC infrastructures.

For details regarding the NFC initialization of my-d™ move lean and my-d™ move lean NFC please refer to the Application Note “How to operate my-d™ devices in NFC Forum Type 2 Tag infrastructures”.

Attention**: **The pre-configuration of SLE 66R01LN is non-reversible and the my-d™ move lean NFC cannot be overwritten and used as plain, standard my-d™ move lean anymore.

4.4 UID coding

To identify SLE 66R01L and SLE 66R01LN chip the manufacturer code and a chip family identifier are coded into the UID as described in Table 6. The chip family identifier can be used to determine the basic command set for the chip.

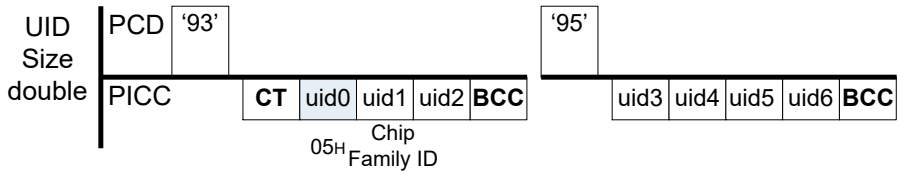

Figure 10 SLE 66R01L and SLE 66R01LN double-size UID

Table 6 UID coding

UID field	Value	Description
uid0	05_H	IC manufacturer code
uid1	$7X_H$	Chip family identifier Higher Nibble: 0111_B: my-d™ move lean and my-d™ move lean NFC Lower Nibble: Part of the UID number

4.5 Supported standards

SLE 66R01L and SLE 66R01LN support the following standards:

- ISO/IEC 14443 Type A (Parts 1, 2, and 3) [2] [3] [4] tested according to ISO/IEC 10373-6 [5] (PICC test and validation)
- NFC Forum Type 2 Tag operation specification

4.6 Command set

The SLE 66R01L and SLE 66R01LN are compliant with the ISO/IEC 14443 Type A standard.

A set of standard ISO/IEC 14443 Type A command is implemented to operate the chip.

Additionally NFC Forum Type 2 Tag commands and a my-d™ move lean and my-d™ move lean NFC specific command set is implemented.

5 Memory organization

The total amount of user memory is 64 byte. It is organized in blocks of 4 bytes each.

It comprises:

- 48 bytes for user data
- 16 bytes for UID, OTP, locking information, IC configuration and manufacturer information

Figure 11 shows the memory structure of the SLE 66R01L and SLE 66R01LN chip.

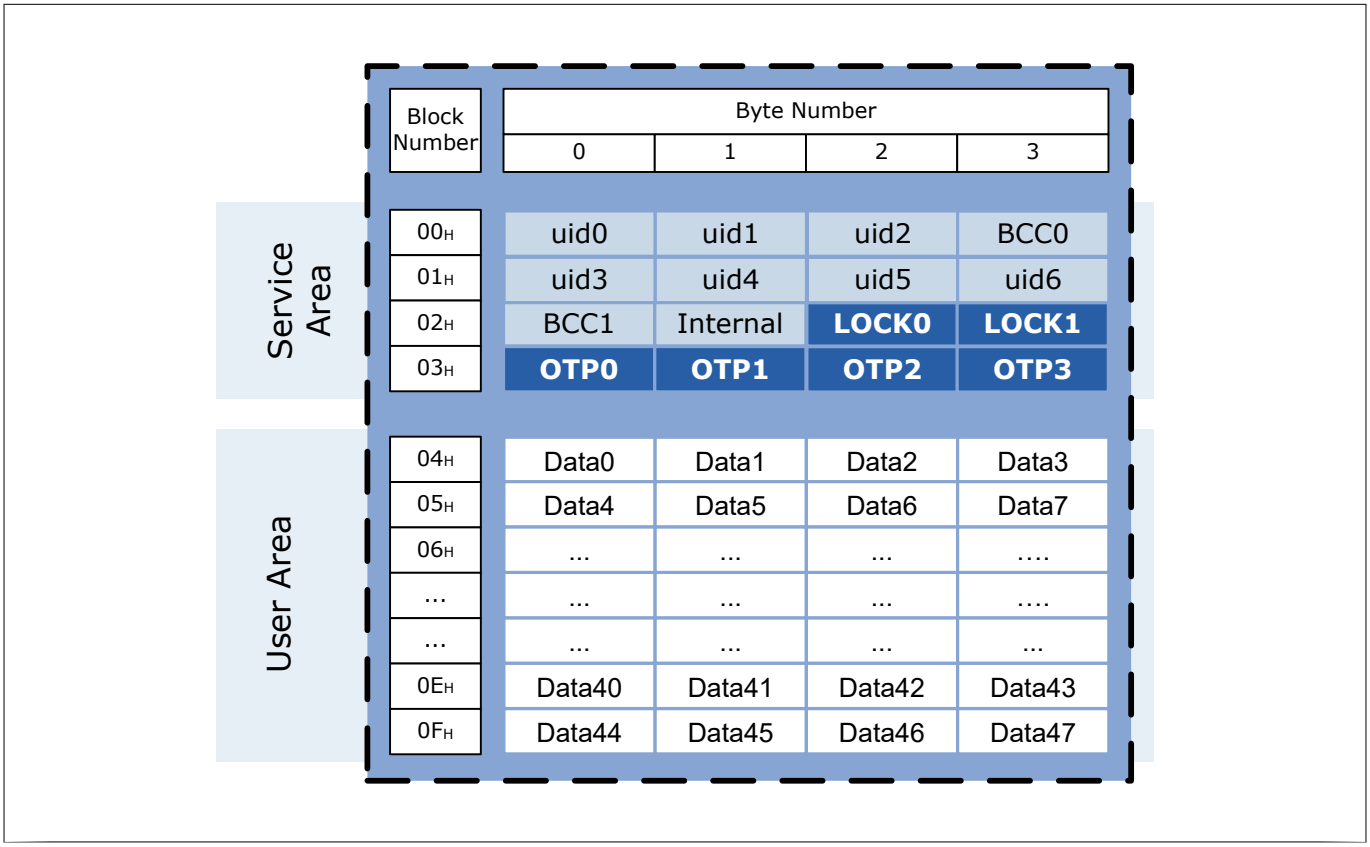

Figure 11 my-d™ move lean and my-d™ move lean NFC memory organization

5.1 User memory Area

Blocks from address 04_H to $0F_H$ belong to the user memory Area (1 and 2). This part of the memory is readable/ writable as well as lockable against unintentional overwriting using a locking mechanism.

5.2 Service Area

The Service Area 1 contains:

- 7 byte double-size UID (plus two bytes of UID BCC information)
- Internal byte
- LOCK0 and LOCK1 to lock the OTP block and blocks in the user Area
- 32-bit OTP memory

5.2.1 Unique identifier (UID)

The 9 bytes of the UID (7 byte UID +2 bytes BCC information) are allocated in block 00_H, block 01_H and byte 1 of block 02_H of the my-d™ move lean and my-d™ move lean NFC memory. All bytes are programmed and locked during the manufacturing process. These bytes cannot be changed.

For the content of the UID the following definitions apply:

- SLE 66R01L and SLE 66R01LN support Cascade Level 2 UID according to the ISO/IEC 14443 Type A which is a 7 byte unique number

The table below describes the content of the UID including the BCC information.

Table 7 UID description

Cascade Level 2 - double-size UID										
UID byte	CT[1]	uid0[2]	uid1[3]	uid2	BCC0[4]	uid3	uid4	uid5	uid6	BCC1[4]

1) CT is the Cascade Tag and designates CL2. It has a value of 88_H. Please note that CT is hardwired and not stored in the memory.
2) uid0 is the manufacturer code: 05_H.
3) uid1 is the Chip Family Identifier. The higher significant nibble identifies a my-d™ move lean and my-d™ move lean NFC chip (0111_B). The lower significant nibble is part of the serial number.
4) BCCx are the UID CLn checkbytes calculated as Exclusive-OR over the four previous bytes (as described in ISO/IEC 14443-3 Type A [4]). BCCx is stored in the memory and read-out during the anti-collision.

5.2.2 Locking mechanism

Bytes LOCK0, LOCK1 allocated in block 02_H represent the one time field programmable bits which are used to lock the blocks in the specified address range from block 03_H (OTP Block) to $0F_H$.

Each block in this range can be individually locked to prevent further write access. A locking mechanism of each block is irreversible, i.e. once the locking information of a particular block (Lx) is set to 1_B it can not be reset back to 0_B anymore. Figure 12 illustrates the locking bytes with the corresponding locking bits.

Furthermore, it is possible to freeze the locking information of some memory areas by setting block locking (BL) bits e.g. if the bit BL 15-10 is set to 1_B then the locking information for the corresponding area (L10 to L15) is not changeable any more. See the example in Table 8.

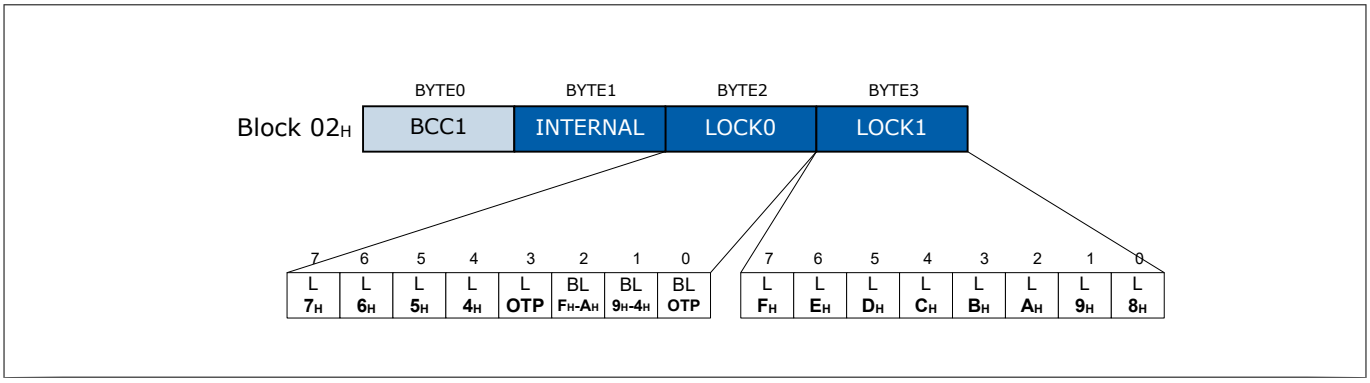

Figure 12 Locking and block locking mechanism

The write one block (WR1B) command should be used to set the locking or block locking information of a certain block.

If WR1B is applied to block 02_H then:

- The byte 0 (BCC1) and byte 1 (INTERNAL) will not be changed

The locking and block locking for a certain block is active immediately after writing. That means that it is not necessary to execute the REQA or WUPA command in order to activate the locking.

Note: If all three BL bits in the LOCK0 byte are set to 1_B then Block 02_H is locked. It is not possible to change the locking bits of this block any more. In this case the SLE 66R01L and SLE 66R01LN responds with NACK to a corresponding Write command.

Table 8 Example for OTP block lock and block lock

BL OTP	L OTP	OTP block state
0_B	0_B	OTP block unlocked
0_B	1_B	OTP block locked
1_B	0_B	OTP block unlocked and can not be locked ever more
1_B	1_B	OTP block locked

An anti-tearing mechanism is implemented for lock bytes on the SLE 66R01L and SLE 66R01LN. This mechanism prevents a stored value to be lost in case of a tearing event. This increases the level of data integrity and it is transparent to the customer.

5.2.3 OTP block

The block 03_H is a One Time Programmable (OTP) block. Bits allocated in this block can only be logically set to 1_B, which is an irreversible process i.e. bits can not be reset to 0_B afterwards.

The write one block (WR1B) command should be used to program a specific OTP value. Incoming data of the WR1B command are bit-wise OR-ed with the current content of the OTP block and the result is written back to the OTP block.

Table 9 Writing to OTP block (block 03_H) from the user point of view

OTP block	Representation bit-wise	Description
Initial value	$0000\ 0000\ 0000\ 0000\ 0000\ 0000\ 0000\ 0000_B$	Production setting
Write $[55550003]_H$	$0101\ 0101\ 0101\ 0101\ 0000\ 0000\ 0000\ 0011_B$	Bit-wise “OR” with previous content of block 03_H
Write $[AA55001C]_H$	$1111\ 1111\ 0101\ 0101\ 0000\ 0000\ 0001\ 1111_B$	Bit-wise “OR” with previous content of block 03_H

An anti-tearing mechanism is implemented for the OTP block on the my-d™ move lean and my-d™ move lean NFC. This mechanism prevents the stored value to be lost in case of a tearing event. This increases the level of data integrity and is transparent to the customer.

5.3 Memory organization for NFC Forum Type 2 Tag

This section describes how to map the my-d™ move lean and my-d™ move lean NFC memory into the memory structures defined in the NFC Forum Type 2 Tag technical specification. This enables the usage of the my-d™ move lean and my-d™ move lean NFC as an NFC Forum Type 2 Tag compatible chip.

5.3.1 NFC Forum static memory structure

The static memory structure is applied to a NFC Forum Type 2 Tag with a memory size equal to 64 bytes (see Figure 13). Blocks 04_H to $0F_H$ are available to store user data.

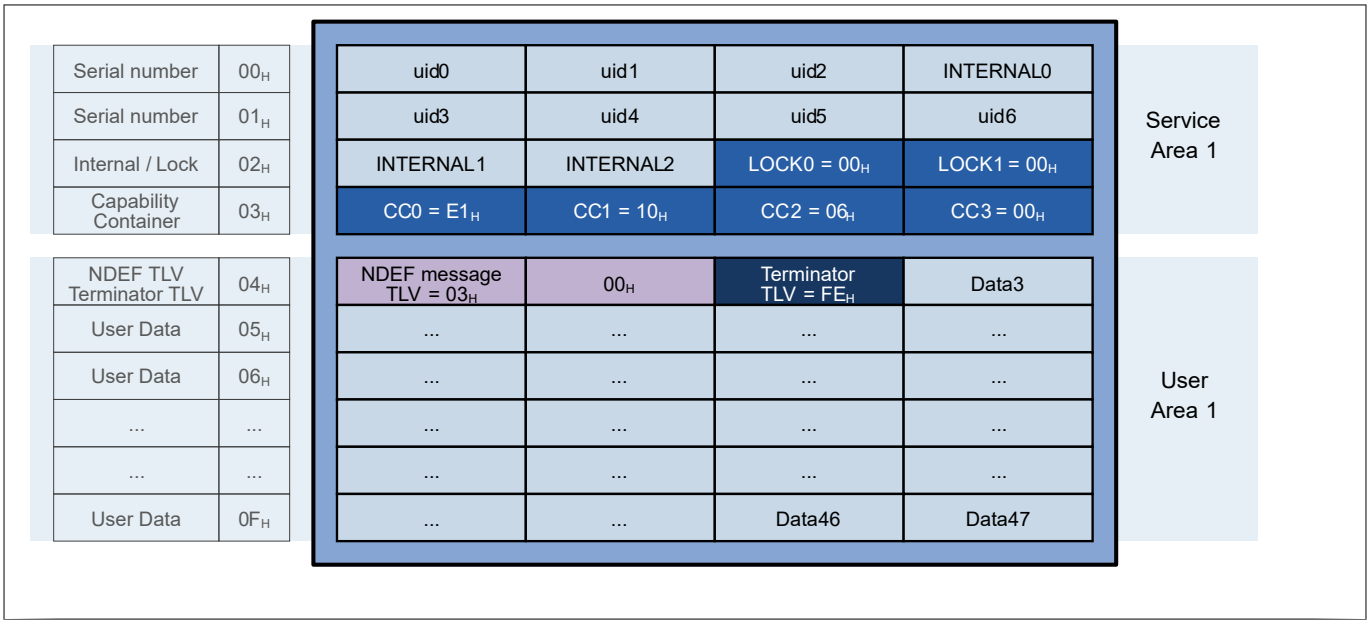

Figure 13 Static memory structure

The static memory structure is characterized by the NDEF message TLV (03_H) starting at block address 04_H. The NFC data shown in Figure 13 is an empty NDEF message (see Table 11).

5.4 Transport configuration

Figure 9 shows the memory overview of SLE 66R01L and SLE 66R01LN. The following sections provide details about the initial memory content of these devices.

5.4.1 Transport configuration my-d™ move lean

The transport configuration of SLE 66R01L contains the following information:

- Service Area contains:
  - Predefined UID (incl. BCC bytes); Read-only
  - LOCK0, LOCK1 set to 00_H
  - OTP0 - OTP3 set to 00_H
- User Area:
  - All data bytes set to 00_H

The SLE 66R01L may be configured to INITIALIZED state according to the definition to the NFC Forum Type 2 Tag life cycle by writing.

- Capability container bytes (see Table 10) to block 03_H
- Empty NDEF message TLV including; Terminator TLV (see Table 11) to block 04_H

5.4.2 Transport configuration my-d™ move lean NFC

SLE 66R01LN is delivered in the INITIALIZED state (life cycle) according to the NFC Forum Type 2 Tag specification.

- Service Area contains:
  - Predefined UID; Read-only
  - LOCK0 and LOCK1 set to 00_H
  - OTP0 - OTP3 contains the CAPABILITY CONTAINER (see Table 10)
- User Area:
  - Contains empty NDEF message TLV including terminator TLV (= FE_H) as indicated in Table 11
  - All other data bytes set to 00_H

Table 10 Capability container settings for my-d™ move lean and my-d™ move lean NFC

Chip type	CC0	CC1[1)]	CC2[2)]	CC3
SLE 66R01LN	$E1_H$	10_H (may be changed to 11_H if needed)	06_H	00_H

1) my-d™ move lean and my-d™ move lean NFC also support version 1.1 of the NFC Forum Type 2 Tag specification.
2) CC2 indicates the memory size of the data area of the Type 2 Tag; the given values represent the maximum values for the chips.

Table 11 defines the empty NDEF message TLV (identified with the Tag field value of 03_H). The length field value is set to 00_H; due to that the value field is not present.

The terminator TLV (FE_H) is the last TLV block in the data area.

Table 11 Empty NDEF message

NDEF message TLV			Terminator TLV		
Tag	Length	Value	Tag	Length	Value
03_H	00_H	-	FE_H	-	-

Note: The pre-configuration of SLE 66R01LN is non-reversible and the my-d™ move lean NFC cannot be overwritten and used as plain, standard my-d™ move lean anymore.

6 Communication principle

This chapter describes the functionality of the SLE 66R01L and SLE 66R01LN.

6.1 Communication between a card (PICC) and a reader (PCD)

It is recommended to read the ISO/IEC 14443 Type A and NFC Forum Type 2 Tag specifications in conjunction with this document to understand the communication protocol as well as the functionality of the SLE 66R01L and SLE 66R01LN as it is based on these specifications.

6.2 State diagram

The SLE 66R01L and SLE 66R01LN fully compliant to ISO/IEC 14443 Type A. All operations on this IC are initiated by an appropriate reader and controlled by the internal logic of the my-d™ move lean and my-d™ move lean NFC.

Figure 14 illustrates the state diagram of SLE 66R01L and SLE 66R01LN.

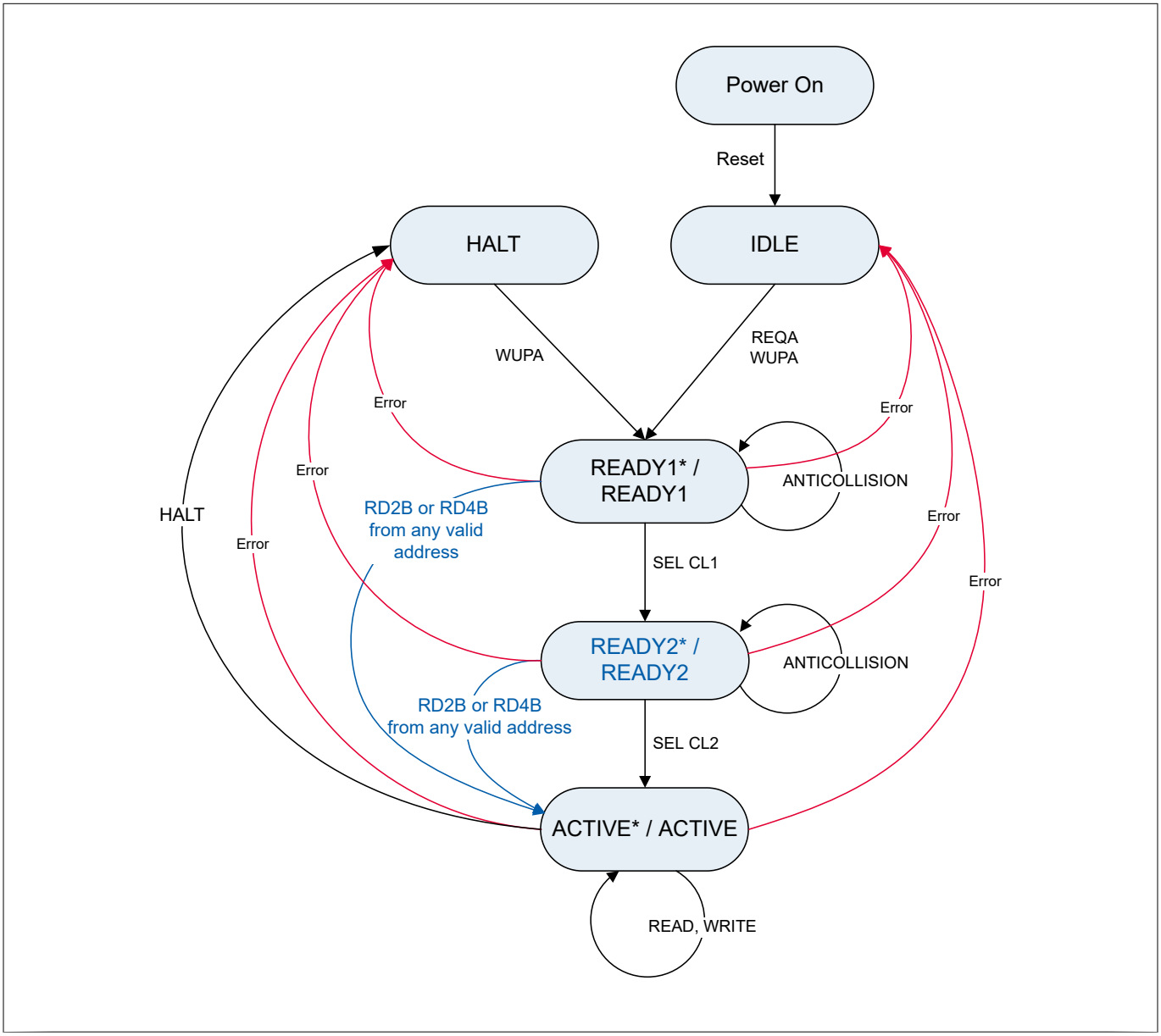

Figure 14 SLE 66R01L and SLE 66R01LN state diagram

Prior to any memory access the card has to be selected according to the ISO/IEC 14443 Type A.

If an unexpected command is received, the chip always returns to IDLE or HALT state, depending from which path it came from (the red paths in the state diagram).

6.2.1 IDLE/HALT state

After Power On, the SLE 66R01L and SLE 66R01LN is in IDLE state.

If REQA or WUPA is executed in this state, the SLE 66R01L and SLE 66R01LN transit to the READY1 state. Any other command is interpreted as an error and the chip stays in IDLE state without any response.

If the HLTA command is executed in ACTIVE/ACTIVE* state, the SLE 66R01L and SLE 66R01LN will transit to HALT state. The HALT state can be left only if the chip receives a WUPA command. Any other command is interpreted as an error and the SLE 66R01L and SLE 66R01LN stays in the HALT state without any response.

6.2.2 READY1/READY1* state

In READY1/READY1* state the first part of the UID can be resolved by using ISO/IEC 14443 Type A anticollision and/or select commands.

After the select command is executed properly the IC transits to READY2/READY2* state in which the second part of the UID can be resolved. The answer to a select command in READY1/READY1* state is Select Acknowledge (SAK) for Cascade level 1, which indicates that the UID is incomplete and the next Cascade level has to be started to resolve the whole UID (see also ISO/IEC 14443 Type A).

However, the SLE 66R01L and SLE 66R01LN can directly transit from READY1/ READY1* state to ACTIVE/ACTIVE* state if a read command RD2B or R4BD with a valid address is executed. Note if more than one SLE 66R01L and SLE 66R01LN is in the reader field, all ICs are selected after the execution of the read command, although all of them have different UIDs.

Any other command or any other interruption is interpreted as an error and the SLE 66R01L and SLE 66R01LN return to IDLE or HALT state without any response, depending from which state it has come from.

6.2.3 READY2/READY2* state

In READY2/READY2* state the second part of the UID can be resolved using ISO/IEC 14443 Type A anticollision and/or select commands.

After the select command is executed properly the IC transits to ACTIVE/ACTIVE* state in which memory can be accessed. The answer to a select command in READY2/READY2* state is SAK for Cascade level 2, which indicates that the UID is complete and the selection process is finished.

However, the SLE 66R01L and SLE 66R01LN can directly transit from READY2/READY2* state to ACTIVE/ACTIVE* state if a read command RD2B or RD4B is executed. Any valid block address can be used in the read command. Note that if more than one SLE 66R01L and SLE 66R01LN is in the reader field, all ICs are selected after the execution of the read command, although all of them have different UIDs.

Any other command or any other interruption is interpreted as an error and the SLE 66R01L and SLE 66R01LN return to IDLE or HALT state without any response, depending from which part it has come from.

6.2.4 ACTIVE/ACTIVE* state

In the ACTIVE/ACTIVE* state memory access commands can be executed.

If SLE 66R01L and SLE 66R01LN is configured to have read/write or write password protection, a password verification is required to access the protected memory pages. In case of successful password verification, read/write access to the whole memory is possible. If no verification is done or the password verification fails, the memory area above block $0F_H$ is locked according to the access rights in the configuration byte.

The ACTIVE/ACTIVE* state is left if the HLTA command is executed properly; the SLE 66R01L and SLE 66R01LN then transit to HALT state and wait until a WUPA command is received.

If any error command is received, the SLE 66R01L and SLE 66R01LN sends “No Response” (NR) or “Not Acknowledge” (NACK) and transits to IDLE or HALT state, depending from which state it has come from.

6.2.5 HALT state

The HLTA command sets the SLE 66R01L and SLE 66R01LN in the HALT state. The SLE 66R01L and SLE 66R01LN sends no response to the HLTA command. In the HALT state the IC can be activated again by a Wake-UP command (WUPA).

Any other data received is interpreted as an error, the SLE 66R01L and SLE 66R01LN sends no response and remains in HALT state.

The exact behavior of a particular command in any of the states above is also described in the specific command description.

6.3 Start up

120 µs after entering the powering field (after the field reset) the SLE 66R01L and SLE 66R01LN is ready to receive a command. If a command is send earlier, the response to this command is not defined.

6.3.1 Startup sequence of the SLE 66R01L and SLE 66R01LN

Each time after the execution of a REQA or WUPA, the SLE 66R01L and SLE 66R01LN reads the configuration byte and sets its internal states accordingly, refer to Figure 15. This information is not updated until the next execution of REQA or WUPA commands in IDLE or HALT state even when the CONFIG byte is changed in the EEPROM.

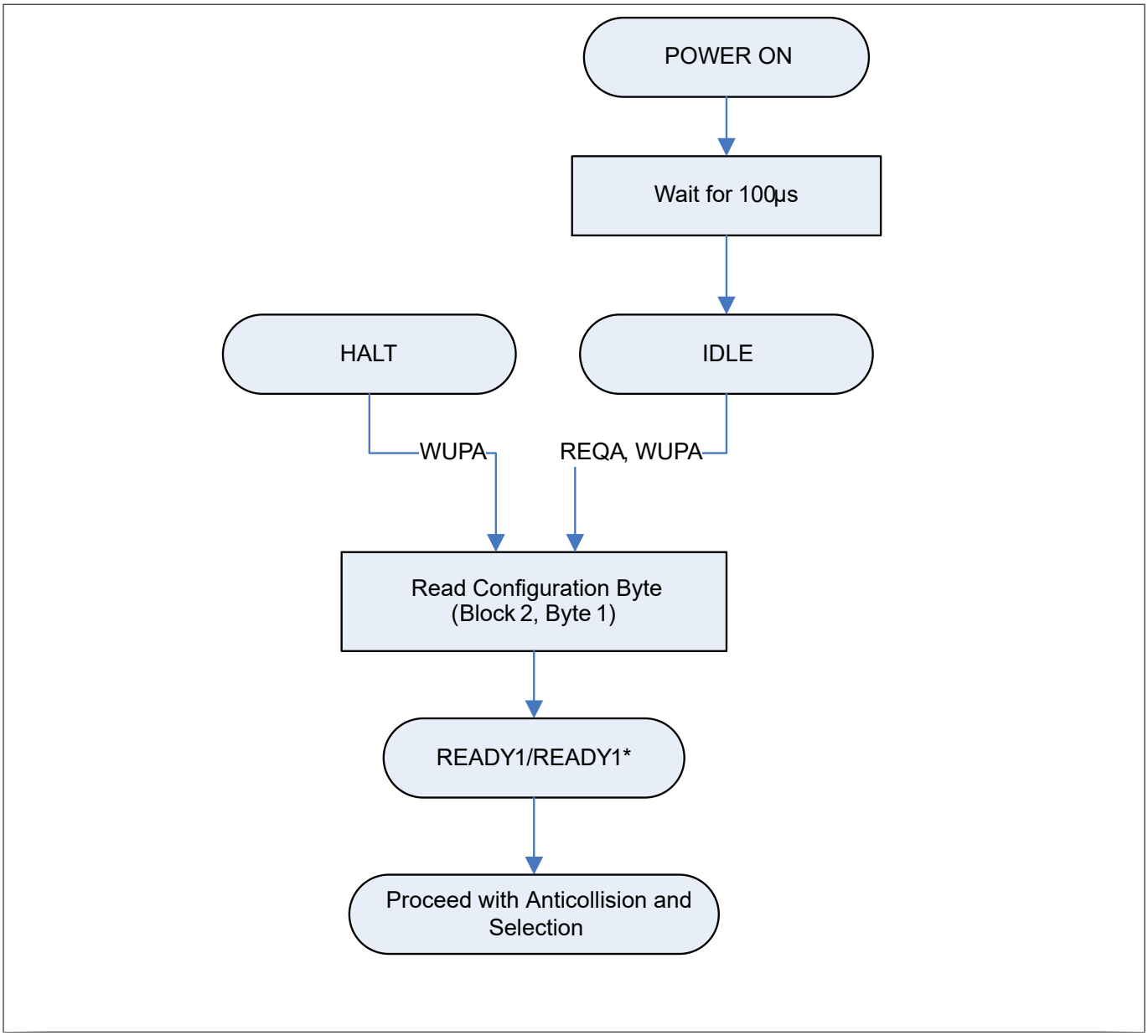

Figure 15 Start up sequence

6.4 Frame delay time

For information about frame delay time (FDT), please refer to ISO/IEC 14443 Type A specification. Generally the FDT is measured between the last rising edge of the pause transmitted by the PCD and the falling edge of the first load modulation within the start bit transmitted by the my-d™ move lean and my-d™ move lean NFC. If more then one ISO/IEC 14443 Type A compatible chip is in the operating field of the reader all of them must respond in a synchronous way which is needed for the anticollision procedure.

For detailed timings see Table 2 of ISO/IEC 14443-3 Type A Specification [4].

Note: The response timing of a particular SLE 66R01L and SLE 66R01LN command is given in the specific command description. However, the timing values are rounded and are not on a grid according the ISO/IEC 14443 Type A.

6.5 Error handling

The SLE 66R01L and SLE 66R01LN responds to valid frames only. Table 12 describes the behavior for different error cases.

Table 12 Behavior in case of an error

Current states	Command or error	Response SLE 66R01L and SLE 66R01LN	Next state
IDLE/HALT READY1/READY1* READY2/READY2*	Invalid Opcode	NR[1)]	IDLE/HALT[2)]
	Parity, Miller error, CRC	NR	IDLE/HALT
	Command too short or too long	NR	IDLE/HALT
	Invalid address	NR	IDLE/HALT
	Other errors	NR	IDLE/HALT
ACTIVE/ACTIVE*	Invalid Opcode	NR	IDLE/HALT
	Parity, Miller Error, CRC	NACK1	IDLE/HALT
	Command too short or too long	NR	IDLE/HALT
	Invalid address	NACK0	IDLE/HALT
	Other errors	NACK0	IDLE/HALT

1) RD4B and RD2B commands in READY1/READY1* and READY2/READY2* exceptionally behave as in ACTIVE/ACTIVE* state.
2) The SLE 66R01L and SLE 66R01LN returns to IDLE or HALT state depending on the state where it has come from.

7 Command set

7.1 Supported ISO/IEC 14443 Type A command set

Table 13 describes the ISO/IEC 14443-3 Type A command set which is supported by the SLE 66R01L and SLE 66R01LN.

For a detailed command description refer to the ISO/IEC 14443-3 Type A functional specification.

Table 13 ISO/IEC 14443-3 Type A command set

Command	Abbreviation	Op-Code	Description
Request A	REQA	26_H	Short frame command Type A request to all ISO/IEC 14443 Type A compatible chips in IDLE state
Wake Up A	WUPA	52_H	Short frame command Type A Wake Up request to all ISO/IEC 14443 Type A compatible chips
Anticollision	AC	93_H NVB_H 95_H NVB_H	Cascade level 1 with the number of valid bits Cascade level 2 with the number of valid bits
Select	SELA	93_H 70_H, 95_H 70_H	Select the UID of Cascade level 1 Select the UID of Cascade level 2
Halt A	HLTA	50_H	Set a chip to a HALT state Important remark: The parameter field of the HLTA command represents the valid address range which is 00_H - $0F_H$

7.2 Memory access command set

The command set of the SLE 66R01L and SLE 66R01LN comprises the NFC Forum Type 2 Tag commands as well as proprietary commands which are additionally implemented to increase data transaction time and increase the protection of the data stored in the memory.

Table 14 lists the memory access command set of the SLE 66R01L and SLE 66R01LN.

Table 14 my-d™ move lean and my-d™ move lean NFC memory access command set

Command	Abbreviation	Op-Code	Description
Read 4 blocks[1)]	RD4B	30_H	This command reads 16 bytes of data out of the memory starting from the specified address A Roll-Back mechanism is implemented: • If block $0F_H$ is reached the read continues from block 00_H
Write 1 block[2)]	WR1B	$A2_H$	If write access is granted, this command programs 4 bytes of data to the specified memory address
Compatibility write command	CPTWR	$A0_H$	This command sends 16 bytes to the SLE 66R01L and SLE 66R01LN but writes only the first 4 bytes of the incoming data to the specified memory address
Read 2 blocks	RD2B	31_H	This command reads 8 bytes out of the memory, starting from the specified address. A Roll-Back mechanism is implemented: • If block $0F_H$ is addressed, the read continues from block 00_H

(table continues...)

Table 14 (continued) my-d™ move lean and my-d™ move lean NFC memory access command set

Command	Abbreviation	Op-Code	Description
Write 2 blocks	WR2B	$A1_H$	If write access is granted, this command writes 8 bytes to the specified address memory. Note that the programming time is 4 ms

1) NFC Forum Type 2 Tag read command.
2) NFC Forum Type 2 Tag write command.

7.2.1 Read 4 Blocks (RD4B)

RD4B command reads 16 bytes of data out of the memory starting from the specified address.

The valid address range is 00_H to $0F_H$.

If any other address is specified the SLE 66R01L and SLE 66R01LN responds with a NACK. A Roll-Back mechanism is implemented:

- If e.g. block $0E_H$ is addressed blocks $0E_H$, $0F_H$, 00_H and 01_H are replied

Table 15 Read 4 Blocks (RD4B)

Command length	Code	Parameter	Data	Integrity mechanism	Response
4 bytes	30_H	Valid address range 00_H - $0F_H$	N.A.	2 bytes CRC (1 parity bit per byte)	16 bytes data +2 bytes CRC or NACK or NR

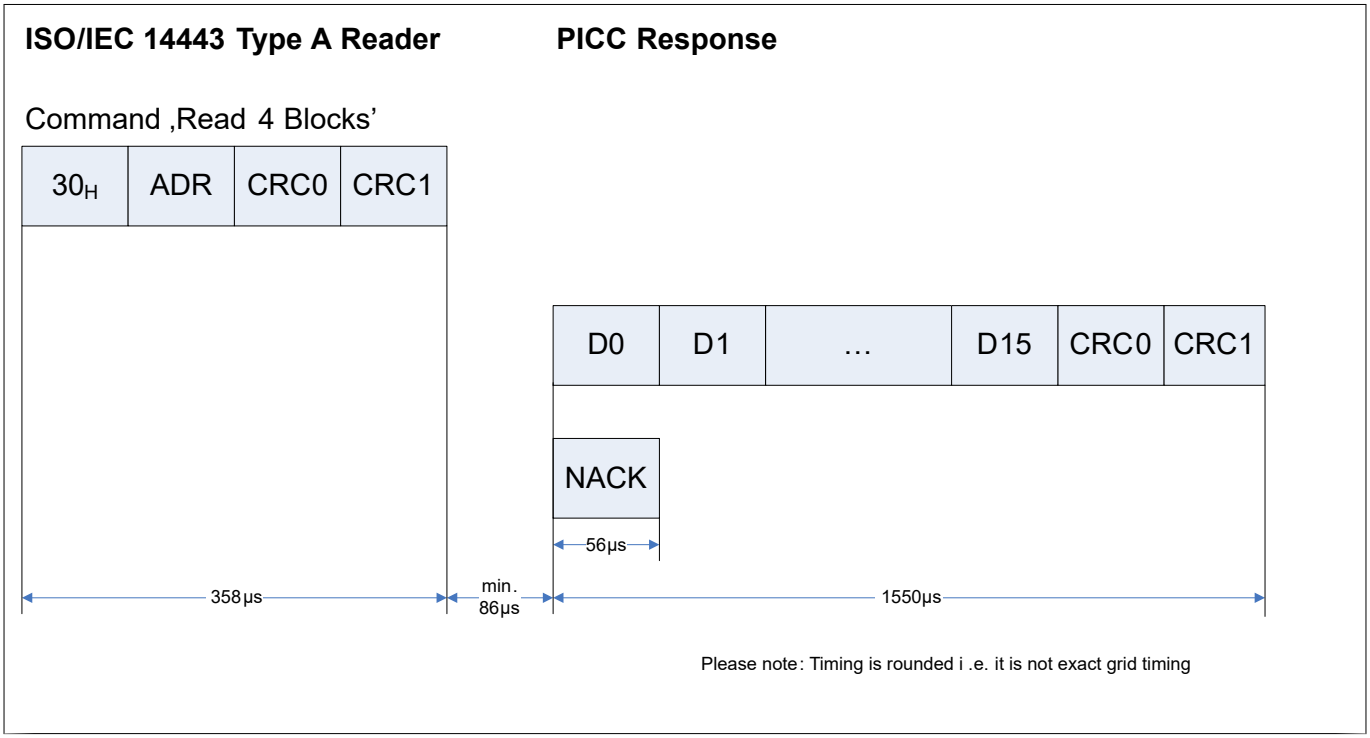

Figure 16 Read 4 Blocks command

7.2.2 Write 1 Block (WR1B)

If the write access is granted the WR1B command is used to program 4 bytes of data to the specified address in the memory. This command should be used to program OTP block and locking bytes as well.

The valid address range is from 02_H to $0F_H$. If any other address is specified the SLE 66R01L and SLE 66R01LN responds with a NACK.

Table 16 Write 1 Block (WR1B)

Command length	Code	Parameter	Data	Integrity mechanism	Response
8 bytes	$A2_H$	Valid address range 02_H - $0F_H$	4 bytes data	2 bytes CRC (1 parity bit per byte)	ACK or NACK or NR

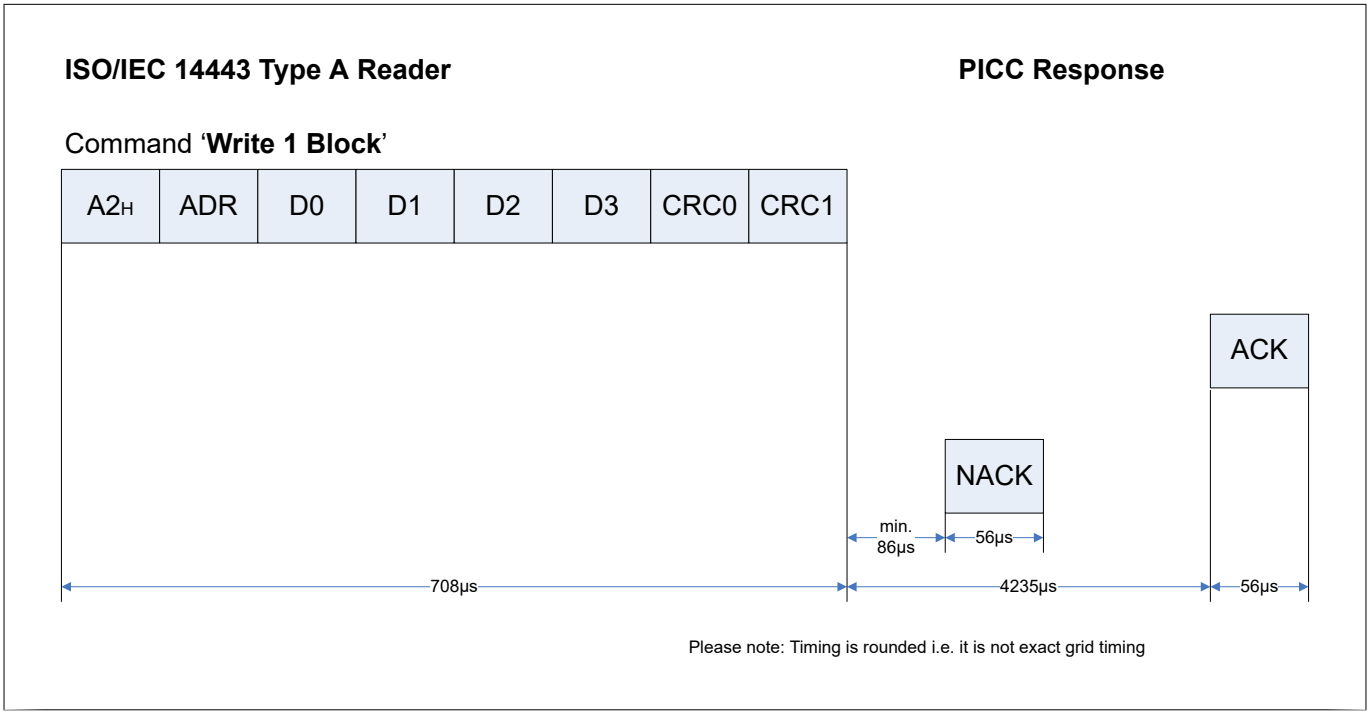

Figure 17 Write 1 Block command

7.2.3 Compatibility write command (CPTWR)

If the write access is granted only the four least significant 4 bytes are written to the specified address. The remaining bytes will be ignored by the SLE 66R01L and SLE 66R01LN. It is recommended to set the remaining bytes 04_H - $0F_H$ to 00_H.

Table 17 Compatibility write (CPTWR)

Command length	Code	Parameter	Data	Integrity mechanism	Response
20 bytes	$A0_H$	Valid address range 02_H - $0E_H$	16 bytes data	2 bytes CRC (1 parity bit per byte)	ACK or NACK or NR

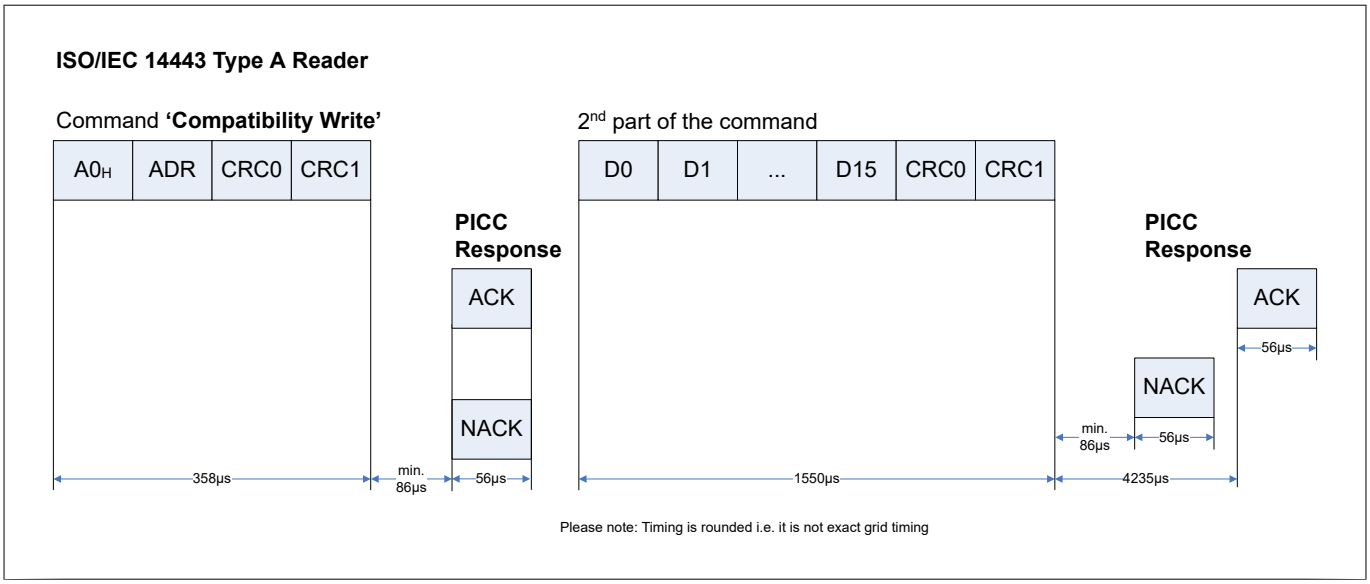

Figure 18 Compatibility write command

7.2.4 Read 2 Blocks (RD2B)

RD2B command reads 8 bytes out of the memory, starting from the specified address.

The valid address range is from 00_H to $0F_H$. If any other address is specified the SLE 66R01L and SLE 66R01LN responds with a NACK. A Roll-Back mechanism is implemented:

- If e.g. block $0F_H$ is addressed blocks $0F_H$ and 00_H are replied

Table 18 Read 2 Block (RD2B)

Command length	Code	Parameter	Data	Integrity mechanism	Response
4 bytes	31_H	Valid address range 00_H - $0F_H$	N.A.	2 bytes CRC (1 parity bit per byte)	8 bytes data +2 bytes data CRC or NACK Shift or NACK

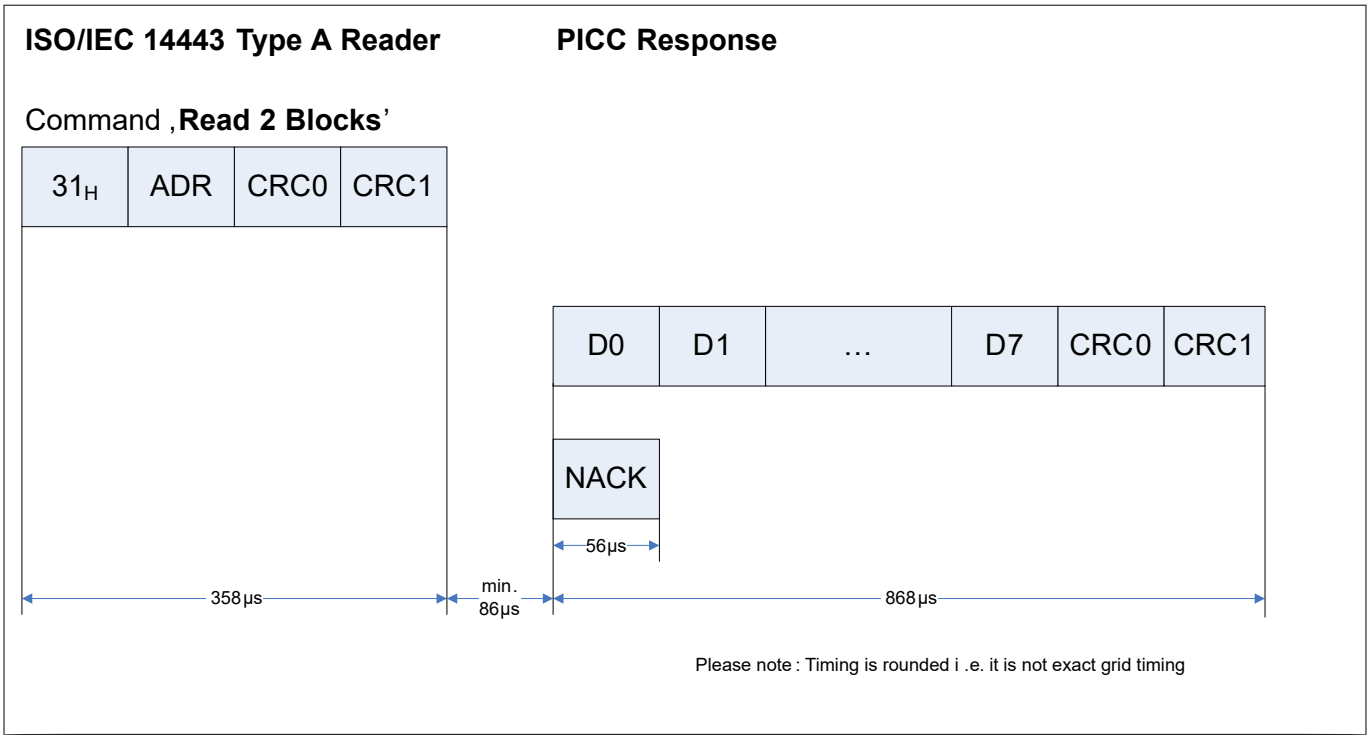

Figure 19 Read 2 Blocks command

7.2.5 Write 2 Blocks (WR2B)

If write access is granted, i.e. if both addressed blocks are writable, the WR2B command is used to program two blocks (8 bytes of data) to the specified address in the memory.

The valid address range is 04_H - $0E_H$. Only even start addresses are allowed. If any other address is specified, the SLE 66R01L and SLE 66R01LN responds with a NACK.

The WR2B command has the same programming time (approximately 4 ms) for writing 8 bytes as the WR1B command which writes 4 bytes of data to the specified memory.

Table 19 Write 2 Block (WR2B)

Command length	Code	Parameter	Data	Integrity mechanism	Response
12 bytes	$A1_H$	Valid address range 04_H - $0E_H$; only even start addresses allowed	8 bytes data	2 bytes CRC (1 parity bit per byte)	ACK or NACK or NR

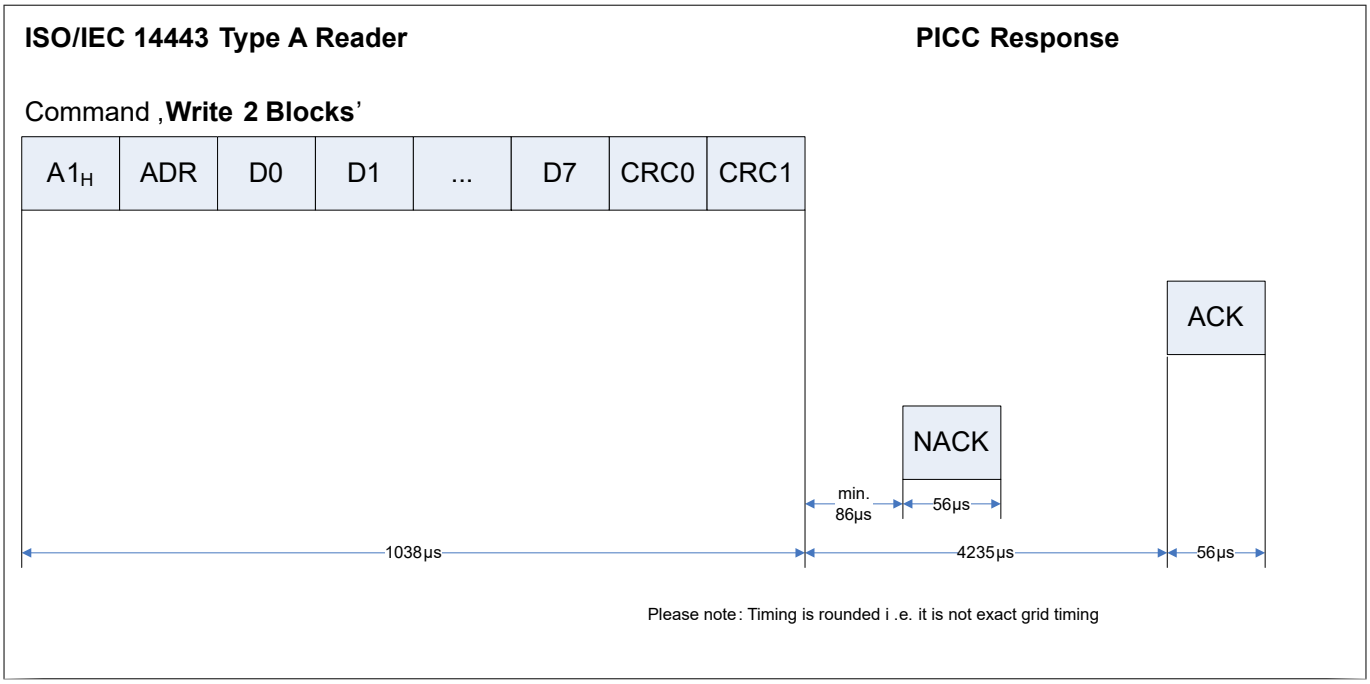

Figure 20 Write 2 Blocks command

7.2.6 HLTA command

The HLTA command is used to set the SLE 66R01L and SLE 66R01LN into the HALT state. The HALT state allows users to separate already identified chips. Contrary to the definition in the ISO/IEC 14443-3 Type A standard, the SLE 66R01L and SLE 66R01LN accept as a parameter the whole address range of 00_H to $0F_H$ with correct CRC for a proper execution of a HLTA command.

Table 20 Halt (HLTA)

Command length	Code	Parameter	Data	Integrity mechanism	Response
4 bytes	50_H	Valid address range 00_H - $0F_H$	N.A.	2 bytes CRC 1 parity bit per byte	NACK or NR

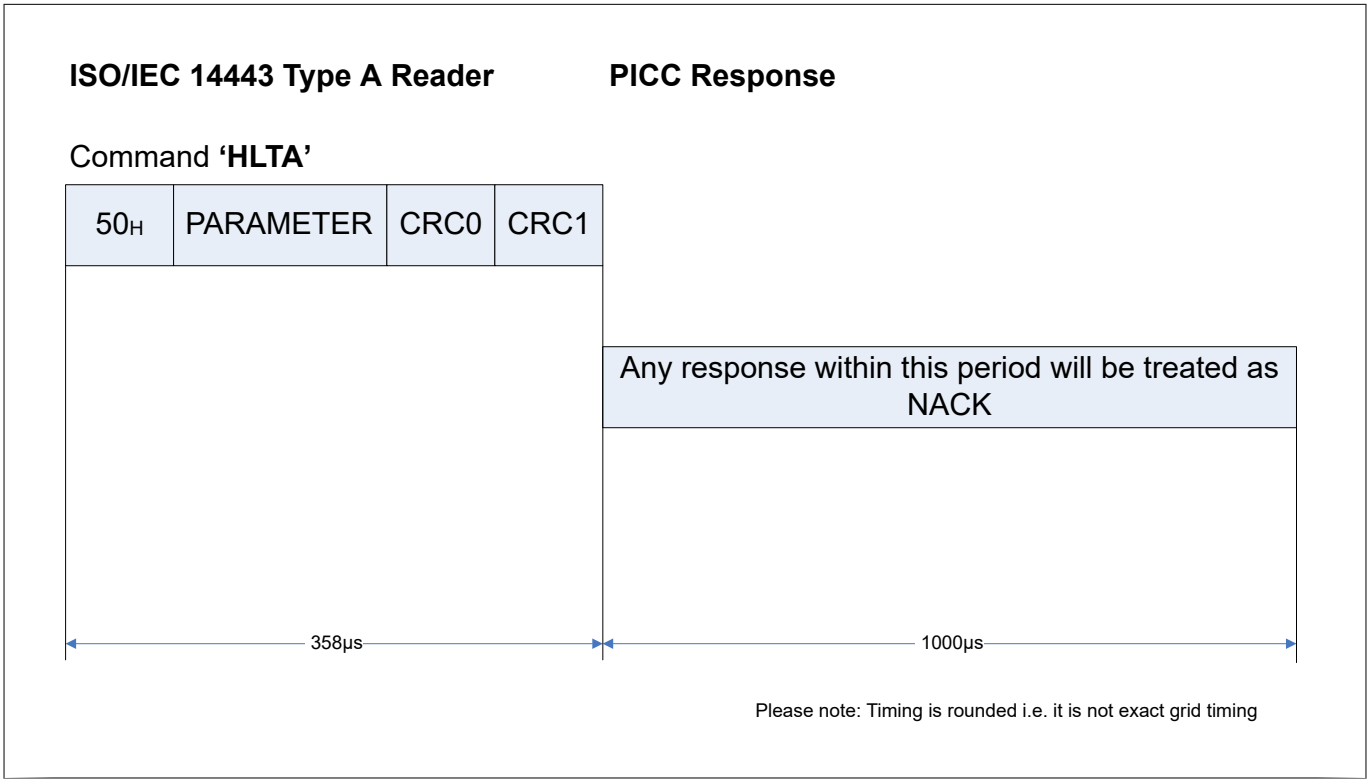

Figure 21 HLTA command

7.3 my-d™ move lean and my-d™ move lean NFC responses

The following sections list valid responses of the SLE 66R01L and SLE 66R01LN.

7.3.1 Command responses

The Acknowledge (ACK) and Not-Acknowledge (NACK) are command responses of the SLE 66R01L and SLE 66R01LN.

Table 21 ACK and NACK as responses

Response	Code (4 bits)	Integrity mechanism
ACK	1010_B (A_H)	N.A.
NACK0	0000_B (0_H)	N.A.

(table continues...)

Table 21 (continued) ACK and NACK as responses

Response	Code (4 bits)	Integrity mechanism
NACK1	0001_B (1_H)	N.A.
NR[1)]	N.A.	N.A.

1) Depending on the current state, the SLE 66R01L and SLE 66R01LN does not respond to some errors.

The response code is A_H for ACK and 0_H or 1_H for NACK. The ACK and NACK are sent as 4-bit response with no CRC and/or parity.

7.3.2 my-d™ move lean and my-d™ move lean NFC identification data

During the anti-collision the SLE 66R01L and SLE 66R01LN sends responses to the REQA and SEL commands.

Table 22 Summary of SLE 66R01L and SLE 66R01LN identification data

Code	Data	Description
ATQA	0044_H	Answer to request, response to REQA and WUPA command, hard coded 2 bytes. Indicates a double-size UID
SAK (cascade level 1)	04_H	Select Acknowledge answer to selection of 1st cascade level. Indicates that the UID is incomplete
SAK (cascade level 2)	00_H	Select Acknowledge answer to selection of 2nd cascade level. Indicates that the UID is complete
CT	88_H	Cascade Tag indicates that UID is not single size UID

8 Operational characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at ambient temperature T_A = 25°C and the given supply voltage.

8.1 Electrical characteristics

f_C = 13.56 MHz sinusoidal waveform, voltages refer to VSS.

Table 23 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Chip input capacitance L_A-L_B	C_{IN}	16.15	17	17.85	pF	$V_{AB\ peak}$ = 3.0 V, f_C = 13.56 MHz, T_A = 25°C
Chip load resistance L_A-L_B	R_{IN}	3	4.5	6	kΩ	$V_{AB\ peak}$ = 3.0 V, f_C = 13.56 MHz, T_A = 25°C
Endurance (erase/write cycles)[1)]		10^4				–
Data retention[1)]		5			Years	
EEPROM erase and write time	t_{prog}			3.8	ms	Combined erase + write; excluding time for command/response transfer between interrogator and chip, T_A = 25°C
ESD protection voltage (L_A, L_B pins)	V_{ESD}	2			kV	JEDEC STD EIA/JESD22 A114-B
Ambient temperature	T_A	-25		+70	°C	For chip
Junction temperature	T_J	-25		+110	°C	For chip

1) Values are temperature dependent.

8.2 Absolute maximum ratings

Stresses above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability, including EEPROM data retention and erase/write endurance. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit (IC). This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this Extended datasheet is not implied.

Table 24 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Input peak voltage between L_A-L_B	V_{INpeak}			6	V	
Input current through L_A-L_B	I_{IN}			30	mA	
Storage temperature	T_S	-40		+125	°C	

References

ISO/IEC

[1] ISO/IEC 18092:2013: *Information technology – Telecommunications and information exchange between systems – Near Field Communication – Interface and Protocol (NFCIP-1) (Second edition)*; 2013-03

[2] ISO/IEC 14443-1:2018: *Cards and security devices for personal identification - Contactless proximity objects - Part 1: Physical characteristics (Fourth edition)*; 2018-04

[3] ISO/IEC 14443-2:2020: *Cards and security devices for personal identification – Contactless proximity objects - Part 2: Radio frequency power and signal interface (Fourth edition)*; 2020-07

[4] ISO/IEC 14443-3:2018: *Cards and security devices for personal identification – Contactless proximity objects – Part 3: Initialization and anticollision (Fourth edition)*; 2018-07

[5] ISO/IEC 10373-6:2020: *Cards and security devices for personal identification — Test methods — Part 6: Contactless proximity objects*

NFC Forum

[6] NFC Forum: *Type 2 Tag Technical Specification (Version 1.2)*; 2021-09-27

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[7] *SLE66R01xx Wafer Specification*; 2021-07 https://www.infineon.com/dgdl/Infineon-Chip_Specification_SLE_66R01xx-AdditionalProductInformation-v01_00-EN.pdf

Glossary

CRC

cyclic redundancy check (CRC)
A procedure that uses a checksum to check the validity of a data transfer.

ECC

error correction code (ECC)
A method for controlling errors in data on an unreliable transfer channel. The sender adds an ECC redundancy information and the receiver is able to verify the data and correct a limited amount of errors.

EEPROM

electrically erasable programmable read-only memory (EEPROM)

ESD

electrostatic discharge (ESD)
The sudden draining of electrostatic charge. Even with small charges, it poses a considerable risk to small semiconductor structures, in particular MOS structures. It is therefore essential to take precautions when dealing with unprotected semiconductors.

FDT

frame delay time (FDT)

IC

integrated circuit (IC)

IEC

International Electrotechnical Commission (IEC)
The international committee responsible for drawing up electrotechnical standards.

ISO

International Organization for Standardization (ISO)

LSB

least significant byte (LSB)

MAC

message authentication code (MAC)
Used to prove message integrity.

MSB

most significant byte (MSB)

NFC

near field communication (NFC)

PCD

proximity coupling device (PCD)
A reader device for NFC cards.

PICC

proximity integrated circuit card (PICC)
A contactless smart card which can be read without inserting it into a reader device.

RFU

reserved for future use (RFU)

RoHS

Restriction of Hazardous Substances in Electrical and Electronic Equipment (RoHS)
EU rules restricting the use of hazardous substances in electrical and electronic equipment to protect the environment and public health.

SMD

surface-mounted device (SMD)

TLV

tag length value (TLV)

TSNP

thin small no-lead package (TSNP)

UID

unique identifier (UID)

Revision history

Reference	Description
Revision 4.0, 2023-08-14	
All	• Updated Sales codes and delivery forms and References • Added SMD package details and RoHS compliance
Revision 3.1, 2022-08-12	
Application segments	Updated Table 5
Revision 3.0, 2021-12-21	
All	• Migrated to latest IFX template and updated editorial changes • Added About this document, References, glossary entries
Revision 2.0, 2019-06-26	
All	• Update on the trademarks • Removed “Preliminary” term
Revision 1.0, 2012-10-25	
All	Initial release

RoHS compliance

On January 27, 2003 the European Parliament and the council adopted the directives:

- 2002/95/EC on the Restriction of the use of certain Hazardous Substances in electrical and electronic equipment ("RoHS")
- 2002/96/EC on Waste Electrical and Electrical and Electronic Equipment ("WEEE")

Some of these restricted (lead) or recycling-relevant (brominated flame retardants) substances are currently found in the terminations (e.g. lead finish, bumps, balls) and substrate materials or mold compounds.

The European Union has finalized the Directives. It is the member states' task to convert these Directives into national laws. Most national laws are available, some member states have extended timelines for implementation. The laws arising from these Directives have come into force in 2006 or 2007.

The electro and electronic industry has to eliminate lead and other hazardous materials from their products. In addition, discussions are on-going with regard to the separate recycling of certain materials, e.g. plastic containing brominated flame retardants.

Infineon is fully committed to giving its customers maximum support in their efforts to convert to lead-free and halogen-free[2)] products. For this reason, Infineon's "Green Products" are ROHS-compliant.

Since all hazardous substances have been removed, Infineon calls its lead-free and halogen-free semiconductor packages "green." Details on Infineon's definition and upper limits for the restricted materials can be found here.

The assembly process of our high-technology semiconductor chips is an integral part of our quality strategy. Accordingly, we will accurately evaluate and test alternative materials in order to replace lead and halogen so that we end up with the same or higher quality standards for our products.

The use of lead-free solders for board assembly results in higher process temperatures and increased requirements for the heat resistivity of semiconductor packages. This issue is addressed by Infineon by a new classification of the Moisture Sensitivity Level (MSL). In a first step the existing products have been classified according to the new requirements.

2 Any material used by Infineon is PBB and PBDE-free. Plastic containing brominated flame retardants, as mentioned in the WEEE directive, will be replaced if technically/economically beneficial.

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