Arm® Cortex®-M33 32-bit MCU+FPU+DSP, 180 MHz, up to 512 KB Flash/128 KB SRAM, Real-time Control

Features

- High-performance, low-power 32-bit single-core Arm® Cortex® M33-based microcontroller with digital signal processor (DSP), floating-point unit (FPU), and state-of-the-art security features; 512 KB Read-While-Write (RWW) Flash with ECC support, and 128 KB SRAM with ECC support
- High-performance, programmable analog subsystem (HPPASS):
  - 1 x 12-bit, 9-Msps SAR ADC supporting up to 24 inputs on 16 parallel idle samplers; 16 dedicated analog inputs and up to 8 analog-capable GPIOs
  - Up to 9 x comparators with <11 ns built-in 10-bit DAC and slope generator
  - Up to 4 x OpAmps, 2 x 12-bit DAC, 3x 3P3Z hardware filter
- Real-time control peripherals:
  - Coordinate rotation digital computer (CORDIC)
  - 16 x 16-bit and 8 x 32 bit timer/counter pulse-width modulator (TCPWM) supporting <100 ps high-resolution pulse-width modulator (HRPWM); 2 x MOTIF
- Communication interfaces: 6x serial communication blocks (SCBs), including 1x SCB with PMBus support, 1x I3C, up to 1x USB FS host/device and up to 2x CAN FD
- Low-power operation modes down to 300 nA: Sleep, Deep Sleep (three modes) and Hibernate
- Up to 86 functional pins: 16 dedicated analog pins; 70 GPIOs with programmable drive modes, strengths, and slew rates, which includes up to 8 analog-capable GPIO pins
- Up to 7x Smart I/O programmable logic blocks supporting 30 Smart I/O capable pins
- Security: Cryptolite (SHA-2, VU, TRNG), AES; PSA L3 ready, DICE ready, and PQC support
- Safety: Class B and SIL 2 capable
- Packages: E-LQFP-64, E-LQFP-80, E-LQFP-100, with T_A = - 40°C to 115°C

Green

Halogen-free

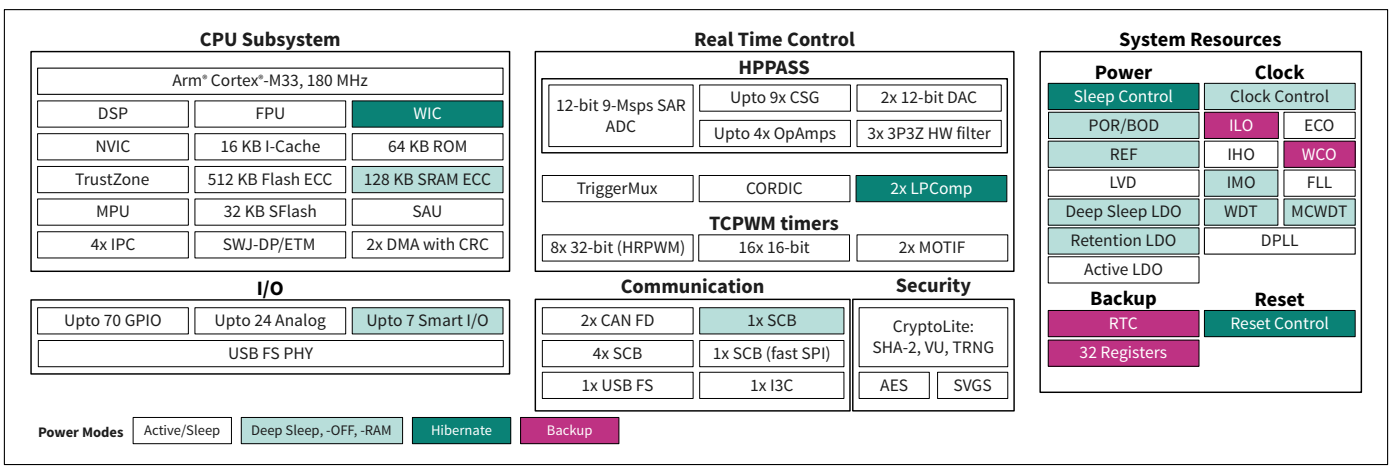
Lead-free

Potential applications

- Motor control in power tools, home appliances, industrial drives, light electric vehicles, robotics, and drones
- Digital power control in switched mode power supply (SMPS) and PFC applications for LED lighting, EV chargers, solar inverters, servers, and PC power supplies
- Wide bandgap technologies (e.g., SiC and GaN) based motor control and power conversion applications

Description

The PSC3M/P6 devices are based on the Arm® Cortex®-M33 running up to 180 MHz with DSP and FPU capability. In addition to the CPU subsystem, the devices contain advanced real-time control peripherals, such as high-performance programmable analog subsystem with ADC, DAC, OpAmps; comparators, advanced timers with high-resolution capability. The devices support one Active and five low-power modes for managing and reducing the power consumption depending on application requirements.



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1 Introduction

The PSC3M6 and PSC3P6 devices are part of the PSC3M/P6 MCU family designed for real-time control, enhanced sensing, secure, and low-power operations. Some target applications for these microcontrollers are:

- Industrial motor-controllers
- Power-stage converters
- Home appliances
- Automation devices
- Low-power sensors

A detailed block diagram of the MCU is shown in Figure 1.

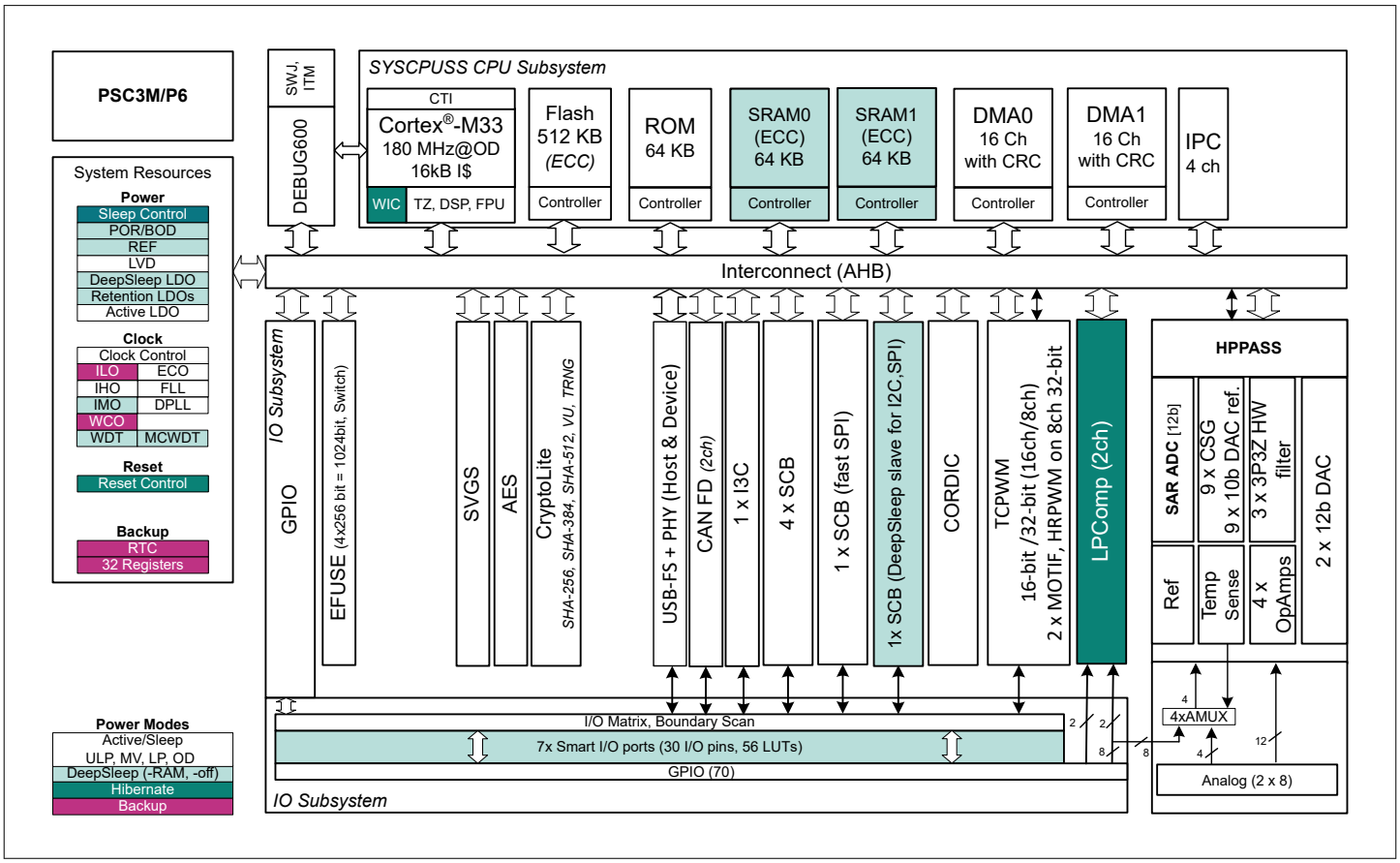


Figure 1 Functional block diagram

Device identification and revisions

Family ID = 0x124(12-bit); Si ID range = F100 - F13F; Major-minor rev ID = 0x1, 0x1

2 Detailed features

This device has the following features:

- CPU subsystem
  - Arm® Cortex®-M33 running up to 180 MHz
  - Digital signal processor (DSP), floating-point unit (FPU), memory protection unit (MPU), 16 KB I-cache
  - 2x 16-channel direct memory access (DMA) controllers with configurable cyclic redundancy check (CRC)
- Memory
  - On-chip flash with ECC support
    - Up to 512-KB flash with read while write (RWW) capability, 64 KB ROM for boot code, and bootloader functions
    - Built-in device firmware upgrade (DFU) support in boot ROM via serial interface (UART/I2C/SPI)
  - Up to 128 KB SRAM with ECC support
    - Full SRAM available in Deep Sleep
    - SRAM data path is protected with a hardware mechanism (ECC) for soft error detection and correction
- Security
  - Platform security architecture level 3 (PSA L3) ready
  - TrustZone framework that establishes an isolated device root of trust (RoT) for trust attestation and software management
  - Step-wise authentication of execution images until the control is handed over to the user code
  - Image authentication and integrity check
  - Cryptography accelerator
    - Hardware acceleration for symmetric (AES-128, AES-256) and asymmetric cryptographic algorithms (RSA and elliptic curve cryptography (ECC)) supported by vector unit (VU) and hash functions (SHA-256, SHA-384, SHA-512)
    - Signature verification: ECDSA NIST P-256, ECDSA NIST P-384 (Default), ECDSA NIST P-521 , LMS SHA256_M32_H10, XMSS-SHA2_10_256
    - True random number generator (TRNG) function
  - Post-quantum cryptography (PQC) algorithm support for ML_DSA and ML_KEM using wolfSSL crypto library
  - DICE ready: Device identifier composition engine (DICE) mechanism support
- Clocking subsystem
  - 8 MHz IMO with Deep Sleep operation offering ±2% accuracy
  - 48 MHz internal high-frequency oscillator (IHO) offering ±1% accuracy
  - 32 kHz internal low frequency oscillator (ILO) offering ±10% accuracy
  - 4 to 36 MHz external crystal oscillator (ECO) support
  - 32.768 kHz external watch crystal oscillator (WCO) usable for real-time clock (RTC)
  - External clock (EXTCLK): Maximum frequency 80 MHz
  - One frequency lock loop (FLL) with 24-100 MHz output range
  - One digital phase-locked loops, DPLL#0, with 25-240 MHz output range
- Low power (1.71 V to 3.63 V) operation
  - Six power modes (Active, Sleep, Deep Sleep, Deep Sleep-RAM, Deep Sleep-OFF, and Hibernate) for fine-grained power management
  - Four power profiles (Ultra Low Power, Medium Frequency, Low Power, Overdrive) to optimize speed vs power consumption in Active mode

- Communication peripherals
  - Serial communication blocks (SCBs)
    - 6x independent run-time-reconfigurable SCBs; each software-configurable as I2C, SPI, or UART in master or slave mode
    - 1x SCB supports Deep Sleep operation and wake-up from Deep Sleep in I2C slave and SPI slave modes
    - 1x SCB supports fast SPI operation at up to 50 MHz
    - All SCBs support single-wire, half-duplex UART mode
    - 1x SCB additionally supports PMBus protocol:
      - Baud rates of up to 1 Mbps
      - Timeout event generation (TGS) for wrong or stuck commands
      - Hardware address screening with support for a minimum of five slave address masks (MSAs) to reject or NACK incoming address commands
      - Compliance with PMBus (v1.4) and SMBus (v3.2) specifications
  - CAN FD
    - Up to 2x CAN FD; 1 instance supports 8 Mbps operation
  - Up to 1x Universal serial bus full-speed host and device with USB PHY
  - 1x I3C interface with over-voltage-tolerant (OVT) I/O support
- High-performance, programmable analog subsystem (HPPASS)
  - Analog-to-digital converter (ADC)
    - 1x 12-bit, 9-Msps SAR ADC with support up to 24 analog inputs
    - 16x parallel sample/hold (S/H) stages supporting simultaneous idle sampling of up to 16 inputs; 12x direct samplers and 4x multiplexed samplers
    - Up to 8 additional GPIOs can be used as ADC inputs
    - 4x multiplexed samplers can be connected to:
      - Dedicated analog pads
      - Analog-capable GPIOs
      - OpAmp outputs
      - Internal references and internal temperature sensor
    - Configurable input gain of 1×, 3×, 6×, and 12× on all 16 S/H circuits
    - Up to 4x OpAmps for signal amplification and conditioning
    - 2x 12-bit R2R DACs. DAC output can be connected to OpAmp inputs or to dedicated analog pin
    - Digital comparator at the output to compare the ADC result against programmed boundary values
    - Digital comparator outputs can be connected to timer/counter pulse-width modulator (TCPWM) (low latency between the modules)
  - Comparator with slope generator (CSG)
    - Up to 9x Active comparators without Deep Sleep functionality, each with a 10-bit DAC to generate the comparator reference
    - Each comparator supports an external reference/threshold through pins
    - Active comparator can be used with the built-in DAC in Hysteresis mode
    - Comparator outputs can be brought to pins for control loop applications
    - Comparator outputs can be connected to TCPWM (low latency between the modules)
    - Logical OR of multiple comparator trigger outputs connected as an input trigger to TCPWM via triggerMUX

- Low-power comparator (LPComp):
  - 2x comparators in LPComp are available in Active, Deep Sleep, and Hibernate modes
  - Comparator inputs and outputs can be connected to external pins; outputs can also be routed internally to TCPWM
  - Option to internally route same signal to multiple comparator inputs
  - Internal fixed reference voltage of 0.6 V ± 0.2 V can be connected to inverting input of the comparators
- Real-time control peripherals
  - Coordinate rotation digital computer (CORDIC)
    - Supports all CORDIC operating modes for solving circular (trigonometric), hyperbolic functions, and integrated independent lookup tables to accelerate calculation
  - Timer/counter pulse-width modulator (TCPWM)
    - 16 x 16-bit TCPWM channels
    - 8 x 32-bit TCPWM channels supporting high-resolution PWM generation (HRPWM) for PWM outputs
    - Center-aligned, edge, and pseudorandom modes
    - Comparator-based triggering of kill signals
    - Shadow update of duty, period, dead-time, output signal polarity, and dithering (pseudorandom mode)
    - Multichannel control: In a group of eight TCPWM channels, one channel within a group can trigger another channel
    - Ability to logically combine the outputs of multiple channels through Smart I/O
    - Dedicated output triggers mux in a group to allow flexibility to the PWM channel as a trigger and/or gate signals to the HPPASS
    - HRPWM feature for period, duty, and dead-time insertion
    - 2x motion interface (MOTIF) supporting:
      - Standalone multi-channel mode
      - Hall sensor interface with autonomous BLDC block commutation support
      - Quadrature encoder interface to decode motor speed and rotor position
- I/O subsystem
  - Programmable GPIO pins
    - Up to 86 functional pins (70 GPIOs; 8 out of 70 GPIOs can be used for analog inputs + 16 dedicated analog-only inputs)
    - Programmable drive modes, strengths, and slew rates
  - Programmable digital
    - Up to 7 Smart I/O-capable ports (30 I/Os, 56 LUTs) enable Boolean operations on I/O signals

3 Chip-level functional description

3.1 Power

The device offers multiple features for managing and reducing power draw. Multiple power modes include Active, Sleep, Deep Sleep, and Hibernate. Deep Sleep has three variations based on retention of SRAM.

The power control block provides assurance that voltage levels meet the requirements of the respective modes. It can:

- Delay mode entry (for example, at power-on reset (POR)) until voltage levels are as required for proper functioning
- Detect operation below safe power supply levels:
  - Generates interrupts for low-voltage detection (LVD)
  - Generates reset for brownout detection (BOD)

The device operates using a single regulated VDDD supply within the range of 1.71 V to 3.63 V. In addition, there is an optional VBACKUP supply that can be used, which has a range of 1.4 V to 3.63 V. A linear regulator powers the core logic at four voltage levels: 0.9 V, 1.0 V, 1.1 V, and 1.2 V. Voltage level switching is implemented by writing to the power control registers. The voltage for the core logic can be set based on the application's performance and power requirements; (see Power modes). With clock gating at peripheral and bus levels, this permits fine-grained optimization of energy usage.

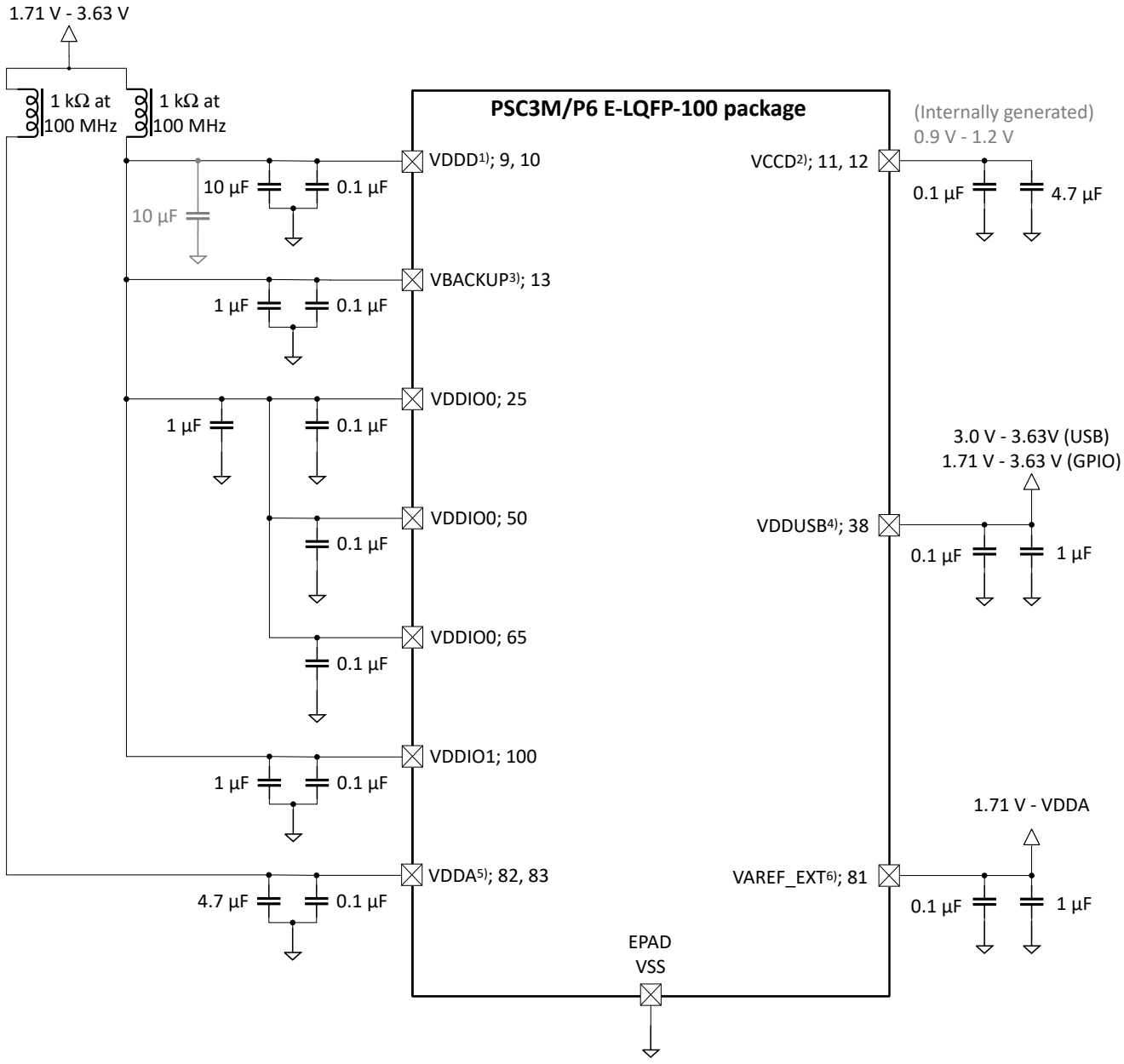
Typically, the backup domain requires an input voltage of 1.4 V to 3.63 V, which can be provided by connecting a backup battery or a super capacitor to the VBACKUP pin. The internal backup switch automatically selects between VDDD and VBACKUP (when VDDD is no longer available) for powering the backup domain peripherals like RTC, WCO, ILO, and Backup registers. Some I/O cells are powered from the VBACKUP supply before the internal backup switch. If the application does not require a dedicated backup source, VBACKUP can be connected to VDDD externally to ensure that the I/O cells powered by VBACKUP are functional.

The device has multiple VDDIO pins that are used to power the I/O cells except the backup domain I/O cells. VDDIO can either be connected to the same supply as VDDD or an independent supply voltage within the valid operating range. This provides more flexibility in terms of choosing the logic level for the port pins powered using different VDDIO supplies. The VDDIO supply can be switched off if the port I/Os are not used. Switching off the VDDIO supply is only allowed in Active or Deep Sleep mode. VDDIO should not be switched off when the device is in Hibernate mode. Refer to the Pins section for information about the VBACKUP or VDDIO supply used for powering the port I/O cells.

3.1.1 Power connections

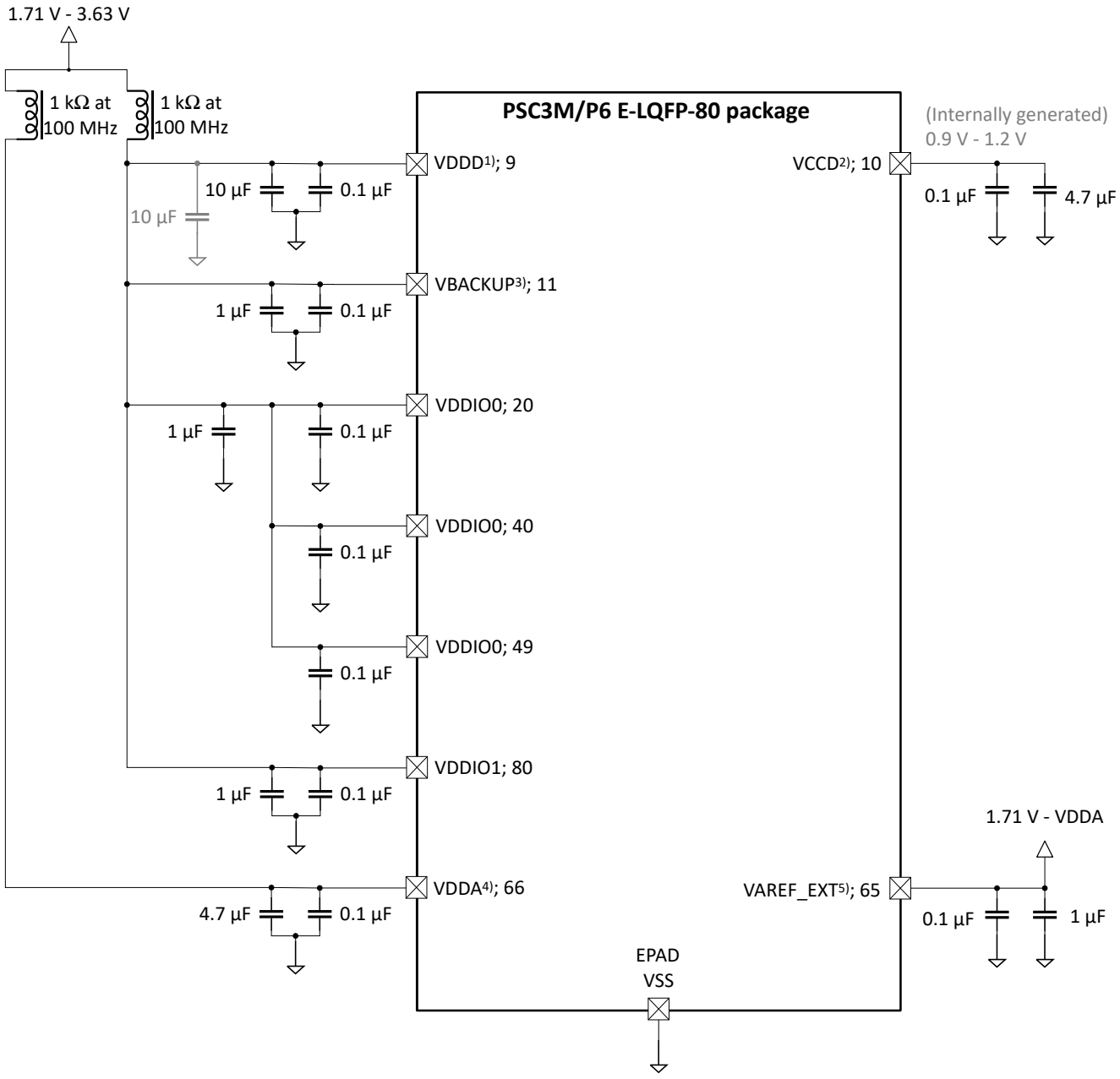
The following power system diagrams show typical connections for the power pins for all the supported packages. In these diagrams, the package pin is shown with the pin name, for example, "VDDD; 9, 10" in Figure 2.

There is no dependency on power supply sequencing.



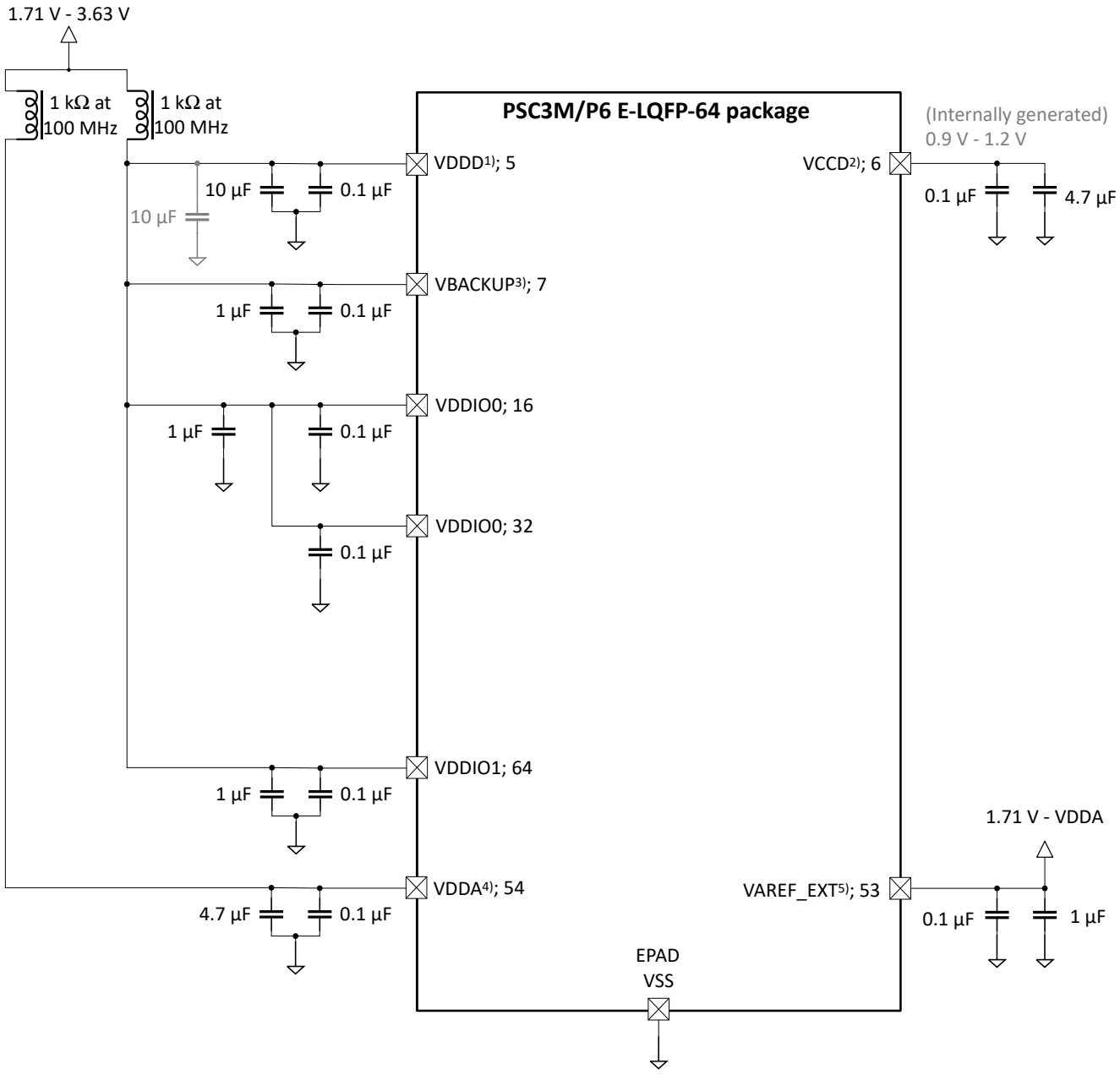
1) A 10 µF capacitor on VDDD supports full operating voltage range for Active/Hibernate modes and Deep Sleep with VDDD ≥ 2.3 V. Use 2x10 µF capacitors or a single 22 µF capacitor for Deep Sleep operation down to 1.71 V.
2) VCCD is internally generated. It is only used to connect external bypass capacitors for the internal LDO. Do not use it to power external circuits.
3) VBACKUP can be connected to a coin cell (1.4 V to 3.63 V) or a supercapacitor depending on the application. If not used, connect it to VDDD.
4) VDDUSB powers the USB PHY (DP and DM lines) or the Port 11 I/O cells for devices without USB support.
5) VDDA should be ≥ 2.7 V to run HPPASS at the highest supported clock speed of 180 MHz.
6) VAREF_EXT can either be connected to a dedicated reference voltage generator (1.71 V to VDDA) or to VDDA externally.

Figure 2 E-LQFP-100 package power connections



1) A 10 µF capacitor on VDDD supports full operating voltage range for Active/Hibernate modes and Deep Sleep with VDDD ≥ 2.3 V. Use 2x10 µF capacitors or a single 22 µF capacitor for Deep Sleep operation down to 1.71 V.
2) VCCD is internally generated. It is only used to connect external bypass capacitors for the internal LDO. Do not use it to power external circuits.
3) VBACKUP can be connected to a coin cell (1.4 V to 3.63 V) or a supercapacitor depending on the application. If not used, connect it to VDDD.
4) VDDA should be ≥ 2.7 V to run HPPASS at the highest supported clock speed of 180 MHz.
5) VAREF_EXT can either be connected to a dedicated reference voltage generator (1.71 V to VDDA) or to VDDA externally.

Figure 3 E-LQFP-80 package power connections



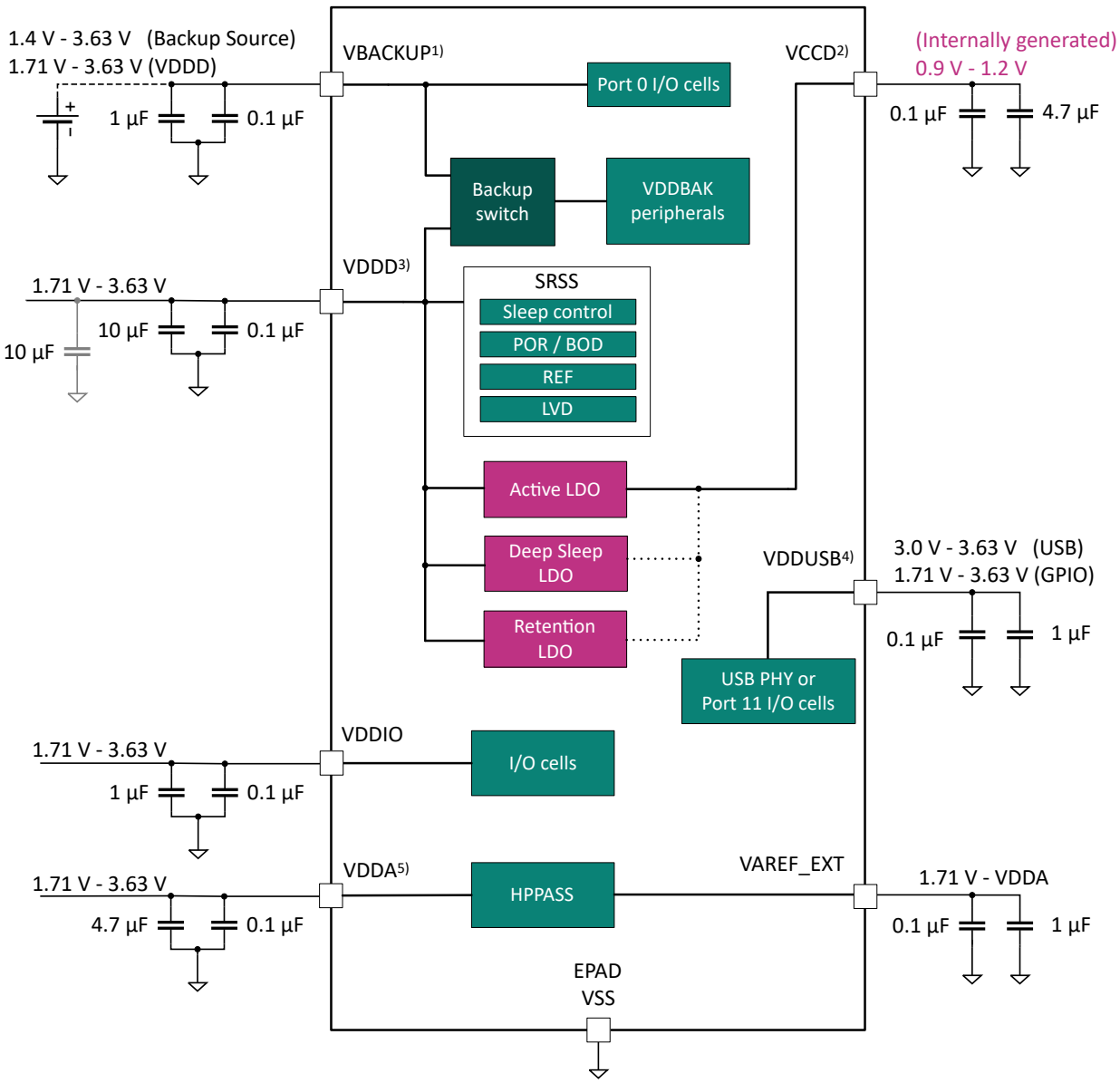
1) A 10 µF capacitor on VDDD supports full operating voltage range for Active/Hibernate modes and Deep Sleep with VDDD ≥ 2.3 V. Use 2x10 µF capacitors or a single 22 µF capacitor for Deep Sleep operation down to 1.71 V.
2) VCCD is internally generated. It is only used to connect external bypass capacitors for the internal LDO. Do not use it to power external circuits.
3) VBACKUP can be connected to a coin cell (1.4 V to 3.63 V) or a supercapacitor depending on the application. If not used, connect it to VDDD.
4) VDDA should be ≥ 2.7 V to run HPPASS at the highest supported clock speed of 180 MHz.
5) VAREF_EXT can either be connected to a dedicated reference voltage generator (1.71 V to VDDA) or to VDDA externally.

Figure 4 E-LQFP-64 package power connection

3.1.2 Power domains

The device has independent power domains, allowing the domain power to be enabled/disabled depending on the power mode.

A diagram of the power connections and routing is shown in Figure 5:



1) VBACKUP can be connected to a coin cell (1.4 V to 3.63 V) or a supercapacitor, depending on the application. If not used, it should be connected to VDDD.
2) VCCD is internally generated. It is only used to connect external bypass capacitors for the internal LDO. Do not use it to power external circuits.
3) A 10 µF capacitor on VDDD supports full operating voltage range for Active/Hibernate modes and Deep Sleep with VDDD ≥ 2.3 V. Use 2x10 µF capacitors or a single 22 µF capacitor for Deep Sleep operation down to 1.71 V.
4) VDDUSB powers the USB PHY (DP and DM lines) or the Port 11 I/O cells for devices without USB support.
5) VDDA should be ≥ 2.7 V to run HPPASS at the highest supported clock speed of 180 MHz.

Figure 5 Power distribution and domains

3.1.3 Power modes

The device can operate in five power modes. These power modes are intended to minimize the average power consumption in an application.

Power modes supported are:

- **Active/Sleep:** All peripherals are powered. The CPU is either active and executing the code or can be put in sleep (clock gated). Any interrupt can wake up the CPU within one CPU clock cycle to resume operation. In Active/Sleep

mode, the core voltage can be set to any of the four values. This impacts both power consumption and maximum clock frequency for CPU and peripherals. The following power profiles are supported in Active/Sleep mode:

- ULP (Ultra Low Power): 0.9 V core voltage with 50 MHz CPU frequency
- MF (Medium Frequency): 1.0 V core voltage with 70 MHz CPU frequency
- LP (Low Power): 1.1 V core voltage with 150 MHz CPU frequency
- OD (Overdrive): 1.2 V core voltage with 180 MHz CPU frequency

- **Deep Sleep:** The CPU is in retention mode. SRAM content is also retained[1]. Only Deep Sleep capable peripherals can wake up the system. Once awake, the operation resumes
- **Deep Sleep-RAM:** The CPU is turned off. SRAM is retained[1] for a warm boot after wake-up. Only Deep Sleep-capable peripherals are operational if enabled and are capable of waking up the system
- **Deep Sleep-OFF** Same as Deep Sleep RAM except RAM is also turned off. The wake-up action is reset or cold boot
- **Hibernate:** All peripherals except backup domain peripherals such as RTC is turned off. All clocks except the backup domain clock and all internal regulators are turned off. The system is reset when it exits the Hibernate mode

3.1.4 Power mode transitions

The device supports Arm® standard power modes; see the Power modes section for details. Table 1 lists the parameters for supported power modes:

Table 1 Power mode support

	Active/Sleep	Deep Sleep	Deep Sleep-RAM	Deep Sleep-OFF	Hibernate	Off
Parameters						
Wake source[1]	Any interrupt	DS peripherals	DS peripherals	DS peripherals	RTC/HIB peripherals	Power on
Wake action	Resume	Resume	Warm boot	Reset/cold boot	Reset	Reset
Wake time	One CPU cycle	<100 µs	Deep Sleep + warm boot	Deep Sleep + cold boot	POR + cold boot < 1 ms	
Resources						
ECO	On/Off	Off	Off	Off	Off	Off
IHO	On	Off	Off	Off	Off	Off
IMO	On	On/Off	Off	Off	Off	Off
ILO	On/Off	On/Off	On/Off	On/Off	On/Off	Off
WCO	On/Off	On/Off	On/Off	On/Off	On/Off	Off
CPU	On/Sleep	Retention	Off	Off	Off	Off
SRAM	On	On	On/Off	Off	Off	Off

1) See Table 2 for the list of peripherals available in DS (Deep Sleep) and HIB (Hibernate) power modes.

1 There is one power switch per SRAM controller, which allows a retention granularity of 64 KB and 128 KB

3.1.5 Power block support

Table 2 shows the available operational states for the major blocks in this device. Note that the operational states possible in low-power modes are generally limited in functionality and parametric performance as compared to their capabilities in the Active power mode. Additionally, blocks that do not support low-power modes such as Deep Sleep and Hibernate cannot wake up the CPU from these power modes. See Power modes for details.

Table 2 Block power modes

Block	Power mode				
	Active	**Sleep**	**Deep Sleep**	**Hibernate**	**Backup**
CPUSS					
CPU	Y	N	N	N	N
NVIC	Y	Y	N	N	N
WIC	Y	Y	Y	Y	N
FLASH	Y	Y	N	N	N
SRAM	Y	Y	Y	N	N
DMA	Y	Y	N	N	N
Programmable digital					
SMART I/O	Y	Y	Y	N	N
Fixed function digital					
TCPWM	Y	Y	N	N	N
SCB	Y	Y	Y[1)]	N	N
USB FS	Y	Y	N[2)]	N	N
I3C	Y	Y	N	N	N
CAN FD	Y	Y	N	N	N
Special function					
CORDIC	Y	N	N	N	N
Analog					
HPPASS (SAR, CSG, AFE, 3P3Z, DAC)	Y	Y	N	N	N
LPComp	Y	Y	Y	Y	N
I/O					
GPIO	Y	Y	Y	Y[3)]	N
Backup					
RTC	Y	Y	Y	Y	Y
Registers	Y	Y	Y	Y	Y

1) Only SCB 0 (I2C, SPI)
2) Supports wake-up
3) Only hibernate_wakeup pins (P2.0 and P9.0) are operational and capable of waking up the device from Hibernate mode. For more information, see the Pins section.

3.2 Security

This product line features an Arm® TrustZone-enabled Cortex®-M33 CPU. It offers an isolated, fully secured, hardware-based Root of Trust (RoT) that supports secure boot, provisioning, and secure debugging.

Both secure and non-secure debug accesses are supported. In non-secure access, the debugger cannot access areas marked as “secure”. For secure access, the device can be “locked”, preventing it from being acquired for testing or debugging. A debug token ensures appropriate access for secure debugging and RMA transitions.

This device is fully compliant with Arm® TrustZone at both hardware and software levels. An additional layer of security is implemented using Infineon-proprietary protection units.

PSA L3-certified components support PSA-compliant cryptographic services, key management, and secure storage services.

***Note**: PSA Level 3 capable only applies to 512 KB Flash variants. Refer Ordering information for details.*

3.2.1 Security features

- **Arm® platform security architecture**: PSA Level 3 capable
- **Secure boot and debug**: Support for secure boot, secure firmware updates, secure debug, and secure RMA mode for field failure analysis
- **Protected firmware features**: Firmware protection based on the part number
- **Hardware crypto accelerator**: Comprehensive support for cryptographic algorithms
- **Secure processing isolation**: Secure isolation of processing environments achieved via Arm® TrustZone
- Infineon-proprietary MPU, MPC, and PPCs for memory and peripheral access control
- **Trusted Firmware-M (TF-M)**: Off-the-shelf secure isolation using Trusted Firmware-M (TF-M) and mbedTLS cryptographic acceleration package
- **Post-quantum cryptography (PQC)**: Supports post-quantum cryptography (PQC) for secure boot and authenticated firmware updates, with ready-to-use PQC libraries for application integration

3.2.2 Security architecture overview

This product line features an Arm® TrustZone-enabled Cortex®-M33 CPU as shown in Figure 6.

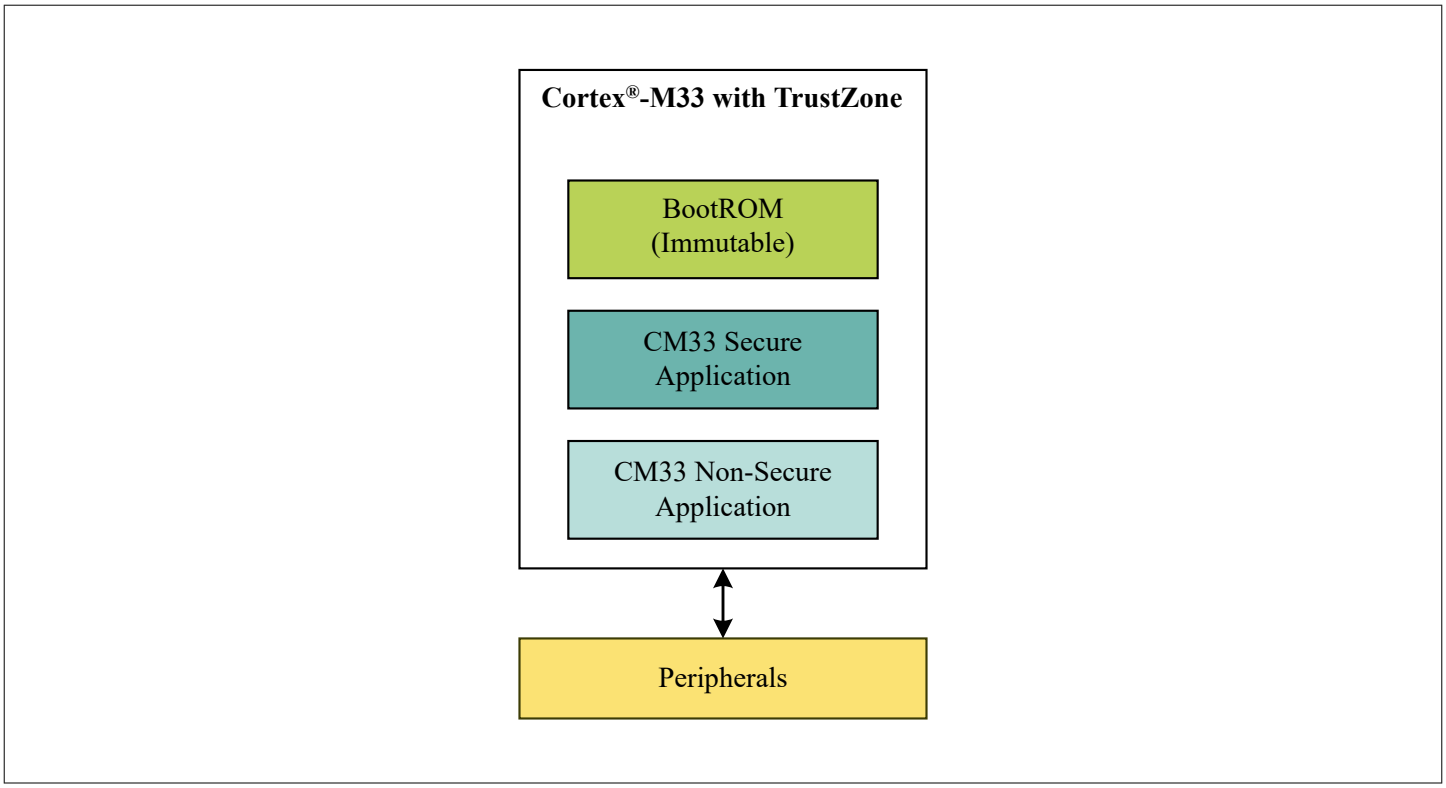


Figure 6 Security architecture diagram

4 Block functional description

4.1 CPU

- Arm® Cortex®-M33 with digital signal processor (DSP)
- Floating-point unit (FPU)
- The TrustZone framework establishes an isolated device root of trust for trusted attestation and software management
- Memory protection unit (MPU): Supports eight regions each for secure and nonsecure MPUs
- Secure attribution unit (SAU): It defines the security status of up to eight memory regions
- Debug facilities including trace (embedded trace macrocell (ETM), no embedded trace buffer (ETB))
- 16 KB I-cache for flash and ROM access

Two separate 4-channel interprocessor communication (IPC) modules (two IRQs each) offers seamless support for semaphores and mailbox structures within secure and nonsecure execution.

The subsystems include an interrupt controller such as a nested vectored interrupt controller (NVIC). It also consists of a wake-up interrupt controller (WIC), which can wake the processor up from system Deep Sleep mode, allowing the main processor power and clocks to be turned-off when the chip is in system Deep Sleep mode.

The CPU subsystem also includes debug interfaces and supports both SWD and JTAG. The chip also supports boundary scan, which is required for testing on a PCB, and a separate test access port (TAP) controller is provided for controlling boundary scan functions.

4.2 DMA

The Cortex®-M33 CPU integrates two DMA controllers that support autonomous data transfers between memory and peripheral registers, with configurable cyclic redundancy check (CRC).

The DMA controllers are bus masters in their respective domains. Each DMA has 16 channels. It has a single transfer engine for all channels that arbitrates for bus master access. The DMA uses the 32-bit AHB bus that shares the same clock as the CPU.

4.3 Cryptography support

One instance of the cryptographic acceleration block that implements hardware support for true random number generator (TRNG), SHA-256, SHA-384, SHA-512, AES-128, AES-256 and vector unit (VU), is provided.

4.4 Memory

The device features multiple nonvolatile and volatile memory types. The CPU and other bus masters can access any memory block. The number of wait states depends on the access path.

4.4.1 Flash

The device offer up to 512 KB of user-programmable flash. The flash supports single and dual bank modes. Dual bank mode supports the RWW feature, which allows reading from one sector while programming the other. In addition, the flash module has ECC support.

4.4.2 SFlash

The device has 32-KB supervisory flash (SFlash) memory. SFlash stores the device trim settings, secure key hashes, and FLASH_BOOT firmware. Device trim settings are used to initialize hardware resources for proper operation. Secure key hashes are used to authenticate Infineon and OEM assets and images. SFlash cannot be used to store user data.

4.4.3 ROM

All devices offer 64 KB of ROM. The ROM contains boot and configuration routines and authentication checks. After a reset event, the boot code in the supervisory ROM (SROM) checks the Reset Cause register to determine whether a Hibernate event was the cause of the reset to provide the fastest possible transition to execute the user code. This minimizes the wake-up time from Hibernate mode as opposed to a power on reset (POR) or an external reset (XRES) event.

4.4.4 RAM

Two independent SRAM controllers are used for two instances of 64 KB SRAM supporting a total of up to 128 KB SRAM memory. The two SRAM controllers use separate power switches, with provision of retaining either one or both instances of the memory during DeepSleep power mode. SRAM has ECC support for soft error detection and correction.

4.5 eFuse

The device contains 1024 one-time programmable (OTP) eFuse bits. These are reserved for system use such as device life-cycle management, trim, and hash values. eFuse bits cannot be directly programmed by the user.

Each fuse is individually programmed; once programmed (or “blown”), its state cannot be changed. Blowing a fuse transitions it from the default state of ‘0’ to ‘1’. To program an eFuse, VDDIO0 must be at 2.5 V ±10%.

Because blowing an eFuse is an irreversible process, any process requiring eFuse programming is recommended only in mass production under controlled factory conditions by Infineon provided provisioning tools.

4.6 Clock system

The PSC3M/P6 clock system is responsible for providing clocks to all subsystems requiring clocks and switching between different clock sources without glitching. In addition, the clock system ensures that no metastable conditions occur.

Furthermore, a clock supervision (CSV) circuit is implemented for each clk_hf domain. The CSV circuit detects a stopped clock or an abnormal frequency of the monitored clock. There are clock counters for both the monitored clock and the reference clock. Parameters for each counter define the frequency of the reference clock and the upper and lower limit for the frequency of the monitored clock.

If the dedicated frequency range comparator detects a stopped clock or a clock outside the specified frequency range, an abnormal state is signaled. Depending on the register settings and how the monitored clock is used on the device, either a reset or an interrupt is generated.

The following clock sources are provided:

- Internal main oscillator (IMO): 8 MHz ±2%, fast wake-up, low jitter
- Internal high-speed oscillator (IHO): 48 MHz ±1%
- Internal low-speed oscillator (ILO): 32 kHz ±10%, also as a wake-up source for the RTC

- External crystal oscillators (ECO and WCO)
  - External crystal oscillator (ECO): 4 MHz - 36 MHz
  - External watch crystal oscillator (WCO): 32.768 kHz
- External clock (EXTCLK): Maximum frequency 80 MHz
- One frequency lock loop (FLL)[1] with 24 -100 MHz output range
- One digital phase-locked loops, DPLL#0, with 25 - 180 MHz output range

***Notes**:*

1. *FLL input clock should to be at least 2.5 times less than the FLL current controlled oscillator frequency. Therefore, with FLL output divider enabled, IHO can be used as FLL input clock source only when FLL output frequency is ≥ 60 MHz.*

4.6.1 Internal main oscillator (IMO)

Internal main oscillator (IMO) operates at a fixed 8 MHz frequency. Its tolerance is ±2%. A high-speed clock can be derived using the IMO plus a DPLL. It has fast wake-up and low jitter.

4.6.2 Internal high-frequency oscillator (IHO)

Internal high-frequency oscillator (IHO) operates at a fixed 48 MHz frequency. Its tolerance is ±1%. A high speed-clock can be derived using the IHO plus DPLL.

4.6.3 Internal low-frequency oscillator (ILO)

The ILO is a low-power oscillator with a typical current of 0.3 µA and frequency of 32 kHz with ±10% accuracy. The ILO can be used as wake-up source for real-time clock (RTC)

4.6.4 External crystal oscillator (ECO)

External crystal oscillator (ECO) can use a crystal with frequency ranging from 4 MHz to 36 MHz for generating a high-precision clock. This option can be used when the precision offered by internal oscillators is not sufficient.

4.6.5 Watch crystal oscillator (WCO)

WCO uses an external 32.768 kHz crystal for applications requiring higher-precision real-time clock (RTC) functionality. WCO clock can be routed directly to the RTC for higher precision and to avoid any glitches due to internal switching of clock sources.

4.6.6 Watchdog timer (WDT)

One watchdog timer (WDT) and one multi-counter watchdog timer (MCWDT) are provided. The WDT is implemented in the clock block running from the ILO or the WCO. This allows the watchdog operation during Deep Sleep and can generate a watchdog reset if not serviced before the timeout. The watchdog reset is recorded in the Reset Cause register.

4.6.7 Real-time clock (RTC)

The device includes a real-time clock (RTC). The RTC has the following features:

- Can operate in both 12-hour format with AM/PM flag and 24-hour format

- Automatic leap year correction
- The alarm feature allows the RTC to generate an interrupt, which may be used to wake up the system from Sleep, Deep Sleep, and Hibernate power modes

4.7 Reset

The device can be reset from various sources, including a software reset. Reset events are asynchronous and ensure reversion to a known state. The reset cause (WDT, MCWDT, Faults, Debug, Software, and Clock Supervision) is recorded in a register, which is sticky through reset, and allows the software to determine the cause of the reset. An XRES pin is available for external reset.

4.8 High-performance programmable analog subsystem (HPPASS)

4.8.1 12-bit SAR analog-to-digital converter (ADC)

The device has one 12-bit SAR ADC with 16 parallel sample and hold (S/H) circuits, that can support up to 24 external inputs as well as additional internal signals.

All S/H circuits support individually selectable input gains of 1, 3, 6, and 12. The SAR ADC supports up to 9-Msps conversion rate. The ADC can operate with a voltage range between 1.71 V to 3.63 V (VDDA). VDDA needs to be between 2.7 V to 3.63 V for running the HPPASS at 180 MHz.The AREF_EXT pin is used to provide the ADC reference voltage. It can be connected to a precision reference voltage generator (1.71 V to VDDA) or connected externally to the AVCC pin.

The idle sampling feature allows ADC triggers to start directly from hold operation. All 16 samplers can be triggered simultaneously for simultaneous idle sampling (same hold instance) and sequential conversion (useful for multi-motor, multi-phase motor control and digital power applications). ADC has a sequencer with eight groups that can be programmed according to the user application. Each group defines a set of inputs that will be simultaneously sampled when that group is triggered by hardware or firmware. Each group supports the control and conversion of up to 16 samplers. The sampling time and conversion priority can be configured individually for each group.

The ADC has a set of built-in post-processing features for the converted digital data, such as averaging (result accumulation of 2, 4, 8, 16, 32, or 64 samples), pseudo differential mode, 2x FIR with 16 taps, 8x limit detect, 3x programmable 3P3Z filters, signed or unsigned result format and 32 entry FIFO. These features help in reducing CPU utilization for analog data acquisition and post-processing.

ADC MUXed inputs can also be internally connected to AFE single- ended or differential outputs, DAC output, or the internal temperature sensor. The ADC is not available in the Deep Sleep and Hibernate power modes.

4.8.2 OpAmps

The device features up to four high-bandwidth, fast-slew rate, rail-to-rail OpAmps with flexible routing and configuration options. The OpAmps can be configured in either high-speed or low-power modes depending on application requirements.

The OpAmps support following routing and configuration options:

- Standalone single-ended operation with external output on analog-capable I/O requiring an external feedback network
- Internal programmable gain amplifier (PGA) in single-ended or differential output modes, with the outputs internally routed to ADC MUXed samplers. Internal PGA mode supports a gain of 1x (follower), 2x, 4x, 8x, 16x, 32x and 64x

4.8.3 Hardware filter (HW filter 3P3Z)

The device features a programmable 3-poles, 3-zeros filter implemented in hardware. It has three structures of compensation filter with support for filter data input manipulation, coefficient scaling, anti-windup, and filter data output manipulation like offset and range limit. The filter input data stream can be fed from AHB interface or through a dedicated data path from the ADC output.

The hardware 3P3Z module features:

- 16-bit input format (q0.15)
- 24-bit output format (q0.23)
- 24-bit coefficients format (q0.23)
- 48-bit multiplier
- 58-bit internal accumulator
- 2-bit gain input
- 3-bit attenuator output

Additional features include support for saturation and rounding operators, arithmetic two's complement processing, and a maximum execution latency of nine CPU clock cycles.

4.8.4 12-bit digital to analog converter (DAC)

The device features two 12-bit resolution DACs with output buffers. These DACs support a maximum update rate of 1 Msps and have a settling time of 500 ns.

4.8.5 Comparator and slope generator (CSG)

The device features up to nine analog comparators organized into up to three groups that operate in Active mode. The comparator output is synchronized to avoid metastability. The comparator output can be routed to a GPIO or TCPWM (through TriggerMux), for example, as an input to kill the PWM signal if an overvoltage or over current condition is detected.

Comparators can use either their built-in 10-bit DACs or another analog input to define the reference threshold voltage. The DAC outputs can also be internally connected to the ADC and measured.

The comparator inputs feature a user programmable 3-bit hysteresis value ranging from 0 to 84 mV. All comparators in the same group share a common hysteresis setting.

The comparator DAC values can be updated by either direct or buffered writes. This capability can be used for slope generation, implementation of wider hysteresis, and LUT waveform generation.

4.8.6 Temperature sensor

The device contains a diode-based temperature sensor. It can be disabled to save power. The temperature sensor is connected to the SAR ADC through AMUX as one of the measurement channels. The precision of the temperature sensor output is ±5°C over the full operating temperature range.

4.9 Low-power comparator (LPComp)

The device provides two low-power comparators that can operate in all power modes. This allows other analog system resources to be disabled while retaining the ability to monitor external voltage levels during Deep Sleep and Hibernate modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode (Hibernate) where the wake-up circuit is activated by a comparator-switch event.

4.10 Fixed function digital

4.10.1 Timer/counter pulse-width modulator (TCPWM)

The TCPWM consists of the following:

- A counter with user-programmable period/duty length PWM outputs
- A capture register to record the count value at the time of an event (which may be an I/O event)
- A period register to either stop or auto reload the counter when its count is equal to the period registers
- Compare registers to generate compare value signals that are used as PWM duty cycle outputs

The block provides accurate and complementary outputs with a programmable offset between them to allow its use as dead-band programmable complementary PWM outputs. It also has a kill input to force the outputs to a predetermined state; this can be used in motor drive and power conversion systems, for example, when an overcurrent state is indicated and the PWMs driving the FETs must be shut off immediately with no time for software intervention.

TCPWM has a Motion Interface (MOTIF) block that can be used in Hall sensor, Quadrature encoder or standalone Multichannel mode.

TCPWM also supports a high-resolution PWM (HRPWM) feature. The 32-bit four-channel TCPWM counters are enhanced with the following functionalities:

- It can program and control the PWM output signals with a typical resolution of less than 100 ps
- It can control the period, duty cycle, and dead-time with the high-resolution function

4.10.2 Serial communication block (SCB)

The PSC3M/P6 has up to six SCB modules, which can be software-configured for I2C, UART, or SPI interface as master or slave when in Active mode. One of the SCB modules can operate in Deep Sleep mode with an external clock with the functionality limited to I2C slave or SPI slave. Every protocol can use a 256-byte-deep FIFO per SCB module. All SCB blocks support DMA transfers.

4.10.2.1 Inter-integrated circuit (I2C)

The hardware I2C block implements a full multi-master and multi-slave interface and is capable of multi-master arbitration. This block can operate at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce the interrupt overhead and latency for the CPU. It also supports EZI2C, which creates a mailbox address range in the memory of the device. This effectively reduces the I2C communication overheads for reading from and writing to an array in the memory. The FIFO significantly reduces the need for clock stretching caused by the CPU not having read the data on time.

Furthermore, the I^2C instances in this device also support the PMBus protocol with the following features:

- Communication at baud rates up to 1 Mbps
- Timeout event generation
- A minimum of five slave address masks for hardware address screening
- De-glitching of SMBCLK and SMBDAT signals to ensure noise-immune communication

4.10.2.2 Universal asynchronous transmitter receiver (UART)

The full-feature UART can operate at up to 8 Mbps. It supports LIN (automotive single-wire interface), IrDA (Infrared interface), and SmartCard (ISO7816) protocols. In addition, it supports the 9-bit multiprocessor mode, which allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as hardware flow

control, parity, break detection, and frame error are supported. The SCB can be configured in half-duplex UART mode for single-wire communication.

4.10.2.3 Serial peripheral interface (SPI)

The SPI mode supports full Motorola SPI, Texas Instruments synchronous serial port (SSP) (essentially adds a start pulse used to synchronize SPI codecs), and National Semiconductor Microwire (a half-duplex form of SPI). The SPI block also supports an EZ-SPI mode in which data interchange is reduced to reading and writing an array in memory. Fast SPI can support master and slave functionalities up to 45 MHz.

4.10.3 Improved inter-integrated circuit (I3C)

This product line has an I3C block. I3C is a MIPI Alliance standard that aims to unify sensor serial interfaces into one pair of wires. All nodes connect to one pair of wires providing protocol support via frame encapsulation at a higher rate, thereby reducing the need for multiple I2C and SPI interfaces. The I3C block provides global signaling, in-band interrupts, time awareness, multi-master capability, and error detection.

4.10.4 Universal serial bus (USB)

The device supports universal serial bus full speed (USB FS) communication in both host and device mode. USB interface can wake up the device from DeepSleep mode.

4.10.5 Controller area network flexible data-rate (CAN FD)

CAN FD features two channels including timestamp support and a 4-KB message RAM per channel. This block supports data rates of up to 8 Mbps.

4.11 Trigger multiplexer (Trigger MUX)

Trigger MUX is used to connect trigger and input/output signals between peripherals as well as GPIO pins. It can be used to connect several TCPWM counter channels to achieve multichannel support. It also provides the extended signal routing functionality such as routing any TCPWM counter PWM outputs to any GPIO pin through peri.tr_io_output[n] alternate function.

The trigger connections between TCPWM and HPPASS are also connected through the Trigger MUX. Any TCPWM counter can be configured to trigger any S/H circuit of the ADC inside HPPASS.

The digital comparator outputs from the ADC and analog comparator outputs are also connected to the TCPWM from the HPPASS through the Trigger MUX. It is possible to route any digital/analog comparator output to any TCPWM group and any counter inside the group.

The connections between the TCPWM and HPPASS are optimized for low latency.

4.12 Coordinate rotation digital computer (CORDIC)

CORDIC is used to precisely compute the transforms used in motor speed and position estimation as well as reference plane transforms commonly used in Field-Oriented Control (FOC). It calculates trigonometric functions in hardware to offload the processing from the main CPU. Supported algorithms include sine, cosine, arctan, sinh, cosh, arctanh, phase, sqrt, and park transform.

4.13 General-purpose input/output (GPIO) ports

The PSC3M/P6 provides up to 68 + 2 GPIO pads. Up to 8 GPIOs are analog capable and can be routed to the four multiplexed analog inputs, making it possible to have a maximum of 24 analog input connections. The GPIO block has the following features:

- Eight drive modes including strong push-pull, resistive pull-up and pull-down, open-drain and open-source, input-only, and disabled
- Analog signal input capability (I/O buffers disabled; signal passed through switches)
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output disables
- Hold mode for latching the previous state (used for retaining the I/O state in Deep Sleep and Hibernate modes)
- Selectable slew rates for dV/dt-related noise control
- Up to 4 over-voltage tolerant (OVT) pins

The pins are organized in logical entities called "ports". During power-on and reset, the blocks are forced to the disabled state so they do not crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a "high-speed I/O matrix" (HSIOM) is used to multiplex between various signals that may connect to an I/O pin.

Data Output and Pin State registers store the values to be driven on the pins and the pins' states.

Every I/O pin can generate an interrupt if so enabled, and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it.

The I/O ports will retain their state during Hibernate mode. If the operation is restored using Reset, then the pins will go to the High-Z state; if the operation is restored by using the wake-up pin, the pin drivers will retain their previously frozen state until the firmware chooses to change it.

Simultaneous output switching in high-current mode requires attention to line termination and decoupling capacitor size to control switching transient voltages.

4.14 Smart I/O (Programmable I/O)

Each smart I/O block contains up to eight programmable LUT arrays out of which up to eight LUT arrays are associated with a particular I/O port that allows integration of board-level glue logic and Boolean functions at the pins. The remaining free LUT arrays can be connected to the I/O LUT array outputs for creating more complex logic functions. It is similar to programmable array logic (PAL) or small programmable logic devices (PLDs). The smart I/O block is interposed between the port pins and the HSIOM (responsible for multiplexing signals from on-chip peripherals to and from the port pins) and the digital signal interconnect (DSI) signals. It is possible to bypass the smart I/O block in order not to impact the propagation delay for critical paths from the DSI to the port pins.

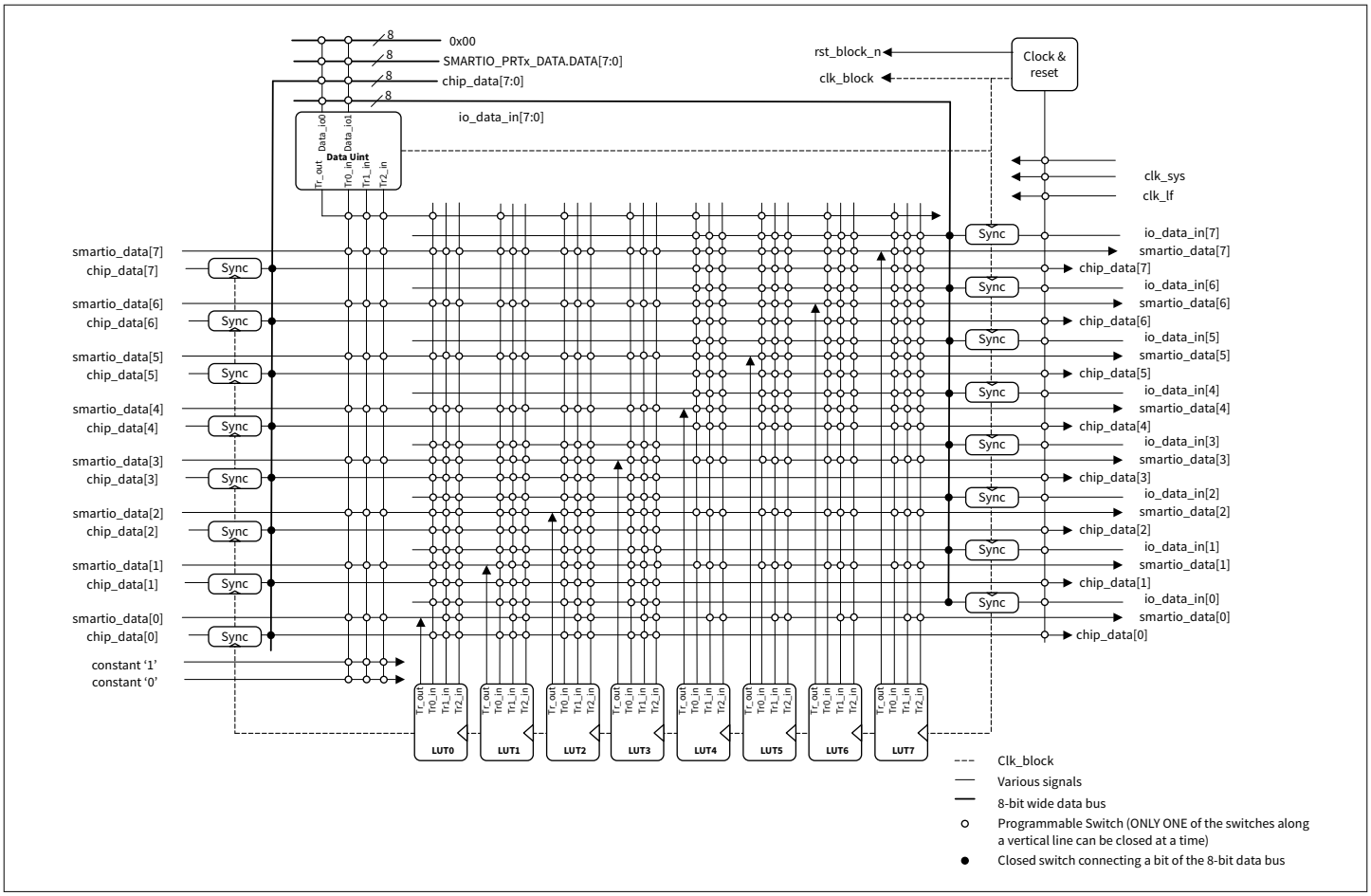


Figure 7 Smart I/O block diagram

The structure is interposed between the GPIO port and the HSIOM.

4.15 Device Firmware Update (DFU)

The PSC3M/P6 immutable BootROM includes a built-in DFU protocol that enables secure and reliable firmware upgrades through a serial interface. By default, DFU functionality is enabled in UART mode. The DFU allows fully flexible SCB, port, pin, and interface configuration using OEM policy fields. See AN243370 – Getting started with PSOC™ Control C3M/P6 MCU security application note for more details.

In the default configuration, DFU functionality is selected during device boot-up based on the state of *P2.3* pin. When the device enters into DFU mode, pins *P8.1* and *P8.3* function as the serial communication interface. Use pull-up or pull-down resistors of 1 kΩ or less connected to VDDIO_1 or VSS to set the DFU enable pin to logic HIGH or LOW. For a High-Z state, the DFU enable pin can be left floating.

Table 3 PSC3M/P6 DFU default settings and available configuration options

Parameter	Default value	Configuration options in OEM policy
DFU Enabled	Enable	Enable, Disable
DFU serial interface	UART on SCB5	UART, I2C, or SPI on any available SCB

(table continues...)

Table 3 (continued) PSC3M/P6 DFU default settings and available configuration options

Parameter	Default value	Configuration options in OEM policy
DFU port pins	UART RX - P8.1 UART TX - P8.3	As per selected SCB alternate function pins
DFU enable pin	P2.3	Any GPIO
DFU entry condition	DFU enable pin pull-up or driven $\overline{\text{HIGH}}$ for DFU entry; pull-down, drive $\overline{\text{LOW}}$ or High-Z for normal operation	Fixed

The following parameters are used for DFU-UART communication:

1. **Baud rate**: 115200
2. **Data bits**: 8
3. **Stop bits**: 1
4. **RTS/CTS**: No
5. **Parity**: None

4.16 Serial wire JTAG debug port/Embedded trace macrocell

Serial wire JTAG debug port (SWJ-DP)

The PSC3M/P6 MCU embeds the Arm® serial wire JTAG debug port (SWJ-DP) which supports 2-wire Serial Wire Debug (SWD) and 4-wire or 5-wire Joint Test Action Group (JTAG) interface. SWD interface is enabled by default after power on and JTAG interface is in disabled state. JTAG can be enabled in 4-wire or 5-wire mode by updating the OEM policy. For more information on updating the OEM policy, refer to the AN240106 - Getting started with PSOC™ Control C3 security.

Embedded trace macrocell (ETM)

Arm® embedded trace macrocell is supported by the PSC3M/P6. It allows reconstruction of program execution using high speed compressed data transmitted on the ETM pins. ETM interface includes a clock (trace.clock) pin and up to four data (trace.data0 to trace.data3) pins. The device only supports parallel trace. Serial trace is not supported.

4.17 Supply voltage glitch sensor (SVGS)

The device includes a voltage glitch sensor designed to detect manipulations of the input voltage by an attacker attempting to disrupt the operation of the device.

The SVGS module provides the following functionality:

- VCCD overshoot monitor with a configurable threshold
- VCCD undershoot monitor with a configurable threshold, using a filtered VCCD signal
- VCCD noise monitor with a configurable threshold
- VDDD undershoot monitor, detecting voltage levels below the brown-out threshold

5 Pins

GPIO ports and analog inputs are powered by VDDx pins as follows:

- P0: VBACKUP
- P1, P2, P3, P4, P5, P6, P7, P10, P12: VDDIO_0
- P8, P9, P13: VDDIO_1
- P11: VDDUSB
- AN_A, AN_B: AVDD

The number of GPIOs is limited in some packages. The E-LQFP-100 package has the full 68+2 GPIOs and 16 dedicated analog inputs; the E-LQFP-80 package has 54 GPIOs and 16 dedicated analog inputs; the E-LQFP-64 package has 39 GPIOs and 16 dedicated analog inputs. For detailed information on the supported packages, see Package information section.

Table 4 Packages and pin information

Pin	Capability		Packages	
		E-LQFP-100	E-LQFP-80	E-LQFP-64
VDDD	-	9	9	5
VDDD	-	10	-	-
VDDA	-	82	66	54
VDDA	-	83	-	-
VDDIO_0_0	-	25	20	16
VDDIO_0_1	-	50	40	32
VDDIO_0_2	-	65	49	-
VDDIO_1	-	100	80	64
VCCD	-	11	10	6
VCCD	-	12	-	-
VDDUSB	-	38	-	-
VSS	-	GND PAD	GND PAD	GND PAD
VAREF_EXT	-	81	65	53
VBACKUP	-	13	11	7
AN_A0	AD, CSG, AFE	69	53	41
AN_A1	AD, CSG, AFE	70	54	42
AN_A2	AD, CSG, AFE	71	55	43
AN_A3	AD, CSG, AFE	72	56	44
AN_A4	AD, CSG, AFE	73	57	45
AN_A5	AD, CSG, AFE, DAC	74	58	46
AN_A6	AD, AFE	75	59	47
AN_A7	AD, AFE	76	60	48
AN_B0	AD, CSG, AFE	77	61	49
AN_B1	AD, CSG, AFE	78	62	50
AN_B2	AD, CSG, AFE	79	63	51
AN_B3	AD, CSG, AFE	80	64	52

(table continues...)

Table 4 (continued) Packages and pin information

Pin	Capability		Packages	
		E-LQFP-100	E-LQFP-80	E-LQFP-64
AN_B4	AM, CSG, AFE	84	67	55
AN_B5	AM, CSG, AFE, DAC	85	68	56
AN_B6	AM, AFE	86	69	57
AN_B7	AM, AFE	87	70	58
XRES	-	8	8	4
P0.0	S	14	12	8
P0.1	S	15	13	9
P1.0	S	19	14	10
P1.1	S	20	15	11
P1.2	S	21	16	12
P1.3	S	22	17	13
P2.0	S	23	18	14
P2.1	S	24	19	15
P2.2	S	26	21	17
P2.3[1)]	S	27	22	18
P3.0	S	28	23	-
P3.1	S	29	24	-
P3.2	S	30	25	-
P3.3	S	31	26	-
P4.0	-	32	27	19
P4.1	-	33	28	20
P4.2	-	34	29	21
P4.3	-	35	30	22
P4.4	-	41	31	23
P4.5	-	42	32	24
P4.6	-	43	33	25
P4.7	-	44	34	26
P5.0	S	45	35	27
P5.1	S	46	36	28
P5.2	S	47	37	29
P5.3	S	48	38	30
P6.0	S, OVT	49	39	31
P6.1	S, OVT	51	41	33
P6.2	S, OVT	52	42	34
P6.3	S, OVT	53	43	35

(table continues...)

Table 4 (continued) Packages and pin information

Pin	Capability	Packages		
		E-LQFP-100	E-LQFP-80	E-LQFP-64
P7.0	-	60	44	36
P7.1	-	61	45	37
P7.2	-	62	46	38
P7.3	-	63	47	39
P7.4	AM, CSG, AFE	64	48	40
P7.5	AM, CSG, AFE	66	50	-
P7.6	AM, CSG, AFE	67	51	-
P7.7	AM, CSG, AFE	68	52	-
P8.0	AM, AC, CSG, AFE	88	71	59
P8.1	AC	89	72	60
P8.2	AM, AC, CSG, AFE	90	73	61
P8.3	AC, AFE	91	74	62
P8.4	AM, CSG, AFE	92	75	-
P8.5	AM, CSG, AFE	93	76	-
P8.6	-	94	77	
P8.7	-	95	78	
P9.0	S	96	79	63
P9.1	S	1	1	1
P9.2	S	2	2	2
P9.3	S	3	3	3
P9.4	S	4	4	-
P9.5	S	5	5	-
P9.6	S	6	6	-
P9.7	S	7	7	-
P10.0	-	16	-	-
P10.1	-	17	-	-
P10.2	-	18	-	-
P11.0[2)]	USB DM	39	-	-
P11.1[2)]	USB DP	40	-	-
P12.0	-	36	-	-
P12.1	-	37	-	-
P12.2	-	54	-	-
P12.3	-	55	-	-
P12.4	-	56	-	-
P12.5	-	57	-	-

(table continues...)

Table 4 (continued) Packages and pin information

Pin	Capability	Packages		
		E-LQFP-100	E-LQFP-80	E-LQFP-64
P12.6	-	58	-	-
P12.7	-	59	-	-
P13.0	-	97	-	-
P13.1	-	98	-	-
P13.2	-	99	-	-

1) P2.3 is the DFU enable pin in the default DFU configuration. Ensure that this pin is not pulled-up or driven high at power on to avoid entering DFU mode unintentionally.

2) Port 11 is available only in devices without USB support. See the Ordering information for details.

Table 5 Pin capability abbreviations

Abbreviation	Capability
AD	Dedicated analog pin directly connected to sampler
AM	Dedicated analog pin/analog capable GPIO pin connected to a MUXed sampler
CSG	Dedicated analog pin that can be connected to CSG input
AC	Analog capable GPIO pin (LPComp input)
AFE	AFE input/output pin
DAC	DAC output pin
S	Smart I/O capable GPIO
USB	USB PHY I/O pin
OVT	Over-voltage tolerant pin

***Notes**:*

1. *All GPIO pins are PWM capable. Any TCPWM channel line or line_compl output can be routed to any GPIO pin.*

2. *The number of LUTs is not impacted by the number of Smart I/O capable GPIO pins available in lower pin-count packages.*

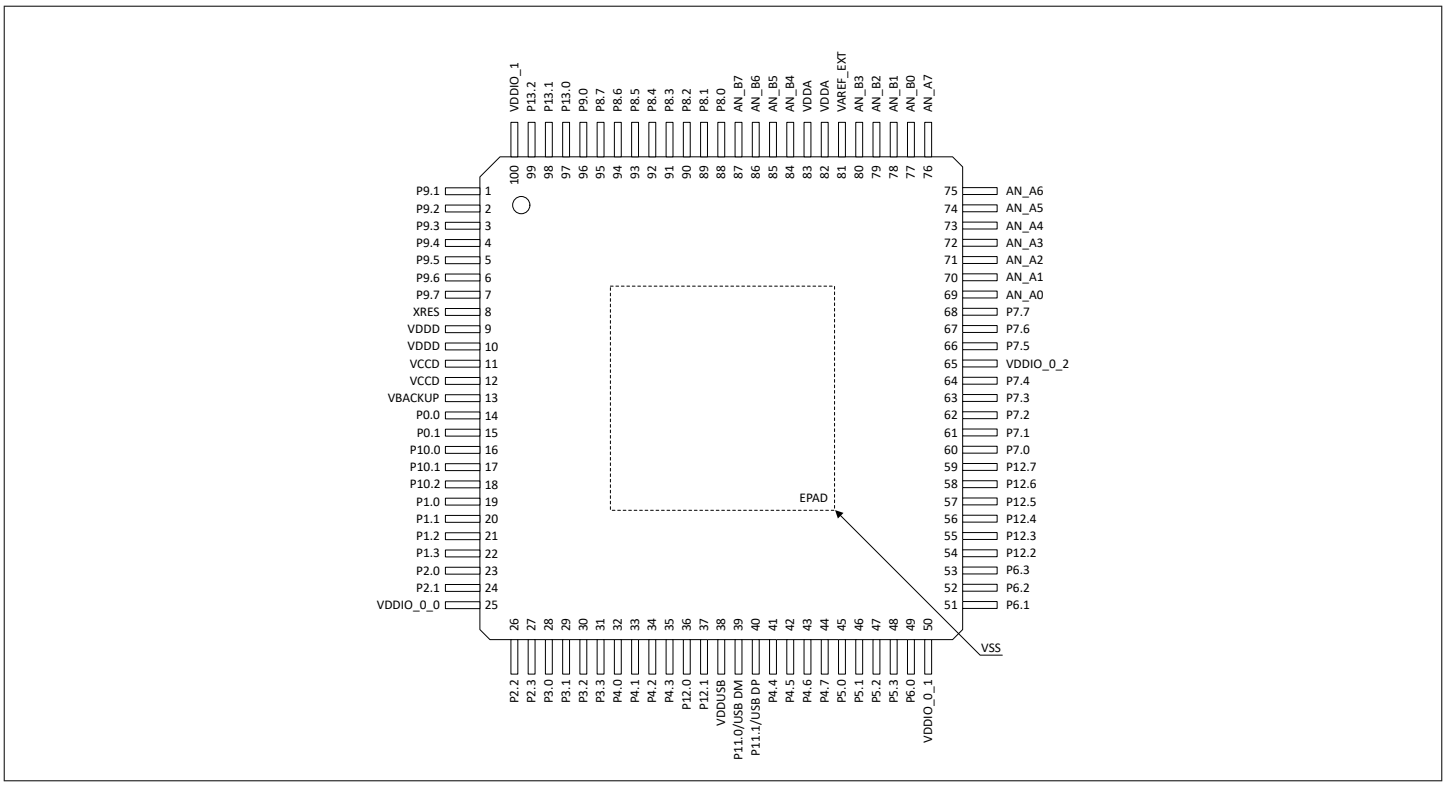


Figure 8 Device pinout for E-LQFP-100 package (top view)

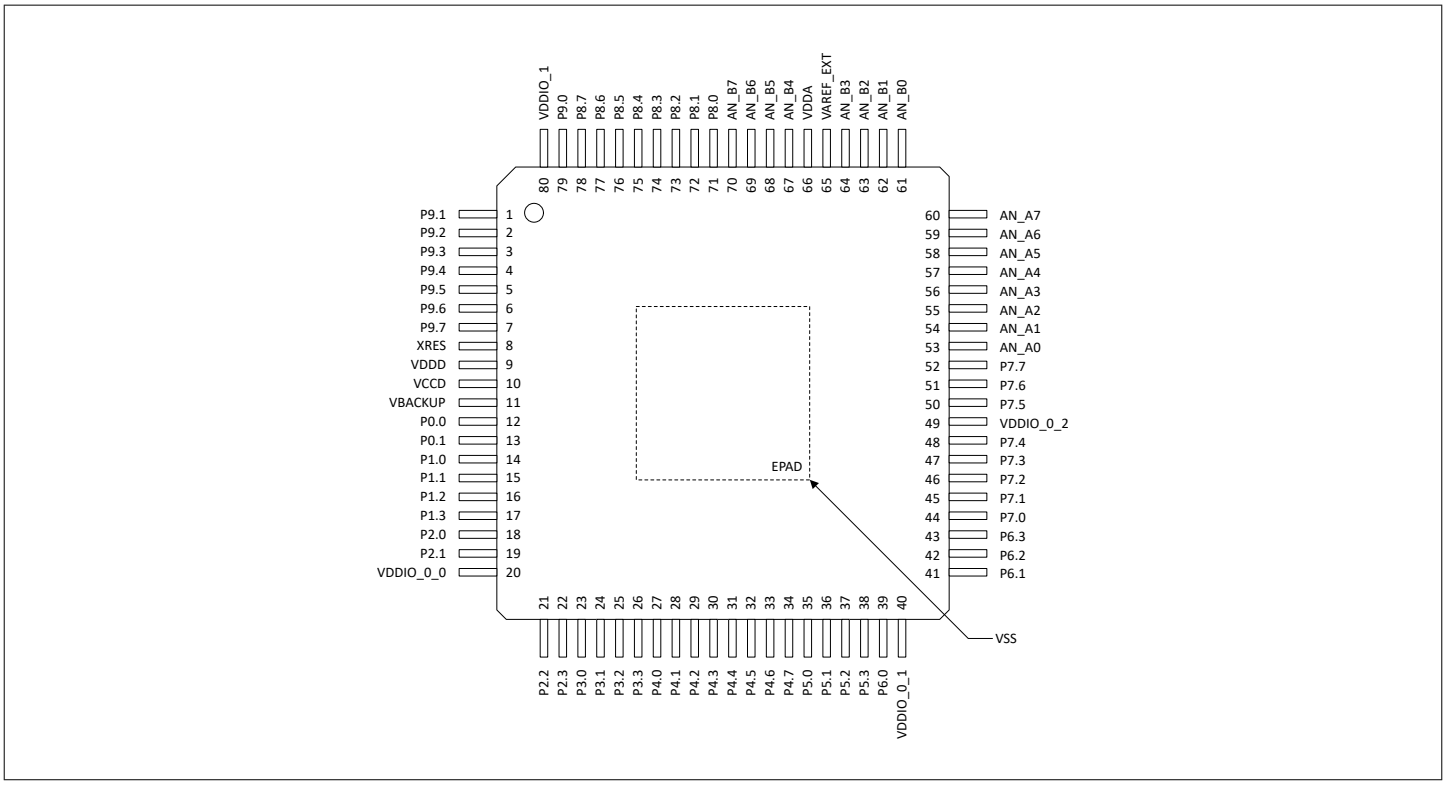


Figure 9 Device pinout for E-LQFP-80 package (top view)

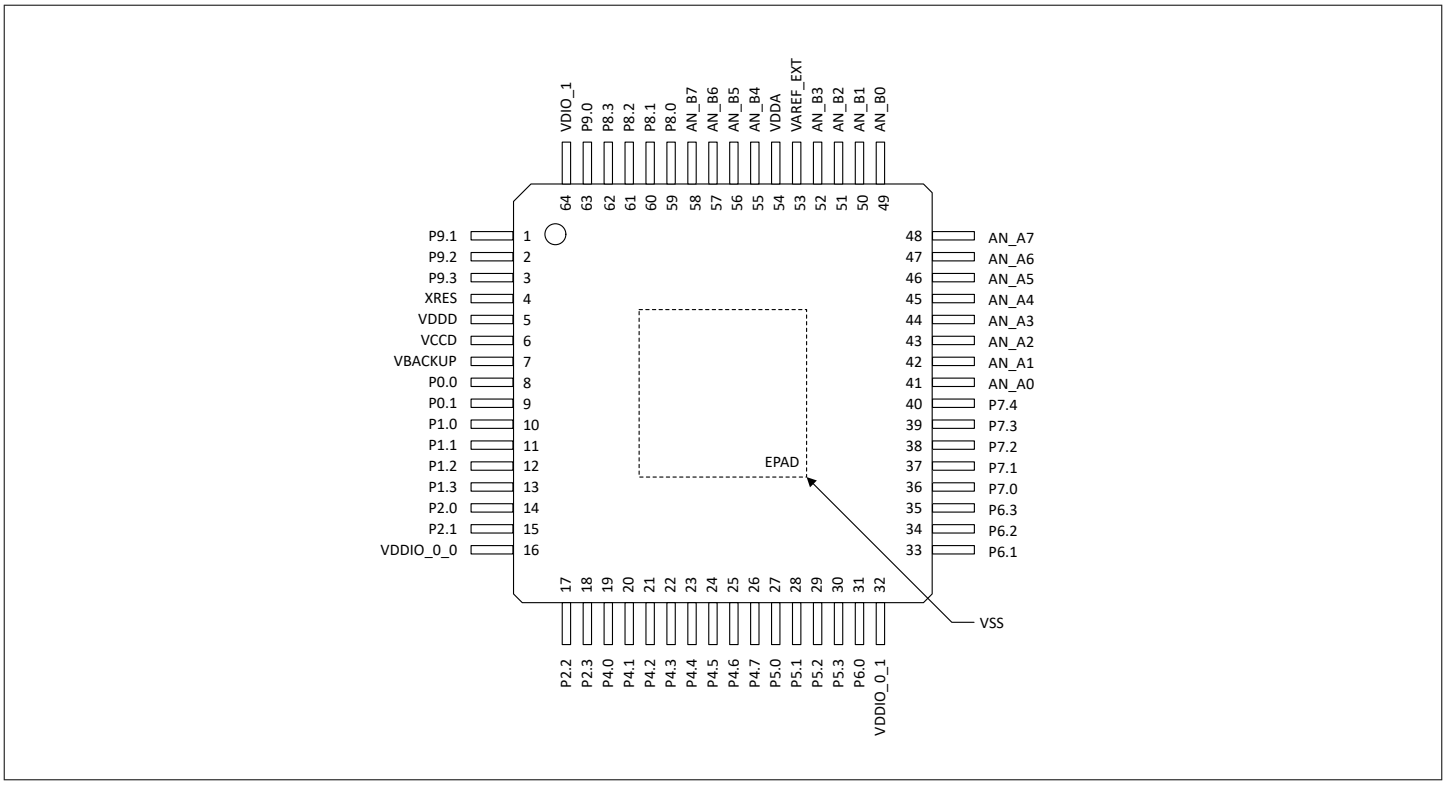


Figure 10 Device pinout for E-LQFP-64 package (top view)

6 GPIO alternate functions

Table 6 GPIO alternate functions and HSIOM routes

GPIO	Alternate functions and HSIOM routes			
P0.0	wco_out	fixed	smartio.io0	fixed
	scb1.spi.select4	ACT #6	ext_clk[1)]	ACT #8
	peri.tr_io_output[75]	ACT #13	peri.tr_io_input[7]	ACT #14
	peri.tr_io_output[7]	ACT #15		
P0.1	wco_in	fixed	smartio.io1	fixed
	scb1.spi.select5	ACT #6	peri.tr_io_output[76]	ACT #13
	peri.tr_io_input[8]	ACT #14	peri.tr_io_output[8]	ACT #15
P1.0	eco_in	fixed	smartio.io0	fixed
	peri.tr_io_output[144]:1	ACT #1	peri.tr_io_output[153]:1	ACT #2
	scb1.uart.cts	ACT #4	scb1.spi.select0	ACT #6
	scb1.i2c.scl_do	ACT #7	peri.tr_io_output[80]	ACT #13
	peri.tr_io_input[12]	ACT #14	peri.tr_io_output[12]	ACT #15
P1.1	eco_out	fixed	smartio.io1	fixed
	peri.tr_io_output[145]:1	ACT #1	peri.tr_io_output[154]:1	ACT #2
	scb1.uart.rts	ACT #4	scb1.spi.clk	ACT #6
	scb1.i2c.sda_do	ACT #7	peri.tr_io_output[81]	ACT #13
	peri.tr_io_input[13]	ACT #14	peri.tr_io_output[13]	ACT #15
P1.2	smartio.io2	fixed	peri.tr_io_output[146]:1	ACT #1
	peri.tr_io_output[155]:1	ACT #2	scb1.uart.rx	ACT #4
	scb1.spi.mosi	ACT #6	scb1.i2c.sda	ACT #7
	peri.tr_io_output[82]	ACT #13	peri.tr_io_input[14]	ACT #14
	peri.tr_io_output[14]	ACT #15	swj.swclk/tclk	DS #5
P1.3	smartio.io3	fixed	peri.tr_io_output[147]:1	ACT #1
	peri.tr_io_output[156]:1	ACT #2	scb1.uart.tx	ACT #4
	scb1.spi.miso	ACT #6	scb1.i2c.scl	ACT #7
	peri.tr_io_output[83]	ACT #13	peri.tr_io_input[15]	ACT #14
	peri.tr_io_output[15]	ACT #15	swj.swdio/tms	DS #5

(table continues...)

Table 6 (continued) GPIO alternate functions and HSIOM routes

GPIO	Alternate functions and HSIOM routes			
P2.0	hibernate_wakeup	fixed	smartio.io0	fixed
	peri.tr_io_output[144]:0	ACT #1	tcpwm0.g2.cnt6+	ACT #2
	scb1.uart.cts	ACT #4	scb1.spi.select0	ACT #6
	scb1.i2c.scl_do	ACT #7	peri.tr_io_output[84]	ACT #13
	peri.tr_io_input[16]	ACT #14	peri.tr_io_output[16]	ACT #15
	swj.tdi	DS #5		
P2.1	smartio.io1	fixed	peri.tr_io_output[145]:0	ACT #1
	tcpwm0.g2.cnt6-	ACT #2	cal_wave	DS #0
	scb1.uart.rts	ACT #4	scb1.spi.clk	ACT #6
	scb1.i2c.scl	ACT #7	peri.tr_io_output[85]	ACT #13
	peri.tr_io_input[17]	ACT #14	peri.tr_io_output[17]	ACT #15
	swj.tdo	DS #5		
P2.2	smartio.io2	fixed	peri.tr_io_output[146]:0	ACT #1
	tcpwm0.g2.cnt7+	ACT #2	scb1.uart.rx	ACT #4
	scb1.spi.mosi	ACT #6	scb1.i2c.sda	ACT #7
	ext_clk[1)]	ACT #8	peri.tr_io_output[86]	ACT #13
	peri.tr_io_input[18]	ACT #14	peri.tr_io_output[18]	ACT #15
P2.3	smartio.io3	fixed	peri.tr_io_output[147]:0	ACT #1
	tcpwm0.g2.cnt7-	ACT #2	scb1.uart.tx	ACT #4
	scb1.spi.miso	ACT #6	scb1.i2c.sda_do	ACT #7
	peri.tr_io_output[87]	ACT #13	peri.tr_io_input[19]	ACT #14
	peri.tr_io_output[19]	ACT #15		
P3.0	smartio.io0	fixed	tcpwm0.g0.cnt4+	ACT #0
	peri.tr_io_output[148]:0	ACT #1	peri.tr_io_output[157]:1	ACT #2
	scb4.uart.cts	ACT #4	scb4.spi.mosi	ACT #6
	scb4.i2c.sda_do	ACT #7	peri.tr_io_output[88]	ACT #13
	peri.tr_io_input[20]	ACT #14	peri.tr_io_output[20]	ACT #15
P3.1	smartio.io1	fixed	tcpwm0.g0.cnt4-	ACT #0
	peri.tr_io_output[149]:0	ACT #1	peri.tr_io_output[158]:1	ACT #2
	scb4.uart.rts	ACT #4	scb4.spi.miso	ACT #6
	scb4.i2c.sda	ACT #7	peri.tr_io_output[89]	ACT #13
	peri.tr_io_input[21]	ACT #14	peri.tr_io_output[21]	ACT #15

(table continues...)

Table 6 (continued) GPIO alternate functions and HSIOM routes

GPIO	Alternate functions and HSIOM routes			
P3.2	smartio.io2	fixed	tcpwm0.g0.cnt5+	ACT #0
	peri.tr_io_output[150]	ACT #1	peri.tr_io_output[159]:1	ACT #2
	scb4.uart.rx	ACT #4	scb4.spi.clk	ACT #6
	scb4.i2c.scl	ACT #7	peri.tr_io_output[90]	ACT #13
	peri.tr_io_input[22]	ACT #14	peri.tr_io_output[22]	ACT #15
P3.3	smartio.io3	fixed	tcpwm0.g0.cnt5-	ACT #0
	peri.tr_io_output[151]	ACT #1	scb4.uart.tx	ACT #4
	scb4.spi.select0	ACT #6	scb4.i2c.scl_do	ACT #7
	peri.tr_io_output[91]	ACT #13	peri.tr_io_input[23]	ACT #14
	peri.tr_io_output[23]	ACT #15		
P4.0	peri.tr_io_output[136]:0	ACT #0	tcpwm0.g1.cnt4+	ACT #1
	tcpwm0.g0.cnt0+	ACT #2	scb4.uart.cts	ACT #4
	scb4.spi.mosi	ACT #6	scb4.i2c.sda_do	ACT #7
	peri.tr_io_output[92]	ACT #13	peri.tr_io_input[24]	ACT #14
	peri.tr_io_output[24]	ACT #15		
P4.1	peri.tr_io_output[137]:0	ACT #0	tcpwm0.g1.cnt4-	ACT #1
	tcpwm0.g0.cnt0-	ACT #2	scb4.uart.rts	ACT #4
	scb4.spi.miso	ACT #6	scb4.i2c.sda	ACT #7
	peri.tr_io_output[93]	ACT #13	peri.tr_io_input[25]	ACT #14
	peri.tr_io_output[25]	ACT #15		
P4.2	peri.tr_io_output[138]:0	ACT #0	tcpwm0.g1.cnt5+	ACT #1
	tcpwm0.g0.cnt1+	ACT #2	scb4.uart.rx	ACT #4
	scb4.spi.clk	ACT #6	scb4.i2c.scl	ACT #7
	peri.tr_io_output[94]	ACT #13	peri.tr_io_input[26]	ACT #14
	peri.tr_io_output[26]	ACT #15		
P4.3	peri.tr_io_output[139]:0	ACT #0	tcpwm0.g1.cnt5-	ACT #1
	tcpwm0.g0.cnt1-	ACT #2	scb4.uart.tx	ACT #4
	scb4.spi.select0	ACT #6	scb4.i2c.scl_do	ACT #7
	peri.tr_io_output[95]	ACT #13	peri.tr_io_input[27]	ACT #14
	peri.tr_io_output[27]	ACT #15		

(table continues...)

Table 6 (continued) GPIO alternate functions and HSIOM routes

GPIO	Alternate functions and HSIOM routes			
P4.4	peri.tr_io_output[140]	ACT #0	tcpwm0.g1.cnt6+	ACT #1
	tcpwm0.g0.cnt2+	ACT #2	scb4.spi.select1	ACT #6
	peri.tr_io_output[98]	ACT #13	peri.tr_io_input[30]	ACT #14
	peri.tr_io_output[30]	ACT #15		
P4.5	peri.tr_io_output[141]	ACT #0	tcpwm0.g1.cnt6-	ACT #1
	tcpwm0.g0.cnt2-	ACT #2	scb4.spi.select2	ACT #6
	peri.tr_io_output[99]	ACT #13	peri.tr_io_input[31]	ACT #14
	peri.tr_io_output[31]	ACT #15		
P4.6	peri.tr_io_output[142]	ACT #0	tcpwm0.g1.cnt7+	ACT #1
	tcpwm0.g0.cnt3+	ACT #2	scb4.spi.select3	ACT #6
	peri.tr_io_output[100]	ACT #13	peri.tr_io_input[32]	ACT #14
	peri.tr_io_output[32]	ACT #15		
P4.7	peri.tr_io_output[143]	ACT #0	tcpwm0.g1.cnt7-	ACT #1
	tcpwm0.g0.cnt3-	ACT #2	peri.tr_io_output[101]	ACT #13
	peri.tr_io_input[33]	ACT #14	peri.tr_io_output[33]	ACT #15
P5.0	smartio.io0	fixed	tcpwm0.g0.cnt6+	ACT #0
	peri.tr_io_output[148]:1	ACT #1	scb3.uart.cts	ACT #4
	scb3.spi.mosi	ACT #6	scb3.i2c.sda	ACT #7
	i3c[0].i3c_sda:1	ACT #10	peri.tr_io_output[102]	ACT #13
	peri.tr_io_input[34]	ACT #14	peri.tr_io_output[34]	ACT #15
P5.1	smartio.io1	fixed	tcpwm0.g0.cnt6-	ACT #0
	peri.tr_io_output[149]:1	ACT #1	scb3.uart.rts	ACT #4
	scb3.spi.miso	ACT #6	scb3.i2c.scl	ACT #7
	i3c[0].i3c_scl:1	ACT #10	peri.tr_io_output[103]	ACT #13
	peri.tr_io_input[35]	ACT #14	peri.tr_io_output[35]	ACT #15
P5.2	smartio.io2	fixed	tcpwm0.g0.cnt7+	ACT #0
	peri.tr_io_output[150]:1	ACT #1	can1.rx	ACT #3
	scb3.uart.rx	ACT #4	scb3.spi.clk	ACT #6
	scb3.i2c.sda	ACT #7	scb3.i2c.sda_do	ACT #8
	peri.tr_io_output[104]	ACT #13	peri.tr_io_input[36]	ACT #14
	peri.tr_io_output[36]	ACT #15		

(table continues...)

Table 6 (continued) GPIO alternate functions and HSIOM routes

GPIO	Alternate functions and HSIOM routes			
P5.3	smartio.io3	fixed	tcpwm0.g0.cnt7-	ACT #0
	peri.tr_io_output[151]:1	ACT #1	can1.tx	ACT #3
	scb3.uart.tx	ACT #4	scb3.spi.select0	ACT #6
	scb3.i2c.scl	ACT #7	scb3.i2c.scl_do	ACT #8
	peri.tr_io_output[105]	ACT #13	peri.tr_io_input[37]	ACT #14
	peri.tr_io_output[37]	ACT #15		
P6.0	smartio.io0	fixed	tcpwm0.g1.cnt4+	ACT #1
	peri.tr_io_output[152]	ACT #2	scb3.uart.cts	ACT #4
	scb3.spi.mosi	ACT #6	scb3.i2c.sda	ACT #7
	i3c[0].i3c_sda:0	ACT #10	peri.tr_io_output[106]	ACT #13
	peri.tr_io_input[38]	ACT #14	peri.tr_io_output[38]	ACT #15
P6.1	smartio.io1	fixed	tcpwm0.g1.cnt4-	ACT #1
	peri.tr_io_output[153]	ACT #2	scb3.uart.rts	ACT #4
	scb3.spi.miso	ACT #6	scb3.i2c.scl	ACT #7
	i3c[0].i3c_scl:0	ACT #10	peri.tr_io_output[107]	ACT #13
	peri.tr_io_input[39]	ACT #14	peri.tr_io_output[39]	ACT #15
P6.2	smartio.io2	fixed	tcpwm0.g1.cnt5+	ACT #1
	peri.tr_io_output[154]	ACT #2	can1.rx	ACT #3
	scb3.uart.rx	ACT #4	scb3.spi.clk	ACT #6
	scb3.i2c.sda	ACT #7	scb3.i2c.sda_do	ACT #8
	peri.tr_io_output[108]	ACT #13	peri.tr_io_input[40]	ACT #14
	peri.tr_io_output[40]	ACT #15		
P6.3	smartio.io3	fixed	tcpwm0.g1.cnt5-	ACT #1
	peri.tr_io_output[155]	ACT #2	can1.tx	ACT #3
	scb3.uart.tx	ACT #4	scb3.spi.select0	ACT #6
	scb3.i2c.scl	ACT #7	scb3.i2c.scl_do	ACT #8
	cpuss.fault[0]:1	ACT #9	peri.tr_io_output[109]	ACT #13
	peri.tr_io_input[41]	ACT #14	peri.tr_io_output[41]	ACT #15

(table continues...)

Table 6 (continued) GPIO alternate functions and HSIOM routes

GPIO	Alternate functions and HSIOM routes			
P7.0	peri.tr_io_output[136]:1	ACT #0	tcpwm0.g1.cnt6+	ACT #1
	peri.tr_io_output[156]	ACT #2	scb2.uart.cts	ACT #4
	scb2.spi.clk	ACT #5	scb2.i2c.scl	ACT #7
	trace.data0	ACT #9	hppass.gpio_out0	ACT #12
	peri.tr_io_output[116]	ACT #13	peri.tr_io_input[48]	ACT #14
	peri.tr_io_output[48]	ACT #15		
P7.1	peri.tr_io_output[137]:1	ACT #0	tcpwm0.g1.cnt6-	ACT #1
	peri.tr_io_output[157]	ACT #2	scb2.uart.tx	ACT #4
	scb2.spi.mosi	ACT #5	scb2.i2c.sda	ACT #7
	trace.data1	ACT #9	hppass.gpio_out1	ACT #12
	peri.tr_io_output[117]	ACT #13	peri.tr_io_input[49]	4
	peri.tr_io_output[49]	ACT #15		
P7.2	peri.tr_io_output[138]:1	ACT #0	tcpwm0.g1.cnt7+	ACT #1
	peri.tr_io_output[158]	ACT #2	scb2.uart.rx	ACT #4
	scb2.spi.miso	ACT #5	scb2.i2c.sda_do	ACT #7
	trace.data2	ACT #9	hppass.gpio_out2	ACT #12
	peri.tr_io_output[118]	ACT #13	peri.tr_io_input[50]	ACT #14
	peri.tr_io_output[50]	ACT #15		
P7.3	peri.tr_io_output[139]:1	ACT #0	tcpwm0.g1.cnt7-	ACT #1
	peri.tr_io_output[159]	ACT #2	scb2.uart.rts	ACT #4
	scb2.spi.select0	ACT #5	scb2.i2c.scl_do	ACT #7
	trace.data3	ACT #9	hppass.gpio_out3	ACT #12
	peri.tr_io_output[119]	ACT #13	peri.tr_io_input[51]	ACT #14
	peri.tr_io_output[51]	ACT #15		
P7.4	pass.gpio_a_aio_esd[0]	fixed	pass.gpio_a_aio_noesd[0]	fixed
	peri.tr_io_output[140]:1	ACT #0	scb2.spi.select1	ACT #5
	trace.clock	ACT #9	hppass.gpio_out4	ACT #12
	peri.tr_io_output[120]	ACT #13	peri.tr_io_input[52]	ACT #14
	peri.tr_io_output[52]	ACT #15		
P7.5	pass.gpio_a_aio_esd[1]	fixed	peri.tr_io_output[141]:1	ACT #0
	scb2.spi.select2	ACT #5	peri.tr_io_output[121]	ACT #13
	peri.tr_io_input[53]	ACT #14	peri.tr_io_output[53]	ACT #15

(table continues...)

Table 6 (continued) GPIO alternate functions and HSIOM routes

GPIO	Alternate functions and HSIOM routes			
P7.6	pass.gpio_a_aio_esd[2]	fixed	pass.gpio_a_aio_noesd[1]	fixed
	peri.tr_io_output[142]:1	ACT #0	scb2.spi.select3	ACT #5
	peri.tr_io_output[122]	ACT #13	peri.tr_io_input[54]	ACT #14
	peri.tr_io_output[54]	ACT #15		
P7.7	pass.gpio_a_aio_esd[3]	fixed	peri.tr_io_output[143]:1	ACT #0
	peri.tr_io_output[123]	ACT #13	peri.tr_io_input[55]	ACT #14
	peri.tr_io_output[55]	ACT #15		
P8.0	lpcomp0.in+	fixed	pass.gpio_b_aio_esd[0]	fixed
	peri.tr_io_output[148]:2	ACT #1	tcpwm0.g2.cnt4+	ACT #2
	scb5.uart.cts	ACT #4	scb5.spi.select0	ACT #5
	scb5.i2c.scl_do	ACT #7	trace.data0	ACT #9
	hppass.gpio_out0	ACT #12	peri.tr_io_output[124]	ACT #13
	peri.tr_io_input[56]	ACT #14	peri.tr_io_output[56]	ACT #15
	swj.trstn	DS #5		
P8.1	lpcomp0.in-	fixed	peri.tr_io_output[149]:2	ACT #1
	tcpwm0.g2.cnt4-	ACT #2	scb5.uart.rx	ACT #4
	scb5.spi.mosi	ACT #5	scb5.i2c.scl	ACT #7
	trace.data1	ACT #9	hppass.gpio_out1	ACT #12
	peri.tr_io_output[125]	ACT #13	peri.tr_io_input[57]	ACT #14
	peri.tr_io_output[57]	ACT #15		
P8.2	lpcomp1.in+	fixed	pass.gpio_b_aio_esd[1]	fixed
	peri.tr_io_output[150]:2	ACT #1	tcpwm0.g2.cnt5+	ACT #2
	can0.rx	ACT #3	scb5.uart.rts	ACT #4
	scb5.spi.miso	ACT #5	scb5.i2c.sda_do	ACT #7
	trace.data2	ACT #9	hppass.gpio_out2	ACT #12
	peri.tr_io_output[126]	ACT #13	peri.tr_io_input[58]	ACT #14
	peri.tr_io_output[58]	ACT #15		

(table continues...)

Table 6 (continued) GPIO alternate functions and HSIOM routes

GPIO	Alternate functions and HSIOM routes			
P8.3	lpcomp1.in-	fixed	pass.gpio_b_aio_noesd[0]	fixed
	peri.tr_io_output[151]:2	ACT #1	tcpwm0.g2.cnt5-	ACT #2
	can0.tx	ACT #3	scb5.uart.tx	ACT #4
	scb5.spi.clk	ACT #5	scb5.i2c.sda	ACT #7
	trace.data3	ACT #9	hppass.gpio_out3	ACT #12
	peri.tr_io_output[127]	ACT #13	peri.tr_io_input[59]	ACT #14
	peri.tr_io_output[59]	ACT #15		
P8.4	pass.gpio_b_aio_esd[2]	fixed	pass.gpio_b_aio_noesd[1]	fixed
	scb5.spi.select1	ACT #5	peri.tr_io_output[128]	ACT #13
	peri.tr_io_input[60]	ACT #14	peri.tr_io_output[60]	ACT #15
P8.5	pass.gpio_b_aio_esd[3]	fixed	scb5.spi.select2	ACT #5
	peri.tr_io_output[129]	ACT #13	peri.tr_io_input[61]	ACT #14
	peri.tr_io_output[61]	ACT #15		
P8.6	scb5.spi.select3	ACT #5	peri.tr_io_output[130]	ACT #13
	peri.tr_io_input[62]	ACT #14	peri.tr_io_output[62]	ACT #15
P8.7	scb5.spi.select4	ACT #5	peri.tr_io_output[131]	ACT #13
	peri.tr_io_input[63]	ACT #14	peri.tr_io_output[63]	ACT #15
P9.0	hibernate_wakeup	fixed	smartio.io0	fixed
	tcpwm0.g2.cnt0+	ACT #0	tcpwm0.g2.cnt6+	ACT #2
	scb0.spi.clk	DS #1	scb0.uart.cts	DS #2
	scb0.i2c.scl	DS #3	scb5.spi.select5	ACT #5
	peri.tr_io_output[132]	ACT #13	peri.tr_io_input[64]	ACT #14
	peri.tr_io_output[64]	ACT #15		
P9.1	smartio.io1	fixed	tcpwm0.g2.cnt0-	ACT #0
	tcpwm0.g2.cnt6-	ACT #2	scb0.spi.select0	DS #1
	scb0.uart.rts	DS #2	scb0.i2c.scl_do	DS #3
	peri.tr_io_output[68]	ACT #13	peri.tr_io_input[0]	ACT #14
	peri.tr_io_output[0]	ACT #15		

(table continues...)

Table 6 (continued) GPIO alternate functions and HSIOM routes

GPIO	Alternate functions and HSIOM routes			
P9.2	smartio.io2	fixed	tcpwm0.g2.cnt1+	ACT #0
	tcpwm0.g2.cnt7+	ACT #2	can0.rx	ACT #3
	scb0.spi.mosi	DS #1	scb0.uart.rx	DS #2
	scb0.i2c.sda	DS #3	trace.clock	ACT #9
	hppass.gpio_out4	ACT #12	peri.tr_io_output[69]	ACT #13
	peri.tr_io_input[1]	ACT #14	peri.tr_io_output[1]	ACT #15
P9.3	smartio.io3	fixed	tcpwm0.g2.cnt1-	ACT #0
	tcpwm0.g2.cnt7-	ACT #2	can0.tx	ACT #3
	scb0.spi.miso	DS #1	scb0.uart.tx	DS #2
	scb0.i2c.sda_do	DS #3	cpuss.clk_fm_pump	ACT #8
	cpuss.fault[0]	ACT #9	peri.tr_io_output[70]	ACT #13
	peri.tr_io_input[2]	ACT #14	peri.tr_io_output[2]	ACT #15
P9.4	smartio.io4	fixed	tcpwm0.g2.cnt2+	ACT #0
	tcpwm0.g2.cnt4+	ACT #2	scb0.spi.select1	DS #1
	peri.tr_io_output[71]	ACT #13	peri.tr_io_input[3]	ACT #14
	peri.tr_io_output[3]	ACT #15		
P9.5	vext_ref_reg	fixed	smartio.io5	fixed
	tcpwm0.g2.cnt2-	ACT #0	tcpwm0.g2.cnt4-	ACT #2
	scb0.spi.select2	DS #1	peri.tr_io_output[72]	ACT #13
	peri.tr_io_input[4]	ACT #14	peri.tr_io_output[4]	ACT #15
P9.6	smartio.io6	fixed	tcpwm0.g2.cnt3+	ACT #0
	tcpwm0.g2.cnt5+	ACT #2	scb0.spi.select3	DS #1
	peri.tr_io_output[73]	ACT #13	peri.tr_io_input[5]	ACT #14
	peri.tr_io_output[5]	ACT #15		
P9.7	svgs.svgs_test_vccd_feed	fixed	smartio.io7	fixed
	tcpwm0.g2.cnt3-	ACT #0	tcpwm0.g2.cnt5-	ACT #2
	scb1.spi.select6	ACT #6	peri.tr_io_output[74]	ACT #13
	peri.tr_io_input[6]	ACT #14	peri.tr_io_output[6]	ACT #15
P10.0	scb1.spi.select1	ACT #6	peri.tr_io_output[77]	ACT #13
	peri.tr_io_input[9]	ACT #14	peri.tr_io_output[9]	ACT #15
P10.1	scb1.spi.select2	ACT #6	peri.tr_io_output[78]	ACT #13
	peri.tr_io_input[10]	ACT #14	peri.tr_io_output[10]	ACT #15

(table continues...)

Table 6 (continued) GPIO alternate functions and HSIOM routes

GPIO	Alternate functions and HSIOM routes			
P10.2	peri.tr_io_output[152]:1	ACT #2	scb1.spi.select3	ACT #6
	peri.tr_io_output[79]	ACT #13	peri.tr_io_input[11]	ACT #14
	peri.tr_io_output[11]	ACT #15		
P12.0	tcpwm0.g1.cnt0+	ACT #1	scb1.spi.select7	ACT #6
	peri.tr_io_output[96]	ACT #13	peri.tr_io_input[28]	ACT #14
	peri.tr_io_output[28]	ACT #15		
P12.1	tcpwm0.g1.cnt0-	ACT #1	scb3.spi.select7	ACT #6
	peri.tr_io_output[97]	ACT #13	peri.tr_io_input[29]	ACT #14
	peri.tr_io_output[29]	ACT #15		
P12.2	tcpwm0.g1.cnt1+	ACT #1	scb3.spi.select1	ACT #6
	peri.tr_io_output[110]	ACT #13	peri.tr_io_input[42]	ACT #14
	peri.tr_io_output[42]	ACT #15		
P12.3	tcpwm0.g1.cnt1-	ACT #1	scb3.spi.select2	ACT #6
	peri.tr_io_output[111]	ACT #13	peri.tr_io_input[43]	ACT #14
	peri.tr_io_output[43]	ACT #15		
P12.4	tcpwm0.g1.cnt2+	ACT #1	scb3.spi.select3	ACT #6
	peri.tr_io_output[112]	ACT #13	peri.tr_io_input[44]	ACT #14
	peri.tr_io_output[44]	ACT #15		
P12.5	tcpwm0.g1.cnt2-	ACT #1	scb3.spi.select4	ACT #6
	peri.tr_io_output[113]	ACT #13	peri.tr_io_input[45]	ACT #14
	peri.tr_io_output[45]	ACT #15		
P12.6	tcpwm0.g1.cnt3+	ACT #1	scb3.spi.select5	ACT #6
	peri.tr_io_output[114]	ACT #13	peri.tr_io_input[46]	ACT #14
	peri.tr_io_output[46]	ACT #15		
P12.7	tcpwm0.g1.cnt3-	ACT #1	scb3.spi.select6	ACT #6
	peri.tr_io_output[115]	ACT #13	peri.tr_io_input[47]	ACT #14
	peri.tr_io_output[47]	ACT #15		
P13.0	scb5.spi.select6	ACT #5	peri.tr_io_output[133]	ACT #13
	peri.tr_io_input[65]	ACT #14	peri.tr_io_output[65]	ACT #15
P13.1	scb5.spi.select7	ACT #5	peri.tr_io_output[134]	ACT #13
	peri.tr_io_input[66]	ACT #14	peri.tr_io_output[66]	ACT #15
P13.2	peri.tr_io_output[135]	ACT #13	peri.tr_io_input[67]	ACT #14
	peri.tr_io_output[67]	ACT #15		

1) ext_clk can be used as both an external clock input and an external clock output, depending on the pin and clock configuration.

Table 7 GPIO alternate functions

Function	GPIOs	Function	GPIOs	Function	GPIOs
cal_wave	P2.1	can0.rx	P8.2, P9.2	can0.tx	P8.3, P9.3
can1.rx	P5.2, P6.2	can1.tx	P5.3, P6.3	cpuss.clk_fm_pump	P9.3
cpuss.fault[0]	P9.3, P6.3	eco_in	P1.0	eco_out	P1.1
ext_clk[1)]	P0.0, P2.2	hibernate_wakeup	P2.0, P9.0	hppass.gpio_out0	P7.0, P8.0
hppass.gpio_out1	P7.1, P8.1	hppass.gpio_out2	P7.2, P8.2	hppass.gpio_out3	P7.3, P8.3
hppass.gpio_out4	P7.4, P9.2	i3c[0].i3c_scl	P5.1, P6.1	i3c[0].i3c_sda	P5.0, P6.0
lpcomp0.in+	P8.0	lpcomp0.in-	P8.1	lpcomp1.in+	P8.2
lpcomp1.in-	P8.3	pass.gpio_a_aio_esd[0]	P7.4	pass.gpio_a_aio_esd[1]	P7.5
pass.gpio_a_aio_esd[2]	P7.6	pass.gpio_a_aio_esd[3]	P7.7	pass.gpio_a_aio_noesd[0]	P7.4
pass.gpio_a_aio_noesd[1]	P7.6	pass.gpio_b_aio_esd[0]	P8.0	pass.gpio_b_aio_esd[1]	P8.2
pass.gpio_b_aio_esd[2]	P8.4	pass.gpio_b_aio_esd[3]	P8.5	pass.gpio_b_aio_noesd[0]	P8.3
pass.gpio_b_aio_noesd[1]	P8.4	peri.tr_io_input[0]	P9.1	peri.tr_io_input[1]	P9.2
peri.tr_io_input[2]	P9.3	peri.tr_io_input[3]	P9.4	peri.tr_io_input[4]	P9.5
peri.tr_io_input[5]	P9.6	peri.tr_io_input[6]	P9.7	peri.tr_io_input[7]	P0.0
peri.tr_io_input[8]	P0.1	peri.tr_io_input[9]	P10.0	peri.tr_io_input[10]	P10.1
peri.tr_io_input[11]	P10.2	peri.tr_io_input[12]	P1.0	peri.tr_io_input[13]	P1.1
peri.tr_io_input[14]	P1.2	peri.tr_io_input[15]	P1.3	peri.tr_io_input[16]	P2.0
peri.tr_io_input[17]	P2.1	peri.tr_io_input[18]	P2.2	peri.tr_io_input[19]	P2.3
peri.tr_io_input[20]	P3.0	peri.tr_io_input[21]	P3.1	peri.tr_io_input[22]	P3.2
peri.tr_io_input[23]	P3.3	peri.tr_io_input[24]	P4.0	peri.tr_io_input[25]	P4.1
peri.tr_io_input[26]	P4.2	peri.tr_io_input[27]	P4.3	peri.tr_io_input[28]	P12.0
peri.tr_io_input[29]	P12.1	peri.tr_io_input[30]	P4.4	peri.tr_io_input[31]	P4.5

(table continues...)

Table 7 (continued) GPIO alternate functions

Function	GPIOs	Function	GPIOs	Function	GPIOs
peri.tr_io_input[32]	P4.6	peri.tr_io_input[33]	P4.7	peri.tr_io_input[34]	P5.0
peri.tr_io_input[35]	P5.1	peri.tr_io_input[36]	P5.2	peri.tr_io_input[37]	P5.3
peri.tr_io_input[38]	P6.0	peri.tr_io_input[39]	P6.1	peri.tr_io_input[40]	P6.2
peri.tr_io_input[41]	P6.3	peri.tr_io_input[42]	P12.2	peri.tr_io_input[43]	P12.3
peri.tr_io_input[44]	P12.4	peri.tr_io_input[45]	P12.5	peri.tr_io_input[46]	P12.6
peri.tr_io_input[47]	P12.7	peri.tr_io_input[48]	P7.0	peri.tr_io_input[49]	P7.1
peri.tr_io_input[50]	P7.2	peri.tr_io_input[51]	P7.3	peri.tr_io_input[52]	P7.4
peri.tr_io_input[53]	P7.5	peri.tr_io_input[54]	P7.6	peri.tr_io_input[55]	P7.7
peri.tr_io_input[56]	P8.0	peri.tr_io_input[57]	P8.1	peri.tr_io_input[58]	P8.2
peri.tr_io_input[59]	P8.3	peri.tr_io_input[60]	P8.4	peri.tr_io_input[61]	P8.5
peri.tr_io_input[62]	P8.6	peri.tr_io_input[63]	P8.7	peri.tr_io_input[64]	P9.0
peri.tr_io_input[65]	P13.0	peri.tr_io_input[66]	P13.1	peri.tr_io_input[67]	P13.2
peri.tr_io_output[0]	P9.1	peri.tr_io_output[1]	P9.2	peri.tr_io_output[2]	P9.3
peri.tr_io_output[3]	P9.4	peri.tr_io_output[4]	P9.5	peri.tr_io_output[5]	P9.6
peri.tr_io_output[6]	P9.7	peri.tr_io_output[7]	P0.0	peri.tr_io_output[8]	P0.1
peri.tr_io_output[9]	P10.0	peri.tr_io_output[10]	P10.1	peri.tr_io_output[11]	P10.2
peri.tr_io_output[12]	P1.0	peri.tr_io_output[13]	P1.1	peri.tr_io_output[14]	P1.2
peri.tr_io_output[15]	P1.3	peri.tr_io_output[16]	P2.0	peri.tr_io_output[17]	P2.1
peri.tr_io_output[18]	P2.2	peri.tr_io_output[19]	P2.3	peri.tr_io_output[20]	P3.0

(table continues...)

Table 7 (continued) GPIO alternate functions

Function	GPIOs	Function	GPIOs	Function	GPIOs
peri.tr_io_output[21]	P3.1	peri.tr_io_output[22]	P3.2	peri.tr_io_output[23]	P3.3
peri.tr_io_output[24]	P4.0	peri.tr_io_output[25]	P4.1	peri.tr_io_output[26]	P4.2
peri.tr_io_output[27]	P4.3	peri.tr_io_output[28]	P12.0	peri.tr_io_output[29]	P12.1
peri.tr_io_output[30]	P4.4	peri.tr_io_output[31]	P4.5	peri.tr_io_output[32]	P4.6
peri.tr_io_output[33]	P4.7	peri.tr_io_output[34]	P5.0	peri.tr_io_output[35]	P5.1
peri.tr_io_output[36]	P5.2	peri.tr_io_output[37]	P5.3	peri.tr_io_output[38]	P6.0
peri.tr_io_output[39]	P6.1	peri.tr_io_output[40]	P6.2	peri.tr_io_output[41]	P6.3
peri.tr_io_output[42]	P12.2	peri.tr_io_output[43]	P12.3	peri.tr_io_output[44]	P12.4
peri.tr_io_output[45]	P12.5	peri.tr_io_output[46]	P12.6	peri.tr_io_output[47]	P12.7
peri.tr_io_output[48]	P7.0	peri.tr_io_output[49]	P7.1	peri.tr_io_output[50]	P7.2
peri.tr_io_output[51]	P7.3	peri.tr_io_output[52]	P7.4	peri.tr_io_output[53]	P7.5
peri.tr_io_output[54]	P7.6	peri.tr_io_output[55]	P7.7	peri.tr_io_output[56]	P8.0
peri.tr_io_output[57]	P8.1	peri.tr_io_output[58]	P8.2	peri.tr_io_output[59]	P8.3
peri.tr_io_output[60]	P8.4	peri.tr_io_output[61]	P8.5	peri.tr_io_output[62]	P8.6
peri.tr_io_output[63]	P8.7	peri.tr_io_output[64]	P9.0	peri.tr_io_output[65]	P13.0
peri.tr_io_output[66]	P13.1	peri.tr_io_output[67]	P13.2	peri.tr_io_output[68]	P9.1
peri.tr_io_output[69]	P9.2	peri.tr_io_output[70]	P9.3	peri.tr_io_output[71]	P9.4
peri.tr_io_output[72]	P9.5	peri.tr_io_output[73]	P9.6	peri.tr_io_output[74]	P9.7
peri.tr_io_output[75]	P0.0	peri.tr_io_output[76]	P0.1	peri.tr_io_output[77]	P10.0

(table continues...)

Table 7 (continued) GPIO alternate functions

Function	GPIOs	Function	GPIOs	Function	GPIOs
peri.tr_io_output[78]	P10.1	peri.tr_io_output[79]	P10.2	peri.tr_io_output[80]	P1.0
peri.tr_io_output[81]	P1.1	peri.tr_io_output[82]	P1.2	peri.tr_io_output[83]	P1.3
peri.tr_io_output[84]	P2.0	peri.tr_io_output[85]	P2.1	peri.tr_io_output[86]	P2.2
peri.tr_io_output[87]	P2.3	peri.tr_io_output[88]	P3.0	peri.tr_io_output[89]	P3.1
peri.tr_io_output[90]	P3.2	peri.tr_io_output[91]	P3.3	peri.tr_io_output[92]	P4.0
peri.tr_io_output[93]	P4.1	peri.tr_io_output[94]	P4.2	peri.tr_io_output[95]	P4.3
peri.tr_io_output[96]	P12.0	peri.tr_io_output[97]	P12.1	peri.tr_io_output[98]	P4.4
peri.tr_io_output[99]	P4.5	peri.tr_io_output[100]	P4.6	peri.tr_io_output[101]	P4.7
peri.tr_io_output[102]	P5.0	peri.tr_io_output[103]	P5.1	peri.tr_io_output[104]	P5.2
peri.tr_io_output[105]	P5.3	peri.tr_io_output[106]	P6.0	peri.tr_io_output[107]	P6.1
peri.tr_io_output[108]	P6.2	peri.tr_io_output[109]	P6.3	peri.tr_io_output[110]	P12.2
peri.tr_io_output[111]	P12.3	peri.tr_io_output[112]	P12.4	peri.tr_io_output[113]	P12.5
peri.tr_io_output[114]	P12.6	peri.tr_io_output[115]	P12.7	peri.tr_io_output[116]	P7.0
peri.tr_io_output[117]	P7.1	peri.tr_io_output[118]	P7.2	peri.tr_io_output[119]	P7.3
peri.tr_io_output[120]	P7.4	peri.tr_io_output[121]	P7.5	peri.tr_io_output[122]	P7.6
peri.tr_io_output[123]	P7.7	peri.tr_io_output[124]	P8.0	peri.tr_io_output[125]	P8.1
peri.tr_io_output[126]	P8.2	peri.tr_io_output[127]	P8.3	peri.tr_io_output[128]	P8.4
peri.tr_io_output[129]	P8.5	peri.tr_io_output[130]	P8.6	peri.tr_io_output[131]	P8.7
peri.tr_io_output[132]	P9.0	peri.tr_io_output[133]	P13.0	peri.tr_io_output[134]	P13.1

(table continues...)

Table 7 (continued) GPIO alternate functions

Function	GPIOs	Function	GPIOs	Function	GPIOs
peri.tr_io_output[135]	P13.2	peri.tr_io_output[136]	P4.0, P7.0	peri.tr_io_output[137]	P4.1, P7.1
peri.tr_io_output[138]	P4.2, P7.2	peri.tr_io_output[139]	P4.3, P7.3	peri.tr_io_output[140]	P4.4, P7.4
peri.tr_io_output[141]	P4.5, P7.5	peri.tr_io_output[142]	P4.6, P7.6	peri.tr_io_output[143]	P4.7, P7.7
peri.tr_io_output[144]	P2.0, P1.0	peri.tr_io_output[145]	P2.1, P1.1	peri.tr_io_output[146]	P2.2, P1.2
peri.tr_io_output[147]	P2.3, P1.3	peri.tr_io_output[148]	P3.0, P5.0, P8.0	peri.tr_io_output[149]	P3.1, P5.1, P8.1
peri.tr_io_output[150]	P3.2, P5.2, P8.2	peri.tr_io_output[151]	P3.3, P5.3, P8.3	peri.tr_io_output[152]	P6.0, P10.2
peri.tr_io_output[153]	P6.1, P1.0	peri.tr_io_output[154]	P6.2, P1.1	peri.tr_io_output[155]	P6.3, P1.2
peri.tr_io_output[156]	P7.0, P1.3	peri.tr_io_output[157]	P7.1, P3.0	peri.tr_io_output[158]	P7.2, P3.1
peri.tr_io_output[159]	P7.3, P3.2	scb0.i2c.scl	P9.0	scb0.i2c.scl_do	P9.1
scb0.i2c.sda	P9.2	scb0.i2c.sda_do	P9.3	scb0.spi.clk	P9.0
scb0.spi.miso	P9.3	scb0.spi.mosi	P9.2	scb0.spi.select0	P9.1
scb0.spi.select1	P9.4	scb0.spi.select2	P9.5	scb0.spi.select3	P9.6
scb0.uart.cts	P9.0	scb0.uart.rts	P9.1	scb0.uart.rx	P9.2
scb0.uart.tx	P9.3	scb1.i2c.scl	P1.3, P2.1	scb1.i2c.scl_do	P1.0, P2.0
scb1.i2c.sda	P1.2, P2.2	scb1.i2c.sda_do	P1.1, P2.3	scb1.spi.clk	P1.1, P2.1
scb1.spi.miso	P1.3, P2.3	scb1.spi.mosi	P1.2, P2.2	scb1.spi.select0	P1.0, P2.0
scb1.spi.select1	P10.0	scb1.spi.select2	P10.1	scb1.spi.select3	P10.2
scb1.spi.select4	P0.0	scb1.spi.select5	P0.1	scb1.spi.select6	P9.7
scb1.spi.select7	P12.0	scb1.uart.cts	P1.0, P2.0	scb1.uart.rts	P1.1, P2.1
scb1.uart.rx	P1.2, P2.2	scb1.uart.tx	P1.3, P2.3	scb2.i2c.scl	P7.0
scb2.i2c.scl_do	P7.3	scb2.i2c.sda	P7.1	scb2.i2c.sda_do	P7.2
scb2.spi.clk	P7.0	scb2.spi.miso	P7.2	scb2.spi.mosi	P7.1
scb2.spi.select0	P7.3	scb2.spi.select1	P7.4	scb2.spi.select2	P7.5
scb2.spi.select3	P7.6	scb2.uart.cts	P7.0	scb2.uart.rts	P7.3
scb2.uart.rx	P7.2	scb2.uart.tx	P7.1	scb3.i2c.scl	P5.1, P5.3, P6.1, P6.3
scb3.i2c.scl_do	P5.3, P6.3	scb3.i2c.sda	P5.0, P5.2, P6.0, P6.2	scb3.i2c.sda_do	P5.2, P6.2

(table continues...)

Table 7 (continued) GPIO alternate functions

Function	GPIOs	Function	GPIOs	Function	GPIOs
scb3.spi.clk	P5.2, P6.2	scb3.spi.miso	P5.1, P6.1	scb3.spi.mosi	P5.0, P6.0
scb3.spi.select0	P5.3, P6.3	scb3.spi.select1	P12.2	scb3.spi.select2	P12.3
scb3.spi.select3	P12.4	scb3.spi.select4	P12.5	scb3.spi.select5	P12.6
scb3.spi.select6	P12.7	scb3.spi.select7	P12.1	scb3.uart.cts	P5.0, P6.0
scb3.uart.rts	P5.1, P6.1	scb3.uart.rx	P5.2, P6.2	scb3.uart.tx	P5.3, P6.3
scb4.i2c.scl	P3.2, P4.2	scb4.i2c.scl_do	P3.3, P4.3	scb4.i2c.sda	P3.1, P4.1
scb4.i2c.sda_do	P3.0, P4.0	scb4.spi.clk	P3.2, P4.2	scb4.spi.miso	P3.1, P4.1
scb4.spi.mosi	P3.0, P4.0	scb4.spi.select0	P3.3, P4.3	scb4.spi.select1	P4.4
scb4.spi.select2	P4.5	scb4.spi.select3	P4.6	scb4.uart.cts	P3.0, P4.0
scb4.uart.rts	P3.1, P4.1	scb4.uart.rx	P3.2, P4.2	scb4.uart.tx	P3.3, P4.3
scb5.i2c.scl	P8.1	scb5.i2c.scl_do	P8.0	scb5.i2c.sda	P8.3
scb5.i2c.sda_do	P8.2	scb5.spi.clk	P8.3	scb5.spi.miso	P8.2
scb5.spi.mosi	P8.1	scb5.spi.select0	P8.0	scb5.spi.select1	P8.4
scb5.spi.select2	P8.5	scb5.spi.select3	P8.6	scb5.spi.select4	P8.7
scb5.spi.select5	P9.0	scb5.spi.select6	P13.0	scb5.spi.select7	P13.1
scb5.uart.cts	P8.0	scb5.uart.rts	P8.2	scb5.uart.rx	P8.1
scb5.uart.tx	P8.3	smartio0.io0	P0.0	smartio0.io1	P0.1
smartio1.io0	P1.0	smartio1.io1	P1.1	smartio1.io2	P1.2
smartio1.io3	P1.3	smartio2.io0	P2.0	smartio2.io1	P2.1
smartio2.io2	P2.2	smartio2.io3	P2.3	smartio3.io0	P3.0
smartio3.io1	P3.1	smartio3.io2	P3.2	smartio3.io3	P3.3
smartio5.io0	P5.0	smartio5.io1	P5.1	smartio5.io2	P5.2
smartio5.io3	P5.3	smartio6.io0	P6.0	smartio6.io1	P6.1
smartio6.io2	P6.2	smartio6.io3	P6.3	smartio9.io0	P9.0
smartio9.io1	P9.1	smartio9.io2	P9.2	smartio9.io3	P9.3
smartio9.io4	P9.4	smartio9.io5	P9.5	smartio9.io6	P9.6
smartio9.io7	P9.7	svgs.svgs_test_vccd_feed	P9.7	swj.swclk/tclk	P1.2
swj.swdio/tms	P1.3	swj.tdi	P2.0	swj.tdo	P2.1
swj.trstn	P8.0	tcpwm0.g0.cnt0+	P4.0	tcpwm0.g0.cnt0-	P4.1
tcpwm0.g0.cnt1+	P4.2	tcpwm0.g0.cnt1-	P4.3	tcpwm0.g0.cnt2+	P4.4
tcpwm0.g0.cnt2-	P4.5	tcpwm0.g0.cnt3+	P4.6	tcpwm0.g0.cnt3-	P4.7
tcpwm0.g0.cnt4+	P3.0	tcpwm0.g0.cnt4-	P3.1	tcpwm0.g0.cnt5+	P3.2
tcpwm0.g0.cnt5-	P3.3	tcpwm0.g0.cnt6+	P5.0	tcpwm0.g0.cnt6-	P5.1

(table continues...)

Table 7 (continued) GPIO alternate functions

Function	GPIOs	Function	GPIOs	Function	GPIOs
tcpwm0.g0.cnt7+	P5.2	tcpwm0.g0.cnt7-	P5.3	tcpwm0.g1.cnt0+	P12.0
tcpwm0.g1.cnt0-	P12.1	tcpwm0.g1.cnt1+	P12.2	tcpwm0.g1.cnt1-	P12.3
tcpwm0.g1.cnt2+	P12.4	tcpwm0.g1.cnt2-	P12.5	tcpwm0.g1.cnt3+	P12.6
tcpwm0.g1.cnt3-	P12.7	tcpwm0.g1.cnt4+	P4.0, P6.0	tcpwm0.g1.cnt4-	P4.1, P6.1
tcpwm0.g1.cnt5+	P4.2, P6.2	tcpwm0.g1.cnt5-	P4.3, P6.3	tcpwm0.g1.cnt6+	P4.4, P7.0
tcpwm0.g1.cnt6-	P4.5, P7.1	tcpwm0.g1.cnt7+	P4.6, P7.2	tcpwm0.g1.cnt7-	P4.7, P7.3
tcpwm0.g2.cnt0+	P9.0	tcpwm0.g2.cnt0-	P9.1	tcpwm0.g2.cnt1+	P9.2
tcpwm0.g2.cnt1-	P9.3	tcpwm0.g2.cnt2+	P9.4	tcpwm0.g2.cnt2-	P9.5
tcpwm0.g2.cnt3+	P9.6	tcpwm0.g2.cnt3-	P9.7	tcpwm0.g2.cnt4+	P8.0, P9.4
tcpwm0.g2.cnt4-	P8.1, P9.5	tcpwm0.g2.cnt5+	P8.2, P9.6	tcpwm0.g2.cnt5-	P8.3, P9.7
tcpwm0.g2.cnt6+	P2.0, P9.0	tcpwm0.g2.cnt6-	P2.1, P9.1	tcpwm0.g2.cnt7+	P2.2, P9.2
tcpwm0.g2.cnt7-	P2.3, P9.3	trace.clock	P7.4, P9.2	trace.data0	P7.0, P8.0
trace.data1	P7.1, P8.1	trace.data2	P7.2, P8.2	trace.data3	P7.3, P8.3
vext_ref_reg	P9.5	wco_in	P0.1	wco_out	P0.0

1) ext_clk can be used as both external clock input and external clock output depending on the pin and clock configuration

7 Electrical specifications

***Note**: All electrical specifications are tentative values derived from simulation results. Final specification values will be updated after device characterization.*

7.1 Absolute maximum ratings

Table 8 Absolute maximum ratings

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SID1	Analog or Digital Supply relative to VSS (VSSD=VSSA)	VDD_ABS	-0.5	-	4	V	Absolute maximum
SID2	Direct digital core voltage input relative to VSSD	VCCD_ABS	-0.5	-	1.1	V	Absolute maximum
SID3	GPIO voltage: VDDD or VDDA	VGPIO_ABS	-0.5	-	4.5	V	Absolute maximum
SID4	Current per GPIO	IGPIO_ABS	-25	-	25	mA	Absolute maximum
SID5	GPIO injection current per pin	IGPIO_injection	-0.5	-	0.5	mA	Absolute maximum
SID3A	Electrostatic discharge human body model(HBM)	ESD_HBM	2000	-	-	V	Absolute maximum
SID4A	Electrostatic discharge charged device model(CDM)	ESD_CDM	500	-	-	V	Absolute maximum
SID5A	Pin current for latchup free operation	LU	-100	-	100	mA	Absolute maximum
SIDWA8	Maximum undershoot voltage for I/O	Vundershoot	-	-	-0.5	V	Duration not to exceed 25% of the duty cycle
SIDWA9	Maximum overshoot voltage for I/O	Vovershoot	-	-	4.13	V	Duration not to exceed 25% of the duty cycle
SIDWA10	Maximum junction temperature	Tj	-	-	125	°C	Absolute maximum

7.2 DC specifications

Table 9 DC specifications

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SID6	Internal regulator	VDDD	1.71	-	3.63	V	
SID7B	GPIO Supply for Ports 1/2/3/4/5/6/7/10 and 12	VDDIO_0	1.71	-	3.63	V	
SID7EP	E-Fuse programming time	EFUSETIME	-	-	5.5	µs	TSWITCHON = 0.5 µs Switch on time of 0.5 µs included
SID7C	GPIO supply for Ports 8/9 and 13	VDDIO_1	1.71	-	3.63	V	
SID7A	Analog power supply for ADC and comparator	VDDA	1.71	-	3.63	V	

(table continues...)

Table 9 (continued) DC specifications

SID7F	Supply for Port 11 (USB or GPIO) when present	VDDUSB	1.71	-	3.63	V	
SID6B	Backup power. Normally shorted to VDDD (supply Port 0)	VBACKUP	1.71	-	3.63	V	Minimum is 1.4 V in Backup mode
SID7D	Chip supply ground	VSSS	-	0	-	V	
SID7E	GPIO supply ground	VSSIO	-	VSSS	-	V	
SID7F	Analog ground	VSSA	-	VSSS	-	V	
SID8	Output voltage for OD mode (for core logic bypass)	VCCD (OD)	-	1.2	-	V	Overdrive mode
SID8A	Output voltage for LP mode (for core logic bypass)	VCCD (LP)	-	1.1	-	V	Low power mode
SID8B	Output voltage for MF mode (for core logic bypass)	VCCD (MF)	-	1	-	V	Medium Frequency mode. Valid for -20 to 125°C.
SID8C	Output voltage for ULP mode (for core logic bypass)	VCCD (ULP)	-	0.9	-	V	Ultra-Low Power mode. Valid for -20 to 125°C.
SID8D	Frequency for core logic in OD mode	FOD	-	180	-	MHz	Overdrive mode
SID8E	Frequency for core logic in LP mode	FLP	-	150	-	MHz	Low Power mode
SID8F	Frequency for core logic in MF mode	FMF	-	70	-	MHz	Medium Frequency mode
SID8G	Frequency for core logic in ULP mode	FULP	-	50	-	MHz	Ultra-Low Power mode
SID10	External Regulator voltage (VCCD) bypass	CEFC	3.8	4.7	5.6	µF	X5R ceramic or better.
SID11	Power supply decoupling capacitor	CEXC	-	10	-	µF	X5R ceramic or better.

7.3 Deep Sleep mode

Table 10 Deep Sleep mode

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SIDDS1	With internal LDO enabled and no SRAM retention	IDD33	-	15.5	-	µA	Not including analog leakage on VDDA and VAREF_EXT
SIDDS1_A	With internal LDO enabled and 64K SRAM retention	IDD33A	-	16.5	-	µA	Not including analog leakage on VDDA and VAREF_EXT

(table continues...)

Table 10 (continued) Deep Sleep mode

SIDDS1_B	With internal LDO enabled and 128K SRAM retention	IDD33B	-	17.5	-	µA	Not including analog leakage on VDDA and VAREF_EXT
SIDDS2	Leakage on analog supply and analog reference in Deep Sleep mode	IDDA	-	0.1	-	µA	

7.4 Hibernate mode

Table 11 Hibernate mode

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SIDHIB1	Leakage current at VDDD = 1.8 V	IDD34	-	300	-	nA	VDDD = 1.8 V. No clocks running (not including analog leakage on VDDA and VAREF_EXT)
SIDHIB2	Leakage current at VDDD = 3.3 V	IDD34A	-	2400	-	nA	VDDD = 3.3 V. No clocks running (not including analog leakage on VDDA and VAREF_EXT)
SIDHIB3	Leakage current at VDDD = 1.8 V with WCO running	IDD35	-	800	-	nA	VDDD = 1.8 V. WCO is running. LPComp active (not including analog leakage on VDDA and VAREF_EXT)
SIDHIB4	Leakage current at VDDD = 3.3 V with WCO running	IDD35A	-	3000	-	nA	VDDD = 3.3 V. WCO is running. LPComp active (not including analog leakage on VDDA and VAREF_EXT)
SIDHIB5	Leakage on analog supply and analog reference in hibernate mode	IDDA	-	100	-	nA	Typical silicon and typical temperature

7.5 Cortex®-M33 Active mode

Table 12 Cortex®-M33 Active mode

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SIDC2	Execute from Cache; CM33 Active PLL. Dhrystone in OD mode & VDDD = 3.3 V	IDD4	-	21	43	mA	VDDD = 3.3 V Max at TA = 105°C All peripherals disabled
SIDC2A	Execute from Cache; CM33 Active PLL. Dhrystone in OD mode & VDDD = 1.8 V	IDD4A	-	21	43	mA	VDDD = 1.8 V Max at TA = 105°C All peripherals disabled
SIDC3	Execute from Cache; CM33 Active PLL. Dhrystone in LP mode and VDDD = 3.3 V	IDD5	-	16.5	35	mA	VDDD = 3.3 V Max at TA = 105°C All peripherals disabled
SIDC3A	Execute from Cache; CM33 Active PLL. Dhrystone in LP mode and VDDD = 1.8 V	IDD5A	-	16.5	35	mA	VDDD = 1.8 V Max at TA = 105°C All peripherals disabled
SIDC4	Execute from Cache; CM33 Active PLL Dhrystone in MF mode and VDDD = 3.3 V	IDD6	-	8	23	mA	VDDD = 3.3 V Max at TA = 105°C All peripherals disabled
SIDC4A	Execute from Cache; CM33 Active PLL Dhrystone in MF mode and VDDD = 1.8 V	IDD6A	-	8	23	mA	VDDD = 1.8 V Max at TA = 105°C All peripherals disabled
SIDC5	Execute from Cache; CM33 Active PLL Dhrystone in ULP mode and VDDD = 3.3 V	IDD7	-	6	19	mA	VDDD = 3.3 V Max at TA = 105°C All peripherals disabled
SIDC5A	Execute from Cache; CM33 Active PLL Dhrystone in ULP mode and VDDD = 1.8 V	IDD7A	-	6	19	mA	VDDD = 1.8 V Max at TA = 105°C All peripherals disabled

7.6 Cortex®-M33 Sleep mode

Table 13 Cortex®-M33 Sleep mode

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SIDS1	CM33 Sleep PLL in OD mode and VDDD = 3.3 V	IDD11	-	11.5	20	mA	VDDD = 3.3 V Max at TA = 105°C
SIDS1A	CM33 Sleep PLL in OD mode and VDDD = 1.8 V	IDD11A	-	11.5	20	mA	VDDD = 1.8 V Max at TA = 105°C
SIDS2	CM33 Sleep PLL in LP mode and VDDD = 3.3 V	IDD12	-	8.6	16	mA	VDDD = 3.3 V Max at TA = 105°C
SIDS2A	CM33 Sleep PLL in LP mode and VDDD = 1.8 V	IDD12A	-	8.6	16	mA	VDDD = 1.8 V Max at TA = 105°C
SIDS3	CM33 Sleep PLL in MF mode and VDDD = 3.3 V	IDD13	-	4.6	12	mA	VDDD = 3.3 V Max at TA = 105°C
SIDS3A	CM33 Sleep PLL in MF mode and VDDD = 1.8 V	IDD13A	-	4.6	12	mA	VDDD = 1.8 V Max at TA = 105°C
SIDS4	CM33 Sleep PLL in ULP mode and VDDD = 3.3 V	IDD14	-	3.5	9.5	mA	VDDD = 3.3 V Max at TA = 105°C
SIDS4A	CM33 Sleep PLL in ULP mode and VDDD = 1.8 V	IDD14A	-	3.5	9.5	mA	VDDD = 1.8 V Max at TA = 105°C

7.7 Boot time

Table 14 Boot time

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SIDBT0	Boot time after reset (without secure boot)	BTIME_NO_SEC	-	-	1.2	ms	
SIDBT1	Boot time after reset (including HASH verification)	BTIME	-	-	18.5	ms	HASH of OEM image size of 256 KB
SIDBT1_A	Boot time after reset (including HASH verification)	BTIME_512	-	-	30.5	ms	HASH of OEM image size of 512 KB
SIDBT2	Boot time after reset (including HASH verification & signature validation) with ECDSA-256	BTIME_VER_256	-	-	93	ms	HASH of OEM image size of 256 KB
SIDBT2_A	Boot time after reset (including HASH verification & signature validation) with ECDSA-P-521	BTIME_VER_521	-	-	336	ms	

7.8 Power mode transition times

Table 15 Power mode transition times

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SID13A	Deep Sleep to Active transition time for VDDD > 2.25 V	TDS_ACT	-	-	45	µs	DS to Active transition with VCCD = 1.2 V and VDDD > 2.25 V
SID13A1	Deep Sleep to Active transition time for VDDD < 2.25 V	TDS_ACT1	-	-	45	µs	DS to Active transition VCCD = 1.2 V and VDDD < 2.25 V
SID13B	Deep Sleep to Active LP transition time for VDDD > 2.25 V	TDS_ACTLP	-	-	26	µs	DS to Active LP transition VCCD = 1.1 V and VDDD > 2.25 V
SID13B1	Deep Sleep to Active LP transition time for VDDD < 2.25 V	TDS_ACTLP1	-	-	26	µs	DS to Active LP transition VCCD = 1.1 V and VDDD < 2.25 V
SID13C	Deep Sleep-RAM to Active transition time	TDSR_ACT	-	-	750	µs	DS-RAM to Active with 1.2 V operation
SID13D	Deep Sleep-RAM to Active LP transition time	TDSR_ACTULP	-	-	750	µs	DS-RAM to Active LP with 1.1 V operation
SID14	Hibernate to Active transition time	THIB_ACT	-	-	1800	µs	Including PLL lock time
SID18	Active to Deep Sleep transition for VDDD > 2.25 V	TACT_DS	-	-	35	µs	With VCCD = 1.2 VVDDD > 2.25 V
SID18A	Active to Deep Sleep transition for VDDD < 2.25 V	TACT_DS1	-	-	35	µs	With VCCD = 1.2 VVDDD < 2.25 V

7.9 Smart IO subsystem specifications

Table 16 Smart IO subsystem specifications

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SID420	Smart I/O bypass delay	SMIO_BYP	-	-	2	ns	For LP mode with VDDD = 3.3 V
SID421	Smart I/O LUT propagation delay	SMIO_LUT	-	6	-	ns	For LP mode with VDDD = 3.3 V

7.10 USB block specifications

Table 17 USB block specifications

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SID322U	Device supply for USB operation (functional operation only)	VUSB_3	3.15	-	3.6	V	USB configured
SID323U	Device supply for USB operation	VUSB_3.3	2.85	-	3.6	V	USB configured
SID325U	Block supply current in Active mode	IUSB_CONFIG	-	8	-	mA	VDDD = 3.3 V
SID328	Block supply current in suspend mode	IUSB_SUSPEND_C	-	0.5	-	mA	VDDD = 3.3 V with device connected
SID329	Block supply current in suspend mode	IUSB_SUSPEND_D	-	0.3	-	mA	VDDD = 3.3 V with device disconnected
SID330U	USB driver impedance	USB_DRIVE_RES	28	-	44	Ω	
SID331U	USB pull-down resistors in Host mode	USB_PULLDOWN	14.3	-	24.8	kΩ	
SID332U	Active mode	USB_PULLUP	900	-	1575	Ω	Bus idle
SID333U	Idle mode range	USB_PULLUP_IDLE	1425	-	3090	Ω	Upstream device transmitting

7.11 XRES Active Low specifications

7.11.1 XRES DC specifications

Table 18 XRES DC specifications

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SID17	IDD when XRES asserted	TXRES_IDD	-	180	-	µA	
SID18	IDD when XRES asserted	TXRES_IDD_1	-	330	-	µA	
SID77	Input voltage high threshold	VIH	1.197	-	-	V	CMOS input
SID78	Input voltage low threshold	VIL	-	-	1.089	V	CMOS input
SID80	Input capacitance	CIN	-	3	-	pF	XRES resistor removed
SID81	Input voltage hysteresis	VHYSXRES	-	100	-	mV	
SID82	Current through protection diode to VDDS/VSSS	IDIODE	-	-	100	µA	

7.11.2 XRES AC specifications

Table 19 XRES AC specifications

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SID15	POR or XRES release to Active transition time	TXRES_ACT	-	-	2.7	ms	With BOOT_OD_CLOCK = 180 MHz. LISTEN_WINDOW = 0. BOOT_SIMPLE_APP configuration.
SID16	XRES pulse width	TXRES_PW	5	-	-	µs	

7.12 GPIO specifications

7.12.1 GPIO DC specifications

Table 20 GPIO DC specifications

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SID57	Input voltage high threshold	VIH	0.7*VDDIO	-	-	V	CMOS input
SID57A	Input current when pad > VDDIO for OVT inputs	Iihs	-	-	10	µA	per I2C spec
SID58	Input voltage low threshold	VIL	-	-	0.3*VDDIO	V	CMOS input
SID243	LVTTL input. VDD ≥ 2.7 V	VIHLVTTL	2	-	-	V	
SID244	LVTTL input VDD ≥ 2.7 V	VILLVTTL	-	-	0.8	V	
SID59	Output Voltage high level	VOH	VDDIO-0.5	-	-	V	Ioh = 6 mA
SID62A	Output Voltage low level	VOL	-	-	0.4	V	Iol = 6 mA
SID63	Pull-up resistor	RPULLUP	3.5	5.6	8.5	kΩ	
SID64	Pull-down resistor	RPULLDOWN	3.5	5.6	8.5	kΩ	
SID65	Input leakage current (Absolute value)	IIL	-	-	2	nA	TA = 25 °C VDDD = 3 V
SID66	Input capacitance	CIN	-	-	5	pF	
SID67	Input hysteresis LVTTL VDD > 2.7 V	VHYSTTL	100	0	-	mV	
SID68	Input hysteresis CMOS	VHYSCMOS	85.5	-	-	mV	
SID69	Current through protection diode to VDDS/VSSS	IDIODE	-	-	100	µA	
SID69A	Maximum total source or sink chip current	ITOT_GPIO	-	-	200	mA	

7.12.2 GPIO AC specifications

Table 21 GPIO AC Specifications

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SID70	Rise time in fast strong mode 10% to 90% of VDDD	TRISEF	-	-	5.5	ns	Cload = 15 pF. 8 mA drive strength. VDDIO ≤ 2.7 V
SID70A	Rise time in fast strong mode 10% to 90% of VDDD	TRISEF_1	-	-	3.5	ns	Cload = 15 pF. 8 mA drive strength. 2.7 V < VDDIO ≤ 3.6 V
SID71	Fall time in fast strong mode 10% to 90% of VDDD	TFALLF	-	-	5.5	ns	Cload = 15 pF. 8 mA drive strength. VDDIO ≤ 2.7 V
SID71A	Fall time in fast strong mode 10% to 90% of VDDD	TFALLF_1	-	-	3.5	ns	Cload = 15 pF. 8 mA drive strength. 2.7 V < VDDIO ≤ 3.6 V
SID72	Rise time in slow strong mode 10% to 90% of VDDD	TRISES_1	-	-	14.4	ns	Cload = 15 pF. 8 mA drive strength. VDDIO ≤ 2.7 V
SID72A	Rise time in slow strong mode 10% to 90% of VDDD	TRISES_2	-	-	7.2	ns	Cload = 15 pF. 8 mA drive strength. 2.7 V < VDDIO ≤ 3.6 V
SID73	Fall time in slow strong mode 10% to 90% of VDDD	TFALLS_1	-	-	14.4	ns	Cload = 15 pF. 8 mA drive strength. VDDIO ≤ 2.7 V
SID73A	Fall time in slow strong mode 10% to 90% of VDDD	TFALLS_2	-	-	7.2	ns	Cload = 15 pF. 8 mA drive strength. 2.7 V < VDDIO ≤ 3.6 V
SID73G	Fall time (30% to 70% of VDD) in slow strong mode	TFALL_I2C	0	-	250	ns	Cload = 10 pF to 400 pF. 8 mA drive strength. Refers to VDDIO_0 and VDDIO_1
SID74	GPIO Fout fast strong mode	FGPIOUT1	-	-	80	MHz	90/10%. 15 pF load. 60/40 duty cycle
SID75	GPIO Fout slow strong mode	FGPIOUT2	-	-	16.7	MHz	90/10%. 15 pF load. 60/40 duty cycle
SID76	GPIO Fout fast strong mode	FGPIOUT3	-	-	7	MHz	90/10%. 25 pF load. 60/40 duty cycle

(table continues...)

Table 21 (continued) GPIO AC Specifications

SID245	GPIO Fout slow strong mode	FGPIOUT4	-	-	3.5	MHz	90/10%. 25 pF load. 60/40 duty cycle
SID246	GPIO input operating frequency	FGPIOIN	-	-	100	MHz	90/10% Vio

7.13 Analog peripherals

7.13.1 Analog subsystem

Table 22 Analog subsystem

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SIDAS1	Leakage on single analog input pin	AIN_LEAK	-300	-	300	nA	
SIDAS2	Input capacitance of CSG	AIN_CAP_CSG	-	-	1	pF	Valid for VDDA ≥ 2.7 V
SIDAS2A	Input capactiance of ADC	AIN_CAP_ADC	-	-	3	pF	Valid for VDDA ≥ 2.7 V. Guaranteed by design
SIDAS3	Total series resistance on channel reaching CSG	AIN_RES_CSGS	-	-	500	Ω	Valid for VDDA ≥ 2.7 V
SIDAS3A	Total parallel resistance on channel reaching CSG	AIN_RES_CSGP	-	-	400	MOhm	Valid for VDDA ≥ 2.7 V
SIDAS4	Total resistance of analog channel directly connected to S/H	AIN_RES_ADC	-	-	740	Ω	Valid for VDDA ≥ 2.7 V
SIDAS4A	Total resistance of analog channel connected to S/H through AMUX	AIN_RES_ADC_AMUX	-	-	2600	Ω	Valid for VDDA ≥ 2.7 V

7.13.2 Low-power comparator DC specifications

Table 23 Low-power comparator DC specifications

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SID84	Input offset voltage for COMP1. Normal power mode	VOFFSET1	-10	-	10	mV	
SID85A	Input offset voltage. Low-power mode	VOFFSET2	-25	±12	25	mV	
SID85B	Input offset voltage. Ultra low-power mode	VOFFSET3	-25	±12	25	mV	
SID86	Hysteresis when enabled in normal mode	VHYST1	-	-	60	mV	
SID86A	Hysteresis when enabled in low-power mode	VHYST2	-	-	80	mV	

(table continues...)

Table 23 (continued) Low-power comparator DC specifications

SID87	Input common mode voltage in normal mode	VICM1	0.1	-	-0.1	V	
SID247	Input common mode voltage in Low Power mode	VICM2	0.1	-	-0.1	V	
SID247A	Input common mode voltage in ultra-low power mode	VICM3	0.1	-	-0.1	V	
SID88	Common mode rejection ratio in normal power mode	CMRR	42	-	-	dB	
SID89	Block current in normal mode	ICMP1	-	-	150	µA	
SID248	Block current in low power mode	ICMP2	-	-	10	µA	
SID249	Block current in ultra low-power mode	ICMP3	-	0.3	0.85	µA	
SID90	DC input impedance of comparator	ZCMP	35000	-	-	kΩ	

7.13.3 Low-power comparator AC specifications

Table 24 Low-power comparator AC specifications

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SID91	Response time. Normal mode. 100 mV overdrive	TRESP1	-	-	100	ns	
SID258	Response time. Low power mode. 100 mV overdrive	TRESP2	-	-	1000	ns	
SID92	Response time. Ultra-low power mode. 100 mV overdrive.	TRESP3	-	-	20	µs	
SID92E	Time from enabling to operation	T_CMP_EN1	-	-	10	µs	Normal and low-power modes. Guaranteed by design.
SID92F	Time from enabling to operation	T_CMP_EN2	-	-	50	µs	Ultra low-power mode. Guaranteed by design.

7.13.4 CSG DC specifications

Table 25 CSG DC specifications

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SIDCSG	Reference voltage for DAC	DAC_REF	-	3.3	-	V	VDDA is used as reference for the DAC.
SIDCSG.1	Input common mode voltage for differential input	VCMR	0.2	-	3.43	V	
SIDCSG.2	Operating current on VDDA at 90 MHz	IVDDA	-	-	2.2	mA	Includes comparator. DAC on VDDA and all internal blocks. Only one instance of CSG
SIDCSG.3	Minimum overdrive voltage at 10 MHz	OD10M		-	15	mV	
SIDCSG.3A	Minimum overdrive voltage at 90 MHz	OD90M		-	50	mV	
SIDCSG.4	DAC integral non linearity	INL	-1	-	2	LSB	Referred to 10-bit DAC with full scale LSB at 3.3 V
SIDCSG.5	DAC differential non linearity	DNL	-1	-	1	LSB	Referred to 10-bit DAC with full scale LSB at 3.3 V

7.13.5 CSG AC specifications

Table 26 CSG AC specifications

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SIDCSG.7	Comparator input referred comparator noise	INPNOISE	-	-	400	uV	
SIDCSG.8	DAC settling within ±1 LSB for ≥ 256 LSB change	DACSET	-	-	33	ns	Up to 1023 LSB code change
SIDCSG.8A	DAC settling within ± 1 LSB for ≤ 255 LSB change	DACSETA	-	-	25	ns	LSB code change of 64 and above(Less than 64 and upto 4 LSB code change is guranteed by design)
SIDCSG.9	DAC observability error by the ADC (CSG accuracy and operation not affected)	DAC_OBSERR	-	-	16	LSB	LSB refers to the 10-bit DAC. Maximum error condition when | VIN-VDAC| = VDDA

(table continues...)

Table 26 (continued) CSG AC specifications

SIDCSG.9A	DAC observability error by the ADC @VDDA/2 (CSG accuracy and operation not affected)	DAC_OBSERRA	-	-	8	LSB	LSB refers to the 10-bit DAC. Maximum error condition when |VIN-VDAC| = VDDA/2
SIDCSG.9B	DAC observability error by the ADC @VDDA/4 (CSG accuracy and operation not affected)	DAC_OBSERRB	-	-	4	LSB	LSB refers to the 10-bit DAC. Maximum error condition when |VIN-VDAC| = VDDA/4

7.13.6 Internal reference specifications

Table 27 Internal reference specifications

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SID93R	Bandgap reference	VREFBG	1.188	1.2	1.212	V	

7.13.7 12-bit SAR ADC DC specifications

Table 28 12-bit SAR ADC DC specifications

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SIDADC	External reference	VAREF_EXT	-	3.3	-	V	For meeting the parameters of the ADC it is recommended to connect reference to VAREF
SIDADC.0	ADC resolution	RES	-	-	12	Bits	
SIDADC.1	Number of sample and hold stages - single ended	SH_S	-	-	16	-	
SIDADC.2	Gain error without calibration	GAINERR_NOCAL	-5	-	5	%	LSB referred to VAREF = 3.3 V
SIDADC.3	Gain error at gain = 1 after calibration	GAINERR_1	-0.1	-	0.1	%	LSB referred to VAREF = 3.3 V
SIDADC.3A	Gain error at gain = 3 after calibration	GAINERR_3	-0.2	-	0.2	%	LSB referred to VAREF = 3.3 V
SIDADC.3B	Gain error at gain = 6 after calibration	GAINERR_6	-0.4	-	0.4	%	LSB referred to VAREF = 3.3 V
SIDADC.3C	Gain error at gain = 12 after calibration	GAINERR_12	-0.6	-	0.6	%	LSB referred to VAREF = 3.3 V
SIDADC.4	Offset Error without calibration	OFFSETERR_NOCAL	-15	-	10	mV	
SIDADC.4A	Offset Error after calibration	OFFSETERR	-2	-	2	mV	

(table continues...)

Table 28 (continued) 12-bit SAR ADC DC specifications

SIDADC.5A	Total unadjusted error for gain = 1	TUE_G1	-4.5	-	4.5	LSB	Gain =1. LSB referred to VAREF = 3.3 V
SIDADC.5B	Total unadjusted error for gain = 3	TUE_G3	-9	-	9	LSB	Gain =3. LSB referred to VAREF = 3.3 V
SIDADC.5C	Total unadjusted error for gain = 6	TUE_G6	-18	-	18	LSB	Gain =6. LSB referred to VAREF = 3.3 V
SIDADC.5D	Total unadjusted error for gain = 12	TUE_G12	-36	-	36	LSB	Gain =12. LSB referred to VAREF = 3.3 V
SIDADC.6	Integral Non Linearity.	A_INL	-2	-	2	LSB	
SIDADC.7	Differential Non Linearity.	A_DNL	-1	-	2	LSB	
SIDADC.8	Current consumption	A_ISAR_1	-	-	13	mA	Current consumption on analog supply VDDA
SIDADC.9	Input voltage range	A_VINS	VSSS	-	VDDA	V	When VDDA > VAREF_EXT ADC result will saturate when VIN = VAREF_EXT

7.13.8 12-bit SAR ADC AC specifications

Table 29 12-bit SAR ADC AC specifications

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SIDADC.9A	Analog Input voltage transient tolerated	A_VINSTRAN	-	-	VDDA +1.5	V	Input current ≤ 3 mA. Valid for max VDDA = 3.3 V. Slew rate for VIN from VDDA to VDDA + 1.5 ≥ 7 us
SIDADC.10	ADC frequency	fADC	90	-	180	MHz	Operating voltage mode: OD. Max when VDDA ≥ 2.7 V. Min when VDDA < 2.7 V
SIDADC.12	RMS noise	A_RMS	-	-	1150	µVrms	1 sigma value

(table continues...)

Table 29 (continued) 12-bit SAR ADC AC specifications

SIDADC.13	Interchannel crosstalk with ≤ 6 samplers	CROSSTALK_5	-7	-	7	LSB	Inter Channel Crosstalk for VAREF = 3.3 V with ≤ 6 samplers ending sampling simultaneously. After crosstalk compensation by software routineMeasured with 10% FS and 90% FS DC input
SIDADC.13A	Interchannel crosstalk with ≤ 11 samplers	CROSSTALK_10	-9	-	9	LSB	Inter Channel Crosstalk for VAREF = 3.3 V with ≤ 11 samplers ending sampling simultaneously. After crosstalk compensation by software routineMeasured with 10% FS and 90% FS DC input
SIDADC.14	Sample rate for continuous conversion at VDDA>2.7V	A_SAMP_1	-	-	9	MSPS	VDDA 2.7 - 3.6 V (this includes minimum sampling time and conversion time). fADC max = 180 MHz
SIDADC.15	Sample rate for continuous conversion at VDDA<2.7V	A_SAMP_2	-	-	4.5	MSPS	VDDA 1.7 - 2.7 V (this includes minimum sampling time and conversion time). fADC max = 90 MHz
SIDADC.16	Signal-to-noise and distortion ratio (SINAD).	A_SINAD	65	-	-	dB	Fin = 10 kHz. Gain =1. VAREF = 3.3 V
SIDADC.17	Start up time after stable supply	T_STARTUP	-	-	1284	cycles	ADC clock frequency define the start up time

(table continues...)

Table 29 (continued) 12-bit SAR ADC AC specifications

SIDADC.18	Maximum calibration time	T_CAL	-	-	2160000	cycles	ADC clock frequency define the calibration time. Calibration is required only after power up. After start up calibration values will be loaded into the ADC calibration registers. Use can decide to skip the power up calibration. Calibration values are not retained when the MCU goes from active to deep sleep and hibernate mode.
SIDADC.19	Minimum sampling time for analog input through analog pad direct connection to S/H	T_SAMPLE	3	-	-	cycles	Referred to fADC
SIDADC.19B	Minimum sampling time for analog input through analog pad connected to S/H via AROUTE (AMUX)	T_SAMPLE_AROUTE	11	-	-	cycles	Referred to fADC
SIDADC.19C	Minimum sampling time for analog input through GPIO or ADFT connected to S/H via AROUTE (AMUX)	T_SAMPLE_GPIO	78	-	-	cycles	Referred to fADC
SIDADC20	Conversion time	T_CONV	-	-	16	cycles	Referred to fADC

7.13.9 AFE DC specifications

Table 30 AFE DC specifications

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SIDAFE_9	Start up time of the AFE	AFE_STARTUP_TIME	-	-	6	µs	
SIDAFE_12	DC gain of AFE	AFE_DC_GAIN	-	90	-	dB	
SIDAFE_14	Offset error	AFE_OFFSET_ERR	-	1	3	mV	
SIDAFE_15	Input range supported by by AFE	AFE_INP_RANGE	VSSA+0.1	-	VDDA-0.1	V	

(table continues...)

Table 30 (continued) AFE DC specifications

SIDAFE_16	Output range supported by AFE	AFE_OUT_RANGE	VSSA + 0.2	-	VDDA - 0.2	V	
SIDAFE_17	DC Load current (External)	AFE_ILOAD	-	-	500	µA	
SIDAFE_18	AFE consumption from VDDA in single ended mode with external load	AFE_IDDA	-	-	350	µA	With zero DC load current
SIDAFE_18A	AFE consumption from VDDA in single ended mode with internal load	AFE_IDDA1	-	-	500	µA	With zero DC load current
SIDAFE_18B	AFE consumption from VDDA in differential ended mode with internal load	AFE_IDDA2	-	-	780	µA	With zero DC load current

7.13.10 AFE AC specifications

Table 31 AFE AC specifications

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SIDAFE_19	Gain variation	AFE_GAIN_VAR	-	-	1	%	
SIDAFE_20	Flicker noise	AFE_FLKR_NOISE	-	.180	-	µV/ sqrt(Hz)	At 1 KHz
SIDAFE_21	Integrated output noise from 10 Hz to 1 GHz	AFE_INTG_NOISE	-	180	-	LSBrms	
SIDAFE_10	Unity gain bandwidth	AFE_UGBW	3.5	10	-	MHz	With external/ internal load
SIDAFE_22	Phase margin	AFE_PM	-	45	-	deg	With external/ internal load
SIDAFE_23	Total harmonic distortion	AFE_THD	60	70		dB	With external/ internal load

7.13.11 R2R DAC and buffer specifications

Table 32 R2R DAC and buffer specifications

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SIDR2R.1	DAC Resolution	Resolution	-	12	-	Bits	Resolution
SIDR2R.2	Gain error	GAINERR	-0.5	-	0.5	%	
SIDR2R.3	DNL of R2R DAC	R_DNL	-1	-	1	LSB	LSB referred to 12-bit with VDDA ≥ 2.7 V
SIDR2R.4	INL of R2R DAC	R_INL	-3	-	3	LSB	LSB referred to 12-bit with VDDA ≥ 2.7 V
SIDR2R.5	Full Scale Range of R2R DAC	R_FULLSCALE	1.71	-	VDDA	V	12-Bit performance guaranteed above VDDA ≥ 2.7 V
SIDR2R.6	DAC settling time for transition between minimum code to maximum or vice-versa	RDAC_SET	-	-	1	µs	DAC settling time in config 3 from code transition to and accuracy of ±1 LSB w.r.t its DC value with 50 pF load cap within 10 to 90% of dynamic range
SIDR2R.8	DC PSRR	R_PSRR	-	-	-80	dB	With VAREF_EXT
SIDR2R.9	DAC consumption from VDDA in 10 mA mode	R_IDDA	-	-	1	mA	VDDA ≥ 2.7 VCapacitive load of 100 pFLoad current = 10 mA

(table continues...)

Table 32 (continued) R2R DAC and buffer specifications

SIDR2R.10	DAC consumption from VDDA in 1 mA mode	R_IDDA_1	-	-	170	µA	VDDA ≥ 2.7 VCapacitive load of 10 pFLoad current = 1 mA
SIDR2R.11	DAC consumption from VDDA in 100 uA mode	R_IDDA_2	-	-	80	µA	VDDA ≥ 2.7 VCapacitive load of 10 pFLoad current = 100 µA
SIDR2R.12	Integrated noise for range of 100 Hz to 1 GHz	R_NOISE	-	-	0.18	µV/ sqrt(Hz)	VDDA ≥ 2.7 VGuaranteed by design
SIDR2R.14	DAC output offset	R_OFFSET	-2	-	2	mV	VDDA ≥ 2.7 V

7.13.12 HRPWM specifications

Table 33 HRPWM specifications

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SIDHRPWM.1	HRPWM Resolution	HR_RES	-	86.81	-	ps	Ensure that VDDA > 2.7 V and clock to TCPWM counter is 180 MHz when HRPWM is enabled. No clock prescalar should be used in PERI or TCPPWM.
SIDHRPWM.2	HRPWM is monotonic	MONOTONIC	-	Yes	-		

7.14 Digital peripherals

7.14.1 TCPWM specifications

Table 34 TCPWM specifications

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SID.TCPWM.2B	Block current consumption at 100 MHz	ITCPWM4	-	-	2800	µA	All counters active in PWM_DT mode with 50% duty cycle
SID.TCPWM.2C	Block current consumption at 180 MHz	ITCPWM4A	-	-	4600	µA	All counters active in PWM_DT mode with HRPWM mode enabled and with 50% duty cycle

(table continues...)

Table 34 (continued) TCPWM specifications

SID.TCPWM.3	Operating frequency (Fc)	TCPWMFREQ	-	-	180	MHz	Fc max = 180 MHz
SID.TCPWM.4	Input Trigger Pulse Width for all Trigger Events	TPWMENEXT	2/Fc	-	-	ns	Trigger Events can be Stop / Start / Reload / Count / Capture / Kill depending on which mode of operation is selected.
SID.TCPWM.5	Output Trigger Pulse widths	TPWMEXT	1.5/Fc	-	-	ns	Minimum possible width of Overflow / Underflow / CC (Counter equals Compare value) trigger outputs
SID.TCPWM.5A	Resolution of Counter	TCRES	1/Fc	-	-	ns	Minimum time between successive counts at VDDD = 3 V
SID.TCPWM.5B	PWM Resolution	PWMRES	1/Fc	-	-	ns	Minimum pulse width of PWM Output at VDDD = 3 V

7.14.2 I3C specifications

Table 35 I3C specifications

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SID800	HDR-DDR data rate in OD/LP mode	I3CF1	-	-	25	Mbps	OD/LP Mode
SID801	HDR-DDR data rate in MF mode	I3CF2	-	-	12	Mbps	MF Mode
SID802	HDR-DDR data rate in ULP mode	I3CF3	-	-	6	Mbps	ULP Mode
SID803	Clock in to Data out for target in OD mode	TSCO_OD	-	-	23	ns	
SID804	Clock in to Data out for target in LP mode	TSCO_LP	-	-	25	ns	
SID805	Clock in to Data out for target in MF mode	TSCO_MF	-	-	28	ns	MF Mode
SID806	Clock in to Data out for target in ULP mode	TSCO_ULP	-	-	37	ns	ULP Mode

7.14.3 SMBUS specifications

Table 36 SMBUS specifications

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SID_SMBUS1	Detect low clock timeout at 100 KHz	T_TIMEOUT1	25	-	35	ms	
SID_SMBUS2	Detect low clock timeout at 400 KHz	T_TIMEOUT2	25	-	35	ms	
SID_SMBUS3	Detect low clock timeout at 1 MHz	T_TIMEOUT3	25	-	35	ms	

7.14.4 Fixed I2C DC specifications

Table 37 Fixed I2C DC specifications

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SID149	Block current consumption at 100 KHz	II2C1	-	-	30	µA	Guaranteed by design
SID150	Block current consumption at 400 KHz	II2C2	-	-	80	µA	Guaranteed by design
SID151	Block current consumption at 1 Mbps	II2C3	-	-	180	µA	Guaranteed by design
SID152	I2C enabled in Deep Sleep mode	II2C4	-	-	1.7	µA	At 60°CGuaranteed by design

7.14.5 Fixed I2C AC specifications

Table 38 Fixed I2C AC specifications

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SID153	Bit Rate	FI2C1	-	-	1	Mbps	

7.14.6 Fixed UART DC specifications

Table 39 Fixed UART DC specifications

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SID160	Block current consumption at 100 Kbits/sec	IUART1	-	-	30	µA	Guaranteed by design
SID161	Block current consumption at 1000 Kbits/sec	IUART2	-	-	180	µA	Guaranteed by design

7.14.7 Fixed UART AC specifications

Table 40 Fixed UART AC specifications

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SID162A	Bit Rate	FUART1	-	-	3	Mbps	At ULP mode
SID162B	Bit Rate	FUART2	-	-	8	Mbps	At LP mode

7.14.8 Fixed SPI DC specifications

Table 41 Fixed SPI DC specifications

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SID163	Block current consumption at 1 Mbits/sec	ISPI1	-	-	220	µA	Guaranteed by design
SID164	Block current consumption at 4 Mbits/sec	ISPI2	-	-	340	µA	Guaranteed by design
SID165	Block current consumption at 8 Mbits/sec	ISPI3	-	-	360	µA	Guaranteed by design
SID165A	Block current consumption at 25 Mbits/sec	ISPI4	-	-	800	µA	Guaranteed by design

7.14.9 Fixed SPI AC specifications for LP/OD/MF/ULP modes unless noted otherwise

Table 42 Fixed SPI AC specifications for LP/OD/MF/ULP modes unless noted otherwise

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SID166	SPI operating frequency master and externally clocked slave mode	FSPI_EXT	-	-	25	MHz	For LP/OD mode
SID166U	SPI operating frequency master and externally clocked slave mode	FSPI_EXT_UL	-	-	6.25	MHz	For ULP mode
SID166A	SPI operating frequency master and externally clocked slave in high speed mode	FSPI_EXT_HS	37.5	-	45	MHz	Min. is for LP mode. max. is for OD mode
SID166AU	SPI operating frequency master and externally clocked slave in high speed mode	FSPI_EXT_HS_UL	12.5	-	17.5	MHz	Min. is for ULP mode. max. is for MF Mode
SID166B	SPI operating frequency master mode	FSPI	-	-	25	MHz	LP and OD mode. FSCB = 100 MHz
SID166BU	SPI operating frequency master mode	FSPI_UL	-	-	6.25	MHz	MF and ULP mode. FSCB = 25 MHz
SID166_OD	SPI operating frequency master in high speed mode	FSPI_HS_OD	-	-	45	MHz	OD mode. FSCB = 180 MHz
SID166BHS	SPI operating frequency master in high speed mode	FSPI_HS	-	-	37.5	MHz	LP mode. FSCB = 150 MHz
SID166BHS_MF	SPI operating frequency master in high speed mode	FSPI_HS_MF	-	-	17.5	MHz	MF mode FSCB = 70 MHz

(table continues...)

Table 42 (continued) Fixed SPI AC specifications for LP/OD/MF/ULP modes unless noted otherwise

SID166BHS_UL	SPI operating frequency master in high speed mode	FSPI_HS_UL	-	-	12.5	MHz	ULP mode. FSCB = 50 MHz
SID166C	SPI slave Internally clocked	FSPI_IC	-	-	4	MHz	MF and ULP mode. FSCB = 25 MHz
SID166C_OD	SPI slave Internally clocked in LP and OD	FSPI_IC_OD	-	-	12.5	MHz	LP and OD mode. FSCB = 100 MHz
SID166C_HS	SPI slave Internally clocked in in high speed mode in MF and ULP	FSPI_IC_HS	7	-	9	MHz	Min at ULP mode FSCB = 50 MHz and max. at MF mode FSCB=70 MHz
SID166C_HS_OD	SPI slave Internally clocked in in high speed Mode in LP and OD	FSPI_IC_HS_OD	18	-	22	MHz	Min. at LP mode. FSCB = 150 MHz and max. at OD mode. FSCB = 180 MHz

7.14.10 Fixed SPI Master mode AC specifications for LP/OD/MF/ULP modes unless noted otherwise

Table 43 Fixed SPI Master mode AC specifications for LP/OD/MF/ULP modes unless noted otherwise

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SID167_INT	SCB clock period	TSCB	-	-	1/ FSCB	ns	FSCB value depends on choice of standard or HS mode as well different power modes (OD/LP/MF/ ULP) as listed below
SID167_INT1	SPI clock period	TSPI	-	-	1/ FSPI	ns	FSPI value depends upon choice between SPI standard or high speed mode and power mode (OD/LP/MF/ULP) as listed below
SID167	MOSI valid after SCK driving edge in OD/LP mode	TDMO	-	-	10	ns	LP/OD mode
SID167UL	MOSI valid after SCK driving edge in MF/ULP mode	TDMO_UL	-	-	40	ns	ULP and MF mode
SID167HS	MOSI valid after SCK driving edge in HS mode in OD/LP mode	TDMO_HS	5	-	7	ns	Max Is OD mode and min. is LP Mode

(table continues...)

Table 43 (continued) Fixed SPI Master mode AC specifications for LP/OD/MF/ULP modes unless noted otherwise

SID167HS_UL	MOSI valid after SCK driving edge in HS mode in MF/ULP mode	TDMO_HS_UL	14	-	20	ns	Max Is ULP mode and min is MF Mode
SID168	MISO valid before SCK capturing edge in OD/LP mode	TDSI	20	-	-	ns	LP/OD Full clock. Late MISO sampling
SID168_ULP	MISO valid before SCK capturing edge in MF/ULP mode	TDSI_ULP	105	-	-	ns	ULP Mode for 50 MHz operation
SID168HS	MISO valid before SCK capturing edge for HS mode in LP mode	TDSI_HS	15	-	-	ns	
SID168HS_OD	MISO Valid before SClock capturing edge for OD mode	TDSI_HS_OD	10	-	-	ns	OD Mode for 50 MHz operation at VDDIO(max)
SID168HS_ULP	MOSI valid after SCK driving edge in HS mode in MF/ULP mode	TDMO_HS_UL	22	-	-	ns	ULP Mode for 50 MHz operation
SID169	MOSI data hold time for OD/LP mode	THMO	0	-	-	ns	Referred to dlave capturing edge in LP and OD mode
SID169_UL	MOSI data hold time for MF/ULP mode	THMO_UL	0	-	-	ns	Referred to slave capturing edge in ULP and MF mode
SID169HS	MOSI data hold time in HS mode in OD/LP mode	THMO_HS	0	-	-	ns	Referred to slave capturing edge for HS SPI in LP and OD mode
SID169HS_UL	MOSI data hold time in HS mode in MF/ULP mode	THMO_HS_UL	0	-	-	ns	Referred to slave capturing edge for HS SPI in ULP and MF mode
SID169A	SSEL valid to first SCK valid edge	TSSELMSCK1	0.25*TSCB	-	-	ns	Referred to Master clock edge for all modes
SID169B	SSEL Hold after last SCK valid edge	TSSELMCK2	0.25*TSPI	-	-	ns	Referred to Master clock edge for all modes

7.14.11 Fixed SPI Slave mode AC specifications for LP/OD/MF/ULP modes unless noted otherwise

Table 44 Fixed SPI Slave mode AC specifications for LP/OD/MF/ULP modes unless noted otherwise

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SID170	MOSI valid before SCK Capturing edge in OD/LP mode	TDMI	5	-	-	ns	LP/OD mode
SID170_UL	MOSI valid before SCK Capturing edge in MF/ULP mode	TDMI_UL	24	-	-	ns	MF and ULP mode
SID170_HS	MOSI valid before SCK Capturing edge in OD/LP mode	TDMI_HS	4	-	-	ns	LP/OD Mode for 50 MHz operation
SID170_HS_UL	MOSI valid before SCK Capturing edge in MF/ULP mode	TDMI_HS_UL	14	-	-	ns	ULP/MF Mode for 50 MHz operation
SID171A	MISO valid after SCK driving edge in Ext. Clk. mode	TDSO_EXT	-	-	20	ns	LP/OD mode
SID171A_UL	MISO valid after SCK driving edge in Ext. Clk. mode	TDSO_EXT_UL	-	-	35	ns	MF and ULP mode
SID171A_HS	MISO valid after SCK driving edge in Ext. Clk. mode	TDSO_EXT_HS	-	-	16	ns	LP for 50 MHz operation
SID171A_HS_OD	MISO valid after SCK driving edge in Ext. Clk. mode	TDSO_EXT_HS_OD	-	-	10	ns	OD Mode for 50 MHz operation with 10 pF load at VDDIO (max)
SID171A_HS_UL	MISO valid after SCK driving edge in Ext. Clk. mode	TDSO_EXT_HS_UL	-	-	25	ns	ULP/MF Mode for 50 MHz operation
SID171	MISO valid after SCK driving edge internally clocked	TDSO	-	-	TDSO_EXT + 2*TSCB	ns	TSCB is Serial Comm Block clock period
SID171B	MISO valid after SCK driving edge internally clocked with median filter enabled	TDSO_M	-	-	TDSO_EXT + 3*TSCB	ns	TSCB is Serial Comm Block clock period
SID172	MOSI and MISO data hold time	THSO	5	-	-	ns	ULP/MF/LP/OD modes. Both for standard and HS SPI
SID172A	SSEL valid to first SCK valid edge	TSSELSCK1	4*TSCB	-	-	ns	SPI Slave internally clocked mode
SID172B	SSEL Hold after Last SCK valid edge	TSSELSCK2	4*TSCB	-	-	ns	SPI Slave internally clocked mode
SID172C	MISO valid after SSEL falling edge in OD/LP mode	TVSS_EXT	-	-	20	ns	LP/OD mode
SID172C_ULP	MISO valid after SSEL falling edge in MF/ULP Modes	TVSS_EXT_ULP	-	-	35	ns	MF and ULP mode

(table continues...)

Table 44 (continued) Fixed SPI Slave mode AC specifications for LP/OD/MF/ULP modes unless noted otherwise

SID172C_HS	MISO valid after SSEL falling edge for HS mode in LP Mode	TVSS_EXT_HS	-	-	16	ns	High speed SPI. LP mode
SID172C_HS_OD	MISO valid after SSEL falling edge for HS mode in OD Mode	TVSS_EXT_HS_OD	-	-	16	ns	High Speed SPI. OD mode
SID172C_HS_UL	MISO valid after SSEL falling edge for HS mode in MF/ULP Modes	TVSS_EXT_HS_UL	-	25	27	ns	High speed SPI. Typical value for MF mode and max value at ULP mode

7.15 Memory

7.15.1 Flash DC specifications

Table 45 Flash DC Specifications

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SID173	Erase and program voltage	VPE	1.71	-	3.63	V	Erase and program not supported at ULP levels
SID173A	Erase and program current	IPE	-	-	6	mA	Guaranteed by design

7.15.2 Flash AC specifications

Table 46 Flash AC specifications

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SID174	Row(Block) write time (erase & program)	TROWWRITE	-	-	16	ms	Row (Block) = 512 Bytes
SID175	Row erase time	TROWERASE	-	-	11	ms	
SID176	Row program time after erase	TROWPROGRAM	-	-	5	ms	
SID180	Total device program time	TDEVPROG	-	-	5.2	ms	
SID181	Flash endurance	FEND	100000	-	-	cycles	
SID182	Flash retention. TA ≤ 25°C. 100K P/E cycles	FRET1	10	-	-	years	
SID182A	Flash retention. TA ≤ 85°C. 10K P/E cycles	FRET2	10	-	-	years	
SID182B	Flash retention. TA ≤ 55°C. 20K P/E cycles	FRET3	20	-	-	years	
SID256	Number of wait states at 180 MHz	TWS180	-	-	9	-	OD mode
SID256A	Number of wait states at 150 MHz	TWS150	-	-	8	-	LP mode
SID256B	Number of wait states at 70 MHz	TWS70	-	-	5	-	MF mode

(table continues...)

Table 46 (continued) Flash AC specifications

SID256C	Number of wait states at 50 MHz	TWS50	-	-	4	-	ULP mode

7.16 System resources

7.16.1 POR

7.16.1.1 POR with Brown-out DC specifications

Table 47 POR with Brown-out DC specifications

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SID190	BOD trip voltage in Active and Sleep modes	VFALLPPOR	1.54	-	-	V	BOD Reset guaranteed for levels below 1.54 V
SID192	BOD trip voltage in Deep Sleep	VFALLDPSLP	1.54	-	-	V	
SID192A	Maximum power supply ramp rate (any supply)	VDDRAMP	-	-	0.1	V/µs	Active Mode

7.16.1.2 POR with Brown-out AC specifications

Table 48 POR with Brown-out AC specifications

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SID194A	Maximum power supply ramp rate (any supply) in Deep Sleep	VDDRAMP_DS	-	-	0.10	V/µs	BOD operation guaranteed

7.16.2 Voltage monitors

7.16.2.1 Voltage monitors DC specifications

Table 49 Voltage monitors DC specifications

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SID196	Voltage monitors DC	VHVDI2	1.57	1.63	1.68	V	
SID197	Voltage monitors DC	VHVDI3	1.76	1.83	1.89	V	
SID198	Voltage monitors DC	VHVDI4	1.95	2.03	2.1	V	
SID199	Voltage monitors DC	VHVDI5	2.05	2.13	2.2	V	
SID200	Voltage monitors DC	VHVDI6	2.15	2.23	2.3	V	
SID201	Voltage monitors DC	VHVDI7	2.24	2.33	2.41	V	
SID202	Voltage monitors DC	VHVDI8	2.34	2.43	2.51	V	
SID203	Voltage monitors DC	VHVDI9	2.44	2.53	2.61	V	
SID204	Voltage monitors DC	VHVDI10	2.53	2.63	2.72	V	
SID205	Voltage monitors DC	VHVDI11	2.63	2.73	2.82	V	

(table continues...)

Table 49 (continued) Voltage monitors DC specifications

SID206	Voltage monitors DC	VHVDI12	2.73	2.83	2.92	V	
SID207	Voltage monitors DC	VHVDI13	2.82	2.93	3.03	V	
SID208	Voltage monitors DC	VHVDI14	2.92	3.03	3.13	V	
SID209	Voltage monitors DC	VHVDI15	3.02	3.13	3.23	V	
SID211	Block current	LVI_IDD	-	5	15	uA	

7.16.3 SWD and Trace

7.16.3.1 SWD and Trace interface

Table 50 SWD and Trace interface

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SID214	Single wire debug clock in OD mode	F_SWDCLK2	-	-	25	MHz	OD mode
SID214LP	Single wire debug clock in LP mode	F_SWDCLK2LP	-	-	20	MHz	LP mode
SID214L	Single wire debug clock in MF/ULP mode	F_SWDCLK2L	-	-	12	MHz	ULP and MF mode
SID215	Single wire debug input setup time	T_SWDI_SETUP	0.25/ fSWDCLK	-	-	ns	
SID216	Single wire debug input hold time	T_SWDI_HOLD	0.25/ fSWDCLK	-	-	ns	
SID217	Single wire debug output valid time	T_SWDO_VALID	-	-	0.5/ fSWDCLK	ns	
SID217A	Single wire debug output hold time	T_SWDO_HOLD	1	-	-	ns	
SID214T	With Trace Data setup/hold times of 2/1 ns in OD mode	F_TRCLK_LP1	-	-	80	MHz	OD Modeload capacitance = 15 pF
SID215T	With Trace Data setup/hold times of 2/1 ns in LP mode	F_TRCLK_LP2	-	-	75	MHz	LP Modeload capacitance = 15 pF
SID216T	With Trace Data setup/hold times of 3/2 ns in MF mode	F_TRCLK_LP3	-	-	35	MHz	MF = 1.0 V MF Modeload capacitance = 15 pF
SID217T	With Trace Data setup/hold times of 3/2 ns in ULP mode	F_TRCLK_ULP	-	-	25	MHz	ULP = 0.9 V ULP Modeload capacitance = 15 pF

7.16.4 Internal oscillator - crystal oscillator - external clock specifications

7.16.4.1 IMO DC specifications

Table 51 IMO DC specifications

Spec ID	Parameter	Symbol	Values			Unit	Note or condition
			Min.	Typ.	Max.		
SID218	IMO operating current at 8 MHz	*IIMO1*	-	9	15	µA	Guaranteed by design

7.16.4.2 IMO AC specifications

Table 52 IMO AC specifications

Spec ID	Parameter	Symbol	Values			Unit	Note or condition
			Min.	Typ.	Max.		
SID223	Frequency variation centered on 8 MHz	*FIMOTOL1*	7.84	8	8.16	MHz	*VDDD* = 1.71 V to 3.63 V $T_A \leq 105$ °C
SID227	Cycle-to-cycle and period jitter	*TJITRIMO*	-	250	-	ps	*VDDD* = 1.71 V to 3.63 V $T_A \leq 105$ °C

7.16.4.3 IHO DC specifications

Table 53 IHO DC specifications

Spec ID	Parameter	Symbol	Values			Unit	Note or condition
			Min.	Typ.	Max.		
SID218A	IHO operating current at 48 MHz	*IIHO1*	-	80	100	µA	Guaranteed by design

7.16.4.4 IHO AC specifications

Table 54 IHO AC specifications

Spec ID	Parameter	Symbol	Values			Unit	Note or condition
			Min.	Typ.	Max.		
SID223A	Frequency variation centered on 48 MHz	*FIHOTOL1*	47.52	48	48.48	MHz	*VDDD* = 1.71 V to 3.63 V $T_A \leq 105$ °C
SID227A	Cycle-to-cycle and period jitter	*TJITRIHO*	-	60	-	ps	*VDDD* = 1.71 V to 3.63 V $T_A \leq 105$ °C

7.16.4.5 ILO DC specifications

Table 55 ILO DC specifications

Spec ID	Parameter	Symbol	Values			Unit	Note or condition
			Min.	Typ.	Max.		
SID231	ILO operating current at 32 KHz	*IILO2*	-	0.3	0.7	µA	Guaranteed by Design

7.16.4.6 ILO AC specifications

Table 56 ILO AC specifications

Spec ID	Parameter	Symbol	Values			Unit	Note or condition
			Min.	Typ.	Max.		
SID234	ILO start-up time	*TSTARTILO1*	-	-	7	µs	Startup time to 95% of final frequency
SID236	ILO duty cycle	*TLIODUTY*	45	50	55	%	
SID237	32 KHz trimmed frequency	*FILOTRIM1*	28.8	32	35.2	kHz	+/-10% variation

7.16.4.7 Frequency locked loop (FLL) specifications

Table 57 Frequency locked loop (FLL) specifications

Spec ID	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note or condition
SID450	Input frequency range.	FLL_RANGE	25	-	100	MHz	
SID451	Output frequency range	FLL_OUT_DIV2_1	24	-	100	MHz	Output range of FLL divided-by-2 output VCCD = 1.2 V/1.1 V
SID451A	Output frequency range	FLL_OUT_DIV2_2	24	-	50	MHz	Output range of FLL divided-by-2 output VCCD = 0.9 V
SID452	Divided-by-2 output. High or Low	FLL_DUTY_DIV2	47	-	53	%	Guaranteed by design
SID454	Time from stable input clock to 1% of final value on deep sleep wakeup	FLL_WAKEUP	-	-	7.5	µs	With IMO input for < 10°C change in temperature while in Deep Sleep and Fout ≥ 50 MHz
SID455	Period jitter (1 sigma) at 100 MHz	FLL_JITTER	50	-	35	ps	Min value is at 48 MHz. Guaranteed by design
SID456	Overall current	FLL_CURRENT	-	-	3.6	µA/MHz	FLL_Out = 100 MHz with VCCD = 1.1 V

7.16.4.8 MHz ECO DC specifications

Table 58 MHz ECO DC specifications

Spec ID	Parameter	Symbol	Values			Unit	Note or condition
			Min.	Typ.	Max.		
SID316	Block operating current with Cload up to 18 pF	*Idd_MHz*	-	800	2200	µA	Max at 36 MHz. Typ at 16 MHz.

7.16.4.9 MHz ECO AC specifications

Table 59 MHz ECO AC specifications

Spec ID	Parameter	Symbol	Values			Unit	Note or condition
			Min.	Typ.	Max.		
SID317	Crystal frequency range	*F_MHz*	4	-	36	MHz	

7.16.4.10 External clock specifications

Table 60 External clock specifications

Spec ID	Parameter	Symbol	Values			Unit	Note or condition
			Min.	Typ.	Max.		
SID_EXT	External clock max input frequency in OD/LP mode	*FEXT*	-	-	80	MHz	OD and LP mode. Duty cycle between 45% and 55% and max rise/fall time of 20% period
SID_EXT1	External clock max input frequency in MF mode	*FEXT_MF*	-	-	50	MHz	MF mode. Duty cycle between 45% and 55% and max rise/fall time of 20% period
SID_EXT2	External clock max input frequency in ULP mode	*FEXT_ULP*	-	-	40	MHz	ULP mode. Duty cycle between 45% and 55% and max rise/fall time of 20% period

7.16.4.11 kHz WCO DC specifications

Table 61 kHz WCO DC specifications

Spec ID	Parameter	Symbol	Values			Unit	Note or condition
			Min.	Typ.	Max.		
SID318	Block operating current with 32 kHz crystal	*Idd_kHz*	-	0.38	1	µA	
SID321E	Equivalent series resistance	*ESR32K*	-	80	-	kΩ	
SID322E	Drive level	*PD32K*	-	-	.001	mW	

7.16.4.12 kHz WCO AC specifications

Table 62 kHz WCO AC specifications

Spec ID	Parameter	Symbol	Values		Unit	Note or condition
			Min.	Typ.	Max.	
SID319	32 KHz trimmed frequency	*F_kHz*	-	32.768	-	kHz	
SID320K	Startup time	*Ton_kHz*	-	-	1000	ms	
SID320E	Frequency tolerance	*FTOL32K*	-	50	250	ppm	May be calibrated to sub-10 ppm levels

7.16.4.13 DPLL specifications

Table 63 DPLL specifications

Spec ID	Parameter	Symbol	Values			Unit	Note or condition
			Min.	Typ.	Max.		
SIPPLL.0	Time to achieve PLL lock at 4 MHz reference	*PLL_LOCK_4M*	-	-	20	µs	
SIPPLL.1	Time to achieve PLL lock at 8 MHz reference	*PLL_LOCK_8M*	-	-	20	µs	
SIPPLL.2	Output frequency from PLL block	*PLL_Out*	-	160	180	MHz	
SIPPLL.3	PLL current	*PLL_IDD*	-	800	1200	uA	For PLL_OUT = 180 MHz. Guaranteed by design
SIPPLL.4	Period jitter	*PLL_PJTR_100*	-200	-	200	ps	For PLL_OUT = 100 MHz. Guaranteed by design
SIPPLL.4A	Period jitter	*PLL_PJTR_180*	-100	-	100	ps	For PLL_OUT = 180 MHz. Guaranteed by design
SIPPLL.7	Duty cycle	*PLL_DC*	45	-	55	%	For PLL_OUT = Fdco/N . N >1 and integer

7.17 JTAG Boundary Scan specifications

7.17.1 JTAG Parameters for OD and LP modes operations

Table 64 JTAG Parameters for OD and LP modes operations

Spec ID	Parameter	Symbol	Values			Unit	Note or condition
			Min.	Typ.	Max.		
SID460	TCK low minimum	*TCKLOWLP*	33	-	-	ns	
SID461	TCK high	*TCKHIGHLP*	11	-	-	ns	
SID461A	Clock period	*TCK_PERIODLP*	-	44	-	ns	30 pF Load
SID462	TDO clock-to-out (max) from falling TCK	*TCK_TDOLP*	-	-	22	ns	
SID463	TDI/TMS setup time before rising TCK	*TSU_TCKLP*	12	-	-	ns	
SID464	TDI/TMS hold time after rising TCK	*TCk_THDLP*	10	-	-	ns	
SID465	TCK to TDO data valid (High-Z to active)	*TCK_TDOVLP*	-	-	22	ns	
SID466	TCK to TDO data valid (active to High-Z)	*TCK_TDOZLP*	-	-	22	ns	
SID467	JTAG TDO hold time	*JTAG_TDO_HOLDLP*	5	-	-	ns	
SID467A	JTAG input transition time	*JTAG_INPUT_TRANSITION_TIMELP*	-	-	5	ns	

8 Ordering information

Table 65 lists the PSC3M/P6 device part numbers and features. All devices include Arm® Cortex®-M33 with 180 MHz CPU speed, 2 ch CAN FD, 8 ch 32-bit timer with high-resolution PWM support, 16 ch 16-bit timer, 12-bit 9 Msps SAR ADC, 2x 12-bit DAC, 4x AFE, Smart I/O, 6x SCB (UART/I2C/SPI), 1x I3C, SVGS, CryptoLite and AES.

Table 65 Ordering information

Product	Flash in KB	SRAM in KB	SAR ADC ch	CORDIC accelerator	MOTIF	3P3Z	CSG	USB FS	PSA capable	GPIO	Package	Silicon ID
PSC3M6GES3AHQ1	512	128	24	Y	2	Y	9	1	L3	68	E-LQFP-100	0xF1001124
PSC3P6GES3AHQ1	512	128	24	N	N	Y	9	0	L3	70	E-LQFP-100	0xF1011124
PSC3M6FDS2AHQ1	256	64	24	Y	2	N	6	1	L2	68	E-LQFP-100	0xF1021124
PSC3P6FDS2AHQ1	256	64	24	N	N	Y	9	0	L2	70	E-LQFP-100	0xF1031124
PSC3M6GES3AFQ1	512	128	24	Y	2	Y	9	0	L3	54	E-LQFP-80	0xF1041124
PSC3P6GES3AFQ1	512	128	24	N	N	Y	9	0	L3	54	E-LQFP-80	0xF1051124
PSC3M6FDS2AFQ1	256	64	24	Y	2	N	6	0	L2	54	E-LQFP-80	0xF1061124
PSC3P6FDS2AFQ1	256	64	24	N	N	Y	9	0	L2	54	E-LQFP-80	0xF1071124
PSC3M6GES3ACQ1	512	128	19	Y	2	Y	9	0	L3	39	E-LQFP-64	0xF1081124
PSC3P6GES3ACQ1	512	128	19	N	N	Y	9	0	L3	39	E-LQFP-64	0xF1091124
PSC3M6FDS2ACQ1	256	64	19	Y	2	N	6	0	L2	39	E-LQFP-64	0xF10A1124
PSC3P6FDS2ACQ1	256	64	19	N	N	Y	9	0	L2	39	E-LQFP-64	0xF10B1124

8.1 Part number nomenclature

PSC3M/P6 MPN decoder:

PS C3 A B CC DD E FF G H II J K

Field	Description	Values	Meaning
PS	Brand	PS	Brand
C3	Family	C3	Family
A	Series	P	Power control
		M	Motor control
B	Sub-series	Entry Line	1-3
		Main Line	4-6
		Performance Line	7-9
CC	Memory (Flash/SRAM)	A	8 KB
		B	16 KB

Field	Description	Values	Meaning
		C	32 KB
		D	64 KB
		E	128 KB
		F	256 KB
		G	512KB
		H	768 KB
		J	1 MB
		K	2 MB
		L	3 MB
		M	4 MB
		N	6 MB
		O	7 MB
		P	8 MB
DD	Security	S2	PSA L2
		S3	PSA L3
E	Special attributes	D	Dual Core
		P	Programmable Power Control Sub-System
FF	Package	AB	EQFP-48 (0.5 mm)
		AC	EQFP-64 (0.5 mm)
		AF	EQFP-80 (0.5 mm)
		AH	QFP-100 (0.5 mm)
		AI	QFP-128 (0.5 mm)
		AE	QFP-144 (0.5 mm)
		LB	VQFN-24 (0.5 mm)
		LC	VQFN-32 (0.5 mm)
		LE	VQFN-40 (0.4 mm)
		LF	VQFN-48 (0.35 mm)
		LG	VQFN-48 (0.4 mm)
		LH	VQFN-64 (0.4 mm)
G	Temperature	C	Consumer (0°C to +70°C)
		I	Industrial (–40°C to +85°C)
		Q	Extended range (–40°C to +105°C)
H	Maximum core frequency	1	100 - 199 MHz
		2	200 - 299 MHz

Field	Description	Values	Meaning
II	Sample (Optional)	ES	Engineering Sample
J	Revision	-	Base
		A	Die revision
K	Packing (Optional)	T	Tape & Reel
		-	Tray

9 Package information

The PSC3M/P6 devices are offered in E-LQFP-64, E-LQFP-80 and E-LQFP-100 packages.

For pinout details, see Pins.

Table 66 Package dimensions

Spec ID#	Package	Description	Package Dwg #
PKG_1	E-LQFP-100	E-LQFP-100 14.0 mm x 14.0 mm x 1.6 mm height with 0.5 mm pitch, 6.5 x 6.5 mm EPAD	002-40570 Rev. *B
PKG_2	E-LQFP-80	E-LQFP-80, 12.0 mm x 12.0 mm x 1.6 mm height with 0.5 mm pitch, 4.6 x 4.6 mm EPAD	002-38596 Rev. *B
PKG_3	E-LQFP-64	E-LQFP-64, 10.0 mm x 10.0 mm x 1.6 mm height with 0.5 mm pitch, 4.0 x 4.0 mm EPAD	002-42581 Rev. **

Table 67 Package characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature	-	-40	25	115[1)]	°C
T_J	Operating junction temperature, all packages	-	-40	-	125	°C
T_{JA}	Package θ_{JA} (E-LQFP-100)	-	-	17.7	-	°C/watt
T_{JB}	Package θ_{JB} (E-LQFP-100)	-	-	9.9	-	°C/watt
T_{JC}	Package θ_{JC} (E-LQFP-100)	-	-	5.6	-	°C/watt
T_{JA}	Package θ_{JA} (E-LQFP-80)	-	-	18.8	-	°C/watt
T_{JB}	Package θ_{JB} (E-LQFP-80)	-	-	7.0	-	°C/watt
T_{JC}	Package θ_{JC} (E-LQFP-80)	-	-	5.6	-	°C/watt
T_{JA}	Package θ_{JA} (E-LQFP-64)	-	-	19.4	-	°C/watt
T_{JB}	Package θ_{JB} (E-LQFP-64)	-	-	5.9	-	°C/watt
T_{JC}	Package θ_{JC} (E-LQFP-64)	-	-	5.7	-	°C/watt

1) T_A can be extended to this range as long as T_J does not exceed the device T_{Jmax}.

***Notes**:*

1. *Thermal resistance between the chip and ambient (θ_{JA}) as per JESD51-2A & JESD51-7.*
2. *Thermal resistance between the chip and the printed circuit board (θ_{JB}) as per JESD51-8 & JESD51-7.*
3. *Thermal resistance between the chip and the package bottom surface by isothermal heat extraction method (θ_{JC}).*
4. *The end-application PCB design and operational profile may differ from the conditions described above. The user shall estimate the maximum power without exceeding the maximum junction temperature (T_J) of 125°C, based on the end-application PCB design and operational profile.*

Thermal calculations

The maximum junction temperature of the chip can be calculated using the following equation:
T_J max = T_A max + (P_D max × T_{JA})
where:

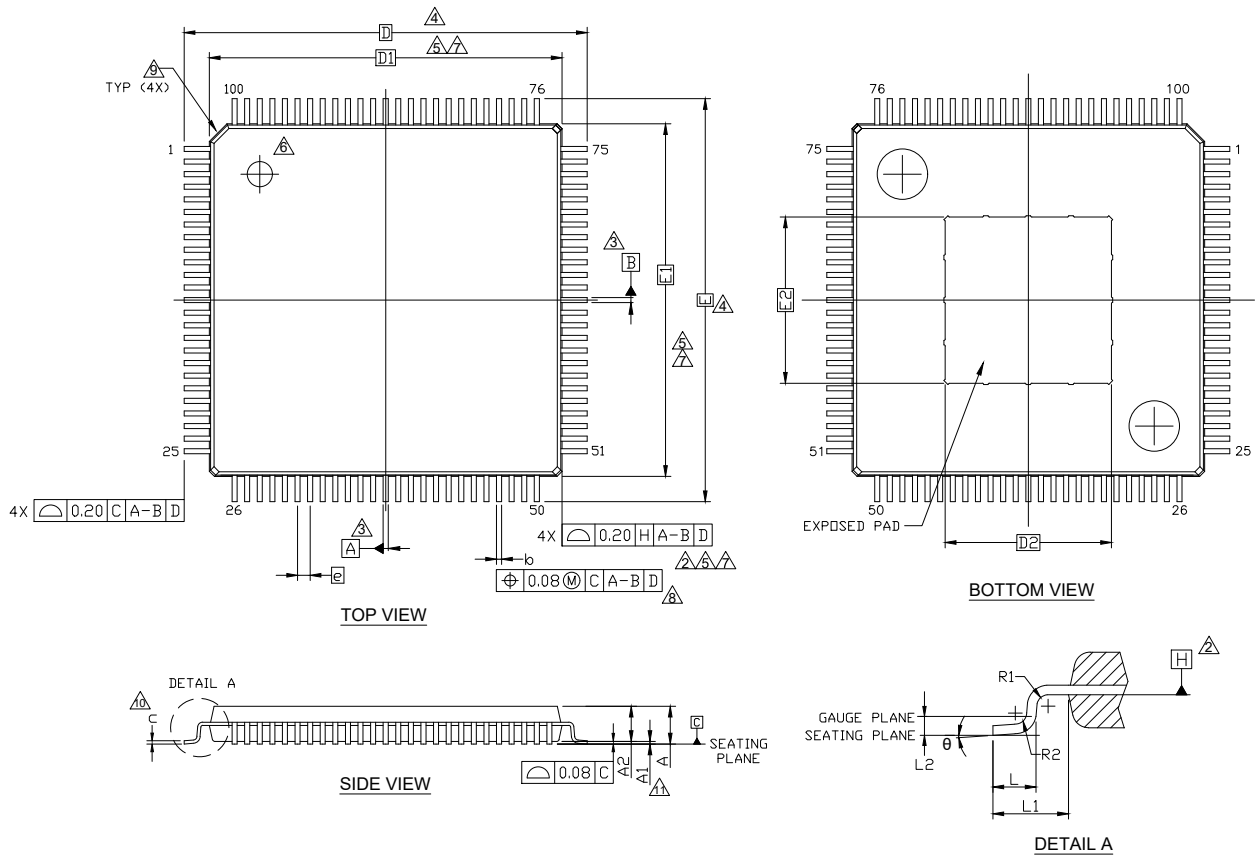
- T_J max is the maximum junction temperature in °C
- T_A max is the maximum ambient temperature in °C
- P_D max is the maximum power dissipation in the chip in watts
- T_{JA} is the package junction to ambient thermal resistance

Table 68 Solder reflow peak temperature

Package	Maximum peak temperature	Maximum time at peak temperature
All packages	260°C	30 seconds

Table 69 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2

Package	MSL
All packages	MSL3



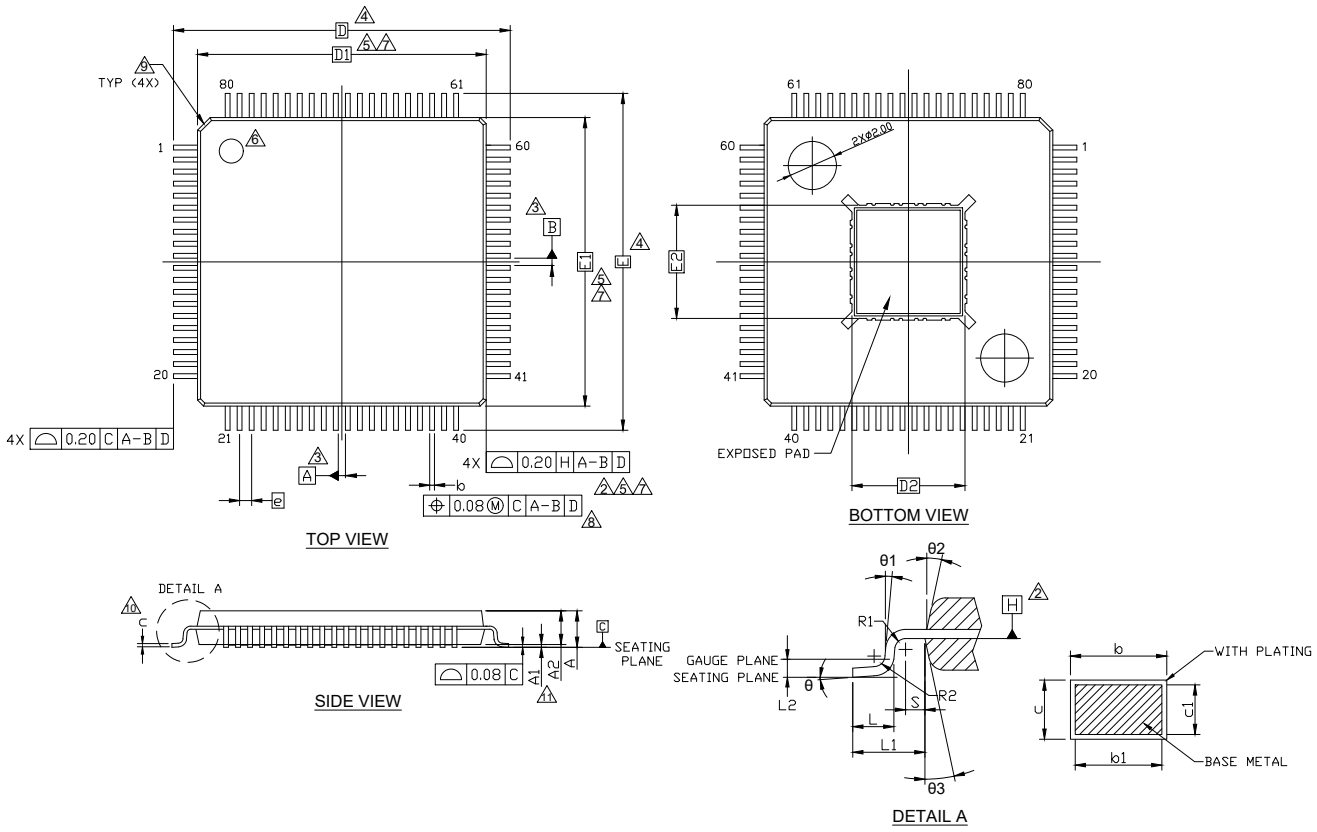
SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
D	16.00 BSC		
D1	14.00 BSC		
D2	6.35	—	6.65
E	16.00 BSC		
E1	14.00 BSC		
E2	6.35	—	6.65
R1	0.08	—	—
R2	0.08	—	0.20
θ	0°	—	8°
c	0.10	0.127	0.20
b	0.17	0.20	0.26
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 REF		
e	0.50 BSC		

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
11. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-40570 Rev *B

Figure 11 E-LQFP-100, 14.0×14.0×1.6 mm



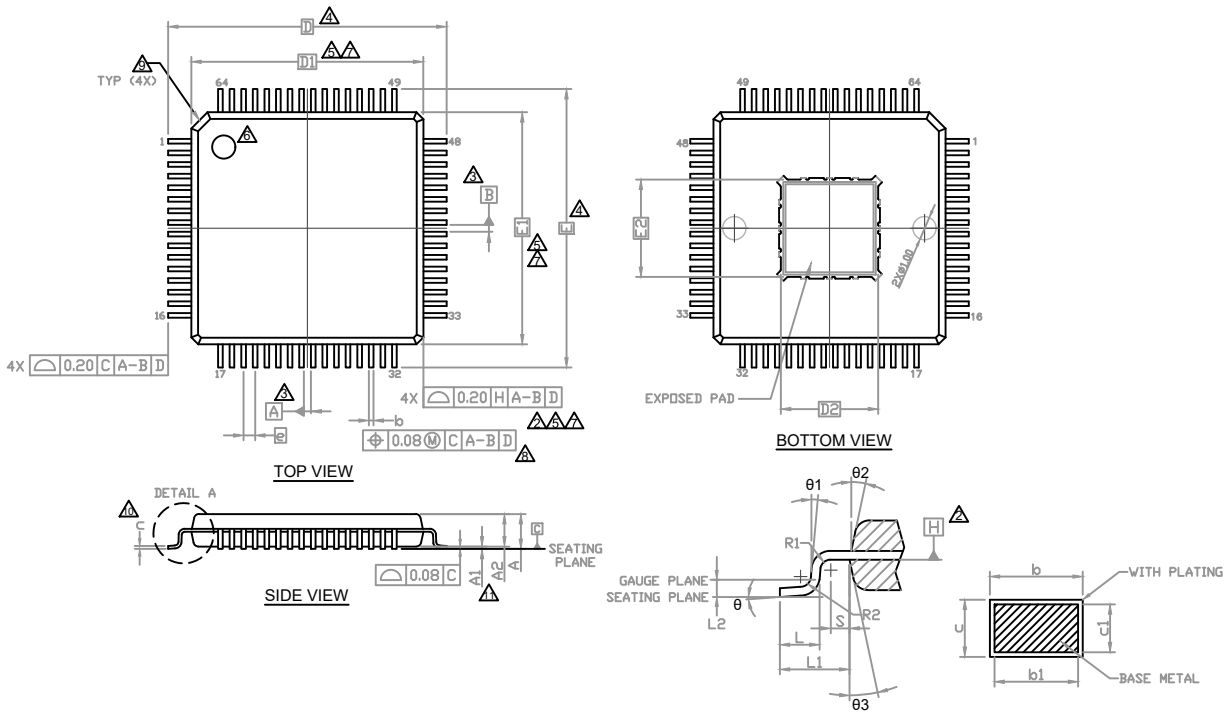
SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
D		14.00 BSC	
D1		12.00 BSC	
D2	4.30	—	4.85
E		14.00 BSC	
E1		12.00 BSC	
E2	4.30	—	4.85
R1	0.08	—	—
R2	0.08	—	0.20
θ	0°	3.5°	7°
θ1	0°	—	—
θ2	11°	12°	13°
θ3	11°	12°	13°
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	—	0.20
c1	0.09	—	0.16

SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
L	0.45	0.60	0.75
L1		1.00 REF	
L2		0.25 REF	
e		0.50 BSC	
S	0.20	—	—

NOTES
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
11. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-38596 Rev. *B

Figure 12 E-LQFP-80, 12.0×12.0×1.6 mm



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
D	12.00 BSC		
D1	10.00 BSC		
D2	3.79	—	4.34
E	12.00 BSC		
E1	10.00 BSC		
E2	3.79	—	4.34
R1	0.08	—	—
R2	0.08	—	0.20
θ	0°	3.5°	7°
θ1	0°	—	—
θ2	11°	12°	13°
θ3	11°	12°	13°
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	—	0.20
c1	0.09	—	0.16

SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 REF		
e	0.50 BSC		
S	0.20	—	—

NOTES
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
11. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

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Figure 13 E-LQFP-64, 10.0×10.0×1.6 mm

10 Errata

This section describes the errata for the PSOC™ Control C3M/P6 MCU product line (PSC3M/P6). Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. For more details, contact Infineon support.

Part numbers affected

Table 70 Part numbers affected

Part number	Device characteristics
All	PSOC™ Control C3M/P6 MCU product line (PSC3M/P6)

PSC3M/P6 qualification status

Silicon in process

PSC3M/P6 errata summary

The following table defines the errata applicability of available product line devices.

***Note**: Click on any item entry to view its description.*

Items	PSC3M/P6	Silicon revision	Fix status
[1]Intermittent faults during AES operations using the AES-256 hardware accelerator	All	1	Fix not planned

1. Intermittent faults during AES operations using the AES-256 hardware accelerator	
Problem definition	The AES-256 hardware accelerator may intermittently enter a locked alarm state, causing subsequent accesses to fault and disrupting cryptographic services that rely on the hardware AES block.
Parameters affected	AES operations, including all data transfers to and from the AES hardware IP
Trigger condition	• AES encryption or decryption processing • Data transfers between the CPU and the AES module
Scope of impact	At runtime, the AES hardware accelerator may sporadically enter an alarm (locked) state. Once in this state, all subsequent accesses to the AES module may result in faults. Any PSA Crypto API function that relies on the hardware AES accelerator may be impacted. For example, the TF-M Protected Storage service, which uses AES-CCM with 128-bit or 256-bit keys.
Workaround	• If an unexpected alarm occurs, reset the AES-256 module from the application software and re-execute the most recent cryptographic operation. The software must track the last successfully completed operation to allow safe recovery • Use Mbed TLS with Cryptolite acceleration as the cryptographic backend instead of the hardware AES block
Fix status	Fix not planned

11 Acronyms

Table 71 Acronyms used in this document

Acronym	Description
ADC	analog-to-digital converter
AES	advanced encryption standard
AFE	analog front-end
AMUX	analog multiplexer
BLDC	brushless direct current
BOD	brown-out detect
CAN	controller area network
CORDIC	coordinate rotation digital computer
CSV	clock supervision
DAC	digital to analog converter
DFU	device firmware upgrade
DSI	digital signal interconnect
DSP	digital signal processor
DMA	direct memory access
ECC	error correcting code
ECO	external crystal oscillators
ETB	embedded trace buffer
ETM	embedded trace macrocell
FET	field effect transistor
FIFO	first in, first out
FOC	field-oriented control
FPU	floating point unit
GPIO	general-purpose input/output
HPPASS	high-performance programmable analog subsystem
HRPWM	high-resolution pulse width modulator
HSIOM	high-speed I/O matrix
I-cache	instruction-cache
I2C	inter-integrated circuit
I3C	improved inter-integrated circuit
IHO	internal high-speed oscillator
ILO	low-speed oscillator
IMO	internal main oscillator

(table continues...)

Table 71 (continued) Acronyms used in this document

Acronym	Description
IPC	inter-processor communication
IRQ	interrupt request
ISR	interrupt service routine
LPComp	low-power comparator
LUT	lookup table
LVD	low-voltage detection
LVTTL	low-voltage transistor-transistor logic
MCWDT	multi-counter watchdog timer
MOTIF	motion interface
MPU	memory protection unit
NVIC	nested vectored interrupt controller
PAL	programmable array logic
PLD	programmable logic device
PLL	phase-locked loops
POR	power-on reset
ROM	read-only memory
RSA	rivest-shamir-adleman, a public-key cryptography algorithm
RTC	real-time clock
RWW	read-while-write
S/H	sample/hold
SAR	successive approximation register
SAU	secure attribution unit
SCB	serial communication blocks
SHA	secure hash algorithm
SPI	serial peripheral interface
SRAM	static random access memory
SRSS	system resources subsystem
TCPWM	timer/counter pulse-width modulator
TRNG	true random number generator
UART	universal asynchronous transmitter receiver
USB FS	universal serial bus full speed
WCO	watch crystal oscillator
WIC	wakeup interrupt controller

(table continues...)

Table 71 (continued) Acronyms used in this document

Acronym	Description
XRES	external reset input pin

12 Document conventions

12.1 Units of measure

Table 72 Units of measure

Symbol	Unit of measure
°C	degree Celsius
KB	1024 bytes
kHz	kilohertz
Mbps	megabits per second
Msps	megasamples per second
MHz	megahertz
ns	nanosecond
%	percent
V	volt

Revision history

Document revision	Date	Description of changes
*C	2026-08-31	Release to web

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