PSOC™ 4500H MCU

Based on Arm® Cortex®-M4F

General description

PSOC™ 4500H is a high-performance, ultra-low-power and secured MCU platform, purpose-built for IoT applications. The PSOC™ 4500H product line, based on the PSOC™ 6 MCU platform, is a combination of a dual CPU microcontroller with low-power flash technology, digital programmable logic, high-performance analog-to-digital conversion and standard communication and timing peripherals.

Features

- 32-bit dual CPU subsystem
  - 150-MHz Arm® Cortex®-M4F (CM4) with single-cycle multiply (Floating Point and Memory Protection Unit)
  - 100-MHz Cortex®-M0+ (CM0+) with single-cycle multiply and MPU
  - User-selectable core logic operation at either 1.1 V or 0.9 V
  - Three DMA controllers
- Memory subsystem
  - 256-KB application flash and 32-KB supervisory flash (SFlash); read-while-write (RWW) support. Two 8-KB flash caches, one for each CPU.
  - 128-KB SRAM with programmable power control and retention granularity
  - One-time-programmable (OTP) 1-Kb eFuse array
- Low-power 1.7-V to 3.6-V operation
  - Six power modes for fine-grained power management
  - Deep Sleep mode current of 7 µA with 64-KB SRAM retention
  - Backup domain with 64 bytes of memory and real-time clock
- Flexible clocking options
  - 8-MHz internal main oscillator (IMO) with ±1% accuracy
  - Ultra-low-power 32-kHz internal low-speed oscillator (ILO)
  - On-chip crystal oscillators (16 MHz to 35 MHz, and 32 kHz)
  - Phase-locked loop (PLL) for multiplying clock frequency
  - Frequency-locked loop (FLL) for multiplying IMO frequency
- Quad-SPI (QSPI)/Serial Memory Interface (SMIF)
  - Execute-In-Place (XIP) from external Quad SPI Flash
  - On-the-fly encryption and decryption
  - 4-KB cache for greater XIP performance with lower power
  - Supports single, dual, and quad interfaces with throughput up to 320 Mbps
- Segment LCD Drive
  - Supports up to 61 segments and up to 8 commons
  - Operates in System Deep Sleep mode
- Serial communication
  - Six run-time configurable serial communication blocks (SCBs)
    - Five SCBs: configurable as SPI, I^2C, or UART
    - One Deep Sleep SCB: configurable as SPI or I^2C
- Timing and pulse-width modulation
  - Twelve timer/counter pulse-width modulators (TCPWMs)
  - Center-aligned, Edge, and Pseudo-random modes
  - Comparator-based triggering of Kill signals

- Programmable analog
  - Two 12-bit 2-Msps SAR ADCs with synchronized sampling, differential and single-ended modes, 16-channel sequencer with result averaging
  - One 12-bit voltage-mode digital-to-analog converter (DAC) with < 2-µs settling time
  - Two low-power comparators available in Deep Sleep and Hibernate modes
  - Two opamps with low-power operation modes
  - Built-in temperature sensor connected to ADC
- Up to 62 Programmable GPIOs
  - One Smart I/O port (6 I/Os) enables Boolean operations on GPIO pins; available during system Deep Sleep
  - Programmable drive modes, strengths, and slew rates
  - Two overvoltage-tolerant (OVT) pins
- Capacitive sensing
  - Capacitive Sigma-Delta (CSD) provides best-in-class SNR, liquid tolerance, and proximity sensing
  - Enables dynamic usage of both self and mutual sensing
  - Automatic hardware tuning (SmartSense)
- Security built into platform architecture
  - ROM-based root of trust via uninterruptible “Secure Boot”
  - Step-wise authentication of execution images
  - Secured execution of code in execute-only mode for protected routines
  - All debug and test ingress paths can be disabled
  - Up to eight protection contexts
- Cryptography accelerators
  - Hardware acceleration for symmetric and asymmetric cryptographic methods and hash functions
  - True random number generation (TRNG) function
- Packages
  - 80-pin TQFP, 64-pin TQFP
- Device identification and revisions
  - Product line ID (12-bit): 0x10E
  - Major/Minor die revision ID: 1/3
  - Firmware Revisions: ROM Boot: 8.1, Flash Boot: 3.1.0.528 (see **Boot Code** section)

  This product line has a JTAG ID which is available through the SWJ interface. It is a 32-bit ID, where:
  - The most significant digit is the device revision, based on the Major Die Revision
  - The next four digits correspond to the part number, for example “E4B0” as a hexadecimal number
  - The three least significant digits are the manufacturer ID, in this case “069” as a hexadecimal number

The Silicon ID system call can be used by firmware to get Silicon ID and ROM Boot data. For more information, see the **technical reference manual (TRM)**.

The Flash Boot version can be read directly from designated addresses 0x1600 2004 and 0x1600 2018. For more information, see the **technical reference manual (TRM)**.

Table of contents

1 Development ecosystem

1.1 PSOC™ 4500H resources

Infineon provides a wealth of data at **www.infineon.com** to help you select the right PSOC™ device and quickly and effectively integrate it into your design. The following is an abbreviated list of resources for PSOC™ 4500H:

- **Overview**: **PSOC™ portfolio**
- **Product selectors**: **PSOC™ 6 MCU**
- **Application notes** cover a broad range of topics, from basic to advanced level, and include the following:
  - **AN221774**: Getting started with PSOC™ 6 MCU on PSOC™ Creator
  - **AN218241**: PSOC™ 6 MCU hardware design considerations
  - **AN213924**: PSOC™ 6 MCU Device Firmware Update (DFU) software development kit guide
  - **AN215656**: PSOC™ 6 MCU dual-core system design
  - **AN219528**: PSOC™ 6 MCU low-power modes and power reduction techniques
  - **AN221111**: PSOC™ 6 MCU designing a custom secured system
  - **AN85951**: PSOC™ 4 and PSOC™ 6 MCU CAPSENSE™ design guide
- **Code examples** demonstrate product features and usage, and are also available on **Infineon GitHub repositories**.
- **Technical reference manuals (TRMs)** provide detailed descriptions of PSOC™ 6 MCU architecture and registers.
- **PSOC™ 6 MCU programming specification** provides the information necessary to program PSOC™ 6 MCU nonvolatile memory
- Development Tools
- **ModusToolbox™** software enables cross platform code development with a robust suite of tools and software libraries
  - **PSOC™ 6 CAD libraries** provide footprint and schematic support for common tools. BSDL files and IBIS models are also available (the links will be provided in a later revision).
- **Training videos** are available on a wide range of topics including the **PSOC™ 6 MCU 101 series**
- **Infineon developer community** enables connection with fellow PSOC™ developers around the world, 24 hours a day, 7 days a week, and hosts a dedicated **PSOC™ 6 MCU community**

1.2 ModusToolbox™ software

ModusToolbox™ software is Infineon’s comprehensive collection of multi-platform tools and software libraries that enable an immersive development experience for creating converged MCU and wireless systems. It is:

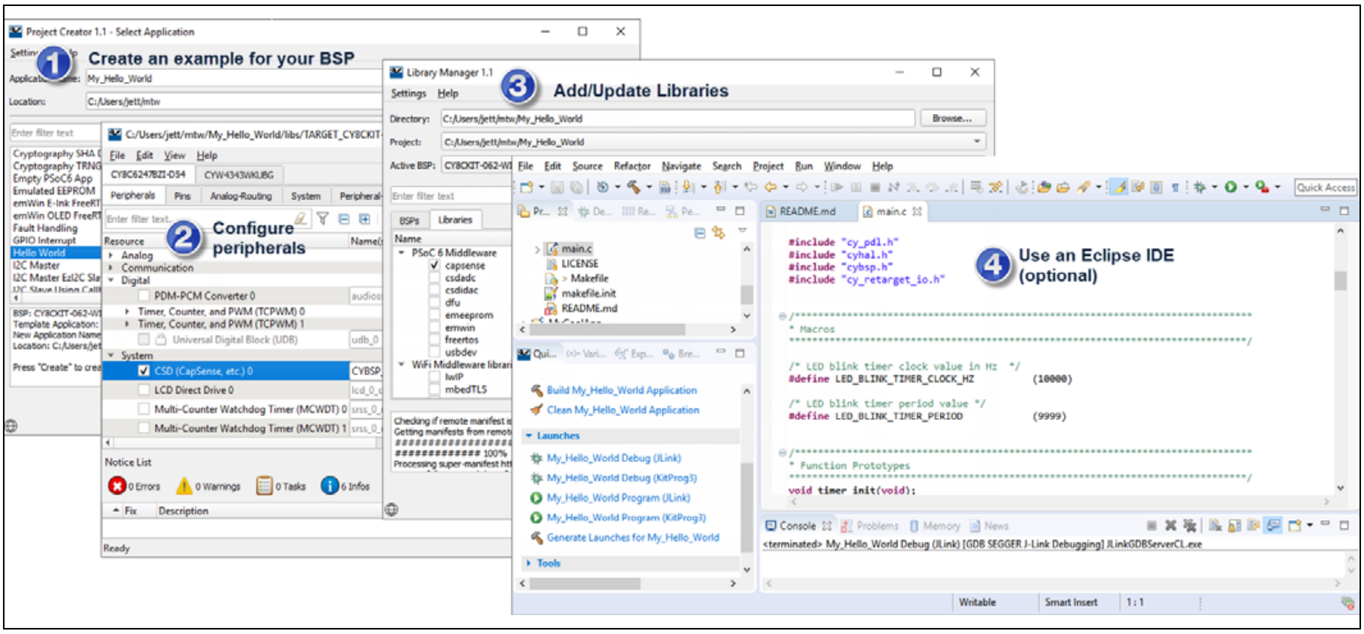
- Comprehensive - it has the resources you need
- Flexible - you can use the resources in your own workflow
- Atomic - you can get just the resources you want

Infineon provides a large collection of code **repositories on GitHub**. This includes:

- Board Support Packages (BSPs) aligned with Infineon’s kits
- Low-level resources, including a hardware abstraction layer (HAL) and peripheral driver library (PDL)
- Middleware enabling industry-leading features such as CAPSENSE™, Bluetooth Low Energy, and mesh networks
- An extensive set of thoroughly tested **code example applications**

Note: The HAL provides a high-level, simplified interface to configure and use the hardware blocks on Infineon MCUs. It is a generic interface that can be used across multiple product families. For example, it wraps the PSOC™ 6 PDL with a simplified API, but the PDL exposes all low-level peripheral functionality. You can leverage the HAL’s simpler and more generic interface for most of an application, even if one portion requires finer-grained control.

ModusToolbox™ software is IDE-neutral and easily adaptable to your workflow and preferred development environment. It includes a project creator, peripheral and library configurators, a library manager, as well as the optional Eclipse IDE for ModusToolbox™ software. For information on using Infineon tools, refer to the documentation delivered with ModusToolbox software, and **AN228571: Getting started with PSOC™ 6 MCU on ModusToolbox™ software**.



```
#include "cy_pdl.h"
#include "cyhal.h"
#include "cybsp.h"
#include "cy_retarget_io.h"


/*******************************************************************************
* Macros
*******************************************************************************/

/* LED blink timer clock value in Hz  */
#define LED_BLINK_TIMER_CLOCK_HZ          (10000)

/* LED blink timer period value */
#define LED_BLINK_TIMER_PERIOD            (9999)


/*******************************************************************************
* Function Prototypes
*******************************************************************************/
void timer init(void);
```

```
<terminated> My_Hello_World Debug (JLink) [GDB SEGGER J-Link Debugging] JLinkGDBServerCL.exe
```

Figure 1 ModusToolbox™ software tools

2 Blocks and functionality

Figure 2 shows the major subsystems and a simplified view of their interconnections. The color coding shows the lowest power mode where a block is still functional. For example, the SRAM is functional down to Sleep mode.

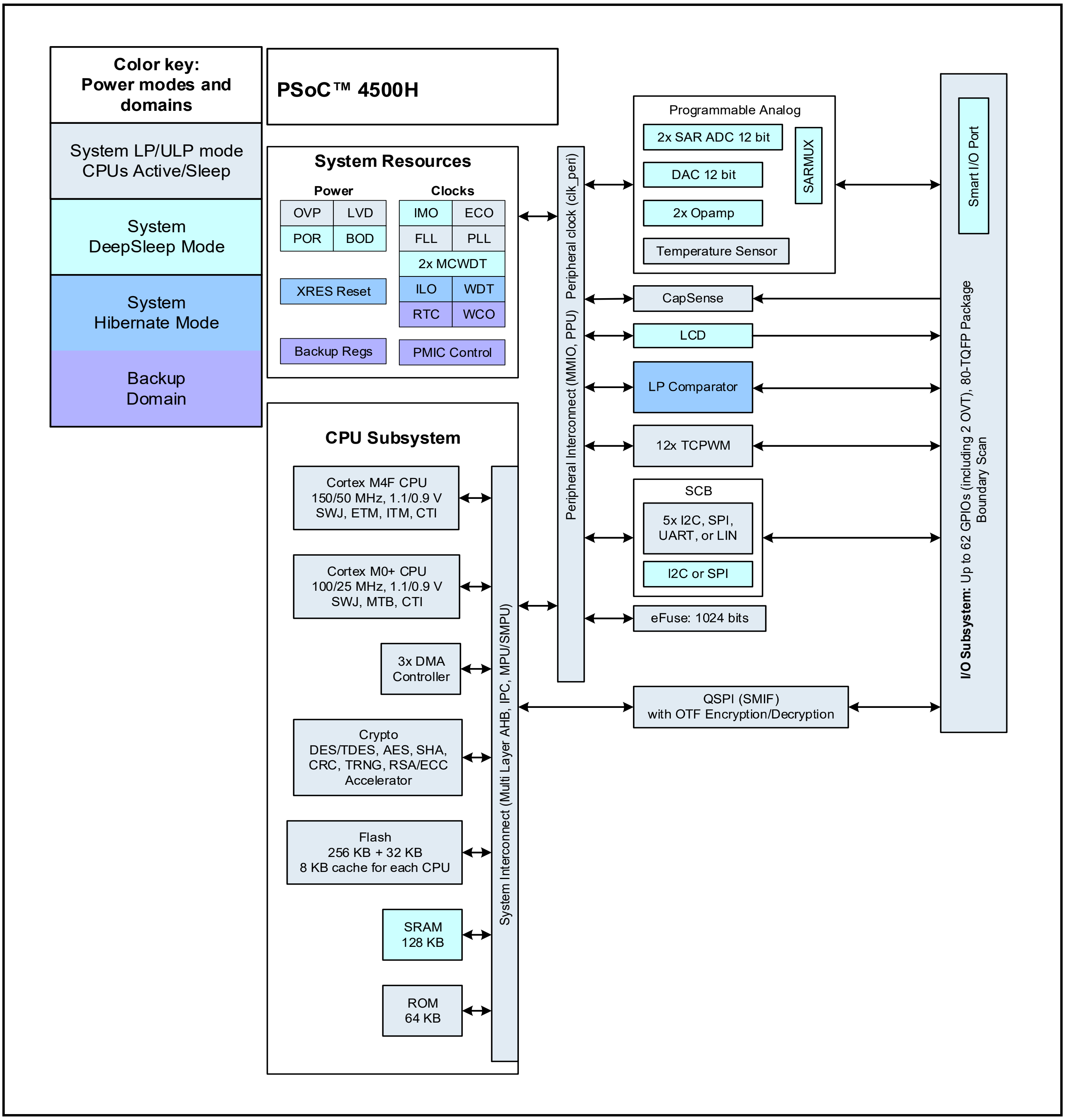


Figure 2 Block diagram

There are three debug access ports, one each for CM4 and CM0+, and a system port.

PSOC™ 4500H devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware. All device interfaces can be permanently disabled (device security) for applications concerned about attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. The security level is settable by the user.

Complete debug-on-chip functionality enables full device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The Eclipse IDE for ModusToolbox™ software provides fully integrated programming and debug support for these devices. The SWJ (SWD and JTAG) interface is fully compatible with industry-standard third party probes. With the ability to disable debug features, with very robust flash protection, and by allowing customer-proprietary functionality to be implemented in on-chip programmable blocks, PSOC™ 4500H provides multiple levels of security.

3 Functional description

The following sections provide an overview of the features, capabilities and operation of each functional block identified in the block diagram in **Figure 2**. For more detailed information, refer to the following documentation:

- Board Support Package (BSP) documentation

  BSPs are available on **GitHub**. They are aligned with Infineon kits and provide files for basic device functionality such as hardware configuration files, startup code, and linker files. The BSP also includes other libraries that are required to support a kit. Each BSP has its own documentation, but typically includes an API reference such as the example **here**. This **search link** finds all currently available BSPs on the Infineon GitHub site.

- Hardware Abstraction Layer API reference manual

  The Infineon Hardware Abstraction Layer (HAL) provides a high-level interface to configure and use hardware blocks on Infineon MCUs. It is a generic interface that can be used across multiple product families. You can leverage the HAL's simpler and more generic interface for most of an application, even if one portion requires finer-grained control. The **HAL API Reference** provides complete details. Example applications that use the HAL download it automatically from the GitHub repository.

- Peripheral Driver Library (PDL) Application Programming Interface (API) reference manual

  The Peripheral Driver Library (PDL) integrates device header files and peripheral drivers into a single package and supports all PSOC™ 6 MCU product lines. The drivers abstract the hardware functions into a set of easy-to-use APIs. These are fully documented in the **PDL API Reference**. Example applications that use the PSOC™ 6 PDL download it automatically from the GitHub repository.

- Architecture technical reference manual (TRM)

  The architecture TRM provides a detailed description of each resource in the device. This is the next reference to use if it is necessary to understand the operation of the hardware below the software provided by PDL. It describes the architecture and functionality of each resource and explains the operation of each resource in all modes. It provides specific guidance regarding the use of associated registers.

- Register technical reference manual

  The register TRM provides a complete list of all registers in the device. It includes the breakdown of all register fields, their possible settings, read/write accessibility, and default states. All registers that have a reasonable use in typical applications have functions to access them from within PDL. Note that ModusToolbox and PDL may provide software default conditions for some registers that are different from and override the hardware defaults.

3.1 CPU and memory subsystem

PSOC™ 4500H has multiple bus masters, as **Figure 2** shows. They are: CPUs, DMA controllers, QSPI, and a Crypto block. Generally, all memory and peripherals can be accessed and shared by all bus masters through multi-layer Arm® AMBA high-performance bus (AHB) arbitration. Accesses between CPUs can be synchronized using an inter-processor communication (IPC) block.

3.1.1 CPUs

There are two Arm® Cortex® CPUs:

The Cortex®-M4 (CM4) has single-cycle multiply, a floating-point unit (FPU), and a memory protection unit (MPU). It can run at up to 150 MHz. This is the main CPU, designed for a short interrupt response time, high code density, and high throughput.

CM4 implements a version of the Thumb instruction set based on Thumb-2 technology(defined in the ***Armv7-M Architecture Reference Manual***).

The Cortex®-M0+ (CM0+) has single-cycle multiply, and an MPU. It can run at up to 100 MHz; however, for CM4 speeds above 100 MHz, CM0+ and bus peripherals are limited to half the speed of CM4. Thus, for CM4 running at 150 MHz, CM0+ and peripherals are limited to 75 MHz.

CM0+ is the secondary CPU; it is used to implement system calls and device-level security, safety, and protection features. CM0+ provides a secured, uninterruptible boot function. This guarantees that post boot, system integrity is checked and memory and peripheral access privileges are enforced.

CM0+ implements the Armv6-M Thumb instruction set (defined in the ***Armv6-M Architecture Reference Manual***).

The CPUs can be selectively placed in their Sleep and Deep Sleep power modes as defined by Arm®.

Both CPUs have nested vectored interrupt controllers (NVIC) for rapid and deterministic interrupt response, and wakeup interrupt controllers (WIC) for CPU wakeup from Deep Sleep power mode.

The CPUs have extensive debug support. PSOC™ 4500H has a debug access port (DAP) that acts as the interface for device programming and debug. An external programmer or debugger (the “host”) communicates with the DAP through the device serial wire debug (SWD) or Joint Test Action Group (JTAG) interface pins. Through the DAP (and subject to device security restrictions), the host can access the device memory and peripherals as well as the registers in both CPUs.

Each CPU offers debug and trace features as follows:

- CM4 supports six hardware breakpoints and four watchpoints, 4-bit embedded trace macrocell (ETM), serial wire viewer (SWV), and printf()-style debugging through the single wire output (SWO) pin.
- CM0+ supports four hardware breakpoints and two watchpoints, and a micro trace buffer (MTB) with 4 KB dedicated RAM.

PSOC™ 4500H also has an Embedded Cross Trigger for synchronized debugging and tracing of both CPUs.

3.1.2 Interrupts

This product line has 175 system and peripheral interrupt sources and supports interrupts and system exception on both CPUs. CM4 has 175 interrupt request lines (IRQ), with the interrupt source ‘n’ directly connected to IRQn. CM0+ has eight interrupts IRQ[7:0] with configurable mapping of one or more interrupt sources to any of the IRQ[7:0]. CM0+ also supports eight internal (software only) interrupts.

Each interrupt supports configurable priority levels (eight levels for CM4 and four levels for CM0+). Up to four system interrupts can be mapped to each of the CPUs’ non-maskable interrupts (NMI). Up to 45 interrupt sources are capable of waking the device from Deep Sleep power mode using the WIC. Refer to the **technical reference manual** for details.

3.1.3 InterProcessor Communication (IPC)

In addition to the Arm® SEV and WFE instructions, a hardware InterProcessor Communication (IPC) block is included. It includes 16 IPC channels and 16 IPC interrupt structures. The IPC channels can be used to implement data communication between the processors. Each IPC channel also implements a locking scheme which can be used to manage shared resources. The IPC interrupts let one processor interrupt the other, signaling an event. This is used to trigger events such as notify and release of the corresponding IPC channels. Some IPC channels and other resources are reserved, as **Table 1** shows:

Table 1 **Distribution of IPC channels and other resources**

Resources available	Resources consumed
IPC channels, 16 available	8 reserved
IPC interrupts, 16 available	8 reserved
Other interrupts	1 reserved
CM0+ NMI	Reserved
Other resources: clock dividers, DMA channels, etc.	1 CM0+ interrupt mux

3.1.4 Direct Memory Access (DMA) Controllers

This product line has three DMA controllers, with 32, 30, and 2 channels, which support CPU-independent accesses to memory and peripherals. The descriptors for DMA channels can be in SRAM or flash. Therefore, the number of descriptors are limited only by the size of the memory. Each descriptor can transfer data in two nested loops with configurable address increments to the source and destination. The size of data transfer per descriptor varies based on the type of DMA channel. Refer to the **technical reference manual** for details.

3.1.5 Cryptography Accelerator (Crypto)

This subsystem consists of hardware implementation and acceleration of cryptographic functions and random number generators.

The Crypto subsystem supports the following:

- Encryption/Decryption Functions
  - Data Encryption Standard (DES)
  - Triple DES (3DES)
  - Advanced Encryption Standard (AES) (128-, 192-, 256-bit)
  - Elliptic Curve Cryptography (ECC)
  - RSA cryptography functions
- Hashing functions
  - Secure Hash Algorithm (SHA)
  - SHA-1
  - SHA-224/-256/-384/-512
- Message authentication functions (MAC)
  - Hashed message authentication code (HMAC)
  - Cipher-based message authentication code (CMAC)
- 32-bit cyclic redundancy code (CRC) generator
- Random number generators
  - Pseudo random number generator (PRNG)
  - True random number generator (TRNG)

3.1.6 Protection units

This product line has multiple types of protection units to control erroneous or unauthorized access to memory and peripheral registers. CM4 and CM0+ have Arm® MPUs for protection at the bus master level. Other bus masters use additional MPUs. Shared memory protection units (SMPUs) help implement memory protection for memory/resources that are shared among multiple bus masters. Peripheral protection units (PPU) are similar to SMPUs but are designed for protecting the peripheral register space.

Protection units support memory and peripheral access attributes including address range, read/write, code/data, privilege level, secured/non-secured, and protection context. Some protection unit resources are reserved for system usage; see the **technical reference manual (TRM)** for details.

3.1.7 Memory

PSOC™ 4500H contains flash, SRAM, ROM, and eFuse memory blocks.

- Flash

  There is up to 256 KB of application flash, organized in 128 KB sectors. There is also a 32 KB supervisory flash (SFlash) sector.

  Data stored in SFlash includes device trim values, **Flash Boot** code, and encryption keys. After the device transitions into the "Secure" lifecycle stage, SFlash can no longer be changed.

  The flash has 128-bit-wide accesses to reduce power. This enables flash updates during code execution. Write operations can be performed at the row level. A row is 512 bytes. Read operations are supported in both System Low Power and Ultra-Low Power modes, however write operations may not be performed in System Ultra-Low Power mode.

  The flash controller has two caches, one for each CPU. Each cache is 8 KB, with 4-way set associativity.

- SRAM

  Up to 128 KB of SRAM is provided. Power control and retention granularity is implemented in 32 KB blocks allowing the user to control the amount of memory retained in Deep Sleep. Memory is not retained in Hibernate mode.

- ROM

  The 64-KB ROM, also referred to as the supervisory ROM (SROM), provides code (**ROM Boot**) for several system functions. The ROM contains device initialization, flash write, security, eFuse programming, and other system-level routines. ROM code is executed only by the CM0+ CPU, in protection context 0. A system function can be initiated by either CPU, or through the DAP. This causes an NMI in CM0+, which causes CM0+ to execute the system function.

- eFuse

  A one-time-programmable (OTP) eFuse array consists of 1024 bits, of which 648 are reserved for system use such as die ID, device ID, initial trim settings, device life cycle, and security settings. The remaining bits are available for storing security key information, hash values, unique IDs or similar custom content.

  Each fuse is individually programmed; once programmed (or "blown"), its state cannot be changed. Blowing a fuse transitions it from the default state of 0 to 1. To program an eFuse, V_{DDIO0} must be at 2.5 V ± 5%, at 14 mA.

  Because blowing an eFuse is an irreversible process, programming is recommended only in mass production programming under controlled factory conditions. For more information, see **PSOC™ 6 MCU programming specifications**.

3.1.8 Boot Code

Two blocks of code, **ROM Boot** and **Flash Boot**, are pre-programmed into the device and work together to provide device startup and configuration, basic security features, life-cycle stage management and other system functions.

- ROM Boot

  On a device reset, the boot code in ROM is the first code to execute. This code performs the following:

  - Integrity checks of flash boot code
  - Device trim setting (calibration)
  - Setting the device protection units
  - Setting device access restrictions for lifecycle states

  ROM cannot be changed and acts as the root of trust in a secured system.

- Flash Boot

  Flash boot is firmware stored in SFlash that ensures that only a validated application may run on the device. It also ensures that the firmware image has not been modified, such as by a malicious third party.

  Flash boot:

  - Is validated by ROM Boot
  - Runs after ROM Boot and before the user application
  - Enables system calls
  - Configures the Debug Access Port
  - Launches the user application in the CM0+ (CM4 for single-CPU devices)

  If the user application cannot be validated, then flash boot ensures that the device is transitioned into a safe state.

3.1.9 Memory Map

Both CPUs have a fixed address map, with shared access to memory and peripherals. The 32-bit (4 GB) address space is divided into Arm-defined regions shown in **Table 2**. Note that Code can be executed from the code and External RAM regions.

Table 2 **Address Map for CM4 and CM0+**

Address range	Name	Use
0x0000 0000 to 0x1FFF FFFF	Code	Program code region. Data can also be placed here. It includes the exception vector table, which starts at address 0.
0x2000 0000 to 0x3FFF FFFF	SRAM	Data region. This region is not supported in PSOC™ 4500H.
0x4000 0000 to 0x5FFF FFFF	Peripheral	All peripheral registers. Code cannot be executed from this region. CM4 bit-band in this region is not supported in PSOC™ 4500H.
0x6000 0000 to 0x9FFF FFFF	External RAM	SMIF or Quad SPI, (see the **Quad-SPI/Serial Memory Interface (SMIF)** section). Code can be executed from this region.
0xA000 0000 to 0xDFFF FFFF	External Device	Not used.
0xE000 0000 to 0xE00F FFFF	Private Peripheral Bus	Provides access to peripheral registers within the CPU core.
0xE010 A000 to 0xFFFF FFFF	Device	Device-specific system registers.

The device memory map shown in **Table 3** applies to both CPUs. That is, the CPUs share access to all PSOC™ 4500H memory and peripheral registers.

Table 3 **Internal Memory Address Map for CM4 and CM0+**

Address range	Memory type	Size
0x0000 0000 to 0x0000 FFFF	ROM	64 KB
0x0800 0000 to0x0801 FFFF	SRAM	Up to 128 KB
0x1000 0000 to0x1003 FFFF	Application flash	Up to 256 KB
0x1600 0000 to 0x1600 7FFF	Supervisory flash	32 KB

Note that the PSOC™ 4500H SRAM is located in the Arm® Code region for both CPUs (see **Table 2**). There is no physical memory located in the CPUs' Arm® SRAM regions.

3.2 System resources

3.2.1 Power system

The power system provides assurance that voltage levels are as required for each respective mode and will either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (brown-out detect (BOD)) when the power supply drops below specified levels. The design guarantees safe chip operation between power supply voltage dropping below specified levels (for example, below 1.7 V) and the reset occurring. There are no voltage sequencing requirements. The V_{DDD} supply (1.7 to 3.6 V) powers an on-chip low-dropout regulator (LDO). The LDO offers a selectable (0.9 or 1.1 V) core operating voltage (V_{CCD}). The selection lets users choose between two system power modes:

- System Low Power (LP) operates V_{CCD} at 1.1 V and offers high performance, with no restrictions on device configuration.
- System Ultra Low Power (ULP) operates V_{CCD} at 0.9 V for exceptional low power, but imposes limitations on maximum clock speeds.

In addition, a backup domain adds an “always on” functionality using a separate power domain supplied by a backup supply (V_{BACKUP}) such as a battery or supercapacitor. It includes a real-time clock (RTC) with alarm feature, supported by a 32.768-kHz watch crystal oscillator (WCO), and power-management IC (PMIC) control. Pin 5 of Port 0 (P0.5) can be assigned as an enable signal for an external PMIC.

RTC alarms can be used as a trigger for the PMIC enable signal. The backup domain can generate a wake-up interrupt to the chip via the RTC timers or an external input.

3.2.2 Power modes

PSOC™ 4500H can operate in four system and three CPU power modes. These modes are intended to minimize the average power consumption in an application. For more details on power modes and other power-saving configuration options, see the application note, **AN219528: PSOC™ 6 MCU low-power modes and power reduction techniques** and the **Architecture TRM, Power Modes chapter**.

Power modes supported by PSOC™ 4500H MCUs, in the order of decreasing power consumption, are:

- System Low Power (LP) – All peripherals and CPU power modes are available at maximum speed
- System Ultra Low Power (ULP) – All peripherals and CPU power modes are available, but with limited speed
- CPU Active – CPU is executing code in system LP or ULP mode
- CPU Sleep – CPU code execution is halted in system LP or ULP mode
- CPU Deep Sleep – CPU code execution is halted and system Deep Sleep is requested in system LP or ULP mode
- System Deep Sleep – Only low-frequency peripherals are available after both CPUs enter CPU Deep Sleep mode
- System Hibernate – Device and I/O states are frozen and the device resets on wakeup

CPU Active, Sleep, and Deep Sleep are standard Arm®-defined power modes supported by the Arm CPU instruction set architecture (ISA). LP, ULP, Deep Sleep and Hibernate modes are additional low-power modes supported by PSOC™ 4500H.

3.2.3 Clock system

Figure 3 shows that the clock system of this product line consists of the following:

- Internal main oscillator (IMO)
- Internal low-speed oscillator (ILO)
- Watch crystal oscillator (WCO)
- External MHz crystal oscillator (ECO)
- External clock input
- One phase-locked loop (PLL)
- One frequency locked loop (FLL)

Clocks may be buffered and brought out to a pin on a smart I/O port.

The default clocking when the application starts is CLK_HF[0] being driven by the IMO and the FLL. CLK_HF[0], clk_fast, clk_peri, and clk_slow are all either 50 MHz (LP mode) or 25 MHz (ULP mode). All other clocks, including all peripheral clocks, are off.

3.2.4 Internal main oscillator (IMO)

The IMO is the primary source of internal clocking. It is trimmed at the factory to achieve the specified accuracy. The IMO frequency is 8 MHz and tolerance is ±1%.

3.2.5 Internal low-speed oscillator (ILO)

The ILO is a very low power oscillator, nominally 32 kHz, which operates in all power modes. The ILO can be calibrated against a higher accuracy clock for better accuracy.

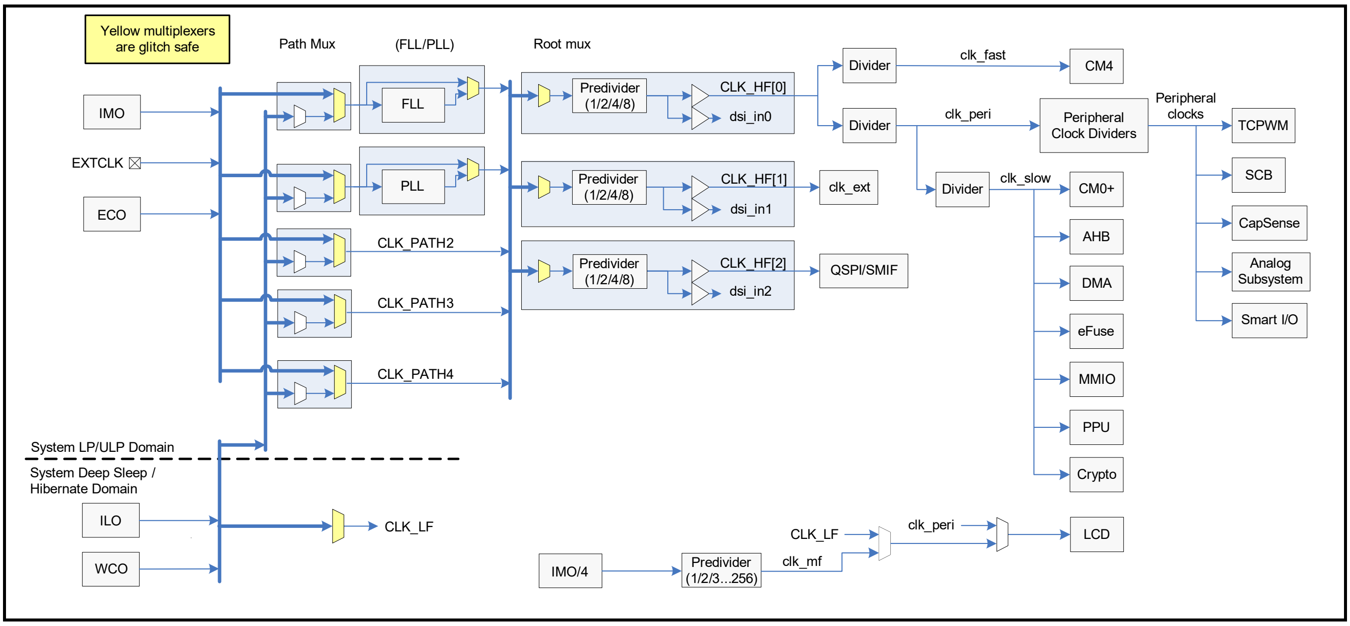


Figure 3 Clocking diagram

3.2.6 External crystal oscillators

Figure 4 shows all of the external crystal oscillator circuits for this product line. The component values shown are typical; check the **Table 44** for the crystal values, and the crystal datasheet for the load capacitor values. The ECO and WCO require balanced external load capacitors. For more information, see the TRM and **AN218241, PSOC™ 6 MCU hardware design considerations**.

The crystal oscillator can be sensitive to GPIO switching noise and requires the following constraints for reliable operation with a broad range of crystals over the range of 16 to 35 MHz:

1. Port 12 must be used in low slew rate (slow) mode which limits switching frequency to 2.5 MHz.
2. Port 11, which includes the QSPI interface, must be limited to 60-MHz operation with the QSPI and in Drive Mode 2; please see the TRM for details.

For more information, see **Table 4** and the **GPIO** section.

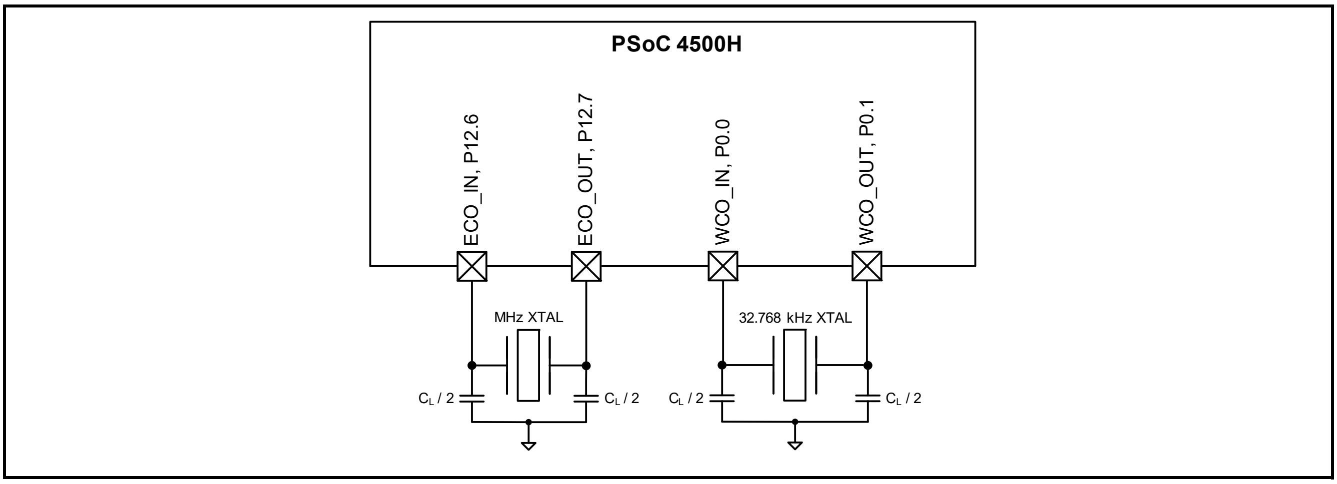


Figure 4 Oscillator circuits

3.2.7 Watchdog timers (WDT, MCWDT)

PSOC™ 4500H has one WDT and two multi-counter WDTs (MCWDT). The WDT has a 16-bit free-running counter. Each MCWDT has two 16-bit counters and one 32-bit counter, with multiple operating modes. All of the 16-bit counters can generate a watchdog device reset. All of the counters can generate an interrupt on a match event.

The WDT is clocked by the ILO. It can do interrupt/wakeup generation in LP/ULP, Deep Sleep, and Hibernate power modes. The MCWDTs are clocked by LFCLK (ILO or WCO). It can do periodic interrupt / wakeup generation in LP/ULP and Deep Sleep power modes.

3.2.8 Clock dividers

Integer and fractional clock dividers are provided for peripheral use and timing purposes. There are:

- Four 8-bit clock dividers
- Eight 16-bit integer clock dividers
- Two 16.5-bit fractional clock dividers
- One 24.5-bit fractional clock divider

3.2.9 Trigger routing

PSOC™ 4500H contains a trigger multiplexer block. This is a collection of digital multiplexers and switches that are used for routing trigger signals between peripheral blocks and between GPIOs and peripheral blocks.

There are two types of trigger routing. Trigger multiplexers have reconfigurability in the source and destination. There are also hardwired switches called “one-to-one triggers”, which connect a specific source to a destination. The user can enable or disable the route.

3.2.10 Reset

PSOC™ 4500H can be reset from a variety of sources:

- Power-on reset (POR) to hold the device in reset while the power supply ramps up to the level required for the device to function properly. POR activates automatically at power-up.
- Brown-out detect (BOD) reset to monitor the digital voltage supply V_{DDD} and generate a reset if V_{DDD} falls below the minimum required logic operating voltage.
- External reset dedicated pin (XRES) to reset the device using an external source. The XRES pin is active low. It can be connected either to a pull-up resistor to V_{DDD}, or to an active drive circuit, as **Figure 5** shows. If a pull-up resistor is used, select its value to minimize current draw when the pin is pulled low; 4.7 kΩ to 100 kΩ is typical.

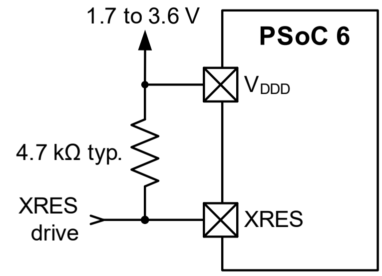


Figure 5 **XRES connection diagram**

- Watchdog timer (WDT or MCWDT) to reset the device if firmware fails to service it within a specified timeout period.
- Software-initiated reset to reset the device on demand using firmware.
- Logic-protection fault can trigger an interrupt or reset the device if unauthorized operating conditions occur; for example, reaching a debug breakpoint while executing privileged code.
- Hibernate wakeup reset to bring the device out of the system Hibernate low-power mode.

Reset events are asynchronous and guarantee reversion to a known state. Some of the reset sources are recorded in a register, which is retained through reset and allows software to determine the cause of the reset.

3.3 Programmable analog subsystems

3.3.1 12-bit SAR ADC

The two 12-bit, 2-Msps SAR ADCs can operate at a maximum clock rate of 36 MHz and require a minimum of 18 clocks at that frequency to do a 12-bit conversion. One of three internal references may be used for an ADC reference voltage: V_{DDA}, $V_{DDA/2}$, and an analog reference (AREF). AREF is nominally 1.2 V, trimmed to ±1%; see **Table 21**). An external reference may also be used, by driving a V_{REF} pin. When using $V_{DDA/2}$ or AREF as a reference, an external bypass capacitor may be connected to a V_{REF} pin to improve performance in noisy conditions. These reference options allow ratio-metric readings or absolute readings at the accuracy of the reference used. The input range of the ADCs is the full supply voltage between V_{SS} and V_{DDA}/V_{DDIOA}. The ADCs may be configured with a mix of single ended and differential signals in the same configuration.

The ADCs' sample-and-hold (S/H) aperture is programmable to allow sufficient time for signals with a high impedance to settle, if required. System performance is 65 dB for true 12-bit precision provided appropriate references are used and system noise levels permit it.

The ADCs are connected to fixed sets of pins through input sequencers. A sequencer cycles through the selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, the aggregate sampling bandwidth is equal to 2 Msps whether it is for a single channel or distributed over several channels). The result of each channel is buffered, so that an interrupt may be triggered only when a full scan of all channels is complete. Also, a pair of range registers can be set to detect and cause an interrupt if an input exceeds a minimum and/or maximum value. This allows fast detection of out-of-range values without having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software. An ADC can also be connected, under firmware control, to most other GPIO pins via the analog multiplexer bus (AMUXBUS). The ADCs are not available in Hibernate mode. The ADC operating range is 1.71 V to 3.6 V.

The ADCs have synchronous sampling, for applications such as power supply monitoring and motor control. A SAR ADC may be operated in Deep Sleep mode using a clock of either 2 MHz or 8 MHz (LPOSC).

3.3.2 Temperature sensor

Each SAR ADC block contains a temperature sensor. The sensor consists of a diode biased by a current source. It can be disabled to save power. The temperature sensor may be connected directly to a SAR ADC as one of the measurement channels. The ADC digitizes the temperature sensor’s output, and a Infineon-supplied software function may be used to convert the reading to a temperature, with calibration and linearization.

3.3.3 12-bit digital-analog converter

There is a 12-bit voltage mode DAC on the chip, which can settle in less than 2 µs. The DAC may be driven by the DMA controllers to generate user-defined waveforms. The DAC output from the chip can either be the resistive ladder output (highly linear near ground) or a buffered output using an opamp in the CTBm block.

3.3.4 Continuous time block mini (CTBm) with two opamps

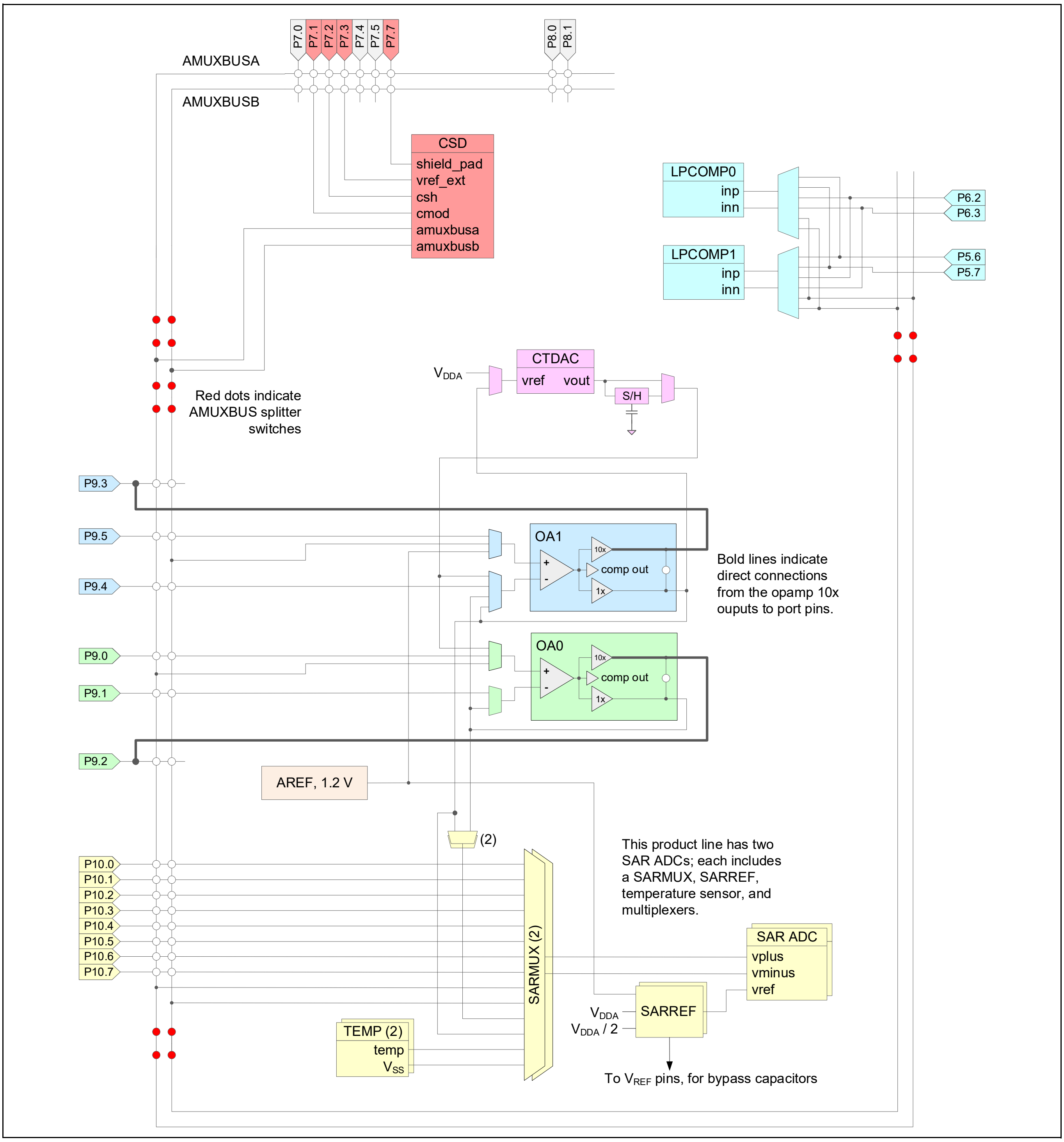
This block consists of two opamps, which have their inputs and outputs connected to pins and other analog blocks, as **Figure 6** shows. They have three power modes (high, medium, and low) and a comparator mode. The opamps can be used to buffer SAR inputs and DAC outputs. The non-inverting inputs of these opamps can be connected to either of two pins, thus allowing independent sensors to be used at different times. The pin selection can be made via firmware.

The opamps also support operation in system Deep Sleep mode, with lower performance and reduced power consumption.

3.3.5 Low-power comparators

Two low-power comparators are provided, which can operate in all power modes. This allows other analog system resources to be disabled while retaining the ability to monitor external voltage levels during system Deep Sleep and Hibernate modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator-switch event.

Figure 6 shows an overview of the analog subsystem. This diagram is a high-level abstraction. See the TRM for detailed connectivity information.



Red dots indicate AMUXBUS splitter switches

Bold lines indicate direct connections from the opamp 10x ouputs to port pins.

This product line has two SAR ADCs; each includes a SARMUX, SARREF, temperature sensor, and multiplexers.

To V_{REF} pins, for bypass capacitors

Figure 6 **Analog subsystem**

3.4 Programmable digital

3.4.1 Smart I/O

Smart I/O™ is a programmable logic fabric that enables Boolean operations on signals traveling from device internal resources to the GPIO pins or on signals traveling into the device from external sources. The Smart I/O block sits between the GPIO pins and the high-speed I/O matrix (HSIOM) and is dedicated to a single port.

This product line has one Smart I/O block, on Port 9.When the Smart I/O is not enabled, all signals on Port 9 bypass the Smart I/O hardware.

Smart I/O supports:

- System Deep Sleep operation
- Boolean operations without CPU intervention
- Asynchronous or synchronous (clocked) operation

The Smart I/O block contains a data unit (DU) and eight look up tables (LUTs).

The DU:

- Performs unique functions based on a selectable opcode.
- Can source input signals from internal resources, the GPIO port, or a value in the DU register.

Each LUT:

- Has four selectable input sources. The input signals may be sourced from another LUT, an internal resource, an external signal from a GPIO pin, or from the DU.
- Acts as a programmable Boolean logic table.
- Can be synchronous or asynchronous.

3.5 Fixed-function digital

3.5.1 Timer/counter/pulse-width modulator (TCPWM)

- The TCPWM supports the following operational modes:
  - Timer-counter with compare
  - Timer-counter with capture
  - Quadrature decoding
  - Pulse width modulation (PWM)
  - Pseudo-random PWM
  - PWM with dead time
- Up, down, and up/down counting modes.
- Clock prescaling (division by 1, 2, 4, ... 64, 128)
- Double buffering of compare/capture and period values
- Underflow, overflow, and capture/compare output signals
- Supports interrupt on:
  - Terminal count – Depends on the mode; typically occurs on overflow or underflow
  - Capture/compare – The count is captured to the capture register or the counter value equals the value in the compare register
- Complementary output for PWMs
- Selectable start, reload, stop, count, and capture event signals for each TCPWM; with rising edge, falling edge, both edges, and level trigger options. The TCPWM has a Kill input to force outputs to a predetermined state.

In this device there are:

- Four 32-bit TCPWMs
- Eight 16-bit TCPWMs

3.5.2 Serial communication blocks (SCB)

This product line has six SCBs:

- Five can implement either I^{2}C, UART, or SPI.
- One SCB (SCB #6) can operate in Deep Sleep mode with an external clock, this SCB can be either SPI slave or I^{2}C slave.

I^{2}C Mode: The SCB can implement a full multi-master and slave interface (it is capable of multimaster arbitration). This block can operate at speeds of up to 1 Mbps (Fast Mode Plus). It also supports EZI2C, which creates a mailbox address range and effectively reduces I^{2}C communication to reading from and writing to an array in memory. The SCB supports a 256-byte FIFO for receive and transmit.

The SCB is compatible with I^{2}C standard-mode, Fast Mode, and Fast Mode Plus devices as defined in the NXP I^{2}C-bus specification and user manual (UM10204). The I^{2}C bus I/O is implemented with GPIOs in open-drain mode.

UART Mode: This is a full-feature UART operating at up to 8 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows the addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. A 256-byte FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI Secure Simple Pairing (SSP) (essentially adds a start pulse that is used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block supports an EZSPI mode in which the data interchange is reduced to reading and writing an array in device SRAM. The SPI interface operates with a 25-MHz clock.

3.5.3 Quad-SPI/Serial Memory Interface (SMIF)

A serial memory interface is provided, running at up to 80 MHz. It supports single, dual, and quad SPI configurations, and supports up to four external memory devices. It supports two modes of operation:

- Memory-mapped I/O (MMIO), a command mode interface that provides data access via the SMIF registers and FIFOs
- Execute in Place (XIP), in which AHB reads and writes are directly translated to SPI read and write transfers.

In XIP mode, the external memory is mapped into the CPU internal address space, enabling code execution directly from the external memory. To improve performance, a 4-KB cache is included. XIP mode also supports AES-128 on-the-fly encryption and decryption, enabling secured storage and access of code and data in the external memory.

3.5.4 LCD

This block drives LCD commons and segments; routing is available to most of the GPIOs. One to eight of the GPIOs must be used for commons, the rest can be used for segments.

The LCD block has two modes of operation: high speed (8 MHz) and low speed (32 kHz). Both modes operate in system LP, ULP, and Deep Sleep modes, however the low-speed mode operates with reduced contrast in system Deep Sleep mode. The 8-MHz IMO is available in system Deep Sleep mode, and can be used to generate a clock for the LCD block. Review the number of common and segment lines, viewing angle requirements, and prototype performance, and then select the appropriate LCD clock frequency before using system Deep Sleep mode.

3.6 GPIO

This device has up to 62 GPIOs. The GPIO block implements the following:

- Eight drive strength modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Hold mode for latching previous state (used for retaining the I/O state in system Hibernate mode)
- Selectable slew rates for dV/dt-related noise control to improve EMI

The pins are organized in logical entities called ports, which are up to 8 pins in width. Data output and pin state registers store, respectively, the values to be driven on the pins and the input states of the pins.

Every pin can generate an interrupt if enabled; each port has an interrupt request (IRQ) associated with it.

The port 3 pins are capable of overvoltage-tolerant (OVT) operation, where the input voltage may be higher than V_{DDD}. OVT pins are commonly used with I^2C, to allow powering the chip OFF while maintaining a physical connection to an operating I^2C bus without affecting its functionality.

GPIO pins can be ganged to source or sink higher values of current. GPIO pins, including OVT pins, may not be pulled up higher than the absolute maximum; see **Electrical specifications**.

During power-on and reset, the pins are forced to the analog input drive mode, with input and output buffers disabled, so as not to crowbar any inputs and/or cause excess turn-on current.

A multiplexing network known as the high-speed I/O matrix (HSIOM) is used to multiplex between various peripheral and analog signals that may connect to an I/O pin.

Analog performance is affected by GPIO switching noise. In order to get the best Analog performance, the following frequency and drive mode constraints must be applied. The DRIVE_SEL values (see **Table 4**) represent drive strengths (see the PSOC™ 4500H architecture and register TRMs for further details).

Table 4 **DRIVE_SEL values**

Ports	Max frequency	Drive strength for $V_{DDD} \leq 2.7$ V	Drive strength for $V_{DDD} > 2.7$ V
Ports 0, 1	8 MHz	DRIVE_SEL 2	DRIVE_SEL 3
Port 2	50 MHz	DRIVE_SEL 1	DRIVE_SEL 2
Ports 3 to 10	16 MHz; 25 MHz for SPI	DRIVE_SEL 2	DRIVE_SEL 3
Ports 11 to 12	80 MHz for SMIF (QSPI)	DRIVE_SEL 1	DRIVE_SEL 2
Ports 9 and 10	Slow slew rate setting for TQFP Packages for ADC performance	No restrictions	No restrictions

3.7 CAPSENSE™ subsystem

CAPSENSE™ is supported in PSOC™ 4500H through a capacitive sigma-delta (CSD) hardware block. It is designed for high-sensitivity self-capacitance and mutual-capacitance measurements, and is specifically built for user interface solutions.

In addition to CAPSENSE™, the CSD hardware block supports three general-purpose functions. These are available when CAPSENSE™ is not being used. Alternatively, two or more functions can be time-multiplexed in an application under firmware control. The four functions supported by the CSD hardware block are:

- CAPSENSE™
- 10-bit ADC
- Programmable current sources (IDAC)
- Comparator

CAPSENSE™

Capacitive touch sensors are designed for user interfaces that rely on human body capacitance to detect the presence of a finger on or near a sensor. Infineon CAPSENSE™ solutions bring elegant, reliable, and simple capacitive touch sensing functions to applications including IoT, industrial, automotive, and home appliances.

The Infineon-proprietary CAPSENSE™ technology offers the following features:

- Best-in-class signal-to-noise ratio (SNR) and robust sensing under harsh and noisy conditions
- Self-capacitance (CSD) and mutual-capacitance (CSX) sensing methods
- Support for various widgets, including buttons, matrix buttons, sliders, touchpads, and proximity sensors
- High-performance sensing across a variety of materials
- Best-in-class liquid tolerance
- SmartSense auto-tuning technology that helps avoid complex manual tuning processes
- Superior immunity against external noise
- Spread-spectrum clocks for low radiated emissions
- Gesture and built-in self-test libraries
- Ultra-low power consumption
- An integrated graphical CAPSENSE™ tuner for real-time tuning, testing, and debugging

ADC

The CAPSENSE™ subsystem slope ADC offers the following features:

- Selectable 8- or 10-bit resolution
- Selectable input range: GND to V_{REF} and GND to V_{DDA} on any GPIO input
- Measurement of V_{DDA} against an internal reference without the use of GPIO or external components

IDAC

The CSD block has two programmable current sources, which offer the following features:

- 7-bit resolution
- Sink and source current modes
- A current source programmable from 37.5 nA to 609 µA
- Two IDACs that can be used in parallel to form one 8-bit IDAC

Comparator

The CAPSENSE™ subsystem comparator operates in the system Low Power and Ultra-Low Power modes. The inverting input is connected to an internal programmable reference voltage and the non-inverting input can be connected to any GPIO via the AMUXBUS.

CAPSENSE™ hardware subsystem

Figure 7 shows the high-level hardware overview of the CAPSENSE™ subsystem, which includes a delta sigma converter, internal clock dividers, a shield driver, and two programmable current sources.

The inputs are managed through analog multiplexed buses (AMUXBUS A/B). The input and output of all functions offered by the CSD block can be provided on any GPIO or on a group of GPIOs under software control, with the exception of the comparator output and external capacitors that use dedicated GPIOs.

Self-capacitance is supported by the CSD block using AMUXBUS A, an external modulator capacitor, and a GPIO for each sensor. There is a shield electrode (optional) for self-capacitance sensing. This is supported using AMUXBUS B and an optional external shield tank capacitor (to increase the drive capability of the shield driver) should this be required. Mutual-capacitance is supported by the CSD block using AMUXBUS A, two external integrated capacitors, and a GPIO for transmit and receive electrodes.

The ADC does not require an external component. Any GPIO that can be connected to AMUXBUS A can be an input to the ADC under software control. The ADC can accept V_{DDA} as an input without needing GPIOs (for applications such as battery voltage measurement).

The two programmable current sources (IDACs) in general-purpose mode can be connected to AMUXBUS A or B. They can therefore connect to any GPIO pin. The comparator resides in the delta-sigma converter. The comparator inverting input can be connected to the reference. Both comparator inputs can be connected to any GPIO using AMUXBUS B; see **Figure 6**. The reference has a direct connection to a dedicated GPIO; see **Table 7**.

The CSD block can operate in active and sleep CPU power modes, and seamlessly transition between LP and ULP system modes. It can be powered down in system Deep Sleep and Hibernate modes. Upon wakeup from Hibernate mode, the CSD block requires re-initialization. However, operation can be resumed without re-initialization upon exit from Deep Sleep mode, under firmware control.

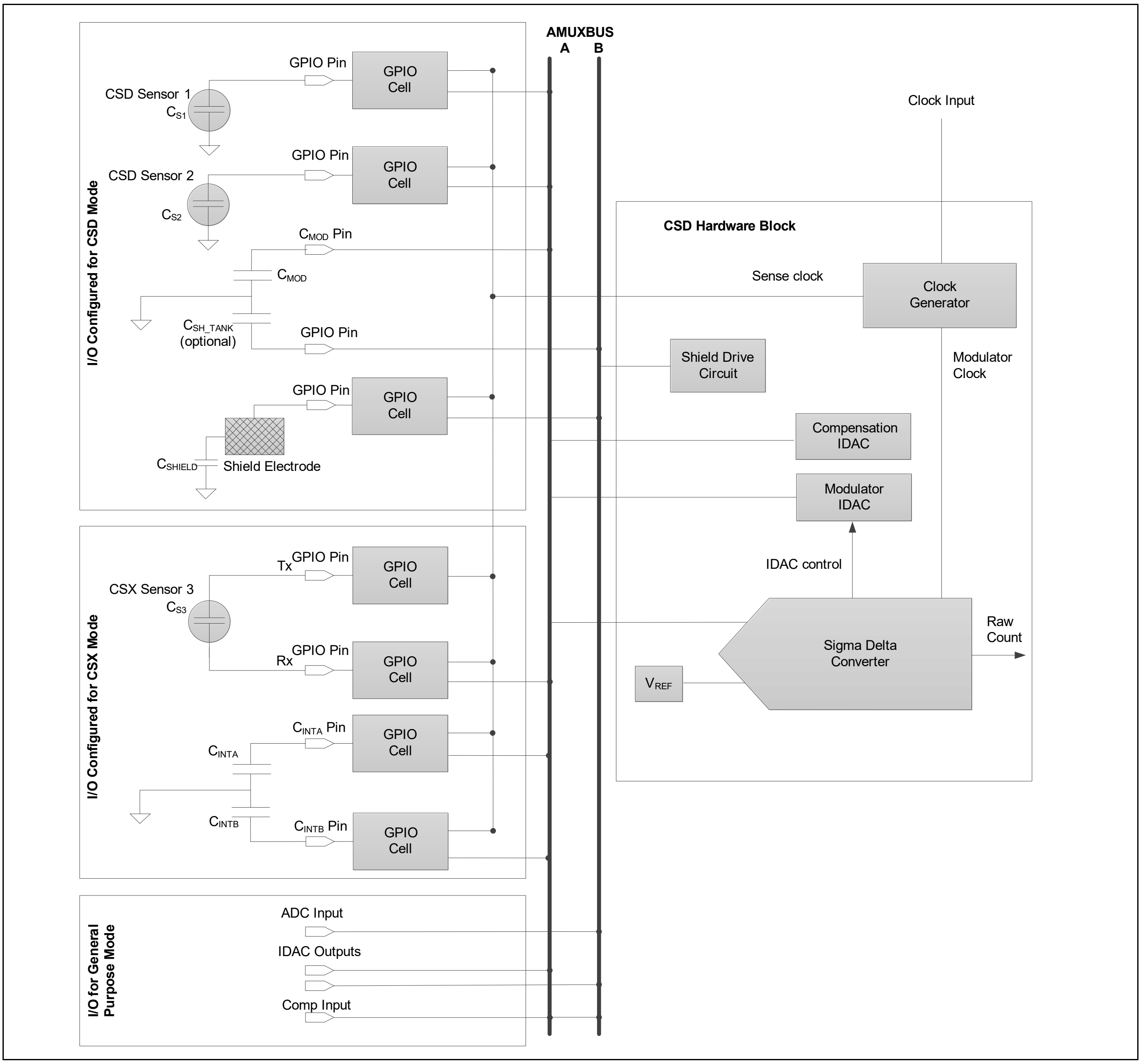


Figure 7 **CAPSENSE™ hardware subsystem**

Figure 8 shows the high-level software overview. Infineon provides middleware libraries for **CAPSENSE™**, **ADC**, and **IDAC** on GitHub to enable quick integration. The Board Support Package for any kit with CAPSENSE™ capabilities automatically includes the CAPSENSE™ library in any application that uses the BSP.

User applications interact only with middleware to implement functions of the CSD block. The middleware interacts with underlying drivers to access hardware as necessary. The CSD driver facilitates time-multiplexing of the CSD hardware if more than one piece of CSD-related middleware is present in a project. It prevents access conflicts in this case.

ModusToolbox™ software provides a CAPSENSE™ configurator to enable fast library configuration. It also provides a tuner for performance evaluation and real-time tuning of the system. The tuner requires an EZI2C communication interface in the application to enable real-time tuning capability. The tuner can update configuration parameters directly in the device as well as in the configurator.

CAPSENSE™ and ADC middleware use the CSD interrupt to implement non-blocking sensing and A-to-D conversion. Therefore, interrupt service routines are a defined part of the middleware, which must be initialized by the application. Middleware and drivers can operate on either CPU. Infineon recommends using the middleware only in one CPU. If both CPUs must access the CSD driver, memory access should be managed in the application.

Refer to **AN85951: PSOC™ 4 and PSOC™ 6 MCU CAPSENSE™ design guide** for more details on CSX sensing, CSD sensing, shield electrode usage and its benefits, and capacitive system design guidelines.

Refer to the API reference guides for **CAPSENSE™**, **ADC**, and **IDAC** available on GitHub.

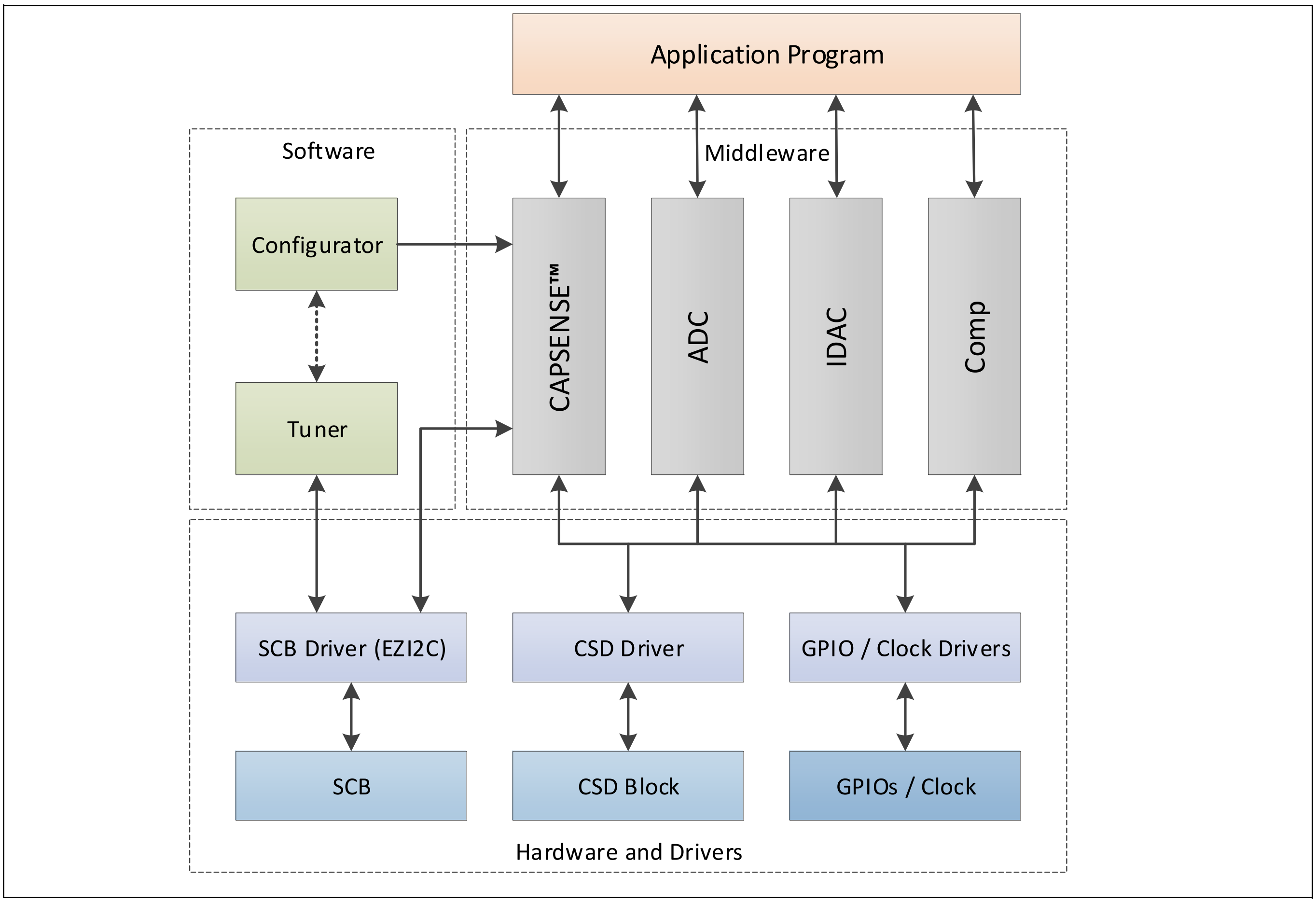


Figure 8 **CAPSENSE™ software/Firmware subsystem**

4 Pinouts

GPIO ports are powered by V_{DDx} pins as follows:

- P0: V_{BACKUP}
- P1, P2, P3: V_{DDIO2}. Port 3 pins are overvoltage tolerant (OVT).
- P5, P6, P7, P8: V_{DDIO1}
- P9, P10: V_{DDIOA}, V_{DDA} (V_{DDIOA}, when present, and V_{DDA} must be connected together on the PCB)
- P11, P12: V_{DDIO0}

Table 5 **Packages and Pin Information**

Pin	Package	
	80-TQFP	64-TQFP
V_{DDD}	1	2
V_{CCD}	80	1
V_{DDA}	59	46
V_{DDIOA}	40	-
V_{DDIO0}	76	62
V_{DDIO1}	39	32
V_{DDIO2}	23	19
V_{BACKUP}	3	3
V_{SS}	2, 11, 24, 38, 41, 58, 77	GND PAD
XRES	10	10
V_{REF}	57, 60	45, 47
P0.0	4	4
P0.1	5	5
P0.2	6	6
P0.3	7	7
P0.4	8	8
P0.5	9	9
P1.0	12	-
P1.1	13	-
P1.2	14	-
P2.0	15	11
P2.1	16	12
P2.2	17	13
P2.3	18	14
P2.4	19	15
P2.5	20	16
P2.6	21	17
P2.7	22	18
P3.0	25	20
P3.1	26	21
P5.0	27	22
P5.1	28	23
P5.2	29	-
P5.6	30	24
P5.7	31	25
P6.2	32	26
P6.3	33	27
P6.4	34	28
P6.5	35	29
P6.6	36	30

Table 5 **Packages and Pin Information** *(continued)*

Pin	Package	
	80-TQFP	64-TQFP
P6.7	37	31
P7.0	42	33
P7.1	43	34
P7.2	44	35
P7.3	45	36
P7.4	46	-
P7.5	47	-
P7.7	48	-
P8.0	49	37
P8.1	50	38
P9.0	51	39
P9.1	52	40
P9.2	53	41
P9.3	54	42
P9.4	55	43
P9.5	56	44
P10.0	61	48
P10.1	62	49
P10.2	63	50
P10.3	64	51
P10.4	65	52
P10.5	66	53
P10.6	67	54
P10.7	68	55
P11.1	69	-
P11.2	70	56
P11.3	71	57
P11.4	72	58
P11.5	73	59
P11.6	74	60
P11.7	75	61
P12.6	78	63
P12.7	79	64

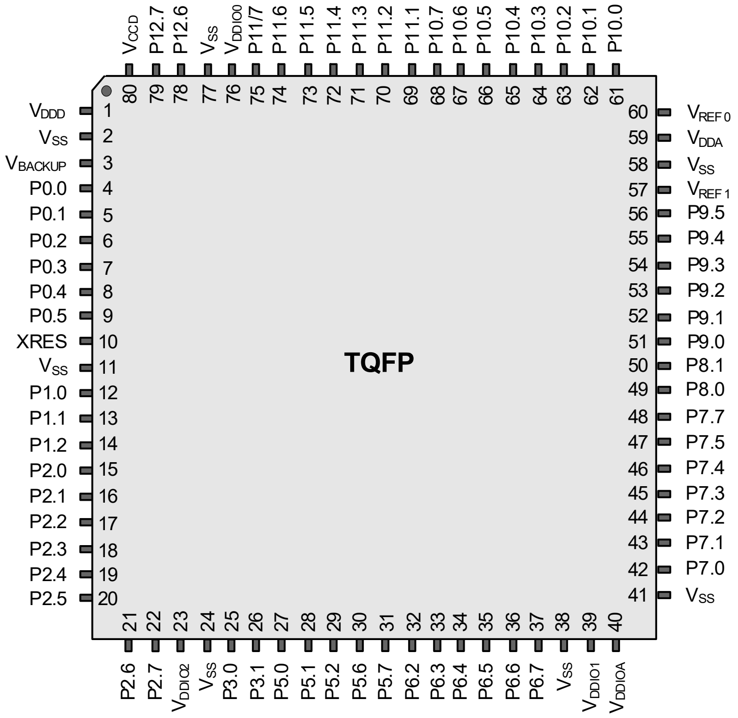


Figure 9 Device pinout for 80-pin TQFP package

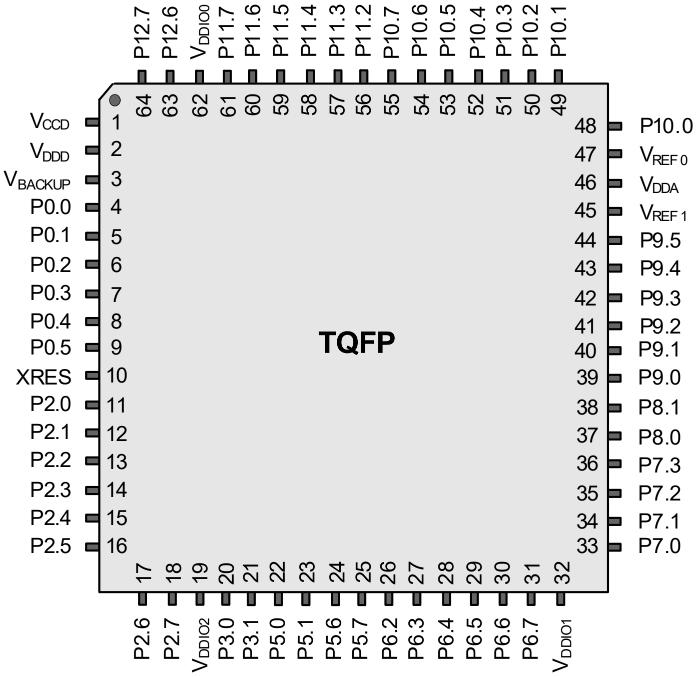


Figure 10 Device pinout for 64-pin TQFP package

Each port pin has multiple alternate functions. These are defined in **Table 6**. The columns ACT #x and DS #y denote active (System LP/ULP) and Deep Sleep mode signals respectively.

The notation for a signal is of the form IPName[x].signal_name[u]:y.

IPName = Name of the block (such as tcpwm), x = Unique instance of the IP, Signal_name = Name of the signal, u = Signal number where there is more than one signal for a particular signal name, y = Designates copies of the signal name.

For example, the name tcpwm[0].line_compl[3]:4 indicates that this is instance 0 of a tcpwm block, the signal is line_compl # 3 (complement of the line output) and this is the fourth occurrence (copy) of the signal. Signal copies are provided to allow flexibility in routing and to maximize use of on-chip resources.

Table 6 Multiple alternate functions

Port/Pin	ACT #0	ACT #1	ACT #2	ACT #3	DS #2	DS #3	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #5	DS #6
P0.0	tcpwm[0].line[0]:0	tcpwm[256].line[0]:0	csd.csd_tx:0	csd.csd_tx_n:0			srss.ext_clk:0				scb[0].spi_select1:0			peri.tr_io_input[0]:0					
P0.1	tcpwm[0].line_compl[0]:0	tcpwm[256].line_compl[0]:0	csd.csd_tx:1	csd.csd_tx_n:1							scb[0].spi_select2:0			peri.tr_io_input[1]:0				cpuss.swj_trstn	
P0.2	tcpwm[257].line[1]:0	tcpwm[257].line[1]:0	csd.csd_tx:2	csd.csd_tx_n:2					scb[0].uart_rx:0	scb[0].i2c_scl:0	scb[0].spi_mosi:0								
P0.3	tcpwm[0].line_compl[1]:0	tcpwm[257].line_compl[1]:0	csd.csd_tx:3	csd.csd_tx_n:3					scb[0].uart_tx:0	scb[0].i2c_sda:0	scb[0].spi_miso:0								
P0.4	tcpwm[0].line[2]:0	tcpwm[258].line[2]:0	csd.csd_tx:4	csd.csd_tx_n:4					scb[0].uart_rts:0		scb[0].spi_clk:0			peri.tr_io_input[2]:0	peri.tr_io_output[0]:2				
P0.5	tcpwm[0].line_compl[2]:0	tcpwm[258].line_compl[2]:0	csd.csd_tx:5	csd.csd_tx_n:5			srss.ext_clk:1		scb[0].uart_cts:0		scb[0].spi_select0:0			peri.tr_io_input[3]:0	peri.tr_io_output[1]:2				
P1.0			csd.csd_tx:6	csd.csd_tx_n:6															
P1.1			csd.csd_tx:7	csd.csd_tx_n:7															
P1.2			csd.csd_tx:8	csd.csd_tx_n:8															
P2.0	tcpwm[0].line[3]:0	tcpwm[0].line[259]:0	csd.csd_tx:9	csd.csd_tx_n:9					scb[1].uart_rx:1	scb[1].i2c_scl:1	scb[1].spi_mosi:1			peri.tr_io_input[4]:0					
P2.1	tcpwm[0].line_compl[3]:0	tcpwm[0].line_compl[259]:0	csd.csd_tx:10	csd.csd_tx_n:10					scb[1].uart_tx:1	scb[1].i2c_sda:1	scb[1].spi_miso:1			peri.tr_io_input[5]:0					
P2.2	tcpwm[0].line[0]:1	tcpwm[0].line[260]:0	csd.csd_tx:11	csd.csd_tx_n:11					scb[1].uart_rts:1		scb[1].spi_clk:1								
P2.3	tcpwm[0].line_compl[0]:1	tcpwm[0].line_compl[260]:0	csd.csd_tx:12	csd.csd_tx_n:12					scb[1].uart_cts:1		scb[1].spi_select0:1								
P2.4	tcpwm[0].line[1]:1	tcpwm[0].line[261]:0	csd.csd_tx:13	csd.csd_tx_n:13							scb[1].spi_select1:1								
P2.5	tcpwm[0].line_compl[1]:1	tcpwm[0].line_compl[261]:0	csd.csd_tx:14	csd.csd_tx_n:14							scb[1].spi_select2:1								

Table 6 **Multiple alternate functions** *(continued)*

Port/Pin	ACT #0	ACT #1	ACT #2	ACT #3	DS #2	DS #3	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #5	DS #6
P2.6	tcpwm[0].line[1]:5	tcpwm[1].line[262]:1	csd.csd_tx:15	csd.csd_tx_n:15		lpcomp.dsi_comp0:0					scb[1].spi_select3:1			peri.tr_io_input[8]:0					
P2.7	tcpwm[0].line_compl[2]:1	tcpwm[0].line_compl[262]:0	csd.csd_tx:16	csd.csd_tx_n:16		lpcomp.dsi_comp1:0								peri.tr_io_input[9]:0					
P3.0	tcpwm[0].line[3]:1	tcpwm[0].line[263]:0	csd.csd_tx:17	csd.csd_tx_n:17					scb[2].uart_rx:1	scb[2].i2c_scl:1				peri.tr_io_input[6]:0					
P3.1	tcpwm[0].line_compl[3]:1	tcpwm[0].line_compl[263]:0	csd.csd_tx:18	csd.csd_tx_n:18					scb[2].uart_tx:1	scb[2].i2c_sda:1				peri.tr_io_input[7]:0					
P5.0	tcpwm[0].line[0]:2	tcpwm[0].line[256]:1	csd.csd_tx:19	csd.csd_tx_n:19					scb[5].uart_rx:0	scb[5].i2c_scl:0	scb[5].spi_mosi:0		canfd[0].ttcan_rx[0]	peri.tr_io_input[10]:0					
P5.1	tcpwm[0].line_compl[0]:2	tcpwm[0].line_compl[256]:1	csd.csd_tx:20	csd.csd_tx_n:20					scb[5].uart_tx:0	scb[5].i2c_sda:0	scb[5].spi_miso:0		canfd[0].ttcan_tx[0]	peri.tr_io_input[11]:0					
P5.2			csd.csd_tx:21	csd.csd_tx_n:21															
P5.6	tcpwm[0].line[1]:2	tcpwm[0].line[257]:1	csd.csd_tx:22	csd.csd_tx_n:22															
P5.7	tcpwm[0].line_compl[1]:2	tcpwm[0].line_compl[257]:1	csd.csd_tx:23	csd.csd_tx_n:23															
P6.2	tcpwm[0].line[3]:2	tcpwm[0].line[259]:1	csd.csd_tx:24	csd.csd_tx_n:24											cpuss.fault_out[0]				
P6.3	tcpwm[0].line_compl[3]:2	tcpwm[0].line_compl[259]:1	csd.csd_tx:25	csd.csd_tx_n:25											cpuss.fault_out[1]				
P6.4	tcpwm[0].line[0]:3	tcpwm[0].line[260]:1	csd.csd_tx:26	csd.csd_tx_n:26	scb[6].i2c_scl:0									peri.tr_io_input[12]:0	peri.tr_io_output[0]:1			cpuss.swj_swo_tdo	scb[6].spi_mosi:0
P6.5	tcpwm[0].line_compl[0]:3	tcpwm[1].line_compl[260]:1	csd.csd_tx:27	csd.csd_tx_n:27	scb[6].i2c_sda:0									peri.tr_io_input[13]:0	peri.tr_io_output[1]:1			cpuss.swj_swdoe_tdi	scb[6].spi_miso:0
P6.6	tcpwm[0].line[1]:3	tcpwm[0].line[261]:1	csd.csd_tx:28	csd.csd_tx_n:28														cpuss.swj_swdio_tms	scb[6].spi_clk:0
P6.7	tcpwm[0].line_compl[1]:3	tcpwm[0].line_compl[261]:1	csd.csd_tx:29	csd.csd_tx_n:29														cpuss.swj_swclk_tclk	scb[6].spi_select0:0
P7.0	tcpwm[0].line[2]:2	tcpwm[0].line[262]:1	csd.csd_tx:30	csd.csd_tx_n:30					scb[4].uart_rx:0	scb[4].i2c_scl:0	scb[4].spi_mosi:0			peri.tr_io_input[14]:0		cpuss.trace_clock			
P7.1	tcpwm[0].line_compl[2]:2	tcpwm[0].line_compl[262]:1	csd.csd_tx:31	csd.csd_tx_n:31					scb[4].uart_tx:0	scb[4].i2c_sda:0	scb[4].spi_miso:0			peri.tr_io_input[15]:0					

Table 6 Multiple alternate functions *(continued)*

Port/Pin	ACT #0	ACT #1	ACT #2	ACT #3	DS #2	DS #3	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #5	DS #6
P7.2	tcpwm[0].line[3]:3	tcpwm[0].line[263]:1	csd.csd_tx:32	csd.csd_tx_n:32					scb[4].uart_rts:0		scb[4].spi_clk:0								
P7.3	tcpwm[0].line_compl[3]:3	tcpwm[0].line_compl[263]:1	csd.csd_tx:33	csd.csd_tx_n:33					scb[4].uart_cts:0		scb[4].spi_select0:0								
P7.4			csd.csd_tx:34	csd.csd_tx_n:34							scb[4].spi_select1:0								
P7.5			csd.csd_tx:35	csd.csd_tx_n:35							scb[4].spi_select2:0								
P7.7			csd.csd_tx:36	csd.csd_tx_n:36								cpuss.clk_fm_pump							
P8.0	tcpwm[0].line[2]:3	tcpwm[0].line[258]:1	csd.csd_tx:37	csd.csd_tx_n:37					scb[4].uart_rx:1	scb[4].i2c_scl:1	scb[4].spi_mosi:1			peri.tr_io_input[16]:0					
P8.1	tcpwm[0].line_compl[2]:3	tcpwm[0].line_compl[258]:1	csd.csd_tx:38	csd.csd_tx_n:38					scb[4].uart_tx:1	scb[4].i2c_sda:1	scb[4].spi_miso:1			peri.tr_io_input[17]:0					
P9.0	tcpwm[0].line[0]:4	tcpwm[0].line[260]:2	csd.csd_tx:39	csd.csd_tx_n:39					scb[2].uart_rx:0	scb[2].i2c_scl:0	scb[2].spi_mosi:0			peri.tr_io_input[18]:0			cpuss.trace_data[3]:1		
P9.1	tcpwm[0].line_compl[0]:4	tcpwm[0].line_compl[260]:2	csd.csd_tx:40	csd.csd_tx_n:40					scb[2].uart_tx:0	scb[2].i2c_sda:0	scb[2].spi_miso:0			peri.tr_io_input[19]:0			cpuss.trace_data[2]:1		
P9.2	tcpwm[0].line[1]:4	tcpwm[0].line[261]:2	csd.csd_tx:41	csd.csd_tx_n:41					scb[2].uart_rts:0		scb[2].spi_clk:0		pass.dsi_ctb_cmp0:1				cpuss.trace_data[1]:1		
P9.3	tcpwm[0].line_compl[1]:4	tcpwm[0].line_compl[261]:3	csd.csd_tx:42	csd.csd_tx_n:42					scb[2].uart_cts:0		scb[2].spi_select0:0		pass.dsi_ctb_cmp1:1				cpuss.trace_data[0]:1		
P9.4			csd.csd_tx:43	csd.csd_tx_n:43							scb[2].spi_select1:0								
P9.5			csd.csd_tx:44	csd.csd_tx_n:44							scb[2].spi_select2:0								
P10.0	tcpwm[0].line[2]:4	tcpwm[0].line[262]:2	csd.csd_tx:45	csd.csd_tx_n:45					scb[1].uart_rx:0	scb[1].i2c_scl:0	scb[1].spi_mosi:0			peri.tr_io_input[20]:0			cpuss.trace_data[3]:0		
P10.1	tcpwm[0].line_compl[2]:4	tcpwm[0].line_compl[262]:2	csd.csd_tx:46	csd.csd_tx_n:46					scb[1].uart_tx:0	scb[1].i2c_sda:0	scb[1].spi_miso:0			peri.tr_io_input[21]:0			cpuss.trace_data[2]:0		
P10.2	tcpwm[0].line[3]:4	tcpwm[0].line[263]:2	csd.csd_tx:47	csd.csd_tx_n:47					scb[1].uart_rts:0		scb[1].spi_clk:0						cpuss.trace_data[1]:0		
P10.3	tcpwm[0].line_compl[3]:4	tcpwm[0].line_compl[263]:2	csd.csd_tx:48	csd.csd_tx_n:48					scb[1].uart_cts:0		scb[1].spi_select0:0						cpuss.trace_data[0]:0		
P10.4	tcpwm[0].line[0]:5	tcpwm[0].line[256]:2	csd.csd_tx:49	csd.csd_tx_n:49							scb[1].spi_select1:0	audioss[0].pdm_clk:0							

Table 6 Multiple alternate functions *(continued)*

Port/Pin	ACT #0	ACT #1	ACT #2	ACT #3	DS #2	DS #3	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #5	DS #6
P10.5	tcpwm[0].line_compl[0]:5	tcpwm[0].line_compl[256]:2	csd.csd_tx:50	csd.csd_tx_n:50							scb[1].spi_select2:0	audioss[0].pdm_data:0							
P10.6	tcpwm[0].line[1]:5	tcpwm[0].line[257]:2	csd.csd_tx:51	csd.csd_tx_n:51							scb[1].spi_select3:0			peri.tr_io_input[22]:0					
P10.7	tcpwm[0].line_compl[1]:5	tcpwm[0].line_compl[257]:2	csd.csd_tx:52	csd.csd_tx_n:52				smif.spi_select2						peri.tr_io_input[23]:0					
P11.1			csd.csd_tx:53	csd.csd_tx_n:53				smif.spi_select1											
P11.2	tcpwm[0].line[3]:5	tcpwm[0].line[259]:2	csd.csd_tx:54	csd.csd_tx_n:54				smif.spi_select0	scb[5].uart_rts:0		scb[5].spi_clk:0								
P11.3	tcpwm[0].line_compl[3]:5	tcpwm[0].line_compl[259]:2	csd.csd_tx:55	csd.csd_tx_n:55				smif.spi_data3	scb[5].uart_cts:0		scb[5].spi_select0:0				peri.tr_io_output[0]:0				
P11.4	tcpwm[0].line[0]:6	tcpwm[0].line[260]:3	csd.csd_tx:56	csd.csd_tx_n:56				smif.spi_data2			scb[5].spi_select1:0				peri.tr_io_output[1]:0				
P11.5	tcpwm[0].line_compl[0]:6	tcpwm[0].line_compl[260]:3	csd.csd_tx:57	csd.csd_tx_n:57				smif.spi_data1			scb[5].spi_select2:0								
P11.6	tcpwm[0].line[1]:6	tcpwm[0].line[261]:3	csd.csd_tx:58	csd.csd_tx_n:58				smif.spi_data0			scb[5].spi_select3:0								
P11.7	tcpwm[0].line_compl[1]:6	tcpwm[0].line_compl[261]:2	csd.csd_tx:59	csd.csd_tx_n:59				smif.spi_clk											
P12.6	tcpwm[0].line[3]:6	tcpwm[0].line[263]:3	csd.csd_tx:60	csd.csd_tx_n:60															
P12.7	tcpwm[0].line_compl[3]:6	tcpwm[0].line_compl[263]:3	csd.csd_tx:61	csd.csd_tx_n:61															

Analog and Smart I/O alternate port pin functionality is provided in **Table 7**.

Table 7 **Port Pin Analog, Digital, and Smart I/O functions**

Port/Pin	**Analog**
P0.0	wco_in
P0.1	wco_out
P5.6	lpcomp.inp_comp0
P5.7	lpcomp.inn_comp0
P6.2	lpcomp.inp_comp1
P6.3	lpcomp.inn_comp1
P6.6	swd_data
P6.7	swd_clk
P7.2	csd.csh_tank
P7.3	csd.vref_ext
P7.7	csd.shield
P9.5	aref_ext_vref
P10.0	sarmux_pads[0]
P10.1	sarmux_pads[1]
P10.2	sarmux_pads[2]
P10.3	sarmux_pads[3]
P10.4	sarmux_pads[4]
P10.5	sarmux_pads[5]
P10.6	sarmux_pads[6]
P10.7	sarmux_pads[7]
P12.6	eco_in
P12.7	eco_out
Port/Pin	**Digital**
P0.4	pmic_wakeup_in hibernate_wakeup[1]
P0.5	pmic_wakeup_out
P8.1 hibernate_wakeup[0]	hibernate_wakeup[0]
Port/Pin	**SMARTIO**
P9.0	smartio[9].io[0]
P9.1	smartio[9].io[1]
P9.2	smartio[9].io[2]
P9.3	smartio[9].io[3]
P9.4	smartio[9].io[4]
P9.5	smartio[9].io[5]

5 Power supply considerations

The following power system diagrams show typical connections for power pins for all supported packages. In these diagrams, the package pin is shown with the pin name, for example "V_{DDA}, 59". For V_{DDx} pins, the I/O port that is powered by that pin is also shown, for example "V_{BACKUP}, 3; I/O port P0".

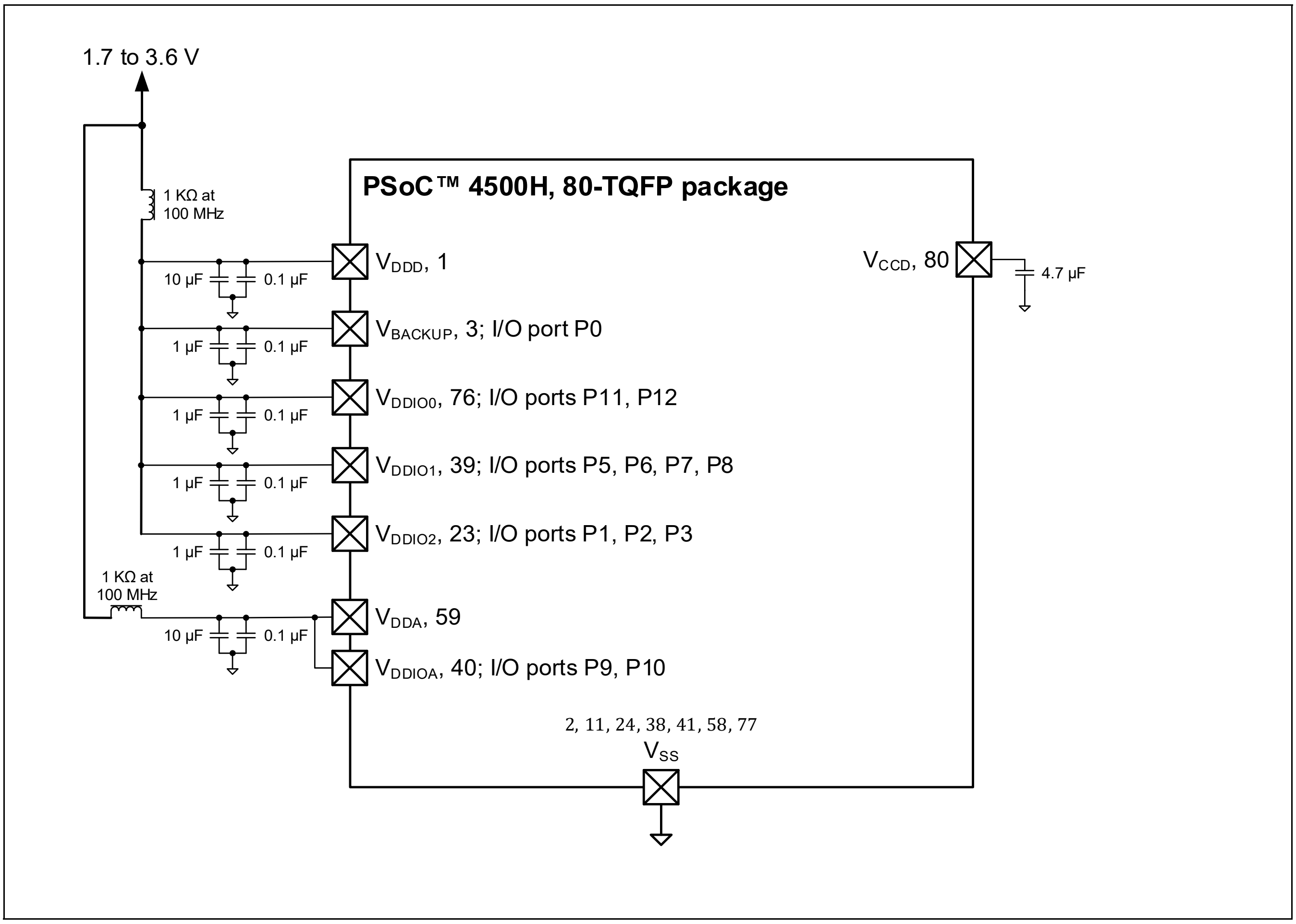


Figure 11 **80-TQFP power connection diagram**

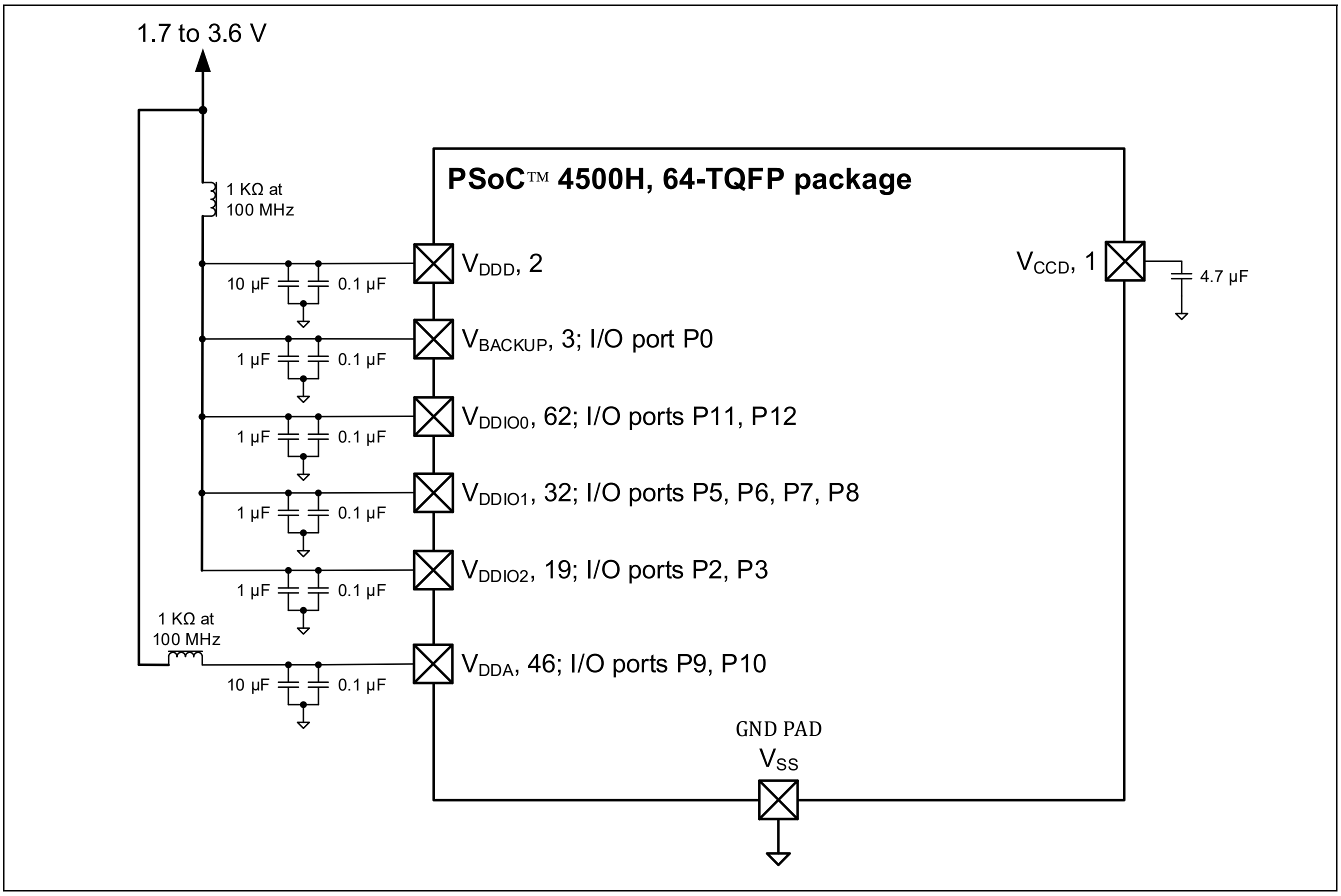


Figure 12 **64-TQFP power connection diagram**

There are as many as eight V_{DDx} supply pins, depending on the package, and multiple V_{SS} ground pins. The power pins are:

- V_{DDD}: the main digital supply.
- V_{CCD}: the main LDO output. It requires a 4.7-µF capacitor for regulation. For more information, see the power system block diagram in the device **technical reference manual (TRM)**.
- V_{DDA}: the supply for the analog peripherals. Voltage must be applied to this pin for correct device initialization and boot up.
- V_{DDIOA}: the supply for I/O ports 9 and 10. If it is present in the device package, it must be connected to V_{DDA}.
- V_{DDIO0}: the supply for I/O ports 11 and 12.
- V_{DDIO1}: the supply for I/O ports 5, 6, 7, and 8.
- V_{DDIO2}: the supply for I/O ports 1, 2, and 3.

- V_{BACKUP}: the supply for the backup domain, which includes the 32-kHz WCO and the RTC. It can be a separate supply as low as 1.4 V, for battery or supercapacitor backup, as **Figure 13** shows. otherwise it is connected to V_{DDD}. It powers I/O port 0.

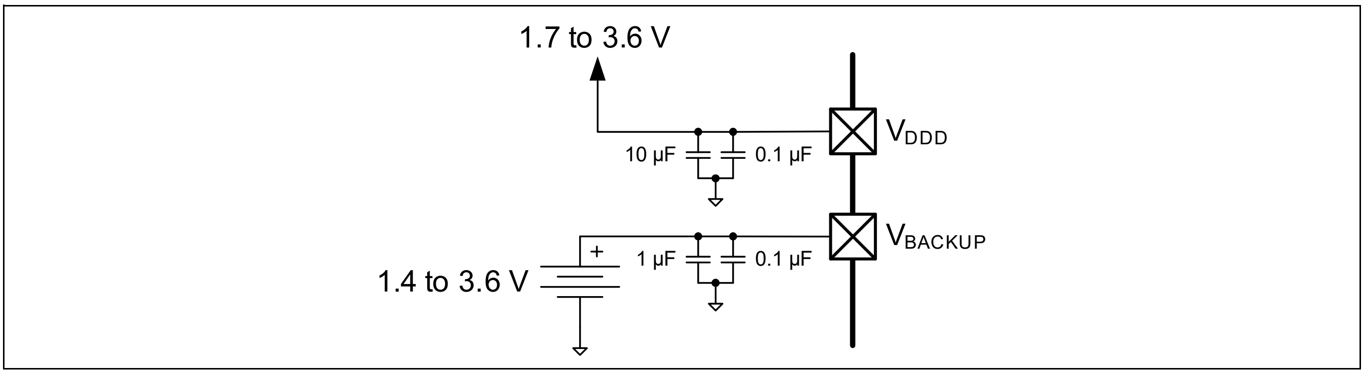


Figure 13 Separate Battery connection to V_{BACKUP}

Table 8 shows a summary of the I/O port supplies:

Table 8 I/O Port supplies

Port	Supply	Alternate supply
0	V_{BACKUP}	V_{DDD}
1,2, 3	V_{DDIO2}	–
5, 6, 7, 8	V_{DDIO1}	–
9, 10	V_{DDIOA}	V_{DDA}
11, 12	V_{DDIO0}	–

Voltage must be applied to the V_{DDD} pin, and the V_{DDA} pin as noted above, for correct device initialization and operation. If an I/O port is not being used, applying voltage to the corresponding V_{DDx} pin is optional.

- V_{SS}: ground pins for the above supplies. All ground pins should be connected together to a common ground.

The V_{DD} power pins are not connected together on chip. They can be connected off chip, in one or more separate nets. If separate power nets are used, they can be isolated from noise from the other nets using optional ferrite beads, as indicated in the diagrams.

No external load should be placed on V_{CCD}, or V_{IND1}, whether or not these pins are used.

There are no power pin sequencing requirements; power supplies may be brought up in any order. The power management system holds the device in reset until all power pins are at the voltage levels required for proper operation.

Note: If a battery is installed on the PCB first, V_{DDD} must be cycled for at least 50 µs. This prevents premature drain of the battery during product manufacture and storage.

Bypass capacitors must be connected to a common ground from the V_{DDx} and other pins, as indicated in the diagrams. Typical practice for systems in this frequency range is to use a 10-µF or 1-µF capacitor in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated for optimal bypassing.

All capacitors and inductors should be ±20% or better. The recommended inductor value is 2.2 µH ± 20% (for example, TDK MLP2012H2R2MT0S1).

It is good practice to check the datasheets for your bypass capacitors, specifically the working voltage and the DC bias specifications. With some capacitors, the actual capacitance can decrease considerably when the applied voltage is a significant percentage of the rated working voltage.

For more information on pad layout, refer to **PSOC™ 6 CAD libraries**.

6 Electrical specifications

All specifications are valid for –40°C ≤ T_A ≤ 85°C and for 1.71 V to 3.6 V except where noted.

6.1 Absolute maximum ratings

Table 9 Absolute maximum ratings[1]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID1	V_{DD_ABS}	Analog or digital supply relative to Vss ($V_{SSD} = V_{SSA}$)	–0.5	–	4	V	–
SID2	V_{CCD_ABS}	Direct digital core voltage input relative to Vssd	–0.5	–	1.2	V	–
SID3	V_{GPIO_ABS}	GPIO voltage; V_{DDD} or V_{DDA}	–0.5	–	V_{DD} + 0.5	V	–
SID4	I_{GPIO_ABS}	Current per GPIO	–25	–	25	mA	–
SID5	$I_{GPIO\_injection}$	GPIO injection current per pin	–0.5	–	0.5	mA	–
SID3A	ESD_HBM	Electrostatic discharge Human Body Model	2200	–	–	V	–
SID4A	ESD_CDM	Electrostatic discharge Charged Device Model	500	–	–	V	–
SID5A	LU	Pin current for latchup-free operation	–100	–	100	mA	–

Note

[1] Usage above the absolute maximum conditions listed in **Table 9** may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150°C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

6.2 Device-level specifications

Table 12 provides detailed specifications of CPU current. **Table 10** summarizes these specifications, for rapid review of CPU currents under common conditions. Note that the max frequency for CM4 is 150 MHz, and for CM0+ is 100 MHz. IMO and FLL are used to generate the CPU clocks; FLL is not used when the CPU clock frequency is 8 MHz.

Table 10 CPU Current specifications summary

Condition	Range	Typ range	Max range
LP Mode, V_{DDD} = 3.3 V, V_{CCD} = 1.1 V, with buck regulator			
CM4 active, CM0+ sleep	Across CPUs clock ranges: 8 MHz–150/100 MHz; Dhrystone with flash cache enabled	0.9 mA–6.9 mA	1.5 mA–8.6 mA
CM0+ active, CM4 sleep		0.8 mA–3.8 mA	1.3 mA–4.5 mA
CM4 sleep, CM0+ sleep		0.7 mA–1.5 mA	1.3 mA–2.2 mA
CM0+ sleep, CM4 off		0.7 mA–1.3 mA	1.3 mA–2 mA
Minimum regulator current mode	Across CM4/CM0+ CPU active/sleep modes	0.6 mA–0.7 mA	1.1 mA–1.1 mA
ULP Mode, V_{DDD} = 3.3 V, V_{CCD} = 0.9 V, with buck regulator			
CM4 active, CM0+ sleep	Across CPUs clock ranges: 8 MHz–50/25 MHz; Dhrystone with flash cache enabled	0.65 mA–1.6 mA	0.8 mA–2.2 mA
CM0+ active, CM4 sleep		0.51 mA–0.91 mA	0.72 mA–1.25 mA
CM4 sleep, CM0+ sleep		0.42 mA–0.76 mA	0.65 mA–1.1 mA
CM0+ sleep, CM4 off		0.41 mA–0.62 mA	0.6 mA–0.9 mA
Minimum regulator current mode	Across CM4/CM0+ CPU active/sleep modes	0.39 mA–0.54 mA	0.6 mA–0.76 mA
Deep Sleep	Across SRAM retention	7 µA–9 µA	–
Hibernate	Across V_{DDD}	300 nA–800 nA	–

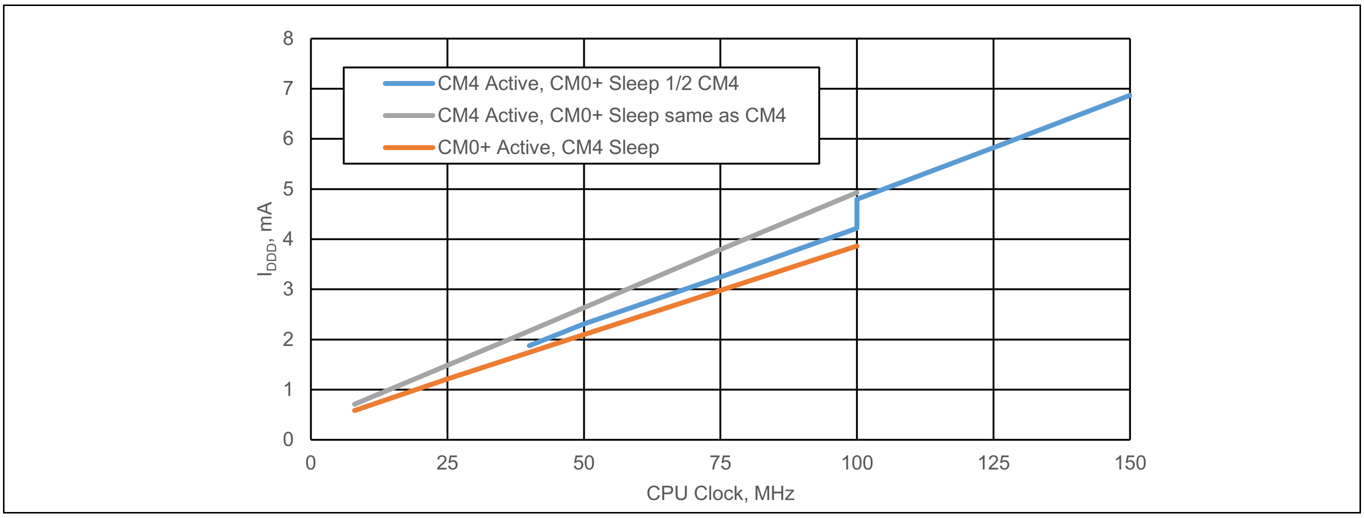


Figure 14 Typical device currents vs. CPU frequency; System low power (LP) mode[2]

Note

2. CM4 Active, CM0+ Sleep 1/2 CM4 trace values are higher because above 100 MHz, the PLL must be used instead of the FLL.

6.2.1 Power supplies

Table 11 Power supply DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID6	V_{DDD}	Internal regulator	1.7	–	3.6	V	–
SID7	V_{DDA}	Analog power supply voltage. Shorted to V_{DDIOA} on PCB	1.7	–	3.6	V	–
SID7A	V_{DDIO1}	GPIO supply for Ports 5 to 8 when present	1.7	–	3.6	V	Must be ≥ V_{DDA} if the CSD block is used in the application
SID7B	V_{DDIO0}	GPIO supply for Ports 11 and 12	1.7	–	3.6	V	–
SID7E	V_{DDIO0}	Supply when programming E-Fuse	2.38	2.5	2.62	V	eFuse programming voltage
SID7EI	$I_{DDEFUSE}$	eFuse programming current	–	–	14	mA	–
SID7EP	EFUSETIME	eFuse programming time	–	–	5	µs	–
SID7C	V_{DDIO2}	GPIO supply for Ports 1 to 3 when present	1.7	–	3.6	V	–
SID7D	V_{DDIOA}	GPIO supply for Ports 9 and 10 when present. Must be connected to V_{DDA} on PCB.	1.7	–	3.6	V	–
SID6B	V_{BACKUP}	Backup power; normally shorted to V_{DDD}	1.7	–	3.6	V	Min is 1.4 V in Backup mode
SID8	V_{CCD} (LP)	Output voltage (for core logic bypass)	–	1.1	–	V	System LP mode
SID9	V_{CCD} (ULP)	Output voltage (for core logic bypass)	–	0.9	–		ULP mode. Valid for –20°C to 85°C.
SID10	C_{EFC}	External regulator voltage (V_{CCD}) bypass	3.8	4.7	5.6	µF	X5R ceramic or better. Value for 0.8 V to 1.2 V.
SID11	C_{EXC}	Power supply decoupling capacitor	–	10	–	µF	X5R ceramic or better

6.2.2 CPU current and transition times

Table 12 CPU current and transition specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
LP range power specifications (for V_{CCD} = 1.1 V)							
Cortex® M4. Active Mode							
Execute with Cache Disabled (Flash)							
SIDF1	I_{DD1}	Execute from Flash; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL. While(1).	–	5.7	6.5	mA	V_{DDD} = 1.8 to 3.3 V, max at 85 °C
SIDF2	I_{DD2}	Execute from Flash; CM4 Active 8 MHz, CM0+ Sleep 8 MHz.With IMO. While(1)	–	2.8	3.5	mA	V_{DDD} = 1.8 to 3.3 V, max at 85 °C
Execute with Cache Enabled							
SIDC1	I_{DD3}	Execute from Cache;CM4 Active 150 MHz, CM0+ Sleep 75 MHz. IMO & PLL. Dhrystone.	–	14.4	15.1	mA	V_{DDD} = 1.8 to 3.3 V, max at 85 °C
SIDC2	I_{DD4}	Execute from Cache;CM4 Active100 MHz, CM0+ Sleep 100 MHz. IMO & FLL. Dhrystone.	–	11.3	12	mA	V_{DDD} = 1.8 to 3.3 V, max at 85 °C
SIDC3	I_{DD5}	Execute from Cache;CM4 Active 50 MHz, CM0+ Sleep 25MHz. IMO & FLL. Dhrystone	–	6.3	7.2	mA	V_{DDD} = 1.8 to 3.3 V, max at 85 °C
SIDC4	IDD6	Execute from Cache;CM4 Active 8 MHz, CM0+ Sleep 8 MHz. IMO. Dhrystone	–	3	3.8	mA	V_{DDD} = 1.8 to 3.3 V, max at 85 °C
Cortex® M0+. Active Mode							
Execute with Cache Disabled (Flash)							
SIDF3	IDD7	Execute from Flash;CM4 Off, CM0+ Active 50 MHz. With IMO & FLL. While (1).	–	5.6	6.3	mA	V_{DDD} = 1.8 to 3.3 V, max at 85 °C
SIDF4	IDD8	Execute from Flash;CM4 Off, CM0+ Active 8 MHz. With IMO. While (1)	–	2.6	3.4	mA	V_{DDD} = 1.8 to 3.3 V, max at 85 °C
Execute with Cache Enabled							
SIDC5	IDD9	Execute from Cache;CM4 Off, CM0+ Active 100 MHz. With IMO & FLL. Dhrystone.	–	9	9.7	mA	V_{DDD} = 1.8 to 3.3 V, max at 85 °C
SIDC6	IDD10	Execute from Cache;CM4 Off, CM0+ Active 8 MHz. With IMO. Dhrystone	–	2.60	3.4	mA	V_{DDD} = 1.8 to 3.3 V, max at 85 °C
Cortex® M4. Sleep Mode							
SIDS1	IDD11	CM4 Sleep 100 MHz, CM0+ Sleep 25 MHz. With IMO & FLL.	–	4	4.6	mA	V_{DDD} = 1.8 to 3.3 V, max at 85 °C
SIDS2	IDD12	CM4 Sleep 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL	–	3.4	4.3	mA	V_{DDD} = 1.8 to 3.3 V, max at 85 °C
SIDS3	IDD13	CM4 Sleep 8 MHz, CM0+ Sleep 8 MHz. With IMO.	–	2.4	3.3	mA	V_{DDD} = 1.8 to 3.3 V, max at 85 °C
Cortex® M0+. Sleep Mode							
SIDS4	IDD14	CM4 Off, CM0+ Sleep 50 MHz. With IMO & FLL.	–	3.8	4.6	mA	V_{DDD} = 1.8 to 3.3 V, max at 85 °C
SIDS5	IDD15	CM4 Off, CM0+ Sleep 8 MHz. With IMO.	–	2.4	3.3	mA	V_{DDD} = 1.8 to 3.3 V, max at 85 °C

Table 12 **CPU current and transition specifications** *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
Cortex® M4. Minimum Regulator Current Mode							
SIDLPA1	IDD16	Execute from Flash; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. While (1).	–	2.8	3.5	mA	V_{DDD} = 1.8 to 3.3 V, max at 85 °C
SIDLPA2	IDD17	Execute from Cache; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. Dhrystone.	–	2.9	3.7	mA	V_{DDD} = 1.8 to 3.3 V, max at 85 °C
Cortex® M0+. Minimum Regulator Current Mode							
SIDLPA3	IDD18	Execute from Flash; CM4 Off, CM0+ Active 8 MHz. With IMO. While (1)	–	2.7	3.6	mA	V_{DDD} = 1.8 to 3.3 V, max at 85 °C
SIDLPA4	IDD19	Execute from Cache; CM4 Off, CM0+ Active 8 MHz. With IMO. Dhrystone.	–	2.7	3.6	mA	V_{DDD} = 1.8 to 3.3 V, max at 85 °C
Cortex® M4. Minimum Regulator Current Mode							
SIDLPS1	IDD20	CM4 Sleep 8 MHz, CM0+ Sleep 8 MHz. With IMO.	–	2.4	3.3	mA	V_{DDD} = 1.8 to 3.3 V, max at 85 °C
Cortex® M0+. Minimum Regulator Current Mode							
SIDLPS3	IDD22	CM4 Off, CM0+ Sleep 8 MHz. With IMO.	–	2.4	3.3	mA	V_{DDD} = 1.8 to 3.3 V, max at 85 °C
Hibernate Mode							
SIDHIB1	IDD34	V_{DDD} = 1.8 V	–	300	–	nA	No clocks running
SIDHIB2	IDD34A	V_{DDD} = 3.3 V	–	1400	–	nA	No clocks running
Power Mode Transition Times							
SID12	T_{LPACT_ACT}	Minimum Regulator Current to LP transition time	–	–	35	µs	Including PLL lock time
SID13	T_{DS_LPACT}	Deep Sleep to LP transition time.	–	–	17	µs	Guaranteed by design
SID14	T_{HIB_ACT}	Hibernate to Active transition time including Boot process.	–	900	–	µs	Including PLL lock time

6.2.3 XRES

Table 13 XRES DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID17	T_{XRES_IDD}	I_{DD} when XRES asserted	–	300	–	nA	V_{DDD} = 1.8 V
SID17A	$T_{XRES\_IDD\_1}$	I_{DD} when XRES asserted	–	1400	–	nA	V_{DDD} = 3.3 V
SID77	V_{IH}	Input voltage HIGH threshold	0.7 × V_{DD}	–	–	V	CMOS input
SID78	V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DD}	V	CMOS input
SID80	C_{IN}	Input capacitance	–	3	–	pF	–
SID81	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	–
SID82	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	–

Table 14 XRES AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID15	T_{XRES_ACT}	Time from XRES release to Active mode including Boot process	–	900	–	µs	Not minimum regulator current mode; Cortex®-M0+ executing at 50 MHz
SID16	T_{XRES_PW}	XRES pulse width	5	–	–	µs	–

6.2.4 GPIO

Table 15 GPIO DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID57	V_{IH}	Input voltage HIGH threshold	0.7 × V_{DD}	–	–	V	CMOS Input
SID57A	I_{IHS}	Input current when Pad > V_{DDIO} for OVT inputs	–	–	10	µA	Per I^2C spec
SID58	V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DD}	V	CMOS Input
SID241	V_{IH}	LVTTL input, V_{DD} < 2.7 V	0.7 × V_{DD}	–	–	V	–
SID242	V_{IL}	LVTTL input, V_{DD} < 2.7 V	–	–	0.3 × V_{DD}	V	–
SID243	V_{IH}	LVTTL input, V_{DD} ≥ 2.7 V	2.0	–	–	V	–
SID244	V_{IL}	LVTTL input, V_{DD} ≥ 2.7 V	–	–	0.8	V	–
SID59	V_{OH}	Output voltage HIGH level	V_{DD} – 0.5	–	–	V	I_{OH} = 8 mA
SID62A	V_{OL}	Output voltage LOW level	–	–	0.4	V	I_{OL} = 8 mA
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	–
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25°C, V_{DD} = 3.0 V
SID65A	I_{IL_CTBM}	Input leakage on CTBm input pins	–	–	4	nA	–
SID66	C_{IN}	Input capacitance	–	–	5	pF	–
SID67	V_{HYSTTL}	Input hysteresis LVTTL V_{DD} > 2.7 V	100	0	–	mV	–
SID68	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DD}	–	–	mV	–
SID69	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	–
SID69A	I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	200	mA	–

Table 16 GPIO AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID70	T_{RISEF}	Rise time in Fast Strong Mode. 10% to 90% of V_{DD}.	–	–	2.5	ns	Cload = 15 pF, 8-mA drive strength
SID71	T_{FALLF}	Fall time in Fast Strong Mode. 10% to 90% of V_{DD}.	–	–	2.5	ns	Cload = 15 pF, 8-mA drive strength
SID72	T_{RISES_1}	Rise time in Slow Strong Mode. 10% to 90% of V_{DD}.	52	–	142	ns	Cload = 15 pF, 8-mA drive strength, $V_{DD} \leq 2.7$ V
SID72A	T_{RISES_2}	Rise time in Slow Strong Mode. 10% to 90% of V_{DD}.	48	–	102	ns	Cload = 15 pF, 8-mA drive strength, 2.7 V < $V_{DD} \leq 3.6$ V
SID73	T_{FALLS_1}	Fall time in Slow Strong Mode. 10% to 90% of V_{DD}.	44	–	211	ns	Cload = 15 pF, 8-mA drive strength, $V_{DD} \leq 2.7$ V
SID73A	T_{FALLS_2}	Fall time in Slow Strong Mode. 10% to 90% of V_{DD}.	42	–	93	ns	Cload = 15 pF, 8-mA drive strength, 2.7 V < $V_{DD} \leq 3.6$ V
SID73G	T_{FALL_I2C}	Fall time (30% to 70% of V_{DD}) in Slow Strong mode.	20 × (V_{DDIO} / 5.5)	–	250	ns	Cload = 10 pF to 400 pF, 8-mA drive strength
SID74	$F_{GPIOUT1}$	GPIO Fout. Fast Strong mode.	–	–	100	MHz	90/10%, 15-pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO Fout; Slow Strong mode.	–	–	16.7	MHz	90/10%, 15-pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO Fout; Fast Strong mode.	–	–	7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID245	$F_{GPIOUT4}$	GPIO Fout; Slow Strong mode.	–	–	3.5	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency; 1.71 V $\leq V_{DD} \leq$ 3.6 V	–	–	100	MHz	90/10% V_{IO}

6.3 Analog Peripherals

6.3.1 Opamp

Table 17 Opamp specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
	I_{DD}	Opamp block current. No load.	–	–	–	–	Overvoltage and temp (–40/105°C) unless stated otherwise
SID269	I_{DD_HI}	power = hi	–	1300	1500	µA	–
SID270	I_{DD_MED}	power = med	–	450	600	µA	–
SID271	I_{DD_LOW}	power = lo	–	250	350	µA	–
	GBW	Load = 20 pF, 0.1mA. V_{DDA} = 2.7 V	–	–	–	–	–
SID272	GBW_HI	power = hi	6	–	–	MHz	–
SID273	GBW_MED	power = med	2	–	–	MHz	–
SID274	GBW_LO	power = lo	–	1	–	MHz	–
	I_{OUT_MAX}	V_{DDA} ≥ 2.7 V, 500 mV from rail	–	–	–	–	–
SID275	$I_{OUT\_MAX\_HI}$	power = hi	10	–	–	mA	–
SID276	$I_{OUT\_MAX\_MID}$	power = med	10	–	–	mA	–
SID277	$I_{OUT\_MAX\_LO}$	power = lo	–	5	–	mA	–
	I_{OUT}	V_{DDA} = 1.7 V, 500 mV from rail	–	–	–	–	–
SID278	$I_{OUT\_MAX\_HI}$	power = hi	4	–	–	mA	–
SID279	$I_{OUT\_MAX\_MID}$	power = med	4	–	–	mA	–
SID280	$I_{OUT\_MAX\_LO}$	power = lo	–	2	–	mA	–
SID281	V_{IN}	Input voltage range	0	–	V_{DDA} – 0.2	V	Charge pump ON
SID282	V_{CM}	Input common mode voltage	0	–	V_{DDA} – 0.2	V	Charge pump OFF, V_{DDA} ≥ 2.7 V
	V_{OUT}	V_{DDA} ≥ 2.7 V	–	–	–	–	–
SID283	V_{OUT_1}	power = hi, Iload = 10 mA	0.5	–	V_{DDA} – 0.5	V	–
SID284	V_{OUT_2}	power = hi, Iload = 1 mA	0.2	–	V_{DDA} – 0.2	V	–
SID285	V_{OUT_3}	power = med, Iload = 1 mA	0.2	–	V_{DDA} – 0.2	V	–
SID286	V_{OUT_4}	power = lo, Iload = 0.1 mA	0.2	–	V_{DDA} – 0.2	V	–
SID288	V_{OS}	Offset voltage. Closed loop configuration.	–1	+/–0.5	1	mV	High mode, 0.2 to V_{DDA} - 0.2
SID288A	V_{OS}	Offset voltage	–	+/–1	–	mV	Medium mode
SID288B	V_{OS}	Offset voltage	–	+/–2	–	mV	Low mode

Table 17 Opamp specifications *(continued)*

Spec ID#	**Parameter**	**Description**	**Min**	**Typ**	**Max**	**Units**	**Details/conditions**
SID290	V_{OS_DR}	Offset voltage drift	–10	+/–3	10	µV/°C	High mode, 0.2 to V_{DDA} – 0.2
SID290A	V_{OS_DR}	Offset voltage drift	–	+/–10	–	µV/°C	Medium mode
SID290B	V_{OS_DR}	Offset voltage drift	–	+/–10	–	µV/C	Low mode
SID291	CMRR	DC Common mode rejection ratio	67	80	–	dB	V_{DDD} = 3.3 V. Vin = 0.2 to V_{DDA} – 0.2.
SID292	PSRR	Power supply rejection ratio at 1 kHz, 10 mV ripple	70	85	–	dB	V_{DDD} = 3.3 V. Vin = $V_{DDA/2}$.
Noise							
SID293	VN1	Input-referred, 1 Hz–1 GHz, power = hi	–	100	–	µVrms	Guaranteed by design
SID294	VN2	Input-referred, 1 kHz, power = hi	–	180	–	nV/rtHz	Guaranteed by design
SID295	VN3	Input-referred, 10 kHz, power = hi	–	70	–	nV/rtHz	Guaranteed by design
SID296	VN4	Input-referred, 100 kHz, power = hi	–	38	–	nV/rtHz	Guaranteed by design
SID297	CLOAD	Stable up to max load. Performance specs at 50 pF.	–	–	125	pF	High and medium
SID298	SLEW_RATE	Output slew rate	4	–	–	V/µs	Cload = 50pF, Power = High, V_{DDA} ≥ 2.7 V. Refer to **Figure 15** and **Figure 16**.
SID299	T_OP_WAKE	From disable to enable, no external RC dominating	–	–	10	µs	For V_{DDA} ≥ 2.7 V
	COMP_MODE	Comparator mode; 50 mV overdrive.	–	–	–	–	–
SID300	TPD1	Response time; power = hi	–	150	–	ns	–
SID301	TPD2	Response time; power = med	–	400	–	ns	–
SID302	TPD3	Response time; power = lo	–	2000	–	ns	–
SID303	V_{HYST_OP}	Hysteresis	–	10	–	mV	–

Table 17 **Opamp specifications** *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
Deep Sleep Mode		Mode 2 is lowest current range. Mode 1 has higher GBW.	–	–	–	–	Deep Sleep mode operation: $V_{DDA} \geq 2.7$ V. V_{IN} is 0.2 to $V_{DDA} - 1.5$ V.
SID_DS_1	IDD_HI_M1	Mode 1, High current	–	1300	1500	µA	Typ at 25°C
SID_DS_2	IDD_MED_M1	Mode 1, Medium current	–	460	600	µA	Typ at 25°C
SID_DS_3	IDD_LOW_M1	Mode 1, Low current	–	230	350	µA	Typ at 25°C
SID_DS_4	IDD_HI_M2	Mode 2, High current	–	100	–	µA	25°C
SID_DS_5	IDD_MED_M2	Mode 2, Medium current	–	40	–	µA	25°C
SID_DS_6	IDD_LOW_M2	Mode 2, Low current	–	15	–	µA	25°C
SID_DS_7	GBW_HI_M1	Mode 1, High current	–	4	–	MHz	25°C
SID_DS_8	GBW_MED_M1	Mode 1, Medium current	–	2	–	MHz	25°C
SID_DS_9	GBW_LOW_M1	Mode 1, Low current	–	0.5	–	MHz	25°C
SID_DS_10	GBW_HI_M2	Mode 2, High current	–	0.5	–	MHz	20-pF load, no DC load 0.2 V to $V_{DDA} - 1.5$ V
SID_DS_11	GBW_MED_M2	Mode 2, Medium current	–	0.2	–	MHz	20-pF load, no DC load 0.2 V to $V_{DDA} - 1.5$ V
SID_DS_12	GBW_LOW_M2	Mode 2, Low current	–	0.1	–	MHz	20-pF load, no DC load 0.2 V to $V_{DDA} - 1.5$ V
SID_DS_13	VOS_HI_M1	Mode 1, High current	–	5	–	mV	0.2 V to $V_{DDA} - 1.5$ V
SID_DS_14	VOS_MED_M1	Mode 1, Medium current	–	5	–	mV	0.2 V to $V_{DDA} - 1.5$ V
SID_DS_15	VOS_LOW_M1	Mode 1, Low current	–	5	–	mV	0.2 V to $V_{DDA} - 1.5$ V
SID_DS_16	VOS_HI_M2	Mode 2, High current	–	5	–	mV	0.2 V to $V_{DDA} - 1.5$ V
SID_DS_17	VOS_MED_M2	Mode 2, Medium current	–	5	–	mV	0.2 V to $V_{DDA} - 1.5$ V
SID_DS_18	VOS_LOW_M2	Mode 2, Low current	–	5	–	mV	0.2 V to $V_{DDA} - 1.5$ V
SID_DS_19	IOUT_HI_M1	Mode 1, High current	–	10	–	mA	Output is 0.5 V to $V_{DDA} - 0.5$ V

Table 17 Opamp specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID_DS_20	IOUT_MED_M1	Mode 1, Medium current	–	10	–	mA	Output is 0.5 V to V_{DDA} – 0.5 V
SID_DS_21	IOUT_LOW_M1	Mode 1, Low current	–	4	–	mA	Output is 0.5 V to V_{DDA} – 0.5 V
SID_DS_22	IOUT_HI_M2	Mode 2, High current	–	1	–	mA	Output is 0.5 V to V_{DDA} – 0.5 V
SID_DS_23	IOU_MED_M2	Mode 2, Medium current	–	1	–	mA	Output is 0.5 V to V_{DDA} – 0.5 V
SID_DS_24	IOU_LOW_M2	Mode 2, Low current	–	0.5	–	mA	Output is 0.5 V to V_{DDA} – 0.5 V

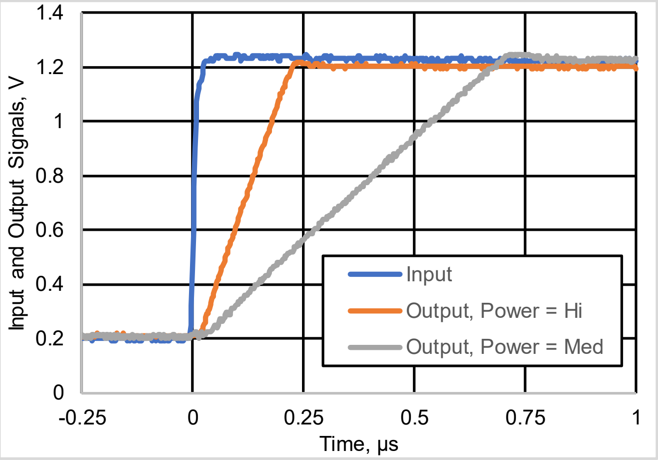


Figure 15 Opamp step response, rising

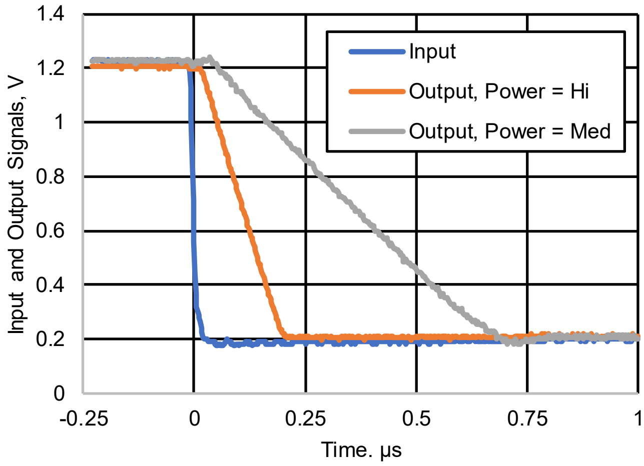


Figure 16 Opamp step response, falling

6.3.2 Low-power (LP) comparator

Table 18 LP comparator DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID84	$V_{OFFSET1}$	Input offset voltage for COMP. Normal power mode.	–10	–	10	mV	–
SID85A	$V_{OFFSET2}$	Input offset voltage. Low-power mode.	–25	±12	25	mV	–
SID85B	$V_{OFFSET3}$	Input offset voltage. Ultra low-power mode.	–25	±12	25	mV	–
SID86	V_{HYST1}	Hysteresis when enabled in Normal mode	–	–	60	mV	–
SID86A	V_{HYST2}	Hysteresis when enabled in Low-power mode	–	–	80	mV	–
SID87	V_{ICM1}	Input common mode voltage in Normal mode	0	–	V_{DDIO1} – 0.1	V	–
SID247	V_{ICM2}	Input common mode voltage in Low power mode	0	–	V_{DDIO1} – 0.1	V	–
SID247A	V_{ICM3}	Input common mode voltage in Ultra low power mode	0	–	V_{DDIO1} – 0.1	V	–
SID88	CMRR	Common mode rejection ratio in Normal power mode	50	–	–	dB	–
SID89	I_{CMP1}	Block current, Normal mode	–	–	150	µA	–
SID248	I_{CMP2}	Block current, Low-power mode	–	–	10	µA	–
SID259	I_{CMP3}	Block current in Ultra low-power mode	–	0.3	0.85	µA	–
SID90	ZCMP	DC input impedance of comparator	35	–	–	MΩ	–

Table 19 LP comparator AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID91	T_{RESP1}	Response time, Normal mode, 100 mV overdrive	–	–	100	ns	–
SID258	T_{RESP2}	Response time, Low power mode, 100 mV overdrive	–	–	1000	ns	–
SID92	T_{RESP3}	Response time, Ultra-low power mode, 100 mV overdrive	–	–	20	µs	–
SID92E	T_CMP_EN1	Time from Enabling to operation	–	–	10	µs	Normal and low-power modes
SID92F	T_CMP_EN2	Time from Enabling to operation	–	–	50	µs	Ultra-low-power mode

6.3.3 Temperature sensor

Table 20 Temperature sensor specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID93	$T_{SENSACC}$	Temperature sensor accuracy	–5	±1	5	°C	–40°C to +105°C

6.3.4 Internal reference

Table 21 Internal reference specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID93R	V_{REFBG}	–	1.188	1.2	1.212	V	–

6.3.5 SAR ADC

Table 22 SAR ADC DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID94	A_RES	SAR ADC resolution	–	–	12	bits	–
SID95	A_CHNLS_S	Number of channels - single-ended	–	–	16	–	8 full speed.
SID96	A-CHNKS_D	Number of channels - differential	–	–	8	–	Diff inputs use neighboring I/O.
SID97	A-MONO	Monotonicity	–	–	–	–	Yes
SID98	A_GAINERR	Gain error	–	–	±0.2	%	With external reference.
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V reference.
SID100	A_ISAR_1	Current consumption at 1 Msps	–	–	1.05	mA	At 1 Msps. External reference mode.
SID100A	A_ISAR_2	Current consumption at 1 Msps	–	–	1.3	mA	At 1 Msps. Internal reference mode.
SID1002	A_ISAR_3	Current consumption at 2 Msps	–	–	1.65	mA	At 2 Msps. External reference mode.
SID1003	A_ISAR_4	Current consumption at 2 Msps	–	–	2.15	mA	At 2 Msps. Internal reference mode.
SID101	A_VINS	Input voltage range - single-ended	V_{SS}	–	V_{DDA}	V	–
SID102	A_VIND	Input voltage range - differential	V_{SS}	–	V_{DDA}	V	–
SID103	A_INRES	Input resistance	–	1	–	kΩ	–
SID104	A_INCAP	Input capacitance	–	5	–	pF	–
SAR in Deep Sleep Mode V_{DDA} = 2.7 V. 2-MHz LPOSC and duty-cycled.							
SIDP121	IDD_CHIP_1	Chip current consumption for 12 bits, 100 ksps Deep Sleep Mode	–	320	–	µA	–
SIDP122	IDD_CHIP_2	Chip current consumption for 12 bits, 500 sps, duty cycle in Deep Sleep Mode	–	16	–	µA	–
SIDP123	IDD_CHIP_3	Chip Current Consumption for 10 bits (10% power mode), 16 ksps Deep Sleep Mode	–	150	–	µA	–
SIDP124	INL_10bits	Integral non-linearity for 10 bits (10% power mode) mode (V_{DDA} ≥ 2.7 V)	–2	–	2	LSB	–

Table 22 SAR ADC DC specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SIDP125	DNL_10bits	Differential non-linearity for 10 bits (10% power mode) mode (V_{DDA} ≥ 2.7 V)	–1	–	1	LSB	–
SIDP126	Vos_10bits	Offset for 10 bits (10% power mode) mode (V_{DDA} ≥ 2.7 V)	–2	–	2	LSB	–
SIDP127	GE_10bits	Gain Error for 10 bits (10% power mode) mode (V_{DDA} ≥ 2.7 V, V_{REF} = 1.2 V bypassed with external cap)	–1	–	1	LSB	–

Table 23 SAR ADC AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID106	A_PSRR	Power supply rejection ratio	70	–	–	dB	–
SID107	A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V.
SID107A	EXT_REF_1	External reference range	1	–	V_{DDA}	V	1 Msps sample rate and below.
SDI107B	Ext_REF_2	External reference range	2	–	V_{DDA}	V	> 1 and up to 2 Msps sample rates
SID1081	A_SAMP_1	Sample rate with external reference; With bypass cap	–	–	2	Msps	V_{DDA} 2.7 V–3.6 V
SID1082	A_SAMP_1	Sample rate with external reference; With bypass cap	–	–	1	Msps	V_{DDA} 1.7 V–3.6 V
SID108A1	A_SAMP_2	Sample rate with V_{DD} Reference; No bypass cap	–	–	2	Msps	V_{DDA} 2.7 V–3.6 V
SID108A2	A_SAMP_2	Sample rate with V_{DD} Reference; No bypass cap	–	–	1	Msps	V_{DDA} 1.7 V–3.6 V
SID108B	A_SAMP_3	Sample rate with Internal reference; With bypass cap	–	–	1	Msps	–
SID108C	A_SAMP_4	Sample rate with internal reference; No bypass cap	–	–	200	ksps	–
SID109	A_SINAD	Signal-to-noise and distortion ratio (SINAD).	64	–	–	dB	Fin = 10 kHz
SID111A	A_INL	Integral non-linearity. Up to 1 Msps	–2	–	2	LSB	All reference mode
SID111B	A_INL	Integral non-linearity. 2 Msps.	–2.5	–	2.5	LSB	External reference or V_{DDA} Reference Mode, V_{REF} ≥ 2 V. V_{DDA} = 2.7 V–3.6 V.

Table 23 **SAR ADC AC specifications** *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID112A	A_DNL	Differential non-linearity. Up to 1 Msps	–1	–	1.5	LSB	All Reference Mode
SID112B	A_DNL	Differential non-linearity. 2 Msps.	–1	–	1.6	LSB	External Reference or V_{DDA} Reference Mode, $V_{REF} \geq 2$ V. V_{DDA} = 2.7 V–3.6 V.
SID113	A_THD	Total harmonic distortion. 1 Msps.	–	–	–65	dB	Fin = 10 kHz. V_{DDA} = 2.7 V–3.6 V.
Both SARs with simultaneous sampling. Fclk = 18 MHz, Data Rate = 1 Msps; $V_{DDA} \geq 2.7$ V; Internal Ref. with Bypass Cap. Simultaneous sampling spec assume the same clock source is used for both SAR ADCs.							
SIDP131	INL	Integral Non Linearity ($V_{DDA} \geq 2.7$ V)	–2	–	2	LSB	–
SIDP132	DNL	Differential Non Linearity ($V_{DDA} \geq 2.7$ V)	–1	–	1	LSB	–
SIDP133	Vos	Offset ($V_{DDA} \geq 2.7$ V)	–2	–	2	LSB	–
SIDP134	GE	Gain Error ($V_{DDA} \geq 2.7$ V, VREF = 1.2 V bypassed with external Cap)	–1	–	1	LSB	–
Both SARs internal op amp buffered with simultaneous sampling VDDA reference. Fclk = 18 MHz, Data Rate = 1 Msps; $V_{DDA} \geq 2.7$ V; $V_{REF} \geq 2$ V. Simultaneous sampling spec assume the same clock source is used for both SAR ADCs.							
SIDP141	INL	Integral Non Linearity ($V_{DDA} \geq 2.7$ V)	–3	–	3	LSB	–
SIDP142	DNL	Differential Non Linearity ($V_{DDA} \geq 2.7$ V)	–1	–	2	LSB	–
SIDP143	Vos	Offset ($V_{DDA} \geq 2.7$ V)	–3	–	3	LSB	–
SIDP144	GE	Gain Error ($V_{DDA} \geq 2.7$V, V_{REF} = 1.2 V bypassed with external Cap)	–1	–	1	LSB	–

6.3.6 DAC

Table 24 12-bit DAC DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID108D	DAC_RES	DAC resolution	–	–	12	bits	
SID111D	DAC_INL	Integral Non-Linearity	–4	–	4	LSB	
SID112D	DAC_DNL	Differential Non Linearity	–2	–	2	LSB	Monotonic to 11 bits.
SID99D	DAC_OFFSET	Output Voltage zero offset error	–10	–	10	mV	For 000 (hex)
SID103D	DAC_OUT_RES	DAC Output Resistance	–	15	–	kΩ	
SID100D	DAC_IDD	DAC Current	–	–	125	µA	
SID101D	DAC_QIDD	DAC Current when DAC stopped	–	–	1	µA	

Table 25 12-bit DAC AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID109D	DAC_CONV	DAC Settling time	–	–	2	µs	Driving through CTBM buffer; 25 pF load
SID110D	DAC_Wakeup	Time from Enabling to ready for conversion	–	–	10	µs	

6.3.7 CSD

Table 26 CSD V2 specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
CSD V2 specifications							
SYS.PER#3	V_{DD_RIPPLE}	Max allowed ripple on power supply, DC to 10 MHz	–	–	±50	mV	V_{DDA} > 2 V (with ripple), 25°C T_A, Sensitivity = 0.1 pF.
SYS.PER#16	$V_{DD\_RIPPLE\_1.8}$	Max allowed ripple on power supply, DC to 10 MHz	–	–	±25	mV	V_{DDA} > 1.75 V (with ripple), 25°C T_A, Parasitic Capacitance (C_P) < 20 pF, Sensitivity ≥ 0.4 pF.
SID.CSD.BLK	I_{CSD}	Maximum block current	–	–	4500	µA	–
SID.CSD#15	V_{REF}	Voltage reference for CSD and Comparator	0.6	1.2	V_{DDA} – 0.6	V	$V_{DDA} – V_{REF} ≥ 0.6$ V
SID.CSD#15A	V_{REF_EXT}	External Voltage reference for CSD and Comparator	0.6		V_{DDA} – 0.6	V	$V_{DDA} – V_{REF} ≥ 0.6$ V
SID.CSD#16	$I_{DAC1IDD}$	IDAC1 (7-bits) block current	–	–	1900	µA	–
SID.CSD#17	$I_{DAC2IDD}$	IDAC2 (7-bits) block current	–	–	1900	µA	–
SID308	V_{CSD}	Voltage range of operation	1.7	–	3.6	V	1.71 V to 3.6 V
SID308A	$V_{COMPIDAC}$	Voltage compliance range of IDAC	0.6	–	V_{DDA} – 0.6	V	$V_{DDA} – V_{REF} ≥ 0.6$ V
SID309	$I_{DAC1DNL}$	DNL	–1	–	1	LSB	–
SID310	$I_{DAC1INL}$	INL	–3	–	3	LSB	If V_{DDA} < 2 V then for LSB of 2.4 µA or less.
SID311	$I_{DAC2DNL}$	DNL	–1	–	1	LSB	–
SID312	$I_{DAC2INL}$	INL	–3	–	3	LSB	If V_{DDA} < 2 V then for LSB of 2.4 µA or less.
SNRC of the following is Ratio of counts of finger to noise. Guaranteed by characterization.							
SID313_1A	SNRC_1	SRSS Reference. IMO + FLL Clock Source. 0.1-pF sensitivity.	5	–	–	Ratio	9.5-pF max. capacitance
SID313_1B	SNRC_2	SRSS Reference. IMO + FLL Clock Source. 0.3-pF sensitivity.	5	–	–	Ratio	31-pF max. capacitance
SID313_1C	SNRC_3	SRSS Reference. IMO + FLL Clock Source. 0.6-pF sensitivity.	5	–	–	Ratio	61-pF max. capacitance

Table 26 **CSD V2 specifications** *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID313_2A	SNRC_4	PASS Reference. IMO + FLL Clock Source. 0.1-pF sensitivity.	5	–	–	Ratio	12-pF max. capacitance
SID313_2B	SNRC_5	PASS Reference. IMO + FLL Clock Source. 0.3-pF sensitivity.	5	–	–	Ratio	47-pF max. capacitance
SID313_2C	SNRC_6	PASS Reference. IMO + FLL Clock Source. 0.6-pF sensitivity.	5	–	–	Ratio	86-pF max. capacitance
SID313_3A	SNRC_7	PASS Reference. IMO + PLL Clock Source. 0.1-pF sensitivity.	5	–	–	Ratio	25-pF max. capacitance
SID313_3B	SNRC_8	PASS Reference. IMO + PLL Clock Source. 0.3-pF sensitivity.	5	–	–	Ratio	86-pF max. capacitance
SID313_3C	SNRC_9	PASS Reference. IMO + PLL Clock Source. 0.6-pF sensitivity.	5	–	–	Ratio	168-pF Max. capacitance
SID314	$IDAC_{1CRT1}$	Output current of IDAC1 (7 bits) in low range	4.2	–	5.7	µA	LSB = 37.5-nA typ.
SID314A	$IDAC_{1CRT2}$	Output current of IDAC1 (7 bits) in medium range	33.7	–	45.6	µA	LSB = 300-nA typ.
SID314B	$IDAC_{1CRT3}$	Output current of IDAC1 (7 bits) in high range	270	–	365	µA	LSB = 2.4-µA typ.
SID314C	$IDAC_{1CRT12}$	Output current of IDAC1 (7 bits) in low range, 2X mode	8	–	11.4	µA	LSB = 37.5-nA typ. 2X output stage
SID314D	$IDAC_{1CRT22}$	Output current of IDAC1 (7 bits) in medium range, 2X mode	67	–	91	µA	LSB = 300-nA typ. 2X output stage
SID314E	$IDAC_{1CRT32}$	Output current of IDAC1 (7 bits) in high range, 2X mode. V_{DDA} > 2 V	540	–	730	µA	LSB = 2.4-µA typ. 2X output stage
SID315	$IDAC_{2CRT1}$	Output current of IDAC2 (7 bits) in low range	4.2	–	5.7	µA	LSB = 37.5-nA typ.
SID315A	$IDAC_{2CRT2}$	Output current of IDAC2 (7 bits) in medium range	33.7	–	45.6	µA	LSB = 300-nA typ.

Table 26 **CSD V2 specifications** *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID315B	$IDAC_{2CRT3}$	Output current of IDAC2 (7 bits) in high range	270	–	365	µA	LSB = 2.4-µA typ.
SID315C	$IDAC_{2CRT12}$	Output current of IDAC2 (7 bits) in low range, 2X mode	8	–	11.4	µA	LSB = 37.5-nA typ. 2X output stage
SID315D	$IDAC_{2CRT22}$	Output current of IDAC2 (7 bits) in medium range, 2X mode	67	–	91	µA	LSB = 300-nA typ. 2X output stage
SID315E	$IDAC_{2CRT32}$	Output current of IDAC2 (7 bits) in high range, 2X mode. V_{DDA} > 2V	540	–	730	µA	LSB = 2.4-µA typ. 2X output stage
SID315F	$IDAC_{3CRT13}$	Output current of IDAC in 8-bit mode in low range	8	–	11.4	µA	LSB = 37.5-nA typ.
SID315G	$IDAC_{3CRT23}$	Output current of IDAC in 8-bit mode in medium range	67	–	91	µA	LSB = 300-nA typ.
SID315H	$IDAC_{3CRT33}$	Output current of IDAC in 8-bit mode in high range. V_{DDA} > 2V	540	–	730	µA	LSB = 2.4-µA typ.
SID320	$IDAC_{OFFSET}$	All zeroes input	–	–	1	LSB	Polarity set by Source or Sink
SID321	$IDAC_{GAIN}$	Full-scale error less offset	–	–	±15	%	LSB = 2.4-µA typ.
SID322	$IDAC_{MISMATCH1}$	Mismatch between IDAC1 and IDAC2 in Low mode	–	–	9.2	LSB	LSB = 37.5-nA typ.
SID322A	$IDAC_{MISMATCH2}$	Mismatch between IDAC1 and IDAC2 in Medium mode	–	–	6	LSB	LSB = 300-nA typ.
SID322B	$IDAC_{MISMATCH3}$	Mismatch between IDAC1 and IDAC2 in High mode	–	–	5.8	LSB	LSB = 2.4-µA typ.
SID323	$IDAC_{SET8}$	Settling time to 0.5 LSB for 8-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID324	$IDAC_{SET7}$	Settling time to 0.5 LSB for 7-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID325	CMOD	External modulator capacitor.	–	2.2	–	nF	5-V rating, X7R or NP0 cap.

Table 27 CSDv2 ADC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
CSDv2 ADC specifications							
SIDA94	A_RES	Resolution	–	–	10	bits	Auto-zeroing is required every millisecond.
SID95	A_CHNLS_S	Number of channels - single ended	–	–	–	16	–
SIDA97	A-MONO	Monotonicity	–	–	Yes	–	V_{REF} mode
SIDA98	A_GAINERR_VREF	Gain error	–	0.6	–	%	Reference Source: SRSS (V_{REF} = 1.20 V, V_{DDA} < 2.2 V), (V_{REF} = 1.6 V, 2.2 V < V_{DDA} < 2.7 V), (V_{REF} = 2.13 V, V_{DDA} > 2.7 V)
SIDA98A	A_GAINERR_VDDA	Gain error	–	0.2	–	%	Reference Source: SRSS (V_{REF} = 1.20 V, V_{DDA} < 2.2V), (V_{REF} = 1.6 V, 2.2 V < V_{DDA} < 2.7 V), (V_{REF} = 2.13 V, V_{DDA} > 2.7 V)
SIDA99	A_OFFSET_VREF	Input offset voltage	–	0.5	–	LSB	After ADC calibration, Ref. Src = SRSS, (V_{REF} = 1.20 V, V_{DDA} < 2.2 V), (V_{REF} = 1.6 V, 2.2 V < V_{DDA} < 2.7 V), (V_{REF} = 2.13 V, V_{DDA} > 2.7 V)
SIDA99A	A_OFFSET_VDDA	Input offset voltage	–	0.5	–	LSB	After ADC calibration, Ref. Src = SRSS, (V_{REF} = 1.20 V, V_{DDA} < 2.2 V), (V_{REF} = 1.6 V, 2.2 V < V_{DDA} < 2.7 V), (V_{REF} = 2.13 V, V_{DDA} > 2.7 V)
SIDA100	A_ISAR_VREF	Current consumption	–	0.3	–	mA	CSD ADC Block current
SIDA100A	A_ISAR_VDDA	Current consumption	–	0.3	–	mA	CSD ADC Block current
SIDA101	A_VINS_VREF	Input voltage range - single ended	V_{SSA}	–	V_{REF}	V	(V_{REF} = 1.20 V, V_{DDA} < 2.2 V), (V_{REF} = 1.6 V, 2.2 V < V_{DDA} < 2.7 V), (V_{REF} = 2.13 V, V_{DDA} > 2.7 V)

Table 27 CSDv2 ADC specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SIDA101A	A_VINS_VDDA	Input voltage range - single ended	V_{SSA}	–	V_{DDA}	V	($V_{REF} = 1.20$ V, $V_{DDA} < 2.2$ V), ($V_{REF} = 1.6$ V, 2.2 V < $V_{DDA} < 2.7$ V), ($V_{REF} = 2.13$ V, $V_{DDA} > 2.7$ V)
SIDA103	A_INRES	Input charging resistance	–	15	–	kΩ	–
SIDA104	A_INCAP	Input capacitance	–	41	–	pF	–
SIDA106	A_PSRR	Power supply rejection ratio (DC)	–	60	–	dB	–
SIDA107	A_TACQ	Sample acquisition time	–	10	–	µs	Measured with 50-Ω source impedance. 10 µs is default software driver acquisition time setting. Settling to within 0.05%.
SIDA108	A_CONV8	Conversion time for 8-bit resolution at conversion rate = Fhclk / (2”(N + 2)). Clock frequency = 50 MHz.	–	25	–	µs	Does not include acquisition time.
SIDA108A	A_CONV10	Conversion time for 10-bit resolution at conversion rate = Fhclk / (2”(N + 2)). Clock frequency = 50 MHz.	–	60	–	µs	Does not include acquisition time.
SIDA109	A_SND_VRE	Signal-to-noise and Distortion ratio (SINAD)	–	57	–	dB	Measured with 50-Ω source impedance.
SIDA109A	A_SND_VDDA	Signal-to-noise and Distortion ratio (SINAD)	–	52	–	dB	Measured with 50-Ω source impedance.
SIDA111	A_INL_VREF	Integral non-linearity. 11.6 ksps	–	–	2	LSB	Measured with 50-Ω source impedance.
SIDA111A	A_INL_VDDA	Integral non-linearity. 11.6 ksps	–	–	2	LSB	Measured with 50-Ω source impedance.
SIDA112	A_DNL_VREF	Differential non-linearity. 11.6 ksps	–	–	1	LSB	Measured with 50-Ω source impedance.
SIDA112A	A_DNL_VDDA	Differential non-linearity. 11.6 ksps	–	–	1	LSB	Measured with 50-Ω source impedance.

6.4 Digital peripherals

6.4.1 Timer/Counter/PWM (TCPWM)

Table 28 TCPWM specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.TCPWM.1	I_{TCPWM1}	Block current consumption at 8 MHz	–	–	70	µA	All modes (TCPWM)
SID.TCPWM.2	I_{TCPWM2}	Block current consumption at 24 MHz	–	–	180	µA	All modes (TCPWM)
SID.TCPWM.2A	I_{TCPWM3}	Block current consumption at 50 MHz	–	–	270	µA	All modes (TCPWM)
SID.TCPWM.2B	I_{TCPWM4}	Block current consumption at 100 MHz	–	–	540	µA	All modes (TCPWM)
SID.TCPWM.3	$TCPWM_{FREQ}$	Operating frequency	–	–	100	MHz	Maximum = 100 MHz
SID.TCPWM.4	$TPWM_{ENEXT}$	Input trigger pulse width for all trigger events	2/Fc	–	–	ns	Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected. FC is counter operating frequency.
SID.TCPWM.5	$TPWM_{EXT}$	Output trigger pulse widths	1.5/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs. FC is counter operating frequency.
SID.TCPWM.5A	TC_{RES}	Resolution of counter	1/Fc	–	–	ns	Minimum time between successive counts. FC is counter operating frequency.
SID.TCPWM.5B	PWM_{RES}	PWM resolution	1/Fc	–	–	ns	Minimum pulse width of PWM output. FC is counter operating frequency.
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	2/Fc	–	–	ns	Minimum pulse width between Quadrature phase inputs. Delays from pins should be similar. FC is counter operating frequency.

6.4.2 Serial communication block (SCB)

Table 29 Serial communication block (SCB) specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
Fixed I^2C DC specifications							
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	30	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	80	µA	–
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	180	µA	–
SID152	I_{I2C4}	I^2C enabled in Deep Sleep mode	–	–	1.7	µA	At 60°C.
Fixed I^2C AC specifications							
SID153	F_{I2C1}	Bit Rate	–	–	1	Mbps	–
Fixed UART DC specifications							
SID160	I_{UART1}	Block current consumption at 100 kbps	–	–	30	µA	–
SID161	I_{UART2}	Block current consumption at 1000 kbps	–	–	180	µA	–
Fixed UART AC specifications							
SID162A	F_{UART1}	Bit Rate	–	–	3	Mbps	ULP Mode
SID162B	F_{UART2}		–	–	8	–	LP Mode
Fixed SPI DC specifications							
SID163	I_{SPI1}	Block current consumption at 1 Mbps	–	–	220	µA	–
SID164	I_{SPI2}	Block current consumption at 4 Mbps	–	–	340	µA	–
SID165	I_{SPI3}	Block current consumption at 8 Mbps	–	–	360	µA	–
SID165A	I_{SP14}	Block current consumption at 25 Mbps	–	–	800	µA	–
Fixed SPI AC specifications for LP Mode (1.1 V) unless noted otherwise.							
SID166	F_{SPI}	SPI Operating frequency externally clocked slave	–	–	25	MHz	6.25-MHz max for ULP (0.9 V) mode
SID166B	F_{SPI_EXT}	SPI operating frequency master (F_{scb} is SPI clock).	–	–	$F_{scb}/4$	MHz	F_{scb} max is 100 MHz in LP (1.1 V) mode, 25 MHz in ULP mode.
SID166A	F_{SPI_IC}	SPI slave internally clocked	–	–	15	MHz	5 MHz max for ULP (0.9 V) mode.

Table 29 **Serial communication block (SCB) specifications** *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
Fixed SPI Master mode AC specifications for LP Mode (1.1 V) unless noted otherwise.							
SID167	T_{DMO}	MOSI valid after SClock driving edge	–	–	12	ns	20 ns max for ULP (0.9 V) mode.
SID168	T_{DSI}	MISO valid before SClock capturing edge	5	–	–	ns	Full clock, late MISO sampling.
SID169	T_{HMO}	MOSI data hold time	0	–	–	ns	Referred to Slave capturing edge
SID169A	$T_{SSELMSCK1SSEL}$	Valid to first SCK Valid edge	18	–	–	ns	Referred to Master clock edge
SID169B	$T_{SSELMCK2SSEL}$	Hold after last SCK Valid edge	18	–	–	ns	Referred to Master clock edge
Fixed SPI Slave mode AC specifications for LP Mode (1.1 V) unless noted otherwise.							
SID170	T_{DMI}	MOSI valid before Sclock capturing edge	5	–	–	ns	–
SID171A	T_{DSO_EXT}	MISO valid after Sclock driving edge in Ext. Clk. mode	–	–	20	ns	35 ns max. for ULP (0.9 V) mode
SID171	T_{DSO}	MISO valid after Sclock driving edge in Internally Clk. mode	–	–	T_{DSO_EXT} + (3 × Tscb)	ns	Tscb is Serial Comm. Block clock period.
SID171B	T_{DSO}	MISO Valid after Sclock driving edge in Internally Clk. Mode with median filter enabled.	–	–	T_{DSO_EXT} + (4 × Tscb)	ns	Tscb is Serial Comm. Block clock period.
SID172	T_{HSO}	Previous MISO data hold time	5	–	–	ns	–
SID172A	$TSSEL_{SCK1}$	SSEL Valid to first SCK valid edge	65	–	–	ns	–
SID172B	$TSSEL_{SCK2}$	SSEL Hold after Last SCK valid edge	65	–	–	ns	–

6.4.3 LCD specifications

Table 30 LCD direct drive DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID154	$I_{LCDLOW1}$	Operating current with 100 kHz LCD block clock in ULP mode in Deep Sleep	–	–	90	µA	32 × 4 small display. 30 Hz. PWM mode. Slow slew rate. 460 kΩ series resistors
SID154A	$I_{LCDLOW2}$	Operating current with 32 kHz LCD block clock in ULP mode in Deep Sleep	–	–	50	µA	–
SID155	C_{LCDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	–
SID156	LCD_{OFFSET}	Long-term segment offset	–	20	–	mV	–
SID157	I_{LCDOP1}	PWM Mode current. 3.3 V bias. 8 MHz IMO. 25°C.	–	0.6	–	mA	32 × 4 segments 50 Hz
SID158	I_{LCDOP2}	PWM Mode current. 3.3 V bias. 8 MHz IMO. 25°C.	–	0.5	–	mA	32 × 4 segments 50 Hz

Table 31 LCD direct drive AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID159	F_{LCD}	LCD frame rate	10	50	150	Hz	–

6.5 Memory

Table 32 Flash DC specifications[3]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID173	VPE	Erase and program voltage	1.71	–	3.6	V	–
SID173A	IPE	Erase and program current	–	–	6	mA	–

Table 33 Flash AC specifications[3]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID174	$T_{ROWWRITE}$	Row write time (erase and program)	–	–	16	ms	Row = 512 bytes
SID175	$T_{ROWERASE}$	Row erase time	–	–	11	ms	–
SID176	$T_{ROWPROGRAM}$	Row program time after erase	–	–	5	ms	–
SID178	$T_{BULKERASE}$	Bulk erase time (256 KB)	–	–	11	ms	–
SID179	$T_{SECTORERASE}$	Sector erase time (128 KB)	–	–	11	ms	256 rows per sector
SID178S	$T_{SSERIAE}$	Subsector erase time	–	–	11	ms	8 rows per subsector
SID179S	$T_{SSWRITE}$	Subsector write time; 1 erase plus 8 program times[4]	–	–	51	ms	–
SID180S	T_{SWRITE}	Sector write time; 1 erase plus 256 program times	–	–	1.3	seconds	–
SID180	$T_{DEVPROG}$	Total device write time	–	–	2.6	seconds	–
SID181	F_{END}	Flash endurance	100K	–	–	cycles	–
SID182	F_{RET1}	Flash retention. $T_A \leq 25°C$, 100K P/E cycles	10	–	–	years	–
SID182A	F_{RET2}	Flash retention. $T_A \leq 85°C$, 10K P/E cycles	10	–	–	years	–
SID182B	F_{RET3}	Flash retention. $T_A \leq 55°C$, 20K P/E cycles	20	–	–	years	–
SID256	T_{WS100}	Number of Wait states at 100 MHz	3	–	–	–	LP mode (1.1 V)
SID257	T_{WS50}	Number of Wait states at 50 MHz	2	–	–	–	ULP mode (0.9 V)

Notes

[3] It can take as much as 16 milliseconds to write to flash. During this time, the device should not be reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

[4] Subsector, sector, and device write times do not include data transfer overhead.

6.6 System resources

6.6.1 Power-on Reset

Table 34 **Power-On-Reset (POR) with Brown-out Detect (BOD) DC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID190	$V_{FALLPPOR}$	BOD trip voltage in system LP and ULP modes.	1.54	–	–	V	Reset guaranteed for V_{DDD} levels below 1.54 V.
SID192	$V_{FALLDPSLP}$	BOD trip voltage in system Deep Sleep mode.	1.54	–	–	V	

Table 35 **POR with BOD AC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID192A	V_{DDRAMP}	Maximum power supply ramp rate (any supply)	–	–	100	mV/µs	System LP mode
SID194A	V_{DDRAMP_DS}	Maximum power supply ramp rate (any supply) in system Deep Sleep mode	–	–	10	mV/µs	BOD operation guaranteed.

6.6.2 Voltage monitors

Table 36 Voltage monitors DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID195R	V_{HVD0}	–	1.18	1.23	1.27	V	–
SID195	V_{HVDI1}	–	1.38	1.43	1.47	V	–
SID196	V_{HVDI2}	–	1.57	1.63	1.68	V	–
SID197	V_{HVDI3}	–	1.76	1.83	1.89	V	–
SID198	V_{HVDI4}	–	1.95	2.03	2.1	V	–
SID199	V_{HVDI5}	–	2.05	2.13	2.2	V	–
SID200	V_{HVDI6}	–	2.15	2.23	2.3	V	–
SID201	V_{HVDI7}	–	2.24	2.33	2.41	V	–
SID202	V_{HVDI8}	–	2.34	2.43	2.51	V	–
SID203	V_{HVDI9}	–	2.44	2.53	2.61	V	–
SID204	V_{HVDI10}	–	2.53	2.63	2.72	V	–
SID205	V_{HVDI11}	–	2.63	2.73	2.82	V	–
SID206	V_{HVDI12}	–	2.73	2.83	2.92	V	–
SID207	V_{HVDI13}	–	2.82	2.93	3.03	V	–
SID208	V_{HVDI14}	–	2.92	3.03	3.13	V	–
SID209	V_{HVDI15}	–	3.02	3.13	3.23	V	–
SID211	LVI_IDD	Block current	–	5	15	µA	–

Table 37 Voltage monitors AC specification

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID212	$T_{MONTRIP}$	Voltage monitor trip time	–	–	170	ns	–

6.6.3 SWD interface

Table 38 SWD and Trace specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SWD and Trace interface							
SID214	F_SWDCLK2	1.7 V ≤ V_{DDD} ≤ 3.6 V	–	–	25	MHz	LP Mode. V_{CCD} = 1.1 V.
SID214L	F_SWDCLK2L	1.7 V ≤ V_{DDD} ≤ 3.6 V	–	–	12	MHz	ULP Mode. V_{CCD} = 0.9 V.
SID215	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
SID216	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
SID217	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5 × T	ns	–
SID217A	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	–
SID214T	F_TRCLK_LP1	With Trace Data setup/hold times of 2/1 ns respectively	–	–	50	MHz	LP Mode. V_{DD} = 1.1 V.
SID215T	F_TRCLK_LP2	With Trace Data setup/hold times of 3/2 ns respectively	–	–	50	MHz	LP Mode. V_{DD} = 1.1 V.
SID216T	F_TRCLK_ULP	With Trace Data setup/hold times of 3/2 ns respectively	–	–	20	MHz	ULP Mode. V_{DD} = 0.9 V.

6.6.4 Internal main oscillator (IMO)

Table 39 IMO DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID218	I_{IMO1}	IMO operating current at 8 MHz	–	9	15	µA	–

Table 40 IMO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID223	$F_{IMOTOL1}$	Frequency variation centered on 8 MHz	–	–	±1	%	–40°C to +85°C
			–	–	±1.5	%	–40°C to +105°C For extended industrial temp MPNs
SID227	T_{JITR}	Cycle-to-Cycle and Period jitter	–	250	–	ps	–

6.6.5 Internal low-speed oscillator (ILO)

Table 41 ILO DC specification

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID231	I_{ILO2}	ILO operating current at 32 kHz	–	0.3	0.7	µA	–

Table 42 ILO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID234	$T_{STARTILO1}$	ILO startup time	–	–	7	µs	Startup time to 95% of final frequency.
SID236	TLIODUTY	ILO Duty cycle	45	50	55	%	–
SID237	$F_{ILOTRIM1}$	ILO frequency	28.8	32	35.2	kHz	Factory trimmed

6.6.6 FLL specifications

Table 43 Frequency locked loop (FLL) specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID450	FLL_RANGE	Input frequency range.	0.001	–	100	MHz	Upper limit is for External input.
SID451	FLL_OUT_DIV2	Output frequency range. V_{CCD} = 1.1 V	24.00	–	100.00	MHz	Output range of FLL divided-by-2 output
SID451A	FLL_OUT_DIV2	Output frequency range. V_{CCD} = 0.9 V	24.00	–	50.00	MHz	Output range of FLL divided-by-2 output
SID452	FLL_DUTY_DIV2	Divided-by-2 output; High or Low	47.00	–	53.00	%	–
SID454	FLL_WAKEUP	Time from stable input clock to 1% of final value on Deep Sleep wakeup	–	–	7.50	µs	With IMO input, less than 10°C change in temperature while in Deep Sleep, and Fout ≥ 50 MHz.
SID455	FLL_JITTER	Period jitter (1 sigma) at 100 MHz	–	–	35.00	ps	50 ps at 48 MHz, 35 ps at 100 MHz
SID456	FLL_CURRENT	CCO + Logic current	–	–	5.50	µA/MHz	–

6.6.7 Crystal oscillator specifications

Table 44 ECO specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
MHz ECO DC specifications							
SID316	I_{DD_MHz}	Block operating current with Cload up to 18 pF	–	800	1600	µA	Max at 35 MHz. Typ at 16 MHz.
MHz ECO AC specifications							
SID317	F_MHz	Crystal frequency range	16	–	35	MHz	Some restrictions apply. Refer to the device TRM.
kHz ECO DC specifications							
SID318	I_{DD_kHz}	Block operating current with 32-kHz crystal	–	0.38	1	µA	–
SID321E	ESR32K	Equivalent series resistance	–	80	–	kΩ	–
SID322E	PD32K	Drive level	–	–	1	µW	–
kHz ECO AC specifications							
SID319	F_kHz	32-kHz frequency	–	32.77	–	kHz	–
SID320	Ton_kHz	Startup time	–	–	1000	ms	–
SID320E	F_{TOL32K}	Frequency tolerance	–	50	250	ppm	May be calibrated to sub-10 ppm levels.

6.6.8 External clock specifications

Table 45 External clock specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID305	$EXTCLK_{FREQ}$	External clock input frequency	0	–	100	MHz	Min 200 kHz for 32 kHz clock operation.
SID306	$EXTCLK_{DUTY}$	Duty cycle; measured at $V_{DD}/2$	45	–	55	%	–

6.6.9 PLL specifications

Table 46 PLL specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID304P	PLL_IN	Input frequency to PLL block	4	–	64	MHz	
SID305P	PLL_LOCK	Time to achieve PLL lock	–	16	35	µs	–
SID306P	PLL_OUT	Output frequency from PLL block	10.625	–	150	MHz	–
SID307P	PLL_IDD	PLL current	–	0.55	1.1	mA	Typ at 100 MHz out.
SID308P	PLL_JTR	Period jitter	–	–	150	ps	100-MHz output frequency.

6.6.10 Clock source switching times

Table 47 Clock source switching time specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID262	$TCLK_{SWITCH}$	Clock switching from clk1 to clk2 in clock periods[5]	–	–	4 clk1 + 3 clk2	periods	–

Note

[5] As an example, if the clk_path[1] source is changed from the IMO to the FLL (see **Figure 4**) then clk1 is the IMO and clk2 is the FLL.

6.6.11 QSPI

Table 48 QSPI specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SMIF QSPI specifications. All specs with 15-pF load.							
SID390Q	Fsmifclock	SMIF QSPI output clock frequency	–	–	80	MHz	LP mode (1.1 V)
SID390QU	Fsmifclocku	SMIF QSPI output clock frequency	–	–	50	MHz	ULP mode (0.9 V)
SID399Q	Clk_dutycycle	Clock duty cycle (high or low time)	45	–	55	%	
SID397Q	Idd_qspi	Block current in LP mode (1.1 V)	–	–	1900	µA	LP mode (1.1 V)
SID398Q	Idd_qspi_u	Block current in ULP mode (0.9 V)	–	–	590	µA	ULP mode (0.9 V)
SID391Q	Tsetup	Input data set-up time with respect to clock capturing edge	4.5	–	–	ns	
SID392Q	Tdatahold	Input data hold time with respect to clock capturing edge	0	–	–	ns	–
SID393Q	Tdataoutvalid	Output data valid time with respect to clock falling edge	–	–	3.7	ns	7.5-ns max for ULP mode (0.9 V)
SID394Q	Tholdtime	Output data hold time with respect to clock rising edge	3	–	–	ns	–
SID395Q	Tseloutvalid	Output Select valid time with respect to clock rising edge	–	–	7.5	ns	15-ns max for ULP mode (0.9 V)
SID396Q	Tselouthold	Output Select hold time with respect to clock rising edge	Tsclk	–	–	ns	Tsclk = Fsmifclk cycle time

6.6.12 Smart I/O

Table 49 Smart I/O Subsystem specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID420	SMIO_BYP	Smart I/O bypass delay	–	–	2	ns	–
SID421	SMIO_LUT	Smart I/O LUT prop delay	–	8	–	ns	–

6.6.13 JTAG Boundary Scan

Table 50 JTAG Boundary Scan

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
JTAG Boundary Scan parameters for 1.1 V (LP) Mode operation:							
SID468	T_{CKLOW}	TCK LOW	52	–	–	ns	–
SID469	TCKHIGH	TCK HIGH	10	–	–	ns	–
SID470	TCK_TDO	TCK falling edge to output valid	–	–	40	ns	–
SID471	TSU_TCK	Input valid to TCK rising edge	12	–	–	ns	–
SID472	TCk_THD	Input hold time to TCK rising edge	10	–	–	ns	–
SID473	TCK_TDOV	TCK falling edge to output valid (High-Z to Active).	40	–	–	ns	–
SID474	TCK_TDOZ	TCK falling edge to output valid (Active to High-Z).	40	–	–	ns	–
JTAG Boundary Scan parameters for 0.9 V (ULP) Mode operation:							
SID468A	TCKLOW	TCK low	102	–	–	ns	–
SID469A	TCKHIGH	TCK high	20	–	–	ns	–
SID470A	TCK_TDO	TCK falling edge to output valid		–	80	ns	–
SID471A	TSU_TCK	Input valid to TCK rising edge	22	–	–	ns	–
SID472A	TCk_THD	Input hold time to TCK rising edge	20	–	–	ns	–
SID473A	TCK_TDOV	TCK falling edge to output valid (High-Z to Active).	80	–	–	ns	–
SID474A	TCK_TDOZ	TCK falling edge to output valid (Active to High-Z).	80	–	–	ns	–

7 Ordering information

Table 51 lists the PSOC™ 4500H part numbers and features. All devices include dual CPU, DMA, DC-DC converter, QSPI SMIF, DAC, LPCOMP, 6 SCBs, and 12 TCPWMs.

Table 51 Ordering Information

Family	Product	Features												Package
		CM4 CPU Speed (LP/ULP)	CM0+ CPU Speed (LP/ULP)	Flash (KB)	SRAM (KB)	SAR ADC	Opamp (CTBm)	CapSense	Segment LCD	TCPWM Blocks	SCB Blocks	QSPI	GPIO	
4500H	CY8C4588AZI-H685	150/50	100/25	256	128	2x 12-bit	2	Y	Y	12	6	1	54	64-TQFP
	CY8C4588AZI-H686	150/50	100/25	256	128	2x 12-bit	2	Y	Y	12	6	1	62	80-TQFP
	CY8C4588AZI-H675	150/50	100/25	256	128	2x 12-bit	2	-	Y	12	6	1	54	64-TQFP
	CY8C4588AZI-H676	150/50	100/25	256	128	2x 12-bit	2	-	Y	12	6	1	62	80-TQFP
	CY8C4588AZQ-H685	150/50	100/25	256	128	2x 12-bit	2	Y	Y	12	6	1	54	64-TQFP
	CY8C4588AZQ-H686	150/50	100/25	256	128	2x 12-bit	2	Y	Y	12	6	1	62	80-TQFP

8 Packaging

This product line is offered in 80-TQFP and 64-E-TQFP packages.

Table 52 Package dimensions

Spec ID#	Package	Description	Package Dwg #
PKG_1	80-pin TQFP	80-pin TQFP, 12 × 12 × 1.6 mm	002-29467
PKG_2	64-pin E-TQFP	64-pin E-TQFP, 10 × 10 × 1.6 mm	002-29202

Table 53 Package characteristics

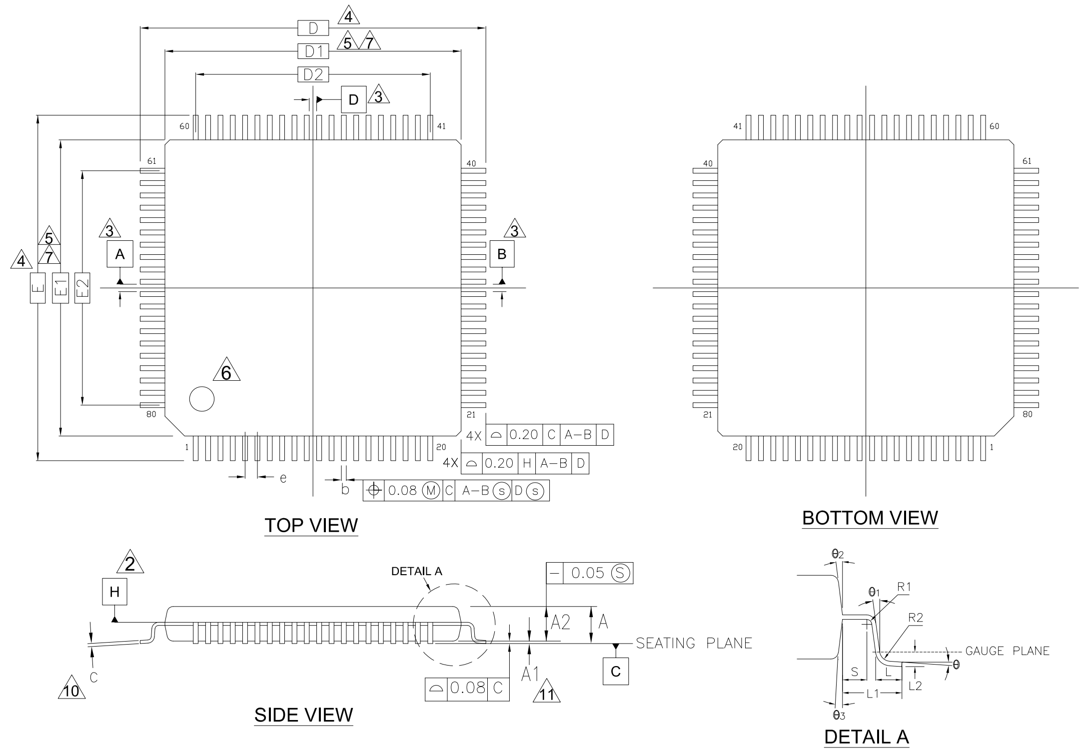
Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature	–	–40	25	85	°C
T_A	Extended Industrial temperature	–	–40	25	105	°C
T_J	Operating junction temperature	–	–40	–	100	°C
T_J	Extended Industrial temperature	–	–40	–	120	°C
T_{JA}	Package θ_{JA} (80-pin TQFP)	–	–	35	–	°C/W
T_{JC}	Package θ_{JC} (80-pin TQFP)	–	–	6	–	°C/W
T_{JA}	Package θ_{JA} (64-pin E-TQFP)	–	–	26	–	°C/W
T_{JC}	Package θ_{JC} (64-pin E-TQFP)	–	–	7	–	°C/W

Table 54 Solder reflow peak temperature

Package	Maximum peak temperature	Maximum time at peak temperature
All packages	260°C	30 seconds

Table 55 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2

Package	MSL
All packages	MSL3



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	——	——	1.60
A1	0.05	——	0.15
A2	1.35	1.40	1.45
D	14.00 BSC		
D1	12.00 BSC		
D2	9.50 BSC		
E	14.00 BSC		
E1	12.00 BSC		
E2	9.50 BSC		
e	0.50 BSC		
R1	0.08	——	——
R2	0.08	——	0.20

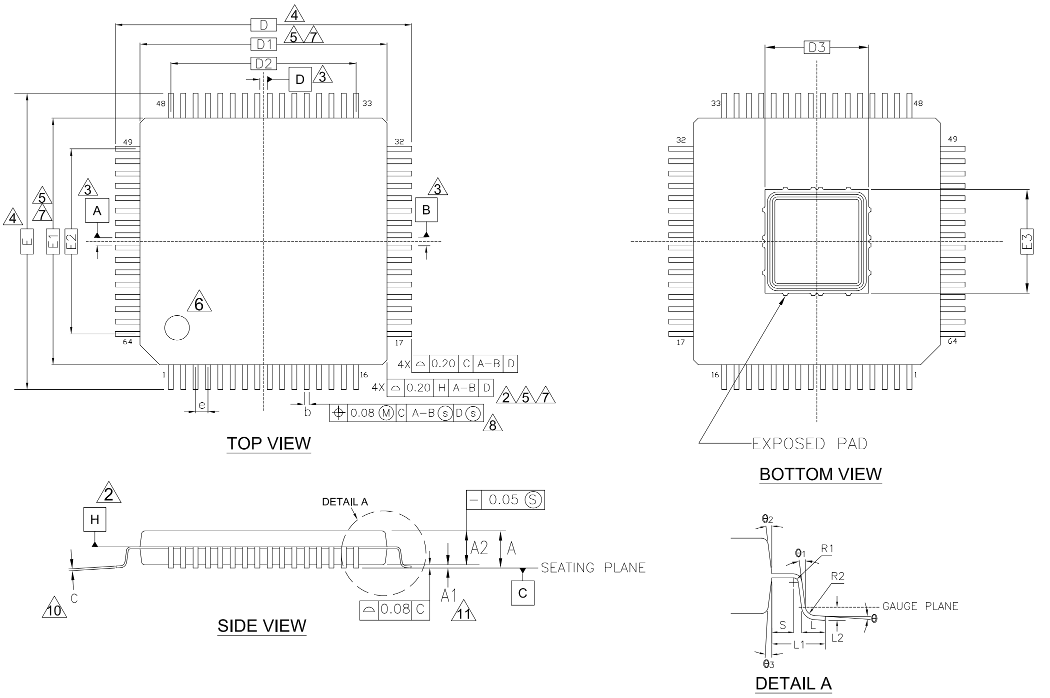
SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
θ	0°	3.5°	7°
θ1	0°	——	——
θ2	11°	12°	13°
θ3	11°	12°	13°
c	0.09	——	0.20
b	0.17	0.20	0.27
S	0.20	——	——
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 REF		

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
11. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-29467 Rev. **

Figure 17 80-pin TQFP ((12.0 × 12.0 × 1.6 mm) AZ80A) package outline (PG-TQFP-80)



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
D	12.00 BSC		
D1	10.00 BSC		
D2	7.50 REF		
D3	4.20 REF		
E	12.00 BSC		
E1	10.00 BSC		
E2	7.50 REF		
E3	4.20 REF		
e	0.50 BSC		

SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
R1	0.08	—	—
R2	0.08	—	0.20
θ	0°	3.5°	7°
θ1	0°	—	—
θ2	11°	12°	13°
θ3	11°	12°	13°
c	0.09	0.127	0.20
b	0.17	0.20	0.27
S	0.20	—	—
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 REF		

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
11. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-29202 Rev. **

Figure 18 64-pin E-TQFP ((10.0 × 10.0 × 1.6 mm) AE64A 4.2 × 4.2 mm E-Pad package outline (PG-TQFP-64)

9 Acronyms

Table 56 **Acronyms**

Acronym	Description
3DES	triple DES (data encryption standard)
ADC	analog-to-digital converter
ADMA3	advanced DMA version 3, a Secured Digital data transfer mode
AES	advanced encryption standard
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm® data transfer bus
AMUX	analog multiplexer
AMUXBUS	analog multiplexer bus
API	application programming interface
Arm®	advanced RISC machine, a CPU architecture
BGA	ball grid array
BOD	brown-out detect
BREG	backup registers
BWC	backward compatibility (eMMC data transfer mode)
CAD	computer aided design
CCO	current controlled oscillator
ChaCha	a stream cipher
CM0+	Cortex®-M0+, an Arm® CPU
CM4	Cortex®-M4, an Arm® CPU
CMAC	cypher-based message authentication code
CMOS	complementary metal-oxide-semiconductor, a process technology for IC fabrication
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CSD	Capacitive Sigma-Delta
CSV	clock supervisor
CSX	Cypress, an Infineon company mutual capacitance sensing method. See also CSD
CTI	cross trigger interface
DAC	digital-to-analog converter, see also IDAC, VDAC
DAP	debug access port
DDR	double data rate
DES	data encryption standard
DFT	design for test
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DSI	digital system interconnect
DU	data unit
DW	data wire, a DMA implementation
ECC	error correcting code
ECC	elliptic curve cryptography
ECO	external crystal oscillator

Table 56 **Acronyms** *(continued)*

Acronym	Description
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
eMMC	embedded MultiMediaCard
ESD	electrostatic discharge
ETM	embedded trace macrocell
FIFO	first-in, first-out
FLL	frequency locked loop
FPU	floating-point unit
FS	full-speed
GND	Ground
GPIO	general-purpose input/output, applies to a PSOC™ pin
HMAC	Hash-based message authentication code
HSIOM	high-speed I/O matrix
I/O	input/output, see also GPIO, DIO, SIO, USBIO
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
I^2S	inter-IC sound
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
IOSS	input output subsystem
IoT	internet of things
IPC	inter-processor communication
IRQ	interrupt request
ISR	interrupt service routine
ITM	instrumentation trace macrocell
JTAG	Joint Test Action Group
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol
LP	low power
LS	low-speed
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MCWDT	multi-counter watchdog timer
MISO	master-in slave-out
MMIO	memory-mapped input output
MOSI	master-out slave-in

Table 56 **Acronyms** *(continued)*

Acronym	Description
MPU	memory protection unit
MSL	moisture sensitivity level
Msps	million samples per second
MTB	micro trace buffer
MUL	multiplier
NC	no connect
NMI	nonmaskable interrupt
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
OTP	one-time programmable
OVP	over voltage protection
OVT	overvoltage tolerant
PASS	programmable analog subsystem
PCB	printed circuit board
PCM	pulse code modulation
PDM	pulse density modulation
PHY	physical layer
PICU	port interrupt control unit
PLL	phase-locked loop
PMIC	power management integrated circuit
POR	power-on reset
PPU	peripheral protection unit
PRNG	pseudo random number generator
PSOC™	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
QD	quadrature decoder
QSPI	quad serial peripheral interface
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
ROM	read-only memory
RSA	Rivest–Shamir–Adleman, a public-key cryptography algorithm
RTC	real-time clock
RWW	read-while-write
RX	receive
S/H	sample and hold
SAR	successive approximation register
SARMUX	SAR ADC multiplexer bus
SC/CT	switched capacitor/continuous time
SCB	serial communication block
SCL	I^2C serial clock
SD	Secured Digital

Table 56 **Acronyms** *(continued)*

Acronym	Description
SDA	I^2C serial data
SDHC	Secured Digital host controller
SDR	single data rate
Sflash	supervisory flash
SHA	secure hash algorithm
SINAD	signal to noise and distortion ratio
SMPU	shared memory protection unit
SNR	signal-to-noise ration
SOF	start of frame
SONOS	silicon-oxide-nitride-oxide-silicon, a flash memory technology
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SROM	supervisory read-only memory
SRSS	system resources subsystem
SWD	serial wire debug, a test protocol
SWJ	serial wire JTAG
SWO	single wire output
SWV	single-wire viewer
TCPWM	timer, counter, pulse-width modulator
TDM	time division multiplexed
THD	total harmonic distortion
TQFP	thin quad flat package
TRM	technical reference manual
TRNG	true random number generator
TX	transmit
UART	universal asynchronous transmitter receiver, a communications protocol
UDB	universal digital block
ULP	ultra-low power
USB	Universal Serial Bus
WCO	watch crystal oscillator
WDT	watchdog timer
WIC	wakeup interrupt controller
WLCSP	wafer level chip scale package
XIP	execute-in-place
XRES	external reset input pin

10 Document conventions

10.1 Units of measure

Table 57 Units of measure

Symbol	Unit of measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
W	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

Revision history

Document revision	Date	Description of change
**	2020-07-24	New datasheet.
*A	2020-08-17	Added **Interprocessor communication (IPC)**. Updated **Analog Subsystem** block diagram. Removed dual-quad and octal support from **Quad-SPI/serial memory interface (SMIF)** and changed the max throughput from 640 to 320 Mbps. Added pin diagrams in **Pinouts**. Updated **Errata**.
*B	2020-11-19	Updated links in **PSOC™ 4500H resources**. Added a note referring to the **Analog Subsystem** diagram and TRM. Changed the format of the "Deep Sleep Mode" row and the "Noise" row in **Opamp specifications**. Updated the VDDA bullet in **Power supply considerations**. Removed references to "All specifications are valid for –40 °C ≤ TA ≤ 85 °C and for 1.71 V to 3.6 V except where noted". Added **XRES connection diagram** and updated XRES section in **Reset**.
*C	2021-01-22	Corrected clock designation in **Figure 2**. Updated recommended values for XRES pull-up resistor in **Reset**. Added **Table 10** and **Figure 14**. Formatted **Table 17**. Corrected error in SID316 and updated description of SID319. Corrected format issues **PSoC™ 4500H resources**.
*D	2021-06-23	Added opamp graphs (**Figure 15** and **Figure 16**). Updated security terminology to Infineon standards. Changed BLE references to Bluetooth LE.
*E	2021-08-04	Removed Errata. Updated values for SIDHIB2, SID13, SID14, SID17A, SID15, SIDP122, SIDP123, and SID313_3A.
*F	2021-09-01	Added extended industrial temperature specs in **Opamp specifications**, **Temperature sensor specifications**, and **IMO AC specifications**. Added extended industrial temperature MPNs in **Ordering information**.
*G	2021-12-06	Updated the analog subsystem diagram. Updated CPU current values in **Features**. Updated SIDC1 description. Updated details/conditions for SID7A. Updated **Figure 14**.
*H	2022-04-12	Updated eFuse description in the **Memory** section.
*I	2022-10-18	Added device identification and revision information in **Features**. Added spec SID304P. Updated **PLL specifications** and **Clock system**. Updated **Protection units**.
*J	2024-09-13	Migrated to Infineon template. Removed preliminary note from **Electrical specifications**.
*K	2025-04-19	Removed package diagrams that are not applicable to PSoC™ 4500H MU and updated the following: **Figure 17**: 002-29467 Rev. ** **Figure 18**: 002-29202 Rev. **

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