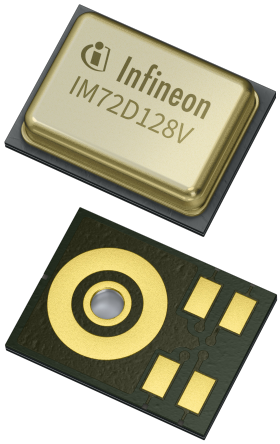
Technical documents

Kits and boards

Ultra-low power digital PDM XENSIV™ MEMS microphone

Features

- Ultra-high signal to noise ratio (SNR) of 71.5 dB(A)
- Ultra-low current consumption in high performance mode (430 µA) and in low power mode (160 µA)
- Component level IP57 water and dust resistant
- Flat frequency response with a low frequency roll-off at 11 Hz
- Package dimensions: 4 mm x 3 mm x 1.2 mm



RoHS

Green

Halogen-free

Potential applications

- Active Noise Cancellation (ANC) headphones and earbuds
- High quality audio capturing
  - Laptops and tablets
  - Conference systems
  - Cameras, camcorders, and camera accessories
- Devices with Voice User Interface (VUI)
  - Smart speakers
  - Home automation
  - IOT devices
- Industrial or home monitoring with audio pattern detection

Product validation

Technology qualified for industrial applications.

Ready for validation in industrial applications according to the relevant tests of IEC 60747 and 60749 or alternatively JEDEC47/20/22.

Description

The IM72D128VV01 is an ultra-high performance XENSIV™ MEMS microphone designed for applications which require a digital PDM MEMS microphone with high SNR (low self-noise), low distortion (high AOP), and very low current consumption.

Very high signal-to-noise ratio (SNR) of 71.5 dB(A) enables far-field and low volume audio pick-up. The flat frequency response (11 Hz low-frequency roll-off) and tight manufacturing tolerance improve performance of multi-microphone (array) applications.

The digital microphone ASIC contains an extremely low-noise preamplifier and a high-performance sigma-delta ADC. Different power modes can be selected in order to suit specific clock frequency and current consumption requirements. Each IM72D128VV01 microphone is calibrated with an advanced Infineon calibration algorithm, resulting in low sensitivity tolerances (±1 dB).

Type	Package	Marking
IM72D128VV01	PG-LLGA-5-3	I72D26

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1 Block diagram

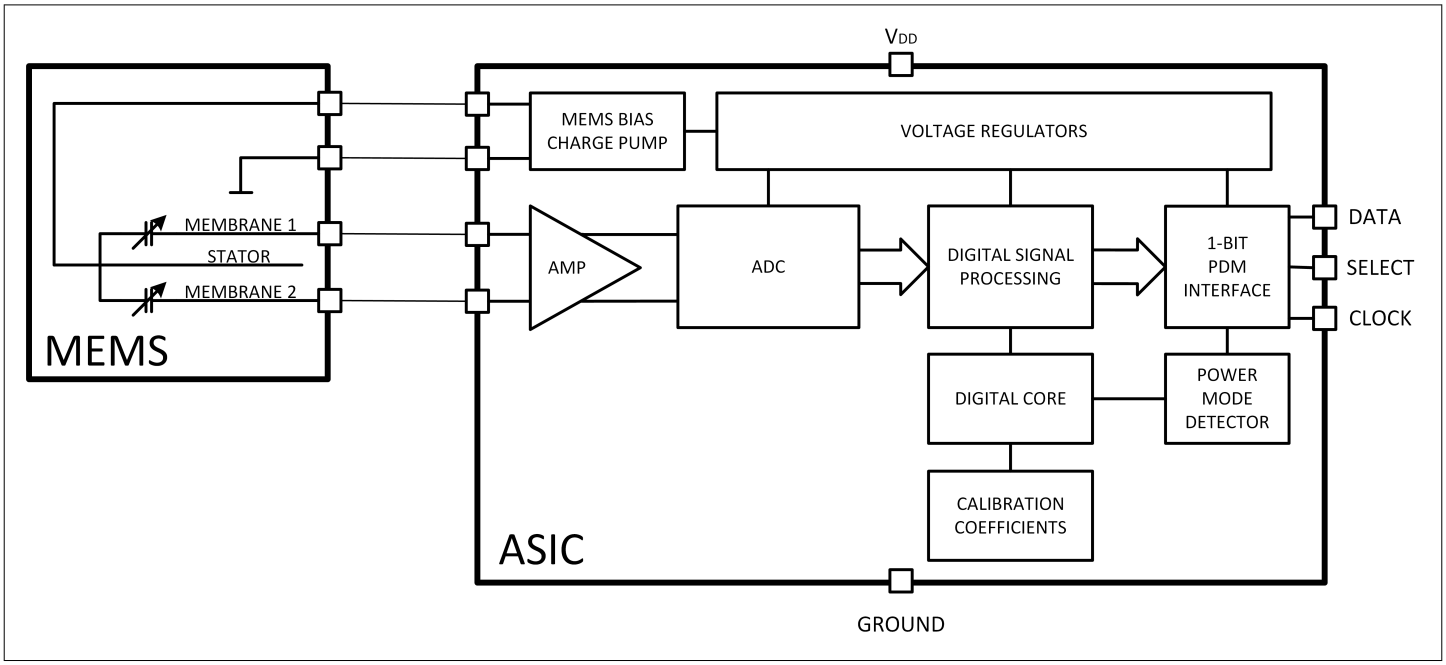

Figure 1 Block diagram

2 Environmental robustness

Infineon's latest Sealed Dual Membrane MEMS technology delivers high ingress protection (IP57) at a microphone level. The sealed MEMS design prevents water or dust from entering between membrane and backplate, preventing mechanical blockage or electric leakage issues commonly observed in MEMS microphones. Microphones built with the Sealed Dual Membrane technology can be used to create IP68 devices, requiring only minimal mesh protection.

Table 1 Environmental robustness

Test Standard	Test Condition
IP5x dust resistance[1)]	Arizona dust A4 coarse, vertical orientation, sound hole upwards, 10 cycles (15 minutes sedimentation, 6 sec blowing)
IPx7 water immersion[2)]	Temporary immersion of 1 meters for 30 minutes. Microphone tested 2 hours after removal

1 The number "5" stands for the dust ingress rating or the capacity to withstand the effects of fine, abrasive dust particles.
2 The "7" specifies the higher water immersion rating.

3 Typical performance characteristics

Test conditions: V_{DD}=1.8 V, f_{CLK}=3.072 MHz, T_A=25°C, unless otherwise specified.

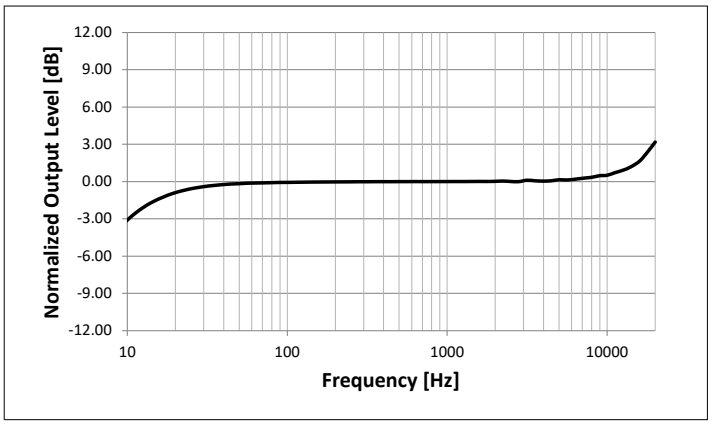

Figure 2 **Typical amplitude response**

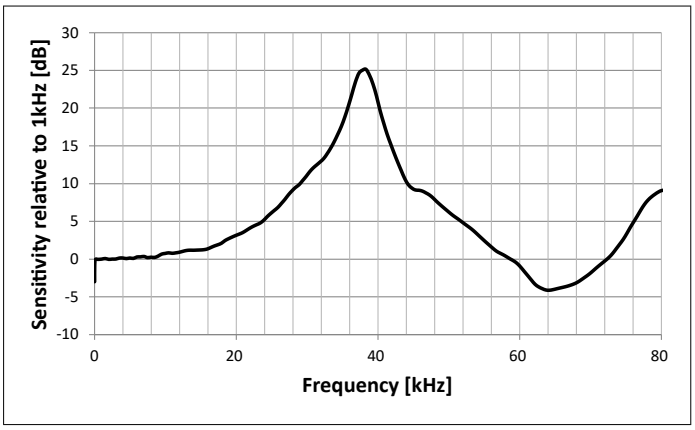

Figure 3 **Typical ultrasonic response**

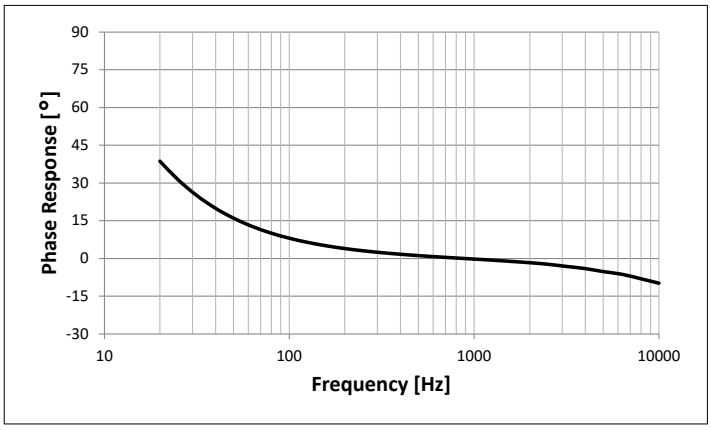

Figure 4 **Typical phase response**

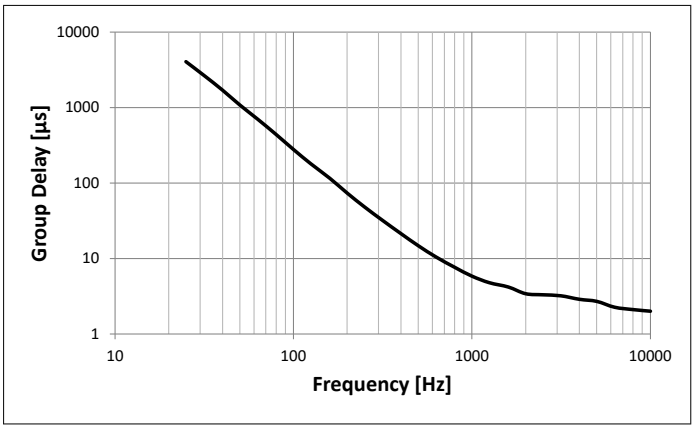

Figure 5 **Typical group delay**

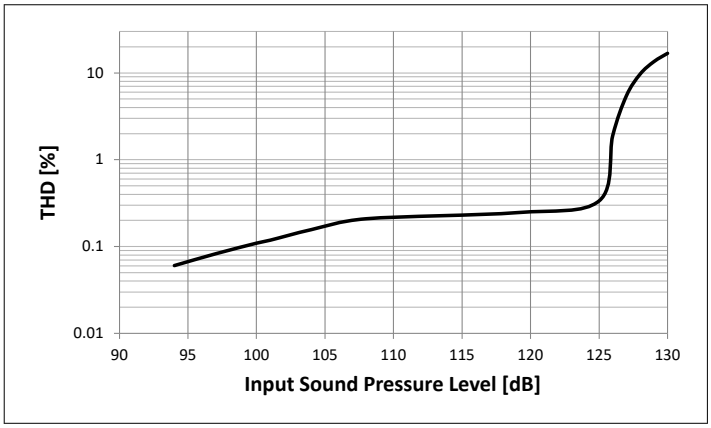

Figure 6 **Typical THD vs SPL**

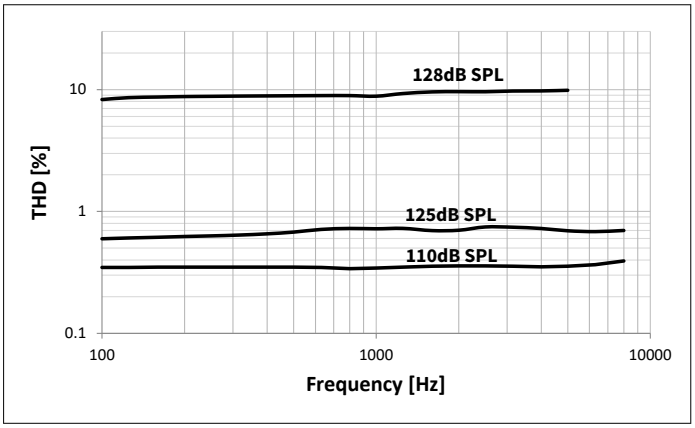

Figure 7 **Typical THD vs frequency**

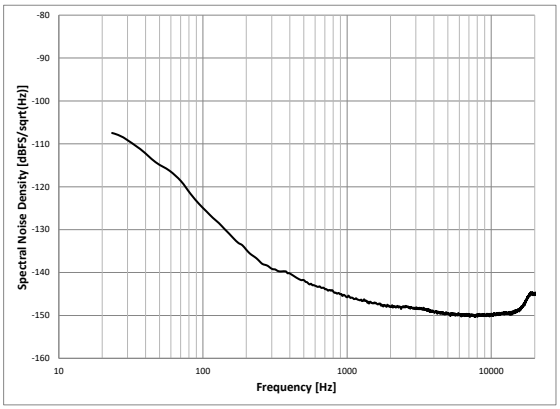

Figure 8 **Typical noise floor (unweighted)**

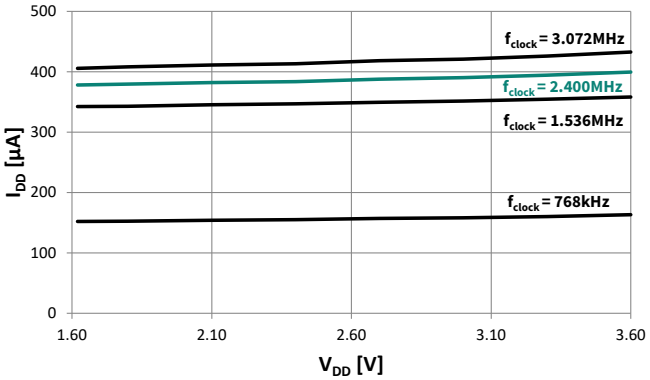

Figure 9 **Typical I_{DD} vs V_{DD}**

4 Acoustic characteristics

Test conditions (unless otherwise specified in the table): V_{DD} = 1.8 V, f_{CLK} = 3.072 MHz, OSR=64, T_A = 25°C, 55% R.H., audio bandwidth 20 Hz to 20 kHz, select pin grounded, no load on DATA, T_{edge} = 9 ns

Table 2 Acoustic specifications

Parameter		Symbol	Values			Unit	Note or Test Condition
			Min.	Typ.	Max.		
Sensitivity		S	-37	-36	-35	dBFS	1 kHz, 94 dBSPL, all operating modes
Low frequency roll-off		LFRO		11		Hz	-3 dB relative to 1 kHz
Resonant frequency peak				37.5		kHz	
Signal to noise ratio	F_{clock} = 768 kHz	SNR		67		dB(A)	20 Hz to 8 kHz bandwidth, OSR: 48, A-weighted
	F_{clock} = 1.536 MHz			70			20 Hz to 12 kHz bandwidth, A-weighted
	F_{clock} = 2.4 MHz			70.5			20 Hz to 20 kHz bandwidth, A-weighted
	F_{clock} = 3.072 MHz			71.5			
Total harmonic distortion	94 dBSPL	THD		0.1		%	Measuring 2nd to 5th harmonics; 1 kHz. S = typ, all operating modes
	125 dBSPL			1.0			
	128 dBSPL			10.0			
Acoustic overload point	10% THD	AOP		128		dBSPL	Measuring 2nd to 5th harmonics; 1 kHz. S = typ, all operating modes
Group delay	250 Hz			60		µs	
	600 Hz			10			
	1 kHz			6			
	4 kHz			3.5			
Phase response	75 Hz			11		°	
	1 kHz			-0.3			
	4 kHz			-4			
Directivity			Omnidirectional				
Polarity		Positive pressure increases density of 1's, negative pressure decreases density of 1's in data output					

5 Free field frequency response

5.1 Free field frequency response

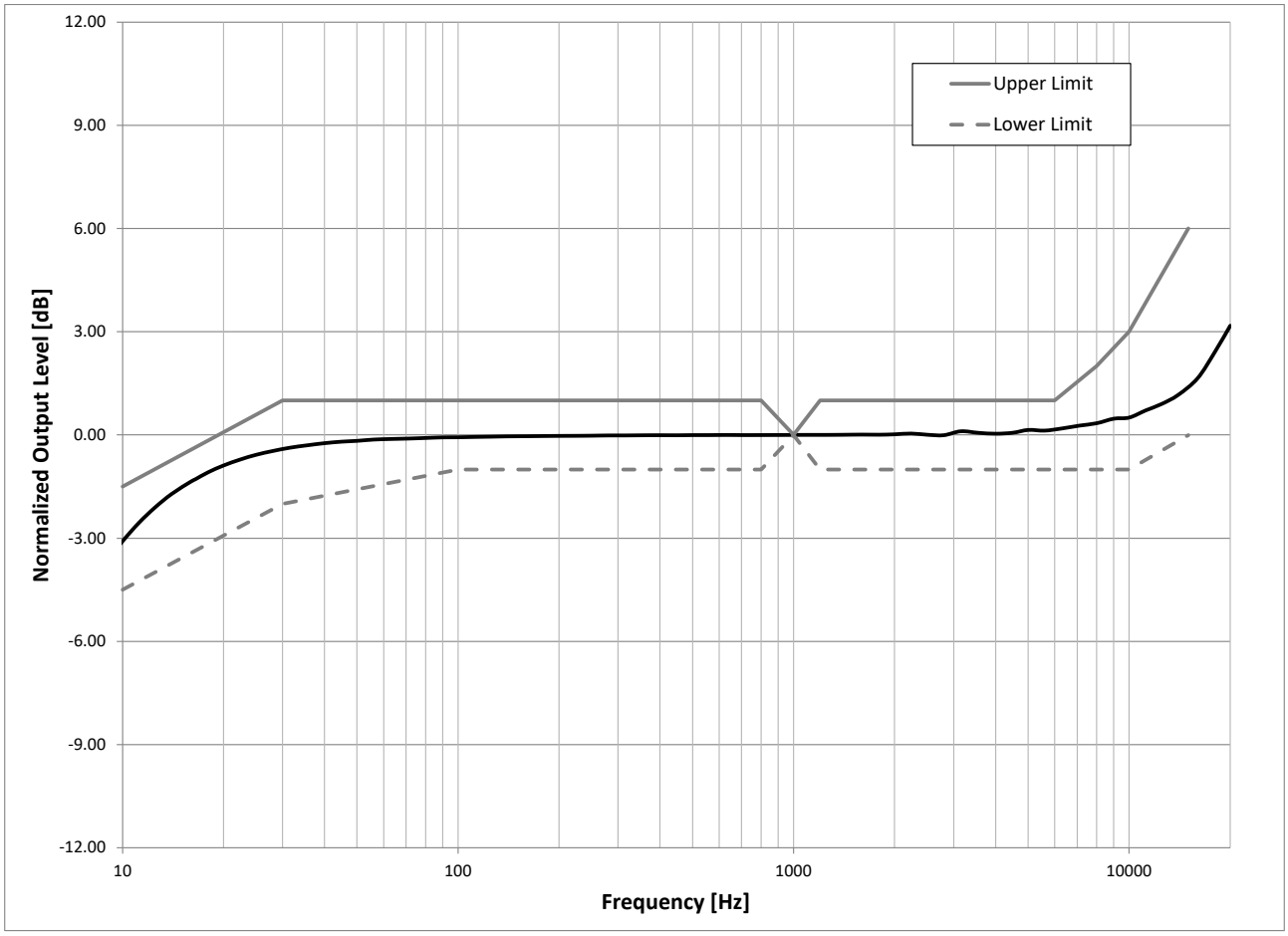

Figure 10 Free field frequency response

Table 3 Free field frequency response, normalized to 1 kHz sensitivity value

Frequency [Hz]	Upper limit [dB]	Lower limit [dB]
10	-1.5	-4.5
30	1	-2
100	1	-1
800	1	-1
1000	0	0
1200	1	-1
6000	1	-1
8000	2	-1
10000	3	-1
15000	6	0

6 Electrical characteristics and parameters

6.1 Absolute maximum ratings

Stresses exceeding the listed maximum ratings may affect device reliability or cause permanent device damage. Functional device operation at these conditions is not guaranteed.

Table 4 Absolute maximum ratings

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Voltage on any pin	V_{max}		3.6	V	
Storage temperature	T_S	-40	125	°C	
Ambient temperature	T_A	-40	85	°C	

6.2 Electrical parameters

Table 5 Electrical parameters and digital interface input

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Supply voltage		V_{DD}	1.62	1.8	3.6	V	3)
Clock frequency range	Standby mode	f_{clock}			330	kHz	4)
	Low power mode		380	480	640	kHz	5)
			730	768	1020	kHz	
	Normal mode		1.17	1.536	1.70	MHz	
	High performance mode		1.9	2.4	2.6	MHz	
			2.9	3.072	3.4	MHz	
V_{DD} ramp-up time					50	ms	Time until $V_{DD} \geq V_{DD_min}$
Input logic low level		V_{IL}			$0.3xV_{DD}$	V	
Input logic high level		V_{IH}	$0.7xV_{DD}$			V	
Clock rise/fall time					13	ns	10% to 90%
Clock duty cycle			45		55	%	
Output load capacitance on DATA		C_{load}			100	pF	

3 A 1 µF bypass capacitor should be placed close to the microphone V_{DD} pad to ensure best SNR performance.
4 Data pad is high impedance in standby mode.
5 Parameter not subject to productive test. Verified by laboratory characterization/design.

6.3 Electrical characteristics

Test conditions (unless otherwise specified in the table): V_{DD} = 1.8 V, f_{CLK} = 3.072 MHz, T_A = 25°C, 55% R.H.

Table 6 General electrical characteristics

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Current consumption	Clock off mode	I_{clock_off}			1	µA	CLOCK pulled low
	Standby mode	$I_{standby}$		90	120		No load on DATA
	F_{clock} = 768 kHz	I_{DD}		160	230		<5pF load on DATA
	F_{clock} = 1.536 MHz			350			
	F_{clock} = 2.4 MHz			390			
	F_{clock} = 3.072 MHz			430	525		
Short circuit current			1		20	mA	Grounded DATA pin
Power supply rejection		PSR_{1k_NM}		-80		dBFS	100 mV_{pp} sine wave on V_{DD} swept from 200 Hz to 20 kHz.
		PSR_{217_NM}		-86		dBFS(A)	100 mV_{pp}, 217 Hz square wave on V_{DD}. A-weighted.
Startup time	±0.5 dB sensitivity accuracy				20	ms	Time to start up in any operating modes after V_{DD_min} and CLOCK have been applied.[6]
	±0.2 dB sensitivity accuracy				50		
Mode switch time	±0.5 dB sensitivity accuracy				20	ms	Time to switch between operating modes. V_{DD} remains on during the mode switch.[6]
	±0.2 dB sensitivity accuracy				50		
Output logic low level		V_{OL}			0.2xV_{DD}	V	
Output logic high level		V_{OH}	0.8xV_{DD}				
Delay Time for DATA Driven		t_{DD}	40		80	ns	Delay time from CLOCK edge (0.5xV_{DD}) to DATA driven.
Delay time for DATA high-Z[7]		t_{HZ}	5		30	ns	Delay time from CLOCK edge (0.5xV_{DD}) to DATA high impedance state
Delay time for DATA valid[8]		t_{DV}			100	ns	Delay time from CLOCK edge (0.5xV_{DD}) to DATA valid (<0.3xV_{DD} or >0.7xV_{DD})
Power-on behaviour		Idle tone is output over PDM within 3 ms of applying V_{DD} and f_{clock}, remains until a valid microphone signal is available. Idle tone consists of alternating 1s and 0s, representing a zero input signal.					

6 Verified at typical PDM clock frequencies for each power mode.
7 t_{hold} is dependent on C_{load}
8 Load on data: C_{load}=100 pF, R_{load}=100 kΩ

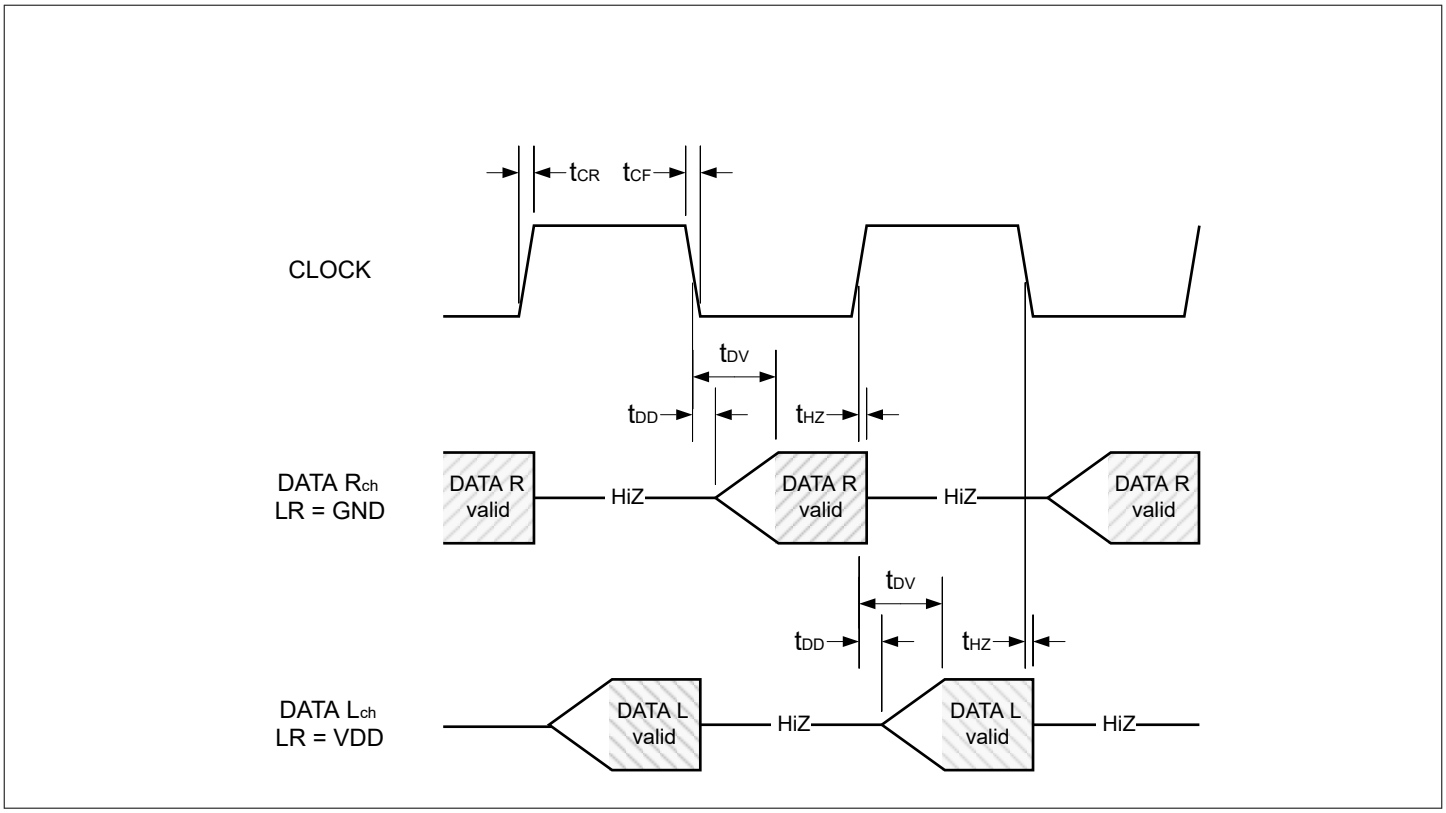

Figure 11 **Timing diagram**

6.4 Audio DC offset

The DC output level encoded in the DC bit stream is determined by the L/R state on startup. In each case the DC output level is stable over time and does not vary with input signal level.

Table 7 **DC output level using L/R pin**

LR state	DC output level (typical)	Unit
LR = GND	-80	dBFS
LR = VDD	-40	dBFS

6.5 Stereo PDM configuration

The IM72D128VV01 is designed to function in circuits with one or two microphones on the PDM bus. When two microphones are connected, data is transmitted alternately according to the L/R pin status of each microphone. When two microphones are connected to a shared PDM bus, the power modes of both microphones will be the same as both are controlled by the same PDM clock. The performance is unchanged relative to a single microphone per bus configuration.

Table 8 PDM channel configuration using L/R pin.

Channel	Data driven	Data high-Z	L/R connection
DATA1	Falling clock edge	Rising clock edge	GND
DATA2	Rising clock edge	Falling clock edge	V_{DD}

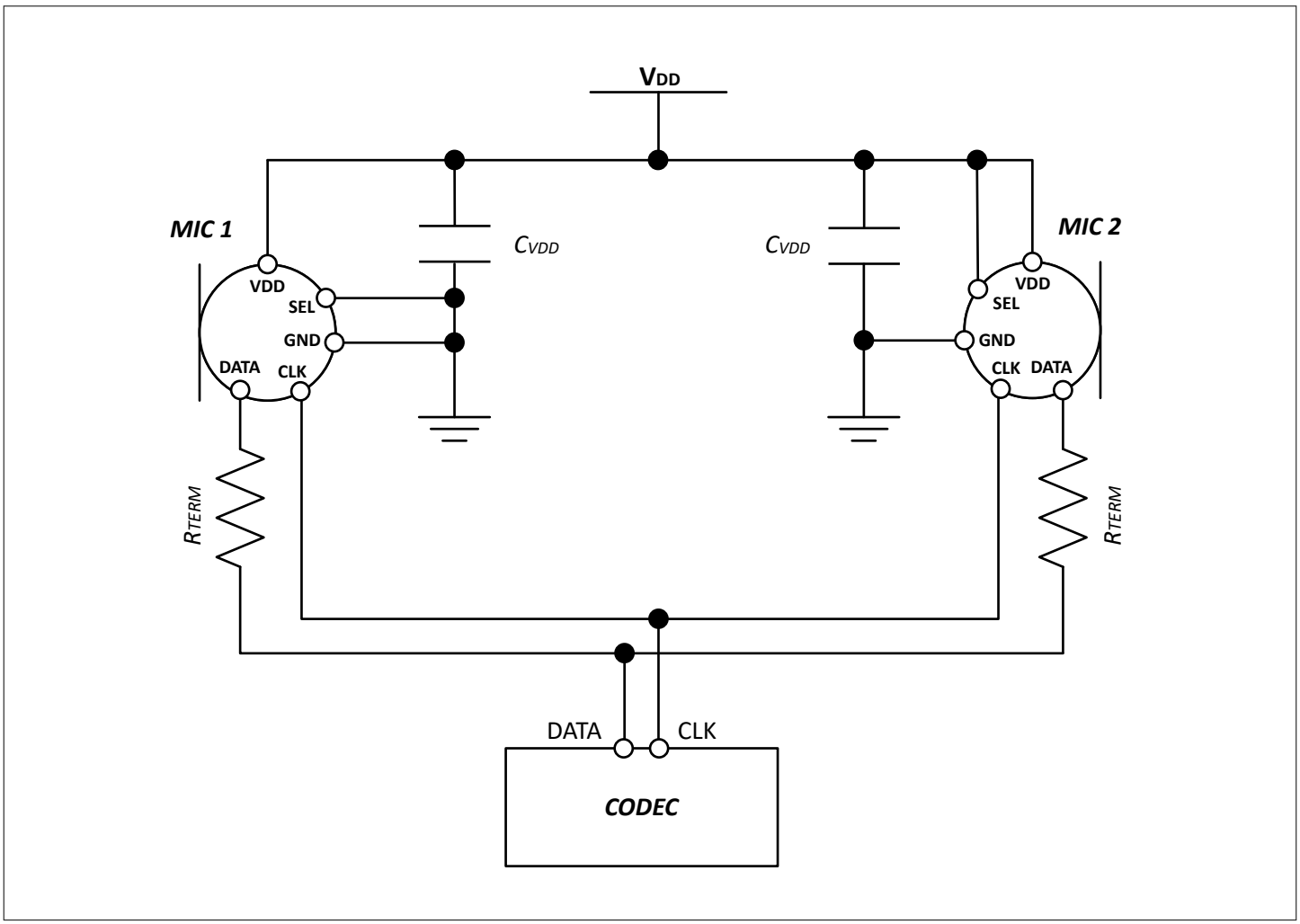

Figure 12 Typical stereo mode configuration

***Note**: For best performance it is strongly recommended to place a 100 nF (C_{VDD_typ}) capacitor between V_{DD} and ground for each microphone. The capacitor should be placed as close to V_{DD} as possible. A termination resistor (R_{TERM}) of about 100 Ω may be added to reduce the ringing and overshoot on the output signal.*

7 Package information

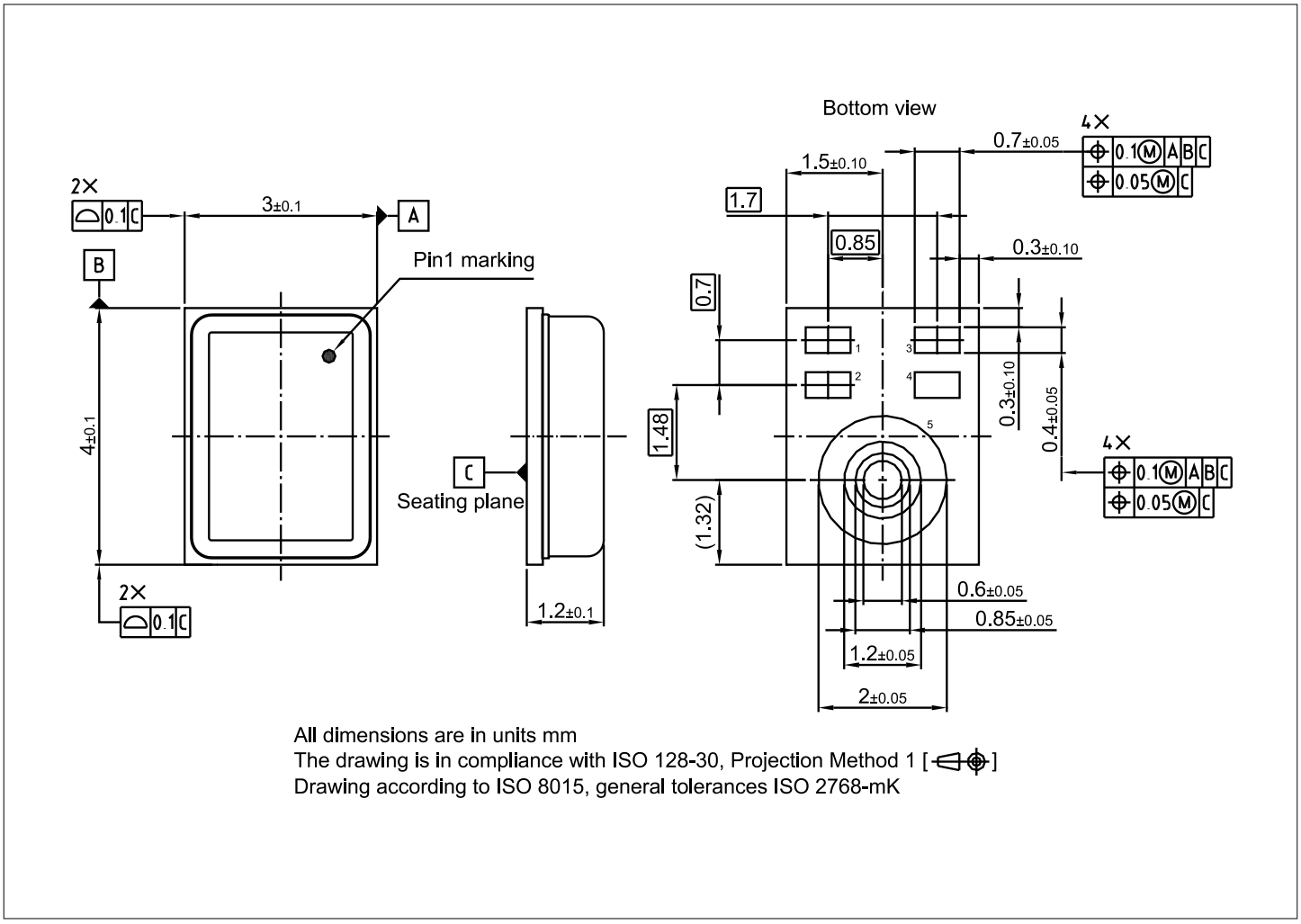

Figure 13 **IM72D128VV01 package drawing**

Table 9 **IM72D128VV01 pin configuration**

Pin Number	Name	Description
1	DATA	PDM data output
2	V_{DD}	Power supply
3	CLOCK	PDM clock input
4	LR	PDM left/right select
5	GND	Ground

8 Footprint and stencil recommendation

The acoustic port hole diameter in the PCB should be larger than the acoustic port hole diameter of the MEMS microphone to ensure optimal performance. A PCB sound port size of radius 0.4 mm (diameter 0.8 mm) is recommended.

The board pad and stencil aperture recommendations shown in Figure 14 are based on Non-Solder Mask Defined (NSMD) pads. The specific design rules of the board manufacturer should be considered for individual design optimizations or adaptations.

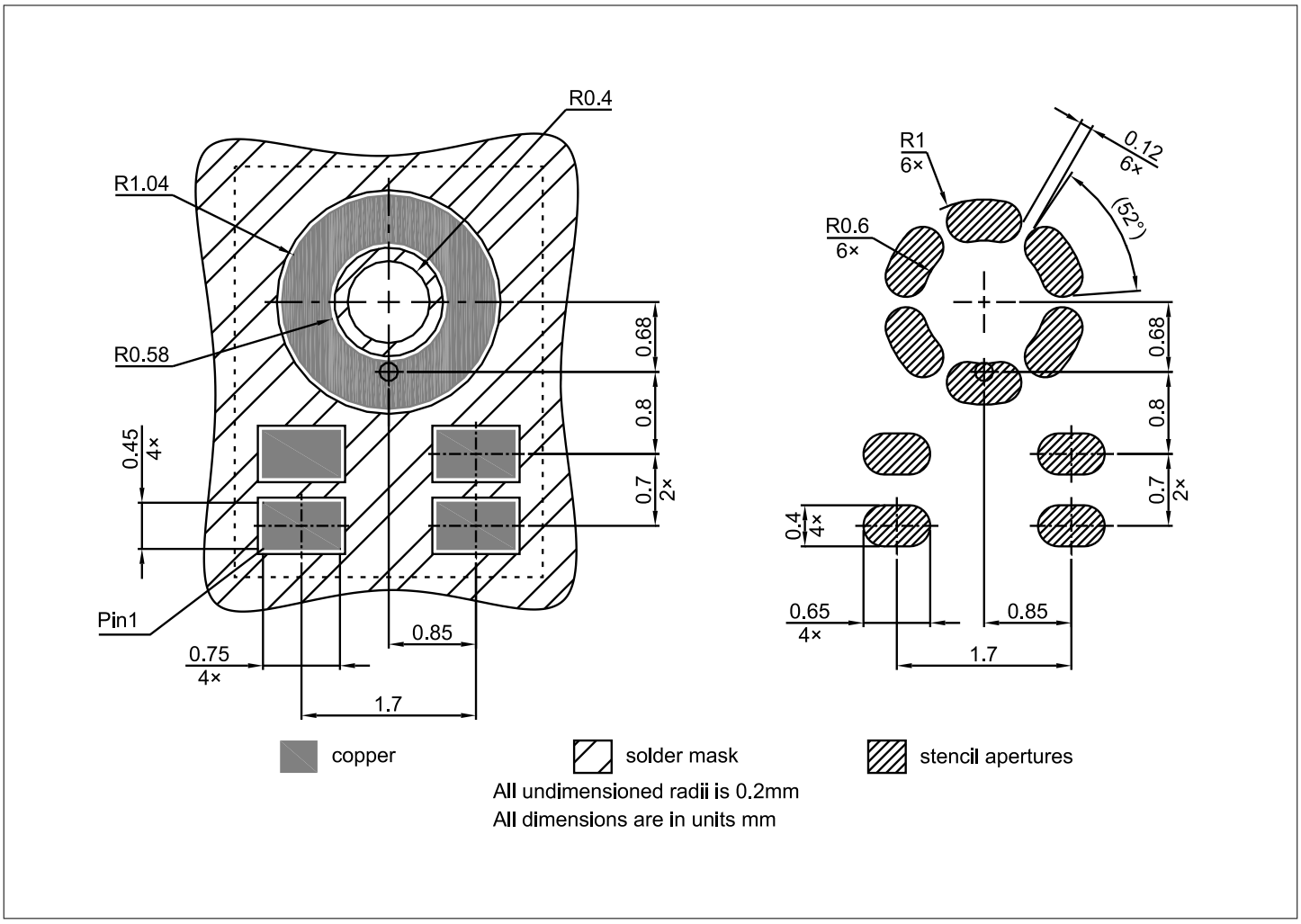

Figure 14 **Footprint and stencil recommendation**

9 Packing information

For shipping and assembly the Infineon microphones are packed in product specific tape-and-reel carriers. A detailed drawing of the carrier can be seen in

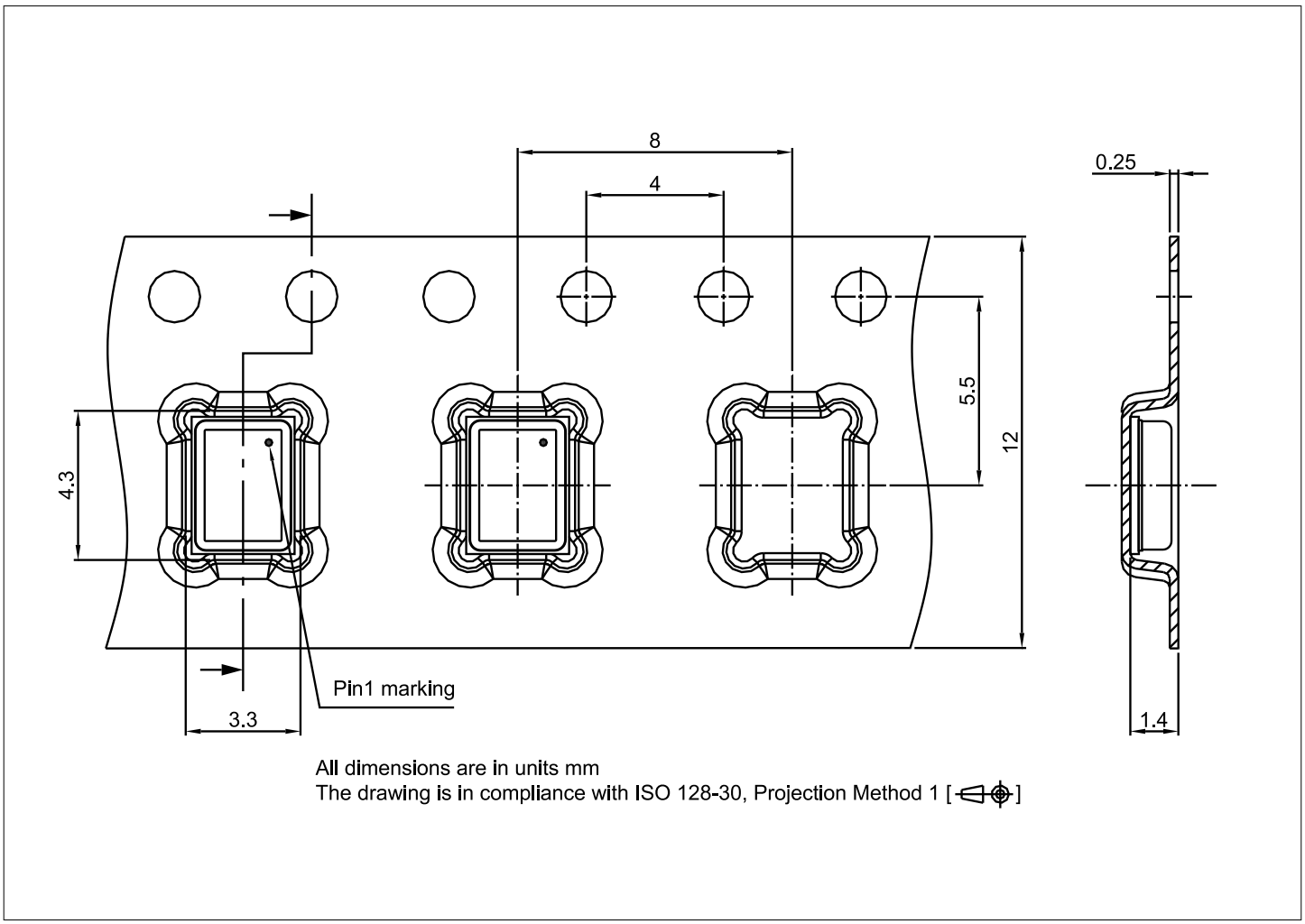

Figure 15 **IM72D128VV01 tape and reel packing information**

Table 10 **IM72D128VV01 packaging information**

Product	Type code	Reel diameter	Quantity per reel
IM72D128VV01	I72D26	13"	5000

10 Reflow soldering and board assembly

Infineon MEMS microphones are qualified in accordance with the IPC/JEDEC J-STD-020D-01. The moisture sensitivity level of MEMS microphones is rated as MSL1. For PCB assembly of the MEMS microphone the widely used reflow soldering using a forced convection oven is recommended.

The soldering profile should be in accordance with the recommendations of the solder paste manufacturer to reach an optimal solder joint quality. The reflow profile shown in Figure 16 is recommended for board manufacturing with Infineon MEMS microphones.

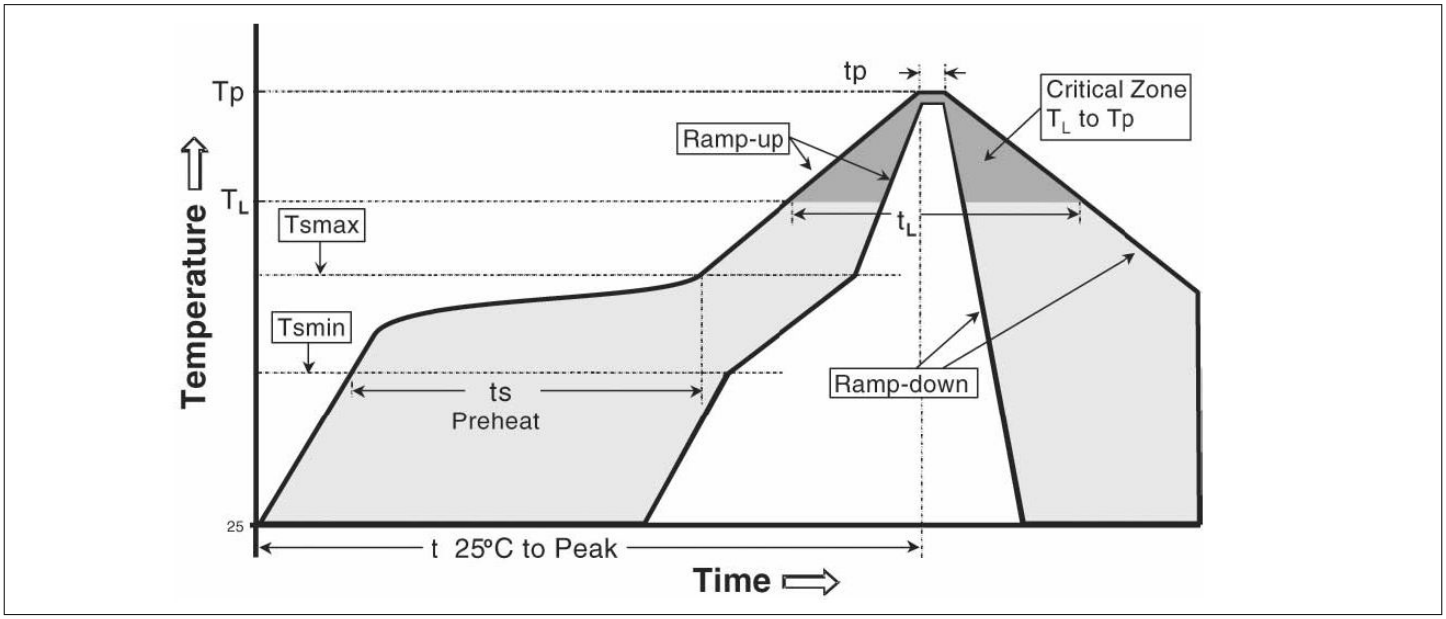

Figure 16 **Recommended reflow profile**

Table 11 **Reflow profile limits**

Profile feature	Pb-Free assembly	Sn-Pb Eutectic assembly
Temperature Min (T_{smin})	150 °C	100 °C
Temperature Max (T_{smax})	200 °C	150 °C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds	60-120 seconds
Ramp-up rate (T_L to T_P)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L)	217 °C	183 °C
Time (t_L) maintained above T_L	60-150 seconds	60-150 seconds
Peak Temperature (T_p)	260°C +0°C/-5°C	235°C +0°C/-5°C
Time within 5°C of actual peak temperature (tp) [9]	20-40 seconds	10-30 seconds
Ramp-down rate	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	8 minutes max.	6 minutes max.

***Note**: For further information please consult the 'General recommendation for assembly of Infineon packages' document which is available on the Infineon Technologies web page*

[9] Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum

The MEMS microphones can be handled using industry standard pick and place equipment. Care should be taken to avoid damage to the microphone structure as follows:

- Do not pick the microphone with vacuum tools which make contact with the microphone acoustic port hole.
- The microphone acoustic port hole should not be exposed to vacuum, this can destroy or damage the MEMS.
- Do not blow air into the microphone acoustic port hole. If an air blow cleaning process is used, the port hole must be sealed to prevent particle contamination.
- It is recommended to perform the PCB assembly in a clean room environment in order to avoid microphone contamination.
- Air blow and ultrasonic cleaning procedures shall not be applied to MEMS Microphones. A no-clean paste is recommended for the assembly to avoid subsequent cleaning steps. The microphone MEMS can be severely damaged by cleaning substances.
- To prevent the blocking or partial blocking of the sound port during PCB assembly, it is recommended to cover the sound port with protective tape during PCB sawing or system assembly.
- Do not use excessive force to place the microphone on the PCB. The use of industry standard pick and place tools is recommended in order to limit the mechanical force exerted on the package.

11 Reliability specifications

The microphone sensitivity after stress must deviate by no more than 3dB from the initial value.

Table 12 Reliability specification

Test	Abbreviation	Test Condition	Standard
Low Temperature Operating Life	LTOL	T_a=-40°C, VDD=3.6V, 1000 hours	JESD22-A108
Low Temperature Storage Life	LTSL	T_a=-40°C, 1000 hours	JESD22-A119
High Temperature Operation Life	HTOL	T_a=+125°C, VDD=3.6V, 1000 hours	JESD22-A108
High Temperature Storage Life	HTSL	T_a=+125°C, 1000 hours	JESD22-A103
Temperature Cycling	PC + TC	Pre conditioning MSL-1	JESD22-A113
		1000 cycles, -40°C to +125°C, 30 minutes per cycle	JESD22-A104
Temperature Humidity Bias	PC + THB	Pre conditioning MSL-1	JESD22-A113
		T_a=+85°C, R.H = 85%, VDD=3.6V, 1000 hours	JESD22-A101
Vibration Test	VVF	20Hz to 2000Hz with a peak acceleration of 20g in X, Y, and Z for 4 minutes each, total 4 -cycles	IEC 60068-2-6
Mechanical Shock	MS	10000g/0.1msec direction ±x,y,z, 5 shocks in each direction, 5 shocks in total	IEC 60068-2-27
Reflow Solder[10)]	RS	3 reflow cycles, peak temperature = +260°C	IPC-JEDEC J-STD-020D-01

(table continues...)

10 The microphone sensitivity must deviate by no more than 1dB from the initial value after 3 reflow cycles.

Table 12 (continued) Reliability specification

Test	Abbreviation	Test Condition	Standard
Electrostatic Discharge -System Level Test	ESD - SLT	3 discharges of ±8kV direct contact to lid while V_{dd} is supplied according to the operational modes; (V_{dd} ground is separated from earth ground)	IEC-61000-4-2
Electrostatic Discharge - Human Body Model	ESD - HBM	1 pulse of ±2kV between all I/O pin combinations	JEDEC-JS001
Electrostatic Discharge - Charged Device Model	ESD - CDM	3 discharges of ±500V direct contact to I/O pins.	JEDEC JS-002

Revision history

Document version	Date of release	Description of changes
v1.0	2024-06-05	Initial release
v1.1	2025-02-25	Fixed typos, no change in acoustic or electrical performance
v1.2	2026-05-04	Fixes to formatting and typos, no change in performance

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Edition 2025-05-04

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference
IFX-hzg1711550963785

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