EZ-PD™ CCG8_CFP USB Type-C Power Delivery controller

General description

EZ-PD™ CCG8_CFP is a dual-port and single-port USB Type-C Power Delivery (PD) controller that complies with the latest USB Type-C and PD specifications. This device provides a complete USB Type-C and USB PD port control solution for dual-role power (DRP) host platforms with Extended power range (EPR) capability. This device includes a VBUS provider path load switch with FETs, integrated current sense, integrated 3:1 SBU MUX with level-shifter and 2:1 SBU MUX with level-shifter[1]. It also contains a hardware CRYPTO block for secure firmware boot and authentication, a 32-bit, 48 MHz Arm® Cortex®-M0+ processor with 128 KB flash and 96 KB ROM, integrating a complete Type-C transceiver including the Type-C termination resistors Rp, Rd, and dead battery Rd[2] termination. EZ-PD™ CCG8_CFP devices are available in a 52-pin QFN package that is compliant with the common footprint package. Both EZ-PD™ CCG8_CFP single- and dual-port variants support EPR up to 28 V without the requirement of any external components.

Applications

- Notebooks and desktops
- Thunderbolt hosts, non-thunderbolt hosts
- Augmented and virtual reality
- Gaming systems
- Docks downstream-facing ports (DFP)[3]

Features

- USB PD
  - Supports the latest USB Power Delivery (USB PD) Specification, rev 3.2
  - EPR capability integrated up to 28 V and up to 48 V using external bill of materials (BOM)
  - Fast role swap (FRS)
  - Extended data messaging
- USB Type-C
  - Integrated current sources for the downstream-facing port (DFP)[3] role (Rp)
    - Default current at 900 mA
    - 1.5 A
    - 3 A
  - Integrated Rd resistor for upstream facing port (UFP)[4] role
  - Integrated VCONN FETs to power EMCA cables
  - Integrated dead battery termination
  - Integrated high-voltage protection on CC and SBU pins to protect against accidental shorts to the VBUS pin on the Type-C connector
- MUX
  - Integrated 3:1 SBU MUX with level-shifter on one Type-C port and 2:1 SBU MUX with level-shifter on the other Type-C port[1] for Alternate modes and closed chasis debug

Notes

1. 2:1 SBU MUX is applicable only for EZ-PD™ CCG8_CFP dual-port devices.
2. See **Ordering information** for specific part numbers that support dead battery Rd termination
3. DFP refers to power source.
4. UFP refers to power sink.

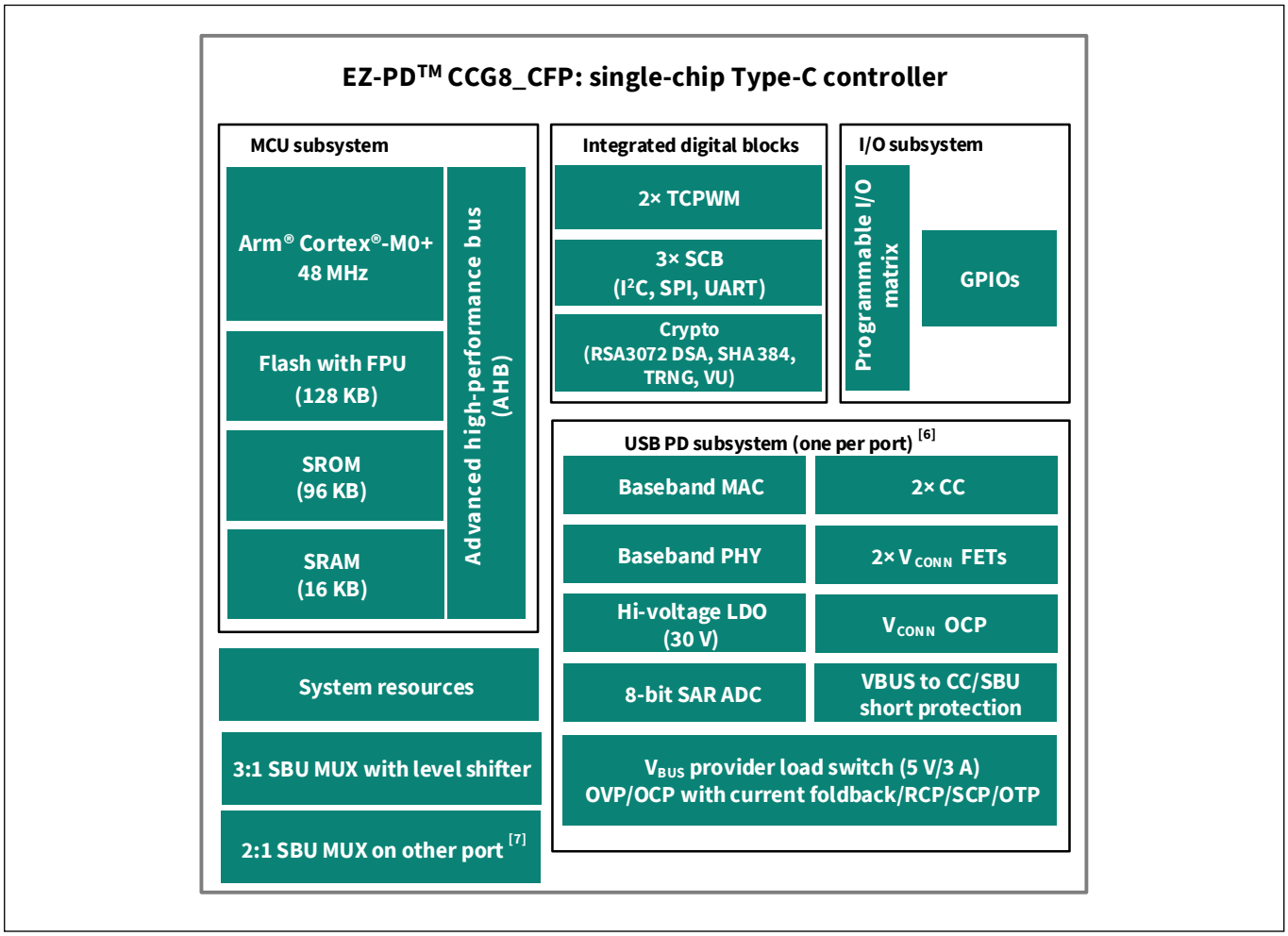
Features

- Integrated provider VBUS load switch[5]
  - Integrated 5 V/3 A back-to-back NFET
  - Slew rate controlled turn-on in the VBUS provider path
  - Configurable overvoltage protection (OVP), overcurrent protection (OCP) with current foldback capability, short-circuit protection (SCP), and reverse-current protection (RCP)
  - Live VBUS current monitoring
  - VBUS discharge NFET on Type-C VBUS
  - Overtemperature protection thermal shutdown using the on-die temperature sensor
- LDO
  - Integrated high-voltage LDO on VBUS for dead battery mode operation
- 32-bit MCU subsystem
  - 48 MHz Arm® Cortex®-M0+ CPU
  - 128 KB flash with FPU
  - 96 KB ROM
  - 16 KB SRAM
- Integrated digital blocks
  - Two TCPWMs that are configurable as timers, counters, or PWMs to meet response times required by the USB PD protocol
  - Three run-time serial communication blocks (SCBs) that can be configured as either I^2C, SPI, or UART peripherals
- Authentication
  - Hardware CRYPTO engine with RSA3072 digital signing algorithm (DSA) and SHA384 hash to support secure boot and authenticated firmware download
  - Vector unit (VU) for asymmetric cryptography capable of performing RSA-3072, SHA384
- Clocks and oscillators
  - Integrated oscillator eliminating the need for an external clock
- Operating range
  - VIN_3V3/VSYS (2.8 V–5.5 V)
  - VBUS (4 V–28 V)
- Packages
  - EZ-PD™ CCG8_CFP: 5.0 × 8.0 × 0.9 mm, 52-pin QFN with 0.4 mm pitch

Notes

5. See **Ordering information** for specific part numbers that support integrated provider FET(s) on the available ports.

Logic block diagram



Notes

6. Only one USB PD subsystem exists for EZ-PD™ CCG8_CFP single-port devices because only one Type-C port is available in the system.
7. 2:1 MUX is applicable only for EZ-PD™ CCG8_CFP dual-port devices on the second Type-C port.

Table of contents

General description 1
Applications 1
Features 1
Logic block diagram 3
Table of contents 4
1 Functional overview 6
1.1 MCU subsystem 7
1.1.1 CPU 7
1.1.2 Memory subsystem (flash, SROM, and RAM) 7
1.2 USB PD subsystem 7
1.2.1 USB PD physical layer 8
1.2.2 VCONN FET 8
1.2.3 ADC 8
1.2.4 SBU MUX 9
1.3 Provider load switch 11
1.3.1 Provider back to back NFET 11
1.3.2 Overvoltage and undervoltage protection on VBUS 11
1.3.3 High-side current sense amplifier for VBUS 11
1.3.4 VBUS reverse current protection 11
1.3.5 VBUS discharge 11
1.3.6 VBUS regulator 11
1.3.7 Gate driver for VBUS provider NFET 11
1.3.8 VBUS tolerant SBU and CC lines 11
1.4 Serial communication block (SCB) 12
1.5 Timer, counter, pulse-width modulator (TCPWM) 12
1.6 CRYPTO accelerator 12
1.7 GPIO interface 12
1.7.1 GPIO power domain 13
1.8 System resources 13
1.8.1 Power system 13
1.8.2 Watchdog timer (WDT) 13
1.8.3 Reset 13
1.8.4 Clock system 13
1.8.5 Internal main oscillator (IMO) clock source 14
1.8.6 Internal low-speed oscillator (ILO) clock source 14
1.8.7 External components 14
2 Power 15
2.1 Power system requirements overview 15
2.2 Power specification 17
3 Pinouts 18
4 Application diagrams 24
5 EZ-PD™ CCG8_CFP layout design guidelines for 52-pin QFN package 28
5.1 Recommended pad size 29
5.2 Stack-up 29
5.3 52-pin QFN fanout 30
5.4 Via count on thermal pads 30
5.5 Via count on power pins 31
5.6 High-Speed routing 31
5.7 CC connections 32
5.8 VDDIO, VCCD, VSYS and VDDD connections 33
5.9 ESD layout 34

Table of contents

6 Electrical specifications 35
6.1 Absolute maximum ratings 35
6.2 Device-level specification 36
6.2.1 DC specifications 36
6.2.2 Global conditions 37
6.2.3 System performance requirements 37
6.2.4 System-level functional requirements 37
6.2.5 GPIO specifications 38
6.2.6 XRES requirements 39
6.2.7 Memory 40
6.2.8 Digital peripherals 41
6.2.9 Power Delivery (PD) peripherals 46
7 Ordering information 54
7.1 Ordering code definitions 54
8 Package diagram 55
Revision history 57

1 Functional overview

This section outlines the different interfaces and the blocks along with the respective operational modes.

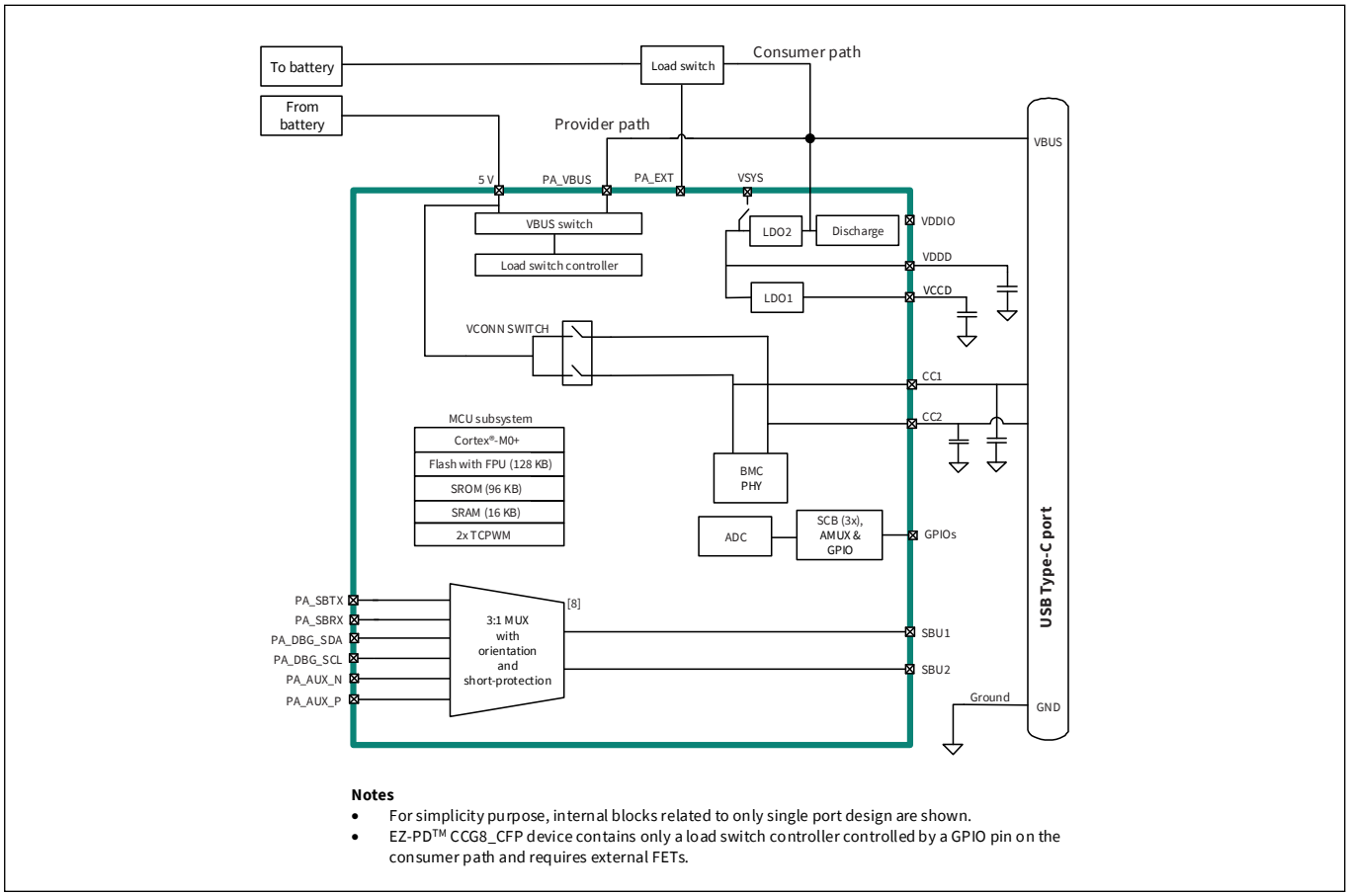


Figure 1 EZ-PD™ CCG8_CFP functional block diagram for single-port device

Notes

8. For dual-port device, 2:1 SBU MUX (without the Px_DBG_SDA and Px_DBG_SCL lines) is present on Port A and 3:1 SBU MUX (with the Px_DBG_SDA & Px_DBG_SCL lines) is present on Port B. x = A or B

1.1 MCU subsystem

1.1.1 CPU

The Arm® Cortex® M0+ is a 32-bit MCU, is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set, which enables fully compatible binary upwards migration of code to higher performance processors such as the Cortex®-M3 and M4. Infineon option includes a hardware multiplier, which provides a 32-bit result in one cycle. It includes an interrupt controller (NVIC block) with 20 Interrupt inputs and a wakeup interrupt controller (WIC), which can wake the processor up from Deep Sleep mode.

1.1.2 Memory subsystem (flash, SROM, and RAM)

The 128 KB flash with FPU and 96 KB ROM store the firmware implementing PD functionality.

The 16 KB RAM is used under software control to store temporary status of system variables and parameters. A supervisory ROM that contains boot and configuration routines is provided.

1.2 USB PD subsystem

This subsystem provides an interface to the Type-C USB port and includes the following:

- USB PD physical layer
- VBUS provider FETs
- VCONN FETs
- ADC
- SBU MUX
- Fault protection: Undervoltage protection (UVP), overvoltage protection (OVP), overcurrent protection (OCP) with current foldback capability, short-circuit protection (SCP), and reverse-current protection (RCP) on VBUS
- High-side current sense amplifier for VBUS
- VBUS discharge
- VBUS regulator
- Provider gate driver for VBUS integrated NFET with FRS
- VBUS-tolerant SBU and CC pins

1.2.1 USB PD physical layer

The USB PD subsystem contains the USB PD physical layer block and supporting circuits. The USB PD physical layer consists of a transmitter and receiver that communicate BMC encoded data over the CC channel per the USB PD 3.1 standard. All communication is half-duplex. The physical layer or PHY practices collision avoidance to minimize communication errors on the channel.

In addition, the USB PD block includes all termination resistors (Rp and Rd) and their switches as required by the USB Type-C specification. Rp and Rd resistors are required to implement connection detection, plug orientation detection and for establishment of the USB source/sink roles. The Rp resistor is implemented as a current source.

The Rd resistor on CC pins are required even when the part is not powered on. This is required for dead battery termination detection and charging.

To support the latest USB PD 3.1 Specification, EZ-PD™ CCG8_CFP single-port and dual-port devices implement the fast role swap (FRS) feature. FRS enables externally powered docks and hubs to rapidly switch to bus power when their external power supply is removed. This feature is supported for provider path.

For more details, see to section 6.3.17 in USB PD 3.2 Specification.

EZ-PD™ CCG8_CFP is fully interoperable with both rev 3.0 and rev 2.0 of the USB Power Delivery Specification.

For detailed requirements, see the following specs:

- Power Delivery Specification rev 3.2
- USB Type-C Specification 2.2 Release

1.2.2 VCONN FET

EZ-PD™ CCG8_CFP sources the power from a 5 V pin to power the EMCA cables through integrated VCONN FETs. Two VCONN FETs are available in EZ-PD™ CCG8_CFP to power either CC1 or CC2 pins. These FETs will source a minimum of 1.5 W power per port over the valid VCONN range of 4.85 V to 5.5 V on the CC1/2 pins when providing power to EMCA cables. At any given time, only one of the VCONN FETs shall be ON. Floating VBUS_P/V5V pin should not cause EZ-PD™ CCG8_CFP to malfunction and draw more current. EZ-PD™ CCG8_CFP implements OCP on VCONN with 350 mA–900 mA min-max limits. CC1 and CC2 are protected from accidental short to VBUS.

1.2.3 ADC

The ADC is a low-footprint 8-bit SAR ADC available for general purpose A–D conversion applications in the chip. The ADC can be accessed from the GPIOs through an on-chip analog MUX. In EZ-PD™ CCG8_CFP, one ADC shall be instantiated per PD port.

1.2.4 SBU MUX

EZ-PD™ CCG8_CFP dual-port device has an integrated 3:1 SBU MUX with level shifter on Port-B and 2:1 SBU MUX with level shifter on Port-A. The EZ-PD™ CCG8_CFP single-port device has integrated 3:1 SBU MUX with level shifter on its port. The Type-C facing SBU pins are protected from accidental short to VBUS.

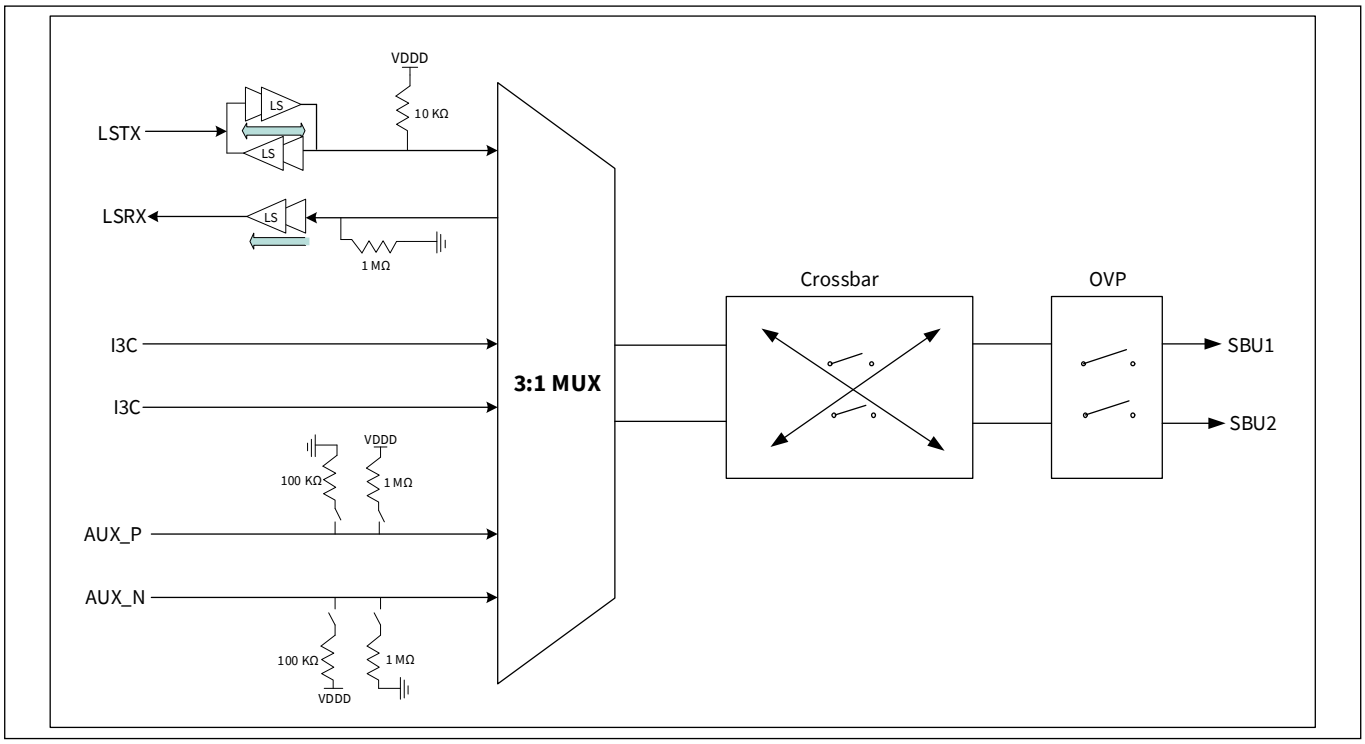


Figure 2 SBU protection and high-speed crossbar switch block diagram

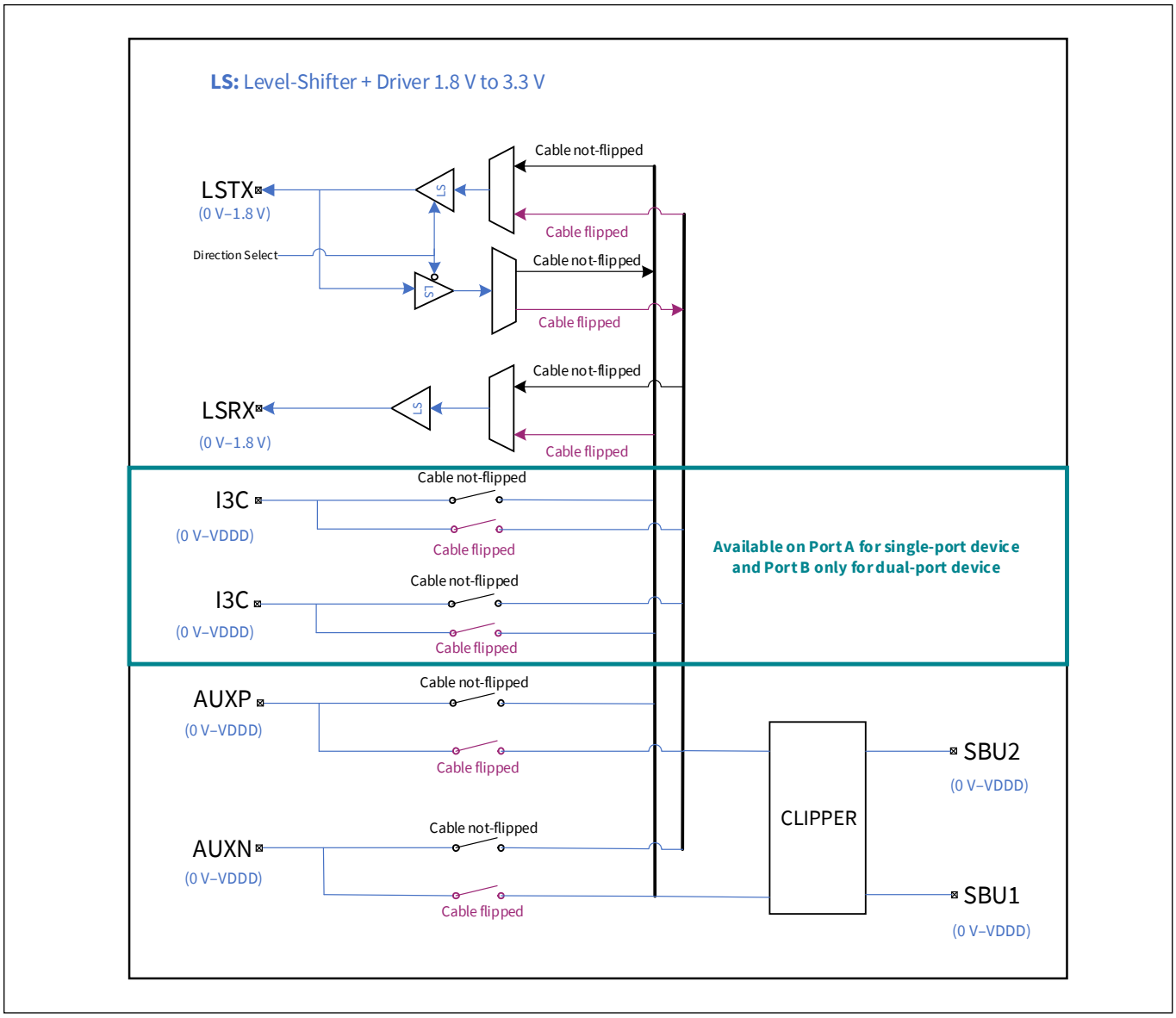


Figure 3 High-speed crossbar switch internal block diagram

By default, the SBU to DBG path is enabled at power-up (or RESET) and the OVP limit is set to 1.8 V. For any changes namely, enabling LSx path, FW must intervene and disable the DBG path switches and then enable the LSx path. There is no RTL control to do this. Leakage specification is not specified on SBU pins; therefore; the OVP circuit is left enabled at power-up as well in all EZ-PD™ CCGX devices.

1.3 Provider load switch

1.3.1 Provider back to back NFET

EZ-PD™ CCG8_CFP includes 5 V/3 A back to back NFETs on each USB Type-C port. EZ-PD™ CCG8_CFP dual-port device supports 3 A on both the ports simultaneously.

1.3.2 Overvoltage and undervoltage protection on VBUS

The chip implements an undervoltage/overvoltage (UVOV) detection circuit for the VBUS supply. The thresholds for both OCP and UVOV are programmable.

1.3.3 High-side current sense amplifier for VBUS

The chip supports programmable threshold VBUS current sensing through VBUS path. The current through the provider NFET is monitored using special replica transistors and the data is used to implement various functions such as OCP detection, SCP detection, current foldback (limiting the current instead of turning off the FET completely) and live VBUS current monitoring. For live VBUS current monitoring feature, the chip is expected to be in Active mode becuase ADC is required to convert the analog signal to digital domain. There exists a current foldback option and so SCP block does not need to be accurate and will only be used to detect hard and fast shorts. For slow shorts, the current foldback will kick-in and ensure lower current till such time as overtemperature protection triggers.

1.3.4 VBUS reverse current protection

EZ-PD™ CCG8_CFP restricts reverse current on VBUS provider path when Type-C VBUS is greater than VIN (provider voltage before the VBUS NFET). EZ-PD™ CCG8_CFP reacts quickly and turns off the VBUS provider NFET. This feature is not supported on consumer path and there will be reverse current whenever the consumer side voltage is higher than connector side voltage on the consumer path.

1.3.5 VBUS discharge

The chip supports high-voltage (28 V) VBUS discharge circuitry inside. After cable removal detection, the chip will discharge the residual charge and bring the floating VBUS back to 0 V.

1.3.6 VBUS regulator

The chip has three (in case of dual-port device)/two (in case of single-port device) input power supplies – VSYS (2.8 V–5.5 V) and VBUS (Port0 and Port1). A regulator operating on these three power supplies will drive the chip operating supply. VSYS always takes priority over VBUS. In the absence of VSYS, the regulator powers the chip from VBUS (Port0 or Port1, whichever is present).

1.3.7 Gate driver for VBUS provider NFET

EZ-PD™ CCG8_CFP has integrated gate driver to drive NFETs on the VBUS provider path. As with other devices in CCGx family that support FRS feature, EZ-PD™ CCG8_CFP also has limitations like over temperature protection, OCP, SCP and RCP fault detections and ILIMIT features are disabled during the FRS event and assuming that provider side supply is present and higher than 4.9 V during the course of FRS event.

1.3.8 VBUS tolerant SBU and CC lines

The chip supports VBUS tolerant SBU and CC lines. In case of SBU/CC short to VBUS through connectors, these lines will be protected internally. Accidental shorts may occur because the SBU/CC pins are placed next to the VBUS pins in the USB Type-C connector. A Power Delivery controller without the high-voltage VBUS short protection will be damaged in the event of accidental shorts. The cable interface will be shut-off when overvoltage is detected on SBU/CC lines. When the protection circuit is triggered, EZ-PD™ CCG8_CFP can handle up to VBUS voltage forever.

1.4 Serial communication block (SCB)

EZ-PD™ CCG8_CFP has three SCB blocks that can be configured for I2C, SPI, or UART. These blocks implement full multimaster and slave I2C interfaces capable of multimaster arbitration. I2C is compatible with the standard Philips I2C Specification V3.0. These blocks can operate at speeds of up to 1 Mbps and have flexible buffering options to reduce interrupt overhead and latency for the CPU.

The SCB blocks support 8-deep FIFOs for receive and transmit, which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time. The FIFO mode is very useful in the absence of DMA. Data throughput is not a critical consideration for I2C. The I2C port I/Os for SCB0 are fail-safe. The I2C port for SCB1–2 are not fail-safe compliant.

1.5 Timer, counter, pulse-width modulator (TCPWM)

The TCPWM block of EZ-PD™ CCG8_CFP supports up to two timers or counters or pulse width modulators. These timers are available for internal timer use by firmware or for providing PWM-based functions on the GPIOs.

1.6 CRYPTO accelerator

The CRYPTO accelerator block will support below requirements:

- Vector unit (VU) to support asymmetric key cryptography
- SHA2 (384-bit)
- Vector unit for asymmetric cryptography capable of performing RSA-3072
- AES (128-bit) supports forward block cipher
- True random number generator (AIS-31 compliant)

1.7 GPIO interface

The EZ-PD™ CCG8_CFP die has 20 GPIOs including the I2C, and SWD pins, which can also be used as GPIOs.

The GPIO block implements the following:

- Eight drive strength modes including strong push-pull, resistive pull-up and pull-down, weak (resistive) pull-up and pull-down, open drain and open source, input only, and disabled.
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output disables
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control

During Power-on and Reset, the blocks are forced to the Disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals such as USB Type-C port are also fixed to reduce internal multiplexing complexity. Data Output and Pin State Registers store the values to be driven on the pins and the states of the pins themselves, respectively. The configuration of the pins can be done by programming of registers through software for each digital I/O Port.

Every I/O pin can generate an interrupt if enabled and each I/O Port has an Interrupt Request (IRQ) and Interrupt Service Routine (ISR) Vector associated with it.

The I/O Ports can retain their state during Deep Sleep mode or remain ON. If operation is restored using reset, the pins will go to the High-Z state. If operation is restored by an interrupt event, then the pin drivers will retain their state until firmware chooses to change it. The I/Os (on data bus) do not draw current on power down.

1.7.1 GPIO power domain

All the GPIOs except PA_EXT and PB_EXT[9] reside in a separate I/O power domain called VDDIO. PA_EXT and PB_EXT[9] reside in the VDDD power domain. The separate VDDIO I/O power domain provides flexible system level interfacing.

1.8 System resources

1.8.1 Power system

The power system is described in detail in the **Power** section. Briefly, it provides assurance that voltage levels are as required for each respective mode and will either delay mode entry (on Power-On-Reset (POR) for instance) until voltage levels are as required for proper function or will generate Resets (brownout (BO) detection).

1.8.2 Watchdog timer (WDT)

A watchdog timer is implemented in the Clock block running from the internal low-speed oscillator (ILO). This allows watchdog operation during Deep Sleep and generate a Watchdog Reset if not serviced before the timeout occurs. The Watchdog Reset is recorded in the Reset Cause register.

1.8.3 Reset

EZ-PD™ CCG8_CFP can be reset from variety of sources including a Software Reset. Reset events are asynchronous and guarantee reversion to a known state. The Reset cause is recorded in a Register, which is sticky through Reset and allows software to determine the cause of the reset. A XRES Pin is reserved for External Reset to avoid complications with configuration and multiple pin functions during Power-on or reconfiguration.

1.8.4 Clock system

EZ-PD™ CCG8_CFP has a fully integrated clock with no external crystal required.

EZ-PD™ CCG8_CFP Clock system provides clocks to all subsystems that require clocks (SCB and PD) and for switching between different clock sources, without glitches. In addition, the clock system ensures that no metastable conditions occur.

The Clock system for EZ-PD™ CCG8_CFP is a strict subset of the M0S8 platform. It consists of the internal main oscillator (IMO) and the internal low-speed oscillator (ILO).

The high-frequency clock (HFCLK) signal can be divided down as shown to generate synchronous clocks for the Digital Peripherals. The clock dividers have 8-bit, 16-bit and 16-bit fractional divide capability. The 16-bit capability allows a lot of flexibility in generating fine-grained frequency values. The Clock dividers generate either enabled clocks (that is, 1 in N clocking where N is the divisor) or an approximately 50% duty cycle clock (exactly 50% for even divisors, one clock difference in the high and low values for odd divisors). In **Figure 4**, PERXYZCLK represents the clocks for different peripherals.

Note
9. Applicable to dual-port device only.

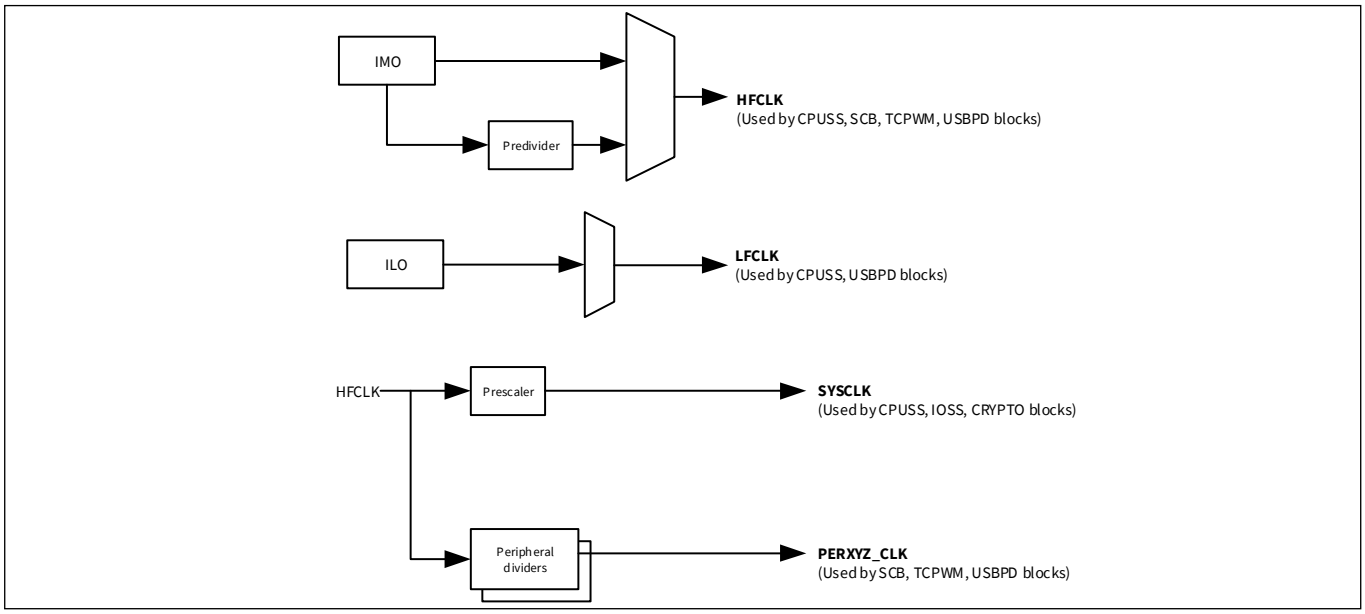


Figure 4 EZ-PD™ CCG8_CFP clocking architecture

1.8.5 Internal main oscillator (IMO) clock source

The internal main oscillator is the primary source of internal clocking in EZ-PD™ CCG8_CFP. It is trimmed during production to achieve the desired accuracy of ±2%. Trim values are stored in supervisory rows in the flash memory. Additional trim settings from Flash can be used to compensate for changes. IMO default frequency for EZ-PD™ CCG8_CFP is 48 MHz ± 2%.

1.8.6 Internal low-speed oscillator (ILO) clock source

The internal low-power oscillator is a very low power, relatively inaccurate oscillator, which is primarily used to generate clocks for peripheral operation in Deep Sleep mode. It is a 32 kHz oscillator with untrimmed accuracy of –70% to +150% and it is capable of being trimmed within ±55%.

1.8.7 External components

EZ-PD™ CCG8_CFP is optimized for a low-cost/low-footprint notebook application. As such, it can operate with a minimum set of external components. The only components required are decoupling capacitors as follows: 4.7 µF capacitor on VDDD, 1 µF for VDDIO, and for VCCD. System will need an external consumer load switch.

2 Power

2.1 Power system requirements overview

Figure 5 shows an overview of the power system requirements for EZ-PD™ CCG8_CFP dual-port system and **Figure 6** shows an overview of the power system requirements for EZ-PD™ CCG8_CFP single-port system. EZ-PD™ CCG8_CFP is able to operate from three possible external supply sources VSYS and Type-C VBUS C (Port 1/2). The VBUS_P/V5V (Port 1/2) supply supports operation over 4.85 V–5.5 V while the VSYS input supports operation over 2.8 V–5.5 V. EZ-PD™ CCG8_CFP has two different power modes: Active and Deep Sleep, transitions between which are managed by the Power system. VDDD is either powered from VBUS_C regulators generating an output of 2.7 V to 3.6 V or is connected to VSYS pin through a power switch. The VCCD pin, the output of the core (1.8 V) regulator, is brought out for connecting a 1 µF capacitor for the regulator stability only. This pin is not supported as a power supply. A separate power domain VDDIO is provided for the GPIOs. VDDIO is expected to be either shorted to VDDD or connected to an external 1.8 V supply that is generated from the VDDD output or from system supply[10].

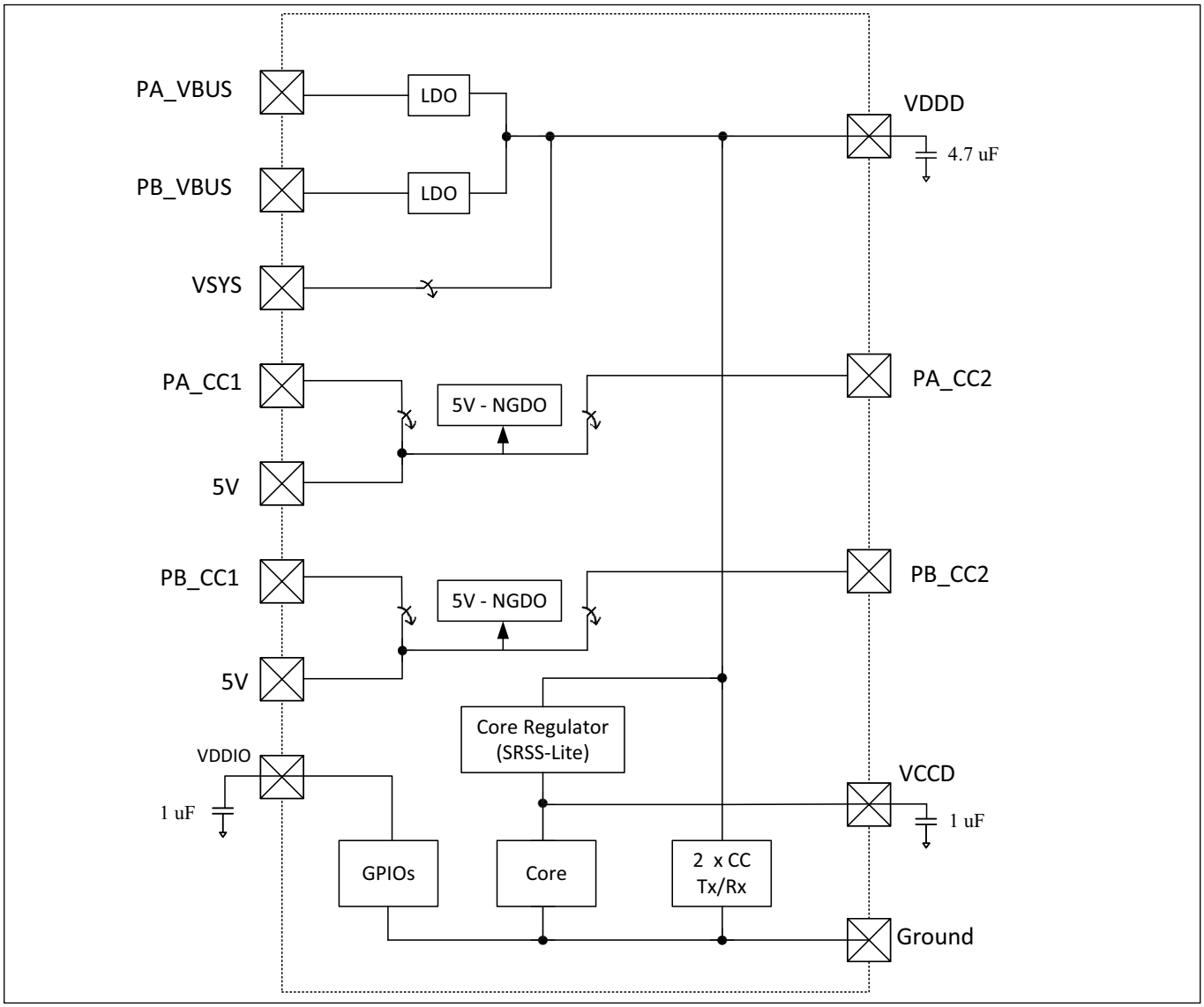


Figure 5 EZ-PD™ CCG8_CFP dual-port power system requirement block diagram

Note
10.If the 1.8 V is derived from system supply, ensure that VDDD is stable before VDDIO is supplied.

Power

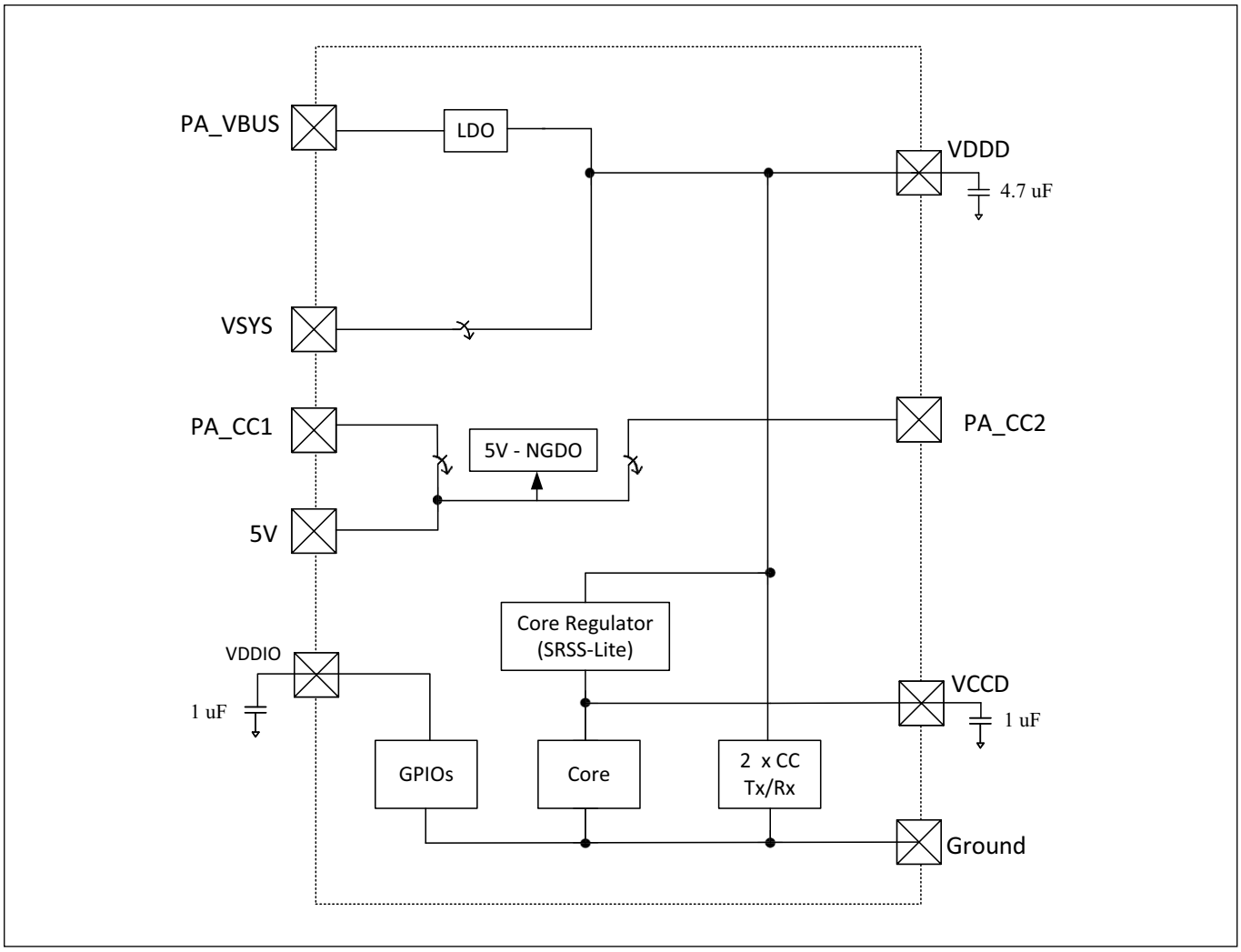


Figure 6 EZ-PD™ CCG8_CFP single-port power system requirement block diagram

2.2 Power specification

See **Electrical specifications** for all quantifiable power specifications.

Table 1 EZ-PD™ CCG8_CFP dual- and single-port power modes

Mode	Description
Reset	Power is valid and XRES is not asserted. An internal reset source is asserted or sleep controller is sequencing the system out of reset.
Active	Power is valid and CPU is executing instructions. This mode includes the critical Type-C power spec requirement.
Deep Sleep	Main regulator and most hard-IP are shut off. Deep Sleep regulator powers logic, but only low-frequency clock is available.

3 Pinouts

Table 2 EZ-PD™ CCG8_CFP single-port pinout

Pin name	Port	Pinout	Pin description
N/C	–	1–10	No connect
PA_DBG_SDA	MUX	11	PORTA SBU MUX output connected to PA_SBU1 during debug mode
PA_DBG_SCL	MUX	12	PORTA SBU MUX output connected to PA_SBU2 during debug mode
GND	GND	13	Ground reference pin. Ties to underside power pad.
GPIO0/RTM_RST/P0.0	GPIO	14	GPIO or reset signals from PD controller to retimer
GPIO1/P0.1	GPIO	15	General purpose I/O
GPIO2/RTM_EN/P0.2	GPIO	16	GPIO or retimer-A load switch enable
GPIO3/P0.3	GPIO	17	General purpose I/O
I2C1_IRQ/P0.4	GPIO	18	Embedded controller interrupt (IRQ for I2C1)
I2C1_SCL/P1.0[11]	GPIO	19	I2C1 clock for communicating with embedded controller
I2C1_SDA/P1.1[11]	GPIO	20	I2C1 data for communicating with embedded controller
I2C2_IRQ/P2.0	GPIO	21	Thunderbolt interrupt (IRQ for I2C2)
I2C2_SCL/P2.1	GPIO	22	I2C2 clock for communicating with SoC or TBT controller
I2C2_SDA/P2.2	GPIO	23	I2C2 data for communicating with SoC or TBT controller
XRES	Power	24	Reset pin (EZ-PD™ CCG8_CFP specific, not a GPIO pin)
I2C3_SCL/P2.3	GPIO	25	I2C3 clock for configuring retimer or DP/USB multi-function MUX
I2C3_SDA/P2.4	GPIO	26	I2C3 data for configuring retimer or DP/USB multi-function MUX
GPIO4/LSTX_DIR_SEL/ SWD_IO/P5.0	GPIO	27	GPIO, LSTX direction select or Serial Wire Debug (SWD) I/O.
GPIO5/SWD_CLK/P5.1	GPIO	28	GPIO or Serial Wire Debug (SWD) CLK
LDO1 (VCCD)	Power	29	Output of internal LDO. Bypass with capacitance to GND. This is not intended to source external circuits.
LDO2 (VDDD)	Power	30	Output of supply switched from VIN_3V3 or VBUS LDO. Bypass with capacitance to GND.
VDDIO	Power	31	I/O supply voltage. This should be connected to an external 1.8 V or 3.3 V rail in the system or LDO2.
VIN_3V3 (VSYS)	Power	32	Supply for core circuitry and I/O. Bypass with capacitor to GND.
PA_SBRX	MUX	33	PORTA SBU MUX output for the SBRX channel (LSRX). LSRX pin operates at 1.8 V by default. Use level-shifter for 3.3 V operation.
PA_SBTX	MUX	34	PORTA SBU MUX output for the SBTX channel (LSTX). LSTX pin operates at 1.8 V by default. Use level-shifter for 3.3 V operation.
PA_AUX_N	Analog	35	PORTA SBU MUX output for the AUX_N channel
PA_AUX_P	Analog	36	PORTA SBU MUX output for the AUX_P channel

Notes

11. The pins indicated are fail-safe. The fail-safe feature ensures that, in the absence of VBUS/VSYS power, a logic high level on these pins due to I2C line activity will not back-power the MCU.
12. The pins indicated are controlled by VDDD and not VDDIO.
13. This is also referenced as VBUS_P, VBUS_P_P0 or V5V in this document.

Pinouts

Table 2 EZ-PD™ CCG8_CFP single-port pinout *(continued)*

Pin name	Port	Pinout	Pin description
PA_SBU2	Analog	37	SBU MUX input for SBU2 from the PORTA USB Type-C connector
PA_SBU1	Analog	38	SBU MUX input for SBU1 from the PORTA USB Type-C connector
PA_CC2	Analog	39	Port A CC1/VCONN for USB PD
PA_CC1	Analog	40	Port A CC2/VCONN for USB PD
PA_VBUS	Power	41, 42	PORTA VBUS sense input and 5-V output from PP5V
PA_EXT/P4.0[12]	GPIO	43	This is a GPIO for controlling an external power path on PORTA. Can be used for sink and source load switches.
GPIO6/FAULT#/P3.0	GPIO	44	GPIO or OCP for port
GPIO7/DEBUG#/P3.1	GPIO	45	GPIO or firmware independent debug
5 V[13]	Power	46, 47, 48, 49	5 V system supply to Px_VBUS and supply for Px_CCy pins as VCONN
GPIO8/PROCHOT#/P3.2	GPIO	50	GPIO or PROCHOT#
GPIO9/P4.1	GPIO	51	General purpose I/O
I2CADDR/P3.3	GPIO	52	Configuration input. Connect to resistor divider between VDDIO and GND.
Ground	Ground	–	EPAD

Notes

11. The pins indicated are fail-safe. The fail-safe feature ensures that, in the absence of VBUS/VSYS power, a logic high level on these pins due to I2C line activity will not back-power the MCU.
12. The pins indicated are controlled by VDDD and not VDDIO.
13. This is also referenced as VBUS_P, VBUS_P_P0 or V5V in this document.

Pinouts

Table 3 EZ-PD™ CCG8_CFP dual-port pinout

Pin name	Port	Pinout	Pin description
PB_VBUS	Power	1, 2	PORTB VBUS sense input and 5-V output from PP5V
PB_CC1	Analog	3	PORTB CC1/VCONN for USB PD
PB_CC2	Analog	4	PORTB CC2/VCONN for USB PD
PB_SBU1	Analog	5	SBU MUX input for SBU1 from the PORTB USB Type-C connector
PB_SBU2	Analog	6	SBU MUX input for SBU2 from the PORTB USB Type-C connector
PB_AUX_P	Analog	7	PORTB SBU MUX output for the AUX_P channel
PB_AUX_N	Analog	8	PORTB SBU MUX output for the AUX_N channel
PB_SBTX	MUX	9	PORTB SBU MUX output for the SBTX channel (LSTX). LSTX pin operates at 1.8 V by default. Use level-shifter for 3.3 V operation.
PB_SBRX	MUX	10	PORTB SBU MUX output for the SBRX channel (LSRX). LSRX pin operates at 1.8 V by default. Use level-shifter for 3.3 V operation.
PB_DBG_SDA	MUX	11	PORTB SBU MUX output connected to PB_SBU1 during debug mode
PB_DBG_SCL	MUX	12	PORTB SBU MUX output connected to PB_SBU2 during debug mode
GND	GND	13	Ground reference pin. Ties to underside power pad.
GPIO0/RTM_RST_A/ P0.0	GPIO	14	GPIO or reset signals from PD controller to retimer-A
GPIO1/RTM_RST_B/ P0.1	GPIO	15	GPIO or reset signals from PD controller to retimer-B
GPIO2/RTM_EN_A/P0.2	GPIO	16	GPIO or retimer-A load switch enable
GPIO3/RTM_EN_B/P0.3	GPIO	17	GPIO or retimer-B load switch enable
I2C1_IRQ/P0.4	GPIO	18	Embedded controller interrupt (IRQ for I2C1)
I2C1_SCL/P1.0[14]	GPIO	19	I2C1 clock for communicating with embedded controller
I2C1_SDA/P1.1[14]	GPIO	20	I2C1 data for communicating with embedded controller
I2C2_IRQ/P2.0	GPIO	21	Thunderbolt interrupt (IRQ for I2C2)
I2C2_SCL/P2.1	GPIO	22	I2C2 clock for communicating with SoC or TBT controller
I2C2_SDA/P2.2	GPIO	23	I2C2 data for communicating with SoC or TBT controller
XRES	Power	24	Reset pin (EZ-PD™ CCG8_CFP specific, not a GPIO pin)
I2C3_SCL/P2.3	GPIO	25	I2C3 clock for configuring retimer or DP/USB multi-function MUX
I2C3_SDA/P2.4	GPIO	26	I2C3 data for configuring retimer or DP/USB multi-function MUX
GPIO4/ LSTX_DIR_SEL_A/ SWD_IO/P5.0	GPIO	27	GPIO, LSTX direction select – A or Serial Wire Debug (SWD) I/O. LSTX pin operates at 1.8 V by default. Use level-shifter for 3.3 V operation.
GPIO5/ LSTX_DIR_SEL_B/ SWD_CLK/P5.1	GPIO	28	GPIO, LSTX direction select – B or Serial Wire Debug (SWD) clock.

Notes

14. The pins indicated are fail-safe. The fail-safe feature ensures that, in the absence of VBUS/VSYS power, a logic high level on these pins due to I2C line activity will not back-power the MCU.
15. The pins indicated are controlled by VDDD and not VDDIO.
16. This is also referenced as VBUS_P, VBUS_P_Px or V5V in this document; x = port number (0 or 1)

Pinouts

Table 3 EZ-PD™ CCG8_CFP dual-port pinout *(continued)*

Pin name	Port	Pinout	Pin description
LDO1 (VCCD)	Power	29	Output of internal LDO. Bypass with capacitance to GND. This is not intended to source external circuits.
LDO2 (VDDD)	Power	30	Output of supply switched from VIN_3V3 or VBUS LDO. Bypass with capacitance to GND.
VDDIO	Power	31	I/O supply voltage. This should be connected to an external 1.8 V or 3.3 V rail in the system or LDO2.
VIN_3V3 (VSYS)	Power	32	Supply for core circuitry and I/O. Bypass with capacitor to GND.
PA_SBRX	Digital MUX	33	PORTA SBU MUX output for the SBRX channel (LSRX). LSRX pin operates at 1.8 V by default. Use level-shifter for 3.3 V operation.
PA_SBTX	Digital MUX	34	PORTA SBU MUX output for the SBTX channel (LSTX). LSTX pin operates at 1.8 V by default. Use level-shifter for 3.3 V operation.
PA_AUX_N	GPIO	35	PORTA SBU MUX output for the AUX_N channel
PA_AUX_P	GPIO	36	PORTA SBU MUX output for the AUX_P channel
PA_SBU2	Analog	37	SBU MUX input for SBU2 from the PORTA USB Type-C connector
PA_SBU1	Analog	38	SBU MUX input for SBU1 from the PORTA USB Type-C connector
PA_CC2	GPIO	39	Port A CC1/VCONN for USB PD
PA_CC1	GPIO	40	Port A CC2/VCONN for USB PD
PA_VBUS	Power	41, 42	PORTA VBUS sense input and 5-V output from PP5V
PA_EXT/P4.0[15]	GPIO	43	This is a GPIO for controlling an external power path on PORTA. Can be used for sink and source load switches.
GPIO6/FAULT#/P3.0	GPIO	44	General purpose I/O or OCP for PORTA/B
GPIO7/DEBUG#/3.1	GPIO	45	General purpose I/O or firmware independent debug
5 V[16]	Power	46, 47, 48, 49	5-V system supply to Px_VBUS and supply for Px_CCy pins as VCONN
GPIO8/PROTCHOT#/P3.2	GPIO	50	GPIO or PROCHOT#
GPIO9/PB_EXT/4.1[15]	GPIO	51	This is a GPIO for controlling an external power path on PORTB. Can be used for sink and source load switches.
I2CADDR/P3.3	GPIO	52	Configuration input. Connect to resistor divider between VDDIO and GND.
Ground	Ground	–	EPAD

Notes

14. The pins indicated are fail-safe. The fail-safe feature ensures that, in the absence of VBUS/VSYS power, a logic high level on these pins due to I2C line activity will not back-power the MCU.
15. The pins indicated are controlled by VDDD and not VDDIO.
16. This is also referenced as VBUS_P, VBUS_P_Px or V5V in this document; x = port number (0 or 1)

Note: EZ-PD™ CCG8_CFP device supports 1.8 V operation on GPIO pins per port basis with open drain configuration. If 1.8 V operation is needed on GPIO pins, an external pull-up resistor needs to be connected. This note is not applicable if the VDDIO pin is connected to 1.8 V.

Pinouts

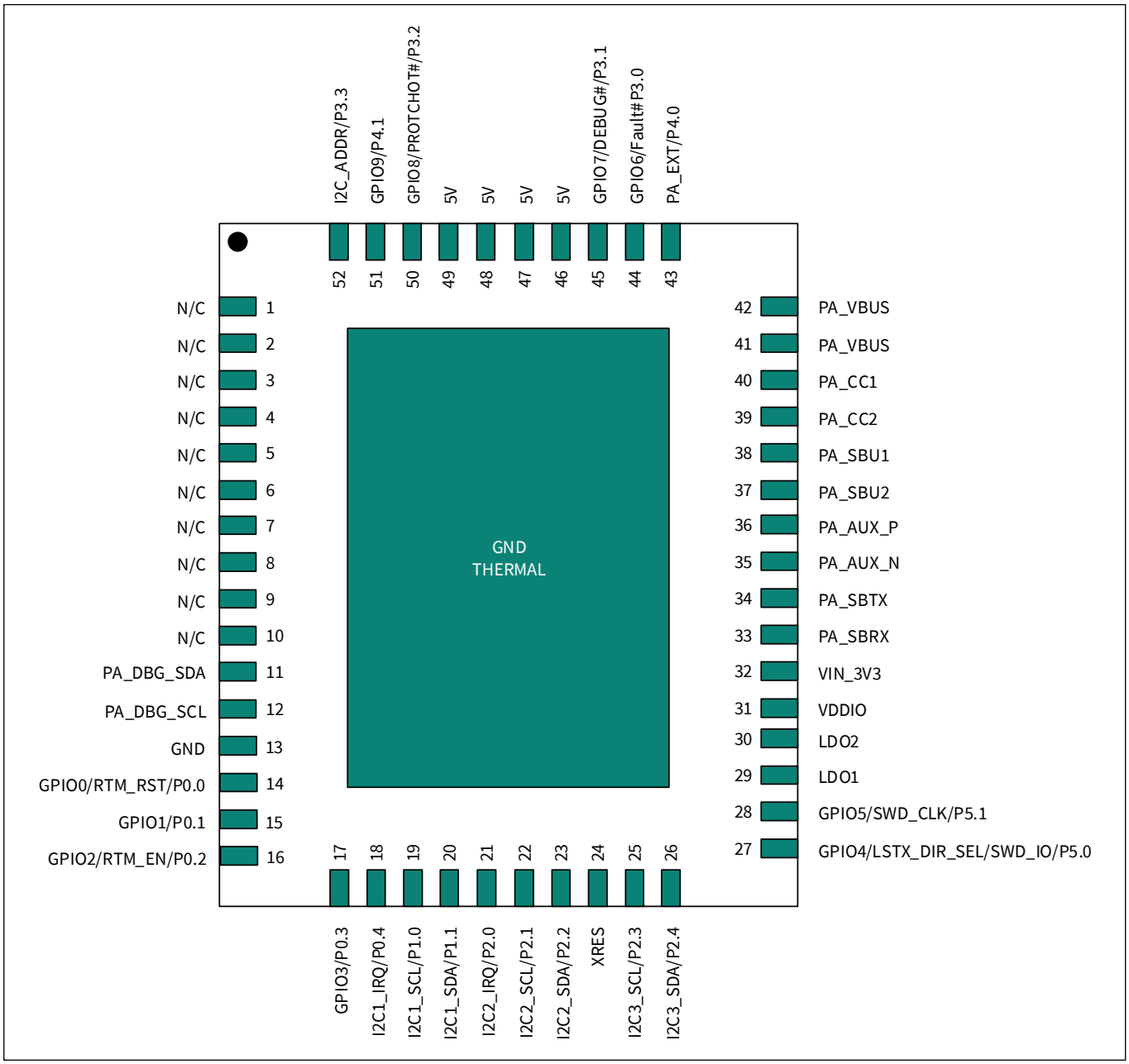


Figure 7 EZ-PD™ CCG8_CFP single-port 52-pin QFN pinout

Pinouts

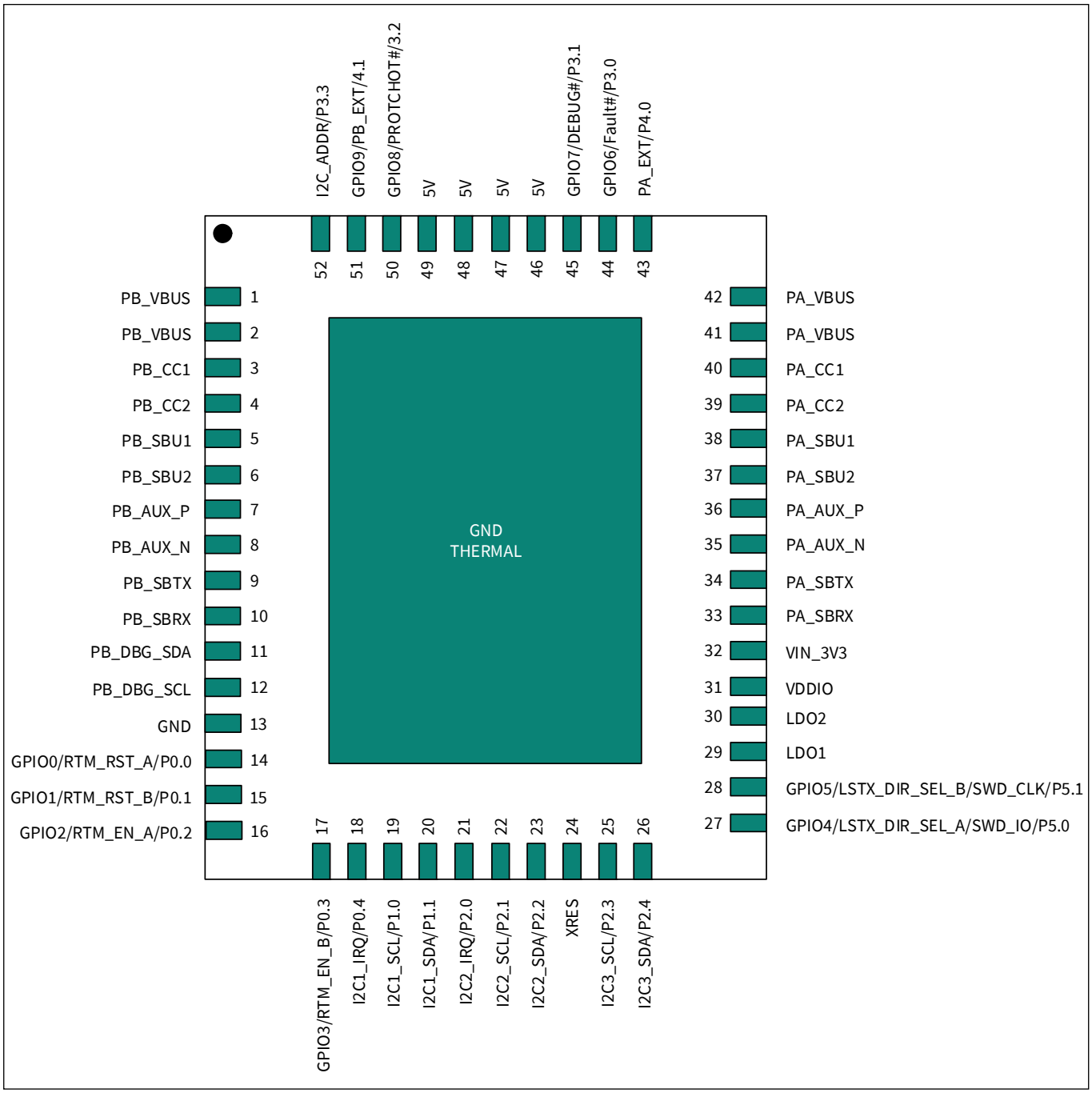


Figure 8 EZ-PD™ CCG8_CFP dual-port 52-pin QFN pinout

4 Application diagrams

Figure 9 shows the application block diagram using EZ-PD™ CCG8_CFP single-port device when VDDIO is set to 3.3 V in a 28 V EPR host system.

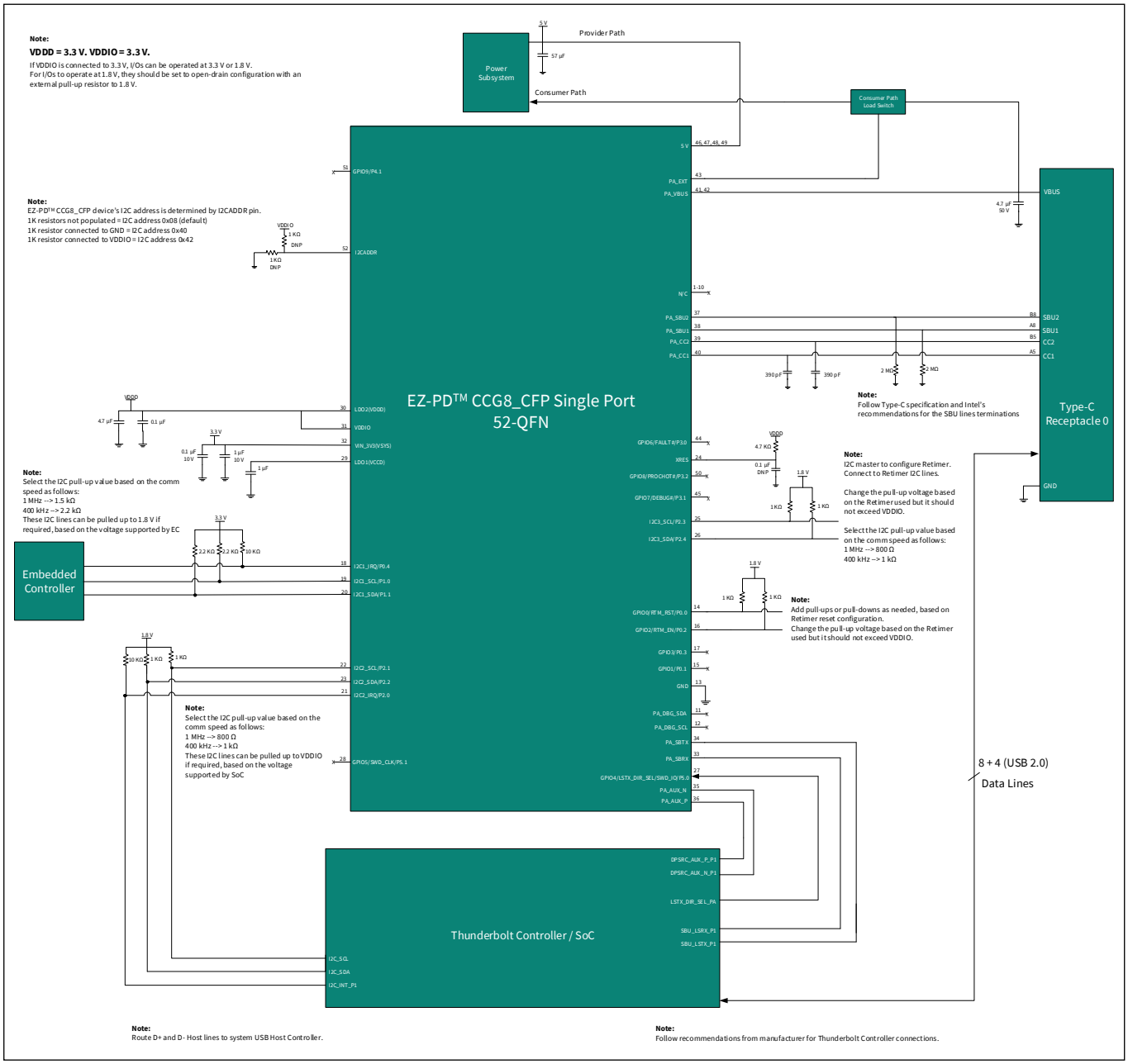


Figure 9 EZ-PD™ CCG8_CFP single-port application block diagram with VDDIO = 3.3 V

Note: *See the **Knowledge Base (KB)** article for information on ESD diode selection.*

Application diagrams

Figure 10 shows the application block diagram using EZ-PD™ CCG8_CFP single-port device when VDDIO is set to 1.8 V in a 28 V EPR Host system.

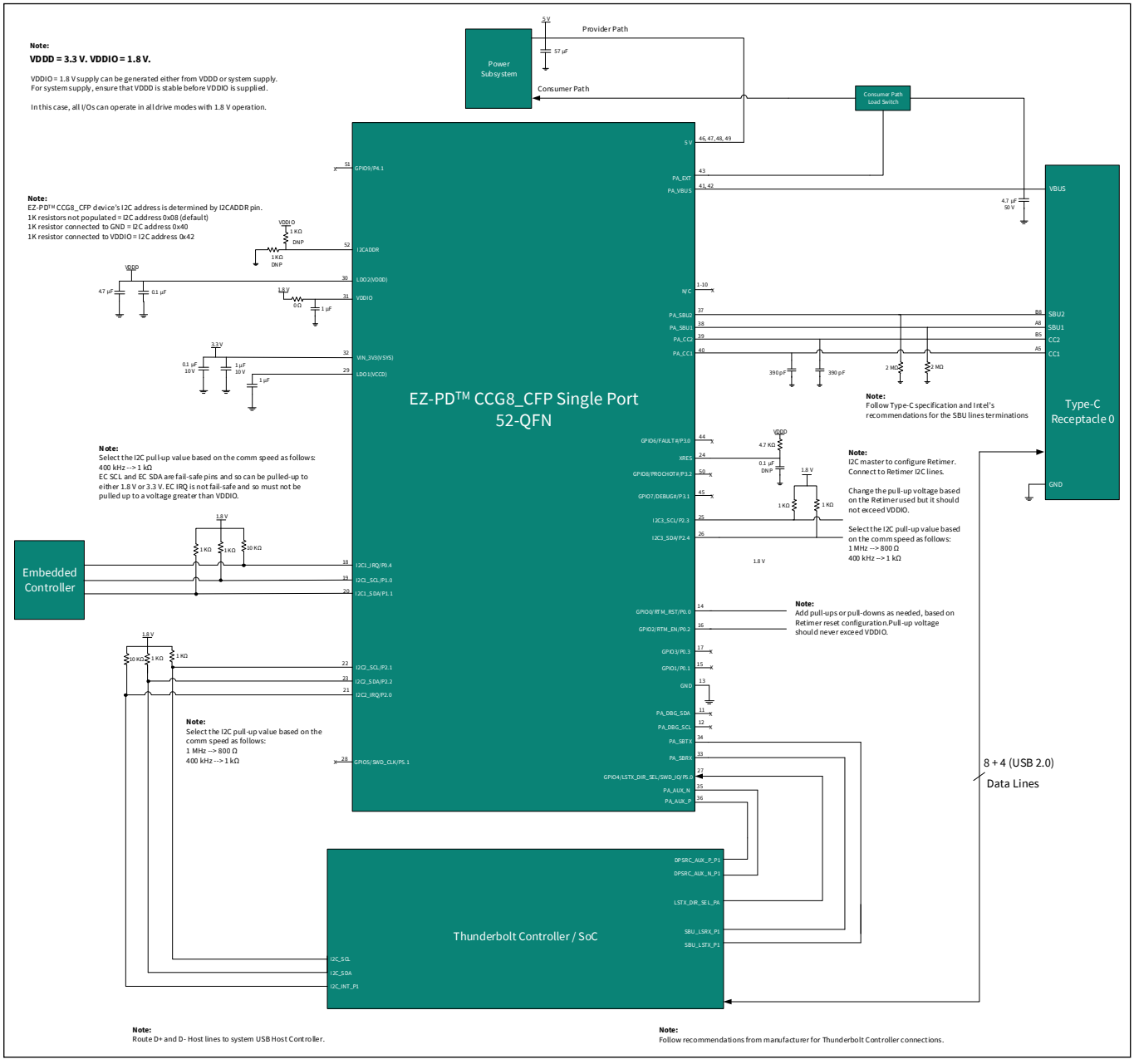


Figure 10 EZ-PD™ CCG8_CFP single-port application block diagram with VDDIO = 1.8 V

Note: *See the **Knowledge Base (KB)** article for information on ESD diode selection.*

Application diagrams

Figure 11 shows the application block diagram using EZ-PD™ CCG8_CFP dual-port device when VDDIO is set to 3.3 V in a 28 V EPR Host system.

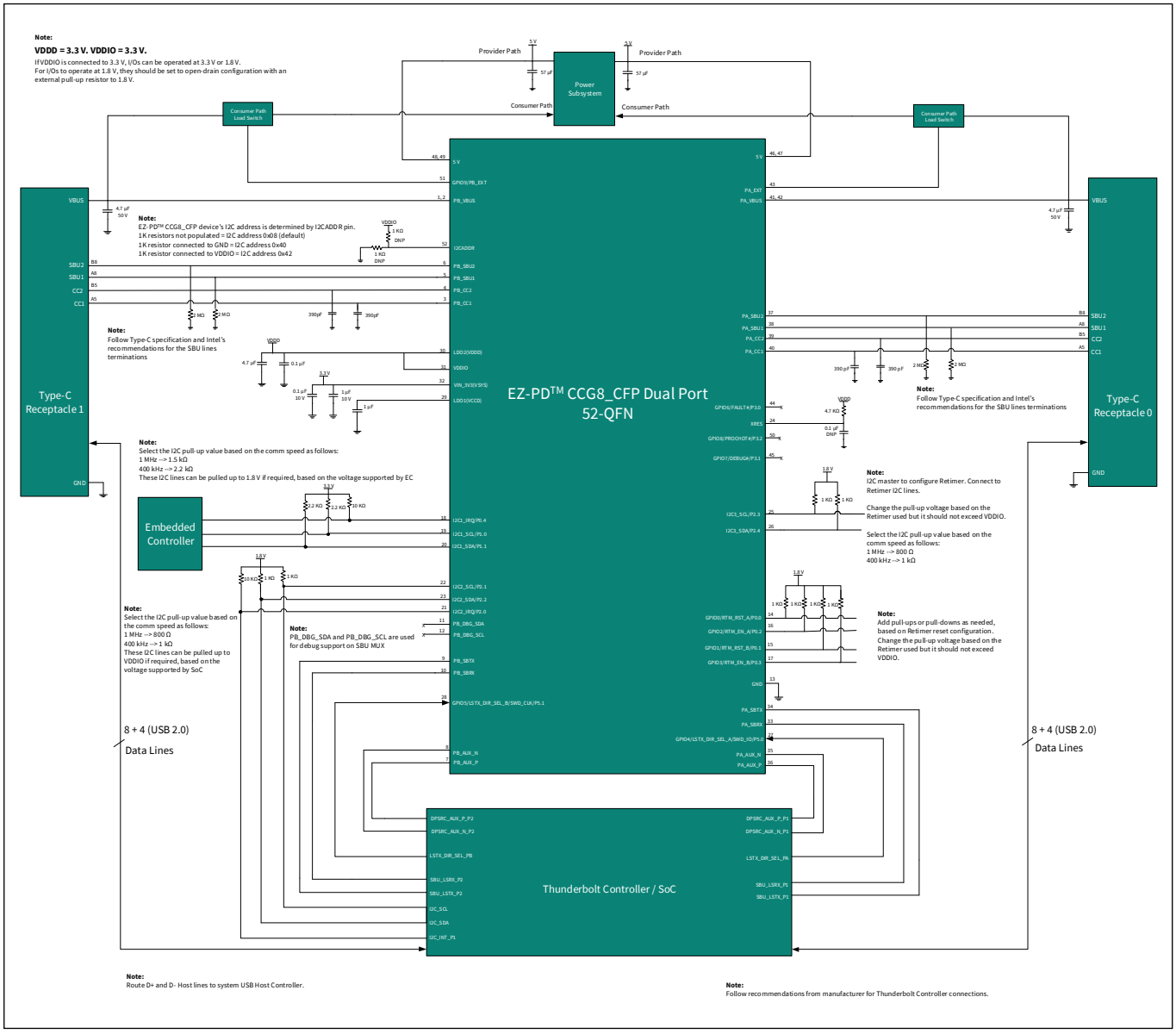


Figure 11 EZ-PD™ CCG8_CFP dual-port application block diagram with VDDIO = 3.3 V

Note: *See the **Knowledge Base (KB)** article for information on ESD diode selection.*

Application diagrams

Figure 12 shows the application block diagram using EZ-PD™ CCG8_CFP dual-port device when VDDIO is set to 1.8 V in 28 V EPR Host system.

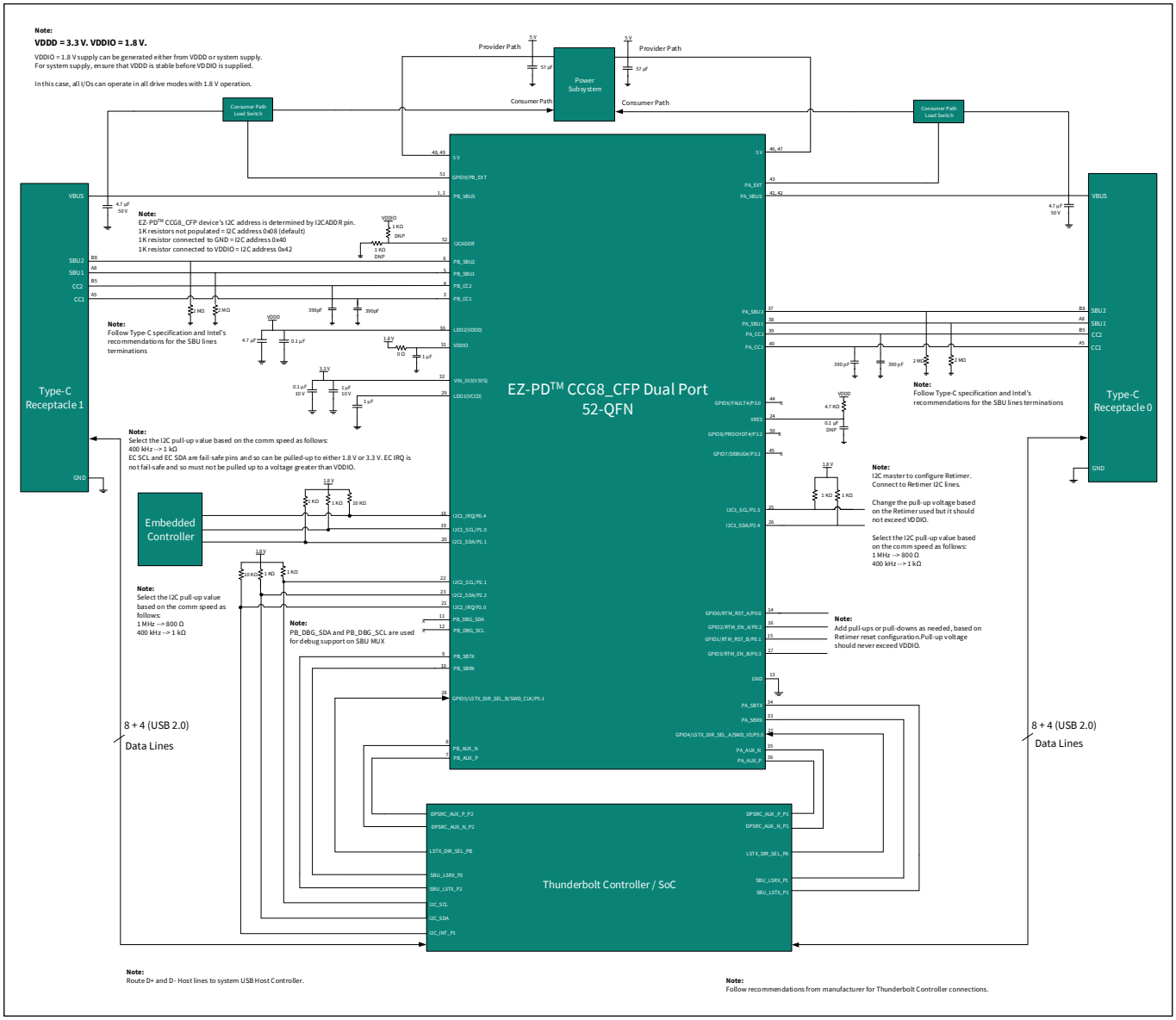


Figure 12 EZ-PD™ CCG8_CFP dual-port application block diagram with VDDIO = 1.8 V

Note: *Contact the Infineon local support team for application diagrams for EPR designs with >28 V support. See the* ***Knowledge Base (KB)*** *article for information on ESD diode selection.*

5 EZ-PD™ CCG8_CFP layout design guidelines for 52-pin QFN package

Figure 13 shows the EZ-PD™ CCG8_CFP device footprint that is recommended. The footprint has rectangular shaped pads in all pins of this package. It is recommended to use rectangular pads to reduce the manufacturing cost by eliminating high-density interconnect (HDI) board processing.

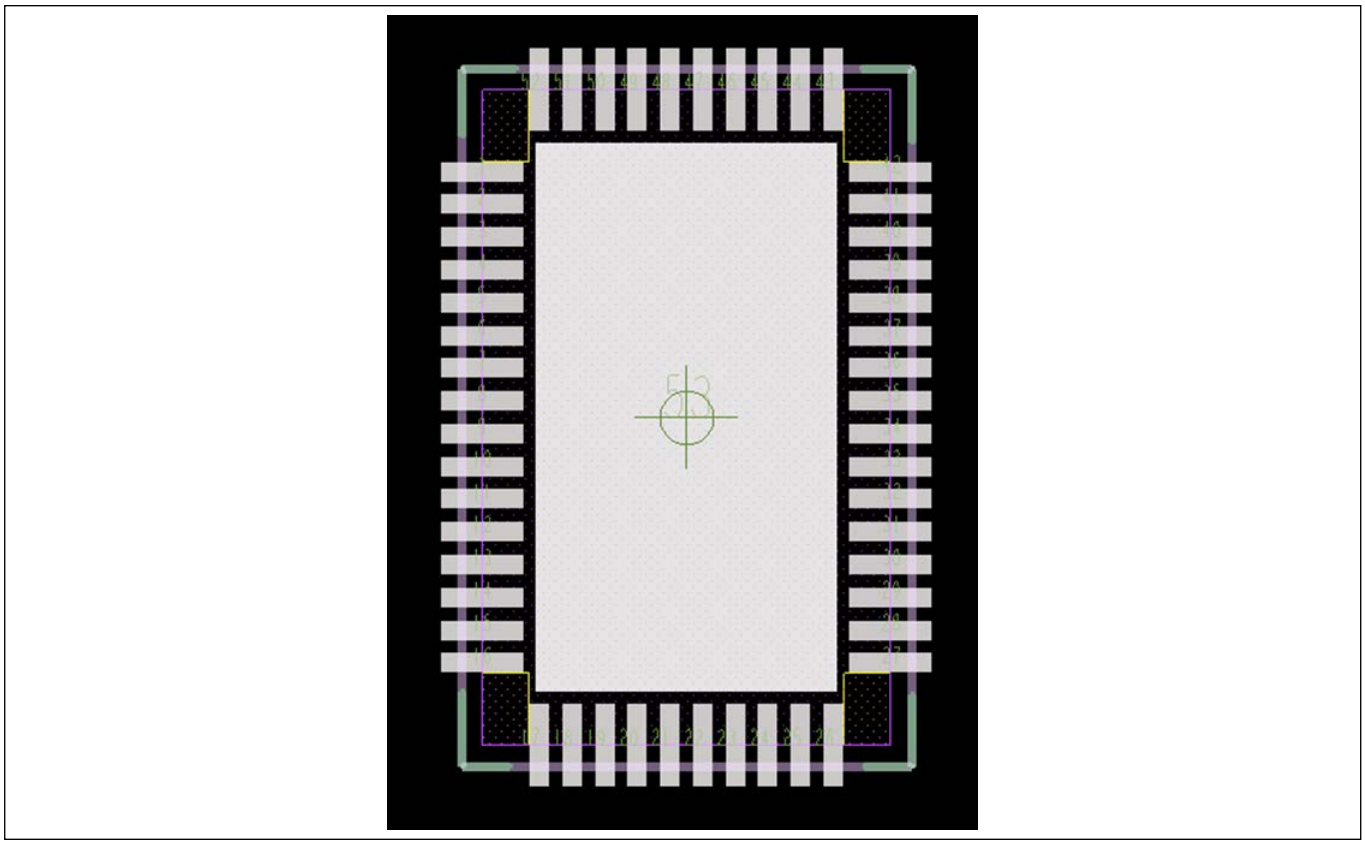


Figure 13 Top-view standard footprint (recommended) for CCG8_CFP

5.1 Recommended pad size

Figure 14 shows the recommended pad size for the QFN package.

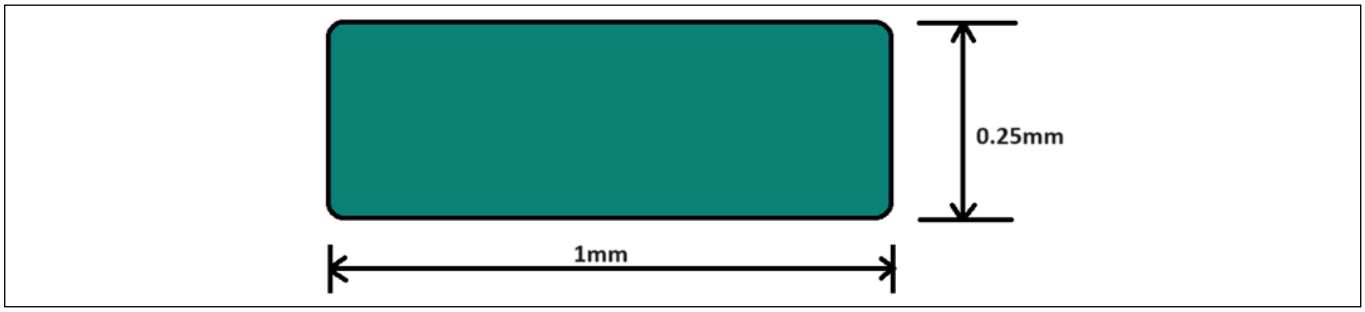


Figure 14 QFN pad size

5.2 Stack-up

Figure 15 shows a typical six-layer stack-up with 1 oz of copper.

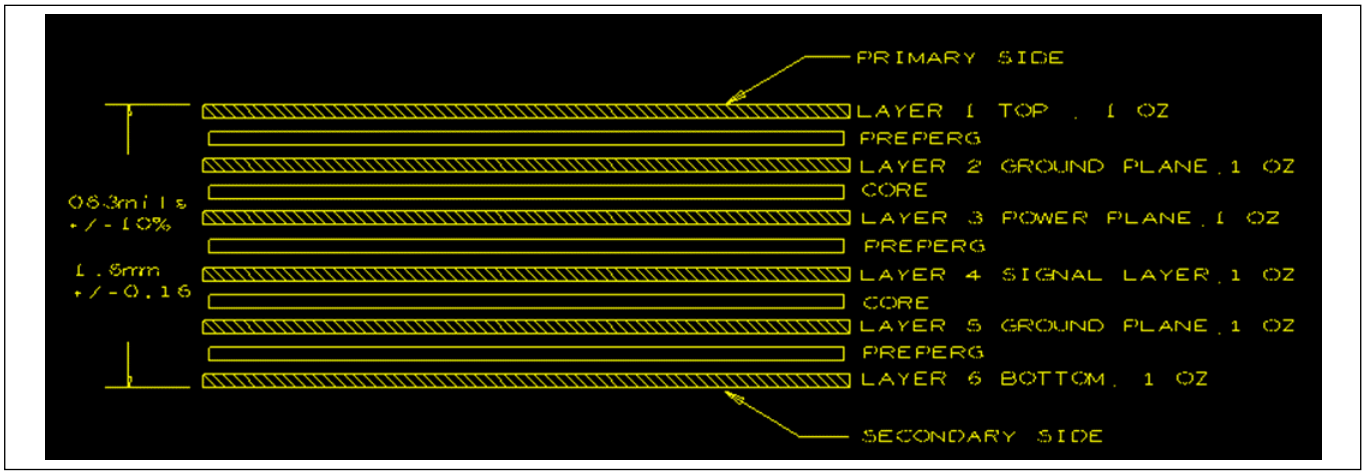


Figure 15 Six-layer stack-up

5.3 52-pin QFN fanout

EZ-PD™ CCG8_CFP 52-pin QFN device uses 5 mil trace width for all the QFN pads and complies to medium-dependent interface (MDI) standards.

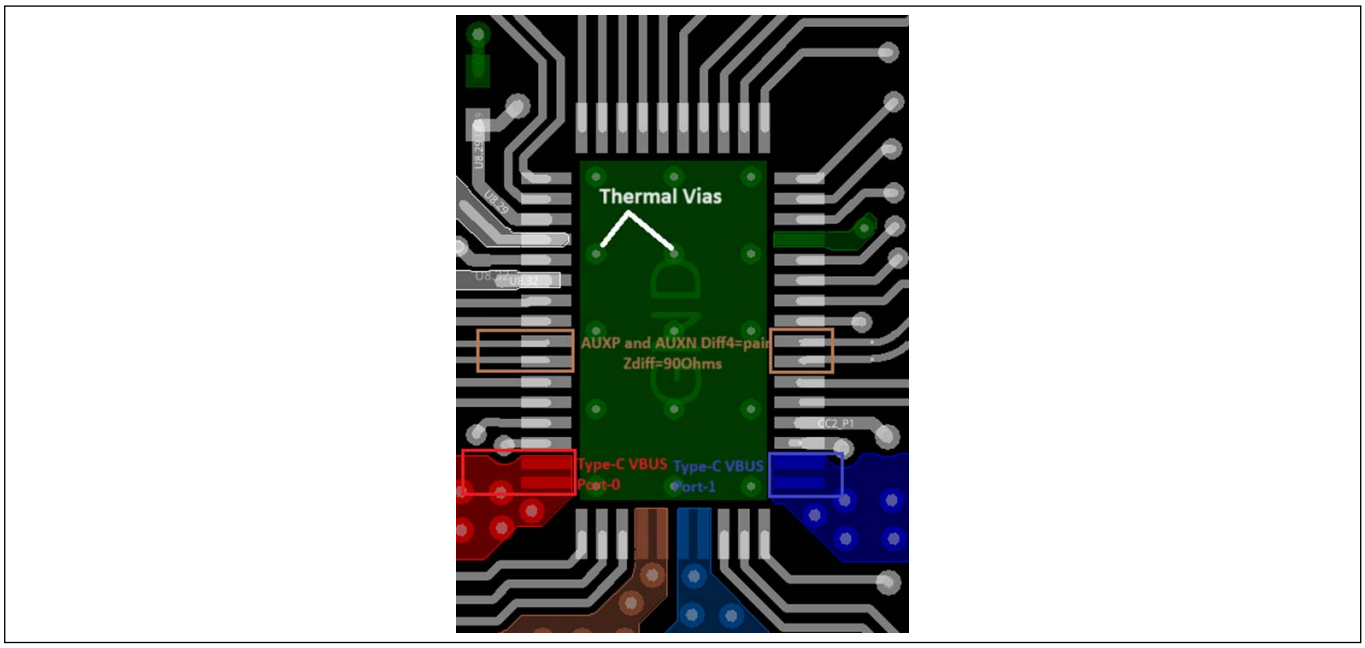


Figure 16 QFN fanout with thermal vias

5.4 Via count on thermal pads

As shown in **Figure 17**, EZ-PD™ CCG8_CFP 52-QFN device has 5 × 3 via array (15 vias) on the thermal pads. The thermal pads should be connected to all the ground planes on the board to meet the thermal performance. Via array means number of vias present on row and column of the exposed pad (EPAD). Each via size should be minimum of 10 mil drill and 20 mil or larger diameter. The big rectangular portion named GND denotes the EPAD and the circles on the EPAD represent the thermal vias.

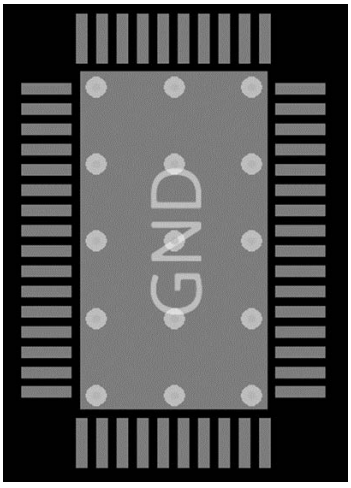


Figure 17 Thermal pad (EPAD) and thermal via

5.5 Via count on power pins

As shown in **Figure 18**, it is recommended that 5 V, Type-C VBUS_P_P0 and Type-C VBUS_P_P1 need at least five vias to be placed near the pins and then connected to a copper pour on adjacent layers and then connected to a larger copper shape. Each via size should be minimum of 10 mil drill and 20 mil diameter.

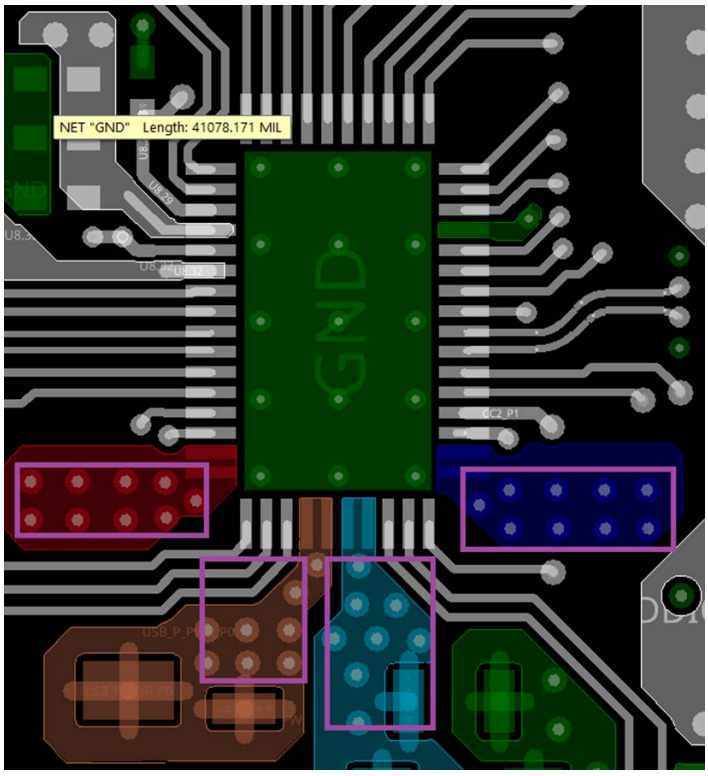


Figure 18 Via count for power pins

5.6 High-Speed routing

There is no High-Speed data requirements for this silicon except AUXP and AUXN lines. The AUXP and AUXN lines should be differentially routed with 90 Ω differential trace impedance and ±10% tolerance. See **Figure 16** for AUXP and AUXN lines.

5.7 CC connections

CC lines for EZ-PD™ CCG8_CFP can carry a maximum of 1 A current. Therefore, the recommended minimum trace width is 10 mils for 10 oz copper thickness. The recommended via size for CC lines is at least 10 mil drill with 16 mils diameter as shown in **Figure 19**.

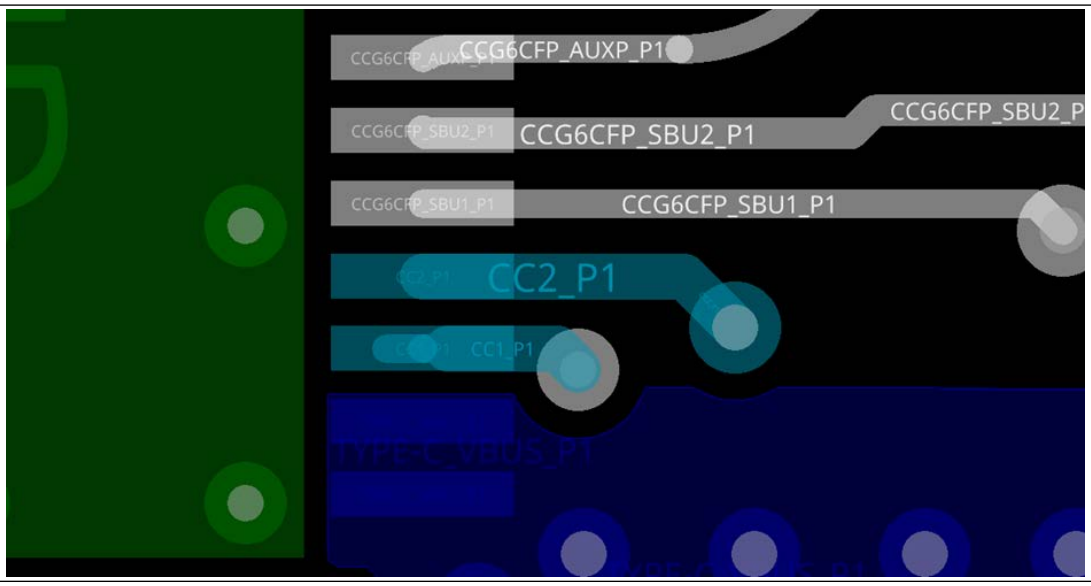


Figure 19 CC1 and CC2 fanout (showing Port 1)

The capacitors should be placed on the bottom layer and near the IC pins as shown in **Figure 20**.

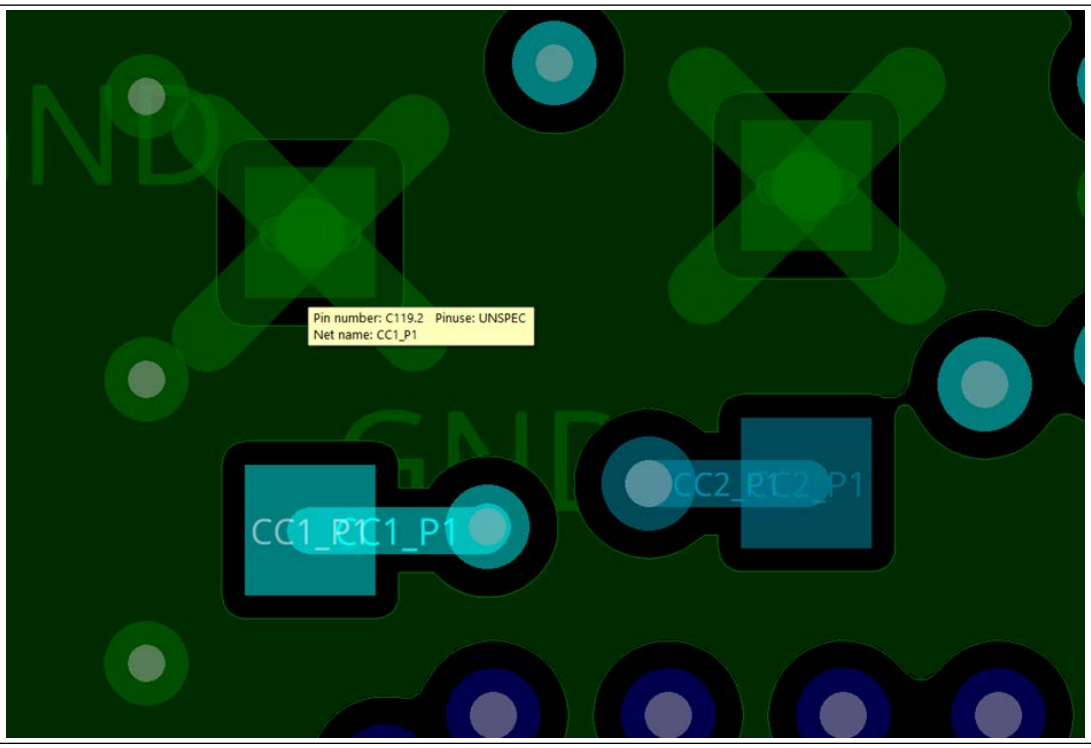


Figure 20 CC1 and CC2 caps

5.8 VDDIO, VCCD, VSYS and VDDD connections

For the VDDIO, VCCD, VSYS ,and VDDD lines, it is recommended to place the decoupling capacitors near the IC pins and then place the bulk capacitors.

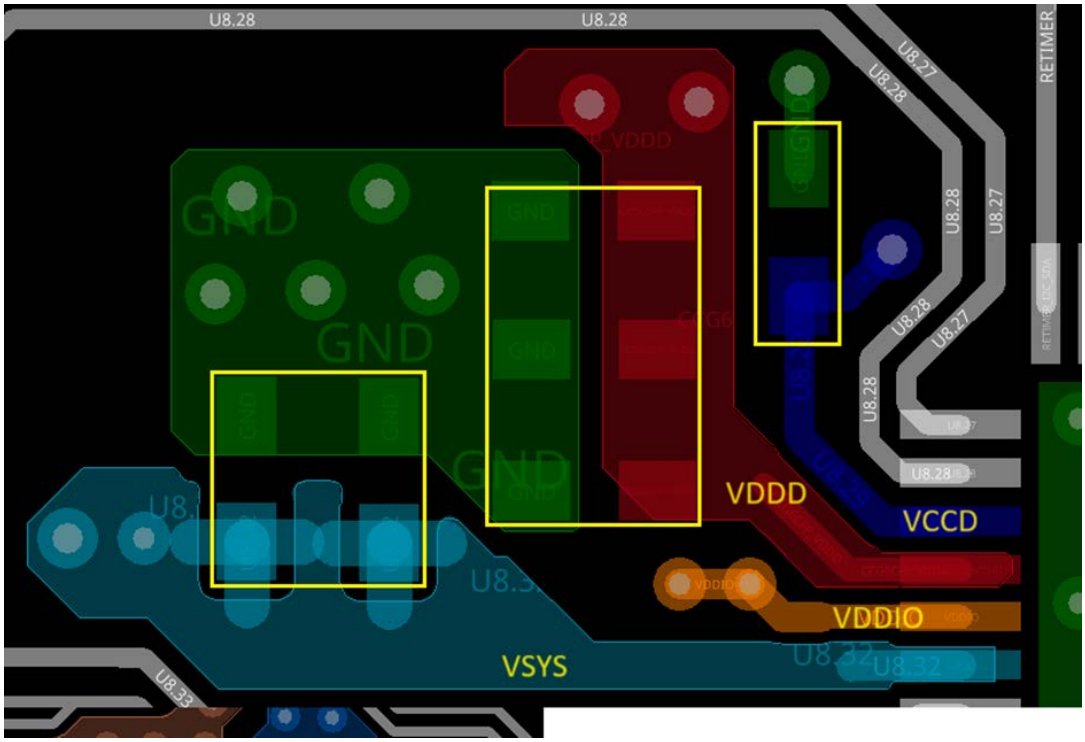


Figure 21 Top layer placement of caps

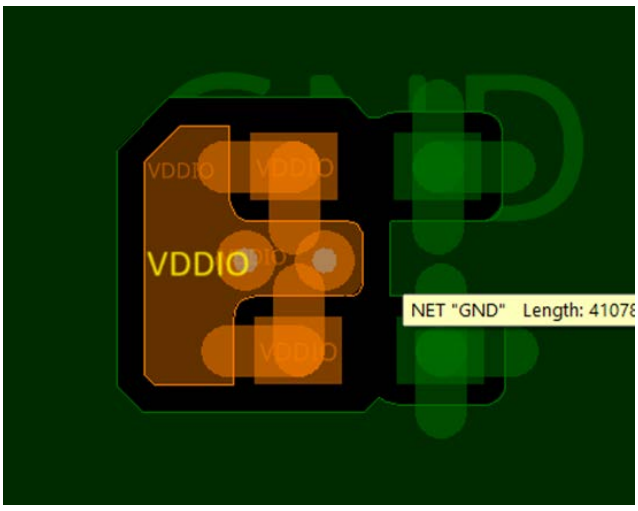
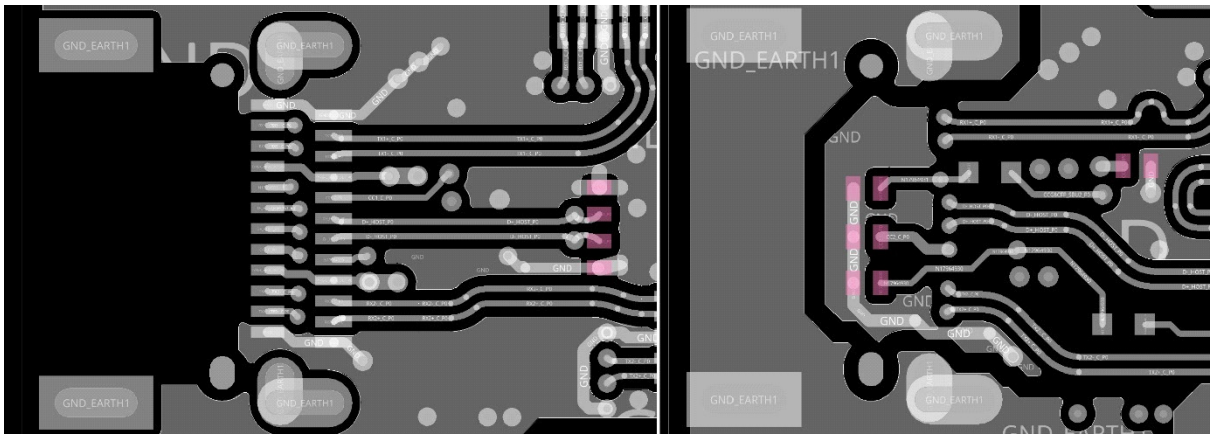


Figure 22 Bottom layer placement of VDDIO caps

5.9 ESD layout

As shown in **Figure 23**, it is recommended to place the ESD diode as close to the connector as possible. Do not route any other sensitive signals near the TVS diode.



Top-side routing near Type-C connector (left), and bottom-side routing near Type-C connector(right)

Figure 23 ESD diode placement

6 Electrical specifications

6.1 Absolute maximum ratings

Table 4 Absolute maximum ratings[17]

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PWR.ABS#1	VDDIO_ABS	IO Supply relative to Vss (Vssio = Vssd = Vssa)	–0.50	–	6	V	Absolute Minimum-Maximum
SID.PWR.ABS#3	VGPIO_ABS	GPIO voltage	–0.5	–	6	V	Absolute Minimum-Maximum. It cannot be more than “VDDIO + 0.5” at any point.
SID.PWR.ABS#4	VGPIO_FAIL-SAFE_ABS	GPIO FAILSLAFE voltage	–0.5	–	6	V	Absolute Minimum-Maximum
SID.PWR.ABS#5	GPIO_ABS	Current per GPIO	–25	–	25	mA	Absolute Minimum-Maximum
SID.PWR.ABS#6	GPIO_injection	GPIO injection current per pin	–0.5	–	0.5	mA	Absolute Minimum-Maximum
SID.PD.PWR.ABS#1	V5V_ABS	Min-Max supply voltage relative to VSS	–0.5	–	6	V	Absolute Minimum-Maximum
SID.PD.PWR.ABS#2	VSYS_ABS	Min-Max supply voltage relative to VSS	–0.5	–	6	V	Absolute Minimum-Maximum
SID.PD.PWR.ABS#3	VBUS_ABS	Min-Max VBUS_C_P0/1 voltage relative to VSS	–0.3	–	34	V	Minimum-Absolute Maximum
SID.PD.PIN.ABS#1	VCC_PIN_ABS	Min-Max voltage on CC1 & CC2 pins	–0.5	–	34	V	Absolute Minimum-Maximum
SID.PD.PIN.ABS#2	VSBU_PIN_ABS	Min-Max voltage on SBU1 & SBU2 pins	–0.5	–	34	V	Absolute Minimum-Maximum
SID.PD.PIN.ABS#4	VAUX_PIN_ABS	Min-Max voltage on AUX_N_P0/1, AUX_P_P0/1, DBG1_P0/1 & DB2_P0/1 pins	–0.5	–	6	V	Absolute Minimum-Maximum. It cannot be more than “VDDD + 0.5” at any point
SID.PD.PIN.ABS#6	VLSx_PIN_ABS	Min-Max voltage on LSTx_P0/1 & LSRx_P0/1 pins	–0.5	–	2	V	Absolute Minimum-Maximum. It cannot be more than “VCCD + 0.5” at any point

Note

17. Usage above the absolute maximum conditions listed in **Table 4** may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150°C in compliance with JEDEC standard JESD22-A103, high temperature storage life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

6.2 Device-level specification

All specifications are valid for –40°C ≤ TA ≤ 55°C and TJ ≤ 125°C, except where noted. Specifications are valid for 3.0 V to 5.5 V except where noted.

6.2.1 DC specifications

Table 5 DC specifications (operating conditions)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PWR#1	VDDD	Regulated output voltage when VSYS powered Power Supply voltage (not to be driven externally)	VSYS – 0.1	–	VSYS	V	–40°C to +70°C TA; Load Current from VDDD = 30mA
SID.PWR#1A	VDDD	Regulated output voltage when VBUS powered Power Supply voltage (not to be driven externally)	3	–	3.65	V	–40°C to +70°C TA.
SID.PWR#2	VDDWRITE	Supply voltage for flash write	2.7	–	5.5	V	–40°C to +70°C TA, ALL VDDD.
SID.PWR#4	VDDIO	Supply voltage for IO	1.71	–	VDDD	V	–40°C to +70°C TA, ALL VDDD
SID.PWR#6	VCCD	Supply voltage for core Logic	–	1.8	–	V	Generated internally from VDDD. Cannot supply current to external blocks and must not be forced externally.
SID.PWR#7	Cefc	External Regulator voltage bypass for VCCD	–	1	–	µF	X5R ceramic or better
SID.PWR#8	Cexc	External Regulator voltage bypass for VDDD	–	4.7	–	µF	X5R ceramic or better
SID.PWR#9	Cexv	Power supply decoupling capacitor for V5V_P0 and V5V_P1, VSYS	–	1	–	µF	X5R ceramic or better
SID.PWR#10	Cexio	Power supply decoupling capacitor for VDDIO	–	1	–	µF	X5R ceramic or better
SID.PD.PWR#1	V5V	Power Supply for VCONN	4.85	–	5.5	V	–40CC to +70CC TA
SID.PD.PWR#2	VSYS_UFP	VSYS valid range	2.8	–	3.63	V	UFP applications
SID.PD.PWR#2A	VSYS_DFP_DRP	VSYS valid range	3	–	3.63	V	DFP/DRP applications
SID.PD.PWR#3	VBUS	VBUS_C_P0/1 valid range	4	–	30	V	–
Current Consumption in Deep Sleep Mode. Typical values measured at 25°C.							
SID_IDD	IDD12	Current from VSYS, VSYS = 3.3 V	–	10	–	mA	TA = 25°C, CC IO IN Transmit or Receive, no I/O sourcing current, CPU at 24 MHz, two PD ports active
SID_DS1	IDD_DS1	Current from VSYS, VSYS = 3.3 V. CC wakeup on, Type-C not connected	–	250	–	µA	Power source = VSYS, Type-C Not attached, CC enabled for wakeup, Rp and Rd connected at 70 ms intervals by CPU. Rp, Rd connection should be enabled for both PD ports.
SID_DS3	IDD_DS2	Current from VSYS, VSYS = 3.3 V. CC wakeup on, with SBU, NGDO, SCP, RCP, ILIMIT & UVOV ON	–	635	–	µA	One Port attached (SBU, VCONN, NGDO, SCP, RCP, ILIMIT & UVOV ON), Chip in Deep-sleep
SID_DS3_A	IDD_DS2A	Current from VSYS, VSYS = 3.3 V. CC wakeup on, with SBU, NGDO, SCP, RCP, ILIMIT & UVOV ON	–	970	–	µA	Both Port attached (SBU, VCONN, NGDO, SCP, RCP, ILIMIT & UVOV ON), Chip in Deep-sleep
SID34	IDD29	Current from VSYS. I2C Wakeup and WDT on.	–	150	–	µA	VSYS = 3.3 V, TA = 25°C
SID307	IDD_XR	Current from VSYS while XRES asserted	–	130	–	µA	Power Source = VSYS = 3.3 V, Type-C Not Attached, TA = 25°C

6.2.2 Global conditions

Table 6 Global conditions

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.CHIP#1	TSTG	Storage temperature	–55	–	150	°C	Per JESD22-A103 HTSL Test
SID.CHIP#2	TA	Operation temperature	–40	–	70	°C	–

6.2.3 System performance requirements

Table 7 System performance requirements

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SYS.PER#15	CPU_DMIPS	Minimum MIPS required from the CPU	–	10.8	–	DMIPS	At 12 MHz CPU frequency. 0.9 DMIPS/MHz

6.2.4 System-level functional requirements

Table 8 System-level functional requirements

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SYS.FES#1	T_PWR_RDY	Power up to “Ready to accept I2C / CC command”	–	5	25	ms	–

6.2.5 GPIO specifications

Table 9 GPIO DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GPIO.DC#1	Vih_CMOS	Input Voltage high threshold	0.7 × VDD	–	–	V	CMOS Input
SID.GPIO.DC#2	Vil_CMOS	Input Voltage low threshold	–	–	0.3 × VDD	V	CMOS Input
SID.GPIO.DC#1a	Vih_VDDIO2.7–	LVTTL input, VDD < 2.7 V	0.7 × VDD	–	–	V	–
SID.GPIO.DC#2a	Vil_VDDIO2.7–	LVTTL input, VDD < 2.7 V	–	–	0.3 × VDD	V	–
SID.GPIO.DC#1b	Vih_VDDIO2.7+	LVTTL input, VDD ≥ 2.7 V	2	–	–	V	–
SID.GPIO.DC#2b	Vil_VDDIO2.7+	LVTTL input, VDD ≥ 2.7 V	–	–	0.8	V	–
SID.GPIO.DC#1c	Vih_VCCHIB	VIH, 1.8 V Input Mode	1.26	–	–	V	–
SID.GPIO.DC#2c	Vil_VCCHIB	VIL, 1.8 V Input Mode	–	–	0.54	V	–
SID.GPIO.DC#4	VOH	Output Voltage high level	VDD – 0.6	–	–	V	Ioh = 4 mA at 3 V VDDIO
SID.GPIO.DC#4a	VOH	Output Voltage high level	VDD – 0.5	–	–	V	Ioh = 1 mA at 1.8 V VDDIO
SID.GPIO.DC#5	VOL	Output Voltage low level	–	–	0.6	V	Iol = 4 mA at 1.8 V VDDIO
SID.GPIO.DC#5a	VOL	Output Voltage low level	–	–	0.6	V	Iol = 10 mA at 3 V VDDIO
SID.GPIO.DC#5b	VOL	Output Voltage low level	–	–	0.4	V	Iol = 3 mA at 3 V VDDIO
SID.GPIO.DC#6	RPULLUP	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID.GPIO.DC#7	RPULLDOWN	Pull-down resistor	3.5	5.6	8.5	kΩ	–
SID.GPIO.DC#8	IIL	Input leakage current (absolute value	–	–	2	nA	25°C, VDDIO = 3.0 V
SID.GPIO.DC#9	CIN	Pin capacitance	–	–	9	pF	–
SID.GPIO.DC#3b	VHYSTTL	Input hysteresis LVTTL VDD > 2.7 V	15	40	–	mV	–
SID.GPIO.DC#3	VHYSCMOS	Input hysteresis CMOS	0.05 × VDD	–	–	mV	VDDIO < 4.5 V
SID.GPIO.DC#3a	VHYSCMOS55	Input hysteresis CMOS	200	–	–	mV	VDDIO > 4.5 V
SID.GPIO.DC#3c	VHYS_VCCHIB	Input Hysteresis, 1.8 V Input Mode	90	–	–	mV	VDDIO > 4.5 V
SID.GPIO.DC#10	IDIODE	Current through protection diode to VDD/VSS	–	–	100	µA	–
SID.GPIO.DC#11	ITOT_GPIO	Maximum Total Source or Sink Chip Current when VDDIO supplied externally	–	–	200	mA	–
SID.GPIO.DC#11a	ITOT_GPIO_VDDD	Maximum Total Source or Sink Chip Current when VDDD shorted to VDDIO on board	–	–	10	mA	–

Table 10 GPIO AC specifications

Guaranteed by characterization

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GPIO.AC#1	TRISEF	Rise time in Fast Strong Mode	2	–	12	ns	3.3 V VDD, Cload = 25 pF
SID.GPIO.AC#1a	TRISEF_2V	Rise time in Fast Strong Mode	20	–	100	ns	1.65 V VDD, Cload = 25 pF
SID.GPIO.AC#2	TFALLF	Fall time in Fast Strong Mode	2	–	12	ns	3.3 V VDD, Cload = 25 pF
SID.GPIO.AC#2a	TFALLF_2V	Fall time in Fast Strong Mode	20	–	100	ns	1.65 V VDD, Cload = 25 pF
SID.GPIO.AC#3	TRISES	Rise time in Slow Strong Mode	10	–	60	–	3.3 V VDD, Cload = 25 pF
SID.GPIO.AC#4	TFALLS	Fall time in Slow Strong Mode	10	–	60	–	3.3 V VDD, Cload = 25 pF
SID.GPIO.AC#5	FGPIOUT1	GPIO Fout; 3.3 V ≤ VDD ≤ 5.5 V. Fast Strong mode.	–	–	33	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID.GPIO.AC#6	FGPIOUT2	GPIO Fout; 1.71 V ≤ VDD ≤ 3.3 V. Fast Strong mode.	–	–	16.7	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID.GPIO.AC#7	FGPIOUT3	GPIO Fout; 3.3 V ≤ VDD ≤ 5.5 V. Slow Strong mode.	–	–	7	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID.GPIO.AC#8	FGPIOUT4	GPIO Fout; 1.71 V ≤ VDD ≤ 3.3 V. Slow Strong mode.	–	–	3.5	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID.GPIO.AC#9	FGPIOIN	GPIO input operating frequency; 1.71 V ≤ VDD ≤ 5.5 V	–	–	16	MHz	90/10% Vio

6.2.6 XRES requirements

Table 11 XRES requirements

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.XRES#1	Vih_XRES	Input Voltage high threshold on XRES pin	0.7 × VDDIO	–	–	V	CMOS Input
SID.XRES#2	Vil_XRES	Input Voltage low threshold on XRES pin	–	–	0.3 × VDDIO	V	CMOS Input
SID.XRES#3	Cin_XRES	Input Capacitance on XRES pin	–	–	7	pF	–
SID.XRES#4	Vhysxres	Input voltage hysteresis on XRES pin	–	0.05 × VDDIO	–	mV	–
SID.XRES#5	TXRES	External reset pulse width	5	–	–	µs	–40°C to +70°C TA, All VDDIO
SID.XRES#6	TXRES_GF	External reset glitch filter period	–	20	–	ns	–40°C to +70°C TA, All VDDIO

6.2.7 Memory

Table 12 Memory peripherals (flash macro specs)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.MEM#3	FLASH_ERASE	Row erase time	–	–	13	ms	–40°C to +70°C TA, All VDDD
SID.MEM#4	FLASH_WRITE	Row (Block) write time (erase & program)	–	–	20	ms	–40°C to +70°C TA, All VDDD
SID.MEM#6	FLASH_ENPB	Flash write endurance	100K	–	–	cycles	25°C to 70°C, All VDDD
SID.MEM#8	FLASH_ROW_PGM	Row program time after erase	–	–	7	ms	25°C to 70°C, All VDDD
SID178	TBULKERASE	Bulk erase time (128 KB)	–	–	35	ms	Guaranteed by design
SID180	TDEVPROG	Total device program time	–	–	25	s	Guaranteed by design
SID182	FRET1	Flash retention, TA ≤ 55°C, 100K P/E cycles	20	–	–	years	–
SID182A	FRET2	Flash retention, TA ≤ 85°C, 10K P/E cycles	10	–	–	years	–

Table 13 Memory size specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.MEM#1	FLASH_SIZE	Flash memory size	–	128	–	KB	SONOS Flash amount (bytes)
SID.MEM#2	SRAM_SIZE	SRAM memory size	–	16	–	KB	SRAM amount (bytes)
SID.MEM#3	SROM_SIZE	SROM memory size	–	96	–	KB	SROM amount (bytes)

6.2.8 Digital peripherals

6.2.8.1 ILO/IMO/POR specs

Table 14 ILO/IMO/POR specs

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.CLK#1	FIMO	IMO frequency	–	48	–	MHz	–40°C to +70°C TA, All VDDD
SID.CLK#2	FIMO_RES	IMO frequency resolution	–	0.25	–	%	–40°C to +70°C TA, All VDDD
SID.CLK#3	IMO_STL	IMO settling time when trim register is changed	–	–	200	ns	25°C TA, All VDDD, FIMO = 48 MHz
SID.CLK#4	FCPU	CPU input frequency	–	–	48	MHz	–40°C to +70°C TA, All VDDD
SID.CLK#5	FILO	ILO frequency	20	40	80	kHz	–
SID.CLK#6	SR_POWER_UP	Power supply slew rate during power up	1	–	67	V/ms	–40°C to +70°C TA, All VDDD
SID.CLK#13	Fimotol	Frequency variation at 48 MHz (trimmed)	–	–	±2	%	2.7 V ≤ VDDD < 5.5 V. And –25°C ≤ TA ≤ 70°C
SID.CLK#13A	Fimotolvccd	Frequency variation at 48 MHz (trimmed)	–	–	±4	%	All conditions
SID218	IMO1	IMO Operating current at 48 MHz	–	–	250	µA	–
SID226	TSTARTIMO	IMO Start-up time	–	–	7	µs	–
SID228	TJITRMSIMO2	RMS jitter at 48 MHz	–	145	–	ps	–
SID234	TSTARTILO1	ILO Start-up time	–	–	2	ms	–
SID238	TILODUTY	ILO Duty cycle	40	50	60	%	–
SID305	EXTCLKFREQ	External clock input frequency	–	–	16	MHz	–
SID306	EXTCLKDUTY	Duty cycle; measured at VDD/2	45	–	55	%	–
SID262	TCLKSWITCH	System clock source switching time	3	–	4	Periods	–
SID185	VRISEIPOR	Power-on-Reset (POR) Rising trip voltage	0.8	–	1.5	V	–
SID186	VFALLIPOR	Power-on-Reset (POR) Falling trip voltage	0.7	–	1.4	V	–
SID190	VFALLPPOR	Brown-Out-Detect (BOD) trip voltage active/ sleep modes	1.48	–	1.62	V	–
SID192	VFALLDPSLP	BOD trip voltage in deep sleep mode	1.1	–	1.5	V	–

6.2.8.2 Fixed I2C specifications

Table 15 Fixed I2C AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.I2C#1	FSCLI2C_SM	I2C SCL clock frequency	0	–	100	kHz	Standard Mode
SID.I2C#2	FSCLI2C_FM	I2C SCL clock frequency	0	–	400	kHz	Fast Mode
SID.I2C#33	FSCLI2C_FMP	I2C SCL clock frequency	0	–	1000	kHz	Fast Mode Plus
SID.I2C#3	THDSTAI2C_SM	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4	–	–	µs	Standard Mode
SID.I2C#4	THDSTAI2C_FM	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.6	–	–	µs	Fast Mode
SID.I2C#34	THDSTAI2C_FMP	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.26	–	–	µs	Fast Mode Plus
SID.I2C#5	TSUSTAI2C_SM	Setup time for a repeated START condition	4.7	–	–	µs	Standard Mode
SID.I2C#6	TSUSTAI2C_FM	Setup time for a repeated START condition	0.6	–	–	µs	Fast Mode

Table 15 Fixed I2C AC specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.I2C#35	TSUSTAI2C_FMP	Setup time for a repeated START condition	0.26	–	–	µs	Fast Mode Plus
SID.I2C#7	TLOWI2C_SM	LOW period of the SCL clock	4.7	–	–	µs	Standard Mode
SID.I2C#8	TLOWI2C_FM	LOW period of the SCL clock	1.3	–	–	µs	Fast Mode
SID.I2C#36	TLOWI2C_FMP	LOW period of the SCL clock	0.5	–	–	µs	Fast Mode Plus
SID.I2C#9	THIGHI2C_SM	HIGH period of the SCL clock	4	–	–	µs	Standard Mode
SID.I2C#10	THIGHI2C_FM	HIGH period of the SCL clock	0.6	–	–	µs	Fast Mode
SID.I2C#37	THIGHI2C_FMP	HIGH period of the SCL clock	0.26	–	–	µs	Fast Mode Plus
SID.I2C#11	THDDATI2C	Data hold time	0	–	–	µs	All I2C speeds
SID.I2C#12	TSUDATI2C_SM	Data setup time	250	–	–	ns	Standard Mode
SID.I2C#13	TSUDATI2C_FM	Data setup time	100	–	–	ns	Fast Mode
SID.I2C#38	TSUDATI2C_FMP	Data setup time	50	–	–	ns	Fast Mode Plus
SID.I2C#14	TSUSTOI2C_SM	Setup time for I2C STOP condition	4	–	–	µs	Standard Mode
SID.I2C#15	TSUSTOI2C_FM	Setup time for I2C STOP condition	0.6	–	–	µs	Fast Mode
SID.I2C#39	TSUSTOI2C_FMP	Setup time for I2C STOP condition	0.26	–	–	µs	Fast Mode Plus
SID.I2C#16	CB_SM	Capacitive load for each I2C bus line	–	–	400	pF	Standard Mode
SID.I2C#17	CB_FM	Capacitive load for each I2C bus line	–	–	400	pF	Fast Mode
SID.I2C#40	CB_FMP	Capacitive Load for each I2C bus line	–	–	550	pF	Fast Mode Plus
SID.I2C#18	TVDDATI2C_SM	Data valid time	–	–	3.45	µs	Standard Mode
SID.I2C#19	TVDDATI2C_FM	Data valid time	–	–	0.9	µs	Fast Mode
SID.I2C#41	TVDDATI2C_FMP	Data Valid time	–	–	0.45	µs	Fast Mode Plus
SID.I2C#20	TVDACKI2C_SM	Data valid acknowledge time	–	–	3.45	µs	Standard Mode
SID.I2C#21	TVDACKI2C_FM	Data valid acknowledge time	–	–	0.9	µs	Fast Mode
SID.I2C#42	TVDACKI2C_FMP	Data Valid acknowledge time	–	–	0.45	µs	Fast Mode Plus
SID.I2C#22	TSPI2C_FM	Pulse width of spikes suppressed by input filter	–	–	50	ns	Fast Mode
SID.I2C#43	TSPI2C_FMP	Pulse width of spikes suppressed by input filter	–	–	50	ns	Fast Mode Plus
SID.I2C#23	TBUFI2C_SM	Bus free time between a STOP and START condition	4.7	–	–	µs	Standard Mode
SID.I2C#24	TBUFI2C_FM	Bus free time between a STOP and START condition	1.3	–	–	µs	Fast Mode
SID.I2C#44	TBUFI2C_FMP	Bus Free time between a STOP and START condition	0.5	–	–	µs	Fast Mode Plus
SID.I2C#25	VIL_I2C	Input low voltage	–0.5	–	0.3 × VDDIO	V	Fast and standard mode I2C speeds
SID.I2C#26	VIH_I2C	Input high voltage	0.7 × VDDIO	–	–	V	Fast and standard mode I2C speeds
SID.I2C#27	VOL_I2C_L	Output low voltage, low supply range	–	–	0.2 × VDDIO	V	Fast and standard mode I2C speeds, VDDIO < 2 V, 2 mA sink
SID.I2C#28	VOL_I2C_H	Output low voltage, high supply range	–	–	0.4	V	Fast and standard mode I2C speeds, VDDIO > 2 V, 3 mA sink
SID.I2C#29	IOL_I2C_SM	I2C output low current	3	–	–	mA	Standard Mode, 1.71 V ≤ VDDIO ≤ 5.5 V, load = CB_SM, VOL = 0.4 V
SID.I2C#30	I2C_VHYS_HV	I2C input hysteresis	0.05 × VDDIO	–	–	mV	Fast and standard mode I2C speeds, 2 V ≤ VDDIO < 4.5 V
SID.I2C#30A	I2C_VHYS_5V	I2C input hysteresis	200	–	–	mV	Fast and standard mode I2C speeds, VDDIO > 4.5 V

Table 15 Fixed I2C AC specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.I2C#31	I2C_VHYS_LV	I2C input hysteresis	0.10 × VDDIO	–	–	mV	Fast and standard mode I2C speeds, VDDIO < 2 V
COM.REQ#7	I2C_ADD	I2C address width	–	–	8	bits	7-bit address and 1 RW bit
SID.I2C#32	IOL_I2C_FM	I2C output low current	6	–	–	mA	Fast Mode, 1.71 V ≤ VDDIO ≤ 5.5 V, load = CB_SM, VOL = 0.6 V
SID.I2C#45	IOL_I2C_FMP	I2C Output low current, high voltage range	20	–	–	mA	Fast Mode Plus, 3.0 V ≤ VDDD ≤ 5.5 V, load = CB_FMP, –40°C to 70°C TA, GPIO_FAILSAFE port only
SID.I2C#45A	IOL_I2C_FMP	I2C Output low current, low voltage range	3	–	–	mA	Fast Mode Plus, 1.71 V ≤ VDDD ≤ 3.0 V, load = CB_FMP, –40°C to 70°C TA

Table 16 Fixed I2C DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID149	II2C1	Block current consumption at 100 kHz	–	–	75	µA	–
SID150	II2C2	Block current consumption at 400 kHz	–	–	185	µA	–
SID151	II2C3	Block current consumption at 1 Mbps	–	–	390	µA	–
SID152	II2C4	I2C enabled in Deep Sleep mode	–	–	1.4	µA	–

6.2.8.3 Fixed UART specifications

Table 17 Fixed UART DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID160	IUART1	Block current consumption at 100 kbits/second	–	–	125	µA	–
SID161	IUART2	Block current consumption at 1000 kbits/second	–	–	312	µA	–

Table 18 Fixed UART AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID162	FUART	Bit Rate	–	–	1	Mbps	–

6.2.8.4 Fixed SPI specifications

Table 19 Fixed SPI DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID163	ISPI1	Block current consumption at 1 Mbits/second	–	–	360	µA	–
SID164	ISPI2	Block current consumption at 4 Mbits/second	–	–	560	µA	–
SID165	ISPI3	Block current consumption at 8 Mbits/second	–	–	600	µA	–

Table 20 Fixed SPI AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID166	FSPI	SPI Operating frequency (Master; 6X Oversampling)	–	–	8	MHz	–

Table 21 Fixed SPI master mode AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID167	TDMO	MOSI valid after SClock driving edge	–	–	15	ns	–
SID168	TDSI	MISO valid before SClock capturing edge	20	–	–	ns	Full clock, late MISO sampling
SID169	THMO	Previous MOSI data hold time	0	–	–	ns	Referred to Slave capturing edge

Table 22 Fixed SPI slave mode AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID170	TDMI	MOSI Valid before Sclock Capturing edge	40	–	–	ns	–
SID171	TDSO	MISO Valid after Sclock driving edge	–	–	48 + 3 × Tcpu	ns	Tcpu = 1/Fcpu
SID171A	TDSO_EXT	MISO Valid after Sclock driving edge in Ext. Clk. mode	–	–	48	ns	–
SID172	THSO	Previous MISO data hold time	0	–	–	ns	–
SID172A	TSSELSCK	SSEL Valid to first SCK Valid edge	100	–	–	ns	–

6.2.8.5 Timer requirements

Table 23 Timer requirements

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.TMR#1	SYS_TIM_RES	Sys timer resolution	–	16	–	bits	–40°C to +70°C TA, All VDDD
SID.TMR#2	WDT_RES	Watchdog timer resolution	–	16	–	bits	–40°C to +70°C TA, All VDDD

6.2.8.6 TCPWM requirements

Table 24 TCPWM requirements

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	–	–	145	µA	All modes (Timer/Counter/PWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 8 MHz	–	–	205	µA	All modes (Timer/Counter/PWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 16 MHz	–	–	385	µA	All modes (Timer/Counter/PWM)
SID.TCPWM.3	TCPWMFREQ	Operating frequency	–	–	Fc	MHz	Fc max = CLK_SYS. Maximum = 48 MHz
SID.TCPWM.4	TPWMENEXT	Input Trigger Pulse Width	2/Fc	–	–	ns	For all trigger events[18]
SID.TCPWM.5	TPWMEXT	Output Trigger Pulse widths	2/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	TCRES	Resolution of Counter	1/Fc	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWMRES	PWM Resolution	1/Fc	–	–	ns	Minimum pulse width of PWM Output
SID.TCPWM.5C	QRES	Quadrature inputs resolution	1/Fc	–	–	ns	Minimum pulse width between Quadrature phase inputs.

Note
18. Trigger events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.

6.2.8.7 SWD specifications

Table 25 SWD specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.SWD#1	F_swdclk1	3.3 V ≤ VDDIO ≤ 5.5 V	–	–	14	MHz	SWDCLK < 1/3 CPU clock frequency
SID.SWD#2	F_swdclk2	1.8 V ≤ VDDIO ≤ 3.3 V	–	–	7	MHz	SWDCLK < 1/3 CPU clock frequency
SID.SWD#3	T_swdi_setup	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
SID.SWD#4	T_swdi_hold	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
SID.SWD#5	T_swdo_valid	T = 1/f SWDCLK	–	–	0.50 × T	ns	–
SID.SWD#6	T_swdo_hold	T = 1/f SWDCLK	1	–	–	ns	–

6.2.9 Power Delivery (PD) peripherals

6.2.9.1 ADC DC specifications

Table 26 ADC DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PD.ADC.DC#1	Resolution	ADC Resolution	–	8.00	–	bits	–
SID.PD.ADC.DC#2	INL	Integral Non-Linearity	–1.5	–	1.5	LSB	–
SID.PD.ADC.DC#3	DNL	Differential Non-Linearity	–2.5	–	2.5	LSB	–
SID.PD.ADC.DC#4	Gain Error	Gain Error	–1.5	–	1.5	LSB	–
SID.PD.ADC.DC#5	VREF_ADC1	Reference voltage of ADC	VDDD min	–	VDDD max	V	Reference voltage generated from VDDD
SID.PD.ADC.DC#6	VREF_ADC2	Reference voltage of ADC	2.18	2.2	2.22	V	Reference voltage generated from deep sleep reference

6.2.9.2 VSYS regulator specifications

Table 27 VSYS regulator specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.DC.VDDDSW.1	Res_sw	Resistance from supply input to the output supply vddd	–	–	1.5	Ω	Measured with a load current of 5 mA–10 mA on VDDD.

6.2.9.3 VBUS regulator DC specifications

Table 28 VBUS regulator DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PD.VREG.1	VBUSREG	VBUS regulator output voltage (minimum VBUS = 4 V to 34 V)	2.97	–	3.65	V	Chip powered through VBUS_C_P0/VBUS_C_P1 and Output measured on VDDD
SID.PD.VREG.6	VBUSLINREG	vbus_reg line regulation for VBUS from 4 V to 34 V	–	–	0.5	%/V	–
SID.PD.VREG.8	VBUSLOADREG	vbus_reg load regulation for Iload from 0 mA to 30 mA (VBUS = 4 V to 34 V)	–	–	0.3	%/mA	–
SID.AC.PD.VREG.1	Tstart	Total start up time for the regulator supply outputs	–	–	300	µs	–

6.2.9.4 VBUS discharge specifications

Table 29 VBUS discharge specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.VBUS.DISC.1	Ron1	30 V NMOS ON resistance (with dischg_ds<0> = 1; dischg_ds<4:1> = 0)	1500	–	3000	Ω	–
SID.VBUS.DISC.2	Ron2	30 V NMOS ON resistance (with dischg_ds<1:0> = 1; dischg_ds<4:2> = 0)	750	–	1500	Ω	–
SID.VBUS.DISC.3	Ron3	30 V NMOS ON resistance (with dischg_ds<2:0> = 1; dischg_ds<4:3> = 0)	500	–	1000	Ω	–
SID.VBUS.DISC.4	Ron4	30 V NMOS ON resistance (with dischg_ds<3:0> = 1; dischg_ds<4> = 0)	375	–	750	Ω	–
SID.VBUS.DISC.5	Ron5	30 V NMOS ON resistance (with dischg_ds<4:0> = 1)	300	–	600	Ω	–

6.2.9.5 Provider FET CSA, SCP, RCP

Table 30 Provider FET CSA, SCP, RCP

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
DC.CSA_SCP_RCP.1	SCP_8A	Short circuit current detect @ 8 A	–	±40	–	%	–
DC.CSA_SCP_RCP.3	Ilimit_acc	Current limiting accuracy at 1 A–5 A	–	±15	–	%	–
DC.CSA_SCP_RCP.4	Isense_500mA	Current sensing accuracy at 500 mA	–	±20	–	%	–
DC.CSA_SCP_RCP.5	Iocp_1A	OCP Trip threshold for 1 A	–	130 ± 15	–	%	1 A PD contracts OCP set at 130% of contract value OR user programmable
DC.CSA_SCP_RCP.6	Iocp_5A	OCP Trip threshold for 2 A, 3 A, 4 A and 5 A contracts	–	130 ± 10	–	%	2 A, 3 A, 4 A and 5 A PD contracts OCP set at 130% of contract value or user programmable
DC.CSA_SCP_RCP.7	Vcsa_rcp	Voltage across VBUS_C & VBUS_P for which RCP condition detected	–	12.5	20	mV	–
DC.CSA_SCP_RCP.8	Vbus_max_det	Voltage on VBUS_P pad during provider FET ON (source) for which RCP condition is triggered (this threshold is user programmable)	–	5.375	–	V	–40°C to 70°C TA
AC.CSA_SCP_RCP.1	Toff_scp	Provider NFET switching off after short-circuit current detection	–	1	–	µs	VBUS = 5 V/3 A, Provider path ON, 47 µF ceraminc cap on VBUS_P_P0/1 pins
AC.CSA_SCP_RCP.2	Toff_rcp	Provider NFET switching off after reverse current detect through provider FET (for 28 V hot plug-in)	–	1	–	µs	VBUS = 5 V/3 A, Provider path ON, 47 µF ceraminc cap on VBUS_P_P0/1 pins
AC.CSA_SCP_RCP.3	Ton	Time taken to detect RCP out-of-fault	–	55	80	µs	VBUS_C falls below VBUS _P and start NGDO enable
AC.CSA_SCP_RCP.4	Tilimit	Time taken to limit provider FET current	–	250	–	µs	Time taken between load current crossing the ilimit threshold to load current settling to ilimit

6.2.9.6 VBUS provider transitions

Table 31 VBUS provider transitions

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
DC.NGDO_FET_SYS.1	RDSon	FET RDSon (52-pin QFN)	–	48	–	mΩ	3 A Load current, Short-duration pulse (without self-heating), –40°C to 70°C TA
DC.NGDO_FET_SYS.2	Isw	Continuous current	–	–	3	A	–
AC.NGDO_FET_SY S.1	Ton	VBUS_C Low to High (10% to 90%)	–	5	–	ms	0.8 V to 4.5 V transition on VBUS_C, system-level (100 µF cap and 10 Ω on VBUS_C)
AC.NGDO_FET_SYS.3	Toff	VBUS_C High to Low (90% to 10%) - Under normal condition	–	7	–	µs	4.5 V to 0.8 V transition on VBUS_C, system-level with external FET (with no cap and 10 Ω on VBUS_C)
AC.NGDO_FET_SYS.4	OTSth_OFF	Overtemperature shutdown threshold OFF	–	135	150	°C	–
AC.NGDO_FET_SYS.5	OTSth_ON	Overtemperature shutdown threshold ON	–	90	–	°C	–

6.2.9.7 UVOV

Table 32 UVOV

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.UVOV.1	VTHUVOV1	Voltage threshold accuracy - in active mode using bandgap ref2.	–	±3	–	%	–
SID.UVOV.2	VTHUVOV2	Voltage threshold accuracy - in Deep Sleep mode using Deep Sleep ref.	–	±5	–	%	–
SID.COMP_ACC	COMP_ACC	Comparator input offset at 4 sigma	–15	–	15	mV	–

6.2.9.8 SBU switch

Table 33 SBU switch

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
DC.SBU.1	OVP_threshold	Overvoltage protection detection threshold above vddio	200	–	1200	mV	–40°C to 70°C TA
DC.SBU.2	icc	Block ICC when switch fully ON	–	–	100	µA	–40°C to 70°C TA
DC.SBU.3	Ileak1	Pin leakage current for SBU1, SBU2	–4.5	–	4.5	µA	–40°C to 70°C TA
DC.SBU.4	Ileak2	Pin leakage current for SBU1_5V, SBU2_5V	–1	–	1	µA	–40°C to 70°C TA
DC.SBU_AUX.1	AUX_Ron	ON resistances for AUX switch @ 3.6 V input	–	5	8	Ω	–40°C to 70°C TA
DC.SBU_AUX.2	AUX_Ron_flat	Switch On flat resistances of AUX to SBU1/2 switch (from 0 V to 3.6 V)	–	–	3	Ω	–40°C to 70°C TA
AC.SBU_AUX.1	AUX_Con	Switch Off capacitance	–	120	–	pF	Guaranteed by design
AC.SBU_AUX.2	AUX_BW	–3 dB Bandwidth (Switch ON)	100	–	–	MHz	–40°C to 70°C TA
DC.SBU_DBG.1	I3C_Ron	ON resistances for DBG/I3C switch @ 2 V input	–	–	16	Ω	–40°C to 70°C TA
DC.SBU_DBG.2	I3C_Ron_flat	Switch On flat resistances of DBG/I3C to SBU1/2 switch (from 0 V to 2 V)	–	–	4	Ω	–40°C to 70°C TA
AC.SBU_DBG.1	I3C_Con	Switch Off capacitance	–	120	–	pF	Guaranteed by design
AC.SBU_DBG.2	I3C_BW	–3 dB Bandwidth (Switch ON)	125	–	–	MHz	–40°C to 70°C TA
DC.SBU_LSx.1	UART_Rpu	Pull-Up Resistor	7	10	10.5	KΩ	–40°C to 70°C TA
DC.SBU_LSx.2	UART_Rpd	Pull-Down Resistor	0.7	1	1.05	MΩ	–40°C to 70°C TA
DC.SBU_LSx.3	LSx_Vih	High-Level Input Voltage of UART Pins	0.7 × Vcc	–	–	V	–40°C to 70°C TA; VCC = VDDD (Connector Side) & VCC = 1.8 V (LSx Side)
DC.SBU_LSx.4	LSx_Vih	Low-Level Input Voltage of UART Pins	–	–	0.3 × Vcc	V	–40°C to 70°C TA; VCC = VDDD (Connector Side) & VCC = 1.8 V (LSx Side)
DC.SBU_LSx.5	LSx_Voh	High-Level Output Voltage of UART Pins (IOH = 4 mA)	0.8 × Vcc	–	–	V	–40°C to 70°C TA; VCC = VDDD (Connector Side) & VCC = 1.8 V (LSx Side)
DC.SBU_LSx.6	LSx_Vol	Low-Level Output Voltage of UART Pins (IOL = 4 mA)	–	–	0.2 × Vcc	V	–40°C to 70°C TA; VCC = VDDD (Connector Side) & VCC = 1.8 V (LSx Side)
DC.SBU_LSx.7	LSx_Z	Impedance (Single Ended)	25	50	75	Ω	–40°C to 70°C TA
DC.SBU_LSx.8	LSx_OS	Overshoot of UART Pins	–	–	Vcc + 1	V	–40°C to 70°C TA; VCC = VDDD (Connector Side) & VCC = VDDIO (LSx Side)
DC.SBU_LSx.8	LSx_US	Undershoot of UART Pins	–0.5	–	–	V	–40°C to 70°C TA
AC.SBU_LSx.1	LSx_Cpin_LSxx	Pin Capacitance	–	–	12	pF	–
AC.SBU_LSx.2	LSx_TR_LSxx	Output Rise Time on LSx Pins	–	–	20	ns	–40°C to 70°C TA; CL = 30 pF (including LSx_Cpin_LSxx); Between VOL & VOH
AC.SBU_LSx.3	LSx_TF_LSxx	Output Fall Time on LSx Pins	–	–	20	ns	–40°C to 70°C TA; CL = 30 pF (including LSx_Cpin_LSxx); Between VOL & VOH
DC.SBU.TERM.1	Rpu_aux_1	Pull up resistance on AUX_N	80	–	120	KΩ	–
DC.SBU.TERM.2	Rpu_aux_2	Pull up resistance on AUX_P	0.8	–	1.2	MΩ	–
DC.SBU.TERM.3	Rpd_aux_1	Pull down resistance on AUX_P	80	–	120	KΩ	–

Table 33 SBU switch *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
DC.SBU.TERM.4	Rpd_aux_2	Pull down resistance on AUX_N	0.8	–	1.2	MΩ	–
DC.SBU.TERM.5	Rpd_aux_3	Pull down resistance on AUX_P	329	–	611	KΩ	–
DC.SBU.TERM.6	Rpd_aux_4	Pull down resistance on AUX_N	3.29	–	6.11	MΩ	–
AC.SBU.4	TON	SBU switch turn-on time	–	–	200	µs	–
AC.SBU.5	TOFF	SBU switch turn-off time	–	–	400	µs	–
AC.SBU.3_aux	Off_isolation_AC_aux	Switch isolation at F = 1 MHz, from SBU_5V to SBU pins	−50	–	–	dB	Guaranteed by design
AC.SBU.7_aux	X_talk_AC_1MHz	Cross talk of Switch at F = 1 MHz Cross-talk between UART, AUX and I3C	−50	–	–	dB	Guaranteed by design
AC.SBU.8_aux	X_talk_AC_100kHz	Cross talk of Switch at F = 100 kHz Cross-talk between UART, AUX and I3C	−70	–	–	dB	Guaranteed by design

6.2.9.9 VCONN switch

Table 34 VCONN switch

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.DC.PD.VCONN. 1	Ron	Switch ON resistance at V5V = 5 V with 215 mA load current	–	0.7	1.3	Ω	–
SID.DC.PD.VCONN.3	Ileak	Connector side pin leakage current	–	–	10	µA	–
SID.DC.PD.VCONN.4	VTHDETECT_V5V	Threshold voltage of the v5v detector	2.05	–	2.65	V	–
SID.DC.PD.VCONN.9	Iocp	Overcurrent detection range for CC1/CC2	350	–	900	mA	–
SID.DC.PD.VCONN.10	OVP_threshold	CC1, CC2 overvoltage protection detection threshold above VDDD or V5V whichever is higher	200	–	1200	mV	–
SID.DC.PD.VCONN.11	OVP_hysteresis	Overvoltage protection detection hysteresis	50	–	300	mV	–
SID.DC.PD.VCONN.12	OCP_hysteresis	Overcurrent detection hysteresis	20	–	80	mA	–
SID.AC.PD.VCONN1	Ton	Switch turn-on time	–	–	550	µs	–
SID.AC.PD.VCONN2	Toff	Switch turn-off time	–	–	10	µs	–

6.2.9.10 CC-PHY specifications

Table 35 CC-PHY specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.DC.CC_SHVT.1	vSwing	Transmitter Output High Voltage	1.05	–	1.2	V	–
SID.DC.CC_SHVT.2	vSwing_low	Transmitter Output Low Voltage	–	–	0.075	V	–
SID.DC.CC_SHVT.3	zDriver	Transmitter output impedance	33	–	75	Ω	–
SID.DC.CC_SHVT.4	zBmcRx	Receiver Input Impedance	10	–	–	MΩ	Guaranteed by design
SID.DC.CC_SHVT.5	Idac_std	Source current for USB standard advertisement	64	–	96	µA	–
SID.DC.CC_SHVT.6	Idac_1p5a	Source current for 1.5 A @ 5 V advertisement	165.6	–	194.4	µA	–
SID.DC.CC_SHVT.7	Idac_3a	Source current for 3 A @ 5 V advertisement	303.6	–	356.4	µA	–
SID.DC.CC_SHVT.8	Rd	Pull down termination resistance when acting as UFP (upstream facing port)	4.59	–	5.61	kΩ	–
SID.DC.CC_SHVT.10	zOPEN	CC impedance to ground when disabled	108	–	–	kΩ	–
SID.DC.CC_SHVT.11	DFP_default_0p2	CC Voltages on DFP side - Standard USB	0.15	–	0.25	V	–
SID.DC.CC_SHVT.12	DFP_1.5A_0p4	CC Voltages on DFP side - 1.5 A	0.35	–	0.45	V	–
SID.DC.CC_SHVT.13	DFP_3A_0p8	CC Voltages on DFP side - 3 A	0.75	–	0.85	V	–
SID.DC.CC_SHVT.14	DFP_3A_2p6	CC Voltages on DFP side - 3 A	2.45	–	2.75	V	–
SID.DC.CC_SHVT.15	UFP_default_0p66	CC Voltages on UFP side - Standard USB	0.61	–	0.7	V	–
SID.DC.CC_SHVT.16	UFP_1.5A_1p23	CC Voltages on UFP side - 1.5 A	1.16	–	1.31	V	–
SID.DC.CC_SHVT.17	Vattach_ds	Deep sleep attach threshold	0.3	–	0.6	%	–
SID.DC.CC_SHVT.18	Rattach_ds	Deep sleep pull-up resistor	10	–	50	kΩ	–
SID.DC.CC_SHVT.19	VTX_step	TX Drive voltage step size	80	–	120	mV	No for user and datasheet
SID.DC.CC_SHVT.30	FS_0p53	Voltage threshold for Fast Swap Detect	0.49	–	0.58	V	–

6.2.9.11 Boilerplate specs

Table 36 Boilerplate specs

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
BID#4	TO	Operating Temperature	–40	25	70	°C	Ambient temp inside system enclosure
BID#11	PRG	Device is programmable	–	–	YES	---	See Section Boilerplate Specs in the Spec document
BID#12	PRG_GR	Programming granularity	–	64	–	bytes	Specify min max areas of block programming
BID#13	PRG_WRTP	Device program may be write protected for security	–	–	YES	---	See section Boilerplate specs in the spec document
BID#14	PRG_WRTPGR	Program granularity for write protection, all address ranges	–	64	–	bytes	Specify min max areas of programming
BID#15	RD_PRT	Device program may be read protected for security	–	–	YES	---	See section Boilerplate specs in the spec document
BID#16	PRG_RD_GR	Program granularity for read protection, all address ranges	–	16K	–	bytes	See section Boilerplate specs in the spec document
BID#17	TA	Internal System Ambient Temperature	–40	–	70	°C	Ambient temp inside system enclosure
BID#20	TJ	Junction Temperature	–40	–	125	°C	–
BID#268	PKG_1	Package 1: Type	–	–	QFN	---	BGA, TQFP, QFN, etc.
BID#269	PKG_1Z	Package 1: Height	–	–	1	mm	Must meet customer's system limits (duplicate package rows for each supported package)
BID#270	PKG_1W	Package 1: Width	–	6	–	mm	Must meet customer's system limits
BID#271	PKG_1L	Package 1: Length	–	6	–	mm	Must meet customer's system limits
BID#272	PKG_1PTCH	Package 1: Pin / Bump Pitch	–	0.4	–	mm	Must match customer board capability
BID#273	PKG_1CNT	Package 1: Total signal Pins	–	52	–	pins	Must match customer board capability
BID#274	PKG_1TJA	Package 1: Theta-JA	–	–	32	°C/W	Must meet customer's system limits
BID#274.1	PKG_1TJC	Package 1: Theta-JC	–	–	32	°C/W	Must meet customer's system limits
BID#50	ESD_HBM	Electrostatic discharge human body model	2000	–	–	V	Applicable for all pins except SBU1_P0/1, SBU2_P0/1, CC1_0/1, CC2_0/1, VBUS_P_P0/1 & VBUS_C_P0/1 pins.
BID#51	ESD_HBM_SBU	Electrostatic discharge human body model for SBU1_P0/1, SBU2_P0/1 pins	1000	–	–	V	Only applicable to SBU1_P0/1, SBU2_P0/1 pins
BID#51A	ESD_HBM_CC	Electrostatic discharge human body model for CC1_0/1, CC2_0/1 pins	1000	–	–	V	Only applicable to CC1_0/1 & CC2_0/1 pins
BID#51B	ESD_HBM_VBUS	Electrostatic discharge human body model for VBUS_P_P0/1 & VBUS_C_P0/1 pins	500	–	–	V	Only applicable to VBUS_P_P0/1 & VBUS_C_P0/1 pins
BID#56	ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	Charged Device Model ESD
BID#63	LU	Pin current for Latch-up	–100	–	100	mA	–
BID#186	POR2RDY	Power-on: Logic initialization time	–	3	–	ms	See section Boilerplate specs in the spec document
BID#188	POR_CLKS	Power-on: Will Clocks be absent during Power-up and Reset conditioning?	–	–	YES	---	see section Boilerplate specs in the spec document
BID#191	POR_HIZ_T	Power-on: I/O initialization time	–	3	–	ms	See section Boilerplate specs in the spec document
BID#192	RES_PRES	Power-on: Are there any initialization resources assumed or required by the user?	–	–	YES	---	See section Boilerplate specs in the spec document

Table 36 Boilerplate specs *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
BID#200	POR_INIT	Power-on: Are there special requirements for Program initialization?	–	–	YES	---	See section Boilerplate specs in the spec document
BID#201	WDT_PRES	Upset recovery: Are there any Fail-Safe requirements for this product?	–	–	YES	---	See section Boilerplate specs in the spec document
BID#205	NO_LOAD_COMM	Power down: Is there a requirement for the output pin(s) state in power down?	–	–	YES	---	See section Boilerplate specs in the spec document
BID#207	PWR_NXRES	Can this part power-up without RESET?	–	–	YES	---	See section Boilerplate specs in the spec document
BID#208	PWR_BRND	Can this part indicate a Brown-out without RESET?	–	–	YES	---	See section Boilerplate specs in the spec document
BID#211	POR_HIZ	Does this part have Initialization requirements during external RESET?	–	–	YES	---	See section Boilerplate specs in the spec document
BID#212	POR_PRES	Does this part have requirements for Initialization prior to external RESET?	–	–	YES	---	See section Boilerplate specs in the spec document
BID#227	AC_RIPPLE_V	Power supply noise expectations (amplitude)	–	–	0.1	V	Amplitude of AC riding on DC (pp)
BID#228	AC_RIPPLE_F	Power supply noise expectations (frequency-spectrum)	0	–	20	MHz	Frequency-spectrum of AC riding on DC.
BID#234	PWR_SEQ	Are there any limitations for Power Supply application orders?	–	–	NO	---	–
BID#235	PWR_MON	Can the Power Supply be non-monotonic?	–	–	YES	---	See section Boilerplate specs in the spec document
BID#248	PS_IPEAK	Power Supply hot-plug considerations (inrush current)	–	–	900	mA	–
BID#259	POR_RISE	System Reset or POR rise time	–	–	100	µs	XRES or internal POR monitor
BID#260	POR_FALL	System Reset or POR fall time	–	–	1000	µs	XRES or internal POR monitor
BID#272	CR_LVLS	Clock and Reset Input levels	0.3 × VDDIO	–	0.7 × VDDIO	V	Indicate power levels and power-down requirements for external clock and reset signals. Power supply of the driver chip needs to be same as chip power supply on board which is supplying to Reset and Clock inputs. If not: (1) Analyze power loss situations, which can cause unintentional reset state, (2) Analyze voltage level compatibility issues (e.g., TV input to 3 M clock input), (3) NV memory protection when external clock loss.

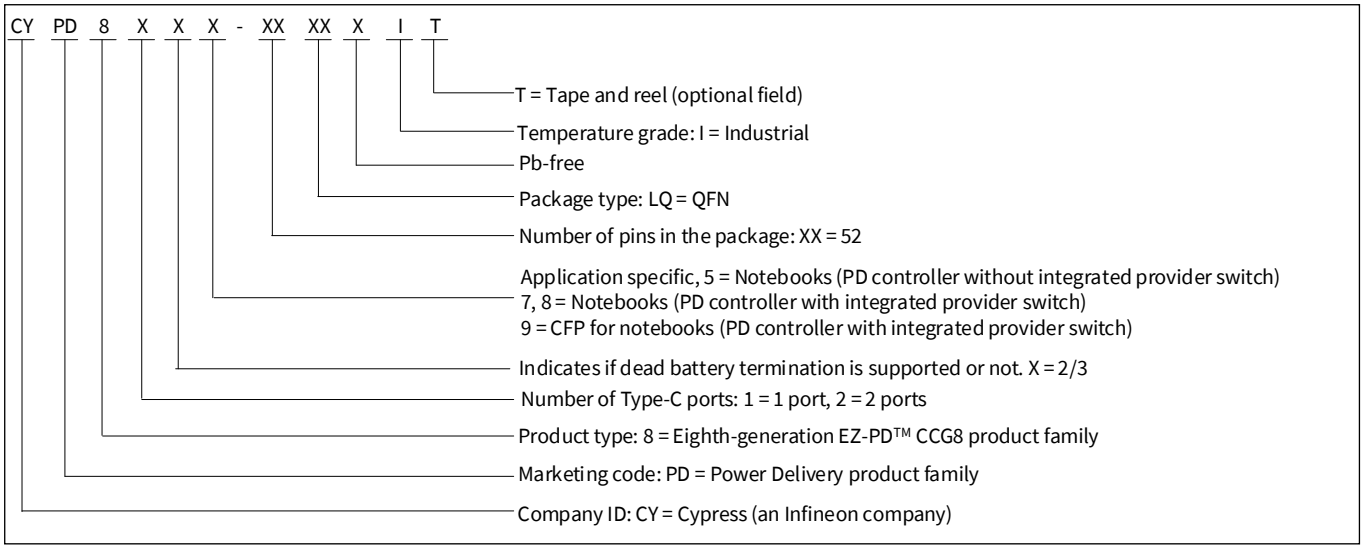
7 Ordering information

Table 37 lists the EZ-PD™ CCG8_CFP part numbers and features.

Table 37 EZ-PD™ CCG8_CFP ordering information

Product	Silicon ID	Application	Type-C ports	Dead battery termination	Termination resistor	Integrated Provider FET on Port0/Port1	Role	Package
CYPD8129-52LQXI	0x3E8011CE	Notebooks	1	Yes	Rp, Rd	Yes/NA	DRP	52-pin QFN
CYPD8129-52LQXIT						Yes/NA		
CYPD8229-52LQXI	0x3E8111CE		2			Yes/Yes		
CYPD8229-52LQXIT						Yes/Yes		
CYPD8139-52LQXI	0x3E9011CE	Docks	1	No		No/NA		
CYPD8139-52LQXIT						No/NA		
CYPD8239-52LQXI	0x3E9111CE		2			No/Yes		
CYPD8239-52LQXIT						No/Yes		

7.1 Ordering code definitions



8 Package diagram

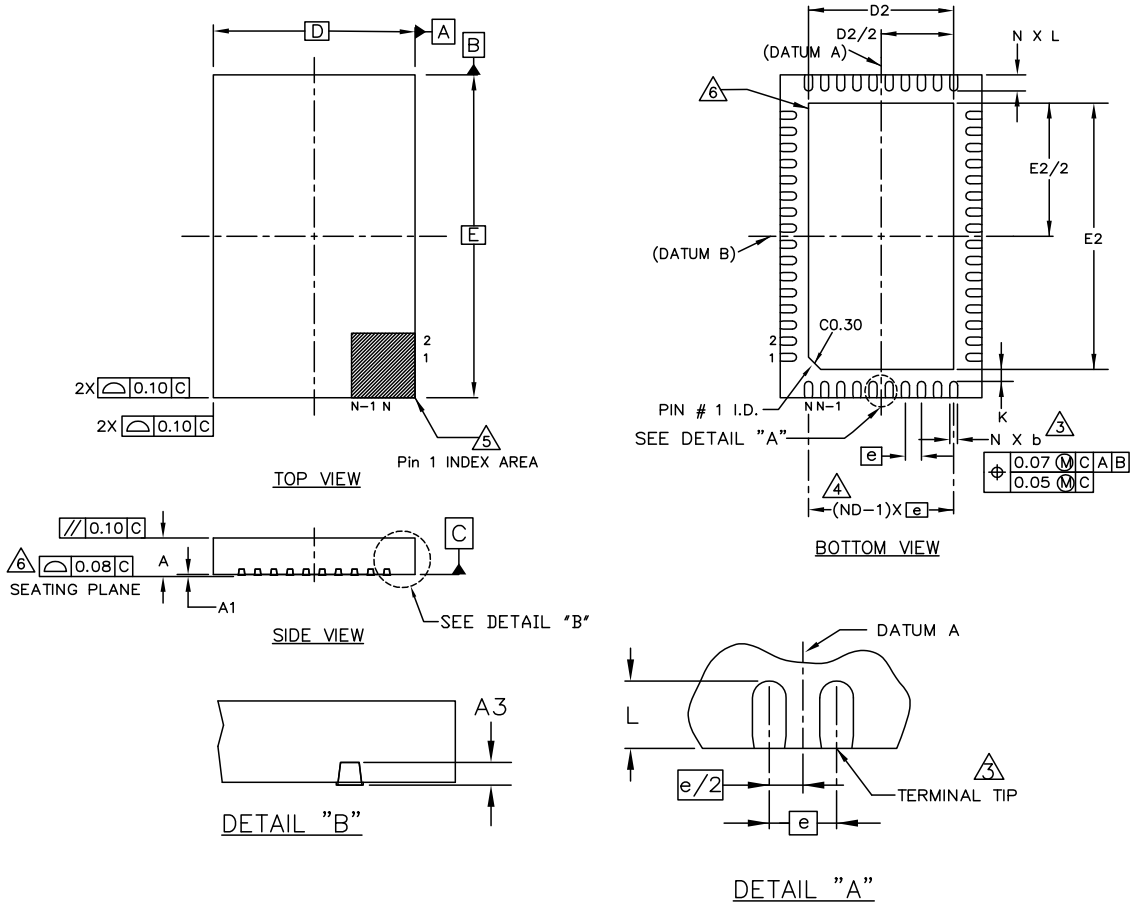
Table 38 EZ-PD™ CCG8_CFP package requirement specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit
BID#17	TA	Internal system ambient temperature	–40	–	70	°C
BID#20	TJ	Junction temperature	–40	–	125	°C
BID#268	PKG_1	Package 1: Type	–	–	QFN	–
BID#269	PKG_1Z	Package 1: Height	–	–	1	mm
BID#270	PKG_1W	Package 1: Width	–	5	–	mm
BID#271	PKG_1L	Package 1: Length	–	8	–	mm
BID#272	PKG_1PTCH	Package 1: Pin/Bump Pitch	–	0.4	–	mm
BID#273	PKG_1CNT	Package 1: Total signal pins	–	52	–	pins
BID#274	PKG_1TJA	Package 1: Theta-JA	–	–	32	°C/W
BID#274.1	PKG_1TJC	Package 1: Theta-JC	–	–	32	°C/W

Table 39 Package details

Package	Description	Package diagram	Spec number
52-pin QFN	52-pin QFN (5.0 × 8.0 × 0.6 mm) with 0.4 mm pitch	See **Figure 24**	002-37974

Package diagram



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
e		0.40 BSC	
N		52	
ND		10	
L	0.30	0.40	0.50
b	0.15	0.20	0.25
D2	3.50	3.60	3.70
E2	6.50	6.60	6.70
D	4.90	5.00	5.10
E	7.90	8.00	8.10
A	0.70	0.80	0.90
A1	0.00	-	0.05
A3		0.152 REF	
K		0.30 REF	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE TOTAL NUMBER OF TERMINALS.
3. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
4. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE.
5. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
6. COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
7. JEDEC SPECIFICATION NO. REF. : N/A.

002-37974 Rev. *A

Figure 24 52-pin QFN (5.0 × 8.0 × 0.9 mm) LT52B, 3.6 × 6.6 mm EPAD (Sawn)

Revision history

Document revision	Date	Description of changes
*D	2024-12-17	Publish to web.
*E	2025-04-30	Updated description and added Note 8 under **Power system requirements overview**. Updated 'VDDIO' pin description under **Table 2** and **Table 3**. Updated details/conditions from 'DC.SBU_LSx.3' to 'DC.SBU_LSx.6' in **Table 33**. Updated ordering information with 'CYPD8239-52LQXI' and 'CYPD8239-52LQXIT' in **Table 37**. Updated **Figure 3**, **Figure 9**, **Figure 10**, **Figure 11**, **Figure 12**, and **Figure 24**.
*F	2026-03-05	Added a column in **Table 37**. Updated values in **Table 31**. Updated **Figure 9**, **Figure 10**, **Figure 11**, **Figure 12**. Added two notes under **Features**. Added note under **Figure 9**, **Figure 10**, **Figure 11**, **Figure 12**.

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