EZ-PD™ CCG7S single-port USB type-C with PD and buck-boost controller

AEC-100 qualified

General description

EZ-PD™ CYPD719X is a highly integrated single-port USB-C Power delivery (PD) solution with an integrated buck-boost controller. It complies with the latest USB-C and PD specifications, and is targeted for automotive charger applications such as head unit (HU) chargers, rear seat entertainment (RSE) and rear seat chargers (RSC). Selected products in the EZ-PD™ CYPD719X product family integrate the external switching FETs to further reduce the BOM and board size. There are three kinds of EZ-PD™ CYPD719X part numbers, the first one is without any integrated FETs, the second is with two buck switching FETs integrated, and the third is with all four switching FETs integrated. Integration offered by EZ-PD™ CYPD719X not only reduces the BOM but also provides a footprint optimized solution for automotive charging needs. It also includes hardware-controlled protection features on the VBUS. EZ-PD™ CYPD719X supports a wide input voltage range (4 V–24 V with 40 V tolerance) and programmable switching frequency (150 kHz–600 kHz) in an integrated PD solution.

EZ-PD™ CYPD719X is the most programmable USB-PD solution with an on-chip 32-bit Arm® Cortex®-M0 processor, 128 KB flash, 16 KB RAM and 32 KB ROM that leaves most flash available for user application use. It also includes various analog and digital peripherals such as ADC, PWMs and timers. The inclusion of a fully programmable MCU with analog and digital peripherals allows the implementation of custom system management functions such as power throttling, load sharing, temperature monitoring, and fault logging.

Applications

- Head unit (HU) charger
- Rear seat charger (RSC)
- Rear seat entertainment (RSE)

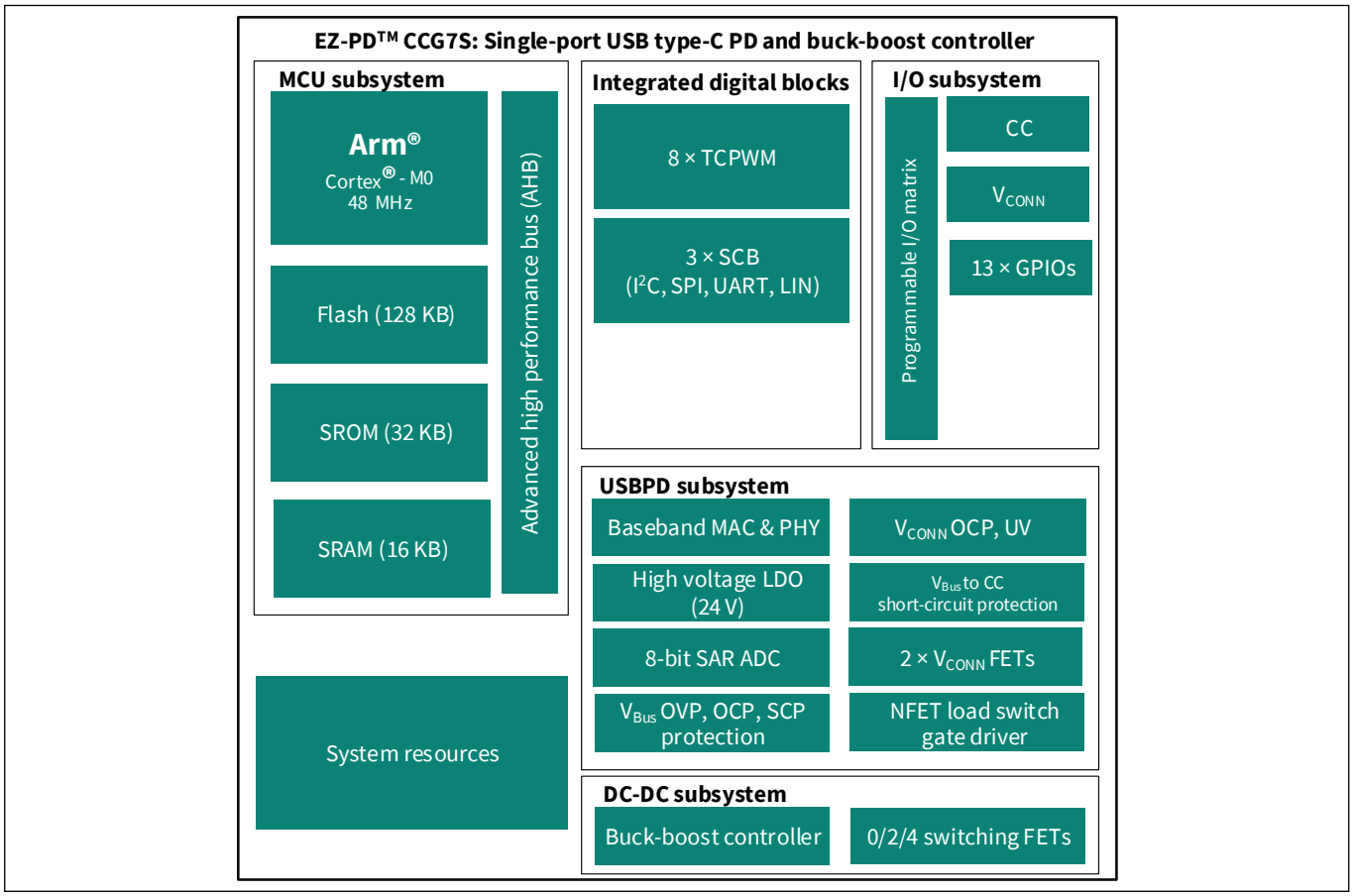
Features

- USBPD
  - Supports one USBPD port
  - Supports latest USBPD 3.2 including programmable power supply (PPS) mode and AVS mode
  - Extended data messaging
- Product validated according to AEC-Q100 Grade 2
- Type-C
  - Configurable resistors R_p and R_d
  - VBUS provider NFET Gate driver
  - Integrated 100 mW VCONN power supply and control
- 1x buck-boost controller
  - 150 kHz to 600 kHz switching frequency
  - 4.5 V to 24 V input, 40 V tolerant
  - 3.3 V to 21.5 V output
  - 20 mV voltage and 50 mA current steps for PPS
  - Supports selectable pulse skipping mode (PSM) and forced continuous current/conduction mode (FCCM)
  - Supports soft start
  - Programmable spread spectrum frequency modulation for low EMI
- 1x legacy/proprietary charging block
  - Supports Qualcomm QC 2.0/3.0/4.0/5.0, Apple charging 3 A, Samsung adaptive fast charging (AFC), USB BC 1.2

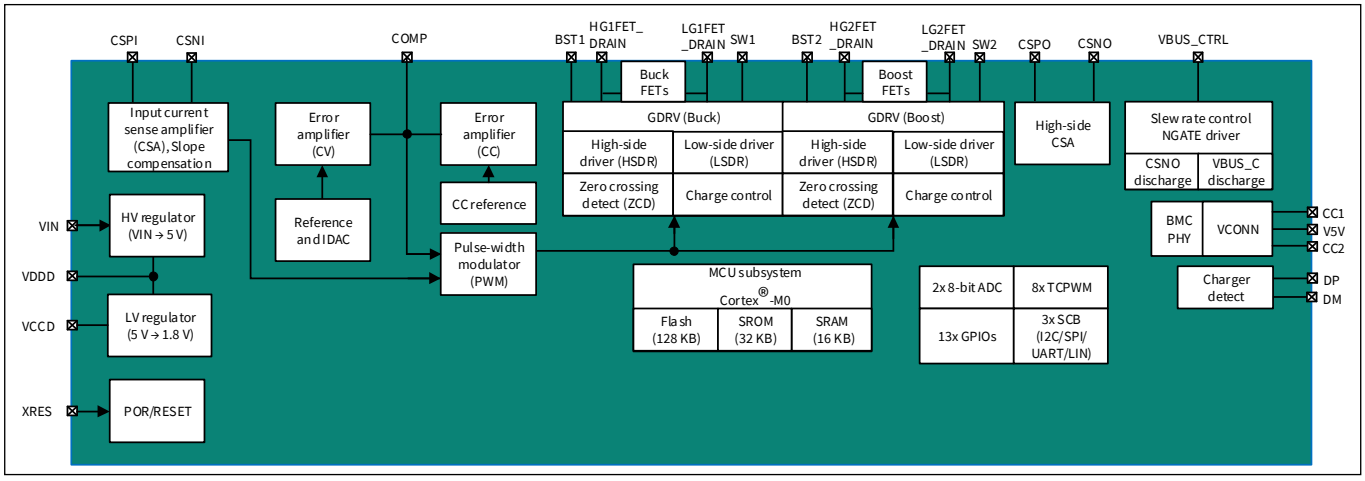
Features

- System-level fault protection
  - On-chip VBUS overvoltage protection (OVP), overcurrent protection (OCP), undervoltage protection (UVP)
  - VBUS to CC short protection
  - VBAT to GND protection FET gate driver
  - Under-voltage lockout (UVLO)
  - Supports over-temperature protection through integrated ADC circuit and internal temperature sensor
  - Supports connector and board temperature measurement using external thermistors
- 32-bit MCU subsystem
  - 48 MHz Arm® Cortex®-M0 CPU
  - 128 KB Flash
  - 16 KB SRAM
  - 32 KB ROM
- Peripherals and GPIOs
  - Up to 13 GPIOs including two overvoltage GPIOs
  - 2x 8-bit ADC
  - 8x 16-bit timer/counter/PWMs (TCPWM)
- Communication interfaces
  - 3x SCBs (I^2C/SPI/UART/LIN)
- Clocks and oscillators
  - Integrated oscillator eliminating the need for an external clock
- Power supply
  - 4 V to 24 V input (40 V tolerant)
  - 3.3 V to 21.5 V output
  - Integrated LDO capable of 5 V @ 75 mA
- Packages
  - EZ-PD™ CYPD719X without integrated FETs: 40-pin QFN, wettable flank, AEC-Q100
  - EZ-PD™ CYPD719X with two buck switching FETs integrated: 39-pin LGA, wettable flank
  - EZ-PD™ CYPD719X with four switching FETs integrated: 40-pin LGA, wettable flank
  - Supports automotive ambient temperature range (–40°C to +105°C) with 125°C operating junction temperature

Logic block diagram



Functional block diagram



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1 Functional overview

1.1 MCU subsystem

1.1.1 CPU

The Arm® Cortex®-M0 in EZ-PD™ CYPD719X devices is a 32-bit MCU, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. It also includes a hardware multiplier, which provides a 32-bit result in one cycle. It includes an Interrupt controller (the NVIC block) with 32 interrupt inputs and a wakeup interrupt controller (WIC), which can wake the processor up from Deep Sleep mode.

1.1.2 Flash ROM and SRAM

EZ-PD™ CYPD719X devices have 128 KB flash and 32 KB ROM for non-volatile storage. ROM stores libraries for authentication and device drivers such as I^2C, SPI, and so on. That spares flash for user application. Flash provides the flexibility to store code for any customer feature and allows firmware upgrades to meet the latest USB power delivery specifications and application needs.

The 16 KB RAM is used under software control to store the temporary status of system variables and parameters. A supervisory ROM that contains boot and configuration routines is provided.

1.2 USBPD subsystem

This subsystem provides the interface to the type-C USB port. This subsystem comprises:

- USBPD physical layer
- VCONN switches and 100 mW VCONN source
- Undervoltage protection (UVP), overvoltage protection (OVP) on VBUS
- Output high-side current sense amplifier (HS CSA) for VBUS
- VBUS discharge control
- Gate driver for VBUS provider NFET
- Charger detection block for legacy charging (for example: BC1.2, Apple charging, and so on)
- VBAT to ground short-circuit protection
- VBUS to CC short-circuit protection

1.2.1 USBPD physical layer

The USBPD subsystem contains the USBPD physical layer block and supporting circuits. The USBPD physical layer consists of a transmitter and receiver that communicate BMC encoded data over the CC channel per the PD 3.2 standard. All communication is half-duplex. The physical layer or PHY implements collision avoidance to minimize communication errors on the channel. The USBPD block includes all termination resistors (R_p and R_d) and their switches as required by the USB-C spec. R_p and R_d resistors are required to implement connection detection, plug orientation detection and for the establishment of the USB source/sink roles. The R_p resistor is implemented as a current source.

The EZ-PD™ CYPD719X device family along with the accompanying firmware is fully complaint with rev 3.2 of the USB Power delivery specification. The device supports programmable power supply (PPS) operation at all valid voltages from 5 V to 21 V.

EZ-PD™ CYPD719X devices support R_p under HW control in unconnected (standby) state to minimize standby power.

EZ-PD™ CYPD719X devices support USBPD extended messages containing data of up to 260 bytes. The extended messages are larger than expected by USBPD 2.0 hardware. As per the USBPD protocol specification, USBPD 3.2 compliant devices implement a chunking mechanism; messages are limited to rev 2.0 sizes unless both source and sink confirm and negotiate compatibility with longer message lengths.

1.2.2 VCONN switches

EZ-PD™ CYPD719X internal LDO voltage regulator is capable of powering a 100 mW VCONN supply for electronically marked cable assemblies (EMCA), VCONN-powered devices (VPD), and VCONN-powered accessories (VPA) as defined in the USB-C specification. All circuitry including VCONN switches and overcurrent protection is integrated in the device. In the event the VCONN current exceeds the VCONN OCP limit, EZ-PD™ CYPD719X can be configured to shut down the type-C port after a certain number of user configurable retries. The port can be re-enabled after a physical disconnect.

1.2.3 VBUS UVP and OVP

VBUS under-voltage and overvoltage faults are monitored using internal resistor dividers. The fault thresholds and response times are user configurable. Refer to the **EZ-PD™ configuration utility** for more details. In the event of a UVP or OVP, EZ-PD™ CYPD719X can be configured to shut down the type-C port after a certain number of user configurable retries. The port can be re-enabled after a physical disconnect.

1.2.4 VBUS OCP and SCP

VBUS overcurrent and short-circuit faults are monitored using internal current sense amplifiers. Similar to OVP and UVP, the OCP and SCP fault thresholds and response times are configurable as well. Refer to the **EZ-PD™ configuration utility** for more details. In the event of OCP or SCP, EZ-PD™ CYPD719X can be configured to shut down the type-C port after a certain number of user configurable retries. The port can be re-enabled after a physical disconnect.

1.2.5 HS-CSA for VBUS

EZ-PD™ CYPD719X device family supports VBUS current measurement and control using an external resistor (5 mΩ) in series with the VBUS path. The voltage drop across this resistor is used to measure the average output current. The same resistor is also used to sense and precisely control the output current in the PPS current foldback mode of operation.

1.2.6 VBUS discharge control

The chip supports high voltage (21.5 V) VBUS discharge circuitry. Upon the detection of device disconnection, faults, or hard resets, the chip will discharge the output VBUS terminals to vSafe5V and/or vSafe0V within the time limits specified in the USBPD specification.

1.2.7 Gate driver for VBUS provider NFET

EZ-PD™ CYPD719X devices have an integrated high voltage gate driver to drive the gate of an external high-side NFET on the VBUS provider path. The gate driver drives the load switch that controls the connection between CSNO and VBUS_C. VBUS_CTRL is the output of this gate driver. To turn off the external NFET, the gate driver drives CSNO low to 0 V. To turn on the external NFET, it drives the gate to CSNO + 8 V. There is an optional slow turn-on feature which reduces the high-current spikes on the output. For a typical gate capacitance of 3 nF, a slow turn-on time of 2 ms to 10 ms is configurable using firmware.

1.2.8 Legacy charge detection and support

EZ-PD™ CYPD719X implements battery charger emulation and detection (source and sink) for USB BC.1.2, legacy Apple charging, Qualcomm quick charge 2.0/3.0/4.0/5.0, and Samsung AFC protocols.

1.2.9 VBAT to ground short protection

EZ-PD™ CYPD719X devices can protect against high currents through the type-C return (ground) path. A NFET and a current sense resistor are placed in series with the ground return path from the type-C connector as shown in **Figure 1**. This resistor senses the current, and if it exceeds the firmware-configured threshold, the NFET is turned off to interrupt the current. This protects against overcurrent conditions caused by external faults (for example, if the type-C connector ground is accidentally connected to the car's battery). The current sense can be implemented with either a single-ended connection (referenced to internal ground) or with a true differential connection (see CSN connection in **Figure 1**). The differential connection provides better current measurement accuracy but uses an extra GPIO pin. In the event of VBAT to ground short protection, EZ-PD™ CYPD719X can be configured to shut down the series FET between the type-C receptacle ground and the system ground. The recovery and retry mechanism can be customized using application firmware.

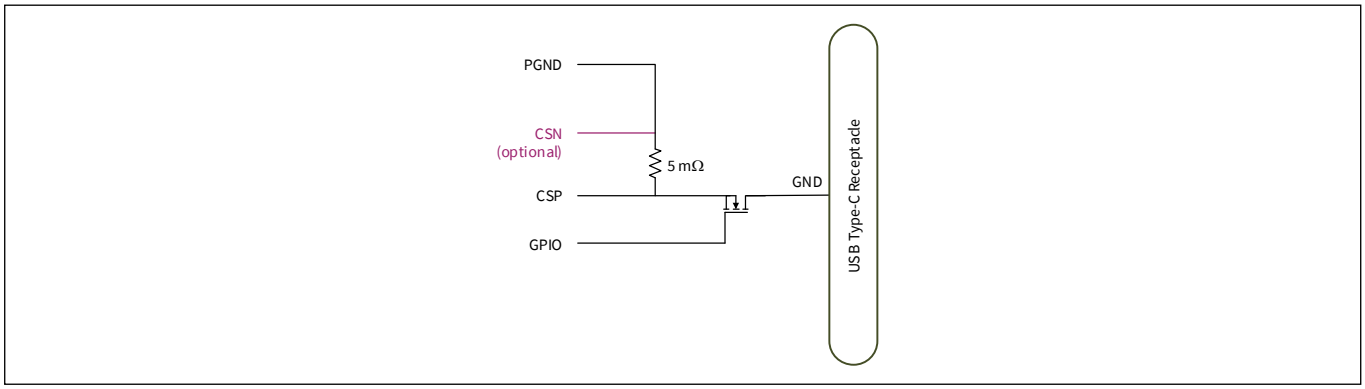


Figure 1 VBAT to ground short circuit protection

1.2.10 VBUS to CC short protection

CC pins have integrated protection from accidental shorts to high voltage VBUS and VBAT. EZ-PD™ CYPD719X devices can handle up to 24 V external voltage on its CC pins without damage. In the event, an overvoltage is detected on the CC pin, it can be configured to shut down the type-C port completely. The port will resume normal operation once the CC voltage detected is within normal range.

1.3 CCGND

The USBPD subsystem includes a separate CGND pin that functions as a remote ground sense. When the Type-C connector is on a separate board, a dedicated sense wire can be routed from the connector to this pin. This configuration eliminates ground potential shifts resulting from long wire resistance.

1.4 Buck-boost subsystem

The buck-boost subsystem in EZ-PD™ CYPD719X devices can be configured to operate in buck-boost mode, buck-only mode or boost-only mode. While buck-boost mode requires four switching FETs, buck-only and boost-only modes require only two FETs. Buck-only mode is useful when EZ-PD™ CYPD719X device's port is used for USB type-A only applications. **Figure 2** shows the buck-boost subsystem's main external components and connections.

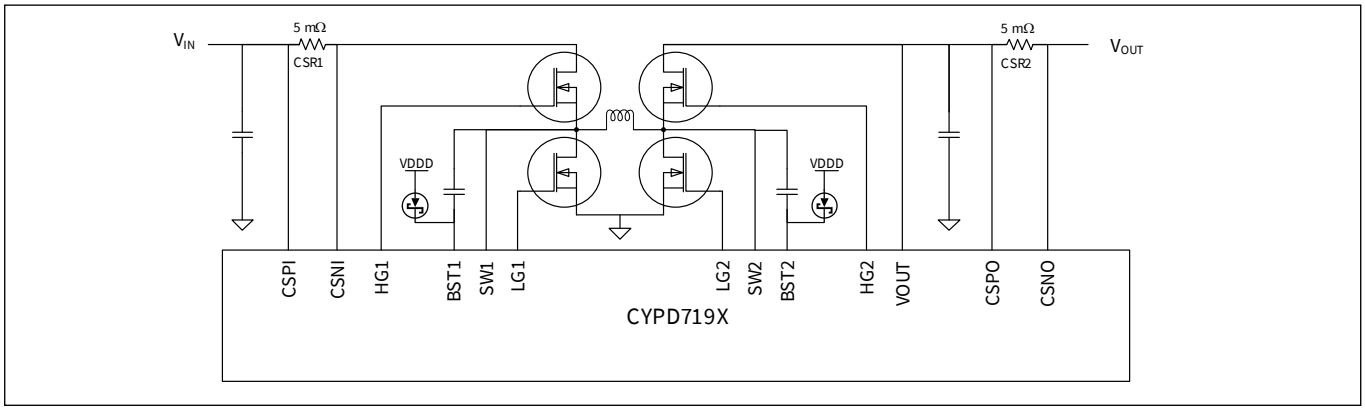


Figure 2 **Buck-boost schematic showing external components using EZ-PD™ CYPD719X without integrated FETs**

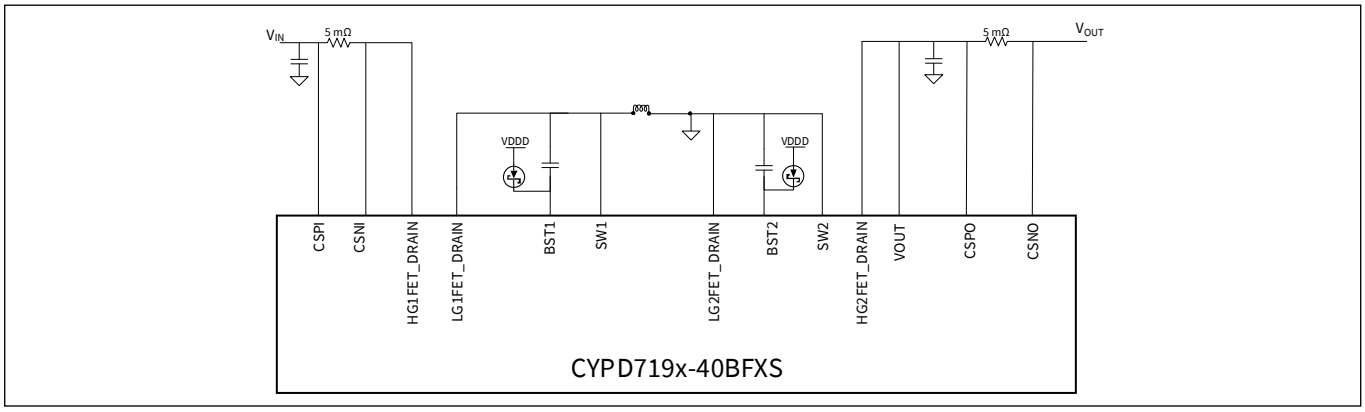


Figure 3 **Buck-boost schematic showing external components using EZ-PD™ CYPD719X with all four integrated FETs**

Buck-boost subsystem in EZ-PD™ CYPD719X devices have the following key functional blocks:

- High side (cycle-by-cycle) current sense amplifier
- High side and low side gate driver
- Pulse width modulator
- Error amplifier

1.4.1 High side (cycle-by-cycle) current sense amplifier (CSA)

EZ-PD™ CYPD719X device's buck-boost controller implements peak current control in both boost and buck modes. A high side current sense amplifier (CSA) is used for peak current sensing through an external resistor (5 as shown in **Figure 2** and **Figure 3**) placed in series with the buck control FET. This current sense amplifier has a high bandwidth and a very wide common mode range. This current sense resistor is connected to the CSA block through pins CSPI and CSNI as shown in **Figure 2** and **Figure 3**. This block implements slope compensation to avoid sub-harmonic oscillation for the internal current loop. In addition to peak current sensing, it provides a current limit comparator for shutting off the buck-boost converter if the current hits an upper threshold which is programmable.

1.4.2 High-side gate driver and low-side gate driver (HG/LG)

EZ-PD™ CYPD719X buck-boost controller provides four n-channel MOSFET gate drivers: two floating high-side gate drivers at the HG1 and HG2 pins, and two ground referenced low-side drivers at the LG1 and LG2 pin. The high side gate drivers drive the high side FET with a nominal VGS of 5 V. The High-side gate driver has a programmable drive strength to drive the switching FET. An external capacitor and Schottky diode form a bootstrap network to collect and store the high voltage source (VIN + ~5 V for HG1 and VBUS + ~5 V for HG2) needed to drive the high-side FET. The low side gate driver drives the low side FET with a nominal VGS of 5 V using energy sourced from EZ-PD™ CYPD719X internal LDO regulator and stored in the capacitor between PVDD and PGND. Low-side gate driver has programmable drive strength to drive the switching FET. In addition to drive strength, the high-side gate driver and the low-side gate driver have programmable options for deadtime control and zero-crossing levels. High-side gate driver and low-side gate driver blocks include zero-crossing detector (ZCD) to implement discontinuous-conduction mode (DCM) mode with diode emulation.

The gate drivers for the switching FETs function at their nominal drive voltage levels (5 V) provided the VIN voltage is between 4.5 V and 24 V.

1.4.3 Error amplifier (EA)

EZ-PD™ CYPD719X buck-boost controller contains two error amplifiers for output voltage and current regulation. The error amplifier is a trans-conductance type amplifier with single compensation pin (COMP) to ground for both the voltage and current loops. In voltage regulation, the output voltage is compared with the internal reference voltage and the output of EA is fed to the PWM block. In current regulation, the average current is sensed by VBUS high side current sense amplifier through the external resistor. The output of the VBUS CSA is compared with an internal reference in error amplifier block and EA output is fed to the PWM block. EZ-PD™ CYPD719X firmware configures and controls the integrated programmable error amplifier circuit for achieving the required VBUS voltage output from the power section.

1.4.4 Pulse width modulator (PWM)

EZ-PD™ CYPD719X device family's PWM block generates the control signals for the gate drivers driving the external FETs in peak current mode control. There are many programmable options for minimum/maximum pulse width, minimum/maximum period, frequency and pulse skip levels to optimize the system design.

EZ-PD™ CYPD719X devices have two firmware-selectable operating modes to optimize efficiency and reduce losses under light load conditions: pulse skipping mode (PSM) and forced continuous conduction mode (FCCM).

1.4.5 Pulse skipping mode (PSM)

In pulse skipping mode, the controller reduces the total number of switching pulses without reducing the active switching frequency by working in "bursts" of normal nominal-frequency switching interspersed with intervals without switching. The output voltage thus increases during a switching burst and decreases during a quiet interval. This mode results in minimal losses at the cost of higher output voltage ripple. When in this mode, EZ-PD™ CYPD719X devices monitor the voltage across the buck or boost sync FET to detect when the inductor current reaches zero; when this occurs, the EZ-PD™ CYPD719X devices switch off the buck or boost sync FET to prevent reverse current flow from the output capacitors (i.e. diode emulation mode). Several parameters of this mode are programmable through firmware, allowing the user to strike their own balance between light load efficiency and output ripple.

1.4.6 Forced continuous conduction mode (FCCM)

In Forced continuous conduction mode (FCCM), the nominal switching frequency is maintained at all times, with the inductor current going below zero (i.e. “backwards” or from the output to the input) for a portion of the switching cycle as necessary to maintain the output voltage and current. This keeps the output voltage ripple to a minimum at the cost of light-load efficiency.

1.5 Buck-boost controller operation regions

The input-side CSA’s output is compared with the output of the error amplifier to determine the pulse width of the PWM. PWM block compares the input voltage and output voltage to determine the buck, boost, and buck-boost regions. The switching time/period of the four gate drivers (HG1, LG1, HG2, LG2) depends upon the region in which the block is operating as well as the mode such as DCM or FCCM. The exact VIN vs VOUT thresholds for transitions into and out of each region are adjustable in firmware including the hysteresis.

1.5.1 Buck region operation (VIN >> VBUS)

When the VIN voltage is significantly higher than the required VBUS voltage, EZ-PD™ CYPD719X devices operate in the buck region. In this region, the boost side FETs are inactivated, with the boost control FET (connected to LG2) turned off and the boost sync FET (connected to HG2) turned on. The buck side FETs are controlled as a buck converter with synchronous rectification as shown in **Figure 4**.

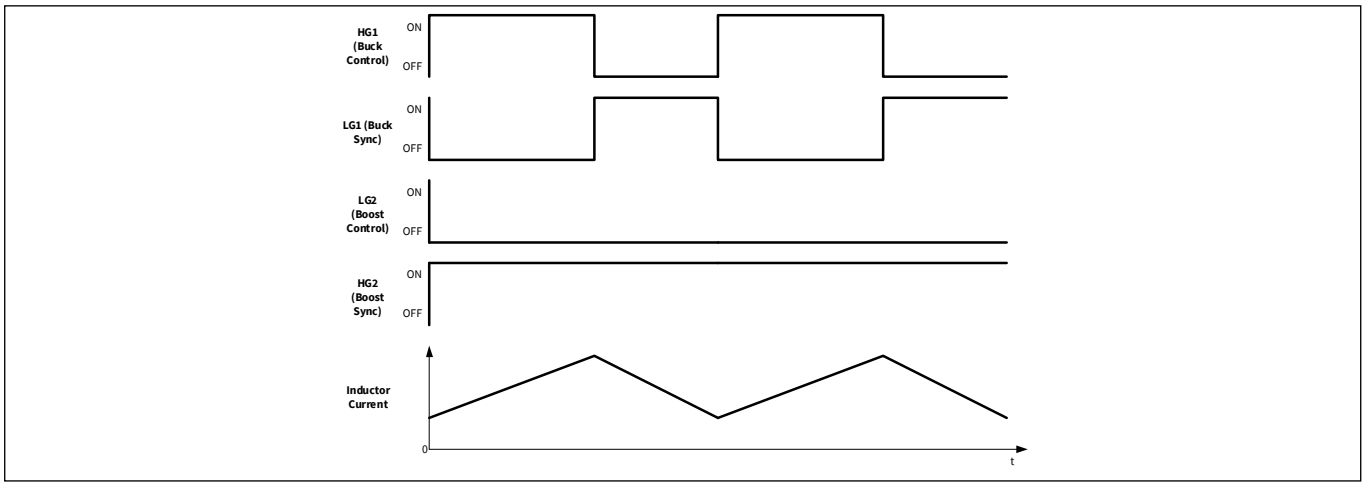


Figure 4 Buck operation waveforms

1.5.2 Boost region operation (VIN << VBUS)

When the VIN voltage is significantly lower than the required VBUS voltage, EZ-PD™ CYPD719X devices operate in the boost region. In this region, the buck side FETs are inactivated, with the sync FET turned off and the buck control FET turned on. The boost side FETs are controlled as a boost converter with synchronous rectification as shown in **Figure 5**.

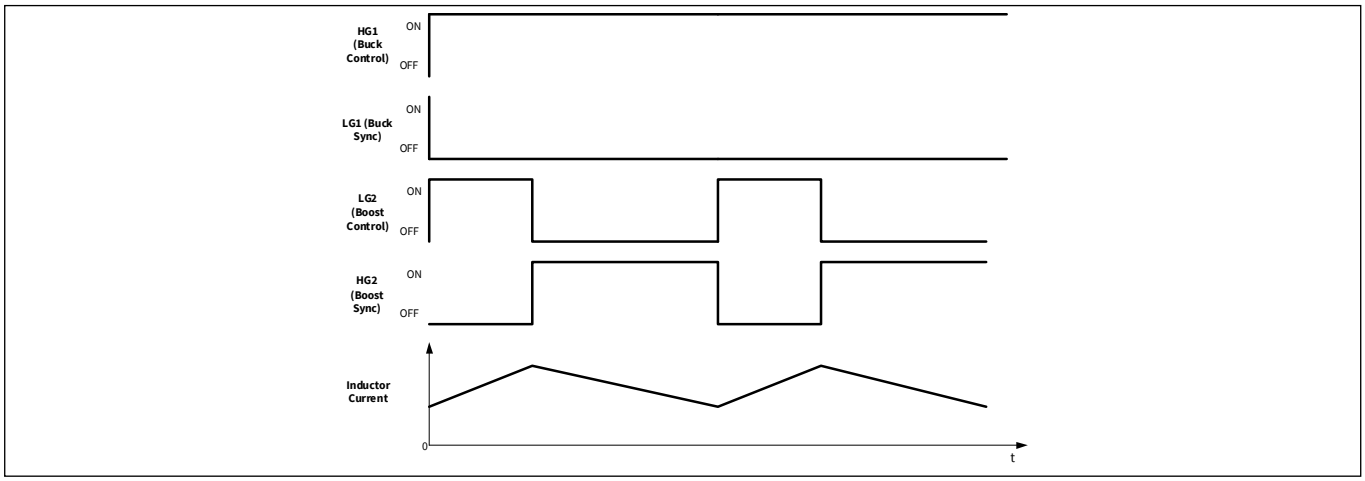


Figure 5 **Boost operation waveforms**

1.5.3 Buck-boost region 1 operation (VIN ~> VBUS)

When the VIN voltage is slightly higher than the required VBUS voltage, EZ-PD™ CYPD719X devices operate in the buck-boost region 1. In this region, the boost side works at a fixed 20% duty cycle (programmable) while the buck side (LG1 / HG1) duty cycle is modulated to control the output voltage. All four FETs are switching every cycle in this operating region as shown in **Figure 6**.

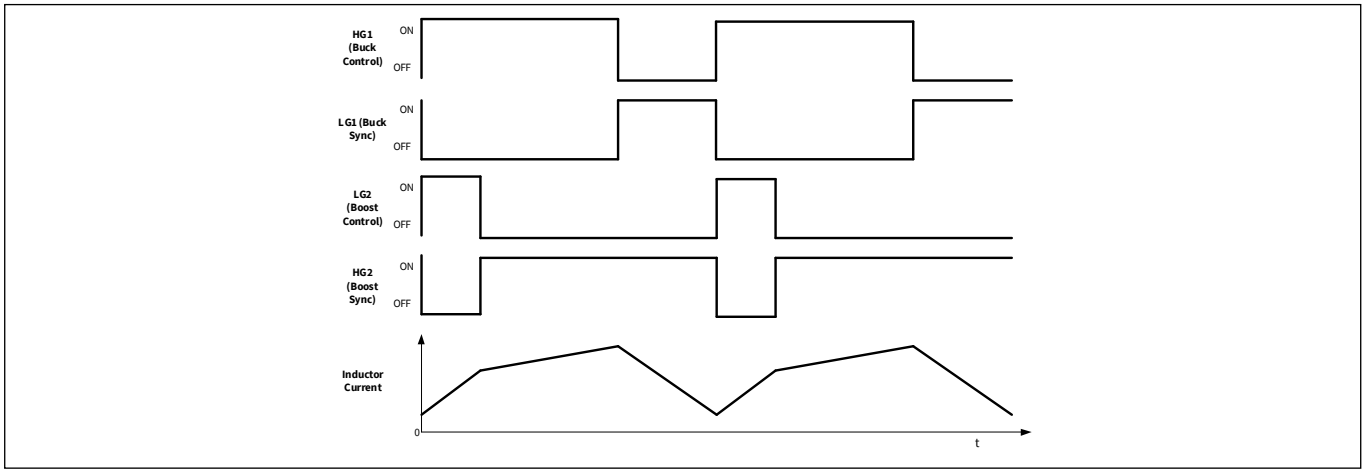


Figure 6 **Buck-boost region 1 (VIN ~> VBUS) operation waveforms**

1.5.4 Buck-boost region 2 operation (VIN ~< VBUS)

When the VIN voltage is slightly lower than the required VBUS voltage, EZ-PD™ CYPD719X devices operate in the buck-boost region 2. In this region, the buck side works at a fixed 80% duty cycle (programmable) while the boost side (LG2) duty cycle is modulated to control the output voltage. All four FETs are switching every cycle in this operating region as shown in **Figure 7**.

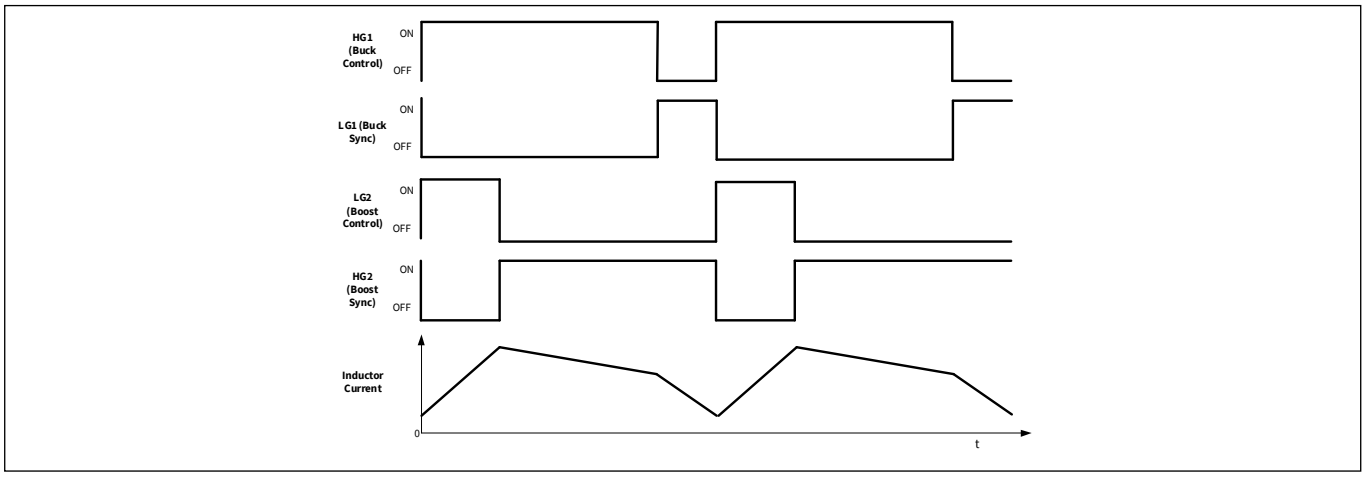


Figure 7 **Buck-boost region 2 (VIN ~< VBUS) operation waveforms**

1.5.5 Switching frequency and spread spectrum

EZ-PD™ CYPD719X devices offer programmable switching frequency between 150 kHz and 600 kHz. The controller supports spread spectrum clocking within the operating frequency range in all operating modes. Spread spectrum is essential for charging applications to meet EMC/EMI requirements by spreading emissions caused by switching over a wide spectrum instead of a fixed frequency, thereby reducing the peak energy at any particular frequency. Both the switching frequency and the spread spectrum span are firmware programmable.

1.6 Analog blocks

1.6.1 ADC

EZ-PD™ CYPD719X devices have two 8-bit SAR ADCs for general purpose A-D conversion applications in the chip. The ADCs can be accessed from the GPIOs through an on-chip analog mux. See **Table 33** for detailed specs on the ADCs.

1.7 Integrated digital blocks

1.7.1 Serial communication block (SCB)

EZ-PD™ CYPD719X devices have three SCB blocks that can be configured for I^2C, SPI, UART or LIN. These blocks implement full multi-master and slave I^2C interfaces capable of multi-master arbitration. This I^2C implementation is compliant with the standard Philips I^2C specification v3.0. These blocks operate at speeds of up to 1 Mbps and have flexible buffering options to reduce interrupt overhead and latency for the CPU. The SCB blocks support 8-byte deep FIFOs for receive and transmit, which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time. The I^2C port I/Os for SCB0 are overvoltage tolerant (OVT). The I^2C ports for SCB1-2 are not OVT tolerant.

1.7.2 Timer, counter, pulse-width modulator (TCPWM)

The TCPWM block of EZ-PD™ CYPD719X devices support eight timers or counters or pulse-width modulators. These timers are available for internal timer use by firmware or for providing PWM-based functions on the GPIOs.

1.8 I/O subsystem

The EZ-PD™ CYPD719X devices have 13 GPIOs including the I^2C and SWD pins which can also be used as GPIOs. The GPIO block implements the following:

- Eight output drive modes
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Disabled
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output disables
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control.
- Overvoltage tolerance (OVT) on one pair of GPIOs

During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix (HSIOM) is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals such as USB-C port are also fixed in order to reduce internal multiplexing complexity. Data output registers and pin state register store, respectively, the values to be driven on the pins and the states of the pins themselves.
The configuration of the pins can be done by the programming of registers through software for each digital I/O port. Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it.

The I/O ports can retain their state during Deep Sleep mode or remain ON. If the operation is restored using reset, then the pins shall go the high-Z state. If operation is restored by an interrupt event, then the pin drivers shall retain their state until firmware chooses to change it. The IOs (on data bus) do not draw current on power down.

1.9 System resources

1.9.1 Watchdog timer

EZ-PD™ CYPD719X devices have a watchdog timer running from the internal low-speed oscillator (ILO). This allows Watchdog operation during Deep Sleep and generate a watchdog reset if not serviced before the timeout occurs. The watchdog reset is recorded in the reset cause register.

1.9.2 Reset

EZ-PD™ CYPD719X devices can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is preserved through reset and allows application firmware to determine the cause of the reset. XRES pin is the dedicated pin for asserting an external hardware reset.

1.9.3 Clock system

EZ-PD™ CYPD719X devices have a fully integrated clock with no external crystal required. EZ-PD™ CYPD719X device's clock system is responsible for providing clocks to all sub-systems that require clocks (SCB and PD) and for switching between different clock sources.

The HFCLK signal can be divided down as shown to generate synchronous clocks for the digital peripherals. The clock dividers have 8-bit, 16-bit and 16-bit fractional divide capability. The 16-bit capability allows a lot of flexibility in generating fine-grained frequency values. The clock dividers generate either enabled clocks (that is, 1 in N clocking where N is the divisor) or an approximately 50% duty cycle clock (exactly 50% for even divisors, one clock difference in the high and low values for odd divisors).

In **Figure 8**, PERXYZ_CLK represents the clocks for different peripherals.

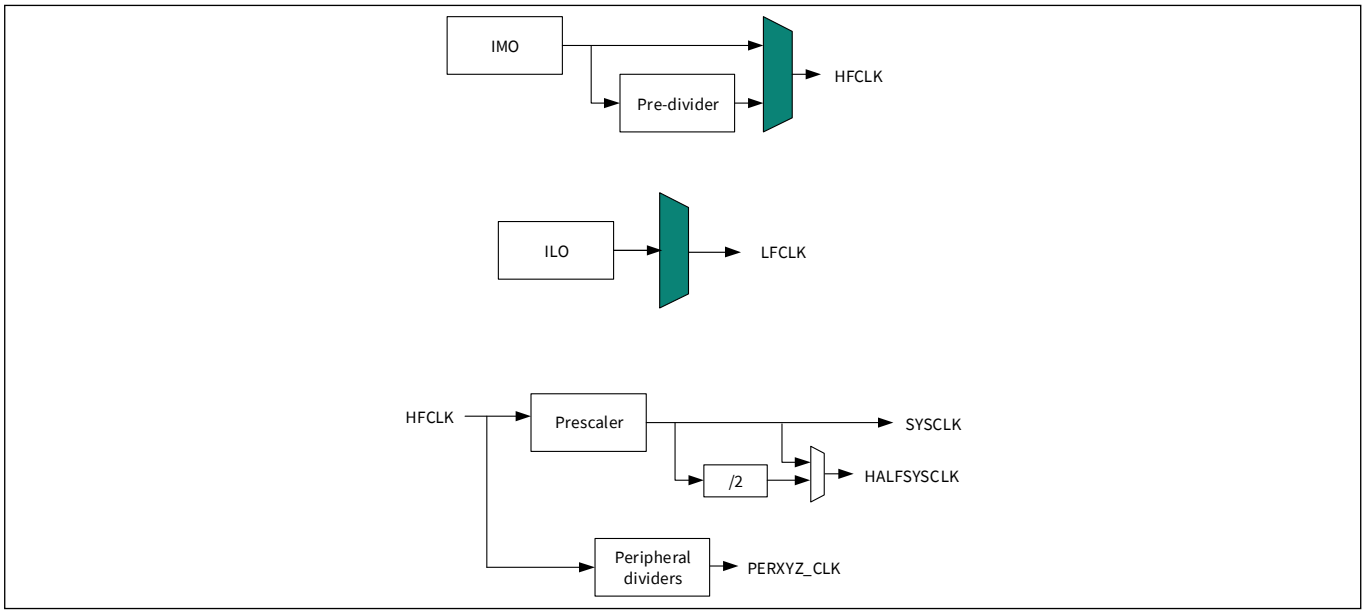


Figure 8 Clocking architecture of EZ-PD™ CYPD719X devices

1.9.4 IMO clock source

The internal main oscillator is the primary source of internal clocking in EZ-PD™ CYPD719X devices. IMO default frequency for EZ-PD™ CYPD719X devices is 48 MHz ± 2%.

1.9.5 ILO clock source

The internal low-power oscillator is a very low-power, relatively inaccurate, oscillator, which is primarily used to generate clocks for peripheral operation in USB suspend (Deep Sleep) mode.

2 Power subsystem

Figure 9 shows an overview of the power subsystem architecture for EZ-PD™ CYPD719X devices. The power subsystem of EZ-PD™ CYPD719X devices operate from VIN supply which can vary from 4 V to 24 V. The VDDD pin, the output of an internal 5 V LDO, gets input from VIN supply. The current capability of the VDDD pin is up to 75 mA including internal as well as external loads. EZ-PD™ CYPD719X devices have two different power modes: Active and Deep Sleep, transitions between which are managed by the power system. The VCCD pin, the output of the core (1.8 V) regulator, is brought out for connecting a 0.1 µF capacitor for the regulator stability only. This pin is not supported as a power supply for external load.

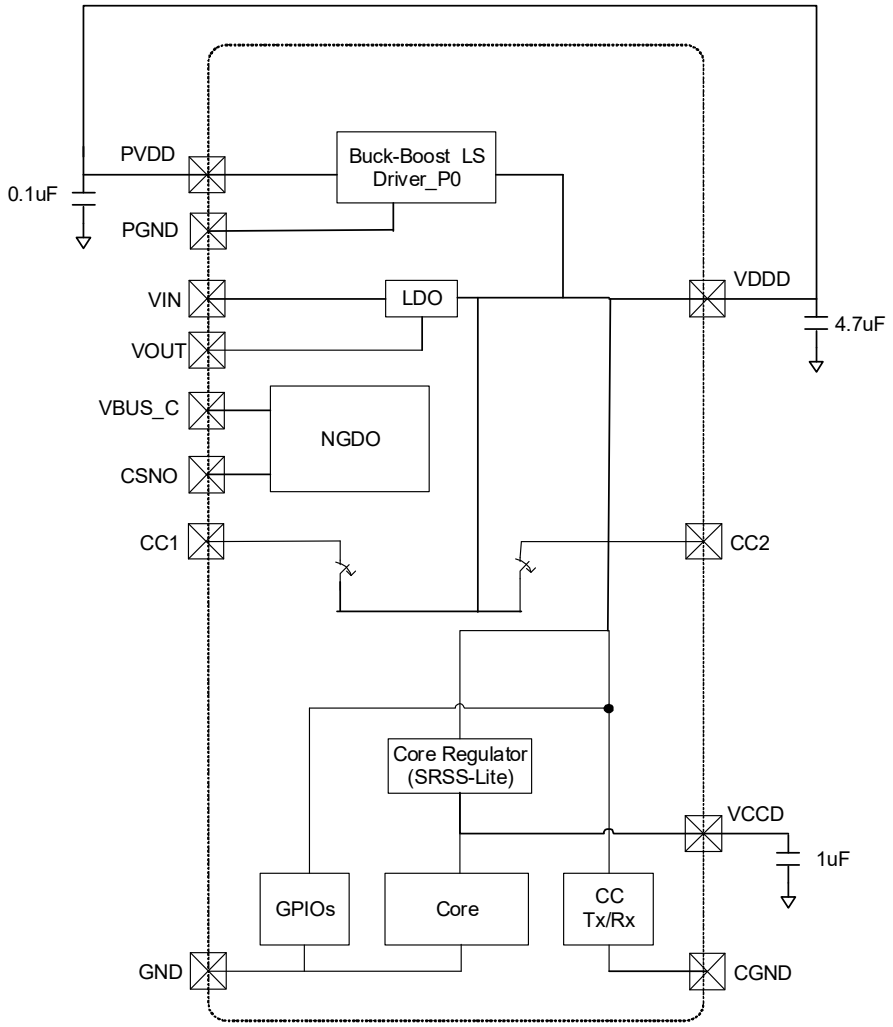


Figure 9 Power system requirement block diagram

2.1 VIN undervoltage lockout (UVLO)

EZ-PD™ CYPD719X supports UVLO to allow the device to shut down when the input voltage is below the reliable level. It guarantees predictable behavior when the device is up and running.

2.2 Using external VDDD supply

By default, external VDDD is not supported for EZ-PD™ CYPD719X devices. However, usage of external VDDD supply can be enabled using firmware. The prerequisite for enabling external forcing of VDDD is to always maintain VIN higher than VDDD.

2.3 Power modes

The Power modes of the device accessible and observable by the user are listed in **Table 1**.

Table 1 Power modes

Mode	Description
RESET	Power is valid and XRES is not asserted. An internal reset source is asserted or Sleep controller is sequencing the system out of reset.
ACTIVE	Power is valid and CPU is executing instructions.
SLEEP	Power is valid and CPU is not executing instructions. All logic that is not operating is clock gated to save power.
DEEP SLEEP	Main regulator and most hard-IP are shut off. Deep Sleep regulator powers logic, but only low-frequency clock is available.
XRES	Power is valid and XRES is asserted. Core is powered down.

3 Pin list

Table 2 CYPD7191, CYPD7199: 40-QFN package pinout

Sl#	Pin name	Absolute minimum (V)	Absolute maximum (V)	Description
1	HG1	–0.5	PVDD + 0.5[1, 2, 3]	Buck high side gate driver output. Connect to the buck (input) side control (high side) FET gate. Use a wide trace to minimize inductance of this connection. Absolute min and max are with respect to SW1 pin.
2	SW1	–0.7	35	Negative power rail of the buck high side gate driver. This is also connected to one input terminal of zero current detection of buck low side gate driver. Connect to the switch node (inductor) on the buck (input) side. Use a short and wide trace to minimize the inductance and resistance of this connection.
3	LG1	–0.5	PVDD + 0.5[1]	Buck low side gate driver output. Connect to the buck (input) side sync (low side) FET gate. Use a wide trace to minimize inductance of this connection.
4	PGND	–0.3	0.3	Ground of low side gate driver. This is also connected to one input terminal of zero current detection of buck low side gate driver. Connect directly to the port's board ground plane.
5	PVDD	–	VDDD	Supply of low side gate driver. Connect to VDDD. Use 1 µF and 0.1 µF bypass capacitors as close to the EZ-PD™ CYPD719X IC as possible.
6	LG2	–0.5	PVDD + 0.5[1]	Boost low side gate driver output. Connect to the boost (output) side control (low side) FET gate. Use a wide trace to minimize inductance of this connection.
7	VOUT	–0.3	24	Output of the Buck-boost converter. This is also connected to one input terminal of reverse current protection of Boost high side gate driver. Connect to the boost sync (high side) FET's drain. Use a dedicated (Kelvin) trace for this connection.
8	SW2	–0.3	24	Negative power rail of the boost high side gate driver. This is also connected to one input terminal of reverse current protection of boost high side gate driver. Connect to the switch node (inductor) on the boost (output) side. Use a short and wide trace to minimize the inductance and resistance of this connection.
9	HG2	–0.5	PVDD + 0.5[1, 4]	Boost high side gate driver output. Connect to the boost (output) side sync (high side) FET gate. Use a wide trace to minimize inductance of this connection.

Notes
1. Maximum voltage must not exceed 6 V.
2. Maximum absolute voltage w.r.t GND must not exceed 40 V.
3. The absolute maximum value is with respect to SW1.
4. The absolute maximum value is with respect to SW2.

Table 2 CYPD7191, CYPD7199: 40-QFN package pinout *(continued)*

Sl#	Pin name	Absolute minimum (V)	Absolute maximum (V)	Description
10	BST2	–	PVDD + 0.5[1, 4]	Boosted power supply of the boost high side gate driver. Bootstrap capacitor node. Connect Schottky diode from VDDD to BST2. Also, connect a bootstrap capacitor from this pin to SW2.
11	VBUS_CTRL	–0.5	32	VBUS NFET gate driver output. Connect to the provider NFET's gate.
12	COMP	–0.5	PVDD + 0.5[1]	Error amplifier output pin. Connect a compensation network to GND. Contact Infineon for assistance in designing the compensation network.
13	VBUS_C	–0.3	24	type-C connector VBUS voltage. Connect to the type-C connector's VBUS pin.
14	CSNO	–0.3	24	Negative input of output current sensing amplifier. Connect to negative terminal of the output current sense resistor.
15	CSPO	–0.3	24	Positive input of output current sensing amplifier. Connect to positive terminal of the output current sense resistor.
16	CC2	–0.5	24	Type-C connector configuration channel 2. Connect directly to the CC2 pin on the port's Type-C connector. Also connect a 390-pF capacitor to ground.
17	CC1	–0.5	24	Type-C connector configuration channel 1. Connect directly to the CC1 pin on the port's Type-C connector. Also connect a 390-pF capacitor to ground.
18	DP_GPIO0	–0.5	PVDD + 0.5[1]	USB D+/GPIO: D+ for implementing BC 1.2, AFC, QC or Apple charging. EZ-PD™ CYPD719X does not support USB data transmission on this pin.
19	DM_GPIO1	–0.5	PVDD + 0.5[1]	USB D–/GPIO: D– for implementing BC 1.2, AFC, QC or Apple charging. EZ-PD™ CYPD719X does not support USB data transmission on this pin.
20	VDDD	–	6	5 V LDO output. Connect a 1 µF ceramic bypass capacitor to this pin.
21	CSP_GPIO2	–0.5	PVDD + 0.5[1]	GPIO/positive input terminal of VBAT - GND protection circuit. Connect to the positive terminal of the VBAT - GND short protection current sense resistor.
22	CSN_GPIO3	–0.5	PVDD + 0.5[1]	GPIO/negative input terminal of VBAT - GND protection circuit/hot plug detect. Connect to the negative terminal of the VBAT - GND short protection current sense resistor. For single-ended current sensing, this pin need not be connected to the current sense resistor. For applications supporting DisplayPort (for example, Rear seat entertainment (RSE)), this is the Hotplug Detect output pin.

Notes
1. Maximum voltage must not exceed 6 V.
2. Maximum absolute voltage w.r.t GND must not exceed 40 V.
3. The absolute maximum value is with respect to SW1.
4. The absolute maximum value is with respect to SW2.

Table 2 CYPD7191, CYPD7199: 40-QFN package pinout *(continued)*

Sl#	Pin name	Absolute minimum (V)	Absolute maximum (V)	Description
23	GPIO4	–0.5	PVDD + 0.5[1]	GPIO/VBAT to GND protection FET gate drive.
24	CGND	–0.3	0.5	CC block ground. Connect to the exposed pad (EPAD).
25	GPIO5	–0.5	PVDD + 0.5[1]	GPIO
26	GPIO6	–0.5	PVDD + 0.5[1]	GPIO
27	GPIO7	–0.5	PVDD + 0.5[1]	GPIO
28	GPIO8	–0.5	PVDD + 0.5[1]	GPIO/SWD programming and debug clock signal.
29	GPIO9	–0.5	PVDD + 0.5[1]	GPIO/SWD programming and debug data signal.
30	GPIO10	–0.5	PVDD + 0.5[1]	GPIO
31	XRES	–0.5	PVDD + 0.5[1]	External reset - active LOW. Contains a 3.5 kΩ to 8.5 kΩ internal pull-up.
32	GPIO11	–0.5	PVDD + 0.5[1]	GPIO
33	GPIO12	–0.5	PVDD + 0.5[1]	GPIO
34	GND	–	–	Chip ground. Connect to the exposed pad (EPAD).
35	VDDD	–	6	5 V LDO output. Connect a 10 µF bypass capacitor to this pin.
36	VCCD	–	–	1.8 V core LDO output. Connect a 0.1 µF bypass capacitor to ground. Do not connect anything else to this pin.
37	VIN	–0.3	40	4 V–24 V input supply. Connect a ceramic bypass capacitor to GND close to this pin.
38	CSPI	–0.3	40	Positive input of input current sense amplifier. Connect to the positive terminal of the input current sense resistor. Use a dedicated (Kelvin) connection.
39	CSNI	–0.3	40	Negative input of Input current sense amplifier. Connect to the negative terminal of the input current sense resistor. Use a dedicated (Kelvin) connection.
40	BST1	–	PVDD + 0.5[1, 2, 3]	Boosted power supply of the buck high side gate driver. Bootstrap capacitor node. Connect Schottky diode from VDDD to BST1. Also, connect a bootstrap capacitor from this pin to SW1.
–	EPAD	–	–	Exposed ground pad. Connect directly to pin 34.

Notes
1. Maximum voltage must not exceed 6 V.
2. Maximum absolute voltage w.r.t GND must not exceed 40 V.
3. The absolute maximum value is with respect to SW1.
4. The absolute maximum value is with respect to SW2.

Table 3 CYPD7192, CYPD7193, CYPD7198: 39-LGA package pinout

Pin no.	Pin name	Absolute minimum (V)	Absolute maximum (V)	Description
1	NC	–0.5	VIN + PVDD + 0.5[6]	Floating, do not connect
2	SW1	–0.7	35	Negative power rail of the buck high-side gate driver. This is also connected to one input terminal of zero current detection of buck low-side gate driver. Connect to the switch node (inductor) on the buck (input) side. Use a short and wide trace to minimize the inductance and resistance of this connection.
3	NC	–0.5	PVDD + 0.5[5]	Floating, do not connect
4	PVDD	–	VDDD	Supply of low-side gate driver. Connect to VDDD. Use 1 µF and 0.1 µF bypass capacitors as close to the EZ-PD™ CCG7SAF IC as possible.
5	LG2	–0.5	PVDD + 0.5[5]	Boost low-side gate driver output. Connect to the boost (output) side control (low side) FET gate. Use a wide trace to minimize inductance of this connection.
6	VOUT	–0.3	24	Output of the buck-boost converter. This is also connected to one input terminal of reverse current protection of Boost high-side gate driver. Connect to the boost sync (high side) FET's drain. Use a dedicated (Kelvin) trace for this connection.
7	SW2	–0.3	24	Negative power rail of the boost high-side gate driver. This is also connected to one input terminal of reverse current protection of boost high-side gate driver. Connect to the switch node (inductor) on the boost (output) side. Use a short and wide trace to minimize the inductance and resistance of this connection.
8	HG2	–0.5	VOUT + PVDD + 0.5[6]	Boost high-side gate driver output. Connect to the boost (output) side sync (high side) FET gate. Use a wide trace to minimize inductance of this connection.

Notes
5. Max voltage must not exceed 6 V.
6. Max absolute voltage wrt GND must not exceed 40 V.

Table 3 CYPD7192, CYPD7193, CYPD7198: 39-LGA package pinout *(continued)*

Pin no.	Pin name	Absolute minimum (V)	Absolute maximum (V)	Description
9	BST2	–	PVDD + 0.5[5]	Boosted power supply of the boost high-side gate driver. Bootstrap capacitor node. Connect Schottky diode from VDDD to BST2. Also, connect a bootstrap capacitor from this pin to SW2.
10	VBUS_CTRL	–0.5	32	VBUS NFET gate driver output. Connect to the provider NFET's gate.
11	COMP	–0.5	PVDD + 0.5[5]	Error amplifier output pin. Connect a compensation network to GND. Contact Infineon for assistance in designing the compensation network.
12	VBUS_C	–0.3	24	Type-C connector VBUS voltage. Connect to the type-C connector's VBUS pin.
13	CSPO	–0.3	24	Positive input of output current sensing amplifier. Connect to positive terminal of the output current sense resistor.
14	CSNO	–0.3	24	Negative input of output current sensing amplifier. Connect to negative terminal of the output current sense resistor.
15	CC2	–0.5	24	Type-C connector configuration channel 2. Connect directly to the CC2 pin on the port's type-C connector. Also connect a 390 pF capacitor to ground.
16	CC1	–0.5	24	Type-C connector configuration channel 1. Connect directly to the CC2 pin on the port's type-C connector. Also connect a 390 pF capacitor to ground.
17	DP_GPIO0	–0.5	PVDD + 0.5[5]	USB D+/GPIO: D+ for implementing BC 1.2, AFC, QC or Apple charging. EZ-PD™ CCG7SAF does not support USB data transmission on this pin.
18	DM_GPIO1	–0.5	PVDD + 0.5[5]	USB D+/GPIO: D– for implementing BC 1.2, AFC, QC or Apple charging. EZ-PD™ CCG7SAF does not support USB data transmission on this pin.
19	VDDD	–	6	5 V LDO output. Connect a 1 µF ceramic bypass capacitor to this pin.

Notes
5. Max voltage must not exceed 6 V.
6. Max absolute voltage wrt GND must not exceed 40 V.

Table 3 CYPD7192, CYPD7193, CYPD7198: 39-LGA package pinout *(continued)*

Pin no.	Pin name	Absolute minimum (V)	Absolute maximum (V)	Description
20	CSP_GPIO2	–0.5	PVDD + 0.5[5]	GPIO/ positive input terminal of VBAT – GND protection circuit. Connect to the positive terminal of the VBAT – GND short protection current sense resistor.
21	CSN_GPIO3	–0.5	PVDD + 0.5[5]	GPIO/negative input terminal of VBAT – GND protection circuit/hot plug detect. Connect to the negative terminal of the VBAT – GND short protection current sense resistor. For single-ended current sensing, this pin need not be connected to the current sense resistor. For applications supporting DisplayPort (for example, Rear seat entertainment (RSE)), this is the Hotplug Detect output pin.
22	GPIO4	–0.5	PVDD + 0.5[5]	GPIO
23	CGND	–0.3	0.5	CC block ground. Connect to the exposed pad (EPAD).
24	GPIO5	–0.5	PVDD + 0.5[5]	GPIO
25	GPIO6	–0.5	PVDD + 0.5[5]	GPIO
26	GPIO7	–0.5	PVDD + 0.5[5]	GPIO
27	GPIO8	–0.5	PVDD + 0.5[5]	GPIO/SWD programming and debug clock signal
28	GPIO9	–0.5	PVDD + 0.5[5]	GPIO/SWD programming and debug data signal
29	GPIO10	–0.5	PVDD + 0.5[5]	GPIO
30	XRES	–0.5	PVDD + 0.5[5]	External reset – active low. Contains a 3.5 kΩ to 8.5 kΩ internal pull-up.
31	GPIO11	–0.5	PVDD + 0.5[5]	GPIO
32	GPIO12	–0.5	PVDD + 0.5[5]	GPIO
33	VDDD	–	6	5 V LDO output. Connect a 10 µF bypass capacitor to this pin.
34	VCCD	–	–	1.8 V core LDO output. Connect a 0.1 µF bypass capacitor to ground. Do not connect anything else to this pin.
35	VIN	–0.3	40	4 V–24 V input supply. Connect a ceramic bypass capacitor to GND close to this pin.

Notes
5. Max voltage must not exceed 6 V.
6. Max absolute voltage wrt GND must not exceed 40 V.

Table 3 CYPD7192, CYPD7193, CYPD7198: 39-LGA package pinout *(continued)*

Pin no.	Pin name	Absolute minimum (V)	Absolute maximum (V)	Description
36	CSPI	–0.3	40	Positive input of input current sense amplifier. Connect to the positive terminal of the input current sense resistor. Use a dedicated (Kelvin) connection.
37	CSNI	–0.3	40	Negative input of Input current sense amplifier. Connect to the negative terminal of the input current sense resistor. Use a dedicated (Kelvin) connection.
38	BST1	–	PVDD + 0.5[5]	Boosted power supply of the buck high-side gate driver. Bootstrap capacitor node. Connect Schottky diode from VDDD to BST1. Also, connect a bootstrap capacitor from this pin to SW1.
39	PGND	–0.3	0.3	Ground of low-side gate driver. This is also connected to one input terminal of zero current detection of buck low-side gate driver. Connect directly to the port's board ground plane.
EPAD P1	LGFET_DRAIN	–	–	Exposed drain of LG1FET
EPAD P2	HGFET_DRAIN	–	–	Exposed drain of HG1FET
EPAD P3	EPAD	–	–	GND

Notes
5. Max voltage must not exceed 6 V.
6. Max absolute voltage wrt GND must not exceed 40 V.

Table 4 CYPD7194, CYPD7195, CYPD7196, CYPD7197: 40-LGA package pinout

Pin no.	Pin name	Absolute minimum (V)	Absolute maximum (V)	Description
1	GPIO9	–0.5	PVDD + 0.5[7]	P1.0: GPIO/SWD programming and debug data signal
2	GPIO10	–0.5	PVDD + 0.5[7]	P2.2: GPIO
3	XRES	–0.5	PVDD + 0.5[7]	External reset – active LOW. Contains a 3.5 kΩ to 8.5 kΩ internal pull-up.
4	GPIO11	–0.5	PVDD + 0.5[7]	P3.0: GPIO
5	GPIO12	–0.5	PVDD + 0.5[7]	P3.1: GPIO
6	VDDD	–	6	5 V LDO output. Connect a 10 µF bypass capacitor to this pin.
7	VCCD	–	–	1.8 V core LDO output. Connect a 0.1 µF bypass capacitor to ground. Do not connect anything else to this pin.
8	VIN	–0.3	40	4 V–24 V input supply. Connect a ceramic bypass capacitor to GND close to this pin.
9	CSPI	–0.3	40	Positive input of input current sense amplifier. Connect to the positive terminal of the input current sense resistor. Use a dedicated (Kelvin) connection.
10	CSNI	–0.3	40	Negative input of Input current sense amplifier. Connect to the negative terminal of the input current sense resistor. Use a dedicated (Kelvin) connection.
11	HG1FET_DRAIN	–	40	Buck MOSFET drain, which is Input to the Buck control / high side MOSFET
12	BST1	–	PVDD + 0.5[7]	Boosted power supply of the buck high-side gate driver. Bootstrap capacitor node. Connect Schottky diode from VDDD to BST1. Also, connect a bootstrap capacitor from this pin to SW1.
13	PGND	–0.3	0.3	Ground of low-side gate driver. Connect directly to the Buck synchronous / low side MOSFET source. This is also connected to one input terminal of zero current detection (ZCD) circuit.
14	LG1FET_DRAIN	–	40	Buck synchronous MOSFET drain, which is Buck switch node. It is connected to the drain of the internal Buck synchronous / low side MOSFET and the source of internal Buck control / high side Buck MOSFET.
15	SW1	–0.7	35	Negative power rail of the buck high-side gate driver. Connect to the switch node (inductor) on the buck (input) side. This is also connected to another input terminal of zero current detection (ZCD) circuit.

Notes
7. Maximum voltage must not exceed 6 V.
8. Maximum absolute voltage wrt GND must not exceed 40 V.

Table 4 CYPD7194, CYPD7195, CYPD7196, CYPD7197: 40-LGA package pinout *(continued)*

Pin no.	Pin name	Absolute minimum (V)	Absolute maximum (V)	Description
16	PVDD	–	VDDD	Supply of low-side gate driver. Connect to VDDD. Use 1 µF and 0.1 µF bypass capacitors as close to the EZ-PD™ CCG7SA4F IC as possible.
17	SW2	–0.3	24	Negative power rail of the boost high-side gate driver. This is connected to one input terminal of reverse current protection (RCP) circuit. Connect to the switch node (inductor) on the boost (output) side.
18	LG2FET_DRAIN	–	40	Boost / control MOSFET drain, which is Boost switch node. It is connected to the drain of the internal Boost control / low side MOSFET and the source of internal synchronous/ high side Boost MOSFET
19	PGND	–0.3	0.3	Ground of low-side Boost MOSFET gate driver.. Connect directly to the low-side Boost MOSFET source.
20	BST2	–	PVDD + 0.5[7]	Boosted power supply of the boost high-side gate driver. Bootstrap capacitor node. Connect Schottky diode from VDDD to BST2. Also, connect a bootstrap capacitor from this pin to SW2.
21	HG2FET_DRAIN	–	40	Boost MOSFET drain, which is output of synchronous Boost / High side MOSFET. This also output of the buck-boost converter. This is connected to another input terminal of reverse current protection (RCP) circuit
22	VOUT	–0.3	24	Output of the buck-boost converter. This is also connected to one input terminal of reverse current protection of Boost high-side gate driver. Connect to the boost sync (high side) FET's drain. Use a dedicated (Kelvin) trace for this connection.
23	VBUS_CTRL	–0.5	32	VBUS NFET gate driver output. Connect to the provider NFET's gate.
24	COMP	–0.5	PVDD + 0.5[7]	Error amplifier output pin. Connect a compensation network to GND. Contact Infineon for assistance in designing the compensation network.
25	VBUS_C	–0.3	24	Type-C connector VBUS voltage. Connect to the type-C connector's VBUS pin.
26	CSPO	–0.3	24	Positive input of output current sensing amplifier. Connect to positive terminal of the output current sense resistor.
27	CSNO	–0.3	24	Negative input of output current sensing amplifier. Connect to negative terminal of the output current sense resistor.

Notes
7. Maximum voltage must not exceed 6 V.
8. Maximum absolute voltage wrt GND must not exceed 40 V.

Table 4 CYPD7194, CYPD7195, CYPD7196, CYPD7197: 40-LGA package pinout *(continued)*

Pin no.	Pin name	Absolute minimum (V)	Absolute maximum (V)	Description
28	CC1	–0.5	24	Type-C connector configuration channel 1. Connect directly to the CC1 pin on the port's type-C connector. Additionally, connect a 390 pF capacitor to ground.
29	CC2	–0.5	24	Type-C connector configuration channel 2. Connect directly to the CC2 pin on the port's type-C connector. Additionally, connect a 390 pF capacitor to ground.
30	DP_GPIO0	–0.5	PVDD + 0.5[7]	P0.0: USB D+/GPIO: D+ for implementing BC 1.2, AFC, QC or Apple charging. EZ-PD™ CCG7SA4F does not support USB data transmission on this pin.
31	DM_GPIO1	–0.5	PVDD + 0.5[7]	P0.1: USB D+/GPIO: D– for implementing BC 1.2, AFC, QC or Apple charging. EZ-PD™ CCG7SA4F does not support USB data transmission on this pin.
32	VDDD	–	6	5 V LDO output. Connect a 1 µF ceramic bypass capacitor to this pin.
33	CSP_GPIO2	–0.5	PVDD + 0.5[7]	P0.2: GPIO/ positive input terminal of VBAT – GND protection circuit. Connect to the positive terminal of the VBAT – GND short protection current sense resistor.
34	CSN_GPIO3	–0.5	PVDD + 0.5[7]	P0.3: GPIO/negative input terminal of VBAT – GND protection circuit/hot plug detect. Connect to the negative terminal of the VBAT – GND short protection current sense resistor. For single-ended current sensing, this pin need not be connected to the current sense resistor. For applications supporting DisplayPort (for example, Rear seat entertainment (RSE)), this is the Hotplug Detect output pin.
35	GPIO4	–0.5	PVDD + 0.5[7]	P0.5: GPIO
36	CGND	–0.3	0.5	CC block ground.
37	GPIO5	–0.5	PVDD + 0.5[7]	P1.4: GPIO
38	GPIO6	–0.5	PVDD + 0.5[7]	P1.3: GPIO
39	GPIO7	–0.5	PVDD + 0.5[7]	P1.2: GPIO
40	GPIO8	–0.5	PVDD + 0.5[7]	P1.1: GPIO
EPAD P5	GND	–	–	GND

Notes
7. Maximum voltage must not exceed 6 V.
8. Maximum absolute voltage wrt GND must not exceed 40 V.

Table 5 GPIO ports, pins and their functionality

GPIO #	SCB function			TCPWM		
	UART	SPI	I2C	ACT#0	ACT#1	ACT#3
DP_GPIO0	–	–	–	–	–	–
DM_GPIO1	–	–	–	–	–	–
CSP_GPIO2	–	–	–	tcpwm0_line	tcpwm.tr_compare_match[0]:0	tcpwm.tr_in[0]
CSN_GPIO3	–	–	–	tcpwm.line[1]:0	tcpwm.tr_compare_match[1]:0	tcpwm.tr_in[1]
GPIO4	–	–	–	tcpwm.line[2]:0	tcpwm.tr_compare_match[2]:0	tcpwm.tr_in[2]
GPIO5	scb[1].uart_rts:0	scb[1].spi_select0:0	–	tcpwm.line[7]:0	tcpwm.tr_compare_match[7]:0	tcpwm.tr_in[7]
GPIO6	scb[1].uart_rx:0	scb[1].spi_clk:0	scb[1].i2c_scl:0	tcpwm.line[6]:0	tcpwm.tr_compare_match[6]:0	–
GPIO7	scb[1].uart_tx:0	scb[1].spi_miso:0	scb[1].i2c_sda:0	tcpwm.line[5]:0	tcpwm.tr_compare_match[5]:0	–
GPIO8	scb[0].uart_rts:0	scb[0].spi_select0:0	scb[2].i2c_scl:0	tcpwm.line[4]:0	tcpwm.tr_compare_match[4]:0	–
GPIO9	scb[0].uart_cts:0	scb[0].spi_mosi:0	scb[2].i2c_sda:0	tcpwm.line[3]:0	tcpwm.tr_compare_match[3]:0	–
GPIO10	scb[1].uart_cts:0	scb[0].spi_miso:0	–	–	–	tcpwm.tr_in[6]
GPIO11	scb[0].uart_tx:0	scb[1].spi_mosi:0	scb[0].i2c_sda:0	–	–	–
GPIO12	scb[0].uart_rx:0	scb[0].spi_clk:0	scb[0].i2c_scl:0	srss.ext_clk:0	–	–

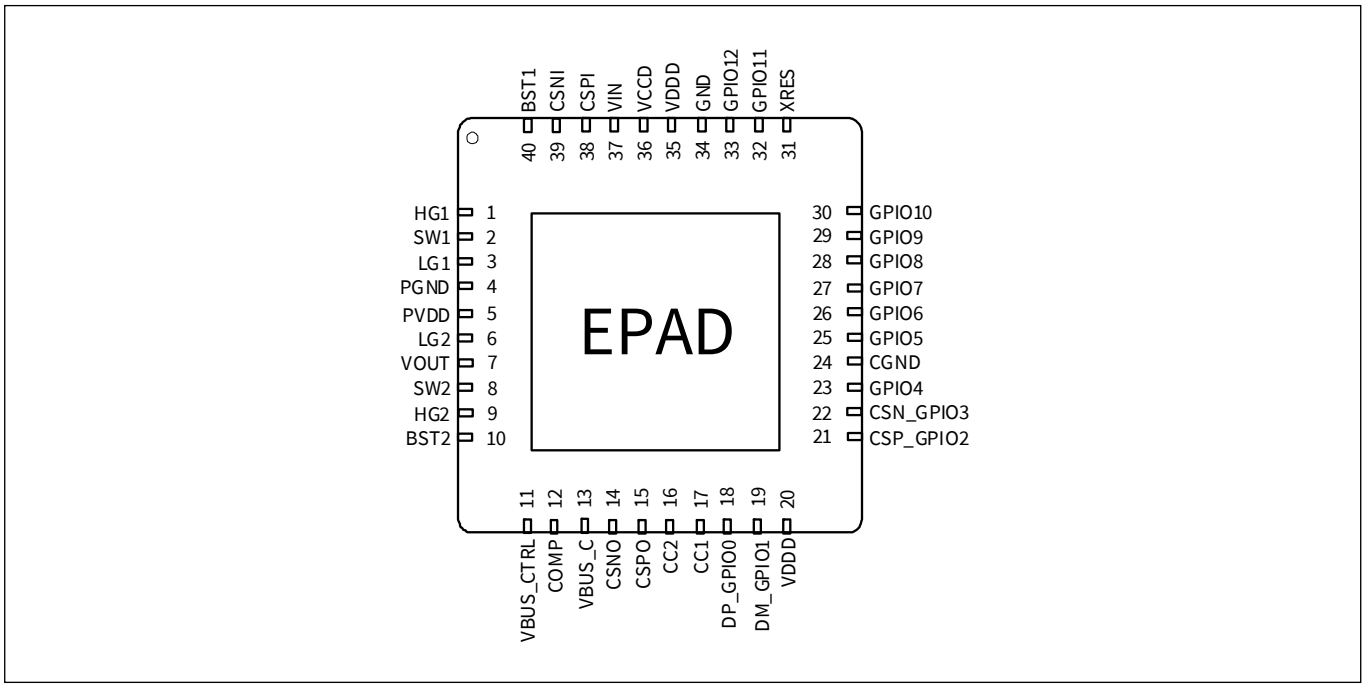


Figure 10 **EZ-PD™ CYPD719X without integrated switching FETs (CYPD7191, CYPD7199) 40-QFN pinout**

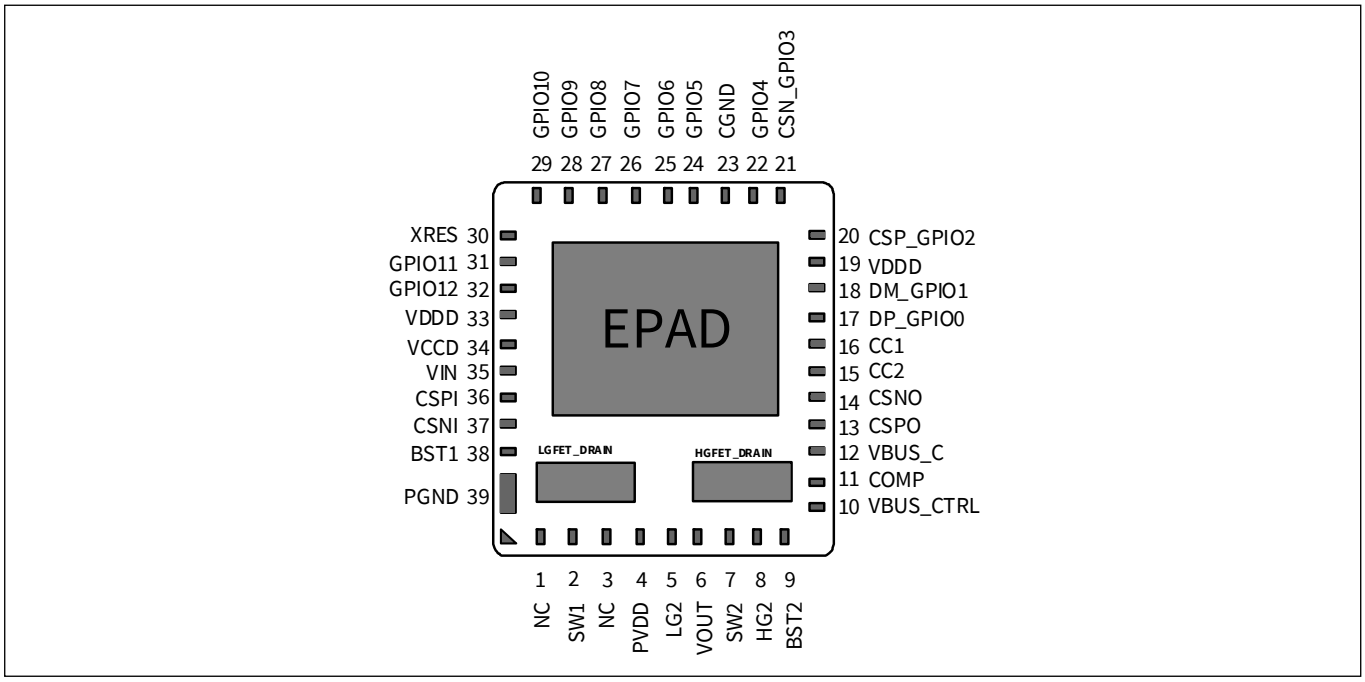


Figure 11 **EZ-PD™ CYPD719X with two buck switching FETs integrated (CYPD7192, CYPD7193, CYPD7198) 39-LGA package pinout**

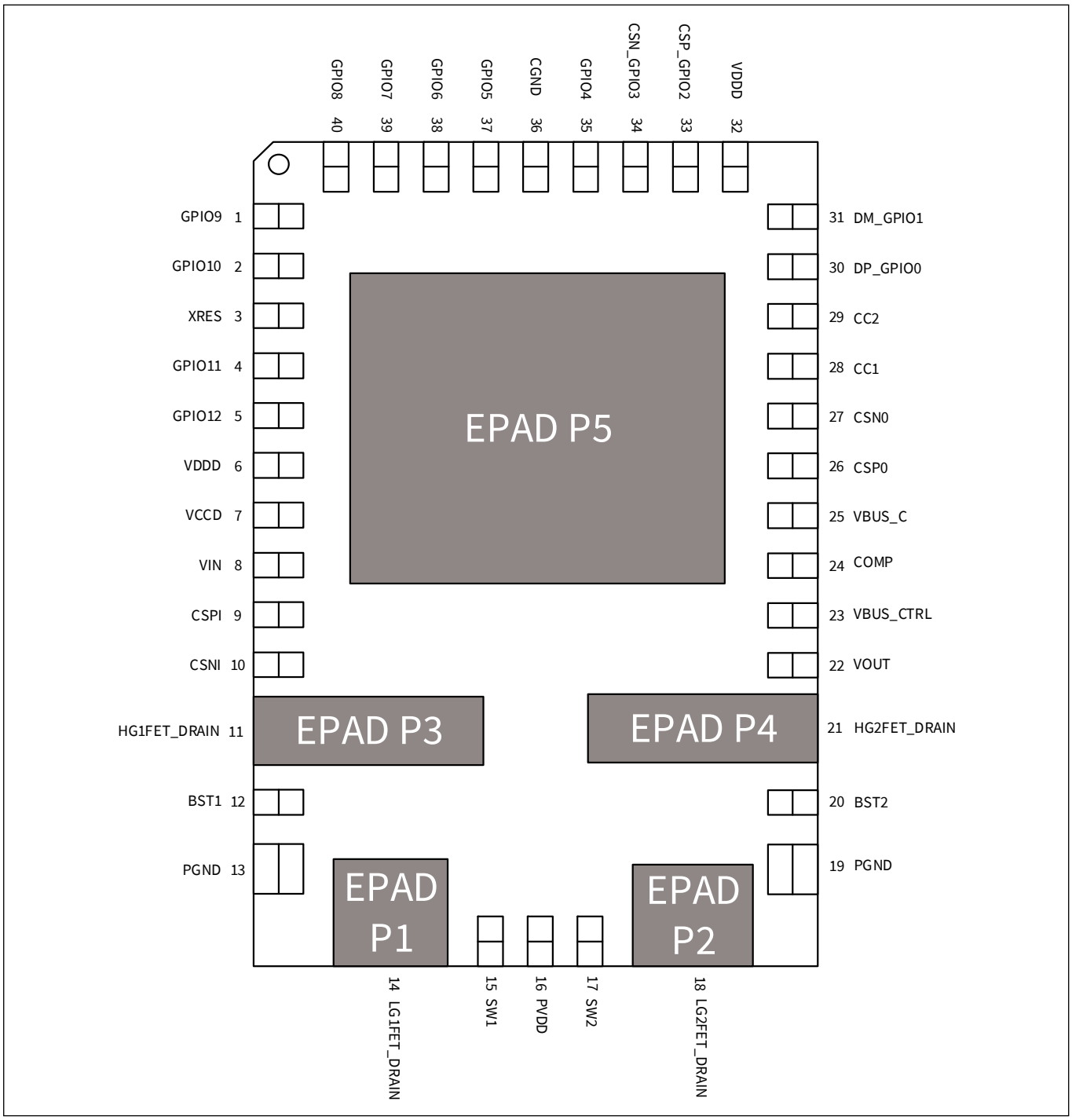


Figure 12 **EZ-PD™ CYPD719X with four switching FETs integrated (CYPD7194, CYPD7195, CYPD7196, CYPD7197) 40-LGA package pinout**

4 EZ-PD™ CYPD719X programming and bootloading

There are two ways to program application firmware into a EZ-PD™ CYPD719X device:

1. Programming the device flash over SWD Interface
2. Application firmware update over specific interfaces (CC, I2C, LIN)

Generally, the EZ-PD™ CYPD719X devices are programmed over SWD interface only during development or during the manufacturing process of the end-product. Once the end-product is manufactured, the EZ-PD™ CYPD719X device's application firmware can be updated via the appropriate bootloader interface. By default, the EZ-PD™ CYPD719X devices ship with a combined I2C/CC bootloader. Infineon strongly recommends customers to use the **EZ-PD™ configuration utility** to turn off the application FW update over CC or I2C interface in the firmware that is updated into EZ-PD™ CYPD719X's flash before mass production. This prevents unauthorized firmware from being updated over CC interface in the field. If you desire to retain the application firmware update over CC/ I2C interfaces feature post-production for on-field firmware updates, contact **Infineon Sales** for further guidelines.

4.1 Programming the device flash over SWD interface

The EZ-PD™ CYPD719X family of devices can be programmed using the SWD interface. Infineon provides programming hardware called **CY8CKIT-005 MiniProg4 kit**, which can be used to program the flash as well as debug firmware. The flash is programmed by downloading the information from a hex file.

As shown in the block diagram (see **Figure 13**), the SWD_DAT and SWD_CLK pins are connected to the host programmer's SWDIO (data) and SWDCLK (clock) pins respectively. During SWD programming, the device can be powered by the host programmer by connecting its VTARG (power supply to the target device) to VDDD pins of EZ-PD™ CYPD719X device. If the EZ-PD™ CYPD719X device is powered using an on-board power supply, it can be programmed using the "reset programming" option. For more details, see the **CCGx (CYPDxxxx) programming specifications**.

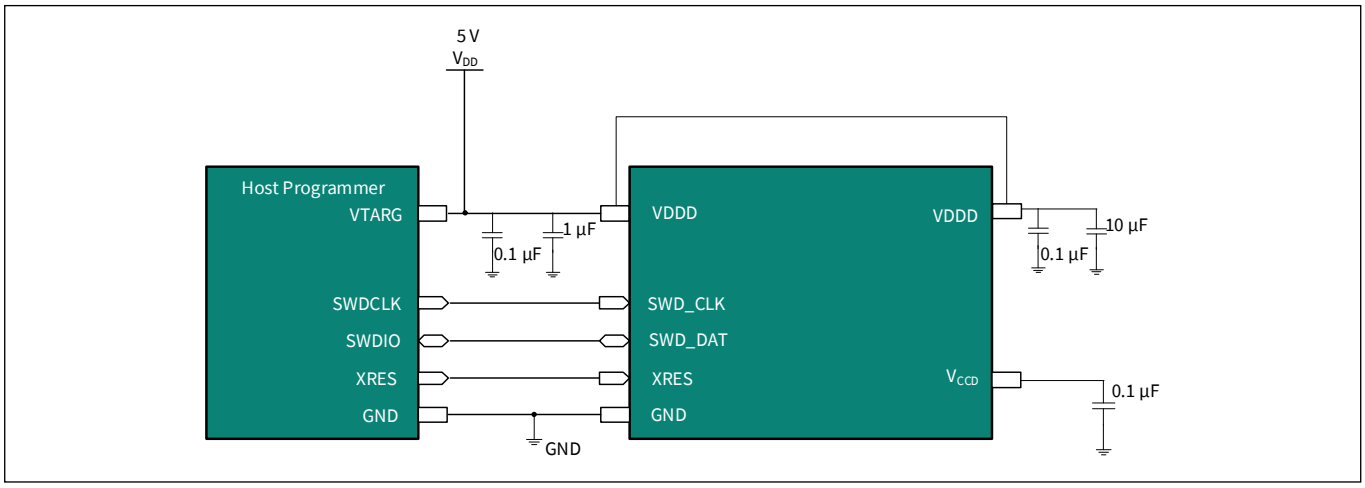


Figure 13 Connecting the programmer to CYPD719X device

4.2 Application firmware update using bootloader

There are two bootloader options available in EZ-PD™ CYPD719X:

- **CC and I2C bootloader:** This bootloader has the GPIO 4, Pin 35 set to strong drive low to drive the FET for VBAT to GND short-circuit protection. VBUS_CTRL pin in the bootloader is configured to control the Provider FET. The bootloader will work for designs with and without provider FET
- **LIN bootloader:** The LIN-based bootloader supports firmware and configuration updates over LIN interface using HPI. By default, this bootloader is not available in the parts that are shipped from the factory. EZ-PD™ CYPD719X silicon from the factory will ship with the CC and I2C bootloader programmed at the factory

4.2.1 Application firmware update over CC interface

For bootloading EZ-PD™ CYPD719X applications over the CC interface, the **CY4532 EVK** or **CCPROG PAT: USB-C Power Adapter Programmer and Tester** is used to send programming and configuration data as Infineon-specific vendor-defined messages (VDMs) over the CC line. The CY4532 EVK's power board or PAT tester is connected to the system containing EZ-PD™ CYPD719X device on one end and a Windows PC running the EZ-PD™ Configuration Utility as shown in **Figure 14** on the other end to bootload the EZ-PD™ CYPD719X device.

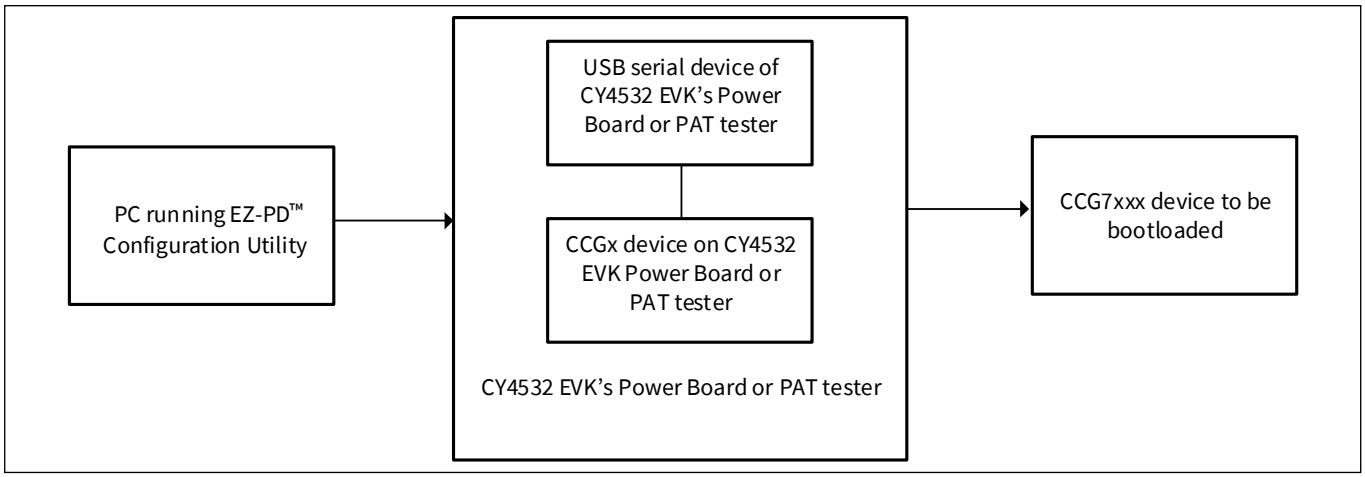


Figure 14 Application firmware update over CC interface

The application firmware (FW) update feature over CC interface is intended for use during development and manufacturing. Infineon strongly recommends customers to use the **EZ-PD™ Configuration Utility** to turn off the application FW update over CC interface in the firmware that is updated into EZ-PD™ CYPD719X's flash before mass production. This prevents unauthorized firmware from being updated over CC-interface in the field. See the knowledge base article **KBA230192** on how to configure this in EZ-PD™ Configuration Utility. If you desire to retain the application firmware update over CC interface feature post-production for on-field firmware updates, contact **Infineon support** for further guidelines on how to use authenticated CC bootloader.

4.2.2 Application firmware update over I2C interface

The default bootloader supports both CC and I2C interface. For boot loading EZ-PD™ CYPD719X applications over the I2C interface, any host processor can implement the legacy boot commands. Contact **Infineon support** for more details regarding the host processor implementation.

The connections between the host processor and EZ-PD™ CYPD719X for the bootloading via I2C interface is shown in **Figure 15**. If the user desires to retain the application firmware update over I2C interface feature post-production for on-field firmware updates, contact **Infineon support** for further guidelines on how to use authenticated LIN bootloader.

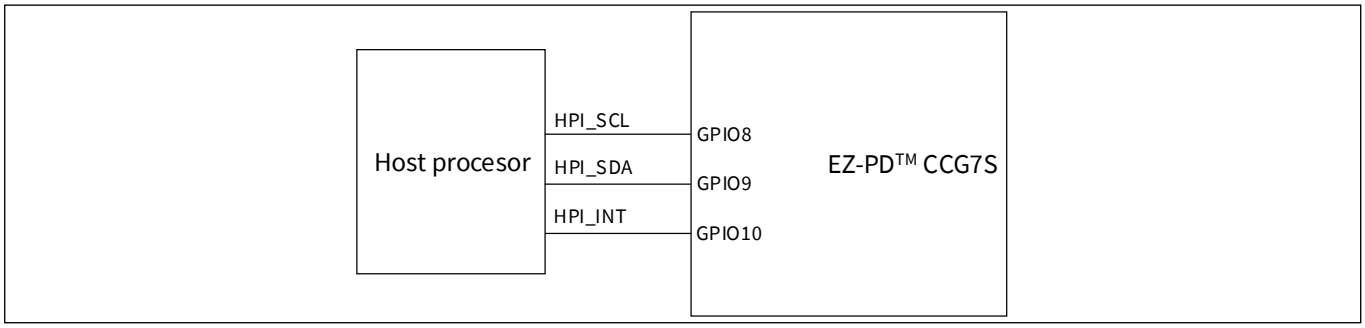


Figure 15 GPIO mapping for the application firmware update over I2C interface

4.2.3 Application firmware update over LIN interface

The LIN-based bootloader supports firmware and configuration updates over LIN interface using HPI. The command sequence is same for all the bootloader interfaces irrespective of the underlying communication protocol (CC/I2C/LIN).

The LIN bootloader will support standard diagnostic commands over UDS protocol thereby enabling easy integration with automotive LIN Network and helping in reduced design cycle time for customers. The default baud rate in the LIN bootloader is 19200.

The connections between the LIN transceiver and EZ-PD™ CYPD719X for the bootloading via LIN interface is shown in **Figure 16**. If the user desires to retain the application firmware update over LIN interface feature post-production for on-field firmware updates, contact **Infineon support** for further guidelines on how to use authenticated I2C bootloader.

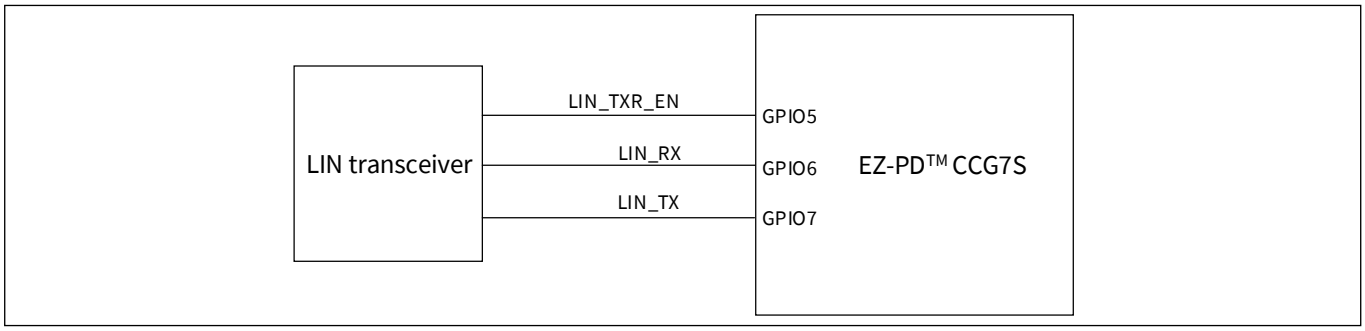


Figure 16 GPIO mapping for the application firmware update over LIN interface

5 Applications

Figure 17 shows a typical single-port head unit charger application block diagram using the EZ-PD™ CYPD719X device. A head unit charger (also known as center stack) is located prominently in the center of the dashboard or console. They are powered by the car battery and are used for charging the mobile/tablet and for media transfer using USB data communications. In this application, EZ-PD™ CYPD719X is always in DFP role supporting the charging of the device. It negotiates the power with the connected device and uses the integrated buck-boost controller to supply the required voltage and current.

The DP/DM lines of the type-C receptacles are connected to the host processor/hub, for data connectivity to the head unit. These pins are also connected to EZ-PD™ CYPD719X to support legacy charging protocol BC v1.2 CDP. The I2C interface is used to interface with the host processor/hub, to support host processor interface (HPI) commands, provide status to the head unit, and support FW updates. Note that per the battery charging specification 1.2, other legacy charging protocols other than BC v1.2 CDP cannot be supported in conjunction with USB data communication.

EZ-PD™ CYPD719X measures various temperatures using external NTC thermistors. EZ-PD™ CYPD719X throttles the output power based on temperature and/or shuts off the power under critical conditions. It also monitors the battery voltage and lowers the output power if the battery voltage is lower than the user-configured threshold. When no load is connected to the USB-C port, EZ-PD™ CYPD719X remains in standby mode without switching on the buck-boost controller.

For more details on the CYPD7191-40LDXS ordering information, see **Table 49**.

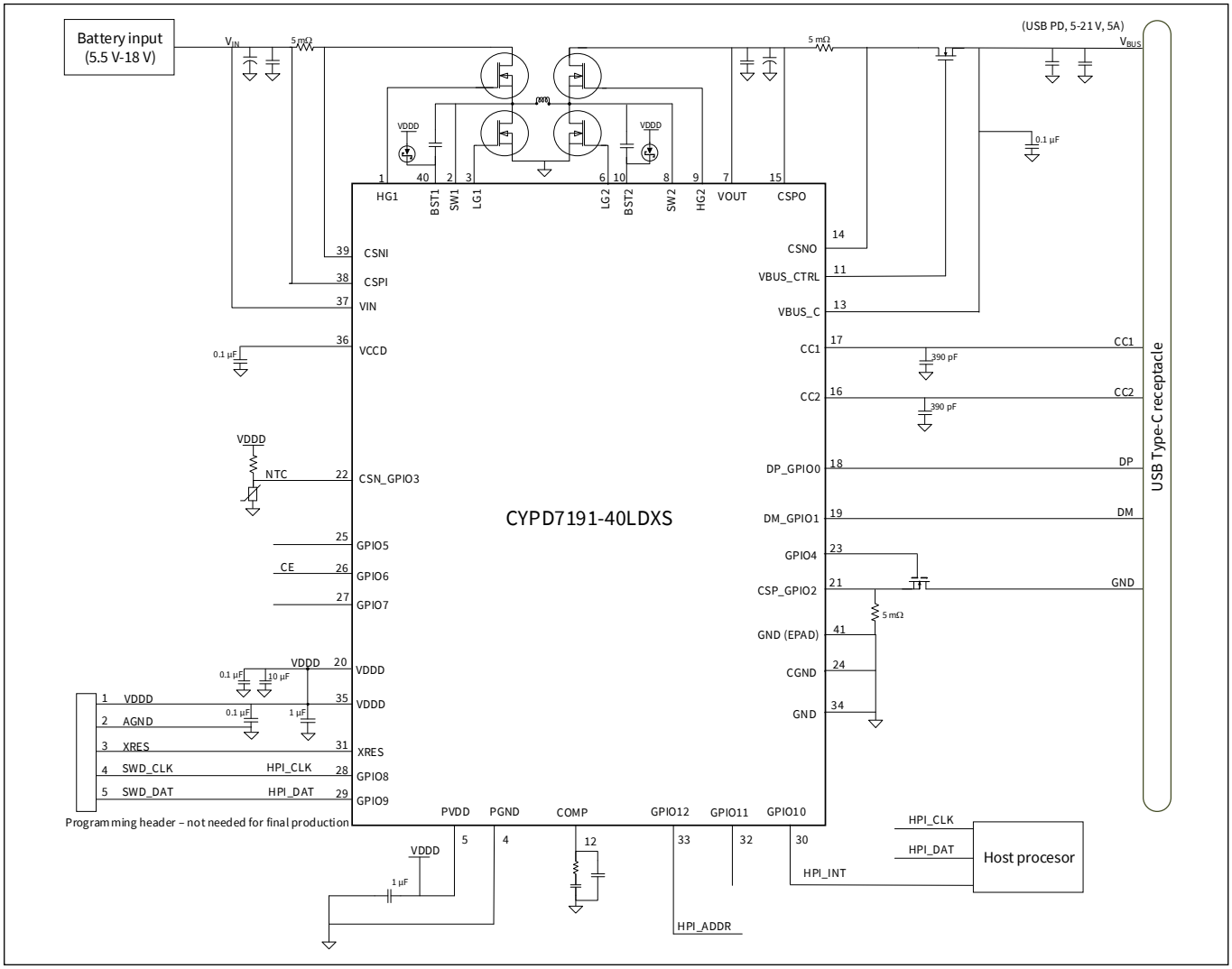


Figure 17 **Head unit (HU) charger application diagram using EZ-PD™ CYPD719X with all four external FETs**

Table 6 provides the head unit GPIO pin mapping for the application diagram in **Figure 17**.

Table 6 Head unit (HU) GPIO pin mapping

Pin name	Function	GPIO	HU
DP_GPIO0	USB DP of type-C port. Supports BC 1.2, QC, Apple charging and AFC	P0.0	DP
DM_GPIO1	USB DM of type-C port. Supports BC 1.2, QC, Apple charging and AFC	P0.1	DM
CSP_GPIO2	CSP pin on ground side to implement VBAT to GND short circuit protection	P0.2	VBATT_CSP
CSN_GPIO3	Thermistor	P0.3	NTC
GPIO4	GPIO to control the FET for VBAT to GND short circuit protection	P0.5	VBATT_FET
GPIO5	Free GPIO	P1.4	GPIO
GPIO6	Chip enable from external hardware	P1.3	CE
GPIO7	Free GPIO	P1.2	GPIO
GPIO8	Connect to the host programmer's SWDCLK (clock) for programming the EZ-PD™ CYPD719X device. This pin is also connected to the HPI CLK pin of the external host processor.	P1.1	HPI_SCL
GPIO9	Connect to the host programmer's SWDIO (data) for programming the EZ-PD™ CYPD719X device. This pin is also connected to the HPI DATA pin of the external host processor.	P1.0	HPI_SDA
GPIO10	HPI interrupt	P2.2	HPI_INT
GPIO11	Free GPIO	P3.0	GPIO
GPIO12	HPI address detection pin	P3.1	HPI_ADDR

Figure 18 shows a dual-port head unit charger application block diagram using two EZ-PD™ CCG7S with four switching FETs integrated. The dual-port head unit designs that support power sharing and require firmware to be updated over I2C should use the part number CYPD7195-40BFXS with all four FETs integrated or CYPD7193-39BFXS with two buck switching FETs integrated.

For more details on the CYPD7195-40BFXS ordering information, see **Table 49**.

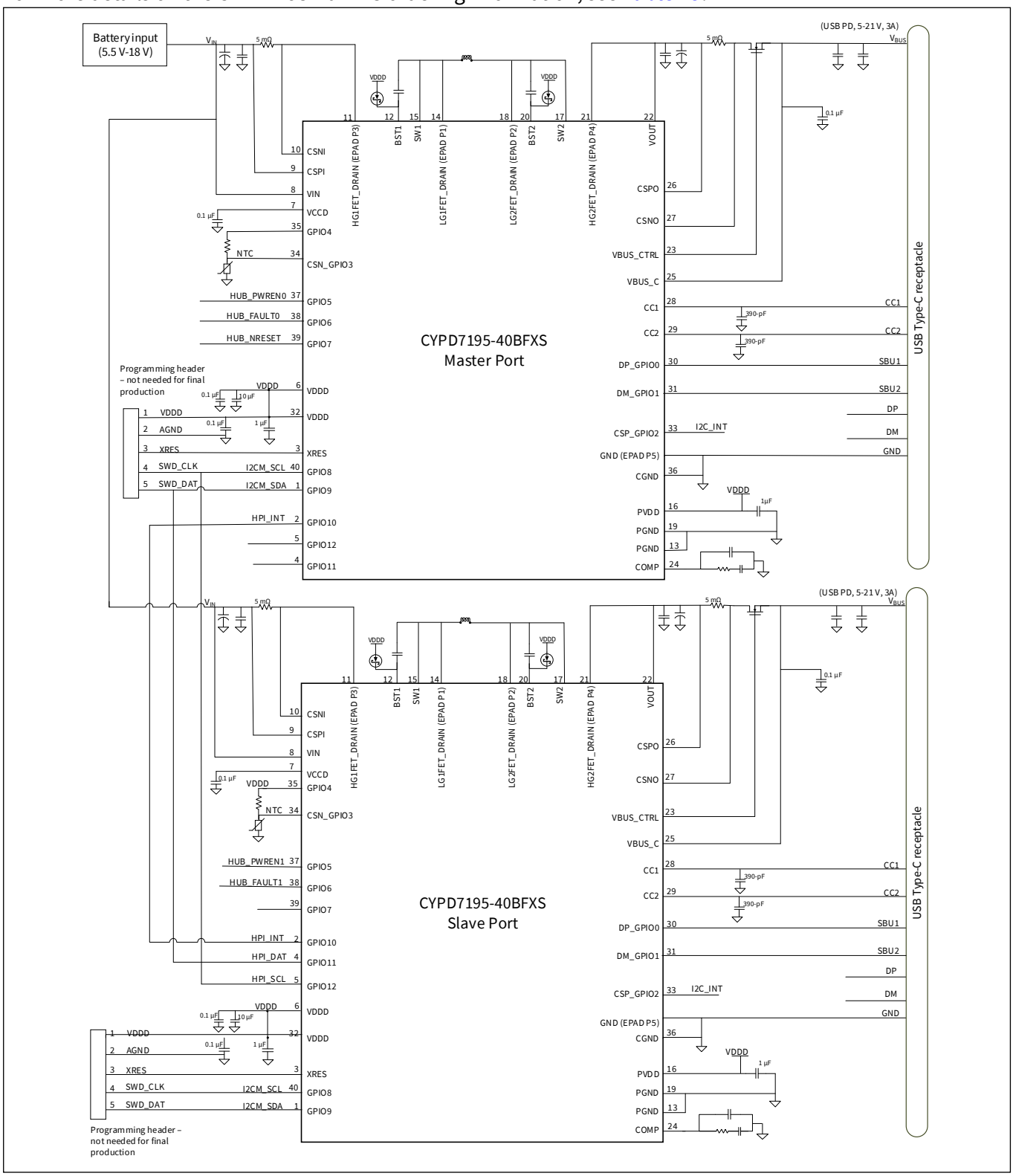


Figure 18 **Dual-port head unit (HU) charger application diagram using EZ-PD™ CYPD719X with four switching FETs integrated**

Table 7 Dual-port head unit GPIO pin mapping - Master port (port 0)

Pin name	Function	GPIO	
DP_GPIO0	This GPIO is connected to the SBU1 pin of type-C Connector to implement moisture detection.	P0.0	SBU1
DM_GPIO1	This GPIO is connected to the SBU2 pin of type-C Connector to implement moisture detection.	P0.1	SBU2
CSP_GPIO2	I2C_INT connected to the Hub	P0.2	I2C_INT
CSN_GPIO3	Thermistor	P0.3	NTC
GPIO4	This GPIO is used to bias the Thermistor	P0.5	NTC_Bias
GPIO5	Power Enable output connected to the port 0 of the Hub. This is used for enabling/ disabling the Port 0	P1.4	HUB_PWREN0
GPIO6	This is port 0's OCP fault indication pin connected to the Hub	P1.3	HUB_FAULT0
GPIO7	This GPIO is connected to the Reset pin of the Hub	P1.2	HUB_NRESET
GPIO8	Master port's I2C Data for implementing load sharing between two EZ-PD™ CCG7S devices. Connect to the host programmer's SWDCLK (clock) for programming the EZ-PD™ CCG7S.	P1.1	SWD_CLK/ I2CM_SCL
GPIO9	Master port's I2C Clock for implementing load sharing between two EZ-PD™ CCG7S devices. Connect to the host programmer's SWDIO (data) for programming the EZ-PD™ CCG7S.	P1.0	SWD_DAT/ I2CM_SDA
GPIO10	HPI Interrupt pin to implement load sharing	P2.2	HPI_INT
GPIO11	I2C Data connected to the Hub	P3.0	HPI_SDA
GPIO12	I2C Clock	P3.1	HPI_SCL

Table 8 Dual-port head unit GPIO pin mapping - Slave port (port 1)

Pin name	Function	GPIO	
DP_GPIO0	This GPIO is connected to the SBU1 pin of type-C Connector to implement moisture detection.	P0.0	SBU1
DM_GPIO1	This GPIO is connected to the SBU2 pin of type-C Connector to implement moisture detection.	P0.1	SBU2
CSP_GPIO2	I2C_INT connected to the Hub	P0.2	I2C_INT
CSN_GPIO3	Thermistor	P0.3	NTC
GPIO4	This GPIO is used to bias the Thermistor	P0.5	NTC_Bias
GPIO5	Power Enable output connected to the port 1 of the Hub. This is used for enabling/ disabling the Port 1	P1.4	HUB_PWREN1
GPIO6	This is port 1's OCP fault indication pin connected to the Hub	P1.3	HUB_FAULT1
GPIO7	Free GPIO	P1.2	GPIO
GPIO8	I2C Clock connected to the Hub Connect to the host programmer's SWDCLK (clock) for programming the EZ-PD™ CCG7S	P1.1	SWD_CLK/ I2CM_SCL
GPIO9	I2C Data connected to the Hub Connect to the host programmer's SWDIO (data) for programming the EZ-PD™ CCG7S	P1.0	SWD_DAT/ I2CM_SDA
GPIO10	HPI Interrupt pin to implement load sharing	P2.2	HPI_INT
GPIO11	Slave port's I2C Data for implementing load sharing between two EZ-PD™ CCG7S devices.	P3.0	HPI_SDA
GPIO12	Slave port's I2C Clock for implementing load sharing between two EZ-PD™ CCG7SA4F devices.	P3.1	HPI_SCL

Figure 19 shows a typical rear seat charger (RSC) application block diagram using EZ-PD™ CYPD719X device with four external switching FETs. **Figure 20** shows a typical rear seat charger (RSC) application block diagram using EZ-PD™ CYPD719X device with all four switching FETs integrated. This application is similar to the head unit charger application without the hub and data communications. There is no host processor/hub in this application. This application can be configured to support the legacy charging protocols - BC1.2 DCP, Qualcomm QC2.0/3.0, Apple charging, and Samsung AFC.

See **Figure 22** for an example of an RSC application in which only step-down (buck) conversion is required. EZ-PD™ CCG7SF with two integrated FETs can be used for this application.

For more details on the CYPD7191-40LDXS ordering information, see **Table 49**.

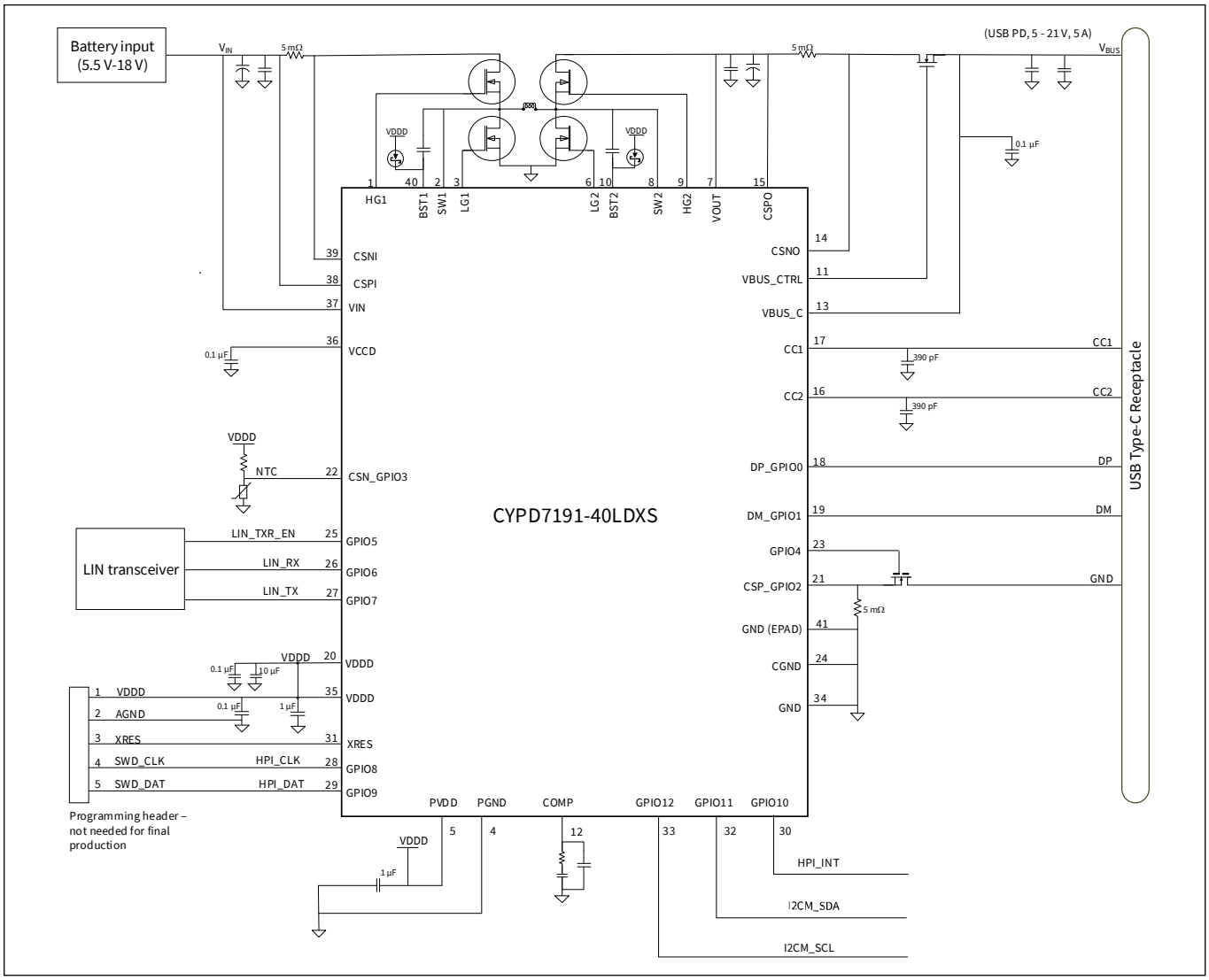


Figure 19 **Rear seat charger (RSC) application diagram using EZ-PD™ CYPD719X with all four external FETs**

For more details on the CYPD7194-40LFXS ordering information, see **Table 49**.

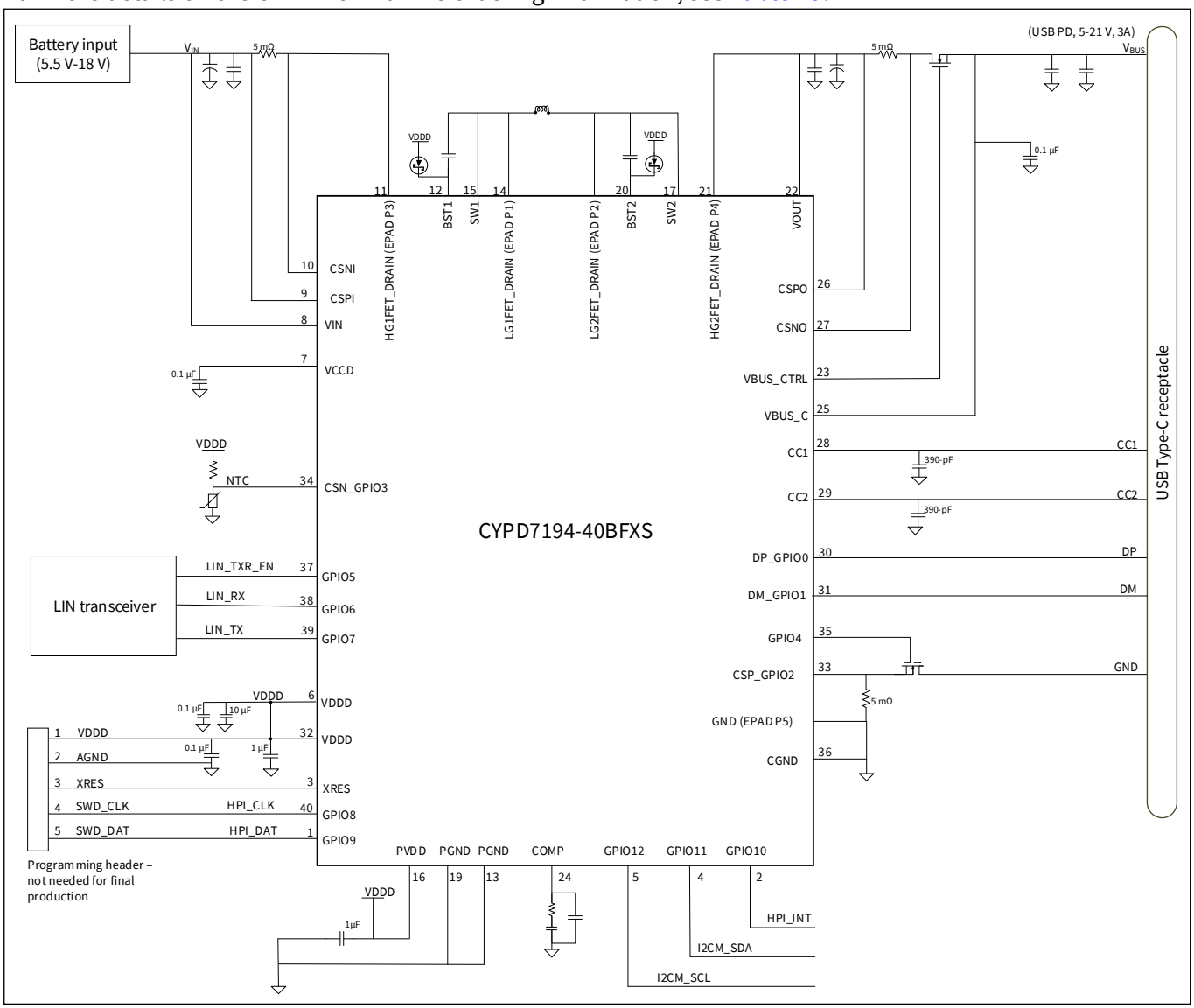


Figure 20 **Rear seat charger (RSC) application diagram using EZ-PD™ CYPD719X with all four switching FETs integrated**

Table 9 provides the RSC GPIO pin mapping for the application diagram in **Figure 19** and **Figure 20**.

Table 9 Rear seat charger (RSC) GPIO pin mapping

Pin name	Function	GPIO	HU
DP_GPIO0	USB DP of type-C port. Supports BC 1.2, QC, Apple charging and AFC	P0.0	DP
DM_GPIO1	USB DM of type-C port. Supports BC 1.2, QC, Apple charging and AFC	P0.1	DM
CSP_GPIO2	CSP pin on ground side to implement VBAT to GND short-circuit protection	P0.2	VBATT_CSP
CSN_GPIO3	Thermistor	P0.3	NTC
GPIO4	GPIO to control the FET for VBAT to GND short-circuit protection	P0.5	VBATT_FET
GPIO5	LIN trans receiver enable	P1.4	LIN_TXR_EN
GPIO6	LIN RX pin	P1.3	LIN_RX
GPIO7	LIN TX pin	P1.2	LIN_TX
GPIO8	Connect to the host programmer's SWDCLK (clock) for programming the EZ-PD™ CCG7 device. This is also the HPI slave SCL pin for implementing load sharing between two EZ-PD™ CCG7SA4F devices.	P1.1	HPI_SCL
GPIO9	Connect to the host programmer's SWDDAT (data) for programming the EZ-PD™ CCG7SA4F device. This is also the HPI slave SDA pin for implementing load sharing between two EZ-PD™ CCG7SA4F devices.	P1.0	HPI_SDA
GPIO10	HPI interrupt	P2.2	HPI_INT
GPIO11	Master I2C SDA for implementing load sharing between two EZ-PD™ CCG7SA4F devices	P3.0	I2CM_SDA
GPIO12	Master I2C SCL for implementing load sharing between two EZ-PD™ CCG7SA4F devices	P3.1	I2CM_SCL

Figure 21 shows the connections required for implementing load sharing between the two EZ-PD™ CYPD719X devices for the RSC application.

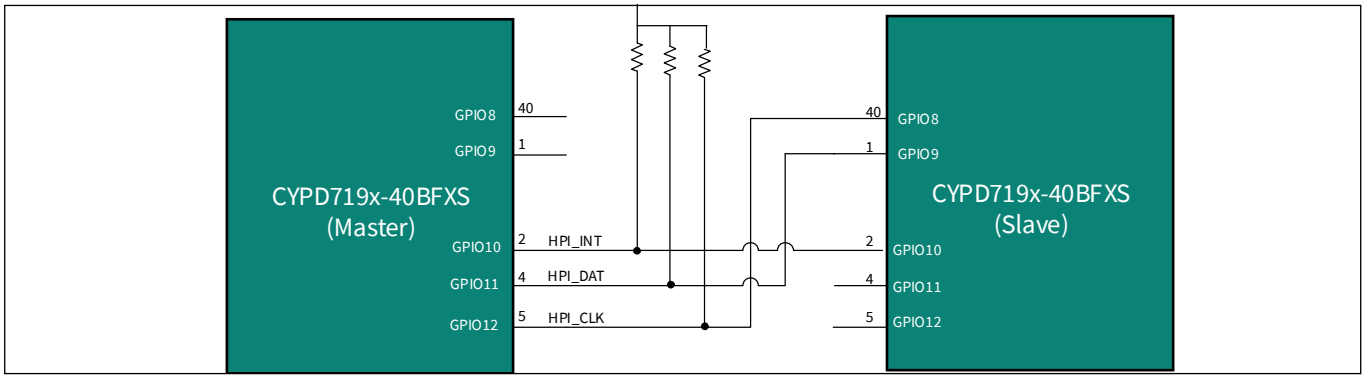


Figure 21 Load sharing between two EZ-PD™ CYPD719X devices

For more details on the CYPD7196-40BFXS ordering information, see **Table 49**.

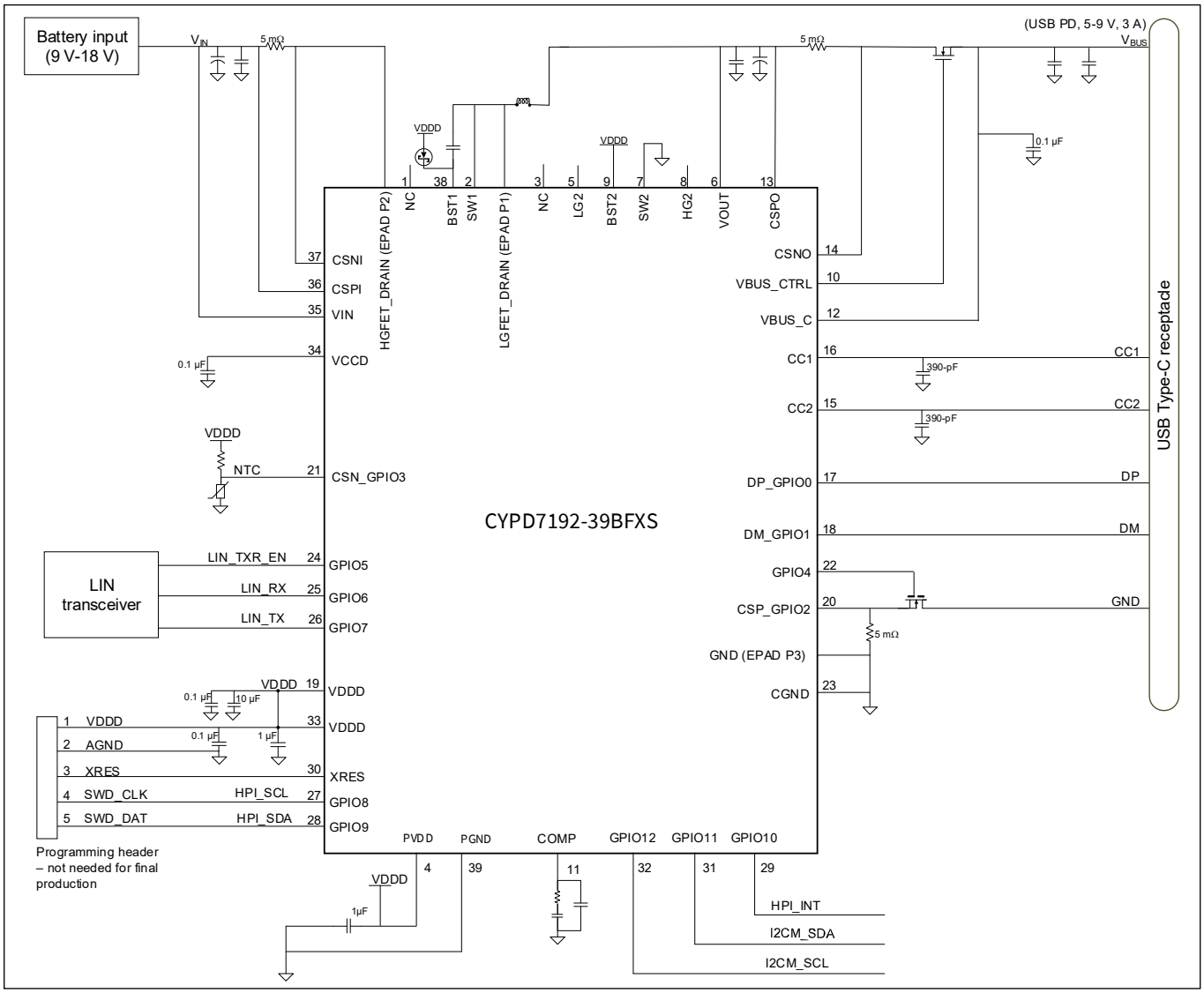


Figure 22 **Rear seat charger (RSC) buck only application diagram using EZ-PD™ CYPD719X with two buck FETs integrated**

Figure 23 shows the rear seat entertainment (RSE) DP Sink application block diagram using EZ-PD™ CYPD719X with four external switching FETs. **Figure 24** shows a typical rear seat entertainment (RSE) DP sink application block diagram using EZ-PD™ CYPD719X device with all four switching FETs integrated. In this application, the port is used for charging and streaming video content from a DisplayPort source (for example, a mobile phone, PC, or a tablet) to a monitor. **Figure 25** shows the rear seat entertainment (RSE) DP Source application block diagram using EZ-PD™ CYPD719X with four external switching FETs. **Figure 24** shows a typical rear seat entertainment (RSE) DP source application block diagram using EZ-PD™ CYPD719X device with all four switching FETs integrated. EZ-PD™ CYPD719X supports DisplayPort alternate mode and controls the external DisplayPort Multiplexer through I2C.

DP Alt Mode is a key functionality that empowers USB-C connectors to efficiently transmit and convey DisplayPort video signals. This feature plays a critical role in rear-seat entertainment applications, enabling the extension or mirroring of screens across diverse devices through a USB-C port that supports DP Alt Mode. Additionally, DP Alt Mode seamlessly operates alongside other USB functions, allowing for concurrent data transfer, device charging, and video output, delivering enhanced utility and flexibility. EZ-PD™ CYPD719X also communicates with the system's SoC over I2C.

For more details on the CYPD7199-40LDXS ordering information, see **Table 49**.

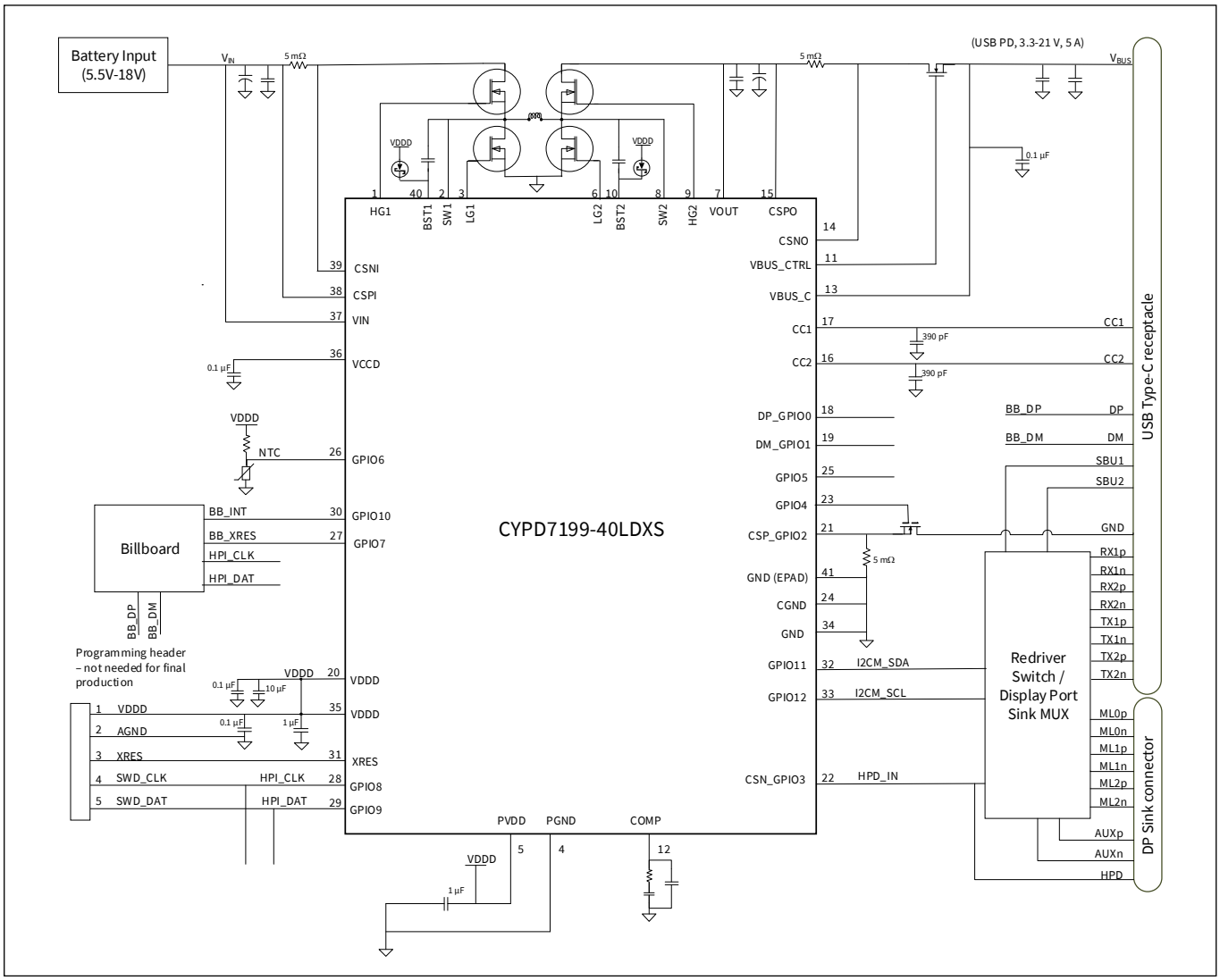


Figure 23 **Rear seat entertainment (RSE) DP Sink application diagram using EZ-PD™ CYPD719X with all four external FETs**

For more details on the CYPD7196-40BFXS ordering information, see **Table 49**.

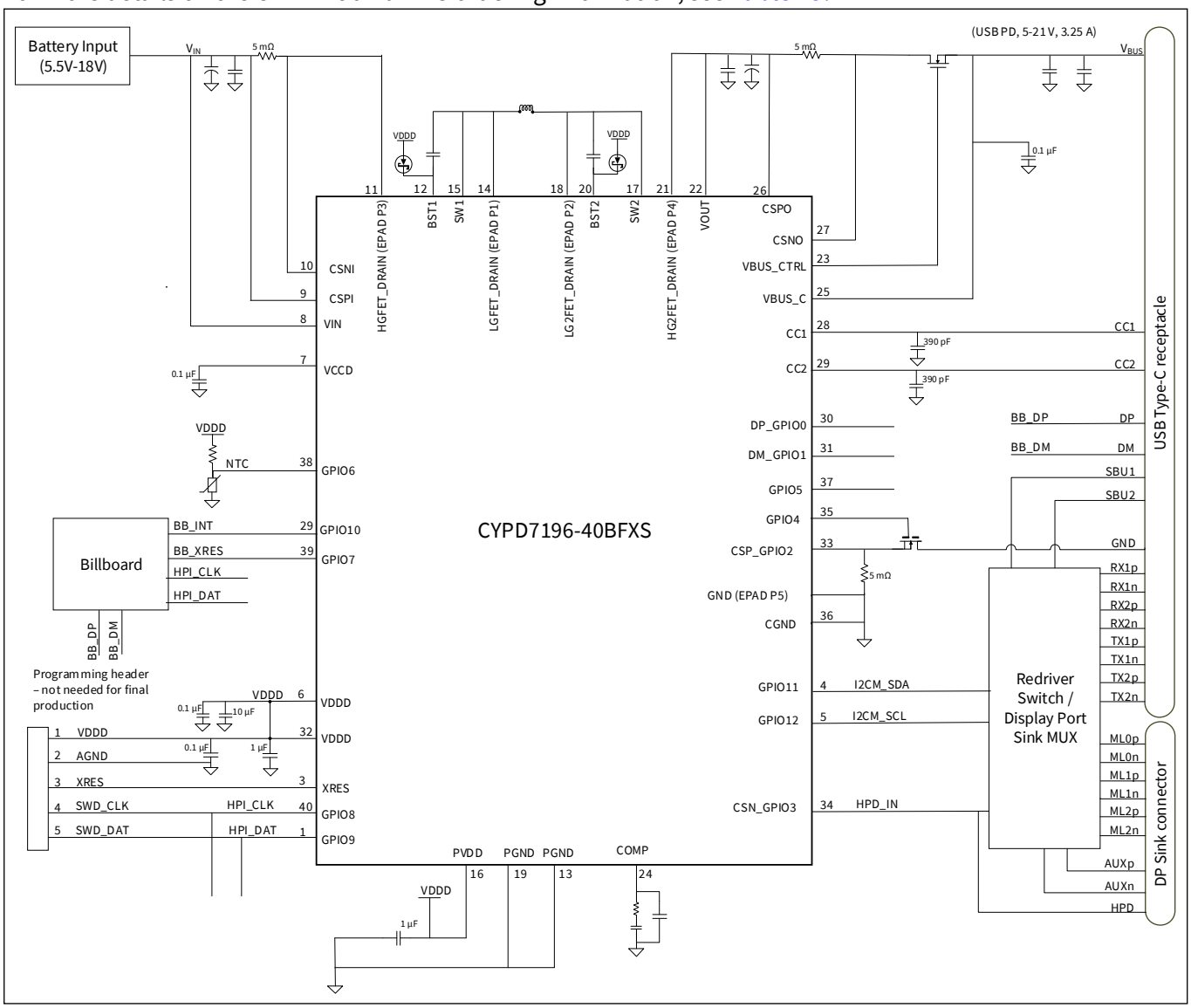


Figure 24 **Rear seat entertainment (RSE) DP Sink application diagram using EZ-PD™ CYPD719X with all four switching FETs integrated**

Table 10 provides the RSE DP Sink GPIO pin mapping for the application diagrams in **Figure 23** and **Figure 24**.

Table 10 Rear seat entertainment (RSE) DP Sink GPIO pin mapping

Pin name	Function	GPIO	RSE
DP_GPIO0	Free GPIO	P0.0	GPIO
DM_GPIO1	Free GPIO	P0.1	GPIO
CSP_GPIO2	CSP pin on ground side to implement V_{BAT} to GND short circuit protection	P0.2	V_{BATT_CSP}
CSN_GPIO3	Hot Plug Detect	P0.3	HPD_IN
GPIO4	GPIO to disable the FET for V_{BAT} to GND short circuit protection	P0.5	V_{BATT_FET}
GPIO5	Free GPIO	P1.4	GPIO
GPIO6	Thermistor	P1.3	NTC
GPIO7	Billboard reset pin	P1.2	BB_XRES
GPIO8	Connect to the host programmer's SWDCLK (clock) for programming the EZ-PD™ CYPD719X	P1.1	SWD_CLK/ HPI_SCL
GPIO9	Connect to the host programmer's SWDIO (data) for programming the EZ-PD™ CYPD719X	P1.0	SWD_DAT/ HPI_SDA
GPIO10	Interrupt pin connecting to the Billboard	P2.2	BB_INT
GPIO11	Master I2C SDA to control the display port mux	P3.0	I2CM_SDA
GPIO12	Master I2C SCL to control the display port mux	P3.1	I2CM_SCL

For more details on the CYPD7199-40BDXS ordering information, see **Table 49**.

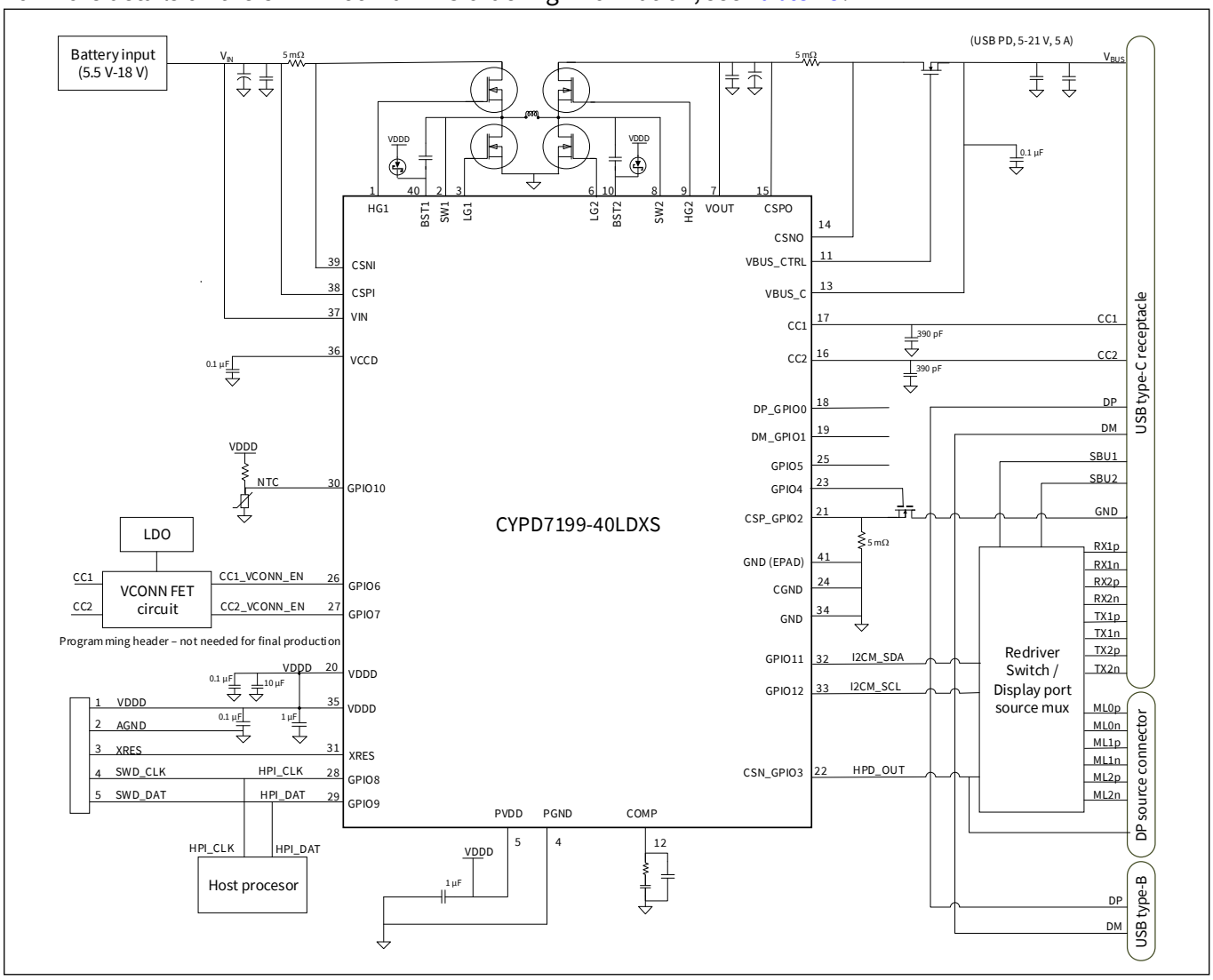


Figure 25 **Rear seat entertainment (RSE) DP Source application diagram using EZ-PD™ CYPD719X with all four external FETs**

For more details on the CYPD7196-40BFXS ordering information, see **Table 49**.

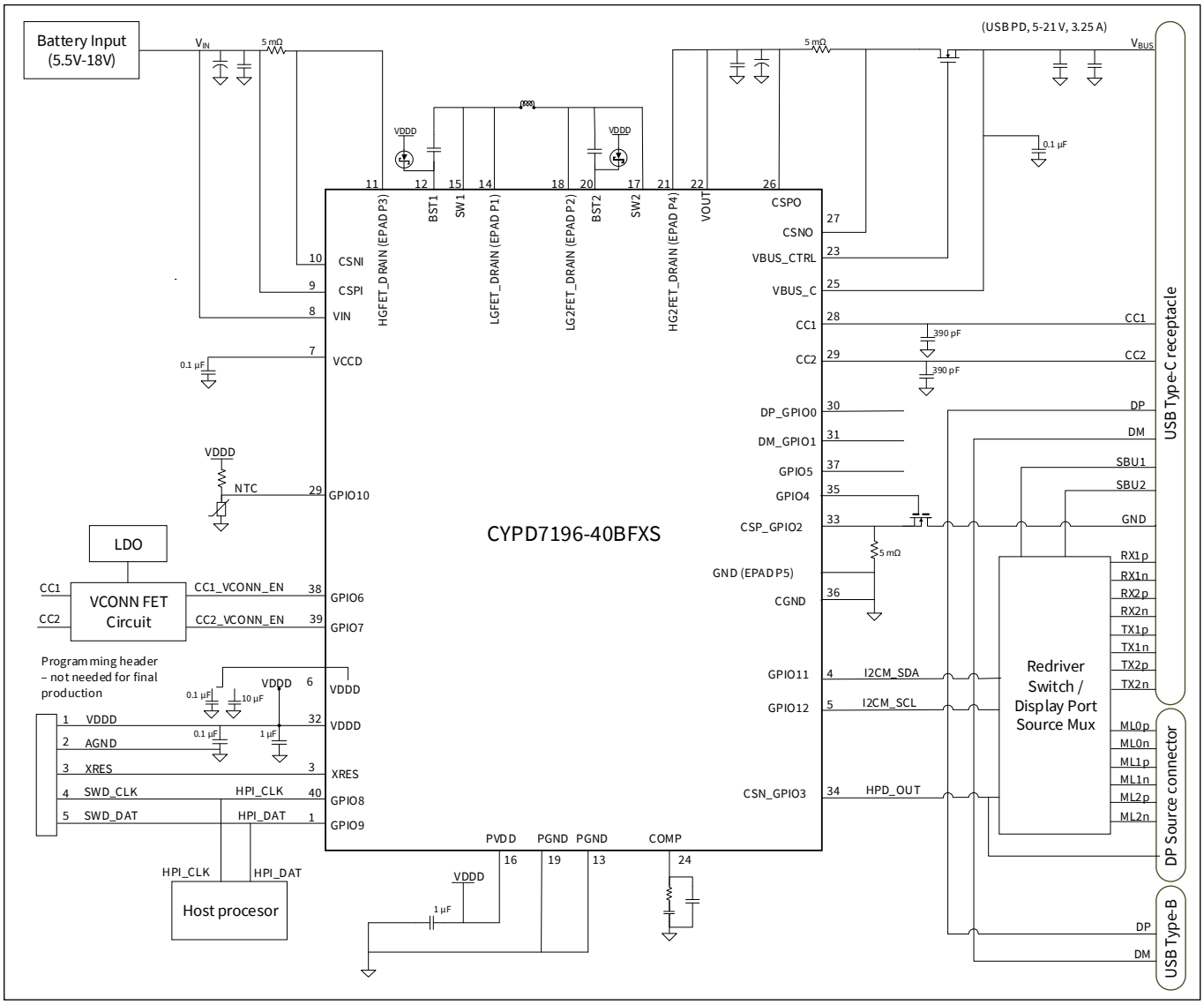


Figure 26 **Rear seat entertainment (RSE) DP source application diagram using EZ-PD™ CYPD719X with all four switching FETs integrated**

Table 11 provides the RSE DP Source GPIO pin mapping for the application diagram in Figure 26.

Table 11 Rear seat entertainment (RSE) DP Source GPIO pin mapping

Pin name	Function	GPIO	RSE
DP_GPIO0	Free GPIO	P0.0	GPIO
DM_GPIO1	Free GPIO	P0.1	GPIO
CSP_GPIO2	CSP pin on ground side to implement VBAT to GND short circuit protection	P0.2	VBATT_CSP
CSN_GPIO3	Hot Plug Detect	P0.3	HPD_OUT
GPIO4	GPIO to disable the FET for VBAT to GND short circuit protection	P0.5	VBATT_FET
GPIO5	Free GPIO	P1.4	GPIO
GPIO6	Enable CC1 VCONN	P1.3	CC1_VCONN_CTRL
GPIO7	Enable CC2 VCONN	P1.2	CC2_VCONN_CTRL
GPIO8	Connect to the host programmer's SWDCLK (clock) for programming the CYPD719X	P1.1	SWD_CLK/HPI_SCL
GPIO9	Connect to the host programmer's SWDIO (data) for programming the CYPD719X	P1.0	SWD_DAT/HPI_SDA
GPIO10	Thermistor	P2.2	NTC
GPIO11	Master I2C SDA to control the display port mux	P3.0	I2CM_SDA
GPIO12	Master I2C SCL to control the display port mux	P3.1	I2CM_SCL

6 Electrical specifications

6.1 Absolute maximum ratings

Table 12 Absolute maximum ratings[9]

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
V_{IN_MAX}	Maximum input supply voltage	–	–	40	V	–
V_{DDD_MAX}	Maximum supply voltage relative to V_{SS}	–	–	6		–
V_{5V_MAX}	Maximum supply voltage relative to V_{SS}	–	–	6		–
$V_{BUS_C_MAX}$	Max V_{BUS_C} (P0/P1) voltage relative to Vss	–	–	24		–
$V_{CC_PIN_ABS}$	Max voltage on CC1 and CC2 pins	–	–	24		–
V_{GPIO_ABS}	Inputs to GPIO	–0.5	–	V_{DDD} + 0.5		–
$V_{GPIO_OVT_ABS}$	OVT GPIO voltage	–0.5	–	6		–
I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	–
$I_{GPIO_INJECTION}$	GPIO injection current, max for $V_{IH} > V_{DDD}$, and min for $V_{IL} < V_{SS}$	–0.5	–	0.5		Absolute max, current injected per pin
ESD_HBM	Electrostatic discharge human body model	2000	–	–	V	All pins except LG1FET_DRAIN (EPAD P1), LG2FET_DRAIN (EPAD P2), HG1FET_DRAIN (EPAD P3), and HG2FET_DRAIN (EPAD P4)
		–	–	2000		All pins except LG1FET_DRAIN (EPAD P1), LG2FET_DRAIN (EPAD P2), HG1FET_DRAIN (EPAD P3), and HG2FET_DRAIN (EPAD P4)
		–	–	500		LG1FET_DRAIN (EPAD P1), LG2FET_DRAIN (EPAD P2), HG1FET_DRAIN (EPAD P3), and HG2FET_DRAIN (EPAD P4)
ESD_CDM	Electrostatic discharge charged device model	500	–	–		Charged device model ESD
LU	Pin current for latch-up	–100	–	100	mA	–
T_J	Junction temperature	–40	–	125	°C	–

Note

9. Usage above the absolute maximum conditions listed in **Table 12** may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150°C in compliance with JEDEC Standard JESD22-A103, high temperature storage life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

6.2 Device-level specifications

All specifications are valid for –40°C ≤ T_A ≤ 105°C and T_J ≤ 125°C, except where noted. Specifications are valid for 3.0 V to 5.5 V except where noted.

6.2.1 DC specifications

Table 13 DC specifications (operating conditions)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PWR#1	V_{IN}	Input supply voltage	4.0	–	24	V	–
SID.PWR#1A	V_{IN_BB}	Buck-boost operating input supply voltage	4.5	–	24		–
SID.PWR#2	V_{DDD_REG}	VDDD output with VIN 5.5 V to 24 V, max load = 75 mA	4.6	–	5.5		–
SID.PWR#2A	V_{DDD_BYPASS}	VDDD output with VIN 4.5 V to 5.5 V, max load = 75 mA	V_{IN} – 0.7	–	5.5		–
SID.PWR#3	V_{DDD_MIN}	VDDD output with VIN 4 V to 4.5 V, max load = 20mA	V_{IN} – 0.2	–	–		–
SID.PWR#20	VBUS	VBUS_C valid range	3.3	–	21.5		–
SID.PWR#5	V_{CCD}	Regulated output voltage (for core Logic)	–	1.8	–		–
SID.PWR#16	C_{EFC_VCCD}	External regulator voltage bypass for VCCD	80	100	120	nF	X5R ceramic
SID.PWR#17	C_{EXC_VDDD}	Power supply decoupling capacitor for V_{DDD}	–	10	–	µF	
SID.PWR#18	C_{EXV}	Bootstrap supply capacitor (BST1, BST2)	–	0.1	–		
SID.PWR#24	I_{DD_ACT}	Supply current at 0.4 MHz switching frequency	–	50	–	mA	T_A = 25°C, VIN = 12 V. CC IO IN transmit or receive, no I/O sourcing current, No VCONN load current, CPU at 24 MHz, PD port active. Buck-boost converter on, 3 nF gate driver capacitance.

Table 13 DC specifications (operating conditions) *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
Deep Sleep mode							
SID_DS1	I_{DD_DS1}	V_{IN} = 12 V. CC wakeup on, type-C not connected, Source mode	–	80	–	µA	Type-C not attached, CC enabled for wakeup. R_p connection should be enabled for the PD port. T_A = 25°C. All faults disabled including VBAT-GND short protection.
SID_DS2	I_{DD_DS2}	VIN = 12 V, GPIO wake-up	–	50	–		USBPD disabled. Wake-up from GPIO. T_A = 25°C. All faults disabled.
SID_DS3	I_{DD_DS3}	VIN = 12 V. CC wakeup on, type-C not connected, Source mode	–	300	–		Type-C not attached, CC enabled for wakeup. R_p connection should be enabled for the PD port. T_A = 25°C. All faults disabled except VBAT-GND short protection.

6.2.2 CPU

Table 14 CPU specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.CLK#4	F_{CPU}	CPU input frequency	–	–	48	MHz	–40°C ≤ T_A ≤ +105°C, all V_{DDD}
SID.PWR#19	$T_{DEEPSLEEP}$	Wake-up from Deep Sleep mode	–	35	–	µs	–
SYS.XRES#5	T_{XRES}	External reset pulse width	5	–	–		

6.2.3 GPIO

Table 15 GPIO DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GIO#9	V_{IH_CMOS}	Input voltage high threshold	$0.7 \times V_{DDD}$	–	–	V	CMOS input
SID.GIO#10	V_{IL_CMOS}	Input voltage low threshold	–	–	$0.3 \times V_{DDD}$		
SID.GIO#11	V_{IH_TTL}	LVTTL input	2.0	–	–		–40°C ≤ TA ≤ +105°C
SID.GIO#12	V_{IL_TTL}	LVTTL input	–	–	0.8		–40°C ≤ TA ≤ +105°C
SID.GIO#7	V_{OH_3V}	Output voltage high level	$V_{DDD} - 0.6$	–	–		I_{OH} = –4 mA, –40°C ≤ T_A ≤ +105°C
SID.GIO#8	V_{OL_3V}	Output voltage low level	–	–	0.6		I_{OL} = 10 mA, –40°C ≤ T_A ≤ +105°C
SID.GIO#2	Rpu	Pull-up resistor when enabled	3.5	5.6	8.5	kΩ	–40°C ≤ T_A ≤ +105°C
SID.GIO#3	Rpd	Pull-down resistor when enabled	3.5	5.6	8.5		
SID.GIO#4	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	+25°C T_A, 3-V V_{DDD}
SID.GIO#5	C_{PIN_A}	Max pin capacitance	–	–	22	pF	–40°C ≤ T_A ≤ +105°C, capacitance on DP, DM pins
SID.GIO#6	C_{PIN}	Max pin capacitance	–	3	7		–40°C ≤ T_A ≤ +105°C, all V_{DDD}, all other I/Os
SID.GIO#13	V_{HYSTTL}	Input hysteresis, LVTTL, V_{DDD} > 2.7 V	100	–	–	mV	V_{DDD} > 2.7 V
SID.GIO#14	$V_{HYSCMOS}$	Input hysteresis CMOS	$0.1 \times V_{DDD}$	–	–		–

Table 16 GPIO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GIO#16	T_{RISEF}	Rise time in fast strong mode	2	–	12	ns	C_{load} = 25 pF, –40°C ≤ T_A ≤ +105°C
SID.GIO#17	T_{FALLF}	Fall time in fast strong mode	2	–	12		
SID.GIO#18	T_{RISES}	Rise time in slow strong mode	10	–	60		
SID.GIO#19	T_{FALLS}	Fall time in slow strong mode	10	–	60		
SID.GIO#20	F_{GPIO_OUT1}	GPIO F_{OUT}; 3.0 V ≤ V_{DDD} ≤ 5.5 V. Fast strong mode.	–	–	16	MHz	
SID.GIO#21	F_{GPIO_OUT2}	GPIO F_{OUT}; 3.0 V ≤ V_{DDD} ≤ 5.5 V. Slow strong mode.	–	–	7		
SID.GIO#22	F_{GPIO_IN}	GPIO input operating frequency; 3.0 V ≤ V_{DDD} ≤ 5.5 V.	–	–	16		–40°C ≤ T_A ≤ +105°C

Table 17 GPIO OVT DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GPIO_20VT_GIO#4	GPIO_20VT_I_LU	GPIO_20VT latch up current limits	–140	–	140	mA	Max / min current in to any input or output, pin-to-pin, pin-to-supply
SID.GPIO_20VT_GIO#5	GPIO_20VT_RPU	GPIO_20VT pull-up resistor value	3.5	–	8.5	kΩ	–40°C ≤ T_A ≤ +105°C, all V_{DDD}
SID.GPIO_20VT_GIO#6	GPIO_20VT_RPD	GPIO_20VT pull-down resistor value	3.5	–	8.5		–40°C ≤ T_A ≤ +105°C, all V_{DDD}
SID.GPIO_20VT_GIO#16	GPIO_20VT_IIL	GPIO_20VT input leakage current (absolute value)	–	–	2	nA	+25°C T_A, 3-V V_{DDD}
SID.GPIO_20VT_GIO#17	GPIO_20VT_CPIN	GPIO_20VT pin capacitance	–	–	10	pF	–40°C ≤ T_A ≤ +105°C, all V_{DDD}

Table 17 GPIO OVT DC specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GPIO_20VT_GIO#33	GPIO_20VT_Voh	GPIO_20VT output voltage high level	VDDD – 0.6	–	–	V	I_{OH} = -4 mA
SID.GPIO_20VT_GIO#36	GPIO_20VT_Vol	GPIO_20VT output voltage low level	–	–	0.6		I_{OL} = 8 mA
SID.GPIO_20VT_GIO#41	GPIO_20VT_Vih_LVTTL	GPIO_20VT LVTTL input	2	–	–		–40°C ≤ T_A ≤ +105°C, all V_{DDD}
SID.GPIO_20VT_GIO#42	GPIO_20VT_Vil_LVTTL	GPIO_20VT LVTTL input	–	–	0.8		–40°C ≤ T_A ≤ +105°C, all V_{DDD}
SID.GPIO_20VT_GIO#43	GPIO_20VT_Vhysttl	GPIO_20VT input hysteresis LVTTL	100	–	–	mV	–40°C ≤ T_A ≤ +105°C, all V_{DDD}
SID.GPIO_20VT_GIO#45	GPIO_20VT_ITOT_GPIO	GPIO_20VT maximum total sink pin current to ground	–	–	95	mA	V (GPIO_20VT pin) > V_{DDD}

Table 18 GPIO OVT AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GPIO_20VT_70	GPIO_20VT_TriseF	GPIO_20VT rise time in fast strong mode	1	–	15	ns	All V_{DDD}, C_{load} = 25 pF
SID.GPIO_20VT_71	GPIO_20VT_TfallF	GPIO_20VT fall time in fast strong mode	1	–	15		
SID.GPIO_20VT_GIO#46	GPIO_20VT_TriseS	GPIO_20VT rise time in slow strong mode	10	–	70		
SID.GPIO_20VT_GIO#47	GPIO_20VT_TfallS	GPIO_20VT Fall time in slow strong mode	10	–	70		
SID.GPIO_20VT_GIO#48	GPIO_20VT_FGPIO_OUT1	GPIO_20VT GPIO Fout; 3 V ≤ V_{DDD} ≤ 5.5 V. Fast strong mode.	–	–	33	MHz	
SID.GPIO_20VT_GIO#50	GPIO_20VT_FGPIO_OUT3	GPIO_20VT GPIO Fout; 3 V ≤ V_{DDD} ≤ 5.5V. Slow strong mode.	–	–	7		
SID.GPIO_20VT_GIO#52	GPIO_20VT_FGPIO_IN	GPIO_20VT GPIO input operating frequency; 3 V ≤ V_{DDD} ≤ 5.5 V	–	–	8		All V_{DDD}

6.2.4 XRES

Table 19 XRES DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.XRES#1	V_{IH_XRES}	Input voltage high threshold on XRES pin	$0.7 \times V_{DDD}$	–	–	V	CMOS input
SID.XRES#2	V_{IL_XRES}	Input voltage low threshold on XRES pin	–	–	$0.3 \times V_{DDD}$		
SID.XRES#3	C_{IN_XRES}	Input capacitance on XRES pin	–	–	7	pF	–
SID.XRES#4	$V_{HYSXRES}$	Input voltage hysteresis on XRES pin	–	$0.05 \times V_{DDD}$	–	mV	–

6.3 Digital peripherals

The following specifications apply to the timer/counter/PWM peripherals in the timer mode.

6.3.1 Pulse width modulation (PWM) for GPIO pins

Table 20 PWM AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.TCPWM.1	$TCPWM_{FREQ}$	Operating frequency	–	–	Fc	MHz	Fc max = CLK_SYS
SID.TCPWM.3	T_{PWMEXT}	Output trigger pulse width	2/Fc	–	–	ns	Minimum possible width of overflow, underflow, and CC (Counter equals compare value) outputs
SID.TCPWM.4	T_{CRES}	Resolution of counter	1/Fc	–	–		Minimum time between successive counts
SID.TCPWM.5	PWM_{RES}	PWM resolution	1/Fc	–	–		Minimum pulse width of PWM output

6.3.2 I^2C

Table 21 Fixed I^2C AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	–

6.3.3 UART

Table 22 Fixed UART AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	–

6.3.4 SPI

Table 23 Fixed SPI AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID166	F_{SPI}	SPI operating frequency (master; 6X oversampling)	–	–	8	MHz	–

Table 24 Fixed SPI master mode AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID167	T_{DMO}	MOSI valid after SClock driving edge	–	–	15	ns	–
SID168	T_{DSI}	MISO valid before SClock capturing edge	20	–	–		Full clock, late MISO sampling
SID169	T_{HMO}	Previous MOSI data hold time	0	–	–		Referred to slave capturing edge

Table 25 Fixed SPI Slave mode AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID170	T_{DMI}	MOSI valid before Sclock capturing edge	40	–	–	ns	–
SID171	T_{DSO}	MISO valid after Sclock driving edge	–	–	$48 + (3 \times T_{CPU})$		$T_{CPU} = 1/F_{CPU}$
SID171A	T_{DSO_EXT}	MISO valid after Sclock driving edge in ext clk mode	–	–	48		–
SID172	T_{HSO}	Previous MISO data hold time	0	–	–		–
SID172A	$T_{SSELSCK}$	SSEL valid to first SCK valid edge	100	–	–		–

6.3.5 Memory

Table 26 Flash AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.MEM#2	FLASH_ WRITE	Row (block) write time (Erase and program)	–	–	20	ms	–40°C ≤ T_A ≤ +85°C, all V_{DDD}
SID.MEM#1	FLASH_ ERASE	Row erase time	–	–	15.5		
SID.MEM#5	FLASH_ ROW_PGM	Row program time after erase	–	–	7		
SID178	$T_{BULKERASE}$	Bulk erase time (32 KB)	–	–	35		-
SID180	$T_{DEVPROG}$	Total device program time	–	–	7.5	s	
SID.MEM#6	FLASH_ENPB	Flash write endurance	100k	–	–	cycles	25°C ≤ T_A ≤ 55°C, all V_{DDD}
SID182	F_{RET1}	Flash retention, T_A ≤ 55°C, 100K P/E cycles	20	–	–	years	–
SID182A	F_{RET2}	Flash retention, T_A ≤ 85°C, 10K P/E cycles	10	–	–		–

6.4 System resources

6.4.1 Power-on-reset (POR) with brown out

Table 27 Imprecise power-on reset (IPOR)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID185	$V_{RISEIPOR}$	Power-on reset (POR) rising trip voltage	0.80	–	1.50	V	–40°C ≤T_A ≤ +105°C, all V_{DDD}
SID186	$V_{FALLIPOR}$	POR falling trip voltage	0.70	–	1.4		

Table 28 Precise POR

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID190	$V_{FALLPPOR}$	Brown-out detect (BOD) trip voltage in active/sleep modes	1.48	–	1.62	V	–40°C ≤ T_A ≤ +105°C, all V_{DDD}
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep mode	1.1	–	1.5		

6.4.2 SWD interface

Table 29 SWD interface specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.SWD#1	F_SWDCLK1	3.0 V ≤ V_{DDIO} ≤ 5.5 V	–	–	14	MHz	–
SID.SWD#2	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
SID.SWD#3	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 × T	–	–		
SID.SWD#4	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.50 × T		
SID.SWD#5	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–		

6.4.3 Internal main oscillator

Table 30 IMO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.CLK#13	F_{IMOTOL}	Frequency variation at 48 MHz (trimmed)	–	–	±2	%	3.0 V ≤ V_{DDD} < 5.5 V. –40°C ≤ T_A ≤ 105°C
SID226	$T_{STARTIMO}$	IMO start-up time	–	–	7	µs	–40°C ≤ T_A ≤ +105°C, all V_{DDD}
SID.CLK#1	F_{IMO}	IMO frequency	24	–	48	MHz	

6.4.4 Internal low-speed oscillator

Table 31 ILO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID234	$T_{STARTILO1}$	ILO start-up time	–	–	2	ms	–40°C ≤ T_A ≤ +105°C, all V_{DDD}
SID238	$T_{ILODUTY}$	ILO duty cycle	40	50	60	%	
SID.CLK#5	F_{ILO}	ILO frequency	20	40	80	kHz	–

6.4.5 PD

Table 32 PD DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.DC.cc_shvt.1	vSwing	Transmitter output high voltage	1.05	–	1.2	V	–
SID.DC.cc_shvt.2	vSwing_low	Transmitter output low voltage	–	–	0.075		–
SID.DC.cc_shvt.3	zDriver	Transmitter output impedance	33	–	75	W	–
SID.DC.cc_shvt.4	zBmcRx	Receiver input impedance	10	–	–	MΩ	–
SID.DC.cc_shvt.5	Idac_std	Source current for USB standard advertisement	64	–	96	µA	–
SID.DC.cc_shvt.6	Idac_1p5a	Source current for 1.5 A at 5 V advertisement	166	–	194		–
SID.DC.cc_shvt.7	Idac_3a	Source current for 3 A at 5 V advertisement	304	–	356		–
SID.DC.cc_shvt.8	Rd	Pull down termination resistance when acting as UFP (upstream facing port)	4.59	–	5.61	kΩ	–
SID.DC.cc_shvt.10	zOPEN	CC impedance to ground when disabled	108	–	–		–
SID.DC.cc_shvt.11	DFP_default_0p2	CC voltages on DFP side-standard USB	0.15	–	0.25	V	–
SID.DC.cc_shvt.12	DFP_1.5A_0p4	CC voltages on DFP side-1.5A	0.35	–	0.45		–
SID.DC.cc_shvt.13	DFP_3A_0p8	CC voltages on DFP side-3A	0.75	–	0.85		–
SID.DC.cc_shvt.14	DFP_3A_2p6	CC voltages on DFP side-3A	2.45	–	2.75		–
SID.DC.cc_shvt.15	UFP_default_0p66	CC voltages on UFP side-standard USB	0.61	–	0.7		–
SID.DC.cc_shvt.16	UFP_1.5A_1p23	CC voltages on UFP side-1.5A	1.16	–	1.31		–
SID.DC.cc_shvt.17	Vattach_ds	Deep Sleep attach threshold	0.3	–	0.6	%	–
SID.DC.cc_shvt.18	Rattach_ds	Deep Sleep pull-up resistor	10	–	50	kΩ	–
SID.DC.cc_shvt.19	VTX_step	TX drive voltage step size	80	–	120	mV	–

6.4.6 Analog-to-digital converter

Table 33 ADC DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.ADC.1	Resolution	ADC resolution	–	8	–	Bits	–
SID.ADC.2	INL	Integral non-linearity	–1.5	–	1.5	LSB	Reference voltage generated from bandgap.
SID.ADC.3	DNL	Differential non-linearity	–2.5	–	2.5		Reference voltage generated from V_{DDD}.
SID.ADC.4	Gain Error	Gain error	–1.5	–	1.5		Reference voltage generated from bandgap.
SID.ADC.5	VREF_ADC1	Reference voltage of ADC	V_{DDDmin}	–	V_{DDDmax}	V	Reference voltage generated from V_{DDD}.
SID.ADC.6	VREF_ADC2	Reference voltage of ADC	1.96	2.0	2.04		Reference voltage generated from Deep Sleep reference.

6.4.7 HS CSA

Table 34 HS CSA DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.HSCSA.1	Csa_Acc1	CSA accuracy 5 mV < Vsense < 10 mV	–15	–	15	%	Active mode
SID.HSCSA.2	Csa_Acc2	CSA accuracy 10 mV < Vsense < 15 mV	–10	–	10		
SID.HSCSA.3	Csa_Acc3	CSA accuracy 15 mV < Vsense < 25 mV	–5	–	5		
SID.HSCSA.4	Csa_Acc4	CSA accuracy 25 mV < Vsense	–3	–	3		
SID.HSCSA.7	Csa_SCP_Acc1	CSA SCP at 6 A with 5 mΩ sense resistor	–10	–	10		
SID.HSCSA.8	Csa_SCP_Acc2	CSA SCP at 10 A with 5 mΩ sense resistor	–10	–	10		
SID.HSCSA.9	Csa_OCP_1A	CSA OCP at 1 A with 5 mΩ sense resistor	104	130	156		
SID.HSCSA.10	Csa_OCP_5A	CSA OCP for 5 A with 5 mΩ sense resistor	123	130	137		

Table 35 HS CSA AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.HSCSA.AC.1	T_{SCP_GATE}	Delay from SCP threshold trip to external NFET power gate turn off	–	3.5	–	µs	1 nF NFET gate
SID.HSCSA.AC.2	$T_{SCP_GATE_1}$	Delay from SCP threshold trip to external NFET power gate turn off	–	8	–		3 nF NFET gate

6.4.8 UV/OV

Table 36 UV/OV specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.UVOV.1	VTHOV1	Overvoltage threshold Accuracy, 4 V to 11 V	–3	–	3	%	Active mode
SID.UVOV.2	VTHOV2	Overvoltage threshold Accuracy, 11 V to 21.5 V	–3.2	–	3.2		
SID.UVOV.3	VTHUV1	Undervoltage threshold Accuracy, 3 V to 3.3 V	–4	–	4		
SID.UVOV.4	VTHUV2	Undervoltage threshold Accuracy, 3.3 V to 4.0 V	–3.5	–	3.5		
SID.UVOV.5	VTHUV3	Undervoltage threshold Accuracy, 4.0 V to 21.5 V	–3	–	3		

6.4.9 VCONN switch

Table 37 VCONN switch DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
DC.VCONN.1	VCONN_OUT	VCONN output voltage with 20 mA load current	4.5	–	5.5	V	–
DC.VCONN.2	I_{LEAK}	Connector side pin leakage current	–	–	10	µA	–
DC.VCONN.3	I_{OCP}	VCONN overcurrent protection threshold	22.5	30	42.5	mA	–

Table 38 VCONN switch AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
AC.VCONN.1	T_{ON}	VCONN switch turn-on time	–	–	600	µs	–
AC.VCONN.2	T_{OFF}	VCONN switch turn-off time	–	–	10		–

6.4.10 V_{BUS}

Table 39 V_{BUS} discharge specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.VBUS.DISC.1	R1	20 V NMOS ON resistance for DS = 1	500	–	2000	Ω	Measured at 0.5 V.
SID.VBUS.DISC.2	R2	20 V NMOS ON resistance for DS = 2	250	–	1000		
SID.VBUS.DISC.3	R4	20 V NMOS ON resistance for DS = 4	125	–	500		
SID.VBUS.DISC.4	R8	20 V NMOS ON resistance for DS = 8	62.5	–	250		
SID.VBUS.DISC.5	R16	20 V NMOS ON resistance for DS = 16	31.25	–	125		
SID.VBUS.DISC.6	Vbus_stop_error	Error percentage of final VBUS value from setting	–	–	10	%	When VBUS is discharged to 5 V.

6.4.11 Voltage regulation

Table 40 Voltage regulation DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.DC.VR.1	VOUT	CSNO output voltage range	3.3	–	21.5	V	–
SID.DC.VR.2	VR	CSNO voltage regulation accuracy	–	±3	±5	%	–
SID.DC.VR.3	VIN_UVLO	VIN supply below which chip will get reset	1.7	–	3.0	V	–

Table 41 Voltage regulator AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.VREG.1	T_{START}	Total startup time for the regulator supply outputs	–	–	200	µs	–

6.4.12 VBUS gate driver

Table 42 VBUS gate driver DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GD.1	GD_VGS	Gate to source overdrive during ON condition	4.5	5	10	V	NFET driver is ON.
SID.GD.2	GD_RPD	Resistance when pull-down enabled	–	–	2	kΩ	Applicable on VBUS_CTRL to turn off external NFET.
SID.GD.5	GD_drv	Programmable typical gate current	0.3	–	9.75	µA	–

Table 43 VBUS gate Driver AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GD.3	T_{ON}	VBUS_CTRL low to high (1 V to VBUS + 1 V) with 3 nF external capacitance	2	5	10	ms	CSNO = 5 V
SID.GD.4	T_{OFF}	VBUS_CTRL high to low (90% to 10%) with 3 nF external capacitance	–	7	–	µs	CSNO = 21.5 V

6.4.13 PWM controller

Table 44 Buck-boost PWM controller specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
PWM.1	F_{SW}	Switching frequency	150	–	600	kHz	–
PWM.2	FSS	Spread spectrum frequency dithering span	–	10	–	%	–
PWM.3	Ratio_ buck_BB	Buck to buck boost ratio	–	1.16	–	V/V	–
PWM.4	Ratio_ boost_BB	Boost to buck boost ratio	–	0.84	–		–

6.4.14 NFET gate driver

Table 45 Buck-boost NFET gate driver specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
DR.1	R_HS_PU	Top-side gate driver on-resistance-gate pull-up	–	2	–	Ω	–
DR.2	R_HS_PD	Top-side gate driver on-resistance-gate pull-down	–	1.5	–		–
DR.3	R_LS_PU	Bottom-side gate driver on-resistance-gate pull-up	–	2	–		–
DR.4	R_LS_PD	Bottom-side gate driver on-resistance-gate pull-down	–	1.5	–		–
DR.5	Dead_HS	Dead time before high-side rising edge	–	30	–	ns	–
DR.6	Dead_LS	Dead time before low-side rising edge	–	30	–		–
DR.7	Tr_HS	Top-side gate driver rise time	–	25	–		–
DR.8	Tf_HS	Top-side gate driver fall time	–	20	–		–
DR.9	Tr_LS	Bottom-side gate driver rise time	–	25	–		–
DR.10	Tf_LS	Bottom-side gate driver fall time	–	20	–		–

6.4.15 LS-SCP

Table 46 LS-SCP DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.LSSCP.DC.1	SCP_6A	Short circuit current detect @ 6 A	5.4	6	6.6	A	Using differential inputs (CSP_GPIO2, CSN_GPIO3)
SID.LSSCP.DC.1A	SCP_6A_SE	Short circuit current detect @ 6 A	4.5	6	7.5		Using single ended inputs (CSP_GPIO2) and internal ground
SID.LSSCP.DC.2	SCP_10A	Short circuit current detect @ 10 A	9	10	11		Using differential inputs (CSP_GPIO2, CSN_GPIO3)
SID.LSSCP.DC.2A	SCP_10A_SE	Short circuit current detect @ 10 A	7.5	10	12.5		Using single ended inputs (CSP_GPIO2) and internal ground

6.4.16 Switching FETs

Table 47 Switching FET specifications

Spec ID	Parameter	Min	Typ	Max	Unit	Details/conditions
FET.DC.1	Drain-source breakdown voltage ($V_{(BR)DSS}$)	40	–	–	V	V_{GS} = 0 V, I_D = 1 mA
FET.DC.2	Gate threshold voltage $V_{GS(TH)}$	1.2	1.6	2.0	V	V_{DS} = V_{GS}, I_D = 10 µA
FET.DC.3	LGFET ON resistance Low-side MOSFET ($R_{DS(ON)}$)	–	9	–	mΩ	V_{GS} = 5 V, I_D = 8 A
FET.DC.4	HGFET ON resistance High-side MOSFET ($R_{DS(ON)}$)	–	9	–	mΩ	V_{GS} = 5 V, I_D = 8 A
FET.DC.3	LGFET ON resistance Low-side MOSFET ($R_{DS(ON)}$) (for CYPD7197)	–	TBD	–	mΩ	V_{GS} = 5 V, I_D = 8 A
FET.DC.4	HGFET ON resistance High-side MOSFET ($R_{DS(ON)}$) (for CYPD7197)	–	TBD	–	mΩ	V_{GS} = 5 V, I_D = 8 A
FET.AC.1	Turn-on delay time ($t_{d(on)}$)	–	2	–	ns	V_{DS} = 6 V, V_{GS} = 5 V, I_D = 5 A
FET.AC.2	Rise time (t_r)	–	2	–	ns	–
FET.AC.3	Turn-off delay time ($t_{d(off)}$)	–	6	–	ns	–
FET.AC.4	Fall time (t_f)	–	5	–	ns	–
FET.AC.5	Gate plateau voltage ($V_{plateau}$)	–	3.0	–	V	V_{DS} = 6 V, I_D = 5 A, V_{GS} = 0 to 5 V

6.4.17 Thermal

Table 48 Thermal specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.OTP.1	OTP	Thermal shutdown	120	125	130	°C	–

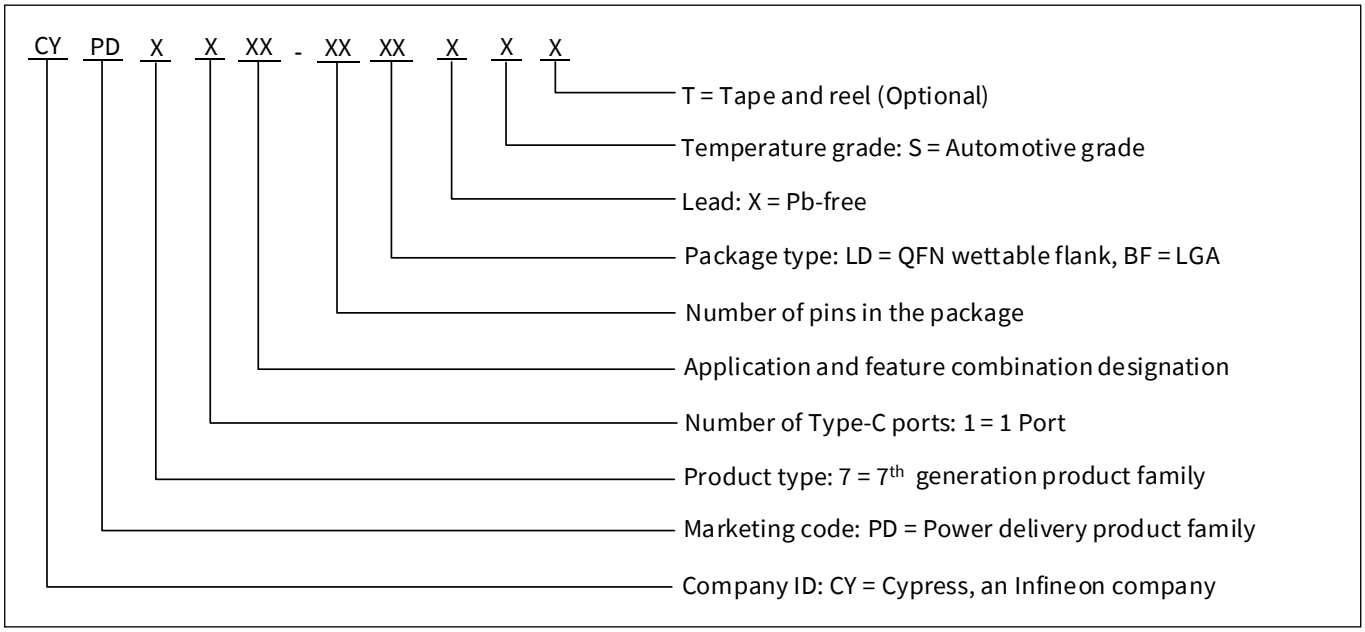
7 Ordering information

Table 49 lists the EZ-PD™ CYPD719X part numbers and features.

Table 49 EZ-PD™ CYPD719X ordering information

Product	Integrated FET's	Application	Role	Recommended Power level	Package type	Package Size
CYPD7191-40LDXS	0	Rear-seat and head unit charger	DFP (Power source only)	Greater than 65 W	40-pin QFN	6 mm x 6 mm
CYPD7191-40LDXST						
CYPD7199-40LDXS		Rear seat entertainment charger (DP alt mode)	DRP with UFP data, DFP with DFP data			
CYPD7199-40LDXST						
CYPD7194-40BFXS	4	Rear seat charger	DFP (Power source only)	Less than equal to 65W without heat sink. Greater than 65 W with heat sink	40-pin LGA	6.5 mm x 9.25 mm
CYPD7194-40BFXST						
CYPD7195-40BFXS		Head unit charger	DFP (Power source only)			
CYPD7195-40BFXST						
CYPD7196-40BFXS		Rear seat entertainment charger (DP alt mode)	DRP with UFP data, DFP with DFP data			
CYPD7196-40BFXST						
CYPD7197-40BFXS		Rear-seat charger	DFP (Power source only)	Less than equal to 30 W		
CYPD7197-40BFXST						
CYPD7192-39BFXS	2	Rear-seat charger	DFP (Power source only)	Less than equal to 65 W, Buck-Boost design or less than 30W Buck only design	39-pin LGA	6 mm x 7 mm
CYPD7192-39BFXST						
CYPD7193-39BFXS		Head unit charger	DFP (Power source only)			
CYPD7193-39BFXST						
CYPD7198-39BFXS		Rear seat entertainment charger (DP alt mode)	DRP with UFP data, DFP with DFP data			
CYPD7198-39BFXST						

7.1 Ordering code definitions



8 Packaging

Table 50 EZ-PD™ CYPD719X without integrated FETs: 40-QFN package characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_J	Operating junction temperature	–	–40	25	125	°C
T_{JA}	Package θ_{JA}	–	–	–	15.45	°C/W
T_{JC}	Package θ_{JC}		–	–	4.4	

Table 51 EZ-PD™ CYPD719X with buck FETs integrated: 39-LGA package characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_J	Operating junction temperature	–	–40	25	125	°C
T_{JA}	Package θ_{JA}	–	–	–	17.7	°C/W
T_{JC}	Package θ_{JC}		–	–	5.17	

Table 52 EZ-PD™ CYPD719X with integrated FETs: 40-LGA package characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_J	Operating junction temperature	–	–40	25	125	°C
T_{JA}	Package θ_{JA}	–	–	–	15.3	°C/W
T_{JC}	Package θ_{JC}		–	–	1.7	

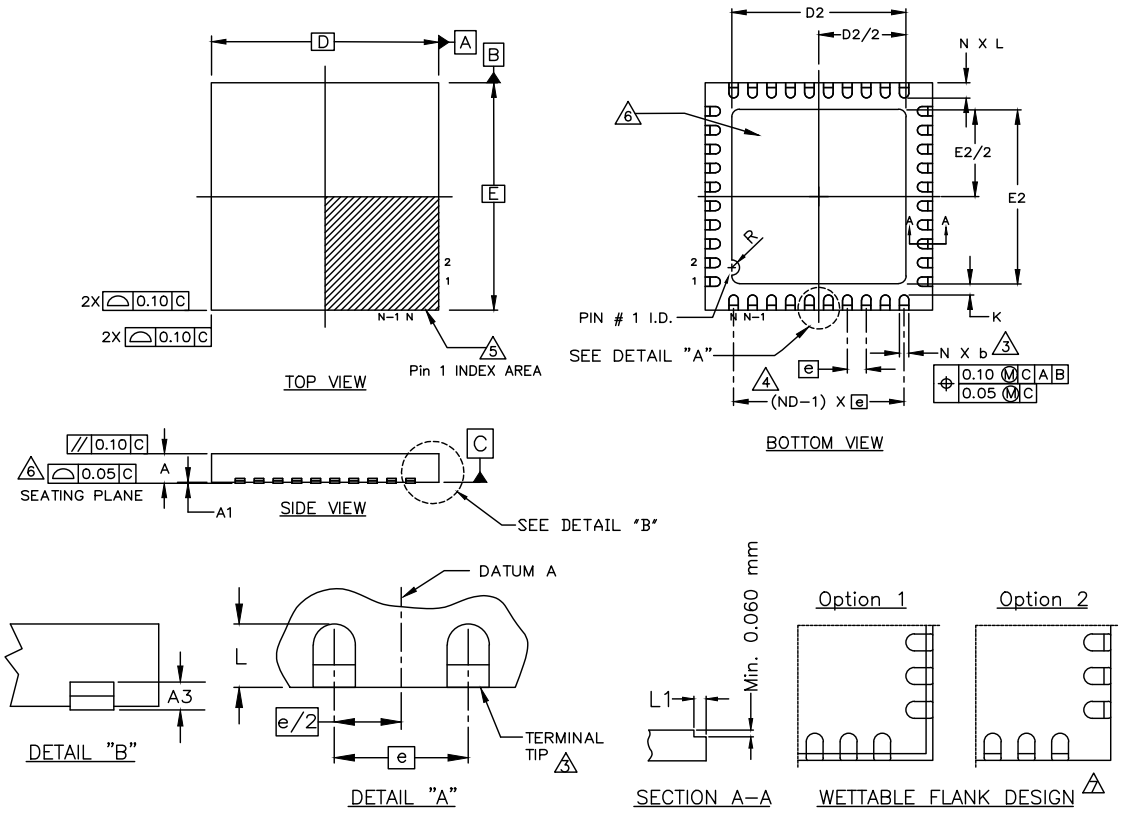
Table 53 Solder reflow peak temperature

Package	Maximum peak temperature	Maximum time within 5°C of peak temperature
40-QFN, 39-LGA, 40-LGA	260°C	30 s

Table 54 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2

Package	MSL
40-QFN, 39-LGA, 40-LGA	MSL 3

8.1 Package diagrams



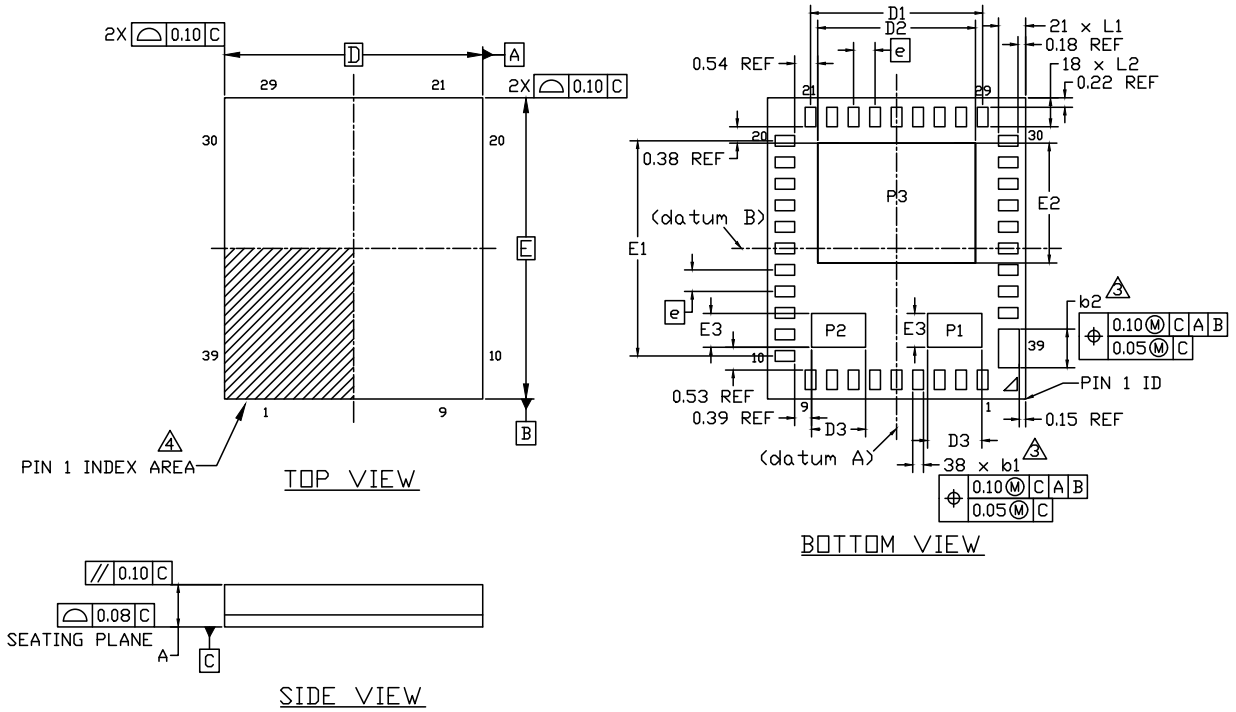
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
e	0.50 BSC		
N	40		
ND	10		
L	0.30	0.40	0.50
b	0.18	0.25	0.30
D2	4.50	4.60	4.70
E2	4.50	4.60	4.70
D	6.00 BSC		
E	6.00 BSC		
A	-	-	0.60
A1	0.00	-	0.05
A3	0.152 REF		
R	0.20 TYP		
K	0.20 MIN		
L1	0.115	0.125	0.135

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE TOTAL NUMBER OF TERMINALS.
3. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
4. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE.
5. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
6. COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
7. PLEASE REFER TO WETTABLE FLANK DESIGN BETWEEN OPTION 1 AND OPTION 2.
8. JEDEC SPECIFICATION NO. REF. : N/A.

002-33635 Rev. *A

Figure 27 40-pin QFN ((6.0 × 6.0 × 0.6 mm) LD40D (4.60 × 4.60 mm) EPAD (Wettable flank)) (PG-VQFN-40)



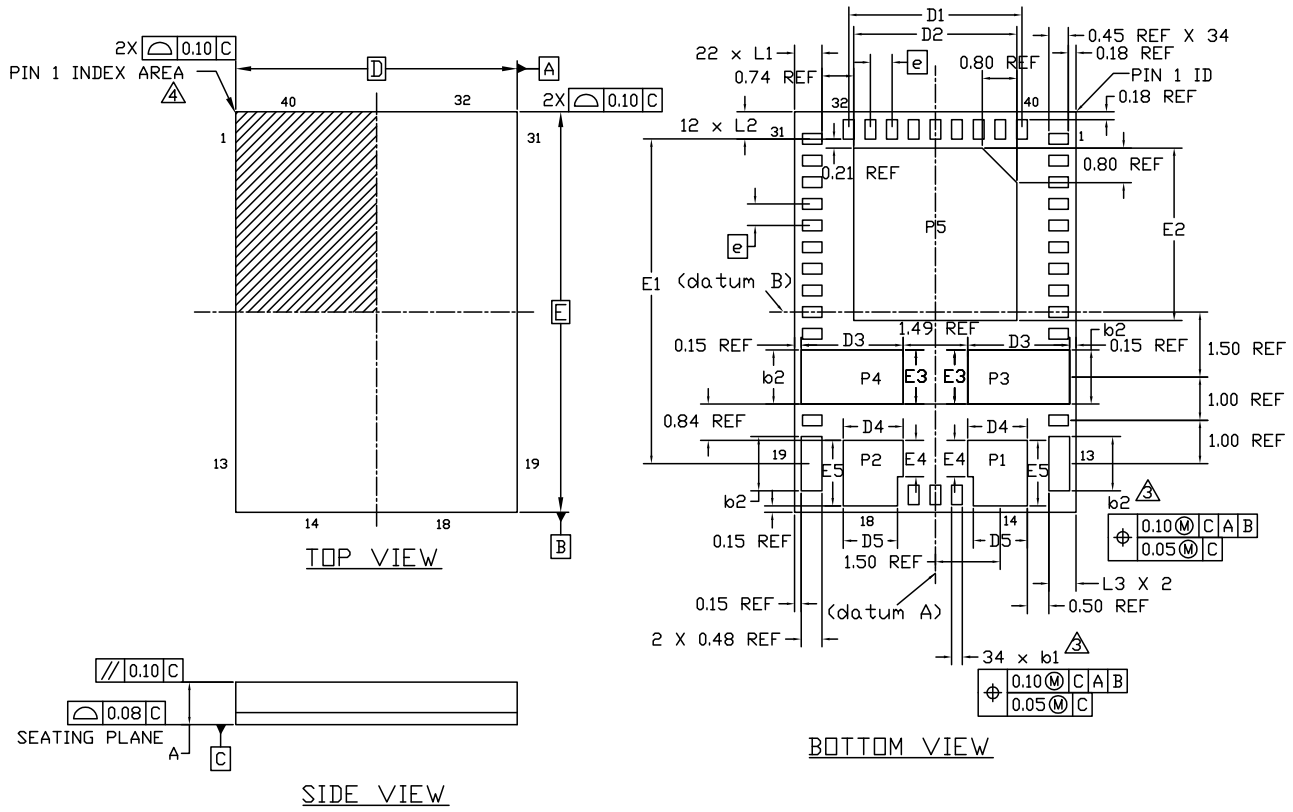
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
b1	0.20	0.25	0.30
b2	0.85	0.90	0.95
D	6.00 BSC		
E	7.00 BSC		
D1	3.90	4.00	4.10
D2	3.57	3.67	3.77
D3	1.16	1.26	1.36
E1	4.90	5.00	5.10
E2	2.68	2.78	2.88
E3	0.69	0.79	0.89
L1	0.58	0.63	0.68
L2	0.62	0.67	0.72
e	0.50 BSC		
N	39		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE TOTAL NUMBER OF LANDS.
3. DIMENSION "b" IS MEASURED AT THE MAXIMUM LAND WIDTH IN A PLANE PARALLEL TO DATUM C.
4. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
5. P1 - LGFET_DRAIN
   P2 - HGFET_DRAIN
   P3 - GND

002-38571 Rev. *B

Figure 28 **39-pin LGA (6.00 × 7.00 × 1.00 mm) BF39A (PG-TFLGA-39)**



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
b1	0.20	0.25	0.30
b2	1.20	1.25	1.30
D	6.50 BSC		
E	9.25 BSC		
D1	3.90	4.00	4.10
D2	3.67	3.77	3.87
D3	2.26	2.36	2.46
D4	1.28	1.38	1.48
D5	1.15	1.25	1.35
E1	7.40	7.50	7.60
E2	3.88	3.98	4.08
E3	1.15	1.25	1.35
E4	0.74	0.84	0.94
E5	1.41	1.51	1.61
L1	0.58	0.63	0.68
L2	0.58	0.63	0.68
L3	0.58	0.63	0.68
e	0.50 BSC		
N	40		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE TOTAL NUMBER OF LEADS.
3. DIMENSION "b" IS MEASURED AT THE MAXIMUM LEAD WIDTH IN A PLANE PARALLEL TO DATUM C.
4. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
5. P1 - LGFET_DRAIN
   P2 - LG2FET_DRAIN
   P3 - HGFET_DRAIN
   P4 - HG2FET_DRAIN
   P5 - GND
6. LEAD NUMBER 1 TO 10, 12, 15 TO 17, 20 AND 22 TO 40 HAVE SAME LEAD LENGTH AND WIDTH.

002-39871 Rev. **

Figure 29 40-pin LGA (6.50 × 9.25 × 1.00 mm) ROA040 (PG-TFLGA-40)

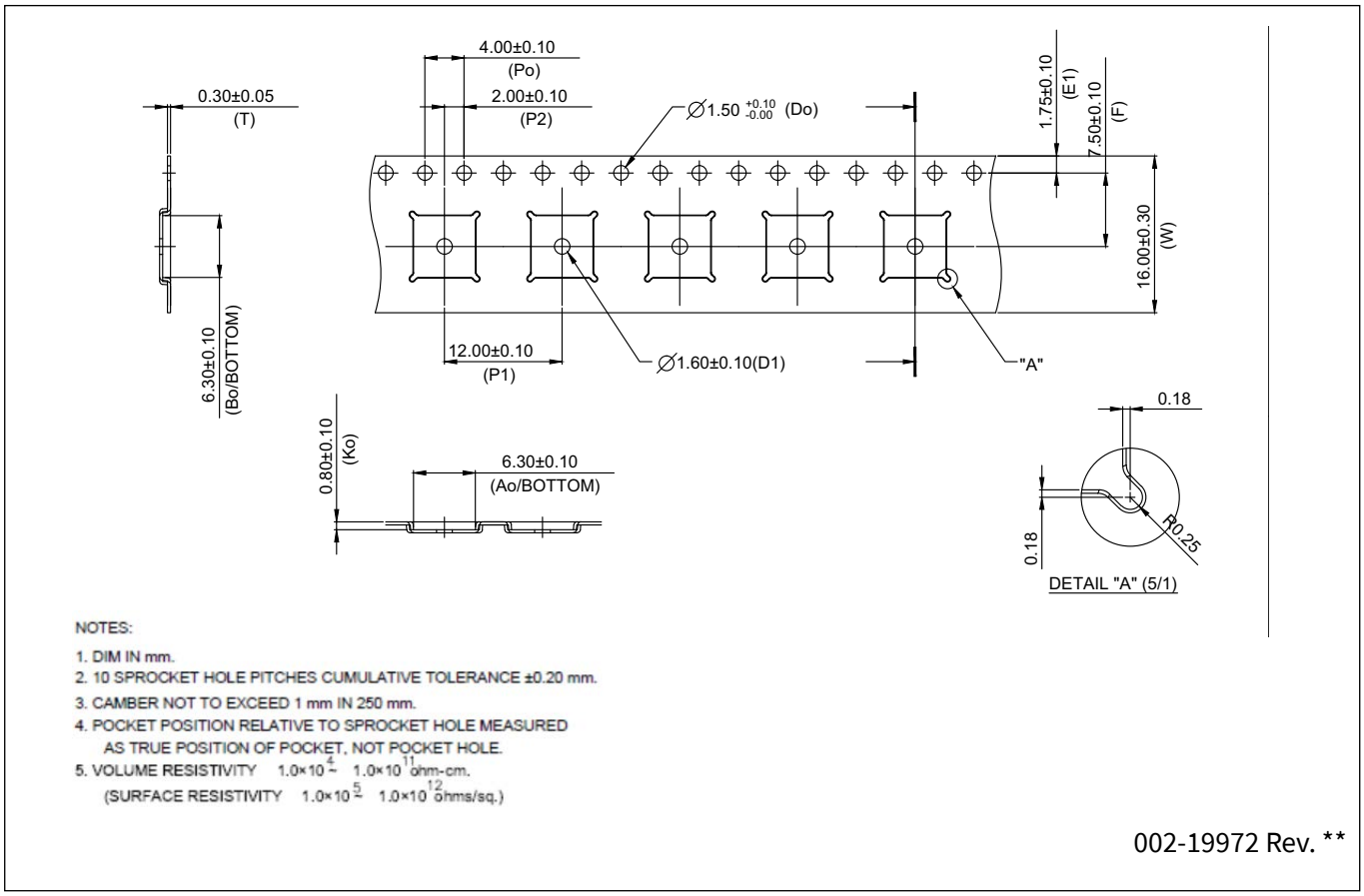
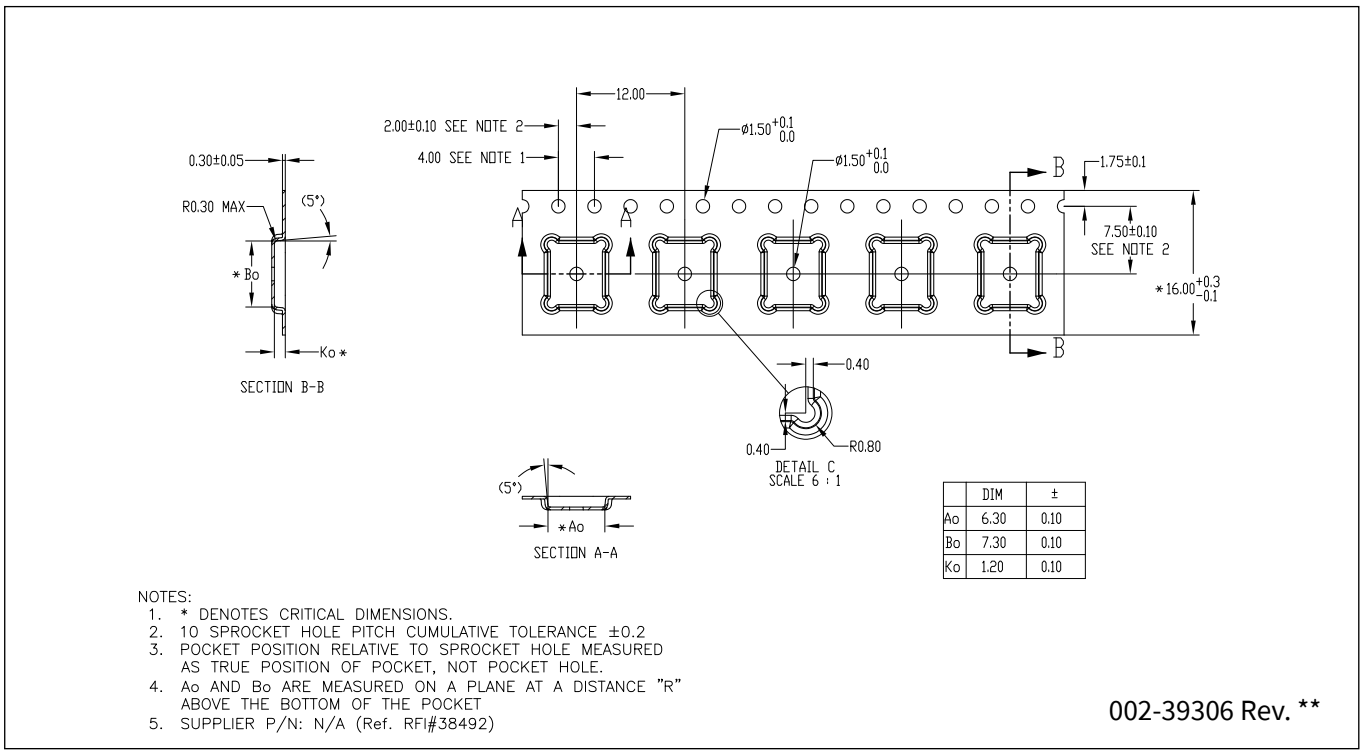


Figure 30 40-pin QFN: Carrier Tape, QFN0606



	DIM	±
Ao	6.30	0.10
Bo	7.30	0.10
Ko	1.20	0.10

Figure 31 39-pin LGA: Carrier Tape

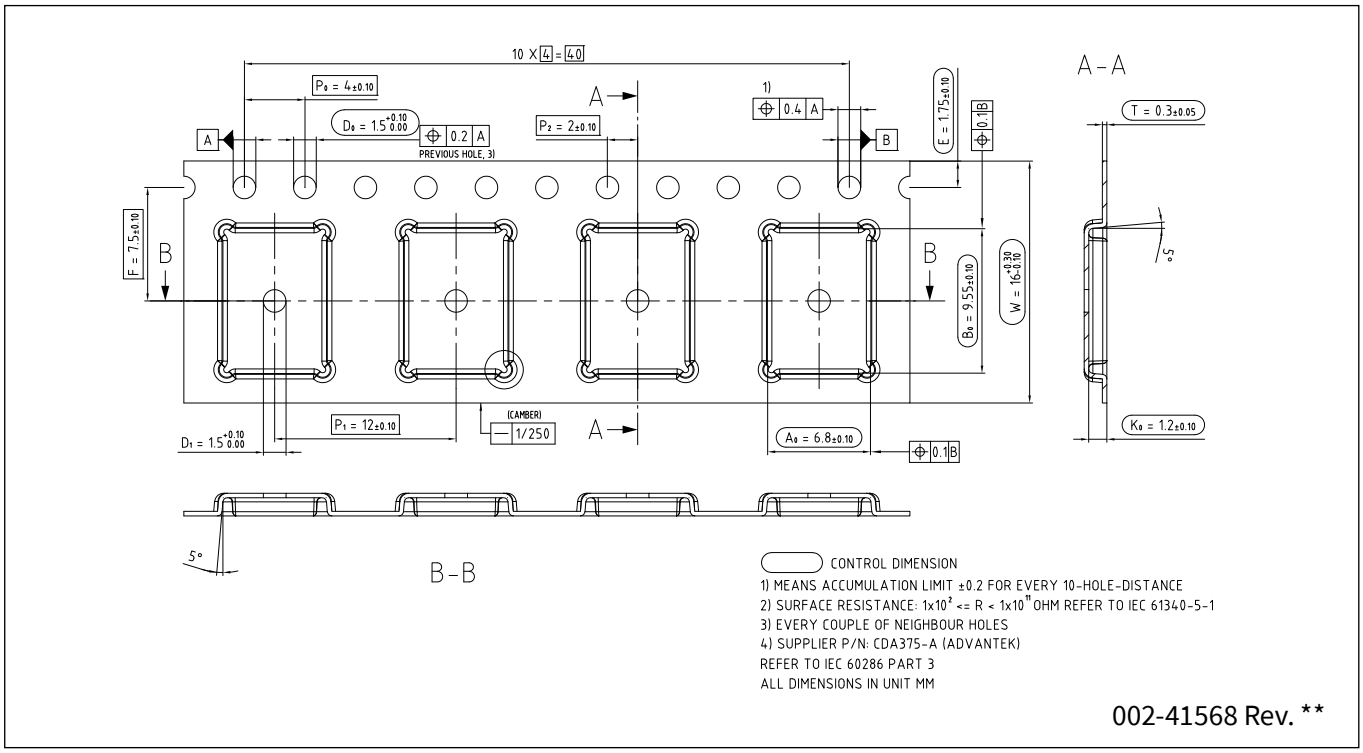


Figure 32 40-pin LGA: Carrier Tape

9 Acronyms

Table 55 Acronyms used in this document

Acronym	Description
ADC	analog-to-digital converter
AFC	Samsung adaptive fast charging
Arm®	advanced RISC machine, a CPU architecture
CPU	central processing unit
CSA	current sense amplifier
DAC	digital-to-analog converter
FCCM	forced continuous current/conduction mode
GPIO	general-purpose input/output
HSDR	high-side driver
I^2C, or IIC	inter-integrated circuit, a communications protocol
IDAC	current DAC
I/O	input/output, see also GPIO
LSDR	low-side driver
MCU	microcontroller unit
OCP	overcurrent protection
OVP	overvoltage protection
PD	power delivery
POR	power-on reset
PSoC™	programmable system-on-chip
PSM	pulse skipping mode
PWM	pulse-width modulator
RAM	random-access memory
SPI	serial peripheral interface, a communications protocol
SRAM	static random access memory
TCPWM	timer/counter/PWM
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UART	universal asynchronous transmitter receiver, a communications protocol
UFP	upstream facing port
UVP	undervoltage protection
USB	universal serial bus
UVLO	under-voltage lockout
VPA	VCONN powered accessories
ZCD	zero crossing detector

10 Document conventions

10.1 Units of measure

Table 56 Units of measure

Symbol	Unit of measure
°C	degrees celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kilo-ohm
Mbps	megabits per second
MHz	megahertz
MΩ	megaohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
mΩ	milliohm
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second

Revision history

Document revision	Date	Description of changes
*F	2023-01-30	Post to external web.
*G	2023-03-08	Updated Apple Charging version to 3 A. Updated **Table 2**. Updated **Figure 23**. Updated **Table 10**. Updated **Table 50**.
*H	2024-06-24	Updated Document Title to read as “CYPD7191, CYPD7199, EZ-PD™ CCG7S Automotive single-port USB Type-C with PD and buck-boost controller”. Updated **Pin list**: Updated **Table 2**. Added **Table 5**. Updated **Applications**: Updated description. Updated to new template. Completing Sunset Review.
*I	2024-07-30	Updated to reflect correct metadata.

Document revision	Date	Description of changes
*J	2024-10-04	Updated Document Title to read as “CYPD7191, CYPD7199, EZ-PD™ CCG7S Automotive single-port USB Type-C with PD and buck-boost controller AEC-100 qualified”. Updated **Features**: Updated description. Updated **Functional overview**: Updated **USBPD subsystem**: Updated **USBPD physical layer**: Updated description. Updated **USBPD physical layer**: Updated **Figure 1** (Updated figure caption only). Updated **Buck-boost controller operation regions**: Updated **Boost region operation (VIN << VBUS)**: Updated **Figure 5**. Updated **EZ-PD™ CYPD719X programming and bootloading**: Updated **Programming the device flash over SWD interface**: Updated **Figure 13**. Updated **Applications**: Updated **Figure 17**. Updated **Figure 19**. Updated description. Updated **Figure 23**. Updated **Table 10**. Added **Figure 25**. Added **Table 11**. Updated **Ordering information**: Updated part numbers.

Document revision	Date	Description of changes
*K	2026-05-25	Removed Automotive from title and updated product code in the header to CYPD719x. As both CCG7SAF and CCG7SA4F datasheets are combined in this document, the following changes where done: Updated **General description**. Removed Automotive applications point in **Features** section. Added two sub-points under package feature in the section **Features**. Added **Figure 3**, **Figure 11**, **Figure 12**, **Figure 18**, **Figure 20**, **Figure 21**, **Figure 24**, **Figure 26**, **Figure 28**, **Figure 29**. Updated **Figure 1**, **Figure 13**, **Figure 22**. Added **Table 3**, **Table 4**, **Table 7**, **Table 8**, **Table 47**, **Table 51**, **Table 52**. Removed Pin column in **Table 5**, **Table 6**, **Table 9**, **Table 10**, **Table 11**. Updated **Table 12**, added ESD_HBM rows from CCG7SAF and CCG7SA4F datasheets. Updated **Table 49**, combined ordering information tables from CCG7SAF and CCG7SA4F datasheets. Updated sentences from extended to switching at few instances in section **High-side gate driver and low-side gate driver (HG/LG)**. Added paragraph after **Table 6**. Added and updated section **Application firmware update using bootloader**. Removed Figure 18, EZ-PD™ CCG7S head unit (HU) charger application diagram. Replaced **Logic block diagram** and **Functional block diagram**. Updated section **Application firmware update over I2C interface**. Added device name in figure caption(CYPD7197), in **Figure 12**. Removed R_G = 3.5 Ω condition at turn-on delay time in **Table 47**. Added heading, **Thermal** under **Table 48**. Changed PPS valid voltage operation range from 3.3 - 21 V to 5 - 21 V at **USBPD physical layer** section, **Figure 17** and **Figure 25**. Added **Figure 31** and **Figure 32**. Added section **CCGND**. Updated **Figure 9**, and figure caption of **Figure 30**.

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