AIROC™ Bluetooth® LE 5.4 MCU for Automotive

General description

Infineon's AIROC™ CYW89829 is a high-performance, ultra-low-power, and secure MCU + Bluetooth® LE platform designed specifically for automotive applications. It integrates a high-performance microcontroller with Bluetooth® LE 5.4 connectivity, high-performance analog-to-digital conversion for audio input, I2S/PCM, CAN, and LIN interfaces, along with other standard communication and timing peripherals.

CYW89829 features a high level of integration to minimize external components, reducing device footprint and implementation costs for Bluetooth® Low Energy solutions. With AEC-Q100 Grade-2 automotive qualification, it is an optimal solution for automotive use cases such as car access systems, battery management systems, automotive sensors, and other related applications.

CYW89829 also includes an integrated power amplifier with a 10 dBm RF output, enabling applications that demand a high link budget and robust RF performance.

Features

- **32-bit application core subsystem**:
  - 48/96 MHz Arm® Cortex®-M33 CPU with single-cycle multiply and memory protection unit (MPU)
  - ARMv8-M architecture
  - CMOS 40-nm process
  - User-selectable core logic operation at either 1.1 V or 1.0 V
  - Active CPU current slope with 1.1 V core operation: Cortex®-M33: 40 µA/MHz
  - Active CPU current slope with 1.0 V core operation: Cortex®-M33: 22 µA/MHz
  - Datawire (DMA) controller with 16 channels
  - 32 KB cache for improved XIP performance with lower power
- **Memory subsystem**:
  - 256 KB SRAM with power and data retention control
  - OTP eFuse array for security provisioning
- **Bluetooth® Low Energy subsystem**:
  - 48-MHz Arm® Cortex®-M33 CPU with 2.4 GHz RF transceiver with 50 Ω antenna drive
  - Digital PHY
  - Link layer engine supporting master and slave modes
  - Programmable TX power: Up to 10 dBm
  - **RX sensitivity**:
    - LE-1 Mbps: –98 dBm
    - LE-2 Mbps: –95 dBm
    - Coded PHY 500 kbps (LE-LR): –101 dBm
    - Coded PHY 125 kbps (LE-LR): –106 dBm
  - Current consumption with 3.0 V supply and internal buck converter:
    - 5.2 mA TX (0dBm)
    - 17.2 mA TX (10 dBm)
    - 5.6 mA RX (LE 1 Mbps)
  - CYW89829 link layer engine supports up to 16 connections in any combination of central and peripheral devices simultaneously, for example, 13 central devices and three peripheral devices, or three central devices and 13 peripheral devices
  - Angle of Arrival (AoA) and Angle of Departure (AoD)[1)]

[1] End users interested in AoA/AoD solutions (such as RTLS, Direction Finding, and more) must develop or obtain licenses for various system components to realize the final solution

Features

- **Low-power operation**:
  - Operates from 1.7 V to 3.6 V
  - Six power modes for fine-grained power management
  - Deep Sleep mode current of 4.6 µA with 64 KB SRAM retention
  - On-chip DC-DC buck converter
- **Flexible clocking options**:
  - 8-MHz internal main oscillator (IMO) with ±2% accuracy
  - Ultra-low-power 32-kHz internal low-speed oscillator (ILO)
  - Two oscillators: High-frequency (24-MHz) for radio PLL and low-frequency (32-kHz watch crystal) for LPO
  - 48 MHz low-power IHO (internal oscillator)
  - Frequency-locked loop (FLL) for multiplying IMO frequency
  - Integer and fractional peripheral clock dividers
- **Quad SPI (QSPI)/serial memory interface (SMIF)**:
  - eXecute-In-Place (XIP) from external quad SPI flash
  - On-the-fly encryption and decryption
  - Support for DDR
  - Supports single, dual, and quad interfaces with throughput up to 384 Mbps
- **Serial communication**:
  - Three run-time configurable serial communication blocks (SCBs):
    - **First SCB**: Configurable as SPI or I^2C
    - **Second SCB**: Configurable as SPI or UART
    - **Third SCB**: Configurable as I^2C or UART
  - Only one protocol is supported by an SCB at a time, and up to two SCBs can be used simultaneously
- **Audio subsystem**:
  - Two pulse-density modulation (PDM) channels
  - One I2S channel with time-division multiplexed (TDM) mode
- **Timing and pulse-width modulation**:
  - Seven 16-bit and two 32-bit timer/counter pulse-width modulator (TCPWM) blocks, for MCU
  - Multiple PWMs to support applications such as color LEDs
  - PWM supports center-aligned, edge, and pseudo-random modes
- **ADC**: 12-bit sigma-delta switched capacitor ADC for DC measurements
- **GPIOs**
  - Up to 28 programmable GPIOs
  - Port 3 (six I/Os) enables Boolean operations on GPIO pins; available during system Deep Sleep
  - Programmable drive modes, strengths, and slew rates
  - Two overvoltage-tolerant (OVT) pins
  - Up to six GPIOs can be used for SMIF
- **Security**:
  - Built-in security architecture:
    - ROM-based root of trust via uninterruptible "Secure Boot"
    - Step-wise authentication of execution images
    - Secure execution of code in execute-only mode for protected routines
    - All debug and test ingress paths can be disabled
    - Up to four protection contexts (one is available for customer code)
    - Secure debug support via authenticated debug token
    - Encrypted image support for external SMIF memory

- **Cryptography hardware**:
  - Hardware acceleration for symmetric cryptographic methods and hash functions
  - True random number generation (TRNG)
- **Packages**: 48-lead QFN, 7.0 × 7.0 × 0.9 mm height with 0.5 mm pitch (AEC-Q100 Grade-2 certified)

Eclipse IDE for ModusToolbox™

ModusToolbox™ is Infineon's comprehensive collection of multi-platform tools and software libraries designed to provide an immersive development experience for creating converged MCU and wireless systems. It is:

- **Comprehensive**: Includes all necessary resources for development
- **Flexible**: Allows seamless integration of resources into any workflow
- **Atomic**: Enables selection and use of only the required resources

Infineon offers a robust collection of code repositories on GitHub, which includes:

- **Board Support Packages (BSPs)**: Aligned with Infineon kits for ease of use
- **Low-level resources**: Includes a Hardware Abstraction Layer (HAL) and Peripheral Driver Library (PDL)
- **Middleware**: Industry-leading features like Bluetooth® Low Energy and mesh networks
- **Code examples**: A wide array of thoroughly tested example applications

***Note**: The HAL provides a high-level, simplified interface for configuring and utilizing hardware blocks on Infineon MCUs and SoCs. It is a generic interface that works across multiple product families. Developers can use the generic HAL interface for most of an application while retaining the ability to implement fine-grained control where needed.*

ModusToolbox™ software is IDE-neutral and easily adapts to any workflow or preferred development environment. It includes:

- Project Creator
- Library Manager
- BSP Assistant
- Peripheral and Library configurators
- Optional Eclipse IDE (for ModusToolbox™ software as shown in Figure 1)

For detailed information on using Infineon tools, refer to the documentation provided with ModusToolbox™.

Eclipse IDE for ModusToolbox™

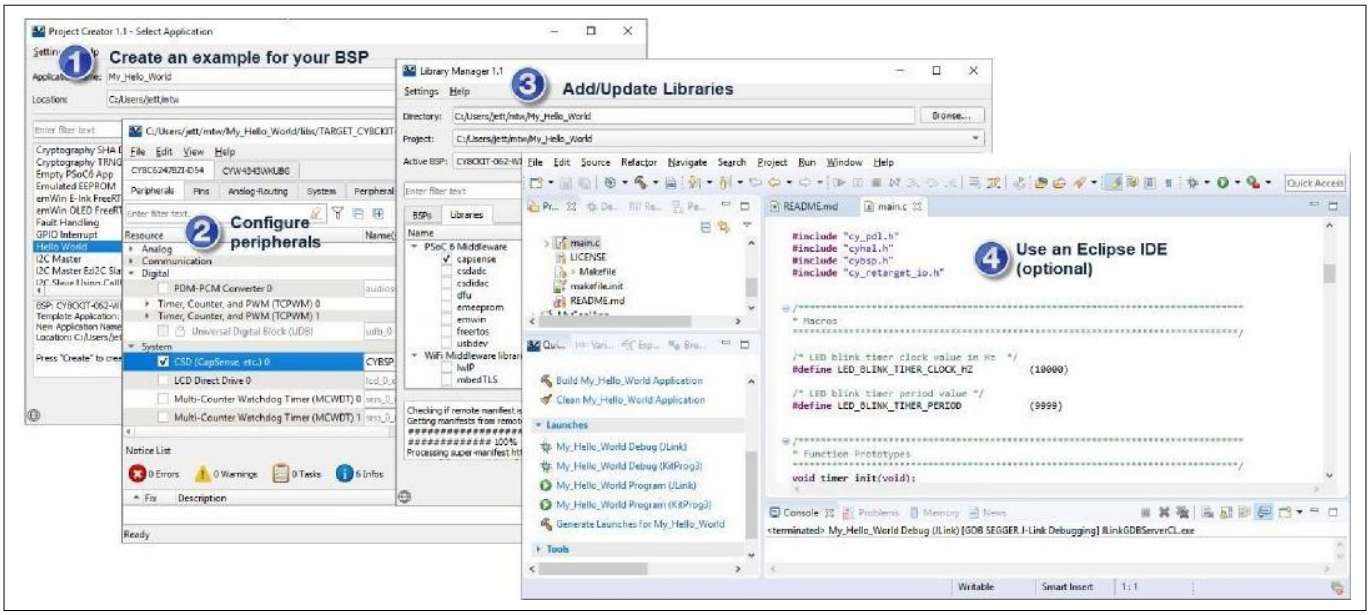

Figure 1 ModusToolbox™ tools

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1 Block diagram

Figure 2 provides an overview of the major subsystems and a simplified representation of their interconnections. Color coding is used to indicate the lowest power mode in which each block remains operational. For instance, the SRAM remains functional even in DS-RAM mode.

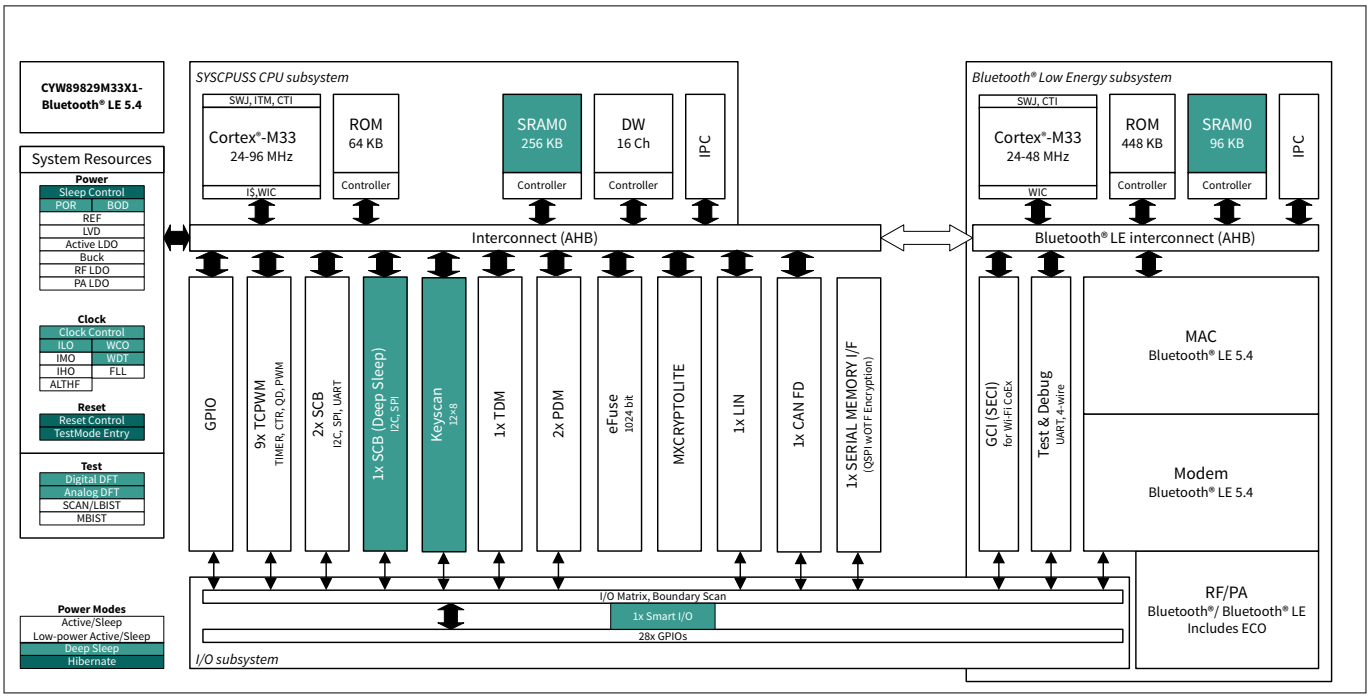


Figure 2 Functional block diagram

AIROC™ CYW89829 devices offer extensive support for programming, testing, debugging, and tracing of both hardware and firmware. For applications requiring enhanced security, all device interfaces can be permanently disabled to prevent attacks from maliciously reprogrammed devices. When maximum device security is enabled, all programming, debug, and test interfaces are fully disabled. The security level is configurable by the user.

The devices include complete debug-on-chip functionality, enabling full debugging within the final system using the standard production device. This functionality does not require special interfaces, debugging ports, simulators, or emulators. Standard programming connections are sufficient to support complete debugging.

The Eclipse IDE for ModusToolbox™, along with other integrated development environments (IDEs), provides fully integrated programming and debugging support for these devices. The SWJ (SWD and JTAG) interface is fully compatible with industry-standard third-party debug probes.

By combining debug features that can be disabled, robust flash protection, and support for customer-proprietary functionality in on-chip programmable blocks, the CYW89829 delivers an exceptional level of security.

2 Functional description

The following sections provide an overview of the features, capabilities, and operation of each functional block identified in Figure 2. For more detailed information, see the corresponding documentation:

- **Board Support Package (BSP) documentation**: BSPs are available on GitHub. They are aligned with Infineon kits and include files for basic device functionality, such as hardware configuration files, startup code, and linker files. The BSP also provides additional libraries required to support a specific kit. Each BSP comes with its own documentation, which typically includes an API reference, as shown in CY8CPROTO-062-4343W BSP. To find all currently available BSPs, use the search functionality on the Infineon GitHub site
- **Hardware Abstraction Layer(HAL) API reference manual**: Infineon's HAL offers a high-level interface for configuring and utilizing hardware blocks on Infineon microcontrollers. It provides a generic interface applicable across multiple product families. HAL simplifies application development by offering a consistent and generic interface for most use cases, even when certain portions of the application require more detailed control. For more information, see HAL API reference. Example applications that use the HAL automatically download it from the GitHub repository

2.1 CPU and memory subsystem

The AIROC™ CYW89829 MCU has multiple bus masters, as shown in Figure 2. These bus masters include the CPU, Datawire, QSPI, and a Crypto block. In general, all memory and peripherals are accessible and shared by all bus masters through multi-layer Arm® AMBA High-Performance Bus (AHB) arbitration.

Additionally, an interprocessor communication (IPC) block facilitates communication between the CPU and the Bluetooth® LE subsystem.

2.1.1 CPU

Cortex®-M33 features single-cycle multiplication and a Memory Protection Unit (MPU). It operates at up to 96 MHz in Low-Power (LP) mode and 48 MHz in Ultra-Low-Power (ULP) mode. This is the primary CPU, designed for short interrupt response time, high code density, and high throughput.

Cortex®-M33 implements a version of the Thumb instruction set based on Thumb-2 technology, as defined in the Armv8-M architecture reference manual. In addition to its high-performance capabilities, the main MCU incorporates device-level security, safety, and protection features.

Cortex®-M33 also provides a secure and interruptible boot function. This ensures that post-boot, system integrity is verified, and memory and peripheral access privileges are strictly enforced.

The CPU has the following power consumption when operating at V_{DDD} = 3.0 V with the internal buck regulator in use.

Table 1 Active current slope at V_{DDD} = 3.0 V using the internal buck regulator

System power mode		
CPU	ULP	LP
	22 µA/MHz	40 µA/MHz

The CPU can be selectively placed into Sleep and Deep Sleep power modes, as defined by Arm®. It also supports a Deep Sleep RAM (DS-RAM) mode, in which almost all circuits, except for RAM, are powered OFF. Data in RAM is retained to maintain the system state. Upon exiting DS-RAM mode, the CPU undergoes a reset but can use the retained data in RAM to bypass software initialization.

The CPU is equipped with nested vectored interrupt controllers (NVIC) for rapid and deterministic interrupt responses, as well as wakeup interrupt controllers (WIC) to enable CPU wakeup from Deep Sleep mode.

CYW89829 includes a debug access port (DAP), which serves as the interface for device programming and debugging. An external programmer or debugger (the “host”) communicates with the DAP via either the Serial Wire Debug (SWD) or Joint Test Action Group (JTAG) interface pins. Through the DAP, and subject to device security restrictions, the host can access the device memory, peripherals, and CPU registers.

The CPU includes several debug and trace features, such as:

- Six hardware breakpoints and four watchpoints
- Serial Wire Viewer (SWV) for data trace
- Printf()-style debugging via the Single Wire Output (SWO) pin

2.1.2 Interrupts

The CPU has interrupt request lines (IRQ), where each interrupt source, designated as ‘n,’ is directly connected to IRQn.

Each interrupt supports eight configurable priority levels, allowing flexible prioritization of interrupt handling. Additionally, one system interrupt can be mapped to the non-maskable interrupt (NMI) of the CPU, ensuring immediate response to critical events.

Multiple interrupt sources are capable of waking the device from Deep Sleep power mode using the WIC.

2.1.3 Datawire

Datawire is a lightweight DMA controller with 16 channels that enable CPU-independent access to memory and peripherals. The channel descriptors are stored in SRAM, and the number of descriptors is limited only by the available memory size. Each descriptor supports data transfer in two nested loops, with configurable address increments for both the source and destination.

2.1.4 Cryptography accelerator (Cryptolite)

A combination of hardware and software supports a wide range of cryptographic functions. Specifically, the following functions are supported:

- **Encryption/decryption**:
  - AES-128 hardware accelerator with the following operating modes:
    - Electronic Code Book (ECB)
    - Cipher Block Chaining (CBC)
    - Cipher Feedback (CFB)
    - Output Feedback (OFB)
    - Counter (CTR
- **Hashing**:
  - Secure Hash Algorithm (SHA-256) hardware accelerator
- **Message Authentication Functions (MAC)**:
  - Hashed Message Authentication Code (HMAC) acceleration using the SHA-256 hardware accelerator
- True Random Number Generator (TRNG)
- Vector unit hardware accelerator
  - RSA-based digital signature verification
  - ECDSA-based digital signature verification

2.1.5 Protection units

CYW89829 includes multiple protection mechanisms to control erroneous or unauthorized access to memory and peripheral registers. Protection units are designed to manage memory and peripheral access attributes, including address range, read/write permissions, code/data separation, privilege level, secure/non-secure operation, and protection context.

These protection units are configured at the “Secure Boot” process to define access privileges and rights for bus masters and peripherals. Up to eight protection contexts are available, with "Secure Boot" operating in protection context 0. The "Secure Boot" sets access privileges for memory and system resources for each protection context, based on the bus master and code privilege level. Multiple protection contexts are available.

2.1.6 AES-128

The AES-128 component accelerates block cipher functionality. It supports forward encryption of a single 128-bit block using a 128-bit key. The SHA-256 component accelerates hash functionality. It enables message schedule calculation for a 512-bit message chunk and the processing of a 512-bit message chunk.

2.1.7 Vector unit (VU)

The VU component accelerates asymmetric key cryptography, such as RSA and ECC. It supports operations like large-integer multiplication and addition. The TRNG component is based on a set of ring oscillators and includes a hardware health monitor for enhanced reliability.

2.1.8 CAN FD

CYW89829 features a controller area network flexible data-rate (CAN FD) controller that supports a single CAN FD channel. All CAN FD controllers are compliant with the ISO 11898-1:2015 standard, and an ISO 16845:2015 certificate is available. The controller also fully implements the time-triggered CAN (TTCAN) protocol, as specified in ISO 11898-4, including TTCAN protocol levels 1 and 2, entirely in hardware.

All message-handling functions are managed by the RX and TX handlers. The RX handler performs message acceptance filtering, transfers received messages from the CAN core to the message RAM, and provides the receive-message status. The TX handler manages the transfer of transmit messages from the message RAM to the CAN core and provides the transmit-message status.

2.1.9 LIN

CYW89829 includes a local interconnect network (LIN) channel. Each channel supports the transmission/ reception of data according to the LIN protocol, compliant with the ISO 17987 standard. The LIN channel interfaces with an external transceiver through a three-pin interface, which includes an enable function, and supports both master and slave functionalities.

Each LIN block supports classic and enhanced checksum options, as well as break detection during message reception and wake-up signaling. Tasks such as break detection, sync field handling, checksum calculation, and error interrupt management are fully implemented in hardware for efficient and reliable operation.

2.1.10 RTC

The real-time clock (RTC) supports fields for Year/Month/Date, Day-of-Week, and Hour:Minute:Second. Both 12-hour and 24-hour formats are available. Additionally, automatic leap-year correction is implemented to ensure accurate date tracking.

2.1.11 Memory

CYW89829 includes SRAM, ROM, and eFuse memory blocks with distinct features and functionalities:

- **SRAM**:
  - The device features 256 KB of SRAM
  - Power control and retention granularity are provided in 64-KB blocks, enabling users to manage the amount of memory retained in Deep Sleep mode
  - Memory retention is not supported in Hibernate mode
- **ROM**:
  - A 64-KB ROM, also referred to as the Supervisory ROM (SROM), provides code (ROM Boot) for various system functions
  - The ROM primarily handles device initialization and security functions
  - ROM code executes in protection context 0
- **eFuse**:
  - The eFuse block is a one-time programmable (OTP) array with 1024 bits, reserved for system use such as storing Die ID, Device ID, initial trim settings, device lifecycle, and security configurations
  - Some bits are available for user programming to store security key information and hash values, ensuring device security
  - Each fuse is individually programmable and, once programmed (or “blown”), its state is irreversible. A blown fuse transitions from the default state of ‘0’ to ‘1’
  - To program an eFuse, VDDIO1 must be set to 2.5 V ± 5%
  - Since blowing an eFuse is irreversible, programming is recommended only during mass production under controlled factory conditions using Infineon-provided provisioning tools

2.1.12 Boot code

On a device reset, the boot code in the ROM is the first code to execute. This code performs several critical functions, including:

- Device trim setting (calibration)
- Configuration of device protection units
- Establishes device access restrictions based on the secure life-cycle state
- Configures the Debug Access Port (DAP)
- Enables secure debugging via an authenticated debug token during the secure lifecycle stage
- Validates the first user code in external flash by checking its digital signature
- Supports On-The-Fly (OTF) decryption of encrypted images stored in external flash for secure execution
- Copies the application bootstrap from external flash to SRAM and transfers execution control to it

***Note**: The ROM code cannot be modified and serves as the Root of Trust (RoT) in a secure system and sets the system clock to a 48 MHz internal high-speed oscillator (IHO) source.*

2.1.13 Memory map

The 32-bit (4 GB) address space is divided into specific regions as shown in Table 2. Code execution is supported from both the Code region and the External RAM region.

Table 2 Address map

Address range	Name	Use
0x0000 0000 to 0x1FFF FFFF	Code	The Program Code region includes the exception vector table, which begins at address 0.
0x2000 0000 to 0x3FFF FFFF	SRAM	Data region
0x4000 0000 to 0x5FFF FFFF	Peripheral	This region contains all peripheral registers. • Code execution is not supported in this region • Bit-banding is also not supported in this region
0x6000 0000 to 0x8FFF FFFF	External NVM	SMIF/Quad SPI (see Serial Memory Interface (SMIF)). Codes can be executed from this region.
0xA000 0000 to 0xDFFF FFFF	External Device	Not used
0xE000 0000 to 0xE00F FFFF	Private Peripheral Bus	Provides access to peripheral registers within the CPU core.
0xE010 0000 to 0xFFFF FFFF	Device	Device-specific system registers

The device memory map is shown in Table 3.

Table 3 Internal memory address map

Address range	Memory type	Size
0x0000 0000 to 0x0001 0000	ROM	64 KB
0x2000 0000 to 0x 2004 0000	SRAM	Up to 256 KB

3 System resources

3.1 Power system

The power system ensures that voltage levels meet the requirements for each respective operating mode. It provides the following capabilities:

- **Mode entry assurance**: The system may delay mode entry (for example, during power-on reset (POR)) until voltage levels are adequate for proper operation
- **Reset generation**: When the power supply drops below specified voltage levels (brown-out detect (BOD)), resets are generated to ensure safe operation
- **Safe operation guarantee**: The system ensures safe chip operation between the point where the power supply voltage drops below specified levels (for example, below 1.7 V) and the reset is triggered

There are no voltage sequencing requirements for CYW89829. However, the device does not support power-on reset (POR) or brown-out detect (BOD) to guarantee the required voltage for eFuse programming.

The V_{DDD} supply (1.7 V to 3.6 V) powers an on-chip buck regulator that provides a selectable core operating voltage (V_{CCD}) of 1.0 V or 1.1 V. This selection allows users to choose between two system power modes based on power and performance requirements:

1. **System Low-Power (LP) mode**:
   - Operates V_{CCD} at 1.1 V
   - Offers high performance with no restrictions on device configuration
2. **System Ultra-Low-Power (ULP) mode**:
   - Operates V_{CCD} at 1.0 V
   - Delivers exceptional power efficiency but imposes limitations on clock speeds

The Bluetooth® radio requires 1.1 V for operation. When the radio is turned on, the Bluetooth® system overrides the user-selected core voltage to ensure proper functionality. Once Bluetooth® radio activity is complete, the system voltage automatically reverts to the user-selected value. See Power supply considerations for more details.

3.1.1 Power modes

CYW89829 supports four system power modes and three CPU power modes, designed to minimize average power consumption during application operation. For detailed information on power modes and additional power-saving configurations, see the relevant application note.

The following power modes are supported by CYW89829, listed in the order of decreasing power consumption:

1. **System Low power (LP)**: All peripherals and CPU power modes are available at maximum speed for high performance
2. **System Ultra-Low-Power (ULP)**: All peripherals and CPU power modes are available, but with reduced speed for improved power efficiency
3. **CPU Active**: The CPU executes code while the system operates in LP or ULP mode
4. **CPU Sleep**: CPU code execution is halted, but the system remains in LP or ULP mode
5. **CPU Deep Sleep**: CPU code execution is halted, and the system transitions to Deep Sleep mode while in LP or ULP mode
6. **System Deep Sleep**: Only low-frequency peripherals remain active after both CPUs enter Deep Sleep mode
7. **Deep Sleep RAM**: RAM and I/O states are retained, while all other system activity stops. Upon exit, the CPU resets but skips software initialization since RAM content is preserved
8. **System Hibernate**: Device and I/O states are frozen. The device resets upon waking up

CPU Active, Sleep, and Deep Sleep are standard Arm®-defined power modes supported by the Arm® CPU instruction set architecture (ISA). Additionally, CYW89829 supports System Low-Power (LP), System Ultra-Low-Power (ULP), System Deep Sleep, Deep Sleep RAM, and System Hibernate as enhanced low-power modes.

3.1.2 CYW89829 clock system

The CYW89829 clock system consists of a combination of oscillators, an external clock, and a frequency-locked loop. Specifically, it includes the following components:

- Internal main oscillator (IMO)
- Internal low-speed oscillator (ILO)
- Watch crystal oscillator (WCO)
- System 24-MHz crystal oscillator
- External clock input
- One frequency-locked loop (FLL)
- Internal high-speed oscillator (IHO)

Clocks may be buffered and routed to a pin on a Smart I/O port. The mapping of ports and associated clock groups to peripherals are shown in Table 4.

Table 4 Mapping of clock groups to peripherals

PCLK group	Root clock (clk_hf)	Peripherals	Frequency		Description
			LP (1.1 V typ)	ULP (1.0 V typ)	
0	clk_hf0	CPU Trace	24 MHz	24 MHz	–
1	clk_hf1	SCB	96 MHz	48 MHz	**Asynchronous peripherals**: Strobe signals are driven through dividers, and the interface clock is generated within the peripheral using the main group clock.
		TCPWM			
		LIN			
		CANFD			
		SMARTIO			
2	clk_hf0	SMIF	96 MHz	48 MHz	The clock is directly connected and passed through from clk_hf. This clock is not used as an interface clock; rather, it is utilized for the MMIO clocks of BTSS and CRYPTO. BTSS uses this clock for both master and slave AHB/ MMIO transactions.
		BTSS			
		CRYPTO			
3	clk_hf1	PDM	96 MHz	48 MHz	The peripheral uses PERI_ACLK with a default divide-by-2 configuration. The required interface

(table continues...)

Table 4 (continued) Mapping of clock groups to peripherals

PCLK group	Root clock (clk_hf)	Peripherals	Frequency		Description
			LP (1.1 V typ)	ULP (1.0 V typ)	
		TDM			frequencies are generated by further division within the peripheral itself.
4	clk_hf2	BTSS	48 MHz	48 MHz	RPU clock for BTSS
5	clk_hf3	ADCMIC	24 MHz	24 MHz	The ADCMIC has a direct connection, and its main clock source (clk_hf3) is derived from clk_althf, which is the BTSS ECO clock.
6	clk_hf1	SMIF	96 MHz	48 MHz	There is a direct connection for the SMIF and SMARTIO peripherals. This clock serves as the interface clock for these peripherals.

3.1.3 Internal main oscillator (IMO)

The internal main oscillator (IMO) is the primary source of internal clocking. It is calibrated during testing to ensure the specified accuracy. The default frequency of the IMO is 8 MHz, with a tolerance of ±2%.

3.1.4 Precision internal low-speed oscillator (PILO)

The precision internal low-speed oscillator (PILO) is a precision, low-power oscillator operating at 32 kHz. It is factory-calibrated to meet Bluetooth® LE requirements. Similar to the internal low-speed oscillator (ILO), the PILO can function in all power modes.

3.1.5 Internal low-speed oscillator (ILO)

The internal low-speed oscillator (ILO) is a very low-power oscillator with a nominal frequency of 32 kHz. It operates in all power modes.

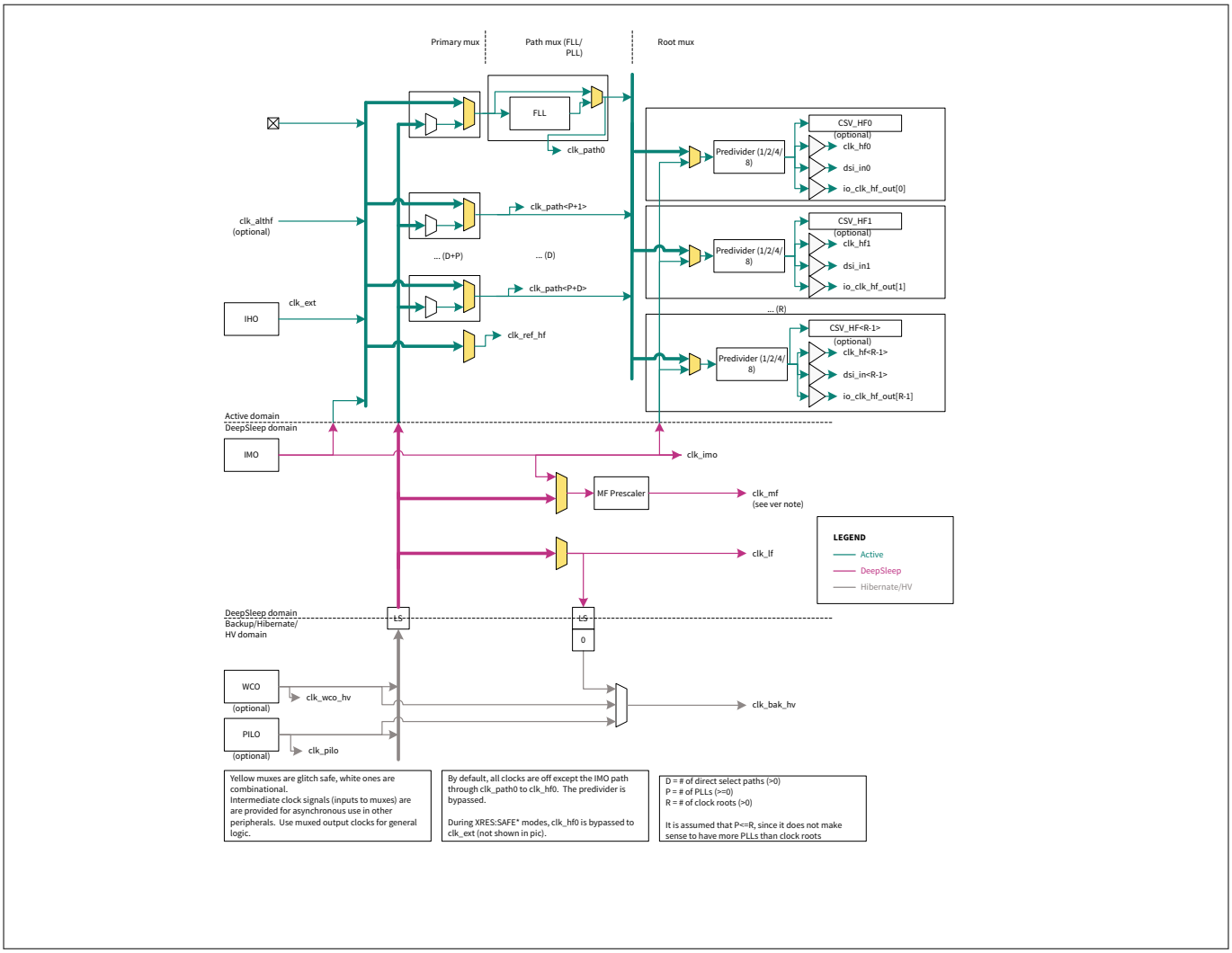


Figure 3 CYW89829 clocking diagram with corresponding oscillators

***Note**: Using the PILO as the clock source for the ILO will result in longer boot time.*

3.2 Main crystal oscillator

CYW89829 uses a 24 MHz crystal oscillator (XTAL). The XTAL must meet the accuracy requirements defined by the Bluetooth® specification. To operate with the crystal oscillator, two external load capacitors are required. The selection of these load capacitors depends on the specific XTAL being used. For more details, see Figure 4.

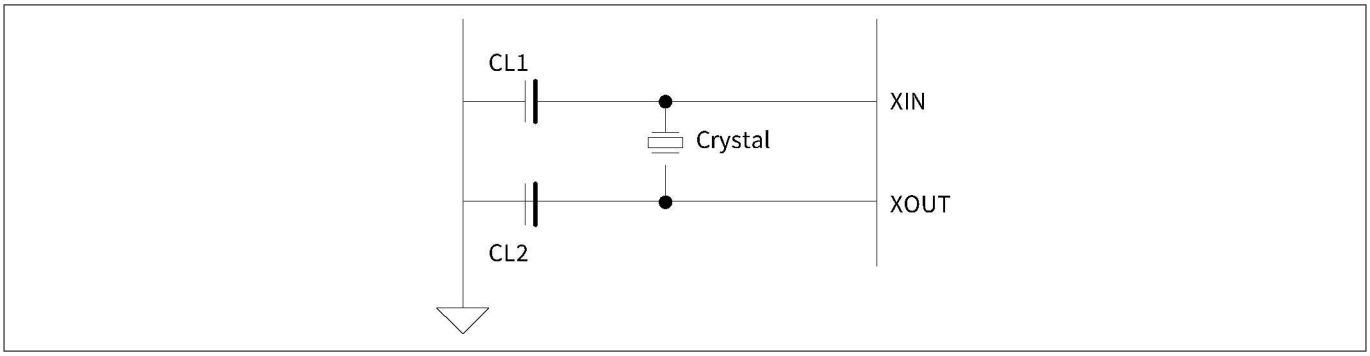


Figure 4 Recommended oscillator configuration

Table 5 Reference crystal electrical specifications

Parameter	Symbol	Electrical specification				Note
		Values				
		Min	Typ	Max	Unit	
Nominal frequency	FL	24			MHz	–
Oscillation mode	–	Fundamental			–	–
Load capacitance	CL	8			pF	–
Frequency tolerance	–	±10			ppm	at 25°C ± 3°C
Frequency stability	–	± 20			ppm	Over operating temperature range (reference 25°C)
Operating temperature	–	–40	–	105	°C	–
Aging	–	±3			ppm	First year at 25°C ± 3°C
Drive level	DL	–	100	200	uW	–
Series resonant resistance	Rr	–	–	60	Ω	–
Shunt capacitance	C0	–	–	3	pF	–
Insulation resistance	–	500	–	–	MΩ	At DC 100 V
Storage temperature range	–	–40	–	125	°C	–

3.3 32 kHz crystal oscillator

CYW89829 includes a 32 kHz oscillator designed to provide accurate timing during low-power operations. Figure 5 shows the 32 kHz XTAL oscillator with external components and Table 6 lists the characteristics of the oscillator. This oscillator can operate with either a 32 kHz or 32.768 kHz crystal oscillator, or it can be driven by a clock input at a similar frequency. The XTAL must meet an accuracy of ±250 ppm or better, as specified by the Bluetooth® requirements, accounting for variations due to temperature and aging.

The default component values for the external load capacitors are:

- C1 = ~6 pF
- C2 = ~6 pF

These capacitor values are used to fine-tune the oscillator.

***Note**: The 32.768-kHz crystal is optional and can be omitted. CYW89829 includes an internal PILO.*

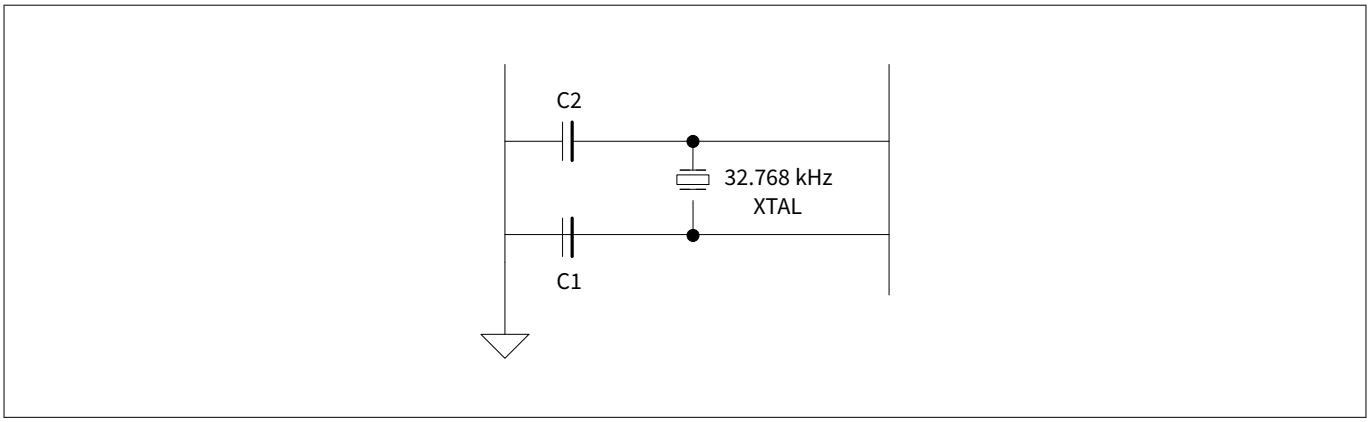


Figure 5 32 kHz oscillator block diagram

Table 6 XTAL oscillator characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output frequency	F_{oscout}	–	–	32.768	–	kHz
Frequency tolerance	–	Over temperature and aging	–	–	250	ppm
XATL driver level	P_{drv}	For crystal selection	–	0.1	0.5	µW
XTAL series resistance	R_{series}	For crystal selection	–	–	70	KΩ
XATL shunt capacitance	C_{shunt}	For crystal selection	–	–	2.2	pF

3.3.1 Watchdog timers (WDT, MCWDT)

CYW89829 includes one watchdog timer (WDT) and two multi-counter watchdog timers (MCWDTs). The WDT features a 16-bit free-running counter. Each MCWDT has two 16-bit counters and one 32-bit counter, supporting multiple operating modes. All 16-bit counters can generate a watchdog reset, while all counters (16-bit and 32-bit) can generate an interrupt on a match event.

The WDT is clocked by the ILO and supports interrupt or wakeup generation in System LP, ULP, Deep Sleep, and Hibernate power modes. The MCWDTs are clocked by the low-frequency clock (LFCLK), which can be sourced from either the ILO or the WCO. The MCWDTs support periodic interrupt or wakeup generation in system LP, ULP, and Deep Sleep power modes.

3.3.2 Clock dividers

Integer and fractional clock dividers are available for peripheral use and timing purposes. These include one or more of the following:

- 8-bit clock dividers
- 16-bit integer clock dividers
- 16.5-bit fractional clock dividers
- 24.5-bit fractional clock dividers

3.3.3 Trigger routing

CYW89829 includes a trigger multiplexer block, which consists of digital multiplexers and switches used for routing trigger signals between peripheral blocks, as well as between GPIOs and peripheral blocks.

There are two types of trigger routing:

1. **Trigger multiplexers**: These provide reconfigurability in selecting the source and destination of trigger signals
2. **One-to-one triggers**: These are hardwired switches that directly connect a specific source to a specific destination

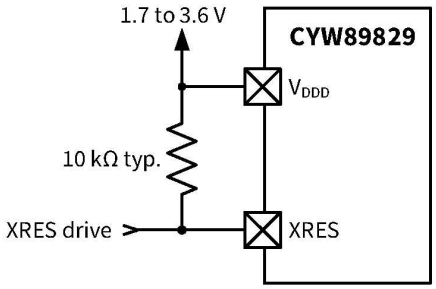
The user can enable or disable the routes as required.

3.3.4 Reset

CYW89829 can be reset from a variety of sources, including the following:

- **Power-on reset (POR)**: The POR holds the device in reset while the power supply ramps up to the level required for proper operation. It activates automatically during power-up
- **Brown-out detect (BOD) reset**: The BOD reset monitors the digital voltage supply (*VDDD*) and generates a reset if *VDDD* falls below the minimum required logic operating voltage
- **External reset pin (XRES)**: The XRES pin is a dedicated input for resetting the device using an external source. It is Active LOW and can be connected either to a pull-up resistor tied to V_{DDD} or to an active drive circuit. If a pull-up resistor is used, its value should be selected to minimize current draw when the pin is pulled LOW; a 10 kΩ resistor is typical

Figure 6 XRES connection diagram



- **Watchdog timer (WDT or MCWDT)**: Resets the device if the firmware fails to service it within a specified timeout period
- **Software-initiated reset**: Resets the device on demand using firmware
- **Logic-protection fault**: Triggers an interrupt or resets the device if unauthorized operating conditions occur, such as reaching a debug breakpoint while executing privileged code
- **Hibernate wakeup reset**: Brings the device out of the system Hibernate Low-power mode

Reset events are asynchronous and ensure that the system reverts to a known state. Some reset sources are recorded in a register that is retained through a reset, allowing software to determine the cause of the reset.

3.4 Bluetooth® LE radio and subsystem

CYW89829 incorporates a Bluetooth® 5.4 LE subsystem, which includes the physical layer (PHY) and link layer (LL) engines, along with an embedded security engine. The Bluetooth® LE subsystem supports all Bluetooth® 5.4 features, including:

- LE 2 Mbps
- LE Long range (500 and 125 kbps)

- LE Advertising extensions
- LE Isochronous channels
- Periodic Advertising with Responses (PAwR)
- Encrypted advertising data
- LE GATT Security levels characteristic
- Advertising coding selection

Infineon also provides an extensive driver library and middleware support for Bluetooth® LE. For more details, see Eclipse IDE for ModusToolbox™.

The physical layer comprises a digital PHY and an RF transceiver that transmits and receives Gaussian frequency shift keying (GFSK) packets at 1 Mbps or 2 Mbps over the 2.4 GHz ISM band. The device supports Bluetooth® LE long range at both 500 kbps and 125 kbps speeds.

The baseband controller is a hybrid hardware and firmware implementation, supporting both master and slave modes. Key protocol elements, such as host controller interface (HCI) and link control, are implemented in firmware. Time-critical functions, including encryption, CRC, data whitening, and access code correlation, are implemented in hardware within the LL engine.

The RF transceiver includes an integrated balun, which provides a single-ended RF port pin to drive a 50 Ω antenna via a matching and filtering network. In the receive direction, the transceiver converts the RF signal from the antenna into a digital bit stream after performing GFSK demodulation. In the transmit direction, it performs GFSK modulation and converts the digital baseband signal into a radio frequency, which is then transmitted through the antenna.

3.5 Programmable analog-to-digital converter (ADC)

3.5.1 Sigma delta ADC

The ADC block consists of a single switched-capacitor Σ-Δ (sigma-delta) ADC core designed for DC measurement. It operates at a clock rate of 12 MHz and has seven GPIO inputs. The internal bandgap reference provides ±5% accuracy without calibration. Various calibration and digital correction schemes can be applied to reduce the absolute error and improve DC measurement accuracy.

The ADC reference voltage can be derived from one of three internal sources:

- VDDA
- VDDA/2
- Analog reference (AREF)

The AREF is nominally 1.2 V and is trimmed to ±1% accuracy.

3.6 Programmable digital

- The system supports both asynchronous and synchronous (clocked) operation
- Deep Sleep operation can function in either mode, depending on the system requirements

3.7 Fixed-function digital

3.7.1 Timer/counter/pulse-width modulator (TCPWM) block

The TCPWM supports the following operational modes:

- Timer-counter with compare
- Timer-counter with capture

- Pulse width modulation (PWM)
- Pseudo-random PWM
- PWM with dead time

The TCPWM block also features:

- Up, down, and up/down counting modes
- Clock pre-scaling (division by 1, 2, 4, ... 64, 128)
- Double buffering of compare/capture and period values
- Underflow, overflow, and capture/compare output signals
- Complementary output for PWMs
- Selectable start, reload, stop, count, and capture event signals for each TCPWM, with options for rising edge, falling edge, both edges, and level triggers
- The TCPWM has a Kill input to force outputs into a predetermined state

Supports interrupts on:

- **Terminal count**: Depends on the mode and typically occurs on overflow or underflow
- **Capture/compare**: Occurs when the count is captured to the capture register or when the counter value matches the compare register

This device includes:

- Two 32-bit TCPWMs
- Seven 16-bit TCPWMs

3.7.2 Serial communication blocks (SCB)

This product line features three serial communication blocks (SCBs).[2]:

1. **First SCB**: Configurable as SPI or I²C
2. **Second SCB**: Configurable as SPI or UART
3. **Third SCB**: Configurable as I²C or UART

One SCB (SCB #0) is capable of operating in system Deep Sleep mode with an external clock. In this mode, it can function as either an SPI slave or an I²C slave.

I²C mode

The SCB implements a full multi-master and slave interface, supporting multimaster arbitration. It operates at speeds of up to 1 Mbps (Fast Mode Plus). Additionally, it supports EZI²C mode, which creates a mailbox address range and simplifies I²C communication by reducing it to reading and writing an array in memory.

The SCB includes a 256-byte FIFO for both receive and transmit operations. It is compatible with I²C Standard mode, Fast mode, and Fast Mode Plus devices. The I²C bus I/O is implemented using GPIO in open-drain modes.

UART mode

The UART is a full-featured module operating at speeds of up to 8 Mbps. It supports various protocols, including:

- Automotive single-wire interface (LIN)
- Infrared interface (IrDA)
- SmartCard (ISO 7816) protocols

These are minor variants of the basic UART protocol. The SCB also supports a 9-bit multiprocessor mode, enabling the addressing of peripherals connected over shared Rx and Tx lines. Common UART functions such as parity error detection, break detection, and frame error detection are supported. The module includes a 256-byte FIFO to tolerate longer CPU service latencies.

[2] Each SCB supports only one protocol at a time, and a maximum of two SCBs can be used simultaneously.

SPI mode

The SPI mode supports the following variants:

- Full SPI
- Secure Simple Pairing (SSP), which adds a start pulse for synchronizing SPI codecs
- Microwire, a half-duplex form of SPI

The SCB also supports EZSPI mode, simplifying data exchange by enabling memory array-based read and write operations. The SPI interface operates with a clock frequency of up to 24 MHz.

3.7.3 Serial Memory Interface (SMIF)

A Serial Memory Interface (SMIF) is provided, operating at speeds of up to 48 MHz. It supports single, dual, and quad SPI configurations and is capable of interfacing with up to four external memory devices. The interface offers two modes of operation:

1. **Memory-mapped I/O (MMIO)**: This is a command-mode interface that allows data access through the SMIF registers and FIFOs
2. **eXecute-in-Place (XIP)**: In this mode, AHB reads and writes are directly translated into SPI read and write transfers. The external memory is mapped into the CYW89829 internal address space, enabling code execution directly from the external memory

To enhance performance in XIP mode, a 32 KB cache is included. Additionally, XIP mode supports AES-128-based on-the-fly encryption and decryption. This ensures secure storage and secure access to code and data stored in external memory.

3.8 GPIO

CYW89829 supports up to 28 GPIOs, which implement:

- **Eight drive strength modes**:
  - Analog input mode (input and output buffers disabled) on some I/Os
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- **Hold mode**: Retains the previous state of the pin, used for maintaining the I/O state during system Hibernate and Deep Sleep modes
- **Selectable slew rates**: Allows control of dV/dt-related noise to improve EMI performance

The pins are organized into logical entities called 'ports', each consisting of up to seven pins. Data output and pin state registers store, respectively, the values to be driven on the pins and the input states of the pins. Every pin can generate an interrupt if enabled, and each port has an associated interrupt request (IRQ).

The Port 4 pins support overvoltage-tolerant (OVT) operation, allowing input voltages higher than VDDD. OVT pins are commonly used with I^2C to maintain a physical connection to an active I^2C bus even when the chip is powered off, without affecting bus functionality.

GPIO pins can be ganged together to source or sink higher current levels. However, GPIO pins, including OVT pins, must not be pulled up beyond their absolute maximum voltage rating. See Electrical specifications.

During power-on and reset, all pins are forced into the analog input drive mode, with input and output buffers disabled. This prevents crowbar currents and excessive turn-on currents. A multiplexing network, referred to as the High-Speed I/O Matrix (HSIOM), is used to route various peripheral and analog signals to GPIO pins.

To achieve optimal performance, certain frequency and drive mode constraints may be applied. The DRIVE_SEL values represent drive strengths. See Table 7 for more details.

Table 7 DRIVE_SEL values

Ports	Maximum frequency	Drive strength for V_{DDD} < 2.7 V	Drive strength for V_{DDD} > 2.7 V
Ports 0, 1	8 MHz	Up to 4 mA	Up to 8 mA
Ports 2 to 5	16 MHz; 24 MHz for SPI	Up to 4 mA	Up to 8 mA

3.9 Special-function peripherals

3.9.1 Audio subsystem

This subsystem consists of the following hardware blocks:

- One inter-IC sound (I2S) interface
- Two pulse-density modulation (PDM) to pulse-code modulation (PCM) decoder channels

I2S interface: The I2S interface implements two independent hardware FIFO buffers: TX and RX which can operate in master or slave mode. The following features are supported:

- **Multiple data formats**: I2S, left-justified, time division multiplexed (TDM) mode A, and TDM mode B
- **Programmable channel/word lengths**: 8, 16, 18, 20, 24, or 32 bits
- **Internal/external clock operation**: Supports sampling rates of up to 192 ksps (Kilosamples per second)
- **Interrupt mask events**: Trigger, not empty, full, overflow, underflow, and watchdog
- **Configurable FIFO trigger level**: Includes datawire support

The I2S interface is commonly used to connect with audio codecs and simple digital-to-analog converters (DACs).

PDM-to-PCM decoder: The PDM-to-PCM decoder implements a single hardware Rx FIFO that decodes a stereo or mono 1-bit PDM input stream into PCM data output. The following features are supported:

- **Configurable PDM clock generation**: Range from 384 kHz to 3.072 MHz
- **Programmable data output word length**: 16, 18, 20, or 24 bits
- **Droop correction and configurable decimation rate**: Supports sampling rates of up to 48 ksps
- Programmable high-pass filter gain
- **Interrupt mask events**: Not empty, overflow, trigger, and underflow
- **Configurable FIFO trigger level**: Includes DMA support

The PDM-to-PCM decoder is commonly used to connect to digital PDM microphones. It supports up to two microphones connected to the same PDM data line.

4 Pinouts

Table 8 Packages and pin information

Pin name	Pin number	I/O	Power domain	Description
	48-lead QFN			
Onboard switching regulator and LDOs				
VDDQ	11	I	–	External supply to PMU analog
VCC_BUCK	13		–	External supply to switching regulator
LX_BUCK	12	O	–	Switching regulator output
VCCD	14		–	Digital LDO output
VCCI	15	I	–	RF and digital LDO input
Baseband supply				
VDDIO_0	37	I	VDDIO_0	Supply for GPIO ports
VDDIO_1	45		VDDIO_1	Supply for GPIO ports and eFuse programming. See Table 11 for eFuse programming requirements.
VDDIO_A	4		VDDIO_A	Supply for analog GPIO ports
VDDA	46		VDDA	Analog power supply voltage
RF power supply				
VCCRF	16	O	–	RFLDO output
VDDD	18	I	–	PALDO and sub-system resources supply
VCCPA	17	O	–	PALDO output
BT_VCOVDD	23	I	BT_VCOVDD	VCO supply
BT_LNAIFVDD	22		BT_LNAIFVDD	LNA and IFPLL supply
BT_PLLVDD	24		BT_PLLVDD	RFPLL and crystal oscillator supply
BT_PAVDD	20		BT_PAVDD	Internal PA supply
Ground pins				
HS-VSS	Center pad	–	VSS	Ground
Radio I/O				
BT_RF	21	I/O	BT_RF	RF antenna port
Crystal				
BT_XTALI	25	I	BT_PLLVDD	The crystal oscillator input requires two external load capacitors to function. The selection of these load capacitors depends on the specific characteristics of the crystal oscillator (XTAL).
BT_XTALO	26	O		Crystal oscillator output

(table continues...)

Table 8 (continued) Packages and pin information

Pin name	Pin number	I/O	Power domain	Description
	48-lead QFN			
GPIO				
P0.0	27	I/O	VDDIO	General input and output port. See Table 9 for alternate functions.
P0.1	28			
P0.2	29			
P0.3	30			
P0.4	31			
P0.5	32			
P1.0	33			
P1.1	34			
P1.2	35			
P1.3	36			
P1.6	38			
P2.0	39			
P2.1	40			
P2.2	41			
P2.3	42			
P2.4	43			
P2.5	44			
P3.0	47			
P3.1	48			
P3.2	1			
P3.3	2			
P3.4	3			
P3.6	5			
P3.7	6			
P4.0	9			
P4.1	10			
P5.0/WCO_OUT	7			
P5.1/WCO_IN	8			
XRES	19	I	–	Active-low system reset without internal pull-up resistor.

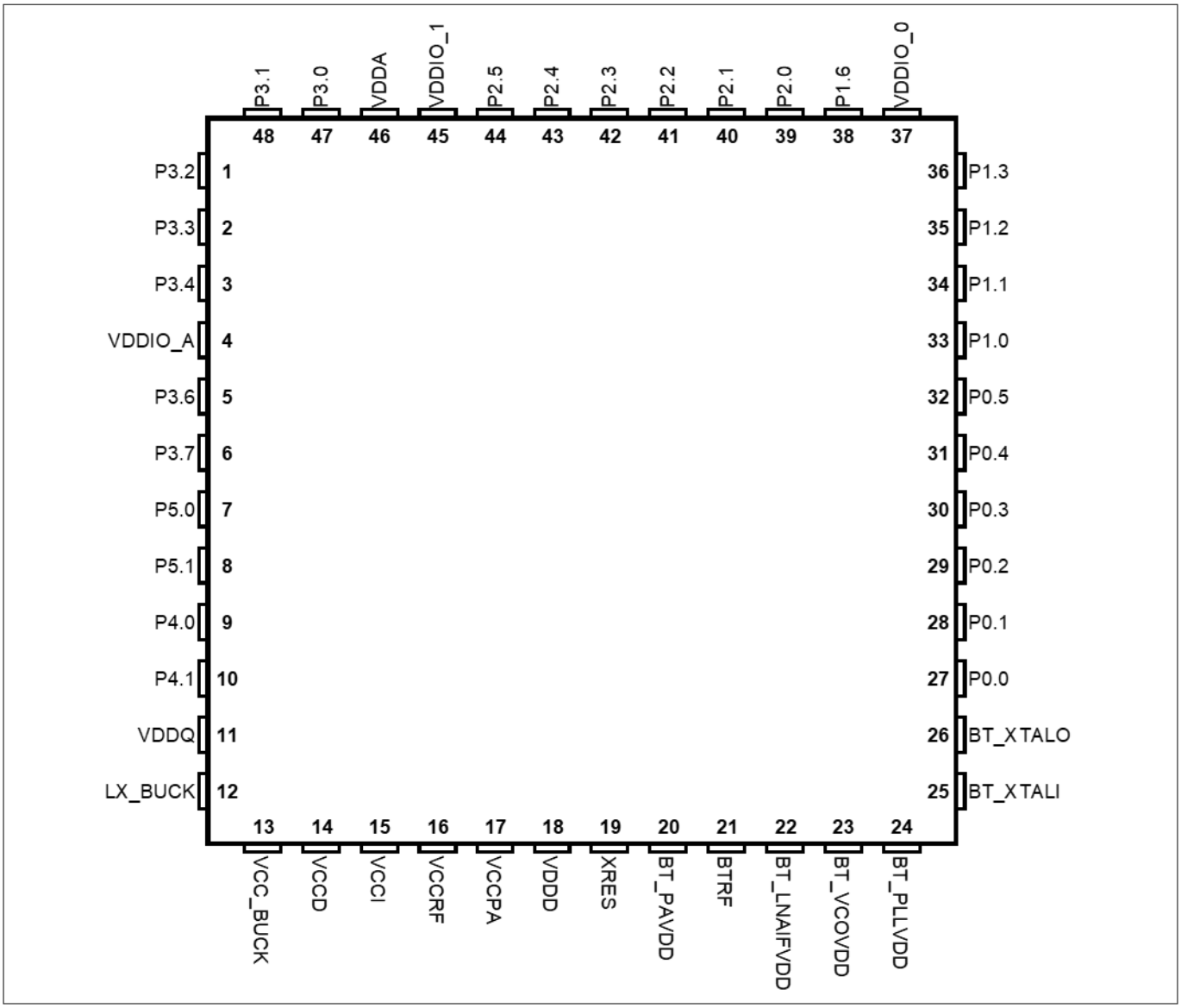


Figure 7 Device pinout for 48-lead QFN package

Each port pin has multiple alternate functions. These are defined in Table 9.

Table 9 Multiple alternate functions[1)]

Port/ Pin	Analog	ACT #0	ACT #1	ACT #2	ACT #3	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #11	ACT #12	ACT #13	ACT #15	DS #2	DS #3	DS #5	DS #6
P0.0	–	tcpwm[0].line_compl[0]:3	tcpwm[0].line_compl[262]:0	–	–	–	–	–	–	–	pdm.pdm_clk[1]:0	–	tdm.tdm_rx_mck[0]:0	–	–	keyscan.ks_col[3]	–	–	scb[0].spi_select1:0
P0.1	–	tcpwm[0].line[1]:3	tcpwm[0].line[256]:1	–	–	–	–	–	–	–	pdm.pdm_data[1]:0	–	tdm.tdm_rx_sck[0]:0	–	–	keyscan.ks_col[4]	–	–	scb[0].spi_select2:0
P0.2	–	tcpwm[0].line_compl[1]:3	tcpwm[0].line_compl[256]:1	–	–	–	–	–	–	–	pdm.pdm_clk[1]:0	–	tdm.tdm_rx_fsync[0]:0	–	–	keyscan.ks_col[11]	scb[0].i2c_scl:0	–	scb[0].spi_mosi:0
P0.3	–	tcpwm[0].line[0]:4	tcpwm[0].line[257]:1	–	–	–	–	–	–	scb[1].spi_select3:0	–	–	tdm.tdm_rx_sd[0]:0	–	–	keyscan.ks_col[12]	scb[0].i2c_sda:0	–	scb[0].spi_miso:0
P0.4	–	tcpwm[0].line_compl[0]:4	tcpwm[0].line_compl[257]:1	–	–	srss.ext_clk:0	cpuss.trace_data[3]:1	–	–	scb[1].spi_select2:0	–	–	tdm.tdm_tx_mck[0]:0	–	–	keyscan.ks_row[0]	–	–	scb[0].spi_clk:0

(table continues...)

Table 9 (continued) Multiple alternate functions[1)]

Port/ Pin	Analog	ACT #0	ACT #1	ACT #2	ACT #3	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #11	ACT #12	ACT #13	ACT #15	DS #2	DS #3	DS #5	DS #6
P0.5	–	tcpwm[0].line[1]:4	tcpwm[0].line[258]:1	btss.antenna_switch_ctrl[0]	–	–	cpuss.trace_data[2]:1	–	–	scb[1].spi_select1:0	–	–	tdm.tdm_tx_sck[0]:0	btss.gci_gpio[0]	smif.spihb_select1	keyscan.ks_row[1]	–	–	–
P1.0	–	tcpwm[0].line_compl[1]:4	tcpwm[0].line_compl[258]:1	btss.antenna_switch_ctrl[1]	btss.rpu_tdo	–	cpuss.trace_data[1]:1	scb[1].uart_cts:0	–	scb[1].spi_select0:0	pdm.pdm_clk[1]:1	–	tdm.tdm_tx_fsync[0]:0	btss.gci_gpio[1]	–	keyscan.ks_row[5]	–	cpuss.swj_swo_tdo	–
P1.1	–	tcpwm[0].line[0]:5	tcpwm[0].line[259]:1	btss.antenna_switch_ctrl[2]	btss.rpu_tdi	–	cpuss.trace_data[0]:1	scb[1].uart_rts:0	–	scb[1].spi_clk:0	pdm.pdm_data[1]:1	–	tdm.tdm_tx_sd[0]:0	btss.gci_gpio[2]:0	–	keyscan.ks_row[6]	–	cpuss.swj_swdoe_tdi	–
P1.2	–	tcpwm[0].line_compl[0]:5	tcpwm[0].line_compl[259]:1	–	btss.rpu_swd	–	cpuss.trace_clock:1	scb[1].uart_rx:0	scb[2].i2c_scl:1	scb[1].spi_mosi:0	–	–	–	btss.gci_gpio[3]	–	–	keyscan.ks_col[17]:0	cpuss.swj_swdio_tms	–
P1.3	–	tcpwm[0].line[1]:5	tcpwm[0].line[260]:1	–	btss.rpu_tck	srss.ext_clk:1	–	scb[1].uart_tx:0	scb[2].i2c_sda:1	scb[1].spi_miso:0	–	–	–	btss.gci_gpio[4]	–	–	keyscan.ks_col[16]:0	cpuss.clk_swj_swclk_tclk	–

(table continues...)

Table 9 (continued) Multiple alternate functions[1)]

Port/ Pin	Analog	ACT #0	ACT #1	ACT #2	ACT #3	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #11	ACT #12	ACT #13	ACT #15	DS #2	DS #3	DS #5	DS #6
P1.6	–	tcpwm[0].line_compl[0]:6	tcpwm[0].line_compl[261]:1	–	–	–	–	–	–	–	–	lin[0].lin_tx[1]:0	–	–	–	keyscan.ks_col[6]	srss.cal_wave	–	–
P2.0	–	–	–	–	–	–	–	–	–	–	–	–	–	–	smif.spihb_select0	–	–	–	–
P2.1	–	–	–	–	–	–	–	–	–	–	–	–	–	–	smif.spihb_data3	–	–	–	–
P2.2	–	–	–	–	–	–	–	–	–	–	–	–	–	–	smif.spihb_data2	–	–	–	–
P2.3	–	–	–	–	–	–	–	–	–	–	–	–	–	–	smif.spihb_data1	–	–	–	–
P2.4	–	–	–	–	–	–	–	–	–	–	–	–	–	–	smif.spihb_data0	–	–	–	–
P2.5	–	–	–	–	–	–	–	–	–	–	–	–	–	–	smif.spihb_clk	–	–	–	–

(table continues...)

Table 9 (continued) Multiple alternate functions[1)]

Port/ Pin	Analog	ACT #0	ACT #1	ACT #2	ACT #3	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #11	ACT #12	ACT #13	ACT #15	DS #2	DS #3	DS #5	DS #6
P3.0	adcmic.gpio_adc_in[0]	tcpwm[0].line[0]:0	tcpwm[0].line[256]:0	–	–	–	cpuss.trace_data[3]:0	scb[2].uart_cts:0	–	scb[1].spi_select0:1	–	–	–	–	–	keyscan.ks_row[7]	–	–	–
P3.1	adcmic.gpio_adc_in[1]	tcpwm[0].line_compl[0]:0	tcpwm[0].line_compl[256]:0	–	–	–	cpuss.trace_data[2]:0	scb[2].uart_rts:0	–	scb[1].spi_clk:1	–	lin[0].lin_en[0]:0	–	–	btss.sysclk_rf	keyscan.ks_row[4]	–	cpuss.rst_swj_trstn	–
P3.2	adcmic.gpio_adc_in[2]	tcpwm[0].line[1]:0	tcpwm[0].line[257]:0	–	–	–	cpuss.trace_data[1]:0	scb[2].uart_rx:0	scb[2].i2c_scl:0	scb[1].spi_mosi:1	pdm.pdm_clk[0]:0	lin[0].lin_rx[0]:0	canfd[0].ttcan_rx[0]:0	adcmic.clk_pdm:0	–	keyscan.ks_col[13]	–	–	–
P3.3	adcmic.gpio_adc_in[3]	tcpwm[0].line_compl[1]:0	tcpwm[0].line_compl[257]:0	–	–	–	cpuss.trace_data[0]:0	scb[2].uart_tx:0	scb[2].i2c_sda:0	scb[1].spi_miso:1	pdm.pdm_data[0]:0	lin[0].lin_tx[0]:0	canfd[0].ttcan_tx[0]:0	adcmic.pdm_data:0	–	keyscan.ks_col[14]	keyscan.ks_col[17]:1	–	–
P3.4	adcmic.gpio_adc_in[4]	tcpwm[0].line[0]:1	tcpwm[0].line[258]:0	–	–	–	cpuss.trace_clock:0	–	–	scb[1].spi_select3:1	–	–	–	–	–	keyscan.ks_col[7]	–	–	–

(table continues...)

Table 9 (continued) Multiple alternate functions[1)]

Port/ Pin	Analog	ACT #0	ACT #1	ACT #2	ACT #3	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #11	ACT #12	ACT #13	ACT #15	DS #2	DS #3	DS #5	DS #6
P3.6	adcmic.gpio_adc_in[6]	tcpwm[0].line[1]:1	tcpwm[0].line[259]:0	–	–	–	–	–	–	scb[1].spi_select1:1	–	–	–	–	–	keyscan.ks_col[9]	–	–	–
P3.7	adcmic.gpio_adc_in[7]	tcpwm[0].line_compl[1]:1	tcpwm[0].line_compl[259]:0	btss.antenna_switch_ctrl[3]	–	–	–	–	–	–	–	–	–	–	–	keyscan.ks_col[10]	–	–	–
P4.0	–	tcpwm[0].line_compl[1]:2	tcpwm[0].line_compl[261]:0	–	–	–	–	scb[2].uart_cts:2	–	–	–	–	–	–	–	keyscan.ks_row[2]	scb[0].i2c_scl:1	–	scb[0].spi_mosi:1
P4.1	–	tcpwm[0].line[0]:3	tcpwm[0].line[262]:0	–	–	–	–	–	–	–	–	–	–	–	–	keyscan.ks_row[3]	scb[0].i2c_sda:1	–	scb[0].spi_miso:1
P5.0/ WCO_OUT	srss.wco_in	tcpwm[0].line[0]:2	tcpwm[0].line[260]:0	–	–	–	–	scb[2].uart_cts:1	scb[2].i2c_scl:2	scb[1].spi_select0:2	pdm.pdm_clk[0]:1	–	canfd[0].ttcan_rx[0]:1	adcmic.clk_pdm:1	–	keyscan.ks_col[0]	–	–	–

(table continues...)

Table 9 (continued) Multiple alternate functions[1)]

Port/ Pin	Analog	ACT #0	ACT #1	ACT #2	ACT #3	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #11	ACT #12	ACT #13	ACT #15	DS #2	DS #3	DS #5	DS #6
P5.1/ WCO_ IN	srss. wco_ out	tcpw m[0]. line_ compl[0]:2	tcpw m[0]. line_ compl[260] :0	–	–	–	–	–	scb[2].i2c_ sda:2	–	pdm. pdm _dat a[0]:1	–	canf d[0].t tcan_ tx[0]: 1	adcm ic.pd m_d ata:1	–	keysc an.ks _col[1]	–	–	scb[0].spi_ selec t0:0

1) The notation for a signal is of the form IPName[x].signal_name[u]:y. IPName = Name of the block (such as tcpwm), x = Unique instance of the IP, Signal_name = Name of the signal, u = Signal number where there are more than one signals for a particular signal name, y = Designates copies of the signal name. For example, the name tcpwm[0].line_compl[3]:4 indicates that this is instance 0 of a tcpwm block, the signal is line_compl # 3 (complement of the line output) and this is the fourth occurrence (copy) of the signal. Signal copies are provided to allow flexibility in routing and to maximize utilization of on-chip resources.

5 Power supply considerations

Figure 8 shows the typical connections for power pins across all supported packages and refers to the 10 dBm PA configuration. For 0 dBm operation, connect BT_PAVDD to VCCRF.

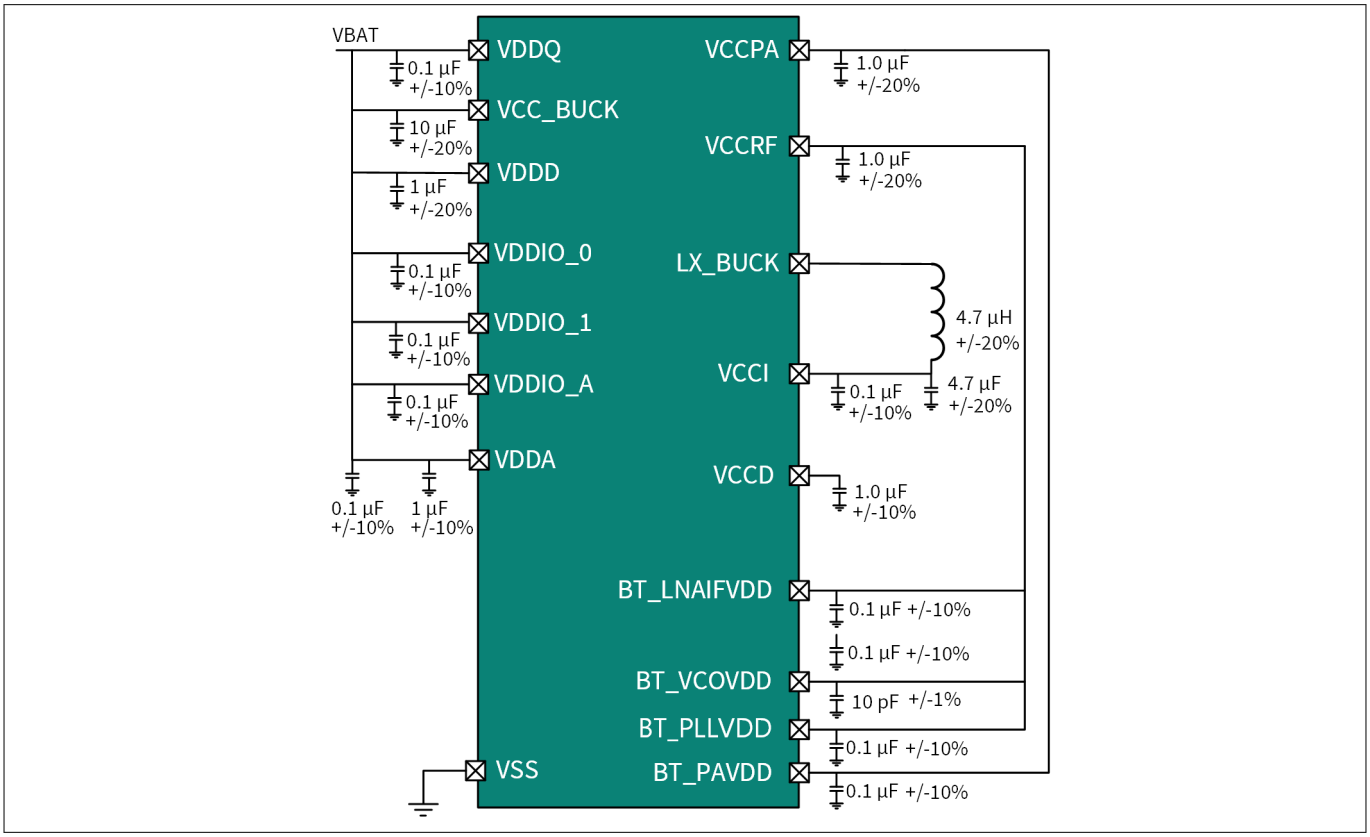


Figure 8 CYW89829 power topology

6 Electrical specifications

All specifications are subject are valid for –40°C < T_A < 105°C and for *VDDD* ranging from 1.7 V to 3.6 V, unless otherwise noted.

6.1 Absolute maximum ratings

Table 10 Absolute maximum ratings[1)]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID1	VDD_{ABS}	Analog or digital supply relative to VSS (V_{SSD} = V_{SSA})	-0.5		4	V	Absolute maximum
SID2	$VCCD_{ABS}$	Direct digital core voltage input relative to V_{SSD}	-0.5		1.2		
SID3	V_{GPIO_ABS}	GPIO voltage; VDDD or VDDA	-0.5		VDDIO + 0.5		
SID4	I_{GPIO_ABS}	Current per GPIO	-25		25	mA	
SID5	$I_{GPIO\_injection}$	GPIO injection current per pin	-0.5		0.5		
SID3A	ESD_HBM	Electrostatic discharge human body model	2200		-	V	
SID4A	ESD_CDM	Electrostatic discharge charged device model	500	-	-		
SID5A	LU	Pin current for latchup-free operation	-100		100	mA	
SIDWA8	$V_{undershoot}$	Maximum undershoot voltage for I/O			-0.5	V	Duration not to exceed 25% of the duty cycle
SIDWA9	$V_{overshoot}$	Maximum overshoot voltage for I/O	-		VDDIO + 0.5		
SIDWA10	T_j	Maximum junction temperature			125	°C	-

1) Usage above the absolute maximum conditions specified in Table 10 may result in permanent damage to the device. Prolonged exposure to absolute maximum conditions can impact device reliability.

The maximum storage temperature is 150°C, as specified in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life.

When the device is used within the range between absolute maximum conditions and normal operating conditions, it may not function according to the specified performance parameters.

6.2 Operating conditions

Table 11 Power supply range, CPU current, and transition time specifications

Spec ID#	Parameter	Description	Values				Details/ conditions
			Min	Typ	Max	Unit	
DC specifications							
SID6	VDDD	Internal regulator	1.7	–	3.6	V	–
SID7	VDDA	Analog power supply voltage. Shorted to VDDIO_A on PCB.					Internally unregulated supply
SID7R SID7C	VCCI	RF/Digital LDO input. Connect to output of internal buck	–	1.16	–	–	–
SID7P	VDDD	PA LDO input	2.7	–	3.6	V	For TX10 mode, BT_PAVDD connected to VCCPA; The minimum supply voltage VDDD is 2.7 V
SID7B	VDDIO_0	GPIO supply for ports	1.7		3.6	V	–
SID7E	VDDIO_1	Supply when programming eFuse	2.38	2.5	2.62	V	eFuse programming voltage is 2.5 V ± 5%
SID7A	VDDIO_A	GPIO supply for analog ports. Short to VDDA on PCB.	1.7	–	3.6	V	–
SID8	VCCD (LP)	Output voltage (for core logic bypass)	–	1.1	–	V	High speed mode
SID9	VCCD (ULP)	Output voltage (for core logic bypass)		1.0			ULP mode; Valid for –40°C to 105°C
SID10	C_{EFC}	External regulator voltage (VCCD) bypass	3.8	4.7	5.6	µF	X6S ceramic or better; Value for 0.8 V to 1.2 V
SID11	C_{EXC}	Power supply decoupling capacitor	–	10	–		X6S ceramic or better
SID12	VCCRF	Output voltage (for radio)	–	1.1	–	V	–

(table continues...)

Table 11 (continued) Power supply range, CPU current, and transition time specifications

Spec ID#	Parameter	Description	Values				Details/ conditions
			Min	Typ	Max	Unit	
SID13	VCCPA	Output voltage (for PA)		2.5			
SID523	VDDQ	External supply to PMU analog	1.7	–	3.6		
SID524	VCC_BUCK	External supply to switching regulator					
SID525	BT_PAVDD	Internal PA supply	1		2.75		
SID526	BT_RF	RF power supply			1.2		
SID527	BT_LNAIFVDD	LNA and IFPLL supply					
SID529	BT_VCOVDD	VCO supply					
CPU currents and transition times Cortex®-M33 Active mode							
Execute with cache enabled							
SIDC2	I_{DD4}	Execute from cache; CM33 Active 96 MHz. FLL. Dhrystone	–	4.8	5.8	mA	VDDD = 3.0 V, Buck ON, Max at 60°C
				7.4	8.4		VDDD = 1.8 V, Buck ON, Max at 60°C
SIDC3	I_{DD5}	Execute from cache; CM33 Active 48 MHz. IHO. Dhrystone		2.4	3.4		VDDD = 3.0 V, Buck ON, Max at 60°C
				3.7	4.1		VDDD = 1.8 V, Buck ON, Max at 60°C
SIDC4	I_{DD6}	Execute from cache; CM33 Active 8 MHz. IHO. Dhrystone		0.90	1.5		VDDD = 3.0 V, Buck ON, Max at 60°C
				1.27	1.75		VDDD = 1.8 V, Buck ON, Max at 60°C
SIDS1	I_{DD11}	CM33 Sleep 96 MHz with FLL		1.5	2.2		VDDD = 3.0 V, Buck ON, Max at 60°C
				2.2	2.7		VDDD = 1.8 V, Buck ON, Max at 60°C

(table continues...)

Table 11 (continued) Power supply range, CPU current, and transition time specifications

Spec ID#	Parameter	Description	Values				Details/ conditions
			Min	Typ	Max	Unit	
SIDS2	I_{DD12}	CM33 Sleep 48 MHz with IHO	–	1.2	1.9	mA	VDDD = 3.0 V, Buck ON, Max at 60°C
				1.7	2.2		VDDD = 1.8 V, Buck ON, Max at 60°C
SIDS3	I_{DD13}	CM33 Sleep 8 MHz with IHO		0.7	1.3		VDDD = 3.0 V, Buck ON, Max at 60°C
				0.96	1.5		VDDD = 1.8 V, Buck ON, Max at 60°C
Deep Sleep mode							
SIDDS1_B	I_{DD33A_B}	With internal Buck enabled and 64K SRAM retention	–	5.7	–	µA	At 25°C (with typical Silicon)
SIDDS2_B	I_{DD33B_B}	With internal Buck enabled and 128K SRAM retention		6.2	–		At 25°C (with typical Silicon)
SIDDS5_B	I_{DD33E_B}	With internal Buck enabled and 256K SRAM retention		7.5	–		At 25°C (with typical Silicon)
SIDDS3_B	I_{DD33C_B}	With internal Buck enabled and 64K SRAM retention DS-RAM		4.5	–		At 25°C (with typical Silicon)
SIDDS4_B	I_{DD33D_B}	With internal Buck enabled and 128K SRAM retention DS-RAM		5	–		At 25°C (with typical Silicon)
SIDDS6_B	I_{DD33F_B}	With internal Buck enabled and 256K SRAM retention DS-RAM		6	–		At 25°C (with typical Silicon)
Hibernate mode							
SIDHIB1	I_{DD34}	VDDD = 1.8 V	–	300	–	nA	No clocks running
SIDHIB2	I_{DD34A}	VDDD = 3.0 V		500			

(table continues...)

Table 11 (continued) Power supply range, CPU current, and transition time specifications

Spec ID#	Parameter	Description	Values				Details/ conditions
			Min	Typ	Max	Unit	
SIDHIB3	I_{DD35}	VDDD = 1.8 V		800			WCO is running
SIDHIB4	I_{DD35A}	VDDD = 3.0 V		1000			
Power mode transition times							
SID13A	T_{DS_ACT}	Deep Sleep to Active transition time. Guaranteed by design.	–	45	60	µs	DS to Active with 1.0 V operation, with upper inrush current limit
SID13B	T_{DS_ACTLP}	Deep Sleep to Active LP transition time. Guaranteed by design.		20	35		DS to Active LP with 0.9 V operation
SID13C	T_{DSR_ACT}	Deep Sleep-RAM to Active transition time. Guaranteed by design.		–	800		DS to Active with 1.0 V operation, with upper inrush current limit
SID13D	T_{DSR_ACTLP}	Deep Sleep-RAM to Active LP transition time. Guaranteed by Design.		–	800		DS-RAM to Active LP with 0.9 V operation
SID14	T_{HIB_ACT}	Hibernate to Active transition time		2000	–		Hibernate to Active with 1.0 V operation, with upper inrush current limit
SID14A	T_{HIB_ACTLP}	Hibernate to Active LP transition time		2000			Hibernate to Active with 0.9 V operation, with upper inrush current limit

***Note**: Usage beyond the absolute maximum conditions listed in Table 10 may result in permanent damage to the device. Prolonged exposure to absolute maximum conditions can adversely affect the reliability of the device. The maximum storage temperature is 150°C, in accordance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When the device operates below absolute maximum conditions but outside normal operating conditions, it may not perform according to its specified parameters.*

6.2.1 Recommended component

Table 12 Recommended component

Parameter	Conditions	Min	Typ	Max	Unit
LX_BUCK external inductor	4.7 µH ±20%, DCR = 230 mΩ ± 20% (for frequency < 1 MHz), Automotive grade	–	4.7	–	µH
LX_BUCK external output capacitor	4.7 µF ±20%, 6.3 V, 0402, X6S, MLCC capacitor	–	4.7	–	µF
VCC_BUCK external input capacitor	10 µF ±20%, 6.3 V, 0402, X6S, ESR < 30 mΩ at 4 MHz, ceramic capacitor	–	10	–	

6.2.2 XRES

Table 13 XRES DC specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
SID17	T_{XRES_IDD}	IDD when XRES asserted	–	300	–	nA	VDDD = 1.8 V
SID17A	$T_{XRES\_IDD\_1}$			800			VDDD = 3.3 V
SID77	V_{IH}	Input voltage high threshold	0.7 × VDDIO	–		V	CMOS input
SID78	V_{IL}	Input voltage low threshold	–		0.3 × VDDIO		
SID80	C_{IN}	Input capacitance		3	–	pF	–
SID81	$V_{HYSXRES}$	Input voltage hysteresis		100		mV	
SID82	I_{DIODE}	Current through protection diode to VDDIO/V_{SS}		–	100	µA	

Table 14 XRES AC specifications

Spec ID#	Parameter	Description	Values				Details/ conditions
			Min	Typ	Max	Unit	
SID15	T_{XRES_ACT}	POR or XRES release to Active transition time	–	1000	–	µs	Normal mode, 96 MHz M33, upper inrush current
SID16	T_{XRES_PW}	XRES pulse width	5	–			–

6.2.3 GPIO

Table 15 GPIO DC specifications

Spec ID#	Parameter	Description	Values				Details/ conditions
			Min	Typ	Max	Unit	
SID57	V_{IH}	Input voltage HIGH threshold	0.7 × VDDIO	–	–	V	CMOS input
SID57A	I_{IHS}	Input current when Pad > VDDIO for OVT inputs	–		10	µA	Per I^2C spec
SID58	V_{IL}	Input voltage LOW threshold			0.3 × VDDIO	V	CMOS input
SID241	V_{IH}	LVTTL input, VDDIO < 2.7 V	0.7 × VDDIO		–		–
SID242	V_{IL}		–		0.3 × VDDIO		
SID243	V_{IH}	LVTTL input, VDDIO > 2.7 V	2.0		–		
SID244	V_{IL}		–		0.8		
SID59	V_{OH}	Output voltage high level	VDDIO – 0.5		–	V	I_{OH} = 8 mA
SID62A	V_{OL}	Output voltage low level	–		0.4	V	I_{OL} = 8 mA
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID64	$R_{PULLDOWN}$	Pull-down resistor					
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25°C, VDDIO = 3.0 V
SID66	C_{IN}	Input capacitance			5	pF	-
SID67	V_{HYSTTL}	Input hysteresis LVTTL VDDIO > 2.7 V	100	0	–	mV	
SID68	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × VDDIO	–			

(table continues...)

Table 15 (continued) GPIO DC specifications

Spec ID#	Parameter	Description	Values				Details/ conditions
			Min	Typ	Max	Unit	
SID69	I_{DIODE}	Current through protection diode to VDDIO/V_{SS}	–		100	µA	
SID69A	I_{TOT_GPIO}	Maximum total source or sink chip current			200	mA	

Table 16 GPIO AC specifications

Spec ID#	Parameter	Description	Values				Details/ conditions
			Min	Typ	Max	Unit	
SID70	T_{RISEF}	Rise time in Fast Strong mode. 10% to 90% of VDDIO	–	3.5	–	ns	C_{LOAD} = 15 pF, 8 mA drive strength, VDDIO > 2.7 V
SID70A	T_{RISEF_1}			5.5			C_{LOAD} = 15 pF, VDDIO < 2.7 V, max slew and drive strength
SID71	T_{FALLF}	Fall time in Fast Strong mode. 10% to 90% of VDDIO		3.5			C_{LOAD} = 15 pF, 8 mA drive strength, VDDIO> 2.7 V
SID71A	T_{FALLF_1}			5.5			C_{LOAD} = 15 pF, VDDIO < 2.7 V, max slew and drive strength
SID72	T_{RISES_1}	Rise time in Slow Strong mode. 10% to 90% of VDDIO	52	–	142		C_{LOAD} = 15 pF, 8 mA drive strength, VDDIO < 2.7 V
SID72A	T_{RISES_2}		48		102		C_{load} = 15 pF, 8 mA drive strength, 2.7 V < VDDIO < 3.6 V

(table continues...)

Table 16 (continued) GPIO AC specifications

Spec ID#	Parameter	Description	Values				Details/ conditions
			Min	Typ	Max	Unit	
SID73	T_{FALLS_1}	Fall time in Slow Strong mode. 10% to 90% of VDDIO	44		211		C_{load} = 15 pF, 8 mA drive strength, VDDIO < 2.7 V
SID74	$F_{GPIOUT1}$	GPIO Fout; Fast Strong mode	–		100	MHz	90/10%,15 pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO Fout; Slow Strong mode			1.5		
SID76	$F_{GPIOUT3}$	GPIO Fout; Fast Strong mode			100		
SID245	$F_{GPIOUT4}$	GPIO Fout; Slow Strong mode			1.3		
SID246	F_{GPIOIN}	GPIO input operating frequency; 1.71 V < VDDIO < 3.6 V			100		90/10% V_{IO}

6.3 Analog peripherals

Table 17 Internal reference specification

Spec ID#	Parameter	Description	Values				Details/ conditions
			Min	Typ	Max	Unit	
SID93R	V_{REFBG}	–	1.188	1.2	1.212	V	–

6.3.1 ADC

Table 18 ADC specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
DM.2	_	Analog supply voltage - VDDA	1.7	_	3.6	V	_

(table continues...)

Table 18 (continued) ADC specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
DM.5		Active current consumption		2		mA	25°C
DM.6		Power down current		0.1	–	µA	25°C - ADC disabled with device in Active mode
DM.8		Absolute error - Includes gain error, offset and distortion	–	–	5	%	
DM.11		ENOB		11	–	Bit	
DM.13		ADC input full scale	0	–	VDDA	Vpp	–
DM.15		Conversion rate	50	100	–	kHz	
DM.17		Signal bandwidth	–	DC	–	Hz	
DM.19		Startup time	–	20		µs	
DM.30		ADC SNR	78		–	dB	0 dB PGA gain, A-weighted
DM.31		ADC THD+N	74	–			–3 dB FS input, 0 dB PGA gain
DM.33		GPIO source impedance	–		1k	Ω	10 µs measurement time

6.4 Digital peripherals

Table 19 Timer/counter/PWM (TCPWM) specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
SID.TCPWM.1	I_{TCPWM1}	Block current consumption at 8 MHz	–	–	70	µA	All modes (TCPWM)
SID.TCPWM.2	I_{TCPWM2}	Block current consumption at 24 MHz			180		
SID.TCPWM.2A	I_{TCPWM3}	Block current consumption at 50 MHz			270		
SID.TCPWM.2B	I_{TCPWM4}	Block current consumption at 100 MHz			540		

(table continues...)

Table 19 (continued) Timer/counter/PWM (TCPWM) specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
SID.TCPWM.3	$TCPWM_{FREQ}$	Operating frequency			100	MHz	Fc max = Fcpu Maximum = 100 MHz
SID.TCPWM.4	$TPWM_{ENEXT}$	Input trigger pulse width for all trigger events	2/Fc		–	ns	Trigger events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.
SID.TCPWM.5	$TPWM_{EXT}$	Output trigger pulse widths	1.5/Fc				Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs
SID.TCPWM.5A	TC_{RES}	Resolution of counter	1/Fc				Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution					Minimum pulse width of PWM output

Table 20 Serial communication block (SCB) specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
I^2C DC specifications							
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	30	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kHz			80		
SID151	I_{I2C3}	Block current consumption at 1 Mbps			180		
SID152	I_{I2C4}	I^2C enabled in Deep Sleep mode			1.7		At 60°C

(table continues...)

Table 20 (continued) Serial communication block (SCB) specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
I²C AC specifications							
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	–
UART DC specifications							
SID160	I_{UART1}	Block current consumption at 100 kbps	–	–	30	µA	–
SID161	I_{UART2}	Block current consumption at 1000 kbps			180		
UART AC specifications							
SID162A	F_{UART1}	Bit rate	–	–	3	Mbps	ULP mode
SID162B	F_{UART2}				8		LP mode
SPI DC specifications							
SID163	I_{SPI1}	Block current consumption at 1 Mbps	–	–	220	µA	–
SID164	I_{SPI2}	Block current consumption at 4 Mbps			340		
SID165	I_{SPI3}	Block current consumption at 8 Mbps			360		
SID165A	I_{SP14}	Block current consumption at 25 Mbps			800		
SPI AC specifications for LP mode (VCCD = 1.1 V) unless noted otherwise							
SID166	F_{SPI}	SPI operating frequency Master and externally clocked Slave	–	–	24	MHz	–
SID166B	F_{SPI_EXT}	SPI operating frequency Master (Fscb is SPI clock)			Fscb/4		Fscb max is 96 MHz in LP mode, 24 MHz in ULP mode
SID166A	F_{SPI_IC}	SPI Slave internally clocked			24		–

(table continues...)

Table 20 (continued) Serial communication block (SCB) specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
SPI AC specifications for ULP mode (VCCD = 1.0 V) unless noted otherwise							
SID166C	F_{SPI}	SPI operating frequency master and externally clocked slave	–	–	12	MHz	–
SID166D	F_{SPI_EXT}	SPI operating frequency master (Fscb is SPI clock)			Fscb/4		Fscb max is 48 MHz in ULP mode
SID166E	F_{SPI_IC}	SPI slave internally clocked			12		–
SPI Master mode AC specifications for LP mode (VCCD = 1.1 V) unless noted otherwise							
SID167	T_{DMO}	MOSI valid after SClock driving edge	–	12	12	ns	20 ns max. for ULP mode
SID168	T_{DSI}	MISO valid before SClock capturing edge	20	–	–		Full clock, late MISO sampling
SID169	T_{HMO}	MOSI data hold time	0		5		Referred to slave capturing edge
SID169C	T_{DHI}	SPI master: MISO hold time after SCLK capturing edge	0	–	–	ns	–
SID169A	$T_{SSELMSCK1}$	SSEL valid to first SCK valid edge	18	21	21		Referred to master clock edge
SPI Master mode AC specifications for ULP mode (VCCD = 1.0 V) unless noted otherwise							
SID167A	T_{DMO}	MOSI valid after SClock driving edge	–	–	26	ns	–
SID167B	T_{DSI}	MISO valid before SClock capturing edge	35	–	–		–

(table continues...)

Table 20 (continued) Serial communication block (SCB) specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
SID167C	T_{HMO}	MOSI data hold time	–	-5	–		–
SID167D	T_{DHI}	SPI master: MISO hold time after SClock capturing edge	0	–	–		–
SID167E	$T_{SSELMSCK1}$	SSEL valid to first SCK valid edge	41	–	–		–
SID167F	$T_{SSELMSCK2}$	SPI SClock pulse width HIGH	41	–	–		–
SPI Slave mode AC specifications for LP mode (VCCD = 1.1 V) unless noted otherwise							
SID170	T_{DMI}	MOSI valid before Sclock capturing edge	5	–	–	ns	–
SID170A	SPI_FREQ	For LP mode	48			MHz	
SID171A	T_{DSO_EXT}	MISO valid after Sclock driving edge in external clock mode	–		20	ns	35 ns max. for ULP mode
SID171	T_{DSO}	MISO valid after Sclock driving edge in internal clock mode			TDSO_EXT + 3 × Tscb		Tscb is Serial Communication Block clock period
SID171B	T_{DSO}	MISO valid after Sclock driving edge in internal clock mode with median filter enabled.			TDSO_EXT + 4 × Tscb		Tscb is Serial Communication Block clock period
SID172	T_{HSO}	Previous MISO data hold time	5.5		–		–

(table continues...)

Table 20 (continued) Serial communication block (SCB) specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
SID172C	T_{HIS}	SPI MOSI hold from SCLK					
SPI Slave mode AC specifications for ULP mode (VCCD = 1.0 V) unless noted otherwise							
SID173A	T_{DMI}	MOSI valid before SClock capturing edge	12	–	–	ns	–
SID174A	T_{DSO_EXT}	MISO valid after SClock driving edge in external clock mode	–	–	35		–
SID174	T_{DSO}	MISO valid after SClock driving edge in internal clock mode	–	–	TDSO_EXT + 3 × Tscb		–
SID174B	T_{DSO}	MISO valid after SClock driving edge in internal clock mode with median filter enabled	–	–	TDSO_EXT + 4 × Tscb		–
SID175	T_{HSO}	Previous MISO data hold time	5.5	–	–		–
SID175C	T_{HIS}	SPI MOSI hold from SClock	5.5	–	–		–
SID175D	CSPI	SPI capacitive load	–	10	–	pF	–

6.5 Audio subsystem

Table 21 Audio subsystem specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
PDM specifications							

(table continues...)

Table 21 (continued) Audio subsystem specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
SID400P	Fmax_ clk_sys	Clock frequency for clk_sys	–	96	–	MHz	PVT18 ss, 0.90 V, –40°C, scl40 library, minimum parameters
SID401	Fmax_ clk_if_srss	Clock frequency for Audio clock reference clk_if_srss		48			PVT18 ss, 0.90 V, –40°C, scl40 library, minimum parameters
SID402	Idyn_act_ typ	Typical dynamic current when cell is active. See the DC specifications table for related static current specifications, if applicable.		–	110	µA/ MHz	PVT16 tt, 1.1 V, 25°C, scl40 library, typical parameters clk_ADC: 49.152 MHz clk_sys: 50 MHz
SID403	Idyn_act_ max	Maximum dynamic active current. See the DC specifications table for related static current specifications, if applicable.			132		PVT20 ff, 1.21 V, 150°C, scl40 library, maximum parameters clk_ADC: 49.152 MHz clk_sys: 50 MHz
SID403A	Idyn_slp_ typ	Typical dynamic current when cell is idle. See the DC specifications table for related static current specifications, if applicable.			80		PVT16 tt, 1.1 V, 25°C, scl40 library, typical parameters, clocks toggling clk_ADC: 49.152 MHz clk_sys: 50 MHz
SID403B	T_SETUP	Receiver setup			10	ns	PVT18 ss, 0.90 V, –40°C, scl40 library, minimum parameters

(table continues...)

Table 21 (continued) Audio subsystem specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
SID404A	CPDM	Load		10	–	pF	–
SID404	PDM_OUT	Audio sample rate	8	–	48	KSPS	–
SID405	PDM_WL	Word length	16	–	24	bits	–
SID412	PDM_ST	Startup time	–	48	–	–	WS (Word Select) cycles
I2S specifications; the same applies for LP and ULP modes unless stated otherwise							
SID413	I2S_WORD	Length of I^2S word	8	–	32	bits	–
SID414B	I2S_BCK_F	Bit Clock frequency in LP mode	–		12.288	MHz	
SID414BU	I2S_BCK_F_U	Bit Clock frequency in ULP mode			3.072		
SID414BP	I2S_BCK_P	Bit Clock period		1/I2S_BCK_F	–	ns	
SID414BPU	I2S_BCK_P_U	Bit Clock period in ULP mode		1/I2S_BCK_F_U			
SID414	I2S_WS_FREQ	Word clock frequency in LP mode		–	192	kHz	
SID414M	I2S_WS_FREQ_U	Word clock frequency in ULP mode			48		
SID435L	I2S_BCK_TL	Bit clock low period in LP Mode	0.35 × I2S_BCK_P		–	ns	
SID415IL	I2S_MCKI_TL	Master clock IN low period in LP (or) ULP mode	0.45 × tMCLK				
SID415IH	I2S_MCKI_TH	Master clock IN high period in LP (or) ULP Mode					
SID415OL	I2S_MCKO_TL	Master clock Out low period in LP (or) ULP mode	0.35 × tMCLK	0.45 × tMCLK to 0.4 × tMCLK			Typ spec 0.45 × tMCLK to 0.4 × tMCLK

(table continues...)

Table 21 (continued) Audio subsystem specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
SID415OH	I2S_MCKO_TH	Master clock Out high period in LP (or) ULP mode		0.45 × tMCLK to 0.4 × tMCLK			
SID416	TDM_OUTPUT_LOAD_MAX	Capacitive load	10	–		pF	–
I2S Slave mode							
SID430	I2S_S_TS_WS	WS setup time before the first edge following the driving edge of bit clock for LP mode	0.2 × I2S_BCK_P	–	–	ns	–
SID430U	I2S_S_TS_WS_U	WS setup time before the first edge following the driving edge of bit clock for ULP mode	0.2 × I2S_BCK_P_U				
SID430A	I2S_S_TH_WS	WS hold time after the first edge following the driving edge of bit clock, LP or ULP mode	0	–	–	ns	–
SID432	I2S_S_SDO	SDO propagation delay from driving edge of bit clock for LP mode	0.3 × I2S_BCK_P		0.2 × I2S_BCK_P		
SID432U	I2S_S_SDO_U	SDO propagation delay from driving edge of bit clock for ULP mode	0.3 × I2S_BCK_P_U		0.2 × I2S_BCK_P_U		
I2S Master mode							

(table continues...)

Table 21 (continued) Audio subsystem specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
SID437	I2S_M_WS	WS propagation delay from driving edge of bit clock for LP mode	0	–	0.2 × I2S_BCK_P	ns	–
SID437_U	I2S_M_WS_U	WS propagation delay from driving edge of bit clock for ULP mode			0.2 × I2S_BCK_P_U		
SID438	I2S_M_SDO	SDO propagation delay from driving edge of bit clock for LP mode			0.2 × I2S_BCK_P		
SID438U	I2S_M_SDO_U	SDO propagation delay from driving edge of bit clock for ULP mode			0.2 × I2S_BCK_P_U		Associated clock edge depends on selected polarity

***Note**: TMCLK_SOC is the internal I2S master clock period.*

6.6 System resources

6.6.1 Power-on-reset (POR)

Table 22 POR with brown-out detect (BOD) DC specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
Precise POR (PPOR)							
SID190	$V_{FALLPPOR}$	BOD trip voltage in Active and Sleep modes. VDDD.	1.54	–	–	V	BOD Reset guaranteed for VDDD levels below 1.54 V
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep. VDDD.	1.54				–

(table continues...)

Table 22 (continued) POR with brown-out detect (BOD) DC specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
SID192A	V_{DDRAMP}	Maximum power supply ramp rate (any supply)	–		100	mV/µs	Active mode

Table 23 POR with BOD AC specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
SID194A	V_{DDRAMP_DS}	Maximum power supply ramp rate (any supply) in system Deep Sleep mode	–	–	10	mV/µs	BOD operation guaranteed

6.6.2 Voltage monitors

Table 24 Voltage monitors DC specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
SID195	V_{HVDI1}	–	1.38	1.43	1.47	V	-
SID196	V_{HVDI2}		1.57	1.63	1.68		
SID197	V_{HVDI3}		1.76	1.83	1.89		
SID198	V_{HVDI4}		1.95	2.03	2.10		
SID199	V_{HVDI5}		2.05	2.13	2.2		
SID200	V_{HVDI6}		2.15	2.23	2.3		
SID201	V_{HVDI7}		2.24	2.33	2.41		
SID202	V_{HVDI8}		2.34	2.43	2.51		
SID203	V_{HVDI9}		2.44	2.53	2.61		
SID204	V_{HVDI10}		2.53	2.63	2.72		
SID205	V_{HVDI11}		2.63	2.73	2.82		
SID206	V_{HVDI12}		2.73	2.83	2.92		
SID207	V_{HVDI13}		2.82	2.93	3.03		
SID208	V_{HVDI14}		2.92	3.03	3.13		
SID209	V_{HVDI15}		3.02	3.13	3.23		
SID211	LVI_IDD	Block current	–	5	15	µA	

Table 25 Voltage monitors AC specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
SID212	$T_{MONTRIP}$	Voltage monitor trip time	–	–	170	ns	–

6.6.3 SWD and trace interface

Table 26 SWD and trace specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
SID214	F_SWDCLK2	1.7 V ≤ VDDD ≤ 3.6 V	–	–	25	MHz	LP mode; VCCD = 1.1 V
SID214L	F_SWDCLK2L				12		ULP mode; VCCD = 1.0 V
SID215	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T		–	ns	For both LP and ULP modes
SID216	T_SWDI_HOLD						
SID217	T_SWDO_VALID		–		0.5 × T		–
SID217A	T_SWDO_HOLD		1		–		
SID214T	F_TRCLK_LP1	With trace data setup/ hold times of 2/1 ns respectively	–		48	MHz	LP mode; VCCD = 1.1 V
SID215T	F_TRCLK_LP2	With trace data setup/ hold times of 3/2 ns respectively			48		
SID216T	F_TRCLK_ULP				24		ULP mode; VCCD = 1.0 V

6.6.4 Internal main oscillator (IMO)

Table 27 IMO DC specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
SID218	I_{IMO1}	IMO operating current at 8 MHz	–	9	15	µA	–

Table 28 IMO AC specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
SID223	FIMOTOL1	Frequency variation centered on 8 MHz	–	–	±2	%	-
SID227	T_{JITR}	Cycle-to-cycle and period jitter	–	±250	–	µs	

6.6.5 Internal low-speed oscillator (ILO)

Table 29 ILO DC specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
SID231	I_{ILO2}	ILO operating current at 32 kHz	–	0.3	0.7	µA	–

Table 30 ILO AC specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
SID234	$T_{STARTILO1}$	ILO startup time	–	–	7	µs	Startup time to 80% of final frequency
			–	–	35	µs	Startup time to 95% of final frequency
SID236	$T_{LIODUTY}$	ILO duty cycle	45	50	55	%	–
SID237	$F_{ILOTRIM1}$	32 kHz trimmed frequency	28.8	32	35.2	kHz	±10% variations

6.6.6 Frequency-locked loop (FLL)

Table 31 FLL specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
SID450	FLL_RANGE	Input frequency range.	0.040	–	96.00	MHz	Upper limit is for External input.
SID451	FLL_OUT_DIV2	Output frequency range. VCCD = 1.1 V	24.00				Output range of FLL divided-by-2 output
SID451A	FLL_OUT_DIV2	Output frequency range. VCCD = 0.9 V			48.00		
SID452	FLL_DUTY_DIV2	Divided-by-2 output; High or Low	47.00		53.00	%	–
SID454	FLL_WAKEUP	Time from stable input clock to 1% of final value on Deep Sleep wakeup	–		11.00	µs	With IMO input, less than 10°C change in temperature while in Deep Sleep, and Fout ≥ 50 MHz
SID455	FLL_JITTER	Period jitter (1 sigma at 100 MHz)			18.00	ps	–
SID456	FLL_CURRENT	CCO + logic current			5.50	µA/MHz	

6.6.7 Crystal oscillator

Table 32 ECO specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
MHz ECO DC specifications							
SID316	I_{DD_MHz}	Block operating current with Cload up to 18 pF	–	1200	–	µA	Type 24 MHz
MHz ECO AC specifications							

(table continues...)

Table 32 (continued) ECO specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
SID317	F_MHz	Crystal frequency range	–	24	–	MHz	–
kHz ECO DC specifications							
SID318	IDD_kHz	Block operating current with 32-kHz crystal	–	0.38	1	µA	–
SID321E	ESR32K	Equivalent series resistance		80	–	kΩ	
SID322E	PD32K	Drive level		–	0.5	µW	
kHz ECO AC specifications							
SID319	F_kHz	32-kHz trimmed frequency	–	32.8	–	kHz	–
SID320	Ton_kHz	Startup time		–	1000	ms	
SID320E	F_{TOL32K}	Frequency tolerance		50	250	ppm	

6.6.8 Clock source switching time

Table 33 Clock source switching time specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
SID262	$TCLK_{SWITCH}$	Clock switching from one CLK_HF to another CLK_HF in clock periods[1)]	–	–	4 clk1 + 3 clk2	periods	–

1) As an example, if the clk_path[1] source is changed from the IMO to the FLL (see Figure 3) then clk1 is the IMO and clk2 is the FLL.

6.6.9 QSPI

Table 34 QSPI specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
QSPI specifications. All specs with 15-pF load							
SID390Q	Fsmifclock	QSPI output clock frequency	–	–	48	MHz	LP mode (1.1 V)
SID390QU	Fsmifclocku	QSPI output clock frequency			24		ULP mode (1.0 V)
SID397Q	Idd_qspi	Block current in LP mode (1.1 V)			1900	µA	LP mode (1.1 V)
SID398Q	Idd_qspi_u	Block current in ULP mode (1.0 V)			590		ULP mode (1.0 V)
SID399A	SDR_TCSH0	CS# active hold to CK	4		–	ns	–
SID399B	SDR_TOUT_SETUP_LF	Output setup time of DQ[3:0] to CK high	5.1				
SID399C	SDR_TOUT_HOLD_LF	Output hold time of DQ[3:0] to CK high					
SID399D	SDR_TIN_V	CK low to DQ[3:0] input valid time	–		6.7		
SID399E	SDR_TIN_HO	CK low to DQ[3:0] input hold time	1		–		

6.6.10 Smart I/O

Table 35 Smart I/O specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
SID420	SMIO_BYP	Smart I/O Bypass delay	–	–	2	ns	–
SID421	SMIO_LUT	Smart I/O LUT prop delay					

6.6.11 JTAG boundary scan

Table 36 JTAG boundary scan

Spec ID#		Parameter	Values				Description
			Min	Typ	Max	Unit	
JTAG boundary scan parameters							
SID460	TCKLOW	TCK LOW minimum	34	–	–	ns	–
SID461	TCKHIGH	TCK HIGH	10				
SID462	TCK_TDO	TDO clock-to-out (max) from falling TCK	–		22		
SID463	TSU_TCK	TDI, TMS setup time before rising TCK	12		–		
SID464	TCk_THD	TDI, TMS Hold time after rising TCK	10				
SID465	TCK_TDOV	TCK to TDO data valid (High-Z to active)	22				
SID466	TCK_TDOZ	TCK to TDO data valid (Active to High-Z).					
JTAG boundary scan parameters for 1.1 V (LP) mode operation							
SID468	TCKLOW	TCK low	52	–	–	ns	–
SID469	TCKHIGH	TCK high	10				
SID469A	TCKPERIOD	CLK_JTAG_PERIOD, 30 pF load	–	62			
SID470	TCK_TDO	TCK falling edge to output valid		–	40		
SID471	TSU_TCK	Input valid to TCK rising edge	12		–		

(table continues...)

Table 36 (continued) JTAG boundary scan

Spec ID#		Parameter	Values				Description
			Min	Typ	Max	Unit	
SID472	TCk_THD	Input hold time to TCK rising edge	10				
SID473	TCK_TDOV	TCK falling edge to output valid (High-Z to active).	40				
JTAG boundary scan parameters for 1.0 V (ULP) mode operation							
SID468A	TCKLOW	TCK low	102	–	–	ns	–
SID469A	TCKHIGH	TCK high	20				
SID470A	TCK_TDO	TCK falling edge to output valid	–		80		
SID471A	TSU_TCK	Input valid to TCK rising edge	22		–		
SID472A	TCk_THD	Input hold time to TCK rising edge	20	–	–	ns	–
SID473A	TCK_TDOV	TCK falling edge to output valid (High-Z to active).	80				
SID474A	TCK_TDOZ	TCK falling edge to output valid (Active to high-Z).					

6.7 Bluetooth® LE

Table 37 Bluetooth® LE subsystem specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
RF receiver specifications (1 Mbps)							
SID317R[1)]	RXS, IDLE	RX sensitivity with ideal transmitter	–	–98	–	dBm	Across RF operating frequency range

(table continues...)

Table 37 (continued) Bluetooth® LE subsystem specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
SID318R[2)]				–96.5			–
SID319R	PRXMAX	Maximum received signal strength at < 30.8% PER		–5			RF-PHY specification (RCV-LE/CA/06/C)
SID320R	CI1	Co-channel interference, wanted signal at –67 dBm and interferer at FRX		9	21	dB	RF-PHY specification (RCV-LE/CA/03/C)
SID321R	CI2	Adjacent channel interference, wanted signal at –67 dBm and interferer at FRX ± 1 MHz		–2	15		
SID322R	CI3	Adjacent channel interference, wanted signal at –67 dBm and interferer at FRX ± 2 MHz		–45	–17		
SID323R	CI4	Adjacent channel interference, wanted signal at –67 dBm and interferer at ≥ FRX ± 3 MHz		–49	–27		
SID324R	CI5	Adjacent channel interference, wanted signal at –67 dBm and interferer at image frequency (FIMAGE)		–31	–9		

(table continues...)

Table 37 (continued) Bluetooth® LE subsystem specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
SID325R	CI6	Adjacent channel interference, Wanted Signal at –67 dBm and Interferer at image frequency (FIMAGE ± 1 MHz)		–35	–15		
RF receiver specifications (2 Mbps)							
SID326[1)]	RXS, IDLE	RX sensitivity with ideal transmitter	–	–95	–	dBm	Across RF operating frequency range
SID327[2)]				–93.5			–
SID328R	PRXMAX	Maximum received signal strength at < 30.8% PER		–5			RF-PHY specification (RCV-LE/CA/06/C)
SID329R	CI1	Co-channel interference, wanted signal at –67 dBm and interferer at FRX		7	21	dB	RF-PHY specification (RCV-LE/CA/03/C)
SID330	CI2	Adjacent channel interference, wanted signal at –67 dBm and interferer at FRX ± 2 MHz		–2	15		
SID331	CI3	Adjacent channel interference, wanted signal at –67 dBm and interferer at FRX ± 4 MHz		–42	–15		

(table continues...)

Table 37 (continued) Bluetooth® LE subsystem specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
SID332	CI4	Adjacent channel interference, wanted signal at –67 dBm and interferer at ≥ FRX ± 6 MHz		–39	–27		
SID333	CI5	Adjacent channel interference, wanted signal at –67 dBm and interferer at image frequency (FIMAGE)		–29	–9		
SID334	CI6	Adjacent channel interference, wanted signal at –67 dBm and interferer at image frequency (FIMAGE ± 2 MHz)		–39	-15		
RF receiver specification S2 (500 kbps)							
SID501	RXS, IDLE	RX sensitivity with ideal transmitter, standard mod index Rx	–	–101	–	dBm	Across RF operating frequency range
SID506	CI1	Co-channel interference, wanted signal at –72 dBm and interferer at FRX	–	5	17	dB	RF-PHY specification (RCV-LE/CA/28/C)
SID507	CI2	Adjacent channel interference, wanted signal at –72 dBm and interferer at FRX ± 1 MHz		–8	11		

(table continues...)

Table 37 (continued) Bluetooth® LE subsystem specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
SID508	CI3	Adjacent channel interference, wanted signal at –72 dBm and interferer at FRX ± 2 MHz		–47	–21		
SID509	CI4	Adjacent channel interference, wanted signal at –72 dBm and interferer at FRX ± 3 MHz		–53	–31		
SID510	CI5	Adjacent channel interference, wanted signal at –72 dBm and Interferer at image frequency (FIMAGE)		–36	–13		
SID511	CI6	Adjacent channel interference, wanted signal at –72 dBm and interferer at image frequency (FIMAGE ± 1 MHz)		–40	–19		
RF Receiver specification S8 (125 kbps)							
SID512	RXS, IDLE	RX sensitivity with Ideal Transmitter[2)]	–	–106	–	dBm	Across RF operating frequency range
SID517	CI1	Co-channel interference, wanted signal at –79 dBm and interferer at FRX		6	12	dB	RF-PHY specification (RCV-LE/CA/29/C)

(table continues...)

Table 37 (continued) Bluetooth® LE subsystem specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
SID518	CI2	Adjacent channel interference, wanted signal at –79 dBm and interferer at FRX ± 1 MHz		–18	6	–	
SID519	CI3	Adjacent channel interference, wanted signal at –79 dBm and interferer at FRX ± 2 MHz		–51	–26		
SID520	CI4	Adjacent channel interference, wanted signal at –79 dBm and interferer at FRX ± 3 MHz		–51	–36		
SID521	CI5	Adjacent channel interference, wanted signal at –79 dBm and interferer at Image frequency (FIMAGE)		–40	–18		
SID522	CI6	Adjacent channel interference, wanted signal at –79 dBm and interferer at Image frequency (FIMAGE ± 1 MHz)		–47	–24		

RF Receiver specification (1 and 2 Mbps)

(table continues...)

Table 37 (continued) Bluetooth® LE subsystem specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
SID338	OBB1	Out of band blocking, wanted signal at -67 dBm and interferer at F = 30–2000 MHz	–30	–	–	dBm	RF-PHY specification (RCV-LE/CA/04/C)
SID339	OBB2	Out of band blocking, wanted signal at –67 dBm and interferer at F = 2003–2399 MHz	–35				RF-PHY specification (RCV-LE/CA/04/C)
SID340	OBB3	Out of band blocking, wanted signal at –67 dBm and interferer at F = 2484–2997 MHz					
SID341	OBB4	Out of band blocking, wanted signal at –67 dBm and interferer at F = 3000–12750 MHz	–30				RF-PHY specification (RCV-LE/CA/04/C)
SID342	IMD	Intermodulation performance, wanted signal at –64 dBm and 1 Mbps Bluetooth® LE, 3rd, 4th and 5th offset channel	–50				RF-PHY specification (RCV-LE/CA/05/C)
SID343	RXSE1	Receiver spurious emission 30 MHz to 1.0 GHz	–		–57		100 kHz measurement bandwidth ETSI EN300 328 V2.1.1
SID344	RXSE2	Receiver spurious emission 1.0 GHz to 12.75 GHz			–53		1 MHz measurement bandwidth ETSI EN300 328 V2.1.1

RF transmitter specifications

(table continues...)

Table 37 (continued) Bluetooth® LE subsystem specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
SID345	TXP, ACC	RF power accuracy	–2	–	2	dB	–
SID346	TX0	Power range	–	23	–		–24 dBm to 0 dBm
	TX10			33			–24 dBm to 10 dBm
SID347	TXP, 0 dBm	Output power, 0 dBm power setting		0		dBm	For TX10 mode, BT_PAVDD connected to VCCPA. The minimum supply voltage VDDD is 2.7 V.
SID348	TXP, 10 dBm	Output power, 10 dBm power setting		10			
SID349	TXP, MIN	Output power, minimum power setting		–20			
SID350	F2Max	Average frequency deviation for 10101010 pattern	185	–		kHz	RF-PHY specification (TRM-LE/CA/05/C)
SID350R	F2Max_2M	Average frequency deviation for 10101010 pattern for 2 Mbps	370				
SID350LR	F1Max_S8	Average frequency deviation for 10101010 pattern for 125 bps	185				RF-PHY specification (TRM-LE/CA/13/C)
SID351	F1AVG	Average frequency deviation for 11110000 pattern	225	250	275		RF-PHY specification (TRM-LE/CA/05/C)
SID351R	F1AVG_2M	Average frequency deviation for 11110000 pattern for 2 Mbps	450	500	550		RF-PHY specification (TRM-LE/CA/05/C)

(table continues...)

Table 37 (continued) Bluetooth® LE subsystem specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
SID351R	F1AVG_S8	Average frequency deviation for 11110000 pattern for 125 kbps	225	250	275		RF-PHY specification (TRM-LE/CA/13/C)
SID352	EO	Eye opening = ΔF2AVG/ΔF1AVG	0.8	–	–	–	RF-PHY specification (TRM-LE/CA/05/C)
SID353	FTX, ACC	Frequency accuracy	–150		150	kHz	RF-PHY specification (TRM-LE/CA/06/C)
SID354	FTX, MAXDR	Maximum frequency drift	–50		50		RF-PHY specification (TRM-LE/CA/06/C)
SID355	FTX, INITDR	Initial frequency drift	–20		20		RF-PHY specification (TRM-LE/CA/06/C)
SID355LR	FTX, INITDR, S8		–19.2		19.2		RF-PHY specification (TRM-LE/CA/14/C)
SID356	FTX, DR	Maximum drift rate	–20		20	kHz/50 µs	RF-PHY specification (TRM-LE/CA/06/C)
	FTX, DR, S8		–19.2		19.2		RF-PHY specification (TRM-LE/CA/14/C)
SID357	IBSE1	In band spurious emission at 2 MHz offset (1 Mbps) In band spurious emission at 4 MHz offset (2 Mbps)	–	–	–20	dBm	RF-PHY specification (TRM-LE/CA/03/C)

(table continues...)

Table 37 (continued) Bluetooth® LE subsystem specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
SID358	IBSE2	In band spurious emission at > 3 MHz offset (1 Mbps) In band spurious emission at > 6 MHz offset (2 Mbps)			–30		
SID359	TXSE1	Transmitter spurious emissions (Averaging), < 1.0 GHz	–	–	–55.5		FCC-15.247
SID360	TXSE2	Transmitter spurious emissions (Averaging), > 1.0 GHz			–41.5		
RF current specifications							
SID361	IRX1_wb	Receive current (1 Mbps)	–	5.7	–	mA	Measured with VCC_BUCK = 3.0 V; In all cases, VCCI = 1.16 V and VCCRF = 1.1 V; For TX0, BT_PAVDD = VCCRF. For TX10, BT_PAVDD = VCCPA = 2.5 V
SID362	ITX1_0dBm	TX current at 0 dBm setting (1 Mbps)		5.2			
SID365R	ITX1_10dBm	TX current at 10 dBm setting (1 Mbps)		17.2			
General RF specifications							
SID373	FREQ	RF operating frequency	2402	–	2480	MHz	–
SID374	CHBW	Channel spacing	–	2	–		
SID375	DR1	On-air data rate (1 Mbps)		1000		kbps	
SID376	DR2	On-air data rate (2 Mbps)		2000			
RSSI specifications							
SID379	RSSI, ACC	RSSI accuracy	–3	–	3	dB	–95 dBm to –20 dBm measurement range
SID380	RSSI, RES	RSSI resolution	–	1	–	dB	–

(table continues...)

Table 37 (continued) Bluetooth® LE subsystem specifications

Spec ID#	Parameter	Description	Values				Details/conditions
			Min	Typ	Max	Unit	
SID381	RSSI, PER	RSSI sample period	–	6	–	µs	–
System-level Bluetooth® LE specifications							
SID433R	Adv_Pwr	Advertising power, 1.28 s advertising interval, 31 bytes, TX 0 dBm	–	44.5	–	µW	Connectible advertising, VBAT = 3.0 V
SID434R	Conn_ Pwr_300	Connection power, 300 ms connection interval, 0 bytes, TX 0 dBm		67.0			VBAT = 3.0 V
SID435R	Conn_ Pwr_1S	Connection power, 1000 ms connection interval, 0 bytes, TX 0 dBm		30.3			

1) Coherent demodulator enabled with stable modulation index.
2) Coherent demodulator enabled with standard modulation index.

***Note**: Power consumption numbers are measured using the watch crystal oscillator (WCO).*

7 Ordering information

Table 38 lists the CYW89829 part numbers and their corresponding features.

Table 38 Ordering part numbers

Product	Package	Ambient operating temperature
CYW89829B1062	7.0 × 7.0 × 0.9 mm 48-lead QFN	–40°C to 105°C

Table 39 Part number decoder information

CYW89829Bxabc	0	1	2	3	4	5	6
a - Flash memory	No memory	512K	1M	2M	-	-	-
b - PL Reserved (Package type)	QFN56 Entry	QFN56 Base	Reserved	77BGA	64BGA	Reserved	QFN48
c - Temp grade	Consumer	Industrial	Auto	-	-	-	-

8 Packaging

This product line is offered in 48-lead QFN package.

Table 40 Package dimensions

Spec ID#	Package	Description	Package drawing number
PKG_2	48-lead QFN	48-lead QFN, 7.0 × 7.0 × 0.9 mm height with 0.5 mm pitch	002-33925

Table 41 Package characteristics

Parameter	Description	Conditions	Values			Unit
			Min	Typ	Max	
T_A	Operating ambient temperature	-	-40	-	105	°C
T_J	Operating junction temperature		-		125	
T_{JA}	Package Θ_{JA} (48-lead QFN)		-	21.0	-	°C/W
T_{JB}	Package Θ_{JB} (48-lead QFN)			3.9		
T_{JC} (top)	Package Θ_{JC} top (48-lead QFN)			14.1		
T_{JC} (bottom)	Package Θ_{JC} bottom (48-lead QFN)			2.1		

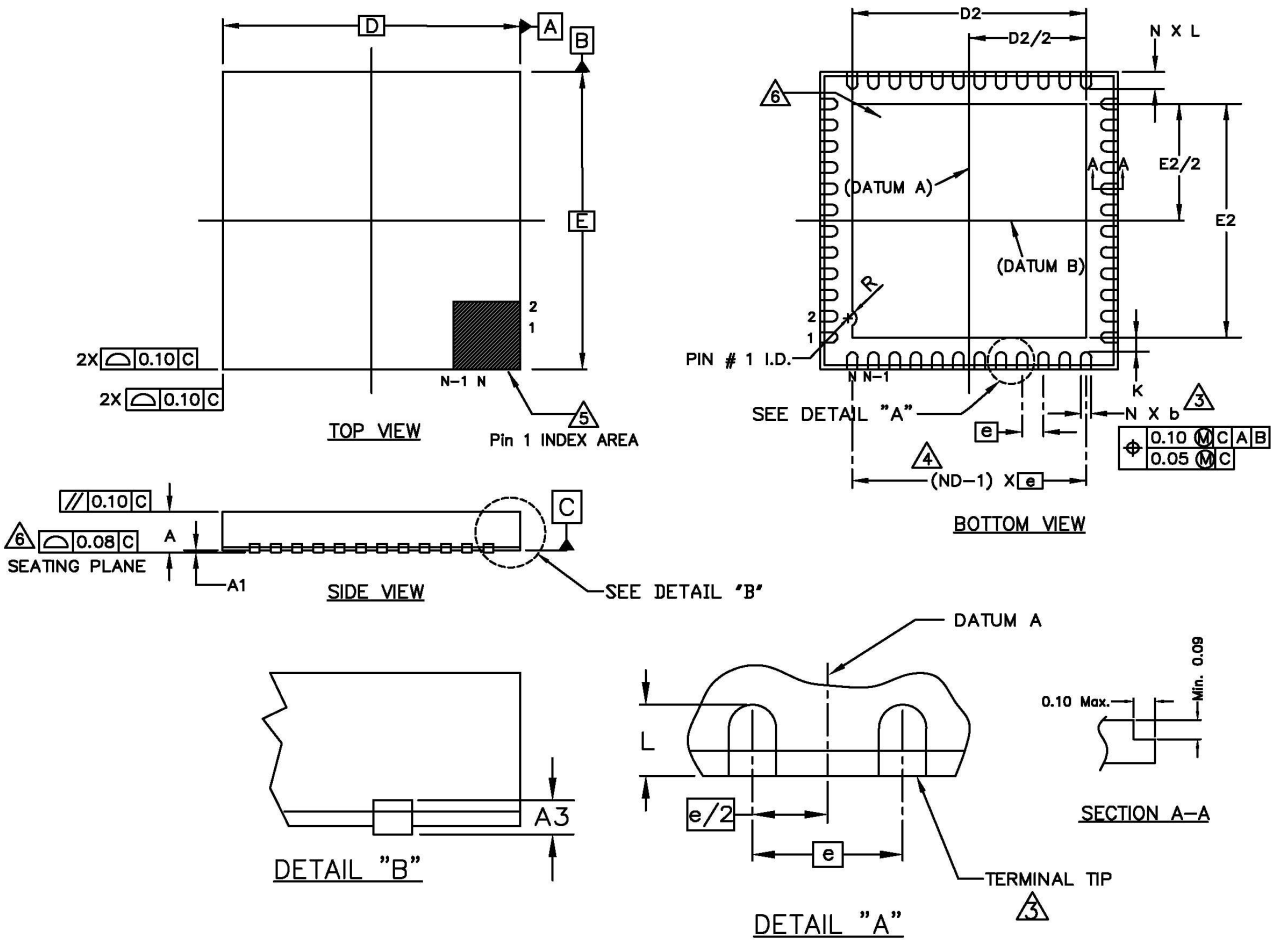
Table 42 Solder reflow peak temperature

Package	Maximum peak temperature	Maximum time at peak temperature
48-lead QFN	260°C	30 s

Table 43 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2

Package	MSL
48-lead QFN	MSL-3

8 Packaging



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
e		0.50 BSC	
N		48	
ND		12	
L	0.30	0.40	0.50
b	0.18	0.25	0.30
D2	5.40	5.50	5.60
E2	5.40	5.50	5.60
D		7.00 BSC	
E		7.00 BSC	
A	-	-	0.90
A1	0.00	-	0.05
A3		0.203 REF	
R		0.20 TYP	
K		0.35 MIN	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE TOTAL NUMBER OF TERMINALS.
3. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
4. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE.
5. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
6. COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
7. JEDEC SPECIFICATION NO. REF. : N/A.

002-33925 Rev. *B

Figure 9 **48-lead QFN (7.0 × 7.0 × 0.9 mm) LV48G (5.5 × 5.5 mm) EPAD (Wettable flank) (PG-VQFN-48)**

9 Document conventions

9.1 Units of measure

Table 44 Units of measure

Symbol	Unit of measure
°C	Degree Celsius
dB	Decibel
fF	Femtofarad
Hz	Hertz
KB	1024 bytes
kbps	Kilobits per second
khr	Kilohour
kHz	Kilohertz
kΩ	Kiloohm
ksps	Kilosamples per second
LSb	Least significant bit
Mbps	Megabits per second
MHz	Megahertz
MΩ	Megaohm
Msps	Megasamples per second
µA	Microampere
µF	Microfarad
µH	Microhenry
µs	Microsecond
µV	Microvolt
µW	Microwatt
mA	Milliampere
ms	Millisecond
mV	Millivolt
nA	Nanoampere
ns	Nanosecond
nV	Nanovolt
Ω	Ohm
pF	Picofarad
ppm	Parts per million

(table continues...)

Table 44 (continued) Units of measure

Symbol	Unit of measure
ps	Picosecond
s	Second
sps	Samples per second
sqrtHz	Square root of hertz
V	Volt

Glossary

3DES
Triple DES (data encryption standard)

ADC
Analog-to-digital converter

AES
Advanced encryption standard

AHB
AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm® data transfer bus

API
Application programming interface

Arm®
Advanced RISC machine, a CPU architecture

BOD
Brown-out detect

BTSS
Bluetooth® sub system

CAD
Computer aided design

CBC
Cipher block chaining

CCO
Current controlled oscillator

CFB
Cipher feedback

CM0+
Cortex®-M0+, an Arm® CPU

CM4
Cortex®-M4, an Arm® CPU

CMOS
Complementary metal-oxide-semiconductor, a process technology for IC fabrication

CPU
Central processing unit

CRC
Cyclic redundancy check, an error-checking protocol

Glossary

CSD
CAPSENSE™ sigma-delta

CTR
Counter

DAC
Digital-to-analog converter, see also IDAC, VDAC

DAP
Debug access port

DES
Data encryption standard

DMA
Direct memory access, see also TD

DNL
Differential nonlinearity, see also INL

DSI
Digital system interconnect

ECB
Electronic code book

ECC
Elliptic curve cryptography

ECDSA
Elliptic curve digital signature algorithm

ECO
External crystal oscillator

EMI
Electromagnetic interference

ESD
Electrostatic discharge

FIFO
First-in, first-out

FLL
Frequency locked loop

FS
Full-speed

GND
Ground

Glossary

GPIO
General-purpose input/output

HMAC
Hash-based message authentication code

HSIOM
High-speed I/O matrix

I/O
Input/output, see also GPIO, DIO, SIO, USBIO

I2C, or IIC
Inter-Integrated Circuit, a communications protocol

I2S
Inter-IC sound

IC
Integrated circuit

IDAC
Current DAC, see also DAC, VDAC

IDE
Integrated development environment

ILO
Internal low-speed oscillator, see also IMO

IMO
Internal main oscillator, see also ILO

INL
Integral nonlinearity, see also DNL

IoT
Internet of things

IPC
Inter-processor communication

IRQ
Interrupt request

JTAG
Joint Test Action Group

LIN
Local Interconnect Network, a communications protocol

LP
Low power

LS
Low-speed

LUT
Lookup table

LVD
Low-voltage detect, see also LVI

LVTTL
Low-voltage transistor-transistor logic

MAC
Multiply-accumulate

MCU
Microcontroller unit

MCWDT
Multi-counter watchdog timer

MISO
Master-in slave-out

MMIO
Memory-mapped input output

MOSI
Master-out slave-in

MPU
Memory protection unit

MSL
Moisture sensitivity level

NMI
Nonmaskable interrupt

NVIC
Nested vectored interrupt controller

OFB
Output feedback

OTP
One-time programmable

OVT
Overvoltage tolerant

PCB
Printed circuit board

PCM
Pulse code modulation

PDM
Pulse density modulation

PHY
Physical layer

PLL
Phase-locked loop

POR
Power-on reset

PRNG
Pseudo random number generator

PSRR
Power supply rejection ratio

PWM
Pulse-width modulator

QSPI
Quad serial peripheral interface

RAM
Random-access memory

RISC
Reduced-instruction-set computing

ROM
Read-only memory

RTC
Real-time clock

RX
Receive

SAR
Successive approximation register

SARMUX
SAR ADC multiplexer bus

SCB
Serial communication block

SHA
Secure hash algorithm

SNR
Signal-to-noise ration

SPI
Serial Peripheral Interface, a communications protocol

SRAM
Static random access memory

SROM
Supervisory read-only memory

SWD
Serial wire debug, a test protocol

SWJ
Serial wire JTAG

SWO
Single wire output

SWV
Serial-wire viewer

TCPWM
Timer, counter, pulse-width modulator

TDM
Time division multiplexed

TRM
Technical reference manual

TRNG
True random number generator

TX
Transmit

UART
Universal Asynchronous Transmitter Receiver, a communications protocol

ULP
Ultra-low power

WCO
Watch crystal oscillator

WDT
Watchdog timer

WIC
Wakeup interrupt controller

Glossary

XIP
Execute-in-place

XRES
External reset input pin

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Document version	Date of release	Description of changes
*C	2026-03-19	Publish to web.

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