

**Please note that Cypress is an Infineon Technologies Company.**

The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

**Continuity of document content**

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

**Continuity of ordering part numbers**

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

The CY9A120L Series are highly integrated 32-bit microcontrollers dedicated for embedded controllers with low-power consumption mode and competitive cost.

These series are based on the ARM® Cortex®-M3 Processor with on-chip Flash memory and SRAM, and have peripheral functions such as various timers, ADCs, DACs and Communication Interfaces (UART, CSIO, I²C, LIN).

The products which are described in this data sheet are placed into TYPE11 product categories in FM3 Family Peripheral Manual.

## Features

### 32-bit ARM® Cortex®-M3 Core

- Processor version: r2p1
- Up to 40 MHz frequency operation
- Integrated Nested Vectored Interrupt Controller (NVIC): 1 NMI (non-maskable interrupt) and 48 peripheral interrupts and 16 priority levels
- 24-bit system timer (Sys Tick): System timer for OS task management

### On-Chip Memories

#### [Flash memory]

- 64 Kbytes
- Read cycle: 0 wait-cycle
- Security function for code protection

#### [SRAM]

This series contains 4 Kbyte on-chip SRAM memories that is connected to System bus of Cortex-M3 core.

- SRAM1: 4 Kbyte

### Multi-function Serial Interface (Max four channels)

- 4 channels without FIFO (ch.0, ch.1, ch.3, ch.5)
- Operation mode is selectable from the followings for each channel.
  - UART
  - CSIO
  - LIN
  - I²C

#### [UART]

- Full duplex double buffer
- Selection with or without parity supported
- Built-in dedicated baud rate generator
- External clock available as a serial clock
- Various error detection functions available (parity errors, framing errors, and overrun errors)

#### [CSIO]

- Full duplex double buffer
- Built-in dedicated baud rate generator
- Overrun error detection function available

#### [LIN]

- LIN protocol Rev.2.1 supported
- Full duplex double buffer
- Master/Slave mode supported
- LIN break field generation (can be changed to 13-bit to 16-bit length)
- LIN break delimiter generation (can be changed to 1-bit to 4-bit length)
- Various error detection functions available (parity errors, framing errors, and overrun errors)

#### [I²C]

Standard-mode (Max 100 kbps) / Fast-mode (Max 400 kbps) supported

## A/D Converter (Max eight channels)

### [12-bit A/D Converter]

- Successive Approximation type
- Conversion time: 0.8  $\mu$ s @ 5 V
- Priority conversion available (priority at 2 levels)
- Scanning conversion mode
- Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for Priority conversion: 4 steps)

### D/A Converter (Max one channel)

- R-2R type
- 10-bit resolution

### Base Timer (Max eight channels)

Operation mode is selectable from the followings for each channel.

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

### General-Purpose I/O Port

This series can use its pins as general-purpose I/O ports when they are not used for peripherals. Moreover, the port relocate function is built-in. It can set which I/O port the peripheral function can be allocated to.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in the port relocate function
- Up to 51 high-speed general-purpose I/O Ports @ 64 pin Package
- Some ports are 5V tolerant
- See List of Pin Functions and I/O Circuit Type to confirm the corresponding pins.

### Dual Timer (32-/16-bit Down Counter)

The Dual Timer consists of two programmable 32-/16-bit down counters.

Operation mode is selectable from the followings for each channel.

- Free-running
- Periodic (=Reload)
- One-shot

## Multi-function Timer

The Multi-function timer is composed of the following blocks.

- 16-bit free-run timer  $\times$  3 ch.
- Input capture  $\times$  3 ch.
- Output compare  $\times$  6 ch.
- A/D activation compare  $\times$  1 ch.
- Waveform generator  $\times$  3 ch.
- 16-bit PPG timer  $\times$  3 ch.  
IGBT mode is contained

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (Motor emergency stop) interrupt function

### Real-time clock (RTC)

The Real-time clock can count

Year/Month/Day/Hour/Minute/Second/A day of the week from 00 to 99.

- The interrupt function with specifying date and time (Year/Month/Day/Hour/Minute) is available. This function is also available by specifying only Year, Month, Day, Hour or Minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

### External Interrupt Controller Unit

- Up to 19 external interrupt input pins @ 64 pin Package
- Include one non-maskable interrupt (NMI) input pin

### Watchdog Timer (Two channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a Hardware watchdog and a Software watchdog.

The Hardware watchdog timer is clocked by the built-in low-speed CR oscillator. Therefore, the Hardware watchdog is active in any low-power consumption modes except RTC, Stop modes.

## Clock and Reset

### [Clocks]

Selectable from five clock sources (2 external oscillators, 2 built-in CR oscillators, and Main PLL).

- Main Clock: 4 MHz to 48 MHz
- Sub Clock: 32.768 kHz
- Built-in high-speed CR Clock: 4 MHz
- Built-in low-speed CR Clock: 100 kHz
- Main PLL Clock

### [Resets]

- Reset requests from INITX pin
- Power-on reset
- Software reset
- Watchdog timers reset
- Low-voltage detection reset
- Clock Super Visor reset

### Clock Super Visor (CSV)

Clocks generated by built-in CR oscillators are used to supervise abnormality of the external clocks.

- If external clock failure (clock stop) is detected, reset is asserted.
- If external frequency anomaly is detected, interrupt or reset is asserted.

### Low-Voltage Detector (LVD)

This Series includes 2-stage monitoring of voltage on the VCC pins. When the voltage falls below the voltage that has been set, Low-Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

### Low-Power Consumption Mode

Four low-power consumption modes supported.

- Sleep
- Timer
- RTC
- Stop

### Debug

Serial Wire JTAG Debug Port (SWJ-DP)

### Unique ID

Unique value of the device (41-bit) is set.

### Power Supply

Wide range voltage: VCC = 2.7 V to 5.5 V

## Contents

<b>1. Product Lineup</b>	<b>6</b>
<b>2. Packages</b>	<b>7</b>
<b>3. Pin Assignment</b>	<b>8</b>
<b>4. List of Pin Functions</b>	<b>9</b>
<b>5. I/O Circuit Type</b>	<b>20</b>
<b>6. Handling Precautions</b>	<b>27</b>
6.1 Precautions for Product Design	27
6.2 Precautions for Package Mounting	28
6.3 Precautions for Use Environment	29
<b>7. Handling Devices</b>	<b>30</b>
<b>8. Block Diagram</b>	<b>32</b>
<b>9. Memory Size</b>	<b>32</b>
<b>10. Memory Map</b>	<b>33</b>
<b>11. Pin Status in Each CPU State</b>	<b>36</b>
<b>12. Electrical Characteristics</b>	<b>41</b>
12.1 Absolute Maximum Ratings	41
12.2 Recommended Operating Conditions	43
12.3 DC Characteristics	44
12.3.1 Current Rating	44
12.3.2 Pin Characteristics	47
12.4 AC Characteristics	48
12.4.1 Main Clock Input Characteristics	48
12.4.2 Sub Clock Input Characteristics	49
12.4.3 Built-in CR Oscillation Characteristics	50
12.4.4 Operating Conditions of Main PLL (In the case of using main clock for input of Main PLL)	51
12.4.5 Operating Conditions of Main PLL (In the case of using built-in high-speed CR for input clock of Main PLL)	51
12.4.6 Reset Input Characteristics	52
12.4.7 Power-on Reset Timing	52
12.4.8 Base Timer Input Timing	53
12.4.9 CSIO/UART Timing	54
12.4.10 External Input Timing	62
12.4.11 I <sup>2</sup> C Timing	63
12.4.12 JTAG Timing	64
12.5 12-bit A/D Converter	65
12.6 10-bit D/A Converter	68
12.7 Low-Voltage Detection Characteristics	69
12.7.1 Low-Voltage Detection Reset	69
12.7.2 Interrupt of Low-Voltage Detection	70
12.8 Flash Memory Write/Erase Characteristics	71
12.8.1 Write / Erase time	71
12.8.2 Write cycles and data hold time	71
12.9 Return Time from Low-Power Consumption Mode	72
12.9.1 Return Factor: Interrupt	72
12.9.2 Return Factor: Reset	74
<b>13. Ordering Information</b>	<b>76</b>
<b>14. Package Dimensions</b>	<b>77</b>
<b>15. Major Changes</b>	<b>78</b>

Document History.....	80
Sales, Solutions, and Legal Information.....	81

## 1. Product Lineup

### Memory Size

Product name		CY9AF121K
On-chip Flash memory		64 Kbytes
On-chip SRAM	SRAM1	4 Kbytes

### Function

Product name			CY9AF121K
Pin count			48
CPU	Cortex-M3		
	Freq.		40 MHz
Power supply voltage range			2.7 V to 5.5 V
Multi-function Serial Interface (UART/CSIO/LIN/I <sup>2</sup> C)			4 ch. (Max) ch.0, ch.1, ch.3, ch.S5: No FIFO (In ch.5, only UART and LIN are available.)
Base Timer (PWC/Reload timer/PWM/PPG)			8 ch. (Max)
MF-Timer	A/D activation compare	1 ch.	1 unit
	Input capture	3 ch.	
	Free-run timer	3 ch.	
	Output compare	6 ch.	
	Waveform generator	3 ch.	
	PPG (IGBT mode)	3 ch.	
Dual Timer			1 unit
Real-Time Clock			1 unit
Watchdog timer			1 ch. (SW) + 1 ch. (HW)
External Interrupts			14 pins (Max) + NMI × 1
I/O ports			36 pins (Max)
12-bit A/D converter			8 ch. (1 unit)
10-bit D/A converter			1 ch. (Max)
CSV (Clock Super Visor)			Yes
LVD (Low-Voltage Detector)			2 ch.
Built-in CR	High-speed		4 MHz
	Low-speed		100 kHz
Debug Function			SWJ-DP
Unique ID			Yes

### Note:

- All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use. See Electrical Characteristics 12.4 AC Characteristics 12.4.3 Built-in CR Oscillation Characteristics for accuracy of built-in CR.

## 2. Packages

Package	Product name
LQFP: LQA048 (0.5 mm pitch)	CY9AF121K
	○

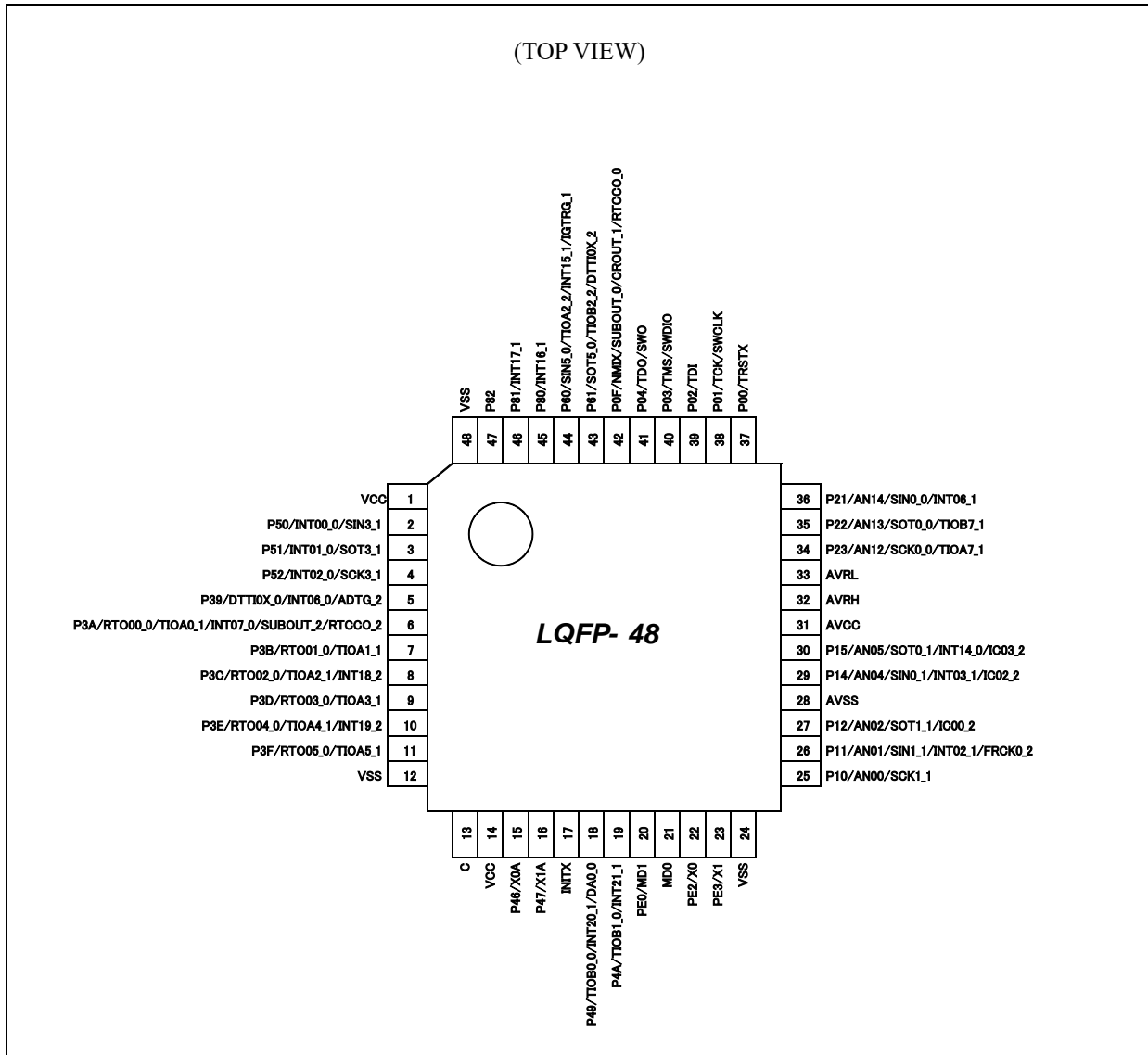
○: Supported

**Note:**

- See *Package Dimensions* for detailed information on each package.

### 3. Pin Assignment

LQA048



**Note:**

- The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

## 4. List of Pin Functions

### List of pin numbers

The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No LQFP-48	Pin Name	I/O circuit type	Pin state type
1	VCC	-	
2	P50 INT00_0 SIN3_1	H*1	K
3	P51 INT01_0 SOT3_1 (SDA3_1)	H*2	K
4	P52 INT02_0 SCK3_1 (SCL3_1)	H*2	K
-	P30 TIOB0_1 INT03_2	E	K
-	P31 TIOB1_1 INT04_2	E	K
-	P32 TIOB2_1 INT05_2	E	K
-	P33 INT04_0 TIOB3_1 ADTG_6	E	K
5	P39 DTTIOX_0 INT06_0 ADTG_2	E	K
6	P3A RTO00_0 (PPG00_0) TIOA0_1 INT07_0 SUBOUT_2 RTCCO_2	G	K
7	P3B RTO01_0 (PPG00_0) TIOA1_1	G	J

Pin No	Pin Name	I/O circuit type		Pin state type
LQFP-48				
8	P3C	G		K
	RTO02_0 (PPG02_0)			
	TIOA2_1			
	INT18_2			
9	P3D	G		J
	RTO03_0 (PPG02_0)			
	TIOA3_1			
10	P3E	G		K
	RTO04_0 (PPG04_0)			
	TIOA4_1			
	INT19_2			
11	P3F	G		J
	RTO05_0 (PPG04_0)			
	TIOA5_1			
12	VSS	-		
13	C	-		
14	VCC	-		
15	P46	D		F
	X0A			
16	P47	D		G
	X1A			
17	INITX	B		C
18	P49	K		K
	TIOB0_0			
	INT20_1			
	DA0_0			
-	SOT3_2 (SDA3_2)			
19	P4A	E		K
	TIOB1_0			
	INT21_1			
-	SCK3_2 (SCL3_2)			
-	P4B	E		K
	TIOB2_0			
	INT22_1			
	IGTRG_0			
-	P4C	E		K
	TIOB3_0			
	INT12_0			
-	P4D	E		K
	TIOB4_0			
	INT13_0			

Pin No	Pin Name	I/O circuit type	Pin state type
LQFP-48			
-	P4E	E	K
	TIOB5_0		
	INT06_2		
20	PE0	C	E
	MD1		
21	MD0	J	D
22	PE2	A	A
	X0		
23	PE3	A	B
	X1		
24	VSS	-	
-	VCC	-	
25	P10	F	L
	AN00		
	SCK1_1 (SCL1_1)		
26	P11	F	M
	AN01		
	SIN1_1		
	INT02_1		
27	FRCK0_2	F	L
	P12		
	AN02		
	SOT1_1 (SDA1_1)		
28	IC00_2	F	L
	AVSS		
29	P14	F	M
	AN04		
	SIN0_1		
	INT03_1		
	IC02_2		
30	P15	F	M
	AN05		
	SOT0_1 (SDA0_1)		
	INT14_0		
	IC03_2		
-	P17	E	K
	INT04_1		
31	AVCC	-	
32	AVRH	-	
33	AVRL	-	
-	P18	E	J
-	P19	E	J

Pin No LQFP-48	Pin Name	I/O circuit type	Pin state type
34	P23	I*2	M
	AN12		
	SCK0_0 (SCL0_0)		
	TIOA7_1		
35	P22	I*2	M
	AN13		
	SOT0_0 (SDA0_0)		
	TIOB7_1		
36	P21	I*1	M
	AN14		
	SIN0_0		
	INT06_1		
37	P00	E	I
	TRSTX		
38	P01	E	I
	TCK		
	SWCLK		
39	P02	E	I
	TDI		
40	P03	E	I
	TMS		
	SWDIO		
41	P04	E	I
	TDO		
	SWO		
-	P0A	E	K
	INT00_2		
-	P0B	E	K
	TIOB6_1		
	INT18_0		
-	P0C	E	K
	TIOA6_1		
	INT19_0		
42	P0F	E	H
	NMIX		
	SUBOUT_0		
	CROUT_1		
	RTCCO_0		
-	P62	E	J
	SCK5_0 (SCL5_0)		
	ADTG_3		

Pin No LQFP-48	Pin Name	I/O circuit type	Pin state type
43	P61	E	J
	SOT5_0 (SDA5_0)		
	TIOB2_2		
	DTTIOX_2		
44	P60	I*2	K
	SIN5_0		
	TIOA2_2		
	INT15_1		
	IGTRG_1		
45	P80	L	K
	INT16_1		
46	P81	L	K
	INT17_1		
47	P82	L	J
48	VSS	-	
-	NC	-	

\*1: 5 V tolerant I/O, without PZR function

\*2: 5 V tolerant I/O, with PZR function

**List of pin functions**

The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin function	Pin name	Function description	Pin No
			LQFP-48 QFN-48
ADC	ADTG_2	A/D converter external trigger input pin	5
	ADTG_3		-
	ADTG_6		-
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	25
	AN01		26
	AN02		27
	AN04		29
	AN05		30
	AN12		34
	AN13		35
	AN14		36
Base Timer 0	TIOA0_1	Base timer ch.0 TIOA pin	6
	TIOB0_0	Base timer ch.0 TIOB pin	18
	TIOB0_1		-
Base Timer 1	TIOA1_1	Base timer ch.1 TIOA pin	7
	TIOB1_0	Base timer ch.1 TIOB pin	19
	TIOB1_1		-
Base Timer 2	TIOA2_1	Base timer ch.2 TIOA pin	8
	TIOA2_2		44
	TIOB2_0	Base timer ch.2 TIOB pin	-
	TIOB2_1		-
	TIOB2_2		43
Base Timer 3	TIOA3_1	Base timer ch.3 TIOA pin	9
	TIOB3_0	Base timer ch.3 TIOB pin	-
	TIOB3_1		-
Base Timer 4	TIOA4_1	Base timer ch.4 TIOA pin	10
	TIOB4_0	Base timer ch.4 TIOB pin	-
Base Timer 5	TIOA5_1	Base timer ch.5 TIOA pin	11
	TIOB5_0	Base timer ch.5 TIOB pin	-
Base Timer 6	TIOA6_1	Base timer ch.6 TIOA pin	-
	TIOB6_1	Base timer ch.6 TIOB pin	-
Base Timer 7	TIOA7_1	Base timer ch.7 TIOA pin	34
	TIOB7_1	Base timer ch.7 TIOB pin	35
Debugger	SWCLK	Serial wire debug interface clock input pin	38
	SWDIO	Serial wire debug interface data input / output pin	40
	SWO	Serial wire viewer output pin	41
	TCK	JTAG test clock input pin	38
	TDI	JTAG test data input pin	39
	TDO	JTAG debug data output pin	41
	TMS	JTAG test mode state input/output pin	40
	TRSTX	JTAG test reset input pin	37

Pin function	Pin name	Function description	Pin No
			LQFP-48 QFN-48
External Interrupt	INT00_0	External interrupt request 00 input pin	2
	INT00_2		-
	INT01_0	External interrupt request 01 input pin	3
	INT02_0	External interrupt request 02 input pin	4
	INT02_1		26
	INT03_1	External interrupt request 03 input pin	29
	INT03_2		-
	INT04_0		-
	INT04_1	External interrupt request 04 input pin	-
	INT04_2		-
	INT05_2	External interrupt request 05 input pin	-
	INT06_0	External interrupt request 06 input pin	5
	INT06_1		36
	INT06_2		-
	INT07_0	External interrupt request 07 input pin	6
	INT12_0	External interrupt request 12 input pin	-
	INT13_0	External interrupt request 13 input pin	-
	INT14_0	External interrupt request 14 input pin	30
	INT15_1	External interrupt request 15 input pin	44
	INT16_1	External interrupt request 16 input pin	45
	INT17_1	External interrupt request 17 input pin	46
	INT18_0	External interrupt request 18 input pin	-
	INT18_2		8
	INT19_0	External interrupt request 19 input pin	-
	INT19_2		10
	INT20_1	External interrupt request 20 input pin	18
	INT21_1	External interrupt request 21 input pin	19
	INT22_1	External interrupt request 22 input pin	-
	NMIX	Non-Maskable Interrupt input pin	42

Pin function	Pin name	Function description	Pin No
			LQFP-48 QFN-48
GPIO	P00	General-purpose I/O port 0	37
	P01		38
	P02		39
	P03		40
	P04		41
	P0A		-
	P0B		-
	P0C		-
	P0F		42
	P10	General-purpose I/O port 1	25
	P11		26
	P12		27
	P14		29
	P15		30
	P17		-
	P18		-
	P19		-
	P21	General-purpose I/O port 2	36
	P22		35
	P23		34
	P30	General-purpose I/O port 3	-
	P31		-
	P32		-
	P33		-
	P39		5
	P3A		6
	P3B		7
	P3C		8
	P3D		9
	P3E		10
	P3F		11
	P46	General-purpose I/O port 4	15
	P47		16
	P49		18
	P4A		19
	P4B		-
	P4C		-
	P4D		-
	P4E		-
	P50	General-purpose I/O port 5	2
	P51		3
	P52		4
	P60	General-purpose I/O port 6	44
	P61		43
	P62		-
	P80	General-purpose I/O port 8	45
	P81		46
	P82		47
	PE0	General-purpose I/O port E	20
	PE2		22
	PE3		23

Pin function	Pin name	Function description	Pin No
			LQFP-48 QFN-48
Multi-function Serial 0	SIN0_0	Multi-function serial interface ch.0 input pin	36
	SIN0_1		29
	SOT0_0 (SDA0_0)	Multi-function serial interface ch.0 output pin. This pin operates as SOT0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA0 when it is used in an I <sup>2</sup> C (operation mode 4).	35
	SOT0_1 (SDA0_1)		30
	SCK0_0 (SCL0_0)	Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a CSIO (operation mode 2) and as SCL0 when it is used in an I <sup>2</sup> C (operation mode 4).	34
Multi-function Serial 1	SIN1_1	Multi-function serial interface ch.1 input pin	26
	SOT1_1 (SDA1_1)	Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA1 when it is used in an I <sup>2</sup> C (operation mode 4).	27
	SCK1_1 (SCL1_1)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a CSIO (operation mode 2) and as SCL1 when it is used in an I <sup>2</sup> C (operation mode 4).	25
Multi-function Serial 3	SIN3_1	Multi-function serial interface ch.3 input pin	2
	SOT3_1 (SDA3_1)	Multi-function serial interface ch.3 output pin. This pin operates as SOT3 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA3 when it is used in an I <sup>2</sup> C (operation mode 4).	3
	SOT3_2 (SDA3_2)		-
	SCK3_1 (SCL3_1)	Multi-function serial interface ch.3 clock I/O pin. This pin operates as SCK3 when it is used in a CSIO (operation mode 2) and as SCL3 when it is used in an I <sup>2</sup> C (operation mode 4).	4
	SCK3_2 (SCL3_2)		-

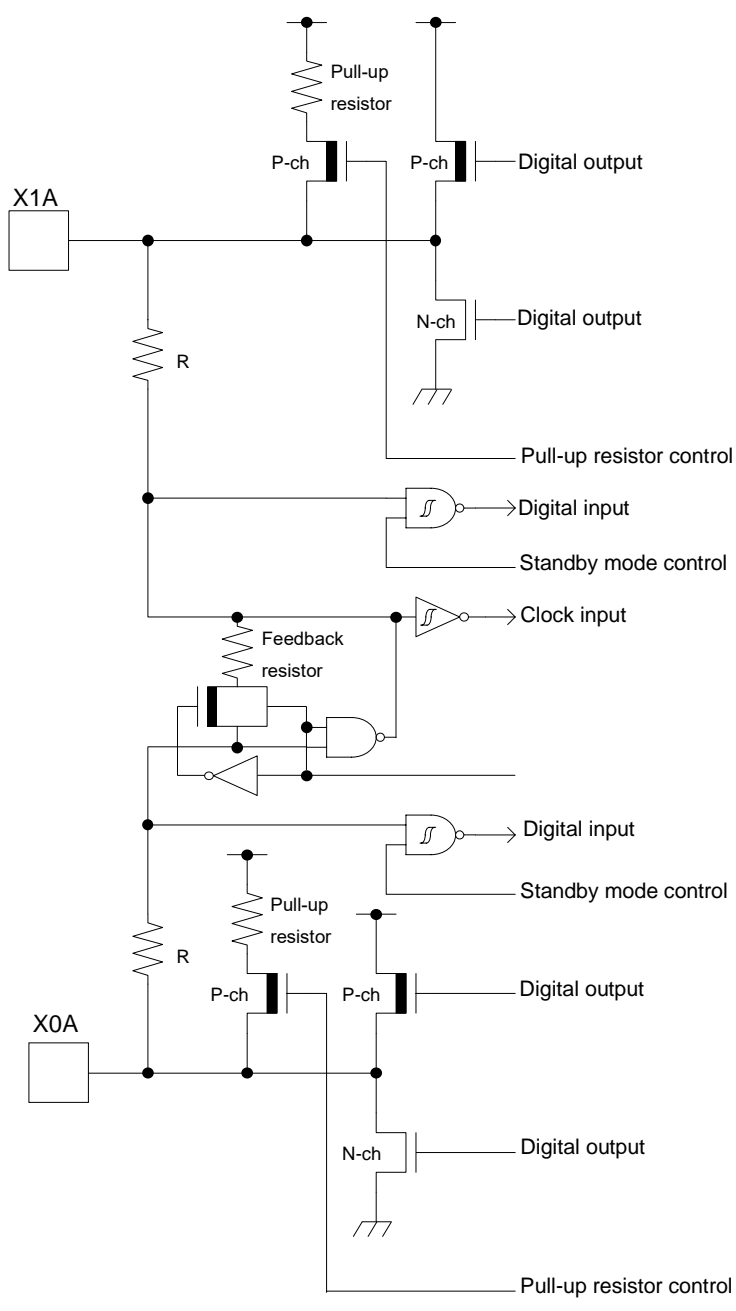
Pin function	Pin name	Function description	Pin No
			LQFP-48 QFN-48
Multi-function Serial 5	SIN5_0	Multi-function serial interface ch.5 input pin	44
	SOT5_0 (SDA5_0)	Multi-function serial interface ch.5 output pin. This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an I <sup>2</sup> C (operation mode 4).	43
	SCK5_0 (SCL5_0)	Multi-function serial interface ch.5 clock I/O pin. This pin operates as SCK5 when it is used in a CSIO (operation mode 2) and as SCL5 when it is used in an I <sup>2</sup> C (operation mode 4).	-
Multi-function Timer 0	DTTIOX_0	Input signal of waveform generator to control outputs RTO00 to RTO05 of Multi-function timer 0.	5
	DTTIOX_2		43
	FRCK0_2	16-bit free-run timer ch.0 external clock input pin	26
	IC00_2	16-bit input capture input pin of Multi-function timer 0. ICxx describes channel number.	27
	IC02_2		29
	IC03_2		30
	RTO00_0 (PPG00_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output mode.	6
	RTO01_0 (PPG00_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output mode.	7
	RTO02_0 (PPG02_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output mode.	8
	RTO03_0 (PPG02_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output mode.	9
	RTO04_0 (PPG04_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output mode.	10
	RTO05_0 (PPG04_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output mode.	11
	IGTRG_0	PPG IGBT mode external trigger input pin	-
	IGTRG_1		44

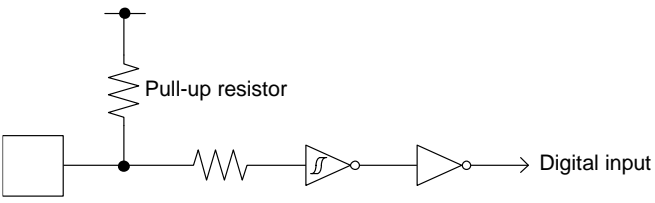
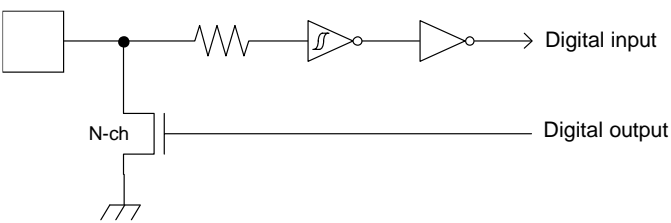
Pin function	Pin name	Function description	Pin No
			LQFP-48 QFN-48
Real-time clock	RTCCO_0	0.5 seconds pulse output pin of Real-time clock	42
	RTCCO_2		6
	SUBOUT_0	Sub clock output pin	42
	SUBOUT_2		6
DAC	DA0_0	D/A converter ch.0 analog output pin	18
Reset	INITX	External Reset Input pin. A reset is valid when INITX="L".	17
Mode	MD0	Mode 0 pin. During normal operation, MD0="L" must be input. During serial programming to Flash memory, MD0="H" must be input.	21
	MD1	Mode 1 pin. During serial programming to Flash memory, MD1="L" must be input.	20
Power	VCC	Power supply Pin	1
			14
			-
GND	VSS	GND Pin	12
			24
			48
Clock	X0	Main clock (oscillation) input pin	22
	X0A	Sub clock (oscillation) input pin	15
	X1	Main clock (oscillation) I/O pin	23
	X1A	Sub clock (oscillation) I/O pin	16
	CROUT_1	Built-in high-speed CR-osc clock output port	42
Analog Power	AVCC	A/D converter and D/A converter analog power supply pin	31
	AVRH	A/D converter analog reference voltage input pin	32
Analog GND	AVSS	A/D converter and D/A converter GND pin	28
	AVRL	A/D converter analog reference voltage input pin	33
C pin	C	Power supply stabilization capacity pin	13

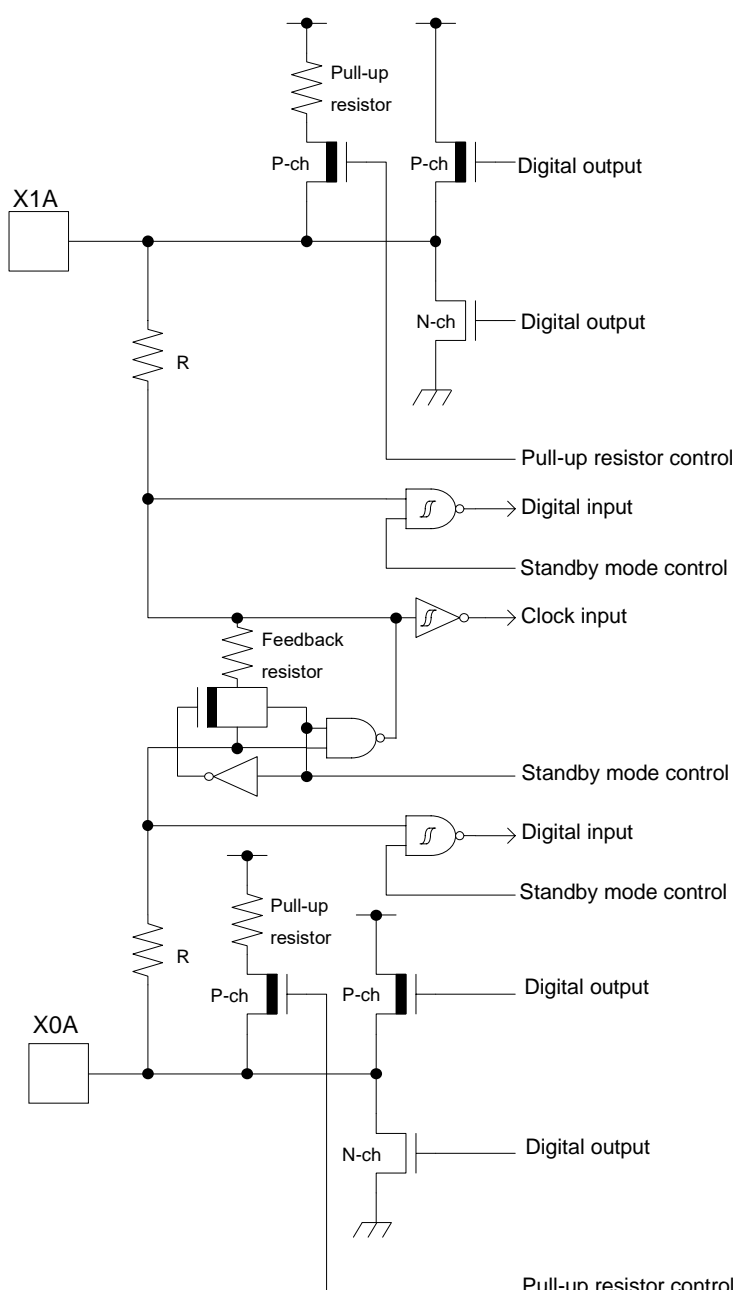
**Note:**

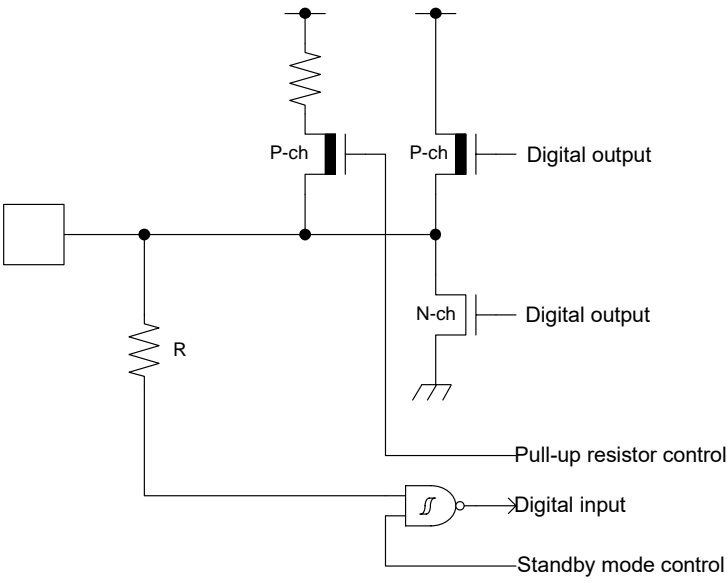
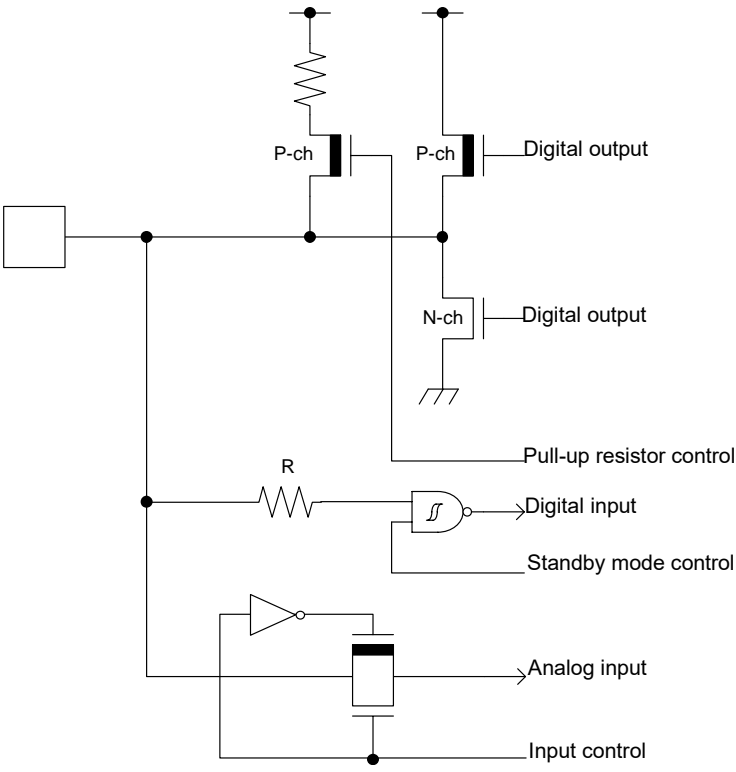
- While this device contains a Test Access Port (TAP) based on the IEEE 1149.1-2001 JTAG standard, it is not fully compliant to all requirements of that standard. This device may contain a 32-bit device ID that is the same as the 32-bit device ID in other devices with different functionality. The TAP pins may also be configurable for purposes other than access to the TAP controller.

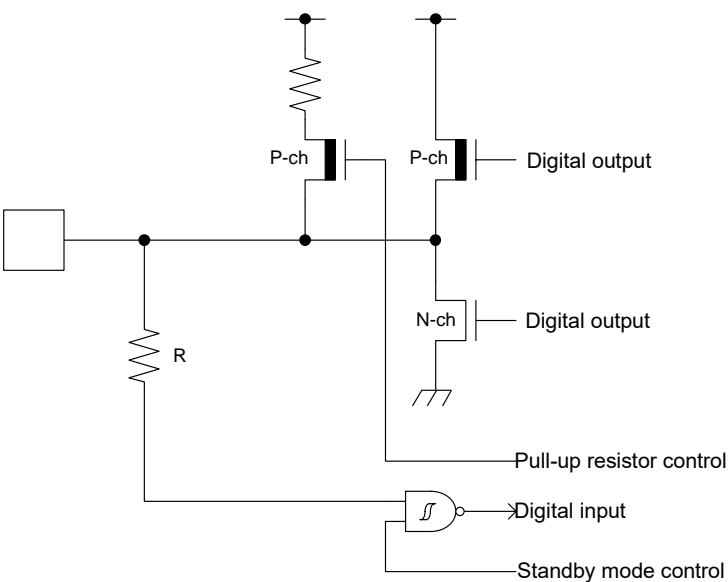
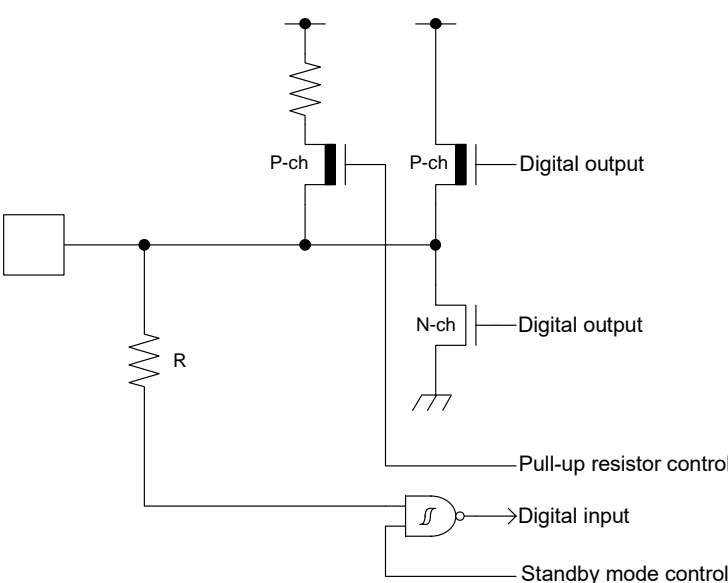
## 5. I/O Circuit Type

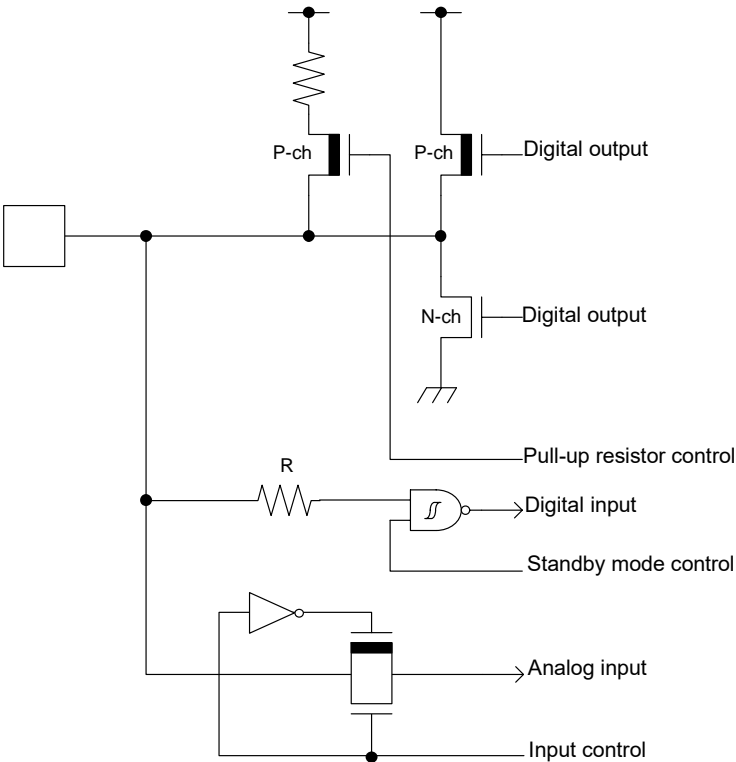
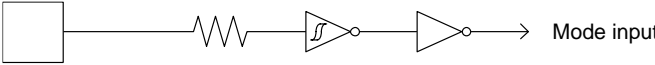
Type	Circuit	Remarks
A	 <p>The diagram illustrates the internal circuitry for I/O Type A. It features two oscillators, X1A and X0A, which are connected to various pins. X1A is connected to a pull-up resistor, a P-ch MOSFET (Digital output), an N-ch MOSFET (Digital output), a resistor R, a Digital input, a Standby mode control, a Clock input, a Feedback resistor, and another Digital input. X0A is connected to a pull-up resistor, a P-ch MOSFET (Digital output), an N-ch MOSFET (Digital output), a resistor R, a Standby mode control, and a Digital output. The diagram also shows internal logic like AND gates and inverters.</p>	<p>It is possible to select the main oscillation / GPIO function</p> <p>When the main oscillation is selected.</p> <ul style="list-style-type: none"> <li>Oscillation feedback resistor : Approximately 1 MΩ</li> <li>With Standby mode control</li> </ul> <p>When the GPIO is selected.</p> <ul style="list-style-type: none"> <li>CMOS level output.</li> <li>CMOS level hysteresis input</li> <li>With pull-up resistor control</li> <li>With standby mode control</li> <li>Pull-up resistor : Approximately 50 kΩ</li> <li><math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> </ul>

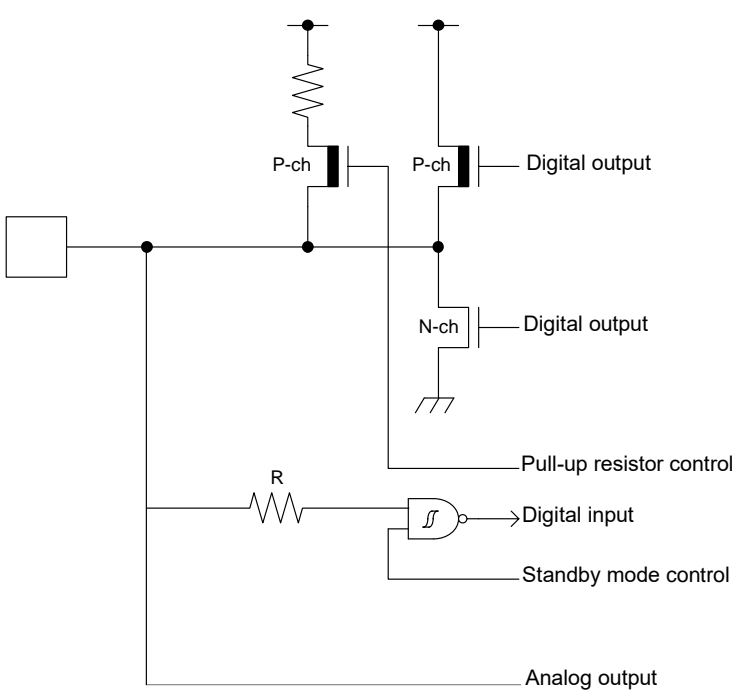
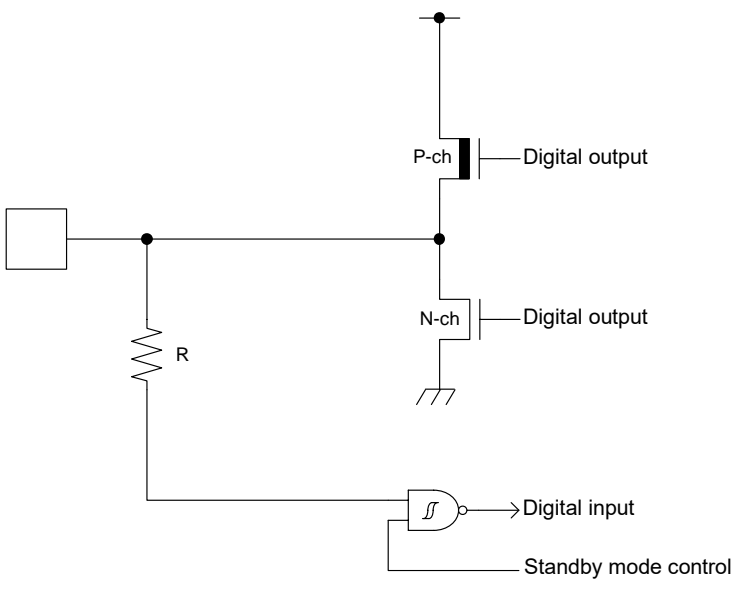
Type	Circuit	Remarks
B	 <p>Pull-up resistor</p> <p>Digital input</p>	<ul style="list-style-type: none"> <li>• CMOS level hysteresis input</li> <li>• Pull-up resistor : Approximately 50 kΩ</li> </ul>
C	 <p>Digital input</p> <p>Digital output</p> <p>N-ch</p>	<ul style="list-style-type: none"> <li>• Open drain output</li> <li>• CMOS level hysteresis input</li> </ul>

Type	Circuit	Remarks
D	 <p>The circuit diagram illustrates the internal connections for Type D. It features two oscillators, X1A and X0A. X1A is connected to a pull-up resistor, a P-ch MOSFET, an N-ch MOSFET, a digital input, a clock input, and a standby mode control. X0A is connected to a pull-up resistor, a P-ch MOSFET, an N-ch MOSFET, a digital input, a standby mode control, and a pull-up resistor control. The diagram also shows a feedback resistor, a digital output, and a pull-up resistor control.</p>	<p>It is possible to select the sub oscillation / GPIO function</p> <p>When the sub oscillation is selected.</p> <ul style="list-style-type: none"> <li>• Oscillation feedback resistor : Approximately 5 MΩ</li> <li>• With Standby mode control</li> </ul> <p>When the GPIO is selected.</p> <ul style="list-style-type: none"> <li>• CMOS level output.</li> <li>• CMOS level hysteresis input</li> <li>• With pull-up resistor control</li> <li>• With standby mode control</li> <li>• Pull-up resistor : Approximately 50 kΩ</li> <li>• I<sub>OH</sub>= -4 mA, I<sub>OL</sub>= 4 mA</li> </ul>

Type	Circuit	Remarks
E		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With pull-up resistor control</li> <li>• With standby mode control</li> <li>• Pull-up resistor : Approximately 50 kΩ</li> <li>• <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> <li>• When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off</li> <li>• +B input is available</li> </ul>
F		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With input control</li> <li>• Analog input</li> <li>• With pull-up resistor control</li> <li>• With standby mode control</li> <li>• Pull-up resistor : Approximately 50 kΩ</li> <li>• <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> <li>• When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off</li> <li>• +B input is available</li> </ul>

Type	Circuit	Remarks
G		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With pull-up resistor control</li> <li>• With standby mode control</li> <li>• Pull-up resistor : Approximately 50 kΩ</li> <li>• <math>I_{OH} = -12 \text{ mA}</math>, <math>I_{OL} = 12 \text{ mA}</math></li> <li>• +B input is available</li> </ul>
H		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• 5 V tolerant</li> <li>• With pull-up resistor control</li> <li>• With standby mode control</li> <li>• Pull-up resistor : Approximately 50 kΩ</li> <li>• <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> <li>• Available to control PZR registers.</li> <li>• Only P51, P52.</li> <li>• When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off</li> </ul>

Type	Circuit	Remarks
I		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With input control</li> <li>• Analog input</li> <li>• 5 V tolerant</li> <li>• With pull-up resistor control</li> <li>• With standby mode control</li> <li>• Pull-up resistor : Approximately 50 kΩ</li> <li>• <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> <li>• Available to control PZR registers. Only P23, P22, P60.</li> <li>• When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off</li> </ul>
J		CMOS level hysteresis input

Type	Circuit	Remarks
K		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With input control</li> <li>• Analog output</li> <li>• With pull-up resistor control</li> <li>• With standby mode control</li> <li>• Pull-up resistor : Approximately 50 kΩ</li> <li>• <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> <li>• When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off</li> </ul>
L		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With standby mode control</li> <li>• <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> </ul>

## 6. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

### 6.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

#### Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

#### Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

#### Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

2. Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device. Therefore, avoid this type of connection.

3. Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

#### Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNP junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

**CAUTION:** The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

#### Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

#### Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

## **Precautions Related to Usage of Devices**

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

**CAUTION:** Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

## **6.2 Precautions for Package Mounting**

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress' recommended conditions. For detailed information about mount conditions, contact your sales representative.

### **Lead Insertion Type**

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

### **Surface Mount Type**

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

### **Lead-Free Packaging**

**CAUTION:** When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

## **Storage of Semiconductor Devices**

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.  
When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

## **Baking**

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

**Static Electricity**

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).  
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

**6.3 Precautions for Use Environment**

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity  
Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.
2. Discharge of Static Electricity  
When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.
3. Corrosive Gases, Dust, or Oil  
Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.
4. Radiation, Including Cosmic Radiation  
Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.
5. Smoke, Flame  
CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

## 7. Handling Devices

### Power supply pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each Power supply pin and GND pin of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1  $\mu\text{F}$  be connected as a bypass capacitor between each Power supply pin and GND pin, between AVCC pin and AVSS pin, between AVRH pin and AVRRL pin near this device.

### Stabilizing power supply voltage

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the recommended operating conditions of the VCC power supply voltage. As a rule, with voltage stabilization, suppress the voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the VCC value in the recommended operating conditions, and the transient fluctuation rate does not exceed 0.1 V/ $\mu\text{s}$  when there is a momentary fluctuation on switching the power supply.

### Crystal oscillator circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator, and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

### Sub crystal oscillator

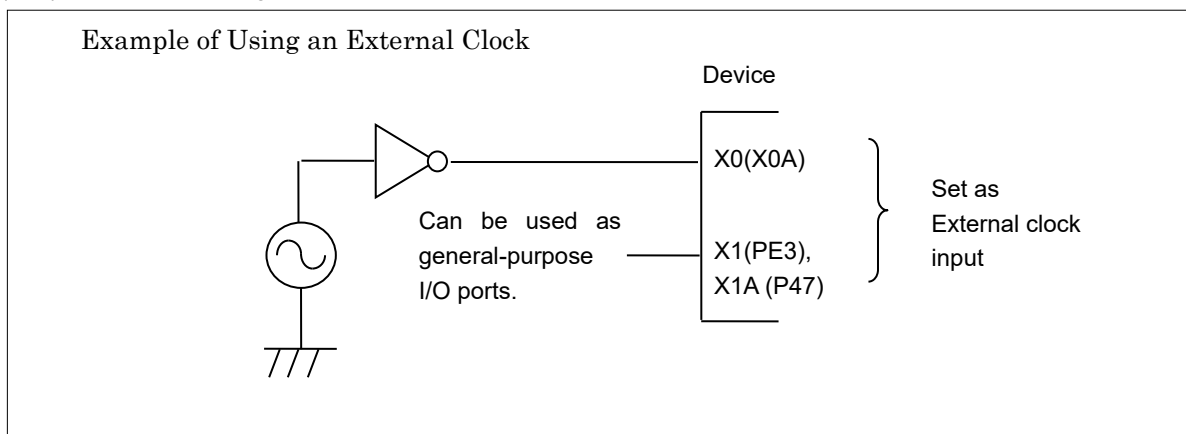
This series sub oscillator circuit is low gain to keep the low current consumption. The crystal oscillator to fill the following conditions is recommended for sub crystal oscillator to stabilize the oscillation.

- Surface mount type
  - Size: More than 3.2 mm  $\times$  1.5 mm
  - Load capacitance: Approximately 6 pF to 7 pF
- Lead type
  - Load capacitance: Approximately 6 pF to 7 pF

### Using an external clock

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1(PE3) can be used as a general-purpose I/O port.

Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input, and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.



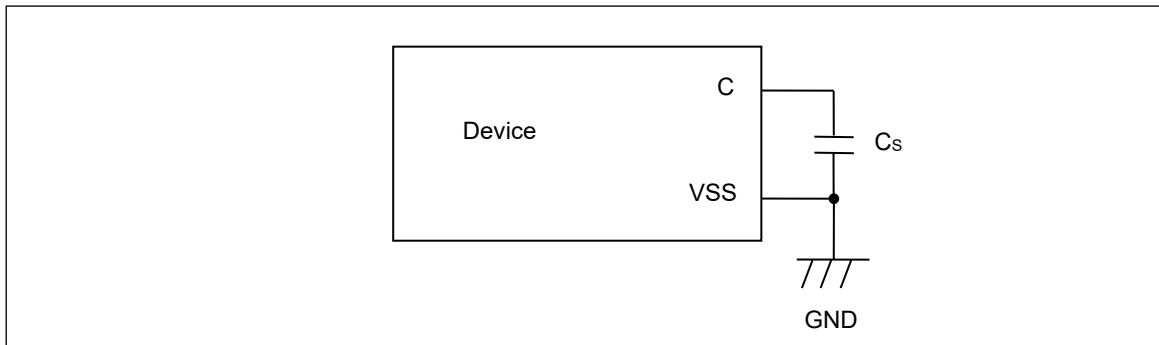
### Handling when using Multi-function serial pin as I<sup>2</sup>C pin

If it is using the multi-function serial pin as I<sup>2</sup>C pins, P-ch transistor of digital output is always disabled. However, I<sup>2</sup>C pins need to keep the electrical characteristic like other pins and not to connect to the external I<sup>2</sup>C bus system with power OFF.

### C Pin

This series contains the regulator. Be sure to connect a smoothing capacitor (C<sub>s</sub>) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor. However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor.

A smoothing capacitor of about 4.7  $\mu$ F would be recommended for this series.



### Mode pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

### Notes on power-on

Turn power on/off in the following order or at the same time.

If not using the A/D converter and D/A converter, connect AVCC = VCC and AVSS = VSS.

Turning on : VCC → AVCC → AVRH

Turning off : AVRH → AVCC → VCC

### Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.

Therefore, design a printed circuit board so as to avoid noise.

Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end. If an error is detected, retransmit the data.

### Differences in features among the products with different memory sizes and between Flash memory products and MASK products

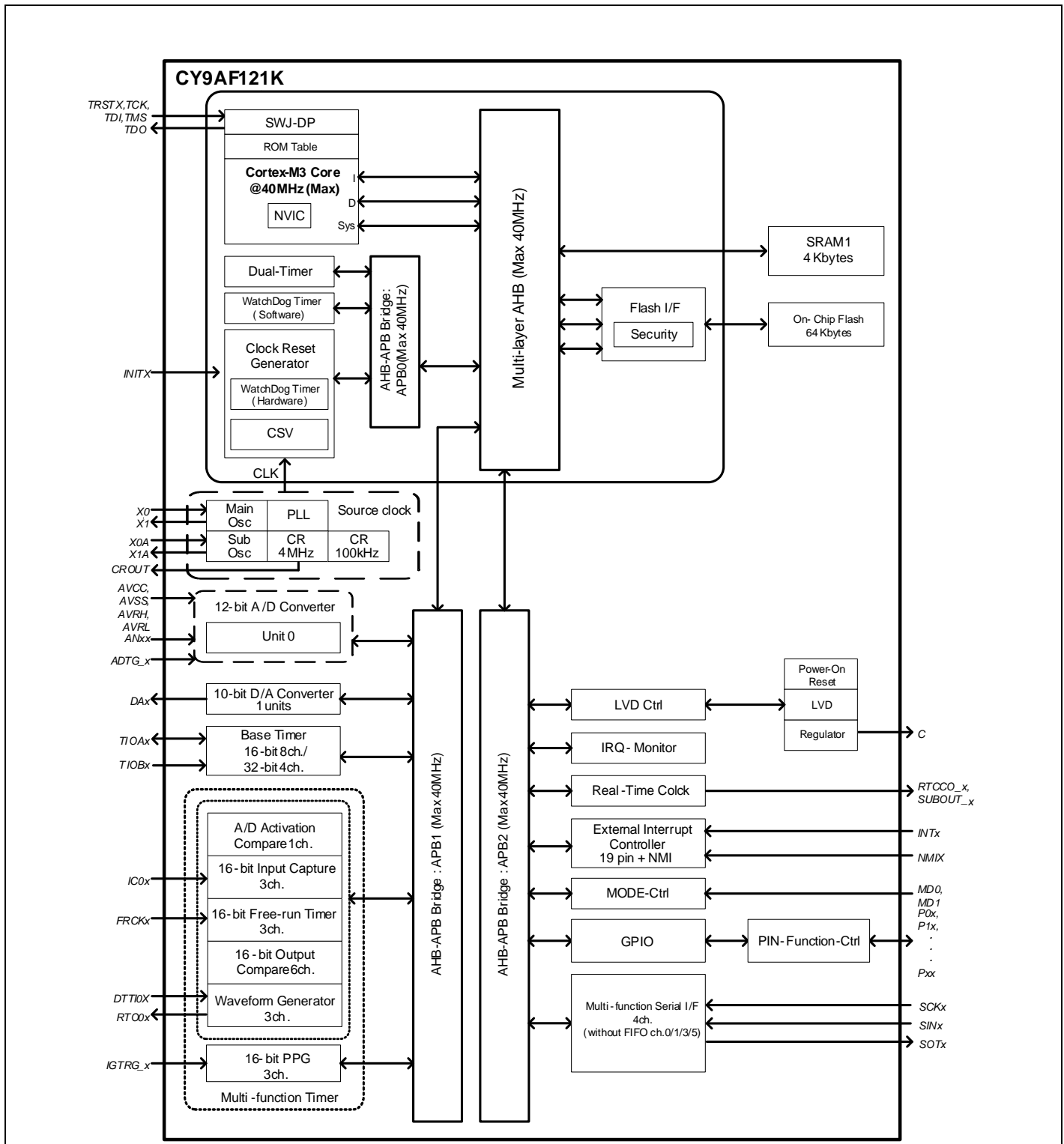
The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash memory products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

### Pull-Up function of 5 V tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5 V tolerant I/O.

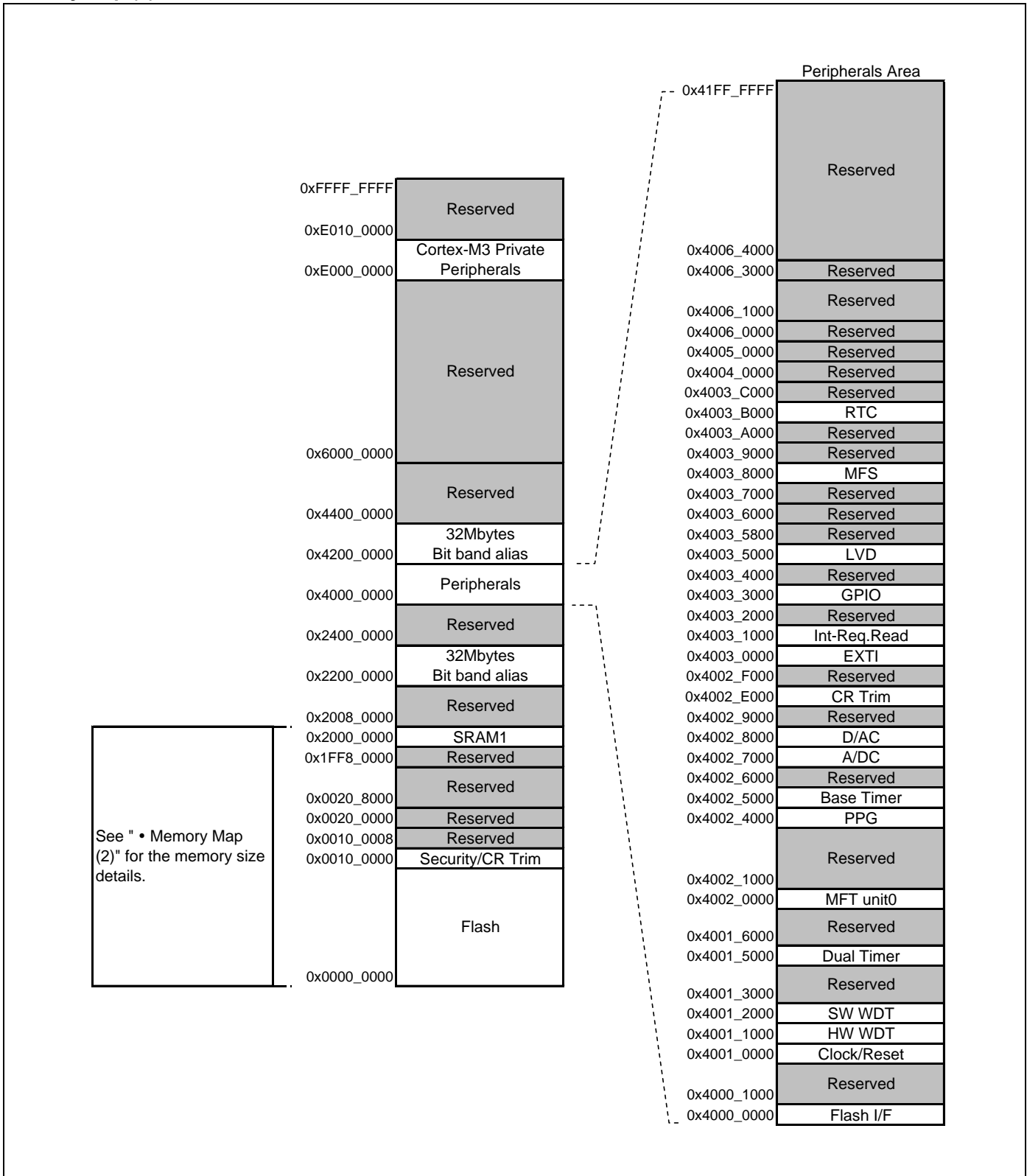
## 8. Block Diagram

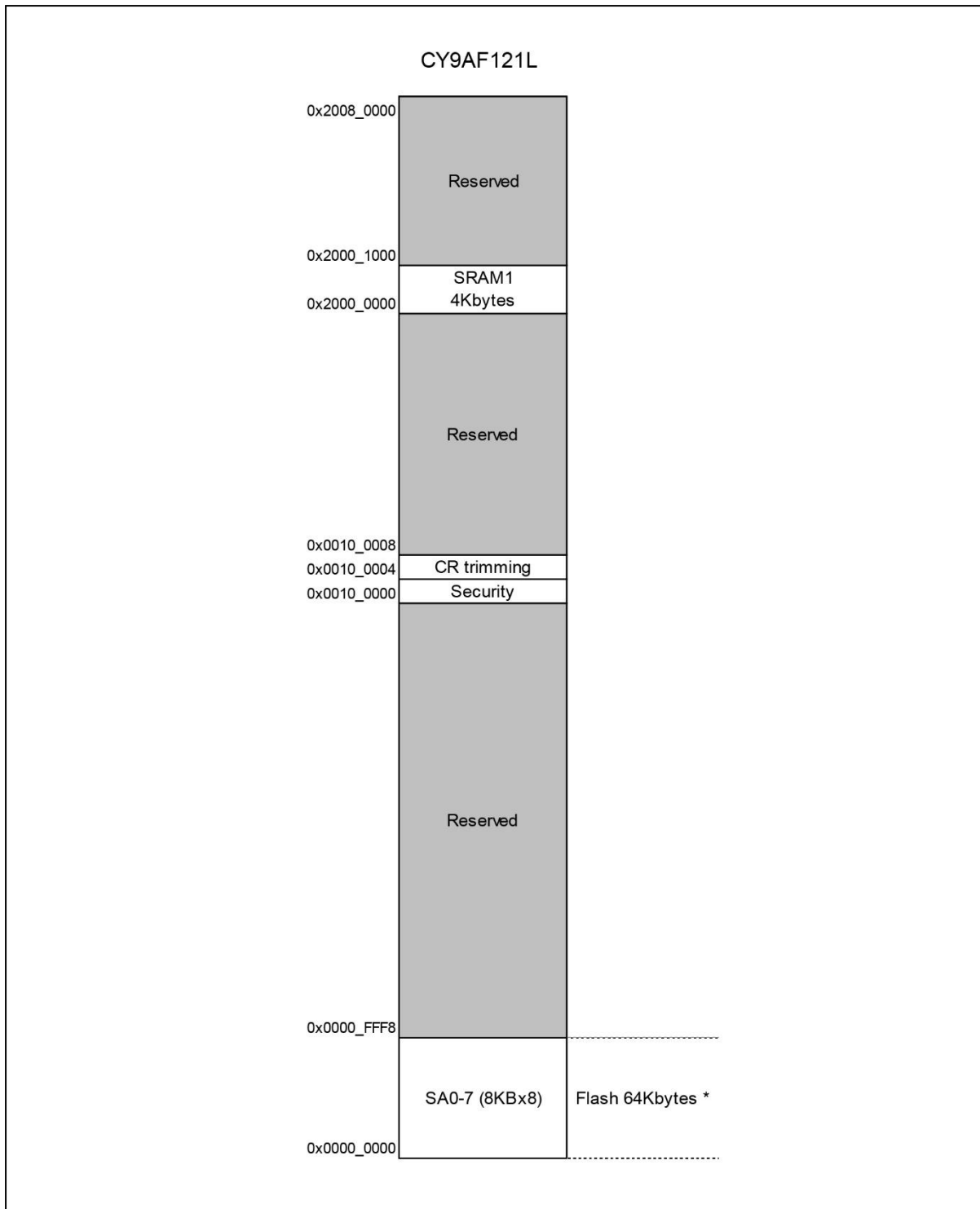


## 9. Memory Size

See Memory size in Product Lineup to confirm the memory size.

## Memory Map (1)



**Memory Map (2)**


\*: See CY9A420L/120L/CY9B120J SERIES FM3 FLASH PROGRAMMING SPECIFICATIONS to confirm the detail of Flash memory.

**Peripheral Address Map**

Start address	End address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	Flash Memory I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control
0x4001_1000	0x4001_1FFF		Hardware Watchdog timer
0x4001_2000	0x4001_2FFF		Software Watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-Timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-function timer unit0
0x4002_1000	0x4002_3FFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base Timer
0x4002_6000	0x4002_6FFF		Reserved
0x4002_7000	0x4002_7FFF		A/D Converter
0x4002_8000	0x4002_8FFF		D/A Converter
0x4002_9000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Built-in CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF	APB2	External Interrupt
0x4003_1000	0x4003_1FFF		Interrupt Source Check Resister
0x4003_2000	0x4003_2FFF		Reserved
0x4003_3000	0x4003_3FFF		GPIO
0x4003_4000	0x4003_4FFF		Reserved
0x4003_5000	0x4003_57FF		Low-Voltage Detector
0x4003_5800	0x4003_5FFF		Reserved
0x4003_6000	0x4003_6FFF		Reserved
0x4003_7000	0x4003_7FFF		Reserved
0x4003_8000	0x4003_8FFF		Multi-function serial Interface
0x4003_9000	0x4003_9FFF		Reserved
0x4003_A000	0x4003_AFFF		Reserved
0x4003_B000	0x4003_BFFF		Real-time clock
0x4003_C000	0x4003_FFFF		Reserved
0x4004_0000	0x4004_FFFF	AHB	Reserved
0x4005_0000	0x4005_FFFF		Reserved
0x4006_0000	0x4006_0FFF		Reserved
0x4006_1000	0x4006_2FFF		Reserved
0x4006_3000	0x4006_3FFF		Reserved
0x4006_4000	0x41FF_FFFF		Reserved

## 11. Pin Status in Each CPU State

The terms used for pin status have the following meanings.

■ INITX=0

This is the period when the INITX pin is the L level.

■ INITX=1

This is the period when the INITX pin is the H level.

■ SPL=0

This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB\_CTL) is set to 0.

■ SPL=1

This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB\_CTL) is set to 1.

■ Input enabled

Indicates that the input function can be used.

■ Internal input fixed at 0

This is the status that the input function cannot be used. Internal input is fixed at L.

■ Hi-Z

Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.

■ Setting disabled

Indicates that the setting is disabled.

■ Maintain previous state

Maintains the state that was immediately prior to entering the current mode.  
If a built-in peripheral function is operating, the output follows the peripheral function.  
If the pin is being used as a port, that output is maintained.

■ Analog input is enabled

Indicates that the analog input is enabled.

**List of Pin Status**

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1	
		-	-	-	-	SPL = 0	SPL = 1
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0
	Main crystal oscillator input pin/ External main clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0
	External main clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0
	Main crystal oscillator output pin	Hi-Z / Internal input fixed at 0/ or Input enable	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*1, Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*1, Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*1, Hi-Z / Internal input fixed at 0
C	INITX input pin	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
E	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Input enabled

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1	
		-	-	-	-	SPL = 0	SPL = 1
F	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0
	Sub crystal oscillator input pin / External sub clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
G	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0
	External sub clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0
	Sub crystal oscillator output pin	Hi-Z / Internal input fixed at 0/ or Input enable	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Maintain previous state	Maintain previous state/When oscillation stops*2, Hi-Z / Internal input fixed at 0	Maintain previous state/When oscillation stops*2, Hi-Z / Internal input fixed at 0
H	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0
	GPIO selected						
I	JTAG selected	Hi-Z	Pull-up / Input enabled	Pull-up / Input enabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at 0

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1	
		-	-	-	-	SPL = 0	SPL = 1
J	Resource selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0
	GPIO selected						
K	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0
	GPIO selected						
L	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0
	GPIO selected						
M	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	Resource other than above selected						Hi-Z / Internal input fixed at 0
	GPIO selected						

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1	
		-	-	-	-	SPL = 0	SPL = 1
N	Analog output selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	*3	*4
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled		Maintain previous state	Maintain previous state
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0
	GPIO selected						

\*1: Oscillation is stopped at Sub timer mode, sub CR timer mode, RTC mode, Stop mode.

\*2: Oscillation is stopped at Stop mode.

\*3: Maintain previous state at timer mode. GPIO selected Internal input fixed at 0 at RTC mode, Stop mode.

\*4: Maintain previous state at timer mode. Hi-Z/Internal input fixed at 0 at RTC mode, Stop mode.

## 12. Electrical Characteristics

### 12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1, *2	$V_{CC}$	$V_{SS} - 0.5$	$V_{SS} + 6.5$	V	
Analog power supply voltage*1, *3	$AV_{CC}$	$V_{SS} - 0.5$	$V_{SS} + 6.5$	V	
Analog reference voltage*1, *3	$AV_{RH}$	$V_{SS} - 0.5$	$V_{SS} + 6.5$	V	
Input voltage*1	$V_I$	$V_{SS} - 0.5$	$V_{CC} + 0.5$ ( $\leq 6.5$ V)	V	
		$V_{SS} - 0.5$	$V_{SS} + 6.5$	V	5 V tolerant
Analog pin input voltage*1	$V_{IA}$	$V_{SS} - 0.5$	$AV_{CC} + 0.5$ ( $\leq 6.5$ V)	V	
Output voltage*1	$V_O$	$V_{SS} - 0.5$	$V_{CC} + 0.5$ ( $\leq 6.5$ V)	V	
Clamp maximum current	$I_{CLAMP}$	-2	+2	mA	*7
Clamp total maximum current	$\sum [I_{CLAMP}]$		+20	mA	*7
L level maximum output current*4	$I_{OL}$	-	10	mA	4 mA type
			20	mA	12 mA type
L level average output current*5	$I_{OLAV}$	-	4	mA	4 mA type
			12	mA	12 mA type
L level total maximum output current	$\sum I_{OL}$	-	100	mA	
L level total average output current*6	$\sum I_{OLAV}$	-	50	mA	
H level maximum output current*4	$I_{OH}$	-	- 10	mA	4 mA type
			- 20	mA	12 mA type
H level average output current*5	$I_{OHAV}$	-	- 4	mA	4 mA type
			- 12	mA	12 mA type
H level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
H level total average output current*6	$\sum I_{OHAV}$	-	- 50	mA	
Power consumption	$P_D$	-	350	mW	
Storage temperature	$T_{STG}$	- 55	+ 150	°C	

\*1: These parameters are based on the condition that  $V_{SS} = AV_{SS} = 0.0$  V.

\*2:  $V_{CC}$  must not drop below  $V_{SS} - 0.5$  V.

\*3: Ensure that the voltage does not exceed  $V_{CC} + 0.5$  V, for example, when the power is turned on.

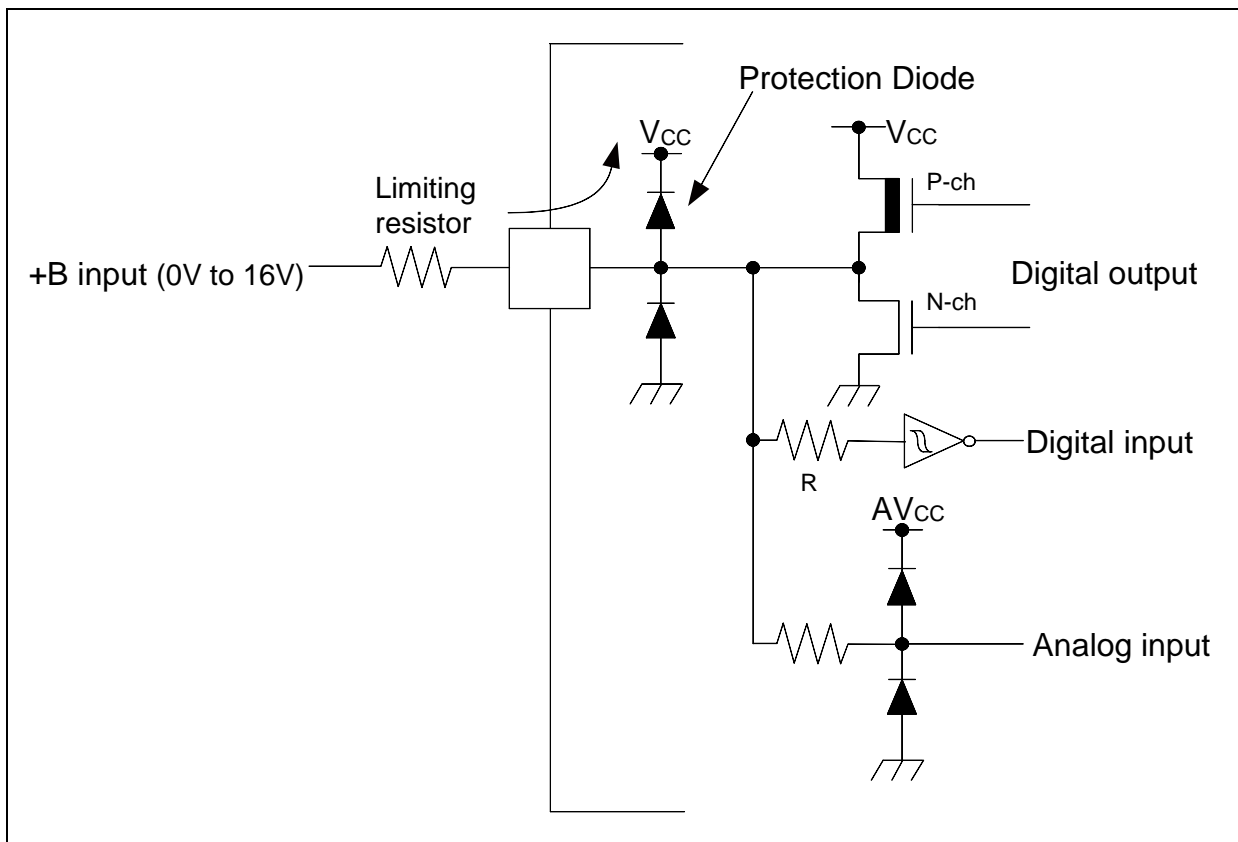
\*4: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

\*5: The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100 ms period.

\*6: The total average output current is defined as the average current value flowing through all of corresponding pins for a 100 ms.

\*7:

- See List of Pin Functions and I/O Circuit Type about +B input available pin.
- Use within recommended operating conditions.
- Use at DC voltage (current) the +B input.
- The +B signal should always be applied a limiting resistance placed between the +B signal and the device.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the device pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the device drive current is low, such as in the low-power consumption modes, the +B input potential may pass through the protective diode and increase the potential at the VCC and AVCC pin, and this may affect other devices.
- Note that if a +B signal is input when the device power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- The following is a recommended circuit example (I/O equivalent circuit).



**WARNING:**

- Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.  
Do not exceed any of these ratings.

## 12.2 Recommended Operating Conditions

(V<sub>SS</sub> = AV<sub>SS</sub> = AVRL = 0.0V)

Parameter		Symbol	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply voltage		V <sub>CC</sub>	-	2.7* <sup>2</sup>	5.5	V	
Analog power supply voltage		AV <sub>CC</sub>	-	2.7	5.5	V	AV <sub>CC</sub> = V <sub>CC</sub>
Analog reference voltage		AVRH	-	2.7	AV <sub>CC</sub>	V	
		AVRL	-	AV <sub>SS</sub>	AV <sub>SS</sub>	V	
Smoothing capacitor		C <sub>S</sub>	-	1	10	μF	For Regulator* <sup>1</sup>
Operating temperature	LQG064, LQC052, LQD064, LQA048, WNS064, WNY048	T <sub>A</sub>	When mounted on four-layer PCB	- 40	+ 105	°C	
			When mounted on double-sided single-layer PCB	- 40	+ 85	°C	

\*1: See C Pin in Handling Devices for the connection of the smoothing capacitor.

\*2: In between less than the minimum power supply voltage and low voltage reset/interrupt detection voltage or more, instruction execution and low voltage detection function by built-in High-speed CR (including Main PLL is used) or built-in Low-speed CR is possible to operate only.

### WARNING:

- The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions. Any use of semiconductor devices will be under their recommended operating condition. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure. No warranty is made with respect to any use, operating conditions, or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

## 12.3 DC Characteristics

### 12.3.1 Current Rating

( $V_{CC} = AV_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = AV_{SS} = AVRL = 0V$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$ )

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Run mode current	$I_{CC}$	VCC	PLL Run mode CPU: 40 MHz, Peripheral: 40 MHz Instruction on Flash	15.5	16	mA	*1, *5
			PLL Run mode CPU: 40 MHz, Peripheral: the clock stops NOP operation Instruction on Flash	9	10.6	mA	*1, *5
			PLL Run mode CPU: 40 MHz, Peripheral: 40 MHz Instruction on RAM	14	15	mA	*1
			High-speed CR Run mode CPU/ Peripheral: 4 MHz*2 Instruction on Flash	1.7	3.0	mA	*1
			Sub Run mode CPU/ Peripheral: 32 kHz Instruction on Flash	63	900	μA	*1, *6
			Low-speed CR Run mode CPU/ Peripheral: 100 kHz Instruction on Flash	88	920	μA	*1
Sleep mode current	$I_{CCS}$	VCC	PLL Sleep mode Peripheral: 40 MHz	9	12	mA	*1, *5
			High-speed CR Sleep mode Peripheral: 4 MHz*2	1	2.1	mA	*1
			Sub Sleep mode Peripheral: 32 kHz	58	880	μA	*1, *6
			Low-speed CR Sleep mode Peripheral: 100 kHz	71	890	μA	*1

\*1: When all ports are fixed.

\*2: When setting it to 4 MHz by trimming.

\*3:  $T_A = +25^{\circ}C$ ,  $V_{CC} = 5.5V$

\*4:  $T_A = +105^{\circ}C$ ,  $V_{CC} = 5.5V$

\*5: When using the crystal oscillator of 4 MHz (Including the current consumption of the oscillation circuit)

\*6: When using the crystal oscillator of 32 kHz (Including the current consumption of the oscillation circuit)

( $V_{CC} = AV_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = AV_{SS} = AV_{RL} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$ )

Parameter	Symbol	Pin name	Conditions		Value		Unit	Remarks
					Typ	Max		
Timer mode current	I <sub>CC</sub> T	VCC	Main Timer mode	T <sub>A</sub> = + 25°C, When LVD is off	1.8	2.1	mA	*1
				T <sub>A</sub> = + 85°C, When LVD is off	-	2.7	mA	*1
	Sub Timer mode		T <sub>A</sub> = + 25°C, When LVD is off	13	44	μA	*1	
			T <sub>A</sub> = + 85°C, When LVD is off	-	730	μA	*1	
RTC mode current	I <sub>CC</sub> R		RTC mode	T <sub>A</sub> = + 25°C, When LVD is off	10	38	μA	*1
				T <sub>A</sub> = + 85°C, When LVD is off	-	570	μA	*1
Stop mode current	I <sub>CC</sub> H		Stop mode	T <sub>A</sub> = + 25°C, When LVD is off	9	32	μA	*1
				T <sub>A</sub> = + 85°C, When LVD is off	-	540	μA	*1

\*1: When all ports are fixed.

\*2:  $V_{CC}=5.5V$

\*3: When using the crystal oscillator of 4 MHz(Including the current consumption of the oscillation circuit)

\*4: When using the crystal oscillator of 32 kHz(Including the current consumption of the oscillation circuit)

### LVD current

( $V_{CC} = AV_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = AV_{SS} = AV_{RL} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$ )

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Low-Voltage detection circuit (LVD) power supply current	I <sub>CC</sub> LVD	VCC	At operation for reset $V_{CC} = 5.5V$	0.13	0.3	μA	At not detect
			At operation for interrupt $V_{CC} = 5.5V$	0.13	0.3	μA	At not detect

### Flash memory current

( $V_{CC} = AV_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = AV_{SS} = AV_{RL} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$ )

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Flash memory write/erase current	I <sub>CC</sub> FLASH	VCC	At Write/Erase	9.5	11.2	mA	

**A/D convertor current**
 $(V_{CC} = AV_{CC} = 2.7V \text{ to } 5.5V, V_{SS} = AV_{SS} = AV_{RL} = 0V, T_A = -40^{\circ}C \text{ to } +105^{\circ}C)$ 

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I <sub>CCAD</sub>	AV <sub>CC</sub>	At operation	0.7	0.9	mA	
			At stop	0.13	13	μA	
Reference power supply current	I <sub>CCAVRH</sub>	AV <sub>RH</sub>	At operation	1.1	1.97	mA	AV <sub>RH</sub> =5.5V
			At stop	0.1	1.7	μA	AV <sub>RH</sub> =5.5V

**D/A convertor current**
 $(V_{CC} = AV_{CC} = 2.7V \text{ to } 5.5V, V_{SS} = AV_{SS} = AV_{RL} = 0V, T_A = -40^{\circ}C \text{ to } +105^{\circ}C)$ 

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I <sub>DDA</sub>	AVCC	At operation AV <sub>CC</sub> = 3.3 V	315	380	μA	*
	I <sub>DSA</sub>		At operation AV <sub>CC</sub> = 5.0 V	475	580	μA	*
			At stop	-	8	μA	*

\*: No-load

### 12.3.2 Pin Characteristics

( $V_{CC} = AV_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = AV_{SS} = AV_{RL} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$ )

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level input voltage (hysteresis input)	$V_{IHS}$	CMOS hysteresis input pin, MD0, MD1	-	$V_{CC} \times 0.8$	-	$V_{CC} + 0.3$	V	
		5V tolerant input pin	-	$V_{CC} \times 0.8$	-	$V_{SS} + 5.5$	V	
L level input voltage (hysteresis input)	$V_{ILS}$	CMOS hysteresis input pin, MD0, MD1	-	$V_{SS} - 0.3$	-	$V_{CC} \times 0.2$	V	
		5V tolerant input pin	-	$V_{SS} - 0.3$	-	$V_{CC} \times 0.2$	V	
H level output voltage	$V_{OH}$	4mA type	$V_{CC} \geq 4.5V$ , $I_{OH} = -4mA$	$V_{CC} - 0.5$	-	$V_{CC}$	V	
			$V_{CC} < 4.5V$ , $I_{OH} = -2mA$					
		12mA type	$V_{CC} \geq 4.5V$ , $I_{OH} = -12mA$	$V_{CC} - 0.5$	-	$V_{CC}$	V	
			$V_{CC} < 4.5V$ , $I_{OH} = -8mA$					
L level output voltage	$V_{OL}$	4mA type	$V_{CC} \geq 4.5V$ , $I_{OL} = 4mA$	$V_{SS}$	-	0.4	V	
			$V_{CC} < 4.5V$ , $I_{OL} = 2mA$					
		12mA type	$V_{CC} \geq 4.5V$ , $I_{OL} = 12mA$	$V_{SS}$	-	0.4	V	
			$V_{CC} < 4.5V$ , $I_{OL} = 8mA$					
Input leak current	$I_{IL}$	-	-	-5	-	+5	$\mu A$	
Pull-up resistance value	$R_{PU}$	Pull-up pin	$V_{CC} \geq 4.5V$	33	50	90	k $\Omega$	
			$V_{CC} < 4.5V$	-	-	180		
Input capacitance	$C_{IN}$	Other than VCC, VSS, AVCC, AVSS, AVRH, AVRL	-	-	5	15	pF	

## 12.4 AC Characteristics

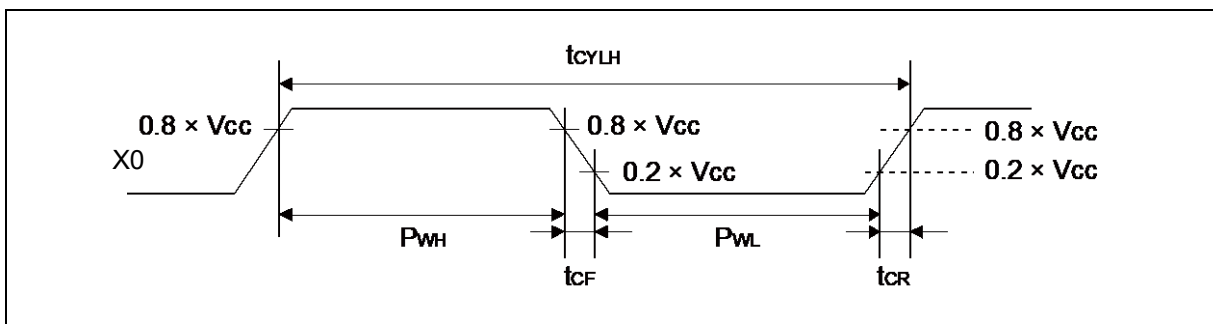
### 12.4.1 Main Clock Input Characteristics

( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$ )

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	$f_{CH}$	X0, X1	$V_{CC} \geq 4.5V$	4	48	MHz	When crystal oscillator is connected
			$V_{CC} < 4.5V$	4	20		
			-	4	48	MHz	When using external Clock
Input clock cycle	$t_{CYLH}$		-	20.83	250	ns	When using external Clock
Input clock pulse width	-		$P_{WH}/t_{CYLH}$ , $P_{WL}/t_{CYLH}$	45	55	%	When using external Clock
Input clock rising time and falling time	$t_{CF}$ , $t_{CR}$		-	-	5	ns	When using external Clock
Internal operating clock frequency <sup>*1</sup>	$f_{CM}$	-	-	-	40	MHz	Master clock
	$f_{CC}$	-	-	-	40	MHz	Base clock (HCLK/FCLK)
	$f_{CP0}$	-	-	-	40	MHz	APB0 bus clock <sup>*2</sup>
	$f_{CP1}$	-	-	-	40	MHz	APB1 bus clock <sup>*2</sup>
	$f_{CP2}$	-	-	-	40	MHz	APB2 bus clock <sup>*2</sup>
Internal operating clock cycle time <sup>*1</sup>	$t_{CYCC}$	-	-	25	-	ns	Base clock (HCLK/FCLK)
	$t_{CYCP0}$	-	-	25	-	ns	APB0 bus clock <sup>*2</sup>
	$t_{CYCP1}$	-	-	25	-	ns	APB1 bus clock <sup>*2</sup>
	$t_{CYCP2}$	-	-	25	-	ns	APB2 bus clock <sup>*2</sup>

\*1: For more information about each internal operating clock, see Chapter 2-1: Clock in FM3 Family Peripheral Manual.

\*2: For about each APB bus which each peripheral is connected to, see Block Diagram in this data sheet.

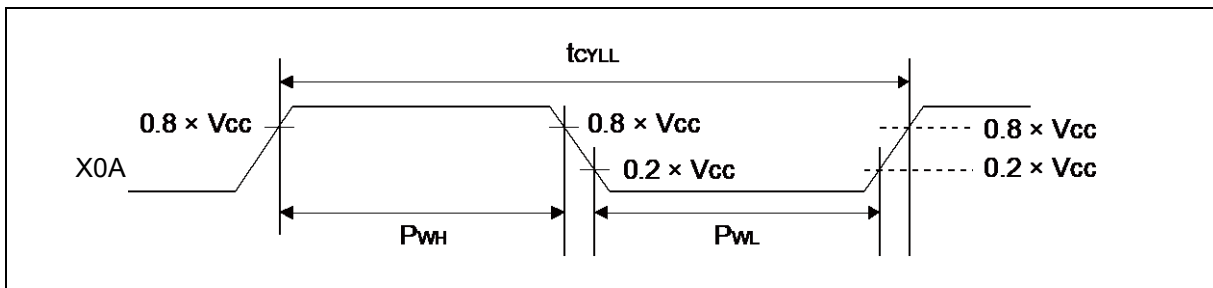


### 12.4.2 Sub Clock Input Characteristics

( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$ )

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	$f_{CL}$	X0A, X1A	-	-	32.768	-	kHz	When crystal oscillator is connected
Input clock cycle	$t_{CYLL}$		-	32	-	100	kHz	When using external clock
Input clock pulse width	-		-	10	-	31.25	$\mu s$	When using external clock
	-		$P_{WH}/t_{CYLL}$ , $P_{WL}/t_{CYLL}$	45	-	55	%	When using external clock

\*: See Sub crystal oscillator in Handling Devices for the crystal oscillator used.



### 12.4.3 Built-in CR Oscillation Characteristics

#### Built-in High-speed CR

( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$ )

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	$f_{CRH}$	$T_A = +25^{\circ}C$ , $3.6V < V_{CC} \leq 5.5V$	3.92	4	4.08	MHz	When trimming*1
		$T_A = 0^{\circ}C$ to $+85^{\circ}C$ , $3.6V < V_{CC} \leq 5.5V$	3.9	4	4.1		
		$T_A = -40^{\circ}C$ to $+105^{\circ}C$ , $3.6V < V_{CC} \leq 5.5V$	3.88	4	4.12		
		$T_A = +25^{\circ}C$ , $2.7V \leq V_{CC} \leq 3.6V$	3.94	4	4.06		
		$T_A = -20^{\circ}C$ to $+85^{\circ}C$ , $2.7V \leq V_{CC} \leq 3.6V$	3.92	4	4.08		
		$T_A = -20^{\circ}C$ to $+105^{\circ}C$ , $2.7V \leq V_{CC} \leq 3.6V$	3.9	4	4.1		
		$T_A = -40^{\circ}C$ to $+105^{\circ}C$ , $2.7V \leq V_{CC} \leq 3.6V$	3.88	4	4.12		
		$T_A = -40^{\circ}C$ to $+105^{\circ}C$	2.8	4	5.2		When not trimming
Frequency stabilization time	$t_{CRWT}$	-	-	-	30	$\mu s$	*2

\*1: In the case of using the values in CR trimming area of Flash memory at shipment for frequency trimming/temperature trimming.

\*2: This is time from the trim value setting to stable of the frequency of the High-speed CR clock.  
After setting the trim value, the period when the frequency stability time passes can use the High-speed CR clock as a source clock.

#### Built-in Low-speed CR

( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$ )

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	$f_{CRL}$	-	50	100	150	kHz	

#### 12.4.4 Operating Conditions of Main PLL (In the case of using main clock for input of Main PLL)

( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$ )

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	$t_{LOCK}$	100	-	-	$\mu s$	
PLL input clock frequency	$f_{PLLI}$	4	-	16	MHz	
PLL multiplication rate	-	5	-	37	multiplier	
PLL macro oscillation clock frequency	$f_{PLLO}$	75	-	150	MHz	
Main PLL clock frequency*2	$f_{CLKPLL}$	-	-	40	MHz	

\*1: Time from when the PLL starts operating until the oscillation stabilizes.

\*2: For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM3 Family Peripheral Manual.

#### 12.4.5 Operating Conditions of Main PLL (In the case of using built-in high-speed CR for input clock of Main PLL)

( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$ )

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	$t_{LOCK}$	100	-	-	$\mu s$	
PLL input clock frequency	$f_{PLLI}$	3.8	4	4.2	MHz	
PLL multiplication rate	-	19	-	35	multiplier	
PLL macro oscillation clock frequency	$f_{PLLO}$	72	-	150	MHz	
Main PLL clock frequency*2	$f_{CLKPLL}$	-	-	40	MHz	

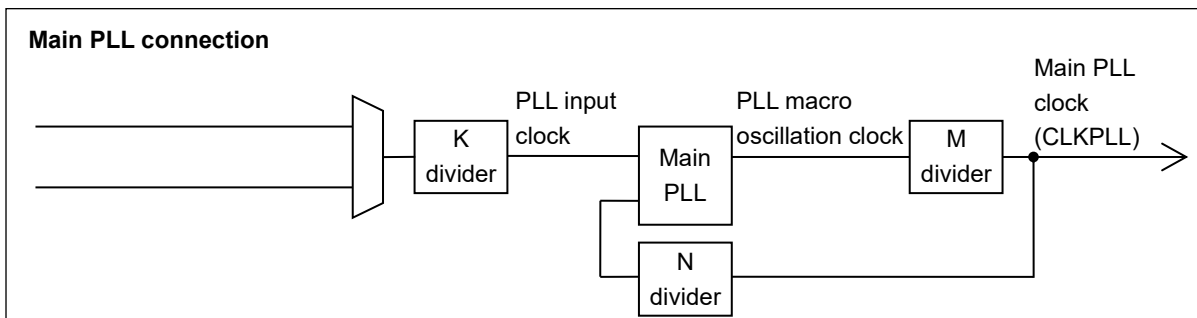
\*1: Time from when the PLL starts operating until the oscillation stabilizes.

\*2: For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM3 Family Peripheral Manual.

**Note:**

- Make sure to input to the main PLL source clock, the high-speed CR clock (CLKHC) that the frequency/temperature has been trimmed.

When setting PLL multiple rate, please take the accuracy of the built-in high-speed CR clock into account and prevent the master clock from exceeding the maximum frequency.



#### 12.4.6 Reset Input Characteristics

( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$ )

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	$t_{INITX}$	INITX	-	500	-	ns	

#### 12.4.7 Power-on Reset Timing

( $V_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$ )

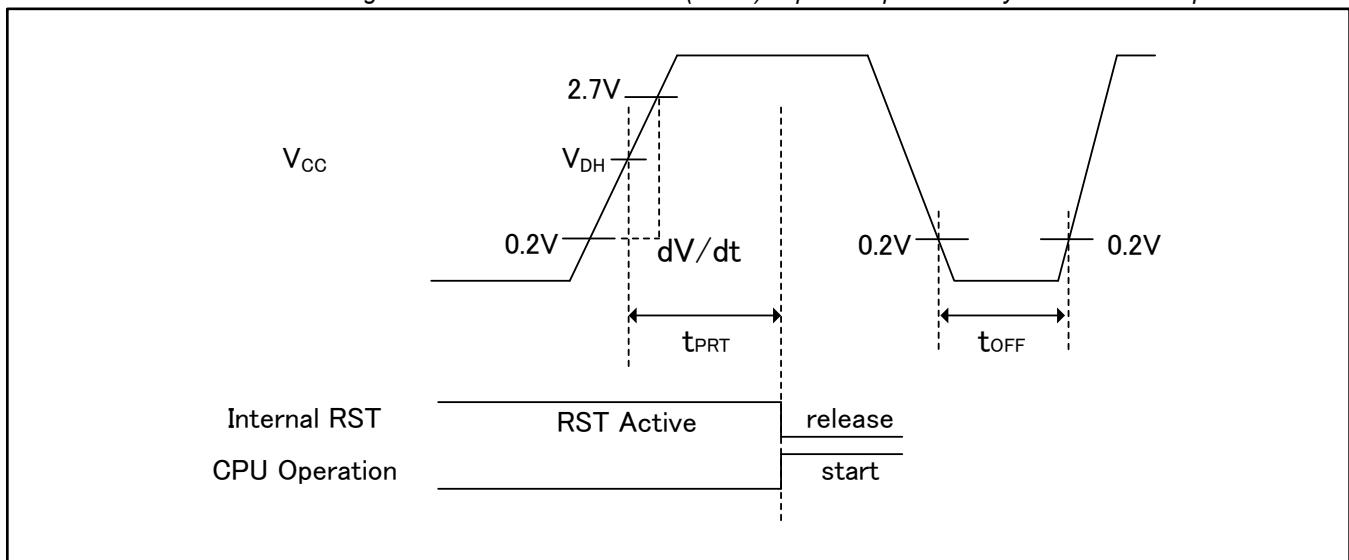
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply shut down time	$t_{OFF}$	VCC	-	1	-	-	ms	*1
Power ramp rate	$dV/dt$		$V_{CC}: 0.2V$ to $2.7V$	1.2	-	1000	mV/ $\mu s$	*2
Time until releasing Power-on reset	$t_{PRT}$		-	0.34	-	3.15	ms	

\*1:  $V_{CC}$  must be held below 0.2 V for minimum period of  $t_{OFF}$ . Improper initialization may occur if this condition is not met.

\*2: This  $dV/dt$  characteristic is applied at the power-on of cold start ( $t_{OFF} > 1$  ms).

#### Note:

– If  $t_{OFF}$  cannot be satisfied designs must assert external reset(INITX) at power-up and at any brownout event per 12. 4. 6.



#### Glossary

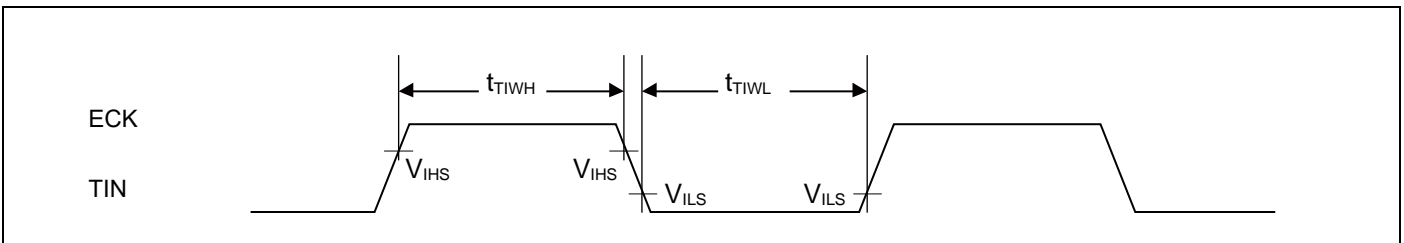
VDH: detection voltage of Low Voltage detection reset. See “12.7 Low-Voltage Detection Characteristics”

### 12.4.8 Base Timer Input Timing

#### Timer input timing

( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$ )

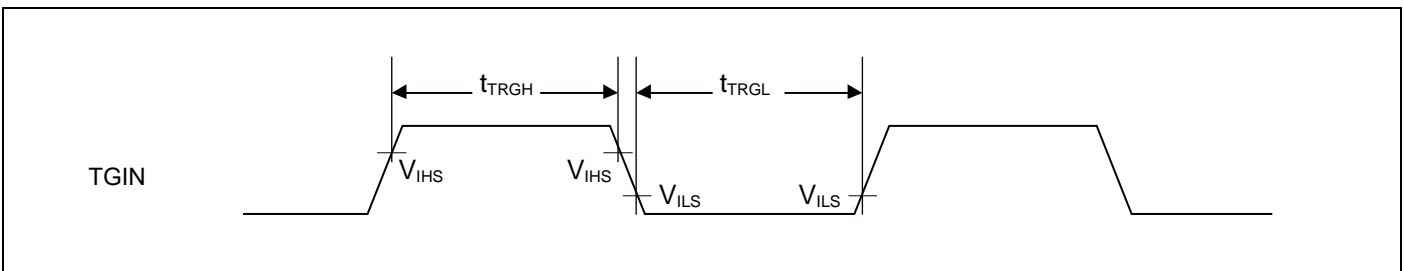
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	$t_{TIWH}$ , $t_{TIWL}$	TIOAn/TIOBn (when using as ECK, TIN)	-	$2t_{CYCP}$	-	ns	



#### Trigger input timing

( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$ )

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	$t_{TRGH}$ , $t_{TRGL}$	TIOAn/TIOBn (when using as TGIN)	-	$2t_{CYCP}$	-	ns	



#### Note:

- $t_{CYCP}$  indicates the APB bus clock cycle time.  
About the APB bus number which the Base Timer is connected to, see Block Diagram in this data sheet.

### 12.4.9 CSIO/UART Timing

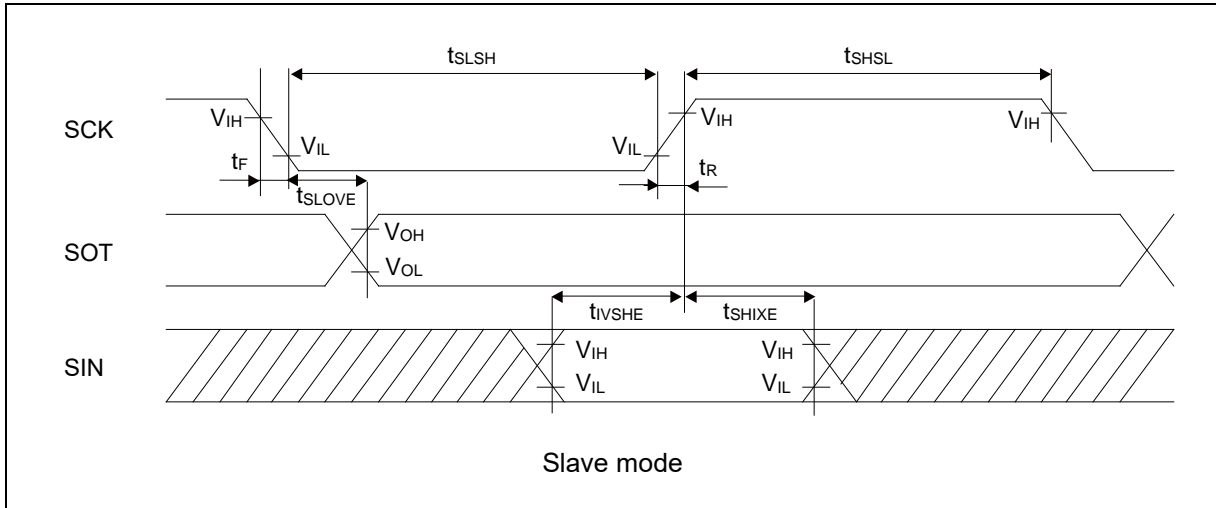
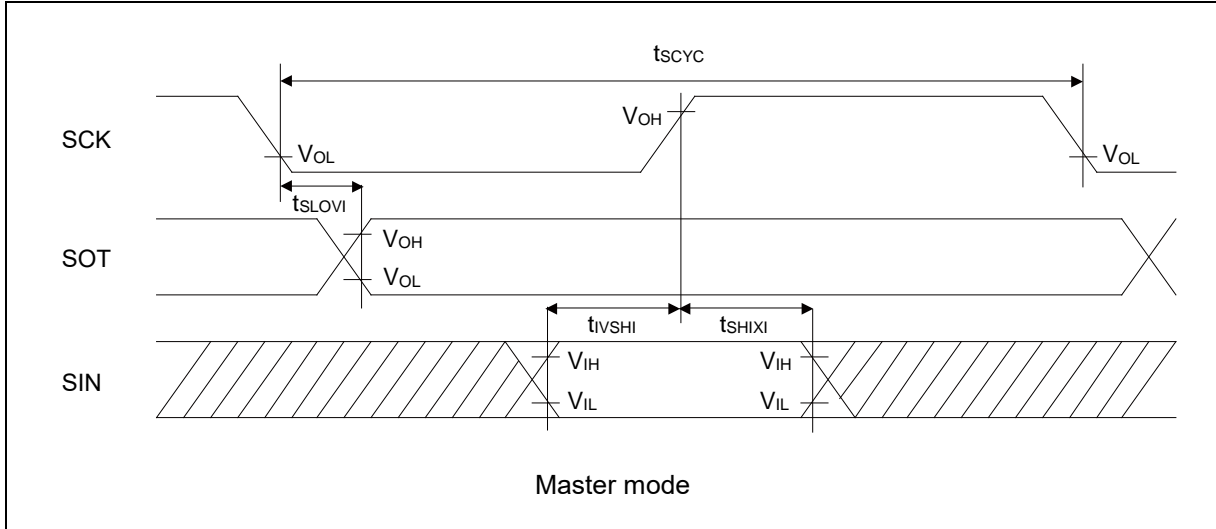
**CSIO (SPI = 0, SCINV = 0)**

( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$ )

Parameter	Symbol	Pin name	Conditions	$V_{CC} < 4.5 V$		$V_{CC} \geq 4.5 V$		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	$t_{SCYC}$	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	$t_{SLOVI}$	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	$t_{IVSHI}$	SCKx, SINx		50	-	30	-	ns
SCK ↑ → SIN hold time	$t_{SHIXI}$	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	$t_{LSLH}$	SCKx		$2t_{CYCP} - 10$	-	$2t_{CYCP} - 10$	-	ns
Serial clock H pulse width	$t_{HSLH}$	SCKx	Slave mode	$t_{CYCP} + 10$	-	$t_{CYCP} + 10$	-	ns
SCK ↓ → SOT delay time	$t_{SLOVE}$	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	$t_{IVSHE}$	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	$t_{SHIXE}$	SCKx, SINx		20	-	20	-	ns
SCK falling time	$t_F$	SCKx		-	5	-	5	ns
SCK rising time	$t_R$	SCKx		-	5	-	5	ns

**Notes:**

- The above characteristics apply to clock synchronous mode.
- $t_{CYCP}$  indicates the APB bus clock cycle time.
- About the APB bus number which Multi-function serial is connected to, see Block Diagram in this data sheet.
- These characteristics only guarantee the same relocate port number.  
For example, the combination of SCKx\_0 and SOTx\_1 is not guaranteed.
- When the external load capacitance  $C_L = 30 pF$ .



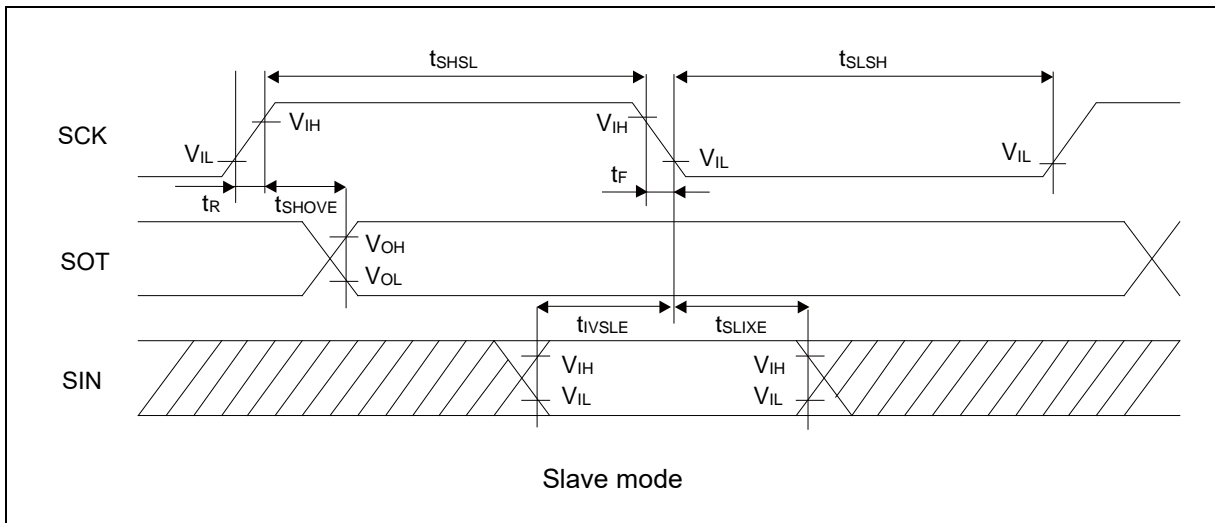
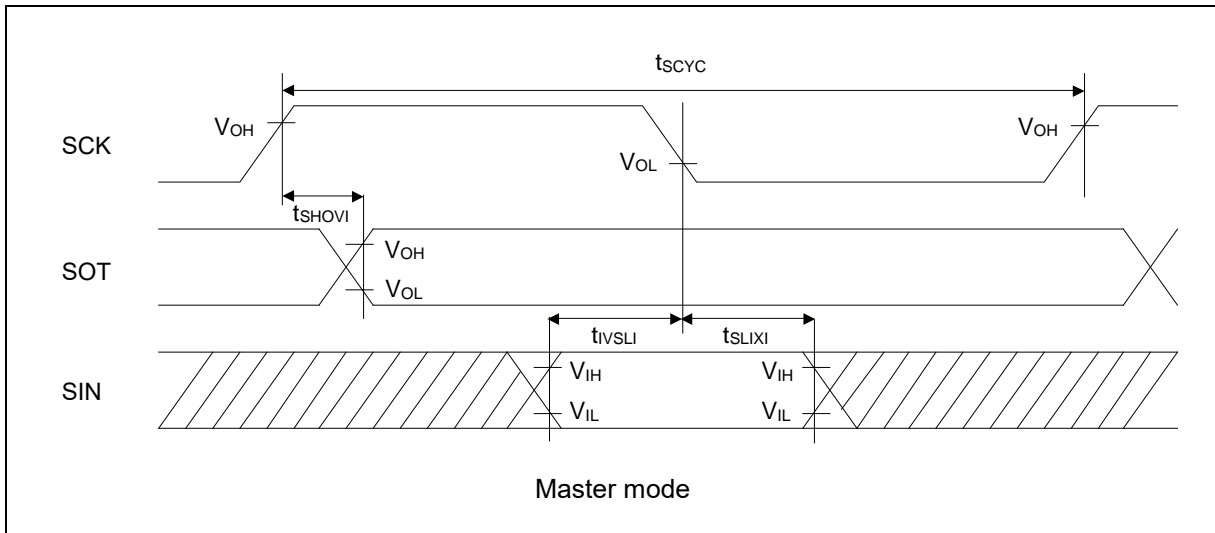
**CSIO (SPI = 0, SCINV = 1)**

 (V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V, T<sub>A</sub> = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	V <sub>CC</sub> < 4.5 V		V <sub>CC</sub> ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t <sub>SCYC</sub>	SCKx	Master mode	4t <sub>CYCP</sub>	-	4t <sub>CYCP</sub>	-	ns
SCK ↑ → SOT delay time	t <sub>SHOVI</sub>	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t <sub>IVSLI</sub>	SCKx, SINx		50	-	30	-	ns
SCK ↓ → SIN hold time	t <sub>SLIXI</sub>	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t <sub>LSLH</sub>	SCKx		2t <sub>CYCP</sub> - 10	-	2t <sub>CYCP</sub> - 10	-	ns
Serial clock H pulse width	t <sub>SHSL</sub>	SCKx	Slave mode	t <sub>CYCP</sub> + 10	-	t <sub>CYCP</sub> + 10	-	ns
SCK ↑ → SOT delay time	t <sub>SHOVE</sub>	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↓ setup time	t <sub>IVSLE</sub>	SCKx, SINx		10	-	10	-	ns
SCK ↓ → SIN hold time	t <sub>SLIXE</sub>	SCKx, SINx		20	-	20	-	ns
SCK falling time	t <sub>F</sub>	SCKx		-	5	-	5	ns
SCK rising time	t <sub>R</sub>	SCKx		-	5	-	5	ns

**Notes:**

- The above characteristics apply to clock synchronous mode.
- t<sub>CYCP</sub> indicates the APB bus clock cycle time.
- About the APB bus number which Multi-function serial is connected to, see Block Diagram in this data sheet.
- These characteristics only guarantee the same relocate port number.  
For example, the combination of SCKx\_0 and SOTx\_1 is not guaranteed.
- When the external load capacitance C<sub>L</sub> = 30 pF.



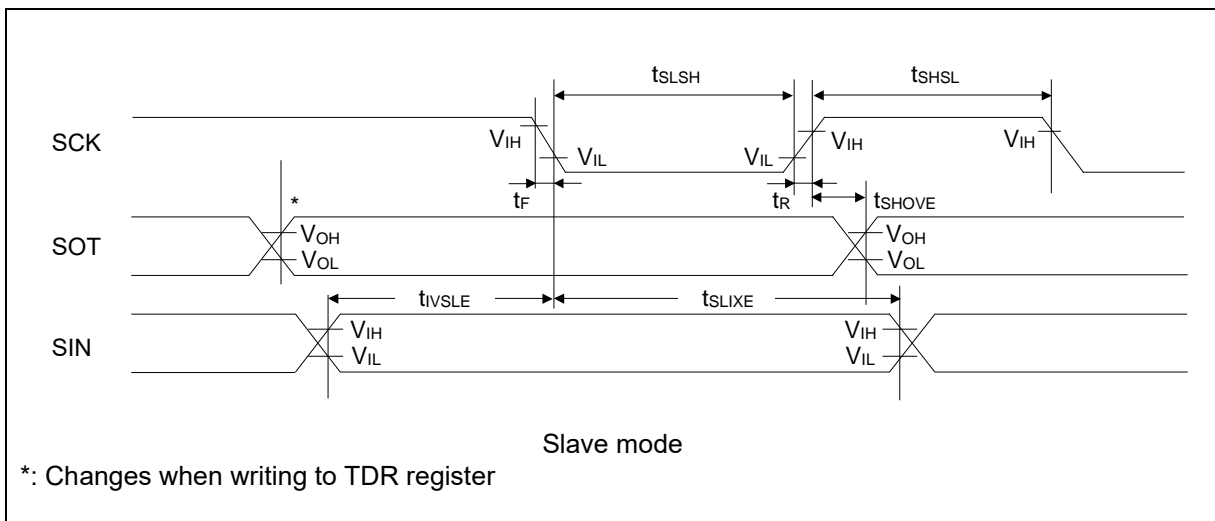
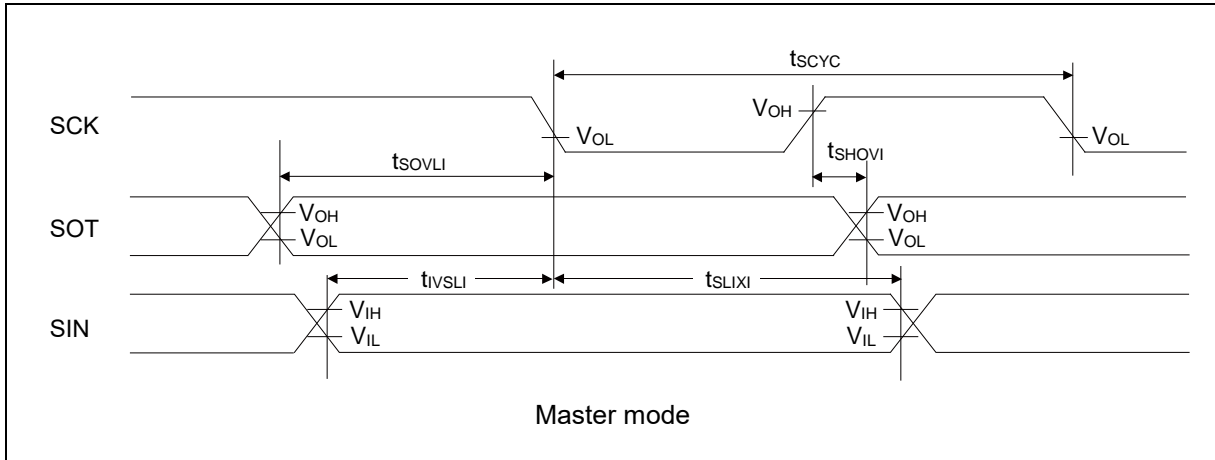
**CSIO (SPI = 1, SCINV = 0)**

 (V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V, T<sub>A</sub> = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	V <sub>CC</sub> < 4.5 V		V <sub>CC</sub> ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t <sub>SCYC</sub>	SCKx	Master mode	4t <sub>CYCP</sub>	-	4t <sub>CYCP</sub>	-	ns
SCK ↑ → SOT delay time	t <sub>SHOVI</sub>	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t <sub>IVSLI</sub>	SCKx, SINx		50	-	30	-	ns
SCK ↓ → SIN hold time	t <sub>SLIXI</sub>	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↓ delay time	t <sub>SOVLI</sub>	SCKx, SOTx		2t <sub>CYCP</sub> - 30	-	2t <sub>CYCP</sub> - 30	-	ns
Serial clock L pulse width	t <sub>SLSH</sub>	SCKx		2t <sub>CYCP</sub> - 10	-	2t <sub>CYCP</sub> - 10	-	ns
Serial clock H pulse width	t <sub>SHSL</sub>	SCKx	Slave mode	t <sub>CYCP</sub> + 10	-	t <sub>CYCP</sub> + 10	-	ns
SCK ↑ → SOT delay time	t <sub>SHOVE</sub>	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↓ setup time	t <sub>IVSLE</sub>	SCKx, SINx		10	-	10	-	ns
SCK ↓ → SIN hold time	t <sub>SLIXE</sub>	SCKx, SINx		20	-	20	-	ns
SCK falling time	t <sub>F</sub>	SCKx		-	5	-	5	ns
SCK rising time	t <sub>R</sub>	SCKx		-	5	-	5	ns

**Notes:**

- The above characteristics apply to clock synchronous mode.
- t<sub>CYCP</sub> indicates the APB bus clock cycle time.
- About the APB bus number which Multi-function serial is connected to, see Block Diagram in this data sheet.
- These characteristics only guarantee the same relocate port number.  
For example, the combination of SCKx\_0 and SOTx\_1 is not guaranteed.
- When the external load capacitance C<sub>L</sub> = 30 pF.

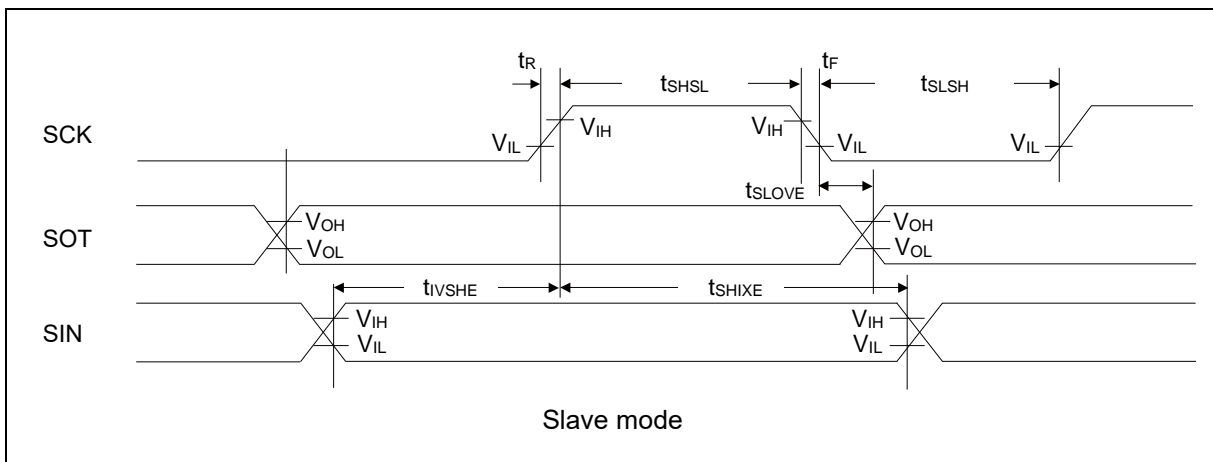
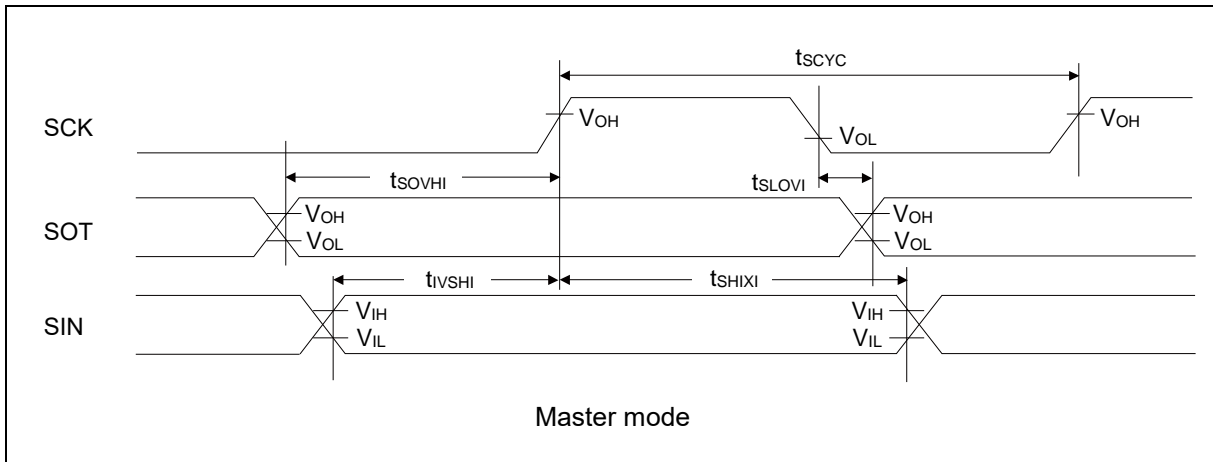


**CSIO (SPI = 1, SCINV = 1)**
 $(V_{CC} = 2.7V \text{ to } 5.5V, V_{SS} = 0V, T_A = -40^{\circ}C \text{ to } +105^{\circ}C)$ 

Parameter	Symbol	Pin name	Conditions	$V_{CC} < 4.5 V$		$V_{CC} \geq 4.5 V$		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	$t_{SCYC}$	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	$t_{SLOVI}$	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	$t_{IVSHI}$	SCKx, SINx		50	-	30	-	ns
SCK ↑ → SIN hold time	$t_{SHIXI}$	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↑ delay time	$t_{SOVHI}$	SCKx, SOTx		$2t_{CYCP} - 30$	-	$2t_{CYCP} - 30$	-	ns
Serial clock L pulse width	$t_{SLSH}$	SCKx		$2t_{CYCP} - 10$	-	$2t_{CYCP} - 10$	-	ns
Serial clock H pulse width	$t_{SHSL}$	SCKx	Slave mode	$t_{CYCP} + 10$	-	$t_{CYCP} + 10$	-	ns
SCK ↓ → SOT delay time	$t_{SLOVE}$	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	$t_{IVSHE}$	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	$t_{SHIXE}$	SCKx, SINx		20	-	20	-	ns
SCK falling time	$t_F$	SCKx		-	5	-	5	ns
SCK rising time	$t_R$	SCKx		-	5	-	5	ns

**Notes:**

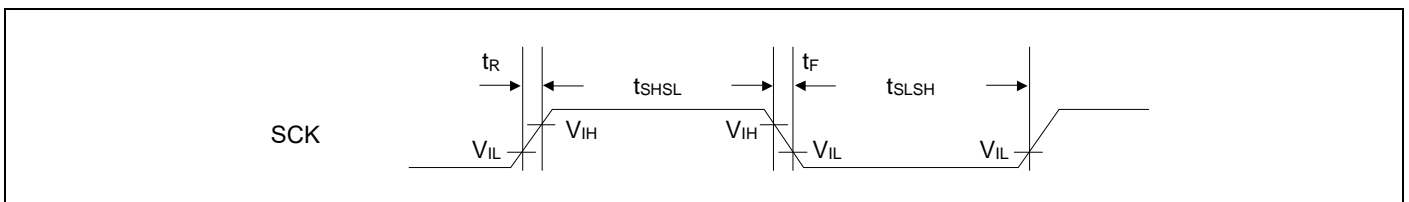
- The above characteristics apply to clock synchronous mode.
- $t_{CYCP}$  indicates the APB bus clock cycle time.
- About the APB bus number which Multi-function serial is connected to, see Block Diagram in this data sheet.
- These characteristics only guarantee the same relocate port number.  
For example, the combination of SCKx\_0 and SOTx\_1 is not guaranteed.
- When the external load capacitance  $C_L = 30 \text{ pF}$ .



### UART external clock input (EXT = 1)

( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$ )

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Serial clock L pulse width	$t_{SLSH}$	$C_L = 30\text{ pF}$	$t_{CYCP} + 10$	-	ns	
Serial clock H pulse width	$t_{SHSL}$		$t_{CYCP} + 10$	-	ns	
SCK falling time	$t_F$		-	5	ns	
SCK rising time	$t_R$		-	5	ns	



#### 12.4.10 External Input Timing

( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$ )

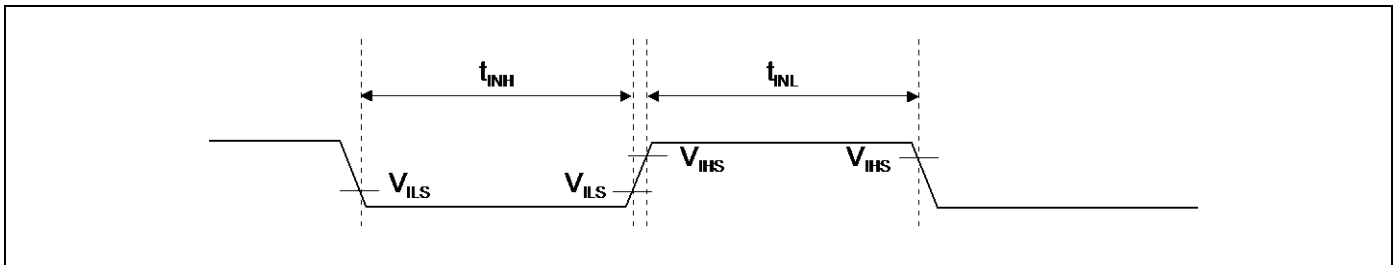
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	$t_{INH}$ , $t_{INL}$	ADTG	-	$2t_{CYCP}^{*1}$	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTTixX	-	$2t_{CYCP}^{*1}$	-	ns	Waveform enerator
		IGTRG	-	$2t_{CYCP}^{*1}$	-	ns	PPG IGBT mode
		INTxx, NMIX	*2	$2t_{CYCP} + 100^{*1}$	-	ns	External interrupt,
			*3	500	-	ns	NMI

\*1:  $t_{CYCP}$  indicates the APB bus clock cycle time.

About the APB bus number which the A/D converter, Multi-function Timer, External interrupt are connected to, see Block Diagram in this data sheet.

\*2: When in Run mode, in Sleep mode.

\*3: When in stop mode, in RTC mode, in timer mode.



### 12.4.11 I<sup>2</sup>C Timing

(V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V, T<sub>A</sub> = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Standard-mode		Fast-mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f <sub>SCL</sub>		0	100	0	400	kHz	
(Repeated) Start condition hold time SDA ↓ → SCL ↓	t <sub>HDSTA</sub>	C <sub>L</sub> = 30 pF, R = (V <sub>p</sub> /I <sub>OL</sub> )* <sup>1</sup>	4.0	-	0.6	-	μs	
SCLclock L width	t <sub>LOW</sub>		4.7	-	1.3	-	μs	
SCLclock H width	t <sub>HIGH</sub>		4.0	-	0.6	-	μs	
(Repeated) Start condition setup time SCL ↑ → SDA ↓	t <sub>SUSTA</sub>		4.7	-	0.6	-	μs	
Data hold time SCL ↓ → SDA ↓ ↑	t <sub>HDDAT</sub>		0	3.45* <sup>2</sup>	0	0.9* <sup>3</sup>	μs	
Data setup time SDA ↓ ↑ → SCL ↑	t <sub>SUDAT</sub>		250	-	100	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t <sub>SUSTO</sub>		4.0	-	0.6	-	μs	
Bus free time between Stop condition and Start condition	t <sub>BUF</sub>		4.7	-	1.3	-	μs	
Noise filter	t <sub>SP</sub>	-	2 t <sub>CYCP</sub> * <sup>4</sup>	-	2 t <sub>CYCP</sub> * <sup>4</sup>	-	ns	

\*1: R and C<sub>L</sub> represent the pull-up resistor and load capacitance of the SCL and SDA lines, respectively.

V<sub>p</sub> indicates the power supply voltage of the pull-up resistor and I<sub>OL</sub> indicates V<sub>OL</sub> guaranteed current.

\*2: The maximum t<sub>HDDAT</sub> must satisfy that it does not extend at least L period (t<sub>LOW</sub>) of device's SCL signal.

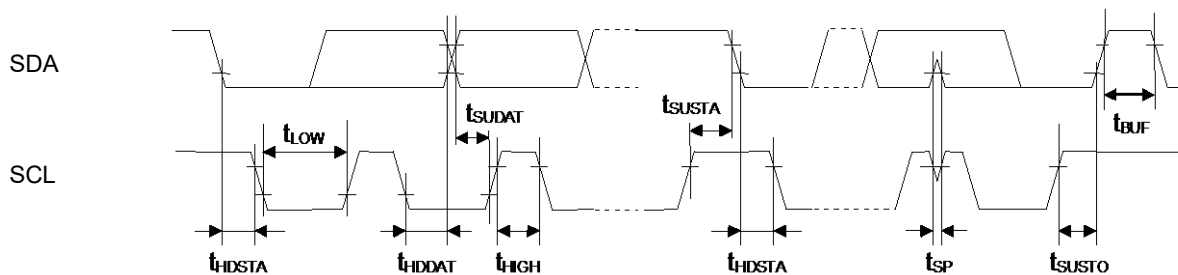
\*3: A Fast-mode I<sup>2</sup>C bus device can be used on a Standard-mode I<sup>2</sup>C bus system as long as the device satisfies the requirement of t<sub>SUDAT</sub> ≥ 250 ns.

\*4: t<sub>CYCP</sub> is the APB bus clock cycle time.

About the APB bus number that I<sup>2</sup>C is connected to, see Block Diagram in this data sheet.

To use Standard-mode, set the APB bus clock at 2 MHz or more.

To use Fast-mode, set the APB bus clock at 8 MHz or more.



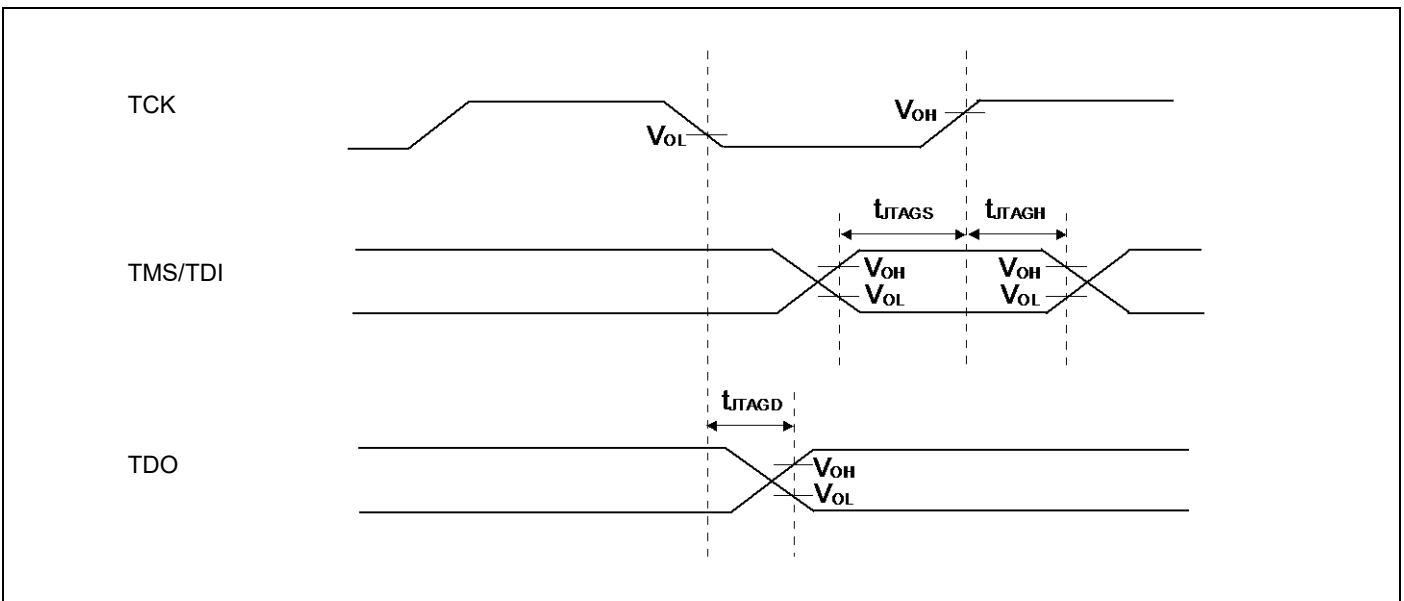
**12.4.12 JTAG Timing**

 ( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$ )

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS, TDI setup time	$t_{JTAGS}$	TCK, TMS, TDI	$V_{CC} \geq 4.5V$ $V_{CC} < 4.5V$	15	-	ns	
TMS, TDI hold time	$t_{JTAGH}$	TCK, TMS, TDI	$V_{CC} \geq 4.5V$ $V_{CC} < 4.5V$	15	-	ns	
TDO delay time	$t_{JTAGD}$	TCK, TDO	$V_{CC} \geq 4.5V$	-	25	ns	
			$V_{CC} < 4.5V$	-	45		

**Note:**

- When the external load capacitance  $C_L = 30\text{ pF}$ .



## 12.5 12-bit A/D Converter

### Electrical characteristics for the A/D converter

( $V_{CC} = AV_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = AV_{SS} = AV_{RL} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$ )

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	-	-	-	$\pm 2.0$	$\pm 4.5$	LSB	AVRH = 2.7 V to 5.5 V
Differential Nonlinearity	-	-	-	$\pm 1.5$	$\pm 2.5$	LSB	
Zero transition voltage	$V_{ZT}$	ANxx	-	$\pm 8$	$\pm 15$	mV	
Full-scale transition voltage	$V_{FST}$	ANxx	-	AVRH $\pm 8$	AVRH $\pm 15$	mV	
Conversion time	-	-	0.8* <sup>1</sup>	-	-	$\mu s$	AVCC $\geq 4.5 V$
			1.0* <sup>1</sup>	-	-	$\mu s$	AVCC < 4.5 V
Sampling time* <sup>2</sup>	$t_s$	-	0.24	-	10	$\mu s$	
Compare clock cycle* <sup>3</sup>	$t_{CK}$	-	40	-	1000	ns	
State transition time to operation permission	$t_{STT}$	-	-	-	1.0	$\mu s$	
Analog input capacity	$C_{AIN}$	-	-	-	9.7	pF	
Analog input resistor	$R_{AIN}$	-	-	-	1.5	k $\Omega$	AVCC $\geq 4.5 V$
					2.2		AVCC < 4.5 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	5	$\mu A$	
Analog input voltage	-	ANxx	AVRL	-	AVRH	V	
Reference voltage	-	AVRH	2.7	-	AVCC	V	
		AVRL	AVSS	-	AVSS		

\*1: The conversion time is the value of sampling time ( $t_s$ ) + compare time ( $t_c$ ).

The condition of the minimum conversion time is the following.

AVCC  $\geq 4.5 V$ , HCLK=25 MHz      sampling time: 240 ns, compare time: 560 ns

AVCC < 4.5 V, HCLK=40 MHz      sampling time: 300 ns, compare time: 700 ns

Ensure that it satisfies the value of the sampling time ( $t_s$ ) and compare clock cycle ( $t_{CK}$ ).

For setting of the sampling time and compare clock cycle, see Chapter 1-1: A/D Converter in FM3 Family Peripheral Manual Analog Macro Part.

The register settings of the A/D Converter are reflected in the operation according to the APB bus clock timing.

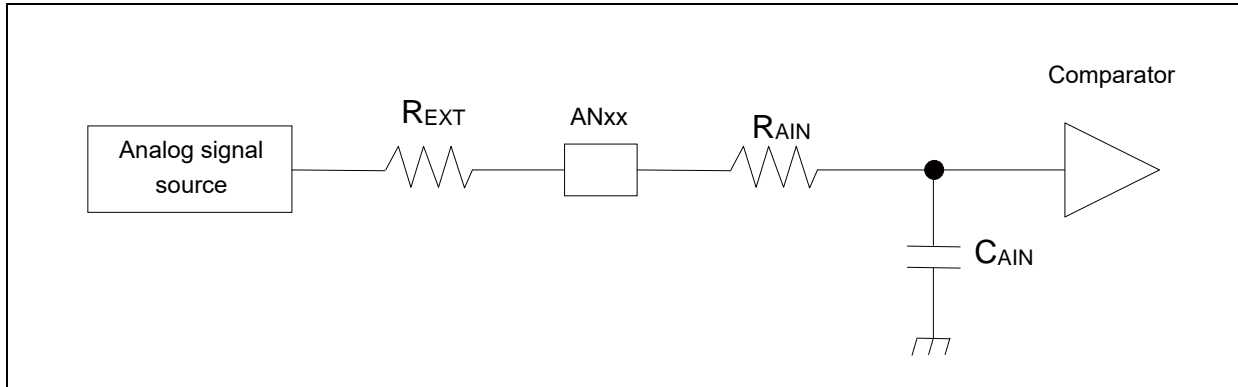
For the number of the APB bus to which the A/D Converter is connected, see Block Diagram.

The Base clock (HCLK) is used to generate the sampling time and the compare clock cycle.

\*2: A necessary sampling time changes by external impedance.

Ensure that it sets the sampling time to satisfy (Equation 1).

\*3: The compare time ( $t_c$ ) is the value of (Equation 2).



(Equation 1)  $t_s \geq (R_{AIN} + R_{EXT}) \times C_{AIN} \times 9$

$t_s$ : Sampling time

$R_{AIN}$ : Input resistor of A/D = 1.3 k $\Omega$  at 4.5 V  $\leq AV_{CC} \leq 5.5$  V ch.0 to ch.2, ch.4, ch.5

Input resistor of A/D = 1.5 k $\Omega$  at 4.5 V  $\leq AV_{CC} \leq 5.5$  V ch.12 to ch.14

Input resistor of A/D = 1.9 k $\Omega$  at 2.7 V  $\leq AV_{CC} < 4.5$  V ch.0 to ch.2, ch.4, ch.5

Input resistor of A/D = 2.2 k $\Omega$  at 2.7 V  $\leq AV_{CC} < 4.5$  V ch.12 to ch.14

$C_{AIN}$ : Input capacity of A/D = 9.7 pF at 2.7 V  $\leq AV_{CC} \leq 5.5$  V

$R_{EXT}$ : Output impedance of external circuit

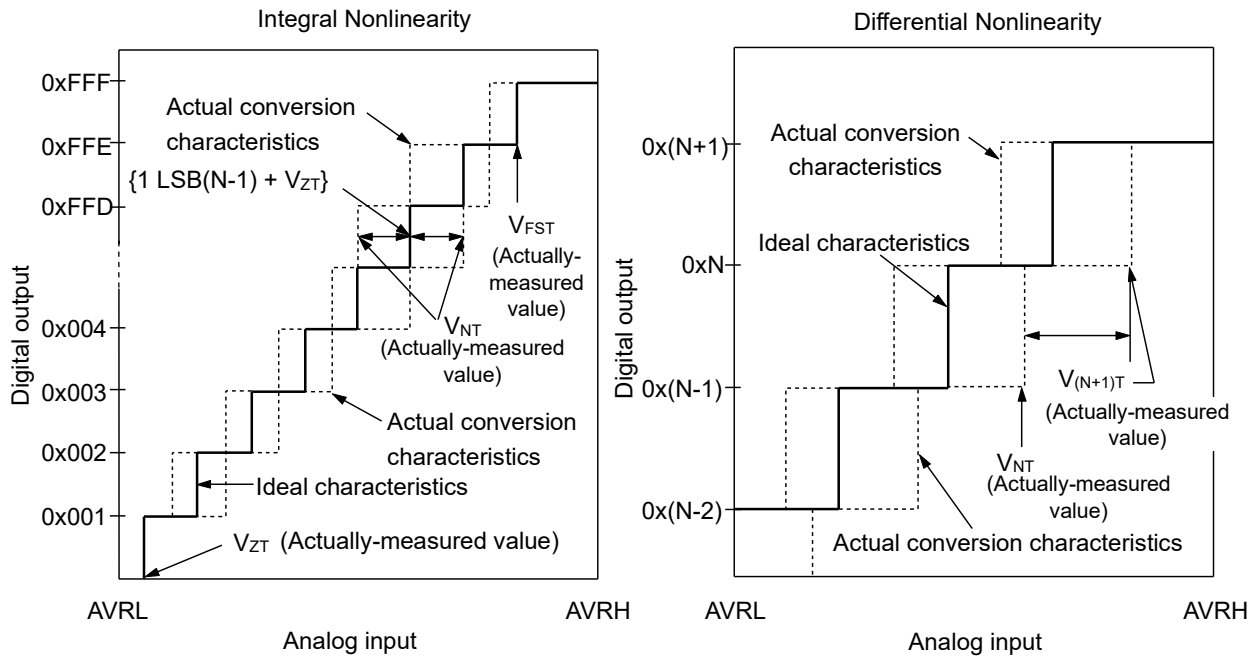
(Equation 2)  $t_c = t_{CCK} \times 14$

$t_c$ : Compare time

$t_{CCK}$ : Compare clock cycle

## Definition of 12-bit A/D Converter Terms

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ↔ 0b000000000001) and the full-scale transition point (0b111111111110 ↔ 0b111111111111) from the actual conversion characteristics.
- Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Integral Nonlinearity of digital output } N = \frac{V_{NT} - \{1\text{LSB} \times (N - 1) + V_{ZT}\}}{1\text{LSB}} \quad [\text{LSB}]$$

$$\text{Differential Nonlinearity of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1\text{LSB}} - 1 \quad [\text{LSB}]$$

$$1\text{LSB} = \frac{V_{FST} - V_{ZT}}{4094}$$

- N: A/D converter digital output value.  
 V<sub>ZT</sub>: Voltage at which the digital output changes from 0x000 to 0x001.  
 V<sub>FST</sub>: Voltage at which the digital output changes from 0xFFE to 0xFFF.  
 V<sub>NT</sub>: Voltage at which the digital output changes from 0x(N - 1) to 0xN.

## 12.6 10-bit D/A Converter

### Electrical Characteristics for the D/A Converter

( $V_{CC} = AV_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = AV_{SS} = AV_{RL} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$ )

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	DAx	-	-	10	bit	
Conversion time	t <sub>C20</sub>		0.47	0.58	0.69	μs	Load 20 pF
	t <sub>C100</sub>		2.37	2.90	3.43	μs	Load 100 pF
Integral Nonlinearity	INL		- 4.0	-	+ 4.0	LSB	*
Differential Nonlinearity	DNL		- 0.9	-	+ 0.9	LSB	*
Output Voltage offset	V <sub>OFF</sub>		-	-	10.0	mV	Code is 0x000
			- 20.0	-	+ 5.4	mV	Code is 0x3FF
Analog output impedance	R <sub>O</sub>		3.10	3.80	4.50	kΩ	D/A operation
		2.0	-	-	MΩ	D/A stop	
Output undefined period	t <sub>R</sub>	-	-	70	ns		

\*: No-load

## 12.7 Low-Voltage Detection Characteristics

### 12.7.1 Low-Voltage Detection Reset

(T<sub>A</sub> = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHR*1 = 00000	2.25	2.45	2.65	V	When voltage drops
Released voltage	VDH		2.30	2.50	2.70	V	When voltage rises
Detected voltage	VDL	SVHR*1 = 00001	2.39	2.60	2.81	V	When voltage drops
Released voltage	VDH		Same as SVHR = 0000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 00010	2.48	2.70	2.92	V	When voltage drops
Released voltage	VDH		Same as SVHR = 0000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 00011	2.58	2.80	3.02	V	When voltage drops
Released voltage	VDH		Same as SVHR = 0000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 00100	2.76	3.00	3.24	V	When voltage drops
Released voltage	VDH		Same as SVHR = 0000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 00101	2.94	3.20	3.46	V	When voltage drops
Released voltage	VDH		Same as SVHR = 0000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 00110	3.31	3.60	3.89	V	When voltage drops
Released voltage	VDH		Same as SVHR = 0000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 00111	3.40	3.70	4.00	V	When voltage drops
Released voltage	VDH		Same as SVHR = 0000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 01000	3.68	4.00	4.32	V	When voltage drops
Released voltage	VDH		Same as SVHR = 0000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 01001	3.77	4.10	4.43	V	When voltage drops
Released voltage	VDH		Same as SVHR = 0000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 01010	3.86	4.20	4.54	V	When voltage drops
Released voltage	VDH		Same as SVHR = 0000 value			V	When voltage rises
LVD stabilization wait time	t <sub>LVDW</sub>	-	-	-	8160 × t <sub>CYCP</sub> *2	μs	
LVD detection delay time	t <sub>LVDL</sub>	-	-	-	200	μs	

\*1: SVHR bit of Low-Voltage Detection Voltage Control Register (LVD\_CTL) is reset to SVHR = 00000 by low voltage detection reset.

\*2: t<sub>CYCP</sub> indicates the APB2 bus clock cycle time.

**12.7.2 Interrupt of Low-Voltage Detection**

 (T<sub>A</sub> = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 00011	2.58	2.80	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.90	3.13	V	When voltage rises
Detected voltage	VDL	SVHI = 00100	2.76	3.00	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.10	3.35	V	When voltage rises
Detected voltage	VDL	SVHI = 00101	2.94	3.20	3.46	V	When voltage drops
Released voltage	VDH		3.04	3.30	3.56	V	When voltage rises
Detected voltage	VDL	SVHI = 00110	3.31	3.60	3.89	V	When voltage drops
Released voltage	VDH		3.40	3.70	4.00	V	When voltage rises
Detected voltage	VDL	SVHI = 00111	3.40	3.70	4.00	V	When voltage drops
Released voltage	VDH		3.50	3.80	4.10	V	When voltage rises
Detected voltage	VDL	SVHI = 01000	3.68	4.00	4.32	V	When voltage drops
Released voltage	VDH		3.77	4.10	4.43	V	When voltage rises
Detected voltage	VDL	SVHI = 01001	3.77	4.10	4.43	V	When voltage drops
Released voltage	VDH		3.86	4.20	4.54	V	When voltage rises
Detected voltage	VDL	SVHI = 01010	3.86	4.20	4.54	V	When voltage drops
Released voltage	VDH		3.96	4.30	4.64	V	When voltage rises
LVD stabilization wait time	t <sub>LVDW</sub>	-	-	-	8160 × t <sub>CYCP</sub> *	μs	
LVD detection delay time	t <sub>LVDL</sub>	-	-	-	200	μs	

 \*: t<sub>CYCP</sub> indicates the APB2 bus clock cycle time.

## 12.8 Flash Memory Write/Erase Characteristics

### 12.8.1 Write / Erase time

(V<sub>CC</sub> = 2.7V to 5.5V, T<sub>A</sub> = - 40°C to + 105°C)

Parameter	Value		Unit	Remarks
	Typ	Max		
Sector erase time	0.3	0.7	s	Includes write time prior to internal erase
Half word (16-bit) write time	16	282	μs	Not including system-level overhead time
Chip erase time	2.4	5.6	s	Includes write time prior to internal erase

\*: The typical value is immediately after shipment, the maximum value is guarantee value under 10,000 cycle of erase/write.

### 12.8.2 Write cycles and data hold time

Erase/write cycles (cycle)	Data hold time (year)	Remarks
1,000	20*	
10,000	10*	

\*: At average + 85°C

## 12.9 Return Time from Low-Power Consumption Mode

### 12.9.1 Return Factor: Interrupt

The return time from Low-Power consumption mode is indicated as follows. It is from receiving the return factor to starting the program operation.

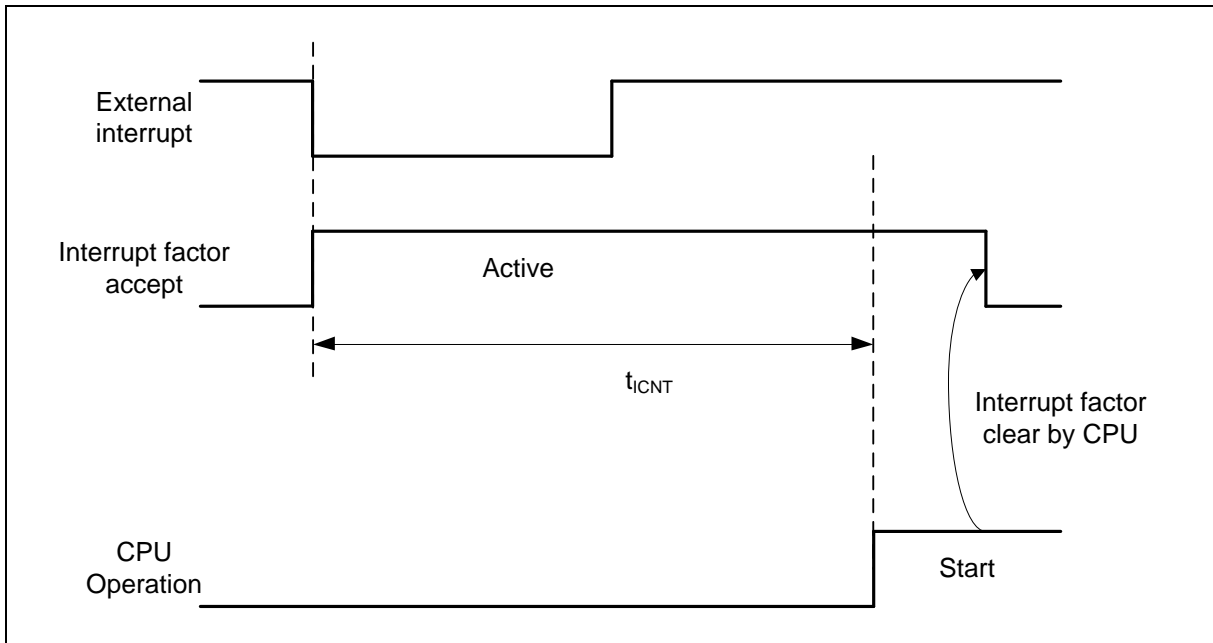
#### Return Count Time

( $V_{CC} = 2.7V$  to  $5.5V$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$ )

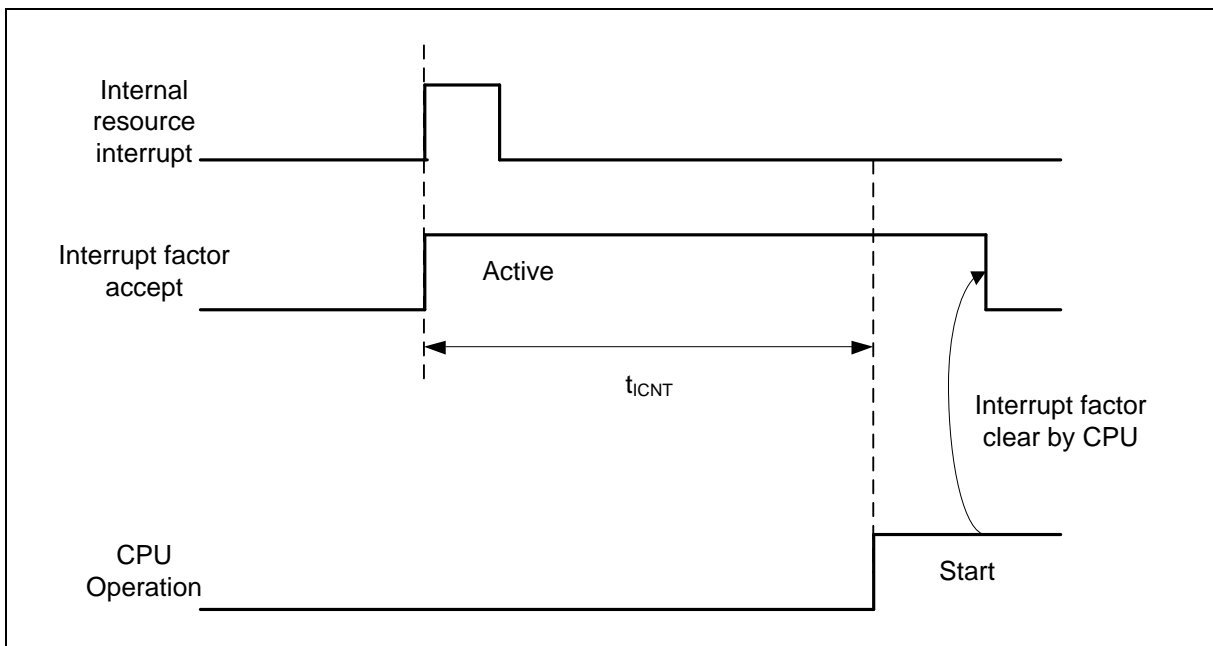
Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	$t_{ICNT}$	$t_{CYCC}$		$\mu s$	
High-speed CR Timer mode, Main Timer mode, PLL Timer mode		43	83	$\mu s$	
Low-speed CR Timer mode		310	620	$\mu s$	
Sub Timer mode		534	724	$\mu s$	
RTC mode, Stop mode		278	479	$\mu s$	

\*: The maximum value depends on the accuracy of built-in CR.

#### Operation example of return from Low-Power consumption mode (by external interrupt\*)



\*: External interrupt is set to detecting fall edge.

**Operation example of return from Low-Power consumption mode (by internal resource interrupt\*)**


\*: Internal resource interrupt is not included in return factor by the kind of Low-Power consumption mode.

**Notes:**

- The return factor is different in each Low-Power consumption modes. See Chapter 6: Low Power Consumption Mode and Operations of Standby Modes in FM3 Family Peripheral Manual.
- When interrupt recovers, the operation mode that CPU recovers depends on the state before the Low-Power consumption mode transition. See Chapter 6: Low Power Consumption Mode in FM3 Family Peripheral Manual.

### 12.9.2 Return Factor: Reset

The return time from Low-Power consumption mode is indicated as follows. It is from releasing reset to starting the program operation.

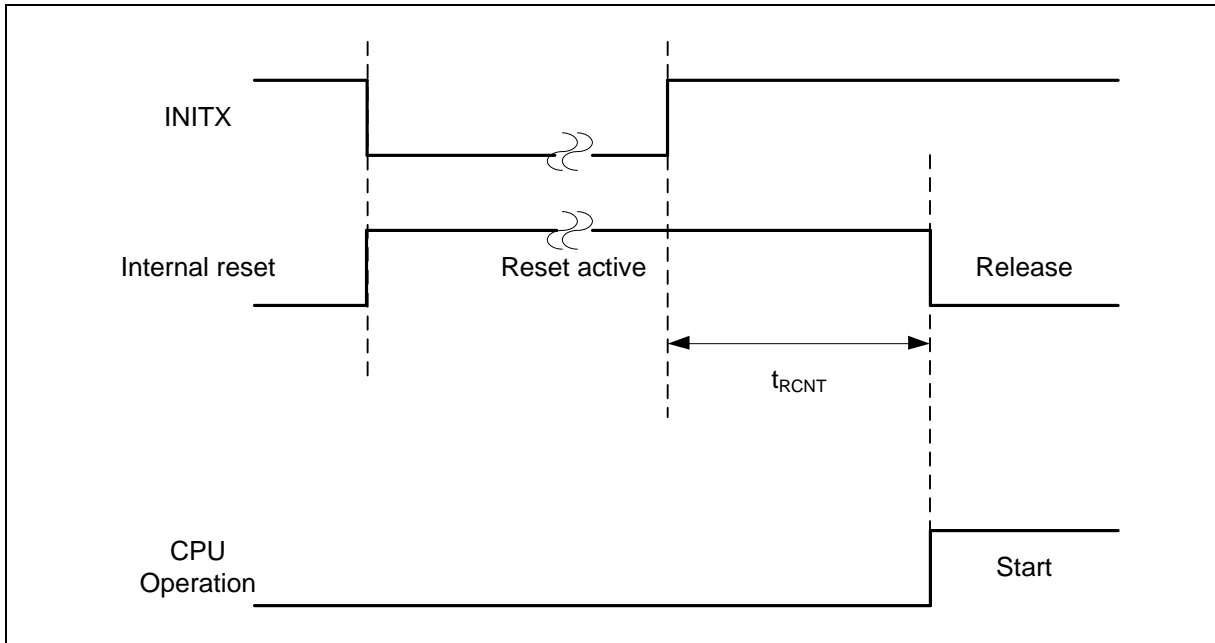
#### Return Count Time

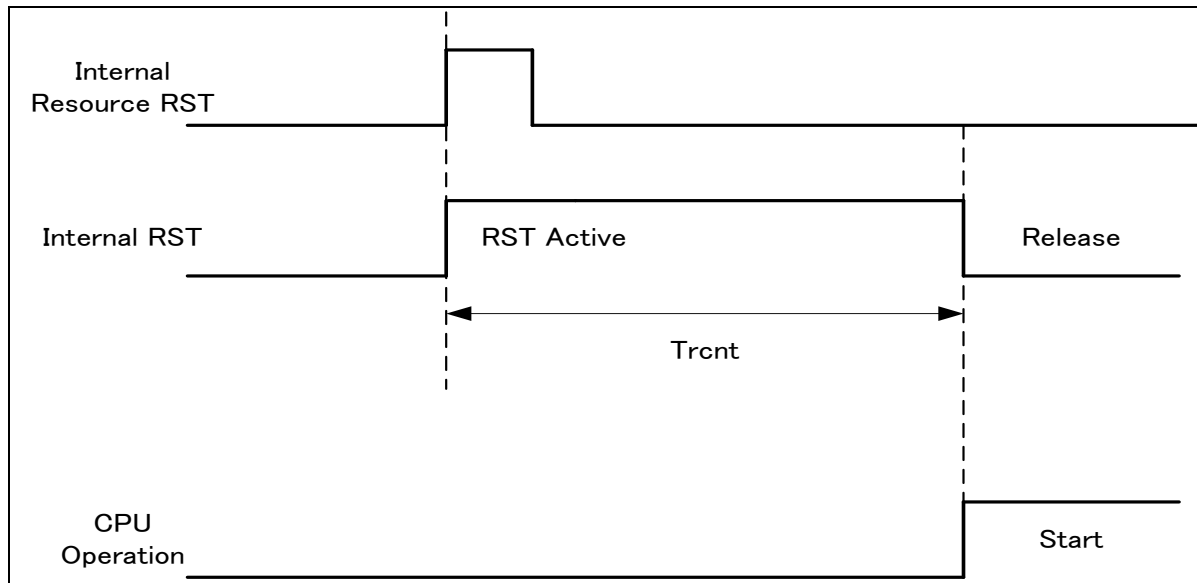
( $V_{CC} = 2.7V$  to  $5.5V$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$ )

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	$t_{RCNT}$	149	264	$\mu s$	
High-speed CR Timer mode, Main Timer mode, PLL Timer mode		149	264	$\mu s$	
Low-speed CR Timer mode		318	603	$\mu s$	
Sub Timer mode		308	583	$\mu s$	
RTC/Stop mode		248	443	$\mu s$	

\*: The maximum value depends on the accuracy of built-in CR.

#### Operation example of return from Low-Power consumption mode (by INITX)



**Operation example of return from low power consumption mode (by internal resource reset\*)**


\*: Internal resource reset is not included in return factor by the kind of Low-Power consumption mode.

**Notes:**

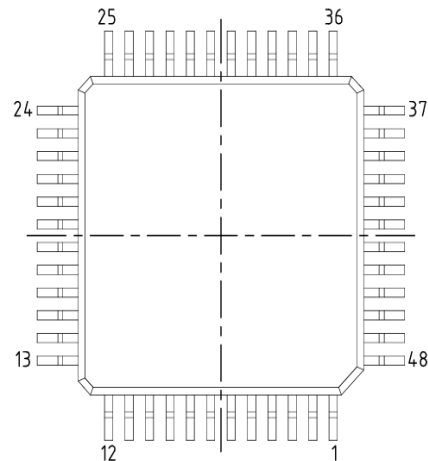
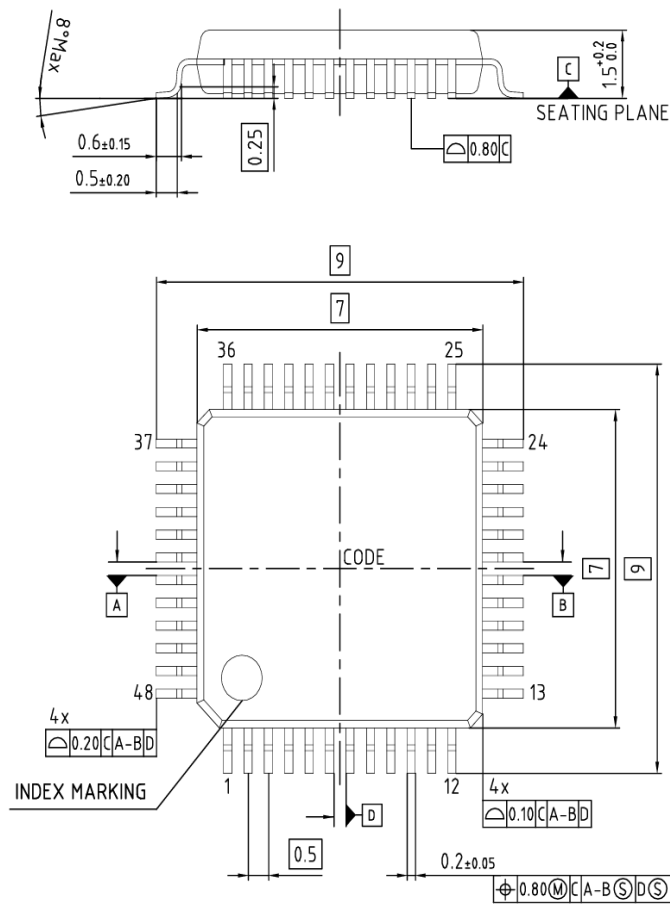
- The return factor is different in each Low-Power consumption modes. See Chapter 6: Low Power Consumption Mode and Operations of Standby Modes in FM3 Family Peripheral Manual.
- When interrupt recovers, the operation mode that CPU recovers depends on the state before the Low-Power consumption mode transition. See Chapter 6: Low Power Consumption Mode in FM3 Family Peripheral Manual.
- The time during the power-on reset/low-voltage detection reset is excluded. See (12.4.7) Power-on Reset Timing in 12.4 AC Characteristics in Electrical Characteristics for the detail on the time during the power-on reset/low -voltage detection reset.
- When in recovery from reset, CPU changes to the high-speed CR run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the main PLL clock stabilization wait time.
- The internal resource reset means the watchdog reset and the CSV reset.

### 13. Ordering Information

Part number	On-chip Flash memory	On-chip SRAM	Package	Packing
CY9AF121KPMC-G-JNE2	64 Kbyte	4 Kbyte	Plastic • LQFP (0.5 mm pitch), 48-pin (LQA048)	

## 14. Package Dimensions

Package Type	Package Code
LQFP 48	LQA048



- 1) DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION OF 0.25 MAX. PER SIDE  
 2) DOES NOT INCLUDE DAMBAR PROTRUSION OF 0.08 MAX. PER SIDE AT MAX. MATERIAL CONDITION

Z8B00248754 V03

## 15. Major Changes

Spanion Publication Number: DS706-00064

Page	Section	Change Results
Revision 0.1		
-	-	Initial release
Revision 0.2		
-	-	Company name and layout design change
Revision 1.0		
-	-	Preliminary → Full Production
2	Features	Revised I <sup>2</sup> C operation mode name
3	Features	Revised the value of A/D conversion time
4	Features	Revised Channel number of MFT A/D activation compare
6	Product Lineup	<ul style="list-style-type: none"> <li>Added notes of Built-in high speed CR accuracy</li> <li>Revised channel number of MFT A/D activation compare</li> </ul>
17	List Of Pin Function • List of pin numbers	Corrected I/O circuit type of P80,P81,P82
29	I/O Circuit Type	Added the remarks of type L
37	Block Diagram	Revised Channel number of MFT A/D activation compare
47	Electrical Characteristics 2. Recommended Operating Conditions	Corrected the minimum value of AVR <sub>H</sub> voltage
48,49	Electrical Characteristics 3.DC Characteristics (1) Current Rating	Revised the values of "TBD"
49	Electrical Characteristics 3.DC Characteristics (1) Current Rating • A/D converter current	<ul style="list-style-type: none"> <li>Corrent the pin name of power supply current</li> <li>Added the at stop condition of power supply current</li> <li>Added the remark of reference power supply current</li> </ul>
55	Electrical Characteristics 3.AC Characteristics (6)Power-on Reset Timing	Revised the values of "TBD"
66	Electrical Characteristics 3.AC Characteristics (10) I <sup>2</sup> C Timing	<ul style="list-style-type: none"> <li>Revised I<sup>2</sup>C operation mode name</li> <li>Revised the value of noise filter</li> </ul>
68	Electrical Characteristics 5. 12-bit A/D Converter	<ul style="list-style-type: none"> <li>Revised the value of zero transition valtage and full-scale transiton valtage</li> <li>Revised the value of conversion time, sampling time, compare clock cycle</li> <li>Corrected the value of state transition time to operation permission</li> <li>Corrected the minimum value of AVR<sub>H</sub> voltage</li> <li>Revised the notes explanation</li> <li>Delete (Preliminary value) description</li> </ul>
71	Electrical Characteristics 6. 10-bit D/A Converter	<ul style="list-style-type: none"> <li>Delete (Preliminary value) description</li> </ul>
72,73	Electrical Characteristics 7. Low-Voltage Detection Characteristics	<ul style="list-style-type: none"> <li>Corrected the values of SV<sub>HR</sub> and SV<sub>HI</sub></li> </ul>
74	Electrical Characteristics 8. Flash Memory Write/Erase Characteristics	<ul style="list-style-type: none"> <li>Revised the values of "TBD"</li> <li>Revised the values of typical</li> <li>Revised the notes of Erase/write cycles and data hold time</li> <li>Delete (target value) description</li> </ul>
75,77	Electrical Characteristics 9. Return Time from Low-Power Consumption Mode	Revised the values of "TBD"
84,85	Package Dimensions	Added the figures of LCC-48P-M74 and LCC-64P-M25
Revision 2.0		
26	I/O Circuit Type	Added about +B input
39	Memory Map • Memory map(2)	Added the summary of Flash memory sector and the note

Page	Section	Change Results
46, 47	Electrical Characteristics 1. Absolute Maximum Ratings	· Added the Clamp maximum current · Added about +B input
48	Electrical Characteristics 2. Recommended Operation Conditions	Added the note about less than the minimum power supply voltage
49, 50	Electrical Characteristics 3. DC Characteristics (1) Current rating	· Changed the table format · Added Main TIMER mode current
56	Electrical Characteristics 4. AC Characteristics (4-1) Operating Conditions of Main PLL (4-2) Operating Conditions of Main PLL	Added the figure of Main PLL connection
57	Electrical Characteristics 4. AC Characteristics (6) Power-on Reset Timing	Changed the figure of timing
59-66	Electrical Characteristics 4. AC Characteristics (8) CSIO/UART Timing	· Modified from UART Timing to CSIO/UART Timing · Changed from Internal shift clock operation to Master mode · Changed from External shift clock operation to Slave mode
70	Electrical Characteristics 5. 12bit A/D Converter	Added the typical value of Integral Nonlinearity, Differential Nonlinearity, Zero transition voltage and Full-scale transition voltage
81	Ordering Information	Changed notation of part number

NOTE: Please see "Document History" about later revised information.

## Document History

Document Title: CY9A120L Series 32-bit ARM® Cortex®-M3 FM3 Microcontroller

Document Number: 002-05669

Revision	ECN	Submission Date	Description of Change
**	-	03/31/2015	Migrated to Cypress and assigned document number 002-05669. No change to document contents.
*A	5168181	03/28/2016	Updated to Cypress template.
*B	5658524	03/13/2017	Updated "12.4.7 Power-On Reset Timing": Changed parameter from "Power Supply rise time(Tr)[ms]" to "Power ramp rate(dV/dt)[mV/us]" and added some comments ( <a href="#">Page 56</a> ). Modified RTC description in "Features, Real-Time Clock(RTC)" as below Changed starting count value from 01 to 00. Deleted "second, or day of the week" in the Interrupt function ( <a href="#">Page 2</a> ). Added Notes for JTAG ( <a href="#">Page 23</a> ), Changed "J-TAG" to "JTAG" in "4 List of Pin Functions" ( <a href="#">Page 18</a> ). Updated Package code and dimensions as follows ( <a href="#">Page 7-12, 47, 80-86</a> ) FPT-48P-M49 -> LQA048, LCC-48P-M74 -> WNY048, FPT-52P-M02 -> LQC052, FPT-64P-M38 -> LQD064, FPT-64P-M39 -> LQG064, LCC-64P-M25 -> WNS064. Added the Baud rate spec in "12.4.9 CSIO/UART Timing" ( <a href="#">Page 58, 60, 62, 64</a> ). Completing Sunset Review.
*C	6516677	05/07/2019	Updated Document Title to read as "CY9A120L Series 32-bit ARM® Cortex®-M3 FM3 Microcontroller". Replaced "MB9A120L Series" with "CY9A120L Series" in all instances across the document. Updated Ordering Information: Updated part numbers. Updated to new template.
*D	8109122	02/18/2025	Updated the Product Lineup, packages, Pin Assignment, List of Pin Functions, Block Diagram, Memory Map. Removed the below part numbers in Ordering Information. <ul style="list-style-type: none"> <li>• CY9AF121KWQN-G-JNE2</li> <li>• CY9AF121KPMC1-G-JNE2</li> <li>• CY9AF121LPMC1-G-JNE2</li> <li>• CY9AF121LPMC-G-JNE2</li> <li>• CY9AF121LWQN-G-JNE2</li> </ul> Replaced Package Dimensions <ul style="list-style-type: none"> <li>• 002-13731 ** with Z8B00248754 V03</li> </ul>

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

### Products

ARM® Cortex® Microcontrollers	<a href="http://cypress.com/arm">cypress.com/arm</a>
Automotive	<a href="http://cypress.com/automotive">cypress.com/automotive</a>
Clocks & Buffers	<a href="http://cypress.com/clocks">cypress.com/clocks</a>
Interface	<a href="http://cypress.com/interface">cypress.com/interface</a>
Internet of Things	<a href="http://cypress.com/iot">cypress.com/iot</a>
Memory	<a href="http://cypress.com/memory">cypress.com/memory</a>
Microcontrollers	<a href="http://cypress.com/mcu">cypress.com/mcu</a>
PSoC	<a href="http://cypress.com/psoc">cypress.com/psoc</a>
Power Management ICs	<a href="http://cypress.com/pmic">cypress.com/pmic</a>
Touch Sensing	<a href="http://cypress.com/touch">cypress.com/touch</a>
USB Controllers	<a href="http://cypress.com/usb">cypress.com/usb</a>

Wireless Connectivity

[cypress.com/wireless](http://cypress.com/wireless)

### PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

### Cypress Developer Community

[Community](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

### Technical Support

[cypress.com/support](http://cypress.com/support)

ARM and Cortex are the registered trademarks of ARM Limited in the EU and other countries. All other trademarks or registered trademarks referenced herein are the property of their respective owners.

© Cypress Semiconductor Corporation, 2013-2025. This document is the property of Cypress Semiconductor Corporation and its subsidiaries ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress shall have no liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. CYPRESS DOES NOT REPRESENT, WARRANT, OR GUARANTEE THAT CYPRESS PRODUCTS, OR SYSTEMS CREATED USING CYPRESS PRODUCTS, WILL BE FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (collectively, "Security Breach"). Cypress disclaims any liability relating to any Security Breach, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any Security Breach. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. "High-Risk Device" means any device or system whose failure could cause personal injury, death, or property damage. Examples of High-Risk Devices are weapons, nuclear installations, surgical implants, and other medical devices. "Critical Component" means any component of a High-Risk Device whose failure to perform can be reasonably expected to cause, directly or indirectly, the failure of the High-Risk Device, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any use of a Cypress product as a Critical Component in a High-Risk Device. You shall indemnify and hold Cypress, its directors, officers, employees, agents, affiliates, distributors, and assigns harmless from and against all claims, costs, damages, and expenses, arising out of any claim, including claims for product liability, personal injury or death, or property damage arising from any use of a Cypress product as a Critical Component in a High-Risk Device. Cypress products are not intended or authorized for use as a Critical Component in any High-Risk Device except to the limited extent that (i) Cypress's published data sheet for the product explicitly states Cypress has qualified the product for use in a specific High-Risk Device, or (ii) Cypress has given you advance written authorization to use the product as a Critical Component in the specific High-Risk Device and you have signed a separate indemnification agreement.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit [cypress.com](http://cypress.com). Other names and brands may be claimed as property of their respective owners.