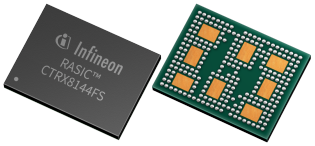
76-81 GHz Radar Transceiver with Antenna Feed in Package



AEC Qualified

RoHS

ISO 26262 compliant

Features

- Four transmit channels and four receive channels in form of waveguide ports
- RF range from 76 GHz to 81 GHz, with fast chirp modulation up to 200 MHz/µs and maximum chirp bandwidth of 4 GHz
- RF performance: TX output power of 14.5 dBm, TX phase noise of -100 dBc/Hz at 1 MHz, and RX noise figure (10 MHz) of 10.2 dB
- Extended functionality to support distributed imaging radar (DIR)
- Support of external reference clock
- Highly flexible sequencer with built-in memory for execution of user-defined ramp scenarios
- Digital PLL enables complex ramp scenario and fast modulation adaptation
- Industry leading RX input linearity (P_{1dB} min. -2.5 dBm) and RF port isolation (40 dB)
- Widely configurable Intermediate Frequency (IF) signal providing a bandwidth up to 22.5 MHz
- Optimized for low power consumption
- Configurable MIPI CSI-2 Interface
- Control and configure via SPI (up to 50 Mbps)
- Integrated housekeeping MCU and access to an external non-volatile memory to execute customized code via CSPI
- I2C enables communication with peripheral devices, e.g., a PMIC
- Built-in calibration and monitoring functionalities for safety applications
- ISO 26262 Safety Element out of Context for safety requirements up to ASIL B
- RoHS-compliant Flip Chip Ball Grid Array (FCBGA) package with 0.5 mm ball pitch

Potential applications

- Automatic Emergency Braking (AEB)
- Highway Assist/Pilot including Adaptive Cruise Control (ACC)
- Lane-Change Assistant (LCA)
- Traffic Jam Assist/Pilot (TJA)

Product validation

Product validation according to AEC-Q100 Grade 1, qualified for automotive applications.

Description

Infineon's RASIC™ CTRX8144FS is a 77 GHz radar transceiver for automotive ADAS applications featuring four transmit and four receive channels. This radar MMIC achieves high output power at low power consumption and industry-leading noise figure. CTRX8144FS is designed with optimized system cost in mind. The flexible configurable CSI-2 interface provides full compatibility to available processing solutions while also enabling connection of the device via a single CSI-2 interface.

The device has been designed using the latest automotive qualified RF technology and is housed inside an automotive-qualified FCBGA package.

Product type	Package	Marking
CTRX8144FS	PG-TF2BGA-xxx-x	CTRX8144FS

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1 Device configurations

The device can be used in a STAND-ALONE configuration or as either PRIMARY DIR or SECONDARY DIR MMIC in a distributed imaging radar (DIR) setup. The default mode (after power-up or hard reset) is STAND-ALONE configuration.

STAND-ALONE configuration:

The device can be configured as STAND-ALONE MMIC, in which case it utilizes an external crystal and generates the clock signal internally.

PRIMARY DIR configuration:

The PRIMARY DIR MMIC utilizes an external crystal and generates a clock signal together with a trigger to start a frequency ramp scenario via the CLKPHY pin. In the PRIMARY DIR configuration the device also uses the CLKPHY signal for self-feeding at CLKIN.

SECONDARY DIR configuration:

The SECONDARY DIR MMIC receives the clock and trigger signal from the PRIMARY DIR MMIC at the CLKIN pin.

Peripheral or MCU mode:

There is a MCU mode and a peripheral mode. In peripheral mode the device is controlled via SPI. In an MCU mode, the device is connected to an external non-volatile memory. Below there is an application example for both peripheral mode and MCU mode in STAND-ALONE configuration.

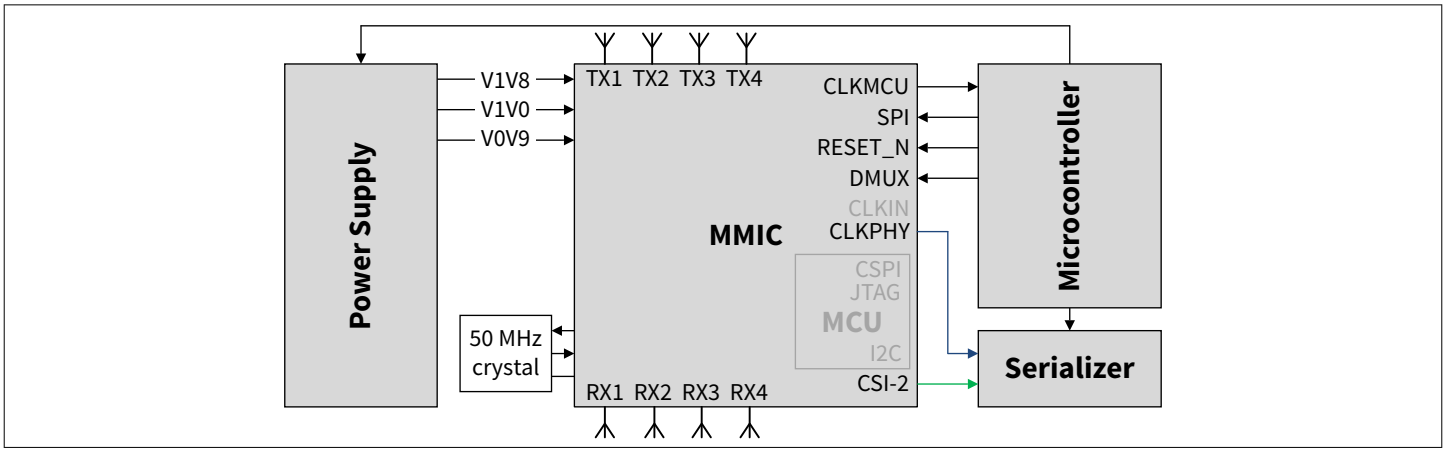


Figure 1 Application example with external MCU (= peripheral mode) and serializer

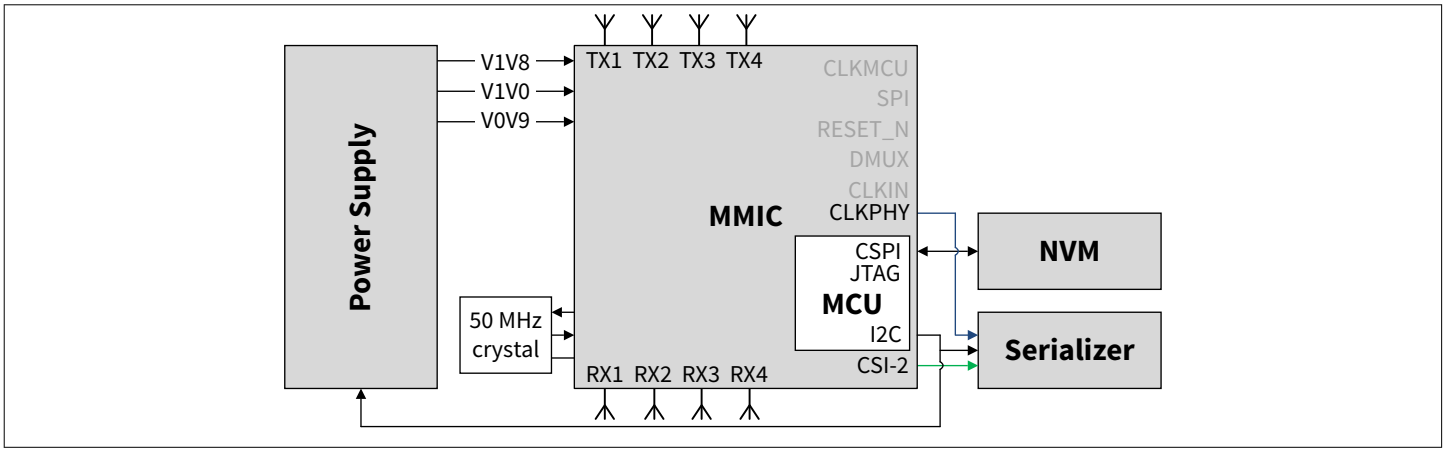


Figure 2 Application example with internal MCU (= MCU mode), external NVM and serializer

In addition, there is an application example for both; peripheral mode and MCU mode in a distributed imaging radar setup.

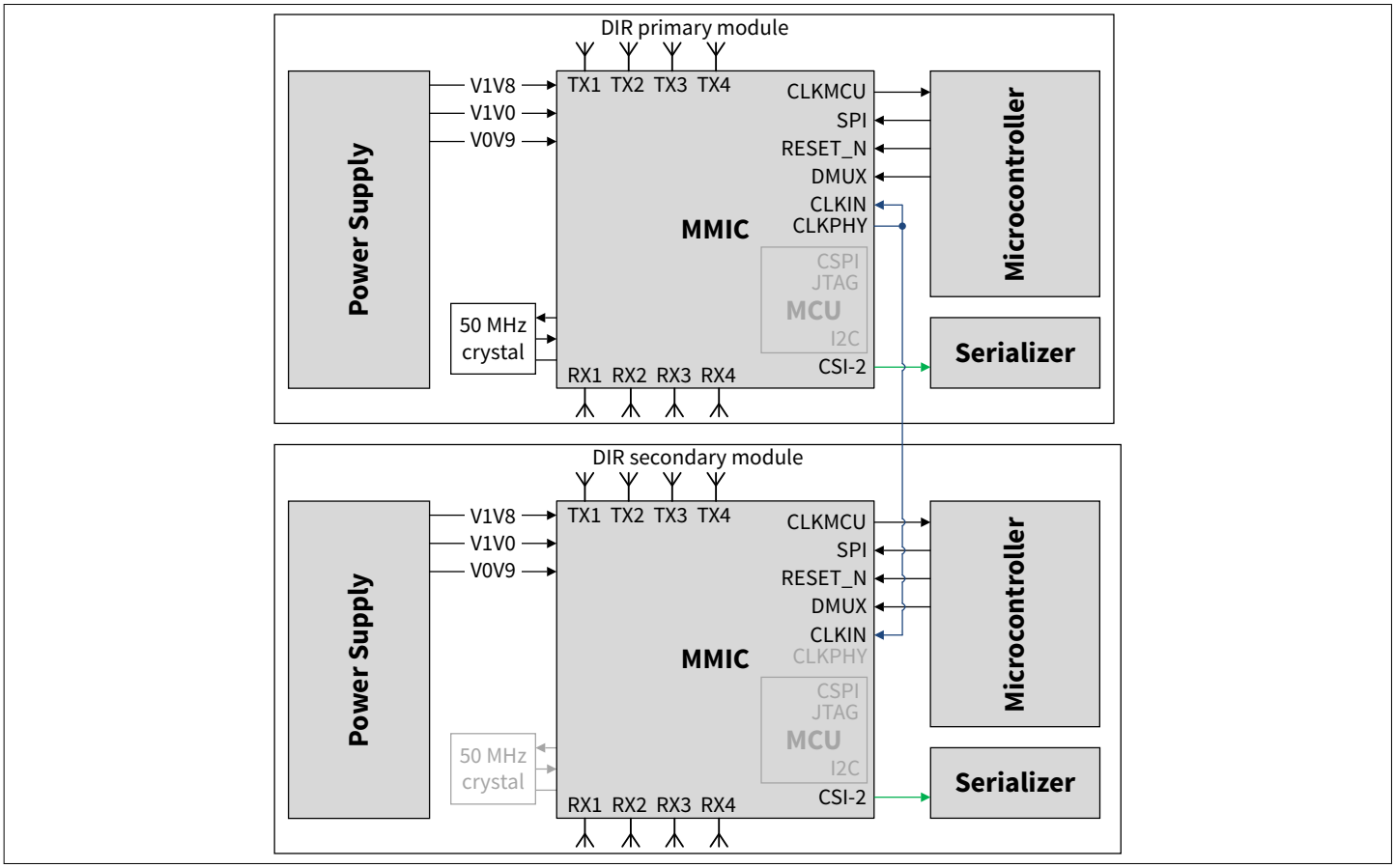


Figure 3 Application example (DIR) with external MCU (= peripheral mode) and serializer

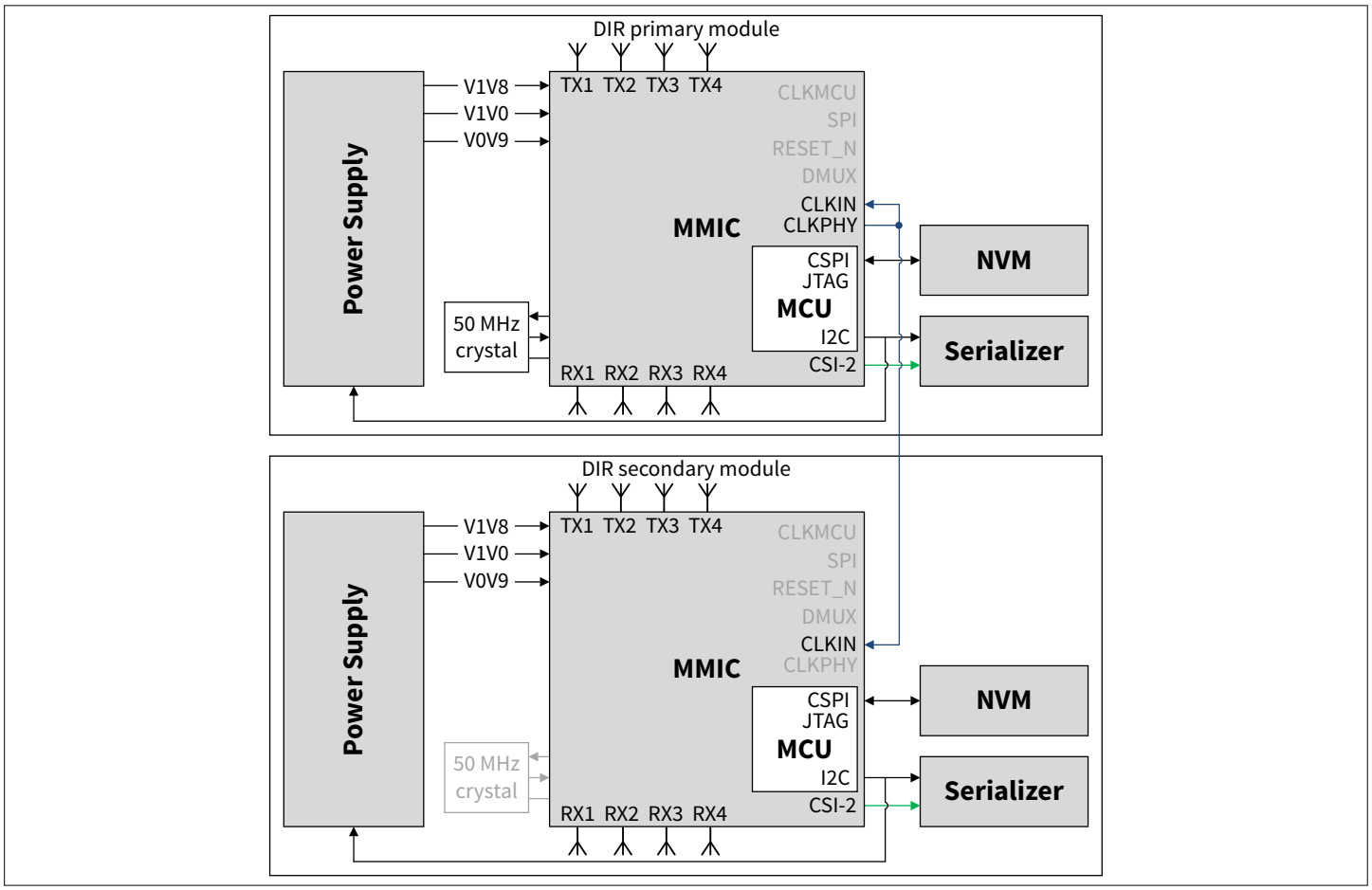


Figure 4 Application example (DIR) with internal MCU (= MCU mode), external NVM and serializer

2 Block diagram

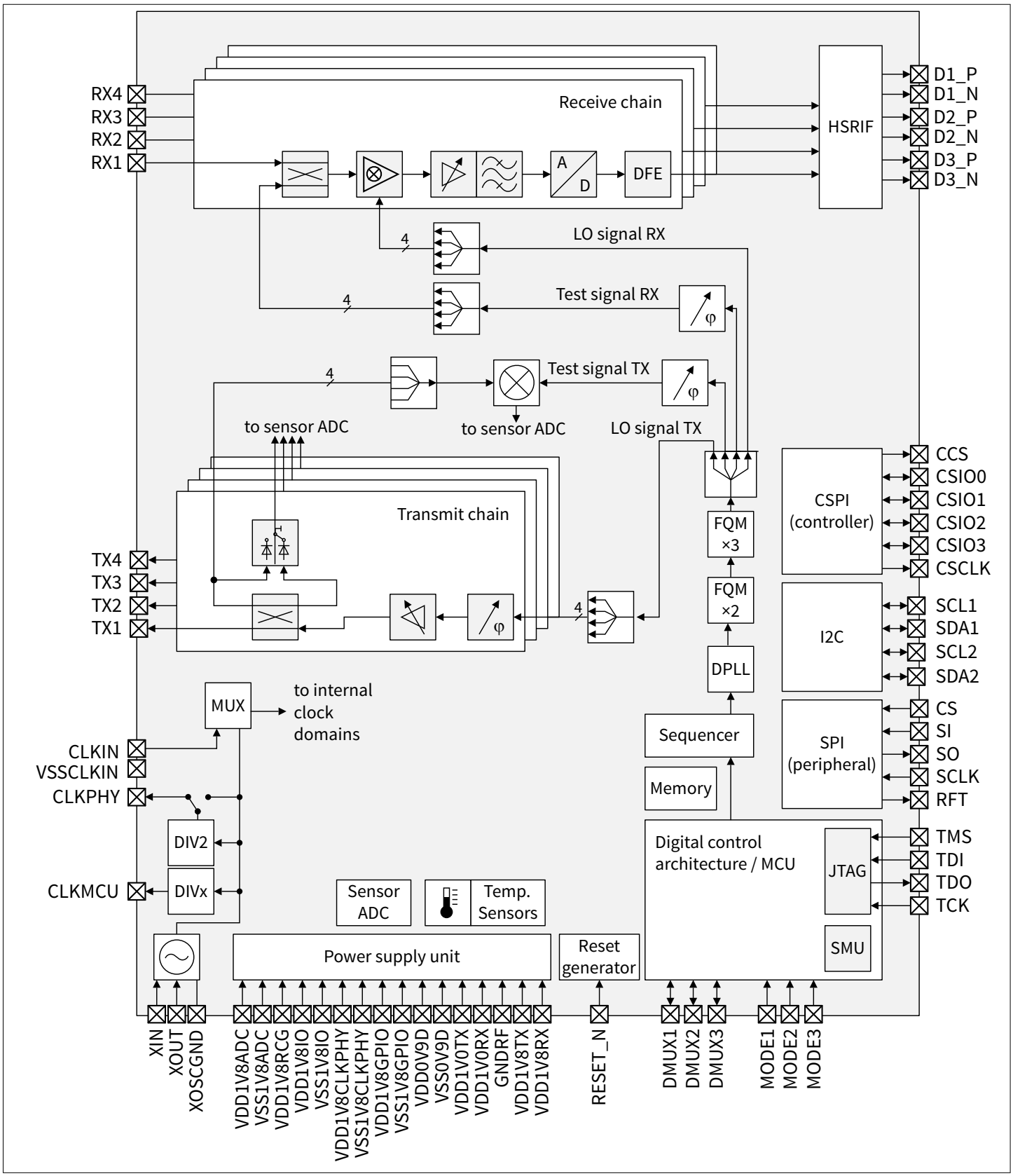


Figure 5 Block diagram

2.1 Application interfaces

The following list describes the hardware interfaces that are available at the ball out of the device used for common application purposes.

Table 1 Application interfaces

Parameter	Number	Interface type
RF transmit channels	4	waveguide ports
RF receive channels	4	waveguide ports
SPI interface	1	single-ended
CSPI interface	1	single-ended
I2C interface	2	single-ended
JTAG interface	1	single-ended
Mode interface	1	single-ended
HSRIF: MIPI D-Phy / CSI-2 channels	3	differential (2× data, 1× clock) MIPI D-Phy / CSI-2 physical pins
CLKIN interface	1	single-ended
Reference clock interface	1	single-ended input (XIN) single-ended output (XOUT)
25 MHz clock interface for the peripherals	1	single-ended output (CLKPHY)
Clock interface for the MCU	1	single-ended output (CLKMCU)
Power supply domains	3	power supply
DMUX pins	3	single-ended input / output
RESET_N pin	1	single-ended input

Interfaces used for common application purposes

RF transmitter

Output of the generated RF transmit signals.

RF receiver

Input of the received RF signals.

Serial Peripheral Interface (SPI)

The device acts as SPI-peripheral and provides access to firmware functions for configuration, control, and monitoring purposes:

- Download RAM firmware
- Configure ramp sequences
- Start and stop ramp execution
- Trigger monitoring and calibration and read-back results

- Read status information
- Configure internal modules (e.g., receiver, transmitter, monitoring, clock generation, etc.)

Controller Serial Peripheral Interface (CSPI)

The device acts as SPI-controller and provides access to an external non-volatile memory purposes:

- Load customized firmware
- Enable firmware updates
- Store/retrieve application data such as sequencer programs and calibration data

Inter-Integrated Circuit (I2C) interface

The I2C interface is used for communication with external components. The interface can operate in either controller or target role as required by the application.

Joint Test Action Group (JTAG) interface

The JTAG interface is used for debugging during development.

Mode interface

The mode interface is used to configure the device during startup e.g., to set it to MCU or peripheral mode.

High Speed Radar Interface (HSRIF) MIPI D-Phy/CSI-2 for sampled RX data

Serialization and transmission of the sampled IF data for RX data. The interface can be configured as up to 2 data channels and up to 1 clock channel.

CLKIN interface

The CLKIN interface enables clock feeding/self-feeding.

Reference clock interface (XIN / XOUT)

An internal RC oscillator is available inside of the MMIC which is intended to be used during start-up only. For radar operation a proper clock signal with an external crystal is needed to generate the reference clocks. If an external active clock source is connected to XIN, the XOUT pin must be left open.

25 MHz clock interface for the peripherals (CLKPHY)

The MMIC provides a clock output for driving the external peripherals interface.

Clock interface for the MCU (CLKMCU)

The MMIC provides a clock output as reference for external devices such as a microcontroller.

Power supply (PSUP)

All supply domains that need to be provided to the chip by external power sources.

Digital multiplexer (DMUX)

Enables to select alternative functions for external pins in order to provide a more flexible HW-SW interface. Mainly to communicate internal digital states and to apply external digital trigger signals.

Reset (RESET_N)

Active low external pin reset with internal pull-down resistor.

3 Ball diagram

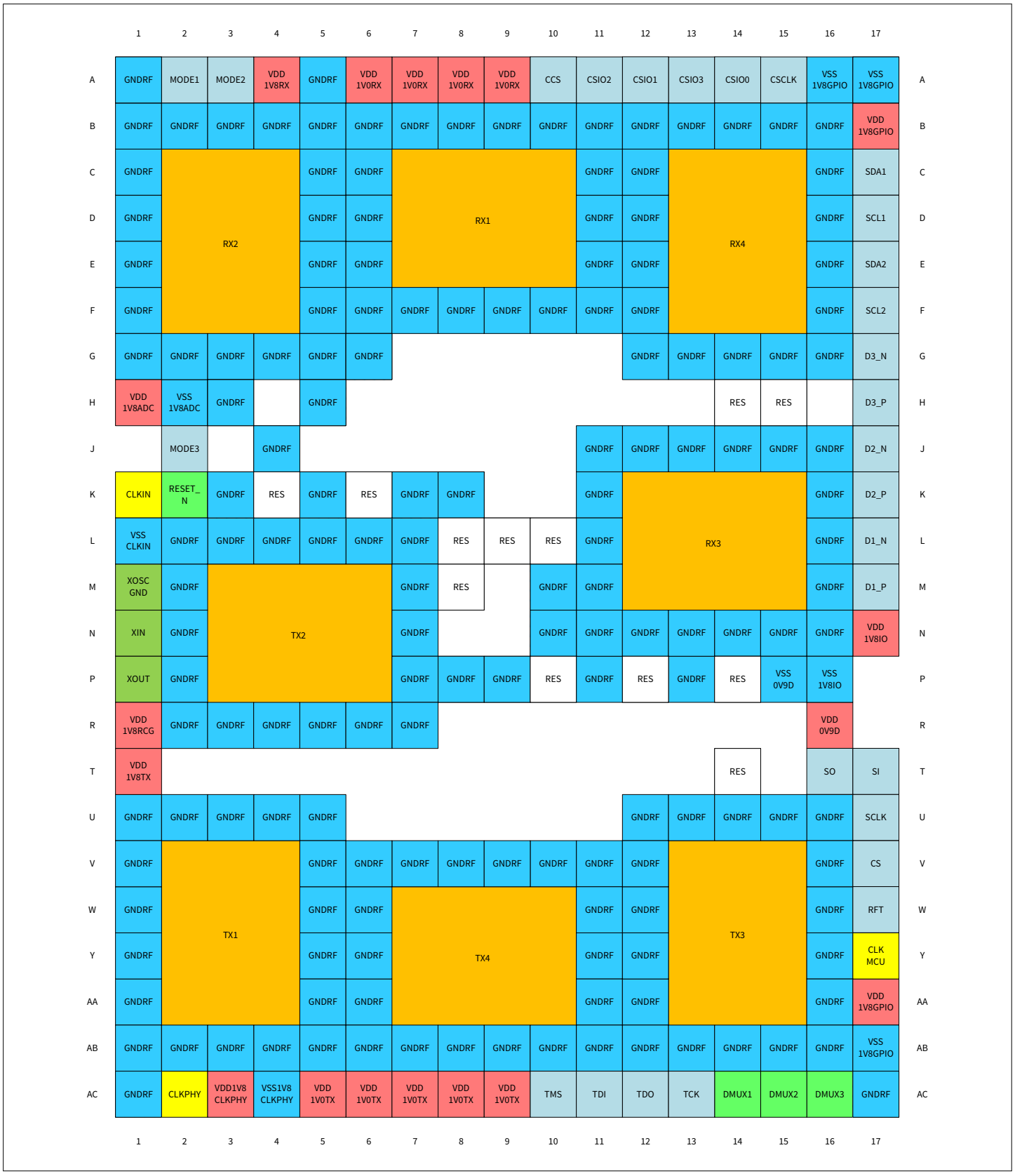


Figure 6 Ball out for FCBGA (top view)

***Note**: The Ball out is still subject to change.*

3.1 Ball definitions and functions

Table 2 RF Interfaces

Ball No.	Name	Pin Type	Buffer Type	Function
–	TX1	RFOUT	–	RF transmit output 1
–	TX2	RFOUT	–	RF transmit output 2
–	TX3	RFOUT	–	RF transmit output 3
–	TX4	RFOUT	–	RF transmit output 4
–	RX1	RFIN	–	RF receive input 1 Note: All RX need to be connected to an appropriate structure on PCB (e.g., antenna)
–	RX2	RFIN	–	RF receive input 2 Note: All RX need to be connected to an appropriate structure on PCB (e.g., antenna)
–	RX3	RFIN	–	RF receive input 3 Note: All RX need to be connected to an appropriate structure on PCB (e.g., antenna)
–	RX4	RFIN	–	RF receive input 4 Note: All RX need to be connected to an appropriate structure on PCB (e.g., antenna)

Table 3 High Speed Interface (CSI-2)

Ball No.	Name	Pin Type	Buffer Type	Function
M17	D1_P	HSI	CSI-2	CSI-2 differential output 1, true Leave this pin open if unused
L17	D1_N	HSI	CSI-2	CSI-2 differential output 1, complement Leave this pin open if unused
K17	D2_P	HSI	CSI-2	CSI-2 differential output 2, true Leave this pin open if unused
J17	D2_N	HSI	CSI-2	CSI-2 differential output 2, complement Leave this pin open if unused
H17	D3_P	HSI	CSI-2	CSI-2 differential output 3, true Leave this pin open if unused
G17	D3_N	HSI	CSI-2	CSI-2 differential output 3, complement Leave this pin open if unused

Table 4 Serial Peripheral Interface (SPI)

Ball No.	Name	Pin Type	Buffer Type	Function
W17	RFT	DIO	TTL / CMOS	Serial peripheral interface, ready for transfer Leave this pin open if unused
V17	CS	DIO	TTL / CMOS	Serial peripheral interface, chip select input Leave this pin open if unused
U17	SCLK	DIO	TTL / CMOS	Serial peripheral interface, clock input Leave this pin open if unused
T17	SI	DIO	TTL / CMOS	Serial peripheral interface, data input Leave this pin open if unused
T16	SO	DIO	TTL / CMOS	Serial peripheral interface, data output Leave this pin open if unused

Table 5 Controller-Serial Peripheral Interface (CSPI)

Ball No.	Name	Pin Type	Buffer Type	Function
A10	CCS	DIO	TTL / CMOS	Controller-serial peripheral interface, chip select input Leave this pin open if unused
A15	CSCLK	DIO	TTL / CMOS	Controller-serial peripheral interface, clock input Leave this pin open if unused
A14	CSIO0	DIO	TTL / CMOS	Controller-serial peripheral interface, data input/ output 0 Leave this pin open if unused
A12	CSIO1	DIO	TTL / CMOS	Controller-serial peripheral interface, data input/ output 1 Leave this pin open if unused
A11	CSIO2	DIO	TTL / CMOS	Controller-serial peripheral interface, data input/ output 2 Leave this pin open if unused
A13	CSIO3	DIO	TTL / CMOS	Controller-serial peripheral interface, data input/ output 3 Leave this pin open if unused

Table 6 Inter-Integrated Circuit (I2C) Interface

Ball No.	Name	Pin Type	Buffer Type	Function
C17	SDA1	DIO	TTL / CMOS	Inter-integrated circuit interface 1, serial data input/ output Leave this pin open if unused
E17	SDA2	DIO	TTL / CMOS	Inter-integrated circuit interface 2, serial data input/ output Leave this pin open if unused

(table continues...)

Table 6 (continued) Inter-Integrated Circuit (I2C) Interface

Ball No.	Name	Pin Type	Buffer Type	Function
D17	SCL1	DIO	TTL / CMOS	Inter-integrated circuit interface 1, serial clock input/ output Leave this pin open if unused
F17	SCL2	DIO	TTL / CMOS	Inter-integrated circuit interface 2, serial clock input/ output Leave this pin open if unused

Table 7 JTAG Interface

Ball No.	Name	Pin Type	Buffer Type	Function
AC13	TCK	DIO	TTL / CMOS	JTAG interface, test clock Connect this pin to GND if unused
AC10	TMS	DIO	TTL / CMOS	JTAG interface, test mode select Leave this pin open if unused
AC11	TDI	DIO	TTL / CMOS	JTAG interface, test data in Leave this pin open if unused
AC12	TDO	DIO	TTL / CMOS	JTAG interface, test data out Leave this pin open if unused

Table 8 Multiplexer

Ball No.	Name	Pin Type	Buffer Type	Function
AC14	DMUX1	DIO	TTL / CMOS	Digital multiplexer 1 Leave this pin open if unused
AC15	DMUX2	DIO	TTL / CMOS	Digital multiplexer 2 Leave this pin open if unused
AC16	DMUX3	DIO	TTL / CMOS	Digital multiplexer 3 Leave this pin open if unused

Table 9 Reference Clock Connections

Ball No.	Name	Pin Type	Buffer Type	Function
P1	XOUT	AIO0V9	–	Crystal connection Connect to 50 MHz crystal or leave open if external active clock source is connected to XIN Connect this pin to XOSCGND if unused (DIR SECONDARY MMIC)
N1	XIN	AIO0V9	–	Crystal connection Connect to 50 MHz crystal or external active clock source via AC coupling Connect this pin to XOSCGND if unused (DIR SECONDARY MMIC)

(table continues...)

Table 9 (continued) Reference Clock Connections

Ball No.	Name	Pin Type	Buffer Type	Function
M1	XOSCGND	GND	–	Crystal oscillator ground Do not connect this pin to a common GND on PCB

Table 10 Clock Input

Ball No.	Name	Pin Type	Buffer Type	Function
K1	CLKIN	AIO1V2	–	Clock input 50 MHz to enable CLK feeding/self-feeding Connect this pin to GND if unused

Table 11 Clock Outputs

Ball No.	Name	Pin Type	Buffer Type	Function
Y17	CLKMCU	DIO	TTL / CMOS	Clock output 25/40/50 MHz Leave this pin open if unused
AC2	CLKPHY	AIO1V8	–	Clock output 25/50 MHz Leave this pin open if unused

Table 12 Other Signals

Ball No.	Name	Pin Type	Buffer Type	Function
K2	RESET_N	DI	TTL / CMOS	Reset input (negative logic) Resets all sequential elements to their initial state; low active Note: there is a built-in pull-down resistor
A2	MODE1	DI	TTL / CMOS	Boot configuration selection bit 1
A3	MODE2	DI	TTL / CMOS	Boot configuration selection bit 2
J2	MODE3	DI	TTL / CMOS	Boot configuration selection bit 3

Table 13 Power Supply

Ball No.	Name	Pin Type	Buffer Type	Function
A6, A7, A8, A9,	VDD1V0RX	PWR	–	1.0 V power supply input, RF RX
AC5, AC6, AC7, AC8, AC9	VDD1V0TX	PWR	–	1.0 V power supply input, RF TX power amplifiers
H1	VDD1V8ADC	PWR	–	1.8 V power supply input, ADC
B17, AA17	VDD1V8GPIO	PWR	–	1.8 V power supply input, digital I/Os
AC3	VDD1V8CLKPHY	PWR	–	1.8 V power supply input, CLKPHY and CLKIN
A4	VDD1V8RX	PWR	–	1.8 V power supply input, RX analog
T1	VDD1V8TX	PWR	–	1.8 V power supply input, TX analog
N17	VDD1V8IO	PWR	–	1.8 V power supply input, I/Os

(table continues...)

Table 13 (continued) Power Supply

Ball No.	Name	Pin Type	Buffer Type	Function
R1	VDD1V8RCG	PWR	–	1.8 V power supply input, analog
R16	VDD0V9D	PWR	–	0.9V power supply input, digital

Table 14 Reserved

Ball No.	Name	Pin Type	Buffer Type	Function
H14, H15, K4, K6, L8, L9, L10, M8, P10, P12, P14, T14	RES	–	–	Internal use

Table 15 Ground

Ball No.	Name	Pin Type	Buffer Type	Function
A1, A5, B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, C1, C5, C6, C11, C12, C16, D1, D5, D6, D11, D12, D16, E1, E5, E6, E11, E12, E16, F1, F5, F6, F7, F8, F9, F10, F11, F12, F16, G1, G2, G3, G4, G5, G6, G12, G13, G14, G15, G16, H3, H5, J4, J11, J12, J13, J14, J15, J16, K3, K5, K7, K8, K11, K16, L2, L3, L4, L5, L6, L7, L11, L16, M2, M7, M10, M11, M16, N2, N7, N10, N11, N12, N13, N14, N15, N16, P2, P7, P8, P9, P11, P13, R2, R3, R4, R5, R6, R7, U1, U2, U3, U4, U5, U12, U13, U14, U15, U16, V1, V5, V6, V7, V8, V9, V10, V11, V12, V16, W1,W5, W6, W7, W11, W12, W16, Y1, Y5, Y6, Y11, Y12, Y16, AA1, AA5, AA6, AA11, AA12, AA16, AB1, AB2, AB3, AB4, AB5, AB6, AB7, AB8, AB9, AB10, AB11, AB12, AB13, AB14, AB15, AB16, AC1, AC17	GNDRF	GND	–	Ground
A16, A17, AB17	VSS1V8GPIO	GND	-	Ground of 1.8 V digital I/O domain
H2	VSS1V8ADC	GND	-	Ground of 1.8 V ADC domain
L1	VSSCLKIN	GND	-	Ground of CLK domain
P15	VSS0V9D	GND	-	Ground of 0.9 V digital domain
P16	VSS1V8IO	GND	-	Ground of 1.8 V digital I/O domain

(table continues...)

Table 15 (continued) Ground

Ball No.	Name	Pin Type	Buffer Type	Function
AC4	VSS1V8CLKPHY	GND	-	Ground of 1.8 V CLKPHY domain

4 General product characteristics

4.1 Absolute maximum ratings

Attention: ***Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the section "functional range" is not implied. Furthermore, only single error cases are assumed. More than one stress/error case may also damage the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions the voltage on VDD pins with respect to ground shall not exceed the values defined by the absolute maximum ratings. Lifetime statements are an anticipation based on an extrapolation of Infineon's qualification test results. The actual lifetime of a component depends on its form of application and type of use etc. and may deviate from such statement. Lifetime statements shall in no event extend the agreed warranty period.***

Table 16 Absolute maximum ratings

Absolute maximum ratings, ambient temperature not below -40°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Maximum RF input power, range 1	$P_{RF_MR_1}$	–	–	5	dBm	Do not operate the device for more than cumulated 300 h equally distributed within given input power range of +1 dBm to +5 dBm. Valid for interfaces of type RFIN and RFOUT.
Maximum RF input power, range 2	$P_{RF_MR_2}$	–	–	1	dBm	Valid for interfaces of type RFIN and RFOUT.
Maximum supply voltage VDD0V9D	V_{DD0V9D_MR}	-0.3	–	1.2	V	Do not operate the device for more than cumulated 2.8 h in the voltage range between max. V_{DD0V9D_FR} and max. V_{DD0V9D_MR}
Maximum supply voltage VDD1V0	V_{DD1V0_MR}	-0.3	–	1.2	V	Valid for all VDD1V0 domains. Do not operate the device for more than cumulated 2.8 h in the voltage range between max. V_{DD1V0_FR} and max. V_{DD1V0_MR}.
Maximum supply voltage VDD1V8	V_{DD1V8_MR}	-0.3	–	2.1	V	Valid for all VDD1V8 domains. Do not operate the device for more than cumulated 2.8 h in the voltage range between max. V_{DD1V8_FR} and max. V_{DD1V8_MR}
Maximum digital pin input voltage, relative	$V_{DIN_MR_rel}$	–	–	0.33	V	Referred to $V_{DD1V8GPIO}$. Valid for DIO and DI. In addition, the overload conditions apply.

(table continues...)

Table 16 (continued) Absolute maximum ratings

Absolute maximum ratings, ambient temperature not below -40°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Maximum digital pin input voltage, absolute	$V_{DIN_MR_abs}$	-0.3	–	2.1	V	Valid for DIO and DI. Do not operate the device for more than cumulated 2.8 h in the voltage range between max. V_{DD1V8_FR} and max. $V_{DIN_MR_abs}$.
Maximum analog pin input voltage VAIO1V8, relative	$V_{AIO1V8_MR_rel}$	–	–	0.33	V	Referred to V_{DD1V8}. Valid for AIO1V8. Do not operate the device for more than cumulated 2.8 h in the voltage range between max. V_{DD1V8_FR} and max. $V_{AIO1V8_MR_abs}$.
Maximum analog pin input voltage VAIO1V8, absolute	$V_{AIO1V8_MR_abs}$	-0.3	–	2.1	V	Valid for AIO1V8. Do not operate the device for more than cumulated 2.8 h in the voltage range between max. V_{DD1V8_FR} and max. $V_{AIO1V8_MR_abs}$.
Maximum analog pin input voltage VAIO0V9, relative	$V_{AIO0V9_MR_rel}$	–	–	0.33	V	Referred to VDD1V8. Valid for XIN.
Maximum analog pin input voltage VAIO0V9, absolute	$V_{AIO0V9_MR_abs}$	-0.3	–	1.2	V	Valid for XIN.
Maximum CLKIN pin voltage, absolute	V_{CLKIN_MR}	-0.3	–	1.2	V	Valid for CLKIN pin. Voltage at CLKIN pin refers to CLKIN_REF
Inactive device: Maximum digital pin input current, 1	$I_{DIN_inact_1}$	-1	–	1	mA	All power supplies at 0 V, pin currents with different polarity not subtracted from each other
Inactive device: Maximum digital pin input current, 2	$I_{DIN_inact_2}$	-10	–	10	mA	All power supplies at 0 V, pin currents with different polarity not subtracted from each other. Do not operate the device for more than cumulated 2.8 h in this condition.

(table continues...)

Table 16 (continued) Absolute maximum ratings

Absolute maximum ratings, ambient temperature not below -40°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Inactive device: Sum of all digital pin input current, 1	$\Sigma I_{DIN_inact_1}$	-20	–	20	mA	All power supplies at 0 V, pin currents with different polarity not subtracted from each other
Inactive device: Sum of all digital pin input current, 2	$\Sigma I_{DIN_inact_2}$	-50	–	50	mA	All power supplies at 0 V, pin currents with different polarity not subtracted from each other. Do not operate the device for more than cumulated 2.8 h in this condition.
Storage temperature	T_{store}	-50	–	150	°C	–
Junction temperature range	T_{J_MR}	-40	–	138	°C	On-chip temperature sensor read values. Failure indication B is executed at a temperature sensor reading of equal or more than 138°C. Do not operate the device for more than cumulated 2.8 h in the temperature range between max. T_J and max. T_{J_MR}.
ESD robustness						
ESD robustness (HBM)	V_{ESD_HBM}	-1	–	1	kV	Human body model (HBM) robustness for ≤ 28 nm according to AEC - Q100 Rev-J. Latchup robustness: class II according to AEC - Q100-004.
ESD robustness (CDM)	V_{ESD_CDM}	-250	–	250	V	Charged device model (CDM) robustness for ≤ 28 nm according to AEC - Q100 Rev-J; voltage level refers to test condition (TC) mentioned in the standard. Latchup robustness: class II according to AEC - Q100-004.

4.2 Functional range

The following functional range must not be exceeded in order to ensure correct operation of the device. All parameters specified in the following sections refer to these operating conditions unless otherwise indicated.

Table 17 Functional range

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply voltage VDD0V9D	V_{DD0V9D_FR}	0.855	0.9	0.945	V	–
Supply voltage VDD1V0	V_{DD1V0_FR}	0.95	1.0	1.05	V	Valid for all VDD1V0 domains.
Supply voltage VDD1V8	V_{DD1V8_FR}	1.71	1.8	1.89	V	Valid for all VDD1V8 domains.
Operating temperature	T_J	-40	–	135	°C	On-chip temperature sensor read values. Ambient temperature not below -40°C according to AEC-Q100 grade 1.
RF operating frequency	f_{RF}	76	–	81	GHz	–
IF bandwidth	f_{IF}	0.001	–	22.5	MHz	–
Power Supply Slope	V_{slope}	2×10^{-6}	–	2	V/µs	Valid for all power supply rails during power-up.

4.3 Firmware functions in RAM

To operate the MMIC, it is needed to download a RAM FW to the MMIC prior to operation once upon power-on, hard reset and depending on the error also after soft reset. Alternatively, the MMIC can load the RAM firmware (including customer FW) during startup from an external flash. Please note that the parameters within this specification are only valid for the RAM FW approved by Infineon accordingly.

4.4 Thermal resistance

Table 18 Thermal resistance

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Thermal resistance junction to ball PCB side	R_{th_JB}	–	5	–	K/W	Junction to ball PCB side. Values are simulated for the following use case: all transmitters at max. output power, all receivers enabled.
Thermal resistance junction to case	R_{th_JC}	–	4	–	K/W	Junction to package case top. Values are simulated for the following use case: all transmitters at max. output power, all receivers enabled.

4.5 Power supply

4.5.1 Power consumption

Table 19 Average power consumption of typical application use cases

Parameter	Description	Typ. Value	Unit	Condition
Average power consumption, stand-alone	Radar cycle 50 ms each (averaged over 2 cycles) 12 ms acquisition 4 ms state transitions 1 ms monitoring 30 ms low power state 3 ms calibration TX/RX monitoring spread across 2 cycles TX/RX calibration done every 10th cycle	0.5	W	1 TX (at max. power), 4 RX
		0.6	W	2 TX (at max. power), 4 RX
		0.7	W	3 TX (at max. power), 4 RX
		0.8	W	4 TX (at max. power), 4 RX

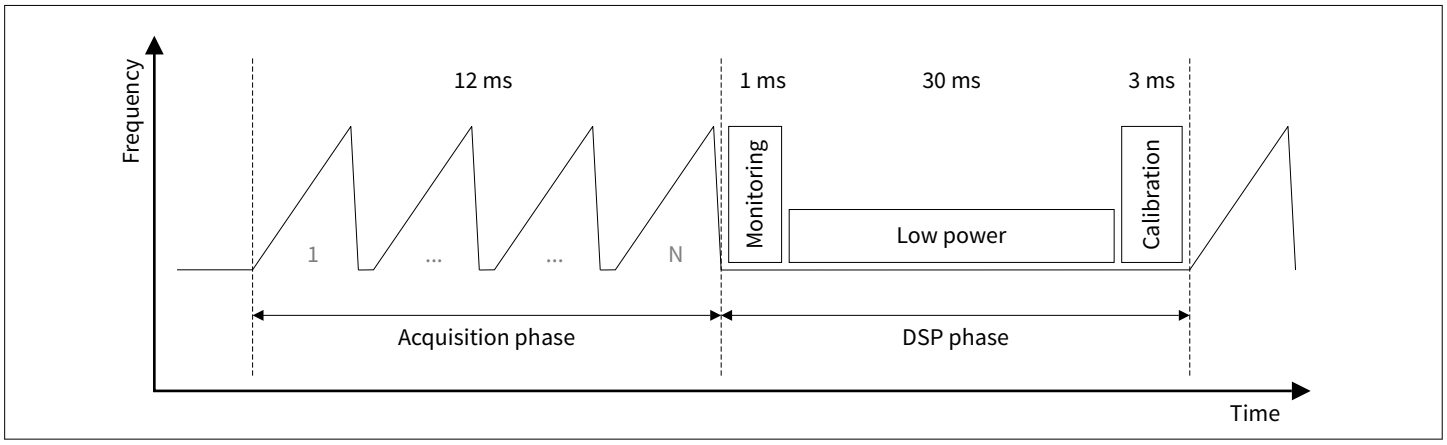


Figure 7 Example use case for average power consumption

4.5.2 Power supply noise

Table 20 defines the max. allowed noise levels at the power supply domains.

Table 20 Power supply noise

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VDD1V8						
Supply noise 1V8 @ 100 kHz	$N_{supply_1V8_100k}$	–	–	225	nV/√Hz	f = 100 kHz Valid for all 1V8 domains except VDD1V8GPIO. Exclusion also possible for VDD1V8CLKPHY if associated functionality (CLKPHY, CLKIN) is not used.
Supply noise 1V8 @ 1 MHz	$N_{supply_1V8_1M}$	–	–	110	nV/√Hz	Linear interpolation on a log-log scale for 100 kHz < f ≤ 1 MHz. Valid for all 1V8 domains except VDD1V8GPIO. Exclusion also possible for VDD1V8CLKPHY if associated functionality (CLKPHY, CLKIN) is not used.
Supply noise 1V8 @ 10 MHz	$N_{supply_1V8_10M}$	–	–	35	nV/√Hz	Linear interpolation on a log-log scale for 1 MHz < f ≤ 10 MHz. Valid for all 1V8 domains except VDD1V8GPIO. Exclusion also possible for VDD1V8CLKPHY if associated functionality (CLKPHY, CLKIN) is not used.
Supply noise 1V8 @ 22.5 MHz	$N_{supply_1V8_22.5M}$	–	–	20	nV/√Hz	Linear interpolation on a log-log scale for 10 MHz < f ≤ 22.5 MHz. Valid for all 1V8 domains except VDD1V8GPIO. Exclusion also possible for VDD1V8CLKPHY if associated functionality (CLKPHY, CLKIN) is not used.
VDD1V0TX						
Supply noise 1V0TX @ 100 kHz	$N_{supply_1V0TX_100k}$	–	–	191	nV/√Hz	f = 100 kHz
Supply noise 1V0TX @ 1 MHz	$N_{supply_1V0TX_1M}$	–	–	44	nV/√Hz	Linear interpolation on a log-log scale for 100 kHz < f ≤ 1 MHz.
Supply noise 1V0TX @ 10 MHz	$N_{supply_1V0TX_10M}$	–	–	32	nV/√Hz	Linear interpolation on a log-log scale for 1 MHz < f ≤ 10 MHz.
Supply noise 1V0TX @ 22.5 MHz	$N_{supply_1V0TX_22.5M}$	–	–	27	nV/√Hz	Linear interpolation on a log-log scale for 10 MHz < f ≤ 22.5 MHz.
VDD1V0RX						
Supply noise 1V0RX @ 100 kHz	$N_{supply_1V0RX_100k}$	–	–	367	nV/√Hz	f = 100 kHz
Supply noise 1V0RX @ 1 MHz	$N_{supply_1V0RX_1M}$	–	–	68	nV/√Hz	Linear interpolation on a log-log scale for 100 kHz < f ≤ 1 MHz.

(table continues...)

Table 20 (continued) Power supply noise

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply noise 1V0RX @ 10 MHz	$N_{supply_1V0RX_10M}$	–	–	35	nV/√Hz	Linear interpolation on a log-log scale for 1 MHz < f ≤ 10 MHz.
Supply noise 1V0RX @ 22.5 MHz	$N_{supply_1V0RX_22.5M}$	–	–	23	nV/√Hz	Linear interpolation on a log-log scale for 10 MHz < f ≤ 22.5 MHz.

4.5.3 Power supply spurs

Table 21 defines the max. allowed spur levels at the power supply domains.

Table 21 Power supply spurs

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VDD1V8						
Supply spurs 1V8 @ 100 kHz	$S_{supply_1V8_100k}$	–	–	25	µVp	f = 100 kHz Valid for all 1V8 domains except VDD1V8GPIO. Exclusion also possible for VDD1V8PHYETH if associated functionality (CLKPHY, CLKIN) is not used.
Supply spurs 1V8 @ 1 MHz	$S_{supply_1V8_1M}$	–	–	12	µVp	Linear interpolation on a log-log scale for 100 kHz < f ≤ 1 MHz. Valid for all 1V8 domains except VDD1V8GPIO. Exclusion also possible for VDD1V8PHYETH if associated functionality (CLKPHY, CLKIN) is not used.
Supply spurs 1V8 @ 10 MHz	$S_{supply_1V8_10M}$	–	–	5	µVp	Linear interpolation on a log-log scale for 1 MHz < f ≤ 10 MHz. Valid for all 1V8 domains except VDD1V8GPIO. Exclusion also possible for VDD1V8PHYETH if associated functionality (CLKPHY, CLKIN) is not used.
Supply spurs 1V8 @ 22.5 MHz	$S_{supply_1V8_22.5M}$	–	–	3	µVp	Linear interpolation on a log-log scale for 10 MHz < f ≤ 22.5 MHz. Valid for all 1V8 domains except VDD1V8GPIO. Exclusion also possible for VDD1V8PHYETH if associated functionality (CLKPHY, CLKIN) is not used.
VDD1V0TX						
Supply spurs 1V0TX @ 100 kHz	$S_{supply_1V0TX_100k}$	–	–	39	µVp	f = 100 kHz
Supply spurs 1V0TX @ 1 MHz	$S_{supply_1V0TX_1M}$	–	–	9	µVp	Linear interpolation on a log-log scale for 100 kHz < f ≤ 1 MHz.

(table continues...)

Table 21 (continued) Power supply spurs

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply spurs 1V0TX @ 10 MHz	$S_{supply_1V0TX_10M}$	–	–	8	µVp	Linear interpolation on a log-log scale for 1 MHz < f ≤ 10 MHz.
Supply spurs 1V0TX @ 22.5 MHz	$S_{supply_1V0TX_22.5M}$	–	–	6	µVp	Linear interpolation on a log-log scale for 10 MHz < f ≤ 22.5 MHz.
VDD1V0RX						
Supply spurs 1V0RX @ 100 kHz	$S_{supply_1V0RX_100k}$	–	–	83	µVp	f = 100 kHz
Supply spurs 1V0RX @ 1 MHz	$S_{supply_1V0RX_1M}$	–	–	10	µVp	Linear interpolation on a log-log scale for 100 kHz < f ≤ 1 MHz.
Supply spurs 1V0RX @ 10 MHz	$S_{supply_1V0RX_10M}$	–	–	6	µVp	Linear interpolation on a log-log scale for 1 MHz < f ≤ 10 MHz.
Supply spurs 1V0RX @ 22.5 MHz	$S_{supply_1V0RX_22.5M}$	–	–	5	µVp	Linear interpolation on a log-log scale for 10 MHz < f ≤ 22.5 MHz.

4.5.4 Current consumption

Table 22 Current consumption

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Current consumption, VDD0V9D	I_{DD0V9D}	–	100	400	mA	CLKPHY on, DMUX pins in default configuration, and no currents at the remaining digital IO pins. All receivers on, all transmitters on.
Current consumption per TX, VDD1V0TX	$I_{DD1V0TX_n}$	–	400	500	mA	Adder per activated TX channel with output power set to maximum (output power reduction set to zero).
Current consumption 4RX, VDD1V0RX	$I_{DD1V0RX}$	–	600	800	mA	All receivers on.
Current consumption 0TX, STAND-ALONE, VDD1V0TX	$I_{DD1V0TX_0}$	–	150	200	mA	All transmitters off.

(table continues...)

Table 22 (continued) Current consumption

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Current consumption, STAND-ALONE, VDD1V8	I_{DD1V8}	–	400	500	mA	Valid for total current of all 1.8 V power supplies. All receivers on.
Current consumption 4TX/4RX, VDD1V0TX	$I_{DD1V0TX_4}$	–	1900	2100	mA	All transmitters on with maximum output power.

5 Electrical characteristics

Functional supply voltage ranges, T_J = -40°C to 135°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified), parameters specified in the frequency range from 76 GHz to 81 GHz.

All RF parameters are referred to an RF reference plane located at the opposite side of the PCB compared to the product, as defined in following figure:

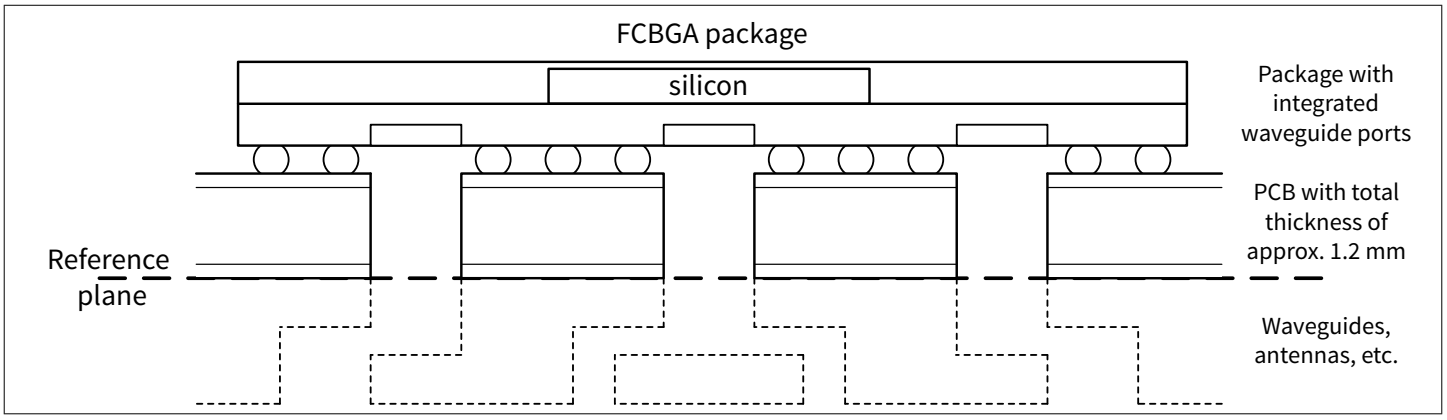


Figure 8 Definition of RF reference plane

The PCB has a total thickness of 1.2 mm. The top copper layer and the bottom copper layer of the PCB have OSP or chemical Sn finish.

The transition from chip to RF reference plane is optimized considering an impedance on the RF reference plane, defined by the waveguide impedance of an ideal air filled waveguide. On the PCB, the reference waveguide cut-out design and solder footprints are defined in following figure with the inner walls of the cut-outs metalized:

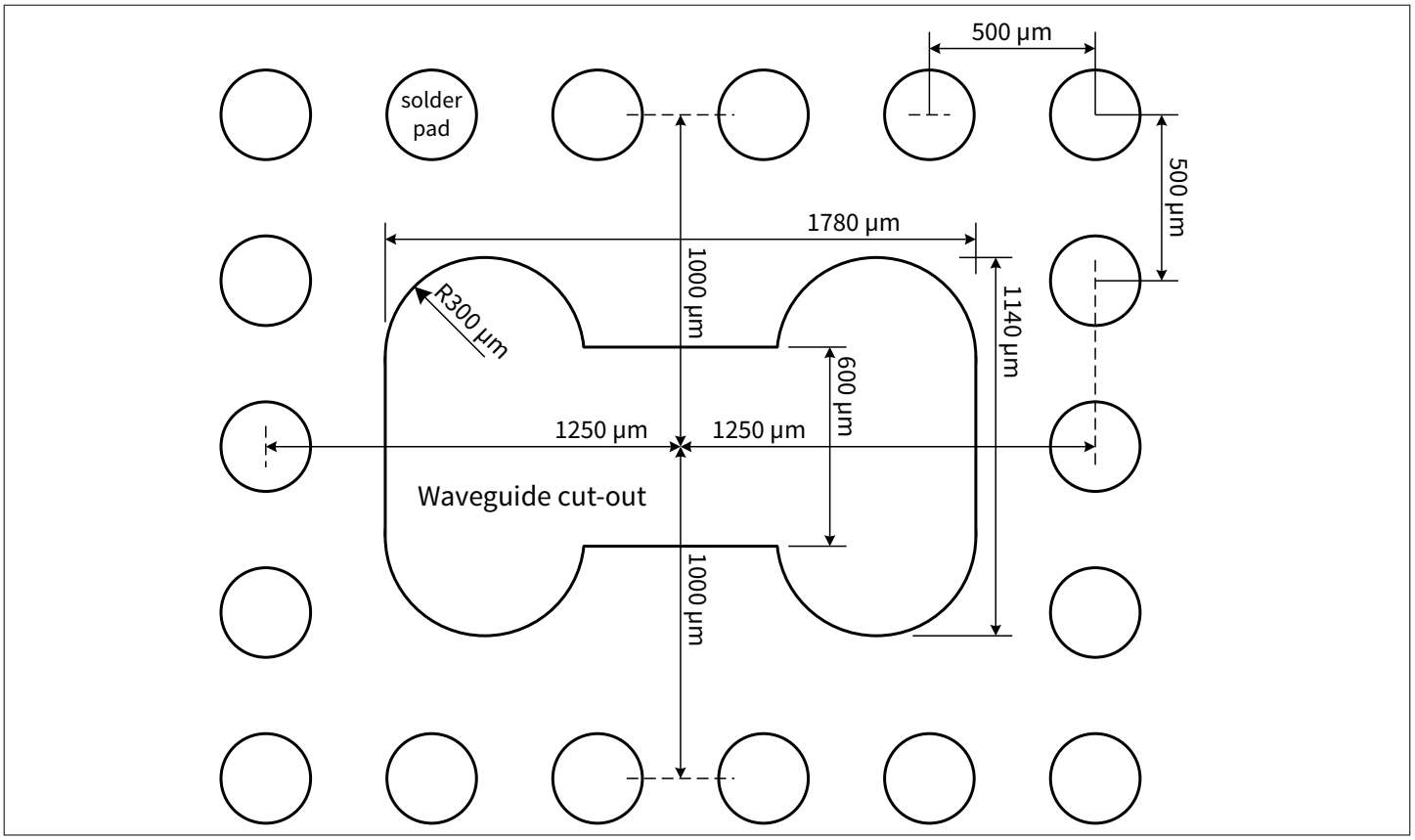


Figure 9 Reference waveguide design

5.1 General

Table 23 General characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Isolation between TX and RX ports	$ISO_{TX/RX}$	40	–	–	dB	Applicable for an Infineon reference footprint.

5.2 Transmitter

5.2.1 General characteristics

Table 24 General characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
RF output power at maximum setting	P_{out}	13.0	14.5	16.0	dBm	Maximal output power setting of a single TX channel.
Isolation between TX ports	$ISO_{TX/TX}$	40	–	–	dB	Applicable for an Infineon reference footprint.
TX phase noise @ 10 kHz, RF range 1	$N_{\varphi_10k_RF1}$	–	-79	-73	dBc/Hz	Valid for 76 ≤ f_{RF} ≤ 77 GHz. Continuous wave (CW) mode. f_{offset} = 10 kHz.
TX phase noise @ 100 kHz, RF range 1	$N_{\varphi_100k_RF1}$	–	-80	-75	dBc/Hz	Valid for 76 ≤ f_{RF} ≤ 77 GHz. Continuous wave (CW) mode. f_{offset} = 100 kHz.
TX phase noise @ 1 MHz, RF range 1	$N_{\varphi_1M_RF1}$	–	-100	-97	dBc/Hz	Valid for 76 ≤ f_{RF} ≤ 77 GHz. Continuous wave (CW) mode. f_{offset} = 1 MHz.
TX phase noise @ 5 MHz, RF range 1	$N_{\varphi_5M_RF1}$	–	-116	-111	dBc/Hz	Valid for 76 ≤ f_{RF} ≤ 77 GHz. Continuous wave (CW) mode. f_{offset} = 5 MHz.
TX phase noise @ 10 MHz, RF range 1	$N_{\varphi_10M_RF1}$	–	-121	-115	dBc/Hz	Valid for 76 ≤ f_{RF} ≤ 77 GHz. Continuous wave (CW) mode. f_{offset} = 10 MHz.
TX phase noise @ 10 kHz, RF range 2	$N_{\varphi_10k_RF2}$	–	-78	-73	dBc/Hz	Valid for 77 GHz < f_{RF} ≤ 81 GHz. Continuous wave (CW) mode. f_{offset} = 10 kHz.

(table continues...)

Table 24 (continued) General characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
TX phase noise @ 100 kHz, RF range 2	$N_{\varphi_100k_RF2}$	–	-78	-73	dBc/Hz	Valid for 77 GHz < f_{RF} ≤ 81 GHz. Continuous wave (CW) mode. f_{offset} = 100 kHz.
TX phase noise @ 1 MHz, RF range 2	$N_{\varphi_1M_RF2}$	–	-98	-95	dBc/Hz	Valid for 77 GHz < f_{RF} ≤ 81 GHz. Continuous wave (CW) mode. f_{offset} = 1 MHz.
TX phase noise @ 5 MHz, RF range 2	$N_{\varphi_5M_RF2}$	–	-114	-109	dBc/Hz	Valid for 77 GHz < f_{RF} ≤ 81 GHz. Continuous wave (CW) mode. f_{offset} = 5 MHz.
TX phase noise @ 10 MHz, RF range 2	$N_{\varphi_10M_RF2}$	–	-120	-114	dBc/Hz	Valid for 77 GHz < f_{RF} ≤ 81 GHz. Continuous wave (CW) mode. f_{offset} = 10 MHz.
TX channel to channel output power drift, range 1	$\lvert P_{drift_TX_1}\rvert$	–	–	1	dB	Power range 1: 0 dB to 3 dB TX output power reduction relative to max. TX output power setting. TX output power drift of the pair of two TX channels relative to each other. See definition of TX channel to channel output power drift for specification conditions.
TX channel to channel output power drift, range 2	$\lvert P_{drift_TX_2}\rvert$	–	–	1.5	dB	Power range 2: 3 dB to 6 dB TX output power reduction relative to max. TX output power setting. TX output power drift of the pair of two TX channels relative to each other. See definition of TX channel to channel output power drift for specification conditions.

Definition of TX channel to channel output power drift

Definition of TX channel to channel output power drift of two transmit channels relative to each other over temperature, supply voltage, RF frequency and time. The transmit power channel to channel drift complies to the following formula:

$$\left|10 \cdot \log\left(\frac{P_m(t_1, f_1, \varphi_{m1}, T_1, V_{DD1})}{P_n(t_1, f_1, \varphi_{n1}, T1, V_{DD1})}\right) - 10 \cdot \log\left(\frac{P_m(t_2, f_2, \varphi_{m2}, T_2, V_{DD2})}{P_n(t_2, f_2, \varphi_{n2}, T_2, V_{DD2})}\right)\right| \leq P_{drift_TX} \quad [\text{dB}] \qquad (1)$$

$\Delta f = |f_1 - f_2|$
$\Delta f \leq 0.5$ GHz
whereas:

- $P_{m,n}$ ... transmit output power in W
- $_{m,n}$ ... channel number of transmit channel

- φ_m ... relative phase of channel m calibrated together with wanted offset power level P_m
- φ_n ... relative phase of channel n calibrated together with wanted offset power level P_n
- t_1, t_2 ... times difference as short as required to settle new conditions within a power cycle of max. 12 h
- f_1, f_2 ... RF frequency within range of operation
- T_1, T_2 ... temperature within range of operation
- V_{DD1}, V_{DD2} ... VDD1V0TX and VDD1V8 supply voltage within range of operation

Premise:
- Power reduction max. 6 dB nominal from max. TX power.
- Transmitting output power and relative phase have to be calibrated together before each measurement.

5.2.2 PLL and VCO

Table 25 PLL and VCO

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
RF overshoot/ undershoot	$f_{DPLL_overshoot}$	–	–	15	MHz	RF bandwidth: 4 GHz, Flyback time: 1 µs.
Measurement ramp slope	$\lvert S_{ramp} \rvert$	3	–	200	MHz/µs	Valid for up- and down-ramp. Parameter ideal ramp deviation error need to be fulfilled.
Static RF frequency resolution	f_{res}	4.5	–	4.6	kHz	CW Static frequency step size. Exact value depends on the accuracy of the external 50 MHz crystal and is defined with f_{ext} (50 MHz)/2^{16} × 6.
Continuously adjustable RF frequency range	f_{ramp}	100	–	4000	MHz	In either up or down direction between 76 and 81 GHz. Payload ramp frequency must be ≥ 100 MHz.
Frequency ramp duration	$t_{payload}$	5.12	–	409.6	µs	Valid for payload ramp segment
Flyback time to reach start frequency of following chirp	$t_{flyback}$	–	–	1	µs	Time until frequency meets start frequency within ±500 kHz starting from chirp end frequency with 4 GHz frequency step.
TX settling time	t_{TX_set}	–	–	1.5	µs	Time from the beginning of chirp (t_{ref} = 0) until ramp linearity requirement (deviation from ideal ramp) is met.
Wait time after TX re-configuration	t_{TX_wait}	–	–	1	µs	Valid for changes on one single channel or multiple channels in parallel Wait time after • enabling or disabling internal load • new TX power and phase setting

(table continues...)

Table 25 (continued) PLL and VCO

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Post payload segment	t_{post}	40	–	–	ns	Same slope as payload segment. Same settings as for payload segment with the following exceptions: • RX sampling disabled (CONFIG0.RX_PAYLOAD_GATE = 0) • Bit CONFIG0.RX_SRC_CNT_RST = 0

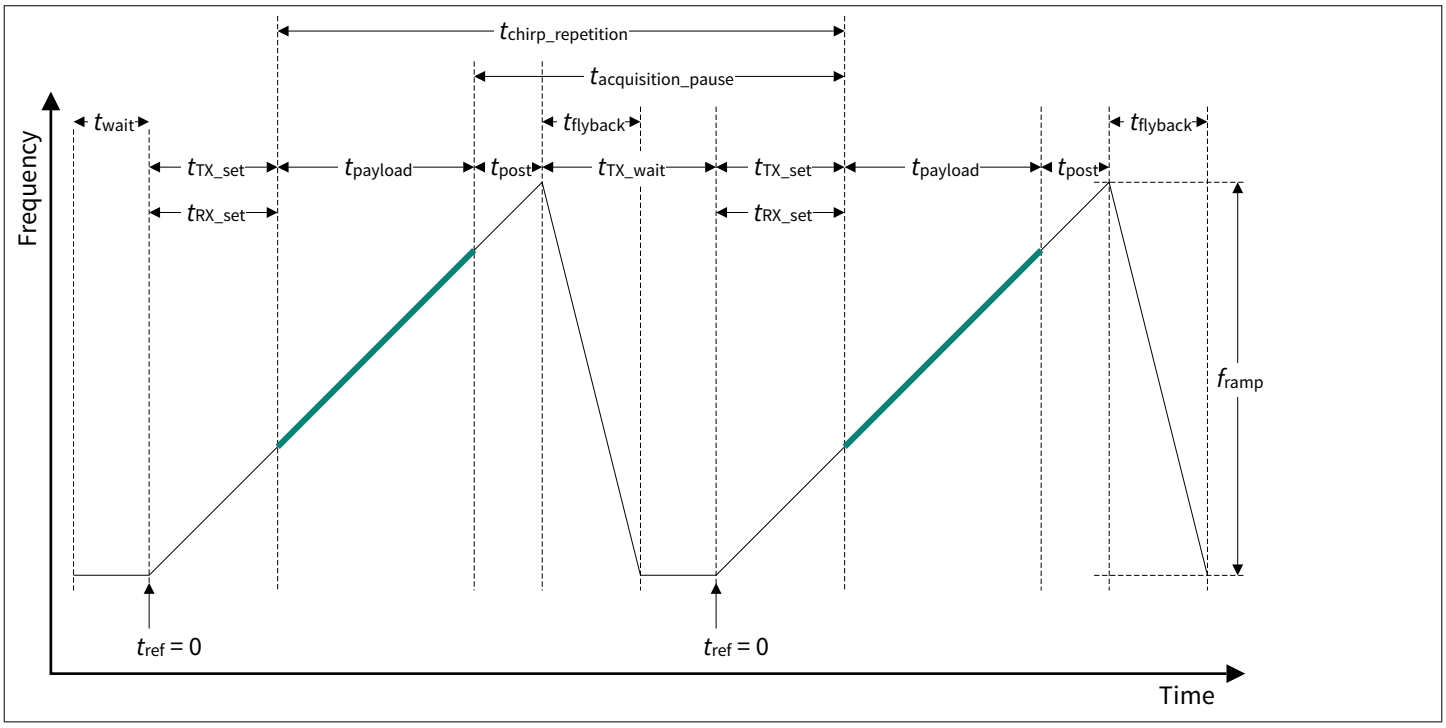


Figure 10 Definition of frequency ramp timings

RF frequency overshoot/undershoot after flyback

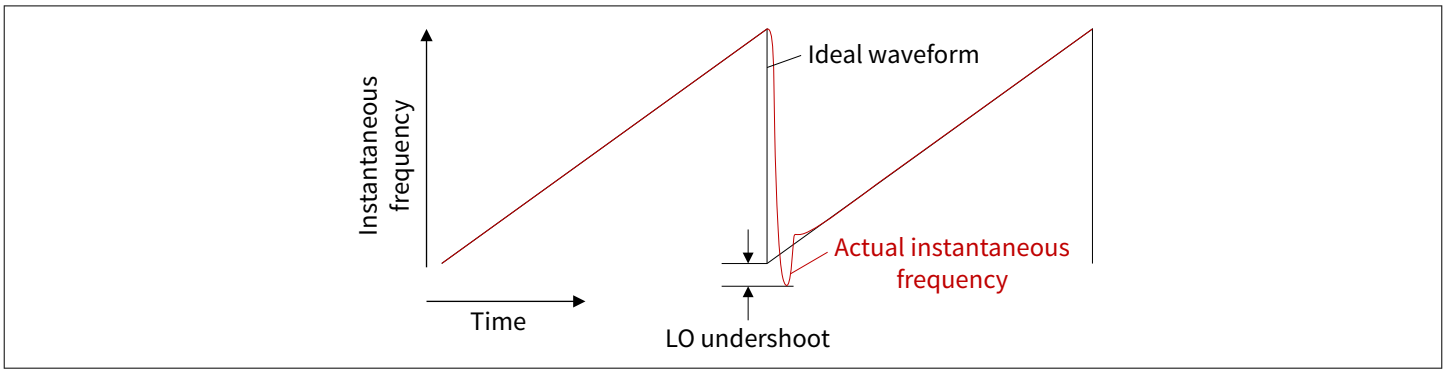


Figure 11 LO frequency undershoot after flyback

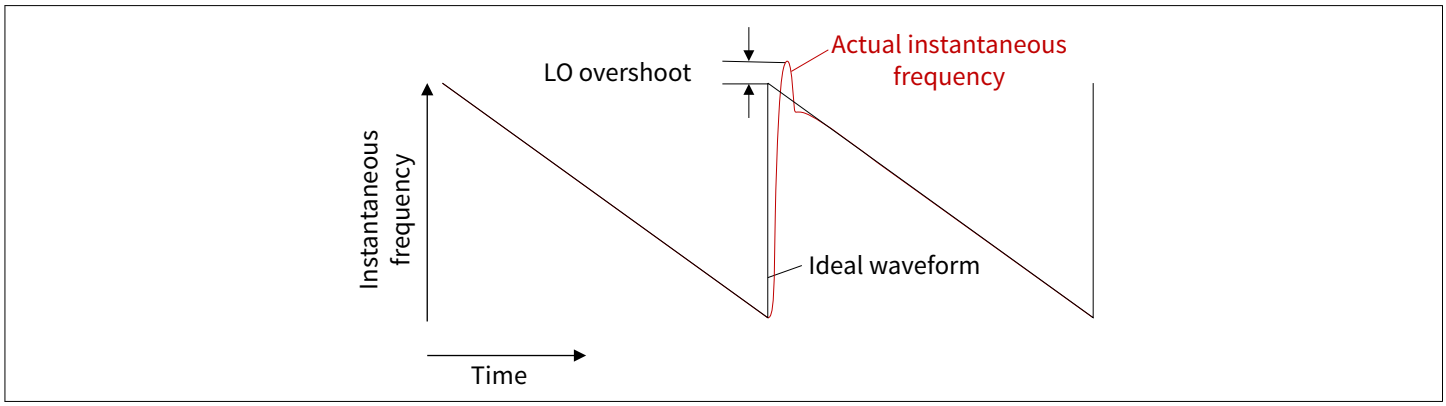


Figure 12 LO frequency overshoot after flyback

5.2.3 TX RF module

Table 26 TX RF module

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Output power reduction range	G_{adjust}	0	–	15	dB	The output power is configurable individually for each TX channel prior to radar sequence. Reduction range from max. TX output power setting.
Output power reduction accuracy for range 1	$\lvert G_{TX_acc_1} \rvert$	–	–	1.5	dB	Power reduction range 1: 0 dB to 6 dB TX output power reduction relative to max. TX output power setting. Constant junction temperature: ±10°C.
Output power reduction accuracy for range 2	$\lvert G_{TX_acc_2} \rvert$	–	–	2	dB	Power reduction range 2: 6 dB to 12 dB TX output power reduction relative to max. TX output power setting. Constant junction temperature: ±10°C.
Output power reduction accuracy for range 3	$\lvert G_{TX_acc_3} \rvert$	–	–	3	dB	Power reduction range 3: 12 dB to 15 dB TX output power reduction relative to max. TX output power setting. Constant junction temperature: ±10°C.
Output power at TX off	P_{TX_leak}	–	–	-30	dBm	VDD for TX PA is on, all TX are programmed to be off.
Residual output power at TX on with internal load active	$P_{TX_int_load}$	–	–	-30	dBm	TX switched to internal load, TX power level calibrated to 0 dB back off, For all TX phase configurations.

(table continues...)

Table 26 (continued) TX RF module

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Output power variation over frequency 76-77 GHz	$\lvert\Delta P_{f_76GHz}\rvert$	–	–	1.5	dB	Maximum range of variation over a frequency ramp. Valid for full output power reduction range.
Output power variation over frequency 77-81 GHz	$\lvert\Delta P_{f_79GHz}\rvert$	–	–	1.5	dB	Maximum range of variation over a frequency ramp. Valid for full output power reduction range.
Output power variation over temperature	$\lvert\Delta P_T\rvert$	–	–	1	dB	Closed-loop power control is activated. Power programming is constant.
TX output phase adjustment accuracy	$\lvert\varphi_{TX_acc}\rvert$	–	–	4	deg	–

Table 27 TX RF module configuration parameters

Configuration Parameter	Symbol	Nominal Range	Unit	Step width	Default	Note
Number of TX phase settings	$N_{TX_\varphi_i}$	up to 256	–	–	–	Number of equidistant phase points on the full unit circle. The first phase point is always 0 degree. Outside of sequencing fixed to 256.

5.2.4 Sequencer

Table 28 Sequencer

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Looping of ramp sets	N_{ramp_loop}	1	–	2048	–	Configurable number of executions of one ramp set.
Number of samples per ramp	$N_{samples_payload}$	0	–	2048	–	Allowed range of number of samples per ramp.

5.3 Receiver

5.3.1 General characteristics

Table 29 General characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Isolation between RX ports	$ISO_{RX/RX}$	40	–	–	dB	Applicable for an Infineon reference footprint.
Input return loss of RX ports	S_{11_RX}	–	–	-12	dB	Referred to RF reference plane. Only valid for RX channels.
Nominal RX conversion gain for ultra low noise operation mode	G_{nom_ULN}	41.0	44.5	48.0	dB FS/mW	Unit is given in dB (FS/mW) (FS .. ADC Full Scale). Valid from the RX RF reference plane to CSI-2 output. RX gain step G_{step}: +3 dB. f_{cutoff_AHP}: 300 kHz. IF tone frequency: 2.0 MHz. Valid for source impedance mismatch better -15 dB.
Nominal RX conversion gain for low noise operation mode	G_{nom_LN}	38	41.5	45	dB FS/mW	Unit is given in dB (FS/mW) (FS .. ADC Full Scale). Valid from the RX RF reference plane to CSI-2 output. RX gain step G_{step}: 0 dB. f_{cutoff_AHP}: 300 kHz. IF tone frequency: 2.0 MHz. Valid for source impedance mismatch better -15 dB.
RX gain steps	G_{step}	–	+3, 0, -3, -6, -12, -18	–	dB	f_{cutoff_AHP}: 300 kHz. IF tone frequency: 2.0 MHz.
RX gain step accuracy	$\lvert G_{step_acc} \rvert$	–	–	1.0	dB	–
Overall gain variation over RF frequency, range 1	$\lvert \Delta G_{f_RF1} \rvert$	–	–	1.5	dB	For a frequency bandwidth of 1 GHz between 76 and 77 GHz. RX gain step G_{step}: 0 dB. f_{cutoff_AHP}: 300 kHz. IF tone frequency: 2.0 MHz.
Overall gain variation over RF frequency, range 2	$\lvert \Delta G_{f_RF2} \rvert$	–	–	2.0	dB	For a frequency bandwidth of 4 GHz between 77 and 81 GHz. RX gain step G_{step}: 0 dB. f_{cutoff_AHP}: 300 kHz. IF tone frequency: 2.0 MHz.

(table continues...)

Table 29 (continued) General characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Overall gain variation over temperature	$\lvert\Delta G_T\rvert$	–	–	2.0	dB	RX gain step G_{step}: 0 dB. f_{cutoff_AHP}: 300 kHz. IF tone frequency: 2.0 MHz.
RX gain balance	$\lvert G_{RX_bal}\rvert$	–	0.3	3	dB	Systematic gain difference between RX channels *m* and *n* between RF test signal coupler and DFE output measured using built-in RX test signal circuitry. All RX channels are equally programmed. f_{cutoff_AHP}: 300 kHz. IF tone frequency: 2.0 MHz
Total RX SSB noise figure @ 1 MHz (TX OFF) for ultra low noise operation mode	$N_{SSB_NB_1M_1}$	–	9.9	12.9	dB	No blocker. All TX turned off. RX gain step G_{step}: +3 dB. For negative gain steps in dB (see RX gain steps), the total noise figure is allowed to increase by no more than the absolute value of gain step in dB. f_{cutoff_AHP}: 300 kHz.
Total RX SSB noise figure @ 10 MHz (TX OFF) for ultra low noise operation mode	$N_{SSB_NB_10M_1}$	–	9.7	12.7	dB	No blocker. All TX turned off. RX gain step G_{step}: +3 dB. For negative gain steps in dB (see RX gain steps), the total noise figure is allowed to increase by no more than the absolute value of gain step in dB. f_{cutoff_AHP}: 300 kHz.
Total RX SSB noise figure @ 1 MHz (TX OFF) for low noise operation mode	$N_{SSB_NB_1M_2}$	–	10.5	13.5	dB	No blocker. All TX turned off. RX gain step G_{step}: 0 dB. For negative gain steps in dB (see RX gain steps), the total noise figure is allowed to increase by no more than the absolute value of gain step in dB. f_{cutoff_AHP}: 300 kHz.
Total RX SSB noise figure @ 10 MHz (TX OFF) for low noise operation mode	$N_{SSB_NB_10M_2}$	–	10.2	13.2	dB	No blocker. All TX turned off. RX gain step G_{step}: 0 dB. For negative gain steps in dB (see RX gain steps), the total noise figure is allowed to increase by no more than the absolute value of gain step in dB. f_{cutoff_AHP}: 300 kHz.

(table continues...)

Table 29 (continued) General characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
RX SFDR single-tone, excl. harmonics, pass band, IF range 1	$SFDR_{single_IF1}$	80	–	–	dB	Valid for $f_{IF} \leq 11.25$ MHz. Single tone in passband applied, input level adjusted to obtain -2 dBFS at HSRIF. TX deactivated. RX gain step G_{step}: 0 dB. f_{cutoff_AHP}: 300 kHz. IF tone frequency 2.0 MHz. All harmonics are excluded. Spurious products masked by phase noise are excluded. External Power supply noise and spurious are excluded. At least 2^{18} IF samples at OSR of 50 MS/s are collected.
RX SFDR single-tone, excl. harmonics, pass band, IF range 2	$SFDR_{single_IF2}$	78	–	–	dB	Valid for $f_{IF} > 11.25$ MHz. Single tone in passband applied, input level adjusted to obtain -4 dBFS at HSRIF. TX deactivated. RX gain step G_{step}: 0 dB. f_{cutoff_AHP}: 300 kHz. IF tone frequency 20.0 MHz. All harmonics are excluded. Spurious products masked by phase noise are excluded. External Power supply noise and spurious are excluded. At least 2^{18} IF samples at OSR of 50 MS/s are collected.
RX input P1dB, stop band	P_{1dB_SB}	-2.5	–	–	dBm	RX gain step G_{step}: -18 dB. f_{cutoff_AHP}: 300 kHz. IF tone frequency: 300 kHz × 0.05.
RX input interception point 2nd order, stop band	IIP_{2_SB}	20	–	–	dBm	RX gain step G_{step}: -12 dB. f_{cutoff_AHP}: 1200 kHz. IF tone 1 frequency: 61 kHz. IF tone 2 frequency: 79 kHz. Power of input tones: -15 dBm.

(table continues...)

Table 29 (continued) General characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
RX input interception point 3rd order, stop band	IIP_{3_SB}	3	–	–	dBm	RX gain step G_{step}: -12 dB. f_{cutoff_AHP}: 1200 kHz. IF tone 1 frequency: 61 kHz. IF tone 2 frequency: 79 kHz. Power of input tones: -15 dBm.
RX channel to channel gain drift	$\lvert G_{drift_RX} \rvert$	–	–	1	dB	See definition of RX channel to channel gain drift for specification conditions.
RX channel to channel phase drift	$\lvert \varphi_{drift_RX} \rvert$	–	–	3.5	deg	See definition of RX channel to channel phase drift for specification conditions.
Passband ripple	$\lvert A_{ripple_PB} \rvert$	–	–	1.5	dB	Amplitude ripple at digital output within IF range. Max. to min. ratio of the whole RX chain between 2 MHz and min(22.5 MHz, 0.45 × OSR). f_{cutoff_AHP}: 300 kHz.
Stopband attenuation	ATT_{SB}	50	–	–	dB	Attenuation of the whole RX chain at 0.55 × OSR up to 3.45 × OSR (output sample rate). Referred to the level of a tone at 2 MHz IF. RX gain step G_{step}: 0 dB. f_{cutoff_AHP}: 300 kHz.
Output sample rate	R_{OSR}	–	–	50	MS/s	Effective output sample rate after decimation
RX settling time between ramps, 1	$t_{RX_set_1}$	–	–	1.4	µs	15% of RX output full scale referring to steady state response. TX power continuously on. Blocker at 8 kHz (chirped measurement, TX loop back). RX gain step G_{step}: 0 dB. f_{cutoff_AHP}: 300 kHz.
RX settling time between ramps, 2	$t_{RX_set_2}$	–	–	1.3	µs	15% of RX output full scale referring to steady state response. TX power continuously on. Blocker at 8 kHz (chirped measurement, TX loop back). RX gain step G_{step}: 0 dB. f_{cutoff_AHP}: 600 kHz.

(table continues...)

Table 29 (continued) General characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
RX settling time between ramps, 3	$t_{RX_set_3}$	–	–	1.2	µs	15% of RX output full scale referring to steady state response. TX power continuously on. Blocker at 8 kHz (chirped measurement, TX loop back). RX gain step G_{step}: 0 dB. f_{cutoff_AHP}: 1200 kHz.
RX settling time between ramps, 4	$t_{RX_set_4}$	–	–	1.2	µs	15% of RX output full scale referring to steady state response. TX power continuously on. Blocker at 8 kHz (chirped measurement, TX loop back). RX gain step G_{step}: 0 dB. f_{cutoff_AHP}: 2400 kHz.
RX settling time between ramps, 5	$t_{RX_set_5}$	–	–	0.9	µs	15% of RX output full scale referring to steady state response. TX power continuously on. Blocker at 8 kHz (chirped measurement, TX loop back). RX gain step G_{step}: 0 dB. f_{cutoff_AHP}: 4800 kHz.

Definition of RX channel to channel gain drift

Definition of RX channel to channel gain drift of two receive channels relative to each other over temperature, supply voltage, RF frequency and time. The receiver channel to channel gain drift complies to the following formula:

$$\left|\left[G_m(t_1, f_1, T_1, V_{DD1}, f_{IF}) - G_n(t_1, f_1, T_1, V_{DD1}, f_{IF})\right] - \left[G_m(t_2, f_2, T_2, V_{DD2}, f_{IF}) - G_n(t_2, f_2, T_2, V_{DD2}, f_{IF})\right]\right| \leq G_{drift_RX} \quad [\mathrm{dB}] \tag{2}$$

$\Delta f = |f_1 - f_2|$
$\Delta f = 0.5$ GHz
whereas:

- G ... overall receiver gain from RF reference plane to CSI-2 data stream in dBFS (i.e. 20·log(% of full-scale amplitude))
- $_{m,n}$ ... channel number of receive channel
- t_1, t_2 ... times difference as short as required to settle new conditions within a power cycle of max. 12 h
- f_1, f_2 ... RF frequency within range of operation
- T_1, T_2 ... temperature within range of operation
- V_{DD1}, V_{DD2} ... VDD1V0RX and VDD1V8 supply voltage within range of operation
- f_{IF} … IF frequency = 2.0 MHz, f_{cutoff_AHP}: 300 kHz
  - Note that f_{IF}, in contrast to all other parameters, the same IF frequency is used for conditions 1 (t_1, f_1, T_1, V_{DD1}) and conditions 2 (t_2, f_2, T_2, V_{DD2})

Assumption: Same input signal at all channels.
Premise: Same settings for all channels.

Definition of RX channel to channel phase drift

Definition of RX channel to channel phase drift of two receive channels relative to each other over temperature, supply voltage, RF frequency and time. The RX channel to channel phase drift complies to the following formula:

$$\left|\left[\varphi_m(t_1, f_1, T_1, V_{DD1}, f_{IF}) - \varphi_n(t_1, f_1, T_1, V_{DD1}, f_{IF})\right] - \left[\varphi_m(t_2, f_2, T_2, V_{DD2}, f_{IF}) - \varphi_n(t_2, f_2, T_2, V_{DD2}, f_{IF})\right]\right| \leq \varphi_{drift_RX} \quad [deg] \tag{3}$$

$\Delta f = |f_1 - f_2|$
$\Delta f = 0.5$ GHz
whereas:

- $\varphi_{m,n}$ ... relative signal phase in CSI-2 data stream
- $_{m,n}$ ... channel number of receive channel
- t_1, t_2 ... times difference as short as required to settle new conditions within a power cycle of max. 12 h
- f_1, f_2 ... RF frequency within range of operation
- $T_1 = 50°C$
- T_2 ... Temperature within range of operation
- V_{DD1}, V_{DD2} ... VDD1V0RX and VDD1V8 supply voltage within range of operation
- f_{IF} … IF frequency = 2.0 MHz, f_{cutoff_AHP}: 300 kHz
  - Note that f_{IF}, in contrast to all other parameters, same IF frequency is used for conditions 1 (t_1, f_1, T_1, V_{DD1}) and conditions 2 (t_2, f_2, T_2, V_{DD2})

Assumption: Same input signal at all channels.
Premise: Same settings for all channels, MMIC only (external structures not considered).

5.3.2 Analog frontend

Table 30 Analog frontend

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Analog 2-nd order HP filter configurable cut-off frequencies	f_{cutoff_AHP}	–	300, 600, 1200, 2400, 4800	–	kHz	-6 dB corner frequency HP2 configuration of 4800 kHz shall not be used for payload ramping phase.
Analog HP filter cut-off frequency accuracy	$\lvert\Delta f_{cutoff_AHP}\rvert$	–	–	10	%	Valid for the following frequencies of f_{cutoff_AHP}: • 300 kHz • 600 kHz • 1200 kHz • 2400 kHz

5.3.3 Digital frontend

The digital data interface supports the data rates and bit width shown in Table 31.

Table 31 Digital data interface

		IF data bit width		
		10-bit	12-bit	14-bit
Output sample rate [MS/s]	**Max. useable IF bandwidth [MHz]**	**Min. bitrate per lane [Mbit/s] No = not supported**		
50.00	22.500	1000.00	1200.00	
33.33	15.000	666.67	800.00	933.33
25.00	11.250	500.00	600.00	700.00
20.00	9.000	400.00	480.00	560.00
16.67	7.500	333.33	400.00	466.67
12.50	5.625	250.00	300.00	350.00
10.00	4.500	200.00	240.00	280.00
8.33	3.750	166.67	200.00	233.33
6.25	2.813	125.00	150.00	175.00
5.00	2.250	100.00	120.00	140.00

Interface configuration as follows:

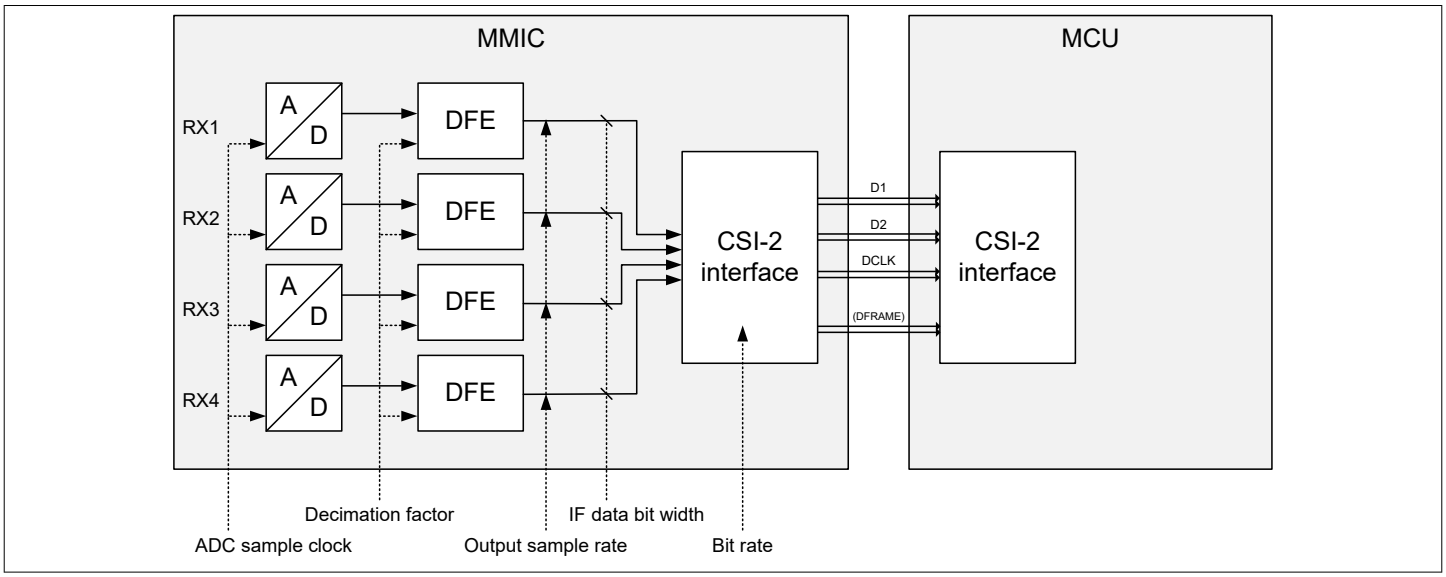


Figure 13 CSI-2 interface connection using 2 data lanes with data transmitted in one data packet (data from four channels interleaved)

5.3.4 CSI-2

The CSI-2 module is compatible with MIPI CSI-2 specification V2.0, based on the subset of the specification with a list of defined restrictions to focus on modes relevant for a radar application.

CSI-2 interface supports 2 data lanes.

D-PHY is based on the MIPI D-PHY v2.1 specification restricted to parameters valid for the transmitter side and with data rates < 1.2 Gbps.

Table 32 CSI-2

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
CSI-2 data rate	R_{CSI-2}	100	–	1200	Mbps	–

5.4 Control subsystem

The device provides a flexible firmware architecture to enable differentiation for the user. Firmware functions are separated between RAM and ROM in order to be able to optimize and customize use cases and to be flexible for late changes and optimizations. In MCU mode, after startup the device uses an SPI controller interface to communicate with an external non-volatile memory device. In this mode, customized firmware can be loaded from the external memory device to the device's instruction RAM which can be executed to control the device.

- ISO 26262-compliant developed CPU and development tools
- Safety mechanisms
  - Safety management unit
  - ECC for memories
  - Memory access protection
  - Bus protection
  - Register monitoring and protection
  - Watchdog for MMIC
  - Enhanced self-test mechanisms
- Enhanced and scalable compute performance with 32 bits

5.4.1 SPI

The SPI interface is designed to operate in mode 3 as a peripheral. Figure 14 illustrates the timings which are listed in this chapter. The voltage levels of the SPI digital signals are documented in Table 42.

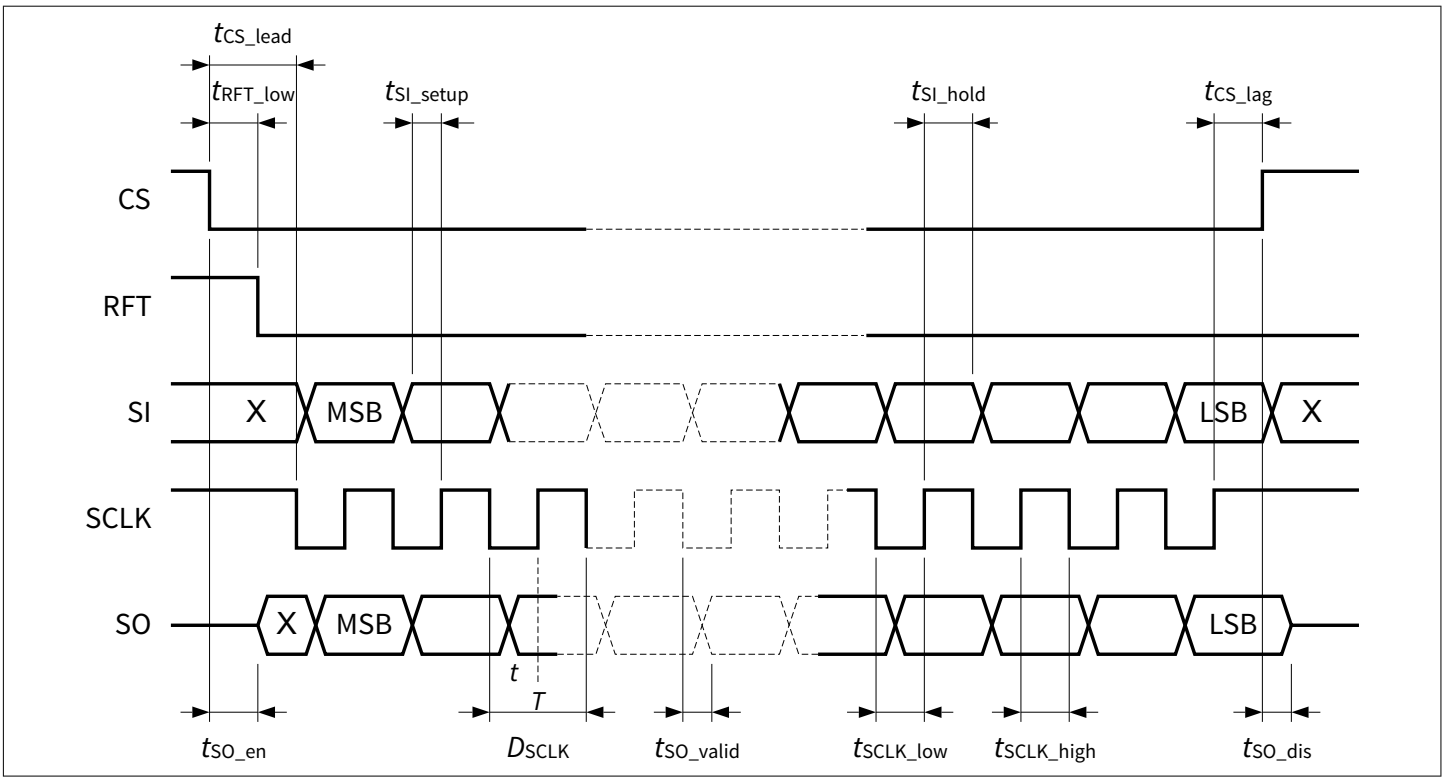


Figure 14 Definition of SPI timing parameters

Table 33 SPI timing parameters

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Serial clock frequency, duplex	f_{SCLK_dpl}	–	–	25	MHz	Theoretical upper limit, max. data rate limited by round-trip delay in application.
Serial clock frequency, receive	f_{SCLK_rec}	–	–	50	MHz	–
Serial clock duty cycle	D_{SCLK}	35	–	65	%	$D_{SCLK} = t / T$
Serial clock high time, duplex	$t_{SCLK_high_dpl}$	18	–	–	ns	–
Serial clock low time, duplex	$t_{SCLK_low_dpl}$	18	–	–	ns	–
Serial clock high time, receive	$t_{SCLK_high_rec}$	8	–	–	ns	–
Serial clock low time, receive	$t_{SCLK_low_rec}$	8	–	–	ns	–
Chip select lead time	t_{CS_lead}	7	–	–	ns	–
Chip select lag time	t_{CS_lag}	7	–	–	ns	–
Serial input setup time	t_{SI_setup}	3	–	–	ns	–
Serial input hold time	t_{SI_hold}	3	–	–	ns	–
Clock to serial output valid time	t_{SO_valid}	–	–	18	ns	$C_L \leq 25$ pF
Chip select low to ready for transfer low time	t_{RFT_low}	–	–	43	ns	$C_L \leq 25$ pF
Chip select low to serial output active time	t_{SO_en}	–	–	43	ns	$C_L \leq 25$ pF, $R_L = 1$ kΩ
Chip select high to serial output high impedance time	t_{SO_dis}	–	–	43	ns	$C_L \leq 25$ pF, $R_L = 1$ kΩ

5.4.2 CSPI

The figure below illustrates the timings which are listed in this chapter.

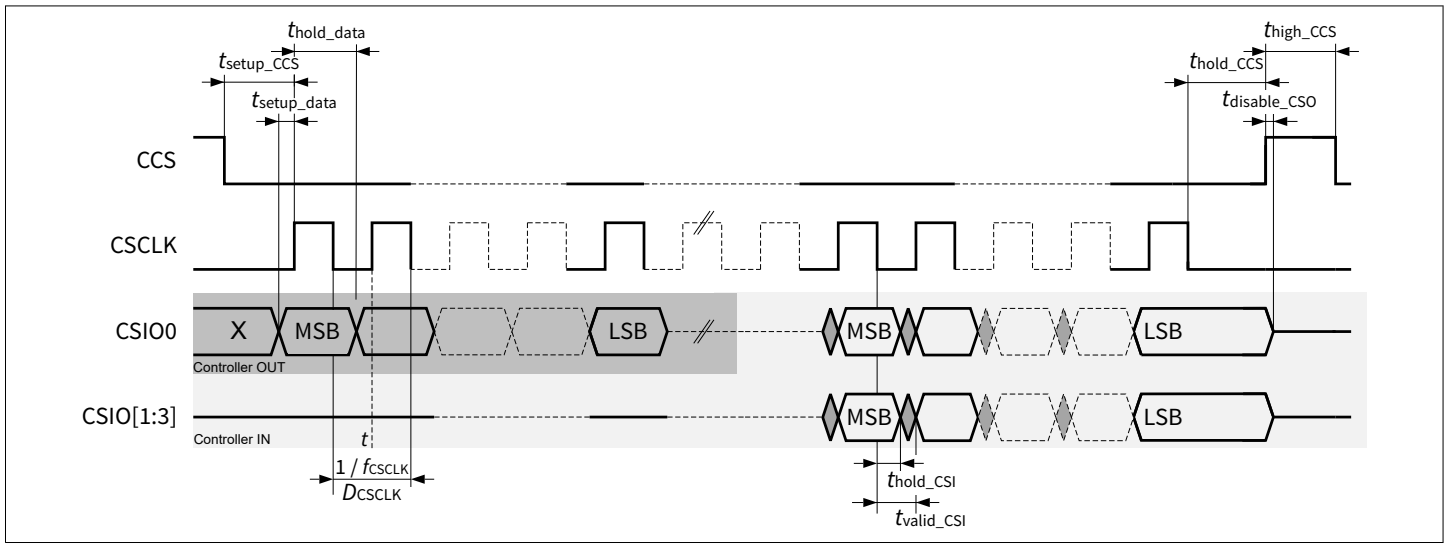


Figure 15 Definition of CSPI timing parameters (Mode 0)

Table 34 CSPI timing parameters

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Controller serial clock frequency	f_{CSCLK}	–	–	25	MHz	–
Controller serial clock duty cycle	D_{CSCLK}	45	–	55	%	$D_{CSCLK} = t / T$
Controller chip select high time	t_{high_CCS}	50	–	–	ns	–
Controller chip select active setup time	t_{setup_CCS}	5	–	–	ns	–
Controller chip select active hold time	t_{hold_CCS}	5	–	–	ns	–
Controller data set-up time	t_{setup_data}	5	–	–	ns	–
Controller data hold time	t_{hold_data}	5	–	–	ns	–
Controller clock low to output valid time	t_{valid_CSI}	–	–	10	ns	–

(table continues...)

Table 34 (continued) CSPI timing parameters

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Controller serial output hold time	t_{hold_CSI}	1	–	–	ns	–
Controller output disable time	$t_{disable_CSO}$	0	–	25	ns	–

5.4.3 I2C

The I2C module of the MMIC supports the following operating modes:

- Standard mode for speeds up to 100 kbits/s
- Fast mode for speeds up to 400 kbits/s
- Fast mode plus for speeds up to 1 Mbits/s

The figure below illustrates the timings which are listed in this chapter.

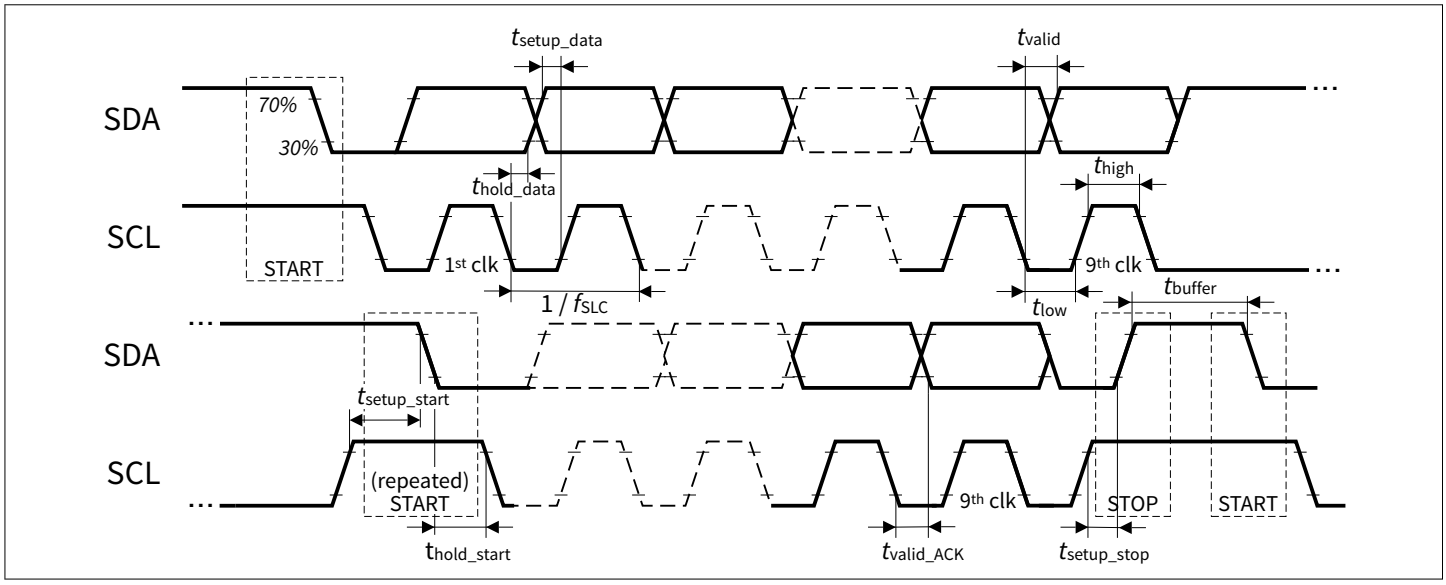


Figure 16 Definition of I2C timing parameter for standard and fast mode

Table 35 I2C timing parameters

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Standard-mode						
Serial clock frequency, standard-mode	f_{SCL_STD}	0	–	100	kHz	–

(table continues...)

Table 35 (continued) I2C timing parameters

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Hold time for (repeated) start condition, standard-mode	$t_{hold_start_STD}$	4	–	–	µs	1)
Low period of SCL clock, standard-mode	t_{low_STD}	4.7	–	–	µs	1)
High period of SCL clock, standard-mode	t_{high_STD}	4	–	–	µs	1)
Set-up time for repeated start condition, standard-mode	$t_{setup_start_STD}$	4.7	–	–	µs	1)
Data hold time, standard-mode	$t_{hold_data_STD}$	0	–	–	µs	1)
Data set-up time, standard-mode	$t_{setup_data_STD}$	250	–	–	ns	1)
Set-up time stop condition, standard-mode	$t_{setup_stop_STD}$	4	–	–	µs	1)
Bus free time between stop and start condition, standard-mode	t_{buffer_STD}	4.7	–	–	µs	1)
Data valid time, standard-mode	$t_{valid_data_STD}$	–	–	3.45	µs	1)
Data valid acknowledge time, standard-mode	$t_{valid_ACK_STD}$	–	–	3.45	µs	1)
Fast-mode						
Serial clock frequency, fast-mode	f_{SCL_F}	0	–	400	kHz	–
Hold time for (repeated) start condition, fast-mode	$t_{hold_start_F}$	0.6	–	–	µs	1)

(table continues...)

Table 35 (continued) I2C timing parameters

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Low period of SCL clock, fast-mode	t_{low_F}	1.3	–	–	µs	1)
High period of SCL clock, fast-mode	t_{high_F}	0.6	–	–	µs	1)
Set-up time for repeated start condition, fast-mode	$t_{setup_start_F}$	0.6	–	–	µs	1)
Data hold time, fast-mode	$t_{hold_data_F}$	0	–	–	µs	1)
Data set-up time, fast-mode	$t_{setup_data_F}$	100	–	–	ns	1)
Set-up time stop condition, fast-mode	$t_{setup_stop_F}$	0.6	–	–	µs	1)
Bus free time between stop and start condition, fast-mode	t_{buffer_F}	1.3	–	–	µs	1)
Data valid time, fast-mode	$t_{valid_data_F}$	–	–	0.9	µs	1)
Data valid acknowledge time, fast-mode	$t_{valid_ACK_F}$	–	–	0.9	µs	1)
Fast-mode plus						
Serial clock frequency, fast-mode plus	f_{SCL_FP}	0	–	1000	kHz	–
Hold time for (repeated) start condition, fast-mode plus	$t_{hold_start_FP}$	0.26	–	–	µs	1)
Low period of SCL clock, fast-mode plus	t_{low_FP}	0.5	–	–	µs	1)

(table continues...)

Table 35 (continued) I2C timing parameters

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
High period of SCL clock, fast-mode plus	t_{high_FP}	0.26	–	–	µs	1)
Set-up time for repeated start condition, fast-mode plus	$t_{setup_start_FP}$	0.26	–	–	µs	1)
Data hold time, fast-mode plus	$t_{hold_data_FP}$	0	–	–	µs	1)
Data set-up time, fast-mode plus	$t_{setup_data_FP}$	50	–	–	ns	1)
Set-up time stop condition, fast-mode plus	$t_{setup_stop_FP}$	0.26	–	–	µs	1)
Bus free time between stop and start condition, fast-mode plus	t_{buffer_FP}	0.5	–	–	µs	1)
Data valid time, fast-mode plus	$t_{valid_data_FP}$	–	–	0.45	µs	1)
Data valid acknowledge time, fast-mode plus	$t_{valid_ACK_FP}$	–	–	0.45	µs	1)

1) Valid for 2.2 kΩ pull-up resistors and a 25 pF load capacitance on each of the SCL and SDA lines.

5.5 Common infrastructure

Failure indication A "ordinary failure indication" - definition:

In case this indication is triggered, the MMIC reacts as follows:

- An error flag is set and provided for readout via a FW call, via SPI or CSI-2.

These indicators are persistent until cleared via a FW call.

Failure indication B "exceptional failure indication" - definition:

In case this indication is triggered, the MMIC reacts as follows (AND)

- The MMIC performs a soft reset.
- An error flag is set and provided for readout via a FW call (after soft reset is completed).

The indicator error flag is persistent until cleared via a FW call.

Note: Configuration interfaces (e.g., SPI and I2C) are interrupted due to soft reset.

Failure indication C "topmost failure indication" - definition:
In case this indication is triggered, the MMIC reacts as follows:

- the MMIC performs a hard reset.

Note: Configuration interfaces (e.g., SPI and I2C) are interrupted due to hard reset.

5.5.1 Reference clock generation

Table 36 Reference clock

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Oscillation frequency	f_{osci}	49.995	50	50.005	MHz	Subsequent parameters only valid when the resulting fundamental tone frequency is in this range.
Oscillator frequency tolerance	Δf_{osci}	-30	–	30	ppm	Valid for crystal $C_1 \leq 3.68$ fF and $ESR_{max} \leq 30\ \Omega$ or $C_1 \leq 2.553$ fF and $ESR_{max} \leq 50\ \Omega$ and $C_L = 8$ pF (with external capacitances (components and board) better than ±3%, $C_{L_XIN\text{-}XOUT\text{-}ext} \leq 0.5$ pF and $C_{L_XIN\text{-}ext}$ and $C_{L_XOUT\text{-}ext}$ according to definition of $C_{L_XOUT\text{-}ext}$ and $C_{L_XIN\text{-}ext}$).
Oscillator negative resistance	R_{neg}	–	–	-300	Ohm	Valid for $C_L = 8$ pF (with external capacitances (components and board) better than ±3%, $C_{L_XIN\text{-}XOUT\text{-}ext} \leq 0.5$ pF and $C_{L_XIN\text{-}ext}$ and $C_{L_XOUT\text{-}ext}$ according to definition of $C_{L_XOUT\text{-}ext}$ and $C_{L_XIN\text{-}ext}$).
Oscillator drive level 1	$P_{DL_30\Omega}$	–	–	250	µW	At crystal Equivalent Series Resistance (ESR) ≤ 30 Ω. Valid for $C_L = 8$ pF (with external capacitances (components and board) better than ±3%, $C_{L_XIN\text{-}XOUT\text{-}ext} \leq 0.5$ pF and $C_{L_XIN\text{-}ext}$ and $C_{L_XOUT\text{-}ext}$ according to definition of $C_{L_XOUT\text{-}ext}$ and $C_{L_XIN\text{-}ext}$).
Oscillator drive level 2	$P_{DL_50\Omega}$	–	–	300	µW	At max. crystal Equivalent Series Resistance (ESR) 30 Ω < ESR ≤ 50 Ω. Valid for $C_L = 8$ pF (with external capacitances (components and board) better than ±3%, $C_{L_XIN\text{-}XOUT\text{-}ext} \leq 0.5$ pF and $C_{L_XIN\text{-}ext}$ and $C_{L_XOUT\text{-}ext}$ according to definition of $C_{L_XOUT\text{-}ext}$ and $C_{L_XIN\text{-}ext}$).
System clock settling time after trigger event	$t_{sys_CLK_set}$	–	–	20	µs	Valid in Sequencing state, from end of wait opcode with trigger source CLKIN selected until data acquisition is allowed again.

(table continues...)

Table 36 (continued) Reference clock

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Reference clock activation and switch-over time	t_{start_clock}	–	–	3.5	ms	Time it takes the device from calling Set_MMIC_Clock() FW function (CS changes from logic low to high) until completion of crystal oscillator start-up and internal clock switch-over indicated by the RFT changing back to logic high. Valid using NDK NX2016SA, Spec.-Nr.: EXS00A-CS09080, C_L = 8 pF (with external capacitances (components and board) better than ±3%, $C_{L_XIN\text{-}XOUT\text{-}ext} \leq$ 0.5 pF and $C_{L_XIN\text{-}ext}$ and $C_{L_XOUT\text{-}ext}$ according to definition of $C_{L_XIN\text{-}ext}$ and $C_{L_XOUT\text{-}ext}$).

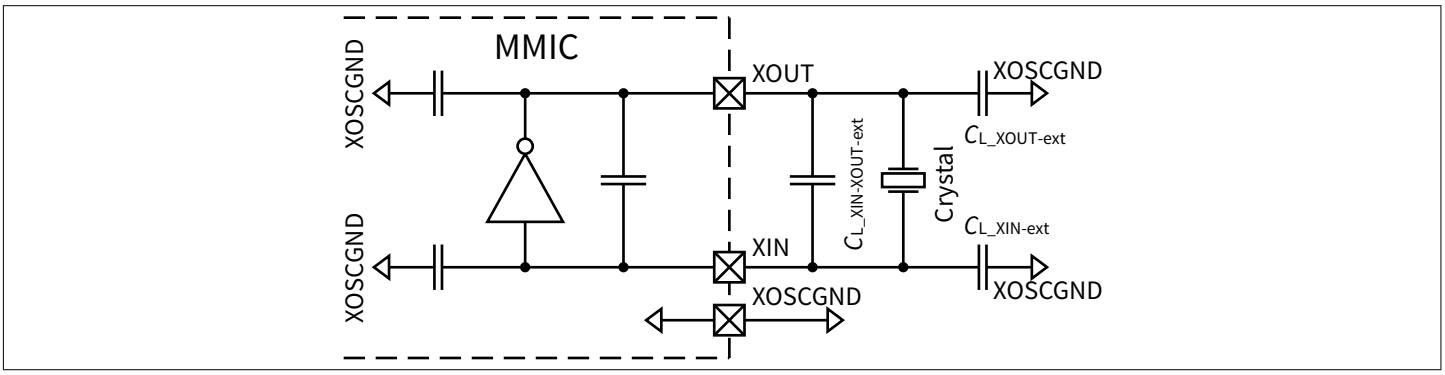


Figure 17 XTAL circuitry

$$C_{L_XIN-ext}\ [pF] = (C_{L_nom.}\ [pF] - 0.42\ [pF] - C_{L_XIN-XOUT-ext}\ [pF]) \times 2 - 4.74\ [pF] \quad (4)$$

$$C_{L_XOUT-ext}\ [pF] = (C_{L_nom.}\ [pF] - 0.42\ [pF] - C_{L_XIN-XOUT-ext}\ [pF]) \times 2 - 1.86\ [pF] \quad (5)$$

whereas:
$C_{L_XIN\text{-}ext}$ and $C_{L_XOUT\text{-}ext}$: total capacitance of component and PCB structures,
$C_{L_nom.}$: nominal load capacitance for which the used crystal was designed,
$C_{L_XIN\text{-}XOUT\text{-}ext}$: differential parasitic capacitance of PCB structures.

***Note**: Preliminary values and subject to change.*

In addition to using the internal reference clock, an external clock fulfilling the specification given in the table below is applicable to the XIN pin.

Table 37 External reference source

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
XIN frequency	f_{XIN}	49.995	50	50.005	MHz	–

(table continues...)

Table 37 (continued) External reference source

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
XIN voltage swing	V_{XIN_swing}	800	–	1100	mV	Peak to peak value, sine or square wave supported, external AC coupling required.
XIN duty cycle	D_{XIN}	45	50	55	%	At mid level of input AC signal
XIN phase noise 10 kHz	$N_{\varphi_XIN_10k}$	–	–	-143	dBc/Hz	Between the defined frequency points ($N_{\varphi_XIN_10k}$ and $N_{\varphi_XIN_100k}$), the noise mask is interpolated linearly on a log-log scale.
XIN phase noise 100 kHz	$N_{\varphi_XIN_100k}$	–	–	-152	dBc/Hz	Between the defined frequency points ($N_{\varphi_XIN_100k}$ and $N_{\varphi_XIN_1M}$), the noise mask is interpolated linearly on a log-log scale.
XIN phase noise 1 MHz	$N_{\varphi_XIN_1M}$	–	–	-154	dBc/Hz	Valid also for frequencies above 1 MHz.
XIN phase spur level 10 kHz to 1 MHz	$S_{\varphi_spur_XIN_10k}$	–	–	-94	dBc	Phase spur level evaluated by threshold crossing with respect to signal mean value.
XIN phase spur level 1 MHz to 10 MHz	$S_{\varphi_spur_XIN_1M}$	–	–	-84	dBc	Phase spur level evaluated by threshold crossing with respect to signal mean value.
XIN phase spur level 10 MHz to 25 MHz	$S_{\varphi_spur_XIN_10M}$	–	–	-64	dBc	Phase spur level evaluated by threshold crossing with respect to signal mean value.
XIN pin capacitance	C_{XIN}	–	–	15	pF	–

Table 38 CLKPHY clock output

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
CLKPHY output duty cycle 25 MHz	D_{CLKPHY}	45	–	55	%	50% to 50% of swing level. 25 MHz frequency setting.
CLKPHY output duty cycle 50 MHz	D_{CLKPHY}	43	–	57	%	50% to 50% of swing level. 50 MHz setting.
CLKPHY jitter 1 kHz to 5 MHz	$t_{CLKPHY_jitter_1k}$	–	–	1	ps	Integrated from 1 kHz - 5 MHz frequency offset. RMS value.
CLKPHY jitter 12 kHz to 25 MHz	$t_{CLKPHY_jitter_12k}$	–	–	1	ps	Integrated from 12 kHz - 25 MHz frequency offset. RMS value.
CLKPHY rise/fall time	$t_{rise/fall_CLKPHY}$	–	–	6	ns	10 - 90%

(table continues...)

Table 38 (continued) CLKPHY clock output

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
CLKPHY DC high voltage	V_{CLKPHY_high}	1.4	–	–	V	–
CLKPHY DC low voltage	V_{CLKPHY_low}	–	–	0.1	V	–
CLKPHY capacitive load	C_{load_CLKPHY}	–	–	15	pF	Maximum load capacitance connected to CLKPHY pin.
CLKPHY resistive load	R_{load_CLKPHY}	50	–	–	kΩ	Minimum load resistance connected to CLKPHY pin towards ground.
CLKPHY phase noise 1 kHz at 25 MHz setting	$N_{\varphi_CLKPHY_1k_25M}$	–	–	-118	dBc/Hz	At 25 MHz output frequency setting. Between the defined frequency points ($N_{\varphi_CLKPHY_1k}$ and $N_{\varphi_CLKPHY_10k}$), the noise mask is interpolated linearly on a log-log scale.
CLKPHY phase noise 10 kHz at 25 MHz setting	$N_{\varphi_CLKPHY_10k_25M}$	–	–	-128	dBc/Hz	At 25 MHz output frequency setting. Between the defined frequency points ($N_{\varphi_CLKPHY_10k}$ and $N_{\varphi_CLKPHY_100k}$), the noise mask is interpolated linearly on a log-log scale.
CLKPHY phase noise 100 kHz at 25 MHz setting	$N_{\varphi_CLKPHY_100k_25M}$	–	–	-143	dBc/Hz	At 25 MHz output frequency setting. Between the defined frequency points ($N_{\varphi_CLKPHY_100k}$ and $N_{\varphi_CLKPHY_1M}$), the noise mask is interpolated linearly on a log-log scale.
CLKPHY phase noise 1 MHz at 25 MHz setting	$N_{\varphi_CLKPHY_1M_25M}$	–	–	-153	dBc/Hz	At 25 MHz output frequency setting. Valid also for frequencies above 1 MHz.

Table 39 CLKMCU clock output

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
CLKMCU output frequency	f_{CLKMCU}	–	25, 40, 50	–	MHz	Users are advised to evaluate the impact of using 40 MHz setting on overall system performance before applying such configurations.
CLKMCU output duty cycle 25 and 50 MHz	$D_{CLKMCU_25_50}$	40	–	60	%	50% to 50% of swing level. Load: C_L=25 pF. Valid for 25 MHz and 50 MHz settings.
CLKMCU output duty cycle 40 MHz	D_{CLKMCU_40}	30	–	70	%	50% to 50% of swing level. Load: C_L=25 pF. Valid for 40 MHz setting.

(table continues...)

Table 39 (continued) CLKMCU clock output

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
CLKMCU output jitter	$t_{CLKMCU_jitter_10k}$	–	–	25	ps	Integrated from 10 kHz - half of selected clock frequency offset. RMS value. Load: C_L=25 pF.

Table 40 50 MHz clock and trigger input

The parameters of CLKIN refer to CLKIN_REF as ground. Noise, frequency, and duty cycle parameters are only valid in the absence of trigger events.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
CLKIN frequency	f_{CLKIN}	49.995	50	50.005	MHz	–
CLKIN voltage range	V_{CLKIN_range}	-0.1	–	1	V	–
CLKIN duty cycle	D_{CLKIN}	38	–	62	%	At mid level of input signal
CLKIN leakage current	I_{CLKIN_leak}	-200	–	200	µA	Valid if input is enabled and on-chip termination is deactivated. Valid for voltage at pin within range of V_{CLKIN_range}.

5.5.2 Temperature sensor

Table 41 Temperature sensor

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Temperature sensor accuracy	T_{acc}	-3	–	3	°C	-40°C < T_J ≤ 138°C
Temperature monitoring reaction time	t_{T_mon}	–	–	2.1	ms	Valid using crystal oscillator or external active clock source as system clock.

The device performs failure indication B when a temperature reading of equal or more than 138°C occurs.

The device performs failure indication A when a temperature reading exceeds a threshold ("thermal warning threshold range"). The value of this threshold is configurable via a FW call.

The device performs event indication M when a temperature reading of T_J of less than -40°C occurs.

5.5.3 Digital port control

Table 42 Digital port control

The parameters listed in this table are valid for all 1.8 V digital input / output pins (DMUX[1-3], CS, SCLK, SI, SO, RFT, RESET_N, CLKMCU, OK).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Pin capacitance	C_{DIN}	–	–	6	pF	–
Pin leakage current	I_{DIN_leak}	-3.5	–	3.5	µA	$0 \le V_{DIN} \le V_{DD1V8}$
Input DC high voltage	V_{in_high}	$0.7 \cdot V_{DD1V8}$	–	–	V	–
Input DC low voltage	V_{in_low}	–	–	$0.3 \cdot V_{DD1V8}$	V	–
Input hysteresis	V_{in_hys}	$0.06 \cdot V_{DD1V8}$	–	–	V	–
Pull-up DC current at input high voltage	$\lvert I_{PU_high} \rvert$	30	–	–	µA	V_{in_high}
Pull-up DC current at input low voltage	$\lvert I_{PU_low} \rvert$	–	–	130	µA	V_{in_low}
Pull-down DC current at input low voltage	$\lvert I_{PD_low} \rvert$	30	–	–	µA	V_{in_low}
Pull-down DC current at input high voltage	$\lvert I_{PD_high} \rvert$	–	–	130	µA	V_{in_high}
Output DC high voltage	V_{out_high}	V_{DD1V8} - 0.65	V_{DD1V8} - 0.4	V_{DD1V8} - 0.25	V	I_{out_high} = 1.1 mA (weakest) I_{out_high} = 2 mA (weak) I_{out_high} = 5.77 mA (strong) I_{out_high} = 8 mA (strongest)
Output DC low voltage	V_{out_low}	0.25	0.4	0.65	V	I_{out_low} = 1.1 mA (weakest) I_{out_low} = 2 mA (weak) I_{out_low} = 5.77 mA (strong) I_{out_low} = 8 mA (strongest)
Rise/fall time, weakest drive strength	$t_{rise/fall,11}$	15	–	68.5	ns	C_L = 25 pF, drive strength setting: weakest, evaluated from $0.1 \cdot V_{DD1V8}$ to $0.9 \cdot V_{DD1V8}$
Rise/fall time, weak drive strength	$t_{rise/fall,10}$	8	–	39.3	ns	C_L = 25 pF, drive strength setting: weak, evaluated from $0.1 \cdot V_{DD1V8}$ to $0.9 \cdot V_{DD1V8}$

(table continues...)

Table 42 (continued) Digital port control

The parameters listed in this table are valid for all 1.8 V digital input / output pins (DMUX[1-3], CS, SCLK, SI, SO, RFT, RESET_N, CLKMCU, OK).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Rise/fall time, strong drive strength	$t_{rise/fall,01}$	2	–	15	ns	C_L = 25 pF, drive strength setting: strong, evaluated from 0.1 · V_{DD1V8} to 0.9 · V_{DD1V8}
Rise/fall time, strongest drive strength	$t_{rise/fall,00}$	0.8	–	11.6	ns	C_L = 25 pF, drive strength setting: strongest, evaluated from 0.1 · V_{DD1V8} to 0.9 · V_{DD1V8}
Maximum allowed output current for DIO	I_{out_max}	–	–	10	mA	Valid for static loads. Dynamic currents (e.g., for charging of capacitance of connected lines) are not limited by this parameter.
Maximum allowed output current for all DIOs	$\Sigma\lvert I_{out_max}\rvert$	–	–	24	mA	This value is the sum of absolute currents, i.e. sink and source currents add up and do not cancel.
Input functional voltage range	V_{DIN_FR}	-0.1	–	1.98	V	Absolute maximum ratings and overload conditions apply additionally.

5.5.4 Power supply monitoring

Table 43 Power supply monitoring

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VDD1V8 undervoltage 1 detection threshold	V_{DD1V8_UV1}	1.62	–	1.71	V	DC voltage on VDD1V8 domain, failure indication A triggered under this threshold.
VDD0V9D undervoltage 2 detection threshold	V_{DD0V9D_UV2}	0.81	–	0.855	V	DC voltage on VDD0V9D domain, failure indication C triggered under this threshold.
VDD1V0RX undervoltage 1 detection threshold	$V_{DD1V0RX_UV1}$	0.9	–	0.95	V	DC voltage on VDD1V0RX domain, failure indication A triggered under this threshold.
VDD1V0TX undervoltage 1 detection threshold	$V_{DD1V0TX_UV1}$	0.9	–	0.95	V	DC voltage on VDD1V0TX domain, failure indication A triggered under this threshold.
DC supply monitoring reaction time	t_{supply_mon}	–	–	5	µs	–

5.5.5 Reset

Table 44 Reset

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Reset duration minimum time	t_{reset_dur}	2	–	–	µs	Minimum duration the reset signal has to be asserted to initiate a hard reset
Reset debouncing	$t_{reset_debounce}$	–	–	0.5	µs	Pulses shorter than this do not result in a hard reset

6 Terminology

A	
AAF	Anti-aliasing Filter
ACC	Adaptive Cruise Control
ADC	Analog to Digital Converter
AEB	Automatic Emergency Braking
AEC	Automotive Electronics Council
AHP	Analog High Pass Filter
B	
BBF	Baseband Filter
C	
CDM	Charged Device Model
CPU	Central Processing Unit
CSI-2	Camera Serial Interface 2
D	
DC	Direct Current
DFE	Digital Frontend
DI	Digital Input
DIO	Digital Input / Output
DIR	Distributed Imaging Radar
DMUX	Digital Multiplexer
DPLL	Digital Phase Locked Loop
E	
ECC	Error Correcting Code
ESD	Electrostatic Discharge
F	
FCBGA	Flip Chip Ball Grid Array
FQM	Frequency Multiplier
FS	Full Scale
G	
GND	Ground
H	
HBM	Human Body Model
HP	High Pass
HSI	High Speed Interface
HSRIF	High Speed Radar Interface

I	
IF	Intermediate Frequency
J	
K	
L	
LCA	Lane-Change Assistant
LO	Local Oscillator
LP	Low Pass
LSB	Least Significant Bit
M	
MMIC	Monolithic Microwave Integrated Circuit
MSB	Most Significant Bit
N	
O	
OSR	Output Sample Rate
P	
PCB	Printed Circuit Board
PLL	Phase Locked Loop
PSUP	Power Supply
PWR	Power
Q	
R	
RAM	Random Access Memory
RES	Reserved
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances Directive
ROM	Read-Only Memory
RX	Receiver/Receive
S	
SFDR	Spurious Free Dynamic Range
SMU	Safety Management Unit
SPI	Serial Peripheral Interface
SSB	Single Sideband
T	
TJA	Traffic Jam Assist/Pilot
TX	Transmitter/Transmit

U	
UV	Undervoltage
V	
VCO	Voltage Controlled Oscillator
VDD	Positive power supply
VSS	Negative power supply
W	
X	
Y	
Z	

7 Revision history

Table 45 Revision history

Revision number	Date of release	Description of changes
Rev. 0.10	2026-09-19	Initial release

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