

BGT24LTR11N16

Silicon germanium 24GHz radar transceiver MMIC

Features

- 24 GHz transceiver MMIC
- Fully integrated low phase noise VCO
- Built-in temperature compensation circuit for VCO stabilization
- Homodyne quadrature receiver
- Frequency divider
- Low-power consumption
- Fully ESD protected device
- Single ended RF and IF terminals
- 200 GHz bipolar SiGe:C technology B7HF200
- Single supply voltage 3.3 V
- TSNP-16-9 plastic package



Potential applications

- Smart home appliances
- Drone collision avoidance
- Traffic monitoring
- Security applications

Description

BGT24LTR11 is a Silicon germanium transceiver MMIC operating from 24.0 GHz up to 24.25 GHz. It is based on a 24 GHz fundamental voltage controlled oscillator (VCO). A built in voltage source delivers a VCO tuning voltage (V_PTAT) which is proportional to absolute temperature. When connected to the VCO tuning pin (V_TUNE) it compensates for the inherent frequency drift of the VCO over temperature thus stabilizing the VCO within the ISM band eliminating the need for a PLL/Microcontroller. An integrated 1:16 frequency divider also allows for external phase lock loop VCO frequency stabilization. The receiver section uses a low noise amplifier (LNA) in front of a quadrature homodyne down conversion mixer in order to provide excellent receiver sensitivity. Derived from the internal VCO signal, a RC polyphase filter (PPF) generates quadrature LO signals for the quadrature mixer. The I/Q IF outputs are available through a single ended terminal respectively. The device is manufactured in a 0.18 μm SiGe:C technology offering a cutoff frequency of 200 GHz. It is packaged in a 16 pin leadless RoHs compliant TSNP package.

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1 Introduction

The BGT24LTR11 is a Silicon Germanium transceiver MMIC operating from 24.0 GHz up to 24.25 GHz. It is based on a 24 GHz fundamental voltage controlled oscillator (VCO). A built in voltage source delivers a VCO tuning voltage (V_PTAT) which is proportional to absolute temperature. When connected to the VCO tuning pin (V_TUNE) it compensates for the inherent frequency drift of the VCO over temperature thus stabilizing the VCO within the ISM band eliminating the need for a PLL/Microcontroller. An integrated 1:16 frequency divider also allows for external phase lock loop VCO frequency stabilization.

Product name	Package	Chip	Marking
BGT24LTR11N16	TSNP-16-9	T1811	LTR11

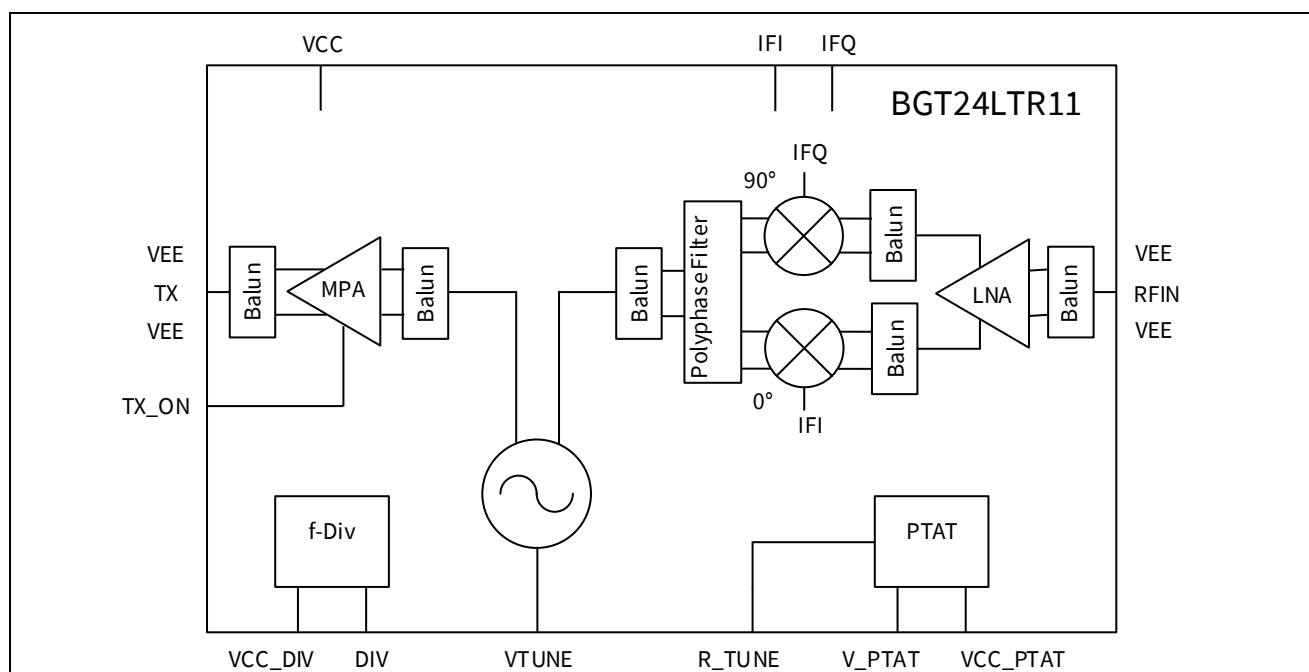


Figure 1 Block diagram

2 Electrical characteristics

2.1 Absolute maximum ratings

Table 1 Absolute maximum ratings: $T_A = -40^{\circ}\text{C}$ to 85°C ; all voltages with respect to ground

Parameter	Symbol	Value			Unit	Test condition
		Min.	Typ.	Max.		
Supply voltage	V_{CC}	-0.3	–	3.6	V	–
Supply voltage divider	V_{CC_DIV}	-0.3	–	3.6	V	–
Supply voltage PTAT voltage source	V_{CC_PTAT}	-0.3	–	3.6	V	–
DC voltage at RF pins	V_{DC_RF}	–	–	0	V	MMIC provides short circuit to GND for RF_IN and TX_OUT
Voltage applied to none-RF I/O pins	$V_{DC_I/O}$	-0.3	–	$V_{CC} + 0.3$	V	–
Total power dissipation	P	–	–	300	mW	–
Ambient temperature range	T_A	-40	–	85	$^{\circ}\text{C}$	–
Storage temperature range	T_{STG}	-50	–	125	$^{\circ}\text{C}$	–

Note: Stresses exceeding the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

2.2 ESD integrity

Table 2 ESD integrity

Parameter	Symbol	Value			Unit	Test condition
		Min.	Typ.	Max.		
ESD robustness HBM ¹	$V_{ESD-HBM}$	-1	–	1	kV	–
ESD robustness CDM ²	$V_{ESD-CDM}$	-500	–	500	V	–

Note: This result is subject to a lot of variations within the manufacturing process as specified by Infineon and the changes in the specific test setup.

2.3 Power supply

Table 3 Power supply characteristics: $T_A = -40^{\circ}\text{C}$ to 85°C

¹ According to ANSI/ESDA/JEDEC JS-001 (R = 1.5k Ω , C = 100pF) for Electrostatic Discharge Sensitivity Testing, Human Body Model (HBM)-Component Level

² According to JEDEC JESD22-C101 Field-Induced Charged Device Model (CDM), Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

Electrical characteristics

Parameter	Symbol	Value			Unit	Test condition
		Min	Typ	Max		
Supply voltage	V_{CC}	3.2	3.3	3.4	V	–
Supply current	I_{CC}	–	45	55	mA	–
Duty cycle	–	1:1000	–	–	–	–
Pulse duration	t_P	1	–	–	μs	–

2.4 Transmitter

Table 4 TX section electrical characteristics: $T_A = -40^\circ C$ to $85^\circ C$; all parameters specified including a TX port matching structure and package footprint provided by UG133248

Parameter	Symbol	Value			Unit	Test condition
		Min.	Typ.	Max.		
VCO frequency range	f_{VCO}	24.050	–	24.250	GHz	V_{PTAT} connected to VTUNE; 16 k Ω resistor connected from R_TUNE to GND
VCO phase noise	P_N	–	–	-55 -80	dBc/Hz	@10 kHz offset @100 kHz offset
VCO AM noise	P_{AM}	–	–	-135	dBc/Hz	@100 kHz offset
Tuning voltage to cover VCO frequency range	V_{TUNE}	0.7	–	2.5	V	–
VCO tuning sensitivity within VCO frequency range	–	–	720	2000	MHz/V	–
Second harmonic suppression	–	25	–	–	dBc	–
Non-harmonic suppression	–	62	–	–	dBc	$f > 10$ GHz; $D_{DIV}=16$
Non-harmonic suppression	–	45	–	–	dBc	$f > 10$ GHz; $D_{DIV}=16$
TX output power	P_{TX}	2	6	10	dBm	–
TX load impedance	Z_{TXOUT}	–	50	–	Ω	Including TX port matching structure according to UG133248
TX_ON low level input voltage (TX=OFF)	$V_{TX_ON_low}$	–	–	0.8	V	TX_ON pin is chip internally pulled up to V_{CC} via typ 98 k Ω resistor
TX_ON high level input voltage (TX=ON)	$V_{TX_ON_high}$	2	–	–	V	TX_ON pin is chip internally pulled up to V_{CC} via typ 98 k Ω resistor
TX_ON input voltage hysteresis	$V_{TX_ON_hys}$	50	–	–	mV	–
TX_ON input current	I_{TX_ON}	-100	–	100	μA	–

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Electrical characteristics

Parameter	Symbol	Value			Unit	Test condition
		Min.	Typ.	Max.		
TX_ON switching time	t_{TX_ON}	–	–	2	ns	–
Power up TX setting time	$t_{TX_Power_up}$	–	–	100	ns	Defines the time TX section requires to settle after V_{CC} supply voltage is within specified range

2.5 Receiver

Table 5 RX characteristics: $T_A = -40^{\circ}\text{C}$ to 85°C ; all parameters specified including RX port matching structure and package footprint provided by UG133248

Parameter	Symbol	Value			Unit	Test condition
		Min.	Typ.	Max.		
RX frequency range	f_{RX}	24	–	24.25	GHz	–
RX input impedance	Z_{RXIN}	–	50	–	Ω	Including RX port matching structure according to UG133248
Voltage conversion gain	G_C	15.5	20	26.5	dB	–
SSB noise figure	NF_{SSB}	–	10	18	dB	Single sideband at $f_{IF} = 100\text{ kHz}$
Input compression point	IP_{1dB}	-28	–	–	dBm	–
Quadrature phase imbalance	ε_P	0	–	24	Deg	–
Quadrature amplitude imbalance	ε_A	-1	–	1	dB	–
IF output impedance	Z_{IF}	–	–	1	k Ω	Single ended

2.6 Frequency divider

Table 6 Frequency divider characteristics: $T_A = -40^{\circ}\text{C}$ to 85°C

Parameter	Symbol	Value			Unit	Test condition
		Min.	Typ.	Max.		
Prescaler division ratio	D_{DIV}	16	–	8192	–	16 if $V_{\text{CC_PTAT}} = 0\text{ V}$, 8192 if $V_{\text{CC_PTAT}} = 3.3\text{ V}$
Prescaler output voltage for division ratio 16	V_{DIV16}	60	120	350	mV	Peak to Peak voltage when DIV_OUT is terminated with $50\ \Omega$ and $D_{\text{DIV}} = 16$
Prescaler output “high” voltage for division ratio 8192	V_{DIV8192H}	2.4	–	–	V	DIV_OUT is loaded with $1\ \text{M}\Omega$, $13\ \text{pF}$
Prescaler output “low” voltage for division ratio 8192	V_{DIV8192L}	–	–	0.8	V	DIV_OUT is loaded with $1\ \text{M}\Omega$, $13\ \text{pF}$
Prescaler supply voltage	$V_{\text{CC_DIV}}$	3.2	3.3	3.4	V	–
Prescaler supply current	$I_{\text{CC_DIV}}$	13	19	25	mA	–

2.7 Proportional to absolute temperature (PTAT) voltage source

Table 7 PTAT voltage source characteristics: $T_A = -40^{\circ}\text{C}$ to 85°C

Parameter	Symbol	Value			Unit	Test condition
		Min.	Typ.	Max.		
Supply voltage	$V_{\text{CC_PAT}}$	3.2	3.3	3.4	V	–
Supply current	$I_{\text{CC_PAT}}$	–	1.5	2.5	mA	–
Output voltage	$V_{\text{OUT_PTAT}}$	0.7	1.3	2	V	–

3 Pin description

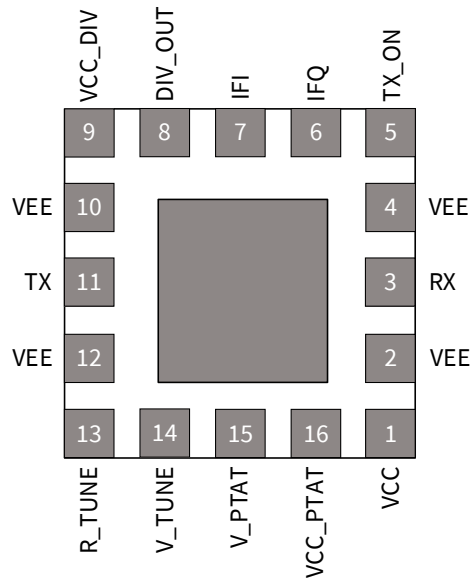


Figure 2 Pinout (top view)

Table 8 Pin definition and function

Pin number	Name	Function
1	VCC	Supply voltage
2	VEE	Ground
3	RX	Receiver RF input
4	VEE	GND
5	TX_ON	Output power enable
6	IFQ	Quadrature phase down converter IF output
7	IFI	In phase down converter IF output
8	DIV_OUT	Frequency divider output
9	VCC_DIV	Supply voltage of prescaler
10	VEE	Ground
11	TX	Transmitter RF output
12	VEE	Ground
13	R_TUNE	VCO operating frequency band select
14	V_TUNE	VCO frequency tuning input
15	V_PTAT	PTAT voltage source output
16	VCC_PTAT	PTAT voltage source power supply

4 Package diagram

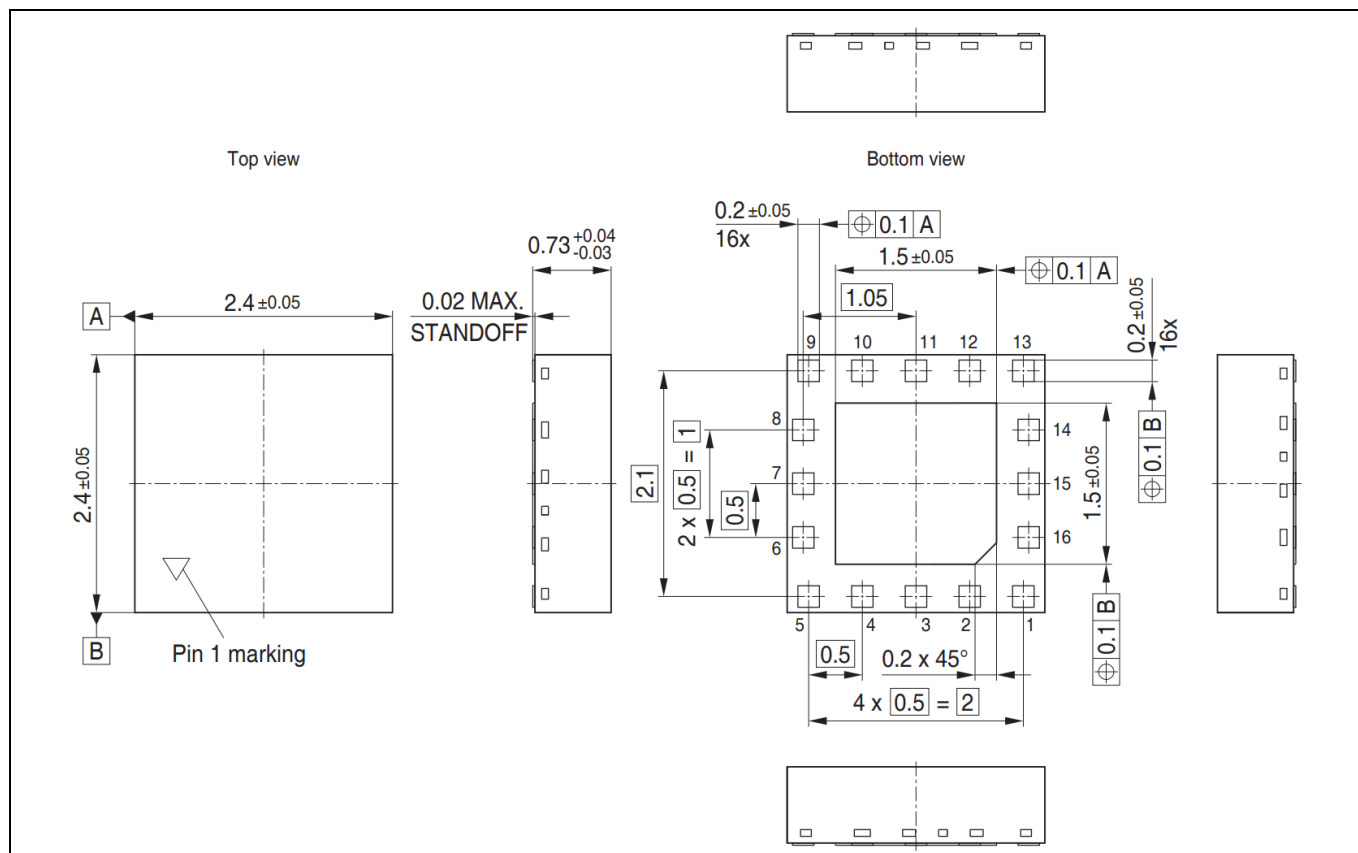


Figure 3 Package outline (top, side, and bottom view) of TSNP-16-9

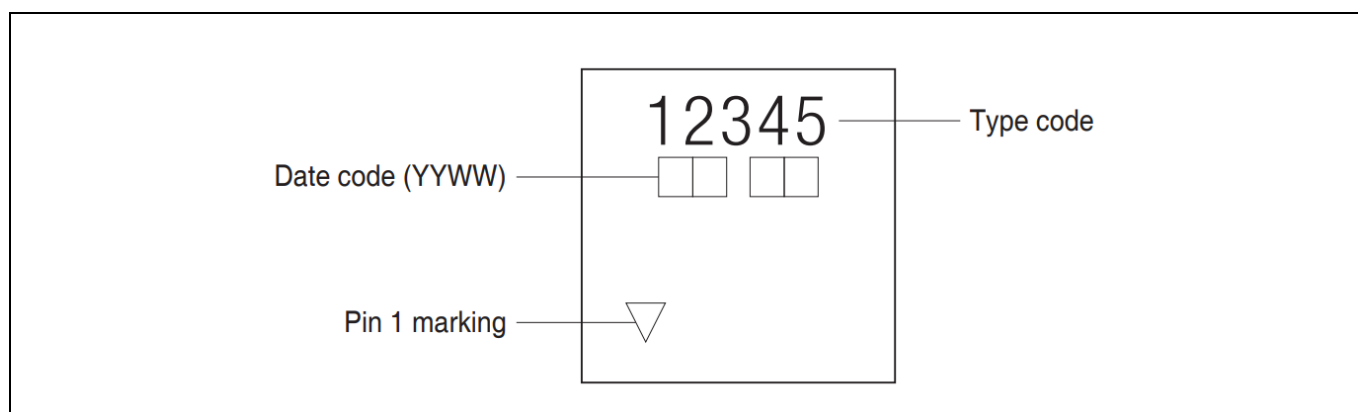


Figure 4 Marking layout of TSNP-16-9 (example)

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Package diagram

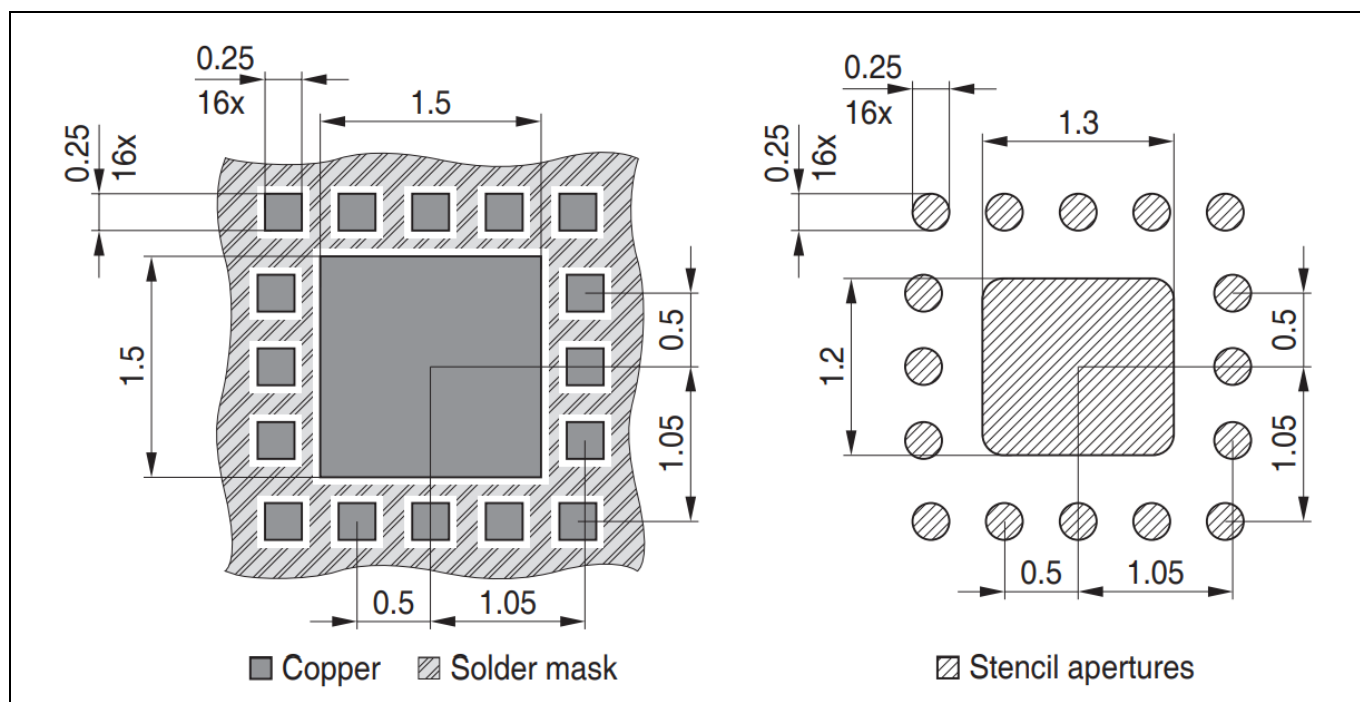


Figure 5 Soldering footprint of TSNP-16-9

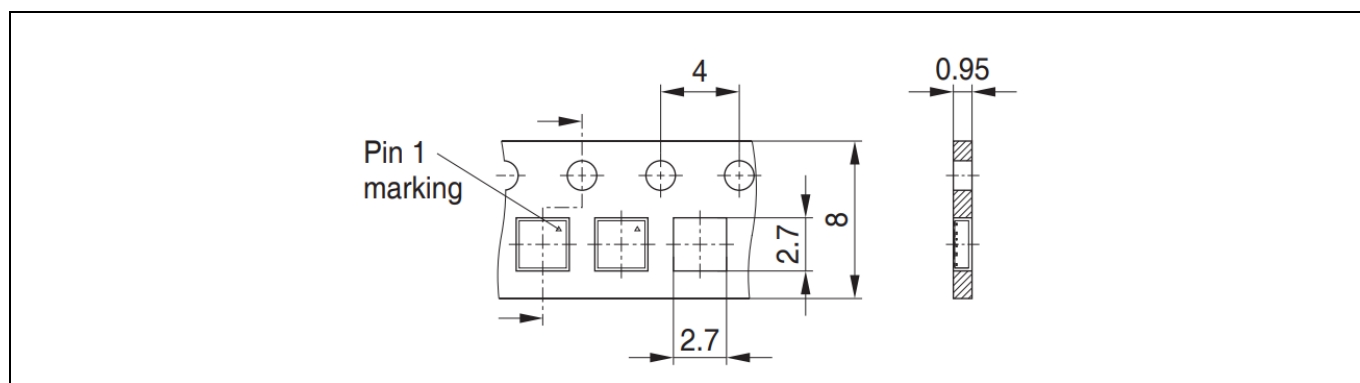


Figure 6 Packing description of TSNP-16-9; $\varnothing$ Reel: 180 mm, Pieces/Reel: 3000, Reels/Box: 1

Glossary

CDM

charged device model

ESD

Electrostatic discharge sensitivity

HBM

human body model

LNA

Low noise amplifier

MMIC

Monolithic microwave integrated circuit

PPF

polyphase filter

RX

Receiver

TX

Transmitter

VCO

Voltage controlled oscillator

Revision history

Document revision	Date	Description of changes
01_10	2017-11-03	Initial release
01_30	2018-05-08	Added Reference to matching structures and footprint according to UG133248 Specification of Harmonic Suppression is limited to second harmonic only Note is added to TX_ON low /high level input voltage specification
01_31	2021-09-15	Typo fixed: TX_ON
01_32	2025-06-25	Updated to the latest Infineon template
01_33	2026-10-07	Updated the max. value for Supply voltage PTAT voltage source in Table 1

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