XENSIV™ Digital temperature sensor

Key benefits & features

The benefits and features of XENSIV™ AS621x, Digital temperature sensor are listed below:

Table 1 Added value of using AS621x

Benefits	Features
High measurement accuracy	± 0.2°C (from -10°C to 65°C, for AS6212) ± 0.3°C (from -40°C to -10°C and from 65°C to 85°C, for AS6212) ± 0.5°C (for remaining temperature span, for AS6212)
Low power consumption	6 µA @ Operation (typical, @4 Hz) 0.1 µA @ Standby (typical)
Supply voltage range	1.71 V - 3.6 V (0°C to 125°C)
Small PCB footprint	1.5 mm x 1 mm (WLCSP)

Applications

- Electronic equipment
  - Tablets
  - Convertibles
  - Laptop
- Personal computers
- Wearables
- HVAC

General description

The AS621x IC is a high accuracy digital temperature sensor system that communicates via a 2-wire digital bus with other devices. It consists of a Si bandgap temperature sensor, an ADC and a digital signal processor.

The family consists of 3 different variants (AS6212, AS6214 and AS6218). The difference between these variants is the temperature accuracy:

Table 2 Variants

Variant	Temperature accuracy	Remark
AS621**2**	±0.2°C	Between -10°C to 65°C
AS621**4**	±0.4°C	Between 0°C to 65°C
AS621**8**	±0.8°C	Between 0°C to 65°C

The high temperature accuracy and an ultra-low power consumption (low operation and quiescent current) makes the AS621x ideally suited for mobile/battery powered applications.

The AS621x is an easy to integrate and use solution, featuring a factory-calibrated sensor, integrated linearization and the possibility to use 8 different I^2C addresses, enabling to use eight AS621x devices on one bus.

Additionally, the AS621x temperature sensor system features an alert functionality, which triggers e.g. an interrupt to protect devices from excessive temperatures.

The AS621x production test setup is calibrated according NIST and the verification equipment is calibrated by an ISO/IEC-17025 accredited laboratory.

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1 Block diagram

The functional blocks of this device are shown below:

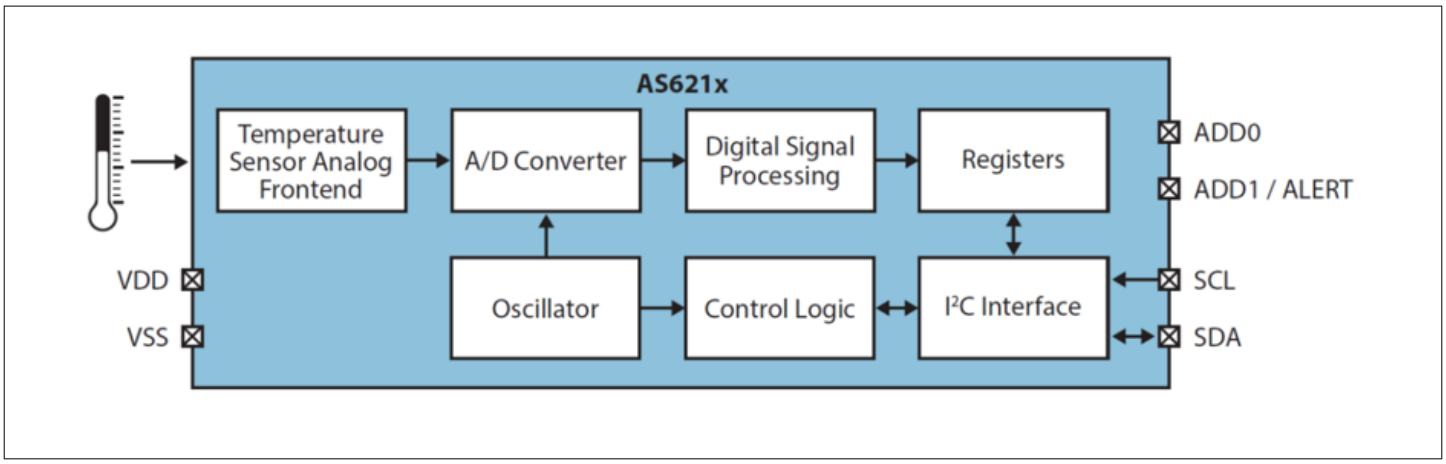


Figure 1 Functional blocks of AS621x

In Figure 1, the functional blocks are depicted. The sensing element for sensing the temperature is a Si bipolar transistor. The analog signal of the sensing element is converted into a digital signal by the A/D converter and the signal is further processed by a digital signal processor and written into the registers. The registers can be accessed via the serial bus interface (I^2C bus).

2 Ordering information

Product type (Infineon)	Product type (ams)	Ordering code	Package	Marking	Delivery form	Delivery quantity
AS6212-AWLT-S-WLP	AS6212-AWLT-S	SP006310307	WLCSP	AS6212	Tape & reel	500 pcs/reel
AS6212-AWLT-L-WLP	AS6212-AWLT-L	SP006310309	WLCSP	AS6212	Tape & reel	12000 pcs/ reel
AS6214-AWLT-S-WLP	AS6214-AWLT-S	SP006310311	WLCSP	AS6214	Tape & reel	500 pcs/reel
AS6214-AWLT-L-WLP	AS6214-AWLT-L	SP006310313	WLCSP	AS6214	Tape & reel	12000 pcs/ reel
AS6218-AWLT-S-WLP	AS6218-AWLT-S	SP006310315	WLCSP	AS6218	Tape & reel	500 pcs/reel
AS6218-AWLT-L-WLP	AS6218-AWLT-L	SP006310317	WLCSP	AS6218	Tape & reel	12000 pcs/ reel

3 Pin assignment

3.1 Pin diagram

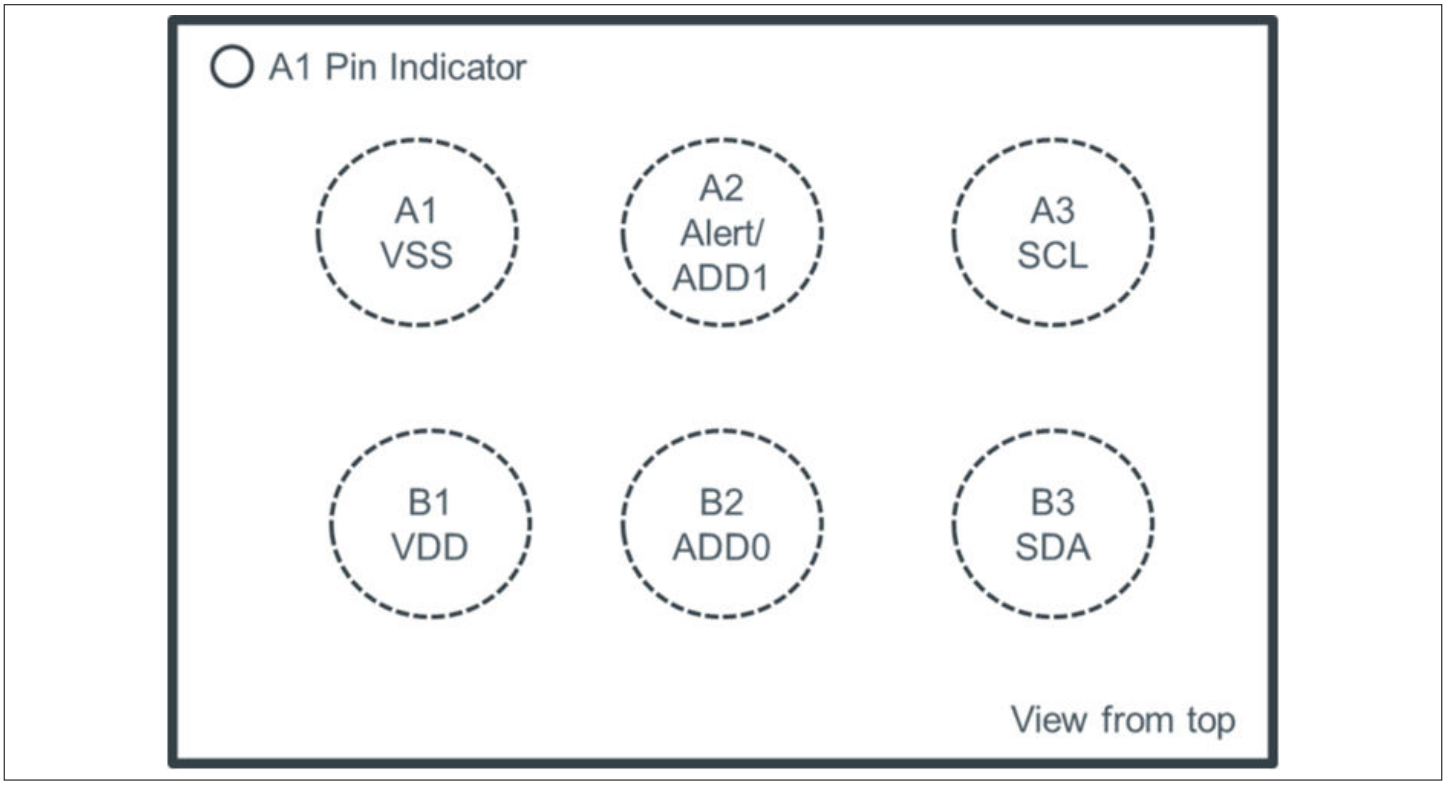


Figure 2 Pin assignment WLCSP

In Figure 2, the pin assignment of the WLCSP package is shown. The viewing side is from the top. The A1 pin is also marked with a point on the top side.

3.2 Pin description

Table 3 Pin description of AS621x (WLCSP)

Pin number	Pin name	Pin type[1)]	Description
A1	VSS	S	Ground pin
A2	ALERT/ADD1	DIO_SOD	Alert output and address select1
A3	SCL	DI_S	Serial interface clock
B1	VDD	S	Positive supply voltage
B2	ADD0	DI_S	Address select 0
B3	SDA	DIO_SOD	Serial interface data

1) Explanation of abbreviations:
S = Supply
DI_S = Digital Schmitt Trigger Input
DIO_SOD = Digital Schmitt Trigger Input / Open Drain Output

In Table 3, the pins of AS621x are described. External pull up resistors (to VDD) are necessary for the pins "SDA" and "SCL".

The pin "ADD0" must not be left unconnected (refer to Bus address for further details).

The pin "ALERT/ADD1" is used to set the I^2C address and has the additional functionality of triggering an interrupt. In case this ALERT functionality is used, a pull up resistor (to VDD) is necessary. If this functionality is not used it must be connected to VSS or SCL, depending on the selected I^2C address (refer to Bus address for further details). It must not be left unconnected.

4 Absolute maximum ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Operating Conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4 Absolute maximum ratings of AS621x

Symbol	Parameter	Min.	Max.	Unit	Comments
Electrical parameters					
V_{DD} / V_{SS}	Supply voltage to VSS	-0.3	4	V	Reference to VSS
VDIO	IO pin voltage	-0.3	4	V	Reference to VSS
I_SCR	Input current (latch up immunity)	-100	100	mA	According to JESD78D
Electrostatic discharge					
ESD_{HBM}	Electrostatic discharge HBM	±2000		V	MIL_STD_833J-3015.9
Temperature ranges and storage conditions					
T_A	Operating ambient temperature	-40	125	°C	
T_J	Operating junction temperature	-40	125	°C	
T_{STRG}	Storage temperature range	-55	125	°C	
T_{BODY}	Package body temperature		260	°C	IPC/JEDEC J-STD-020[1)]
R_{HNC}	Relative humidity (non-condensing)	5	85	%	
MSL	Moisture sensitivity level	1			Unlimited floor life time

1) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices”.

5 Operating conditions

The AS621x is a complete sensor system that has an integrated sensing element, the analog frontend, the A/D converter and the digital signal processing part.

The digital signal processing part consists of the signal processor, the registers and the serial bus interface.

5.1 Analog system parameters

Table 5 Analog system parameters of AS621x

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage	VDD	1.71 2.0	3.0 3.0	3.6 3.6	V	T = 0°C to 125°C T = -40°C to 125°C
Temperature range	T	-40		125	°C	
Standby current consumption	IDD_stdby		0.1 0.3	0.4 9.0	µA	T = -40°C to 65°C T = 65°C to 125°C
Current consumption (4 conversions/s)	IDD_active		6	7 16	µA	T = -40°C to 65°C Serial bus inactive T = 65°C to 125°C Serial bus inactive
Resolution	N		16		Bits	
Conversion time	TS	22	36	51	ms	
Conversion rate	NS		0.25 1 4 8	0.35 1.35 5.5 10.7	Conv/s	CR[1:0] = 00 CR[1:0] = 01 CR[1:0] = 10 CR[1:0] = 11
Supply voltage rise time	TRise_VDD			20	ms	From 0.1 V to 1.6 V
Supply voltage slew rate	SR_VDD	50			mV/ms	From 0.1 V to 1.6 V

In Table 5, an overview of the analog system parameters is given.

The current consumption for less than 4 conversions per second is lower than the values given in Table 5.

Table 6 Temperature accuracy values of AS621x

Variant	Symbol	Min.	Typ.	Max.	Unit	Note
AS6212	T_ERR	-0.3 -0.2 -0.3 -0.5		0.3 0.2 0.3 0.5	°C	T= -40°C to -10°C T= -10°C to 65°C T= 65°C to 85°C T= 85°C to 125°C
AS6214	T_ERR	-1.0 -0.4 -1.0		1.0 0.4 1.0	°C	T= -40°C to 0°C T= 0°C to 65°C T= 65°C to 125°C

(table continues...)

Table 6 (continued) Temperature accuracy values of AS621x

Variant	Symbol	Min.	Typ.	Max.	Unit	Note
AS6218	T_ERR	-1.0 -0.8 -1.0		1.0 0.8 1.0	°C	T= -40°C to 0°C T= 0°C to 65°C T= 65°C to 125°C

In Table 6, the different accuracy values of AS621x are shown. These values are representative for a 3σ distribution. All accuracy values are valid for the complete supply voltage range given in Table 5.

5.2 Digital system parameters

Table 7 Digital system parameters of AS621x

Parameter	Symbol	Pins	Min.	Max.	Unit	Note
High level input voltage	V_IH	SCL, ADD0	0.7 * VDD		V	
Low level input voltage	V_IL	SCL, ADD0		0.3 * VDD	V	
Hysteresis voltage	V_HYST	SCL, ADD0, SDA, Alert	200	1200	mV	
Input leakage current	I_LEAK	SCL; ADD0	-1	1	µA	V_IL = 0.0 V
Low level output voltage	V_OL	Alert		VSS + 0.4	V	I_OL = 3 mA
High level input voltage	V_IH	SDA	0.7 * VDD		V	
Low level input voltage	V_IL	SDA		0.3 * VDD	V	
Low level output voltage	V_OL	SDA		VSS + 0.4	V	
Tristate leakage current	I_OZ	SDA	-10	10	µA	to VSS

In Table 7, an overview of the digital system parameters is given.

5.3 Thermal information

Table 8 Thermal information of AS621x

Parameter	Symbol	Value	Unit
Junction to case (top) thermal resistance	R_{JC}	33.4	K/W
Junction to ball (not board) thermal resistance	R_{JB}	9	K/W
Case to ambient thermal resistance	R_{CA}	31.05	K/W
Junction to ambient thermal resistance (top) $R_{JC} + R_{CA}$	R_{JA}	64.45	K/W
Thermal mass	Mt	1	mJ/K

6 Register description

6.1 Register overview

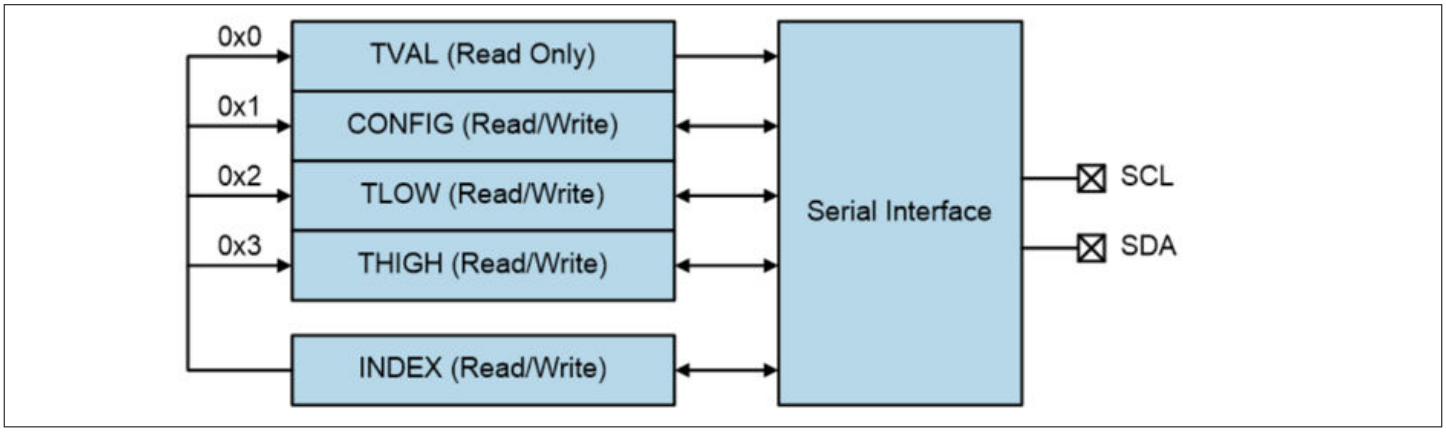


Figure 3 **Register map with serial interface**

In Figure 3, the registers that the device contains are shown.

With the use of the index register, it is possible to address the specific register. The index register is an 8-bit register, where only bits 0 and 1 are used as shown in Table 9 and all other bits are set to 0 and read only.

6.1.1 Index register

Table 9 **Index register**

Bit	Bit name	Default	Access
0	Address bit	0	RW
1	Address bit	0	RW
2	Reserved	0	RO
3	Reserved	0	RO
4	Reserved	0	RO
5	Reserved	0	RO
6	Reserved	0	RO
7	Reserved	0	RO

Table 10 **Register map**

Address	Symbol	Register	Description
0x0	TVAL	Temperature register	Contains the temperature value
0x1	CONFIG	Configuration register	Configuration settings of the temperature sensor
0x2	TLOW	T_{LOW} register	Low temperature threshold value
0x3	THIGH	T_{HIGH} register	High temperature threshold value

The first 2-bit addresses in the index register define the access to the registers shown in Table 10. This means that in order to access the different registers, the index register must be set accordingly. With the exception of the TVAL register (which contains the temperature value data), all registers are read/write accessible.

6.2 Detailed register description

6.2.1 Configuration register (Address 0x1)

Table 11 CONFIGURATION register

Addr: 0x1		CONFIGURATION		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
0	Reserved	0	RO	Reserved
1	Reserved	0	RO	Reserved
2	Reserved	0	RO	Reserved
3	Reserved	0	RO	Reserved
4	Reserved	0	RO	Reserved
5	AL	1	RO	Alert Bit (AL)
6	CR[0]	0	RW	Conversion RATE (CR)
7	CR[1]	1	RW	Conversion RATE (CR)
8	SM	0	RW	Sleep Mode (SM)
9	IM	0	RW	Interrupt Mode (IM)
10	POL	0	RW	Polarity (POL)
11	CF[0]	0	RW	Consecutive Faults (CF)
12	CF[1]	0	RW	Consecutive Faults (CF)
13	Reserved	0	RO	Reserved
14	Reserved	1	RO	Reserved
15	SS	0	RW	Single Shot

The configuration register is a 16-bit register which defines the operation modes of the device. Any read/write operation processes the MSB byte first.

In Table 10, the configuration register is shown. The bits 0-4 and 13-14 are not to be used and are set to read only. The explanation of the other bits are detailed in the following sections.

6.2.2 Alert bit

The alert bit can be used to easily compare the current temperature reading to the thresholds that can be set in the TLOW and THIGH registers.

If the polarity bit is set to 0, the AL bit is read as 1 until the converted temperature value exceeds the defined value in the high temperature threshold register THIGH for the number of defined consecutive faults (bits CF). Such an event causes the AL bit to toggle to 0 and the value is kept until the converted temperature value falls below the defined value in the low temperature threshold register TLOW for the number of defined consecutive faults. If this condition is met, the AL bit is reset to 1.

The polarity bit (POL) defines the active state of the alert bit as depicted in Figure 4.

The alert bit has the same setting as the alert output as long as the device is configured for the comparator mode.

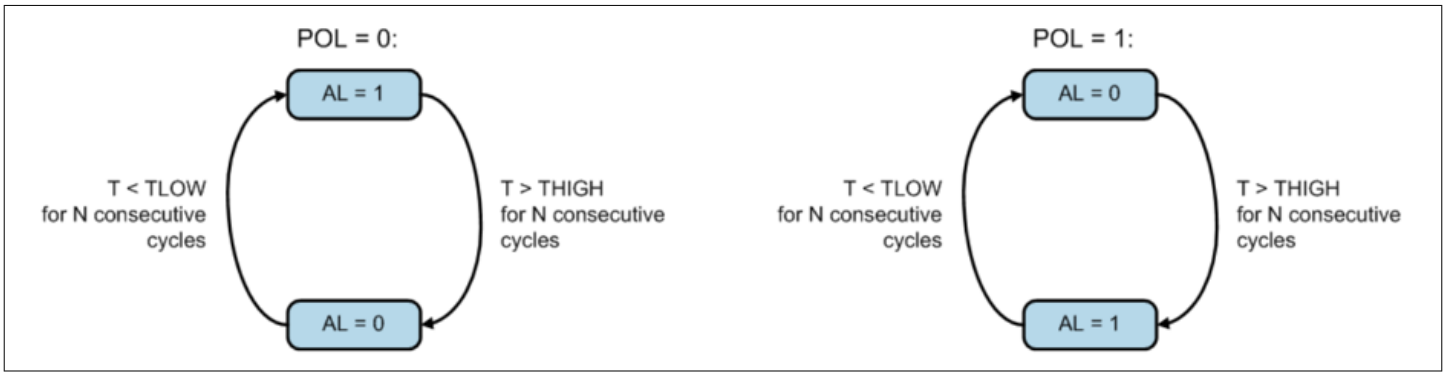


Figure 4 **State diagram of the alert bit**

6.2.3 Conversion rate bits

The conversion rate bits define the number of executed temperature conversions per time unit. Additional readouts of the temperature register between conversions are possible but not recommended because the value is changed only after a conversion is finished.

Values of 125 ms, 250 ms, 1 s and 4 s for a conversion can be configured while the default rate is set to 4 conversions per second. Table 12 summarizes the different configuration settings:

Table 12 **Conversion rate configuration**

Conversion rate bits		**Conversion rate**
Bit 7	**Bit 6**	**Conv/s**
0	0	0.25
0	1	1
1	0	4
1	1	8

The device immediately starts a conversion after a power-on sequence and provides the first result after typ. 36 ms (max. 51 ms). A higher power consumption occurs during the actual conversion while the device stays in the standby mode after a finished conversion until the next conversion is activated. This is shown in Figure 5.

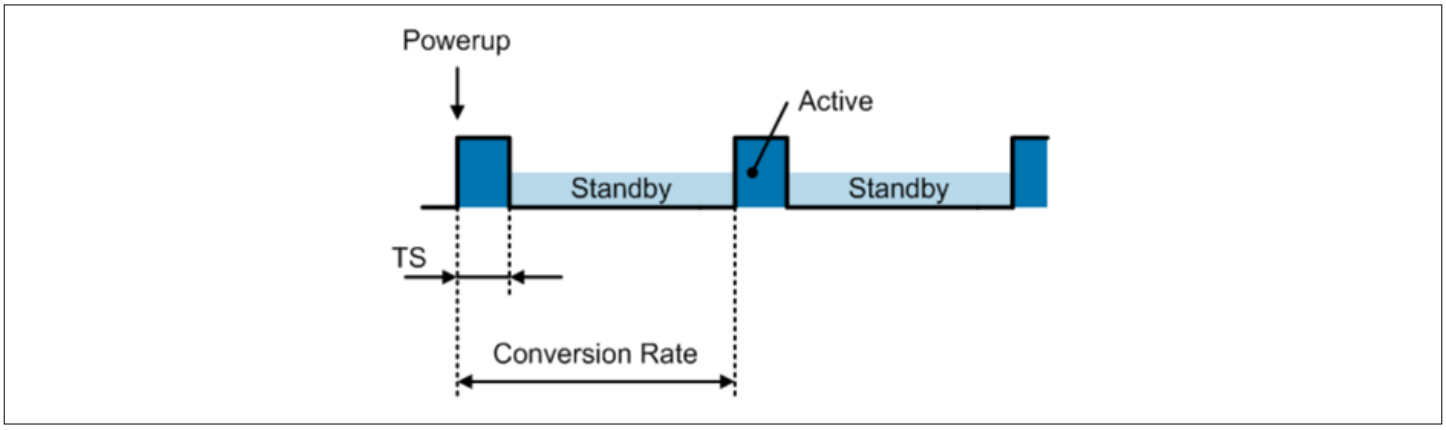


Figure 5 **Conversion sequence**

6.2.4 Sleep mode

The sleep mode is activated by setting the bit SM in the configuration register to 1. This shuts the device down immediately and reduces the power consumption to a minimum value.

The serial interface is the only active circuitry in the sleep mode in order to provide access to the digital registers.

Entering the sleep mode will take some time (120 ms maximum) and the first conversion after the sleep mode has been entered takes longer than the values specified in Table 5. It is therefore recommended when entering sleep mode to trigger a single shot conversion at the same time. After 150 ms (max), the device has then entered the sleep mode and subsequent conversion times are as specified in Table 5.

After resetting the SM bit to 0, the device enters the continuous conversion mode.

Table 13 Sleep mode configuration

Sleep mode bit	Operation mode
0	Continuous Conversion Mode
1	Sleep Mode

6.2.5 Interrupt mode

The interrupt mode bit defines whether the device operates in the temperature comparator mode or the interrupt mode. This defines the operation of the ALERT output as described in the polarity section bit.

Table 14 Interrupt mode configuration

Interrupt mode bit	Configuration mode
0	Comparator mode
1	Interrupt mode

The comparator mode is characterized that if the temperature value exceeds the THIGH value, the alert output is changed (e.g. from high to low if the polarity bit is set to 0 and vice versa). The alert output stays in that condition until the measured temperature drops below the defined TLOW value.

The interrupt mode is characterized that it changes the alert output as soon as the measured temperature crosses the THIGH or TLOW value threshold.

The alert bit has the same setting as the alert output if the device is set to comparator mode.

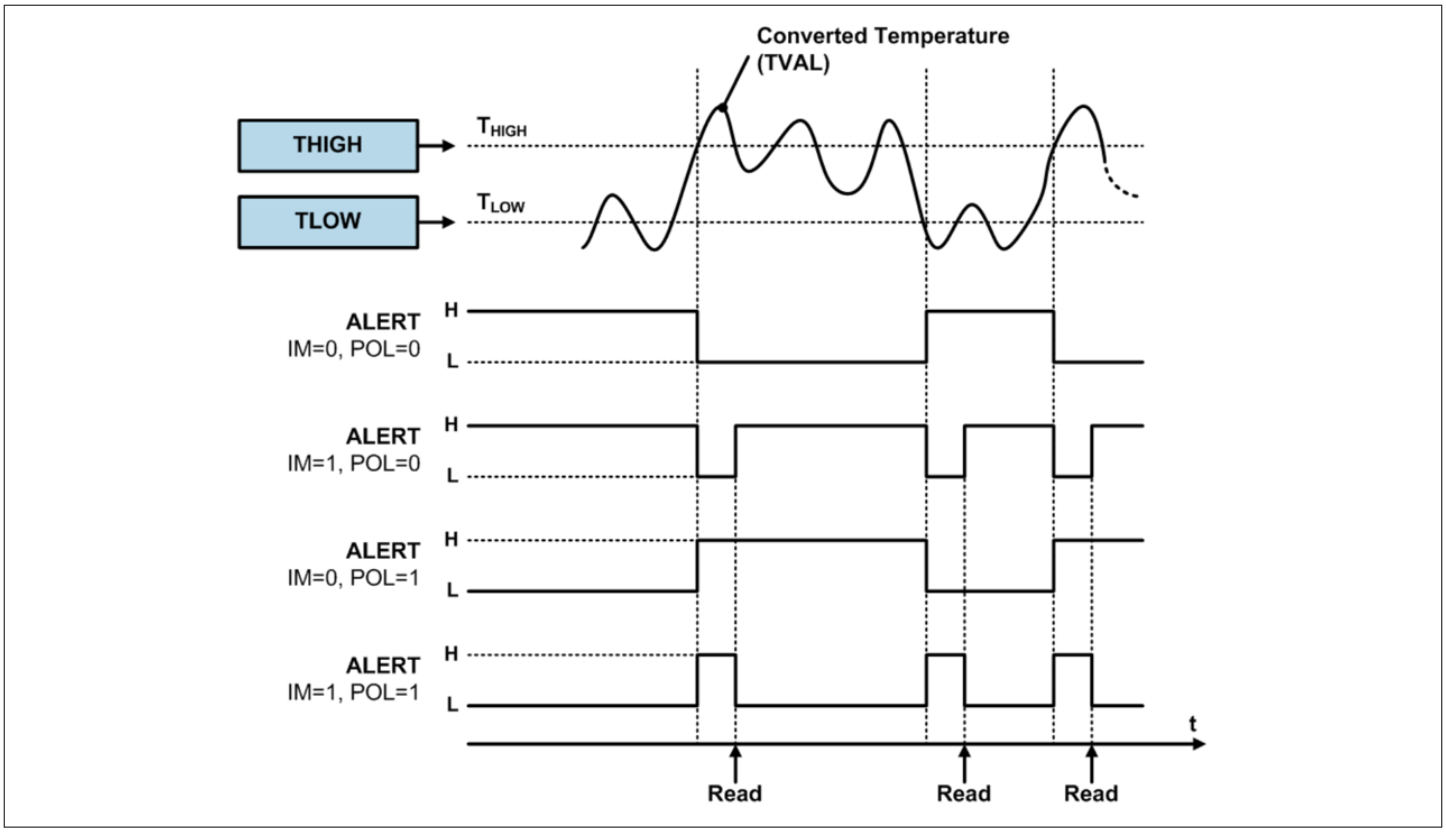


Figure 6 **Alert output functionality**

6.2.6 Polarity bit

The polarity bit configures the polarity of the ALERT output. If the polarity bit is cleared, the ALERT output is low active while it becomes high active if the polarity bit is set to '1'.

Table 15 **Polarity bit configuration**

Polarity bit	ALERT output
0	Active low
1	Active high

6.2.7 Consecutive faults

A fault condition persists if the measured temperature either exceeds the configured value in register THIGH or falls below the defined value in register TLOW. As a result, the ALERT pin indicates the fault condition if a defined number of consecutive temperature readings meets this fault condition. The number of consecutive faults are defined with two bits (12 and 11) and prevent a false alert if environmental temperature noise is present. The register configuration is shown in Table 16.

Table 16 **Consecutive faults bit settings**

Consecutive fault bits		Consecutive faults (N)
Bit 13	**Bit 12**	
0	0	1

(table continues...)

Table 16 (continued) Consecutive faults bit settings

Consecutive fault bits		Consecutive faults (N)
0	1	2
1	0	3
1	1	4

6.2.8 Single shot conversion

The device features a single shot measurement mode if the device is in sleep mode (SM=1). By setting the "Single Shot-bit" to 1, a single temperature conversion is started and the SS-bit can be read as 1 during the active conversion operation. Once the conversion is completed, the device enters the sleep mode again and the SS-bit is set to 0. The single shot conversion allows very low power consumption since a temperature conversion is executed on demand only. This allows a user defined timing of the temperature conversions to be executed and is used if the consecutive operation mode is not required.

The first conversion triggered in this mode has a longer conversion time. In the section Sleep mode it is detailed together with the recommendation to trigger the first conversion simultaneously with entering the sleep mode.

As the device exhibits a very short conversion time, the effective conversion rate can be increased by setting the single shot bit repetitively after a conversion has finished. However, it has to be ensured that the additional power is limited, otherwise self-heating effects have to be considered.

Table 17 Single shot conversion bit settings

Single shot bit	Conversion
0	No conversion ongoing/conversion finished
1	Start single shot conversion/conversion ongoing

6.2.9 High and low limit registers

If the comparator mode is configured (IM=0), the ALERT output becomes active if the temperature equals or exceeds the defined value in register THIGH for the configured number of consecutive faults (N). This configuration is defined by the field CF in the configuration register. The ALERT output remains assigned until the converted temperature value equals or falls below the defined value in register TLOW for the same number of consecutive fault cycles.

If the interrupt mode is configured (IM=1), the ALERT output becomes active if the temperature equals or exceeds the defined value in register THIGH for the configured number of consecutive fault cycles. It remains active until a read operation is executed on any register. The ALERT output is also cleared if the device is set into sleep mode by setting bit SM in the configuration register.

Once the ALERT output is cleared, it is activated again only if the temperature value falls below the configured value in register TLOW. It remains active unless a read operation has taken place.

This sequence is repeated unless the device is set into the comparator mode. This reset command clears the interrupt mode bit and consequently puts the device into the comparator mode.

The sequential behavior is summarized in Figure 7.

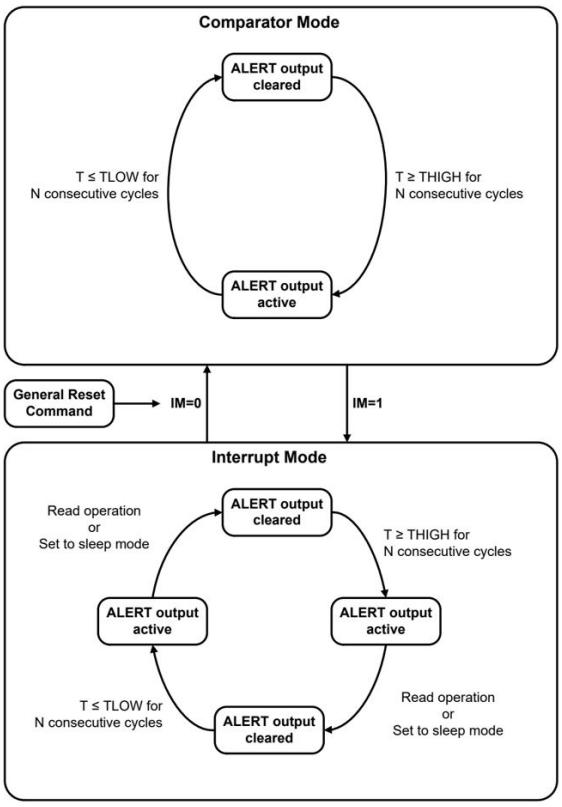


Figure 7 Alert operation modes

Table 18 defines the content of the registers TLOW and THIGH. For data transmission, the MSB byte is transmitted first, followed by the LSB byte. The data format for representing the threshold temperatures is equal to the temperature register (TVAL). After a power-up, the registers are initialized with the following default values:

Table 18 Default values for THIGH and TLOW

Register	Temperature	Binary value
TLOW	75°C	0010 0101 1000 0000
THIGH	80°C	0010 1000 0000 0000

Table 19 defines the register bits of the THIGH and TLOW register.

Table 19 Register bit settings for THIGH/TLOW

Addr: 0x2 / 0x3

Bit	TLOW register	THIGH register	Access
0	0	0	Permanently set to 0
1	0	0	Permanently set to 0
2	0	0	Permanently set to 0
3	0	0	Permanently set to 0
4	L4	H4	RW
5	L5	H5	RW
6	L6	H6	RW

(table continues...)

Table 19 (continued) Register bit settings for THIGH/TLOW

Addr: 0x2 / 0x3

Bit	TLOW register	THIGH register	Access
7	L7	H7	RW
8	L8	H8	RW
9	L9	H9	RW
10	L10	H10	RW
11	L11	H11	RW
12	L12	H12	RW
13	L13	H13	RW
14	L14	H14	RW
15	L15	H15	RW

6.2.10 Temperature register (Address 0x0)

Table 20 Temperature value register

Addr: 0x0

Bit	Bit name
0	T0
1	T1
2	T2
3	T3
4	T4
5	T5
6	T6
7	T7
8	T8
9	T9
10	T10
11	T11
12	T12
13	T13
14	T14
15	T15

The temperature register contains the digitally converted temperature value and can be read by setting the index pointer to the TVAL register (0x0).

Two consecutive bytes must be read to obtain the complete temperature value. The MSB byte (Bits 15 to 8) is transmitted upon the first read access and the LSB byte (Bits 7 to 0) is transmitted after the second read access.

A temperature value is represented as a 2's complement value in order to cover also negative values. After power-up, the temperature value is read as 0°C until the first conversion has been completed. One LSB corresponds to 0.0078125°C (=1/128°C).

The binary values can be calculated according to the following formulas:

Positive values: |Value| / LSB

Negative values: Complement (|Value| / LSB) + 1

Example 75°C:

$$75°C/0.0078125°C = 9600 = Binary \quad 0010 \quad 0101 \quad 1000 \quad 0000 = Hex \quad 2580$$

Example -40°C:

$$\left|\overline{-40°C}\right|/0.0078125°C + 1 = \overline{5120} + 1 = Binary \quad \overline{0001 \quad 0100 \quad 0000 \quad 0000} + 1 = \quad 1110 \quad 1100 \quad 0000 \quad 0000 = Hex \quad EC00$$

Table 21 Temperature conversion examples

Temperature (°C)	Digital output (Binary)	Digital output (Hex)
100.0	0011 0010 0000 0000	3200
75.0	0010 0101 1000 0000	2580
50.0	0001 1001 0000 0000	1900
25.0	0000 1100 1000 0000	0C80
0.125	0000 0000 0001 0000	0010
0.0078125	0000 0000 0000 0001	0001
0.0	0000 0000 0000 0000	0000
-0.0078125	1111 1111 1111 1111	FFFF
-0.125	1111 1111 1111 0000	FFF0
-25.0	1111 0011 1000 0000	F380
-40.0	1110 1100 0000 0000	EC00

6.3 Serial interface

The device employs a standard I²C-serial bus.

6.3.1 Bus description

A data transfer must be invoked by a master device (e.g. microcontroller) which defines the access to the slave device. The master device defines and generates the serial clock (SCL) and the start/stop conditions.

In order to address a specific device, a START condition has to be generated by the master device by pulling the data line (SDA) from a logic high level to a logic low level while the serial clock signal (SCL) is kept at high level.

After the start condition, the slave address byte is transmitted which is completed with a ninth bit which indicates a read (bit='1') or a write operation (bit='0') respectively. All slaves read the data on the rising edge of the clock. An acknowledge signal is generated by the addressed slave during the ninth clock pulse. This acknowledge signal is produced by pulling the pin SDA to a low level by the selected slave.

Subsequently, the byte data transfer is started and finished by an acknowledge bit. A change in the data signal (SDA) while the clock signal (SCL) is high causes a START or STOP condition. Hence, it must be ensured such a condition is prevented during a data transfer phase.

After completing the data transfer, the master generates a STOP condition by pulling the data line (SDA) from low level to high level while the clock signal (SCL) is kept at high level.

6.3.2 Data interface

A bus connection is created by connecting the open drain input/output lines SDA and SCL to the two wire bus. The inputs of SDA and SCL feature Schmitt-trigger inputs as well as low pass filters in order to suppress noise on the bus line. This improves the robustness against spikes on the two wire interface.

Both fast transmission mode (1 kHz to 400 kHz) and high-speed transmission mode (1 kHz to 3.4 MHz) are employed to cover different bus speed settings.

Any data transfer transmits the MSB first and the LSB as last bit.

6.3.3 Bus address

A slave address consists of seven bits, followed by a data direction bit (read/write operation). The slave address can be selected from 8 different address settings by connecting the pin ADD0 and ADD1 to an appropriate signal as summarized in Table 22.

The ADD0 and the ADD1 pin must not be left unconnected.

The address selection with ADD1 depends on the usage of the ALERT function (described in chapter Alert function). In case the ALERT functionality is used, it must be connected via a pull up resistor to VDD. In case the ALERT functionality is not used, the pin must be connected to either SCL or VSS (refer to Table 23 for details).

Table 22 I²C address select configuration

ALERT/ADD1 connection	ADD0 connection	Alert functionality enabled	Device address (bin)	Device address (hex)
SCL	VSS	No	100 0100	0x44
SCL	VDD	No	100 0101	0x45
SCL	SDA	No	100 0110	0x46
SCL	SCL	No	100 0111	0x47
VSS	VSS	No	100 1000	0x48

(table continues...)

Table 22 (continued) I²C address select configuration

ALERT/ADD1 connection	ADD0 connection	Alert functionality enabled	Device address (bin)	Device address (hex)
VSS	VDD	No	100 1001	0x49
VSS	SDA	No	100 1010	0x4A
VSS	SCL	No	100 1011	0x4B
Pull up to VDD	VSS	Yes	100 1000	0x48
Pull up to VDD	VDD	Yes	100 1001	0x49
Pull up to VDD	SDA	Yes	100 1010	0x4A
Pull up to VDD	SCL	Yes	100 1011	0x4B

6.3.4 Read/write operation

In order to access an internal data register, the index register must be written in advance. This register contains the actual register address and selects the appropriate register for an access. A typical transfer consists of the transmission of the slave address with a write operation indication, followed by the transmission of the register address and is finalized with the actual register content data transfer. This implies that every write operation to the temperature sensor device requires a value for the index register prior to the transmission of the actual register data.

The index register defines the register address for both the write and read operation. Consequently, if a read operation is executed, the register address is taken from the index register which was defined from the last write operation.

If a different register needs to be read, the index register has to be written in advance to define the new register address. This is accomplished by transmitting the slave address with a low R/W bit, followed by the new content of the index register. Subsequently, the master provokes a START condition on the bus and transmits the slave address with a high R/W bit in order to initiate a read operation.

Since the index register always keeps its last value, reads can be executed repetitively on the same register.

Similarly to the byte transfer where the MSB is transmitted first, the transfer of a 16-bit word is executed by a two byte transfer whereas the MSB byte is always transmitted first.

6.3.5 Slave operation

The device employs a slave functionality only (slave transmitter and slave receiver) and cannot be operated as a bus master. Consequently, the device never actively drives the SCL line.

6.3.6 Slave receiver mode

Any transmission is invoked by the master device by transmitting the slave address with a low R/W bit. Subsequently, the slave device acknowledges the reception of the valid address by pulling the ninth bit to a low level. Following to acknowledge, the master transmits the content of the index register. This transfer is again acknowledged by the slave device. The next data byte(s) are written to the actual data register which is selected by the index register while each transfer is acknowledged upon a completed transfer by the slave device. A data transfer can be finished if the master transmits a START or a STOP condition on the bus.

6.3.7 Slave transmitter

The master transmits the slave address with a high R/W bit. In turn, the slave acknowledges a valid slave address. Subsequently, the slave transmits the MSB byte of the actual selected data register by the index register. After the

MSB byte transmission, acknowledge is sent by the master. Afterwards, the LSB byte is transmitted by the slave which is also acknowledged by the master after the completed transmission. The data transfer can be terminated by the master by transmitting a Not-Acknowledge after the transmitted slave data or by invoking a START or a STOP condition on the bus.

6.3.8 Alert function

If the device is configured for an interrupt mode operation (IM=1), the ALERT output can be used as an alert signal.

If the polarity bit is set to '0' (POL='0'), the alert condition bit is set to '0' in case the temperature has exceeded the configured value in register THIGH. Accordingly, the alert condition bit is set to '1' if the temperature has fallen below the configured value in register TLOW.

If the polarity bit is set to '1' (POL='1'), the alert condition bit is inverted. Table 23 summarizes the status of the alert condition bit with different alert conditions and polarity configurations.

Table 23 Alert condition bit

Polarity bit	Alert condition	Alert condition bit (AC-Bit)
0	T ≥ THIGH	0
0	T ≤ TLOW	1
1	T ≥ THIGH	1
1	T ≤ TLOW	0

6.3.9 High speed mode

The bus operation is limited to 400 kHz unless a high speed command is issued by the master device as the first byte after a START condition. This switches the bus to a high speed operation which allows data transfer frequencies up to 3.4 MHz. Such a command is not acknowledged by the slave but the input filter time constants on the serial interface (SDA and SCL) are adapted to allow the higher transfer rate.

After a high speed command, the slave address is transmitted by the master in order to invoke a data transfer. The bus keeps operating at the higher operating frequency until the master issues a STOP condition on the serial bus. Upon the reception of the STOP condition by the slave, the input filters are switched to their initial time constants which allow lower transfer rates only.

6.3.10 General call

A general call is issued by the master by transmitting the general call address (000 0000) with a low R/W bit. When this command is issued on the bus, the device acknowledges this command. The device also acknowledges the second byte but ignores the data. Subsequent bytes sent by the master during the general call are not acknowledged.

6.3.11 Start byte

When the master transmits address 000 0000 and a high R/W bit ("START byte") the device acknowledges the address. The device then send the MSB data byte and LSB data byte, where the data corresponds to the content of the register whose address has been last written to. After reset this corresponds to the temperature register.

6.3.12 Timeout function

The serial interface of the slave device is reset if the clock signal SCL is kept low for typ. 30 ms. Such a condition results in a release of the data line by the slave in case it has been pulled to low level. The slave remains inactive after a timeout and waits for a new START command invoked by the bus master. In order to prevent a timeout, the bus transfer rate must be higher than 1 kHz.

6.3.13 Bus conditions

The following conditions occur on the serial bus which is compatible to the I²C-Bus.

Bus idle

The signals SDA and SCL are not actively driven and pulled to a high level by an external pullup resistor.

Start data transfer

A transition of the SDA input from high to low level while the SCL signal is kept at high level results in a START condition. Such a START condition must precede any data transfer.

Stop data transfer

A transition of the SDA input from low to high level while the SCL signal is kept at high level results in a STOP condition. Any data transfer is finished by generating a STOP or START condition.

Data transfer

The master device defines the number of data bytes between a START and STOP condition and there is no limitation in the amount of data to be transmitted.

If it is desired to read only a single MSB byte without the LSB byte, a termination of the data transfer can be provoked by issuing a START or STOP condition on the bus.

Acknowledge

It is mandatory for each slave device to respond with acknowledge if the device is addressed by the master. Acknowledge is indicated by pulling down the data line (SDA) while the clock signal (SCL) is high in the acknowledge clock phase. In order to avoid an unwanted START or STOP condition on the bus, setup and hold times must be met.

The master can signal an end of data transmission by transmitting a Not-Acknowledge on the last transmitted data byte by keeping the acknowledge bit at high level.

6.3.14 Timing characteristics

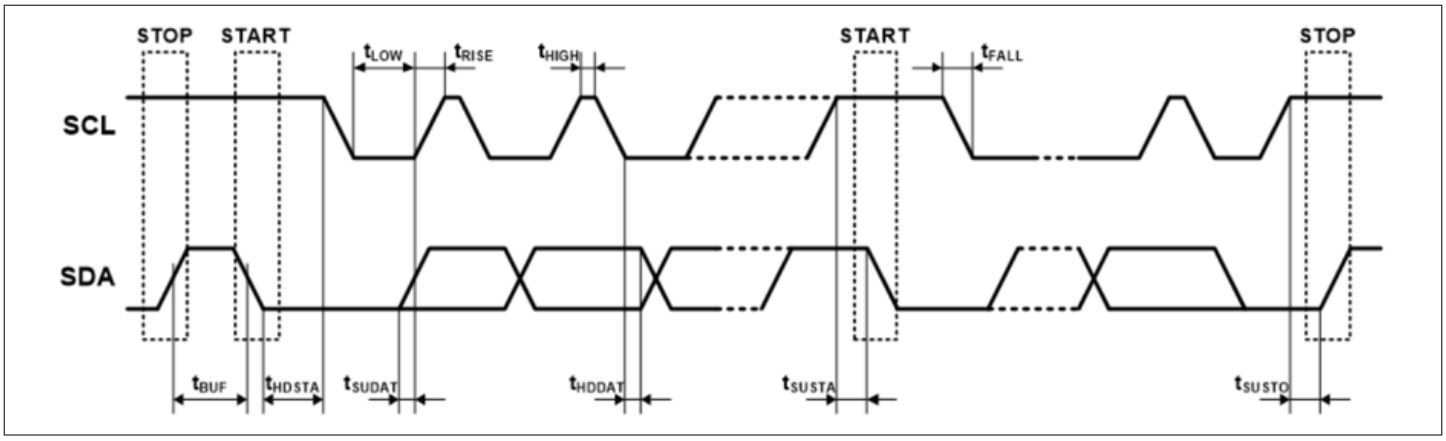


Figure 8 **Serial interface timing diagram**

Table 24 **Bus timing specifications**

Parameter	Symbol	Fast mode		High speed mode		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}	0.001	0.4	0.001	3.4	MHz
Bus free time between STOP and START condition	t_{BUF}	600		160		ns

(table continues...)

Table 24 (continued) Bus timing specifications

Parameter	Symbol	Fast mode		High speed mode		Unit
		Min.	Max.	Min.	Max.	
Hold time after repeated START condition	t_{HDSTA}	100		100		ns
Repeated START condition setup time	t_{SUSTA}	100		100		ns
Data in hold time	t_{HDDAT}	0		0		ns
Data out hold time[1)]	t_{DH}	100		100		ns
Data setup time	t_{SUDAT}	100		10		ns
SCL clock low period	t_{LOW}	1300		160		ns
SCL clock high period	t_{HIGH}	600		60		ns
Clock/Data fall time	t_F		300		80	ns
Clock/Data rise time	t_R		300		80	ns
Clock/Data rise time for SCL ≤ 100 kHz	t_R		1000			ns

1) The device will hold the SDA line high for 100 ns during the falling edge of the SCL.

6.3.15 Timing diagrams

The following timing diagrams depict the different bus operation modes and data transmission:

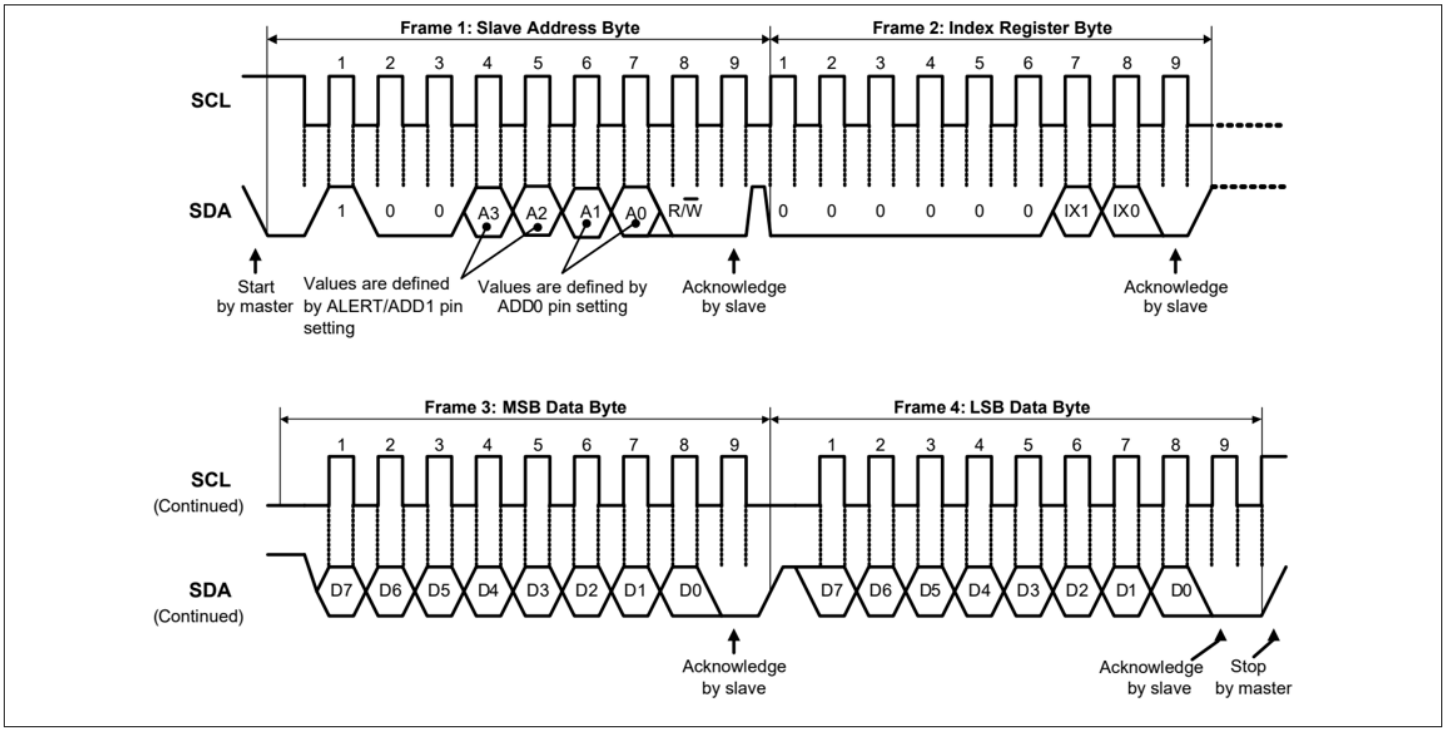


Figure 9 Timing diagram for word write

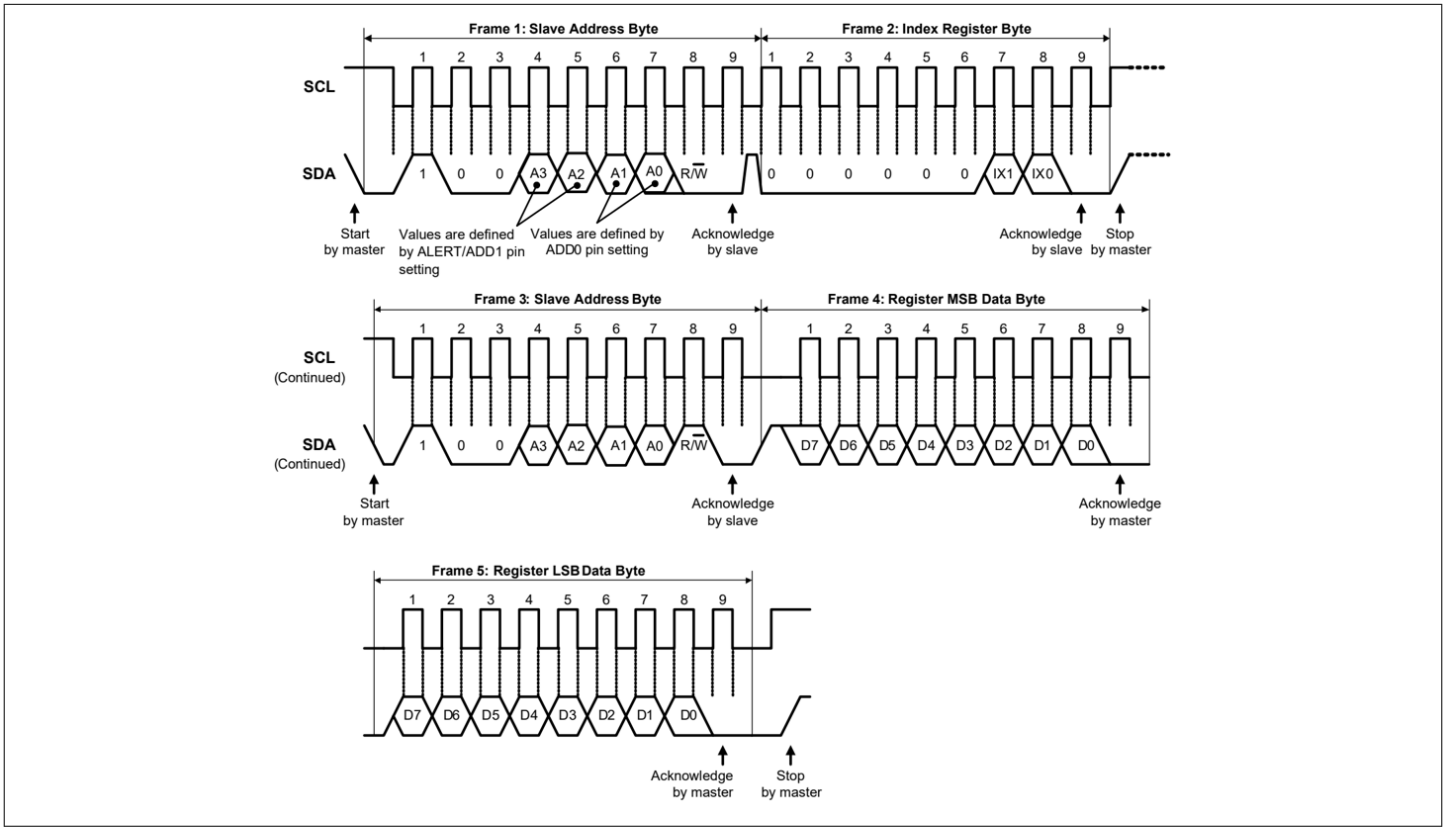


Figure 10 Timing diagram for word read

7 Application information

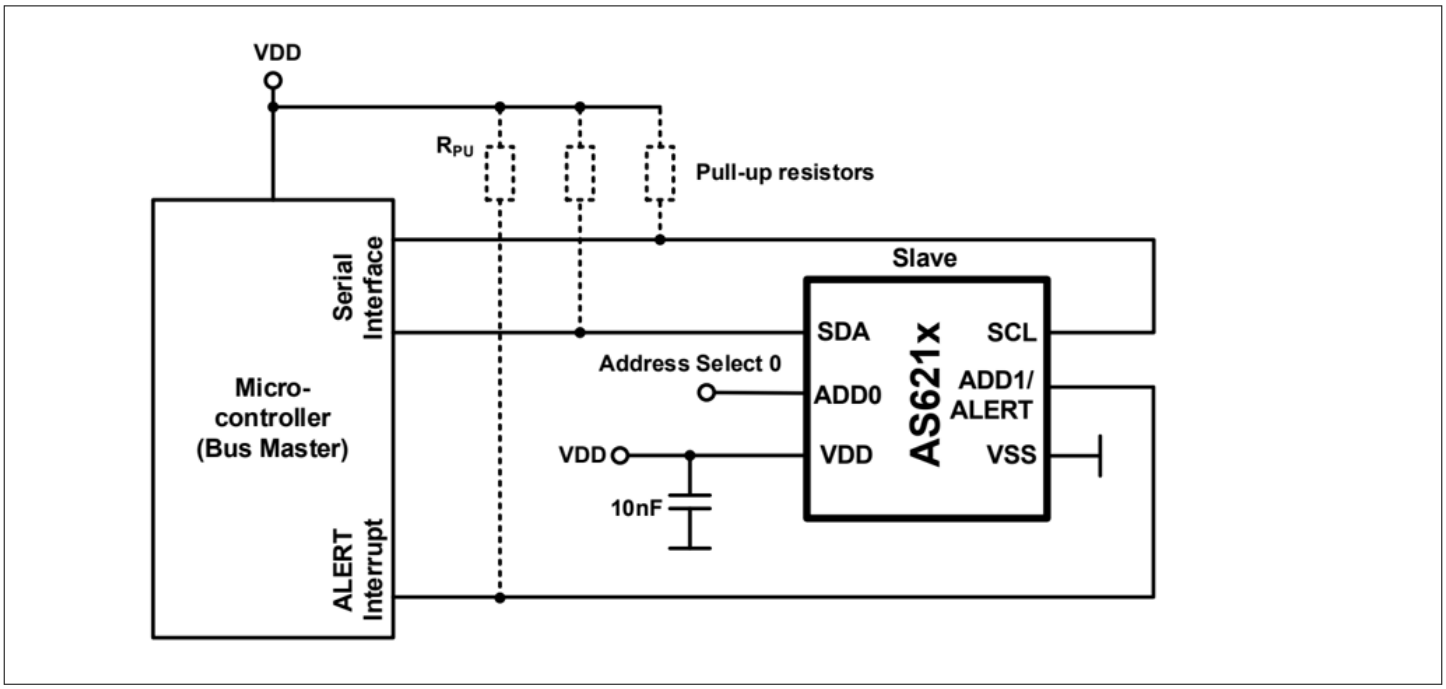


Figure 11 Application example

In Figure 11, the connections of the AS621x temperature sensor to a microcontroller and the supply voltage are shown.

The AS621x is connected to a microcontroller via an I^2C bus (SDA and SCL only). Additionally the Alert output can also be used for temperature monitoring (e.g. using the interrupt mode, refer to IM bit settings), an example is given in Figure 11 where the Alert output is connected to microcontroller.

The I^2C address of the AS621x can be selected by connecting the ADD0 and ADD1 to different pins (see Table 22). These pins must not be left unconnected.

7.1 External components

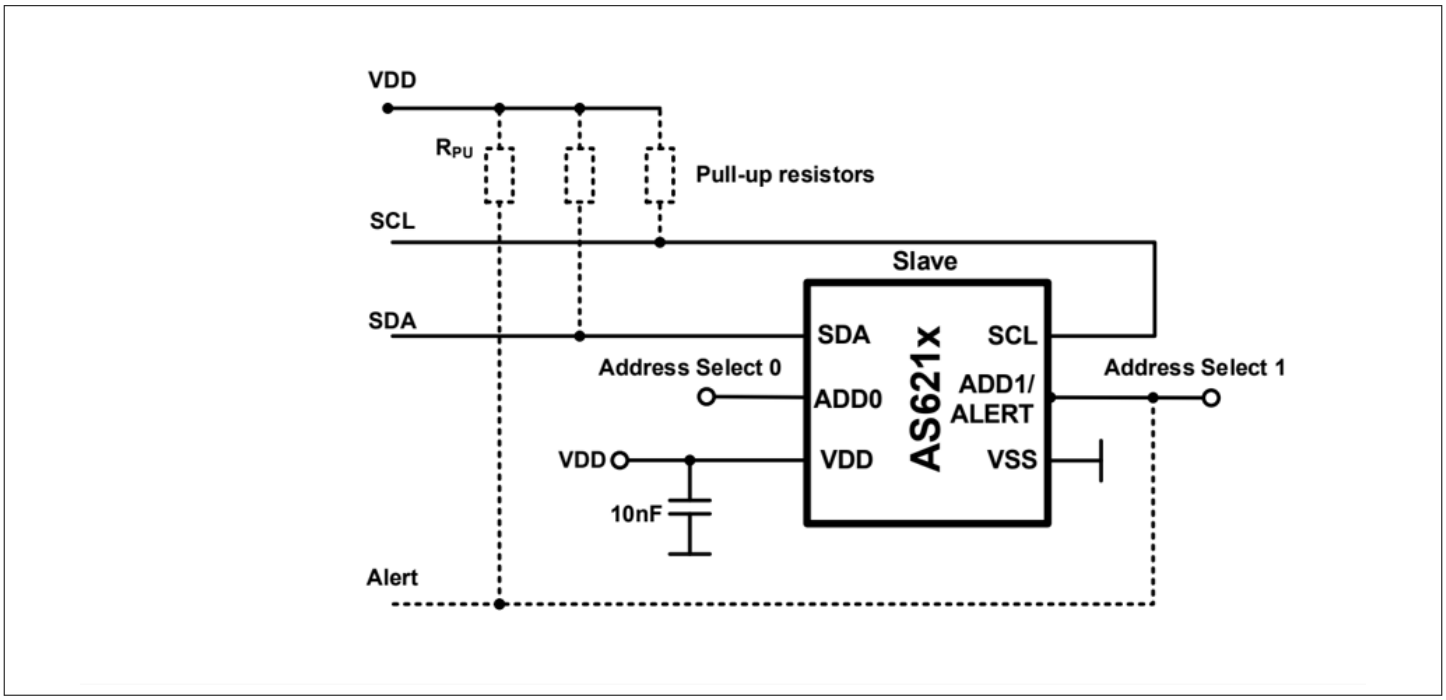


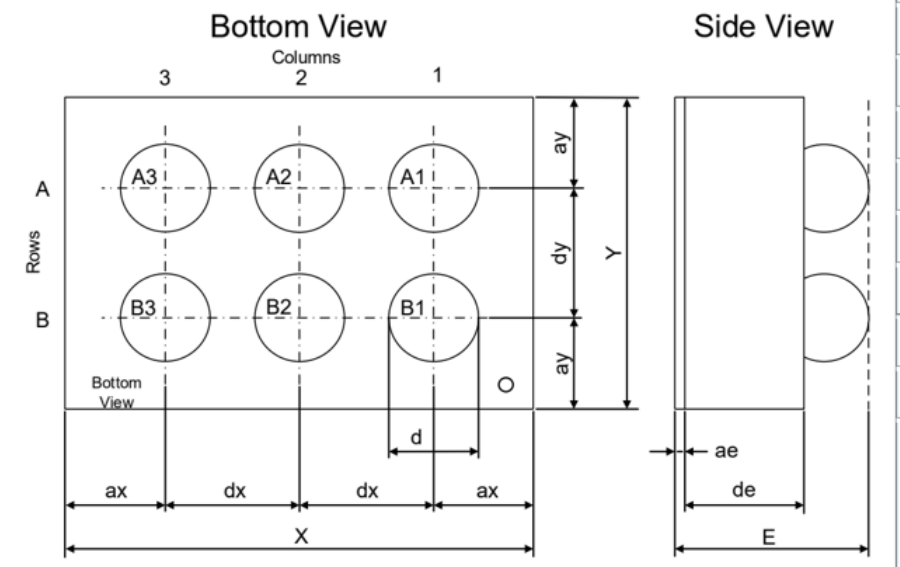
Figure 12 **Schematic with external components**

Table 25 **Values for external components**

Parameter	Min.	Typ.	Unit
Decoupling capacitor	10		nF
Pull-up resistors		10	kΩ

In Figure 12 and Table 25, the schematics and the recommended values for external components are shown.
The decoupling capacitor for the supply should have a value of at least 10 nF.
In order to use the alert functionality, the ALERT/ADD1 pin must be connected via a pull up resistor to VDD.
For the serial interface, pull up resistors to VDD are mandatory.
The pull up resistors on the serial interface and the interrupt depend on the bus capacitance and on the clock speed.

8 Package drawings & markings



Ref	Min	Nom	Max
X	1475	1490	1515
Y	1005	1025	1045
ax		347.5	
dx		400	
ay		312.5	
dy		400	
d		250	
E		600	
ae		22	
de		378	

Figure 13 WLCSP outline drawing

Note:

- *All dimensions are in micrometers. Angles in degrees.*
- *Dimensioning and tolerance conform to ASME Y14.5M-1994.*
- *This package contains no lead (Pb).*
- *This drawing is subject to change without notice.*

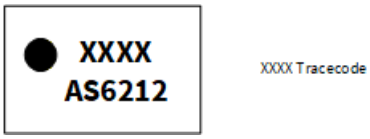


Figure 14 WLCSP package marking/code for AS6212

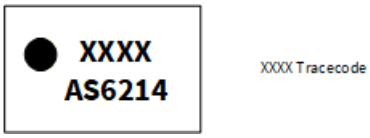


Figure 15 WLCSP package marking/code for AS6214

Figure 16 **WLCSP package marking/code for AS6218**

Revision history

Document revision	Date	Description of changes
1.00	2026-09-10	Document rebranded from ams-OSRAM to Infineon; technical specifications remain unchanged. **Legacy ams changes from previous released version to revision V6.00:** • Updated ordering information

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Edition 2026-09-10

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference
IFX-pml1787041600042

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