

XENSIV™ programmable 360° magnetic angle encoder with buffered sine and cosine output signals

Key benefits & features

The benefits and features of XENSIV™ AS5115, programmable 360° magnetic angle encoder with buffered sine and cosine output signals are listed below:

Table 1 Added value of using AS5115

Benefits	Features
Highest reliability and durability	Contactless high resolution rotational position encoding over a full turn of 360 degrees
Simple programming	Simple user-programmable over serial interface (SSI)
High precision analog output	Buffered sine and cosine output signals
Very low average power consumption	Low Power mode
Easy setup	Serial read-out of multiple interconnected devices using daisy chain mode
Fully automotive qualified	AEC-Q100, grade 0
Small form factor	SSOP 16
Robust environmental tolerance	Wide temperature range: -40°C to 150°C

Applications

The AS5115 is ideal for several automotive and industrial applications such as

- Microcontroller-based systems
- Contactless rotary position sensing
- General purpose for automotive and industrial applications

General description

The AS5115 is a contactless rotary encoder sensor for accurate angular measurement over a full turn of 360° and over an extended ambient temperature range of -40°C to 150°C.

Based on an integrated Hall element array, the angular position of a simple two-pole magnet is translated into analog output voltages. The angle information is provided by means of buffered sine and cosine voltages. This approach gives maximum flexibility in system design, as it can be directly integrated into existing architectures and optimized for various applications in terms of speed and accuracy.

An SSI Interface is implemented for signal path configuration as well as a one time programmable register block (OTP), which allows the customer to adjust the signal path gain to adjust for different mechanical constraints and magnetic field.

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1 Block diagram

The functional blocks of this device are shown below:

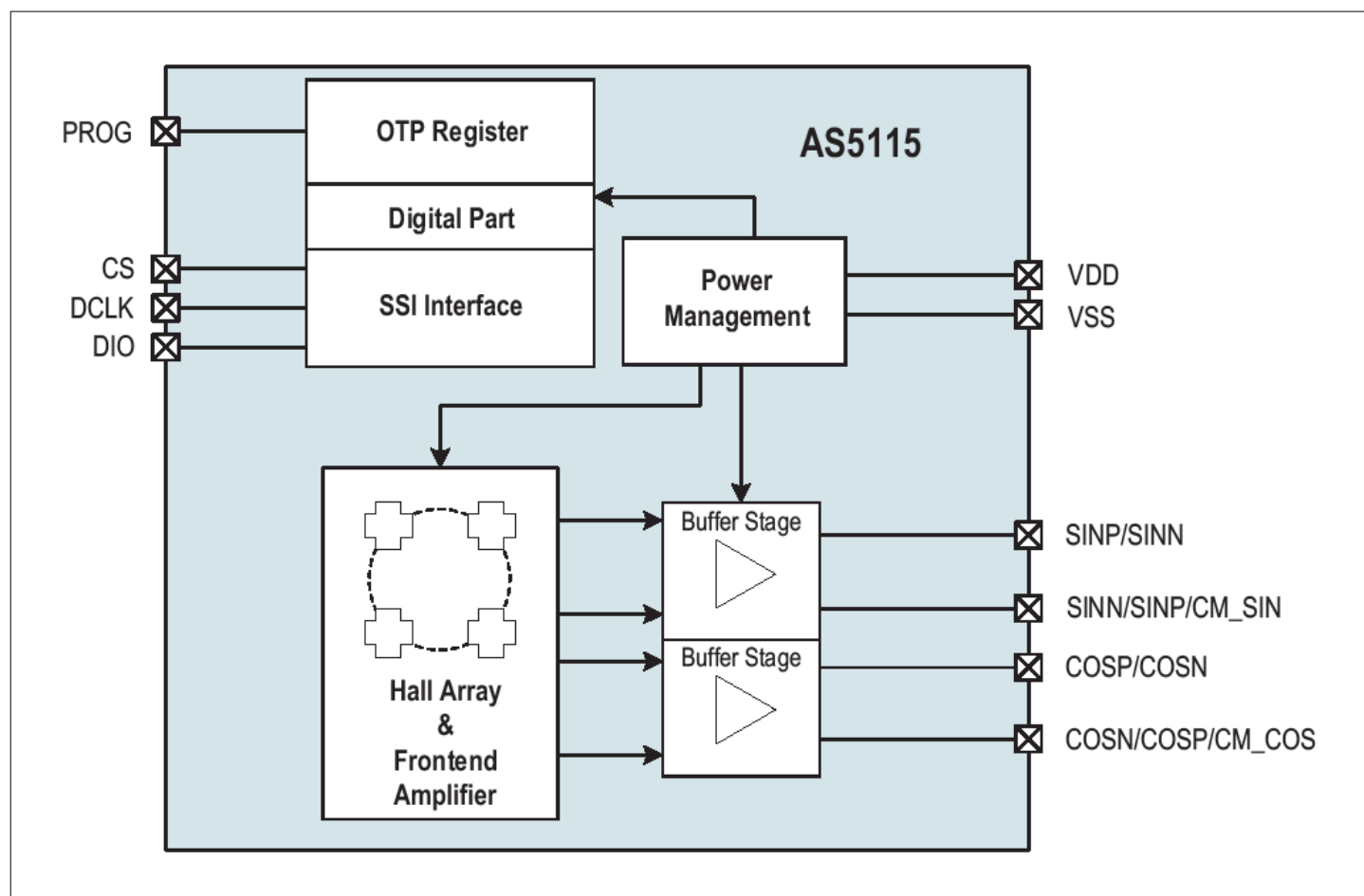


Figure 1 AS5115 block diagram

2 Pin assignments

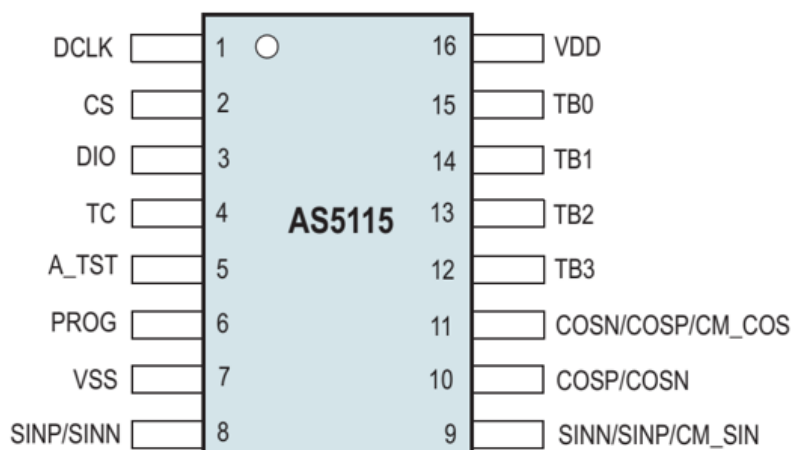


Figure 2 Pin diagram (Top view)

2.1 Pin description

Table 2 Pin description

Pin name	Pin number	Pin type	Description
DCLK	1	Digital input with Schmitt trigger	Clock input for digital interface
CS	2		Clock input for digital interface, Scan enable
DIO	3	Digital input/output	Data I/O for digital interface, Scan input
TC	4	Analog input/output	Test coil
A_TST	5	Analog output/Digital output	Analog test pin, Scan output
PROG	6	Supply pad	OTP programming pad
VSS	7		Also used as VSS of test coil + EasyZapp (double bond)
SINP/SINN	8	Analog output	Buffered analog output
SINN/SINP/CM_SIN	9		
COSP/COSN	10		
COSN/COSP/CM_COS	11		
TB3	12	Analog output/Digital input	Test bus, analog output
TB2	13		

(table continues...)

Table 2 (continued) Pin description

Pin name	Pin number	Pin type	Description
TB1	14		Test bus, analog output; external clock → sync. prod. test
TB0	15	Analog output	Test bus, analog output
VDD	16	Supply pad	Digital + analog supply

3 Absolute maximum ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under [Electrical characteristics](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3 Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Units	Comments
Electrical parameters					
V_{DD}	Supply voltage	-0.3	7	V	
V_{in}	Input pin voltage	-0.3	$V_{DD} + 0.3$	V	
I_{scr}	Input current (latchup immunity)	-100	100	mA	EIA/JESD78 Class II Level A
Electrostatic discharge					
ESD_{HBM}	Electrostatic discharge	± 2		kV	JESD22-A114E
Continuous power dissipation					
P_{tot}	Total power dissipation		275	mW	
Q_{JA}	Package thermal resistance		110	°C/W	Velocity = 0; Multi Layer PCB; Jedec Standard Testboard
Temperature ranges and storage conditions					
T_{strg}	Storage temperature	-65	150	°C	
T_{body}	Package body temperature		260	°C	IPC/JEDEC J-STD-020. The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/JEDEC J-STD-020 'Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices'. The lead finish for Pb-free leaded packages is matte tin(100% Sn).
RH_{NC}	Relative humidity non-condensing	5	85	%	
MSL	Moisture sensitivity level	3			Represents a maximum floor time of 168h

4 Electrical characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Table 4 Operating conditions

Symbol	Parameter	Conditions	Min.	Typ	Max.	Unit
V _{DD}	Positive supply voltage		4.5		5.5	V
V _{SS}	Negative supply voltage		0.0		0.0	V
T _{amb}	Ambient temperature		-40		150	°C

Table 5 DC/AC characteristics for digital inputs and outputs

Symbol	Parameter	Conditions	Min.	Typ	Max.	Unit
--------	-----------	------------	------	-----	------	------

CMOS input

V _{IH}	High level input voltage		0.7 * V _{DD}		V _{DD}	V
V _{IL}	Low level input voltage		0		0.3 * V _{DD}	V
I _{LEAK}	Input leakage current				1	µA

CMOS output

V _{OH}	High level output voltage	4mA	V _{DD} - 0.5		V _{DD}	V
V _{OL}	Low level output voltage	4mA	0		V _{SS} + 0.4	V
C _L	Capacitive load				35	pF

CMOS output tristate

I _{OZ}	Tristate leakage current				1	µA
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Table 6 Magnetic input specifications

Symbol	Parameter	Conditions	Min.	Typ	Max.	Unit
B _{Zpp}	Magnetic input field amplitude	Peak to peak at the radius (=1mm) of the hall array	32		160	mT
B _{offset}	Magnetic field offset	Within the linear range of the magnet	-10		10	mT
f _{rot}	Rotational speed	Maximum 30,000 RPM	0		500	Hz

Table 7 Electrical system specifications

Symbol	Parameter	Conditions	Min.	Typ	Max.	Unit
I _{DD}	Current consumption	Maximum value derived at maximum I _H (Hall Bias Current)			28	mA
t _{power_on}	Power up time				1.275	ms
t _{prop}	Propagation delay	-40°C to 150°C	18	22	30	µs

(table continues...)

Table 7 (continued) Electrical system specifications

Symbol	Parameter	Conditions	Min.	Typ	Max.	Unit
M	Magnetic sensitivity	Version: AS5115	10		60	mV/mT
		Version: AS5115A	20.72	28	35.28	
		Version: AS5115F	13.5	24	34.5	
V _{PP}	Analog output voltage amplitude (peak to peak)		1.38	1.94	2.5	V
AM _{Temp}	AM tracking accuracy over temperature	-40°C to 150°C	-1		1	%
AM	Sin/Cos amplitude mismatch	25°C	-2		2	%
V _{offset1}	Output DC offset voltage	At no input signal; programmable OTP setting (see Device communication/programming)	1.47	1.5	1.53	V
V _{offset2}			2.45	2.5	2.55	
DC _{offsetdrift}	DC offset drift	-40°C to 150°C	-50		50	μV/°C
V _{OUT}	Analog output range		V _{SS} + 0.25		V _{DD} - 0.5	V
I _{OUT}	Output current		-1		1	mA
C _{LOAD}	Capacitive load				1000	pF

4.1 Timing characteristics

Table 8 Timing characteristics

Symbol	Parameter	Conditions	Min.	Typ	Max.	Unit
t1_3	Chip select to positive edge of DCLK	see Figure 5 and Figure 6	30			ns
t2_3	Chip select to drive bus externally		0			ns
t3	Setup time command bit Data valid to positive edge of DCLK		30			ns
t4	Hold time command bit Data valid after positive edge of DCLK		15			ns
t5	Float time positive edge of DCLK for last command bit to bus float				$\frac{1}{(2 + 0) \cdot f_DCLK}$	ns

(table continues...)

Table 8 (continued) Timing characteristics

Symbol	Parameter	Conditions	Min.	Typ	Max.	Unit
t6	Bus driving time Positive edge of DCLK for last command bit to bus drive		$\frac{1}{(2 + 0) \cdot f_DCLK}$			ns
t7	Data valid time positive edge of DCLK to bus valid		$\frac{1}{(2 + 0) \cdot f_DCLK}$		$\frac{1}{(2 + 30) \cdot f_DCLK}$	ns
t8	Hold time data bit Data valid after positive edge of DCLK		$\frac{1}{(2 + 0) \cdot f_DCLK}$			ns
t9_3	Hold time chip select positive edge DCLK to negative edge of chip select		$\frac{1}{(2 + 0) \cdot f_DCLK}$			ns
t10_3	Bus floating time negative edge of chip select to float bus				30	ns
t11	Setup time data bit at write access Data valid to positive edge of DCLK		30			ns
t12	Hold time data bit at write access Data valid after positive edge of DCLK		15			ns
t13_3	Bus floating time negative edge of chip select to float bus		-		30	ns

Note: The digital interface will be reset during the low phase of the CS signal.

5 Detailed description

5.1 Sleep mode

The target is to provide the possibility to reduce the total current consumption. No output signal will be provided when the IC is in sleep mode. Enabling or disabling sleep mode is done by sending the SLEEP or WAKEUP commands via the SSI interface. Analog blocks are powered down with respect to fast wake up time.

5.2 SSI interface

The setup for the device is handled by the digital interface. Each communication starts with the rising edge of the chip select signal. The synchronization between the internal free running analog clock oscillator and the external used digital clock source for the digital interface is done in a way that the digital clock frequency can vary in a wide range.

Table 9 SSI interface pin description

Port	Symbol	Function
Chip select	CS	Indicates the start of a new access cycle to the device. CS = LO → reset of the digital interface
DCLK	DCLK	Clock source for the communication over the digital interface.
Bidirectional data input output	DIO	Command and data information over one single line. The first bit of the command defines a read or write access.

Table 10 SSI interface parameter description

Symbol	Parameter	Notes	Min.	Typ	Max.	Unit
f_DCLK	Clock frequency at normal operation	The nominal value for the clock frequency can be derived from a 10MHz oscillator source.	No limit	5	6	MHz
f_EZ_RW	Clock frequency at easy zap read write access		No limit	5	6	kHz
f_EZ_PROG	Clock frequency at easy zap accessprogram OTP	Correct access to the programmable zener diode block needs a strict timing - the zappulse is exact one period. The nominal value for the clock frequency can be derived from a 10MHz oscillator source.	200		650	kHz
f_EZ_ARB	Clock frequency at easy zap analog readback	20pF external load allowed. The nominal value for the clock frequency can be derived from a 10MHz oscillator source.	No limit	156.3	162.5	kHz

Parameter	Notes
Interface general at normal mode	
Protocol: 5 command bit + 16 data input output	
Command	5-bit command: cmd<4:0> ← bit<21:16>
Data	16-bit data: data<15:0> ← bit<15:0>

Parameter	Notes
Interface general at extended mode	
Protocol: 5 command bit + 46 data input output	
Command	5-bit command: cmd<4:0> ← bit<50:46>
Data	34-bit data: data<45:0> ← bit<45:0>
Interface modes	
Normal read operation mode	cmd<4:0> = <00xxx> → 1 DCLK per data bit
Extended read operation mode	cmd<4:0> = <01xxx> → 4 DCLK per data bit
Normal write operation mode	cmd<4:0> = <10xxx> → 1 DCLK per data bit
Extended write operation mode	cmd<4:0> = <11xxx> → 4 DCLK per data bit

5.3 Device communication/programming

Table 11 Digital interface at normal mode

#	Command	Bin	Mode	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
23	WRITE_CONFIG	10111	write	go2sleep	gen_rst					analog_sig	OB_bypassed								
16	EN_PROG	10000	write	1	0	0	0	1	1	0	0	1	0	1	0	1	1	1	0

Name	Functionality
go2sleep	Enter/leave low power mode (no output signals)
gen_rst	Generates global reset
analog_sig	Switches the channels to the test bus after the PGA
OB_bypassed	Disable and bypass output buffer for testing purpose

Table 12 Digital interface at extended mode

#	Command	Bin	Mode	Factory settings								User settings					
				<45:44>	<43:26>	<25:23>	<22:20>	<19:18>	<17:14>	<13:3>	<12:2>	<11>	<10>	<9>	<8:7>	<6>	<5:0>
31	WRITE_OTP	11111	xtwrite	r	r	r	r	r	r	r	r	invert_channel	cm_sin	cm_cos	gain	dc_offset	hall_bias
25	PROG_OTP	11001	xtwrite	r	r	r	r	r	r	r	r	invert_channel	cm_sin	cm_cos	gain	dc_offset	hall_bias

(table continues...)

Table 12 (continued) Digital interface at extended mode

#	Command	Bin	Mode	Factory settings								User settings					
				<45: 44 >	<43: 26 >	<25: 23 >	<22: 20 >	<19: 18 >	<17: 14 >	<1 3>	<1 2>	<11>	<10>	<9>	<8:7 >	<6>	<5:0 >
15	RD_OTP	011 11	xt read	r	r	r	r	r	r	r	r	invert_ channel	cm_ sin	cm_ cos	gain	dc_ offset	hall_ bias
9	RD_OTP _ANA	010 01	xt read														l

Notes:

1. 'r' stands for reserved bits. They must not be modified, unless otherwise noted
2. Send EN PROG (command 16) in normal mode before accessing the OTP in extended mode
3. OTP assignment will be defined/updated

Table 13 User settings description

Name	Functionality
invert_channel Inverts	SIN and COS channel before the PGA for inverted output function (0 → SIN/COS, 1 → SINN/COSN)
cm_sin	Common mode voltage output enabled at SINN/CM pin (0 → differential, 1 → common)
cm_cos	Common mode voltage output enabled at COSN/CM pin (0 → differential, 1 → common)
gain	PGA gain setting (influences overall magnetic sensitivity), 2-bit
dc_offset	Output DC bias offset (0 → Voffset1=1.5V, 1 → Voffset2=2.5V)
Hall_b	Hall bias setting (influences overall magnetic sensitivity), 6-bit

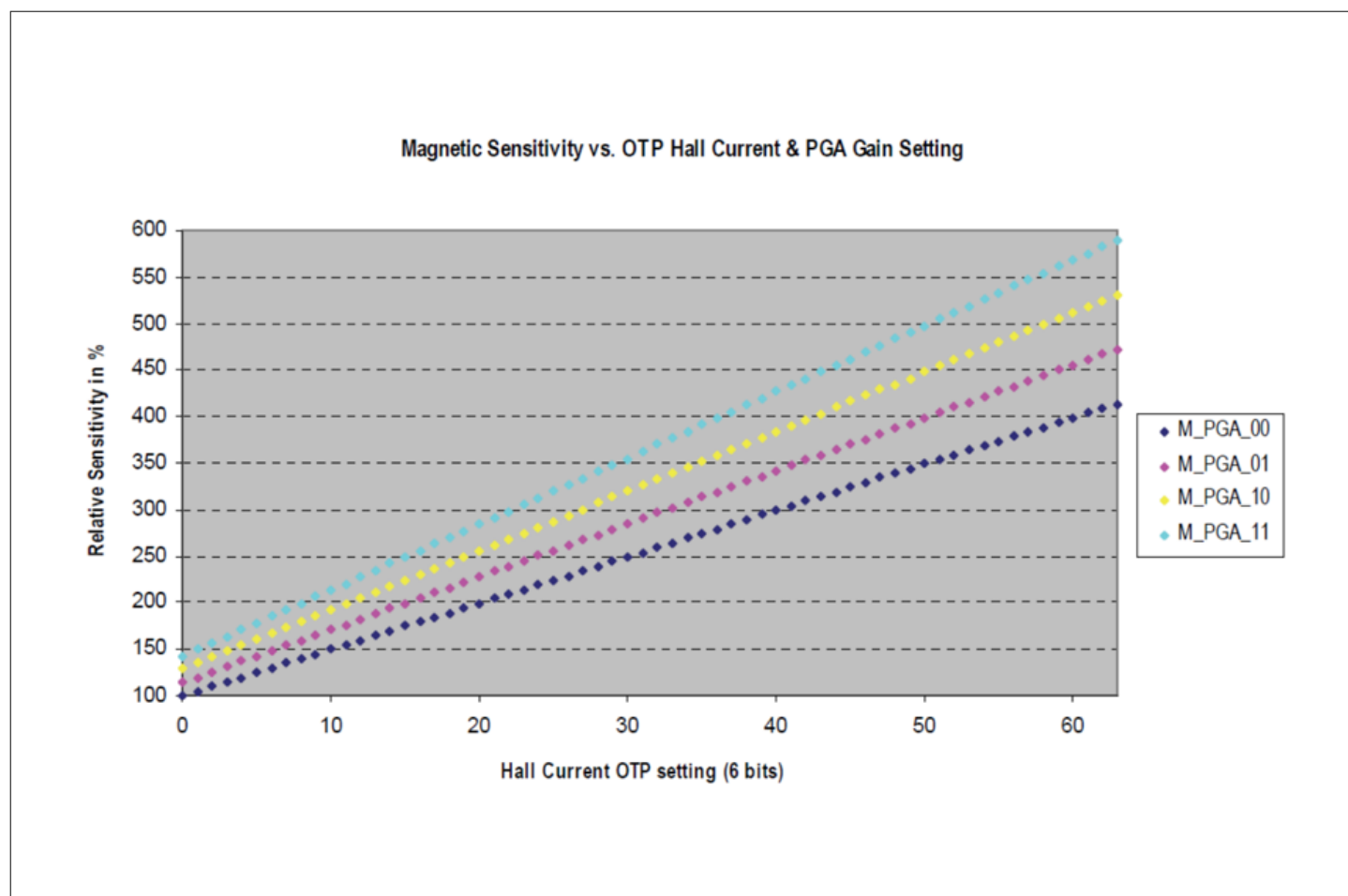


Figure 3 Sensitivity gain settings - Relative sensitivity in %

The amplitude of the output signal is programmable via sensitivity (6bit) and/or gain (2bit) settings (see [Figure 3](#)).

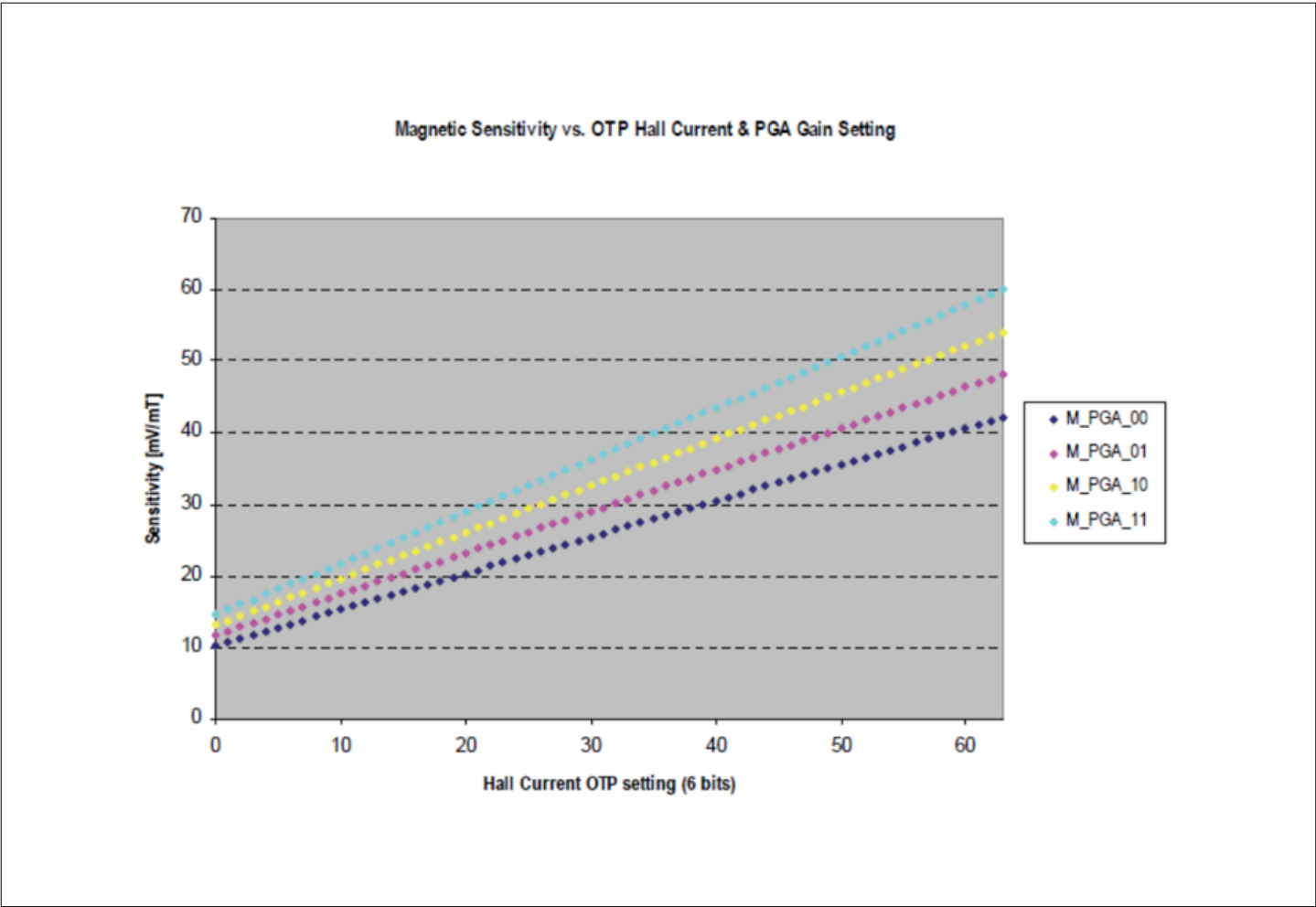


Figure 4 Sensitivity gain settings - Sensitivity [mV/mT]

5.4 Waveform – Digital interface at normal operation mode

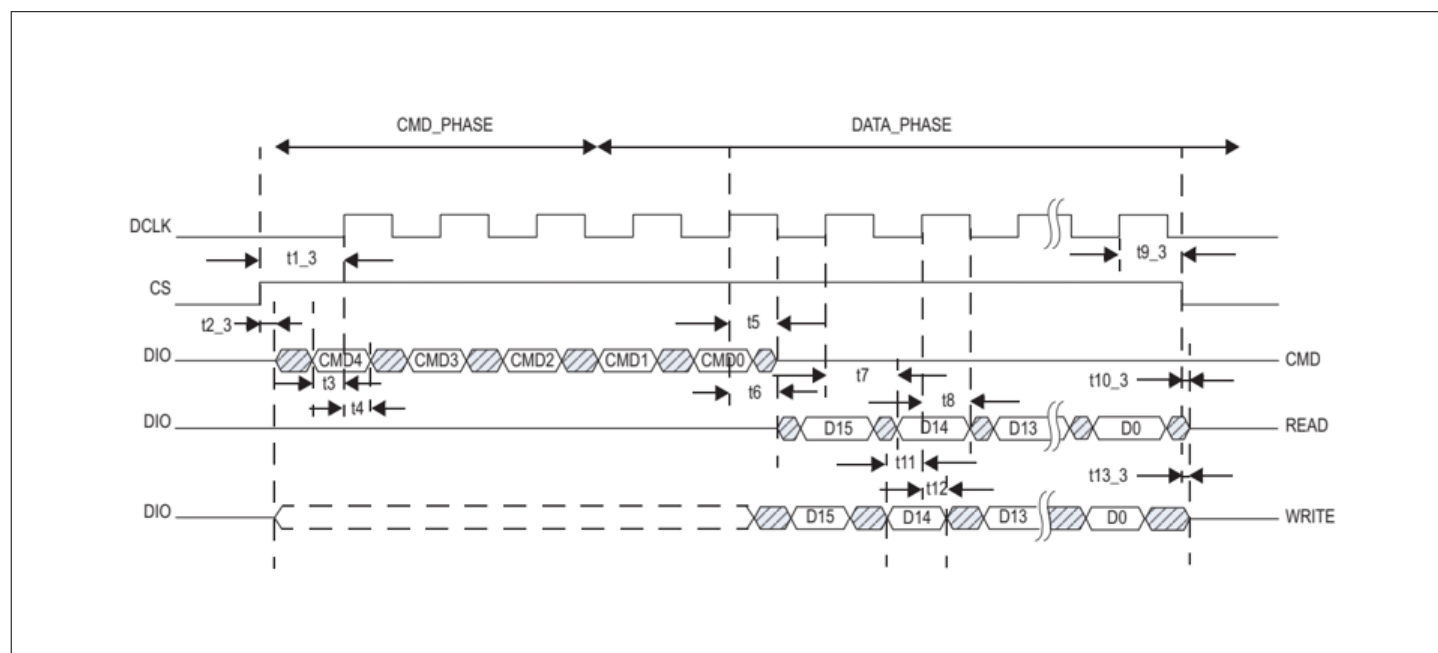


Figure 5 Digital interface at normal operation mode

5.5 Waveform – Digital interface at extended mode

In the extended mode, the digital interface needs four clocks for one data bit due to the internal structure. During this time, the device is able to handle internal signals for special access (e.g. the easy zap interface).

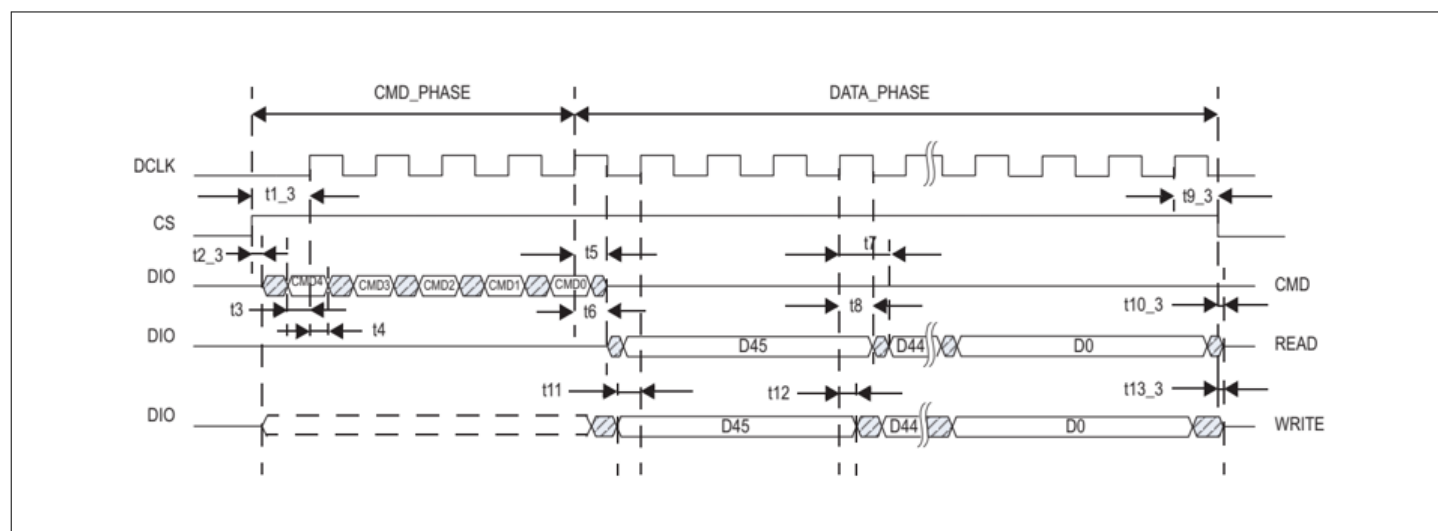


Figure 6 Digital interface at extended mode

5.6 Waveform – Digital interface at analog readback of the Zener diodes

To be sure that all Zener-Diodes are correctly burned, an analog readback mechanism is defined. Perform the 'READ OTP ANA' sequence according to the command table and measure the value of the diode at the end of each phase.

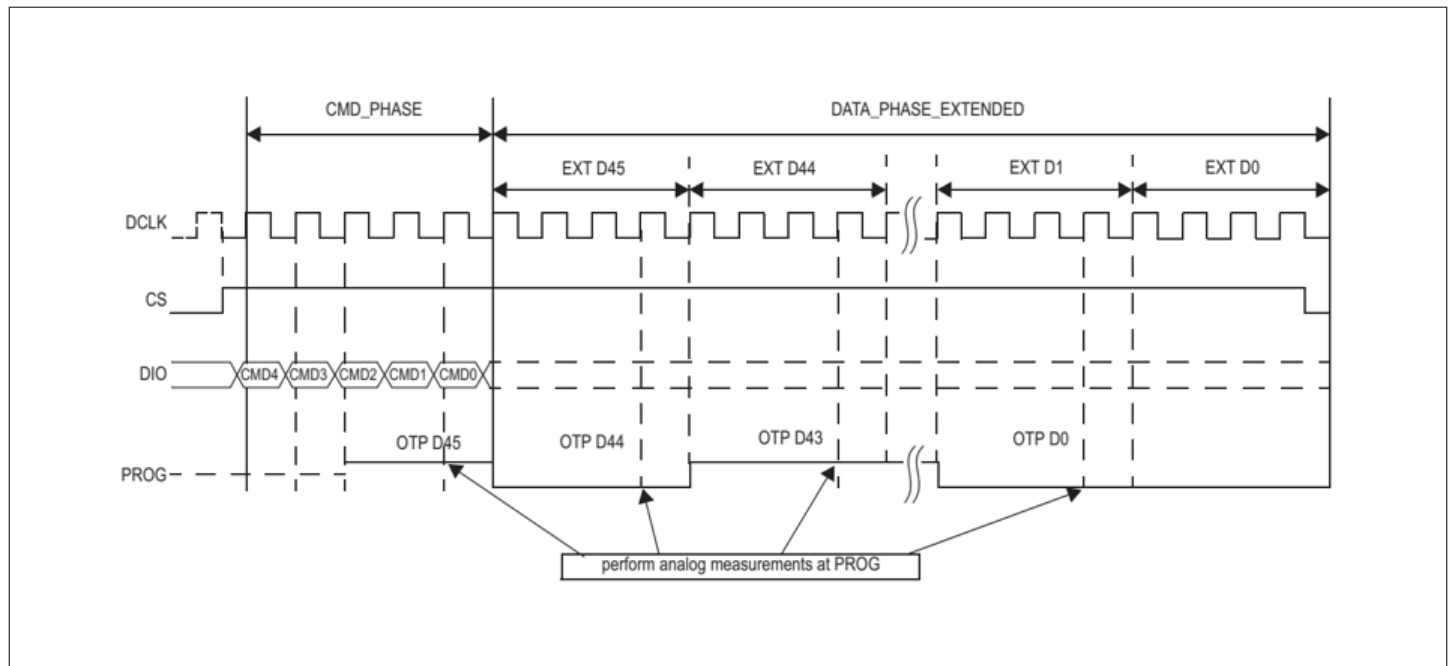


Figure 7 Digital interface at analog readback of Zener diodes

Table 14 Serial bit sequence (16-Bit Read/ Write)

Write command					Read/Write data															
C4	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

5.7 One time programming content

The AS5115 die has an integrated 46-bit OTP ROM (Easyzap) for trimming and configuration purposes. The PROM can be programmed via the serial interface. For irreversible programming, an external programming voltage at PROG pin is needed. For security reasons, the factory trim bits can be locked by a lock bit.

As shown in the figure below, the OTP holds 46 bits. Bit number 44 and 45 are used for OTP testing purposes and ESD protection of the remaining cells.

Name	Bit count	OTP start	OTP end	Access	Comments
Hall_b	6	0	5	User	Sets overall sensitivity
dc_offset	1	6	6	User	Output DC offset setting
gain	2	7	8	User	Output Buffer Gain setting
Lock	1	13	13	Infineon	Set in production test
invert_channel	1	11	11	User	Inverts SIN and COS channel before the PGA for inverted output function
cm_sin	1	10	10	User	Common mode voltage output enabled at SINN/CM pin
cm_cos	1	9	9	User	Common mode voltage output enabled at COSN/CM pin

Note: OTP assignment will be defined/updated.

5.8 Analog Sin/Cos outputs with external interpolator

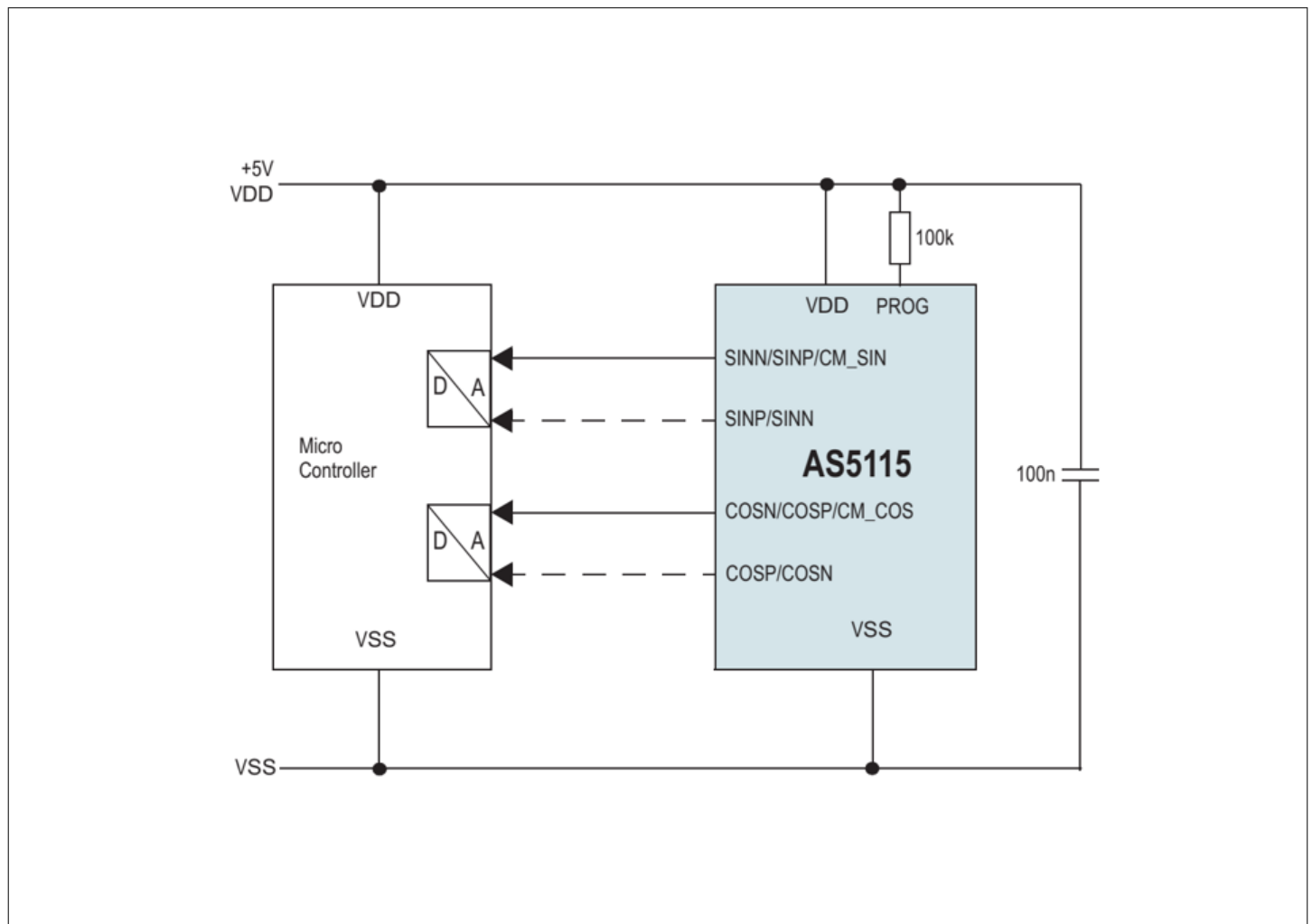


Figure 8 Sine and cosine outputs for external angle calculation

Notes:

1. It is recommended to use a 100k pull-up resistance
2. Default conditions for unused pins are: DCLK, CS, DIO, TC, A_TST, TBO, TB1, TB2, TB3 connect to VSS

The AS5115 provides analog sine and cosine outputs (SINP, COSP) of the Hall array front-end for test purposes. These outputs allow the user to perform the angle calculation by an external ADC + μ C, e.g. to compute the angle with a high resolution. The signal lines must be kept as short as possible. In the case of longer lines, they must be shielded in order to achieve best noise performance.

Through the programming of one bit, you have the possibility to choose between the analog sine and cosine outputs (SINP, COSP) and their inverted signals (SINN, COSN). Furthermore, by programming the bits <9:10> you can enable the common mode output signals of SIN and COS.

5.9 OTP programming and verification

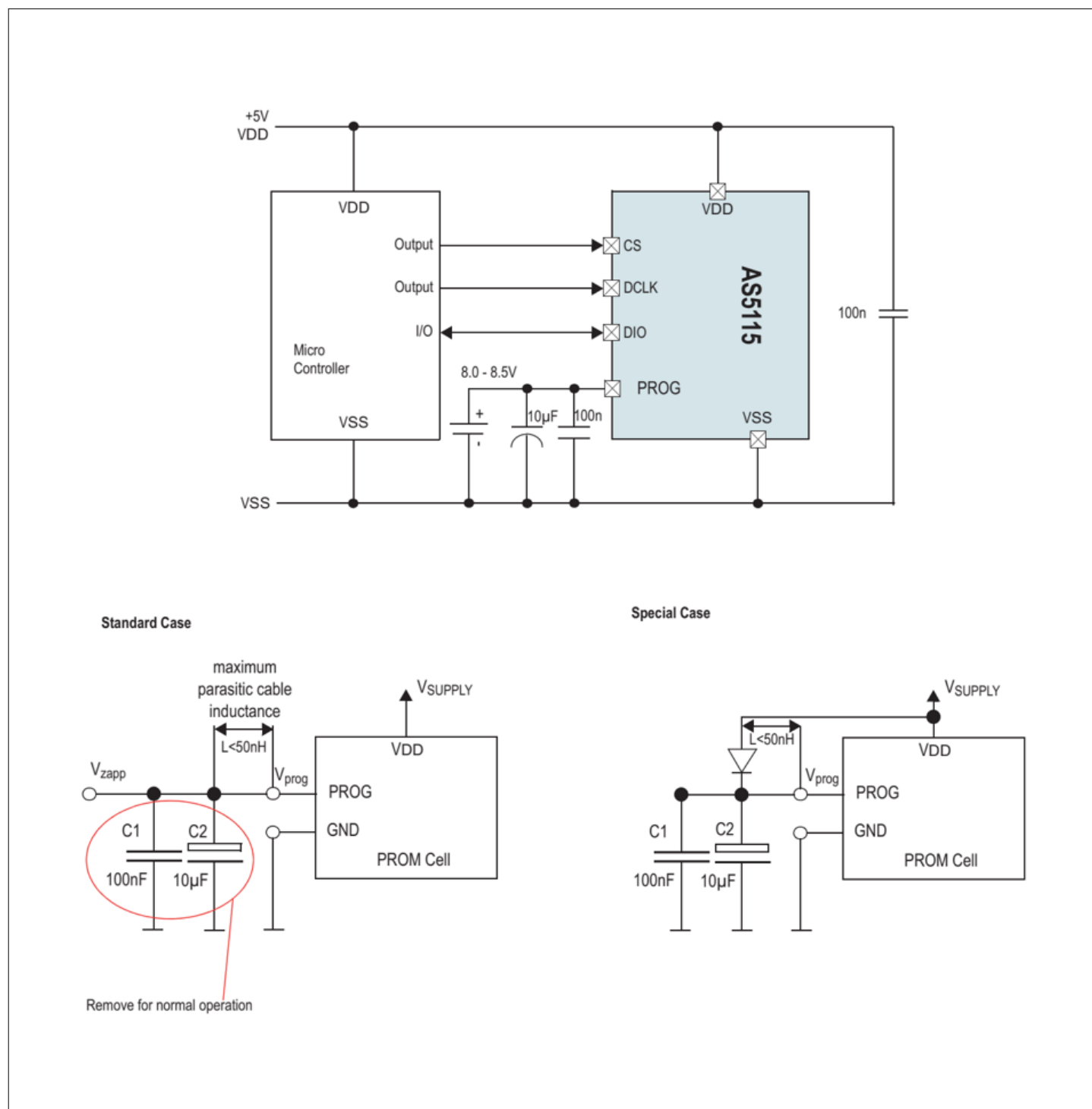


Figure 9 OTP programming connection

Notes:

1. The maximum capacitive load at PROG in normal operation should be less than 20pF. However, during programming the capacitors C1+C2 are needed to buffer the programming voltage during current spikes, but they must be removed for normal operation. To overcome this contradiction, the recommendation is to add a diode (4148 or similar) between PROG and VDD as shown in Figure 9 (special case setup), if the capacitors can not be removed at final assembly.

Due to D1, the capacitors C1+C2 are loaded with VDD - 0.7V at startup, hence not influencing the readout of the internal OTP registers.

During programming the OTP, the diode ensures that no current is flowing from PROG (8V - 8.5V) to VDD (5V). In the standard case (see Figure 9), the verification of a correct OTP readout can be done by analog readback of the OTP register.

As long as the PROG pin is accessible it is recommended to use standard setup. In case the PROG pin is not accessible at final assembly, the special setup is recommended.

For programming of the OTP, an additional voltage has to be applied to the pin PROG. It has to be buffered by a fast 100nF capacitor (ceramic) and a 10μF capacitor. The information to be programmed is set by command 25. The OTP bits 16 until 45 are used for Infineon factory trimming and cannot be overwritten.

Table 15 **OTP programming parameters**

Symbol	Parameter	Min.	Max.	Unit	Note
V _{DD}	Supply Voltage	5	5.5	V	
GND	Ground Level	0	0	V	
V _{zapp}	Programming Voltage	8	8.5	V	At pin PROG
T _{zapp}	Temperature	0	85	°C	
f _{clk}	CLK Frequency		100	kHz	At pin DCLK

After programming, the programmed OTP bits have to be verified by Analog Verification:

By switching into Extended Mode and sending an ANALOG OTP READ command (#9), pin PROG becomes an output, sending an analog voltage with each clock representing a sequence of the bits in the OTP register (starting with D45). A voltage of <500mV indicates a correctly programmed bit ("1") while a voltage level between 2V and 3.5V indicates a correctly unprogrammed bit ("0"). Any voltage level in between indicates incorrect programming.

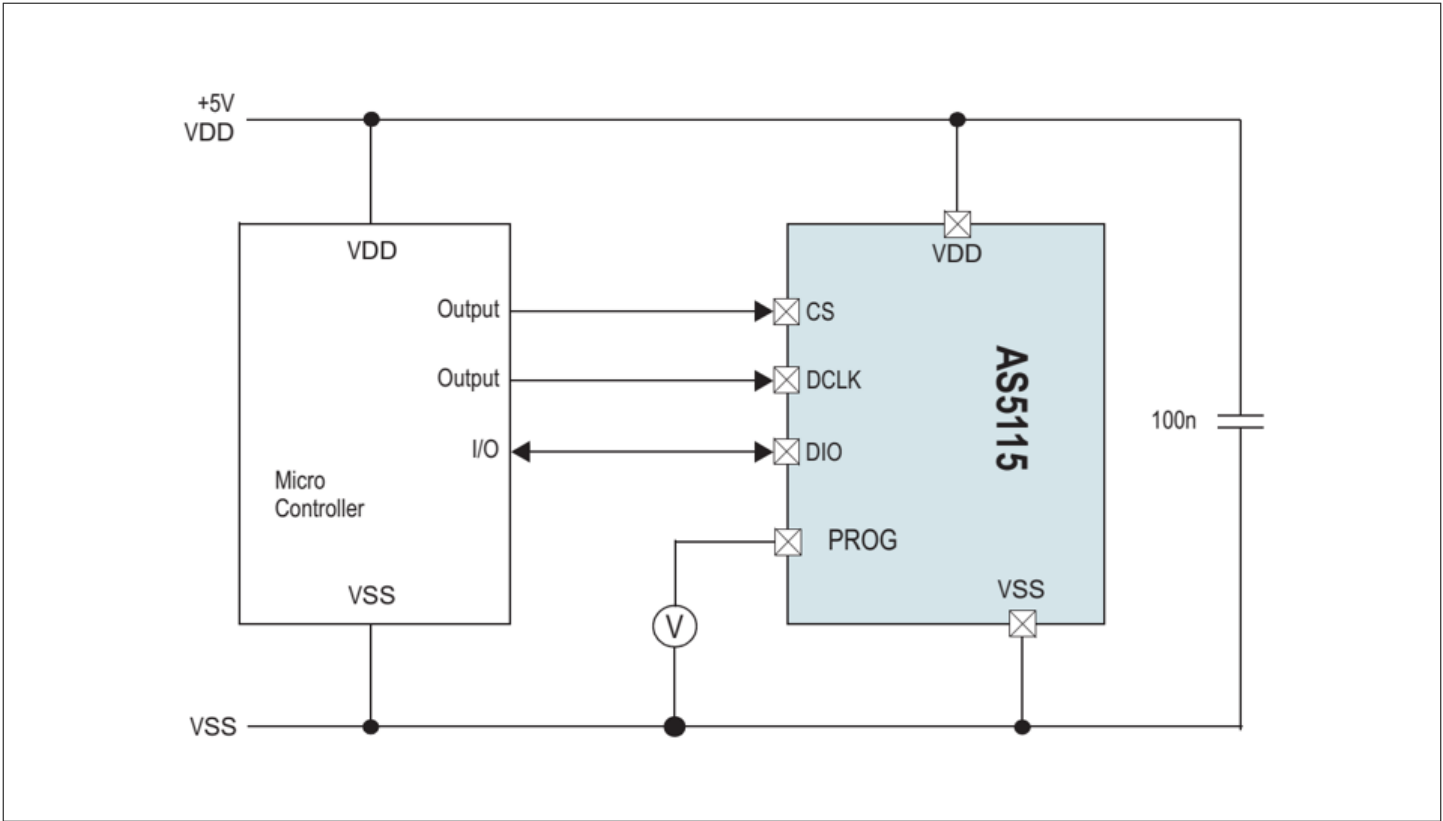


Figure 10 Analog OTP verification

5.10 Pre-programmed version

Table 16 Pre-programmed version

Version	Sensitivity	Output	Output DC offset	PGA gain setting	Hall bias current
AS5115	Not programmed	1.5V	0	Not programmed	Untrimmed
AS5115A	28 mV/mT	2.5V	1	00	14µA
AS5115F	24 mV/mT	1.5V	0	11	8.42µA (trim code 10hex fixed)

6 Application information

6.1 Mechanical data

The internal Hall elements are placed in the center of the package on a circle with a radius of 1 mm.

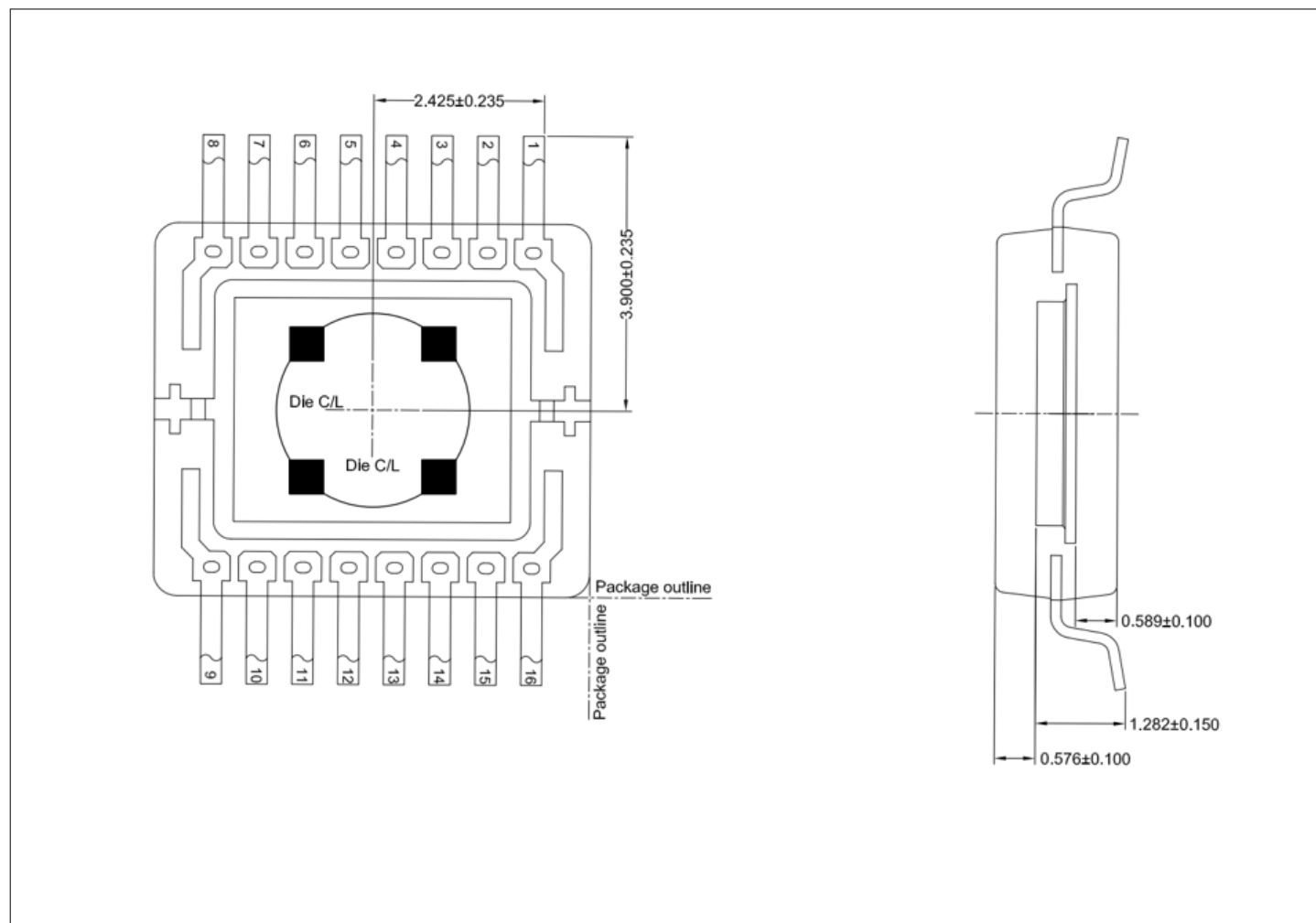


Figure 11 Hall element position

Notes:

1. All dimensions in mm
2. Die thickness $381 \mu\text{m}$
3. Adhesive thickness $30 \pm 15 \mu\text{m}$
4. Leadframe downset $200 \pm 38 \mu\text{m}$
5. Leadframe thickness $152 \pm 8 \mu\text{m}$

7 Package drawings & markings

The devices are available in a 16-lead shrink small outline package.

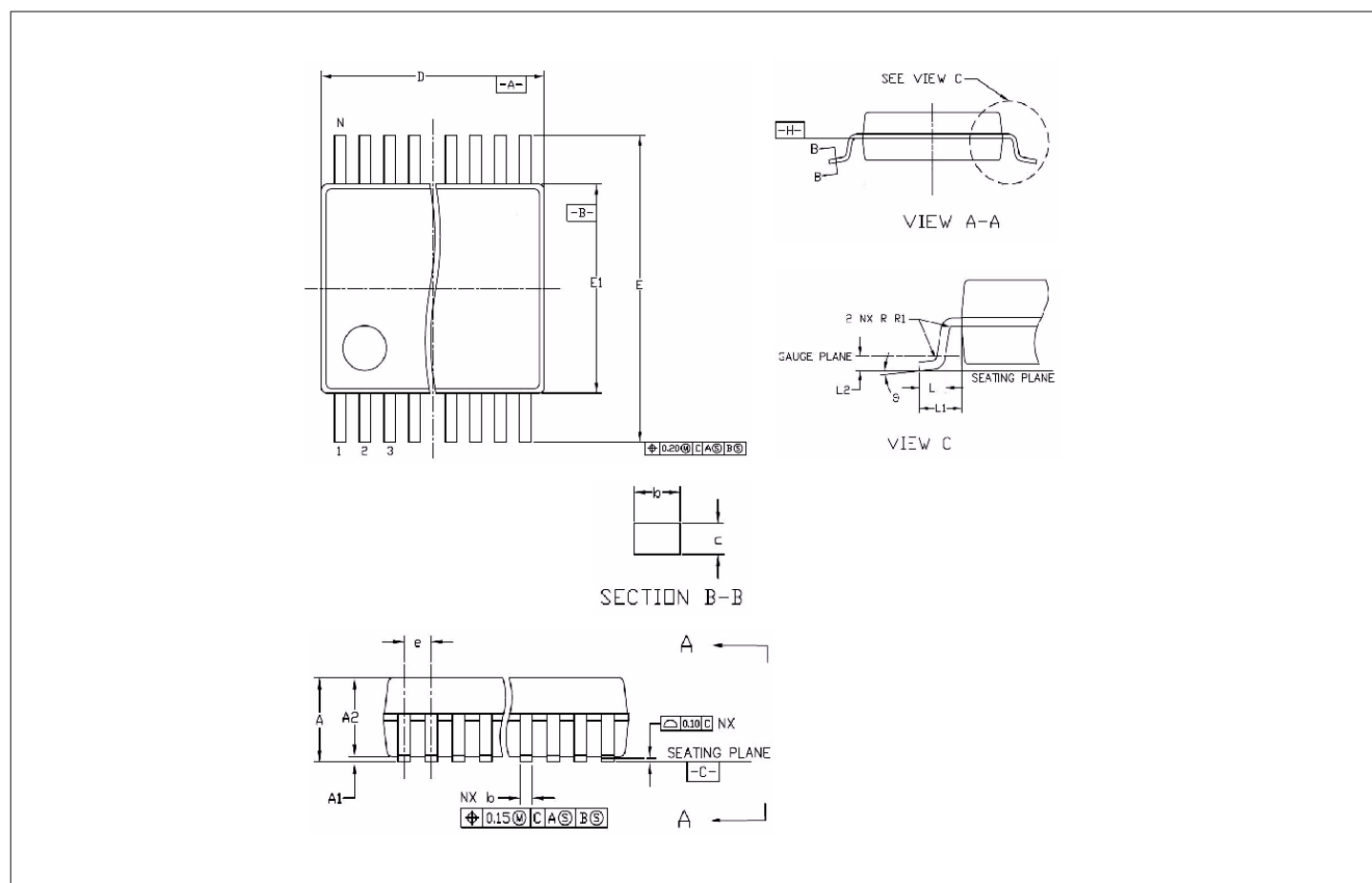


Figure 12 Package drawings and dimensions

Symbol	Min.	Nom	Max.
A	1.73	1.86	1.99
A1	0.05	0.13	0.21
A2	1.68	1.73	1.78
b	0.22	0.3	0.38
c	0.09	0.17	0.25
D	5.9	6.2	6.5
E	7.4	7.8	8.2
E1	5	5.3	5.6
e	-	0.65BSC	-
L	0.55	0.75	0.95
L1	-	1.25REF	-
L2	-	0.25BSC	-
R	0.09	-	-
Θ	0°	4°	8°
N	16		

Figure 13 **Package dimensions**

Notes:

1. Dimensions and toleranceing conform to ASME Y14.5M-1994
2. All dimensions are in millimeters. Angles are in degrees

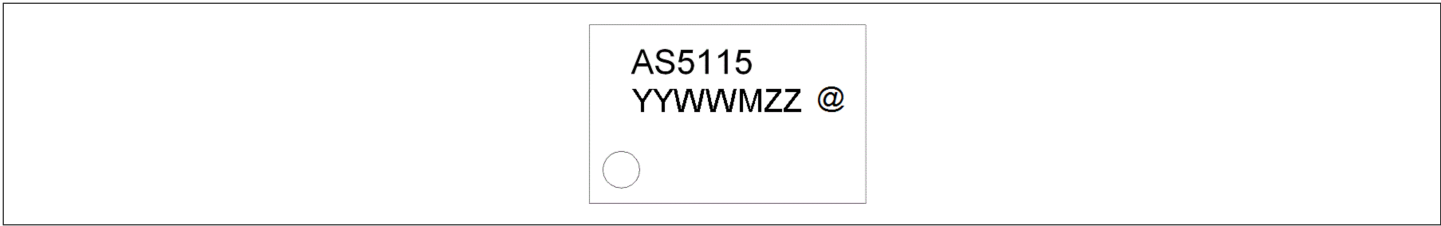


Figure 14 AS5115 marking



Figure 15 AS5115A marking



Figure 16 AS5115F marking

Table 17 AS5115/AS5115A package code

YY	WW	M	ZZ	@
Last two digits of the manufacturing year	Manufacturing week	Plant identifier	Assembly traceability code	Sublot identifier

Table 18 AS5115F package code

XXXXX
Tracecode

8 Ordering information

The devices are available as the standard products shown in [Table 19](#).

Table 19 **Ordering information**

Product type (Infineon)	Product type (ams)	Package	Marking	Ordering code	Delivery form	Delivery quantity
AS5115-HSST-SSOP16	AS5115-HSST	SSOP-16	AS5115	SP006309761	13" Tape & Reel in dry pack	2000 pcs/reel
AS5115-HSSM-SSOP16	AS5115-HSSM	SSOP-16	AS5115	SP006309765	7" Tape & Reel in dry pack	500 pcs/reel
AS5115A-HSSP-SSOP16	AS5115A-HSSP	SSOP-16	AS5115A	SP006309767	13" Tape & Reel in dry pack	2000 pcs/reel
AS5115A-HSSM-SSOP16	AS5115A-HSSM	SSOP-16	AS5115A	SP006309769	7" Tape & Reel in dry pack	500 pcs/reel
AS5115F-HSSP-SSOP16	AS5115F-HSSP	SSOP-16	AS5115F	SP006309779	13" Tape & Reel in dry pack	2000 pcs/reel

9 Revision history

Document revision	Date	Description of changes
1.00	2026-09-30	Document rebranded from ams-OSRAM to Infineon; technical specifications remain unchanged. Changes from previous released version to revision v16-00 • Updated Figure 5 • Updated text under Figure 25 • Updated Figure 27

Trademarks

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