XENSIV™ high-resolution on-axis magnetic angular position sensor

Key benefits and features

The benefits and features of XENSIV™ AS5070, high-resolution on-axis magnetic angular position sensor are listed below:

Table 1 Added value of using AS5070

Benefits	Features
Resolve small angular excursion with high accuracy	12-bit resolution @ 90° minimum arc
Accurate angle measurement	Low output noise, low inherent INL
Higher durability and lower system costs (no shield needed)	Magnetic stray field immunity

Applications

The AS5070 is ideal for applications like:

- Rotary button angle sensors
- Liquid-level measurement systems
- Contactless potentiometers

General description

The AS5070 is a high-resolution angular position sensor for precise absolute angle measurement. The AS5070 is available with an analog output interface (AS5070A) or a digital output interface (AS5070B). The latter can be programmed as a PWM or a SENT-compliant output interface.

Based on a Hall sensor technology, this device measures the orthogonal component of the flux density (Bz) over a full-turn rotation and compensates for external stray magnetic fields with a robust architecture based on a 14-bit sensor array and analog front-end (AFE). A sub-range can be programmed to achieve the best resolution for the application. To measure the angle, only a simple two-pole magnet rotating over the center of the package is required. The magnet may be placed above or below the device. The absolute angle measurement provides an instant indication of the magnet's angular position. The AS5070 operates at a supply voltage of 5 V, and the supply and output pins are protected against overvoltage up to +20 V. In addition the supply pins are protected against reverse polarity up to -20 V. The following figure shows the typical arrangement of AS5070 and a magnet.

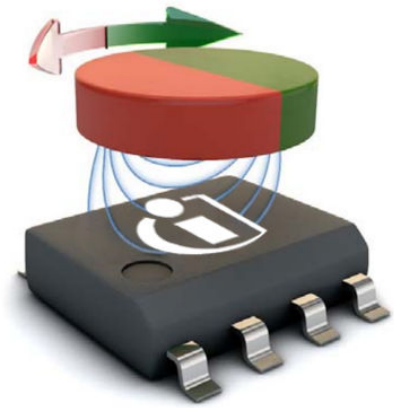


Table of contents

Key benefits and features . . . 1
Applications . . . 1
General description . . . 1
Table of contents . . . 2
1 Block diagram . . . 4
2 Pin assignments . . . 5
3 Absolute maximum ratings . . . 6
4 Electrical characteristics . . . 7
4.1 Timing characteristics . . . 11
5 Detailed description . . . 12
6 Register description . . . 13
6.1 UART interface . . . 15
6.2 Exiting communication mode . . . 16
6.3 Burning the OTP registers . . . 16
6.4 Customer ID . . . 16
6.5 Output linear transfer function . . . 16
6.5.1 Multiple quadrants . . . 19
6.6 Extended magnetic input range . . . 21
6.6.1 Analog output (AS5070A) . . . 21
6.6.2 PWM output (AS5070B) . . . 21
6.6.3 SENT output (AS5070B) . . . 22
6.7 Diagnostics . . . 25
6.7.1 Analog read fail (SM11) . . . 26
6.7.2 Digital readout . . . 26
6.7.3 Analog readout . . . 27
7 Application information . . . 28
7.1 Signature calculation . . . 28
7.2 Programming parameter . . . 28
7.3 Burn and verification of the OTP memory . . . 28
7.4 SOIC8 . . . 31
7.5 External components . . . 32
7.6 Mechanical data . . . 34
8 Package drawings & markings . . . 35
9 Ordering information . . . 37
Revision history . . . 38

Disclaimer 39

1 Block diagram

The functional blocks of the AS5070A, AS5070B are shown in Figure 1 and Figure 2:

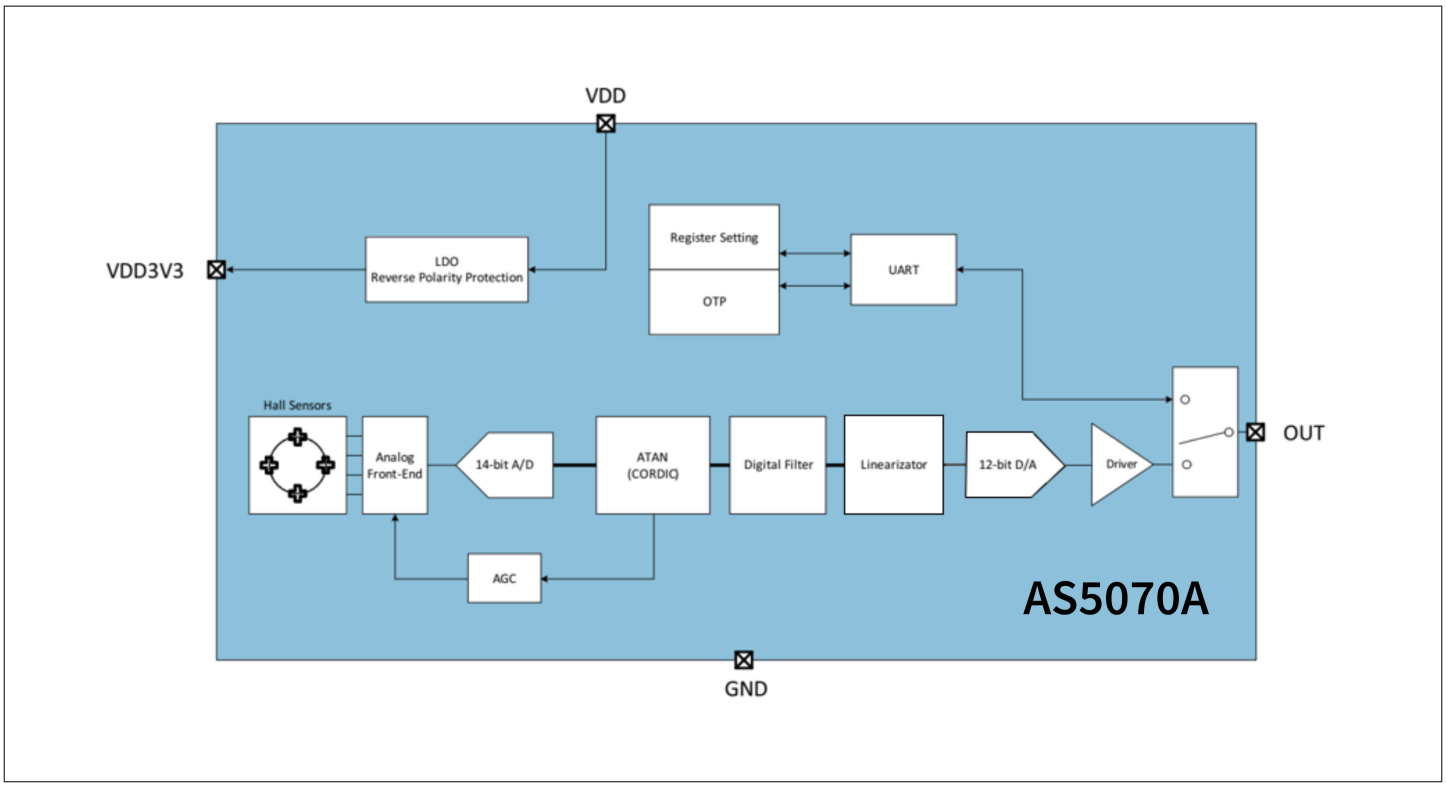


Figure 1 Functional blocks of the AS5070A

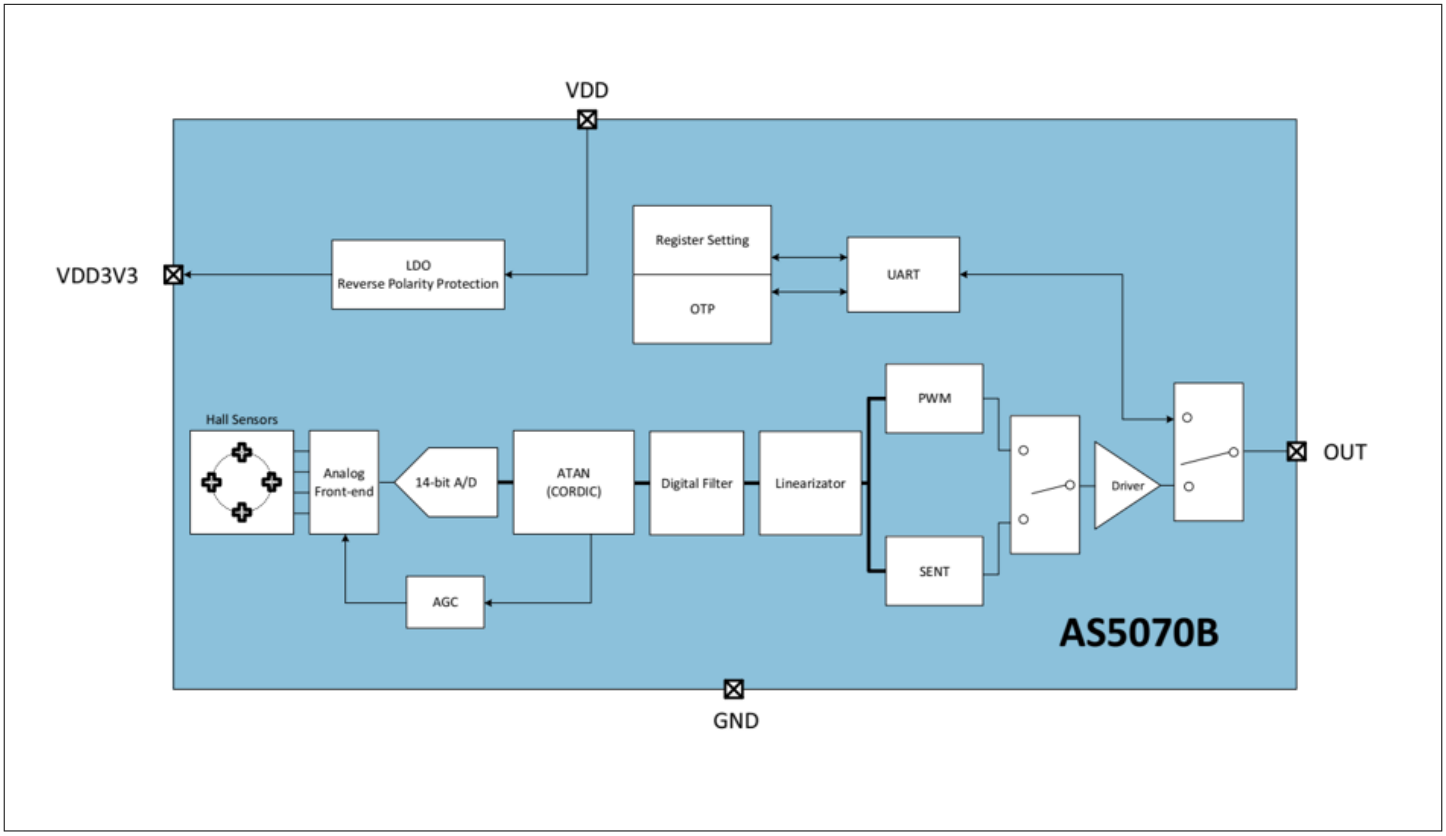


Figure 2 Functional blocks of the AS5070B

2 Pin assignments

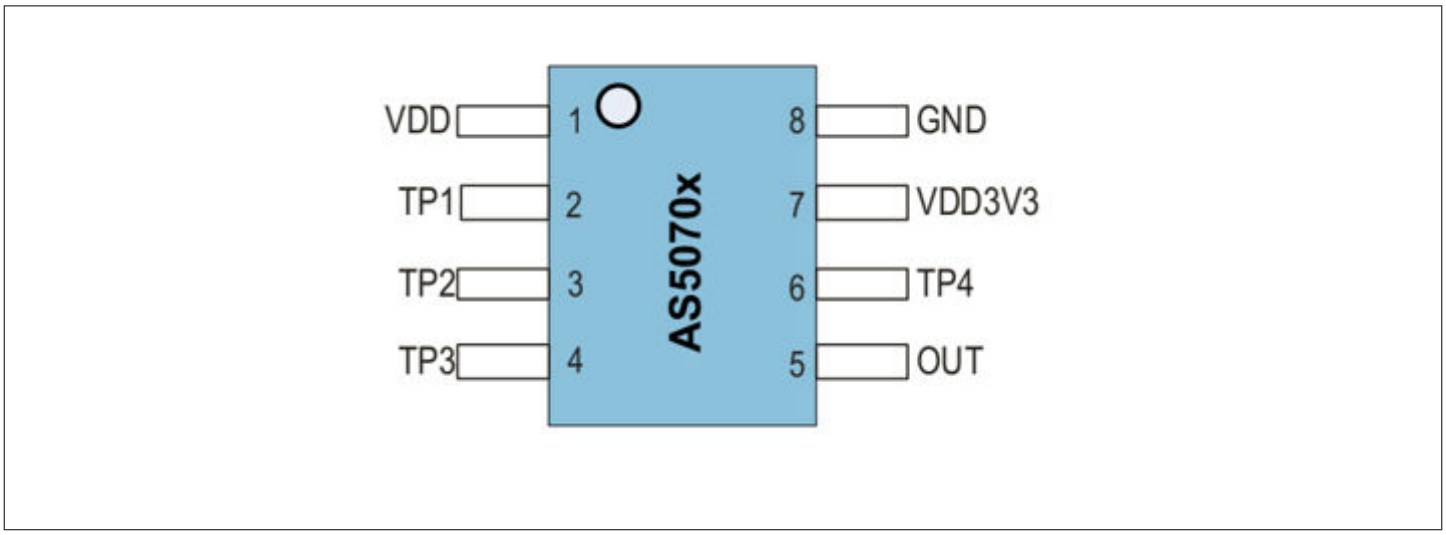


Figure 3 AS5070 pin assignment (top view, SOIC8)

Table 2 AS5070 pin description

Pin number SOIC-8	Pin name	Pin type	Description	Comments
1	VDD	Supply	Positive supply	
2	TP1	NA	Test pin	Connected to ground
3	TP2	NA	Test pin	Leave open
4	TP3	NA	Test pin	Connected to ground
5	OUT	Analog output (AS5070A) Digital output (AS5070B)	Output interface	AS5070A: Analog output AS5070B: PWM or SENT output
6	TP4	NA	Test pin	To be connected to OUT
7	VDD3V3	Supply		3.3 V on-chip low-dropout (LDO) output. Requires an external decoupling capacitor (100 nF).
8	GND	Supply	Ground	

3 Absolute maximum ratings

Stresses beyond those listed under Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Electrical characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3 Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit	Comments
Electrical Parameters					
VDD	DC Supply Voltage at VDD Pin	-20	20	V	Not operational
VOUT	External DC Voltage at OUT Pin	-0.3	20	V	Permanent
VDIFF	DC Voltage difference between VDD and OUT	-20	20		
VREGOUT	DC Voltage at the VDD3V3 Pin	-0.3	5.0	V	
I_{SCR}	Input Current (latch-up immunity)	-100	100	mA	
Continuous Power Dissipation (T_{AMB} = 70°C)					
P_T	Continuous Power Dissipation		300	mW	
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM	±2		kV	
Temperature Ranges and Storage Conditions					
T_{AMB}	Operating Temperature Range	-40	125	°C	Ambient temperature
T_{STRG}	Storage Temperature Range	-55	125	°C	125°C for 1000 h
T_{BODY}	Package Body Temperature		260	°C	The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices." The lead finish for Pb-free leaded packages is "Matte Tin" (100% Sn)
RH_{NC}	Relative Humidity (non-condensing)	5	85	%	
MSL	Moisture Sensitivity Level	3			Represents a maximum floor life time of 168 hours

4 Electrical characteristics

All tolerances that are defined for external components in this datasheet, are needed to be assured over the whole operation conditions range and also over lifetime.

Overall condition: T_{AMB} = -40°C to 125°C, VDD = 4.5 V to 5.5 V;

Components spec; unless otherwise noted.

Table 4 Operating conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VDD	Positive supply voltage		4.5	5.0	5.5	V
VREG	Regulated voltage	VDD3V3 should not be loaded by any external DC current	3.3	3.45	3.6	V
IDD_A	Supply current AS5070A	AGC = 255 (no magnet placed)	4		12	mA
lDD_B	Supply current AS5070B	AGC = 255 (no magnet placed)	4		10	mA
ISTART	Supply current at start-up	VREG = 2.25 V	2.5	5	10	mA
TSUP	Start-up time	Functional mode			10	ms

Table 5 Electrical system characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
CRES	Core resolution				14	bit
ARES	Analog resolution (AS5070A)	Range > 90°			12	bit
DRES	Digital resolution (AS5070B)				12	bit
INLopt	Integral non-linearity (optimum)	Best aligned reference magnet[1)] at 25°C over full turn 360°	-0.5		0.5	deg
INLtemp	Integral non-linearity (optimum)	Best aligned reference magnet[1)] over temperature -40°C to 125°C over full turn 360°	-0.9		0.9	deg
INL	Integral non-linearity	Best aligned reference magnet[1)] over temperature -40°C to 125°C over full turn 360° and displacement	-1.4		1.4	deg
ON	Output noise peak to peak	Static conditions - filter on			1	LSB
ST	Sampling time			125		µs

1) Reference magnet: NdFeB, 8 mm diameter, 2.5 mm thickness

Table 6 Power management - Supply monitor - Timing

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VDDUVTH	VDD undervoltage upper threshold		3.5	4.0	4.5	V
VDDUVTL	VDD undervoltage lower threshold		3.0	3.5	4.0	V
VDDUH	VDD undervoltage hysteresis		300	500	900	mV
UVDT	VDD undervoltage detection time	Time devices detects undervoltage VDD < VDDUVTH	10	50	250	µs
UVRT	Undervoltage recovery time	Time device return into normal mode from failure band VDD > VDDUVTH	10	50	250	µs
VDDOVTH	VDD overvoltage upper threshold		6.0	6.5	7.0	V
VDDOVTL	VDD overvoltage lower threshold		5.5	6.0	6.5	V
VDDOH	VDD overvoltage hysteresis		300	500	900	V
OVDT	VDD overvoltage detection time	Time devices detects overvoltage VDD > VDDOVTL	500	1000	2000	µs
OVRT	VDD overvoltage recovery time	Time device return into normal mode from failure band VDD < VDDOVTL	500	1000	2000	µs
TDETWD	WatchDog error detection time	Time device detects oscillator failure till output is in failure band			12	ms

T_{AMB} = -40°C to 125°C, VDD = 4.5 V to 5.5 V, unless otherwise noted.
Two-pole cylindrical diametrically magnetized source:

Table 7 Magnetic characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Bz	Orthogonal magnetic field strength	Required orthogonal component of the magnetic field strength measured at the package surface along a circle of 1.25 mm MFER = 0	30		70	mT
BzE	Orthogonal magnetic field strength - Extended mode	Required orthogonal component of the magnetic field strength measured at the package surface along a circle of 1.25 mm MFER = 1	10		90	mT

(table continues...)

Table 7 (continued) Magnetic characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Disp[1)]	Displacement radius	Offset between defined device center and magnet axis. Dependent on the selected magnet.		0.5		mm

1) Reference magnet: NdFeB, 6 mm diameter, 2.5 mm thickness

Table 8 Electrical and timing characteristics analog output (AS5070A)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
INLOS	INL output stage		-6		+6	LSB
DNLOS	DNL output stage		-5		+5	LSB
RERR	Ratiometricity error		-0.5%		0.5%	VDD
BVPU	Output voltage broken VDD with pull-up resistor	Pull-up resistor must be in the specified range (see Figure 11)	96		100	%VDD
BGPD	Output voltage broken ground with pull-down resistor	Pull-down resistor must be in the specified range (see Figure 11)	0		4	%VDD
OSSCG	Output short-circuit current GND	OUT = GND	5	10	20	mA
OSSCV	Output short-circuit current VDD	OUT = VDD	-20	-10	-5	mA
OSSDT	Output short-circuit detection time	OUT = GND or OUT = VDD	20	200	600	µs
OSSRT	Output short-circuit recovery time		2	5	20	ms
OLCH	Output level clamping high	Output current at OUT pin -3 mA	96			%VDD
OLCL	Output level clamping low	Output current at OUT pin 3 mA			4	%VDD
OSPSR	Output stage positive step response (driver only)	From 0 to 90%VDD, measured at OUT pin, with RPUOUT = 4.7 kΩ, CLOAD = 1 nF, VDD = 5 V			250	µs
OSNSR	Output stage negative step response (driver only)	From VDD to 10%VDD, measured at OUT pin, with RPUOUT = 4.7 kΩ, CLOAD = 1 nF, VDD = 5 V			250	µs
OSTD	Output stage temperature drift	Of value at mid code, info parameter not tested in production	-0.2		0.2	%

***Notes**:*

1. *For each code the ratiometricity error is defined as follows: VOUTRATE = ((VOUTact - (VOUTtyp * (VDDact/VDDtyp)))/VDDtyp) * 100*

Where,

- *VOUTact is the actual output voltage*
- *VOUTtyp is the typical output voltage*
- *VDDact is the actual supply voltage*
- *VDDtyp is the typical supply voltage*

Table 9 Electrical and timing characteristics PWM output (AS5070B)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
PWMSSOCG	Short-circuit output current	OUT = GND	5	10	20	mA
PWMSSOCV	Short-circuit output current	OUT = VDD	-20	-10	-5	mA
PWMSSDT	PWM short-circuit detection time	OUT = GND or OUT = VDD			5	PWM clock cycles
PWMSSRT	PWM short-circuit recovery time			6		PWM clock cycles
BKPWMVOH	PWM output voltage high in broken condition	Broken VDD or broken GND, OUT = high, RPU = 10 kΩ, PWMVOH = VDD-VOUT	0		0.4	V
BKPWMVOL	PWM output voltage low in broken condition	Broken VDD or broken GND, OUT = low, RPD = 10 kΩ	0		0.4	V
PWMF7	PWM frequency	PWMFR = 111	112.5	125	137.5	Hz
PWMF6	PWM frequency	PWMFR = 110	180	200	220	Hz
PWMF5	PWM frequency	PWMFR = 101	225	250	275	Hz
PWMF4	PWM frequency	PWMFR = 100	360	400	440	Hz
PWMF3	PWM frequency	PWMFR = 011	450	500	550	Hz
PWMF2	PWM frequency	PWMFR = 010	720	800	880	Hz
PWMF1	PWM frequency	PWMFR = 001	900	100	1100	Hz
PWMF0	PWM frequency	PWMFR = 000	1800	2000	2200	Hz
PWMVOH	PWM output voltage level high	IOUT = 5 mA, PWMVOH = VDD - VOUT	0		0.4	V
PWMVOL	PWM output voltage level low	IOUT = 5 mA	0		0.4	V

(table continues...)

Table 9 (continued) Electrical and timing characteristics PWM output (AS5070B)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
PWMSRF	PMM slew rate fast	Between 25% and 75% of VDD, RPUOUT = 4.7 kΩ, CLOUT1 = 1 nF, PWMSR = 0	1	2	4	V/µs
PWMSRS	PMM slew rate slow	Between 25% and 75% of VDD, RPUOUT = 4.7 kΩ, CLOUT1 = 1 nF, PWMSR = 1	0.5	1	2	V/µs

4.1 Timing characteristics

Table 10 Electrical and timing characteristics SENT output (AS5070B)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SENTSSOC	SENT short-circuit output current	OUT = 20 V	10	20	40	mA
SENTSSOC	SENT short-circuit output current	OUT = 0 V	-40	-20	-10	mA
BKSENTVOH	SENT output voltage in broken condition	Broken VDD or broken GND, RPU = 50 kΩ, SENT constantly high	0		1.2	V
SENTVOH	SENT output voltage high		4.1			
SENTVOL	SENT output voltage low				0.5	V
SENTFT	SENT fall time				6.5	µs
SENTRT	SENT rise time				18	µs

Table 11 Electrical and timing characteristics UART interface

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
UARTVIH	UART high level input voltage		70			%VDD
UARTVIL	UART low level input voltage				30	%VDD
UARTVOH	UART high level output voltage		VDD - 0.5 V			%VDD
UARTVOL	UART low level output voltage				0.5	%VDD
UARTBRLIM	UART baud rate		2400		9600	Baud

5 Detailed description

The AS5070 is a Hall-based rotary magnetic position sensor using a CMOS technology. The lateral Hall sensor array converts the magnetic field component perpendicular to the surface of the chip into a voltage.

The signals coming from the Hall sensors are first amplified and filtered before being converted by the analog-to-digital converter (ADC). The output of the ADC is processed by the CORDIC block (Coordinate-Rotation Digital Computer) to compute the angle and magnitude of the magnetic field vector. The sensor and analog front-end (AFE) section works in a closed loop alongside an AGC to compensate for temperature and magnetic field variations. The calculated magnetic field strength (MAG), the automatic gain control (AGC) and the angle can be read through the output pin (OUT) in UART mode.

The magnetic field coordinates provided by the CORDIC block are fed to a digital filter which reduces noise. A linearization block generates the transfer function, including linearization. The AS5070 is available with three different output interfaces: analog ratiometric (AS5070A), digital PWM or SENT (AS5070B).

The output of the AS5070 can be programmed to define a starting position (zero angle) and a stop position (maximum angle). An embedded linearization algorithm allows reducing the system INL error due, for example, to mechanical misalignment, magnet imperfections, etc.

The AS5070 can be programmed through the OUT pin with a UART interface which allows writing an on-chip non-volatile memory (OTP) where the specific settings are stored. The AS5070 can be programmed by the infineon programming tool, both at the component and board level.

6 Register description

Table 12 Non-volatile memory register description

Address	Bit position	Field	Description
0x0A	7:0	CUSTID0	Customer ID byte 0
0x0B	7:0	CUSTID1	Customer ID byte 1
0x0C	7:0	CUSTID2	Customer ID byte 2
0x0D	7:0	CUSTID3	Customer ID byte 3
0x0E	0	PWMINV	PWM inverted
	1	PWMSR	PWM slew rate (0 = PWM slew rate fast PWMSRF, 1 = PWM slew rate slow PWMSRS)
	3:2	DIGOS	Digital output stage (00 = PWM push-pull 01 = PWM pull-down 10 = PWM pull-up 11 = SENT) Only applicable to AS5070B
	6:4	RBKDEB	Read-back debouncing
	7	NA	No use
0x0F	0	FBS	Failure band selection (0 = lower failure band, 1 = upper failure band)
	2:1	HYST	Hysteresis across the brake point
	4:3	QUAD	Quadrant selection
	7:5	PWMFR	PWM frequency selection
0x10	1:0	PWMRTH	PWM rising threshold
	3:2	PWMFTH	PWM falling threshold
	7:4	SENTMID	SENT Message ID
0x11	4:0	SENTTK	SENT tick
	5	SENTESM	Enable SENT serial message
	6	SENTPP	SENT pause pulse enable (0 = disable, 1 = enable)
	7	SENTRC	SENT rolling counter enable (0 = disable, 1 = enable)
0x12	3:0	NA	No use. Default 0
	7:4	NA	No use. Default 0
0x13	3:0	NA	No use. Default 0
	7:4	NA	No use. Default 0
0x14	7:0	CLMPH	Clamping level high Reg 0x14[0] = LSB

(table continues...)

Table 12 (continued) Non-volatile memory register description

Address	Bit position	Field	Description
0x15	3:0		Reg 0x15[3] = MSN
	7:4	CLMPL	Clamping level low Reg 0x15[4] = LSB Reg 0x16[7] = MSN
0x16	7:0		
0x17	7:0	PPOFFSET	Post processing offset Reg 0x17[0] = LSB Reg 0x19[3] = MSB
0x18	7:0		
0x19	3:0		
	7:4	PPGAIN	Post processing gain Reg 0x19[4] = LSB Reg 0x1B[3] = MSB
0x1A	7:0		
0x1B	4:0		Break point Reg 0x1B[5] = LSB Reg 0x1D[2] = MSB
	7:5	BP	
0x1C	7:0		
0x1D	2:0		
	3	MFER	Magnetic field extended range (1 = Bz, 0= BzE)
	4	AER	Angle extended range (set to 1 if the maximum angle excursion is smaller than 22 degree)
	6:5	FILTER	Post processing filter
	7	CUSLOCK	Customer settings lock
0x1E	7:0	SIGN	Signature for error correction code

Table 13 Volatile memory register description

Address	Bit position	Field	R/W	Description
0x22	7:0	DAC12IN	R/W	Input word of the 12-bit output DAC (Reg0x23[3] = MSB, Reg0x22[0] = LSB)
0x23	3:0		R/W	
	4	DAC12INSEL	R/W	DAC 12 input buffer selection
	5	DSPRN	R/W	Digital signal processing reset
	6	GLOAD	R/W	Enable of gload
	7	-	-	Not used
0x32	7:0	ANGLECORDIC	R	Angle of the CORDIC output block. (Reg0x33[5] = MSB, Reg0x32[0] = LSB)
0x33	5:0			
	7:6	-	-	Not used
0x34	7:0	MAG	R	CORDIC magnitude
0x35	7:0	AGC	R	AGC value
0x36	7:0	ANGLEFILTER	R	Angle of the digital filter output block

(table continues...)

Table 13 (continued) Volatile memory register description

Address	Bit position	Field	R/W	Description
0x37	3:0			(Reg0x37[3] = MSB, Reg0x36[0] = LSB)
0x37	7:4	-	-	Not used

Table 14 Special functions

Address	Bit position	Field	Description
0x60	7:0	P2F	Pass-to-functions, see UART
0x61	7:0		
0x62	7:0	BURNOTP	Permanently burn OTP, see UART
0x63	7:0		

6.1 UART interface

The AS5070 is equipped with a UART interface, which allows reading and writing the registers as well as permanently programming the non-volatile memory (OTP). By default (factory setting) the AS5070 is in the so-called Communication Mode and the UART is connected at the output pin (OUT). In this mode, it is possible to configure the register settings. In this mode, the device is in open-drain mode and therefore a pull-up resistor has to be connected on the output.

The UART interface allows reading and writing two consecutive addresses. The standard UART sequence consists of four frames. Each frame begins with a start bit (START), which is followed by 8 data bits (D[0:7]), one parity bit (PAR), and a stop bit (STOP), as shown in Figure 4.

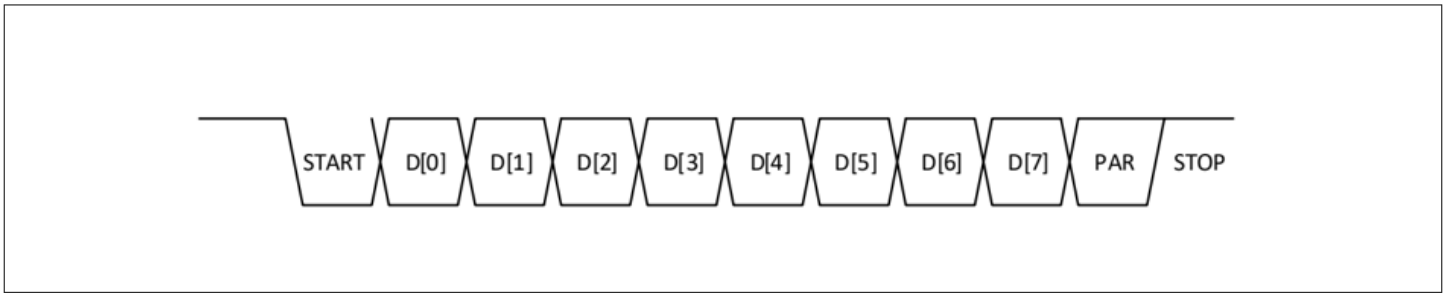


Figure 4 UART frame

The PAR bit is even parity calculated over the data bits (D[0:7]). Each frame is transferred from LSB to MSB.

The four frames are shown in Table 15.

Table 15 UART frame sequence

Frame number	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
1	0x55							
2	R/W	ADDRESS						
3	DATA1							
4	DATA2							

The first frame is the synchronization frame and consists of D[0:7] = 0x55 followed by the parity bit (PAR=0) and the stop bit. This frame synchronizes the baud rate between the AS5070 and the host microcontroller.

The second frame contains the read/write command (D[7] = 0 Write, D[7] = 1 Read) and the address of the register (D[6:0] = ADDRESS).

The content of the third and fourth frames (DATA1 and DATA2) will be written to or read from the location specified by ADDRESS and ADDRESS+1, respectively.

Figure 5 and Figure 6 show examples of read and write.



Figure 5 Example of write (Reg[0x22] = 0x18, Reg[0x23] = 0xA2)

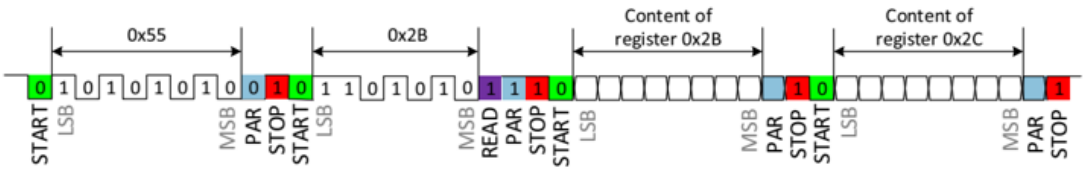


Figure 6 Example of read (Reg[0x2B], Reg[0x2C])

6.2 Exiting communication mode

Communication mode is exited and operational mode is entered with a Pass-to-function (P2F) command, by writing to the virtual registers 0x60 and 0x61:

P2F: write(0x60) = 0x70, write(0x61) = 0x51

No more commands can be sent after sending this command, because the device is permanently placed in operational mode.

6.3 Burning the OTP registers

The BURNOTP command writes the OTP registers with their programmed values. The command is issued by writing to virtual registers 0x62 and 0x63:

BURNOTP: write(0x62) = 0x70, write(0x63) = 0x51

6.4 Customer ID

A specific identifier chosen by the user can be stored in the non-volatile memory. This identifier consists of 4 bytes and can be stored in the locations CUSTID0, CUSTID1, CUSTID2 and CUSTID3.

6.5 Output linear transfer function

A linear transfer function controls the state of the output in response to the absolute orientation of the external magnet. The parameters which control this function are shown in Figure 7.

Table 16 Transfer function control parameters

Symbol	Parameter	Resolution [bit]
T1	Mechanical angle starting point	14
T2	Mechanical angle stop point	14
OT1	Output at the starting point (T1)	12
OT2	Output at the stop point (T2)	12
CLMPL	Clamping level low	12
CLMPH	Clamping level high	12
BP	Breakpoint	14

As shown in the Figure 7, the parameters T1, T2, OT1, and OT2 define the input-to-output linear transfer function. The dedicated programmer for the AS5070 uses the parameters from Table 16 to generate the corresponding settings CLMPL, CLMPH, PPOFFSET, PPGAIN and BP (see Figure 7).

The clamping level parameters CLMPL and CLMPH define the absolute minimum and maximum level of the output. Both clamping levels can be set with the 9 LSBs out of the 12-bit output resolution. This means that the maximum value for CLMPL is one eighth, while CLMPH minimum value is seven-eighths of the output diagnostic. CLMPL and CLMPH must always be set outside of the lower and upper diagnostic failure band defined by the output broken wire voltage (see Figure 7: BGPD and BVPU).

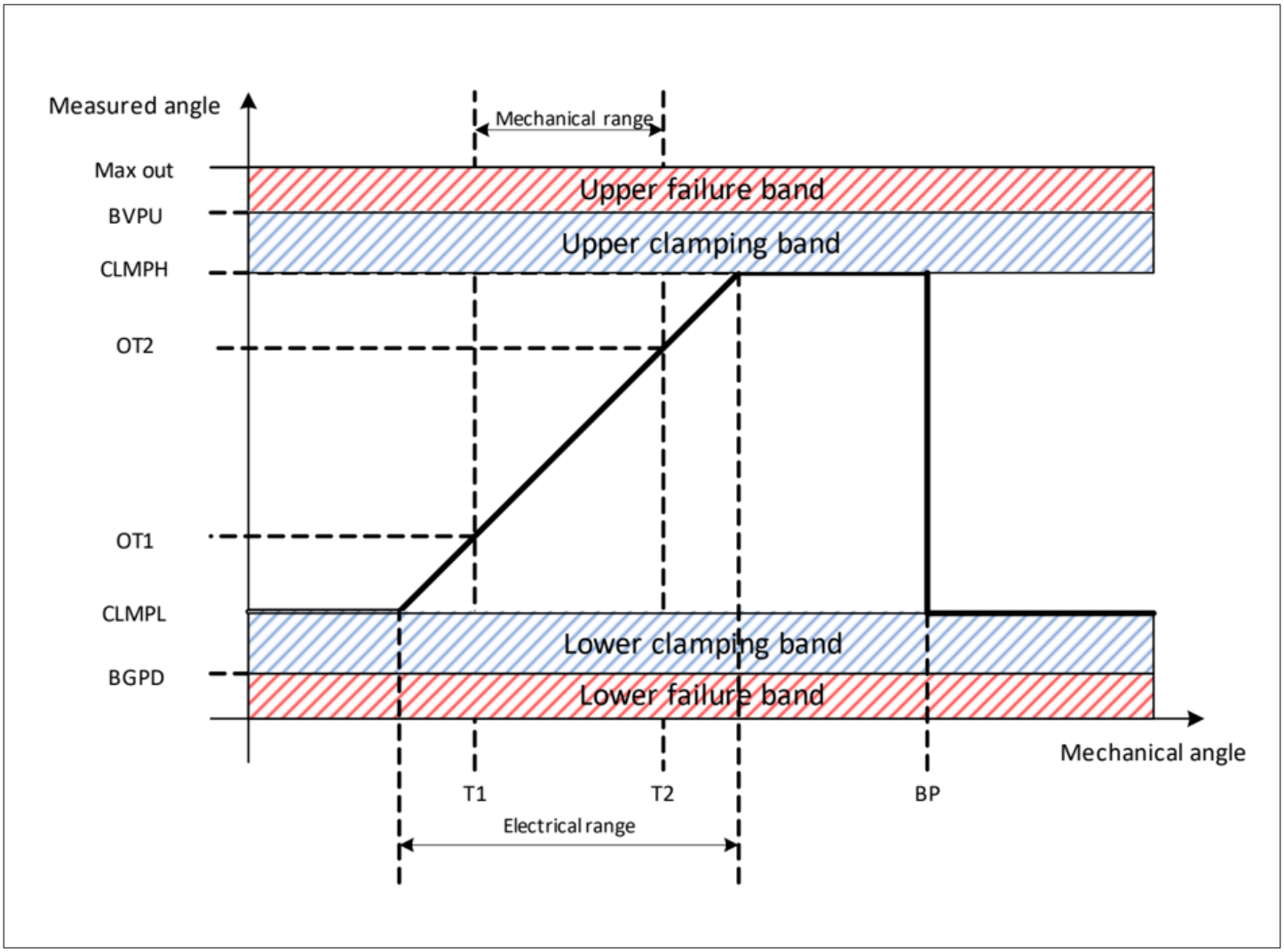


Figure 7 Output transfer function

The breakpoint BP sets the discontinuity point where the output jumps from one clamping level to the other. It is strongly recommended to set the breakpoint at the maximum distance from the start and stop position (T1 and T2). To handle the case of a full turn, a hysteresis function across the breakpoint can be used to avoid sudden jumps between the lower and upper clamping level.

Table 17 Hysteresis setting

HYST	Hysteresis LSBs
00	0
01	56
10	91
11	137

The hysteresis LSB is based on the core resolution (14-bit). The AS5070 features a programmable digital filter. As shown in Table 17 in a static condition (no change of the input), the static error band is ±0.5 LSB (at 12-bit resolution). Whenever an input step occurs, the output (measured angle) follows the input (mechanical angle) entering a certain error band within the step response time. From the time when the output is within the static error band the output takes 1000 ms to settle to the static error band achieving again ±0.5 LSB output noise. The filter is not usable in 360° range, if the Hysteresis setting is on.

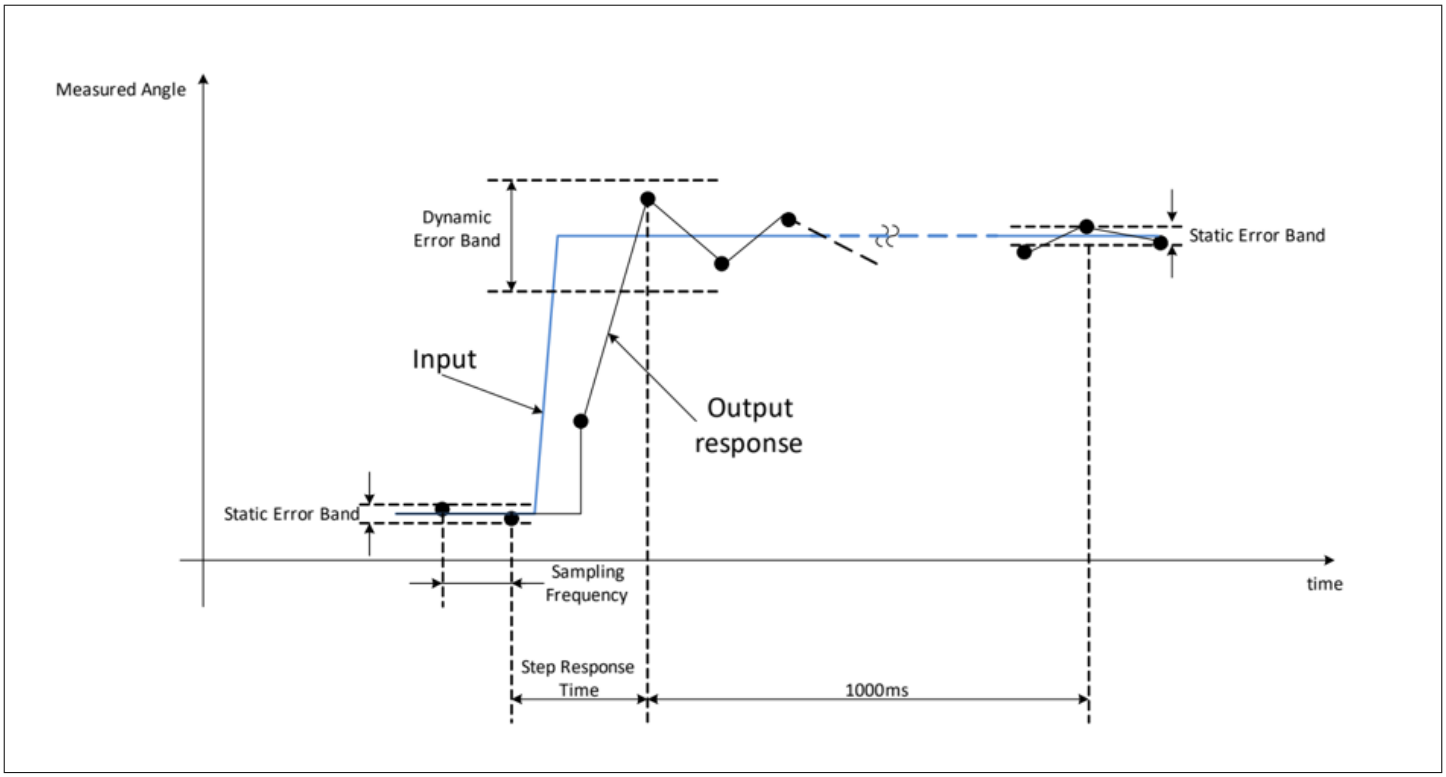


Figure 8 Step response

Table 18 FILTER setting

FILTER	Dynamic error band [LSB]	Step response time [µs]
00	Filter off	Not applicable
01	23	5 CORDIC cycles

The FBS setting allows selecting the failure band (lower or upper) when the output goes into diagnostic mode.

6.5.1 Multiple quadrants

The multiple quadrants option allows repeating the same output control parameters up to 4 times over the full turn rotation as shown in the Figure 9, Figure 10 and Figure 11. The QUAD parameter sets the number of quadrants, as shown in the Table 19.

Table 19 Number of quadrants

QUADEN	Number of quadrants
00	Single
01	Double
10	Triple
11	Quadruple

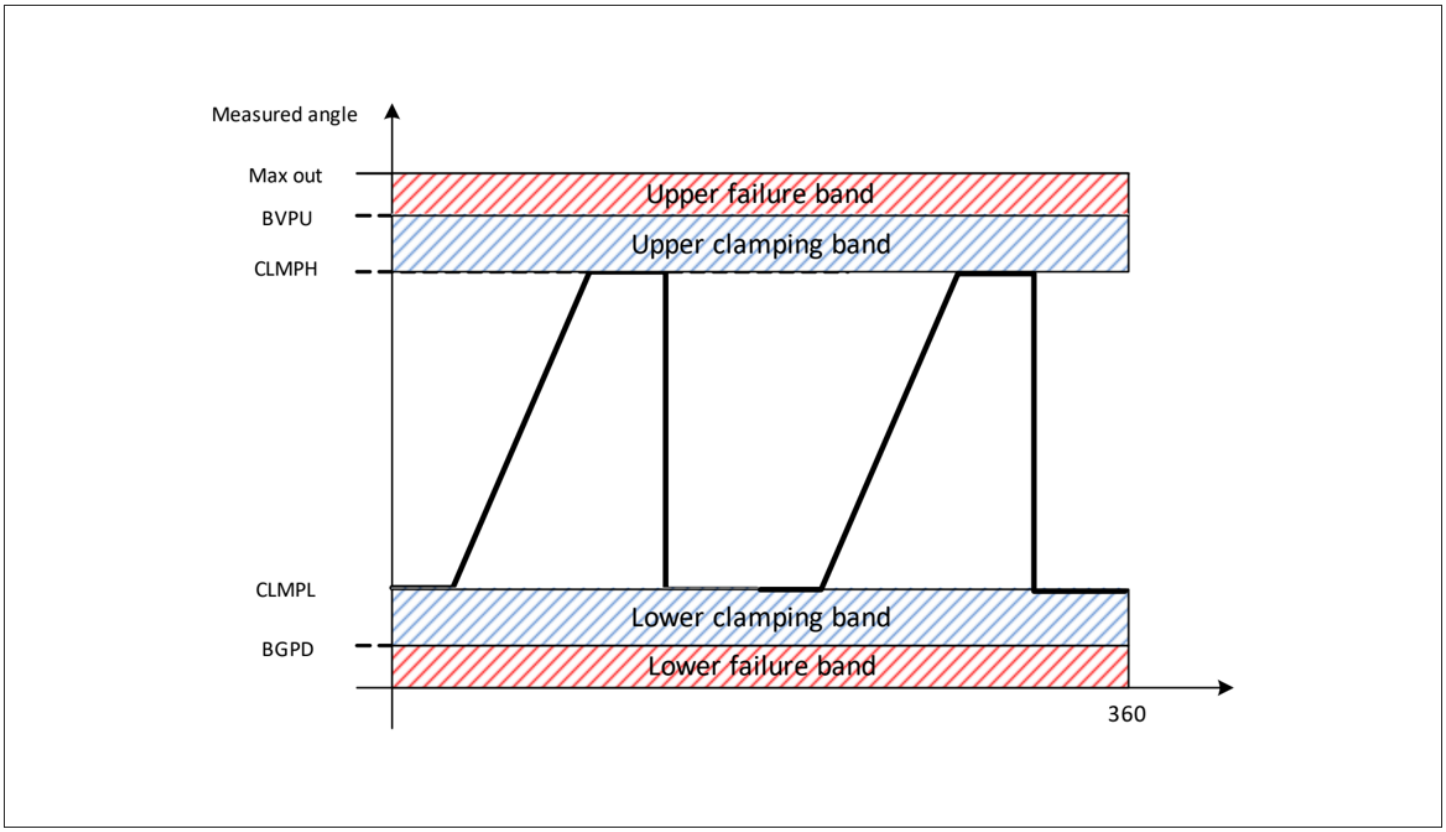


Figure 9 Dual quadrant mode

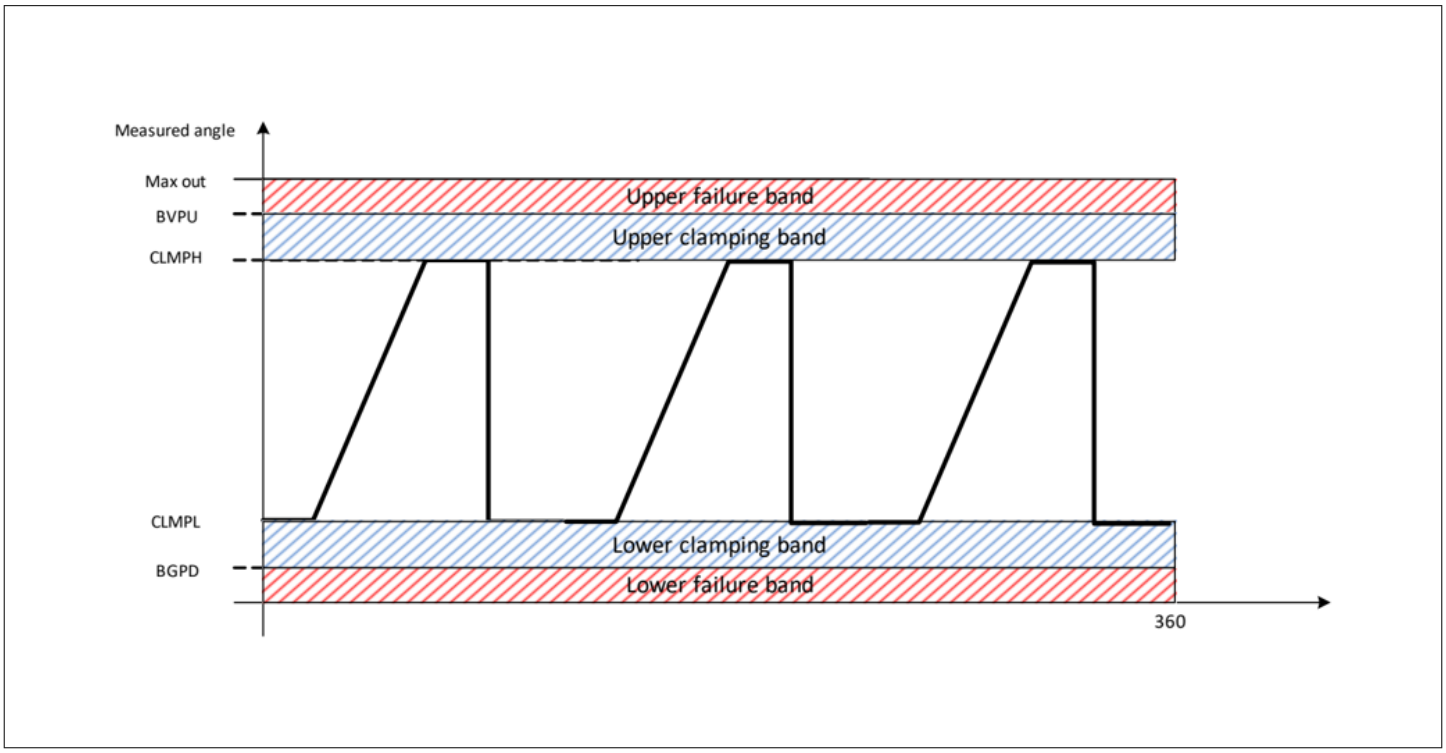


Figure 10 Triple quadrant mode

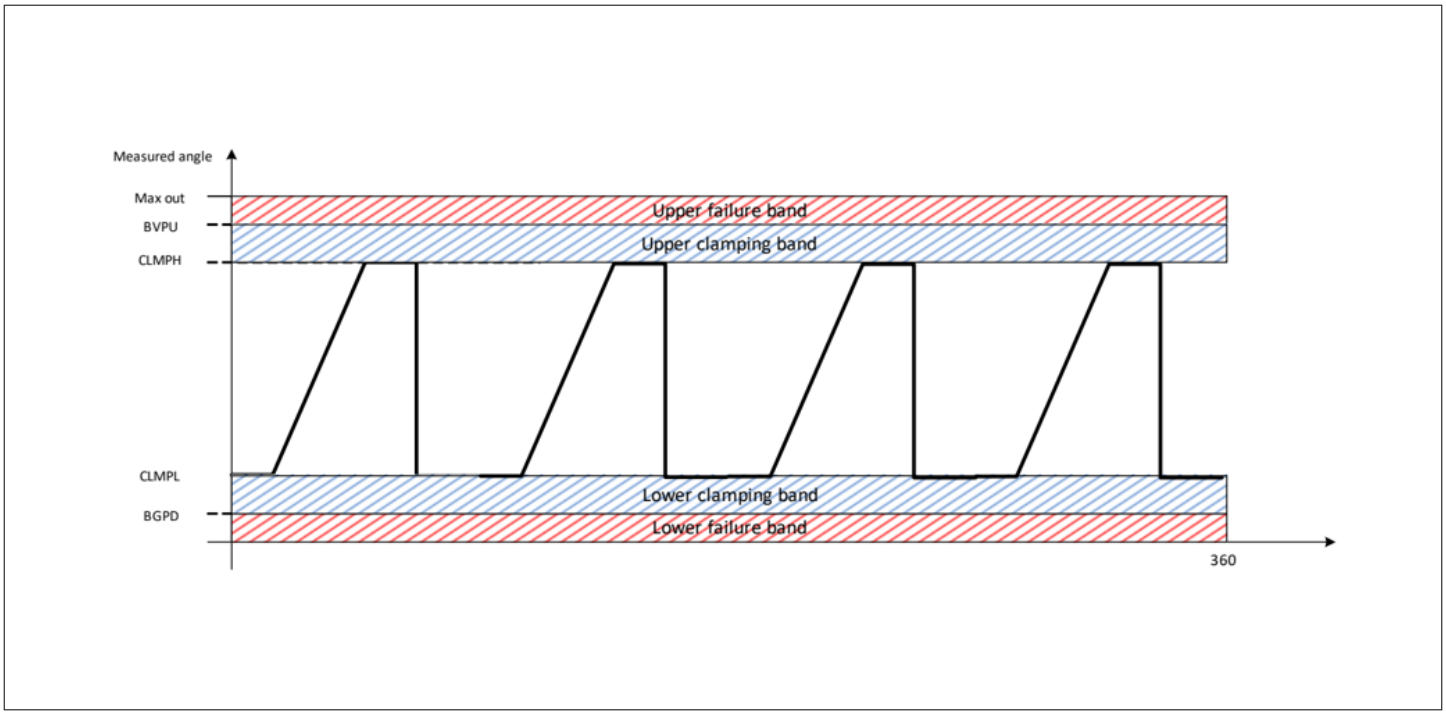


Figure 11 Quadruple quadrant mode

6.6 Extended magnetic input range

The magnetic input field range can be boosted with the MFER bit. The extended magnetic field allows increasing the maximum air gap between the AS5070 and the magnet.

More information can be found in the Application Note.

6.6.1 Analog output (AS5070A)

The AS5070A provides a linear analog ratiometric output signal. The output buffer features a push-pull analog output stage which can be loaded with a pull-down or a pull-up resistor. The output voltage represents the angular orientation of the magnet above the AS5070A on a linear absolute scale and is ratiometric to VDD.

6.6.2 PWM output (AS5070B)

The AS5070B has a PWM output. With the DIGOS setting, the PWM output stage can be programmed as a push-pull, pull-down, or pull-up driver. The duty-cycle of each pulse is proportional to the absolute angular position of the external magnet.

The PWM signal consists of a frame of 4096 clock periods as shown in Figure 12. The PWM frame begins with a certain number of clocks high, defined by the CLMPL, which is followed by the electrical angle information. The frame ends with a certain number of clock pulses low, as defined by the CLMPH. It is possible to invert the frame using the PWMINV setting.

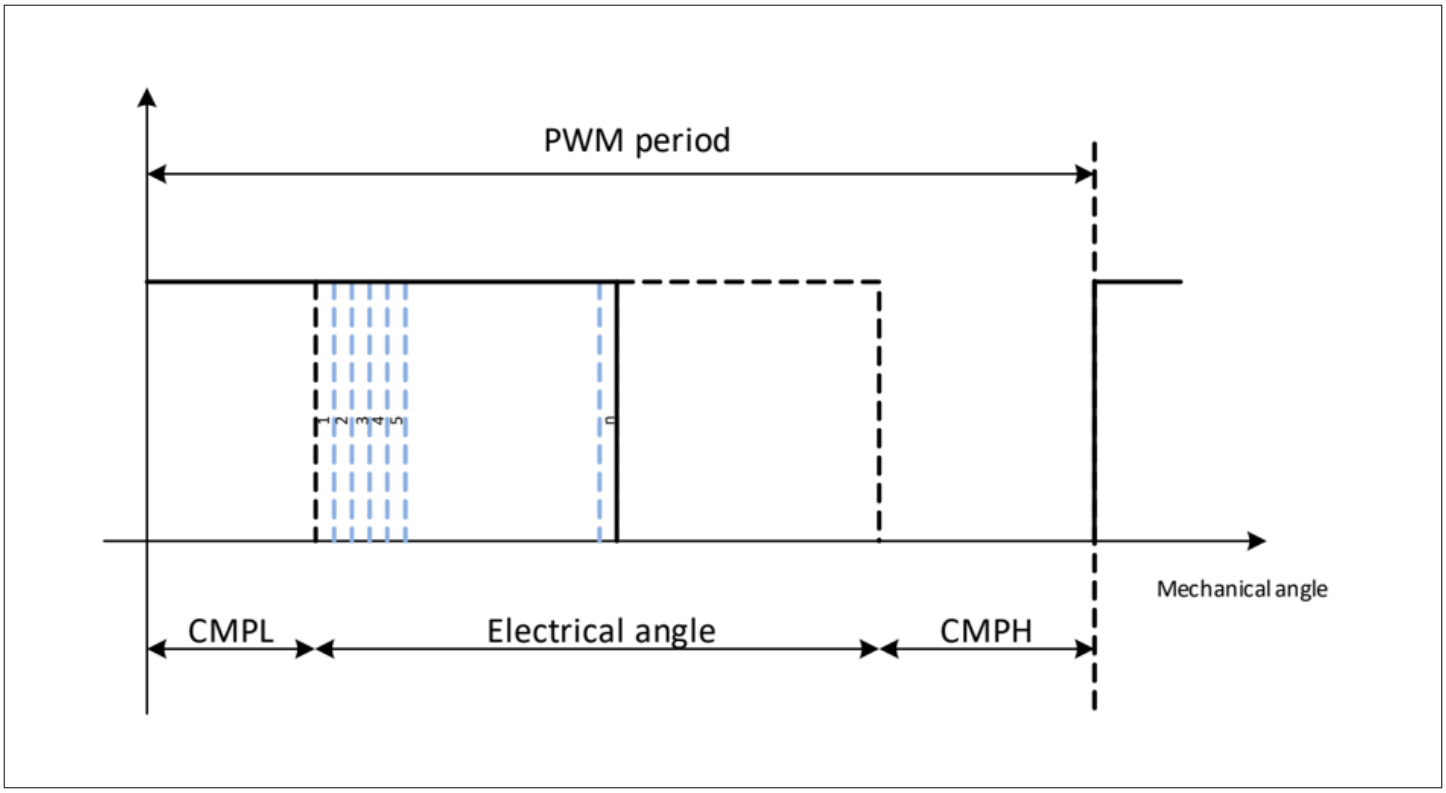


Figure 12 Pulse width modulation frame

The PWMFR setting sets the duration of the PWM frequency.

The PWMSR setting chooses between fast and slow steps.

6.6.3 SENT output (AS5070B)

The AS5070B provides a SENT-compatible output (Single Edge Nibble Transmission) interface which is compliant with the SAE-J2716 standard (Jan-2010) and features the Single Secure Sensor and the Single Sensor protocol (refer to `SENT_J2716_Standard - Appendix A.3 and A.4`). SENT is a single-wire interface based on a unidirectional communication scheme from the sensor (transmitter) to the engine control unit (receiver). The sensor constantly transmits data to the receiver.

The SENT interface can be enabled on the AS5070B with the DIGOS setting.

The SENT frame consists of 8 nibbles in which each nibble is made up by 4 bits. The duration of the nibbles is variable and depends on its content and tick frequency. With the AS5070B, the tick frequency is selected by the SENTTK setting, as shown in Table 20.

Table 20 SENT tick period

SENTTK	SENT tick period (µs)
00000	3
00001	4
00010	4.5
00011	5
00100	5.5
00101	5.75

(table continues...)

Table 20 (continued) SENT tick period

SENTTK	SENT tick period (µs)
00110	6.5
00111	6.75
01000	7.5
01001	8
01010	8.5
01011	9
01100	9.5
01101	10
01110	10.25
01111	10.5
10000	10.75
10001	11
10010	11.25
10011	11.5
10100	11.75
10101	12
10110	12.25
10111	12.5
11000	2.25
11001	2.5
11010	2.75
11011	3
11100	3.25
11101	3.5
11110	3.5
11111	3.5

The nibble protocol consists of:

- 5 clock ticks low
- 7 clock ticks + n clock ticks high

Where n is the decimal representation of the 4 bit data. If the nibble data is zero (data = 0x00, n = 0) the nibble duration is 12 ticks, while if the nibble data is 15 (data = 0xFF, n = 15) its duration is 27 ticks.

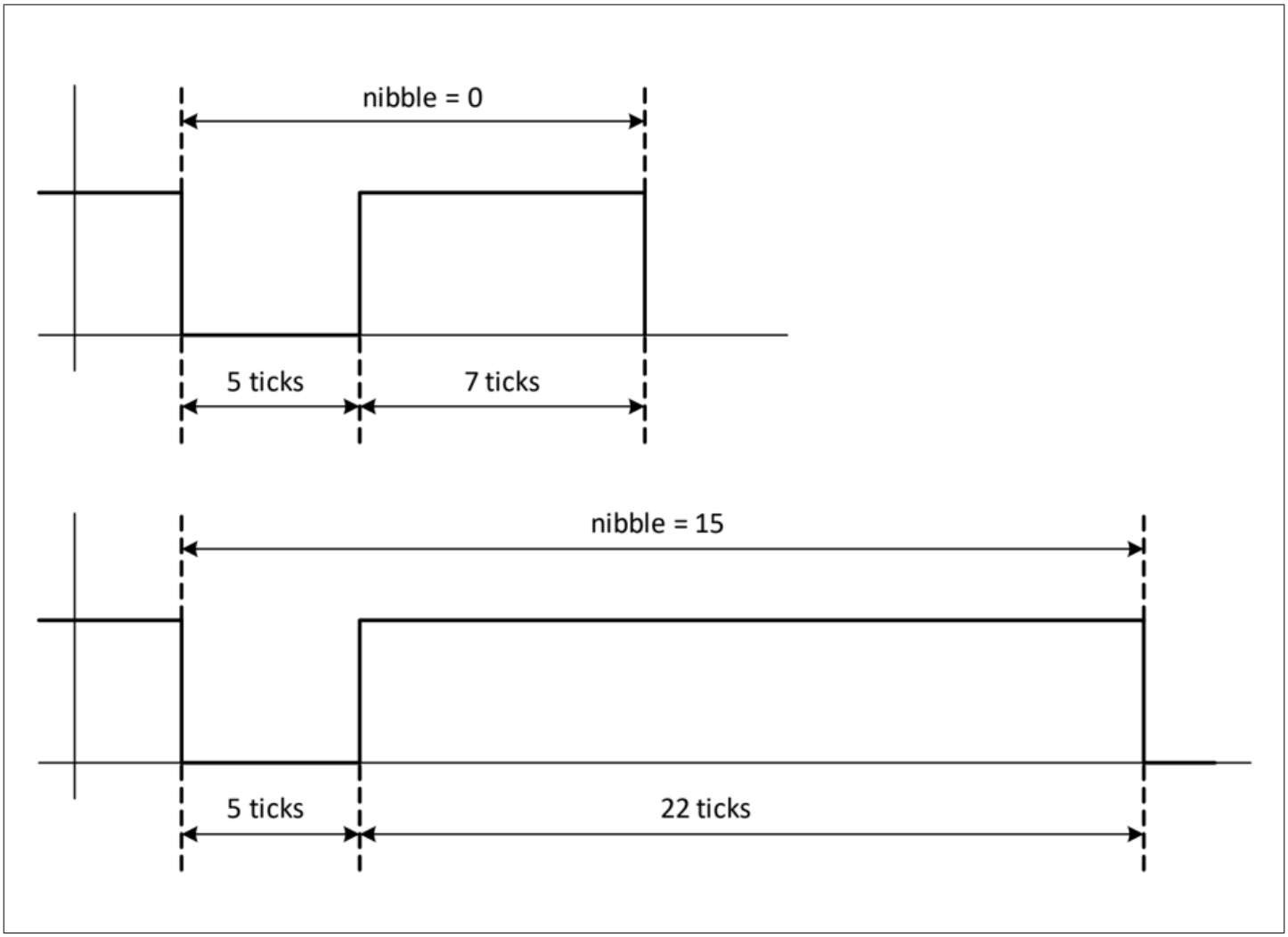


Figure 13 PWM clock period and frequency

The SENT protocol consists of a 56-tick synchronization pulse followed by 8 nibbles. Each nibble is described in Table 21.

Table 21 Nibble description

Nibble	Description
1	Status and communication
2	Angle data most significant nibble
3	Angle data middle significant nibble
4	Angle data least significant nibble
5	Rolling counter most significant nibble
6	Rolling counter least significant nibble
7	Inverted nibble #2
8	CRC checksum

The Status and Communication nibble includes diagnostic status and the Short Serial Message Format, as defined in the SAE J2716 protocol.

Table 22 Status and communication nibble

Bit	Description
0	Error bit: 0 = no sensor error, 1 = sensor error
1	0 (always)
2	Short Serial Message
3	Message Start

The Short Serial Message is transmitted one bit per SENT frame in bit 2 of consecutive frames and consists of 16 bits. The starting bit of a Short Serial Message is indicated by a 1 in bit 3 (Message Start) of the Status and Communication Nibble

Table 23 Serial message

SENT message number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Message Start	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Short Serial Message[2]	SENTMID				MAG								CRC			

The Short Serial Message consists of a message ID (SENTMID) and the magnitude of the magnetic field (MAG). The Short Serial Message is protected by a 4-bit CRC.

The SENTESM bit enables the Short Serial Message, which is otherwise by default disabled.

The angular information is contained in nibbles 2, 3 and 4.

Nibbles 5 and 6 contain a rolling counter which counts the number of sent telegrams and rolls over to 0 after reaching the maximum value of 255. The rolling counter can be disabled, which is not needed in the Single Sensor mode, with the SENTRC bit.

Because the tick clock period is 3 µs, the minimum duration of a SENT telegram is 456 µs, while the maximum duration is 816 µs. the SENTPP bit enables the Pause Pulse, which creates a SENT transmission with a constant duration of 272 ticks.

6.7 Diagnostics

The AS5070 has several self-diagnostic features (safety Mechanism), which are listed in Table 24.

Table 24 Self diagnostic features

SM	Safety mechanism	Recoverable	Safe state
SM1	Watchdog failure	No, if a watchdog error is detected, the sensor provides the error information till a sensor reset happens	Output is going into HIZ --> failure band (depending on output resistor)
SM2	Offset compensation not complete	Yes, if the offset is below the specified threshold, sensor recovers the output	Output is forced in failure band. Depending on FBS setting

(table continues...)

Table 24 (continued) Self diagnostic features

SM	Safety mechanism	Recoverable	Safe state
SM3	CORDIC overflow	Yes, if the magnetic input field is below the specified threshold, sensor recovers the output	Output is forced in failure band. Depending on FBS setting
SM4	Magnetic input field too high/too low	Yes, if the magnetic field is inside the specific range, after the recovery time the sensor leave the failure	Output is forced in failure band. Depending on FBS setting
SM5	Vreg undervoltage	Yes	Hi-z: Failure band related to the out load
SM6	Reverse polarity	Yes, if reverse polarity issue is solved. No direct safety mechanism, it's a protection!	Hi-z: Failure band related to the out load
SM7	VDD overvoltage	Yes, if the VDD is below the specified threshold.	Hi-z: Failure band related to the out load
SM8	VDD undervoltage	Yes, if the VDD is above the specified threshold	Hi-z: Failure band related to the out load
SM9	Broken VDD	Yes	Hi-z: Failure band related to the out load
SM10	ADC check	No, sensor stays in failure band till the sensor is resetting.	Hi-z: Failure band related to the out load
SM11	Analog read fail	Yes	Hi-z: Failure band related to the out load
SM12	Short circuit	Yes	Hi-z: Failure band related to the out load
SM13	Signature	No, sensor stays in failure band till the sensor is resetting	Hi-z: Failure band related to the out load
SM14	Broken GND	Yes	Hi-z: Failure band related to the out load

The FBS setting allows selecting the failure band (lower or upper) when the output goes into diagnostic mode.

6.7.1 Analog read fail (SM11)

If an error occurs, the output will be set in a safe condition (high impedance) after a certain time.

6.7.2 Digital readout

The device is measuring internally the time between rising and falling edge of the digital signal.
The maximum duration of timeout until triggering an error condition is set by PWMRTH and PWMFTH.

Table 25 Timeout setting for rising edge

PWMRTH		Delay (µs)
0	0	Disabled
0	1	24-28
1	0	56-60
1	1	112-120

Table 26 Timeout setting for falling edge

PWMFTH		Delay (µs)
0	0	Disabled
0	1	24-28
1	0	56-60
1	1	112-120

6.7.3 Analog readout

The device reads back the analog signal and compares it with the digital output value. If the difference is too high, the output driver is kept in high impedance.

The maximum duration of timeout until triggering an error condition is set by RDBCKDEB.

Table 27 Timeout setting for analog read back

RDBCKDEB02	RDBCKDEB01	RDBCKDEB00	CORDIC cycles[1)]
0	0	0	0 - Disabled
0	0	1	1
0	1	0	2
0	1	1	4
1	0	0	8
1	0	1	16
1	1	0	32
1	1	1	64

1) 1 CORDIC cycle typ.:111 µs

7 Application information

7.1 Signature calculation

The OTP of AS5070A and AS5070B uses a BIST technique with Multiple Input Signature Register circuits.

To activate this BIST a calculation of the Signature Byte is necessary and has to store into the OTP during the programming sequence.

For calculating the signature byte the content of the whole memory (0x02 to 0x1D) has to be read.

Out of this information the following calculation has to be done.

Byte: 0x02 = data2

….

Byte: 0x1D = data29

```
Unsigned int signature (unsigned int * content)
{
unsigned int misr,misr_shift,misr_xor,misr_msb;
misr = 0;
for (int i=0; i<28; i++) {
misr_shift = (misr<<1);
misr_xor = (misr_shift ^ content[i])%256;
misr_msb = misr/(128);
if (misr_msb == 0)
misr = misr_xor;
else
misr = (misr_xor ^ 29)%256;
}
return misr;
}
content= {,data2,data3,data4,data5,data6,
 data7,data8,data9,data10,data11,
 data12,data13,data14,data15,data16,
 data17,data18,data19,data20,data21,data22,
 data23,data24,data25,data26,data27,data28,data29};
```

7.2 Programming parameter

The programming has to be performed in communication mode. If the cust_lock = 0, the sensor starts in communication mode.

The following procedure and the block diagram are showing the common 2 point calibration. For special calibration procedure:

AS5070A: Analog output driver calibration

AS5070A/AS5070B: Linearization.

Please go in contact with the **infineon** application team.

7.3 Burn and verification of the OTP memory

1. Power on cycle
2. Move magnet to the first mechanical start position
3. Reset the DSP. Writing 0x20 into Reg(0x0023)

4. Read out the measured angle from ANGLECORDIC register: T1 Value
5. Moving of magnet to the second mechanical position (stop position)
6. Read out the measured angle from ANGLECORDIC register: T2 Value
7. Write T1,T2 and all other transfer parameter into the DLL: Calculation of GAIN, Offset, BP, Clamping
8. Write reg(0x000A) to reg (0x001E) with the custom settings and the calculated values from point 7. --> AS5070 Settings
9. Read reg(0x000A) to reg (0x001E) ---> Read register step 1
10. Comparison of AS5070 settings with content of read register step 1
11. If point 10 is correct: Decision: pass 2 function (measurement verification) or programming. Programming sequence starts with point 12
12. Write reg(0x000A) to reg (0x001E) with the custom settings and the calculated values from point 7 + customer lock Bit. --> AS5070 Settings_Prog
13. Read reg(0x0000) to reg (0x001D) ---> Read register step 2
14. Calculation of Signature Byte out of Read register step 2 content: Signature Byte
15. Write 8Bit Signature to reg(0x001E)
16. Write reg(0x000A) to reg (0x001E) with the custom settings and the calculated values from point 7 + customer lock Bit + Signature byte. --> AS5070 Settings_ Prog_final
17. Read reg(0x000A) to reg (0x001E) ---> Read register step 3
18. Comparison of AS5070 Settings_Prog_final with content of read register step 3
19. If point 18 is correct, start the OTP burn procedure by writing: Reg(0x0062)=0x70 and Reg(0x0063)=0x51
20. Programming procedure is complete after 10 ms
21. Clear the memory content writing 0x00 into reg (0x001E)
22. Write Reg0x23=0x40 to set the threshold for the guard band test [1)]
23. 5 ms wait time to refresh the non-volatile memory content with the OTP content
24. Read reg(0x000A) to reg (0x001E) ---> Read register step 4
25. If content from reg (0x001E) compares with content from "Signature Byte" refresh was successful
26. Comparison of AS5070 Settings_Prog_final with content of read register step 4. Mandatory: guard band test [1)]
27. If point 26 fails, the test with the guard band [1)] was not successful and the device is incorrectly programmed. A reprogramming is not allowed
28. Clear the memory content writing 0x00 into reg (0x001E)
29. Write Reg0x23=0x00to set the threshold for the guard band test [1)]
30. 5 ms wait time to refresh the non-volatile memory content with the OTP content
31. Read reg(0x000A) to reg (0x001E) ---> Read register step 5
32. If content from reg (0x001E) compares with content from "Signature Byte" refresh was successful
33. Comparison of AS5070 Settings_Prog_final with content of read register step 5. Mandatory: Guard band test [1)]
34. If point 33 fails, the test with the guard band [1)] was not successful and the device is incorrectly programmed. A reprogramming is not allowed
35. Reset of the device. After power on the Sensor starts in functional mode

1 Guard band test:
Restricted to temperature range: 25°C ± 20°C
Right after the programming procedure (max. 1 hour with same Conditions 25°C ± 20°C)
Same VDD voltage The guard band test is only for the verification of the burned OTP fuses during the programming sequence.
A use of the guard band in other cases is not allowed.

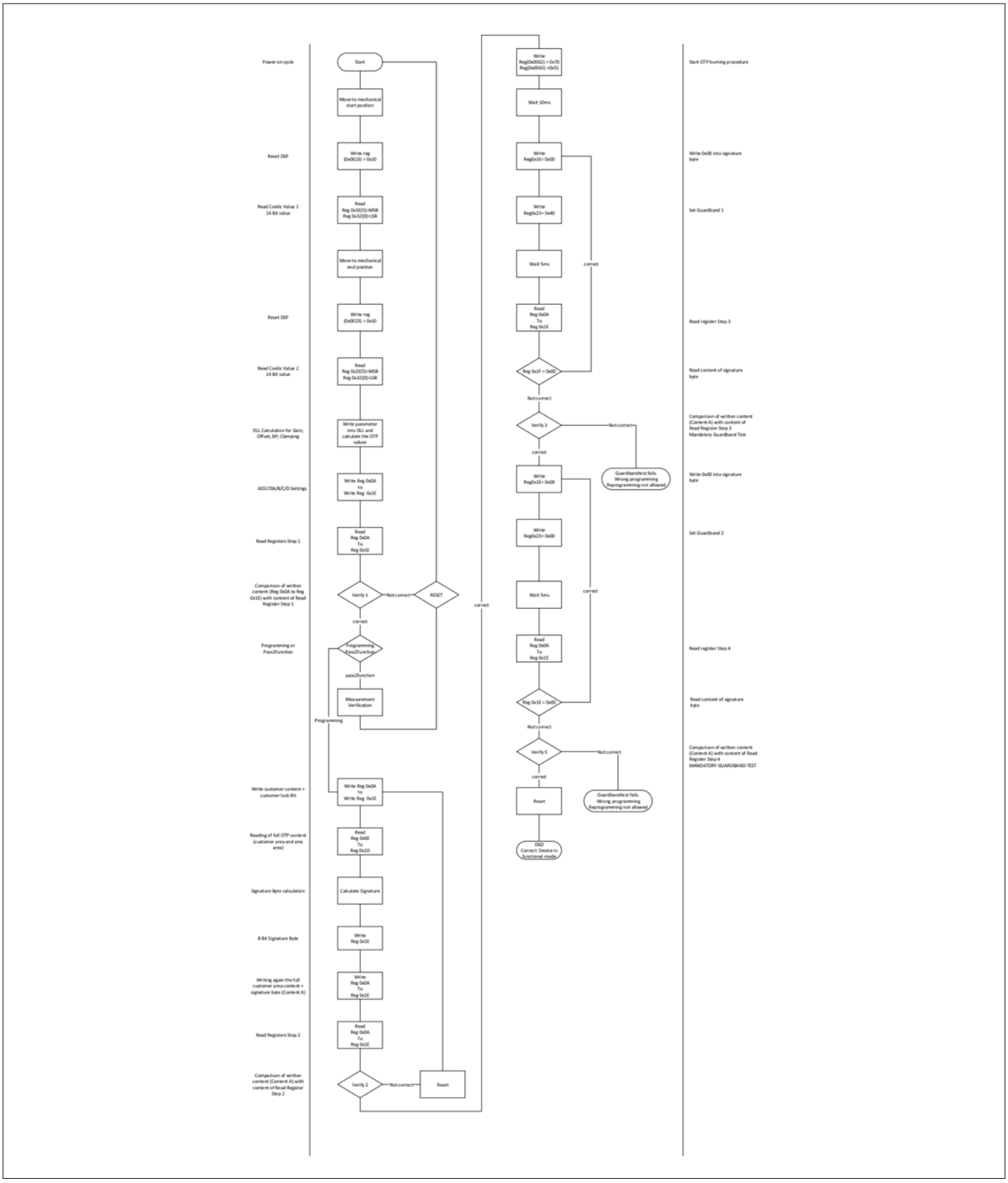


Figure 14 OTP memory burn and verification flowchart

7.4 SOIC8

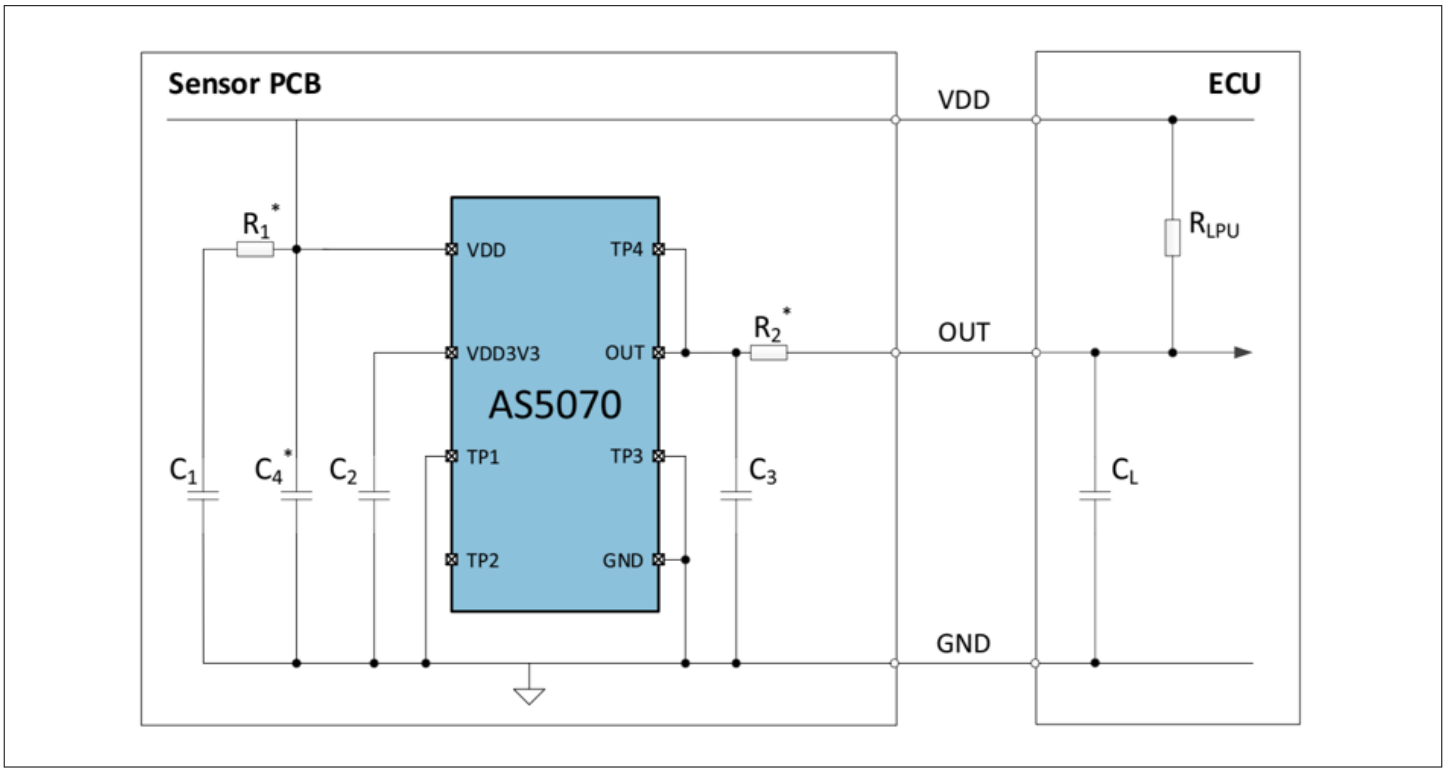


Figure 15 Application with pull-down load resistor (SOIC-8)

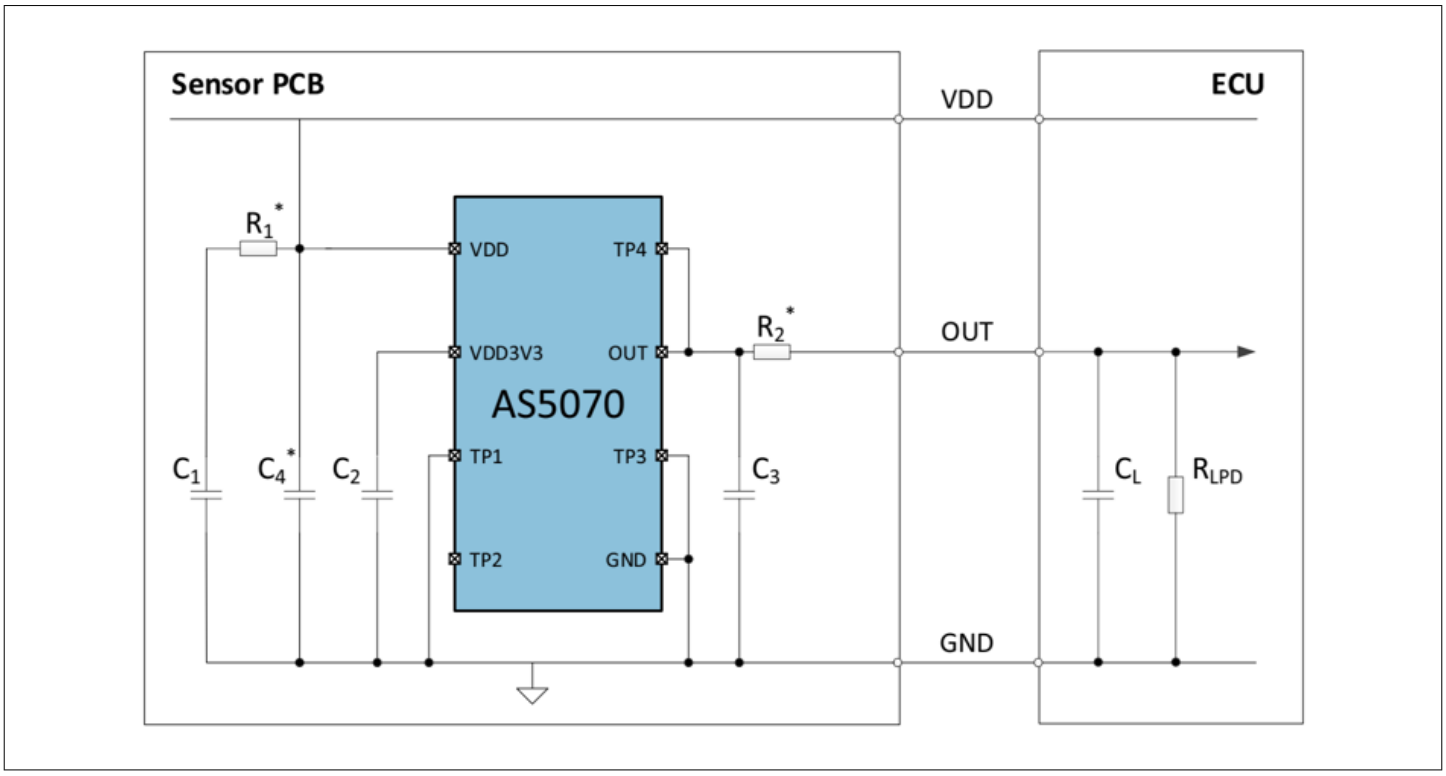


Figure 16 Application with pull-up load resistor (SOIC-8)

Figure 15 and Figure 16 show the recommended schematic in the application. All components marked with (*) are optional and can be used to further increase the EMC.

7.5 External components

Table 28 Recommended external components for AS5070A

Component	Symbol	Min.	Typ.	Max.	Unit	Notes
VDD buffer capacitor	C_1	80	100	120	nF	
VDD3V3 regulator capacitor	C_2	80	100	120	nF	
OUT load capacitor (sensor PCB)	C_3	0		4.7	nF	Do not increase due to programming over output.
VDD capacitor (optional)	C_4^*		4.7		nF	
VDD serial resistor (optional)	R_1^*		10		Ω	
OUT load capacitor (ECU)	C_L	0		20	nF	
OUT serial resistor (optional)	R_2^*		50		Ω	
OUT pull-up resistance	R_{LPU}	4		10	kΩ	
OUT pull-down resistance	R_{LPD}	4		10	kΩ	

Table 29 Recommended external components for AS5070B with PWM output

Component	Symbol	Min.	Typ.	Max.	Unit	Notes
VDD buffer capacitor	C_1	80	100	120	nF	
VDD3V3 regulator capacitor	C_2	80	100	120	nF	
OUT load capacitor (sensor PCB)	C_3	0		4.7	nF	Do not increase due to programming over output.
VDD capacitor (optional)	C_4^*		4.7		nF	
VDD serial resistor (optional)	R_1^*		10		Ω	
OUT load capacitor (ECU)	C_L	0		20	nF	
OUT serial resistor (optional)	R_2^*		50		Ω	
OUT pull-up resistance	R_{LPU}	1		10	kΩ	
OUT pull-down resistance	R_{LPD}	1		10	kΩ	

Table 30 Recommended external components for the AS5070B with SENT output

Component	Symbol	Min.	Typ.	Max.	Unit	Notes
VDD buffer capacitor	C_1	0.8	1	1.2	µF	

(table continues...)

Table 30 (continued) Recommended external components for the AS5070B with SENT output

Component	Symbol	Min.	Typ.	Max.	Unit	Notes
VDD3V3 regulator capacitor	C_2	80	100	120	nF	
OUT load capacitor (sensor PCB)	C_3	0		4.7	nF	Do not increase due to programming over output.
VDD capacitor (optional)	C_4^*		4.7		nF	
VDD serial resistor (optional)	R_1^*		10		kΩ	
OUT load capacitor (ECU)	C_L	0		20	nF	
OUT serial resistor (optional)	R_2^*		50		kΩ	
OUT pull-up resistance	R_{LPU}	10		50	kΩ	
OUT pull-down resistance	R_{LPD}	10		50	kΩ	

7.6 Mechanical data

The internal Hall elements are placed in the center of the package on a circle with a radius of 1.25 mm.

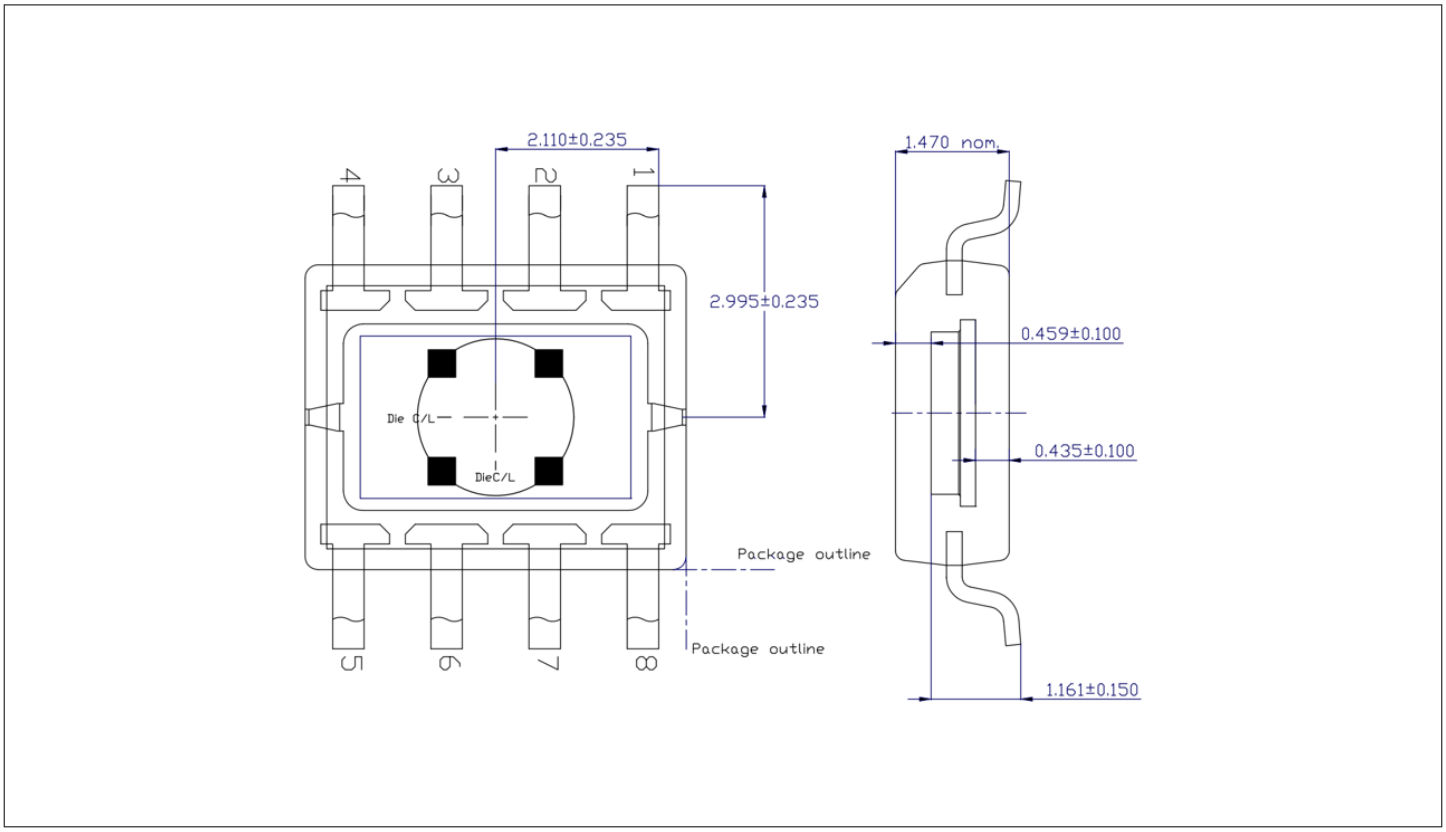
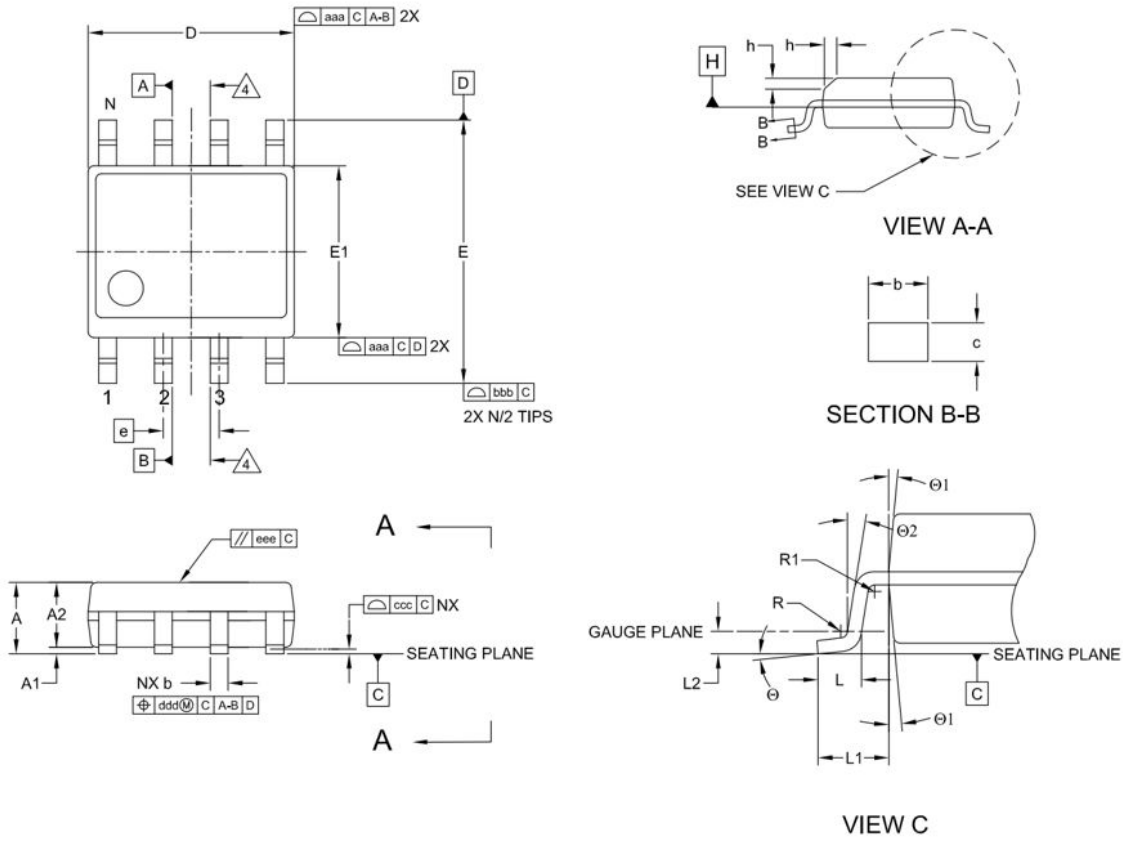


Figure 17 Hall element positions

***Notes**:*

1. *All dimensions in mm*
2. *Die thickness 356 µm nom*
3. *Adhesive thickness 20 ± 10 µm*
4. *Lead frame downest 200 ± 25 µm*
5. *Lead frame thickness 200 ± 8 µm*

8 Package drawings & markings



REF.	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	-	0.25
A2	1.25	-	-
b	0.31	-	0.51
c	0.17	-	0.25
D	-	4.90 BSC	-
E	-	6.00 BSC	-
E1	-	3.90 BSC	-
e	-	1.27 BSC	-
L	0.40	-	1.27
L1	-	1.04 REF	-
L2	-	0.25 BSC	-
R	0.07	-	-
R1	0.07	-	-
h	0.25	-	0.50
Θ	0°	-	8°
Θ1	5°	-	15°
Θ2	0°	-	-
aaa	-	0.10	-
bbb	-	0.20	-
ccc	-	0.10	-
ddd	-	0.25	-
eee	-	0.10	-
fff	-	0.15	-
ggg	-	0.15	-
N		8	

NOTE:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DATUMS A & B TO BE DETERMINED AT DATUM H.

Figure 18 Package outline drawing (SOIC-8)

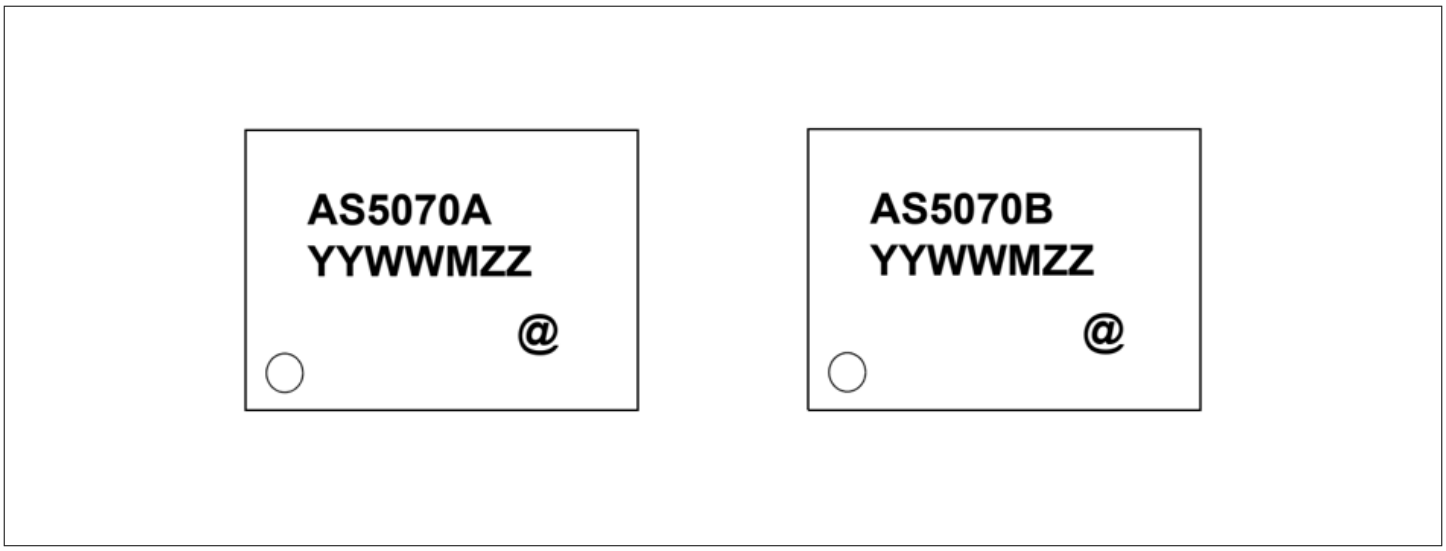


Figure 19 Package markings AS5070 - SOIC8

Table 31 Packaging code YYWWMZZ@

YY	WW	M	ZZ	@
Last two digits of the manufacturing year	Manufacturing week	Plant identifier	Free choice/ traceability code	Sublot identifier

9 Ordering information

Table 32 Ordering information

Product type (Infineon)	Product type (ams OSRAM)	Package	Marking	Delivery form	Delivery quantity
AS5070A-HSOT-SOIC8	AS5070A-HSOT	SOIC8	AS5070A	13" Tape & Reel in dry pack	2500 pcs/reel
AS5070A-HSOM-SOIC8	AS5070A-HSOM	SOIC8	AS5070A	7" Tape & Reel in dry pack	500 pcs/reel
AS5070B-HSOT-SOIC8	AS5070B-HSOT	SOIC8	AS5070B	13" Tape & Reel in dry pack	2500 pcs/reel
AS5070B-HSOM-SOIC8	AS5070B-HSOM	SOIC8	AS5070B	7" Tape & Reel in dry pack	500 pcs/reel

Revision history

Document revision	Date	Description of changes
1.00	2026-10-26	Document rebranded from ams OSRAM to Infineon; technical specifications remain unchanged; added Infineon part numbers in Ordering information table. **Legacy ams changes from 0-01 (2020-Aug-11) to current revision 1-00 (2020-Aug-13)** • Updated note 1 under Figure 48

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