Cypress FM4 Graphics Engine Enabled ARM®Cortex®-M4 Microcontrollers



The S6E2D series is the newest addition to the Cypress FM4 family of microcontrollers. This new ARM® Cortex®- M4 based MCU series incorporates a dedicated hardware graphics engine that enables rich display images with a cost-effective single-chip solution. Using this single-chip solution from Cypress brings sophisticated graphics while significantly reducing dependency on the costly

multi-chip solutions available from other companies.

The graphics engine and 512KB of video RAM allow complex image overlap, mirroring, scaling and image movement with very little CPU overhead. The Cypress solution comes complete with graphics authoring tools and low level libraries for the graphics engine.

The S6E2D series is ideal for embedded applications with TFT displays such as home appliances, multi-function printers, industrial equipment, electronic musical instruments and security systems.

Features

- ARM® Cortex®- M4F CPU Core
- Frequency: up to 160MHz
- Flash/SRAM: 384KB/36KB
- Graphics display controller subsystem:
- 2 dimensional accelerator Blit engine
- Digital RGB interface supporting up to 800×600 (SVGA)
- Internal VRAM: 512KB
- 3separate external bus interfaces: SDRAM, HyperFlash™ and Q-SPI flash
- Optional 2MB VFlash for image storage

- Communication interfaces:
- MFS (UART/SPI/I2C/LIN)8ch
- USB (Host/Device)1ch
- CAN-FD1ch
- SDCARD Interface
- I2S 2ch
- Package Options: LQFP-120/ 176, BGA161



• Memory size: 384KB

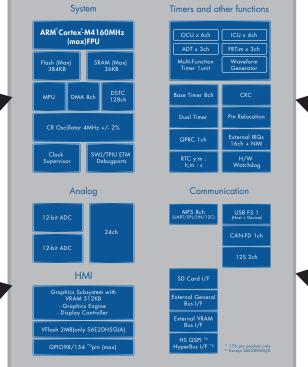
• SRAM size: 36KB

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Embedded graphics engine

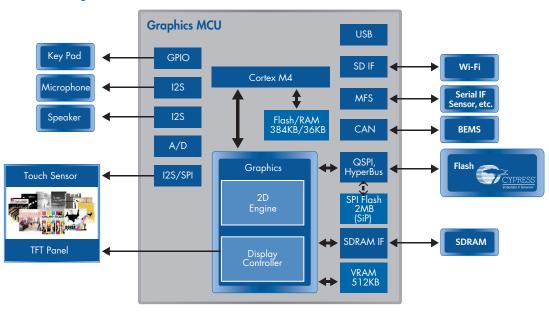
- Display controller w/ panel resolution up to SVGA
- 2D accelerator Blit engine
- Command sequencer
- Internal 512KB VRAM
- Independent external bus interfaces: SDRAM, HyperBus™ & Q-SPI

External SDRAM (via External VRAM Interface)



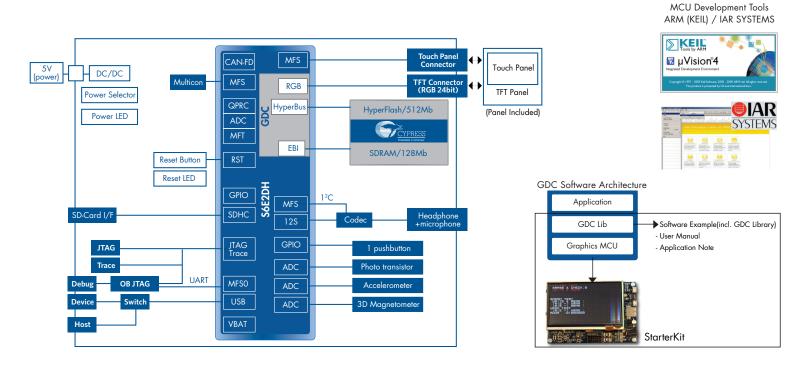
- Advanced timer peripherals
- Multi-function timer
- Base timer
- Programmable CRC
- QPRC
- Rich communication interface
- 8ch MFS (UART/SPI/I2C)
- USB FS (Host/Device)
- I²S Interface 2ch
- CAN-FD
- External general bus interface (flash SRAM SDRAM)

Target application / System block diagram



Development environment / Evaluation board

Graphics Software Development environment



Note: This document may be revised by subsequent versions or modifications due to changes in technical specifications.

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